MEMORY PRODUCTS

DATA BOOK

Spring 1996

DYNAMIC *RAMs*

NEC

Dynamic RAM

Spring 1996 Data Book

Document No. M10547EJ4V0DBU1

Printed in the United States of America.

Index

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

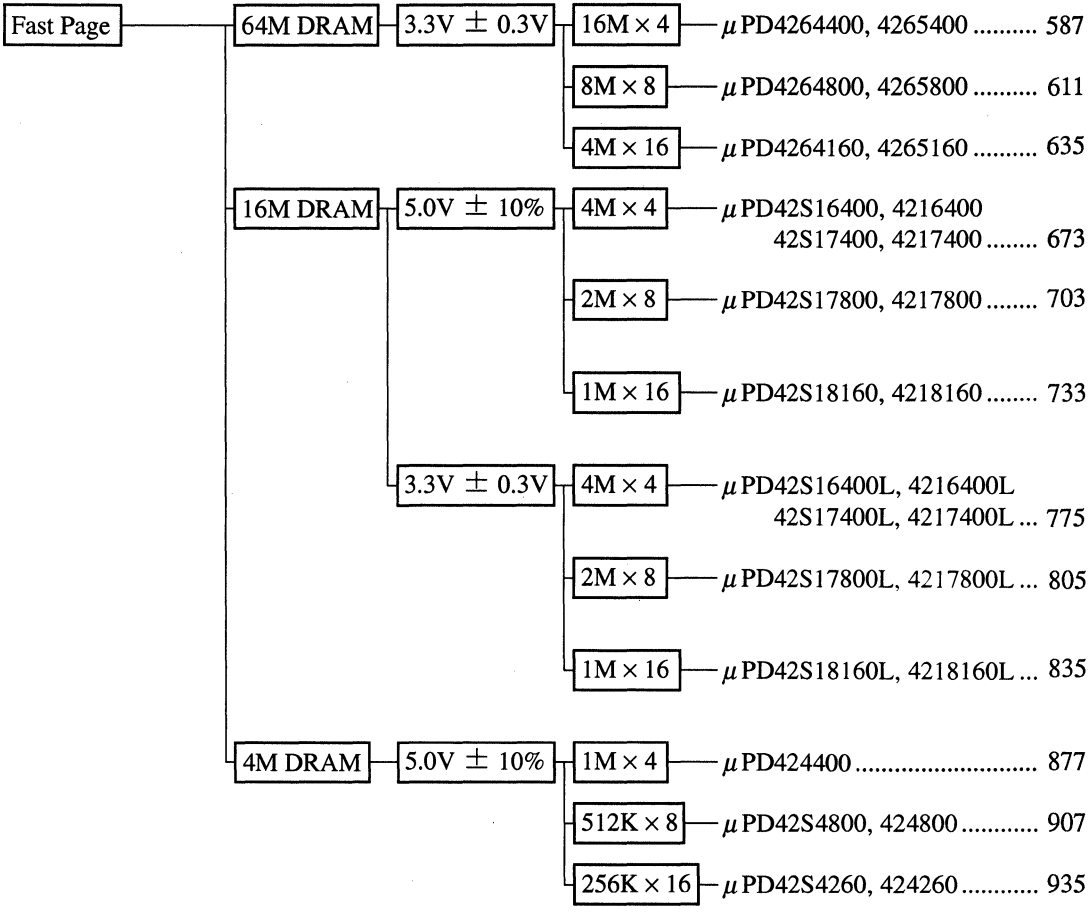
② HANDLING OF UNUSED INPUT PINS FOR CMOS

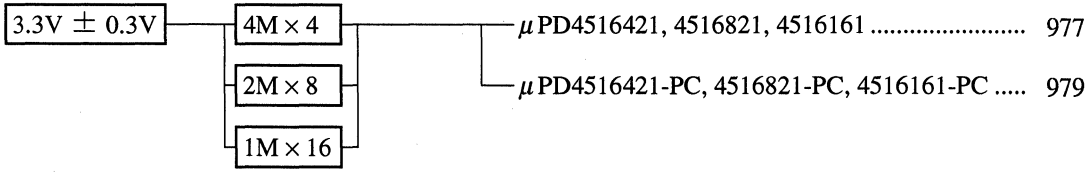
Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Contents

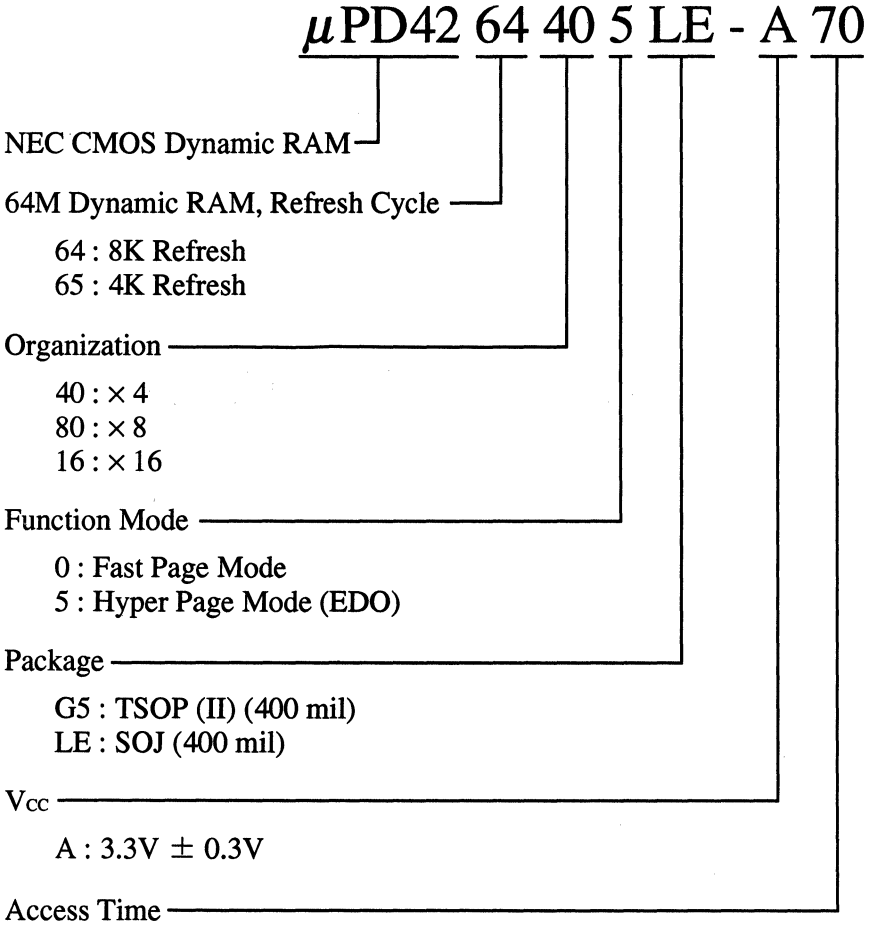




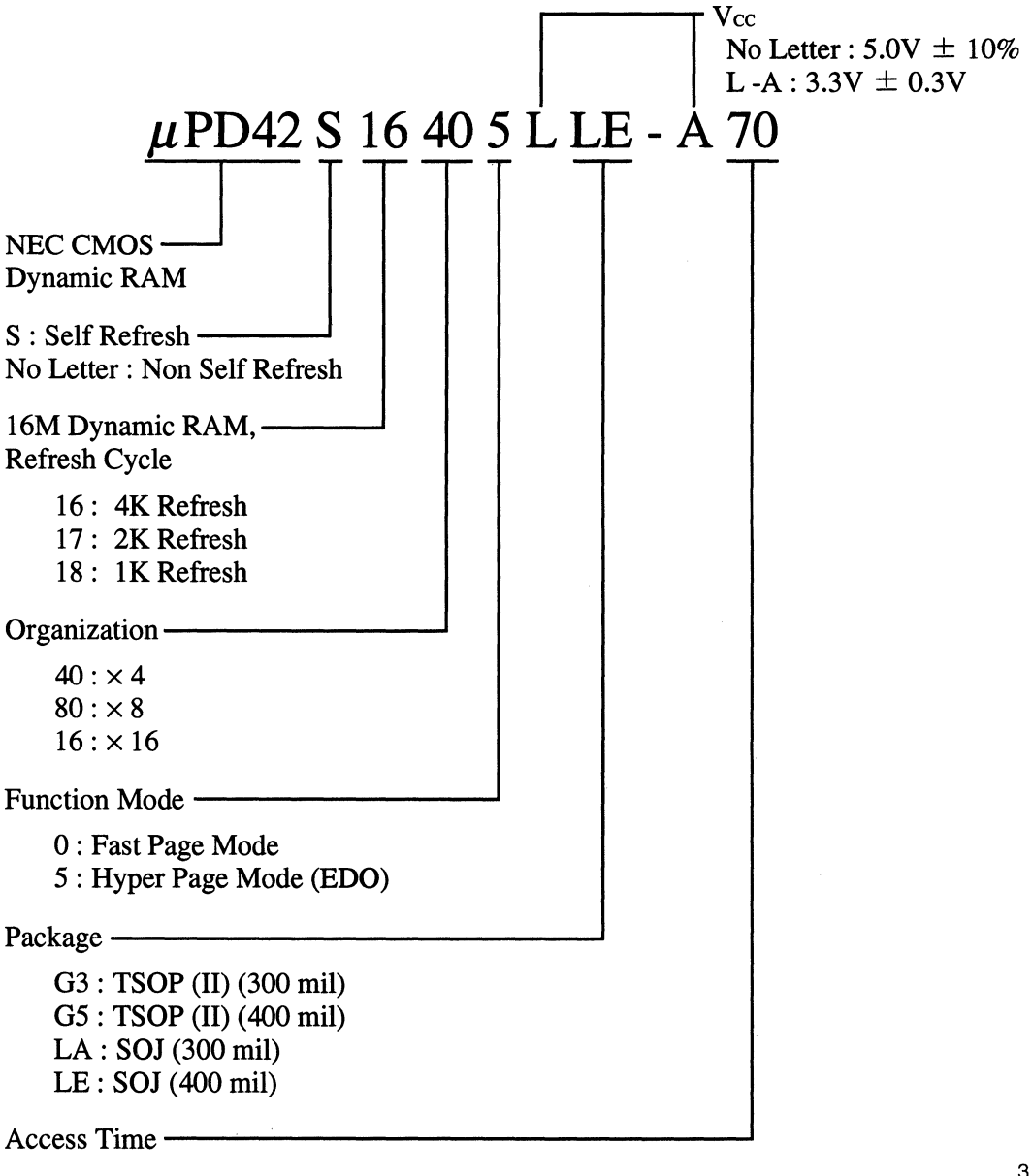
Selection Guide

Part Number

64M DRAM

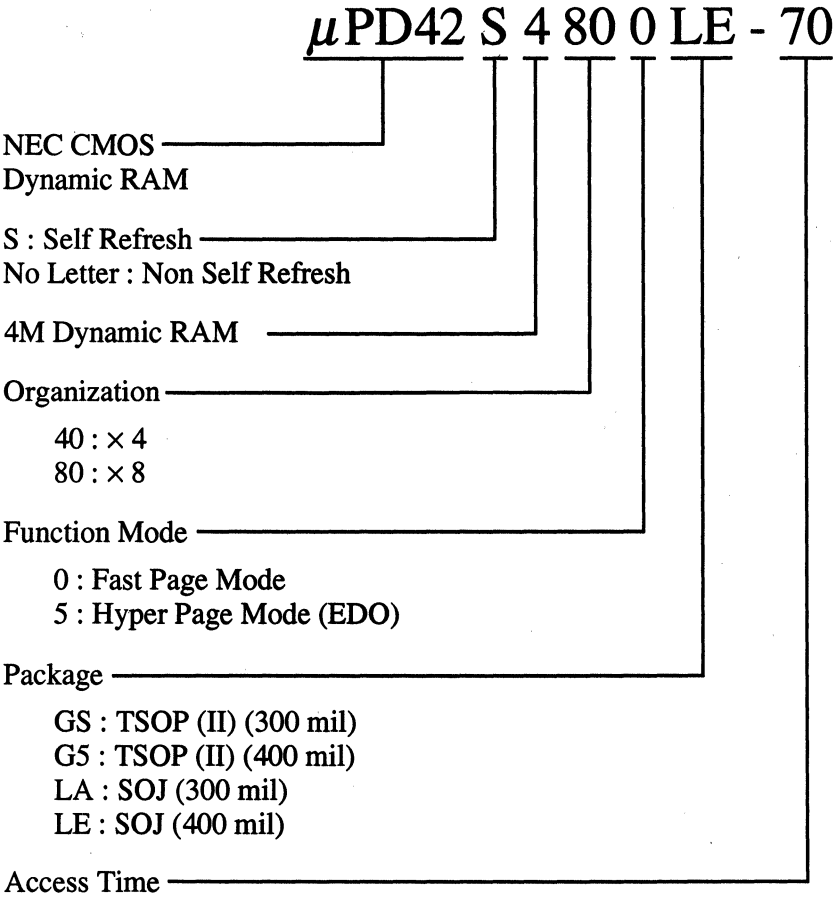


16M DRAM

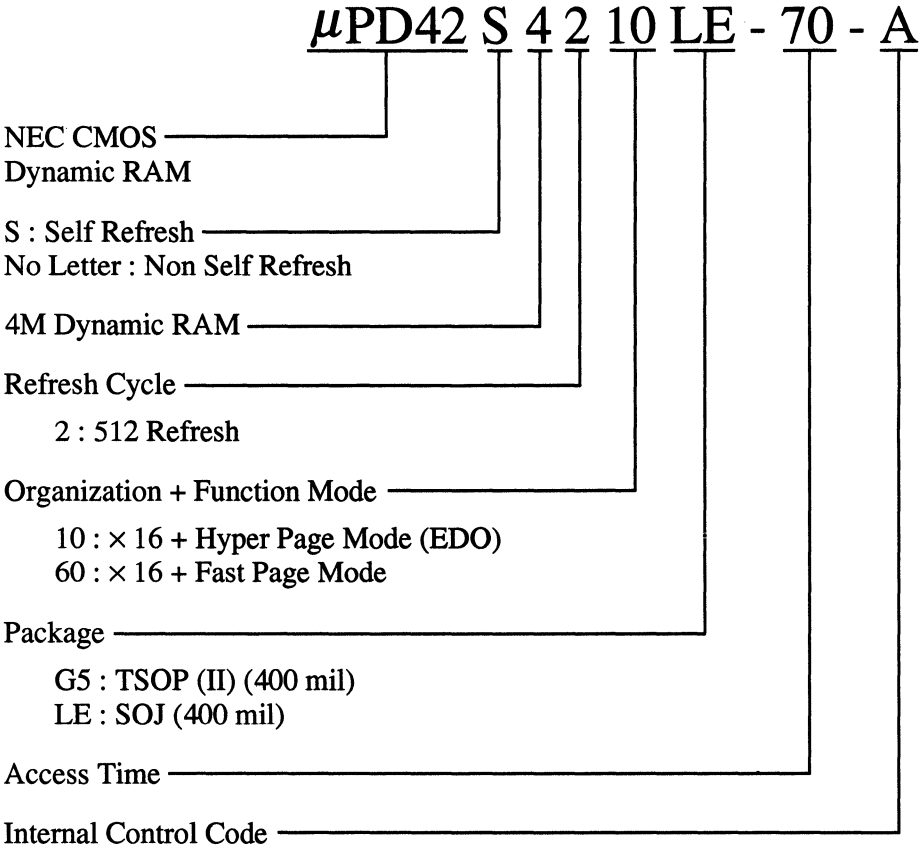

Vcc
No Letter : 5.0V ± 10%
L -A : 3.3V ± 0.3V
μPD42 S 16 40 5 L LE - A 70
NEC CMOS
Dynamic RAM
S : Self Refresh
No Letter : Non Self Refresh
16M Dynamic RAM,
Refresh Cycle
16 : 4K Refresh
17 : 2K Refresh
18 : 1K Refresh
Organization
40 : × 4
80 : × 8
16 : × 16
Function Mode
0 : Fast Page Mode
5 : Hyper Page Mode (EDO)
Package
G3 : TSOP (II) (300 mil)
G5 : TSOP (II) (400 mil)
LA : SOJ (300 mil)
LE : SOJ (400 mil)
Access Time

4M DRAM

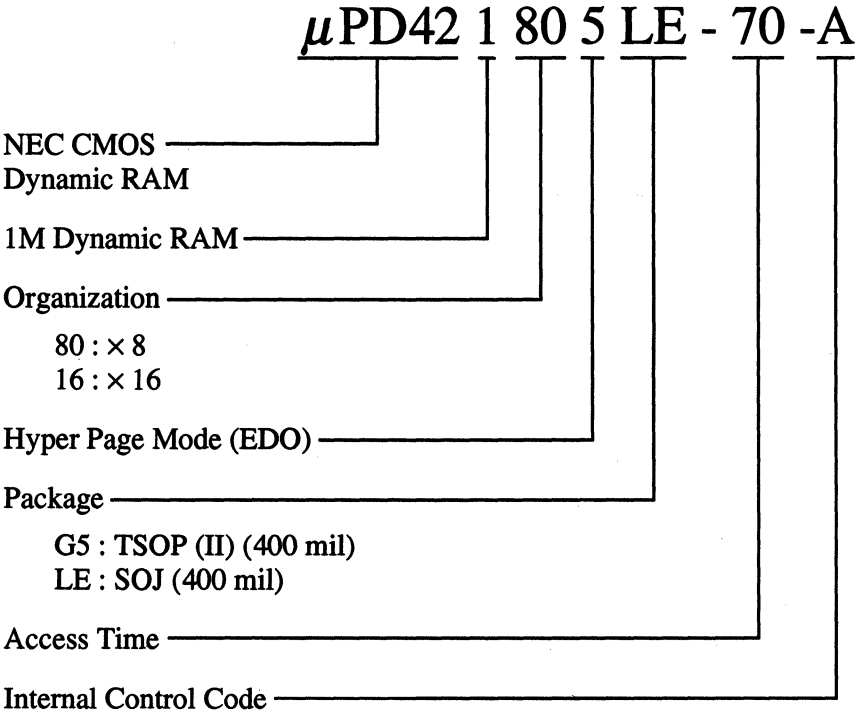
(1) × 4 / × 8


μPD42 S 4 80 0 LE - 70
NEC CMOS
Dynamic RAM
S : Self Refresh
No Letter : Non Self Refresh
4M Dynamic RAM
Organization
40 : × 4
80 : × 8
Function Mode
0 : Fast Page Mode
5 : Hyper Page Mode (EDO)
Package
GS : TSOP (II) (300 mil)
G5 : TSOP (II) (400 mil)
LA : SOJ (300 mil)
LE : SOJ (400 mil)
Access Time

(2) × 16

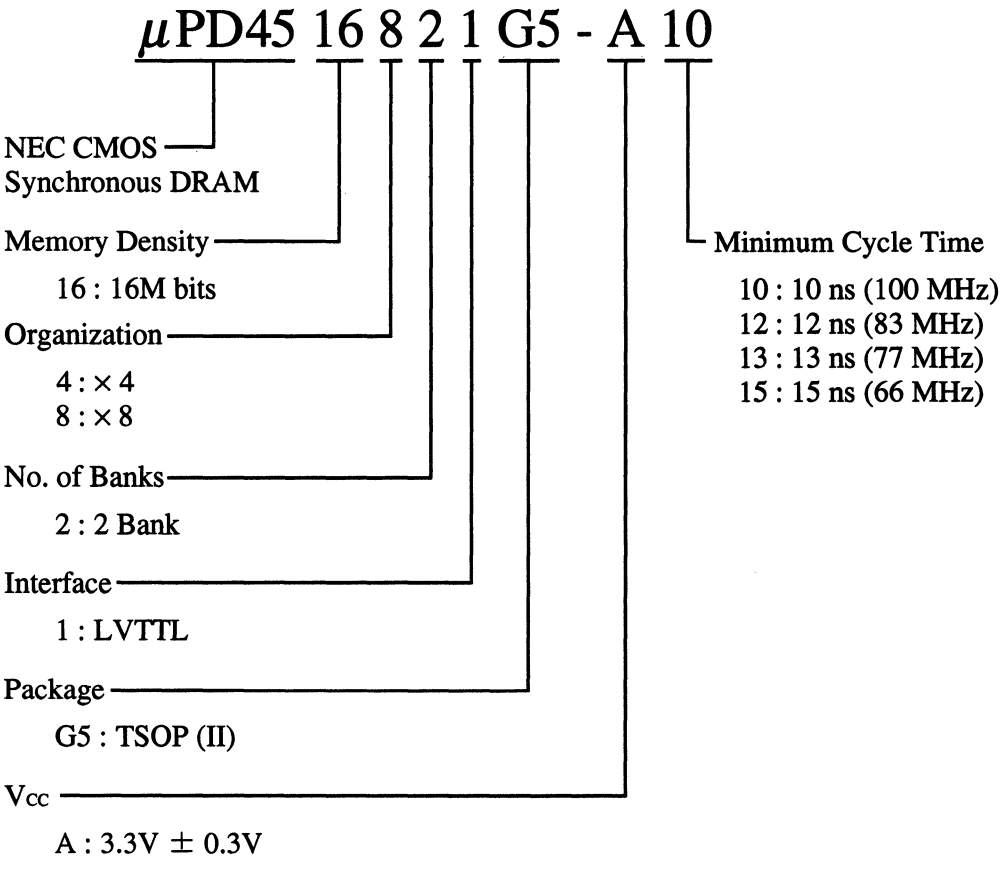

μPD42 S 4 2 10 LE - 70 - A
NEC CMOS
Dynamic RAM
S : Self Refresh
No Letter : Non Self Refresh
4M Dynamic RAM
Refresh Cycle
2 : 512 Refresh
Organization + Function Mode
10 : × 16 + Hyper Page Mode (EDO)
60 : × 16 + Fast Page Mode
Package
G5 : TSOP (II) (400 mil)
LE : SOJ (400 mil)
Access Time
Internal Control Code

1M DRAM

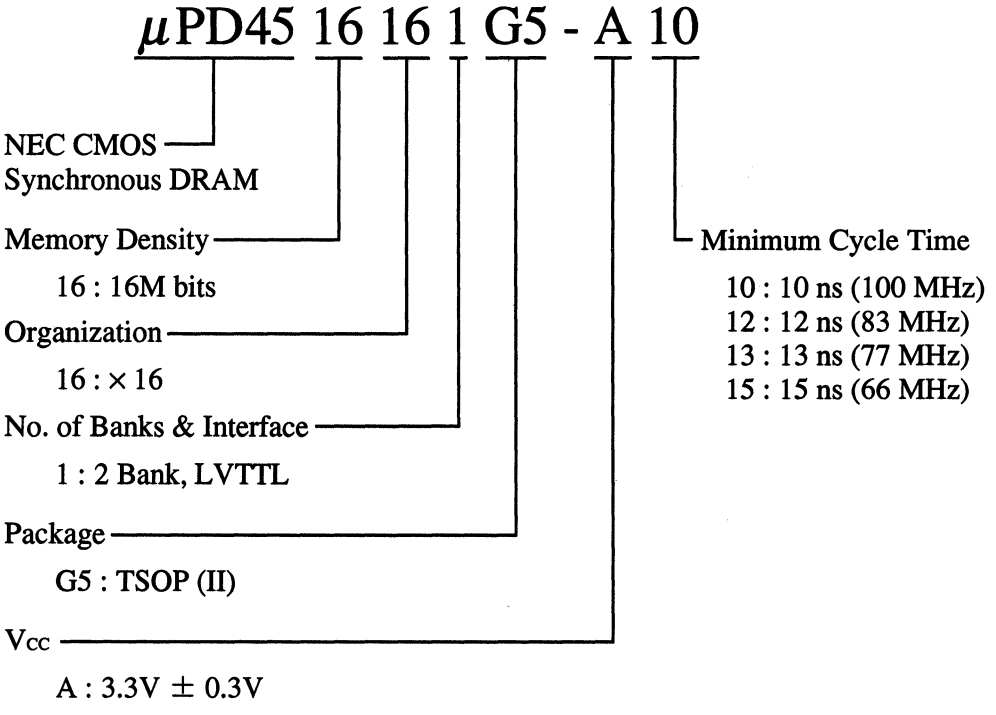

μPD42 1 80 5 LE - 70 -A
NEC CMOS Dynamic RAM
1M Dynamic RAM
Organization
80 : × 8
16 : × 16
Hyper Page Mode (EDO)
Package
G5 : TSOP (II) (400 mil)
LE : SOJ (400 mil)
Access Time
Internal Control Code

Synchronous DRAM

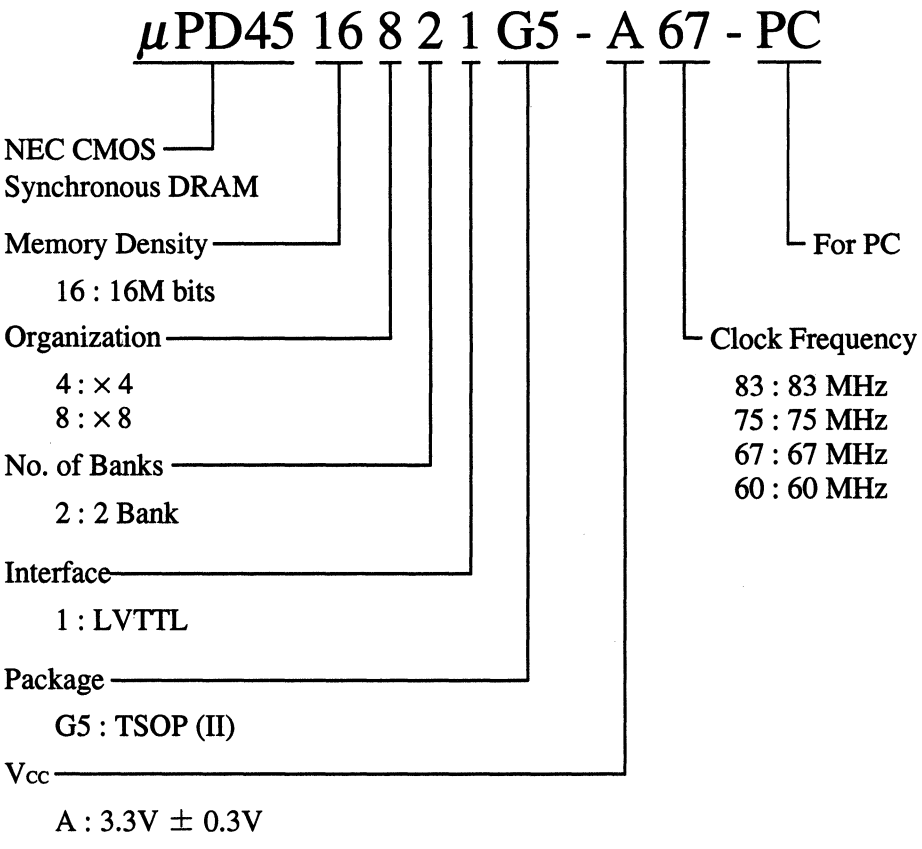
(1) × 4 / × 8



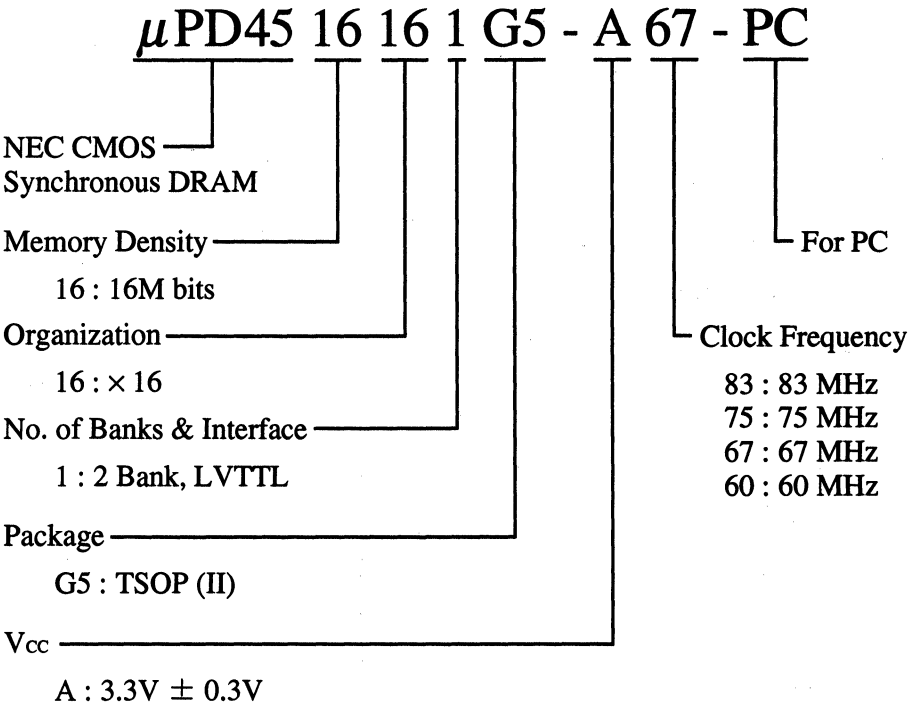
(2) × 16


μPD45 16 16 1 G5 - A 10
NEC CMOS
Synchronous DRAM
Memory Density
16 : 16M bits
Organization
16 : × 16
No. of Banks & Interface
1 : 2 Bank, LVTTL
Package
G5 : TSOP (II)
Vcc
A : 3.3V ± 0.3V
Minimum Cycle Time
10 : 10 ns (100 MHz)
12 : 12 ns (83 MHz)
13 : 13 ns (77 MHz)
15 : 15 ns (66 MHz)

(3) × 4 / × 8 (For PC)


μPD45 16 8 2 1 G5 - A 67 - PC
NEC CMOS
Synchronous DRAM
Memory Density
16 : 16M bits
Organization
4 : × 4
8 : × 8
No. of Banks
2 : 2 Bank
Interface
1 : LVTTL
Package
G5 : TSOP (II)
Vcc
A : 3.3V ± 0.3V
For PC
Clock Frequency
83 : 83 MHz
75 : 75 MHz
67 : 67 MHz
60 : 60 MHz

(4) × 16 (For PC)


μPD45 16 16 1 G5 - A 67 - PC
NEC CMOS
Synchronous DRAM
Memory Density
16 : 16M bits
Organization
16 : × 16
No. of Banks & Interface
1 : 2 Bank, LVTTL
Package
G5 : TSOP (II)
Vcc
A : 3.3V ± 0.3V
Clock Frequency
83 : 83 MHz
75 : 75 MHz
67 : 67 MHz
60 : 60 MHz
For PC

Hyper Page Mode (EDO)
64M Dynamic RAM

NEC

MOS INTEGRATED CIRCUIT

μPD4264405, 4265405

64 M-BIT DYNAMIC RAM
16 M-WORD BY 4-BIT, HYPER PAGE MODE

Description

The μPD4264405, 4265405 are 16,777,216 words by 4 bits CMOS dynamic RAMs with optional hyper page mode.
Hyper page mode is a kind of page mode and is useful for the read operation.
The μPD4264405, 4265405 are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- Hyper page mode
- Single +3.3 V±0.3V power supply
- 16,777,216 words by 4 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD4264405-A50, 4265405-A50	50 ns	84 ns	20 ns
μPD4264405-A60, 4265405-A60	60 ns	104 ns	25 ns
μPD4264405-A70, 4265405-A70	70 ns	124 ns	30 ns

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

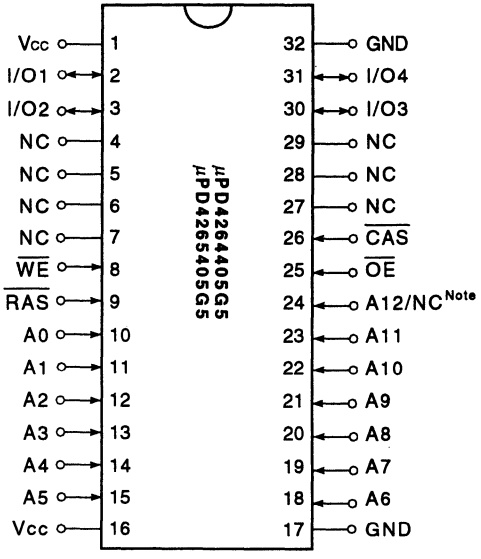
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264405	A0-A12	A0-A10	$\overline{RAS}$ only refresh, Normal Read / Write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265405	A0-A11	A0-A11	$\overline{RAS}$ only refresh, Normal Read / Write	4,096 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	

Ordering Information

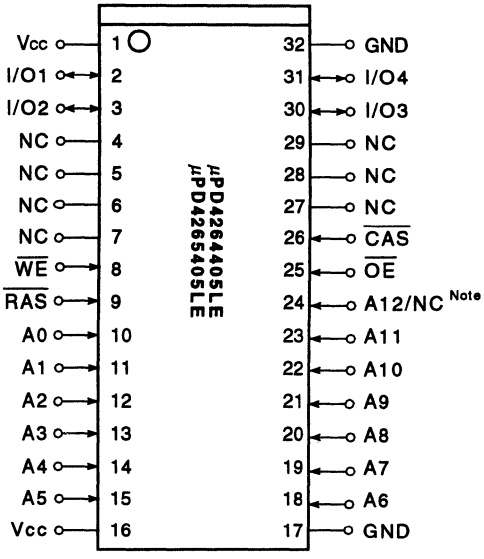
Part number	Access time (MAX.)	Package	Refresh
μPD4264405G5-A50	50 ns	32-pin Plastic TSOP(II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264405G5-A60	60 ns		
μPD4264405G5-A70	70 ns		
μPD4265405G5-A50	50 ns		
μPD4265405G5-A60	60 ns		
μPD4265405G5-A70	70 ns		
μPD4264405LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μPD4264405LE-A60	60 ns		
μPD4264405LE-A70	70 ns		
μPD4265405LE-A50	50 ns		
μPD4265405LE-A60	60 ns		
μPD4265405LE-A70	70 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12...μPD4264405
NC ... μPD4265405

A0 to A12	:	Address Inputs
I/O1 to I/O4	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264405, 4265405 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note 1] and input/output pins I/O1 to I/O4.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to AX[Note 1] (Address inputs)		Address bus. Input total 24-bit of address signal, upper bits and lower bits in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/ Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note1.

Part number	Address inputs	Upper bits	Lower bits
μPD4264405	A0-A12	13	11
μPD4265405	A0-A11	12	12

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is lager than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

Hyper Page Mode

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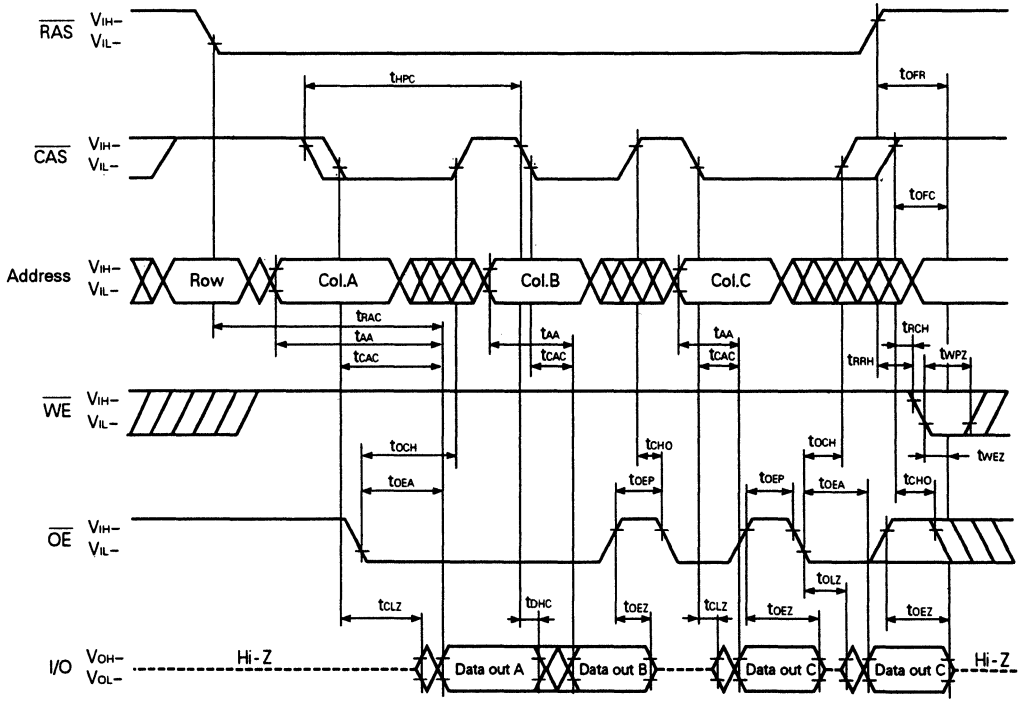
1. **Data output time is extended.**
   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.**
   In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted) [μPD4264405]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		100	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		90		
		I_O = 0 mA	t_{RAC} = 70 ns		80		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH (MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		100	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH (MIN.)}$	t_{RAC} = 60 ns		90		
		t_{RC} = $t_{RC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		80		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL (MAX.)}$	t_{RAC} = 50 ns		100	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		90		
		t_{HPC} = $t_{HPC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1,2
		t_{RC} = $t_{RC (MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
Input leakage current	$I_{I (L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265405]

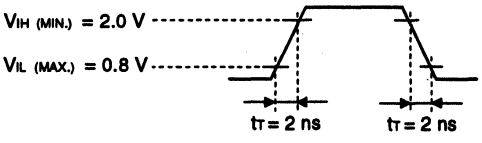
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH(MIN.)}$	t_{RAC} = 60 ns		110		
		t_{RC} = $t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		100		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL(MAX.)}$	t_{RAC} = 50 ns		100	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		90		
		t_{HPC} = $t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1,2
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≦ $V_{IL(MAX.)}$ and $\overline{CAS}$ ≧ $V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

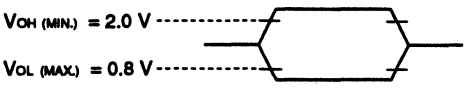
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	84	—	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	30	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	7	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	7	10 000	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	38	—	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	11	37	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	9	25	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	0	—	ns	
Row Address Hold Time	tRAH	7	—	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	0	—	ns	
Column Address Hold Time	tCAH	7	—	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	10	—	13	—	15	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	1	50	ns	
Refresh Time	tREF	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	—	10	—	12	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7	—	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	7	—	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	107	—	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64	—	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27	—	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39	—	47	—	54	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20	—	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	—	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	30	—	35	—	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41	—	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	52	—	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	7	—	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3.4

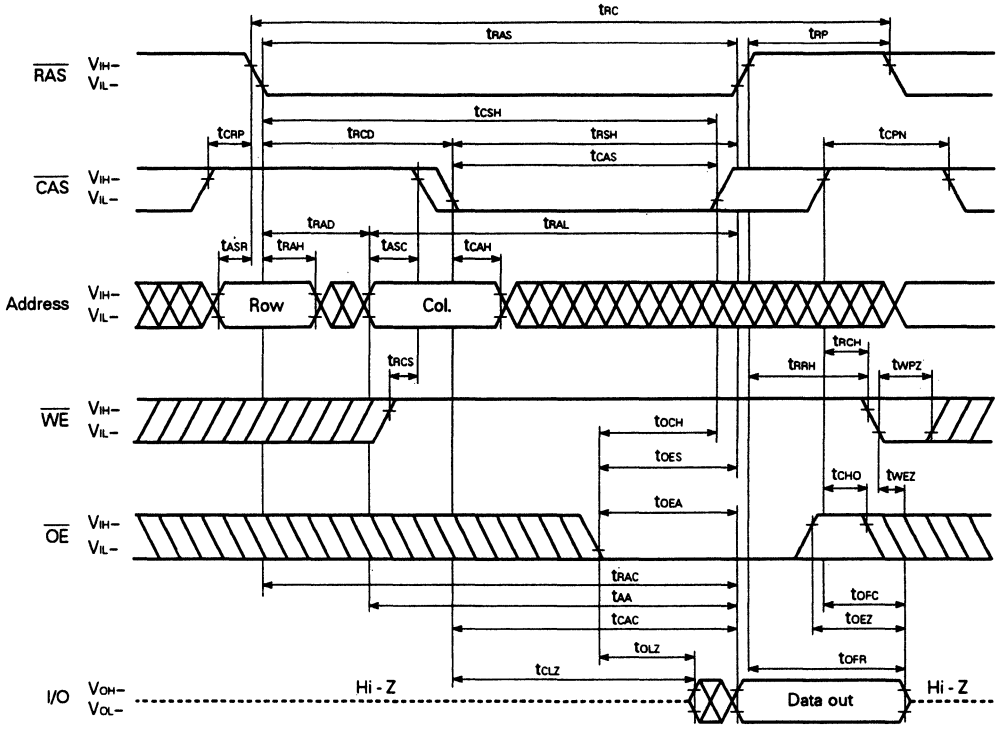
Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.
   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

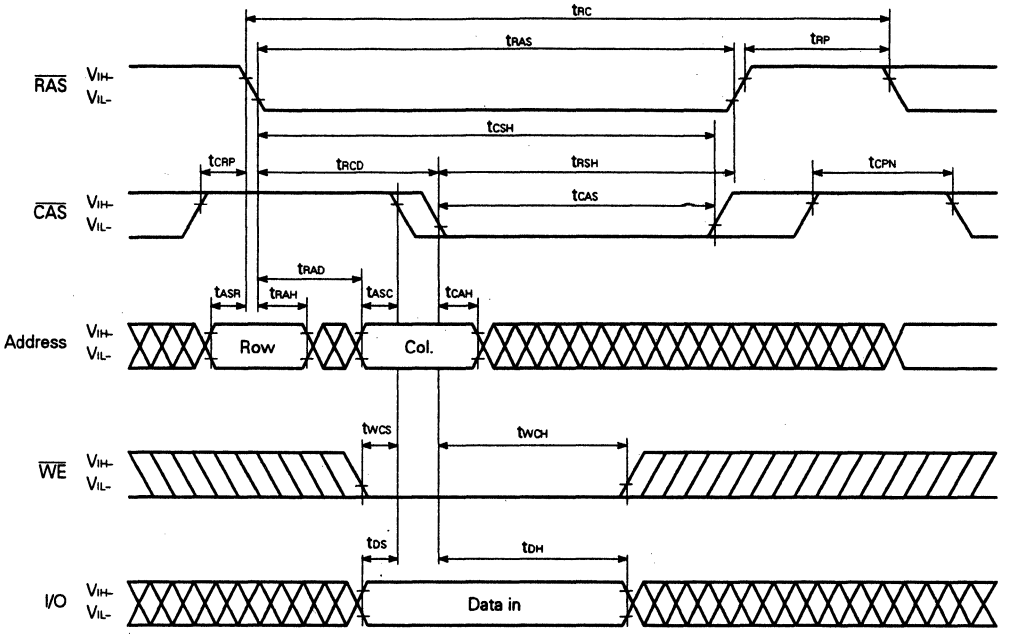
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	—	15	—	15	—	ns	

Read Cycle

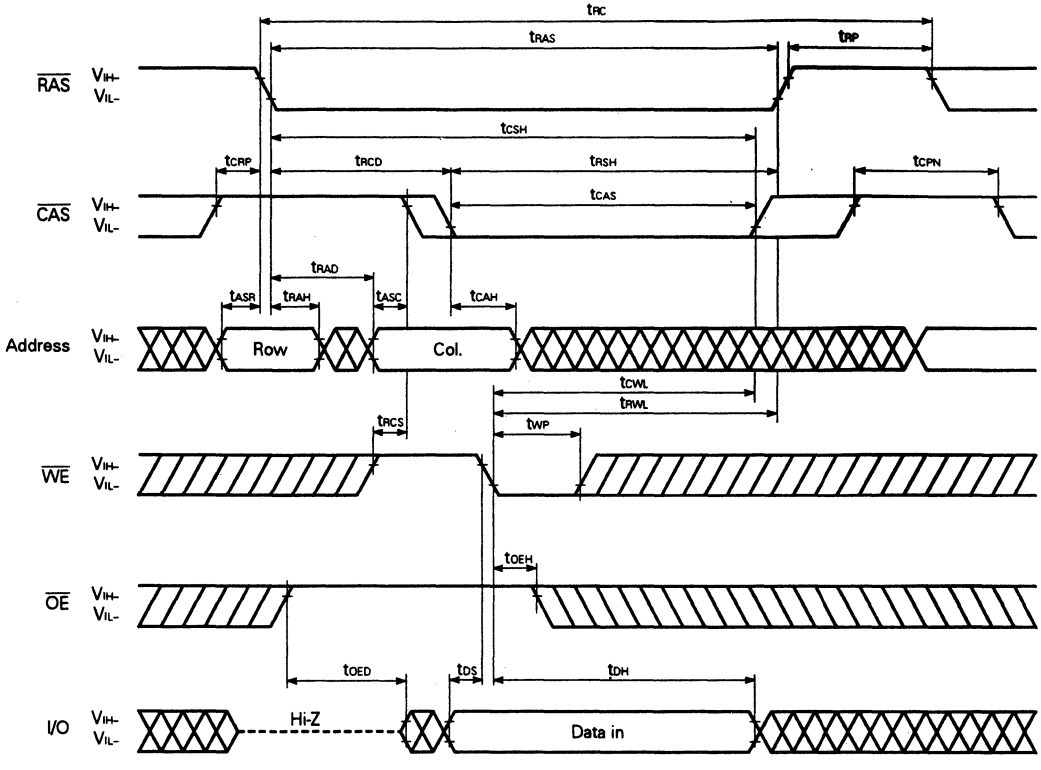

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS VIH– VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCS
tRCH
tRAH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
tOEA
OE VIH– VIL–
tRAC
tAA
tOFC
tOEZ
tCAC
tOLZ
tOFR
tCLZ
I/O VOH– VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

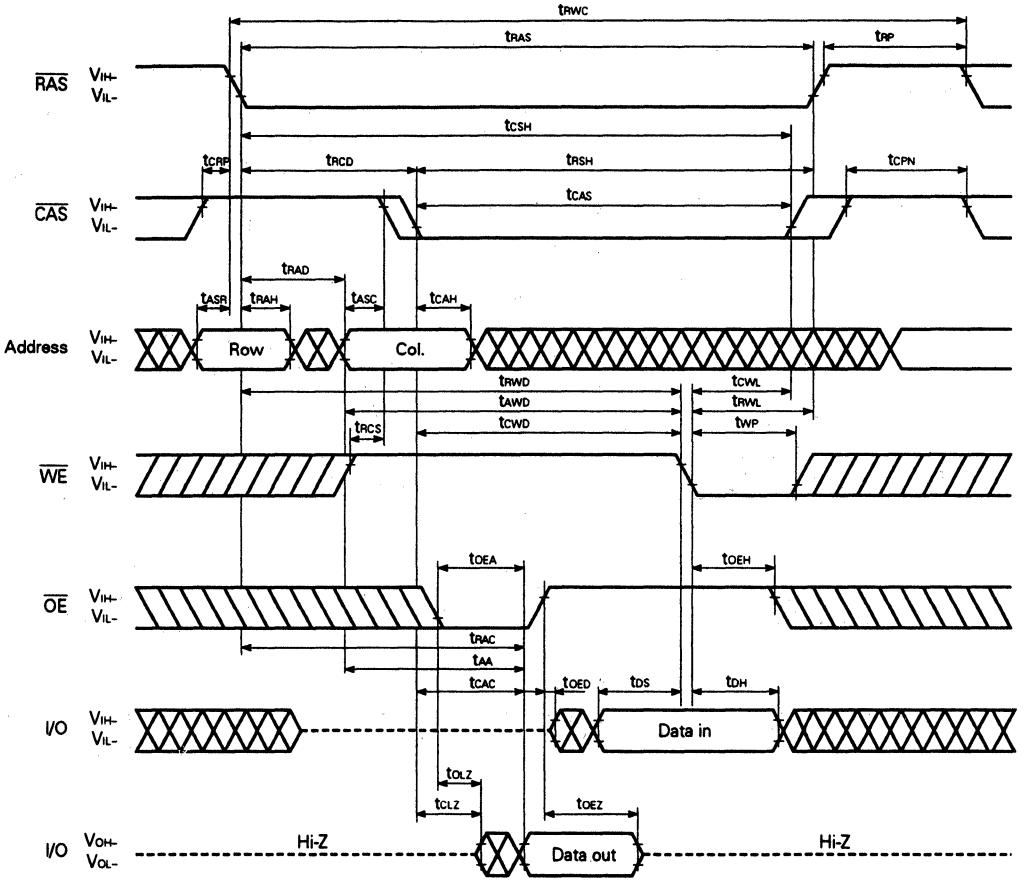


Remark $\overline{OE}$: Don't care

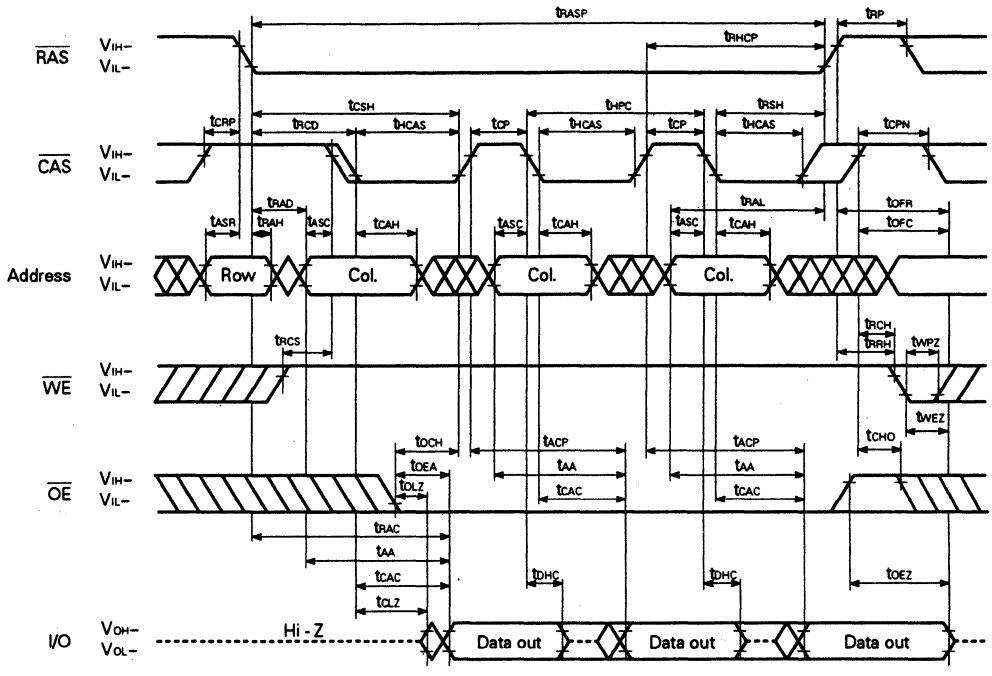
Late Write Cycle



Read Modify Write Cycle

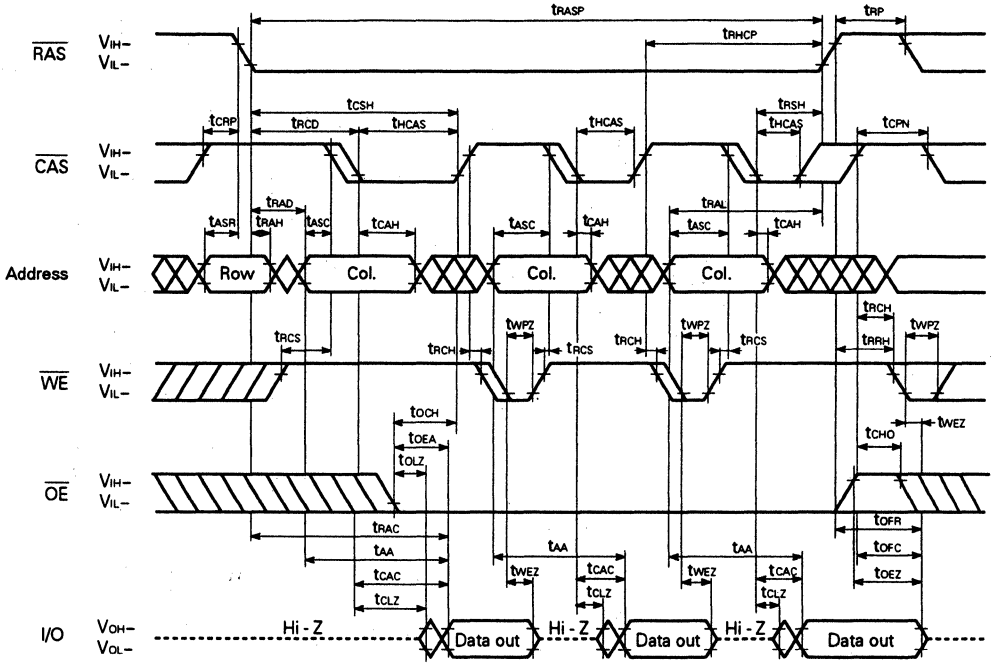


Hyper Page Mode Read Cycle



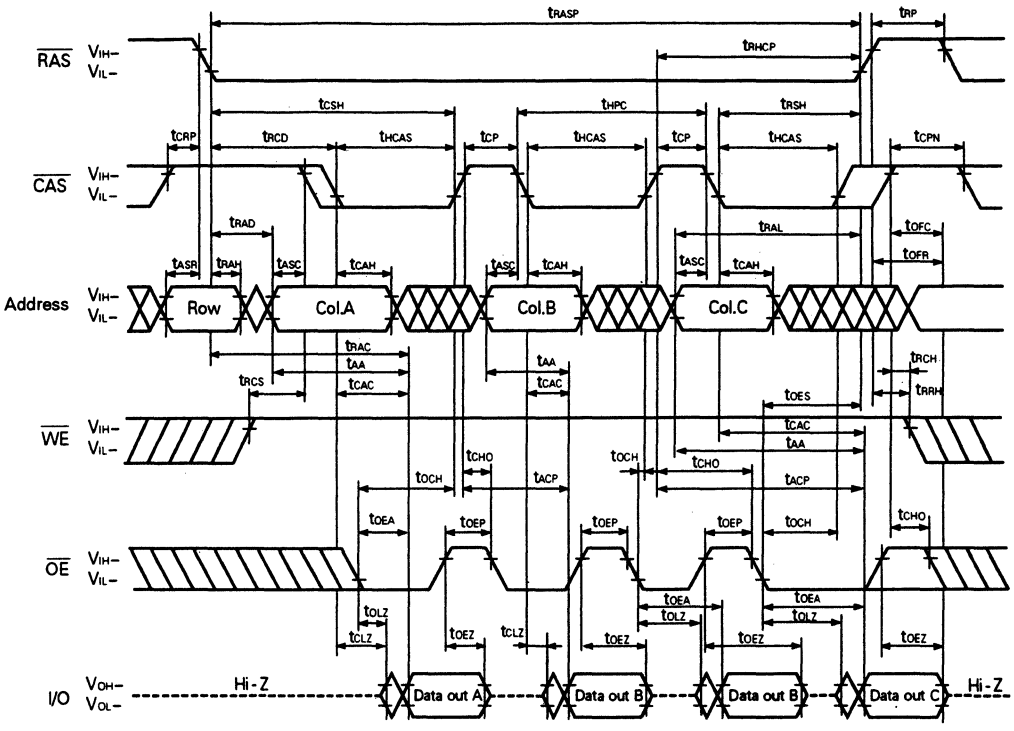
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



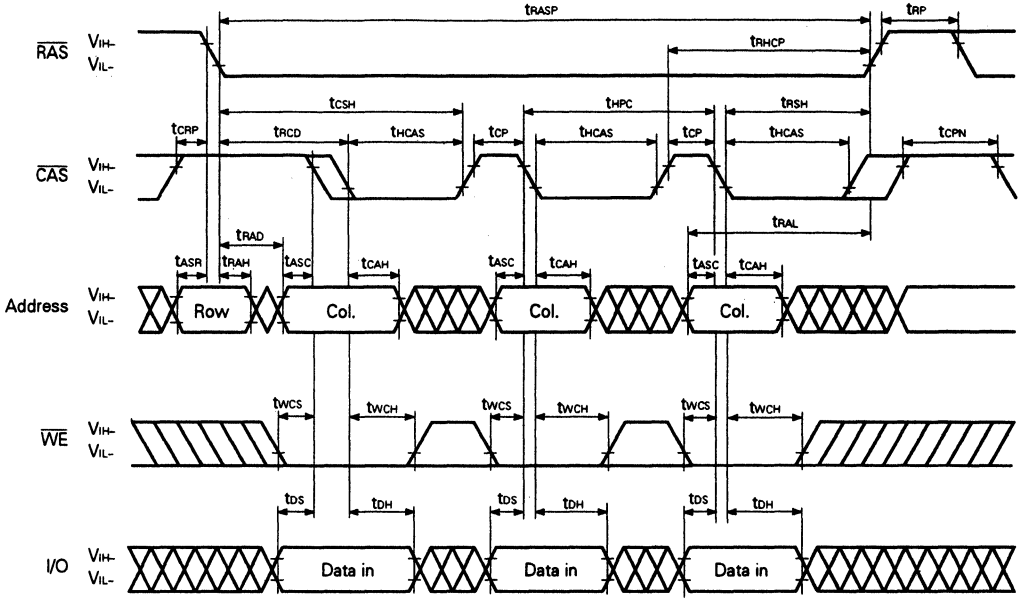
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

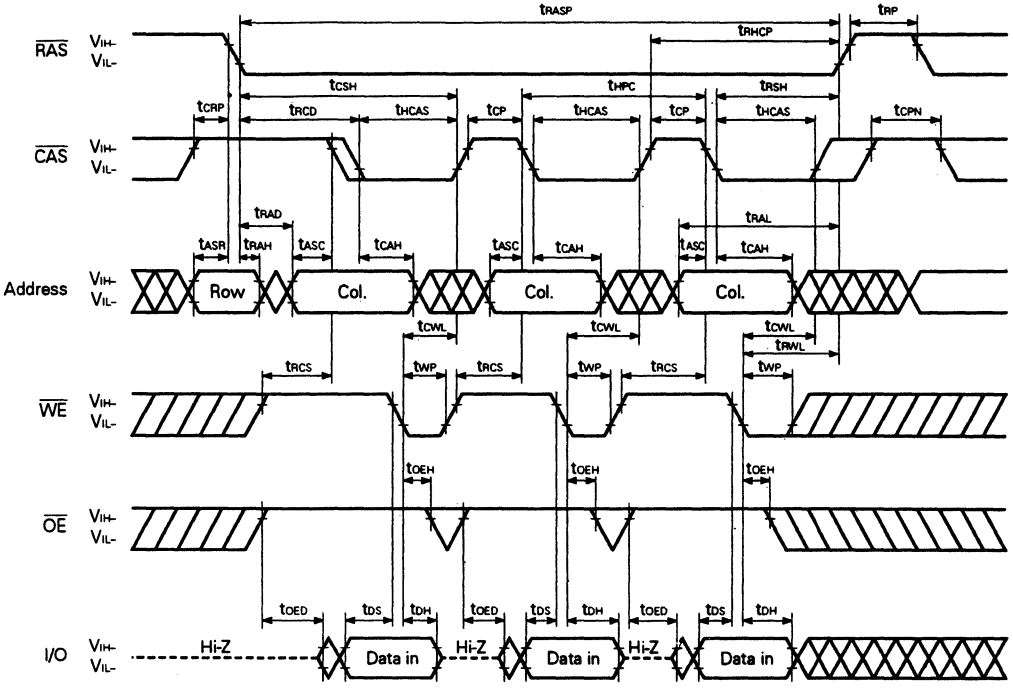
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

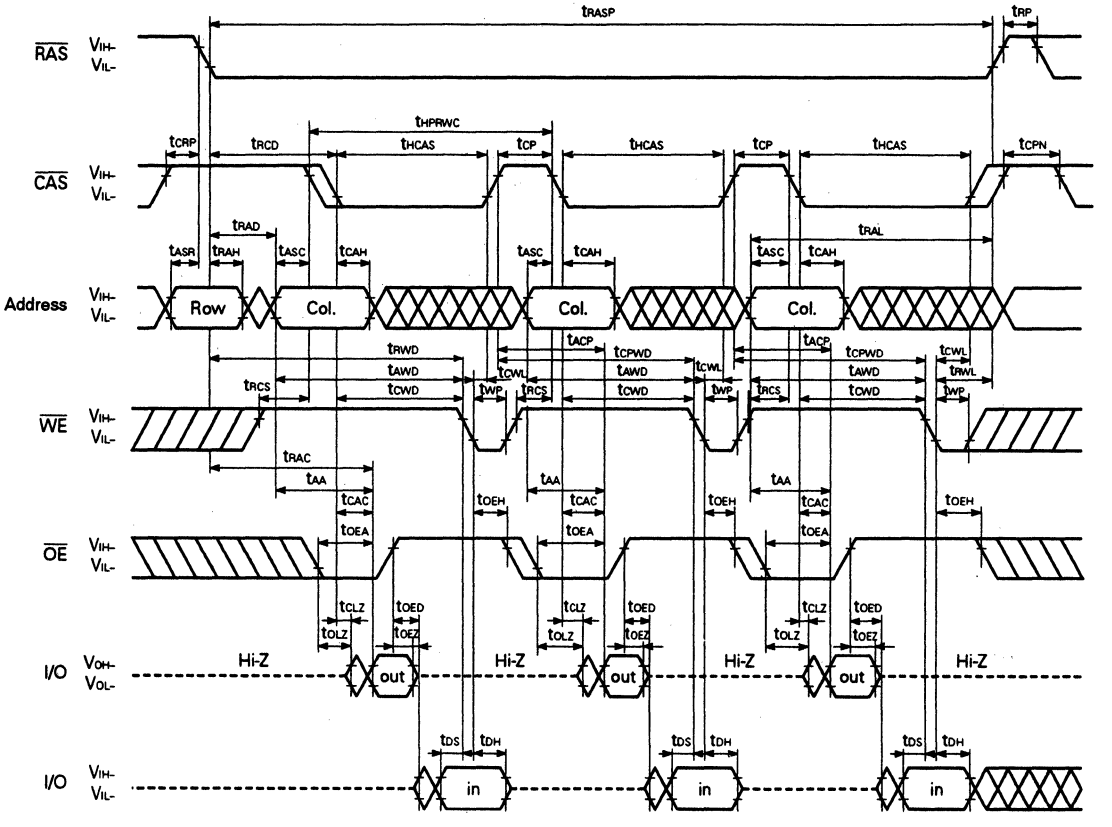
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



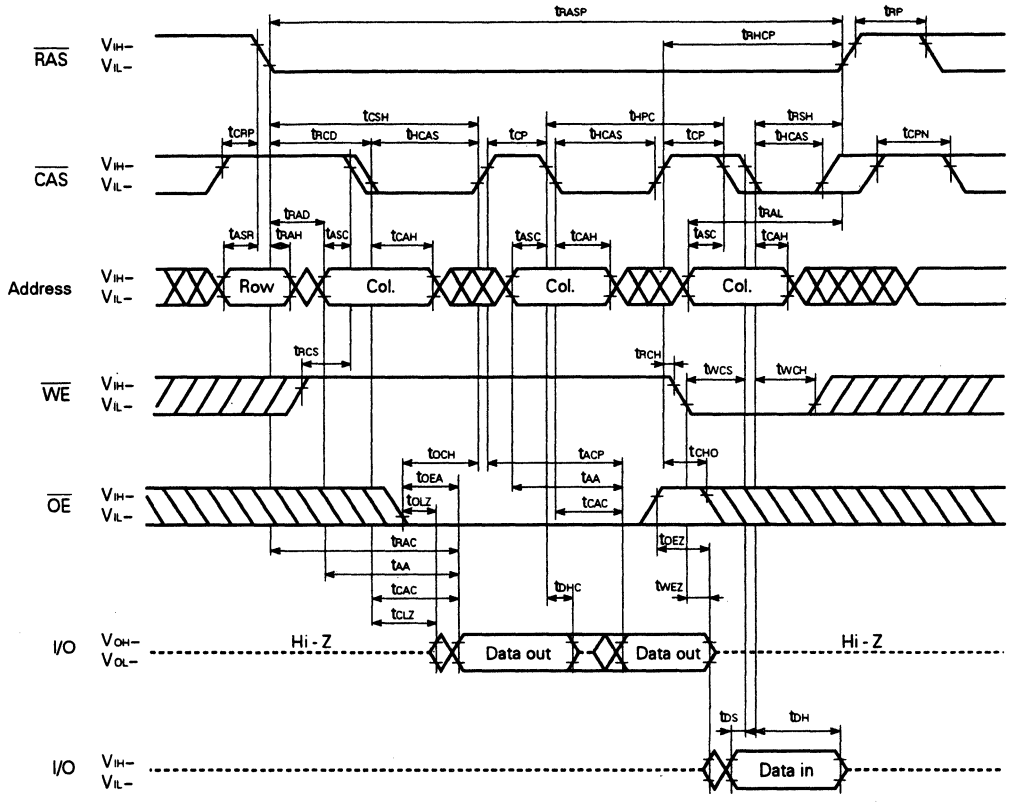
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



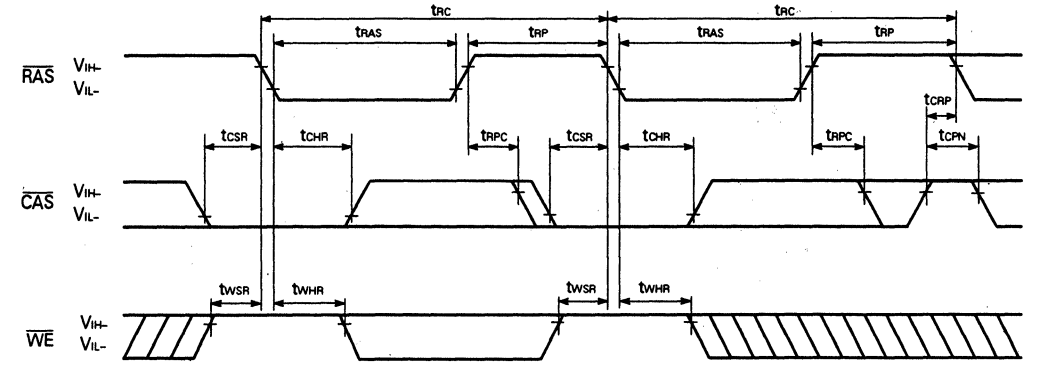
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



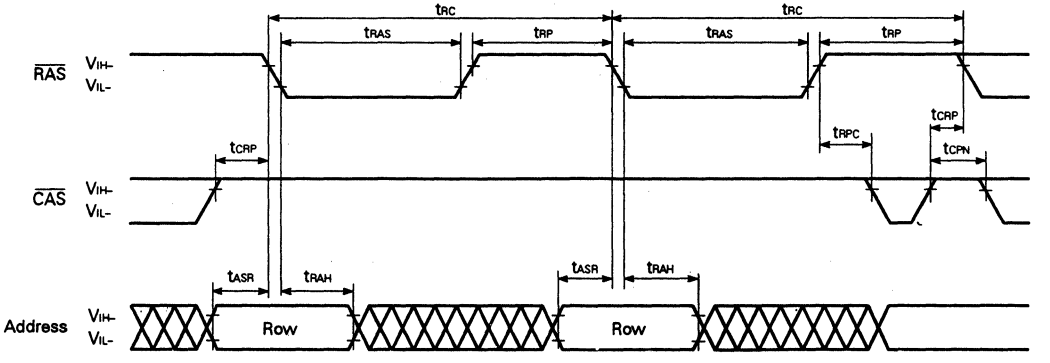
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



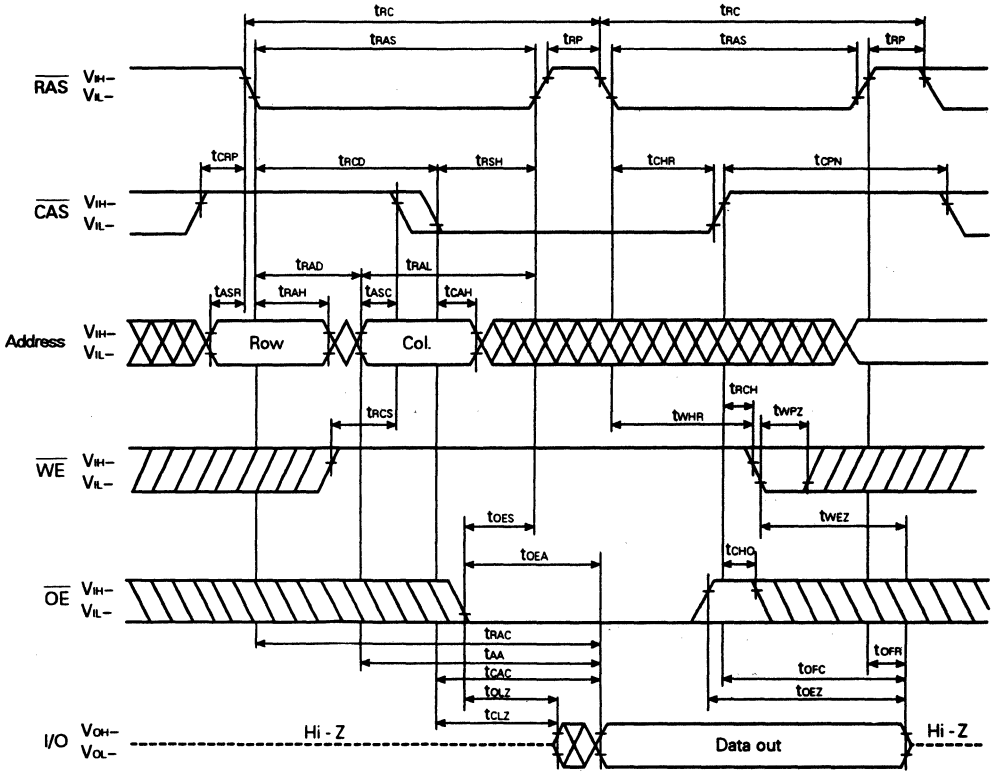
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

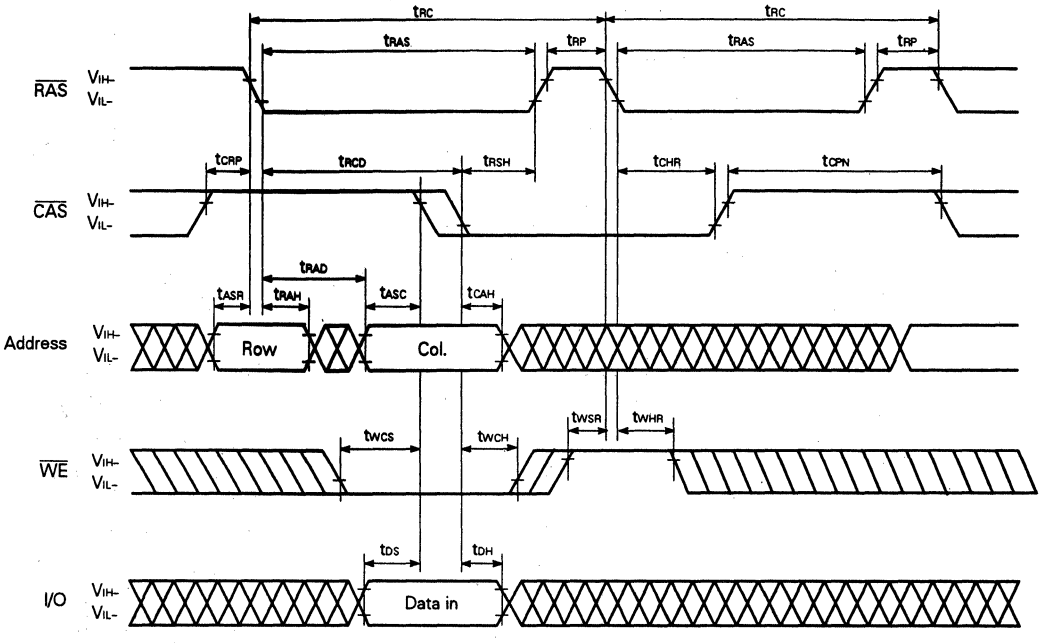


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



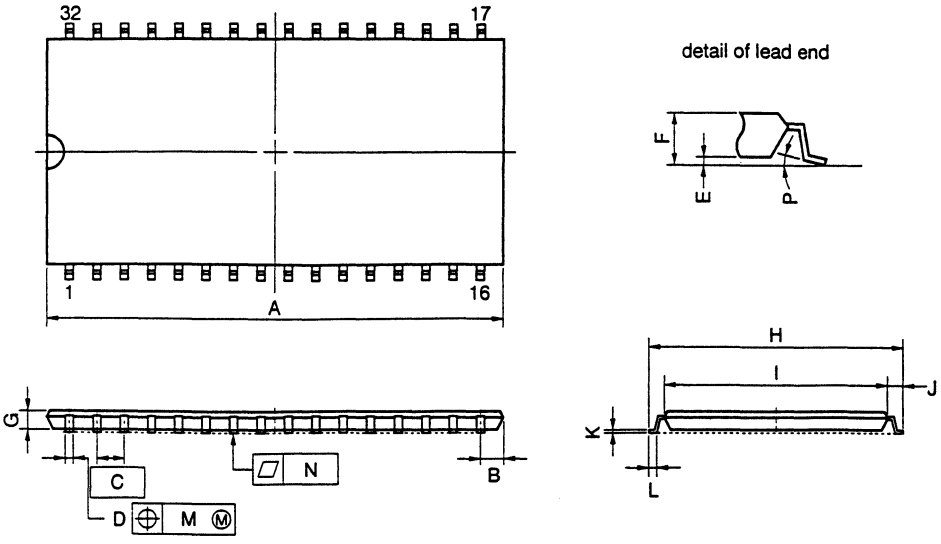
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



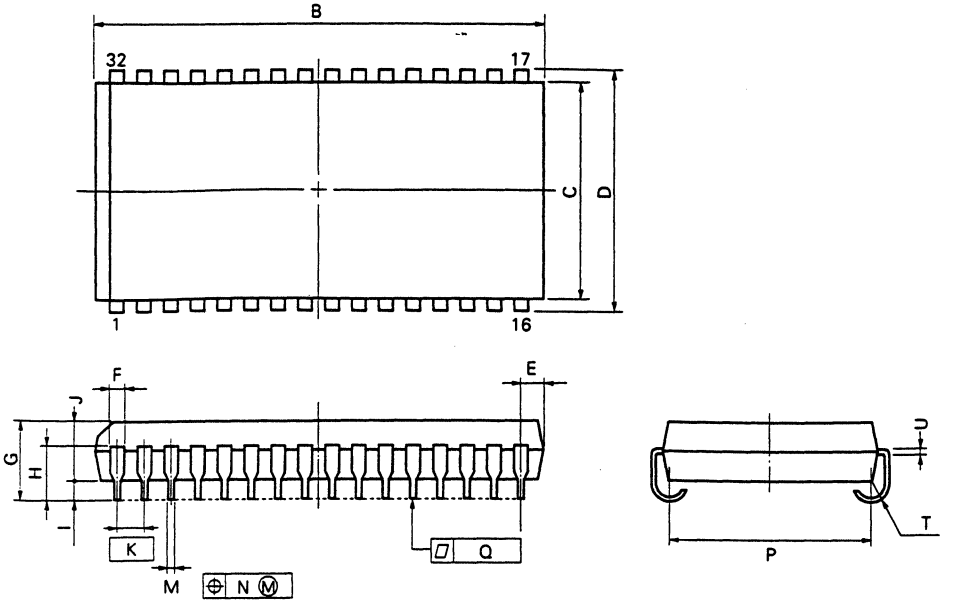
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NEC

MOS INTEGRATED CIRCUIT

μPD4264805, 4265805

64 M-BIT DYNAMIC RAM
8 M-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μPD4264805, 4265805 are 8,388,608 words by 8 bits CMOS dynamic RAMs with optional hyper page mode.
Hyper page mode is a kind of page mode and is useful for the read operation.
The μPD4264805, 4265805 are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- Hyper page mode
- Single +3.3 V±0.3V power supply
- 8,388,608 words by 8 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD4264805-A50, 4265805-A50	50 ns	84 ns	20 ns
μPD4264805-A60, 4265805-A60	60 ns	104 ns	25 ns
μPD4264805-A70, 4265805-A70	70 ns	124 ns	30 ns

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

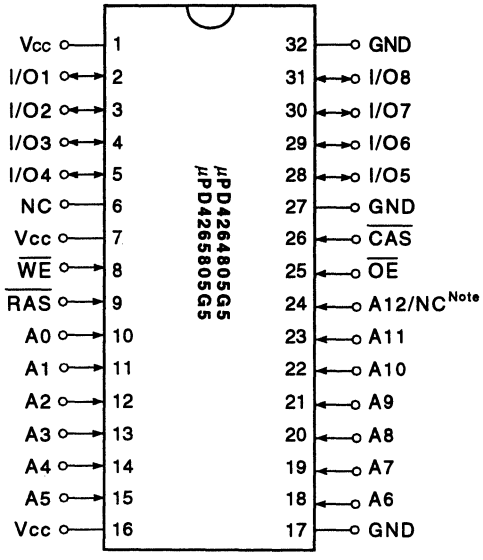
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264805	A0-A12	A0-A9	$\overline{RAS}$ only refresh, Normal Read / Write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265805	A0-A11	A0-A10	$\overline{RAS}$ only refresh, Normal Read / Write	4,096 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	

Ordering Information

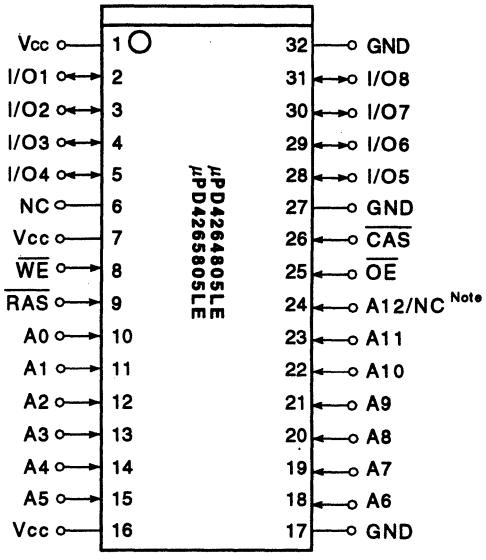
Part number	Access time (MAX.)	Package	Refresh
μPD4264805G5-A50	50 ns	32-pin Plastic TSOP(II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264805G5-A60	60 ns		
μPD4264805G5-A70	70 ns		
μPD4265805G5-A50	50 ns		
μPD4265805G5-A60	60 ns		
μPD4265805G5-A70	70 ns		
μPD4264805LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μPD4264805LE-A60	60 ns		
μPD4264805LE-A70	70 ns		
μPD4265805LE-A50	50 ns		
μPD4265805LE-A60	60 ns		
μPD4265805LE-A70	70 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12...μPD4264805
NC ... μPD4265805

A0 to A12	:	Address Inputs
I/O1 to I/O8	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264805, 4265805 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note 1] and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to AX[Note 1] (Address inputs)		Address bus. Input total 23-bit of address signal, upper bits and lower bits in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note1.

Part number	Address inputs	Upper bits	Lower bits
μPD4264805	A0-A12	13	10
μPD4265805	A0-A11	12	11

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is lager than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

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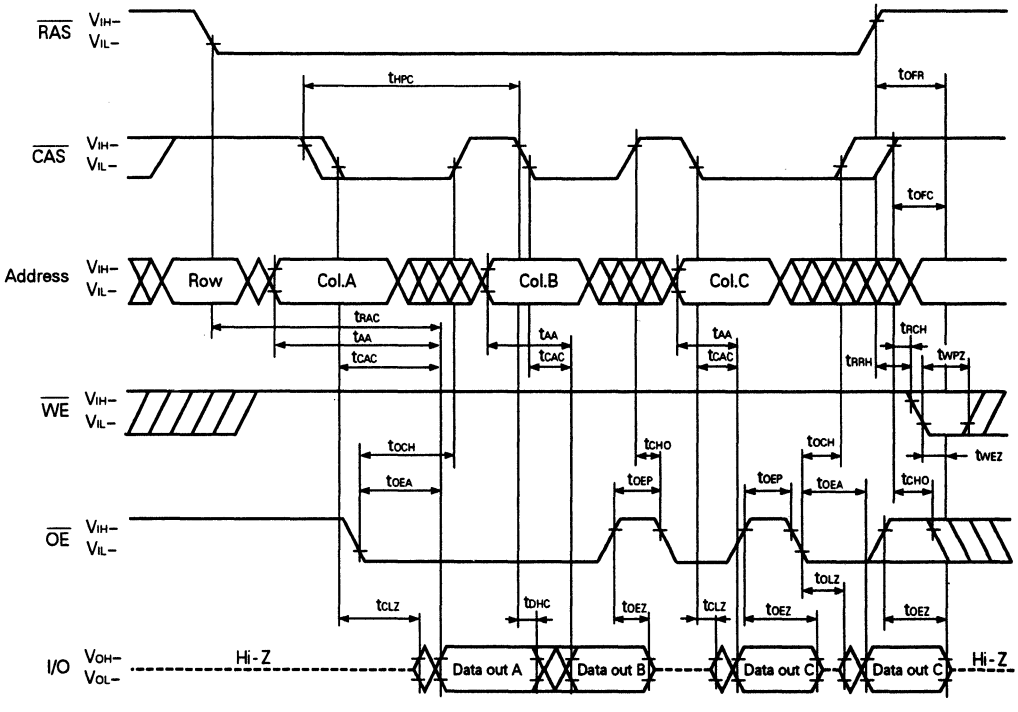
2. **The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.**
   In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted) [μPD4264805]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		105	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		95		
		I_O = 0 mA	t_{RAC} = 70 ns		85		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		105	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH(MIN.)}$	t_{RAC} = 60 ns		95		
		t_{RC} = $t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL(MAX.)}$	t_{RAC} = 50 ns		105	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		95		
		t_{HPC} = $t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265805]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2,3
		$t_{RC} = t_{RC(MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC} - 0.2$ V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2,3,4
		$\overline{CAS} \geqq V_{IH(MIN.)}$	t_{RAC} = 60 ns		115		
		$t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		105		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$	t_{RAC} = 50 ns		105	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		95		
		$t_{HPC} = t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2
		$t_{RC} = t_{RC(MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.

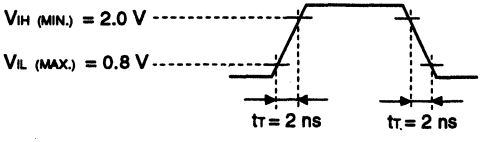
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

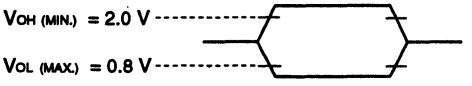
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	84	—	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	30	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	7	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	7	10 000	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	38	—	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	11	37	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	9	25	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	0	—	ns	
Row Address Hold Time	tRAH	7	—	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	0	—	ns	
Column Address Hold Time	tCAH	7	—	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	10	—	13	—	15	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	1	50	ns	
Refresh Time	tREF	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	—	10	—	12	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7	—	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	7	—	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	107	—	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64	—	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27	—	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39	—	47	—	54	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20	—	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	—	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	30	—	35	—	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41	—	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	52	—	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	7	—	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3.4

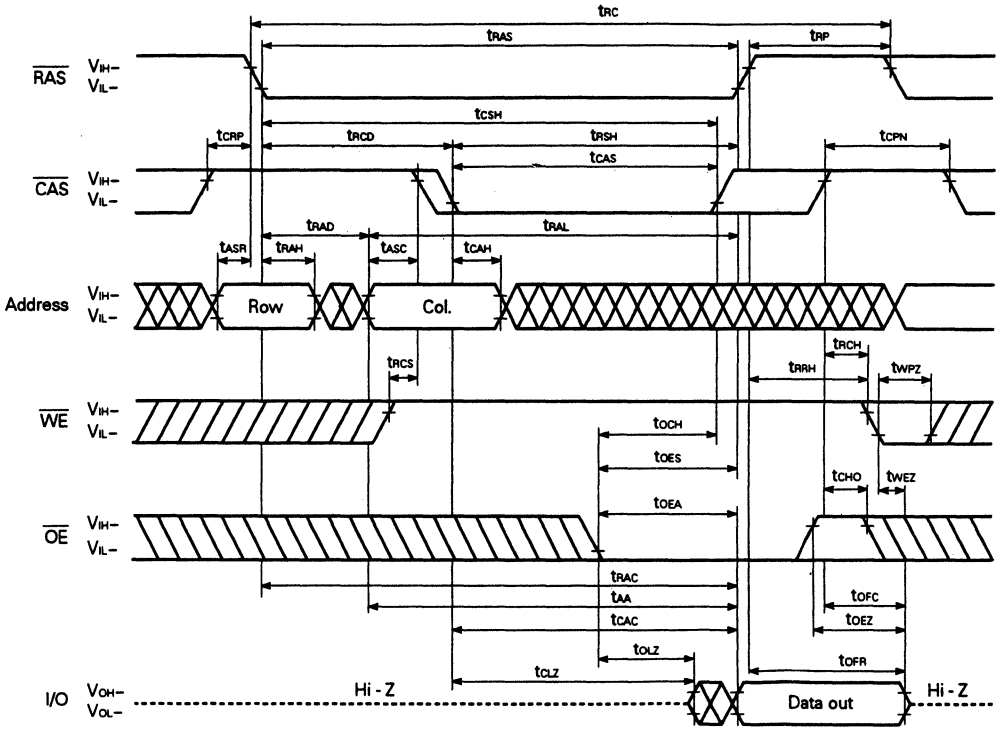
Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.
4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.
   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

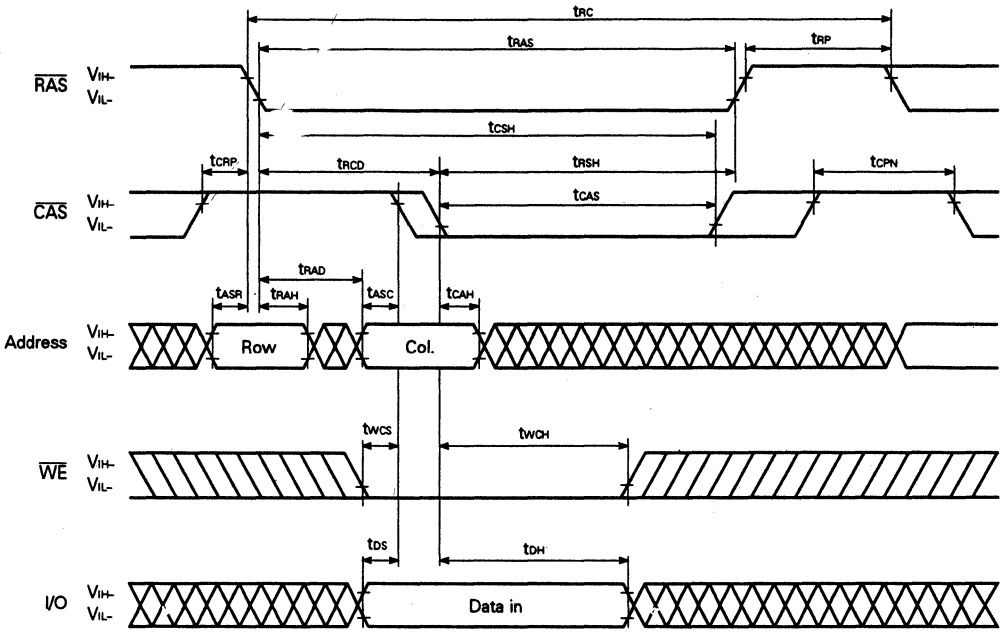
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	15	—	ns	

Read Cycle

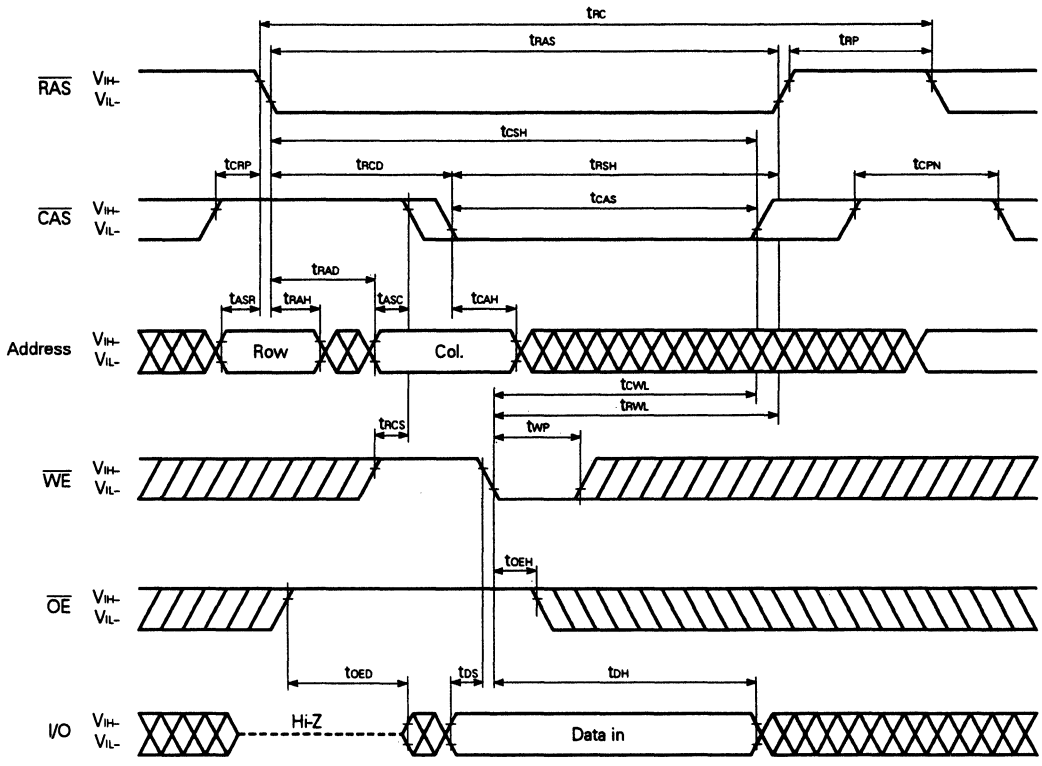

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

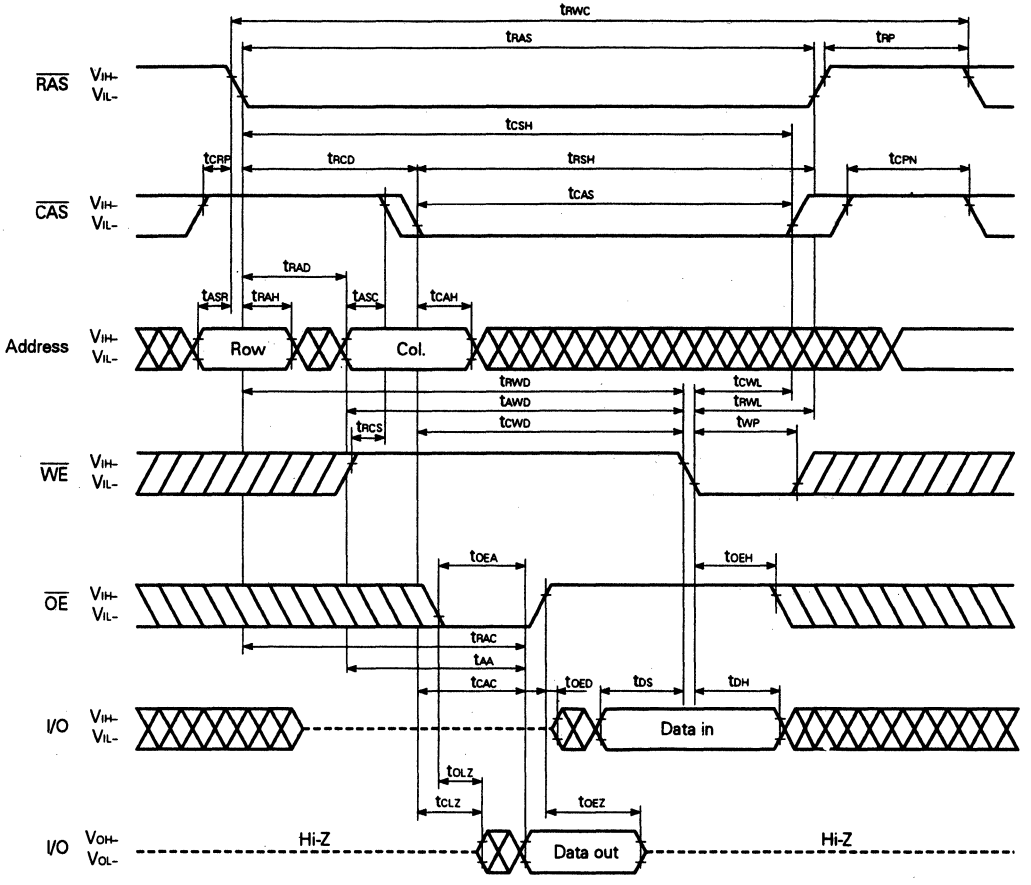


Remark $\overline{OE}$: Don't care

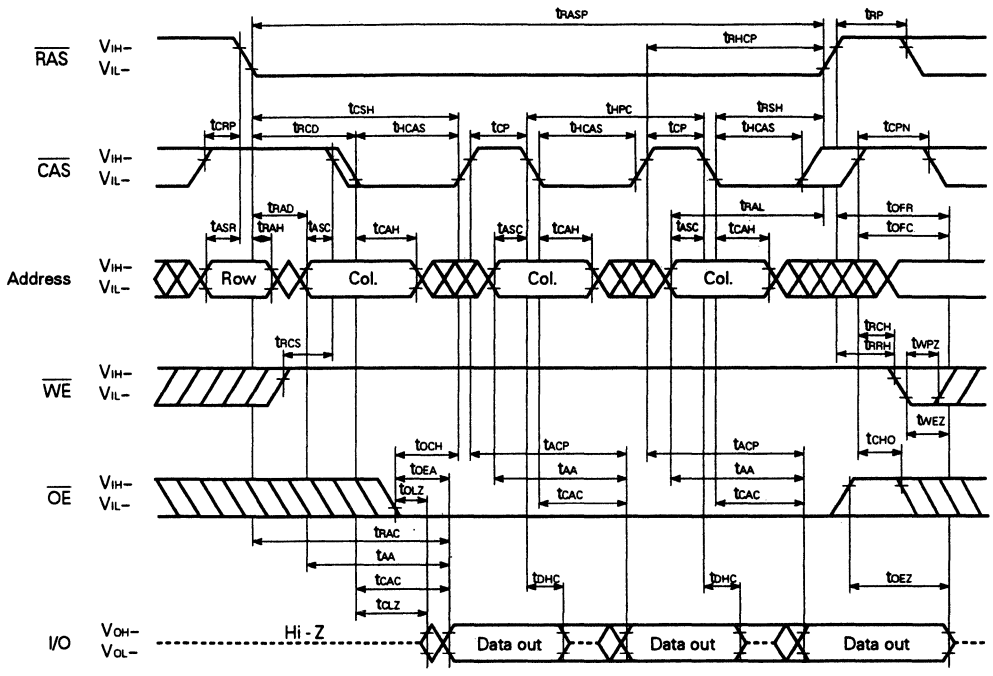
Late Write Cycle



Read Modify Write Cycle

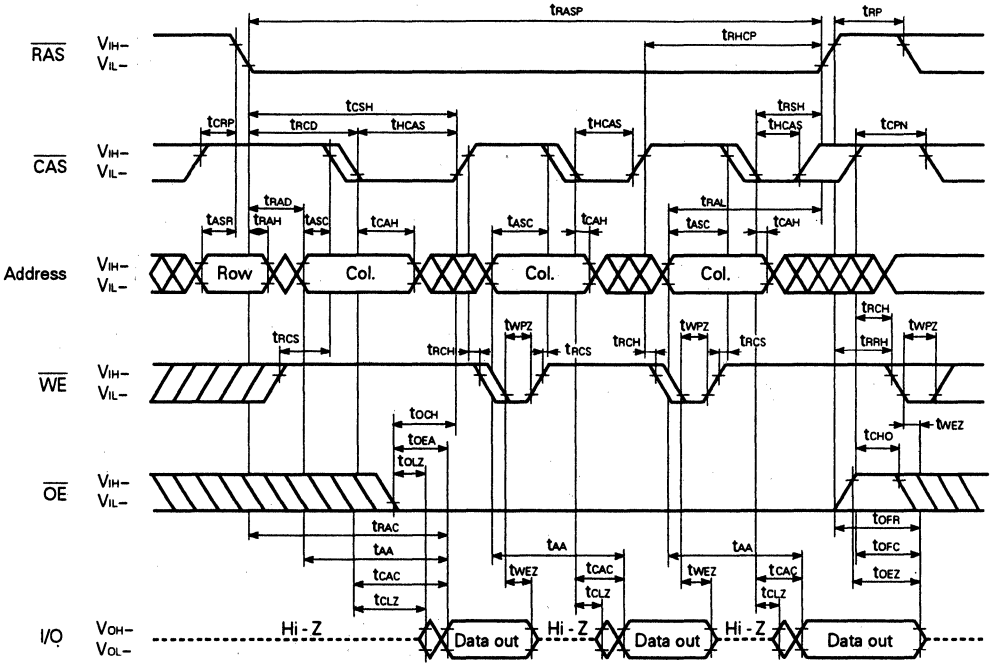


Hyper Page Mode Read Cycle



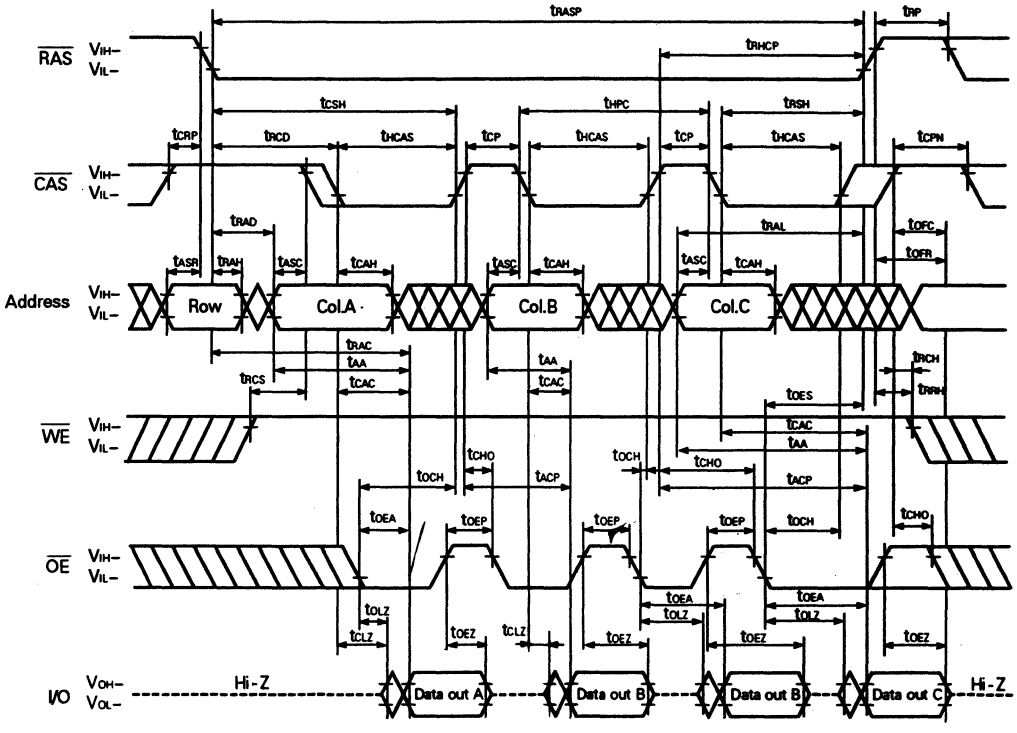
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



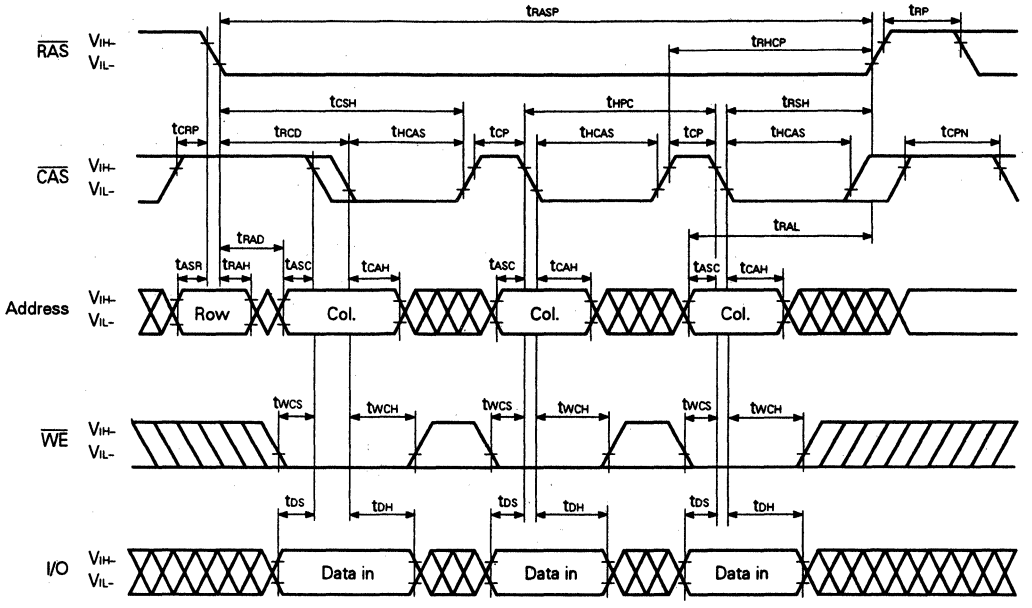
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

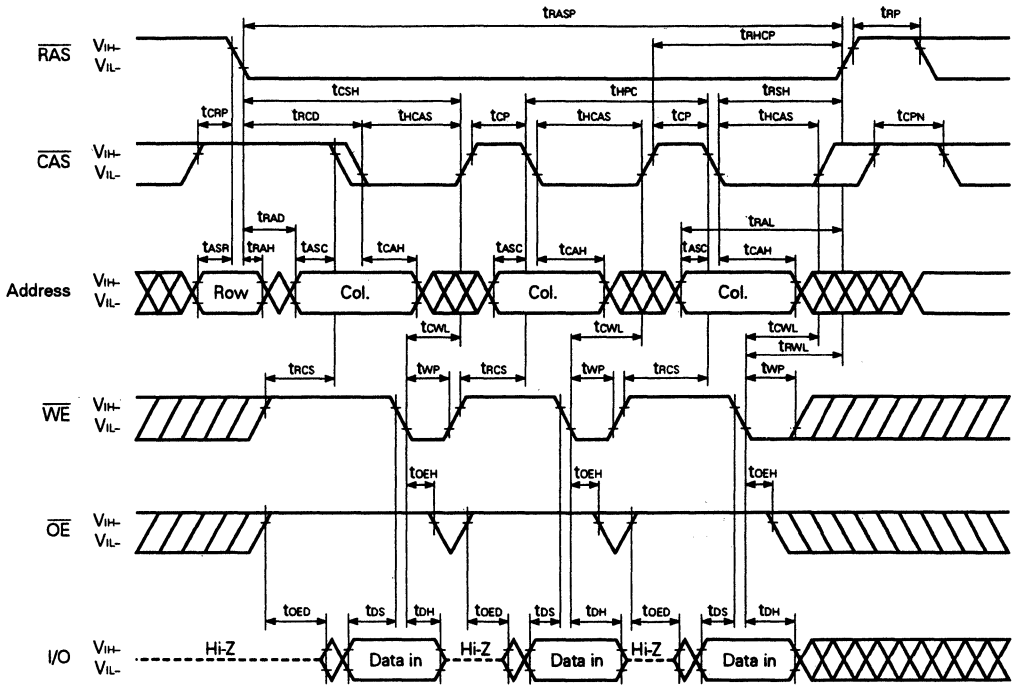
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

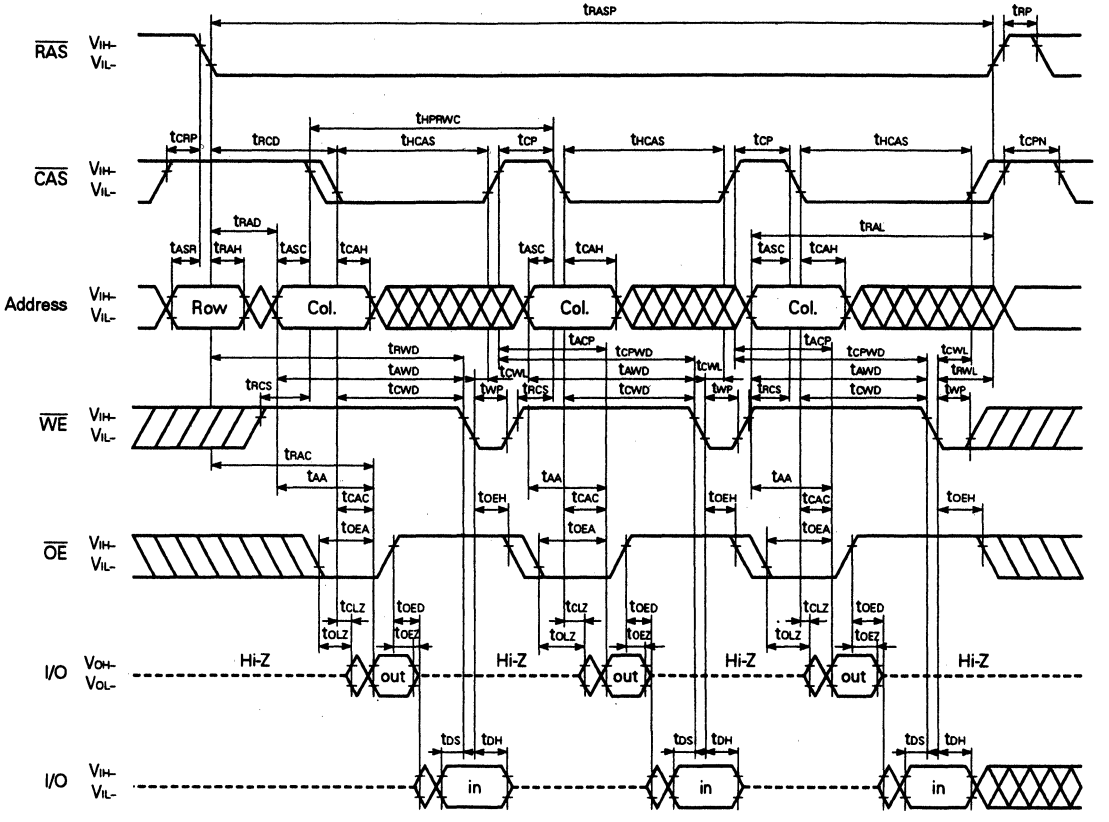
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



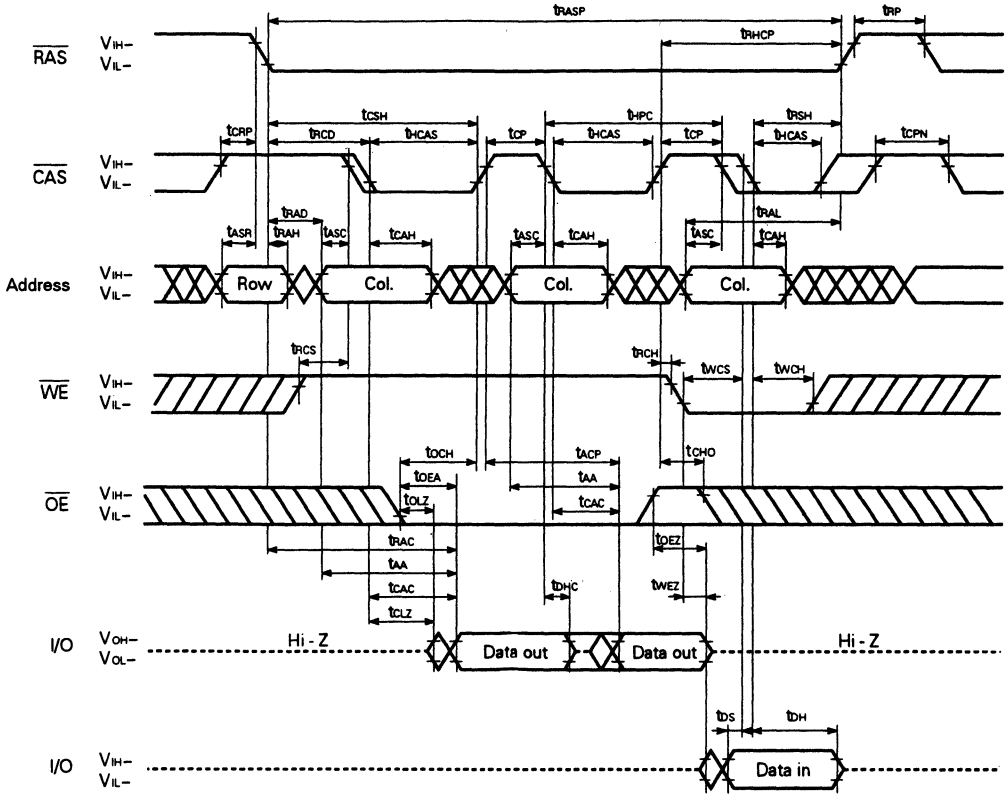
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



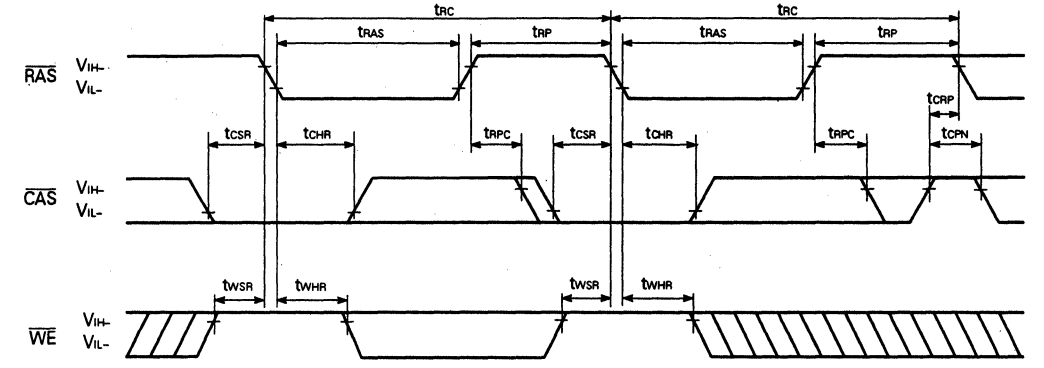
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



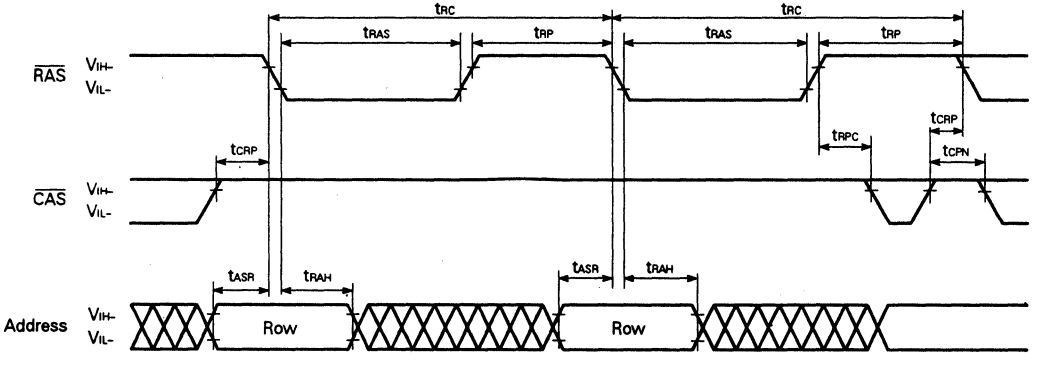
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



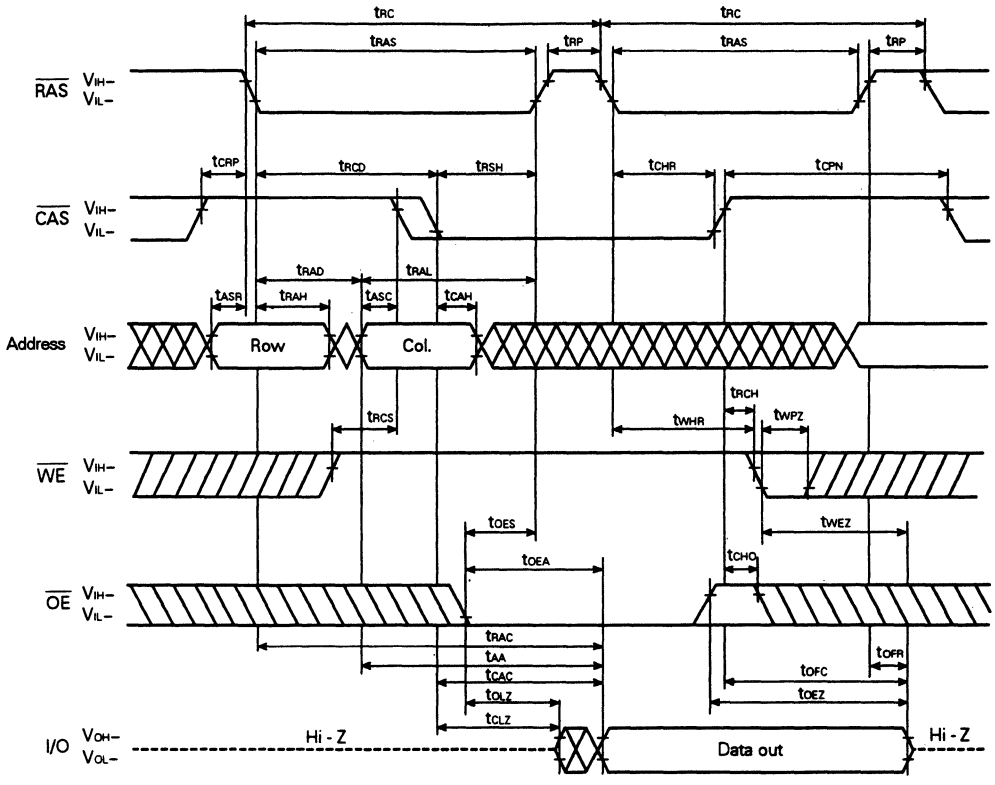
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

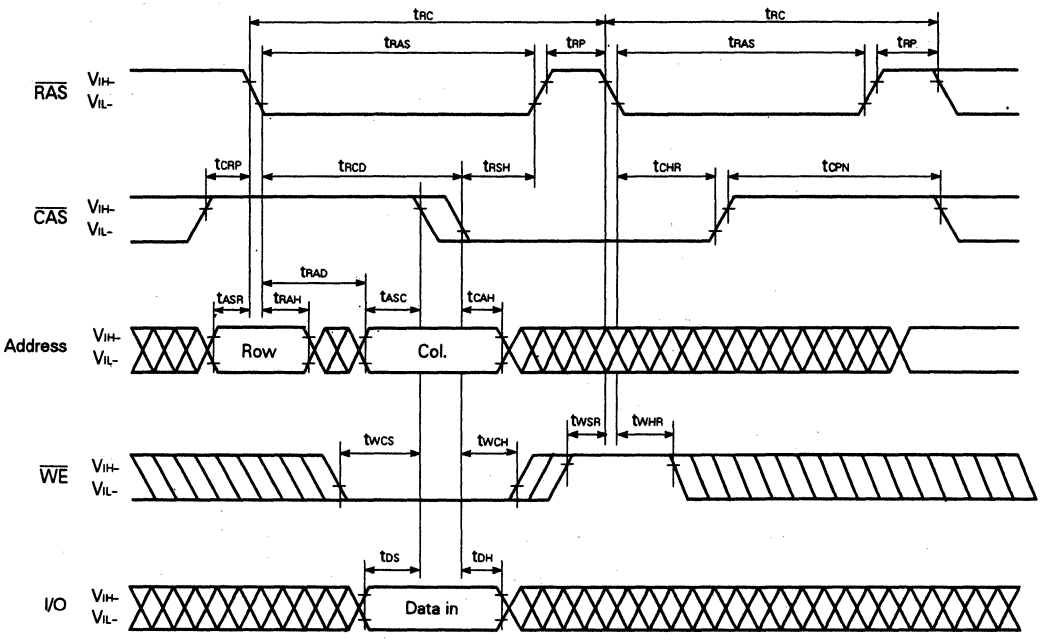


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



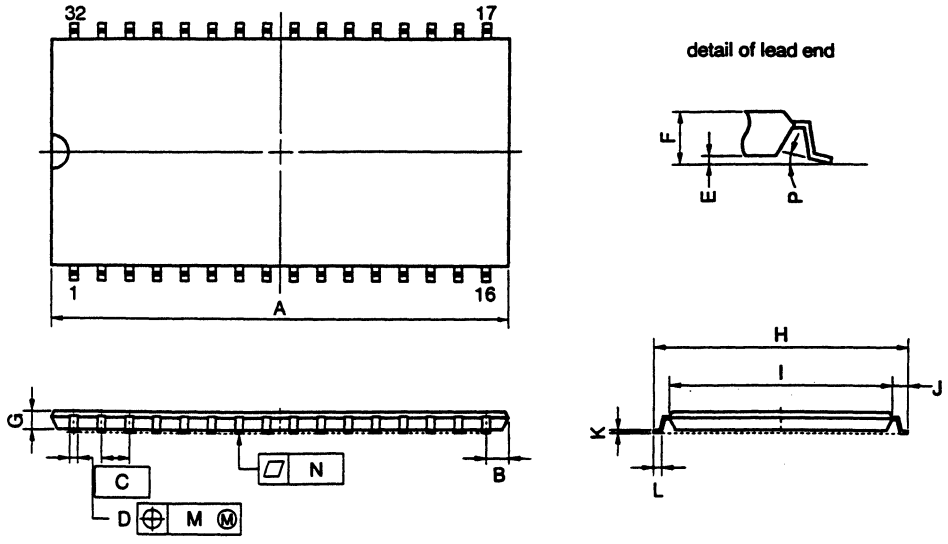
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



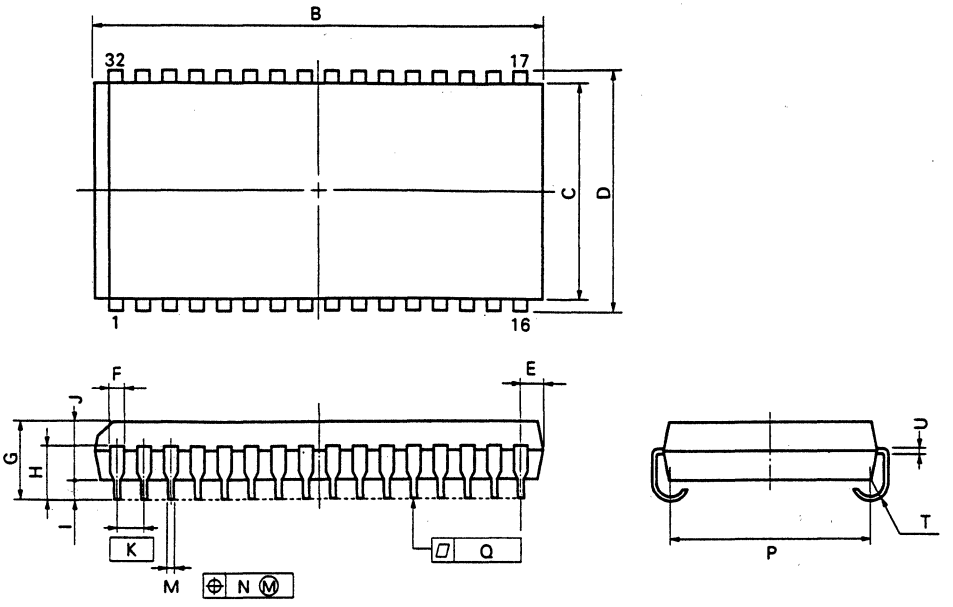
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch, of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

NEC

MOS INTEGRATED CIRCUIT

μPD4264165, 4265165

64 M-BIT DYNAMIC RAM
4 M-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD4264165, 4265165 are 4,194,304 words by 16 bits CMOS dynamic RAMs with optional hyper page mode.
Hyper page mode is a kind of page mode and is useful for the read operation.
The μPD4264165, 4265165 are packaged in 50-pin plastic TSOP(II).

Features

- Hyper page mode
- Single +3.3 V±0.3V power supply
- 4,194,304 words by 16 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD4264165-A50, 4265165-A50	50 ns	84 ns	20 ns
μPD4264165-A60, 4265165-A60	60 ns	104 ns	25 ns
μPD4264165-A70, 4265165-A70	70 ns	124 ns	30 ns

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

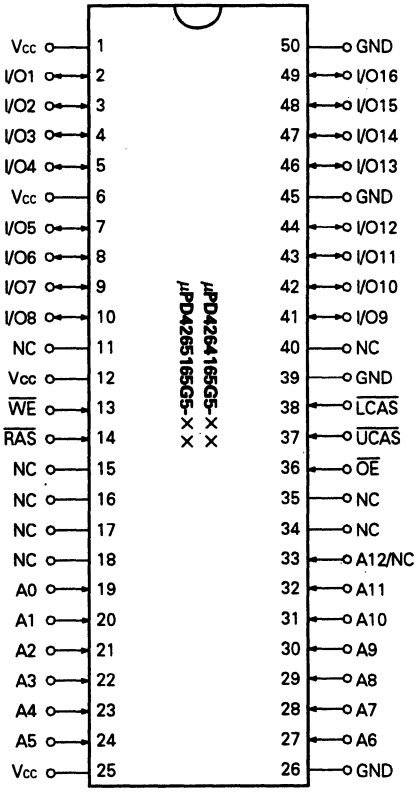
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264165	A0-A12	A0-A8	$\overline{RAS}$ only refresh, Normal Read / Write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265165	A0-A11	A0-A9	$\overline{RAS}$ only refresh, Normal Read / Write	4,096 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD4264165G5-A50	50 ns	50-pin Plastic TSOP(II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264165G5-A60	60 ns		
μPD4264165G5-A70	70 ns		
μPD4265165G5-A50	50 ns		
μPD4265165G5-A60	60 ns		
μPD4265165G5-A70	70 ns		

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)



Note A12...μPD4264165
NC ... μPD4265165

A0 to A12	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
VCC	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264165, 4265165 have input pins $\overline{RAS}$, $\overline{CAS}$ Note 1, $\overline{WE}$, $\overline{OE}$, Address Note 2 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to AX Note 2 (Address inputs)		Address bus. Input total 22-bit of address signal, upper bits and lower bits in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2.

Part number	Address inputs	Upper bits	Lower bits
μPD4264165	A0-A12	13	9
μPD4265165	A0-A11	12	10

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is lager than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

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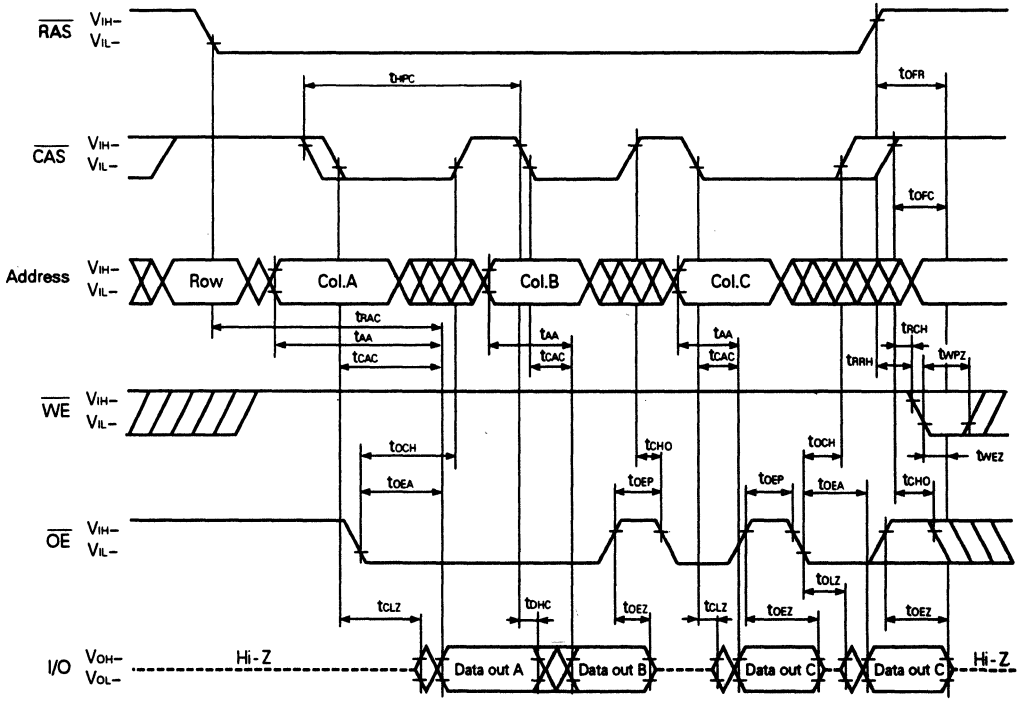
The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. **Data output time is extended.**
   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.**
   In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted) [μPD4264165]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		110	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		100		
		I_O = 0 mA	t_{RAC} = 70 ns		90		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH (MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		110	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH (MIN.)}$	t_{RAC} = 60 ns		100		
		t_{RC} = $t_{RC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		90		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL (MAX.)}$	t_{RAC} = 50 ns		110	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		100		
		t_{HPC} = $t_{HPC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1,2
		t_{RC} = $t_{RC (MIN.)}$	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
Input leakage current	$I_{I (L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265165]

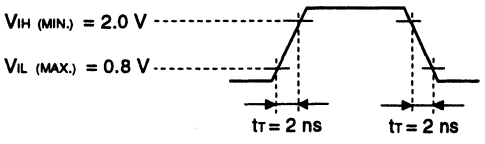
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH(MIN.)}$	t_{RAC} = 60 ns		120		
		t_{RC} = $t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		110		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL(MAX.)}$	t_{RAC} = 50 ns		110	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		100		
		t_{HPC} = $t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1,2
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≦ $V_{IL(MAX.)}$ and $\overline{CAS}$ ≧ $V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

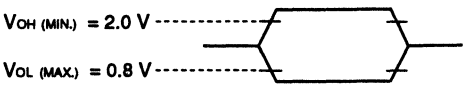
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	84	—	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	30	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	7	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	7	10 000	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	38	—	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	11	37	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	9	25	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	0	—	ns	
Row Address Hold Time	tRAH	7	—	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	0	—	ns	
Column Address Hold Time	tCAH	7	—	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	10	—	13	—	15	—	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$	tMRH	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	1	50	ns	
Refresh Time	tREF	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	—	10	—	12	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7	—	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	7	—	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	107	—	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64	—	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27	—	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39	—	47	—	54	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20	—	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	—	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	30	—	35	—	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41	—	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	52	—	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	7	—	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

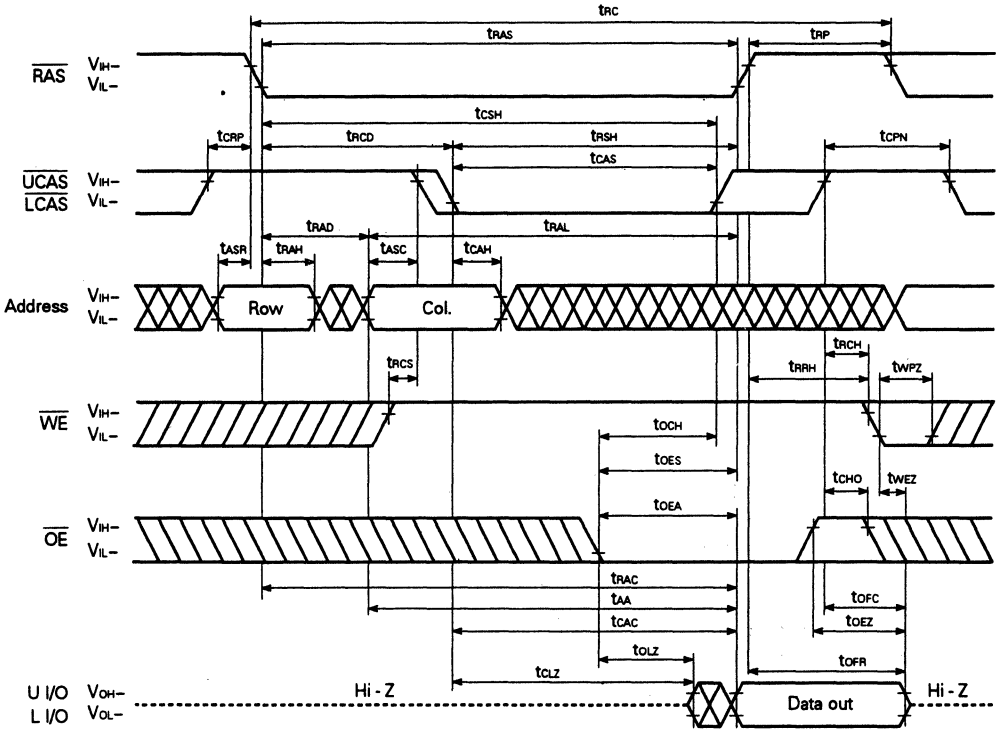
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.

   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

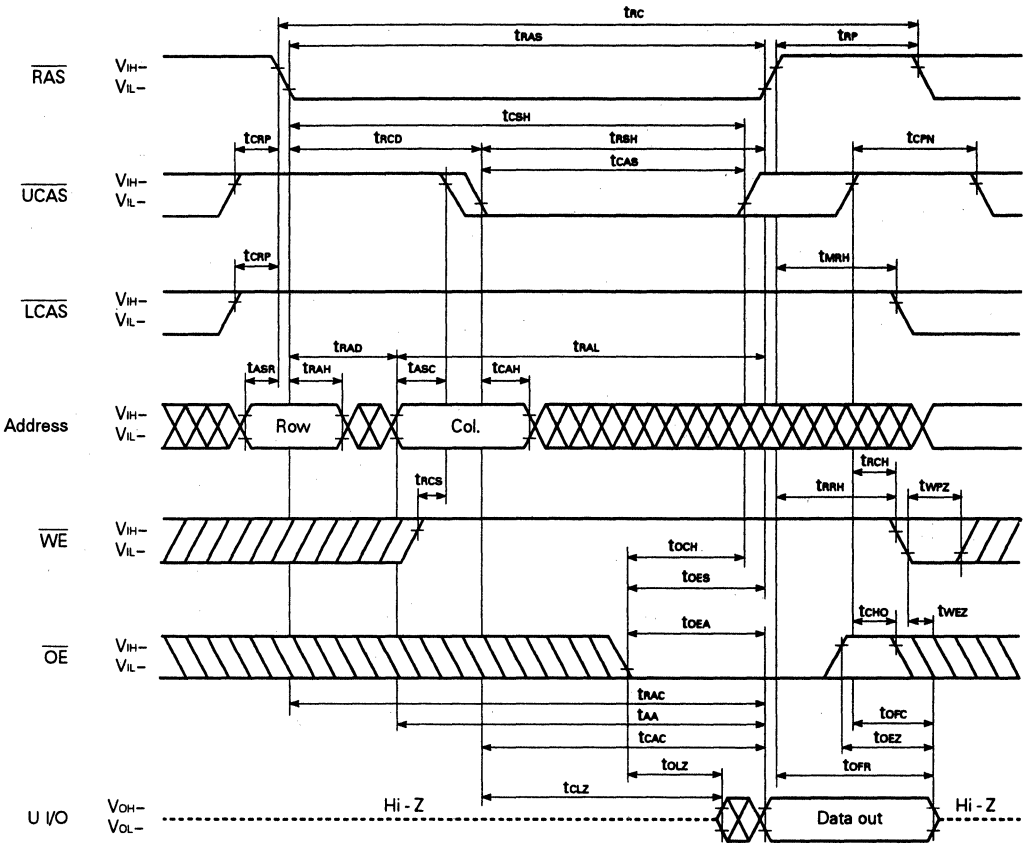
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	—	15	—	15	—	ns	

Read Cycle

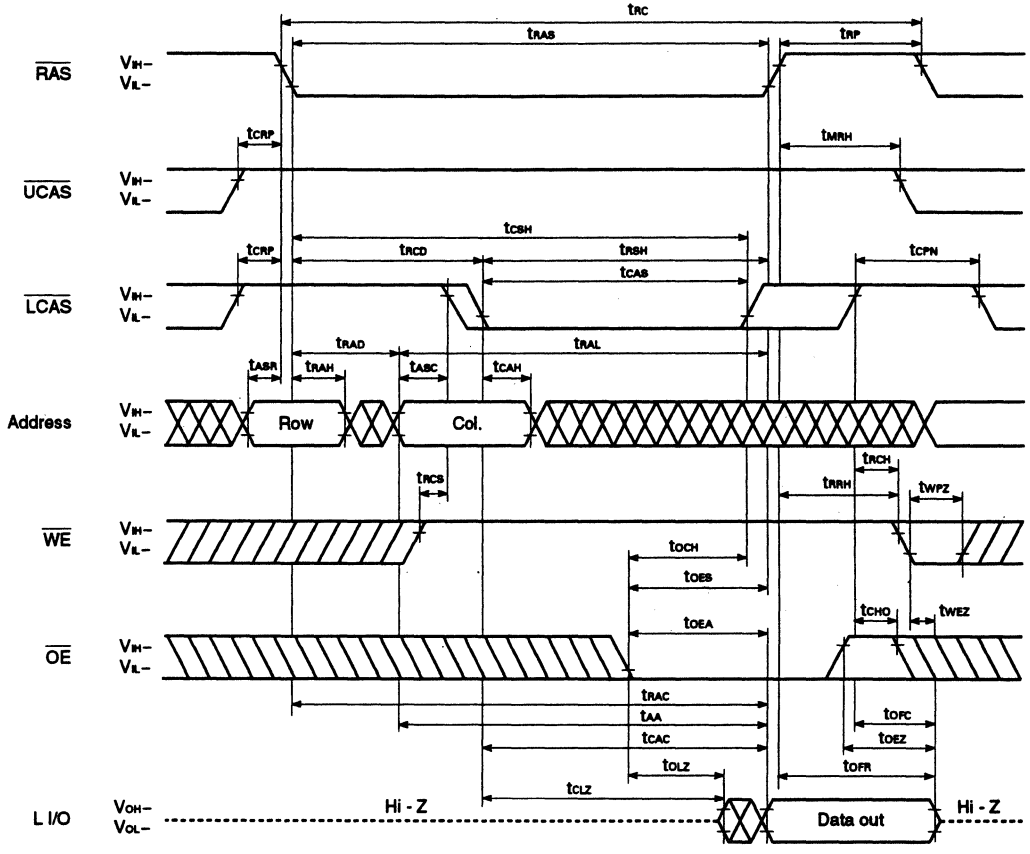

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS VIH– LCAS VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
tOEA
OE VIH– VIL–
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O VOH– L I/O VOL–
Hi-Z
Data out
Hi-Z

Upper Byte Read Cycle



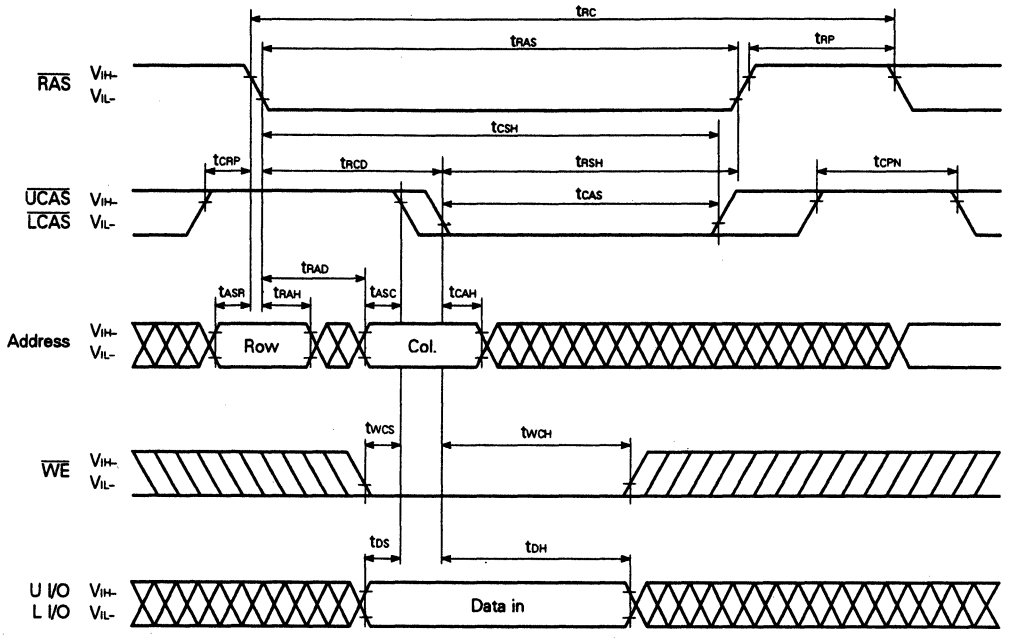
Remark L I/O: Hi-Z

Lower Byte Read Cycle



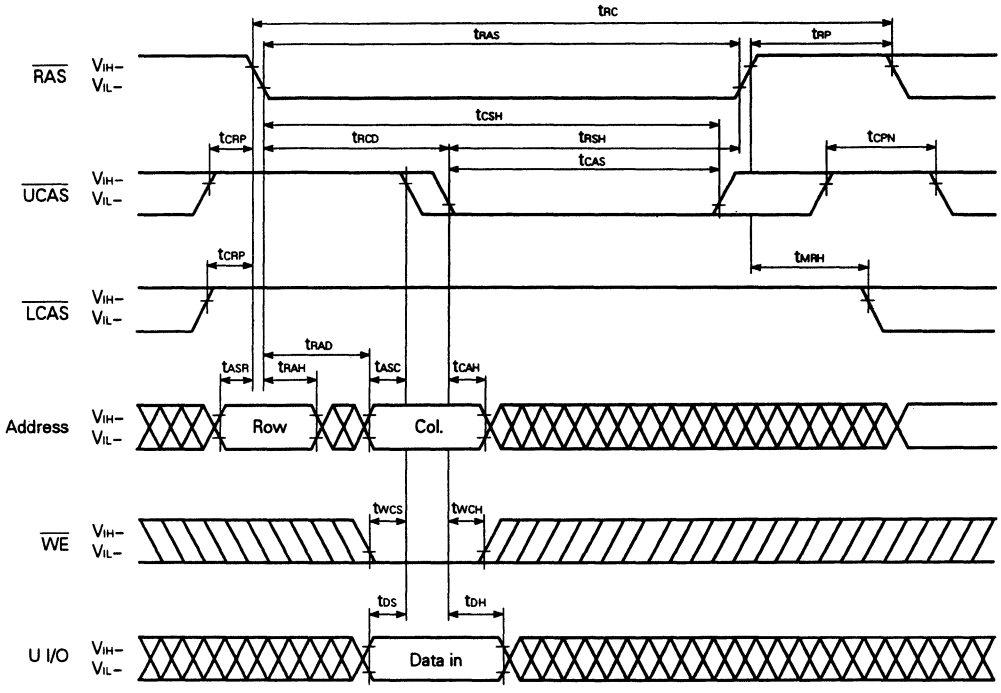
Remark U I/O: Hi-Z

Early Write Cycle



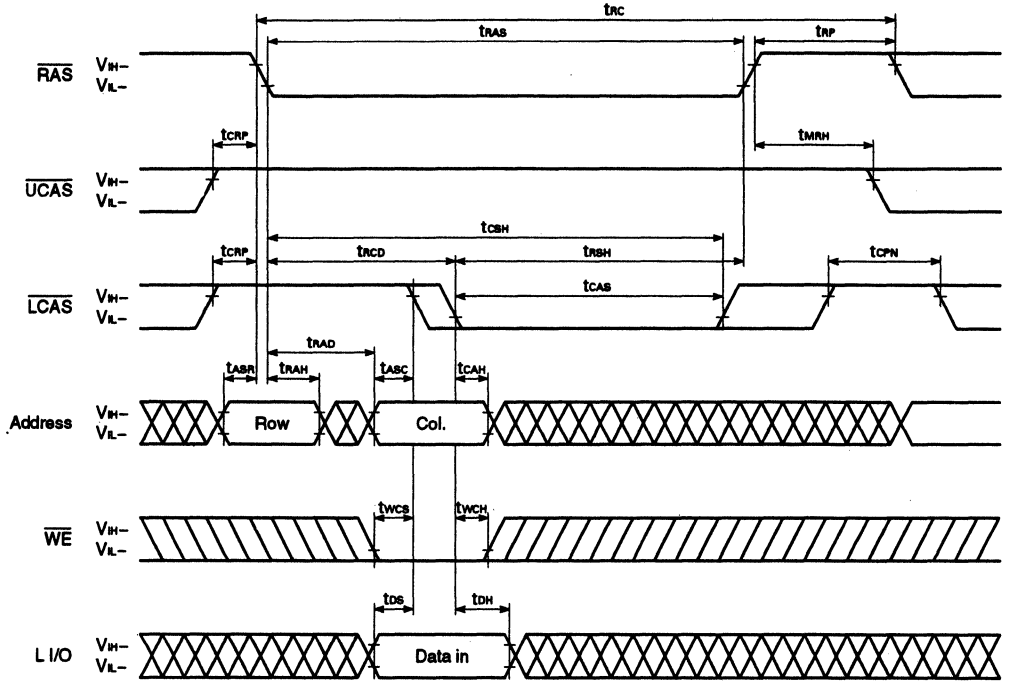
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



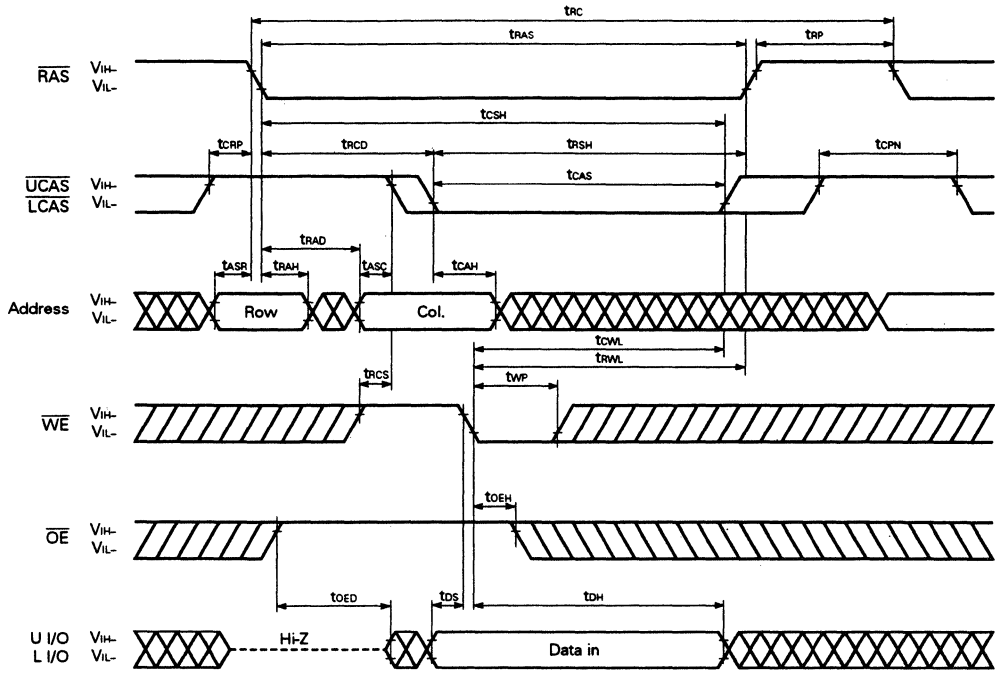
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

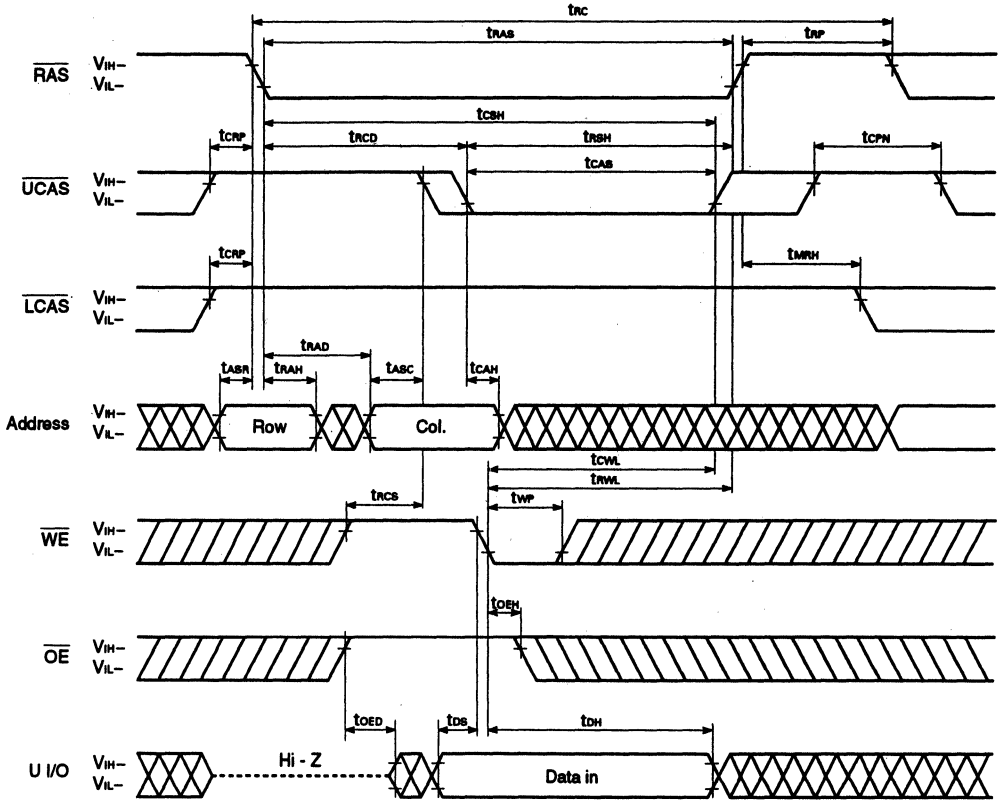


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

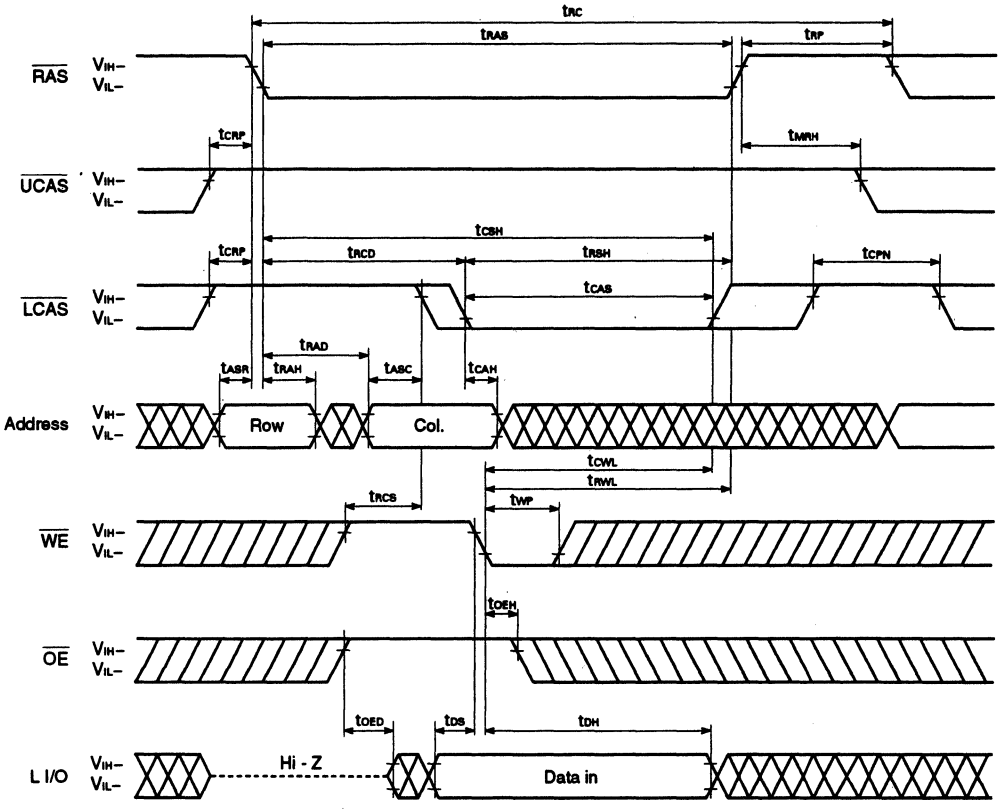


Upper Byte Late Write Cycle



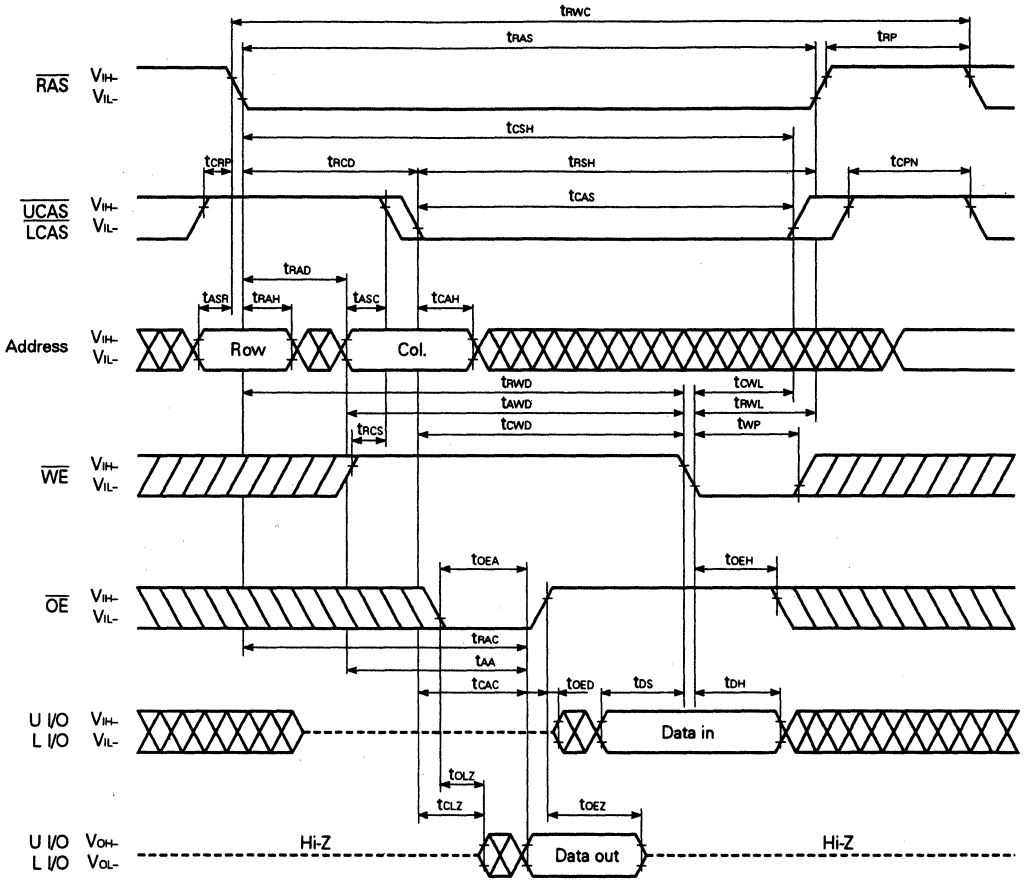
Remark L I/O: Don't care

Lower Byte Late Write Cycle

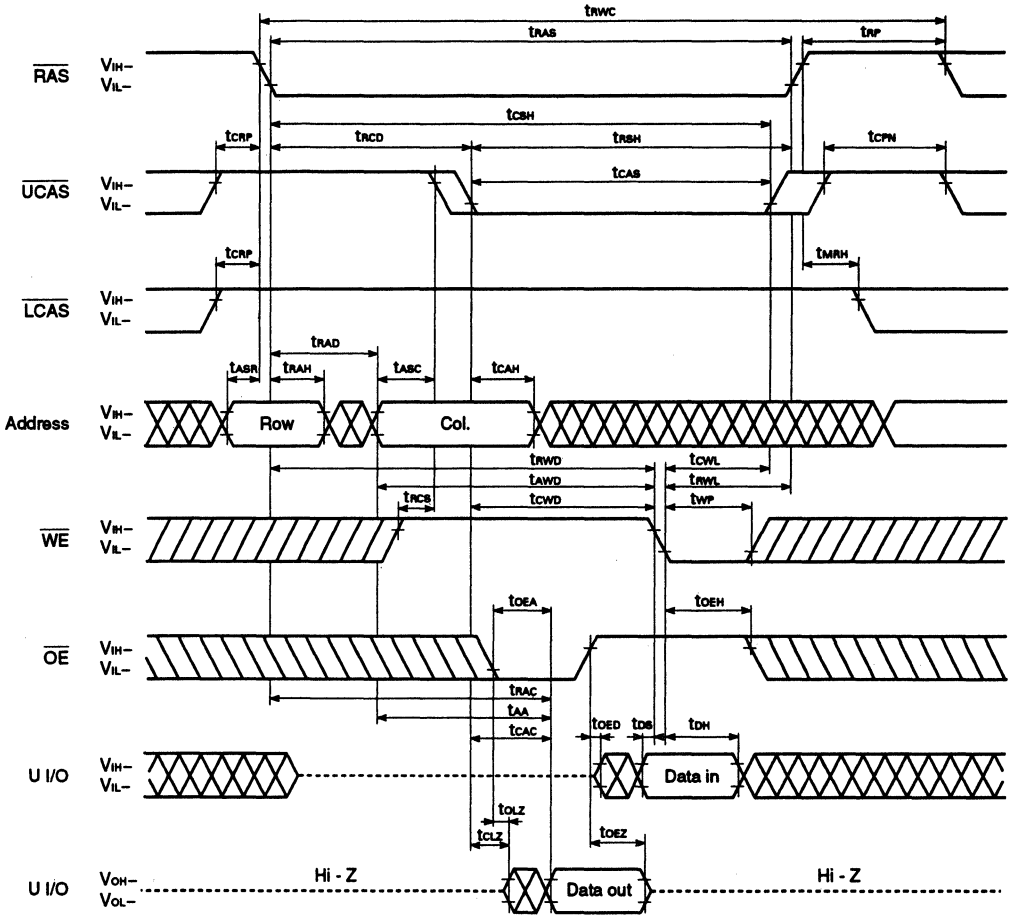


Remark U I/O: Don't care

Read Modify Write Cycle

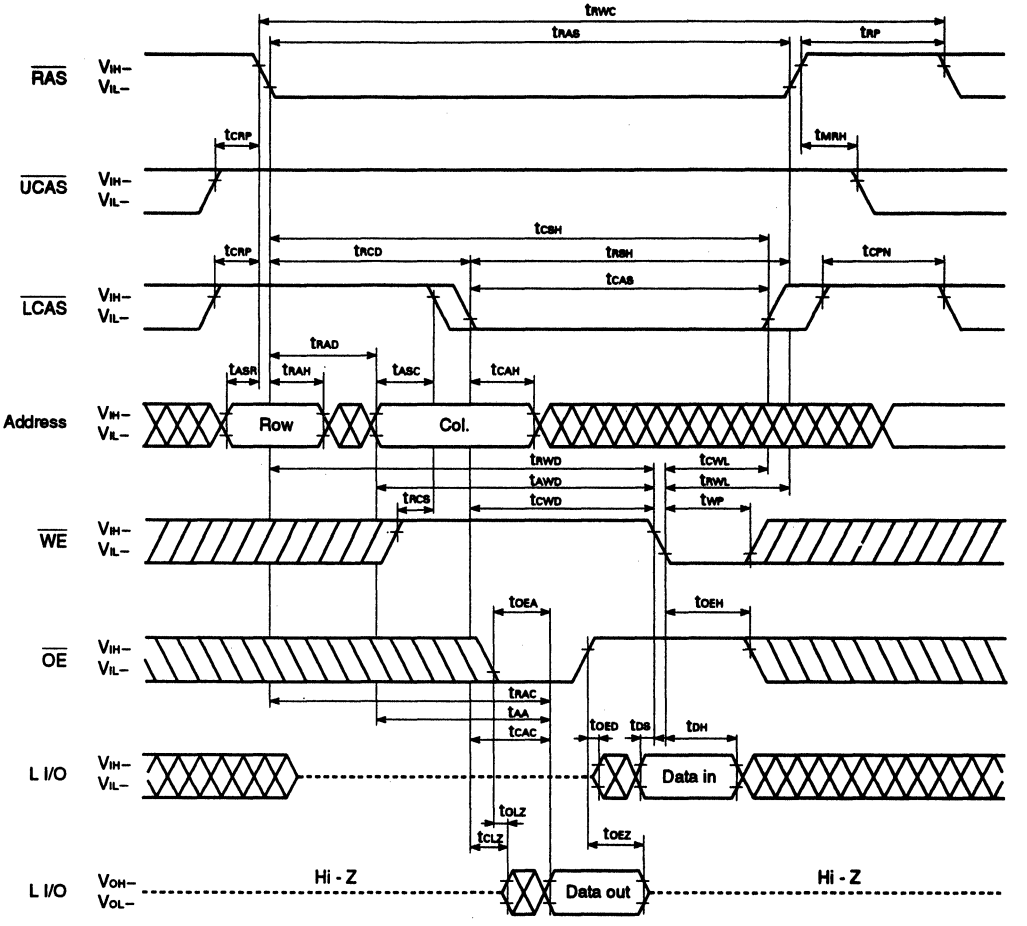


Upper Byte Read Modify Write Cycle



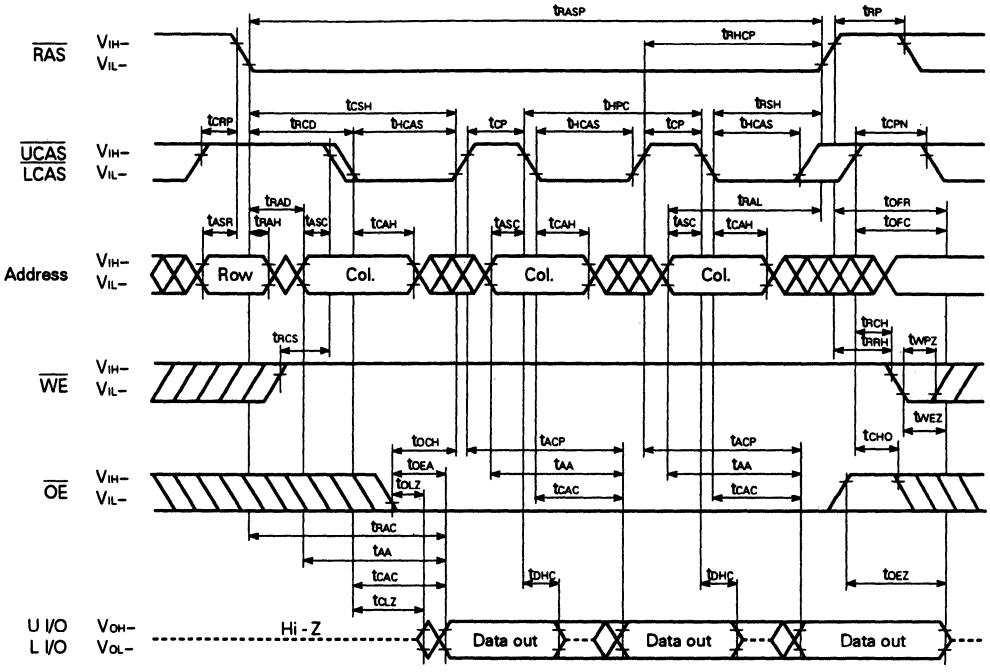
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



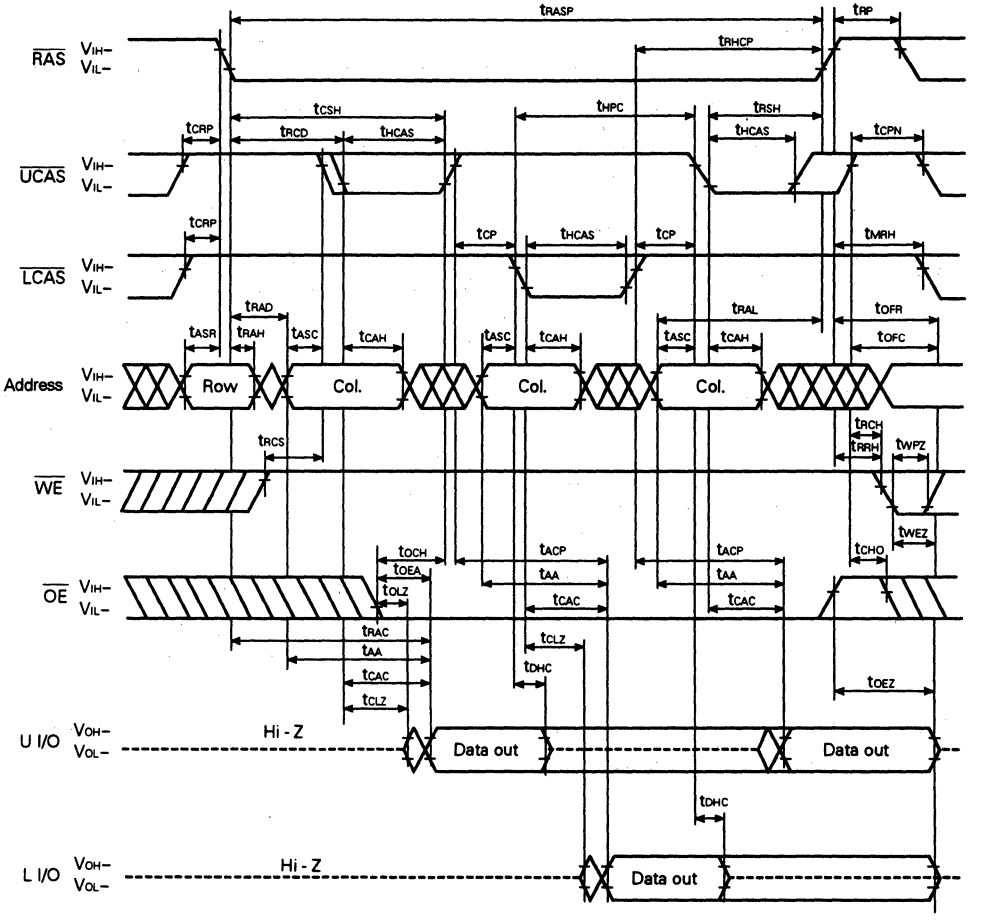
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Read Cycle



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

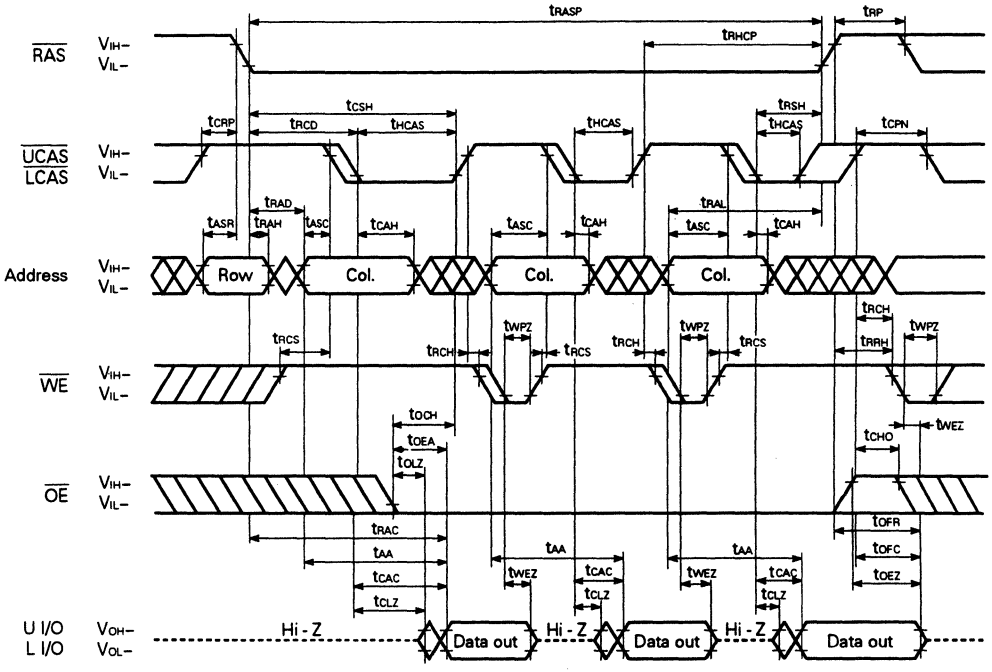
Hyper Page Mode Byte Read Cycle



Remark 1. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

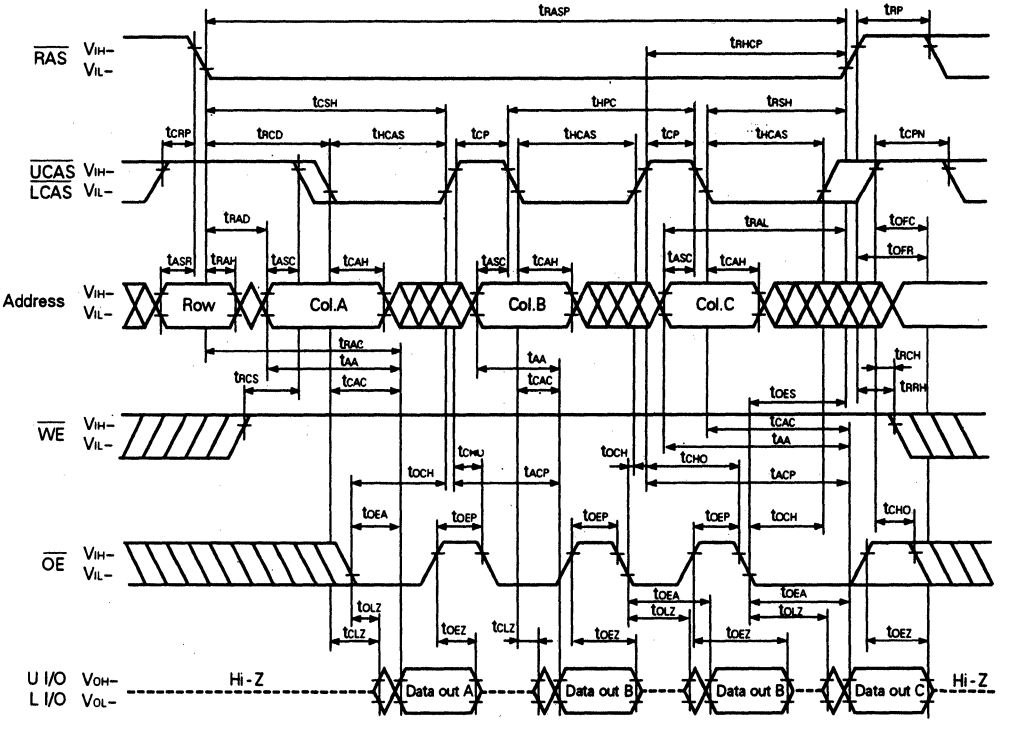
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



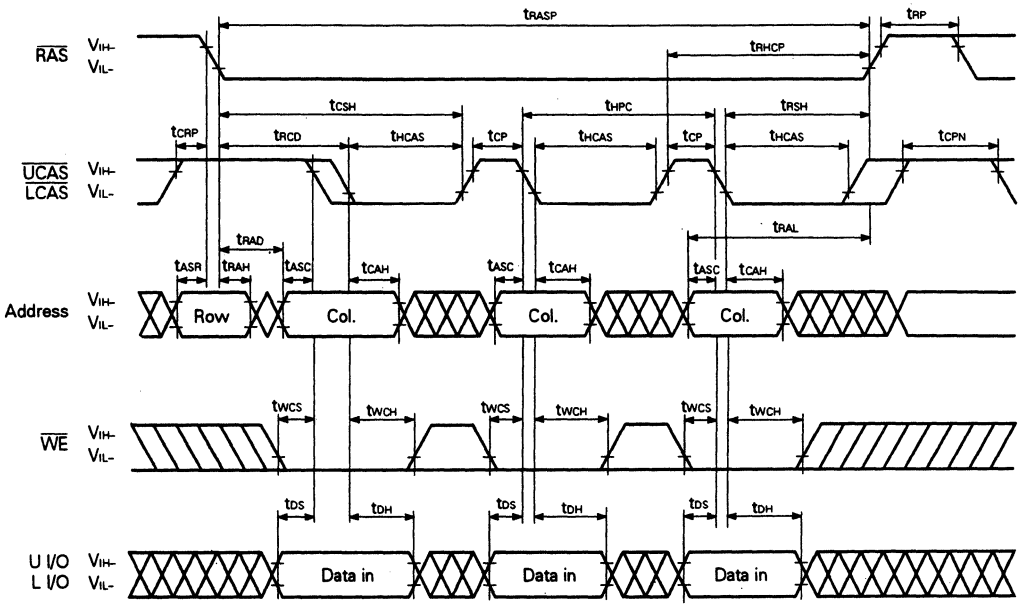
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

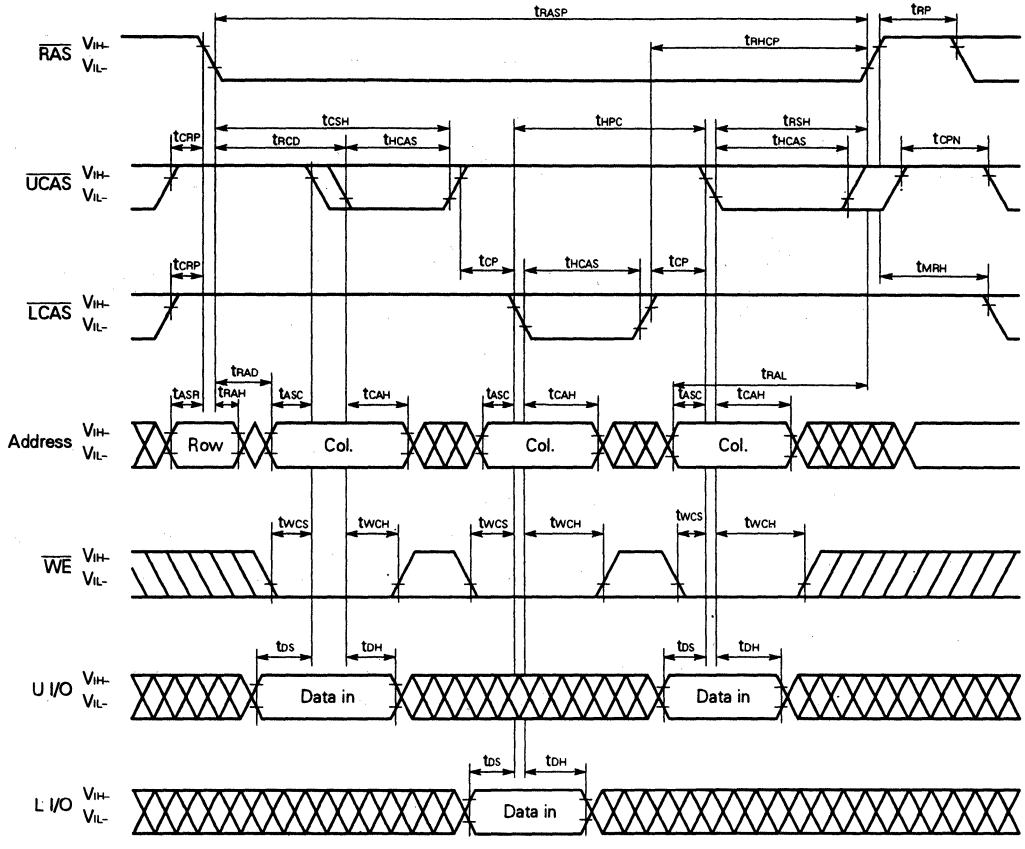
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

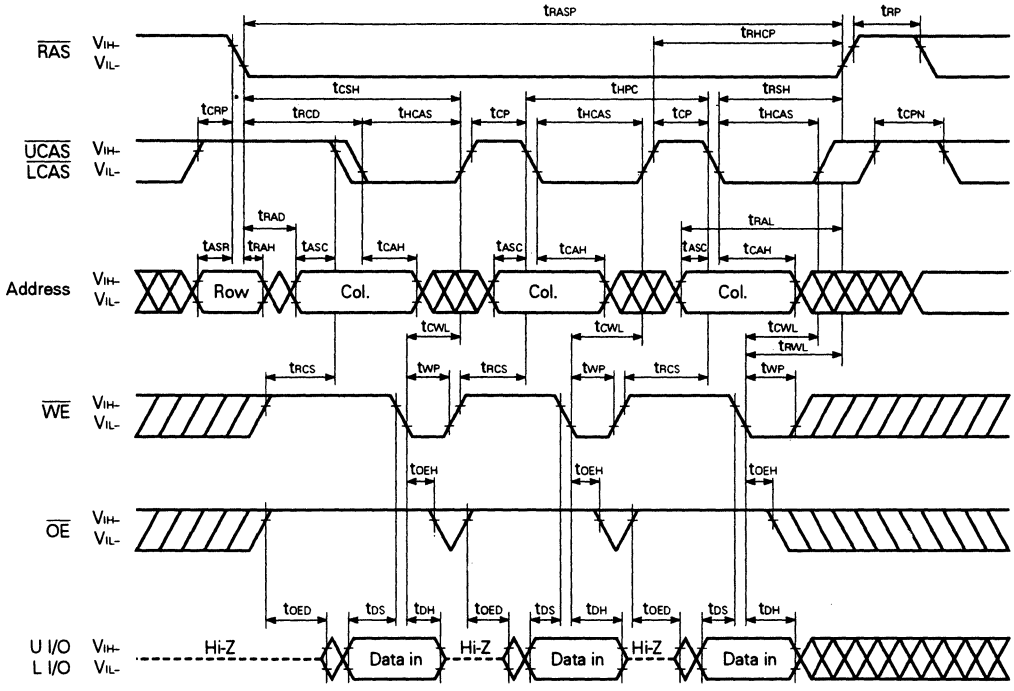
Hyper Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

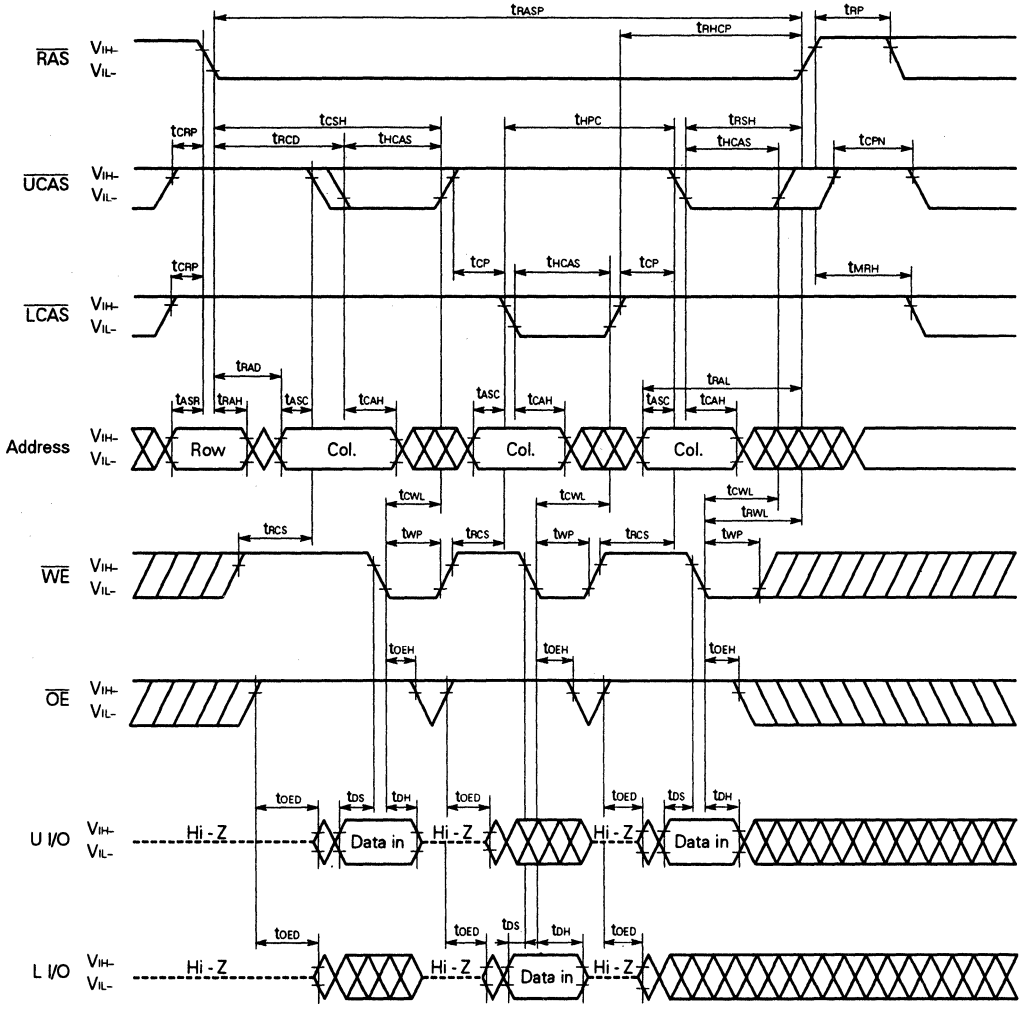
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode Late Write Cycle



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

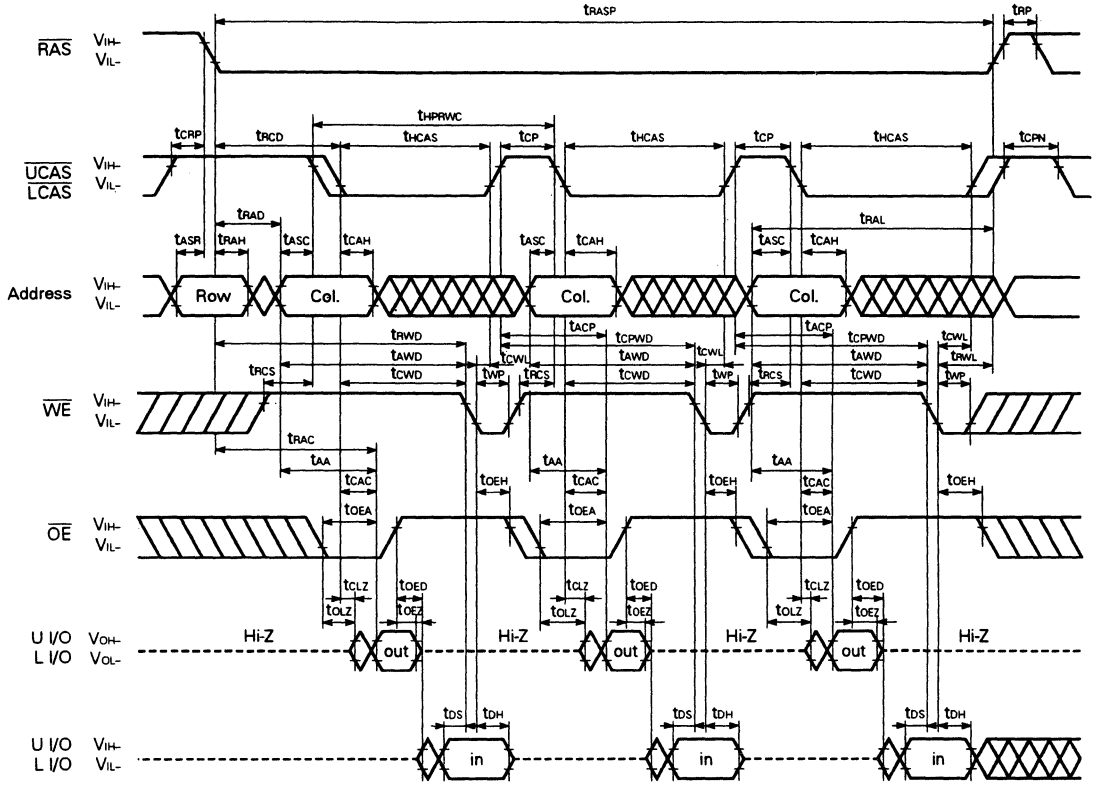
Hyper Page Mode Byte Late Write Cycle



Remarks 1. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

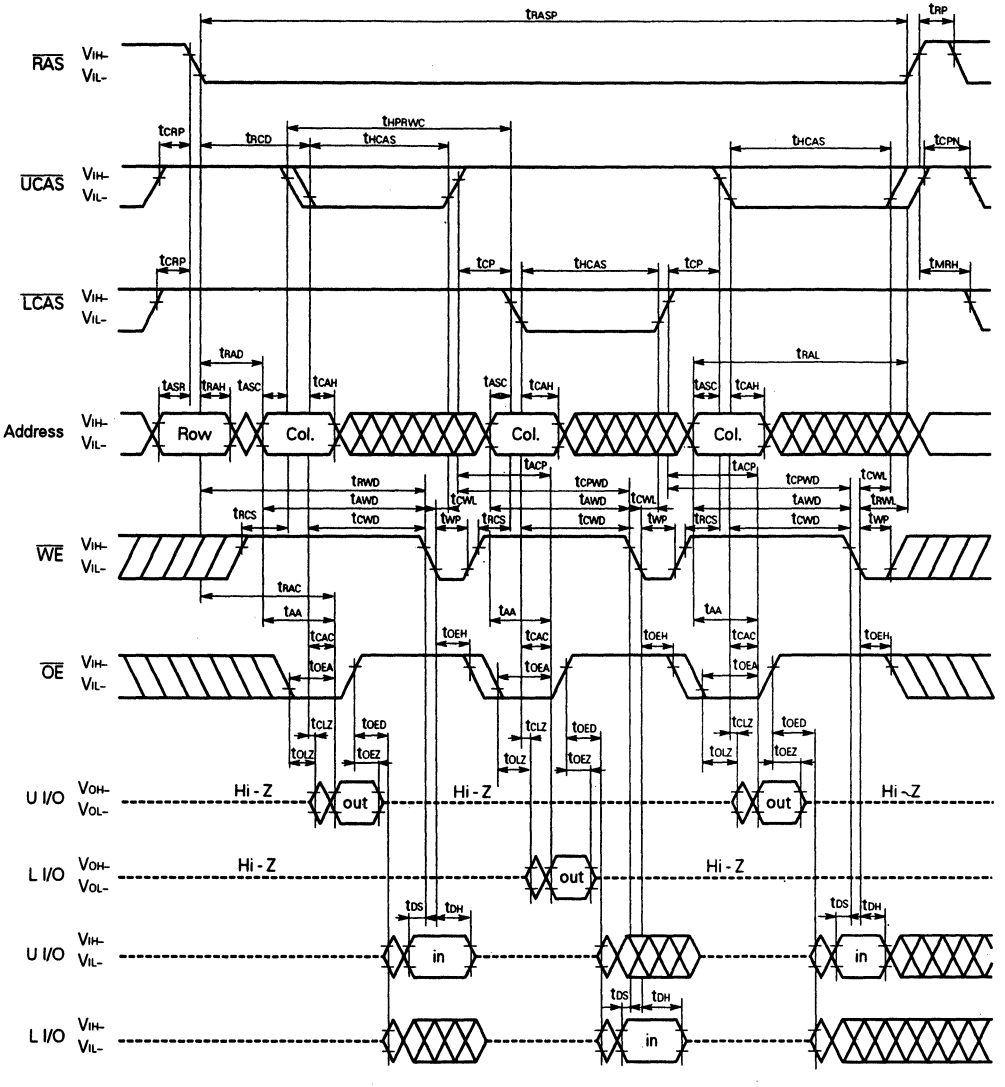
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode Read Modify Write Cycle



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

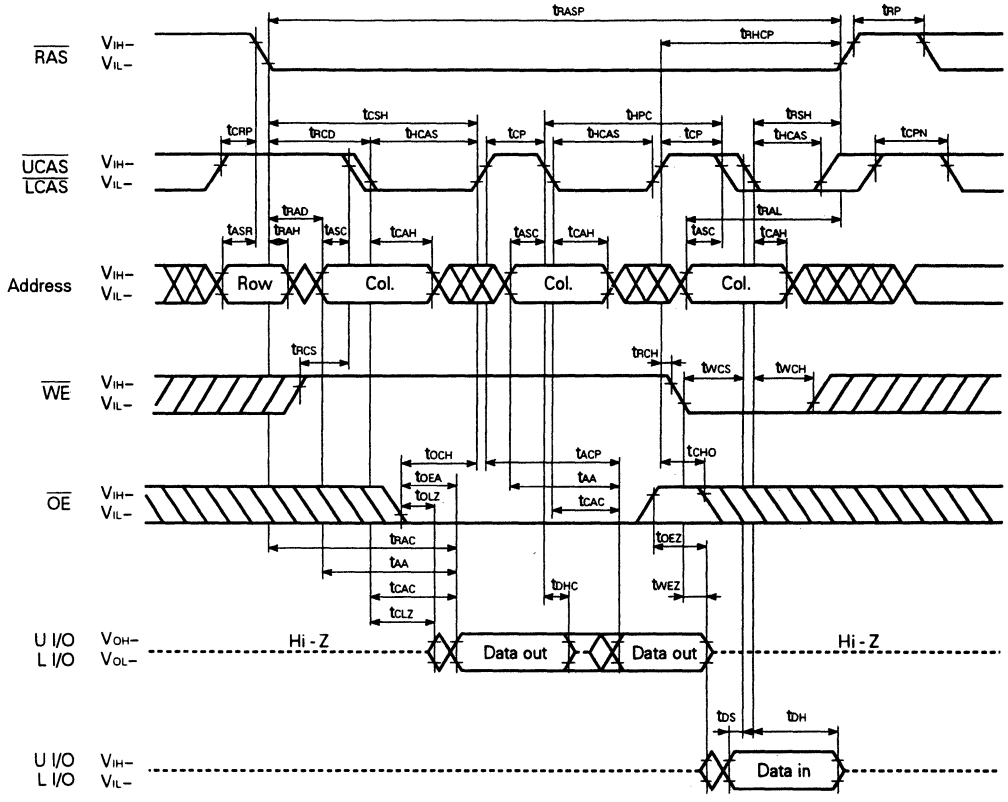
Hyper Page Mode Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

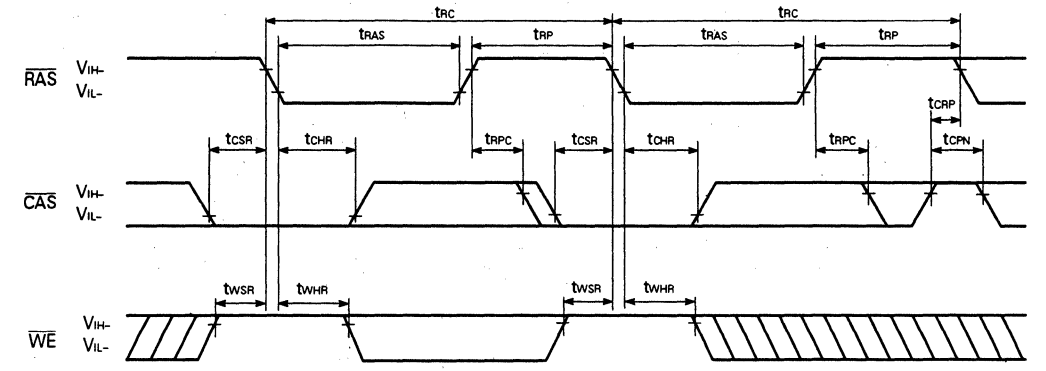
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode Read and Write Cycle



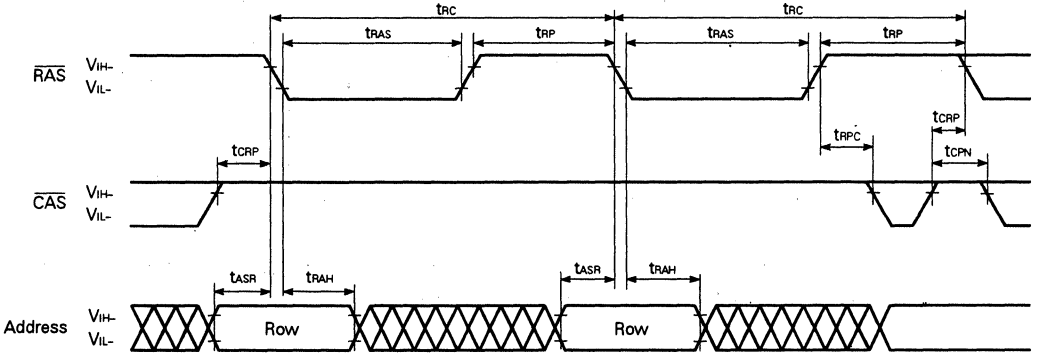
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



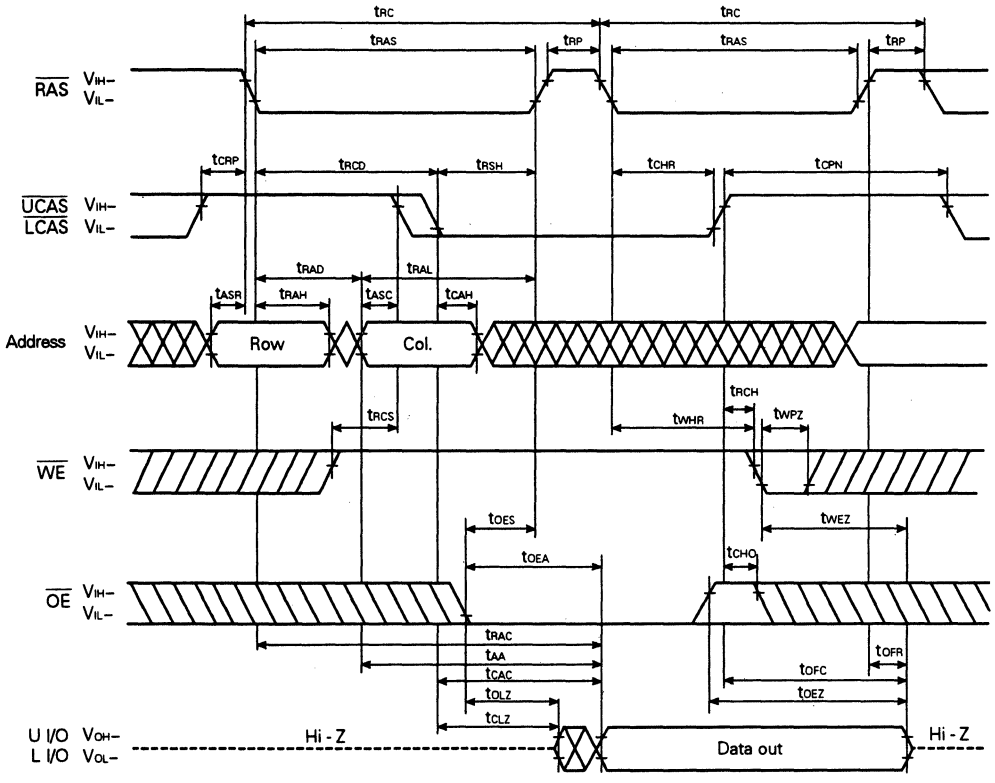
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

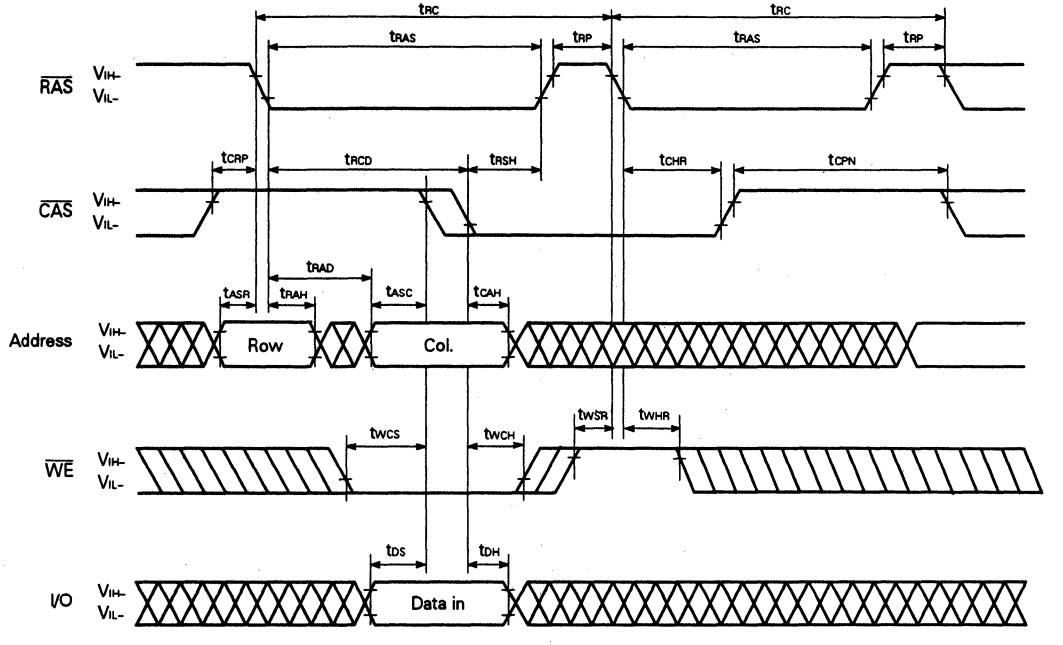


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



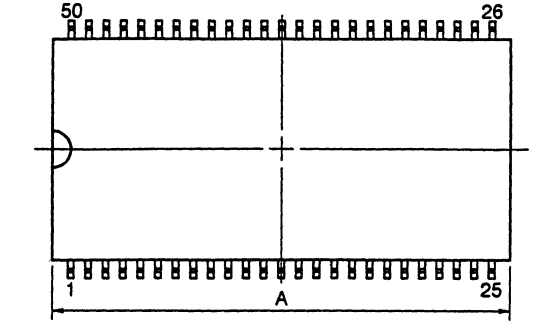
Hidden Refresh Cycle (Write)



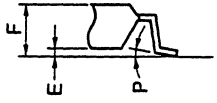
Remark $\overline{OE}$: Don't care

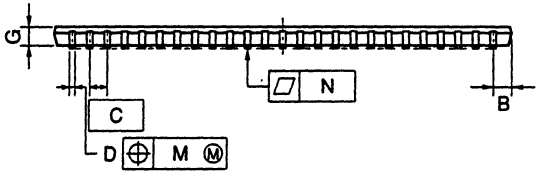
Package Drawings

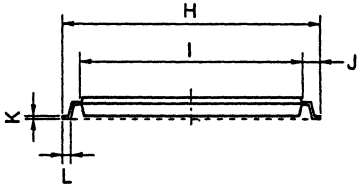
50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S16165L, 4216165L.

Types of Surface Mount Device

μPD4264165G5, 4265165G5: 50-pin plastic TSOP (II) (400 mil)

Hyper Page Mode (EDO)
16M Dynamic RAM
[5.0V ± 10%]

NEC

MOS INTEGRATED CIRCUIT

μPD42S16405, 4216405

16 M-BIT DYNAMIC RAM
4 M-WORD BY 4-BIT, HYPER PAGE MODE (EDO)

Description

The μPD42S16405, 4216405 are 4,194,304 words by 4 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S16405 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S16405, 4216405 are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 4 bits organization
- Single +5.0 V ±10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S16405-50, 4216405-50	550 mW	50 ns	84 ns	20 ns
μPD42S16405-60, 4216405-60	495 mW	60 ns	104 ns	25 ns
μPD42S16405-70, 4216405-70	440 mW	70 ns	124 ns	30 ns

- μPD42S16405 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

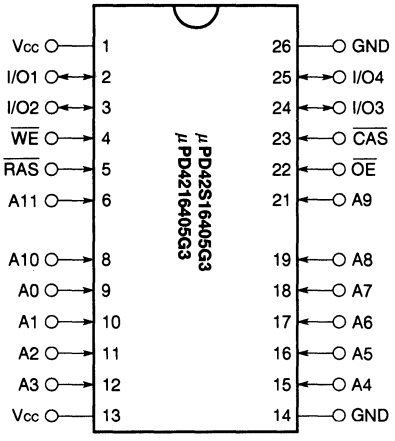
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16405	4,096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	1.4 mW (CMOS level input)
μPD4216405	4,096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

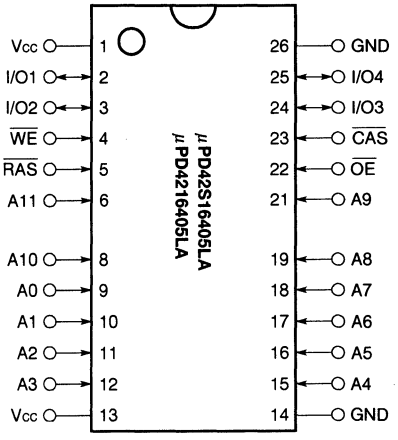
Part number	Access time (MAX.)	Package	Refresh
μPD42S16405G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S16405G3-60	60 ns		
μPD42S16405G3-70	70 ns		
μPD42S16405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD42S16405LA-60	60 ns		
μPD42S16405LA-70	70 ns		
μPD4216405G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4216405G3-60	60 ns		
μPD4216405G3-70	70 ns		
μPD4216405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD4216405LA-60	60 ns		
μPD4216405LA-70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

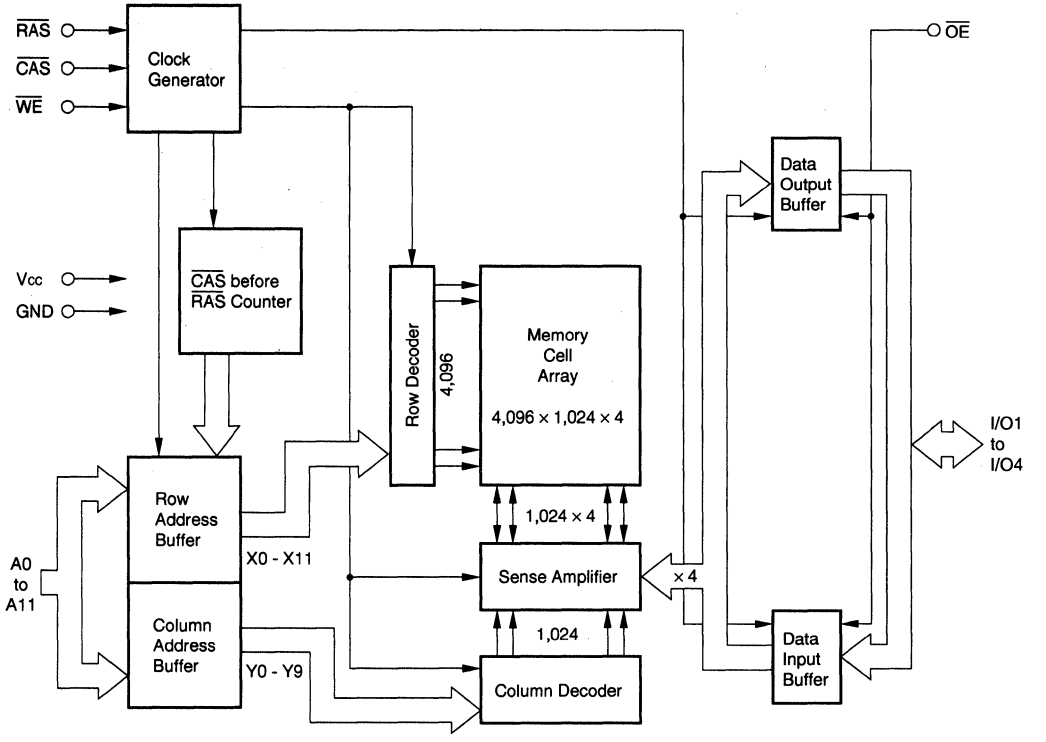


26-pin Plastic SOJ (300 mil)



A0 to A11 : Address Inputs
I/O1 to I/O4: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD42S16405, 4216405 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 12-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

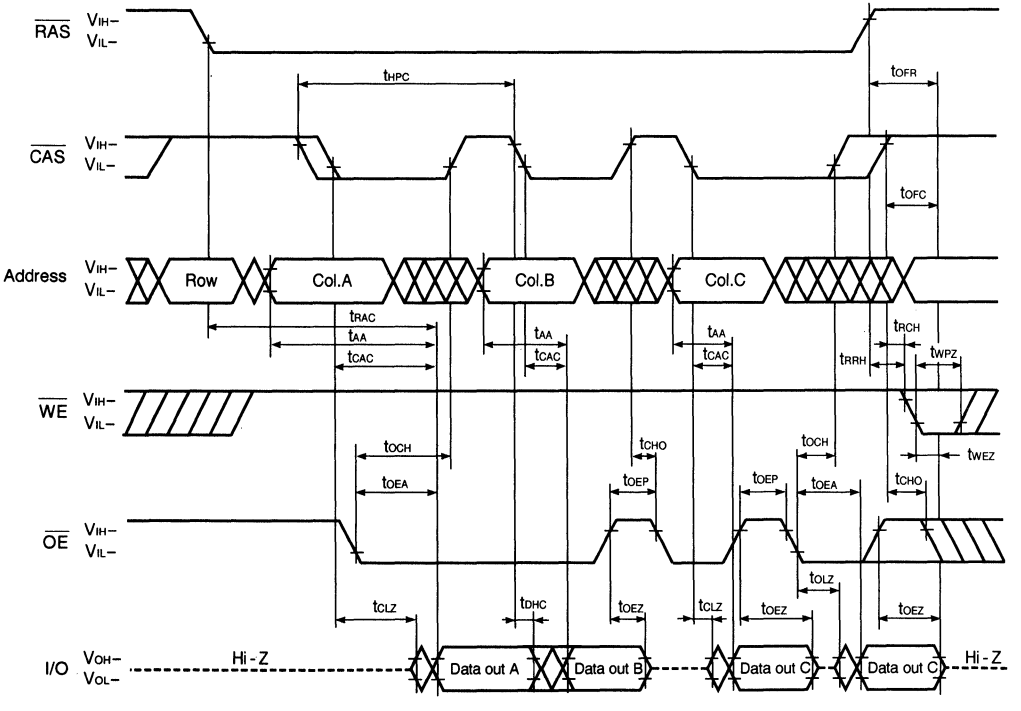
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 3
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
Standby current	μPD42S16405	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.25		
	μPD4216405		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 3, 4
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 5
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16405)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V	$t_{RAS} \leq$ 300 ns		450	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq$ 1 μs		600	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16405)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

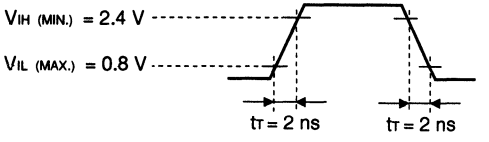
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

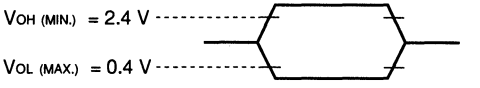
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

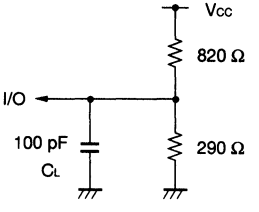
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	84	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time		tRP	30	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	7	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	50	10,000	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	7	10,000	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		tRSH	10	–	10	–	12	–	ns	
$\overline{CAS}$ hold time		tCSH	38	–	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	11	37	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	9	25	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	ns	
Row address hold time		tRAH	7	–	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	ns	
Column address hold time		tCAH	7	–	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	10	–	13	–	15	–	ns	
Transition time (rise and fall)		tT	1	50	1	50	1	50	ns	
Refresh time	μPD42S16405	tREF	–	128	–	128	–	128	ms	4
	μPD4216405		–	64	–	64	–	64		

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16405.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	7	–	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	7	–	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	7	–	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	7	–	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	107	–	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	64	–	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	20	–	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	7	10,000	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	41	–	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	52	–	66	–	75	–	ns	
Data output hold Time	t_{DHC}	5	–	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	7	–	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

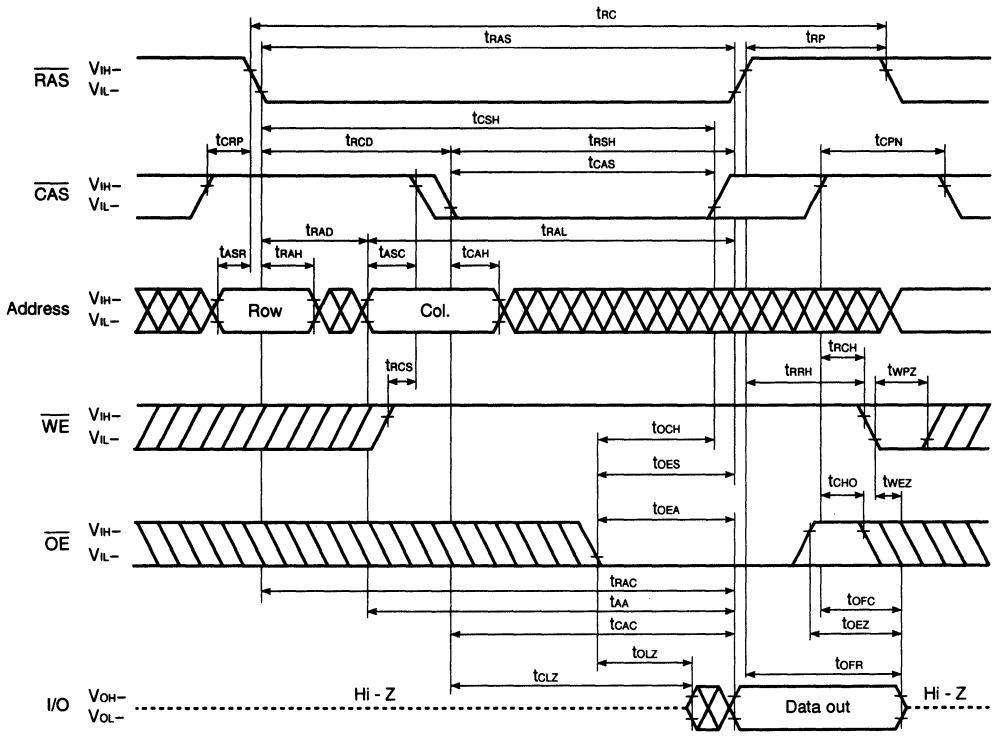
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

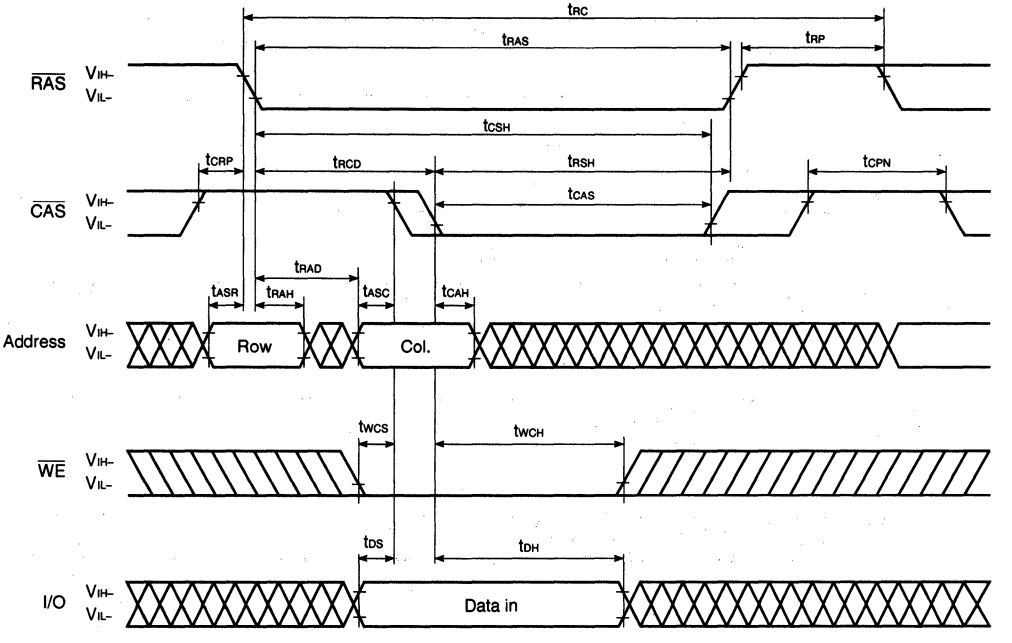
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	90	–	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16405.

Read Cycle

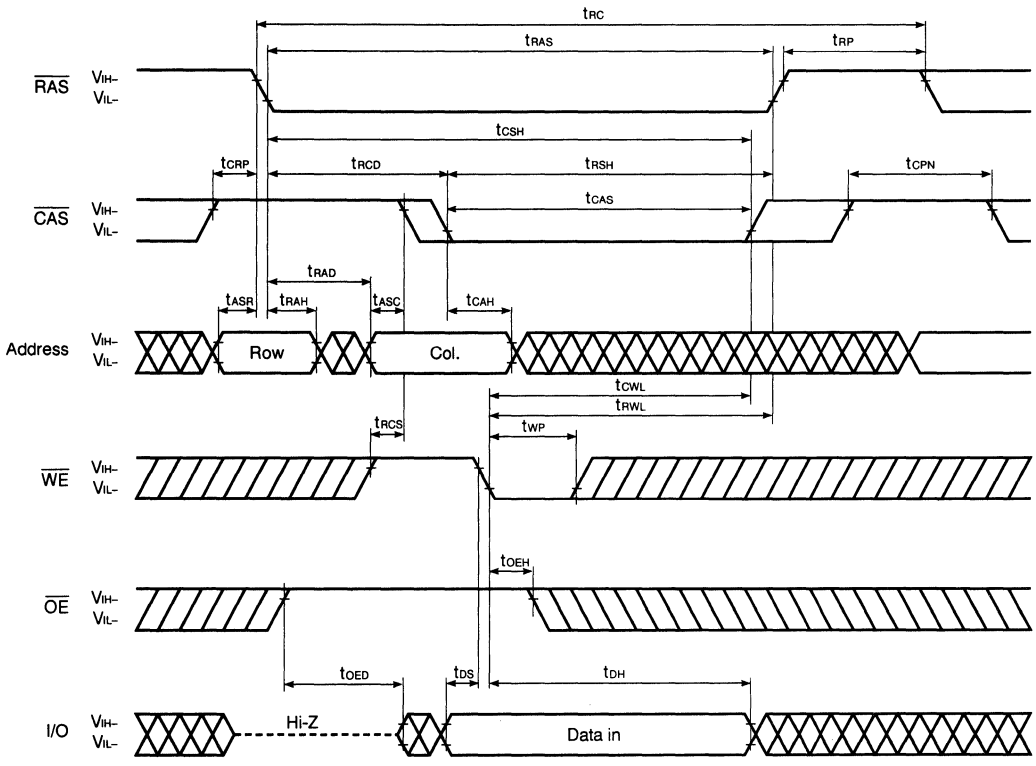

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tOEZ
tCAC
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

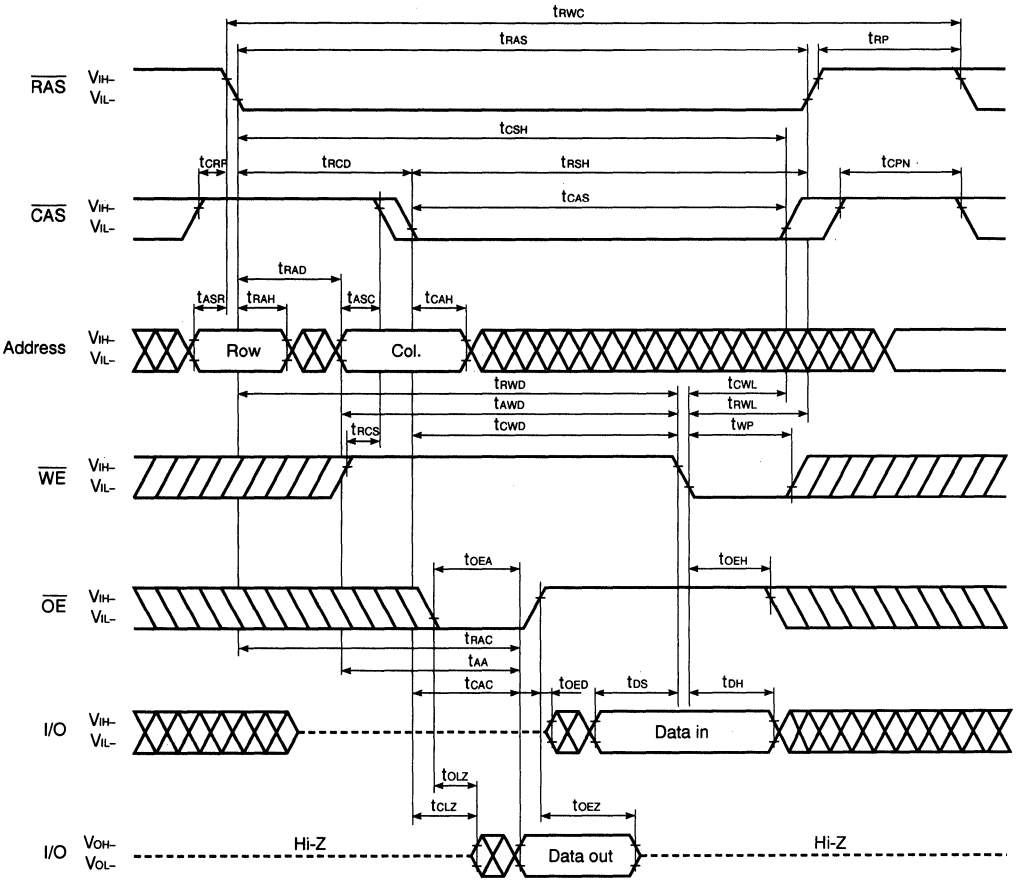


Remark $\overline{OE}$: Don't care

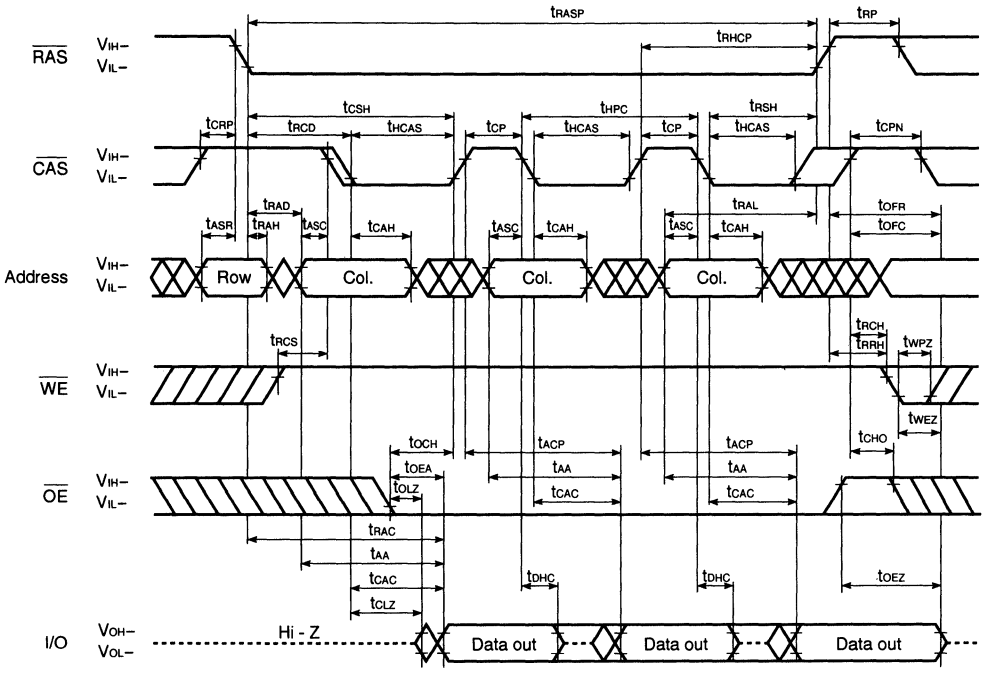
Late Write Cycle



Read Modify Write Cycle

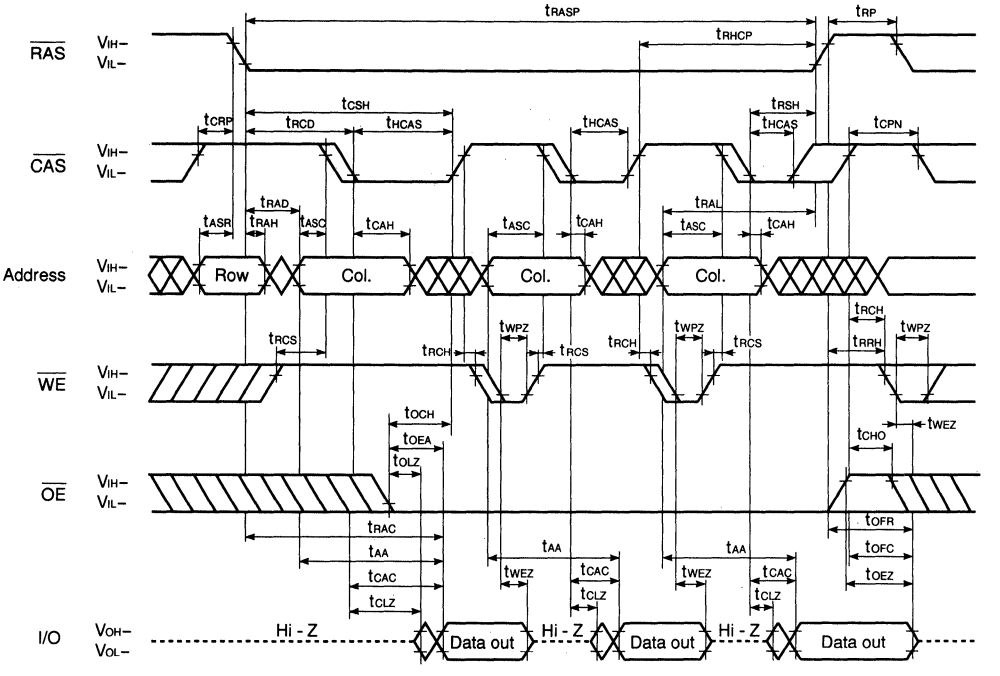


Hyper Page Mode (EDO) Read Cycle



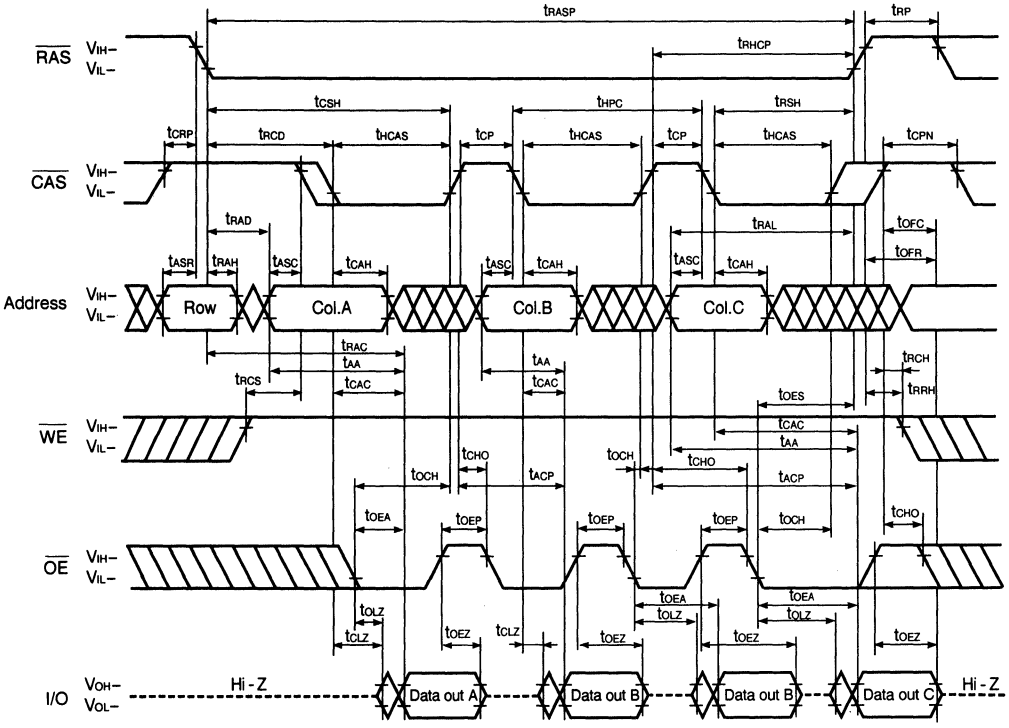
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



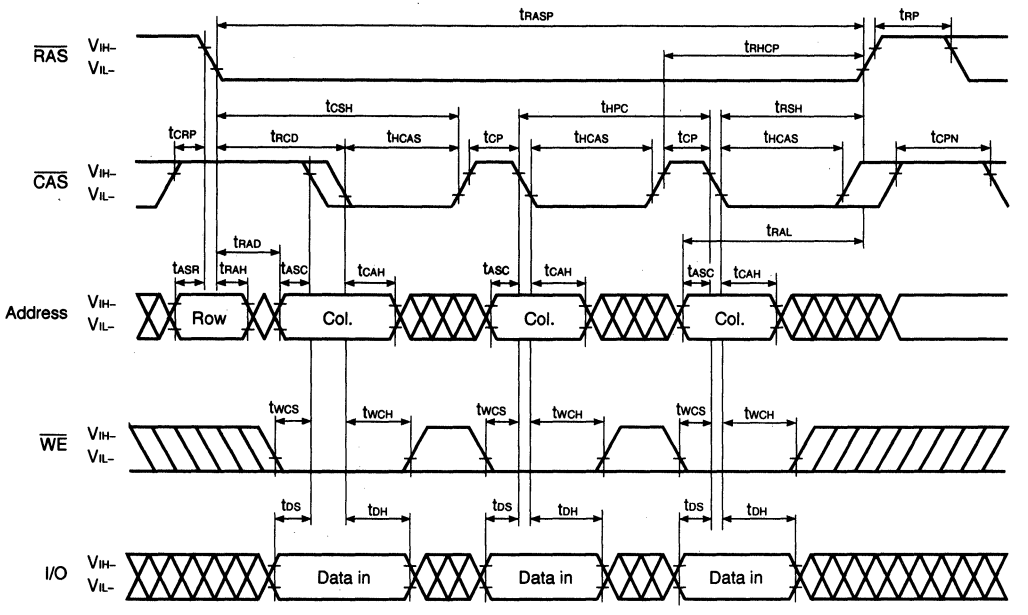
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

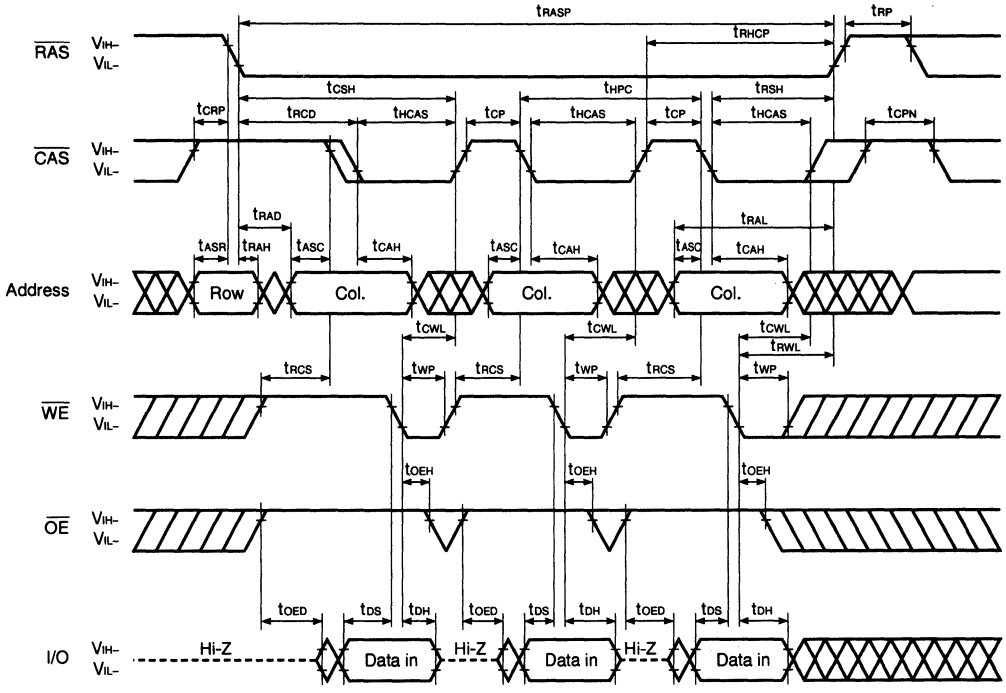
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

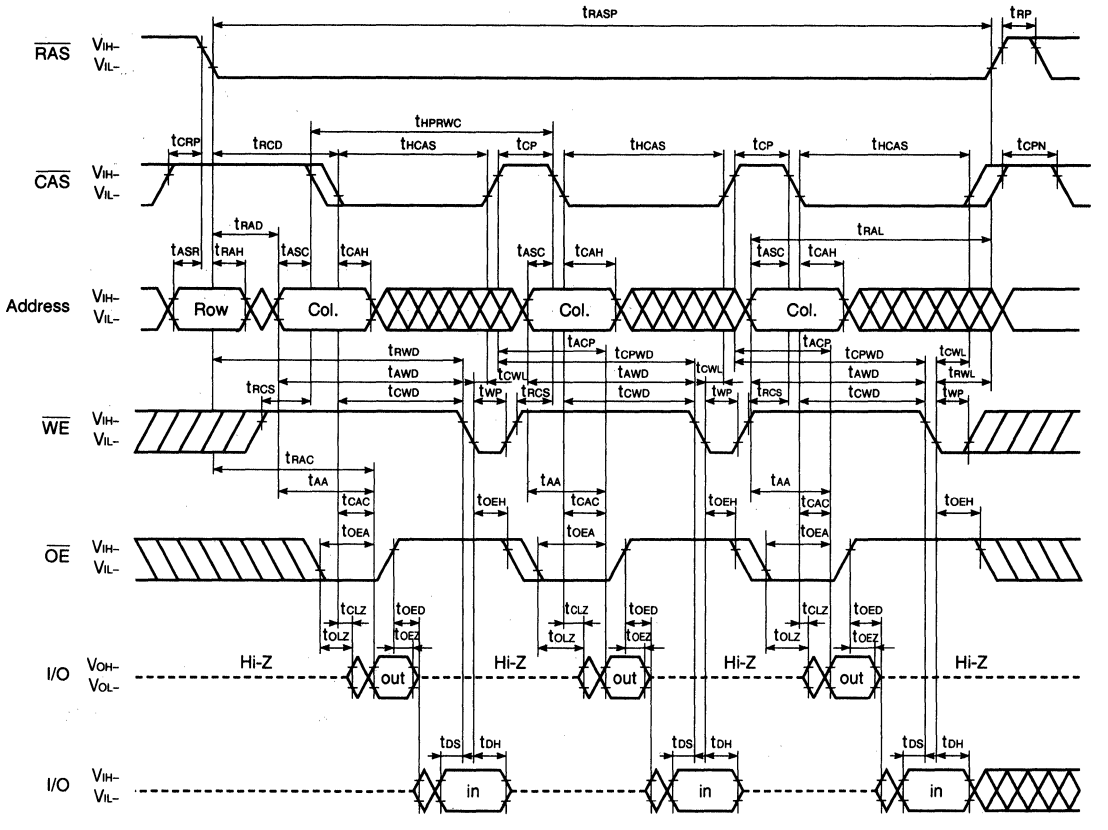
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



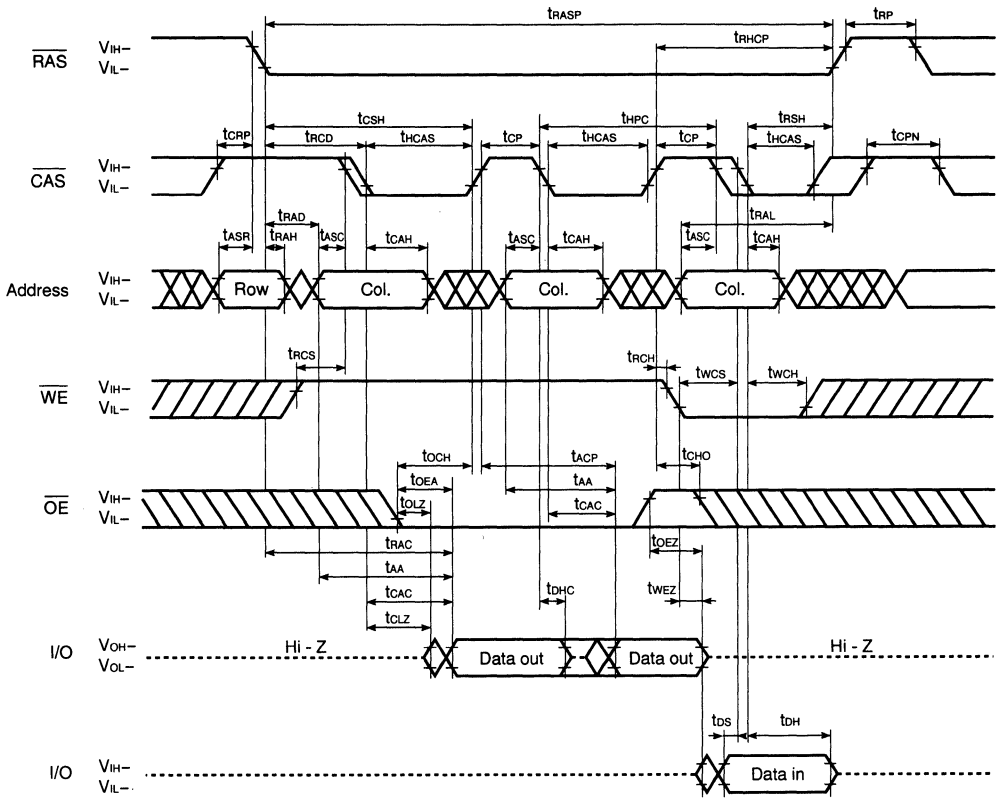
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



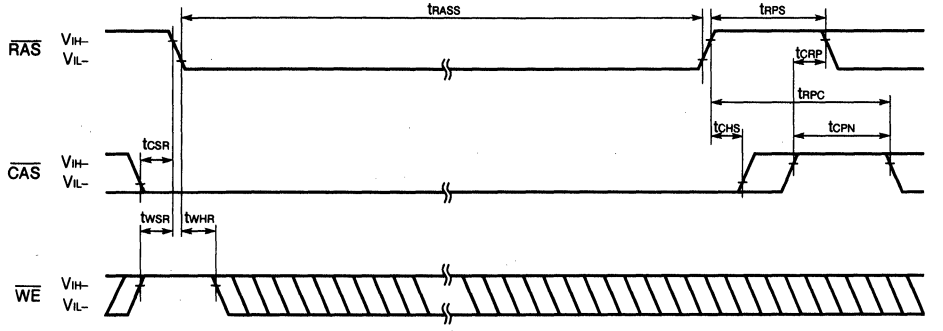
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16405)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

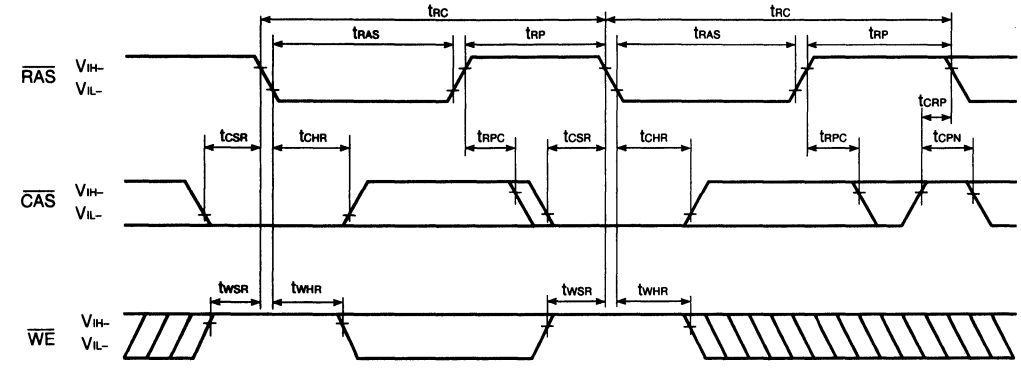
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

★ **(3)** If $t_{RASS(MIN.)}$ is not saisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (4,096/128 ms) should be met.

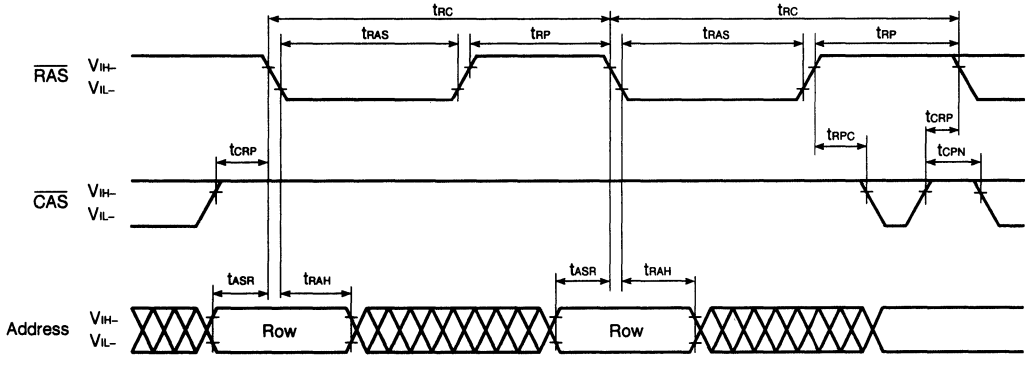
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



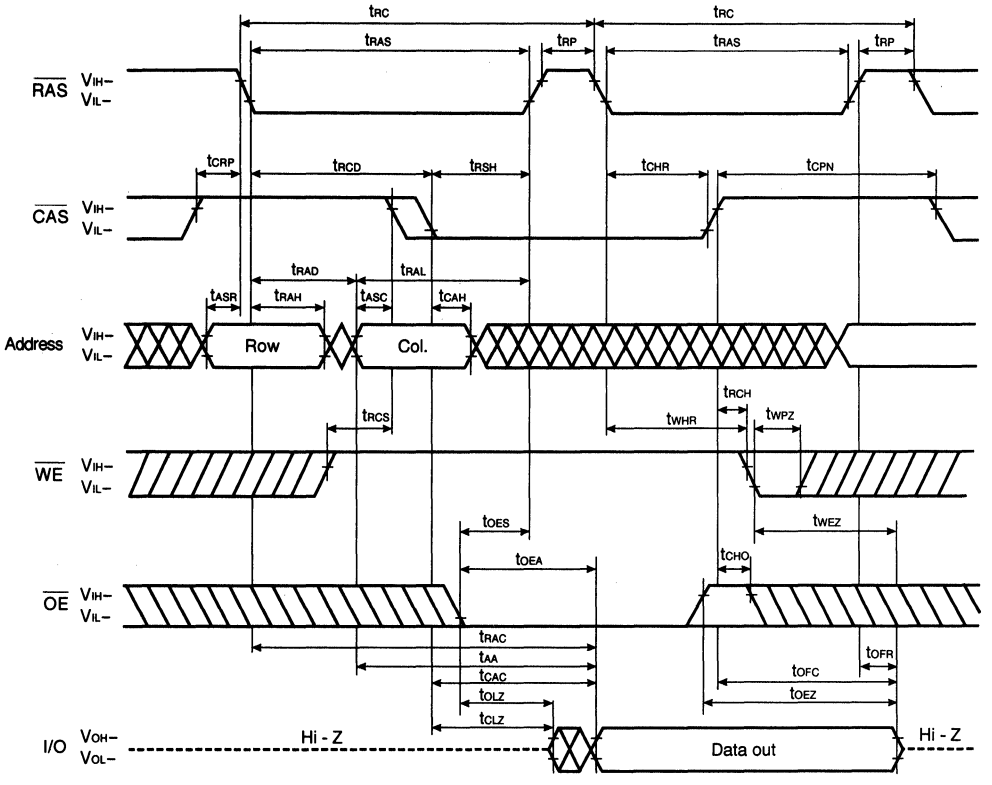
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

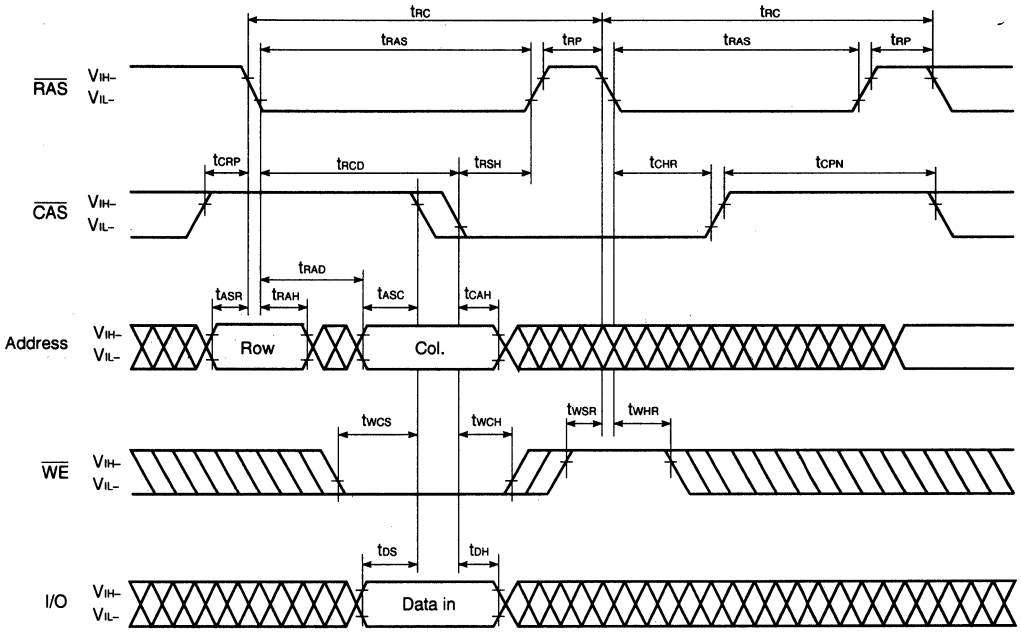


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

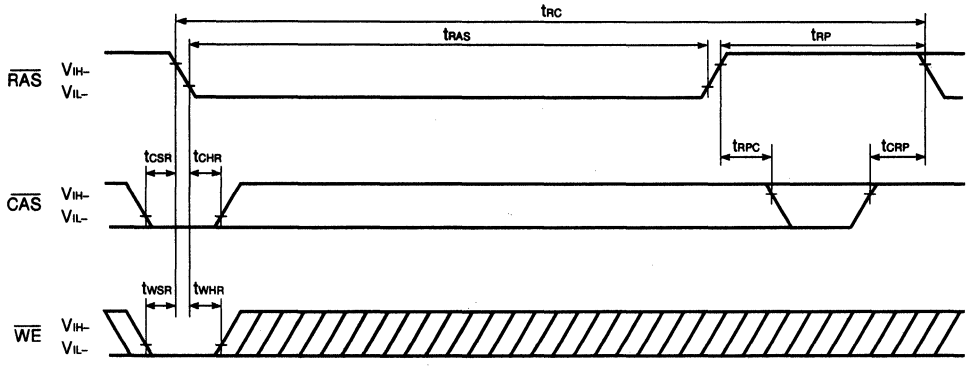


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

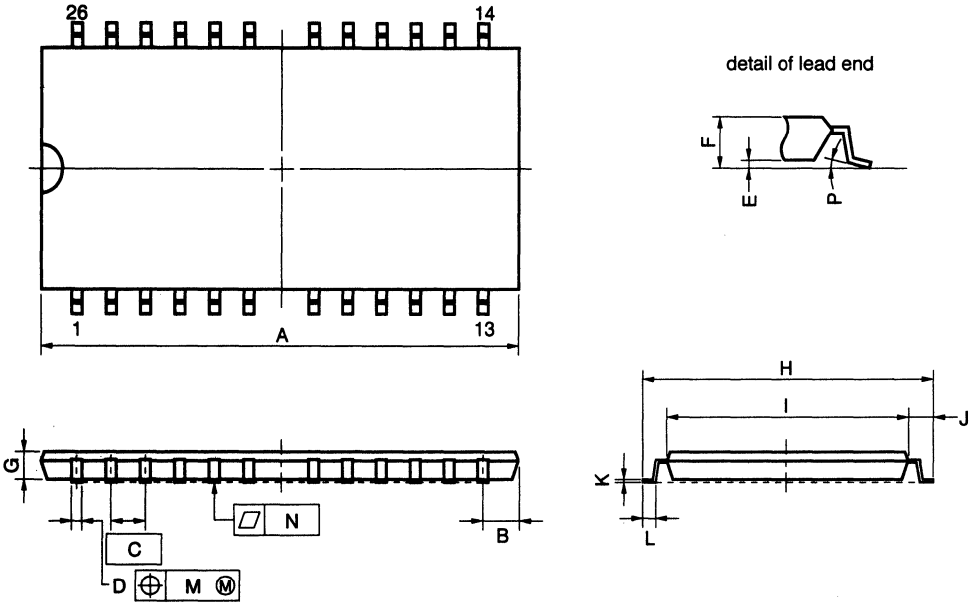
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



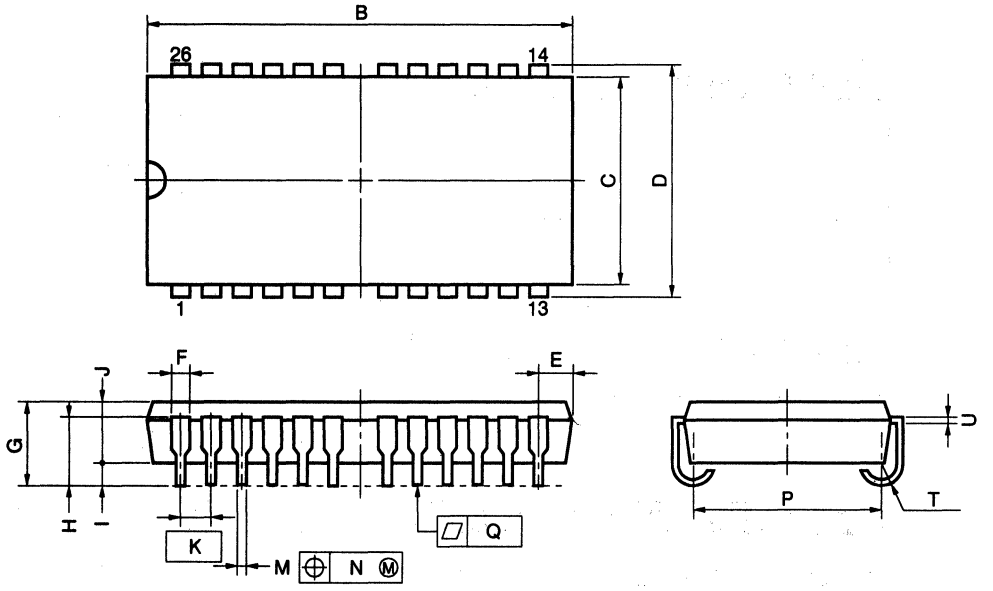
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	3^{+7}_{-3}	3^{+7}_{-3}

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16405, 4216405.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16405G3, 4216405G3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16405LA, 4216405LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S17405, 4217405

16 M-BIT DYNAMIC RAM
4 M-WORD BY 4-BIT, HYPER PAGE MODE (EDO)

Description

The μPD42S17405, 4217405 are 4,194,304 words by 4 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S17405 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S17405, 4217405 are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 4 bits organization
- Single +5.0 V ±10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S17405-50, 4217405-50	660 mW	50 ns	84 ns	20 ns
μPD42S17405-60, 4217405-60	605 mW	60 ns	104 ns	25 ns
μPD42S17405-70, 4217405-70	550 mW	70 ns	124 ns	30 ns

- μPD42S17405 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

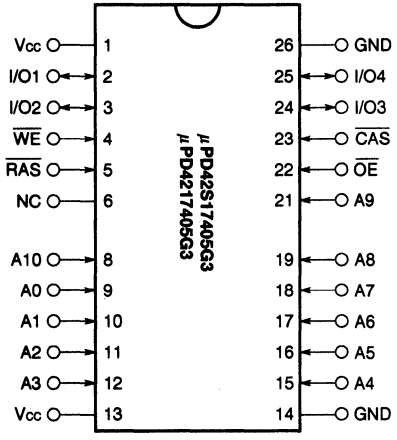
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17405	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	1.4 mW (CMOS level input)
μPD4217405	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

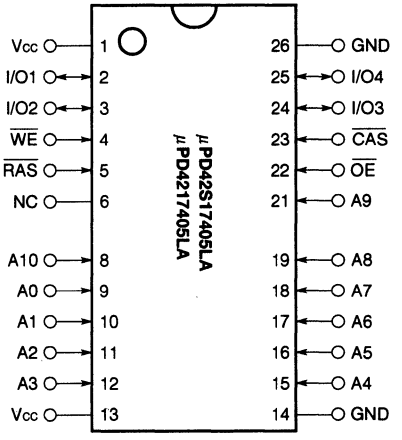
Part number	Access time (MAX.)	Package	Refresh
μPD42S17405G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17405G3-60	60 ns		
μPD42S17405G3-70	70 ns		
μPD42S17405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD42S17405LA-60	60 ns		
μPD42S17405LA-70	70 ns		
μPD4217405G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217405G3-60	60 ns		
μPD4217405G3-70	70 ns		
μPD4217405LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD4217405LA-60	60 ns		
μPD4217405LA-70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

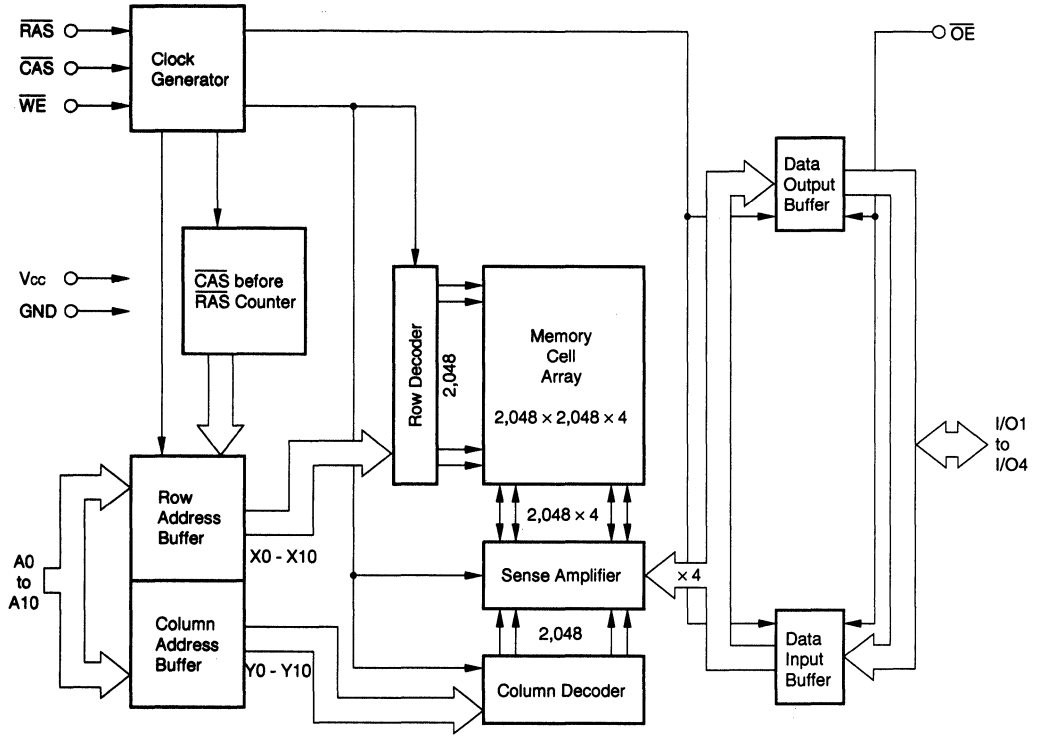


26-pin Plastic SOJ (300 mil)



A0 to A10 : Address Inputs
I/O1 to I/O4: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17405, 4217405 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A10 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 11-bit and lower 11-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

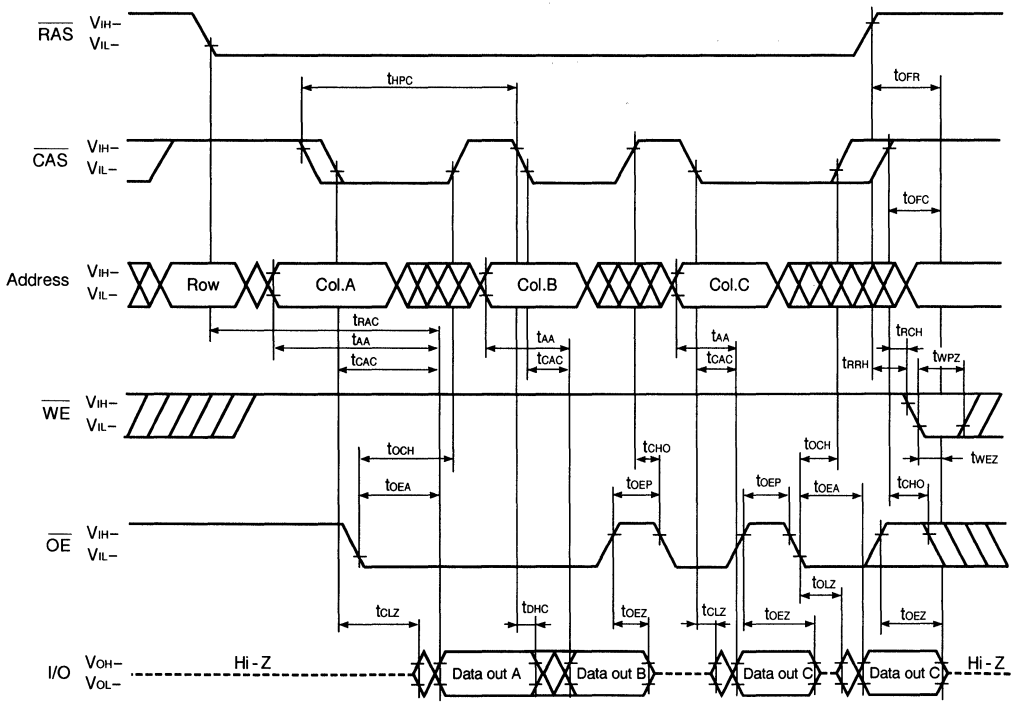
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO) , read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to HI-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2, 3
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Standby current	μPD42S17405	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.25		
	μPD4217405		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2, 3, 4
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 5
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17405)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V	$t_{RAS} \leq 300$ ns		400	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		500	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17405)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

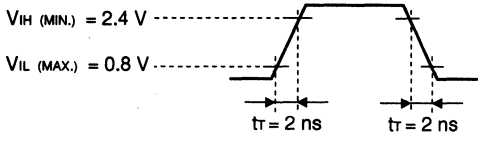
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

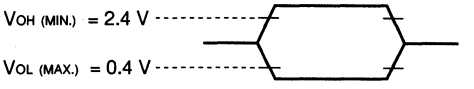
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

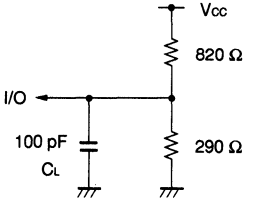
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	84	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time		tRP	30	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	7	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	50	10,000	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	7	10,000	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		tRSH	10	–	10	–	12	–	ns	
$\overline{CAS}$ hold time		tCSH	38	–	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	11	37	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	9	25	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	ns	
Row address hold time		tRAH	7	–	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	ns	
Column address hold time		tCAH	7	–	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	10	–	13	–	15	–	ns	
Transition time (rise and fall)		tT	1	50	1	50	1	50	ns	
Refresh time	μPD42S17405	tREF	–	128	–	128	–	128	ms	4
	μPD4217405		–	32	–	32	–	32		

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S17405.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	7	–	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	7	–	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	7	–	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	7	–	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	107	–	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	64	–	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	20	–	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	7	10,000	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	41	–	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	52	–	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	7	–	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

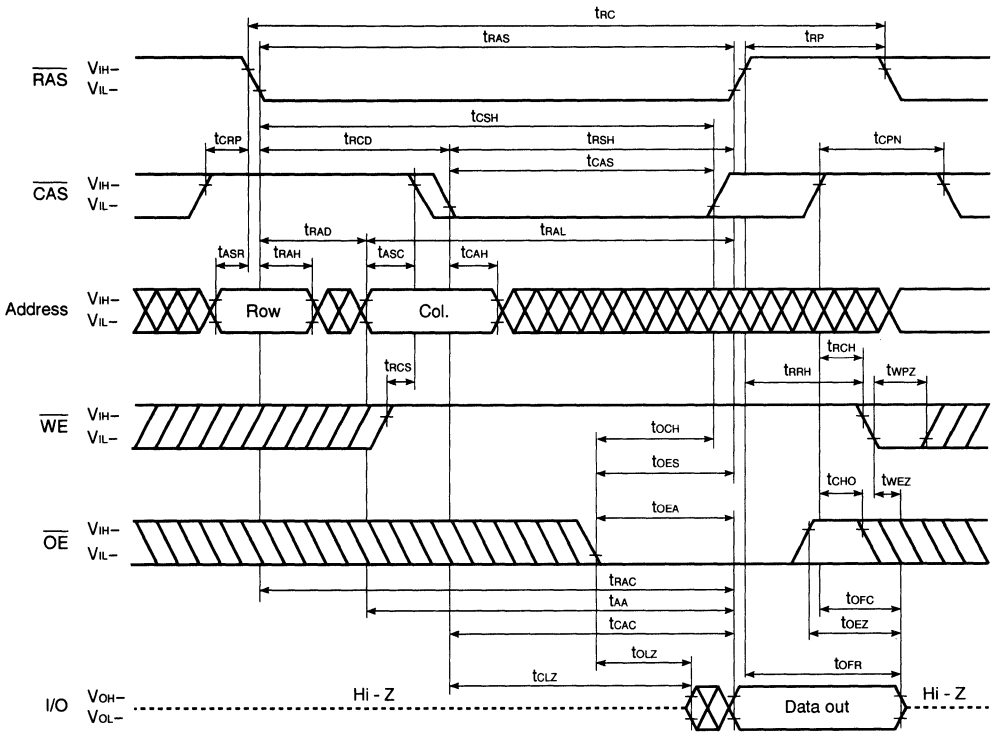
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

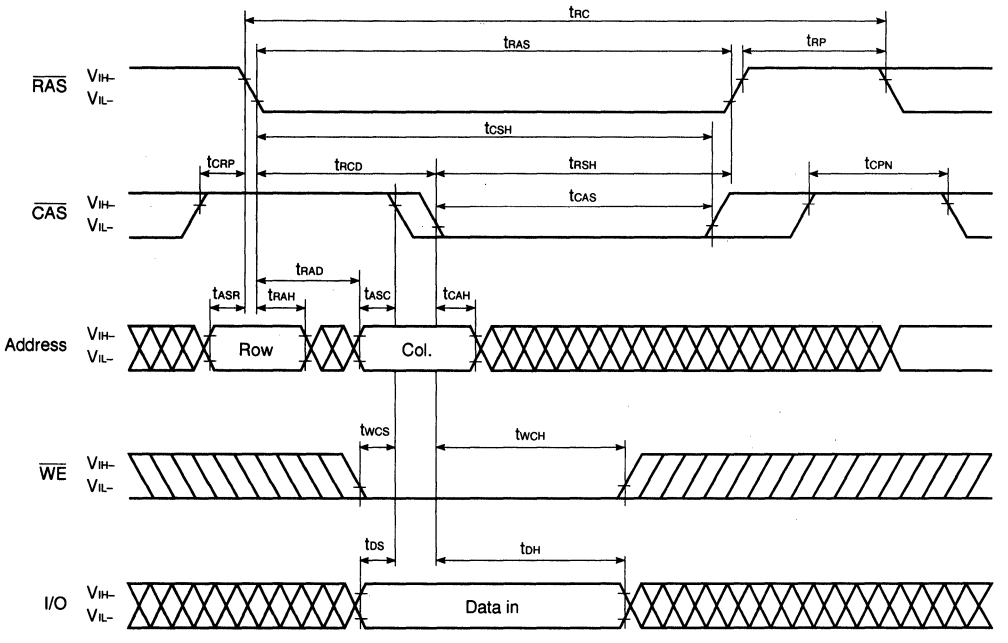
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	90	–	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17405.

Read Cycle

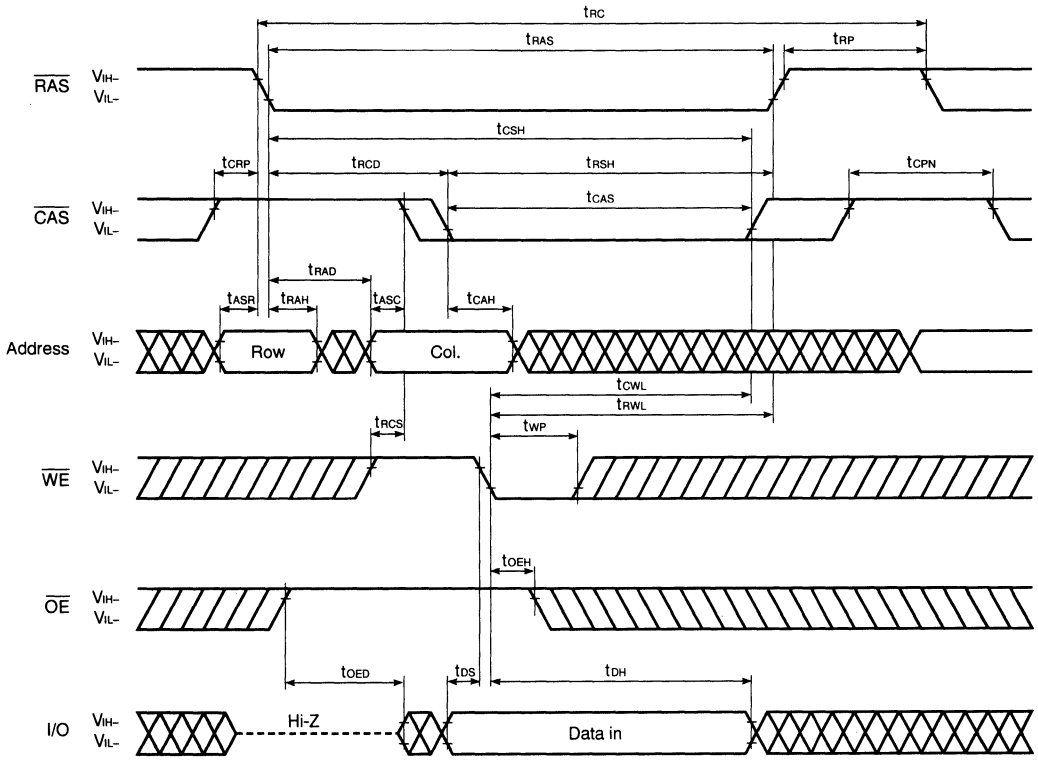

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

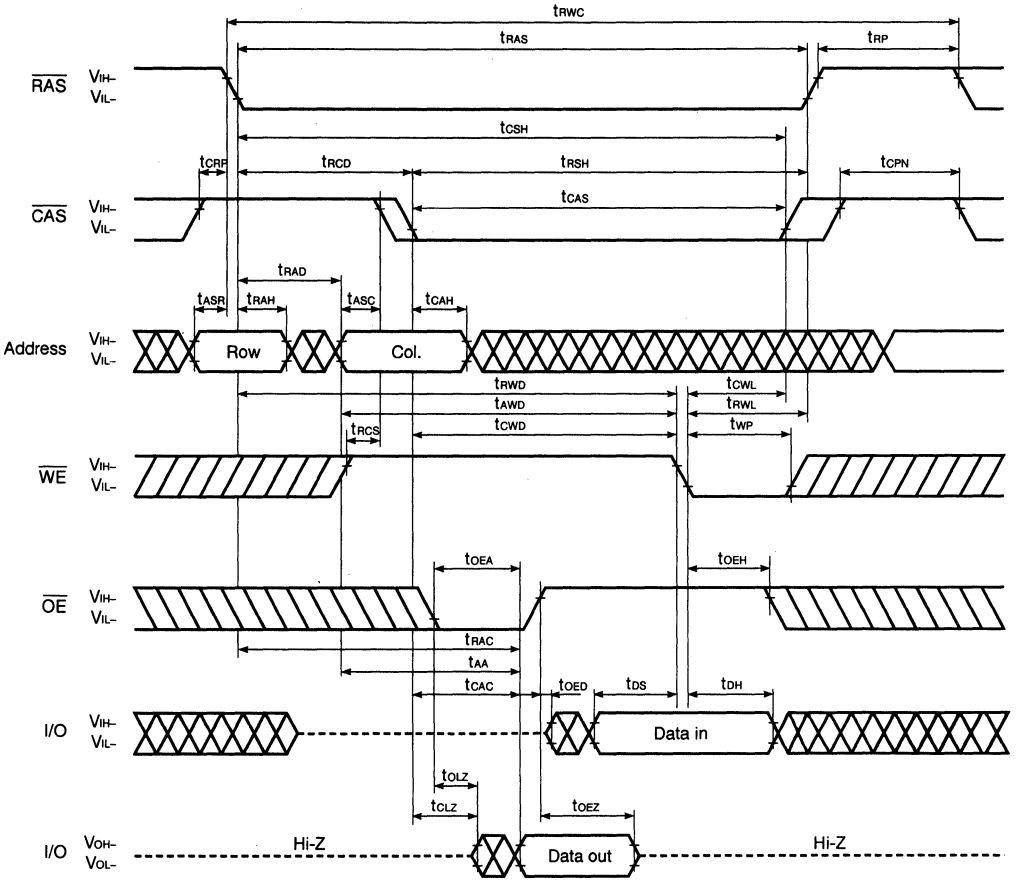


Remark $\overline{OE}$: Don't care

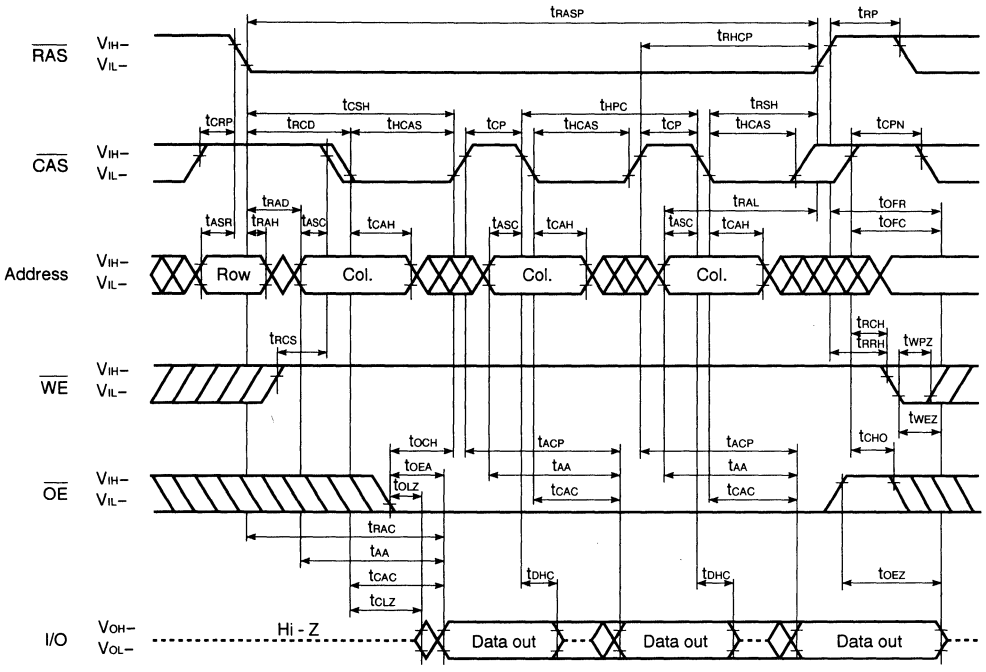
Late Write Cycle



Read Modify Write Cycle

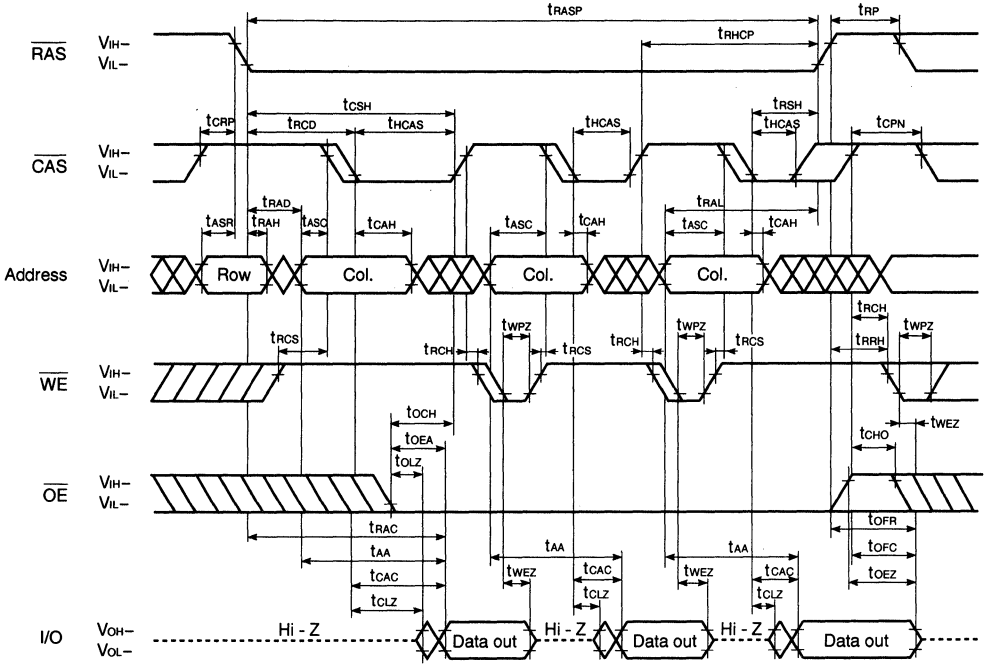


Hyper Page Mode (EDO) Read Cycle



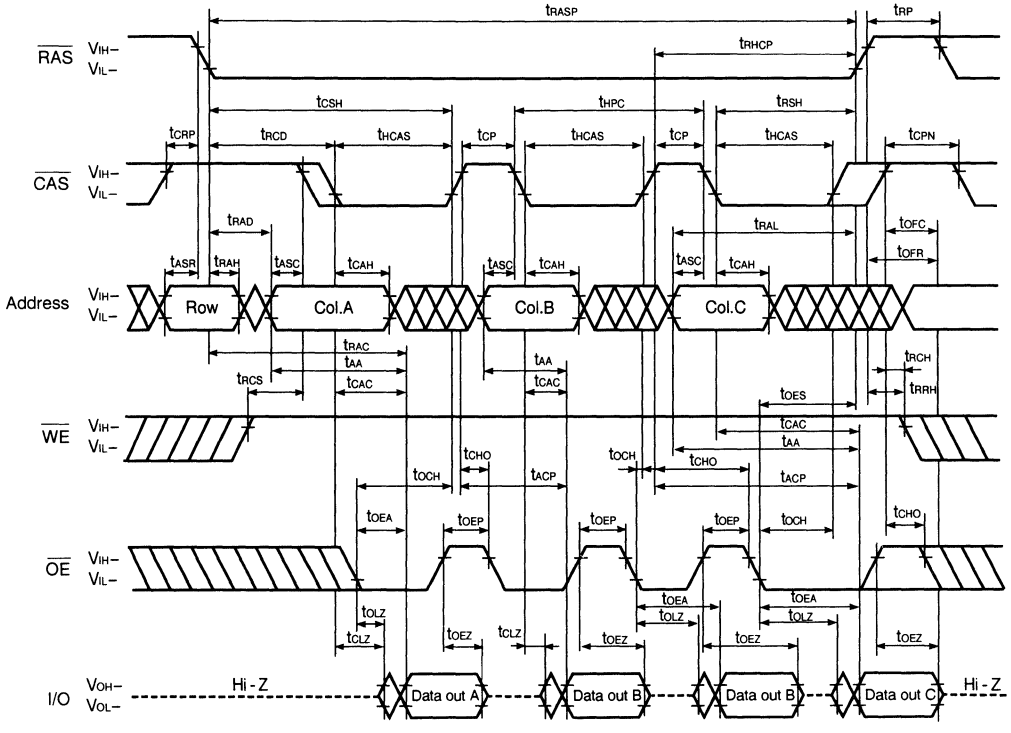
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



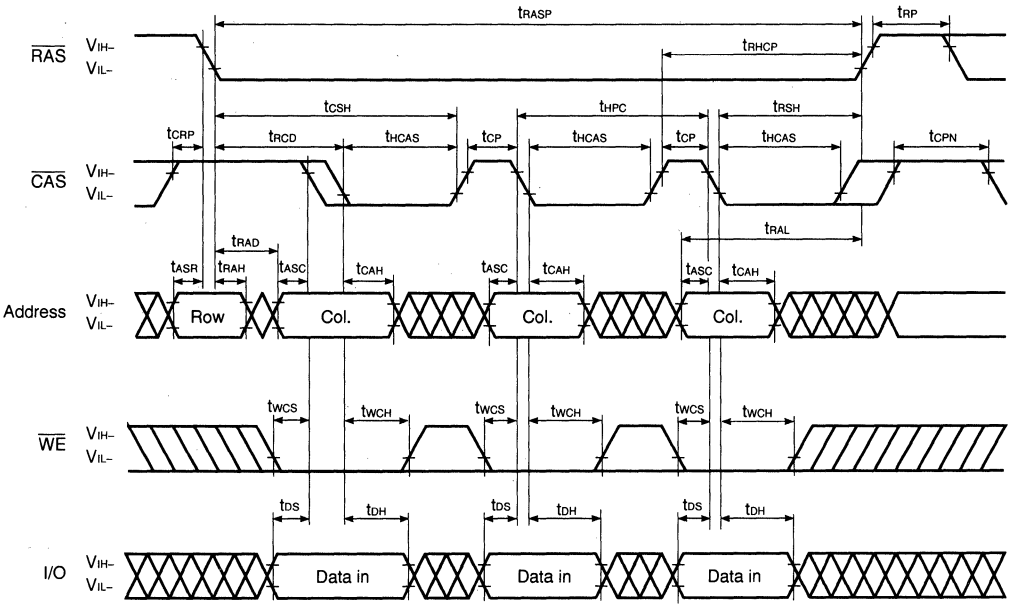
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

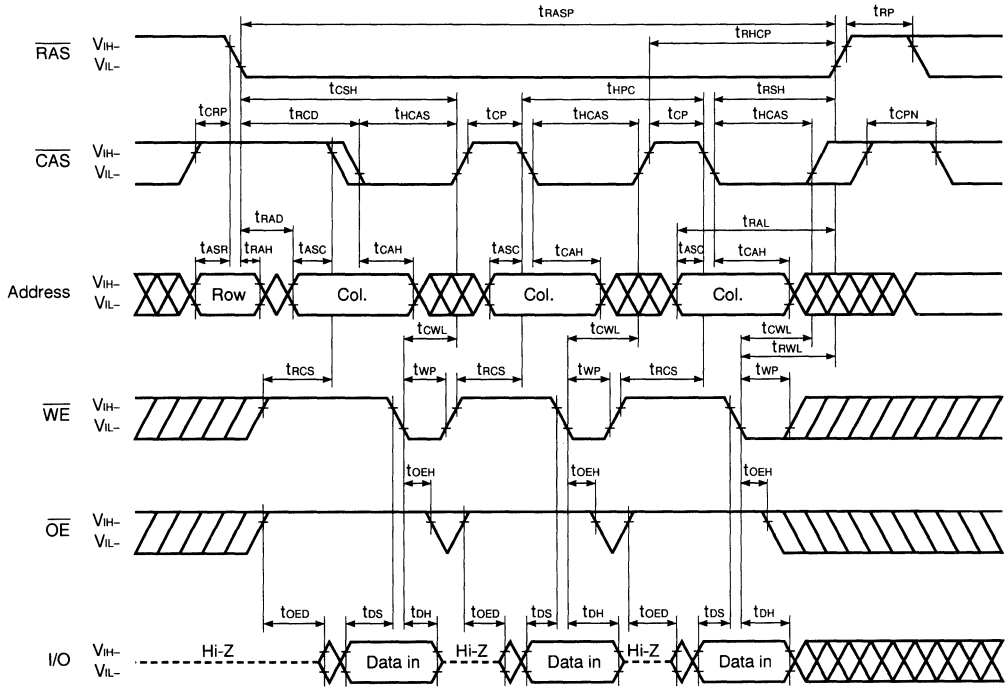
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

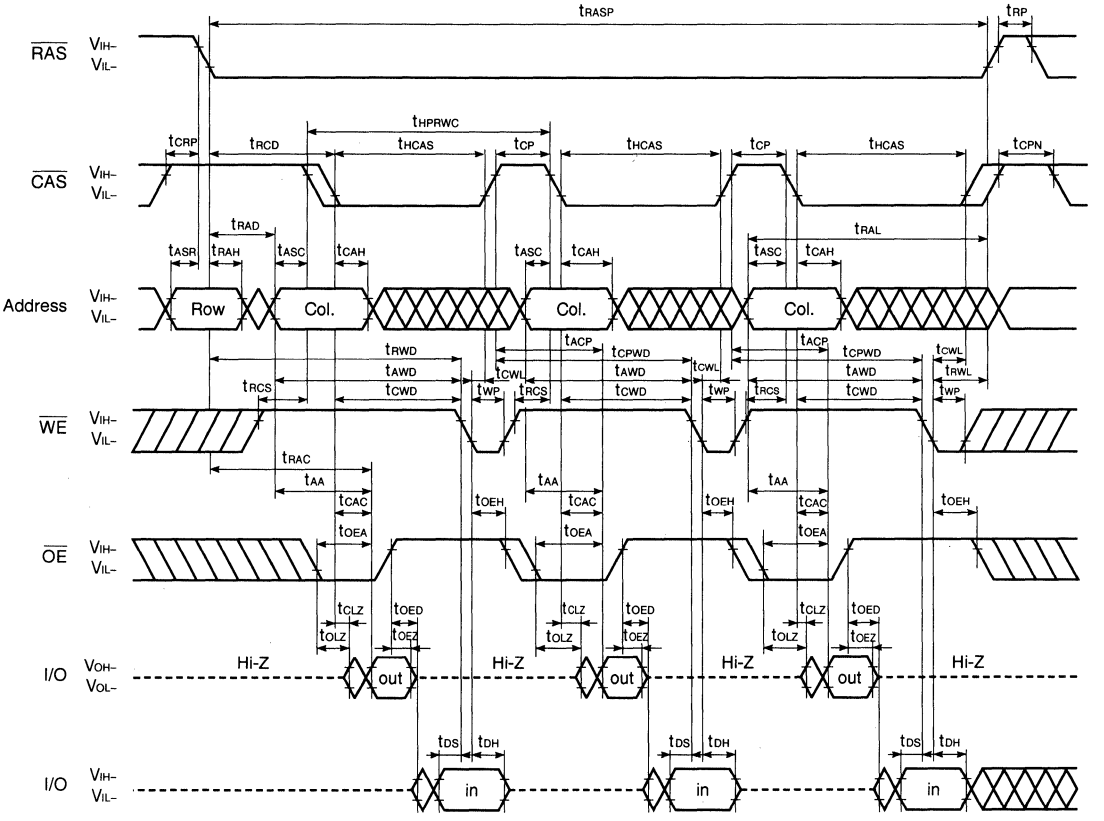
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



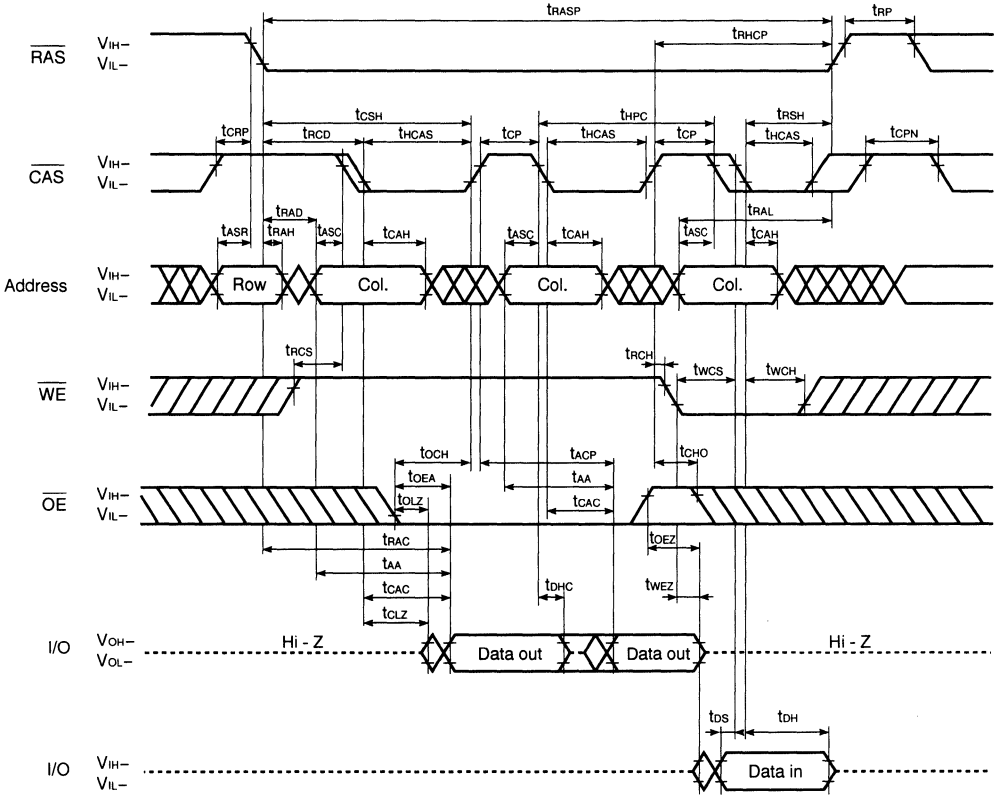
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



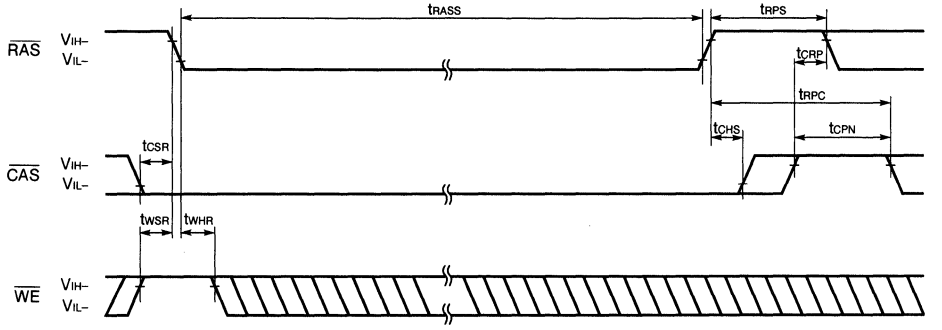
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17405)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

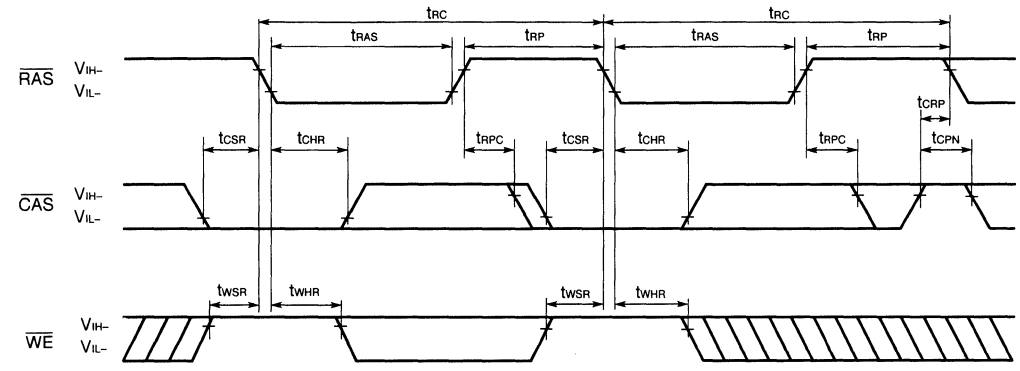
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (2,048/128 ms) should be met.

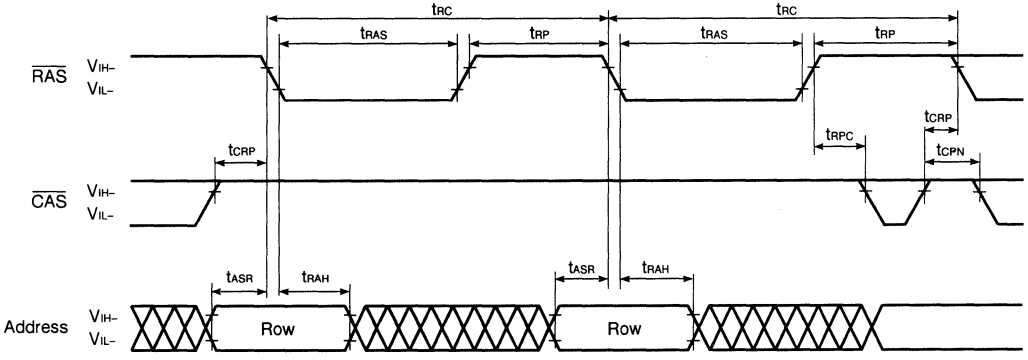
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



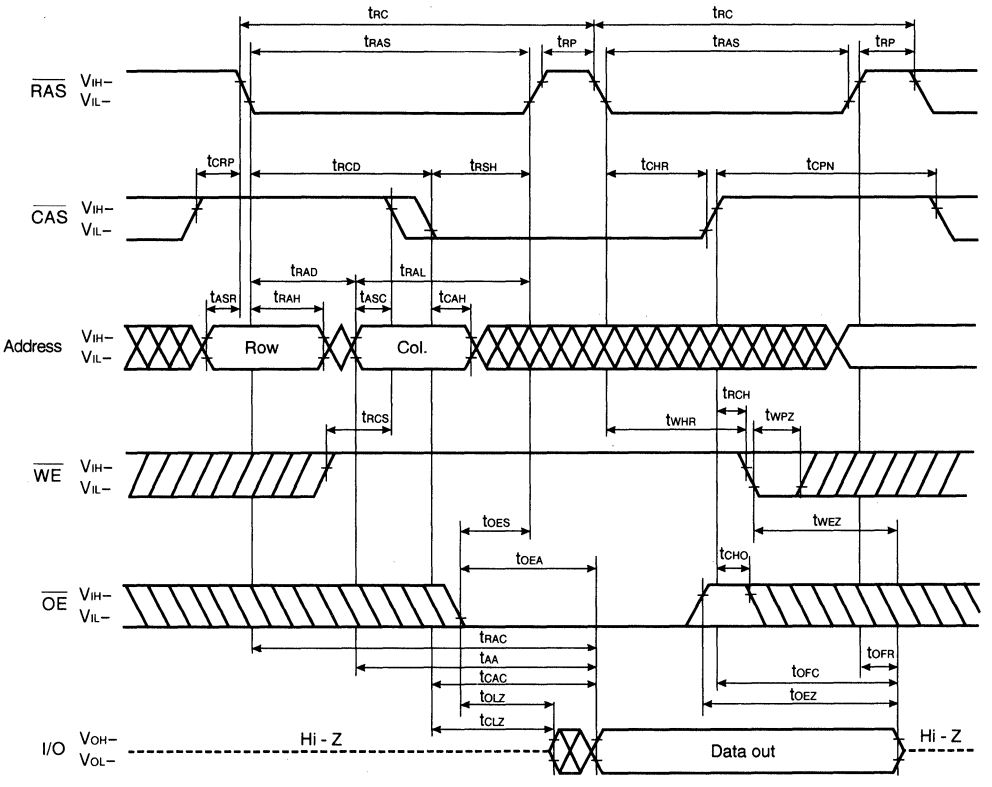
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

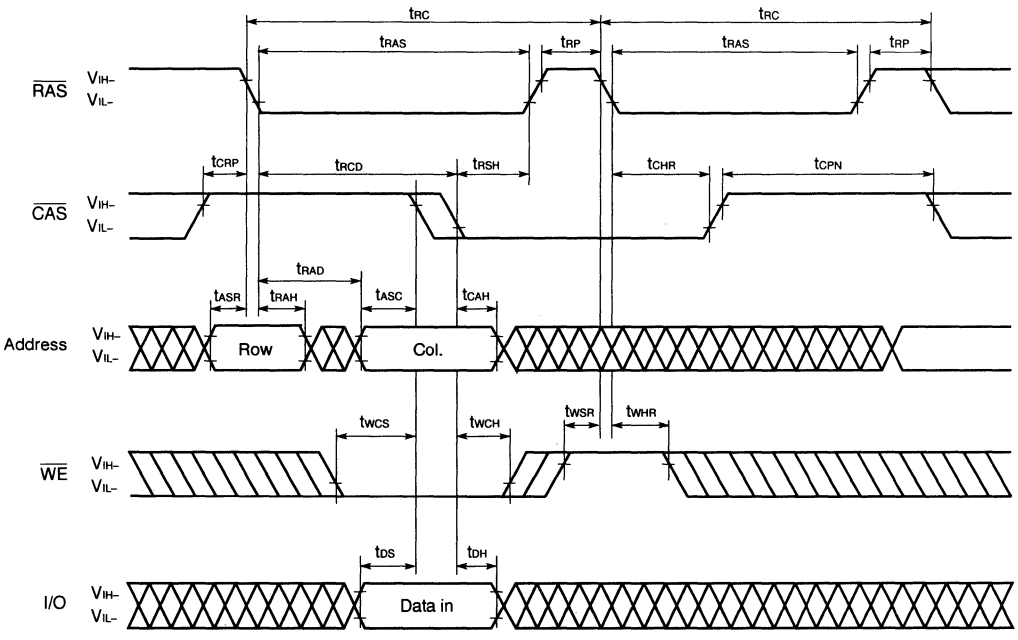


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

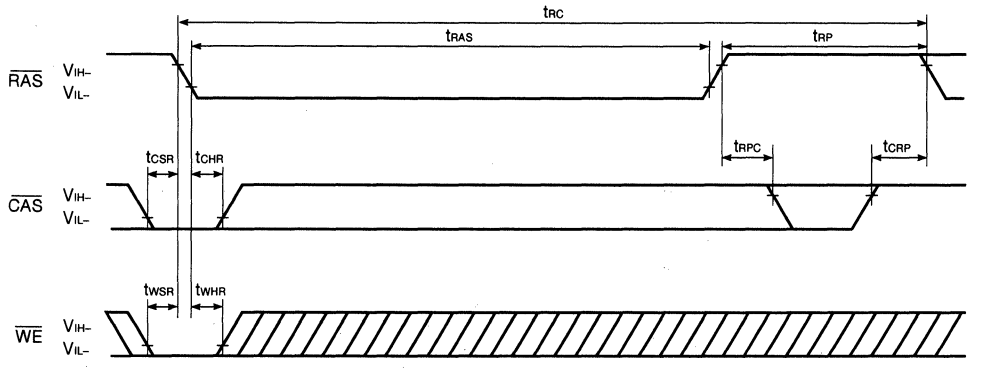


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

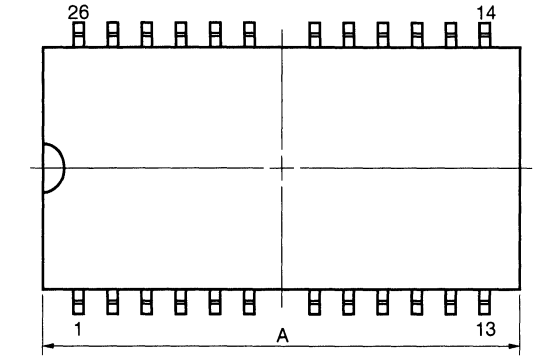
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

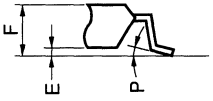
The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

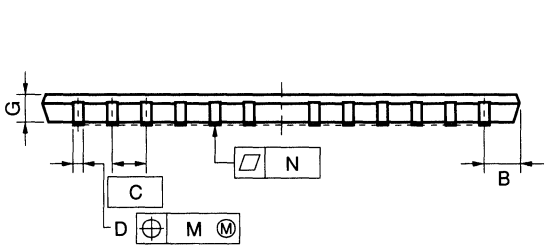
Package Drawings

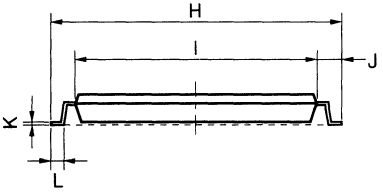
26PIN PLASTIC TSOP(II) (300 mil)



detail of lead end







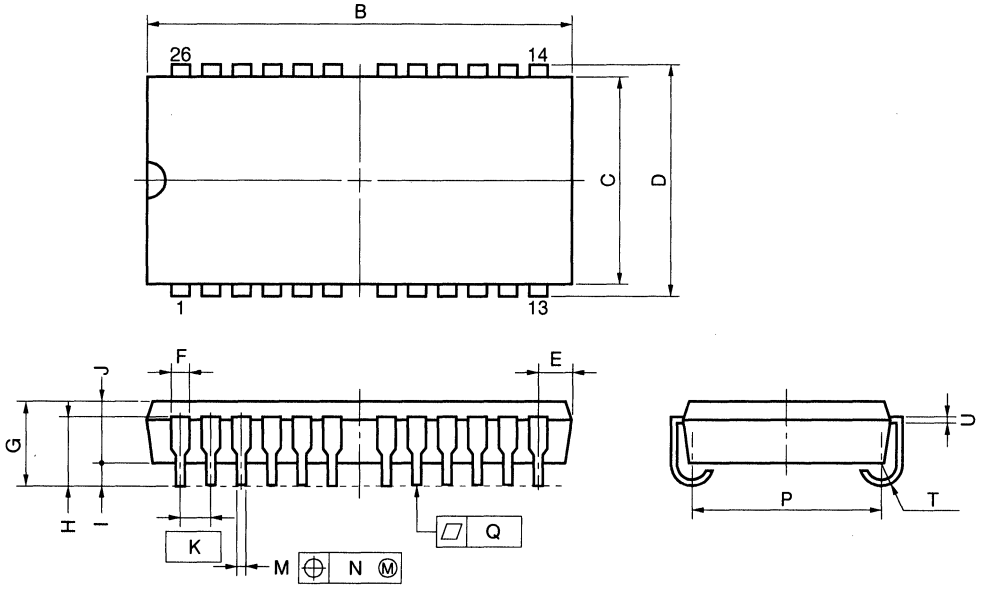
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	3^{+7}_{-3}	3^{+7}_{-3}

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17405, 4217405.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17405G3, 4217405G3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S17405LA, 4217405LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S17805, 4217805

16 M-BIT DYNAMIC RAM
2 M-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μPD42S17805, 4217805 are 2,097,152 words by 8 bits CMOS dynamic RAMs with optional hyper page mode.
Hyper page mode is a kind of the page mode and is useful for the read operation.
Besides, the μPD42S17805 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.
The μPD42S17805, 4217805 are packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 8 bits organization
- Single +5.0 V ±10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD42S17805-60, 4217805-60	605 mW	60 ns	104 ns	25 ns
μPD42S17805-70, 4217805-70	550 mW	70 ns	124 ns	30 ns

- The μPD42S17805 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

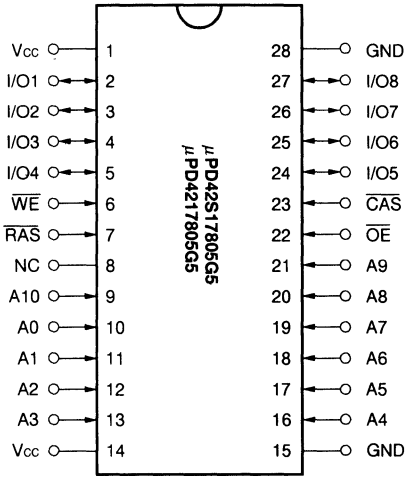
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17805	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μPD4217805	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

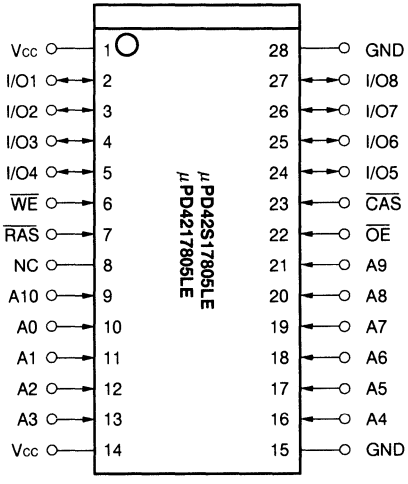
Part number	Access time (MAX.)	Package	Refresh
		28-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17805G5-60	60 ns		
μPD42S17805G5-70	70 ns		
		28-pin Plastic SOJ (400 mil)	
μPD42S17805LE-60	60 ns		
μPD42S17805LE-70	70 ns		
		28-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217805G5-60	60 ns		
μPD4217805G5-70	70 ns		
		28-pin Plastic SOJ (400 mil)	
μPD4217805LE-60	60 ns		
μPD4217805LE-70	70 ns		

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

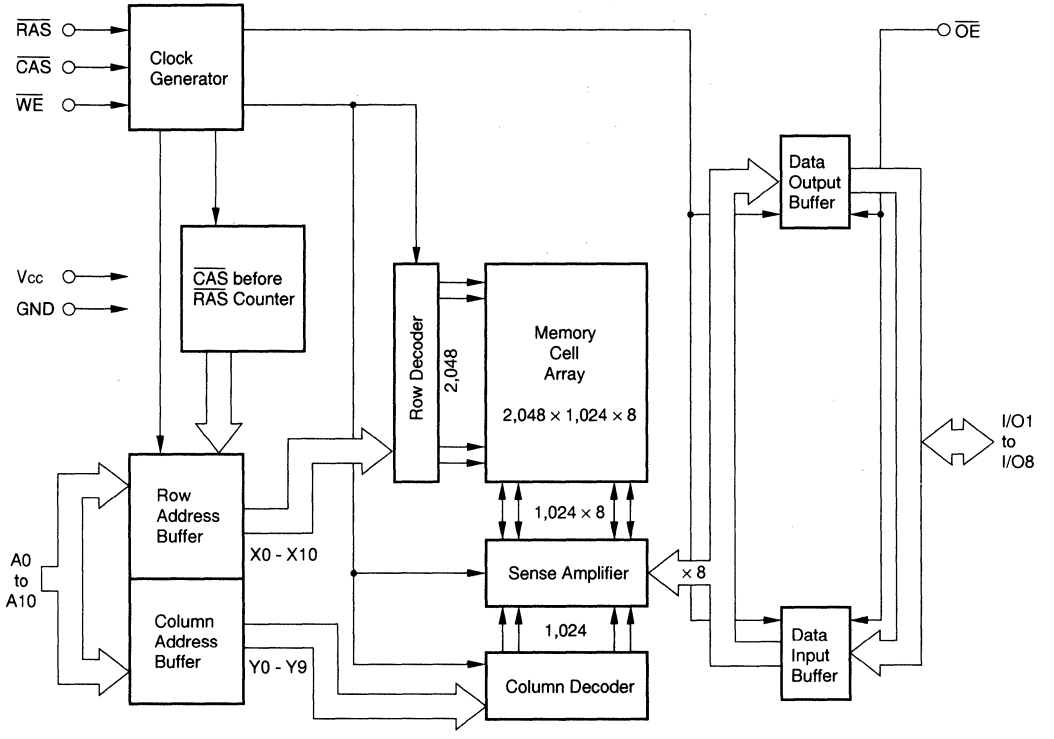


28-pin Plastic SOJ (400 mil)



A0 to A10 : Address Inputs
I/O1 to I/O8: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17805, 4217805 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A10 and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 21-bit of address signal, upper 11-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 2,097,152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

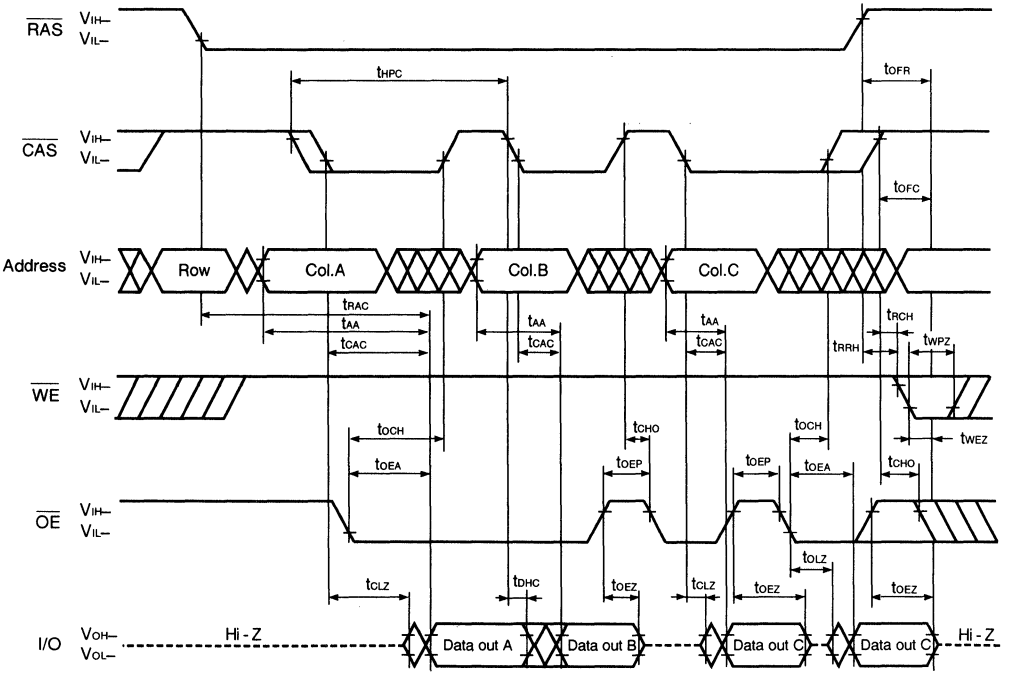
In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA				mA	1, 2, 3
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Standby current	μPD42S17805	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.25		
	μPD4217805		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA				mA	1, 2, 3, 4
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Operating current (Hyper page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA				mA	1, 2, 5
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA				mA	1, 2
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17805)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$	$t_{RAS} \leq 300$ ns		400	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		500	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17805)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$ I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

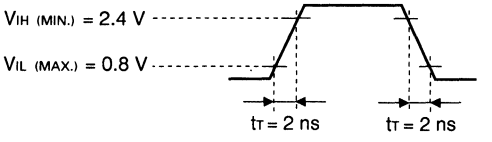
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

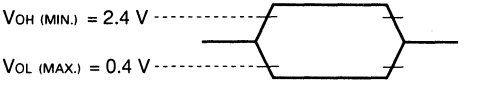
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

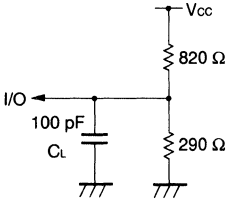
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time		tRP	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ Pulse Width		tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time		tRSH	10	–	12	–	ns	
$\overline{CAS}$ Hold Time		tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		tRCD	14	45	14	52	ns	2
$\overline{RAS}$ to Column Address Delay Time		tRAD	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	–	5	–	ns	3
Row Address Setup Time		tASR	0	–	0	–	ns	
Row Address Hold Time		tRAH	10	–	10	–	ns	
Column Address Setup Time		tASC	0	–	0	–	ns	
Column Address Hold Time		tCAH	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time		tOED	13	–	15	–	ns	
Transition Time (Rise and Fall)		tT	1	50	1	50	ns	
Refresh Time	μPD42S17805	tREF	–	128	–	128	ms	4
	μPD4217805		–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S17805.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ Precharge Time	t_{OEP}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

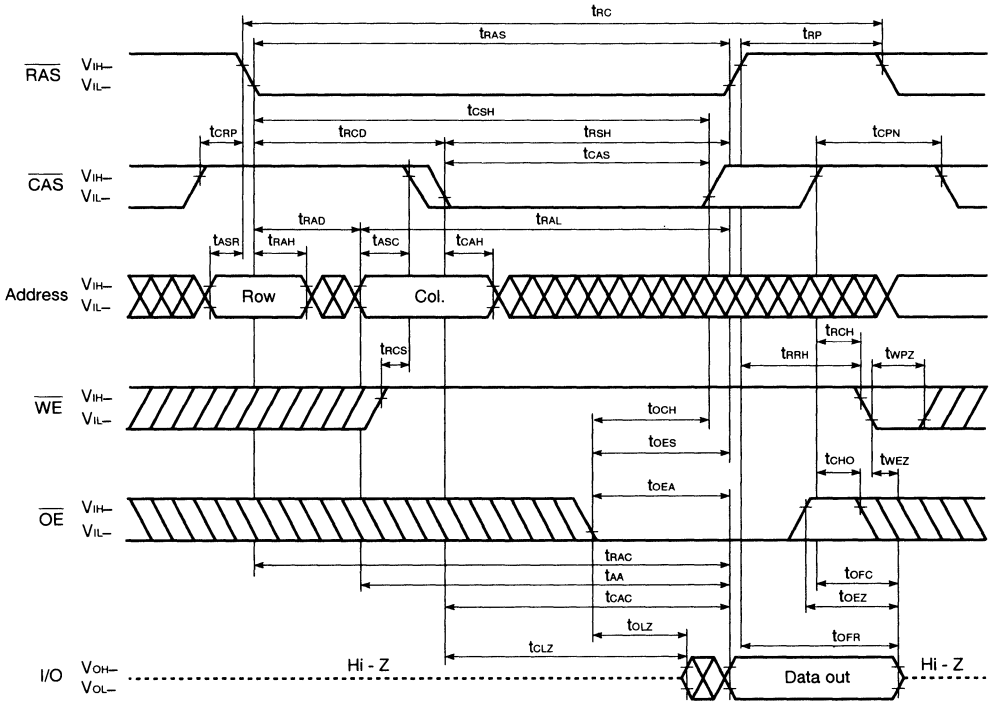
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

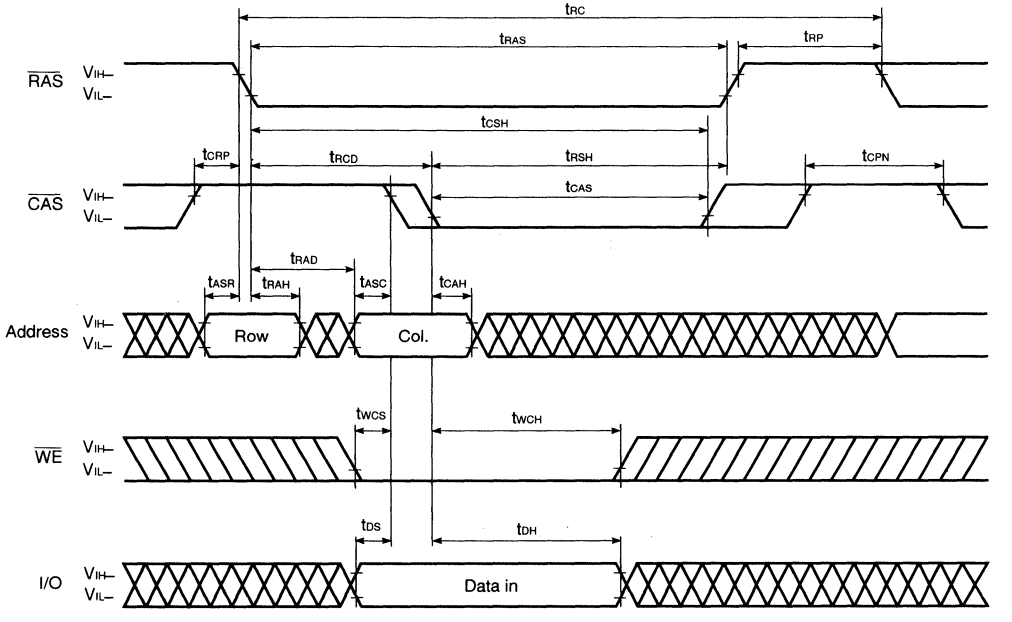
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ Setup Time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17805.

Read Cycle

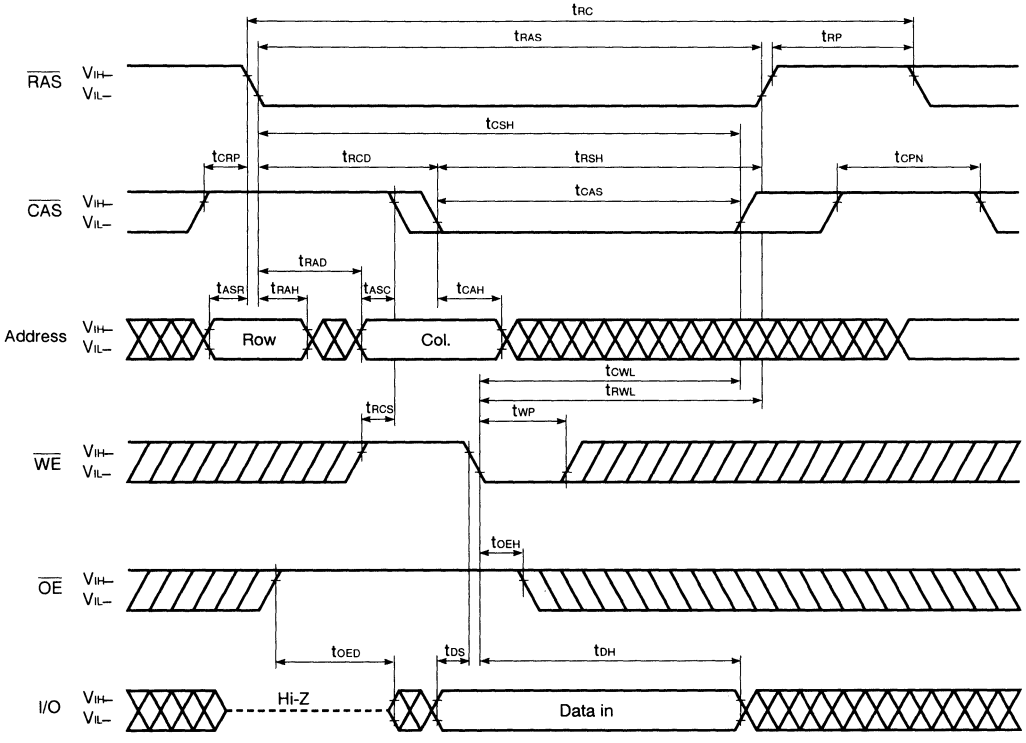

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCS
tRCH
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

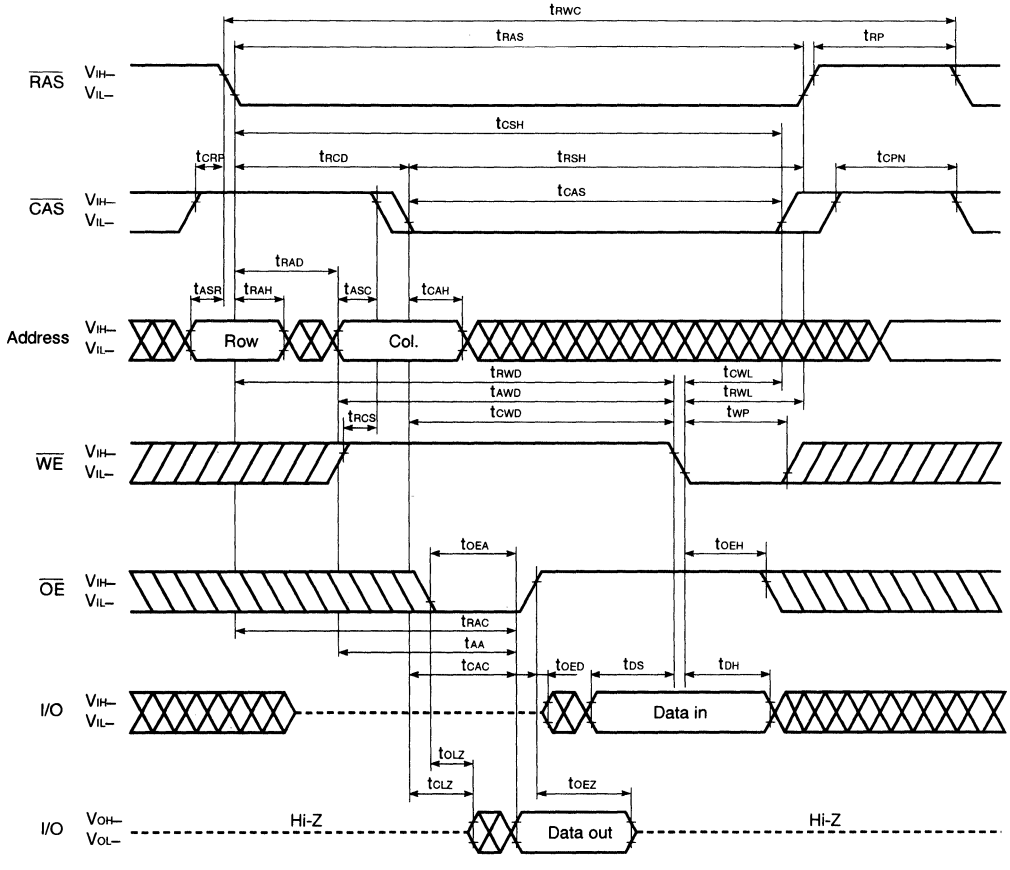


Remark $\overline{OE}$: Don't care

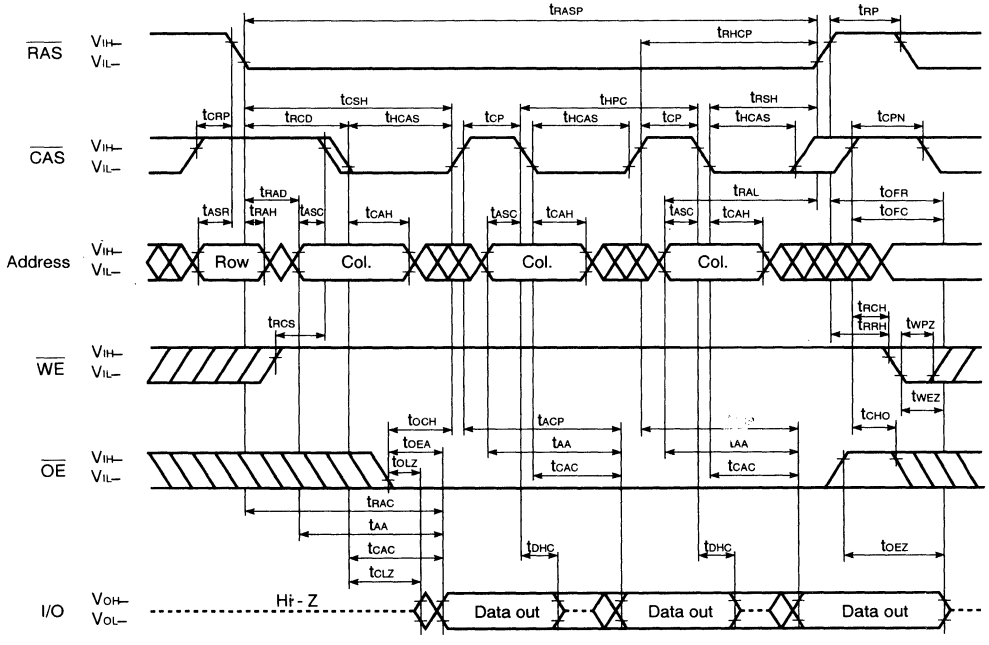
Late Write Cycle



Read Modify Write Cycle

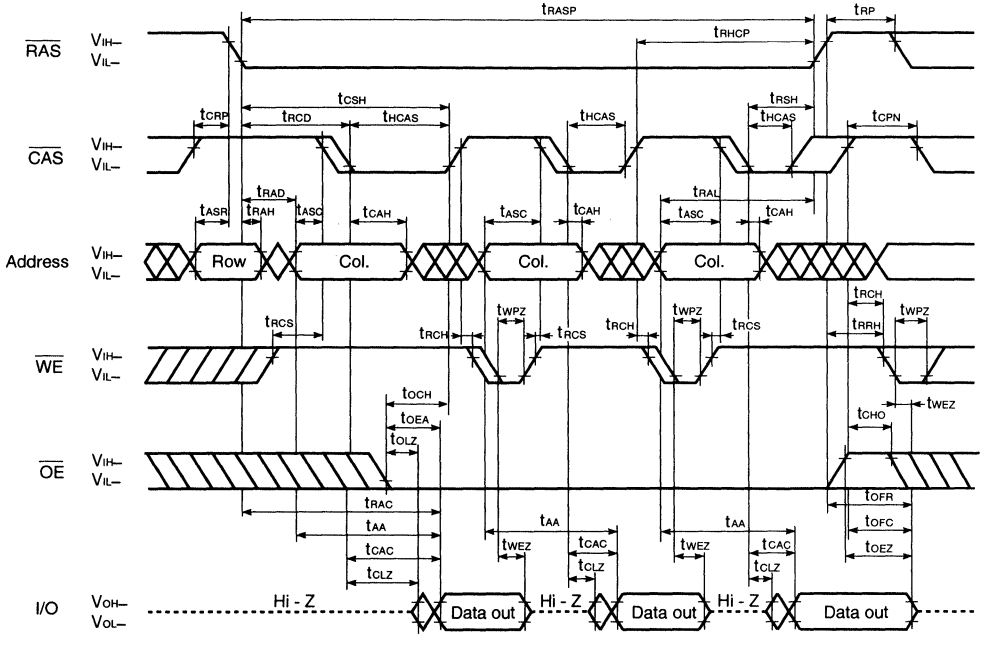


Hyper Page Mode Read Cycle



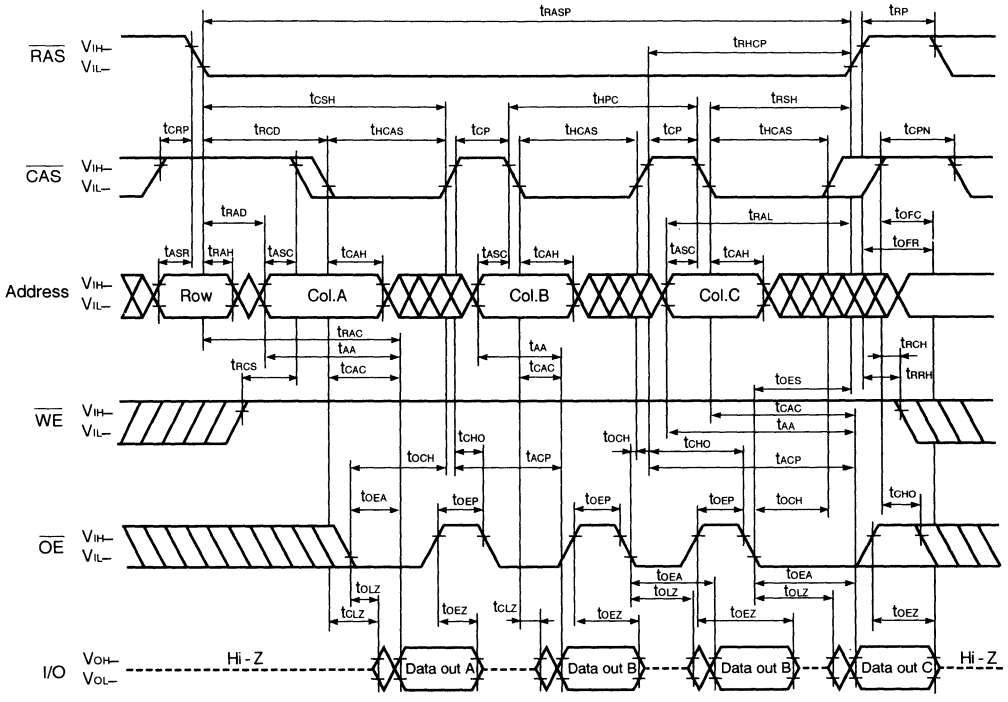
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



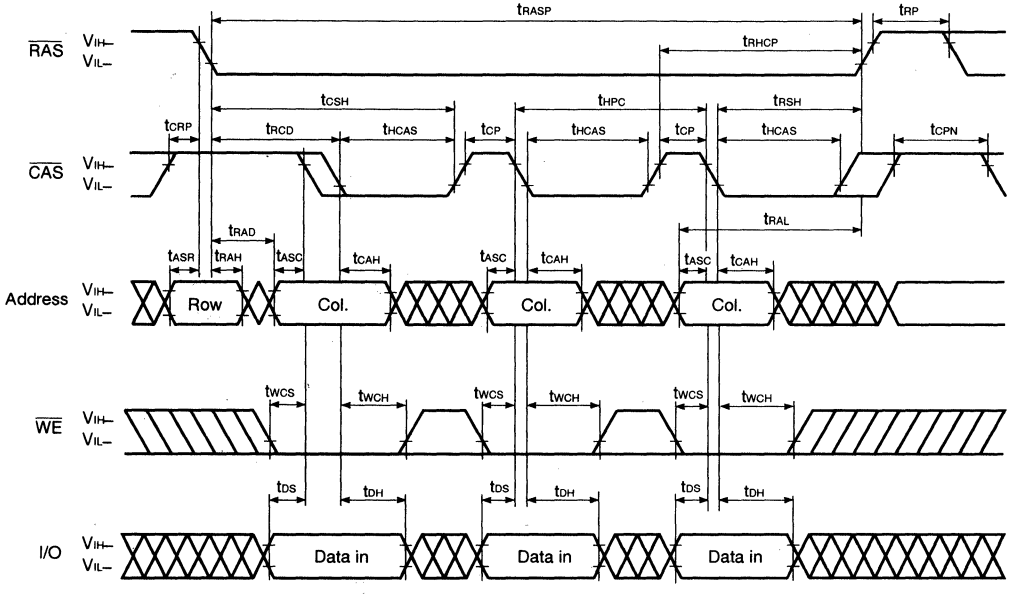
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

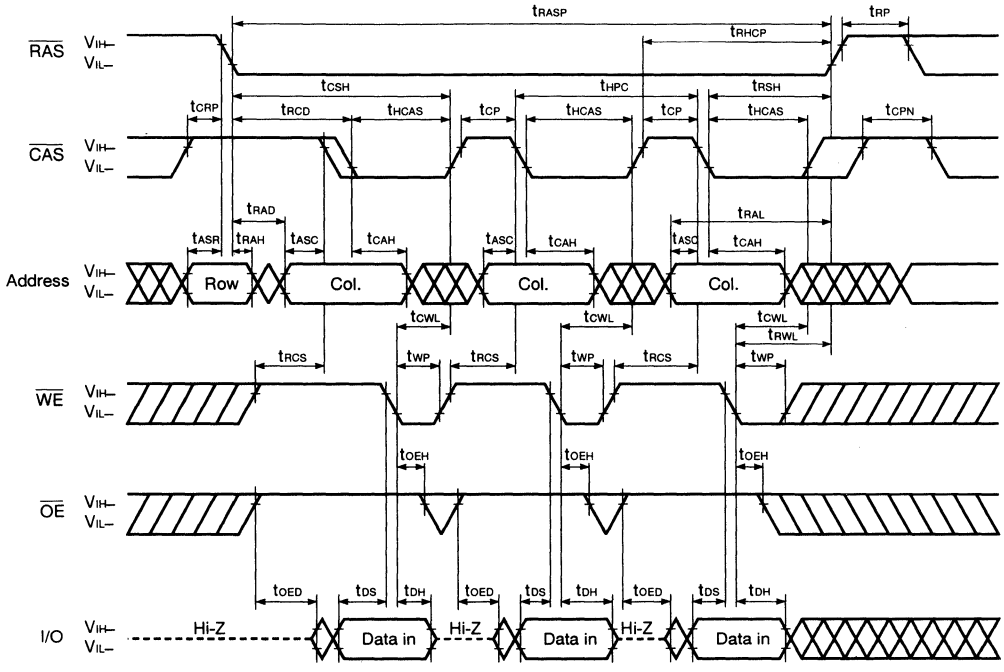
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

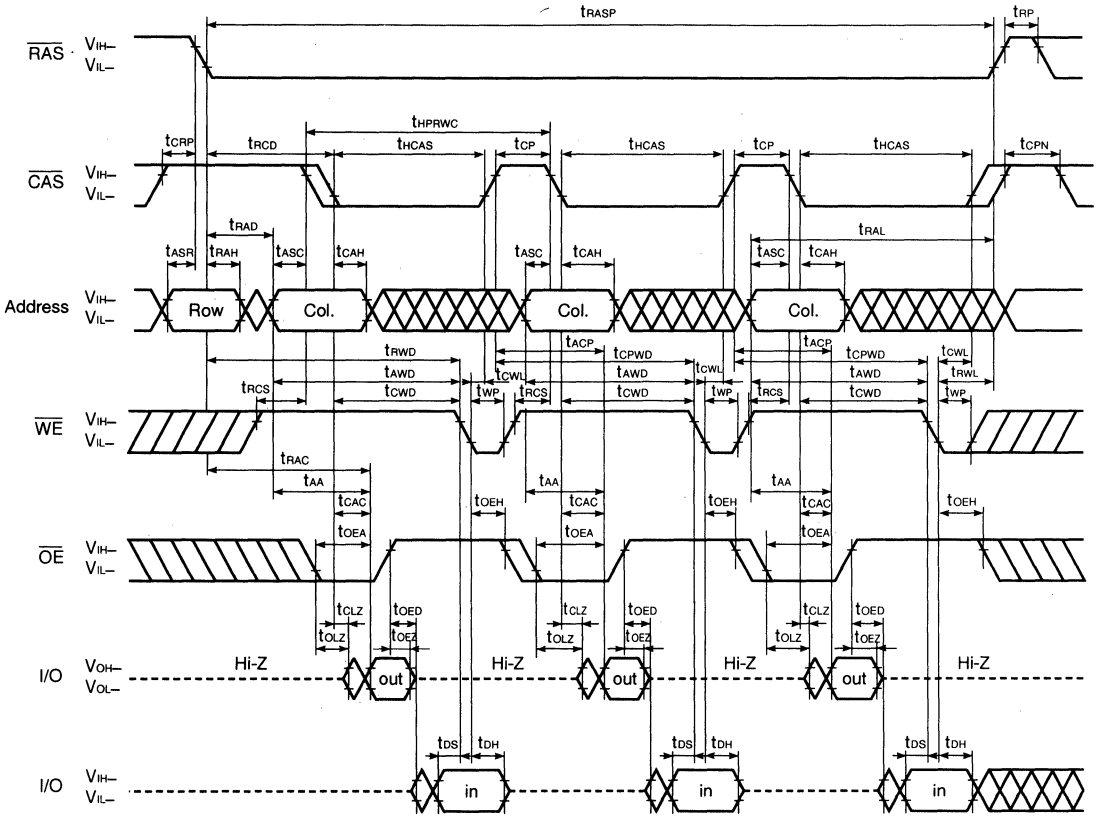
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



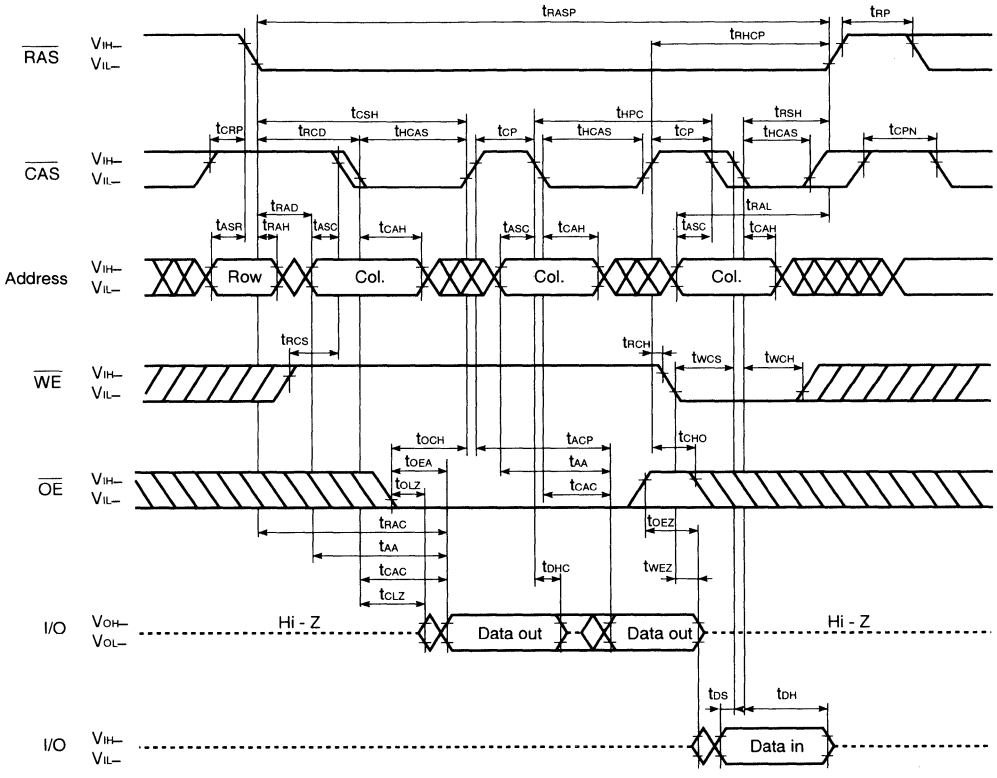
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



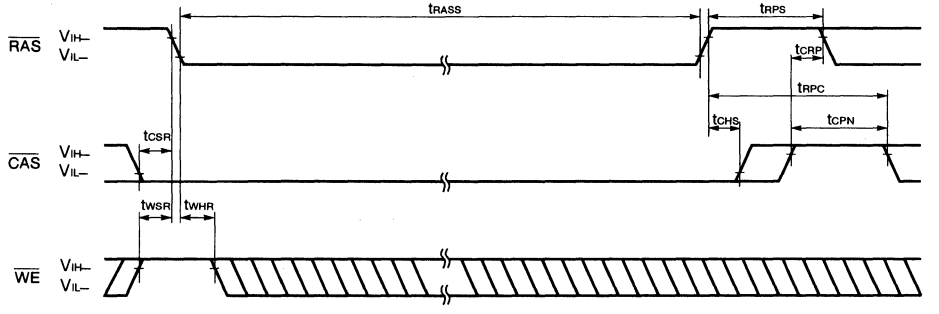
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17805)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

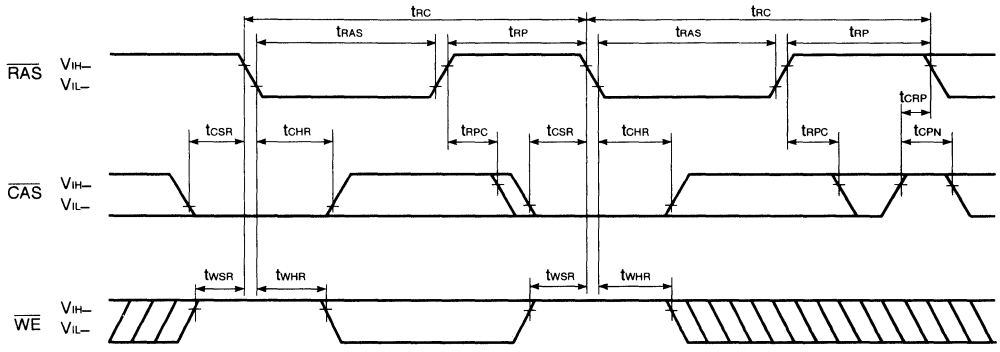
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (2,048/128 ms) should be met.

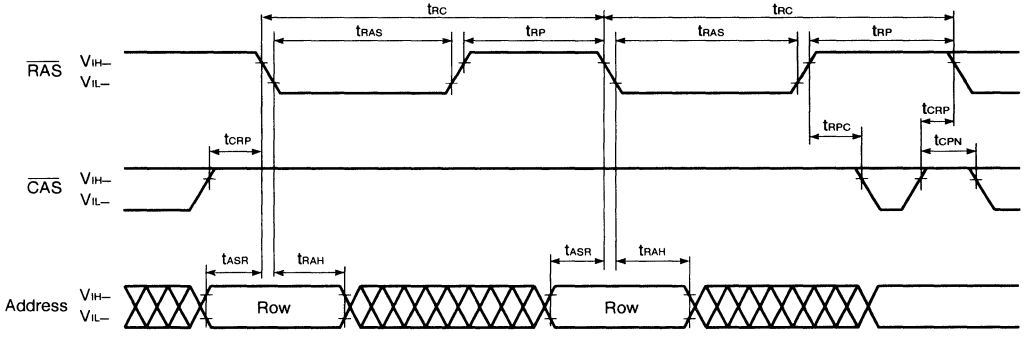
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



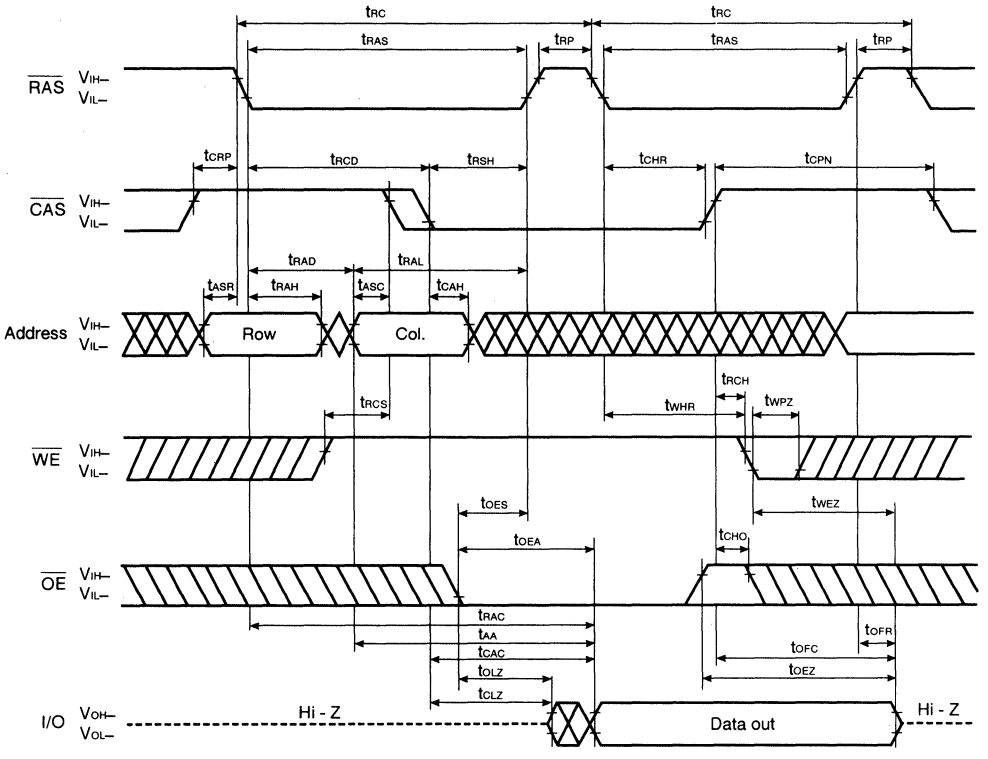
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

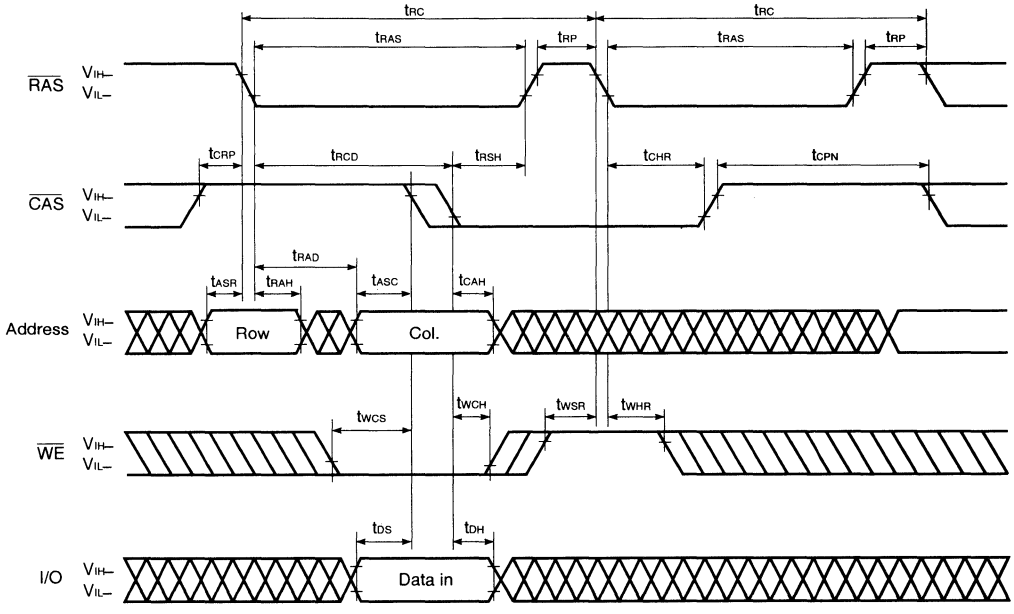


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

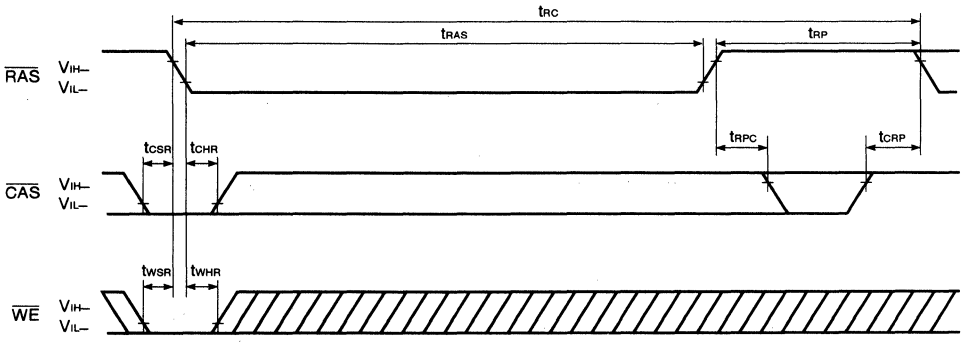


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the ×16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

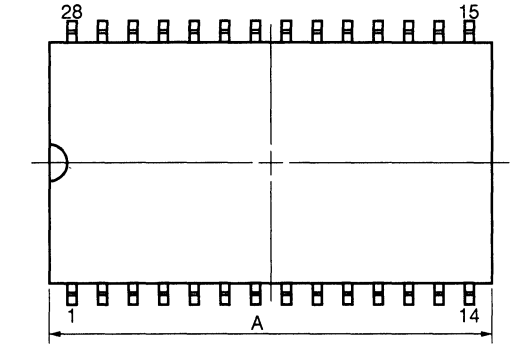
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

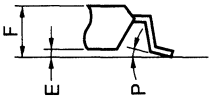
The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

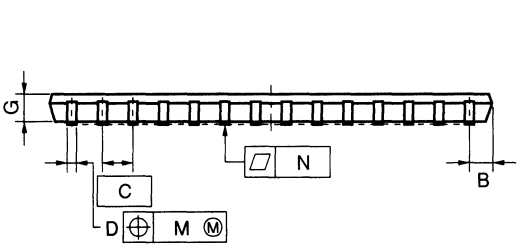
Package Drawings

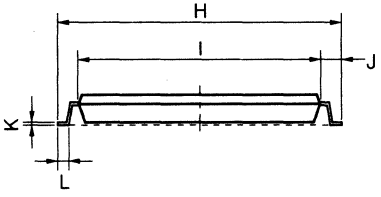
28PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







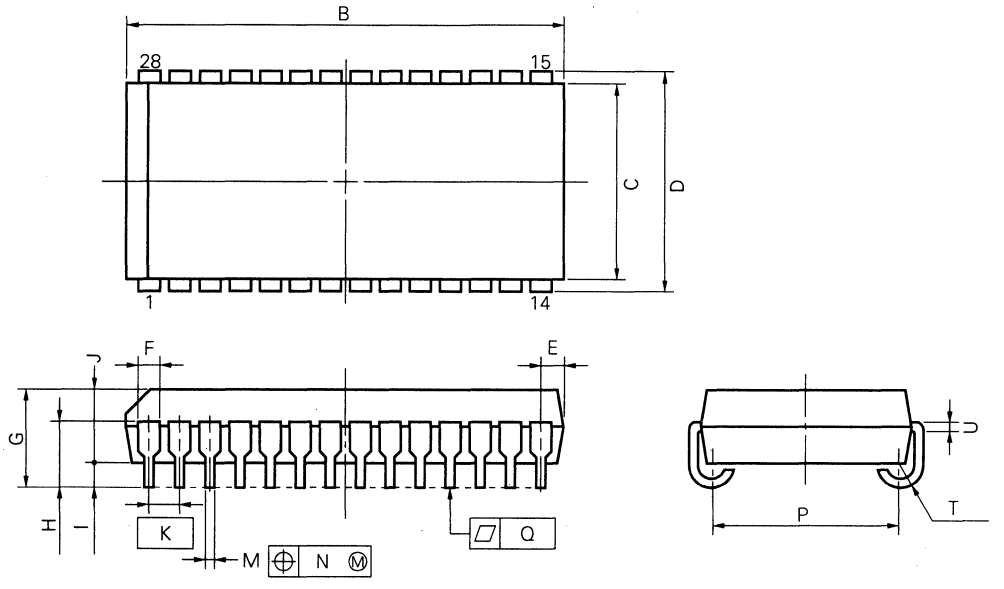
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S17805, 4217805.

Types of Surface Mount Device

μPD42S17805G5, 4217805G5 : **28-pin plastic TSOP (II) (400 mil)**
μPD42S17805LE, 4217805LE : **28-pin plastic SOJ (400 mil)**

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD42S18165, 4218165

16 M-BIT DYNAMIC RAM
1 M-WORD BY 16-BIT, HYPER PAGE MODE (EDO), BYTE READ/WRITE MODE

Description

The μPD42S18165, 4218165 are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S18165 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S18165, 4218165 are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 16 bits organization
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S18165-60, 4218165-60	880 mW	60 ns	104 ns	25 ns
μPD42S18165-70, 4218165-70	825 mW	70 ns	124 ns	30 ns

- The μPD42S18165 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

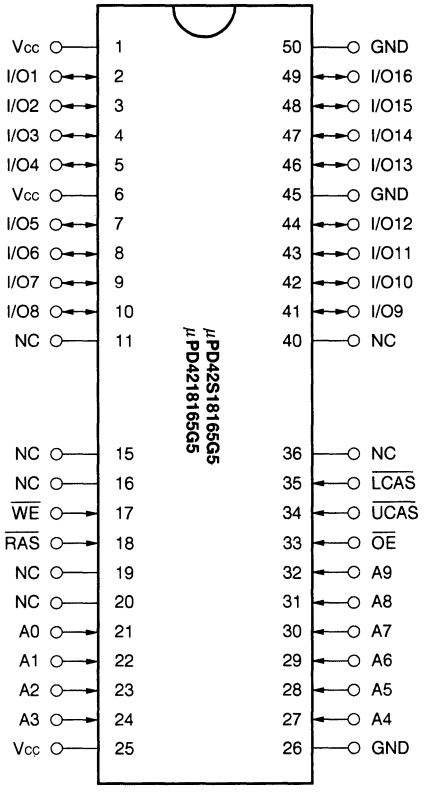
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S18165	1,024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μPD4218165	1,024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

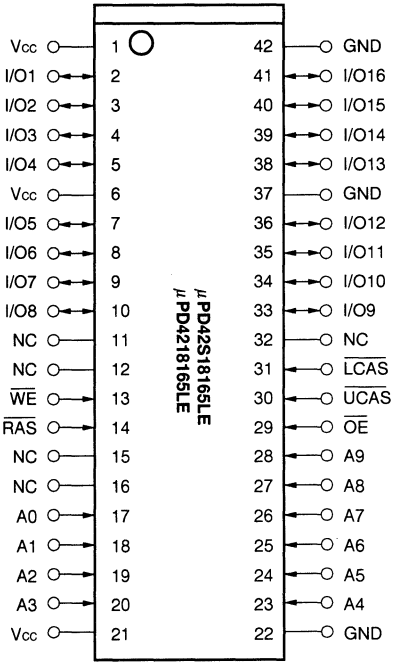
Part number	Access time (MAX.)	Package	Refresh
		50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18165G5-60	60 ns		
μPD42S18165G5-70	70 ns		
		42-pin plastic SOJ (400 mil)	
μPD42S18165LE-60	60 ns		
μPD42S18165LE-70	70 ns		
		50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218165G5-60	60 ns		
μPD4218165G5-70	70 ns		
		42-pin plastic SOJ (400 mil)	
μPD4218165LE-60	60 ns		
μPD4218165LE-70	70 ns		

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

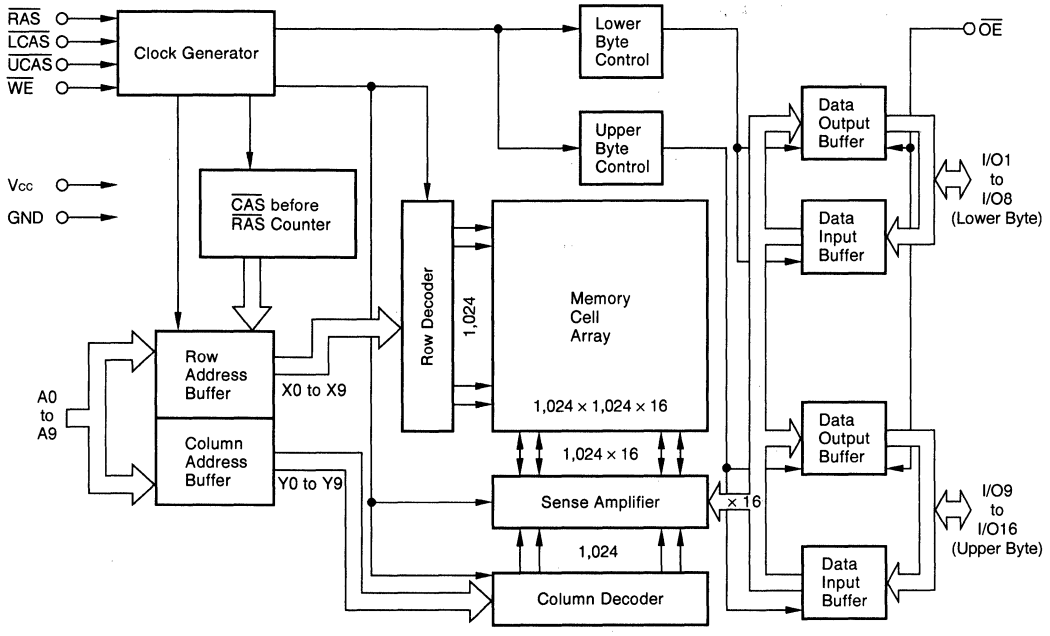


42-pin Plastic SOJ (400 mil)



A0 to A9	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S18165, 4218165 have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

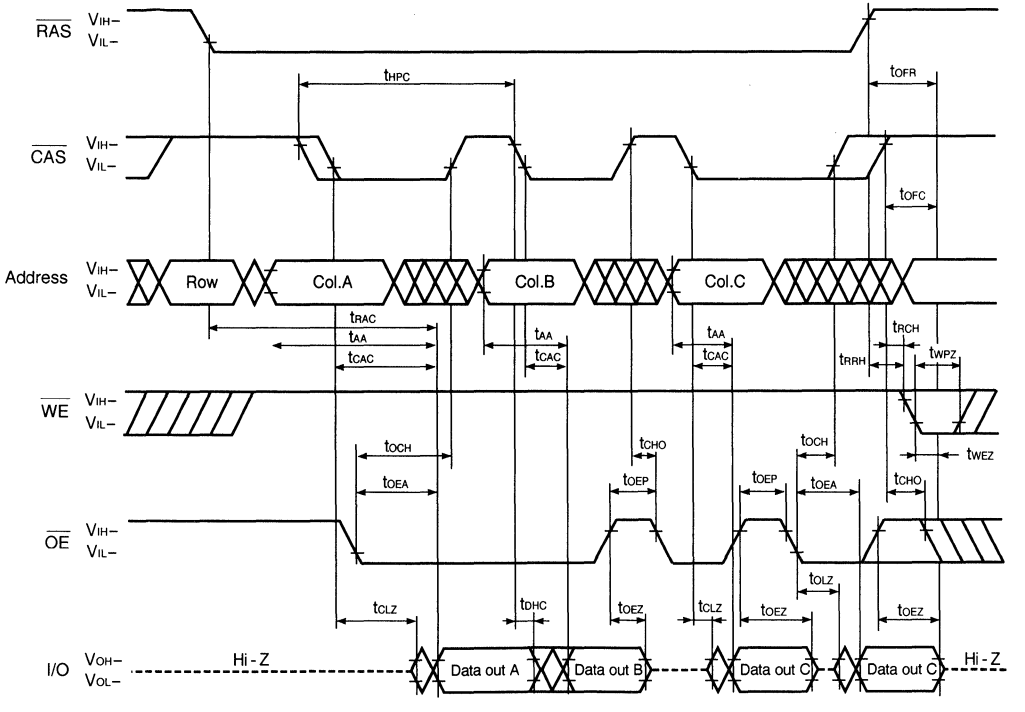
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling				mA	1, 2, 3
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		160		
				t_{RAC} = 70 ns		150		
Standby current	μPD42S18165	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.25		
	μPD4218165		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$				mA	1, 2, 3, 4
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		160		
				t_{RAC} = 70 ns		150		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling				mA	1, 2, 5
			$t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling				mA	1, 2
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		160		
				t_{RAC} = 70 ns		150		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18165)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$, 0 V ≤ $V_{IL} \leq$ 0.2 V	$t_{RAS} \leq$ 300 ns		350	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, Address: V_{IH} or V_{IL}, $\overline{WE}$, $\overline{OE}$: V_{IH}, I_O = 0 mA	$t_{RAS} \leq$ 1 μs		400	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S18165)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$, 0 V ≤ $V_{IL} \leq$ 0.2 V, I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V, All other pins not under test = 0 V		–10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V, Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

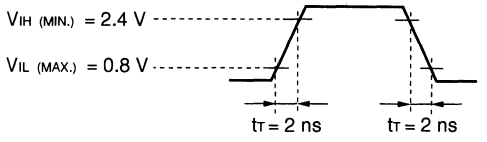
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

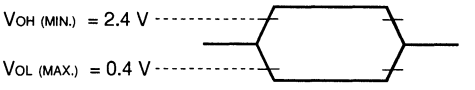
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

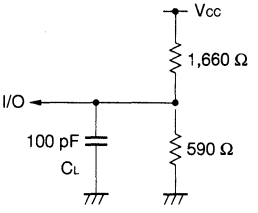
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	104	–	124	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		tRSH	10	–	12	–	ns	
$\overline{CAS}$ hold time		tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		tMRH	0	–	0	–	ns	
Transition time (rise and fall)		tT	1	50	1	50	ns	
Refresh time	μPD42S18165	tREF	–	128	–	128	ms	4
	μPD4218165		–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S18165.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

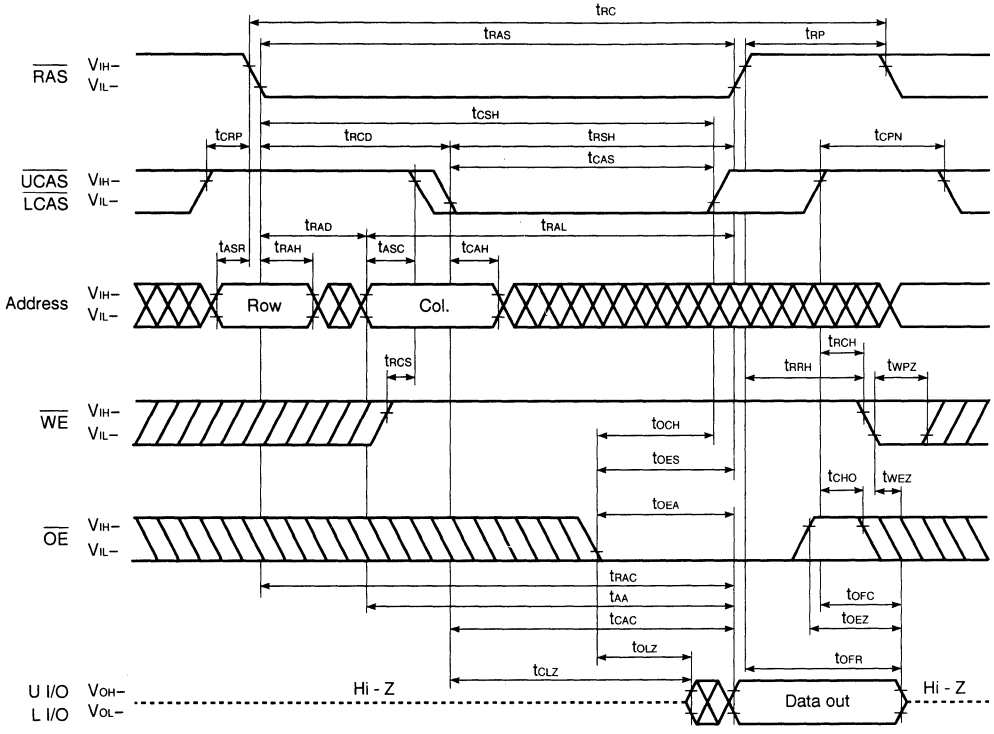
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

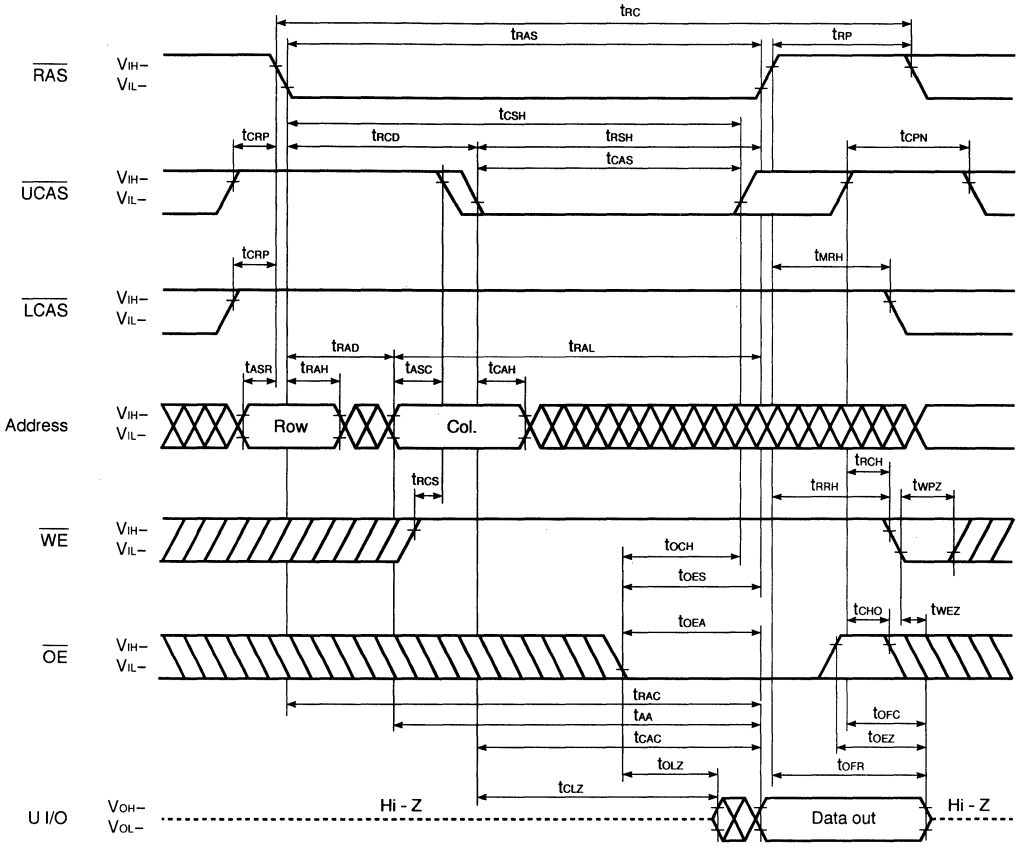
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S18165.

Read Cycle

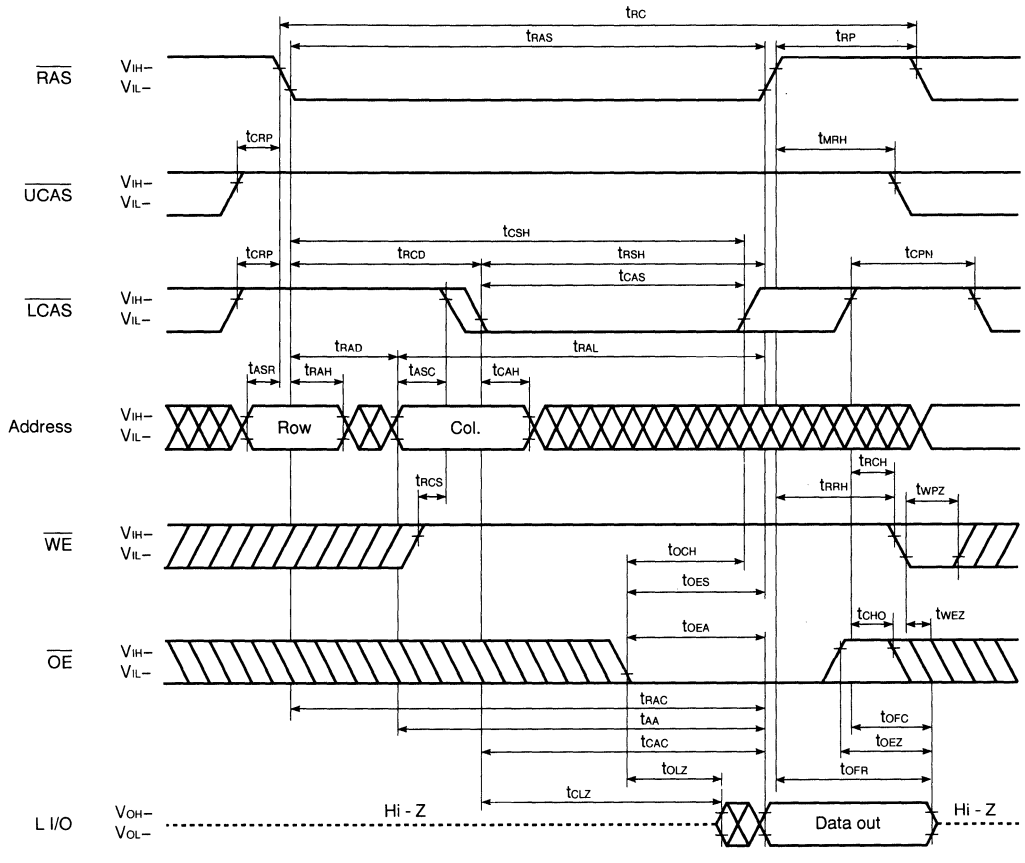

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



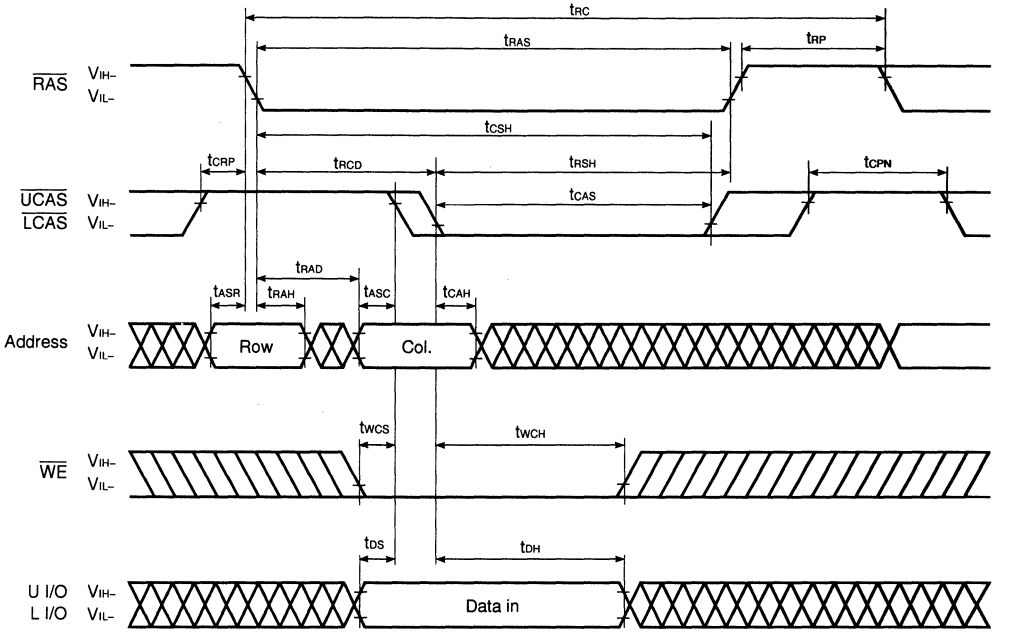
Remark L I/O: Hi-Z

Lower Byte Read Cycle



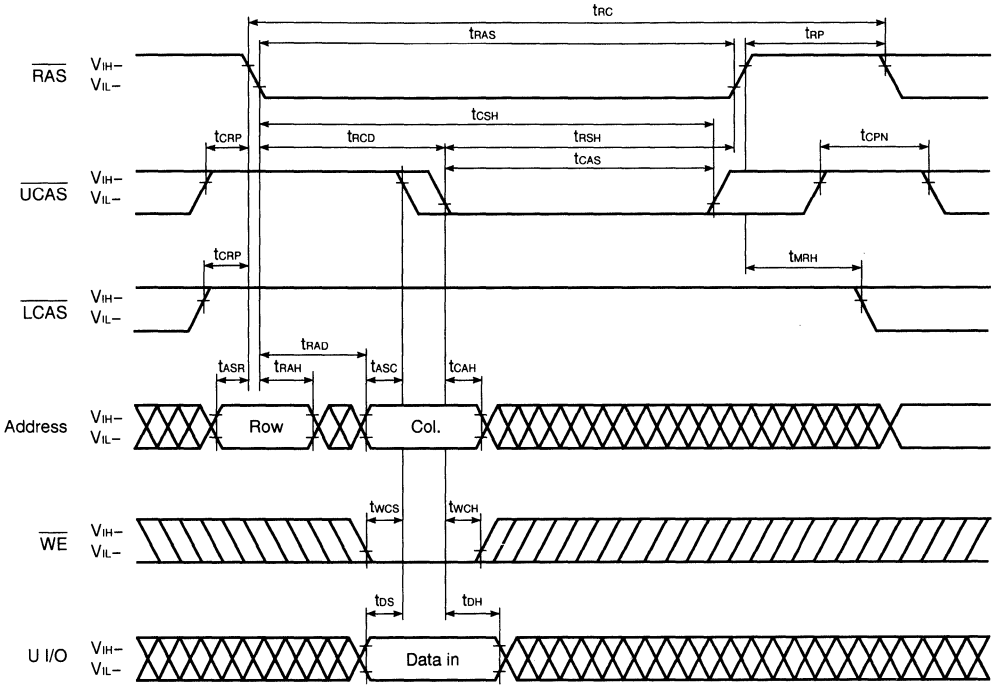
Remark U I/O: Hi-Z

Early Write Cycle



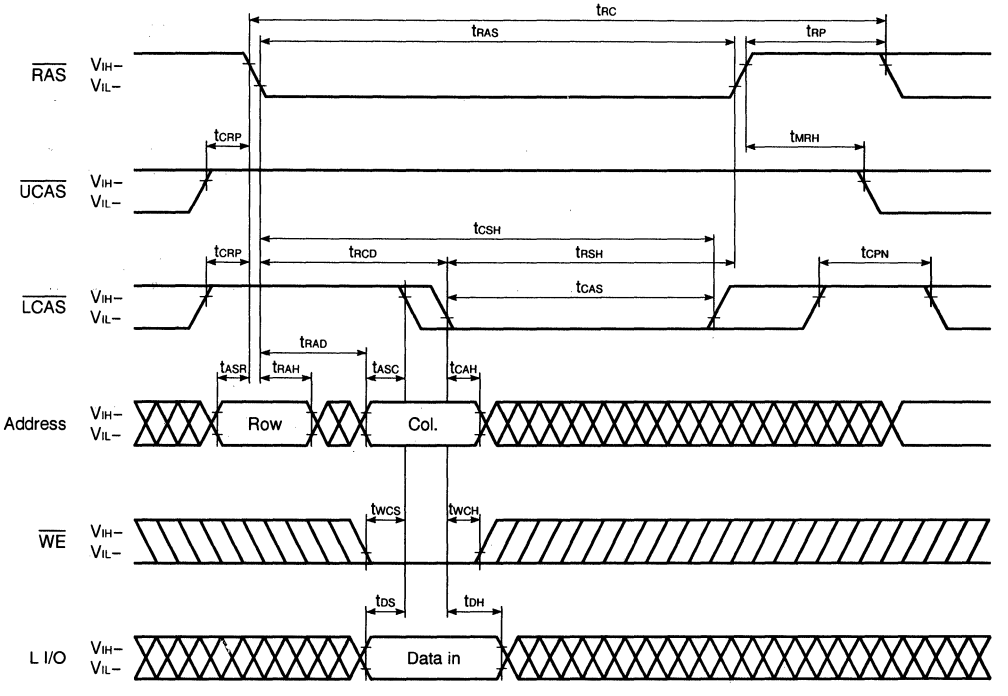
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



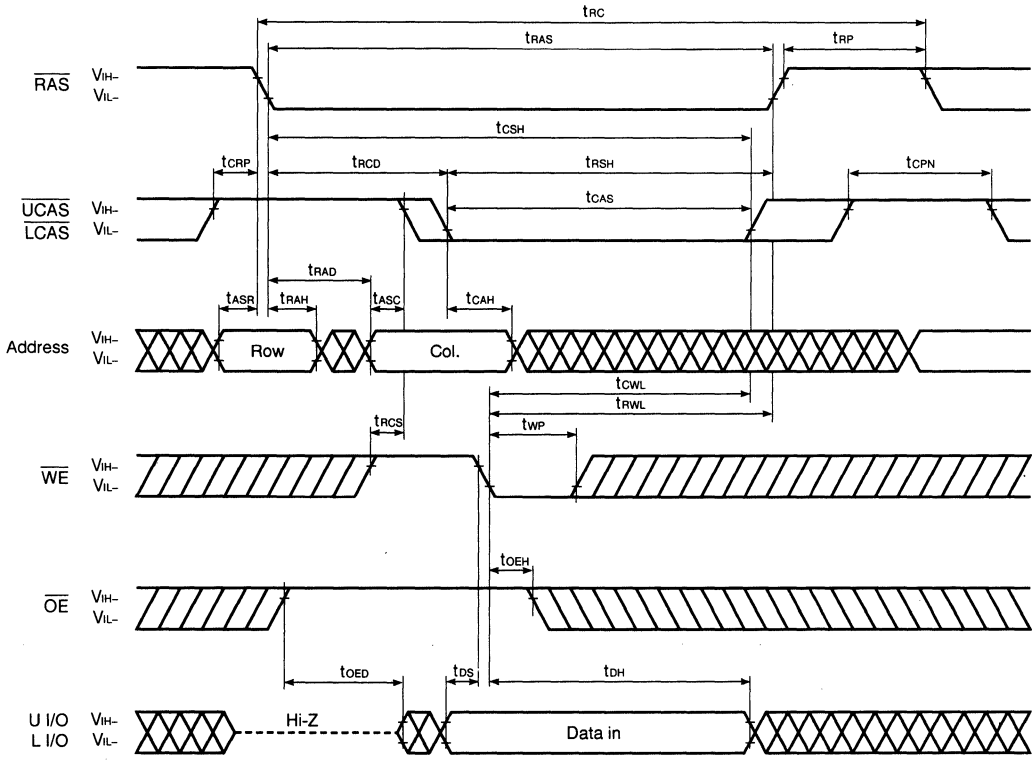
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

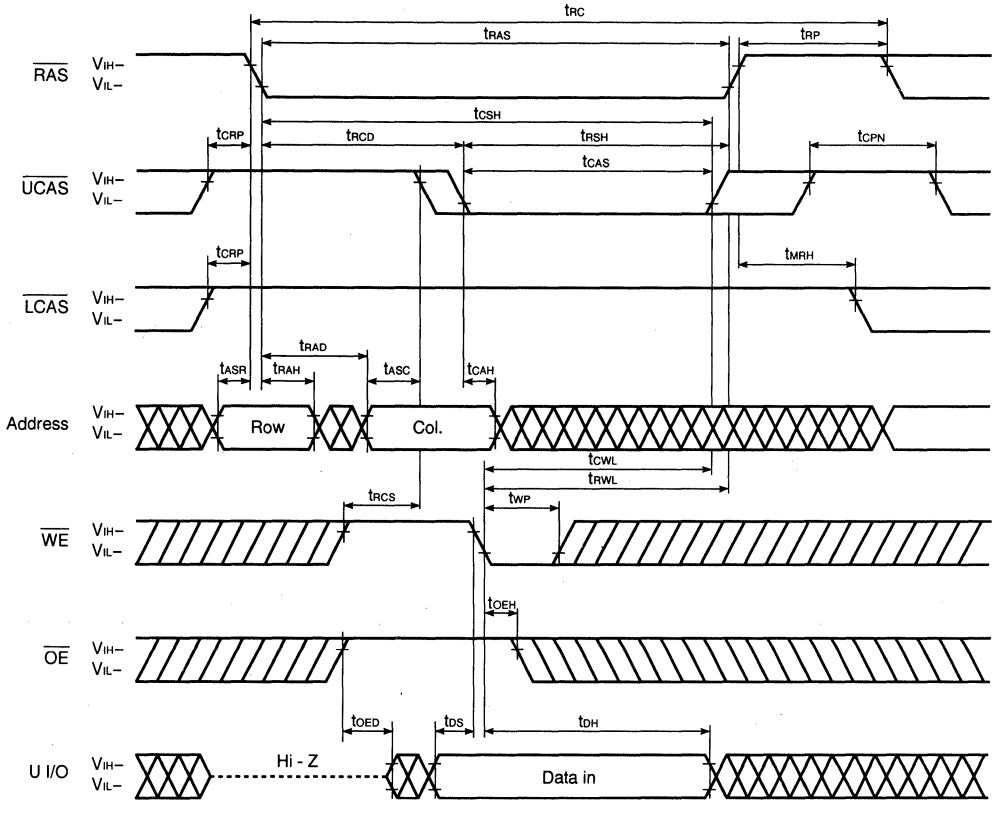


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

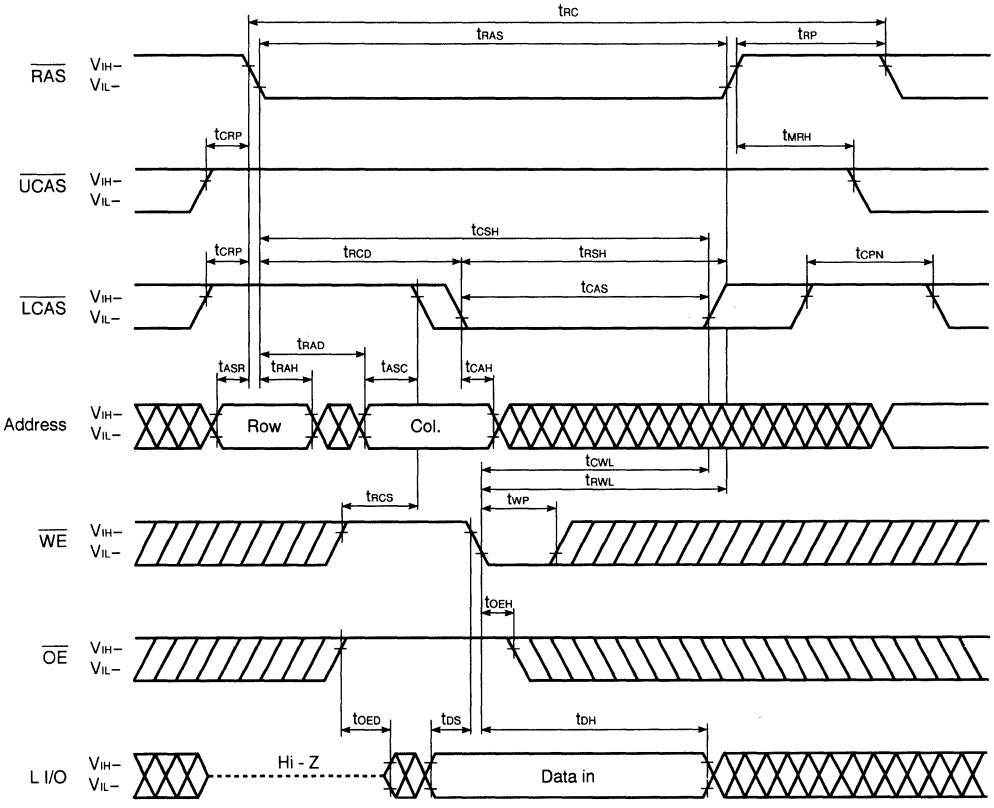


Upper Byte Late Write Cycle



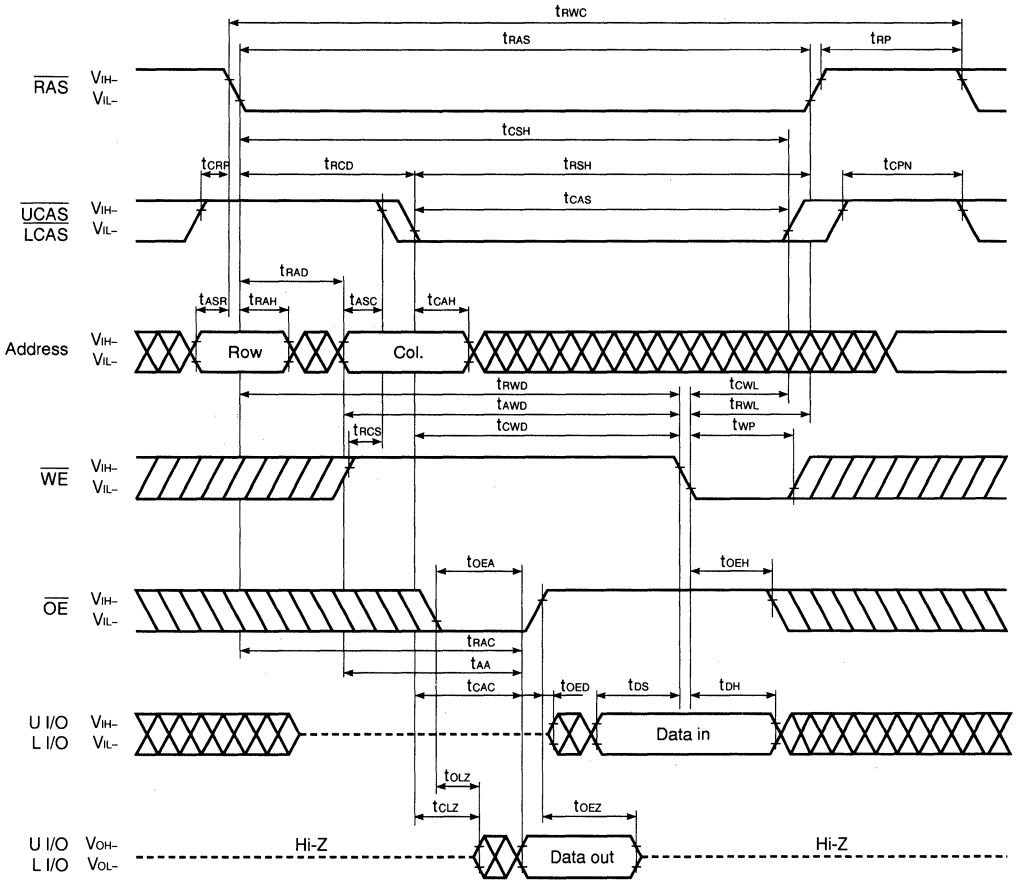
Remark L I/O: Don't care

Lower Byte Late Write Cycle

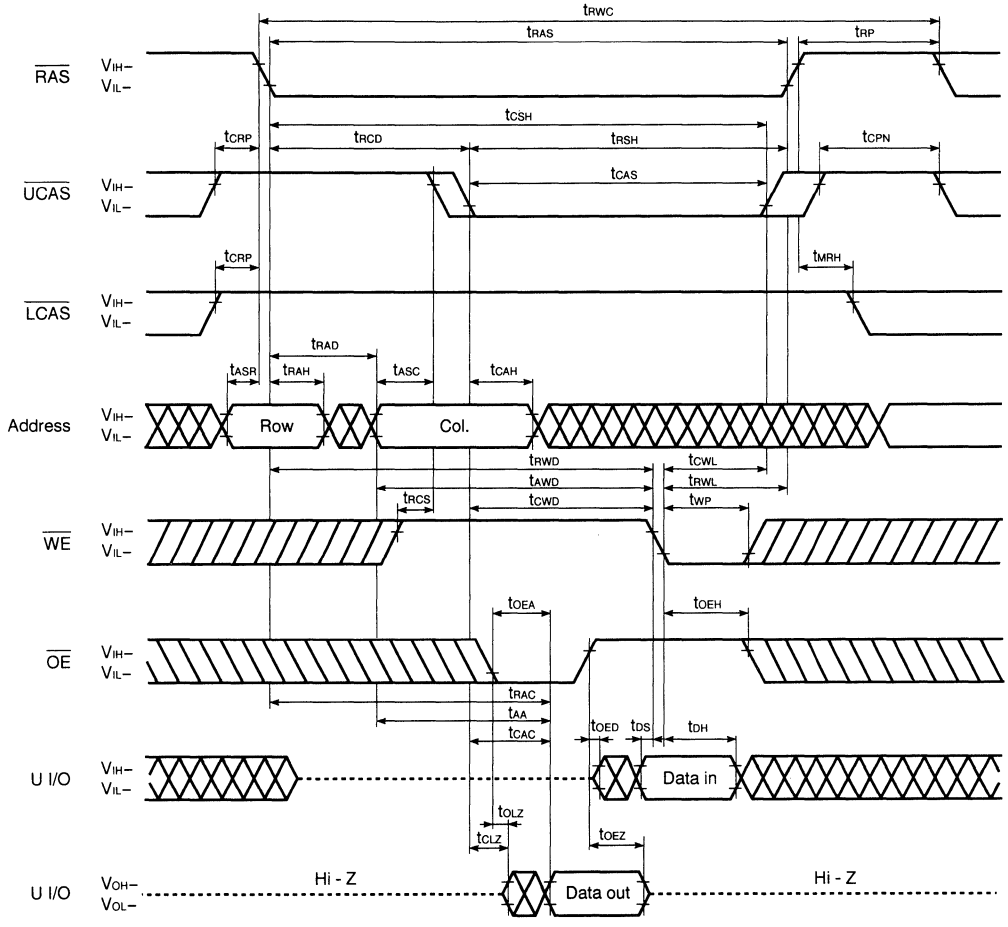


Remark L I/O: Don't care

Read Modify Write Cycle

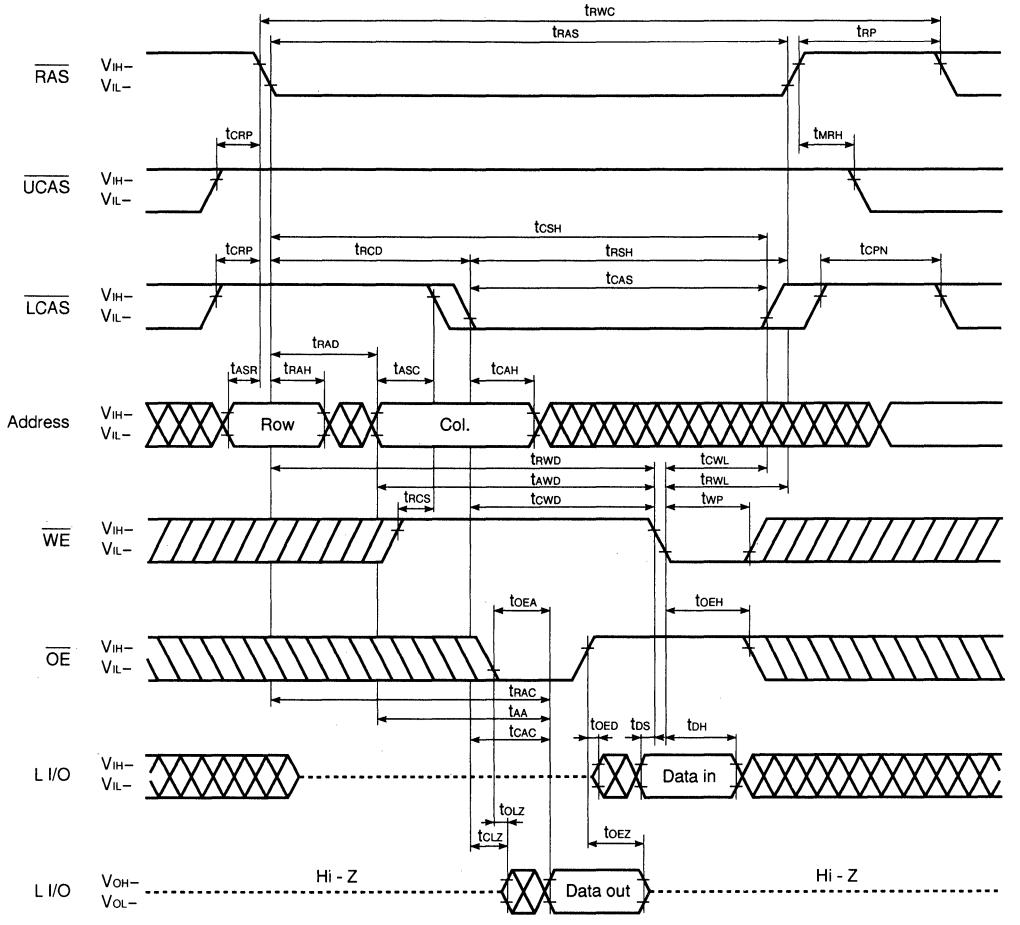


Upper Byte Read Modify Write Cycle



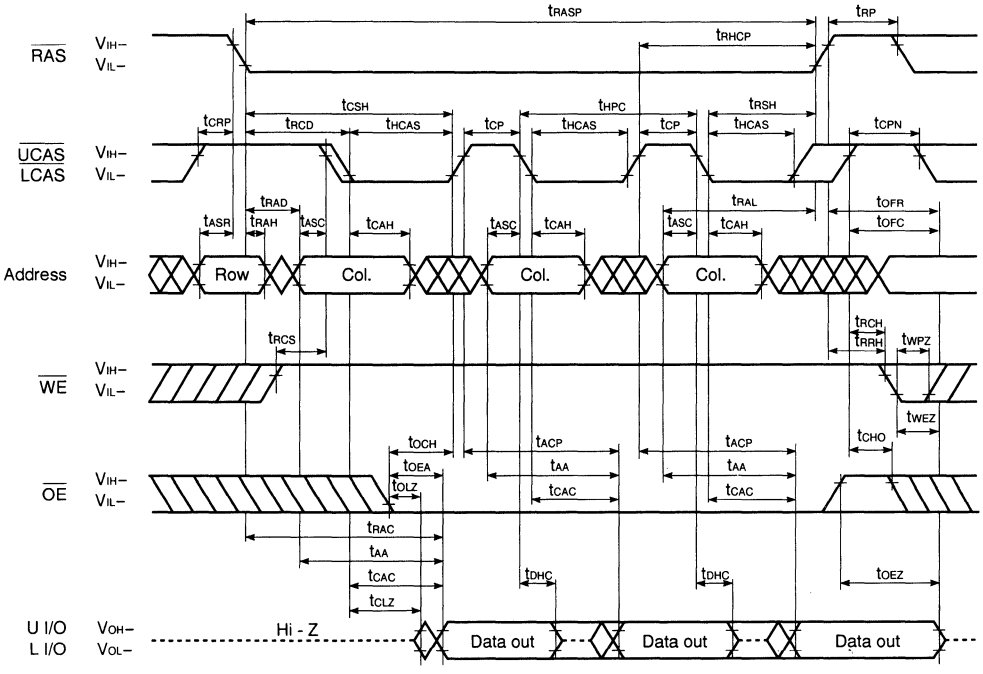
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



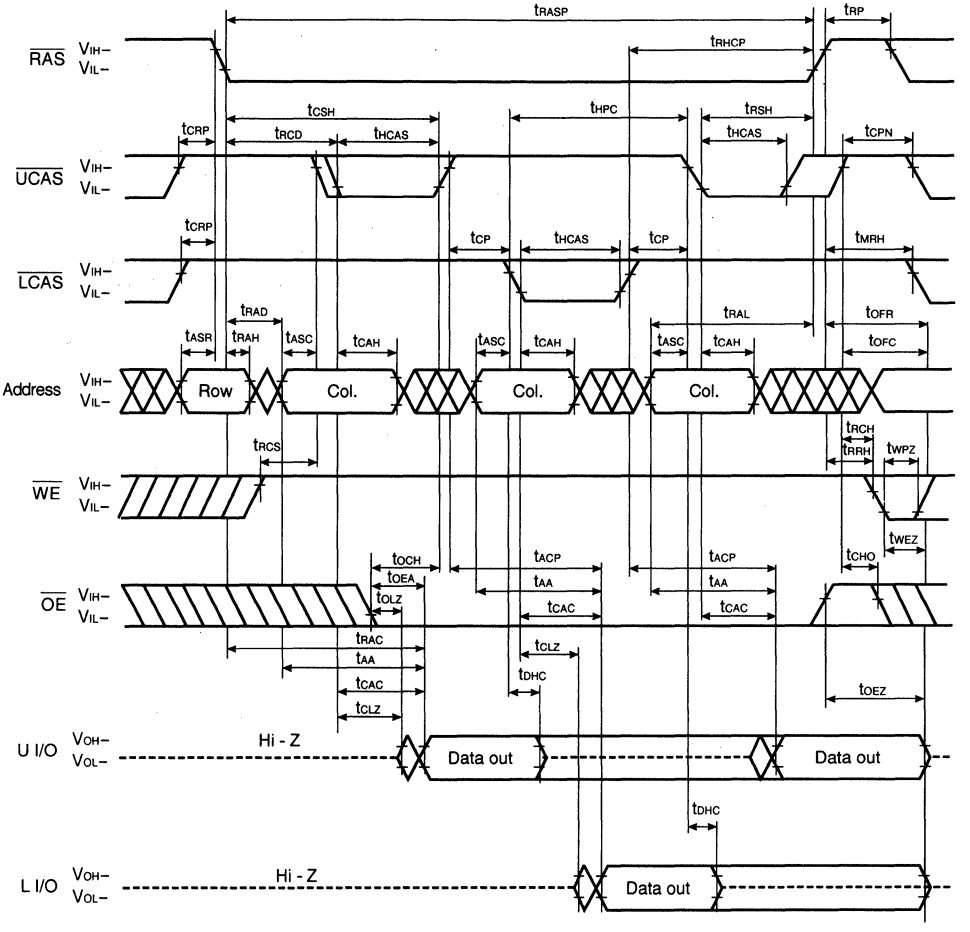
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

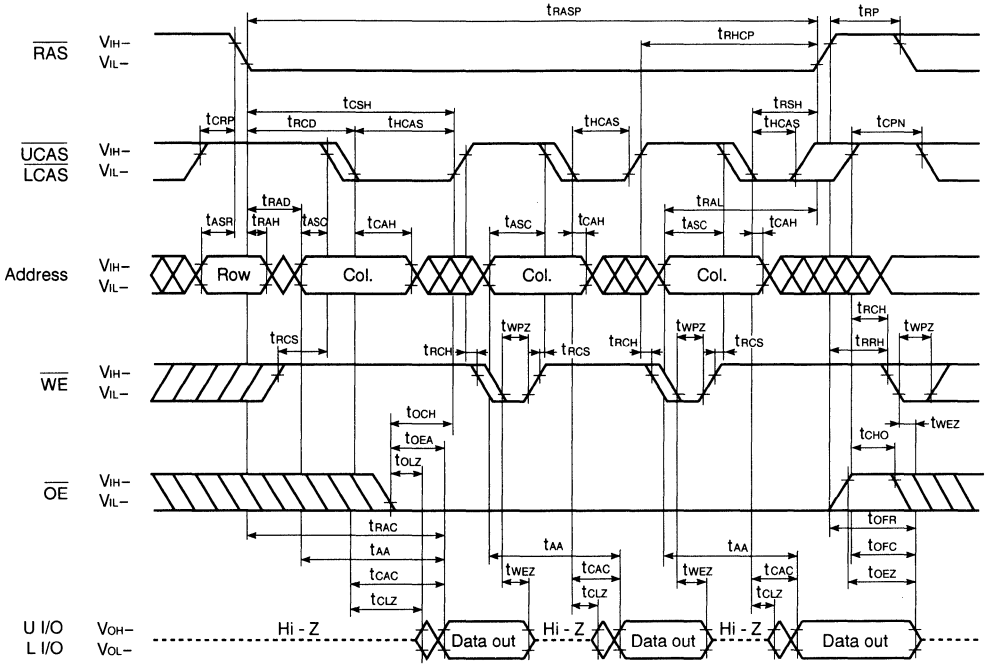
Hyper Page Mode (EDO) Byte Read Cycle



Remark 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

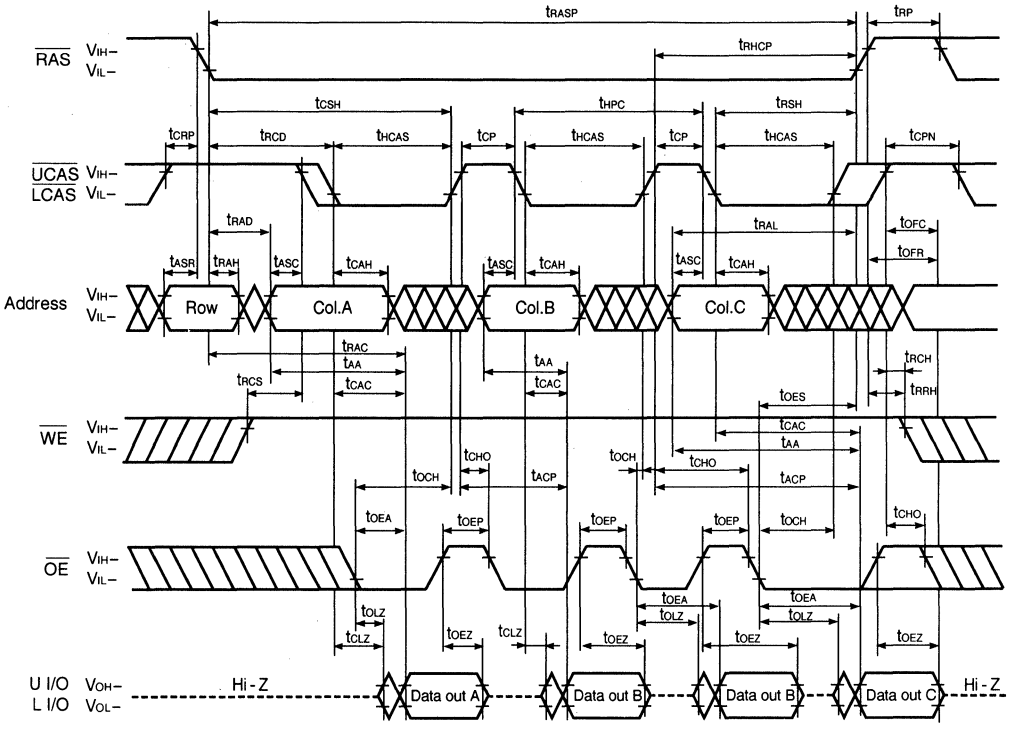
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



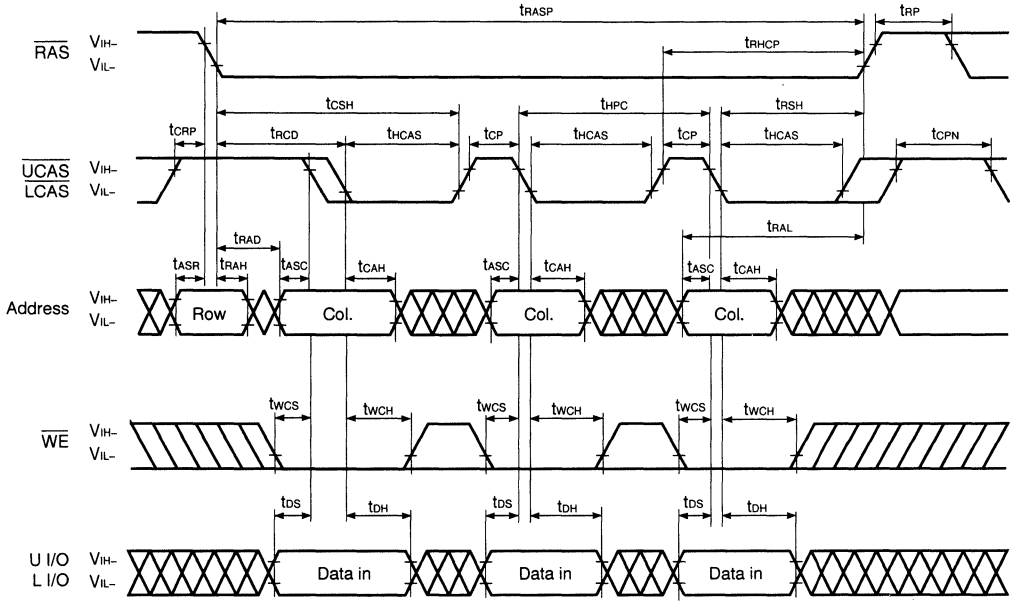
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

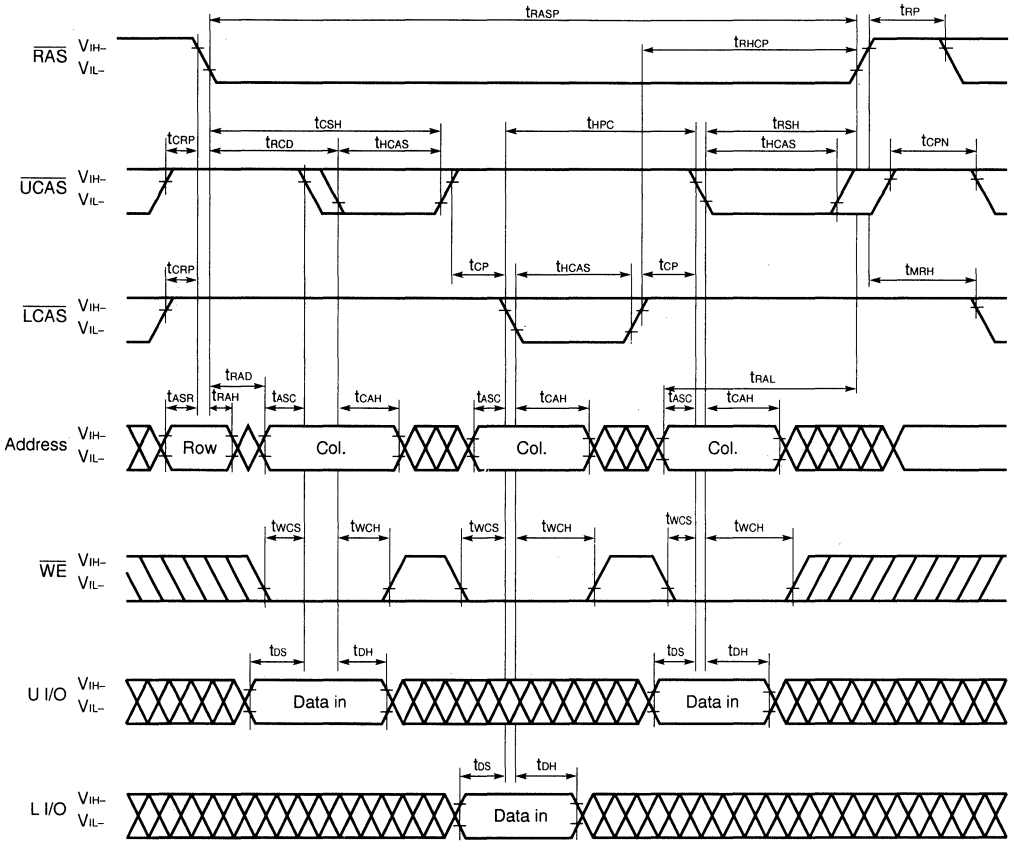
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Byte Early Write Cycle

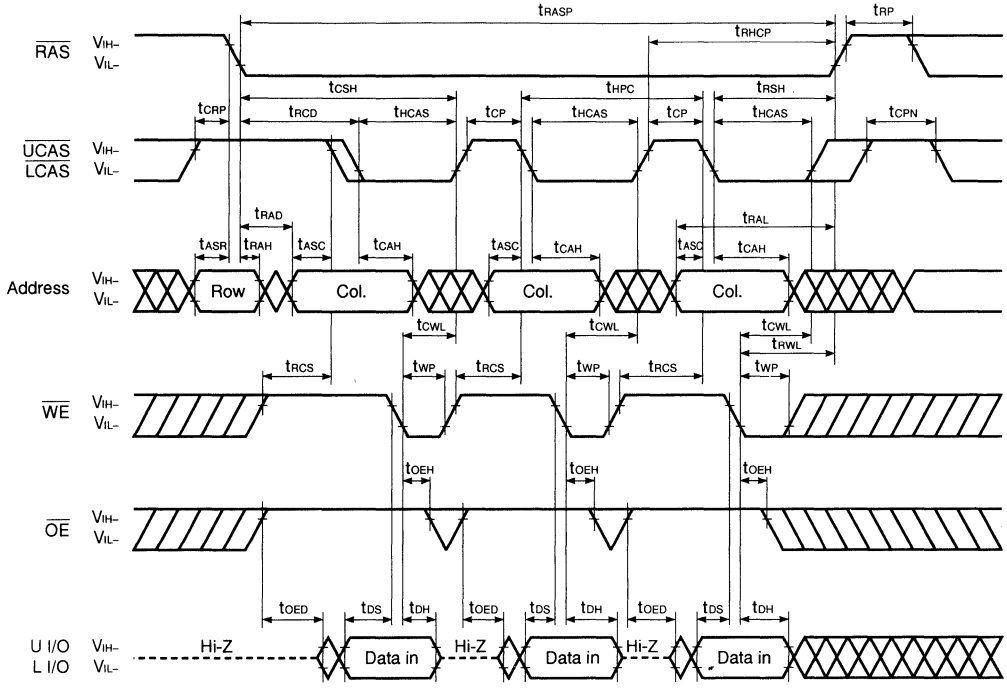


Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

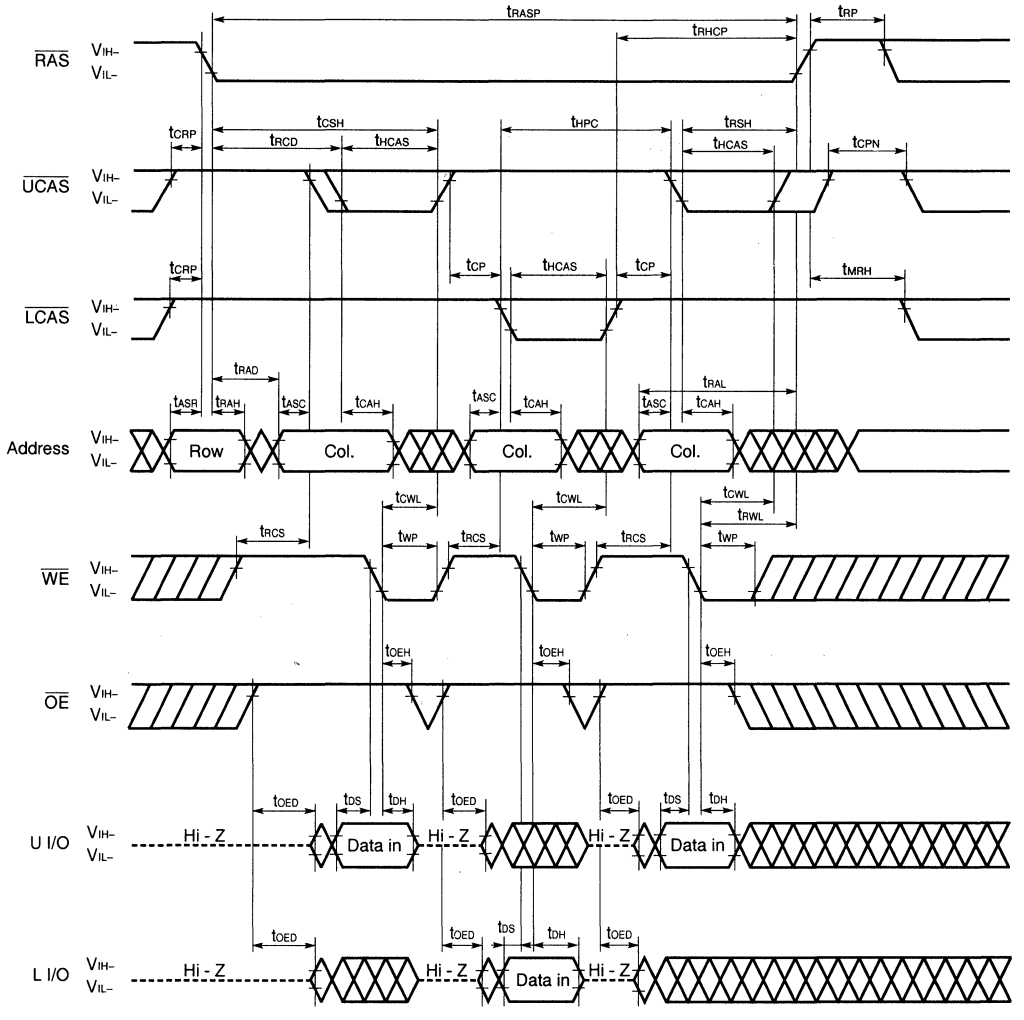
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

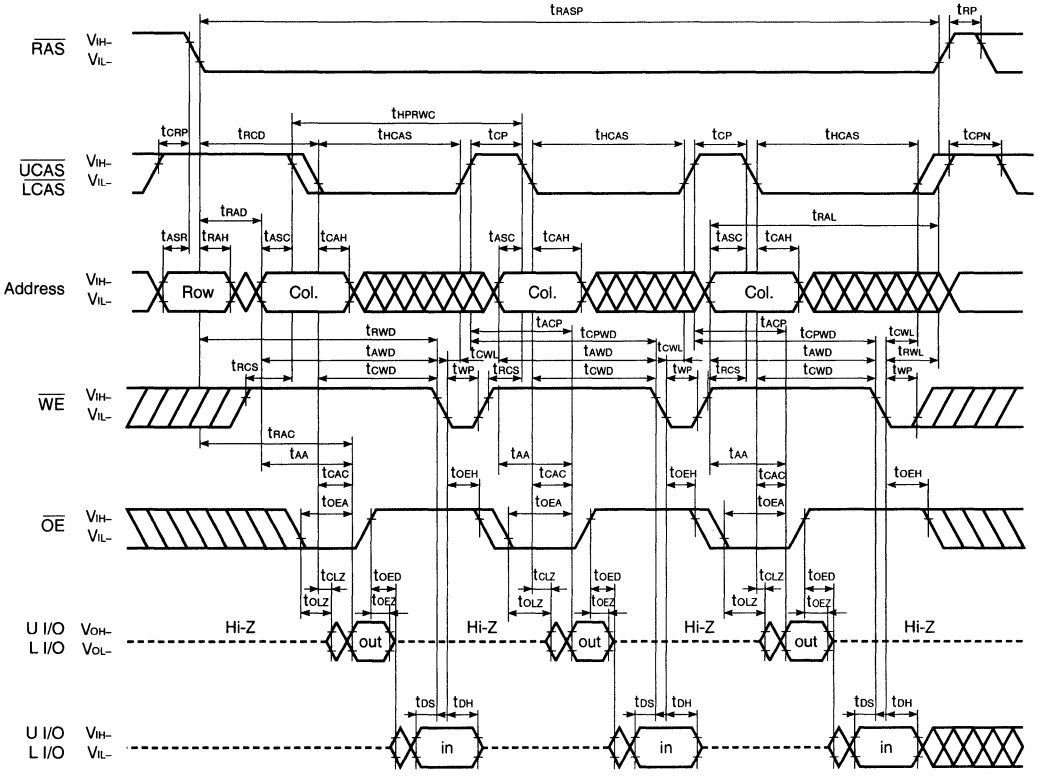
Hyper Page Mode (EDO) Byte Late Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

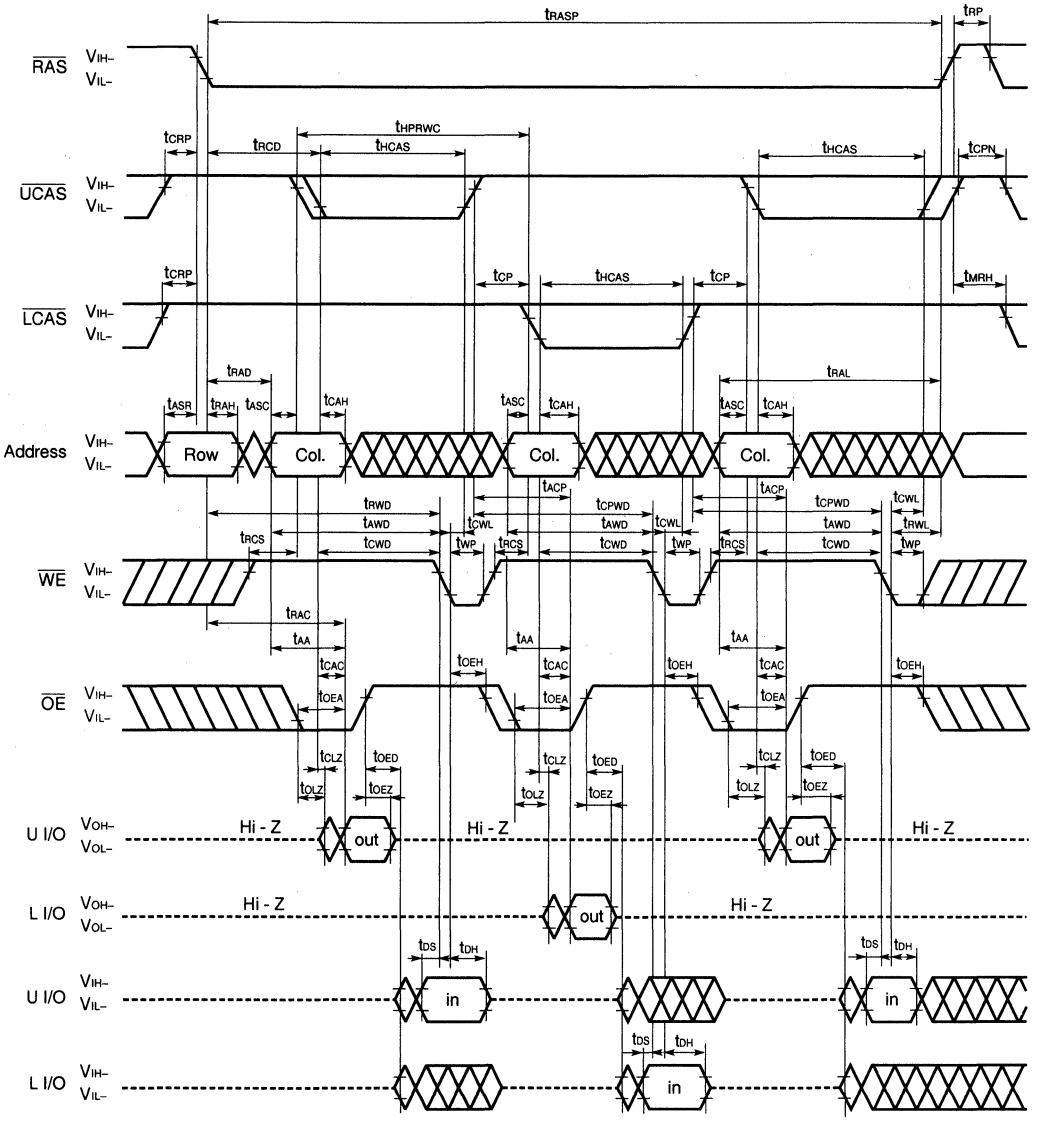
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

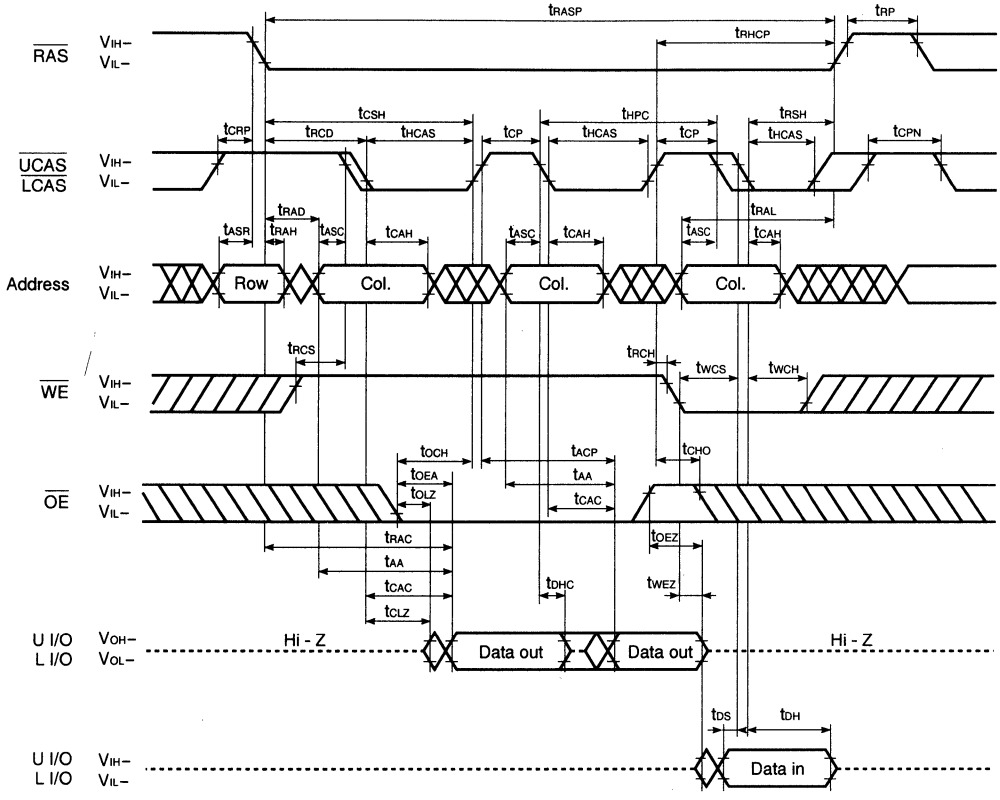
Hyper Page Mode (EDO) Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

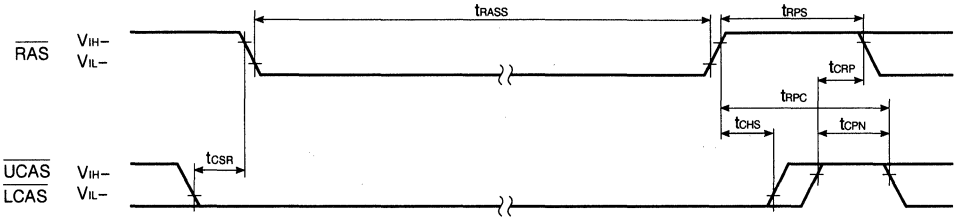
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18165)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

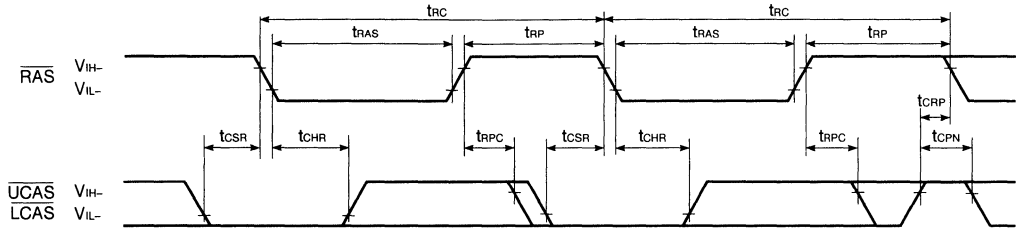
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100$ μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (1,024/128 ms) should be met.

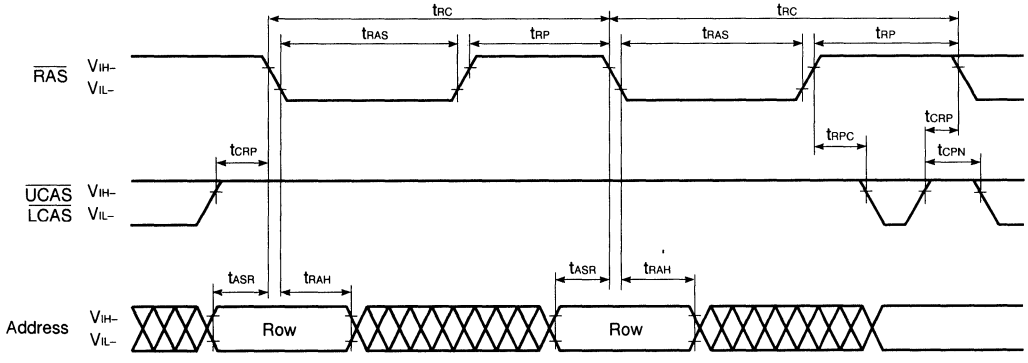
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



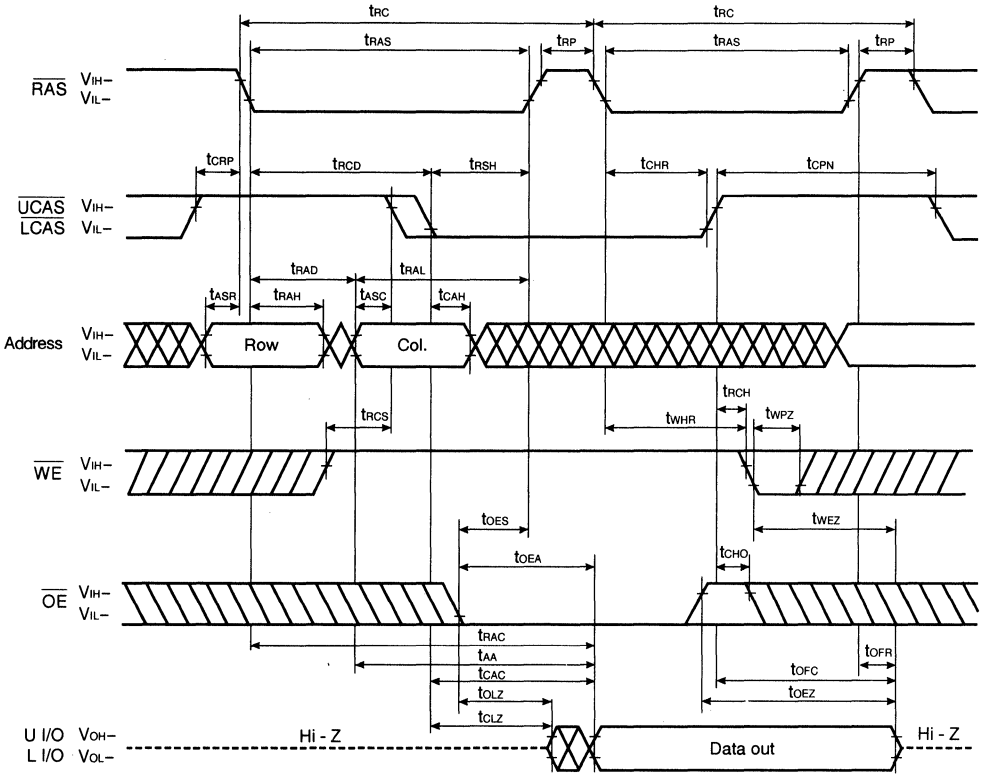
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

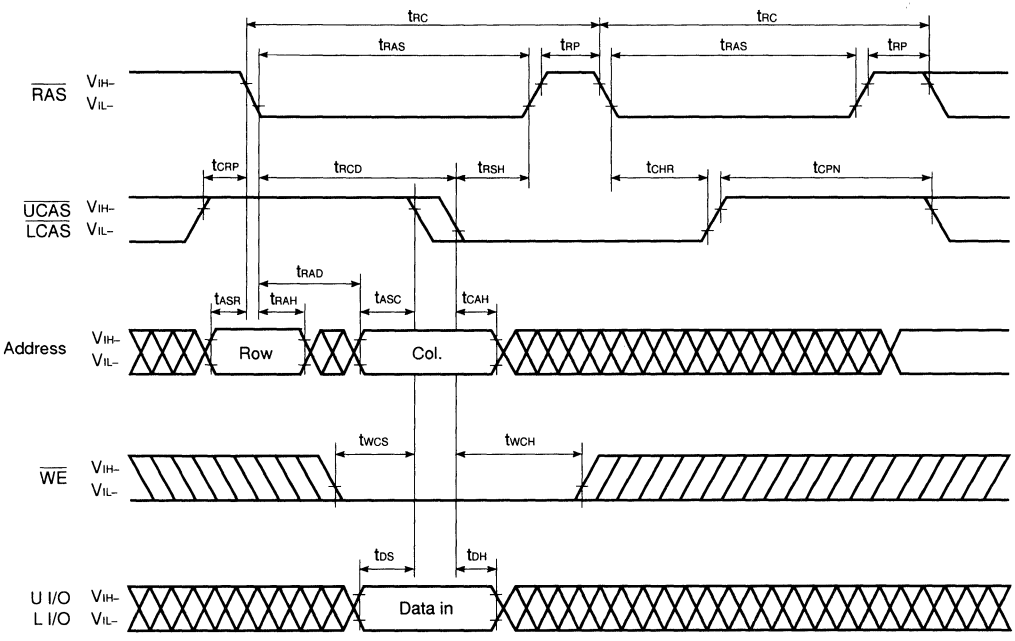


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



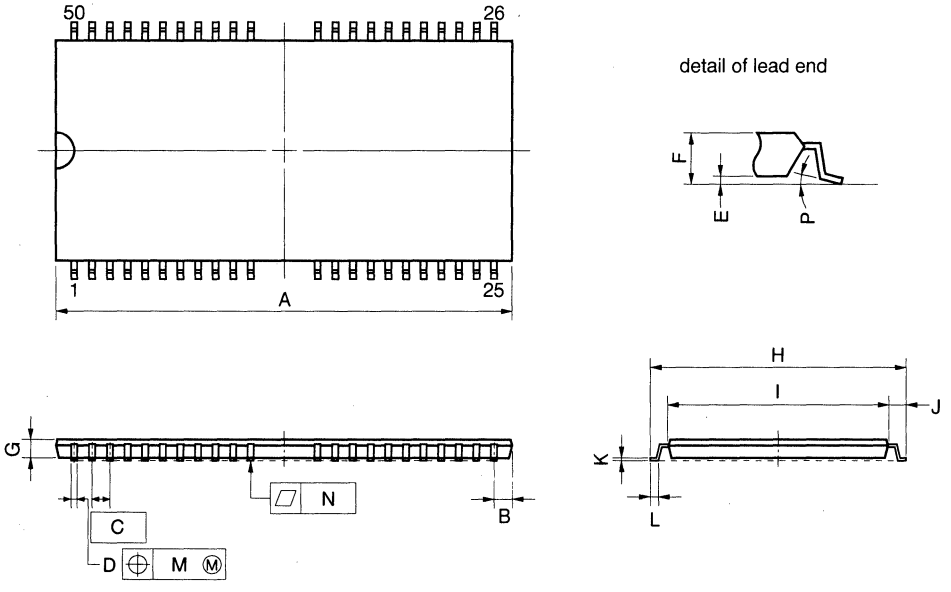
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



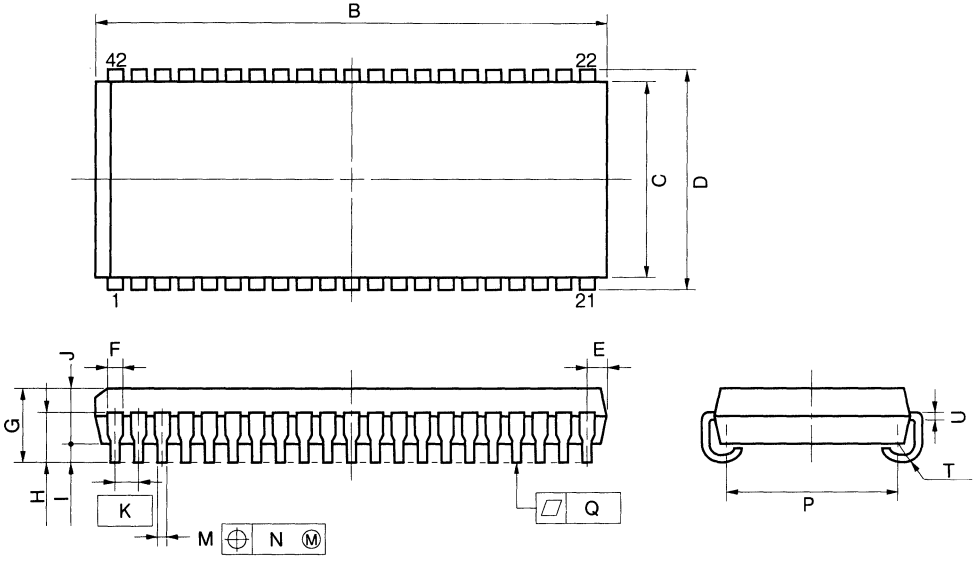
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S18165, 4218165.

Types of Surface Mount Device

μPD42S18165G5, 4218165G5: 50-pin plastic TSOP (II) (400 mil)
μPD42S18165LE, 4218165LE: 42-pin plastic SOJ (400 mil)

Hyper Page Mode (EDO)
16M Dynamic RAM
[3.3V ± 0.3V]

NEC

MOS INTEGRATED CIRCUIT

μPD42S16405L, 4216405L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, HYPER PAGE MODE (EDO)

Description

The μPD42S16405L, 4216405L are 4,194,304 words by 4 bits CMOS dynamic RAM with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S16405L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S16405L, 4216405L are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 4 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S16405L-A60, 4216405L-A60	324 mW	60 ns	104 ns	25 ns
μPD42S16405L-A70, 4216405L-A70	288 mW	70 ns	124 ns	30 ns

- μPD42S16405L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

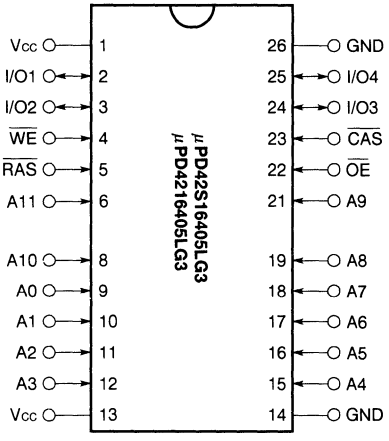
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16405L	4,096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	0.54 mW (CMOS level input)
μPD4216405L	4,096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

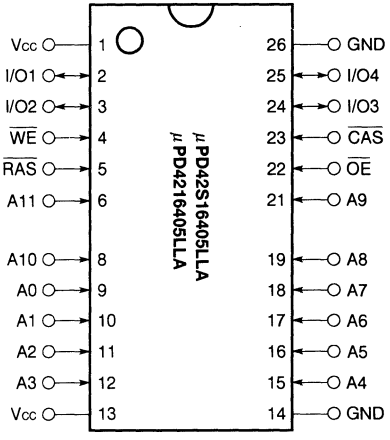
Part number	Access time (MAX.)	Package	Refresh
μPD42S16405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S16405LG3-A70	70 ns		
μPD42S16405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD42S16405LLA-A70	70 ns		
μPD4216405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4216405LG3-A70	70 ns		
μPD4216405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4216405LLA-A70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

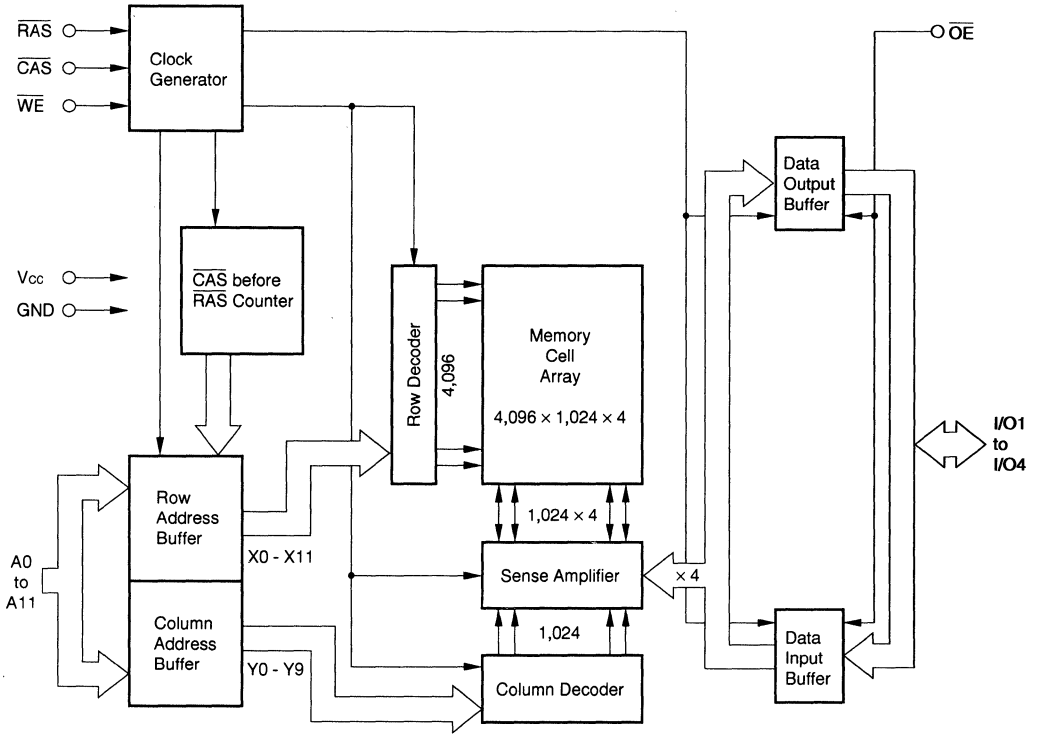


26-pin Plastic SOJ (300 mil)



A0 to A11 : Address Inputs
I/O1 to I/O4: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD42S16405L, 4216405L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 12-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Hyper Page Mode (EDO)

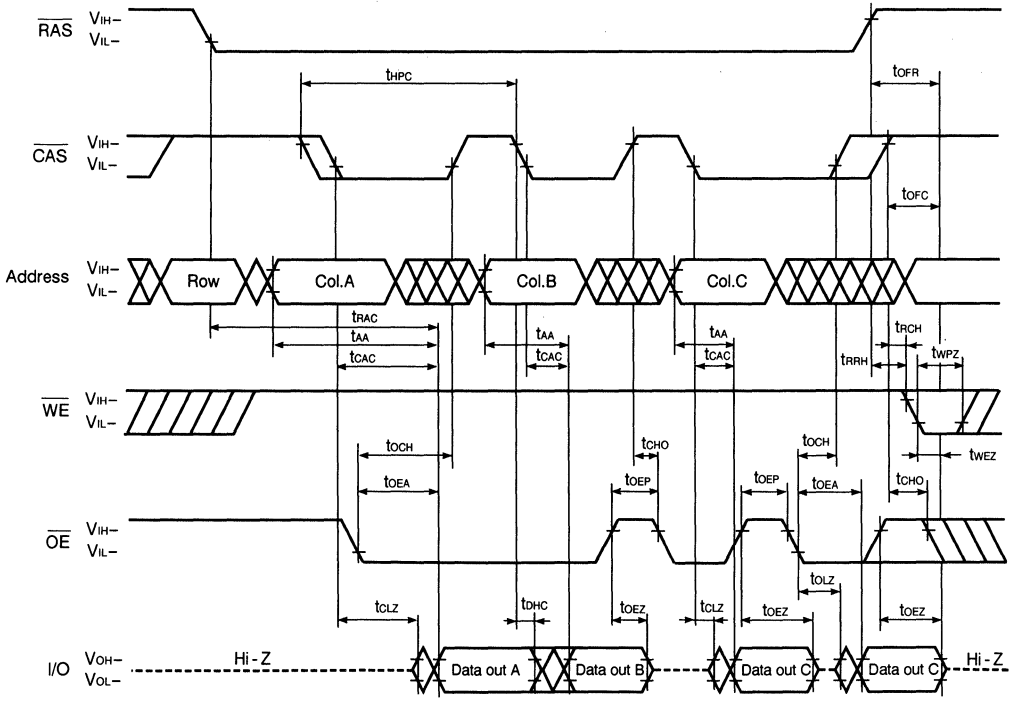
The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. **Data output time is extended.**
   In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode .**
   In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		80	mA	1, 2, 3
				t_{RAC} = 70 ns		70		
Standby current	μPD42S16405L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.15		
	μPD4216405L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		80	mA	1, 2, 3, 4
				t_{RAC} = 70 ns		70		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		80	mA	1, 2
				t_{RAC} = 70 ns		70		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16405L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq 0.2$ V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		220	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16405L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq 0.2$ V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

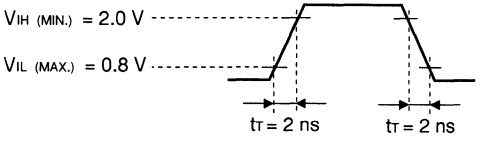
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

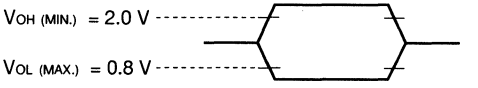
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

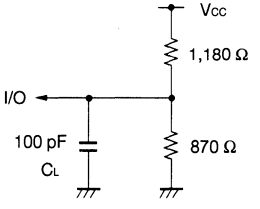
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes	
			MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time		tRC	104	–	124	–	ns		
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns		
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns		
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1	
$\overline{CAS}$ pulse width		tCAS	10	10,000	12	10,000	ns		
$\overline{RAS}$ hold time		tRSH	15	–	20	–	ns		★
$\overline{CAS}$ hold time		tCSH	45	–	50	–	ns		★
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	14	45	14	52	ns	2	
$\overline{RAS}$ to column address delay time		tRAD	12	30	12	35	ns	2	
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3	
Row address setup time		tASR	0	–	0	–	ns		
Row address hold time		tRAH	10	–	10	–	ns		
Column address setup time		tASC	0	–	0	–	ns		
Column address hold time		tCAH	10	–	12	–	ns		
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns		
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns		
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns		
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns		
Transition time (rise and fall)		tT	1	50	1	50	ns		
Refresh time	μPD42S16405L	tREF	–	128	–	128	ms	4	
	μPD4216405L		–	64	–	64			

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16405L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	20	–	ns	★
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

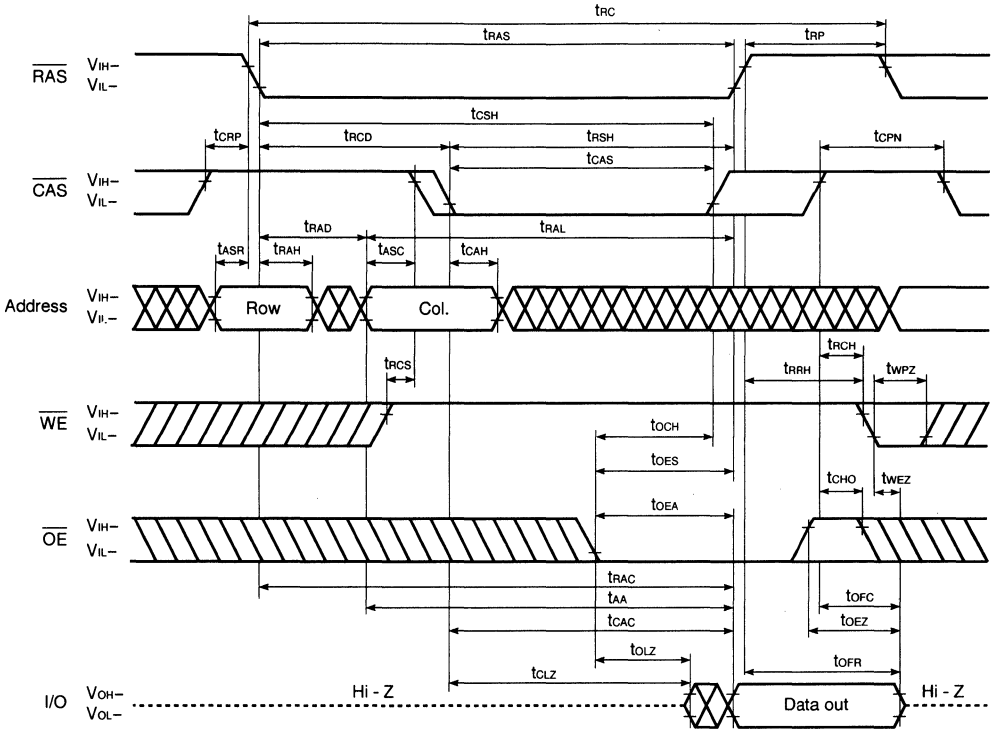
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

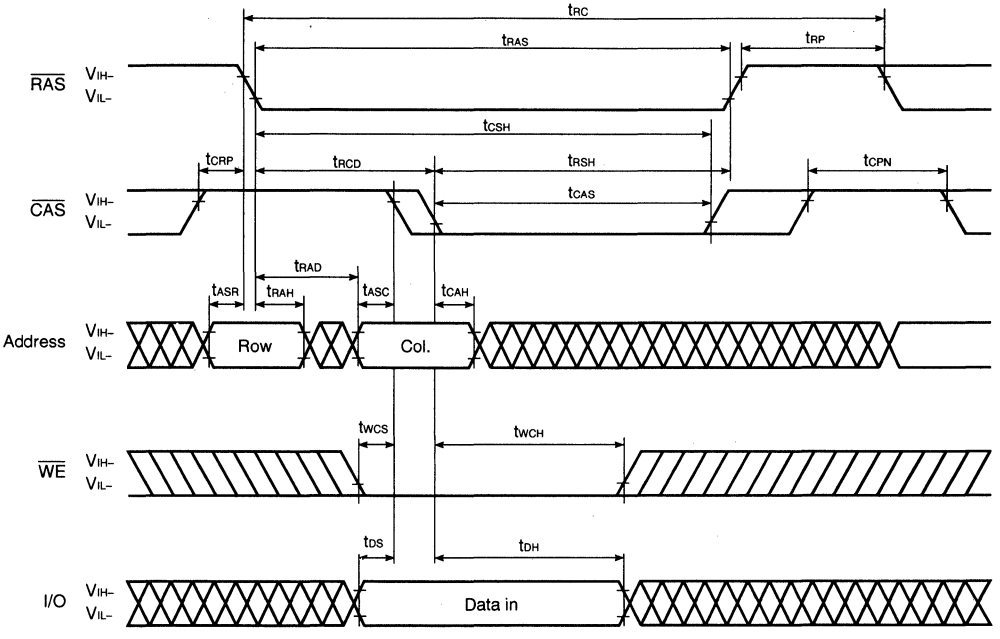
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16405L.

Read Cycle

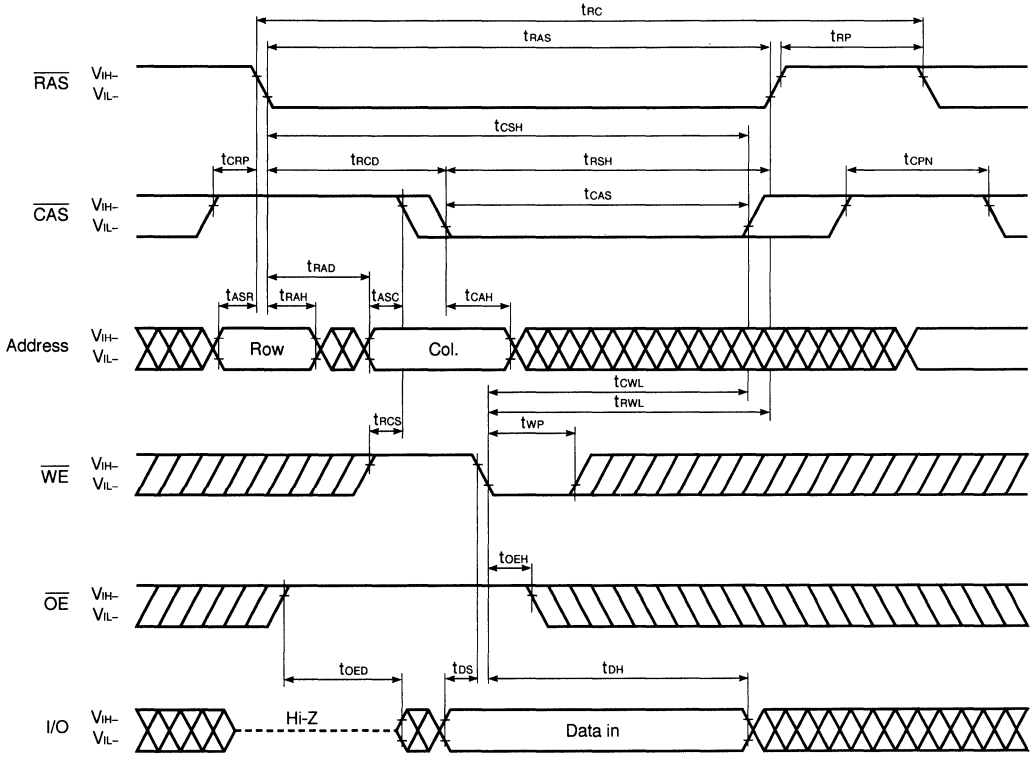

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

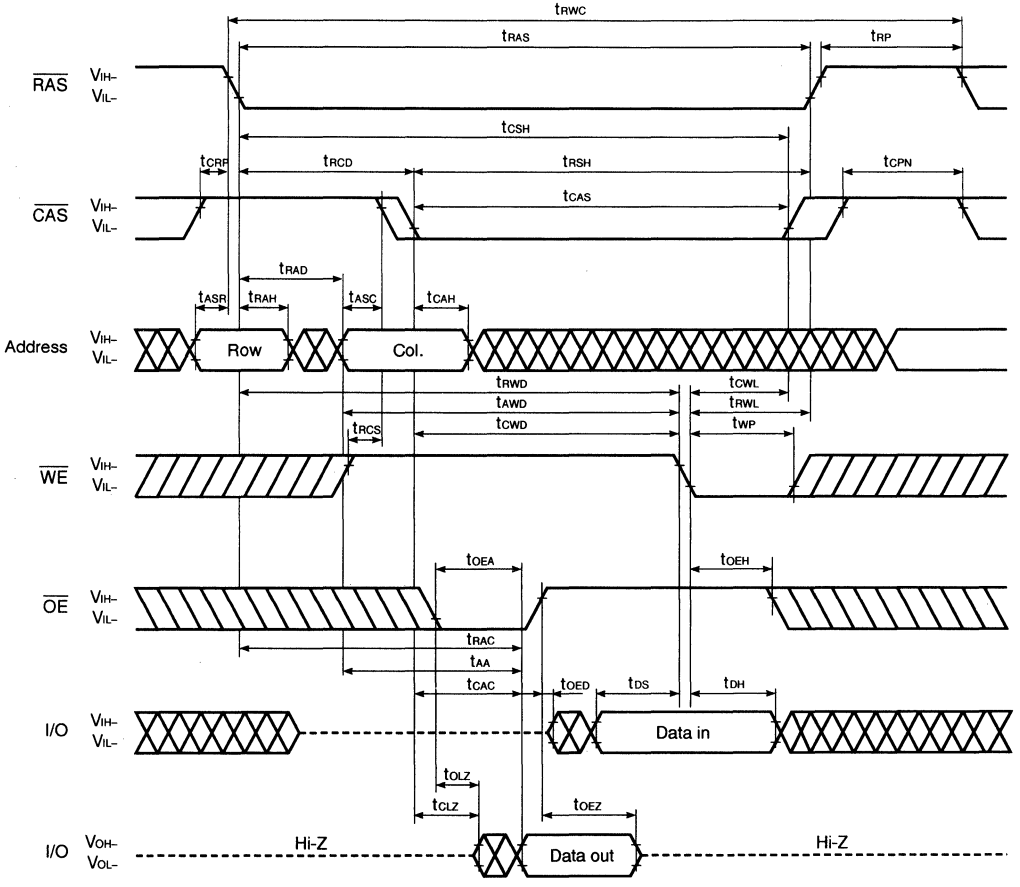


Remark $\overline{OE}$: Don't care

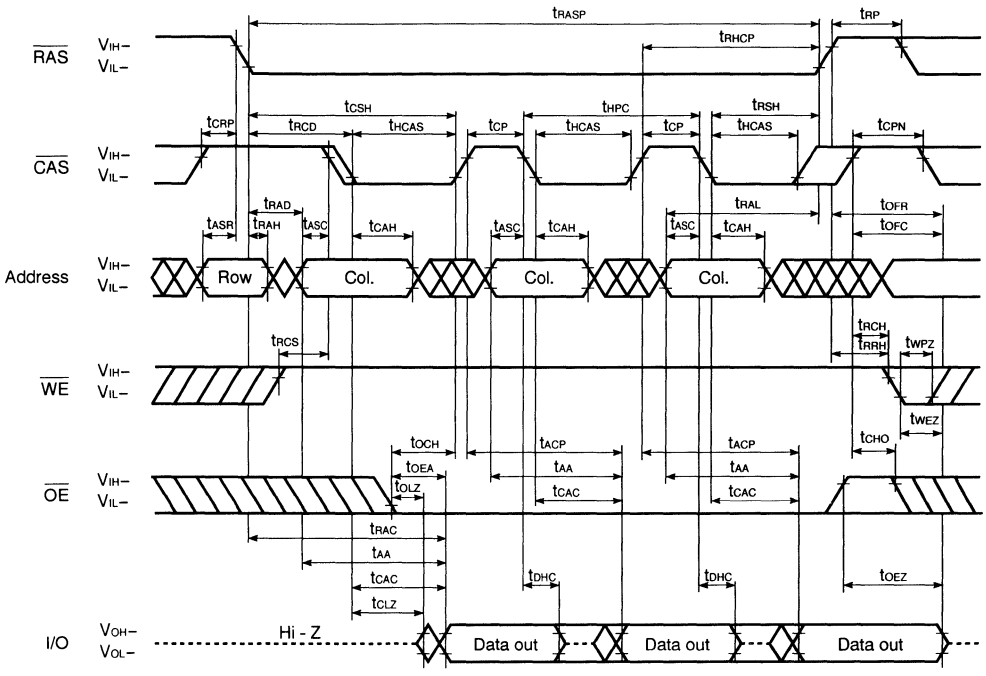
Late Write Cycle



Read Modify Write Cycle

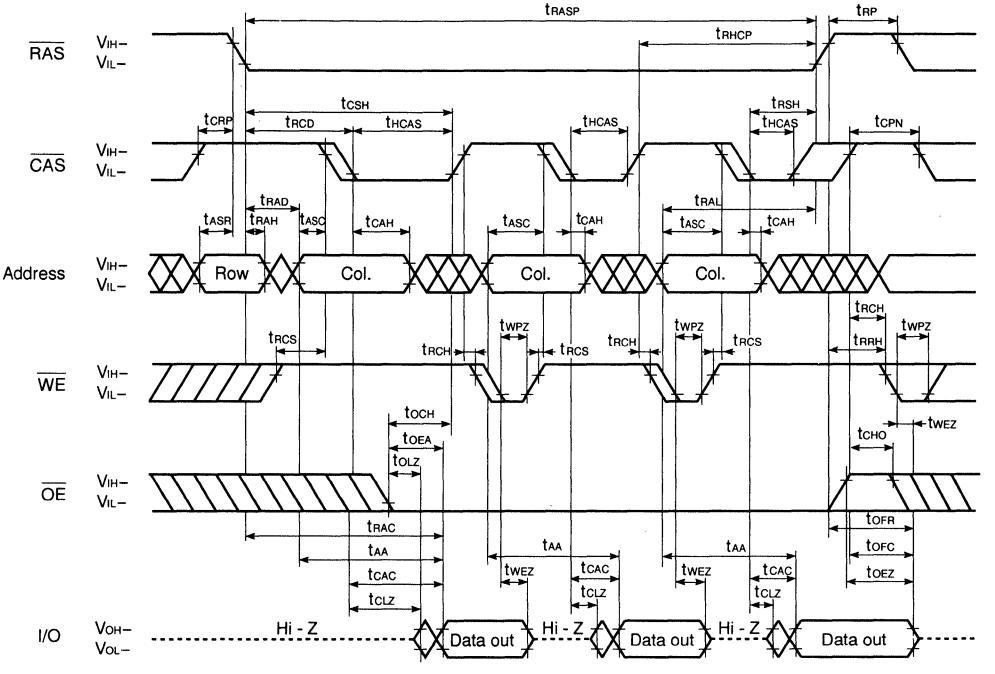


Hyper Page Mode (EDO) Read Cycle



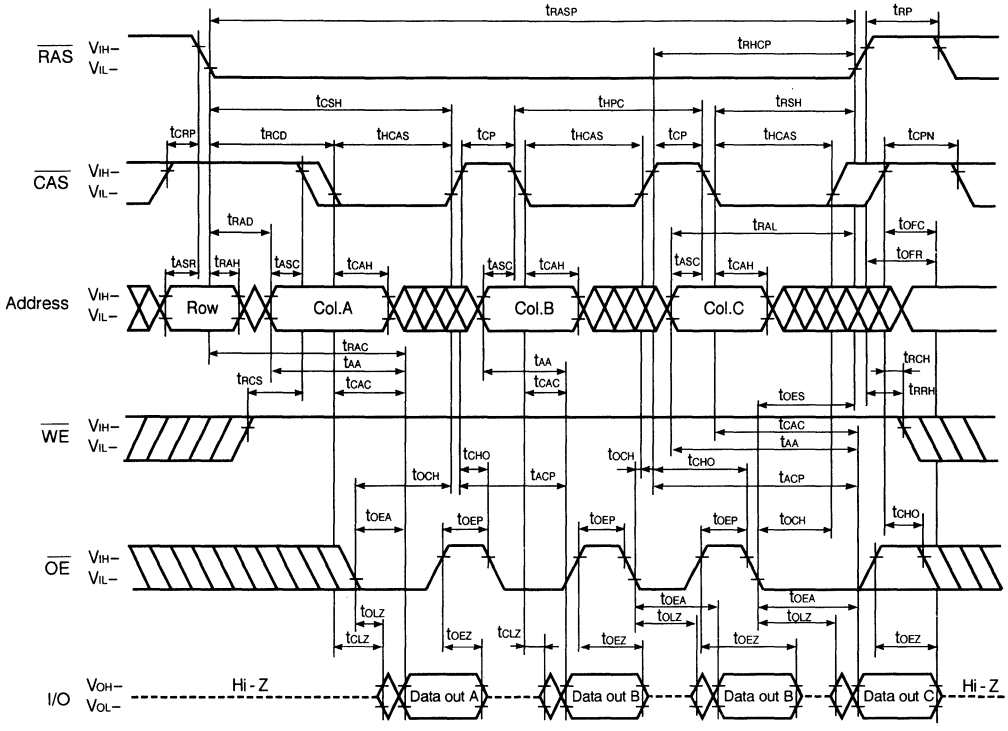
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



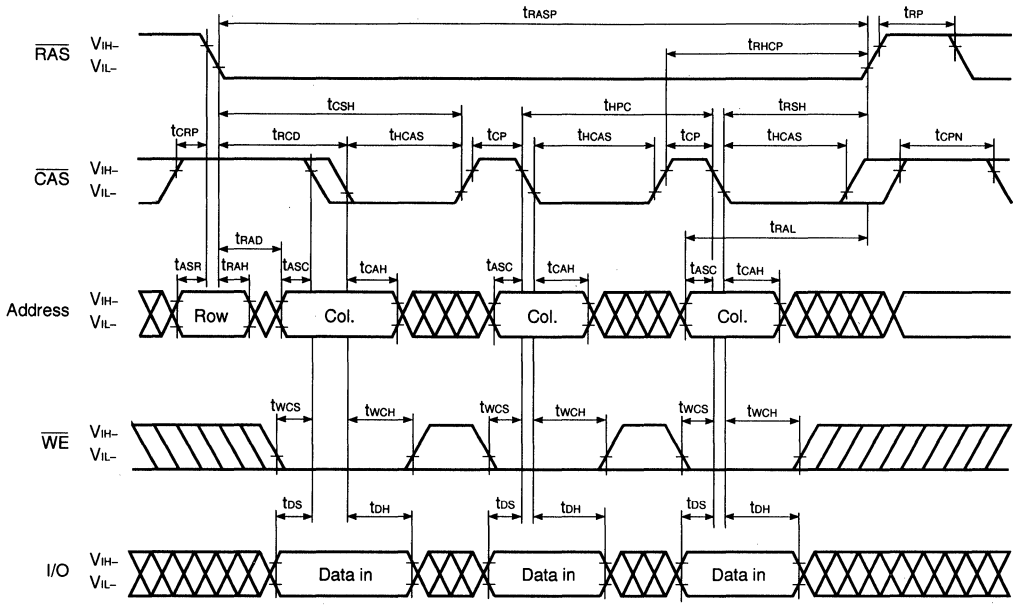
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

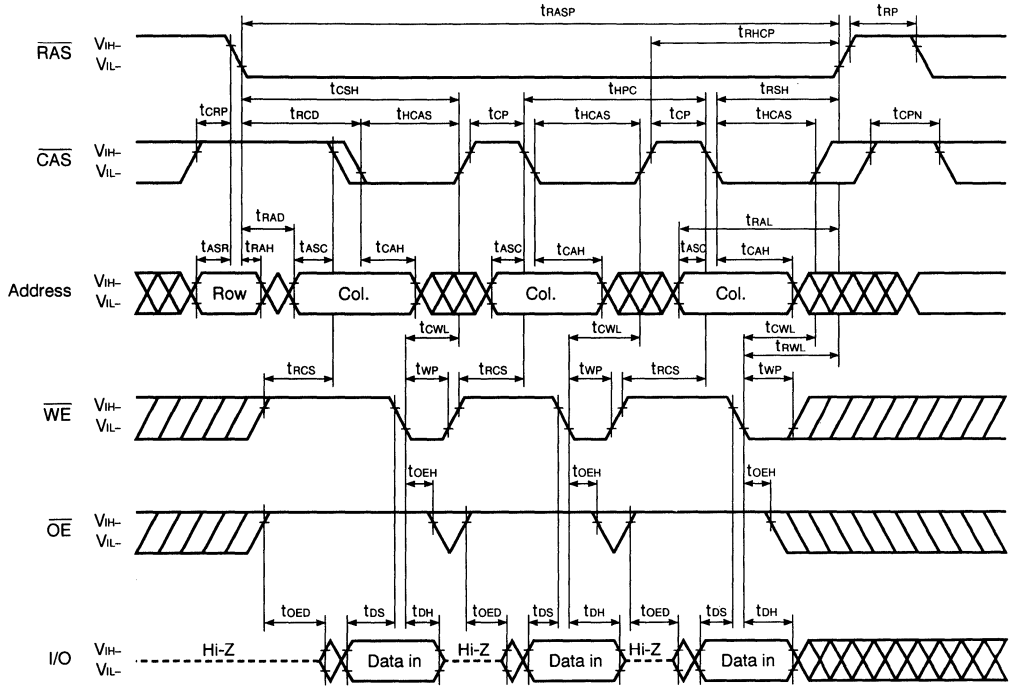
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

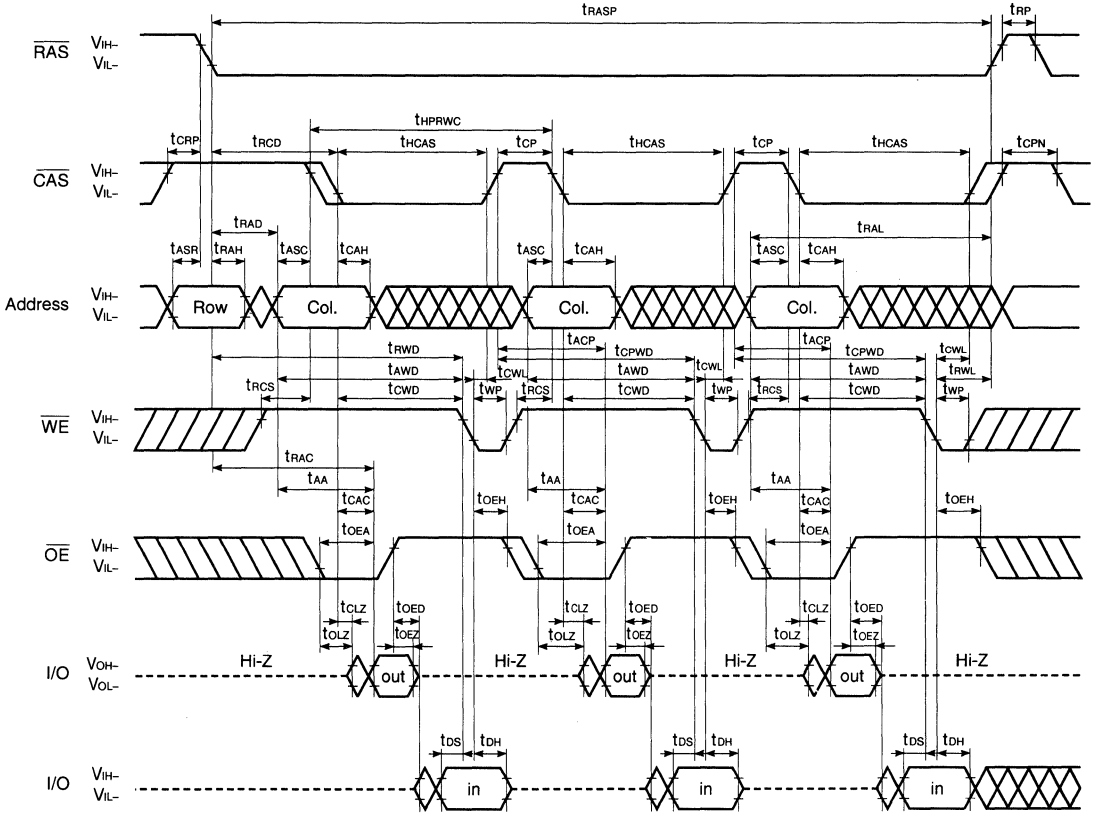
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



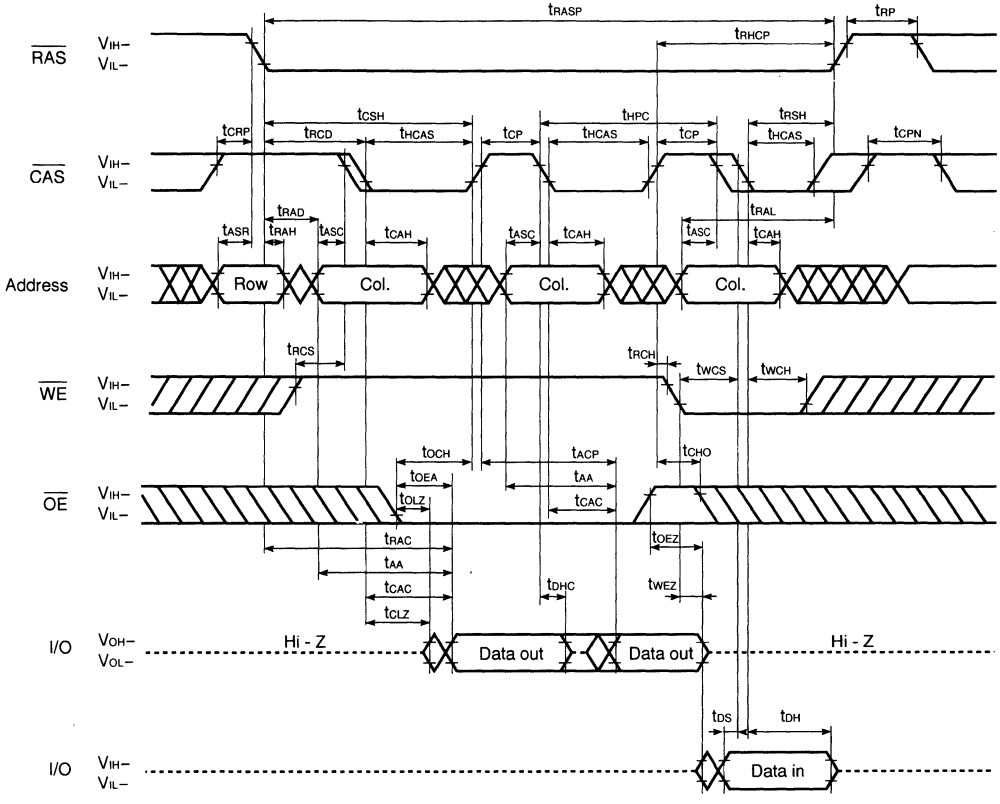
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



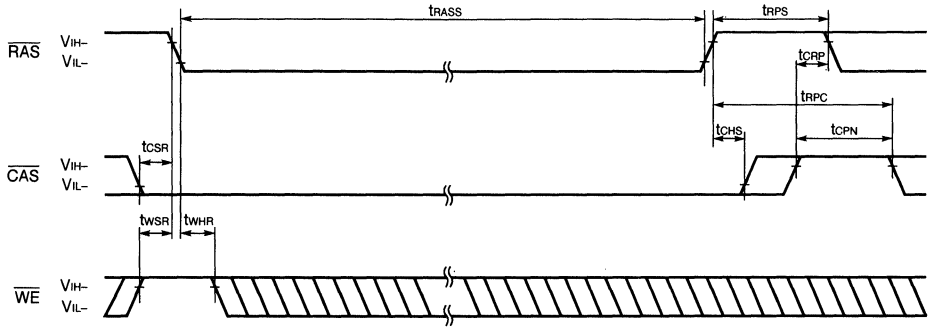
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16405L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

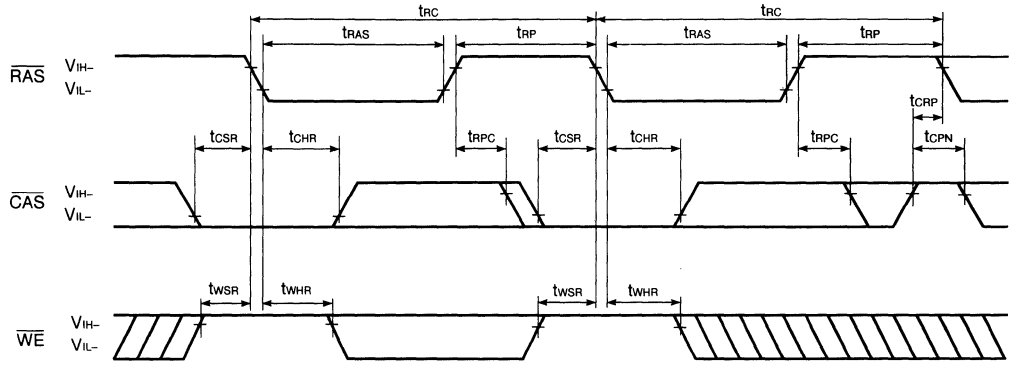
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (4,096/128 ms) should be met.

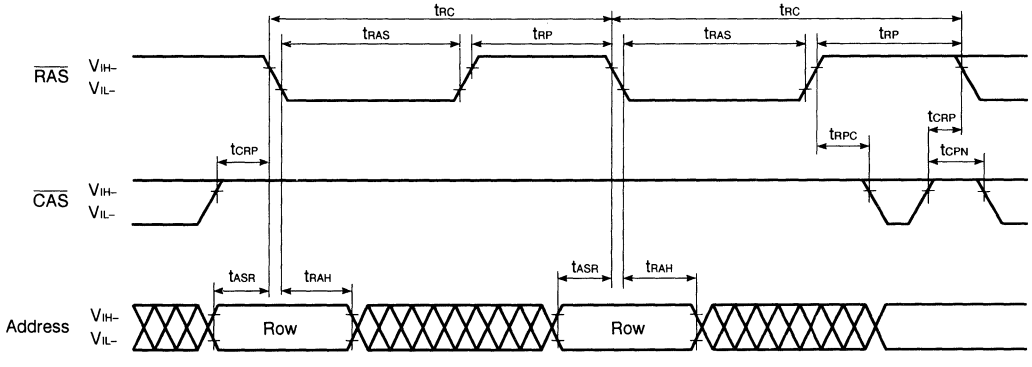
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



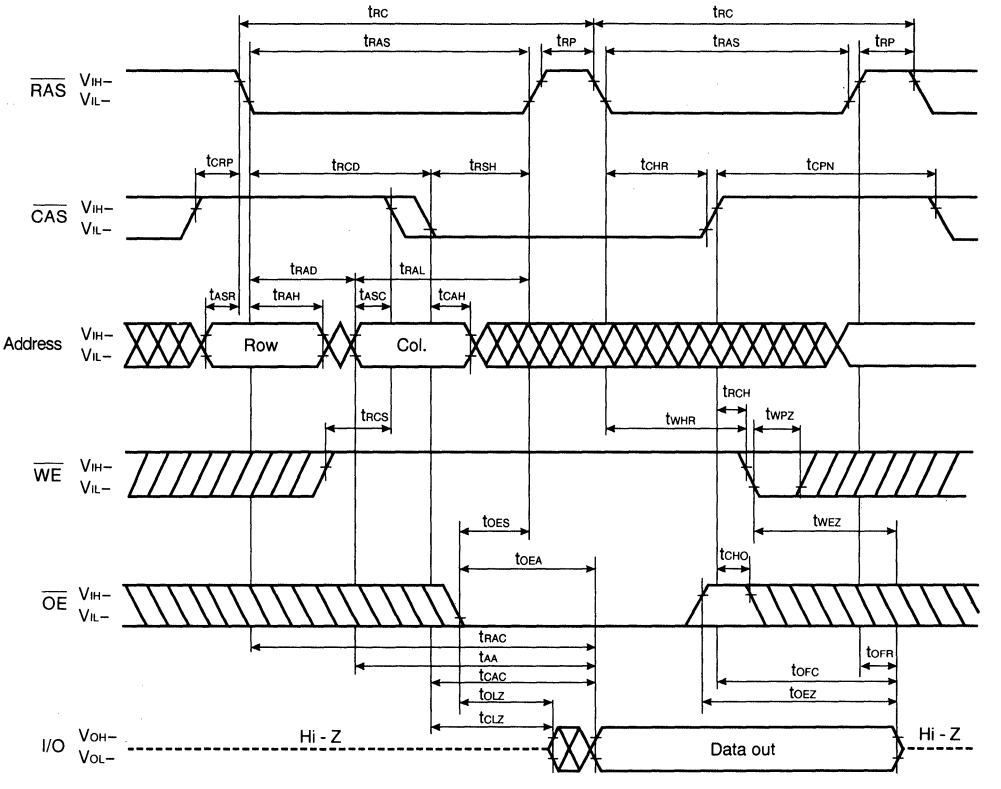
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

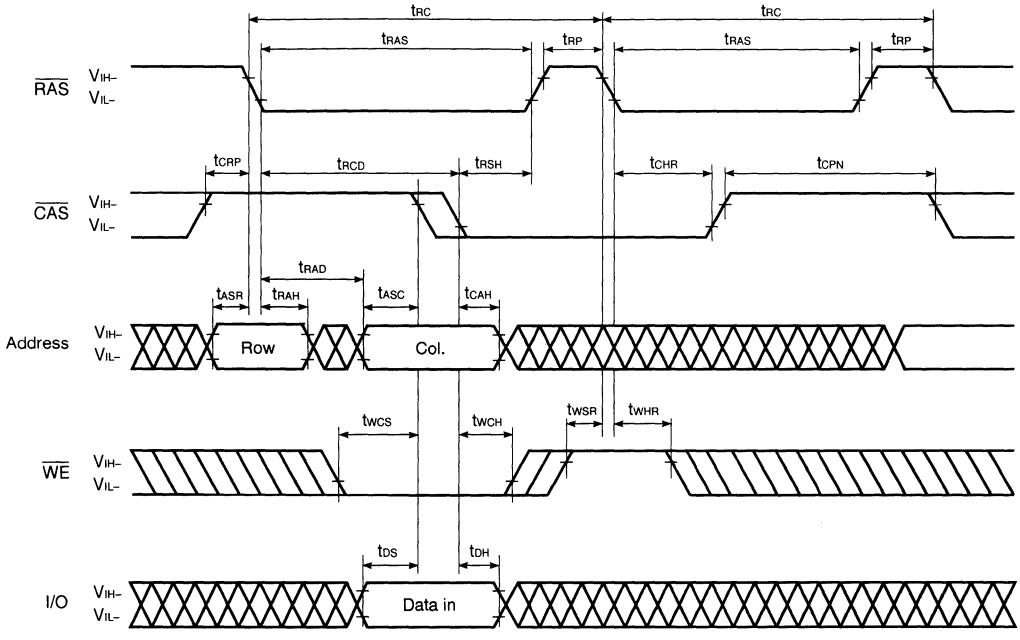


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

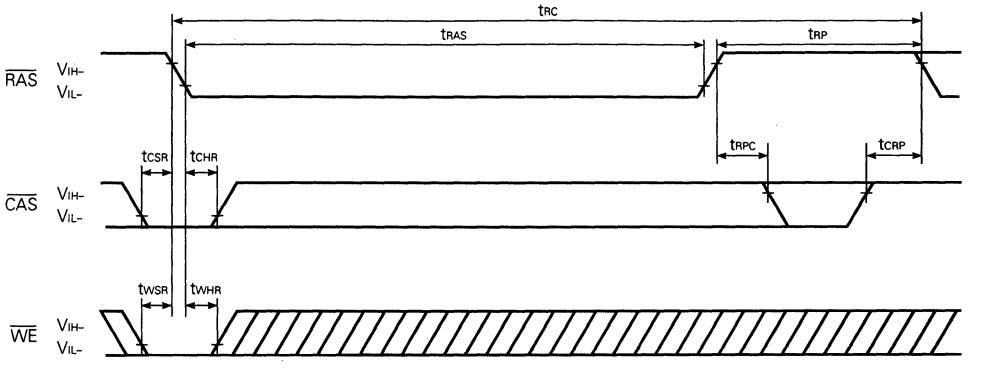


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

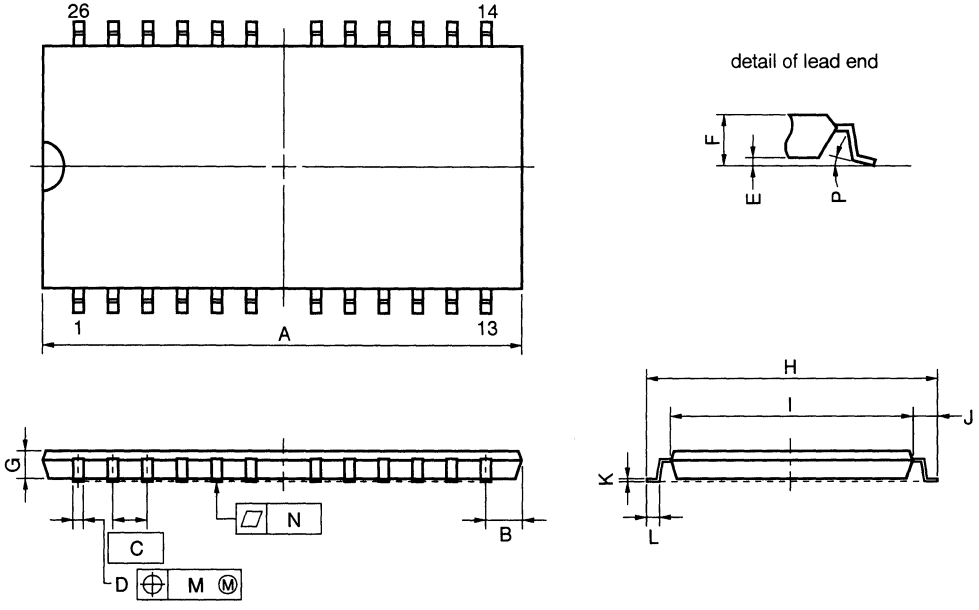
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



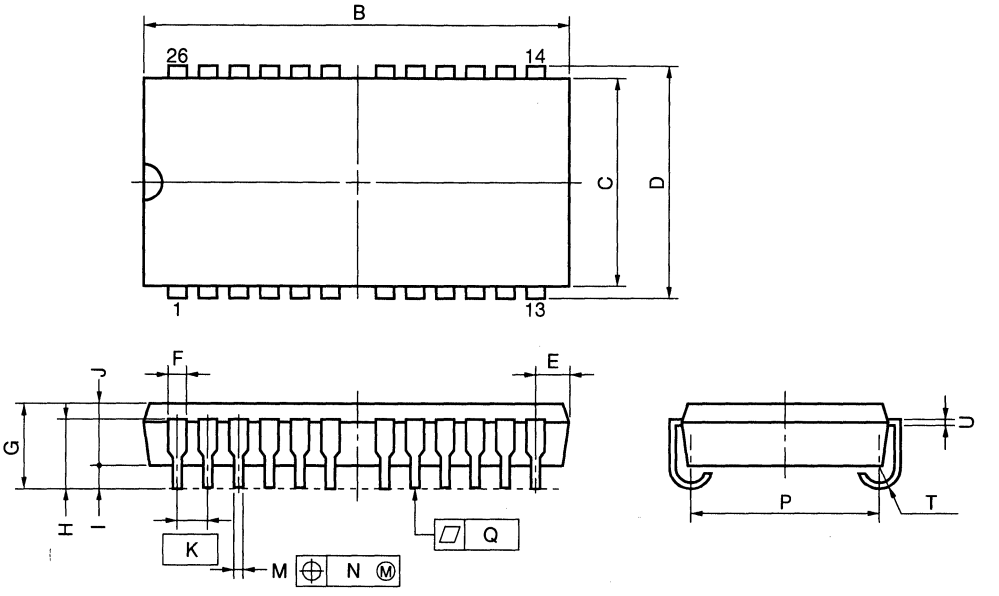
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16405L, 4216405L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16405LG3, 4216405LG3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16405LLA, 4216405LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S17405L, 4217405L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, HYPER PAGE MODE (EDO)

Description

The μPD42S17405L, 4217405L are 4,194,304 words by 4 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S17405L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S17405L, 4217405L are packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 4,194,304 words by 4 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S17405L-A60, 4217405L-A60	360 mW	60 ns	104 ns	25 ns
μPD42S17405L-A70, 4217405L-A70	324 mW	70 ns	124 ns	30 ns

- μPD42S17405L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

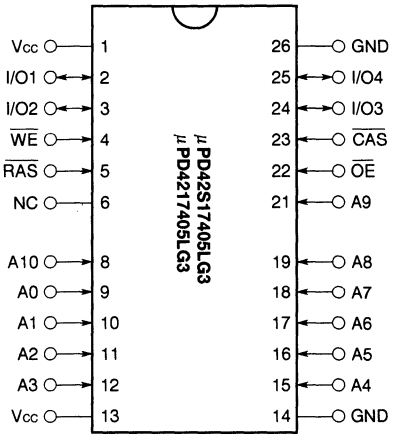
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17405L	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	0.54 mW (CMOS level input)
μPD4217405L	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

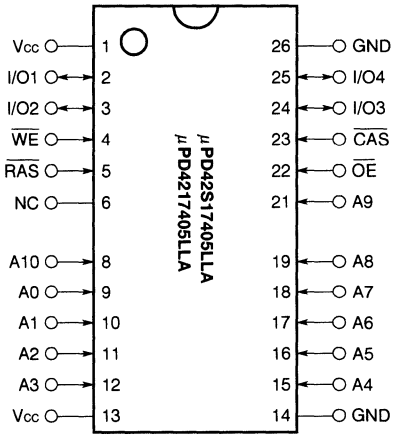
Part number	Access time (MAX.)	Package	Refresh
μPD42S17405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17405LG3-A70	70 ns		
μPD42S17405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD42S17405LLA-A70	70 ns		
μPD4217405LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217405LG3-A70	70 ns		
μPD4217405LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4217405LLA-A70	70 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

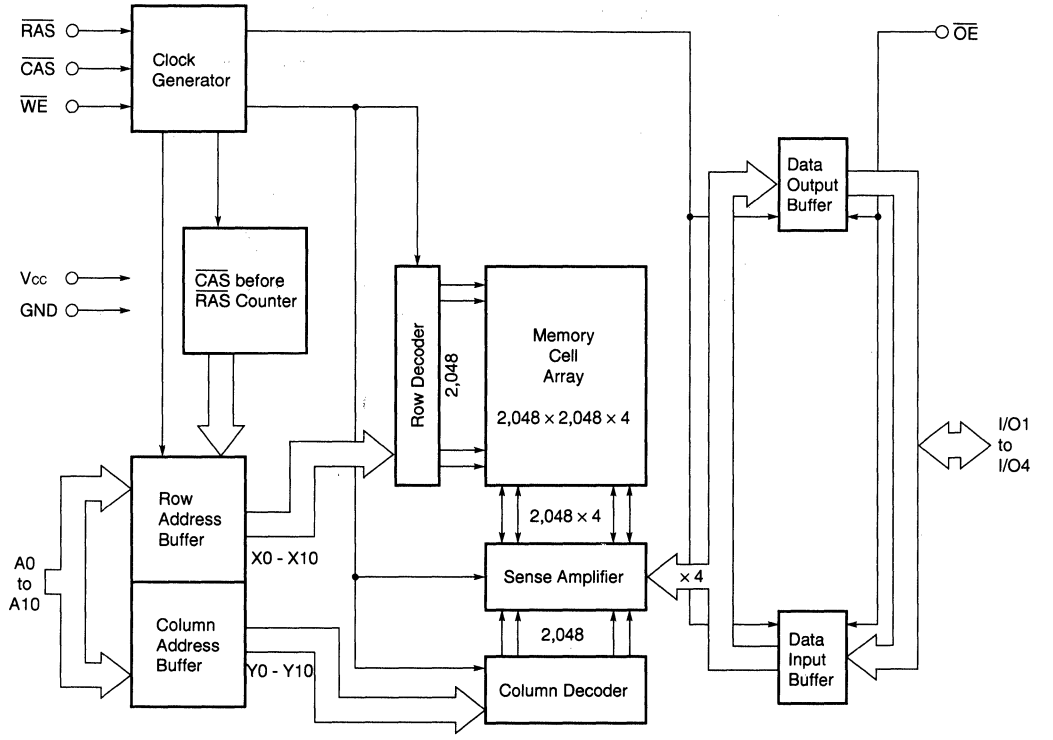


26-pin Plastic SOJ (300 mil)



A0 to A10 : Address Inputs
I/O1 to I/O4: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17405L, 4217405L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A10 and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper 11-bit and lower 11-bit in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

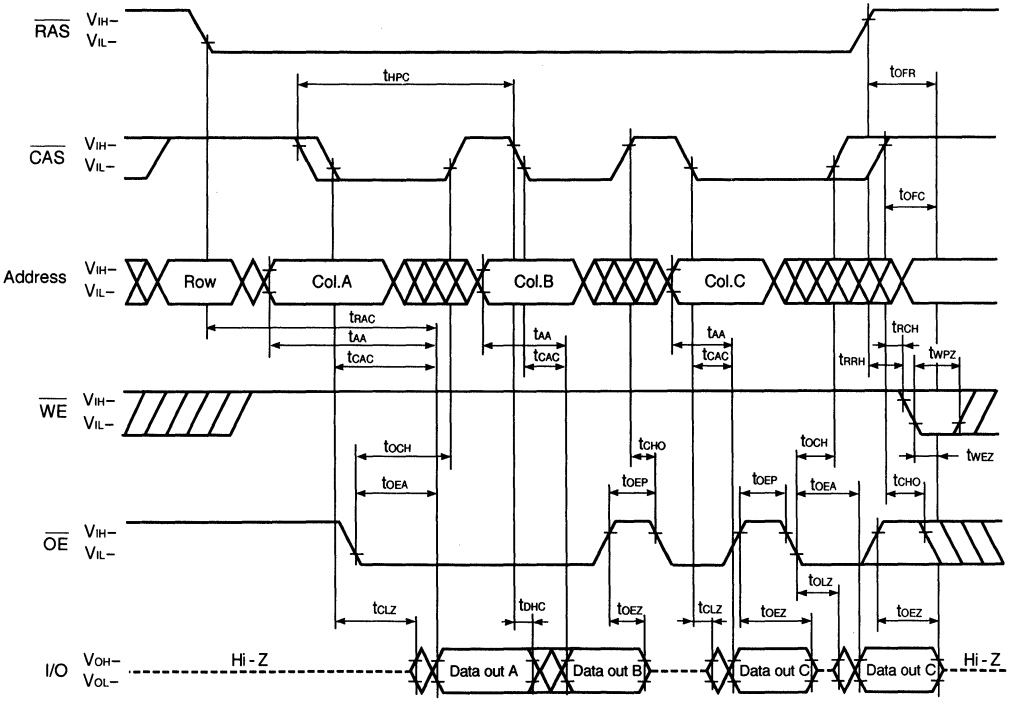
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2, 3
				t_{RAC} = 70 ns		90		
Standby current	μPD42S17405L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4217405L		$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2, 3, 4
				t_{RAC} = 70 ns		90		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2
				t_{RAC} = 70 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17405L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		200	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17405L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$ and $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$.

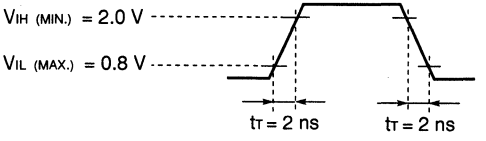
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

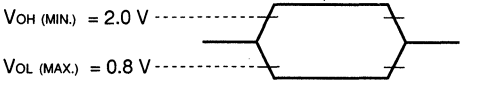
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

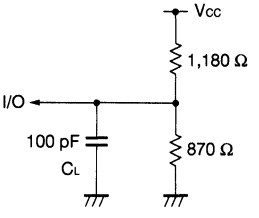
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes	
			MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time		tRC	104	–	124	–	ns		
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns		
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns		
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1	
$\overline{CAS}$ pulse width		tCAS	10	10,000	12	10,000	ns		
$\overline{RAS}$ hold time		tRSH	15	–	20	–	ns		★
$\overline{CAS}$ hold time		tCSH	45	–	50	–	ns		★
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	14	45	14	52	ns	2	
$\overline{RAS}$ to column address delay time		tRAD	12	30	12	35	ns	2	
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3	
Row address setup time		tASR	0	–	0	–	ns		
Row address hold time		tRAH	10	–	10	–	ns		
Column address setup time		tASC	0	–	0	–	ns		
Column address hold time		tCAH	10	–	12	–	ns		
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns		
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns		
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns		
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns		
Transition time (rise and fall)		tT	1	50	1	50	ns		
Refresh time	μPD42S17405L	tREF	–	128	–	128	ms	4	
	μPD4217405L		–	32	–	32			

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S17405L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

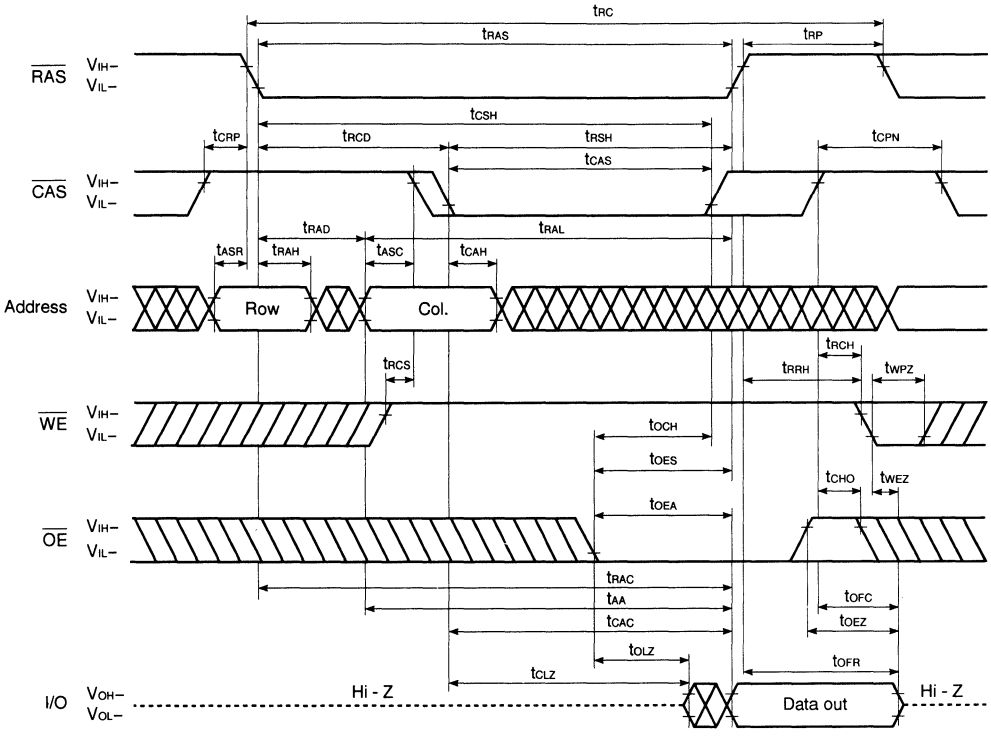
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

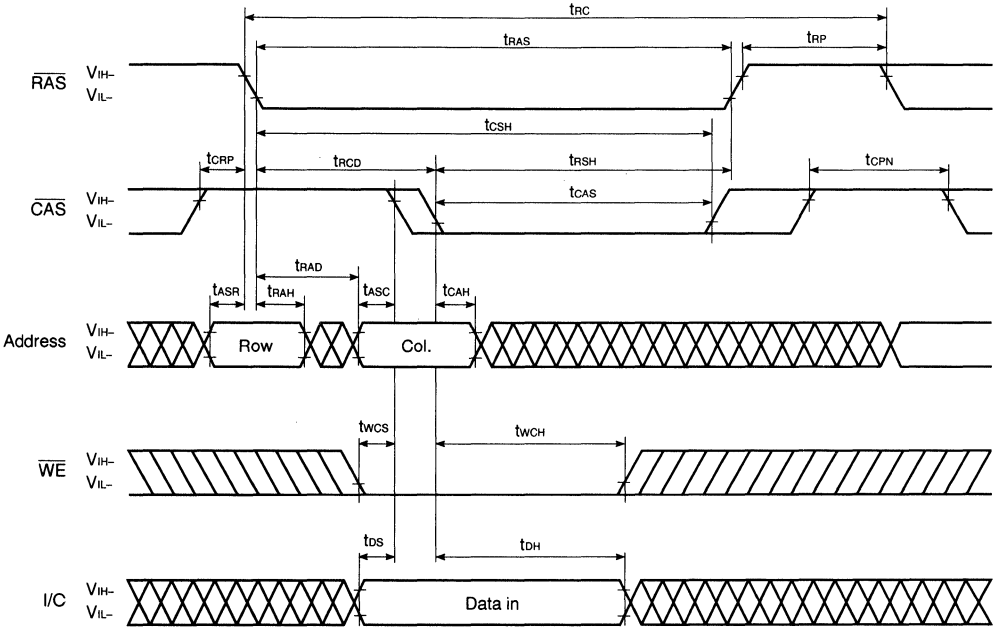
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17405L.

Read Cycle

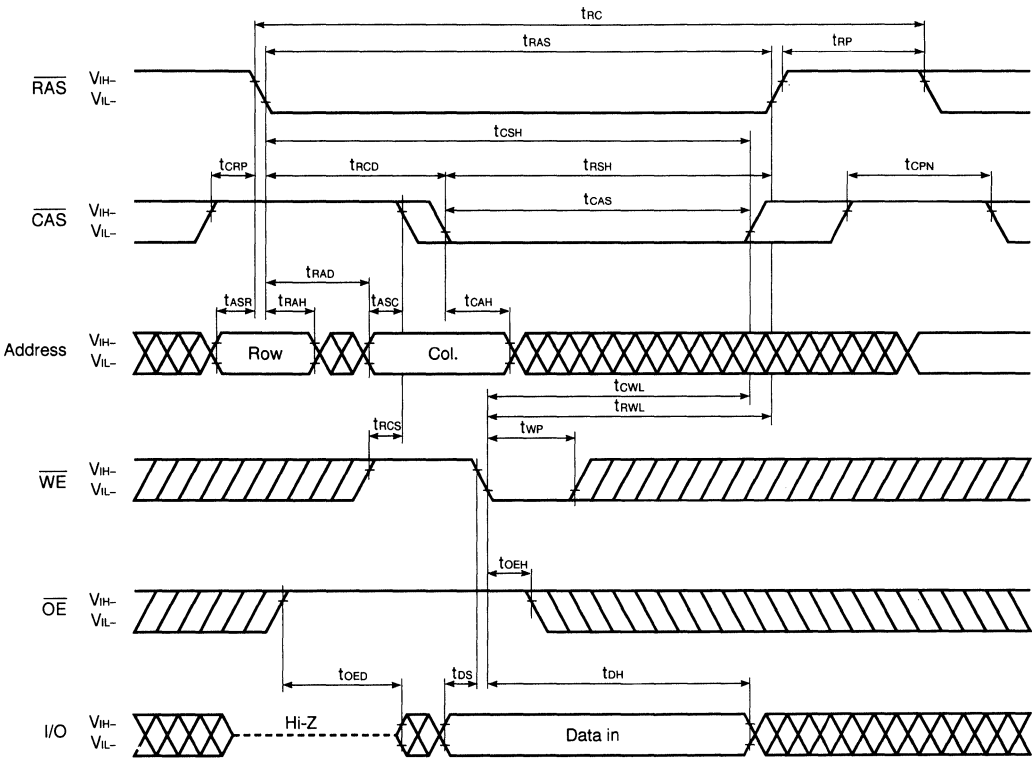

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

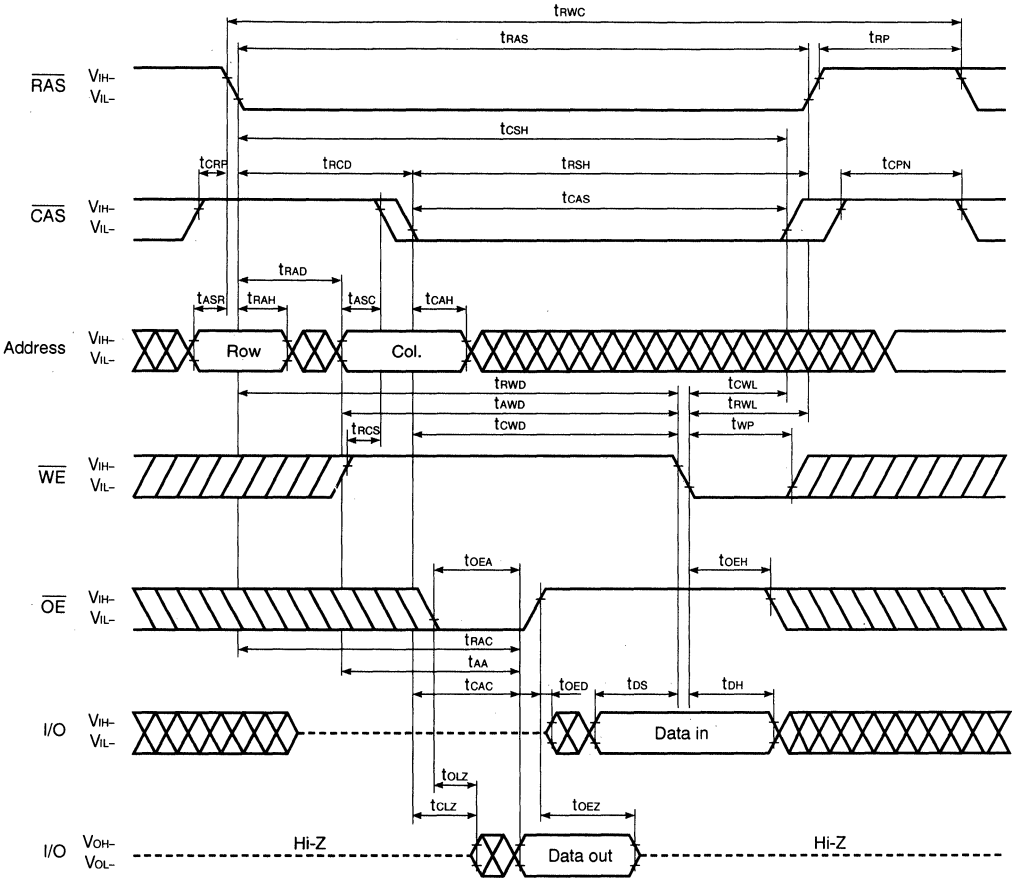


Remark $\overline{OE}$: Don't care

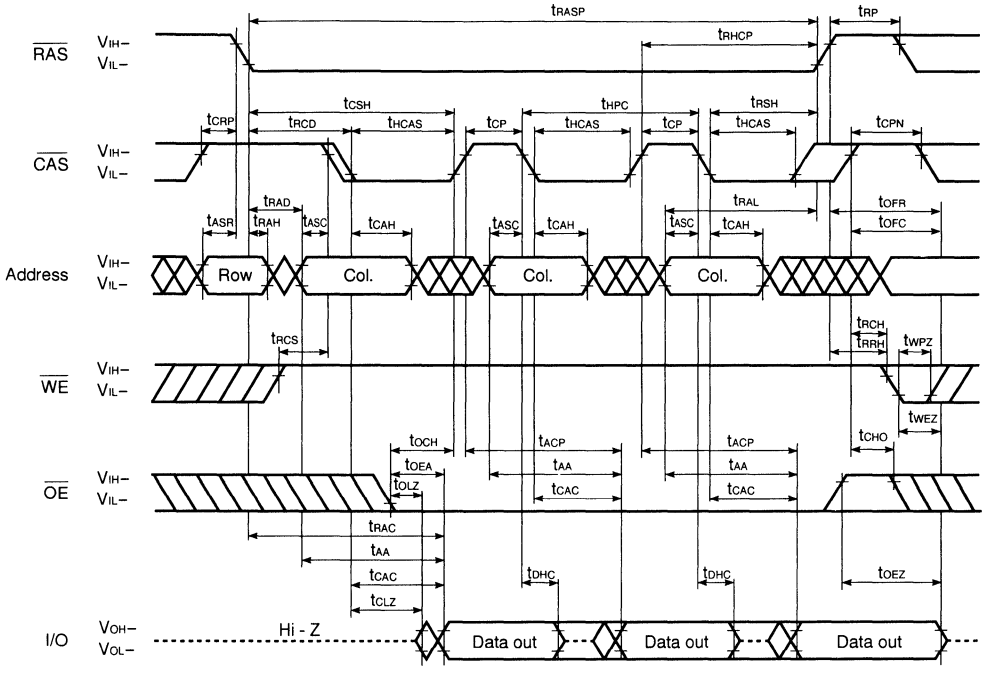
Late Write Cycle



Read Modify Write Cycle

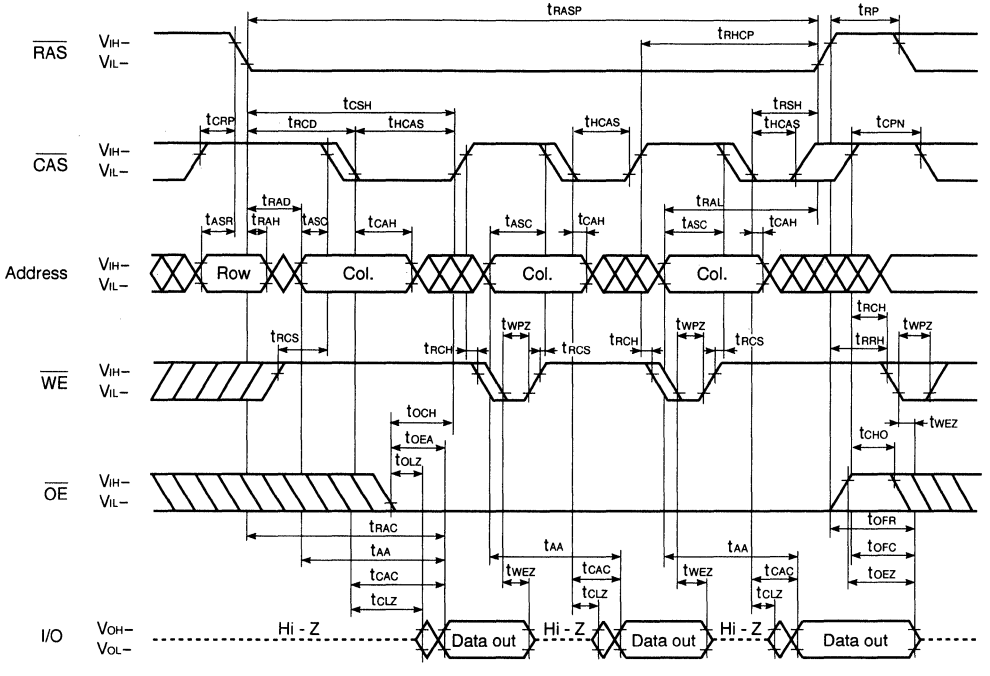


Hyper Page Mode (EDO) Read Cycle



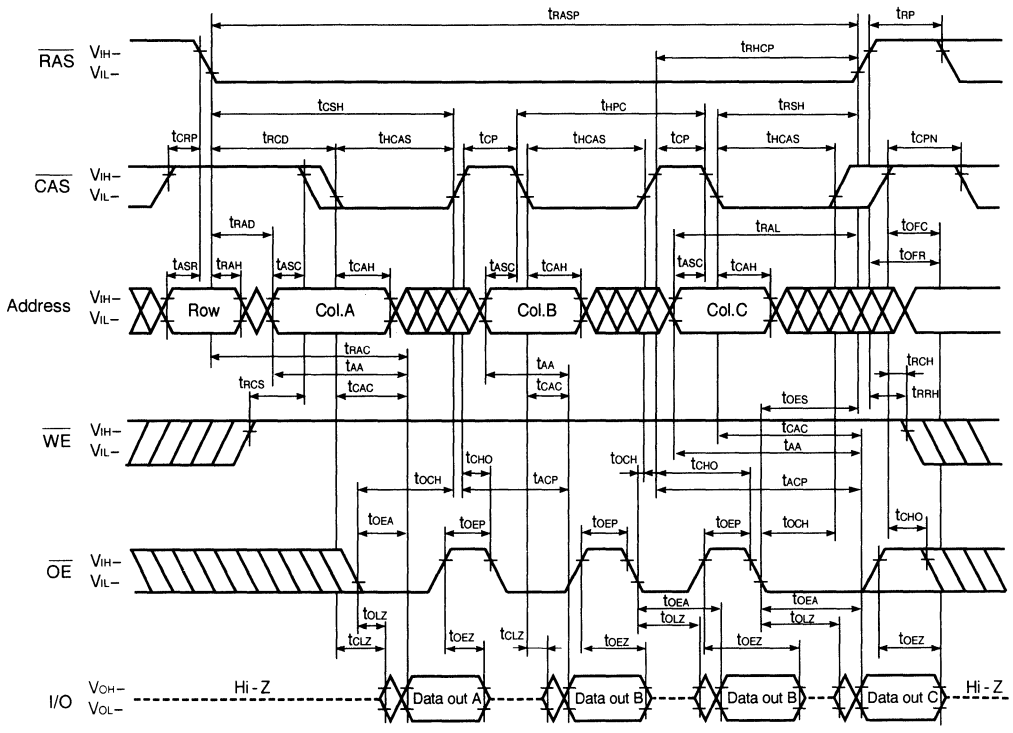
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



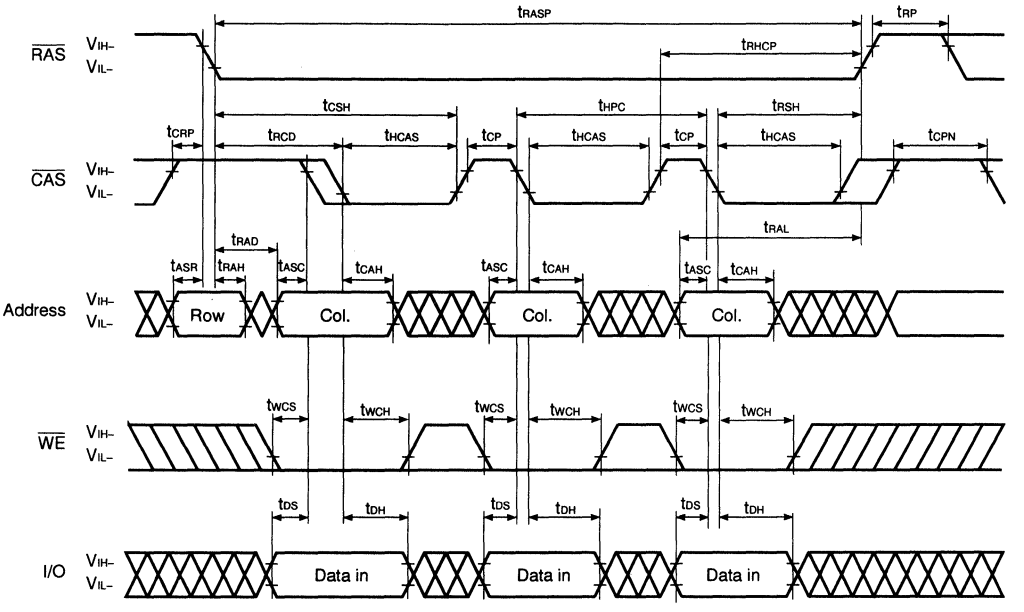
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

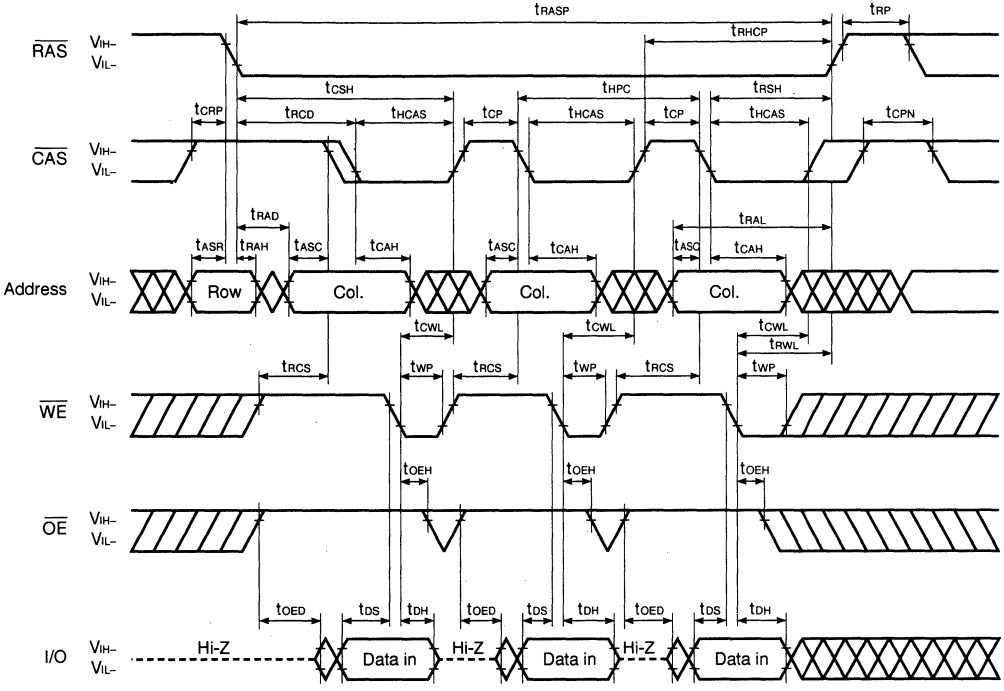
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

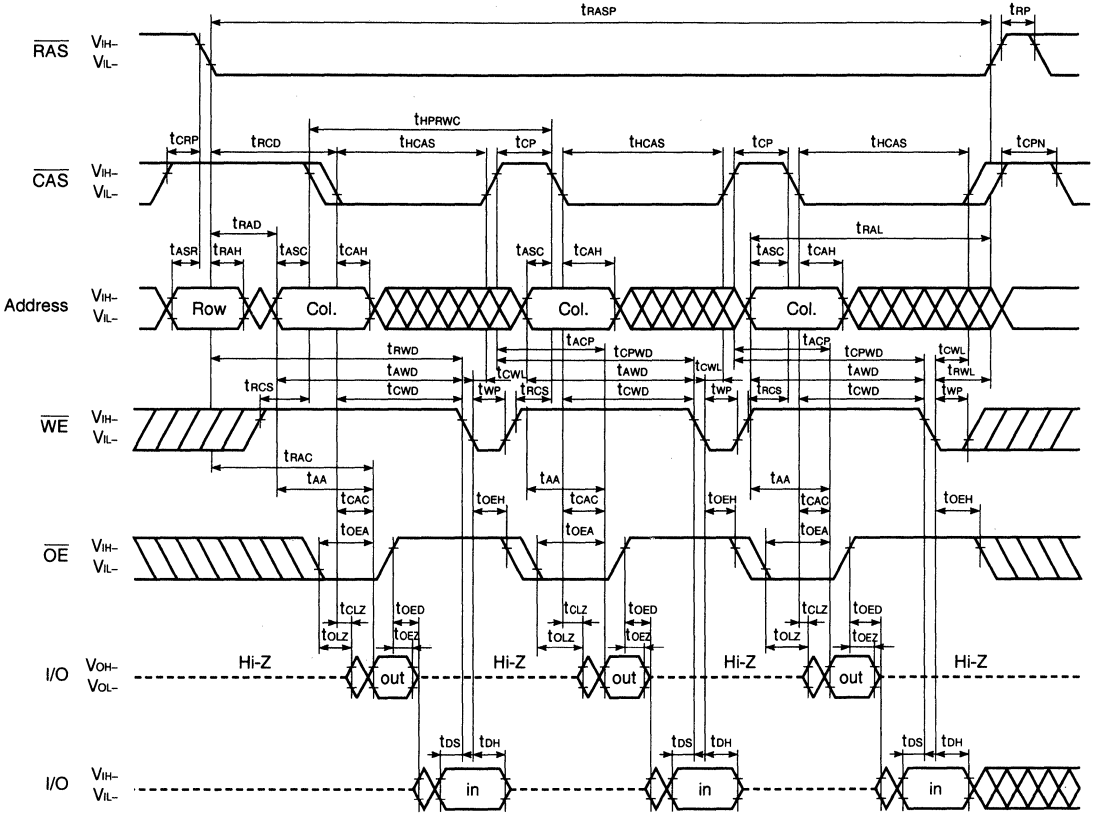
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



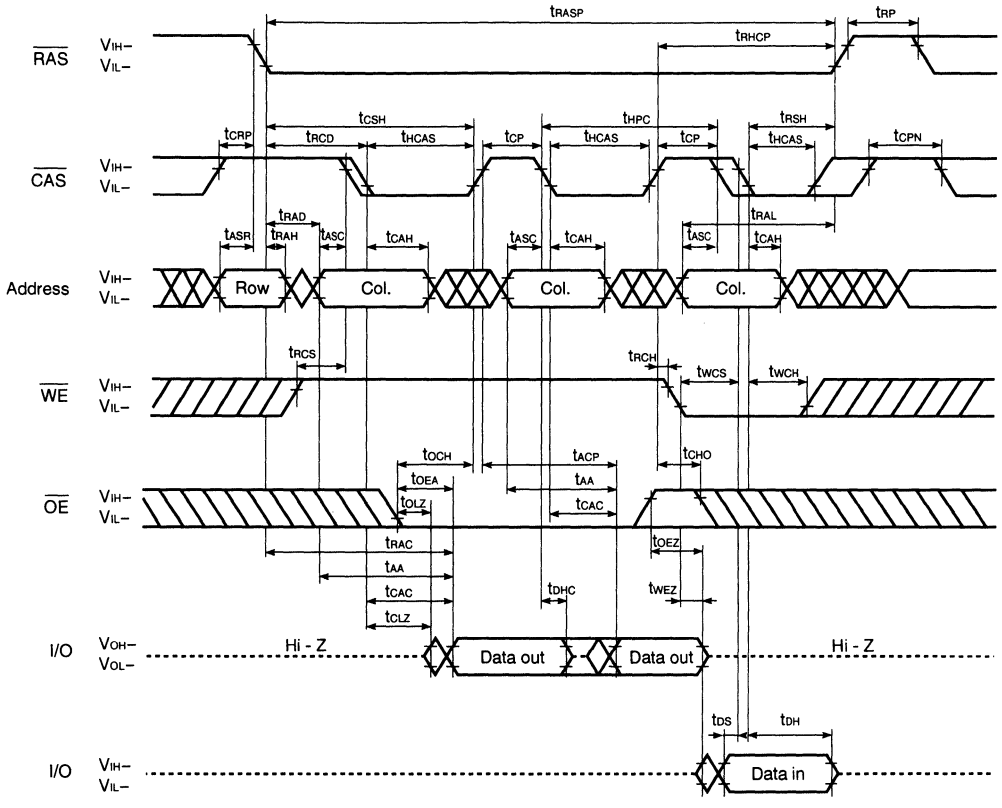
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



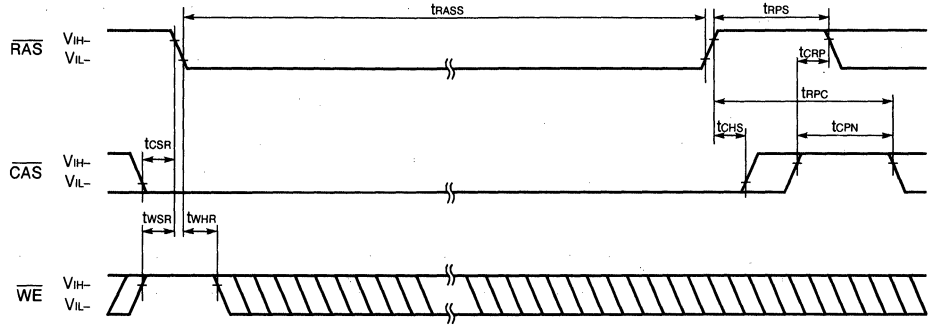
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17405L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

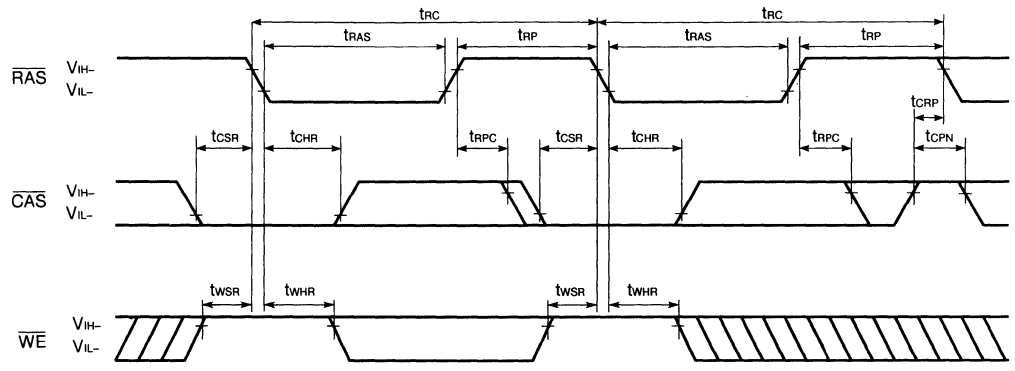
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (2,048/128 ms) should be met.

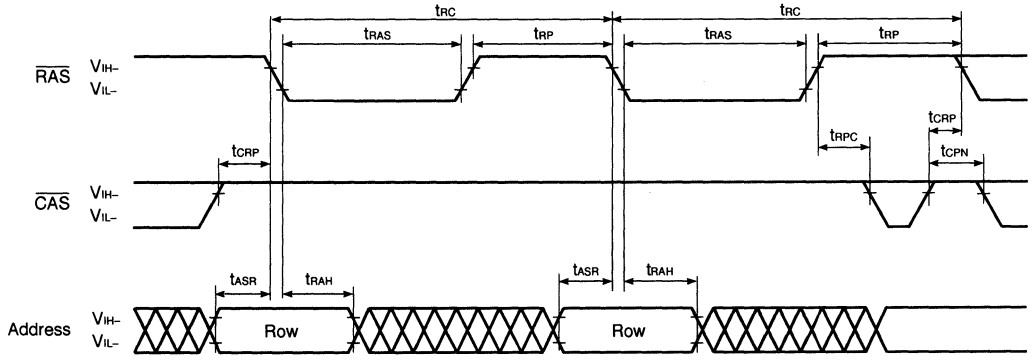
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



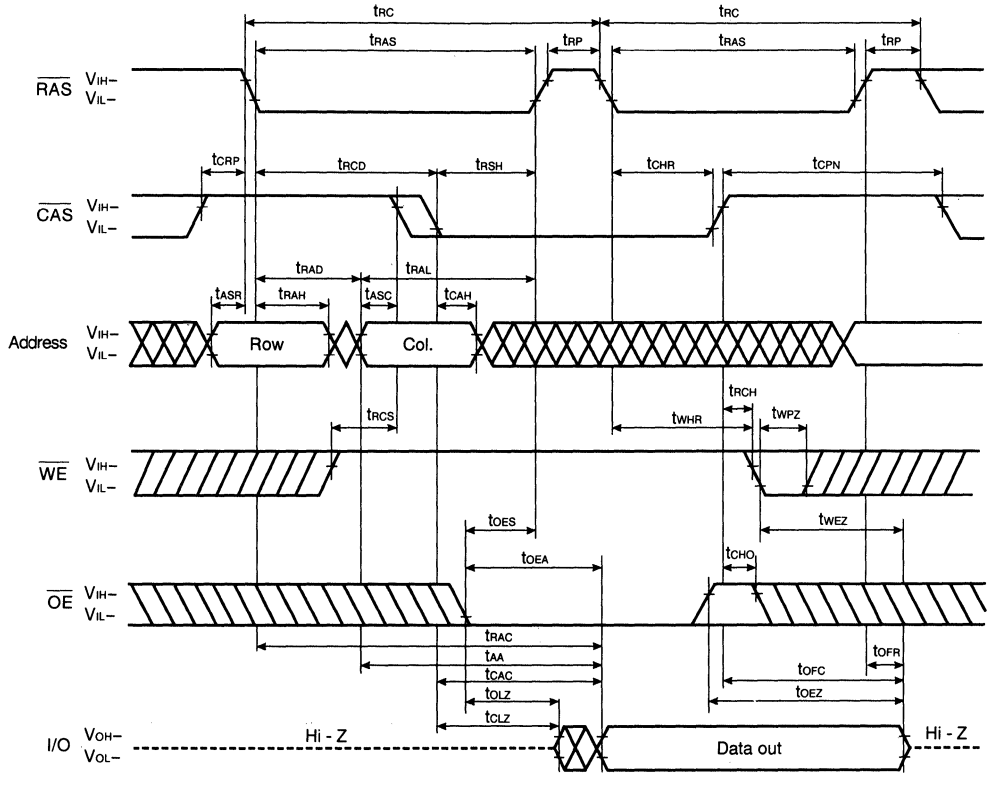
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

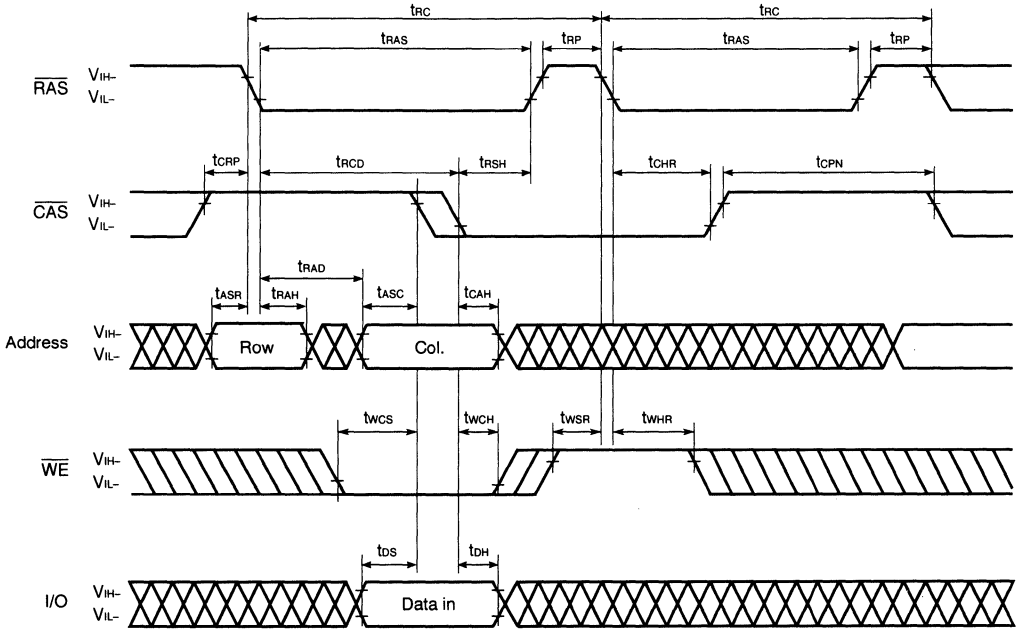


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

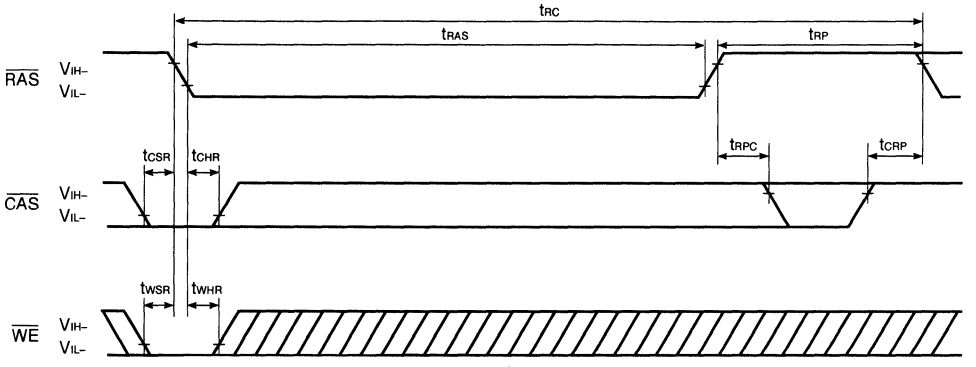


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

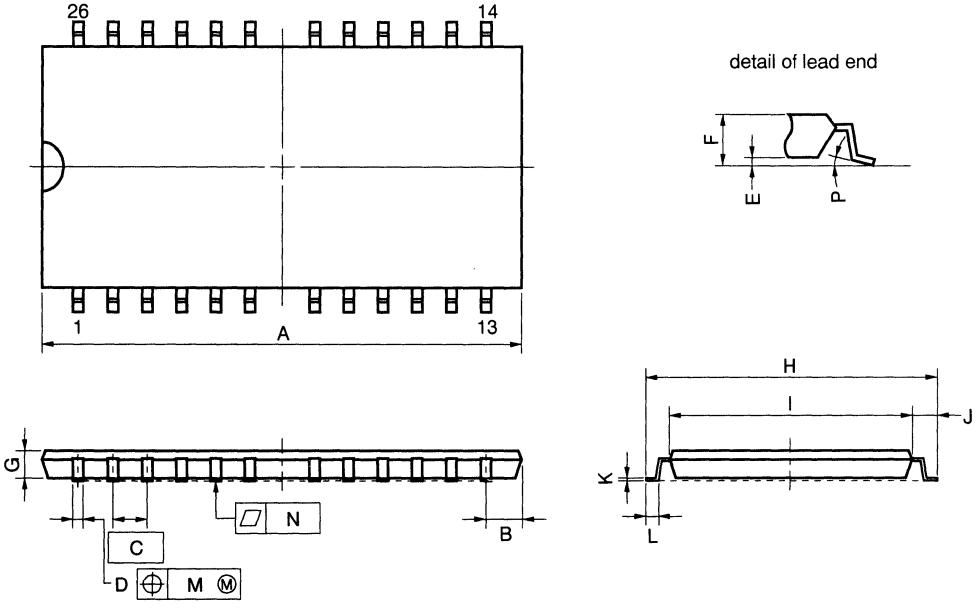
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



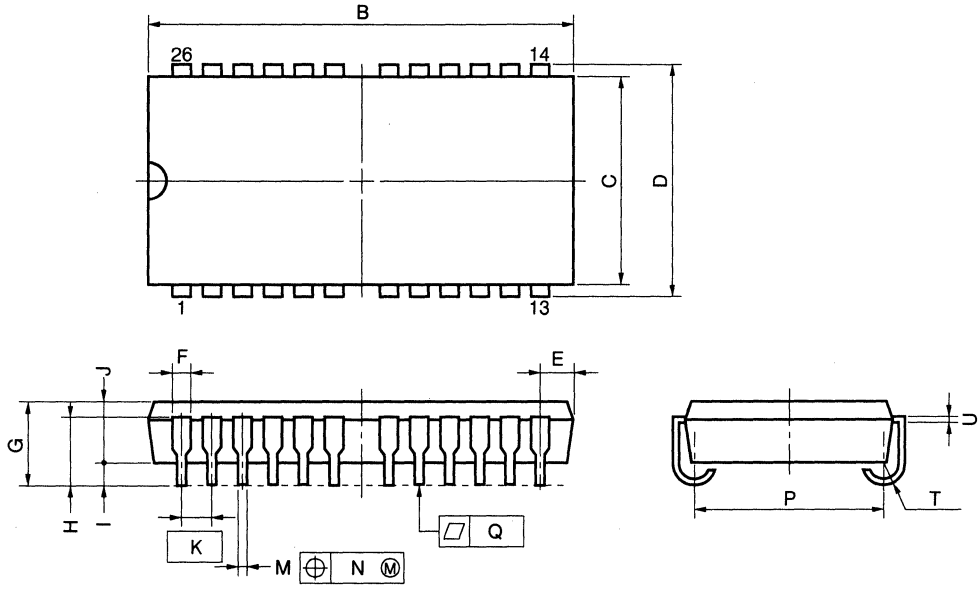
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	3^{+7}_{-3}	3^{+7}_{-3}

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17405L, 4217405L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17405LG3, 4217405LG3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S17405LLA, 4217405LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S17805L, 4217805L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 2 M-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μPD42S17805L, 4217805L are 2,097,152 words by 8 bits CMOS dynamic RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S17805L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S17805L, 4217805L are packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 8 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD42S17805L-A60, 4217805L-A60	360 mW	60 ns	104 ns	25 ns
μPD42S17805L-A70, 4217805L-A70	324 mW	70 ns	124 ns	30 ns

- The μPD42S17805L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

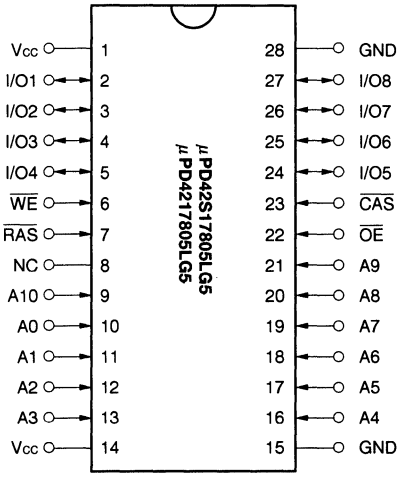
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17805L	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4217805L	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

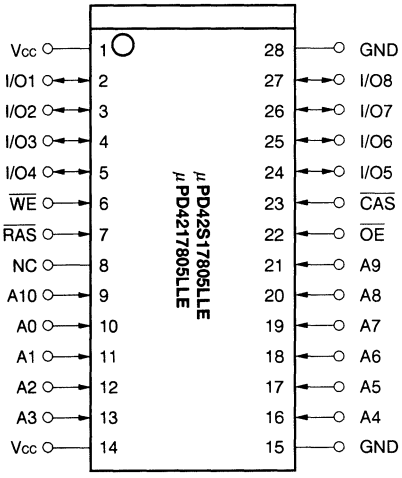
Part number	Access time (MAX.)	Package	Refresh
μPD42S17805LG5-A60	60 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh
μPD42S17805LG5-A70	70 ns		$\overline{CAS}$ before $\overline{RAS}$ refresh
μPD42S17805LLE-A60	60 ns	28-pin Plastic SOJ (400 mil)	$\overline{RAS}$ only refresh
μPD42S17805LLE-A70	70 ns		Hidden refresh
μPD4217805LG5-A60	60 ns	28-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh
μPD4217805LG5-A70	70 ns		$\overline{RAS}$ only refresh
μPD4217805LLE-A60	60 ns	28-pin Plastic SOJ (400 mil)	Hidden refresh
μPD4217805LLE-A70	70 ns		

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

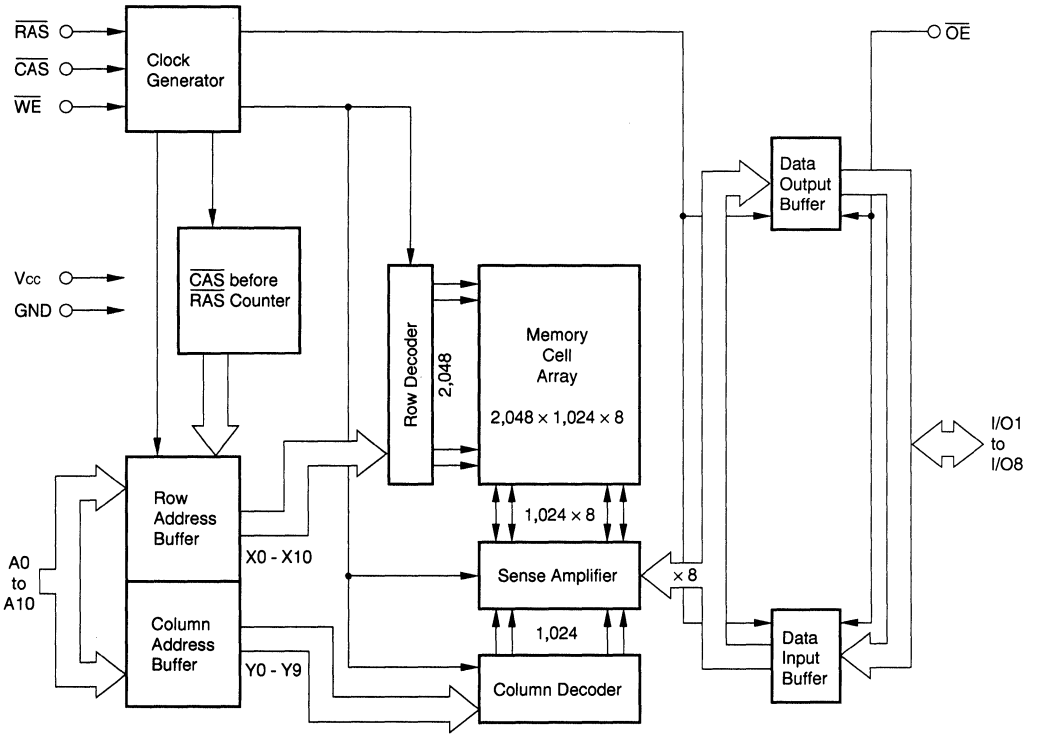


28-pin Plastic SOJ (400 mil)



A0 to A10 : Address Inputs
I/O1 to I/O8 : Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S17805L, 4217805L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A10 and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 21-bit of address signal, upper 11-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 2,097,152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

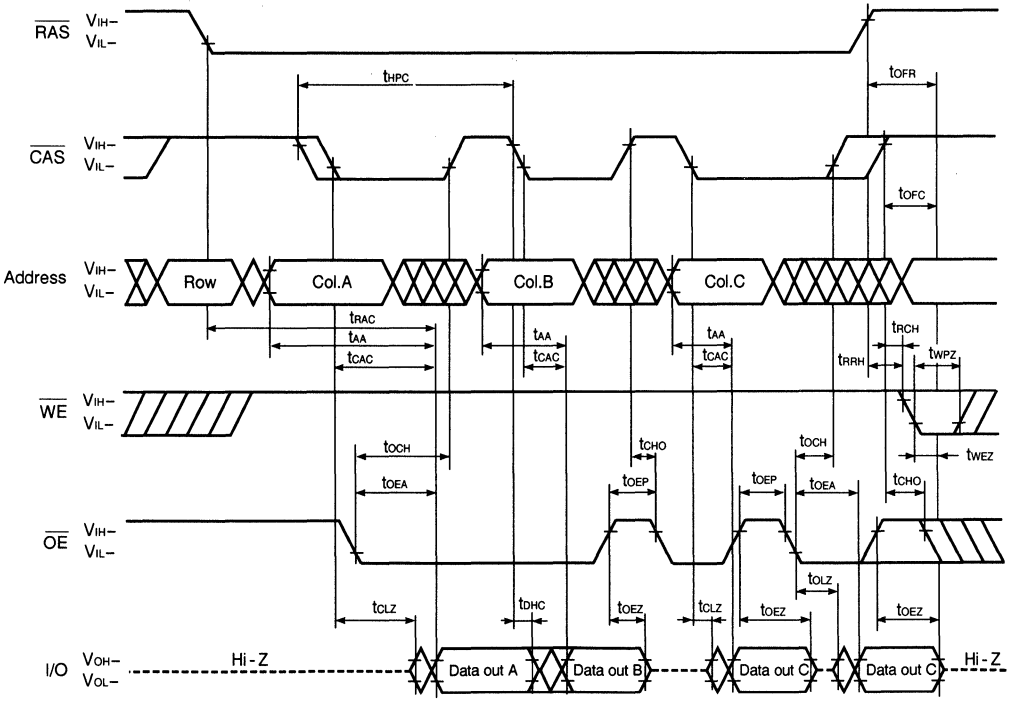
In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2, 3
				t_{RAC} = 70 ns		90		
Standby current	μPD42S17805L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4217805L		$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2, 3, 4
				t_{RAC} = 70 ns		90		
Operating current (Hyper page mode)		I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		100	mA	1, 2
				t_{RAC} = 70 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17805L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		200	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17805L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$ and $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$.

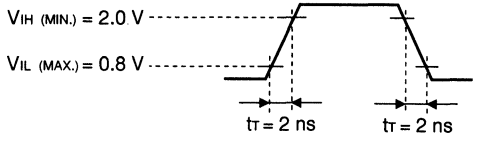
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

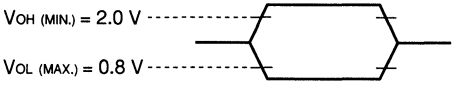
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

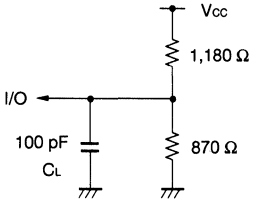
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time		tRP	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ Pulse Width		tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ Hold Time		tRSH	10	–	12	–	ns	
$\overline{CAS}$ Hold Time		tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		tRCD	14	45	14	52	ns	2
$\overline{RAS}$ to Column Address Delay Time		tRAD	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	–	5	–	ns	3
Row Address Setup Time		tASR	0	–	0	–	ns	
Row Address Hold Time		tRAH	10	–	10	–	ns	
Column Address Setup Time		tASC	0	–	0	–	ns	
Column Address Hold Time		tCAH	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time		tOED	13	–	15	–	ns	
Transition Time (Rise and Fall)		tT	1	50	1	50	ns	
Refresh Time	μPD42S17805L	tREF	–	128	–	128	ms	4
	μPD4217805L		–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S17805L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	30	–	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	–	40	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ Precharge Time	t_{OEP}	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	10	–	10	–	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

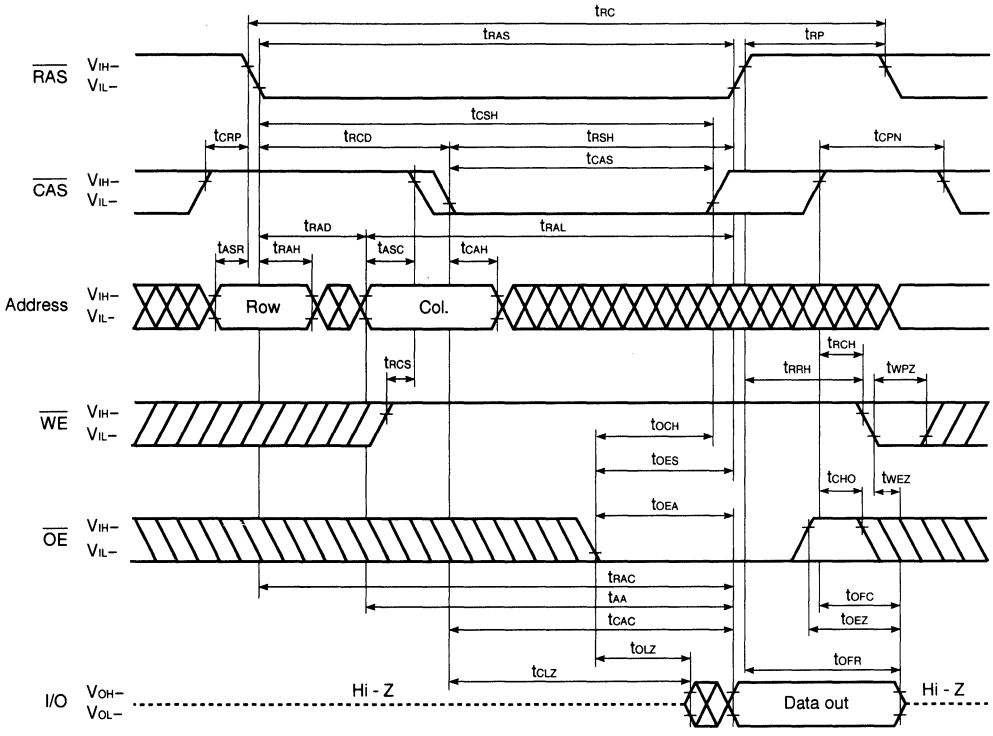
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

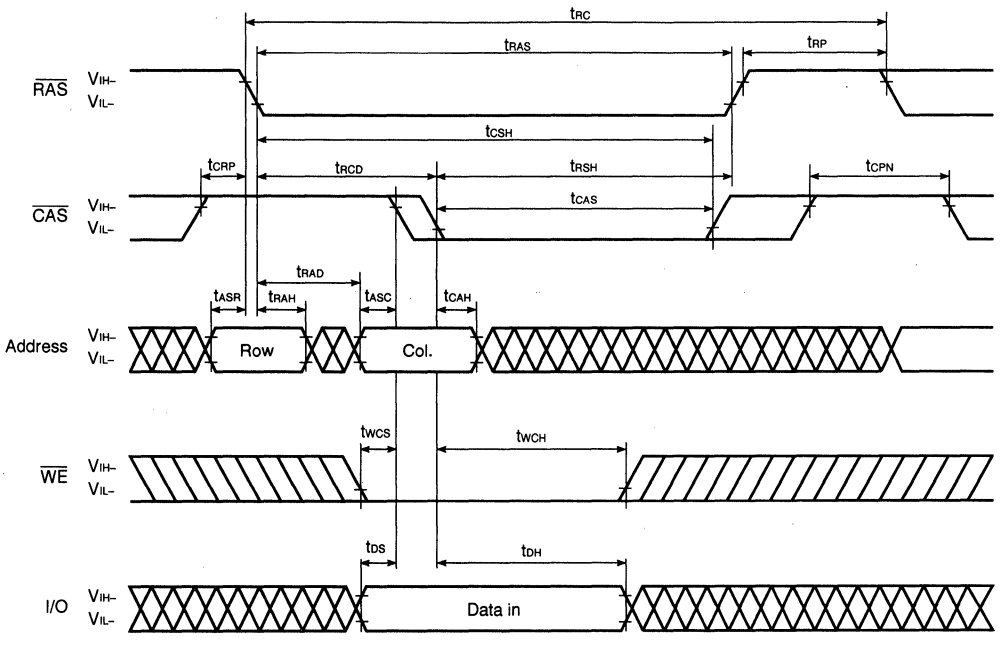
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ Setup Time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ Hold Time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17805L.

Read Cycle

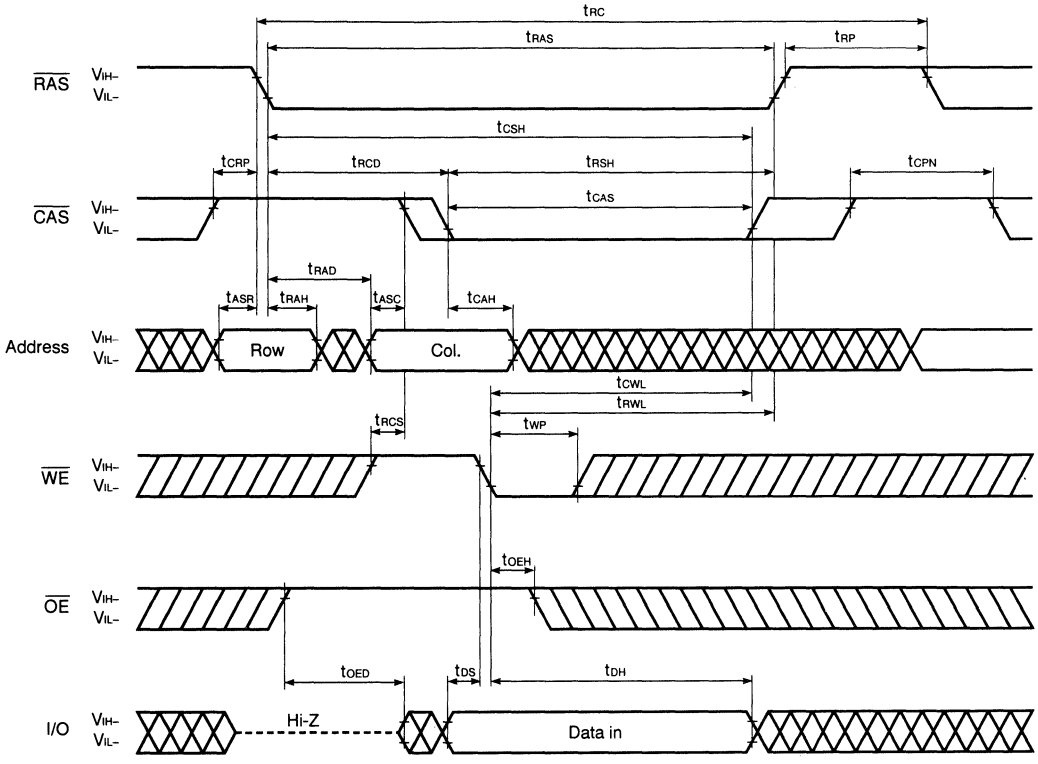

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

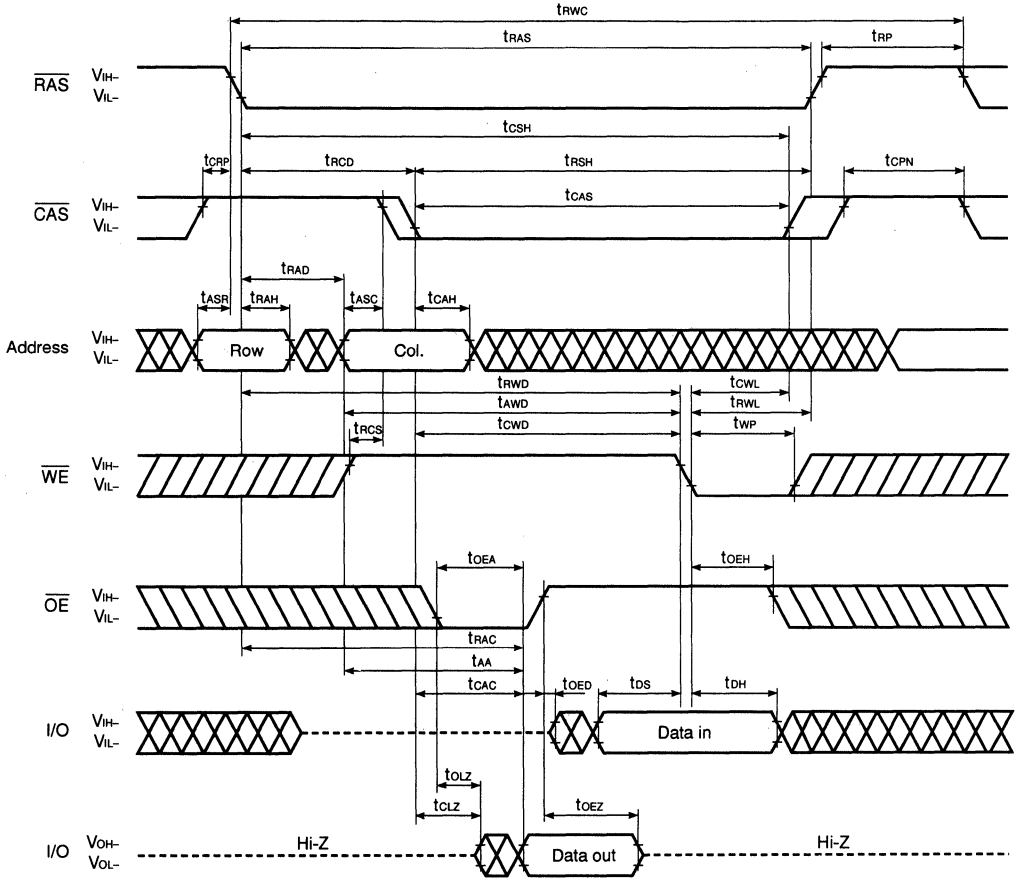


Remark $\overline{OE}$: Don't care

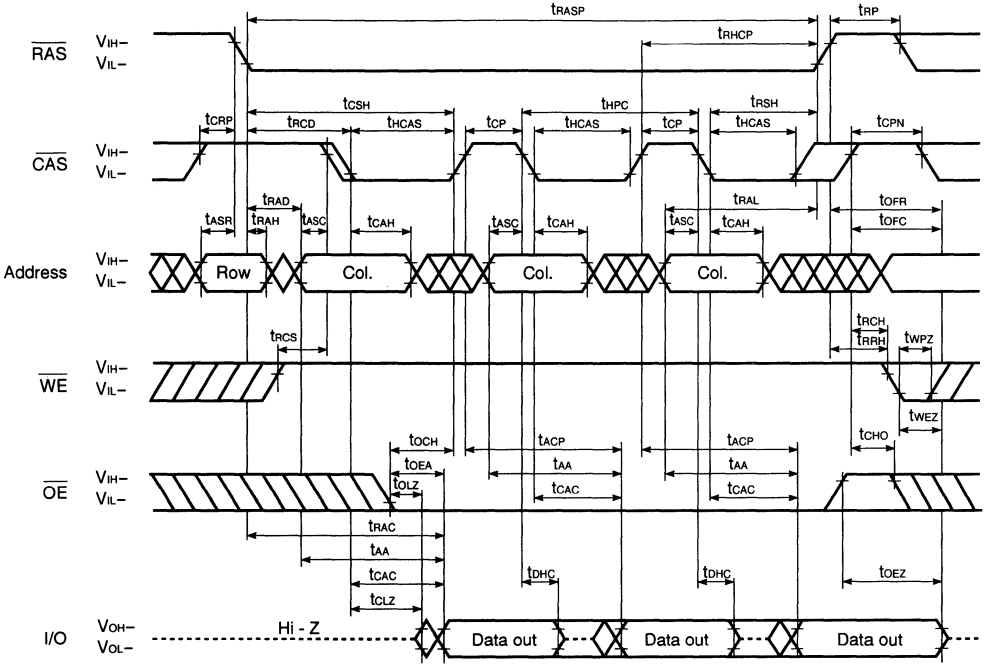
Late Write Cycle



Read Modify Write Cycle

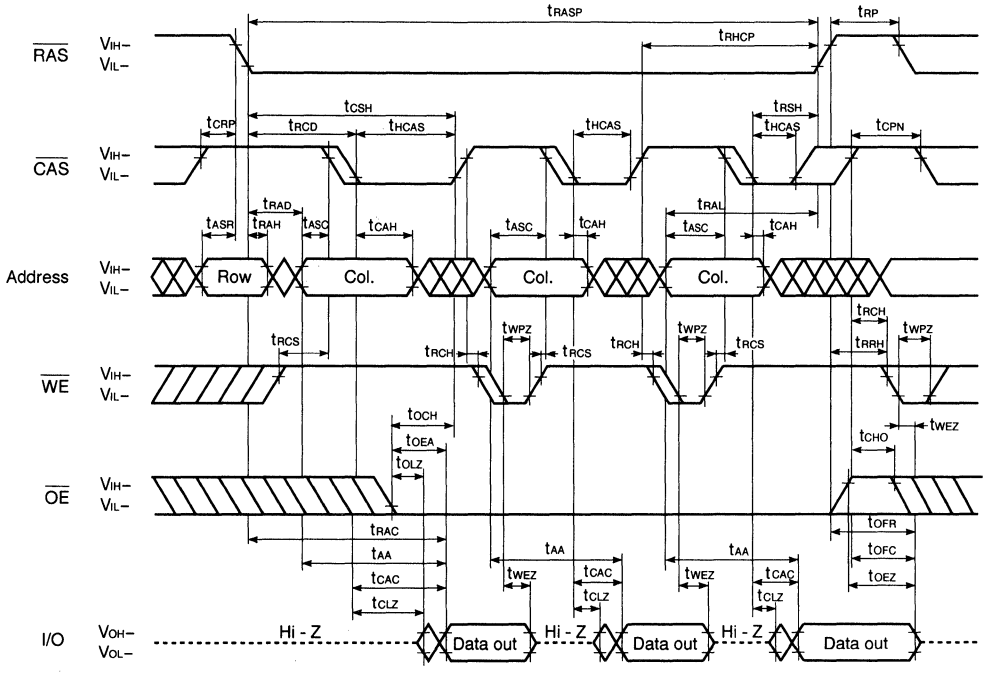


Hyper Page Mode Read Cycle



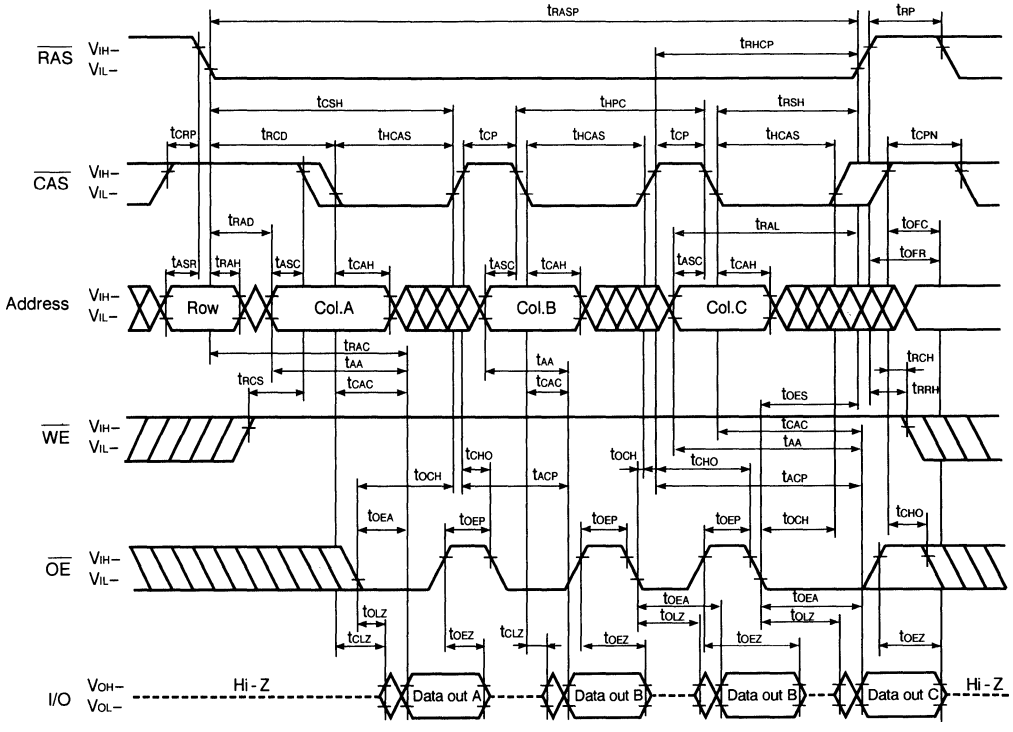
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



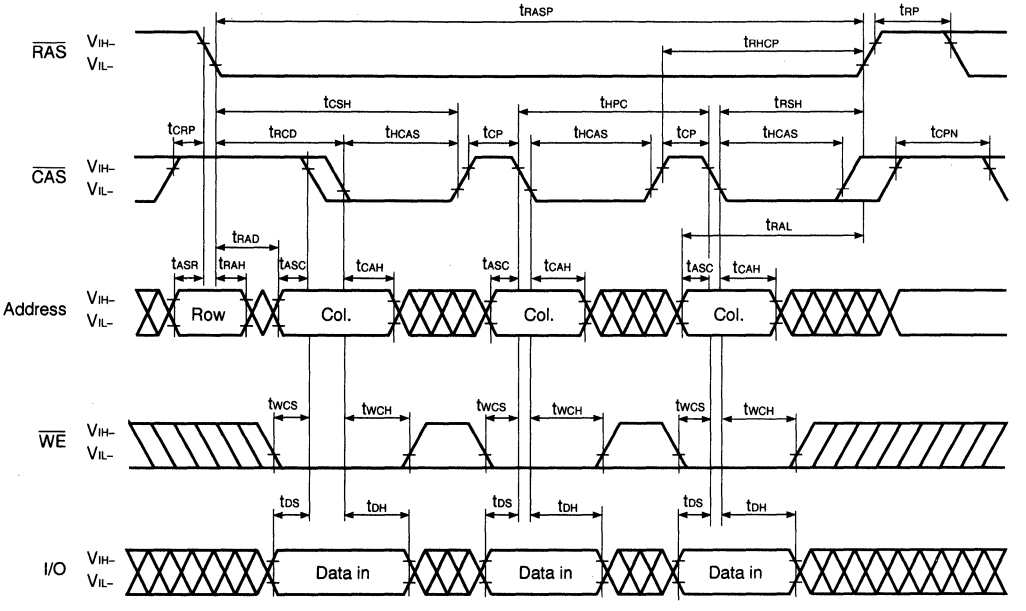
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

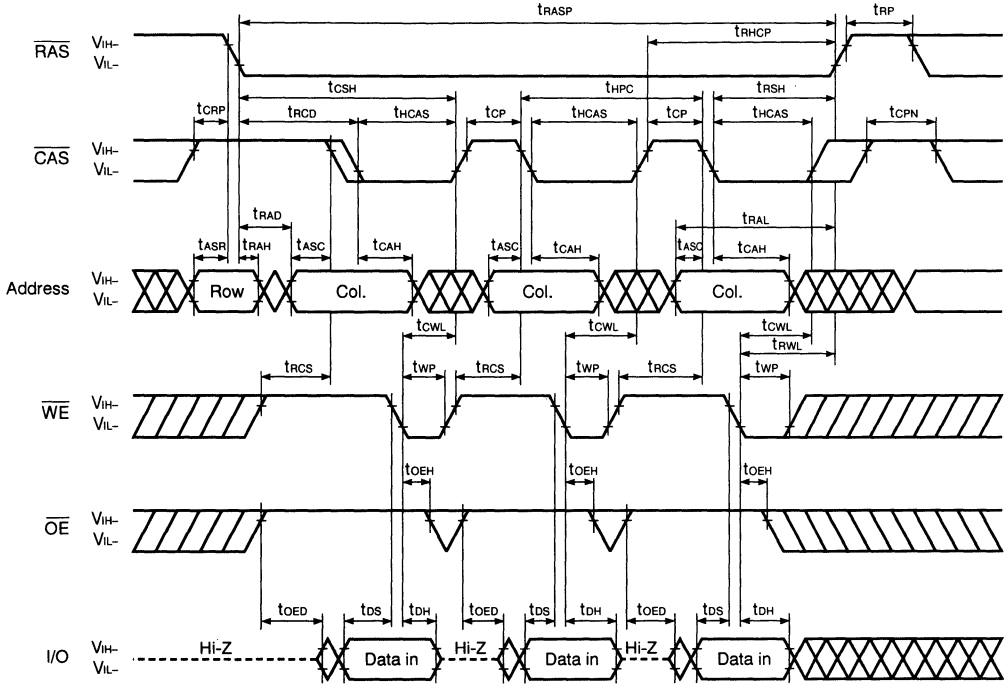
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

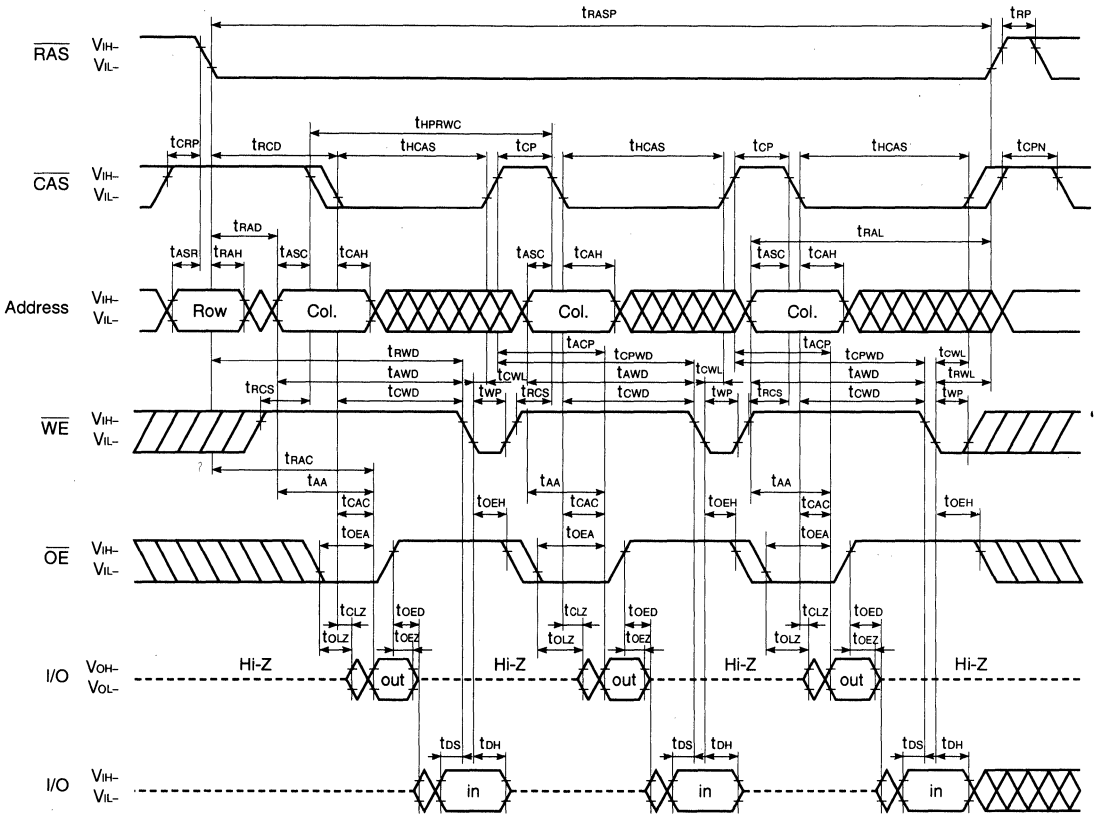
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



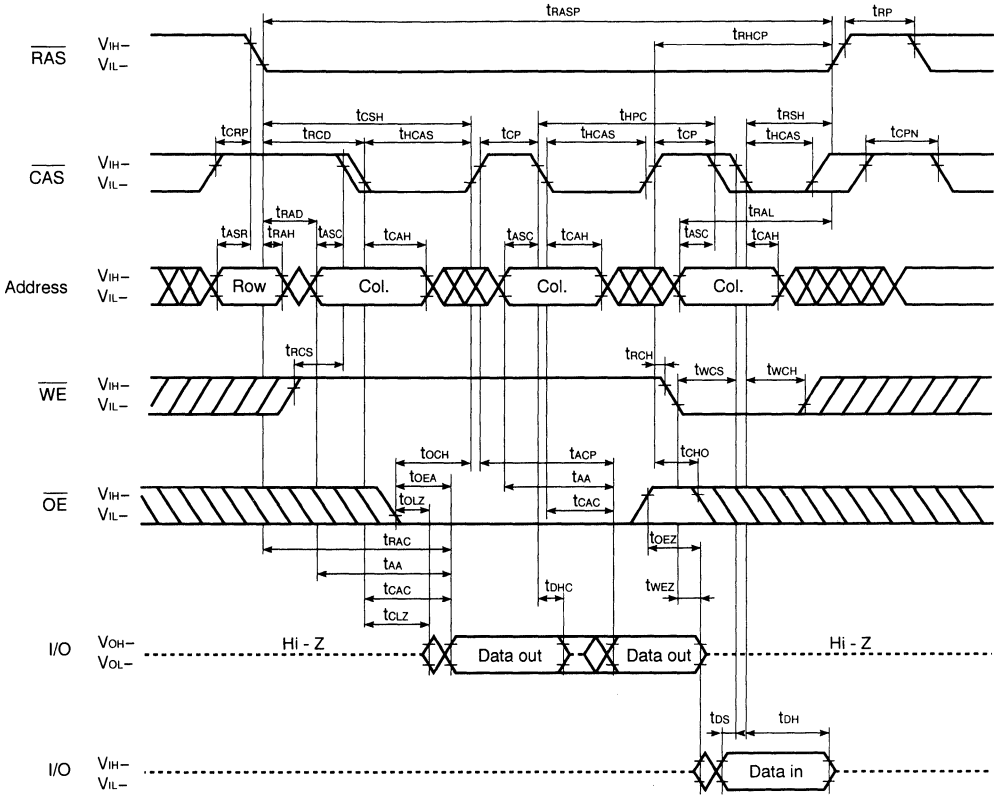
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



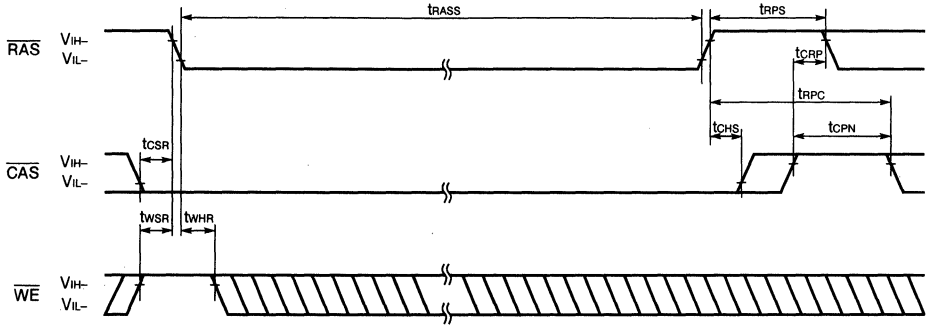
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17805L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

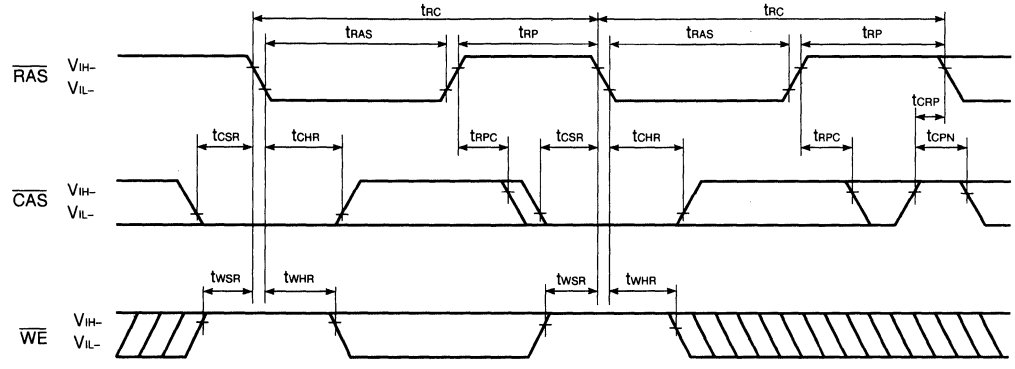
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (2,048/128 ms) should be met.

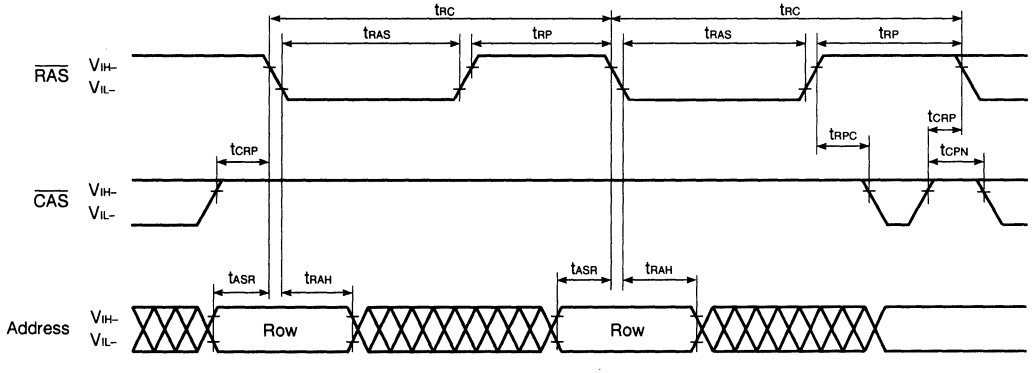
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



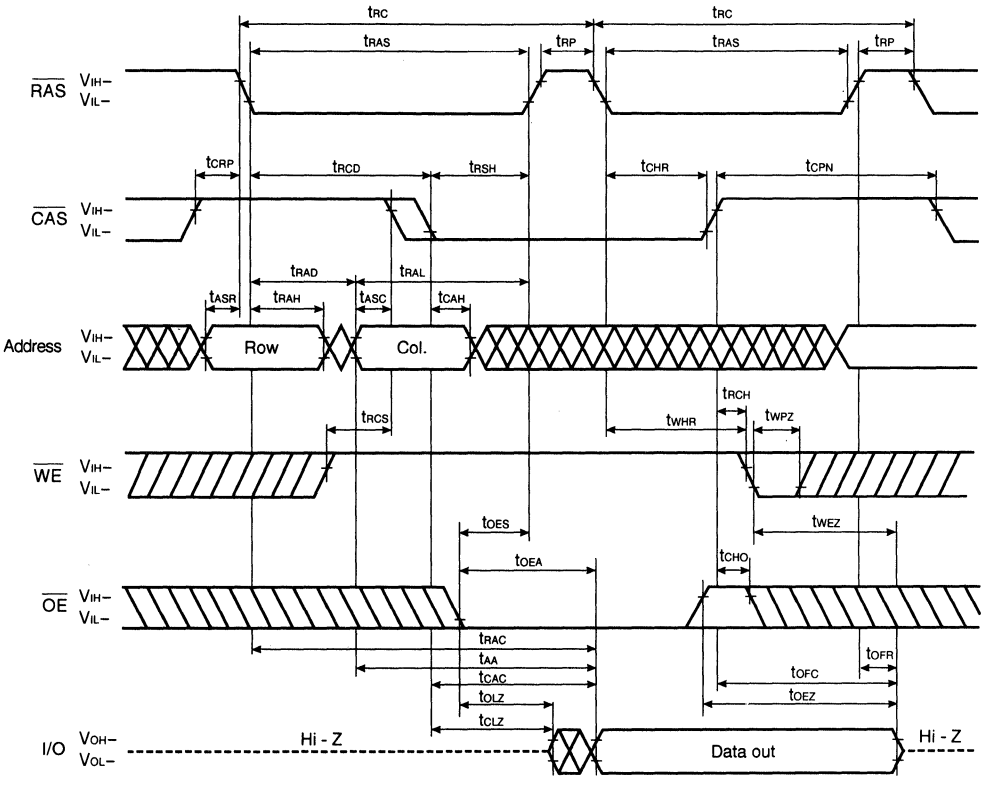
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

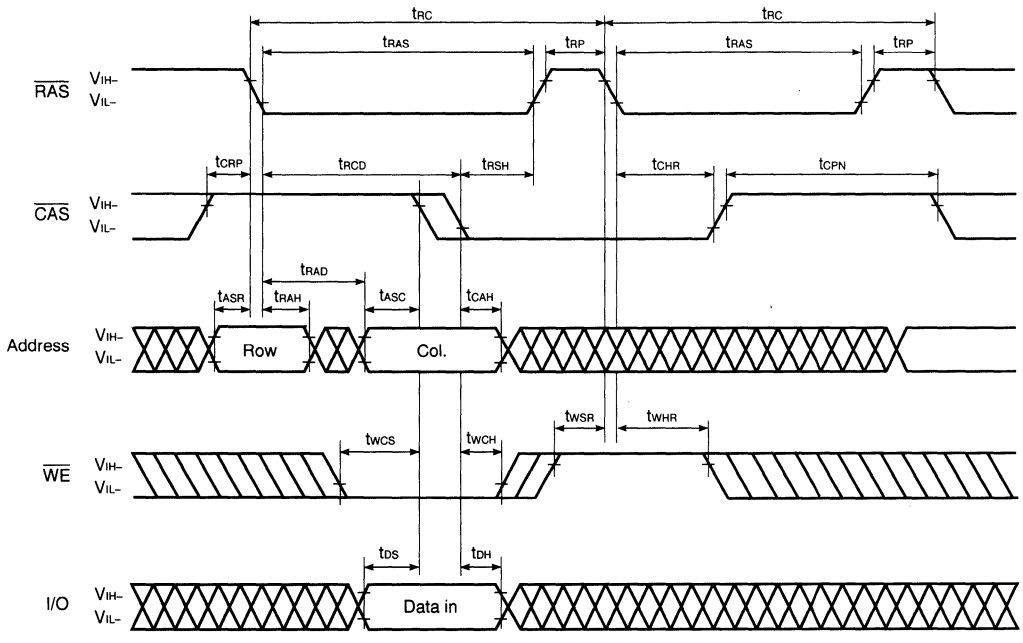


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

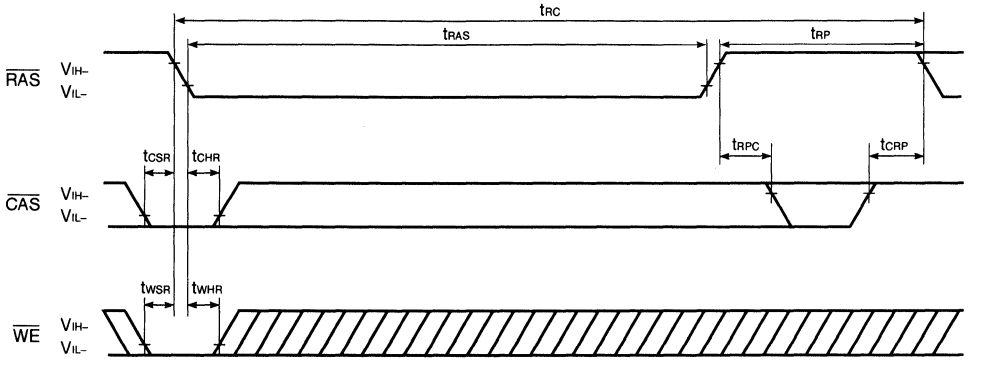


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

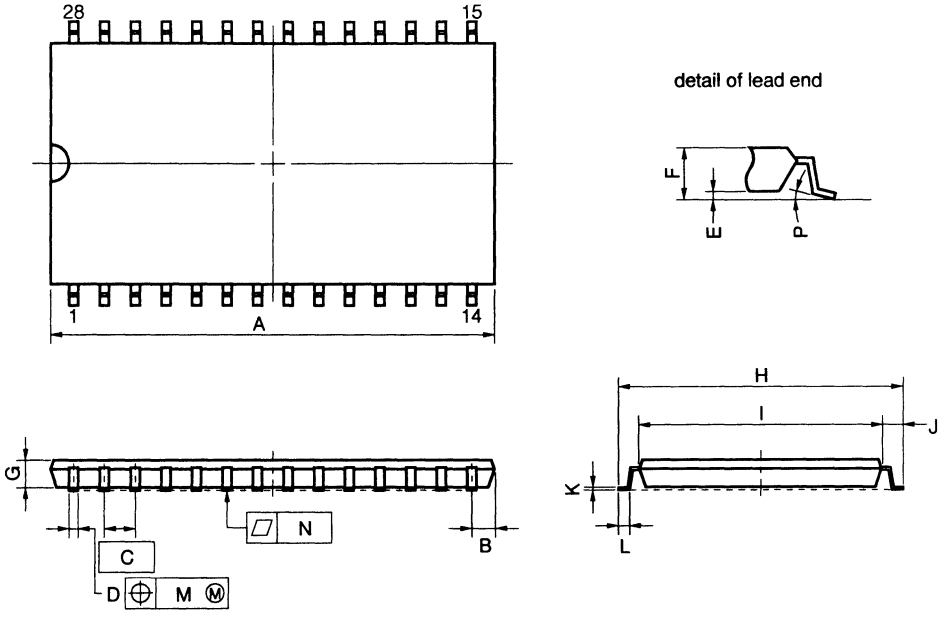
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

28PIN PLASTIC TSOP(II) (400 mil)



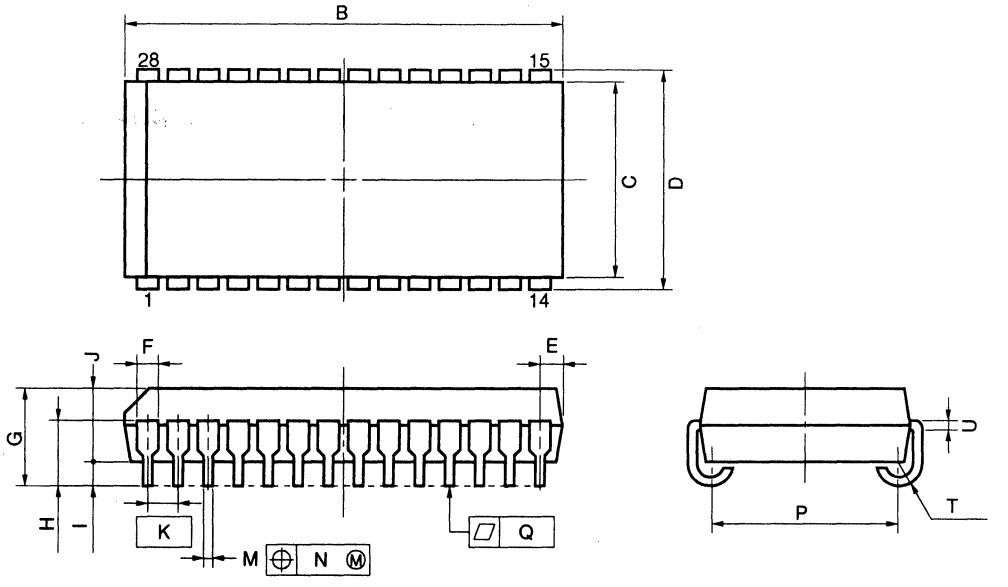
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S17805L, 4217805L.

Types of Surface Mount Device

μPD42S17805LG5, 4217805LG5 : 28-pin plastic TSOP (II) (400 mil)
μPD42S17805LLE, 4217805LLE : 28-pin plastic SOJ (400 mil)

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD42S16165L, 4216165L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 1 M-WORD BY 16-BIT, HYPER PAGE MODE(EDO), BYTE READ/WRITE MODE

Description

The μPD42S16165L, 4216165L are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S16165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S16165L, 4216165L are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 16 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S16165L-A60, 4216165L-A60	396 mW	60 ns	104 ns	25 ns
μPD42S16165L-A70, 4216165L-A70	360 mW	70 ns	124 ns	30 ns

- The μPD42S16165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

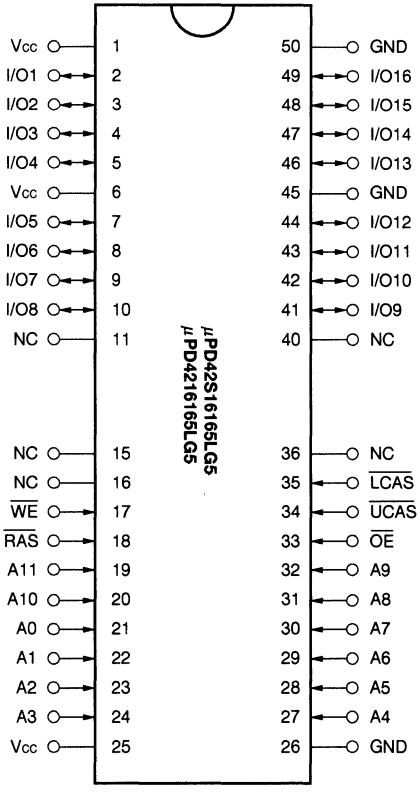
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16165L	4,096 cycles / 128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4216165L	4,096 cycles / 64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

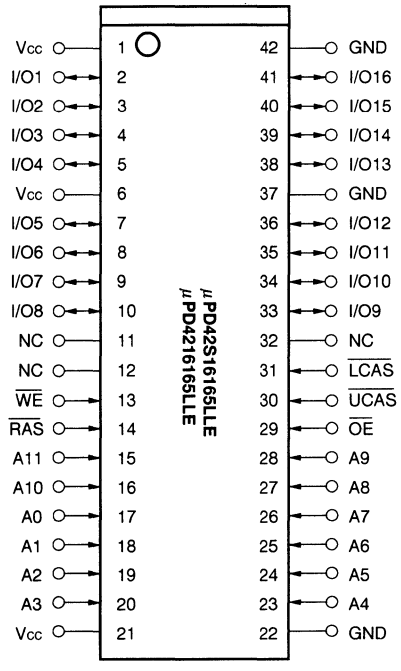
Part number	Access time (MAX.)	Package	Refresh
μPD42S16165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S16165LG5-A70	70 ns		
μPD42S16165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD42S16165LLE-A70	70 ns		
μPD4216165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4216165LG5-A70	70 ns		
μPD4216165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD4216165LLE-A70	70 ns		

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

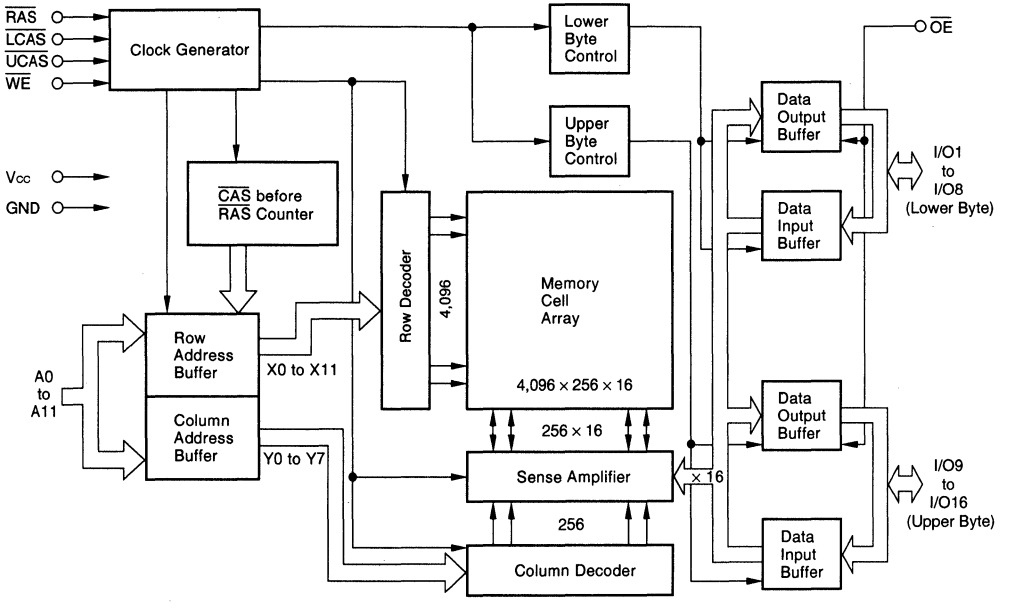


42-pin Plastic SOJ (400 mil)



A0 to A11	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S16165L, 4216165L have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A11 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 12-bit and lower 8-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

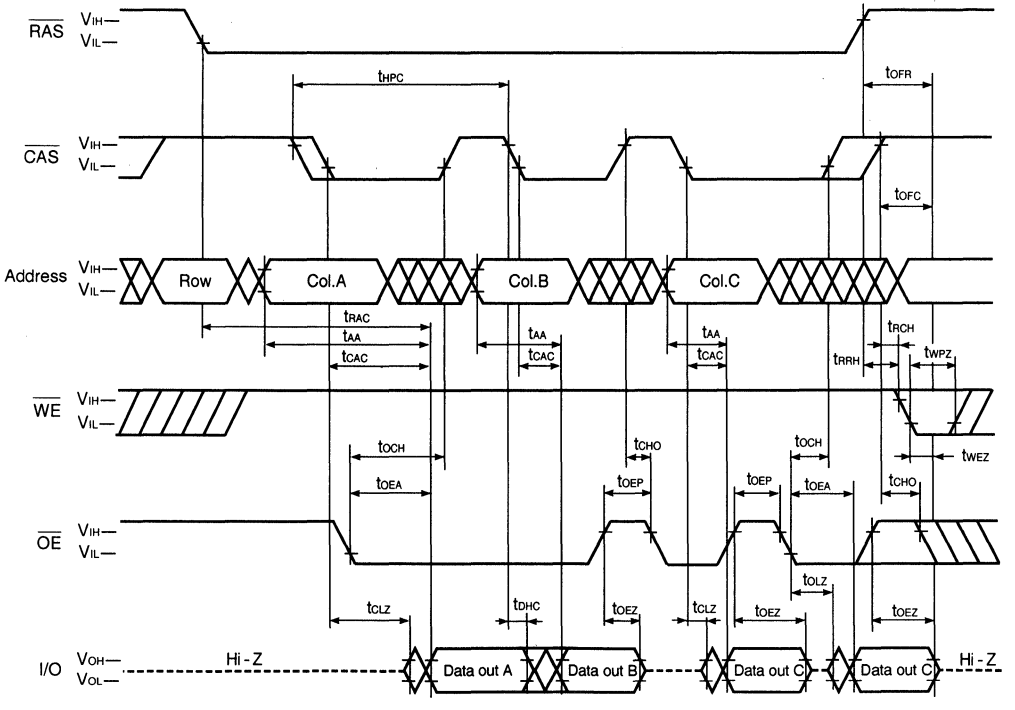
The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. **Data output time is extended.**
   In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**
   In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		90	mA	1, 2, 3
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		80		
Standby current	μPD42S16165L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.15		
	μPD4216165L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$	t_{RAC} = 60 ns		90	mA	1, 2, 3 ,4
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		80		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		110	mA	1, 2, 5
			$t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		90	mA	1, 2
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16165L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		220	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16165L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

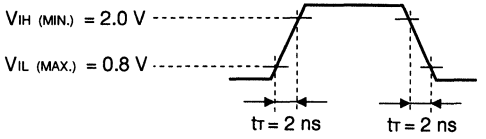
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

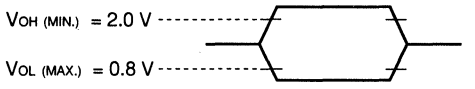
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

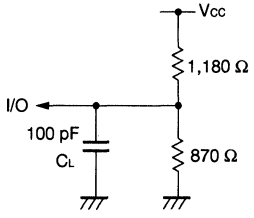
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	104	–	124	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		tRSH	10	–	12	–	ns	
$\overline{CAS}$ hold time		tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		tMRH	0	–	0	–	ns	
Transition time (rise and fall)		tT	1	50	1	50	ns	
Refresh time	μPD42S16165L	tREF	–	128	–	128	ms	4
	μPD4216165L		–	64	–	64	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16165L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	17	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

★

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

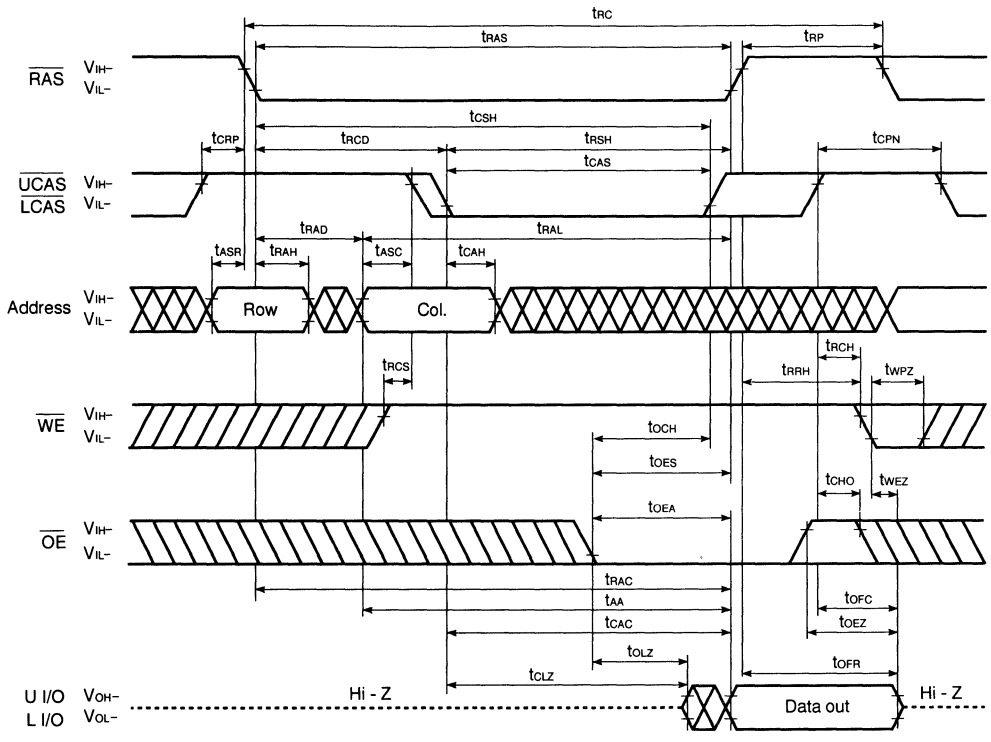
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

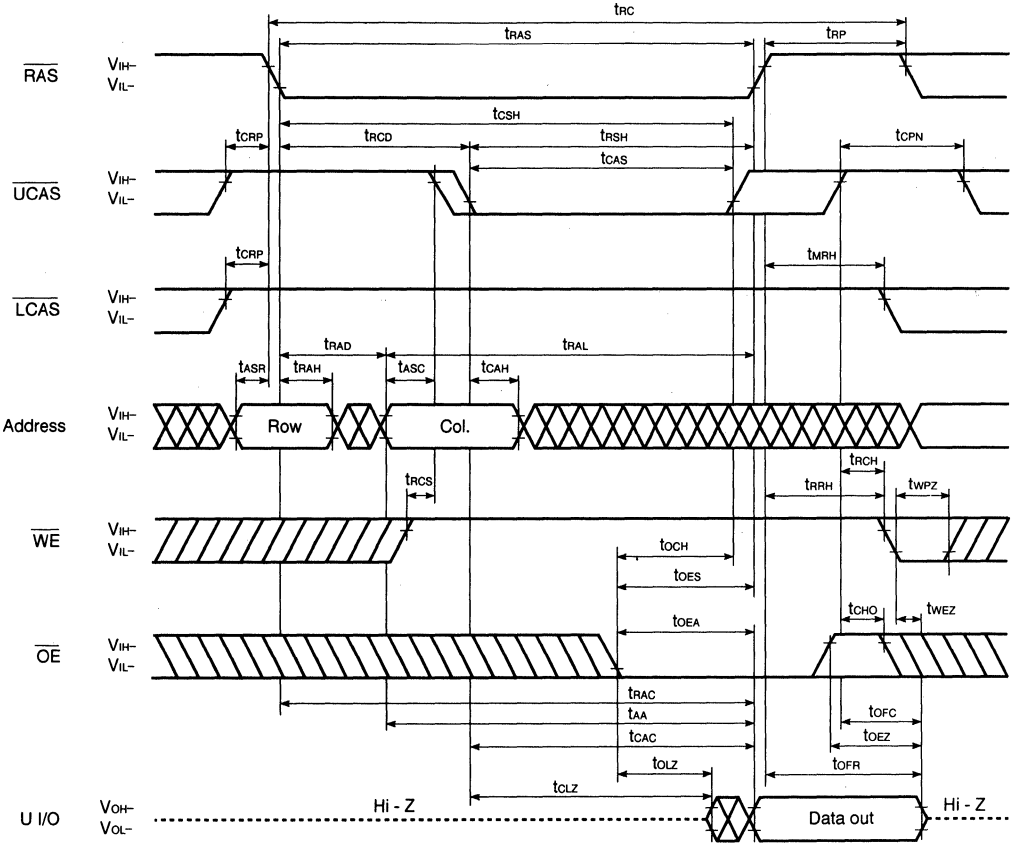
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16165L.

Read Cycle

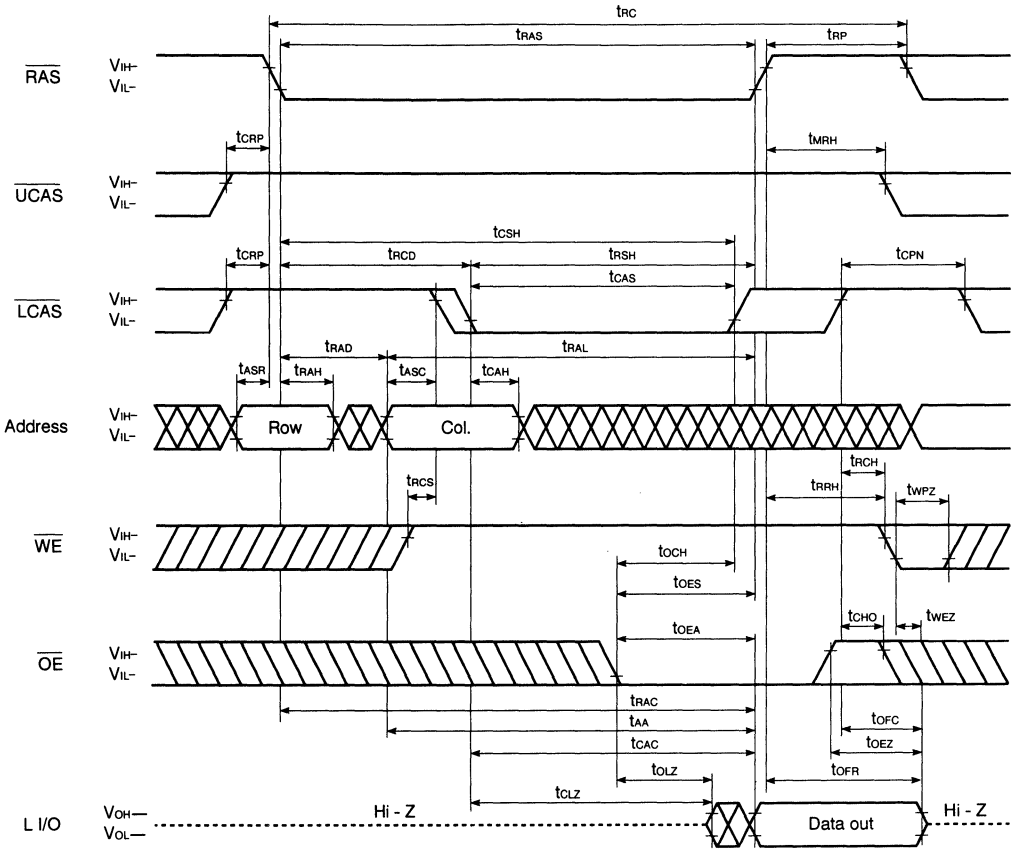

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS VIH–
LCAS VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
tOEA
OE VIH– VIL–
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O VOH–
L I/O VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



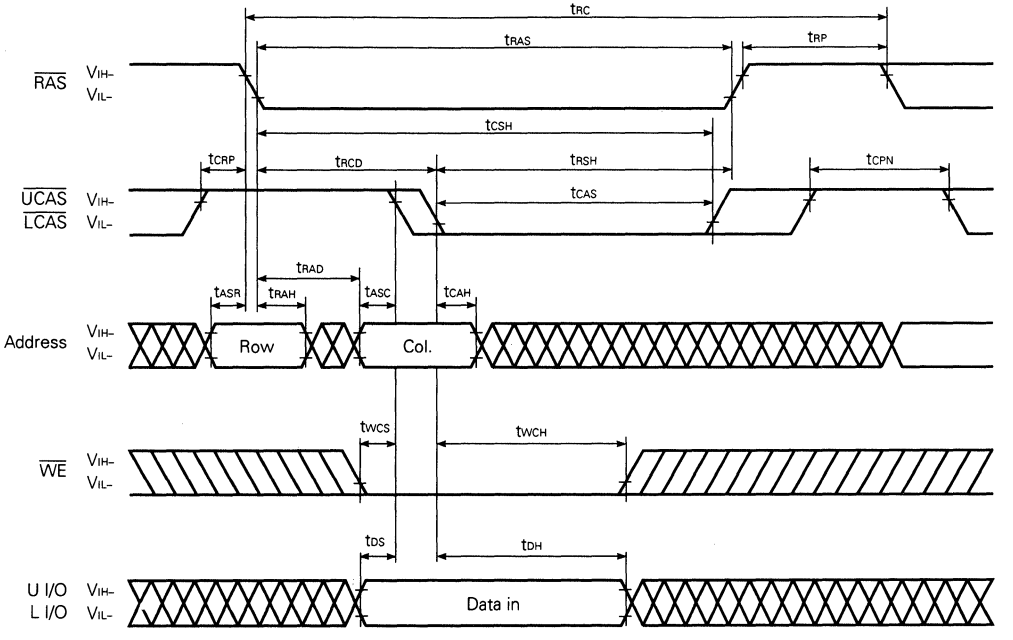
Remark L I/O: Hi-Z

Lower Byte Read Cycle



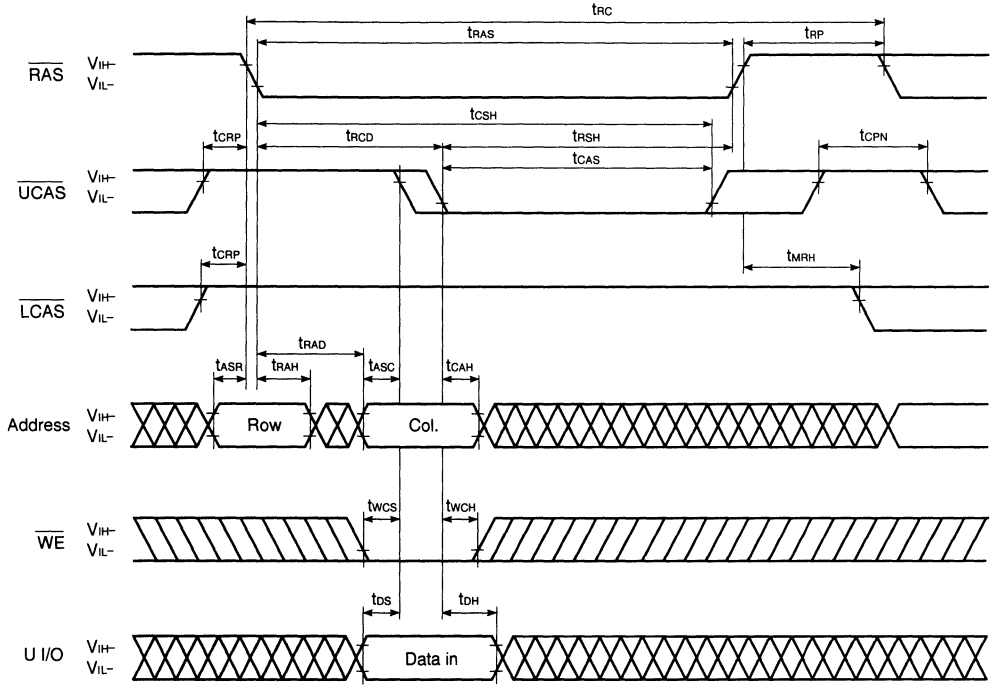
Remark U I/O: Hi-Z

Early Write Cycle



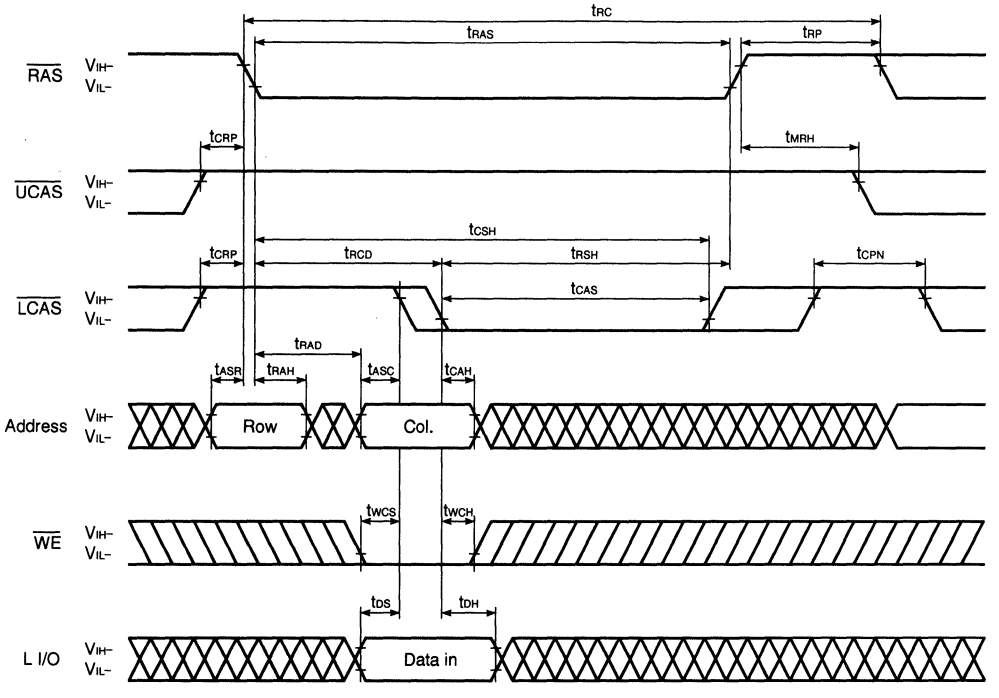
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



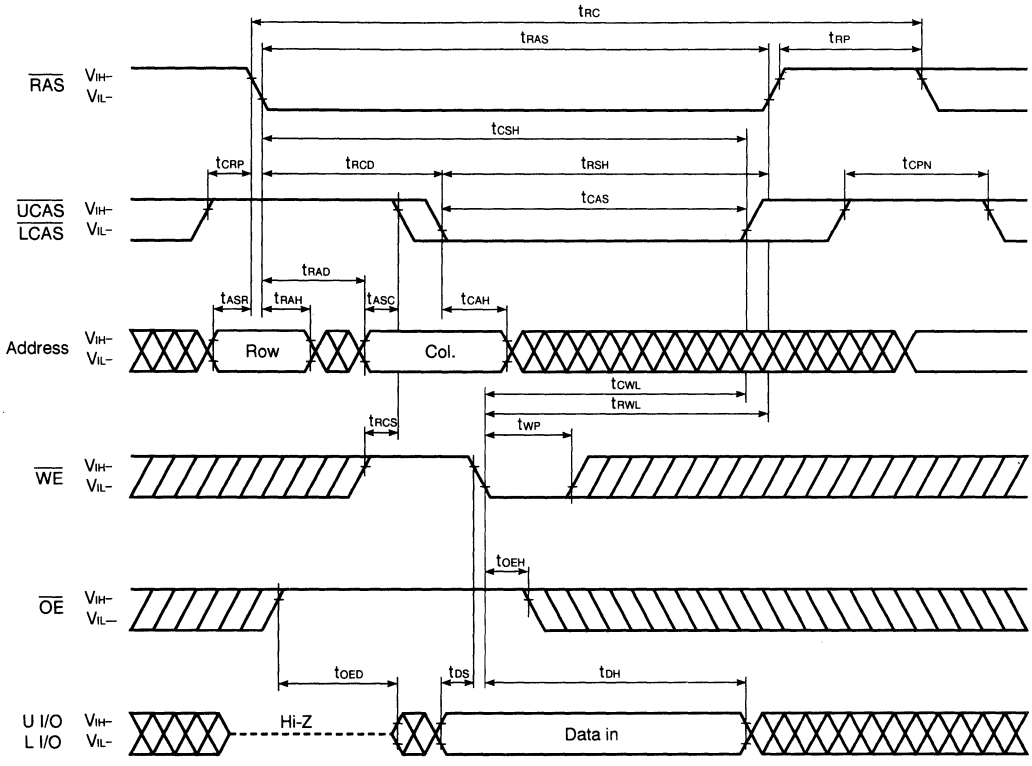
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

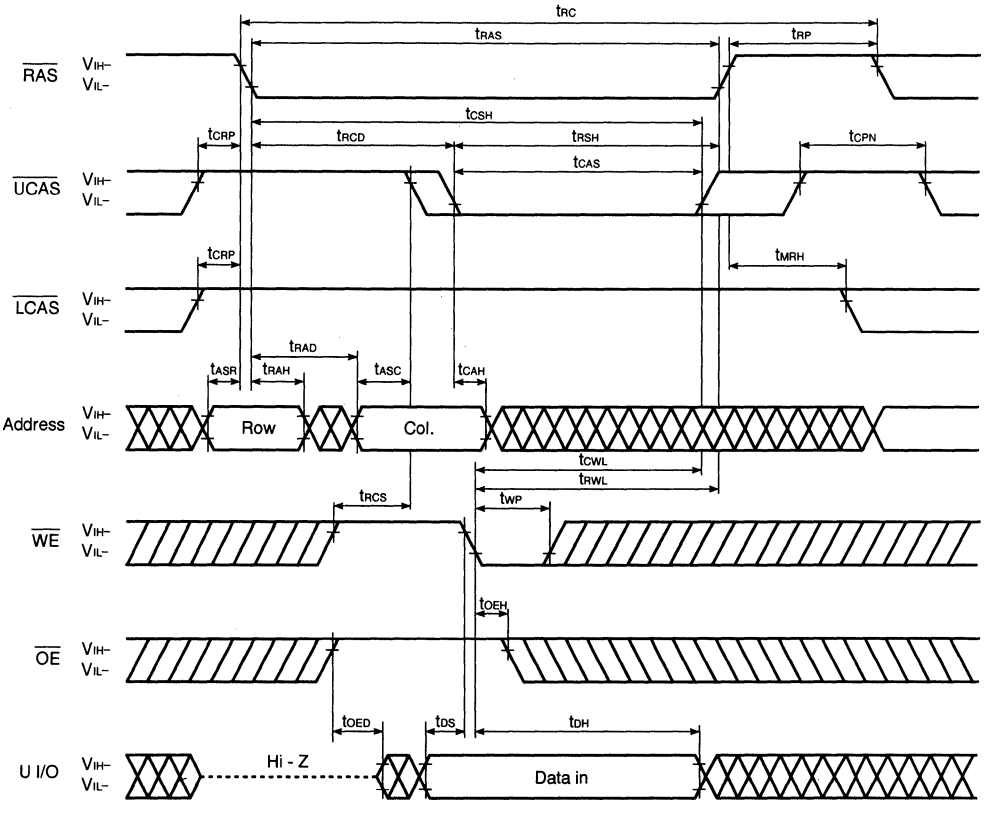


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

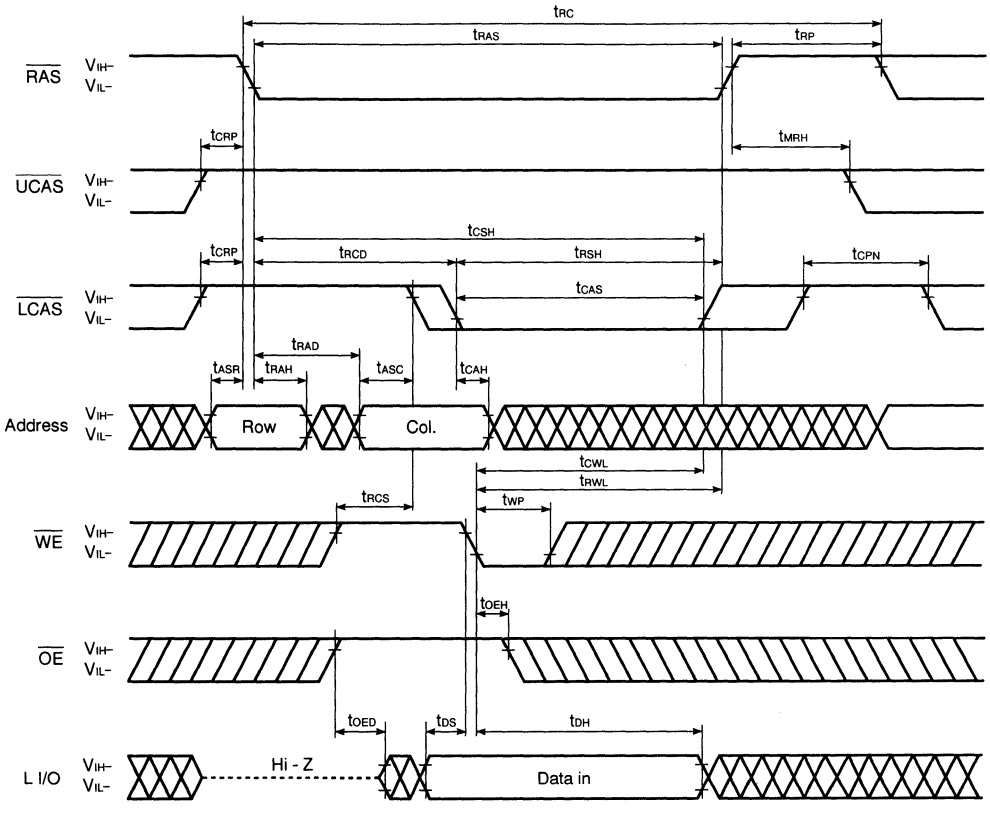


Upper Byte Late Write Cycle



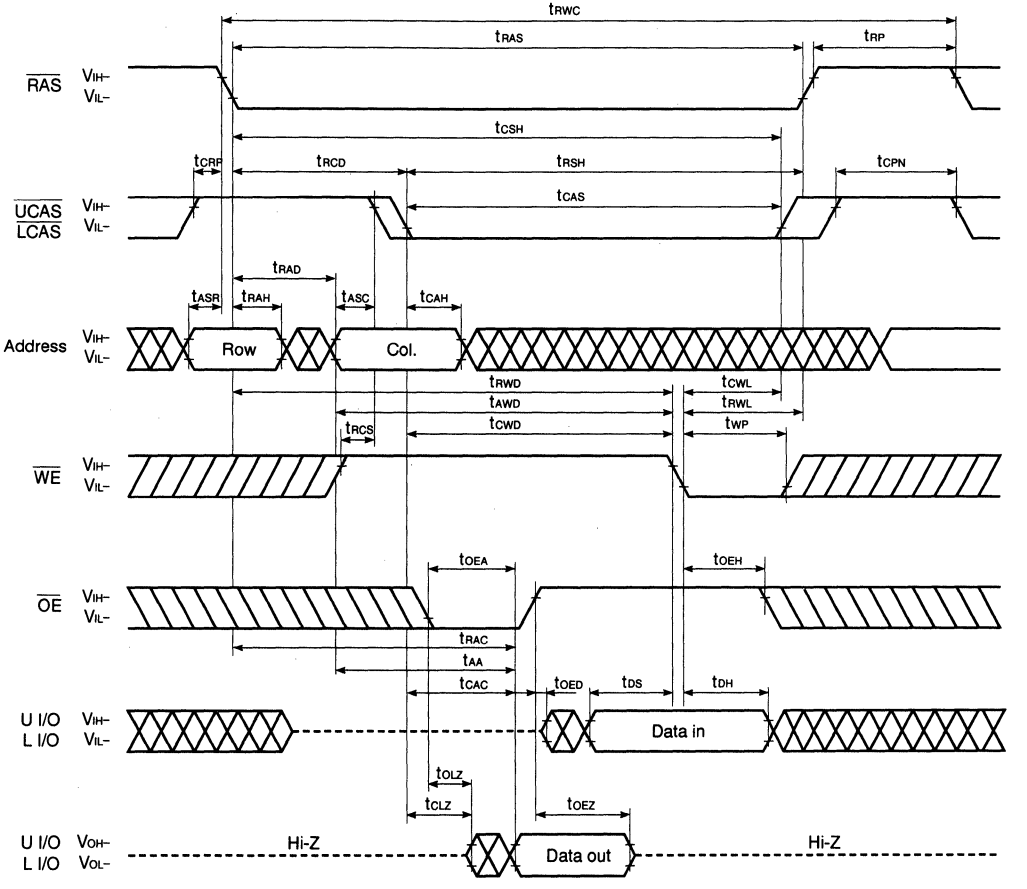
Remark L I/O: Don't care

Lower Byte Late Write Cycle

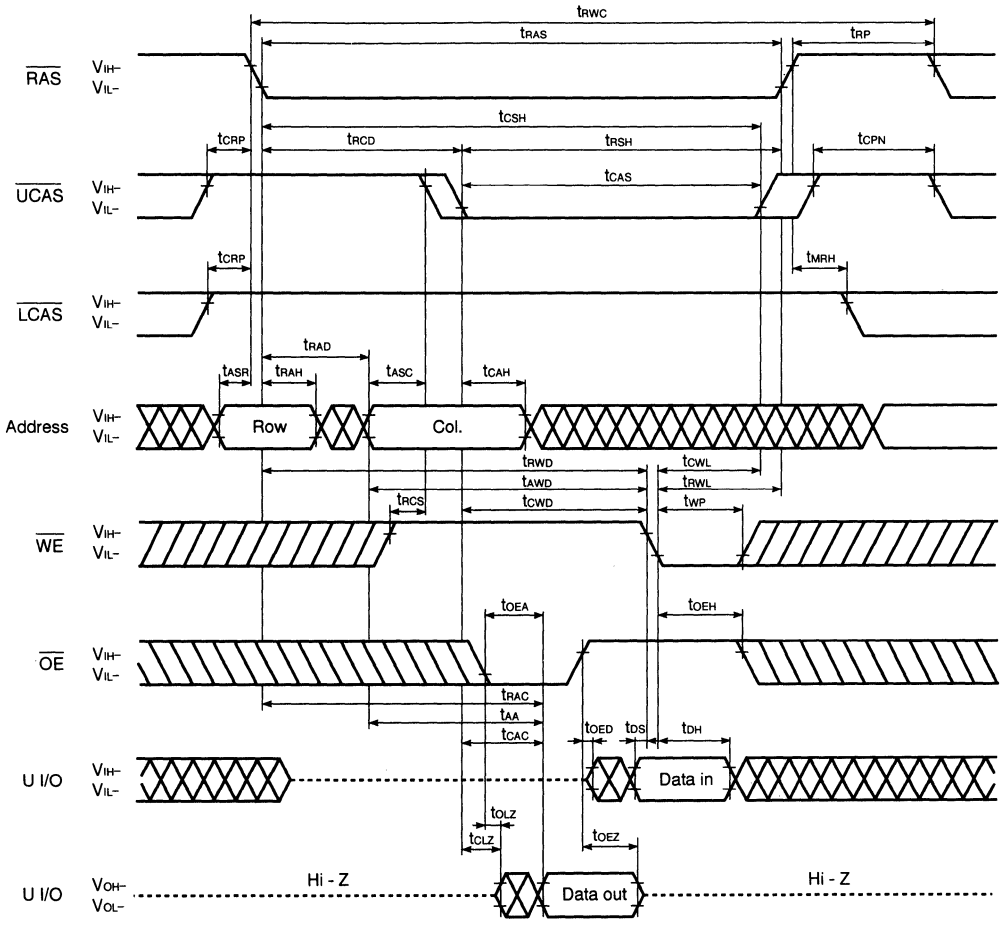


Remark U I/O: Don't care

Read Modify Write Cycle

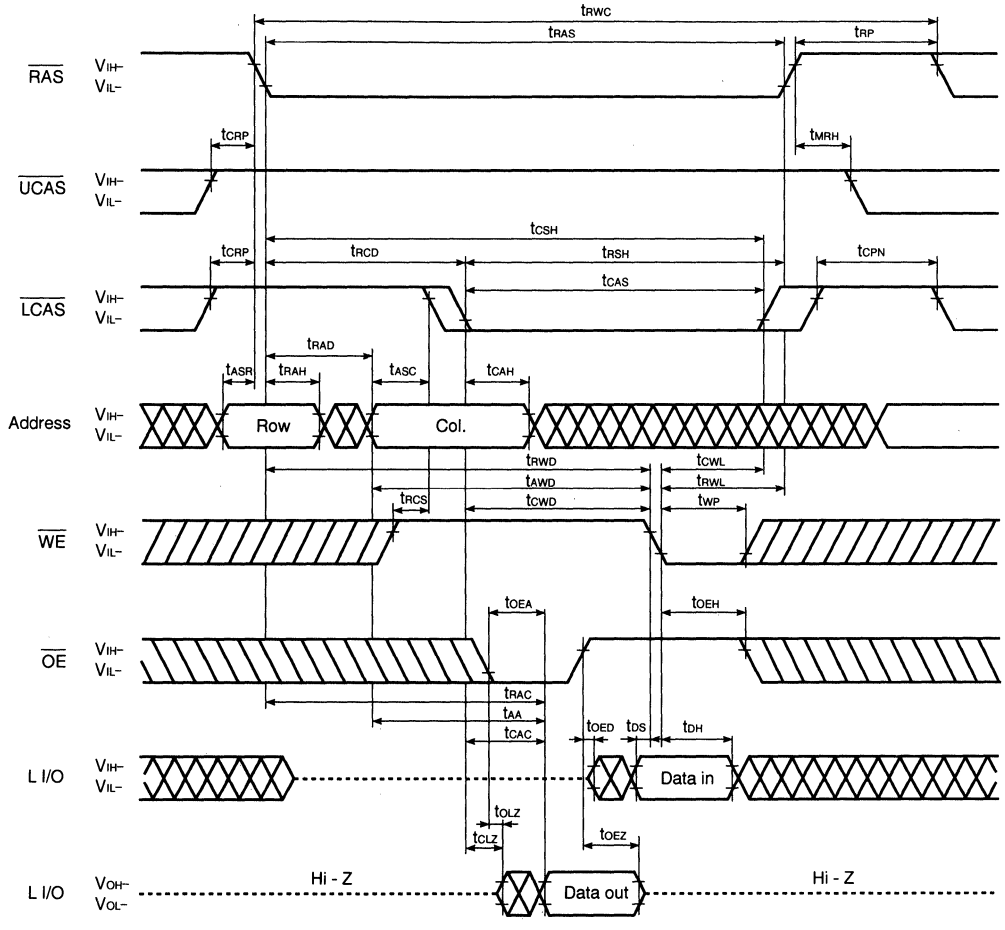


Upper Byte Read Modify Write Cycle



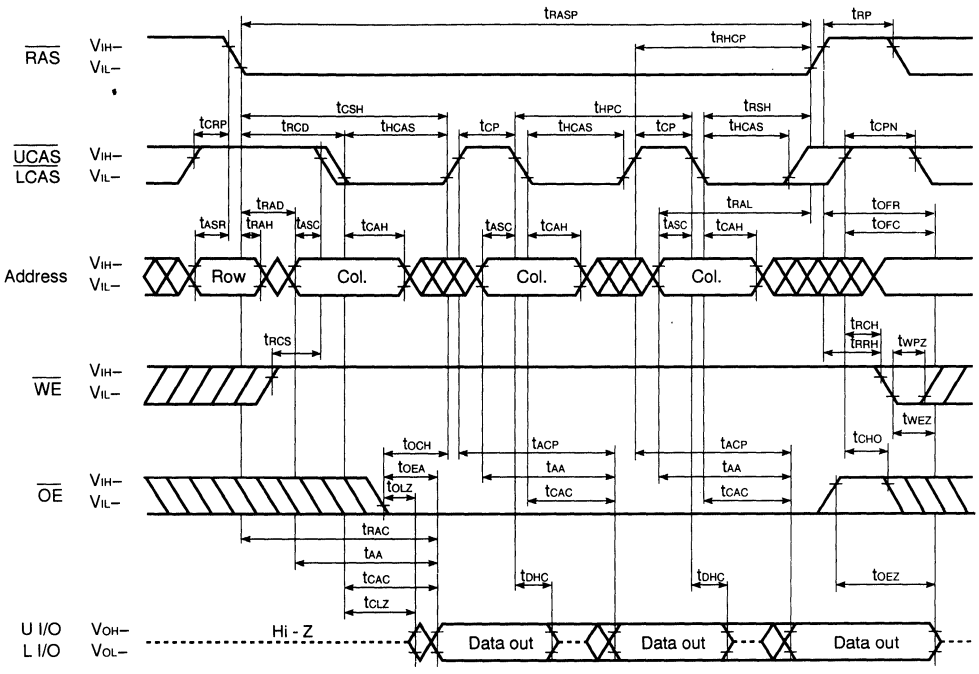
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



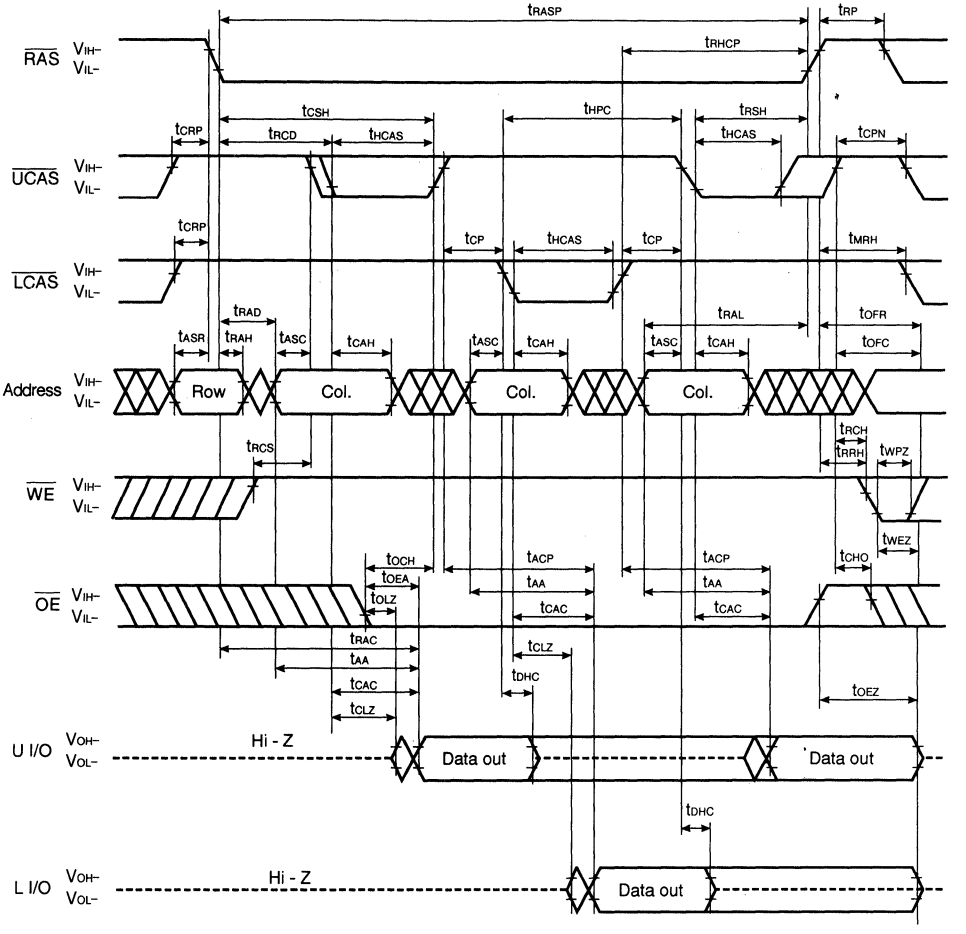
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

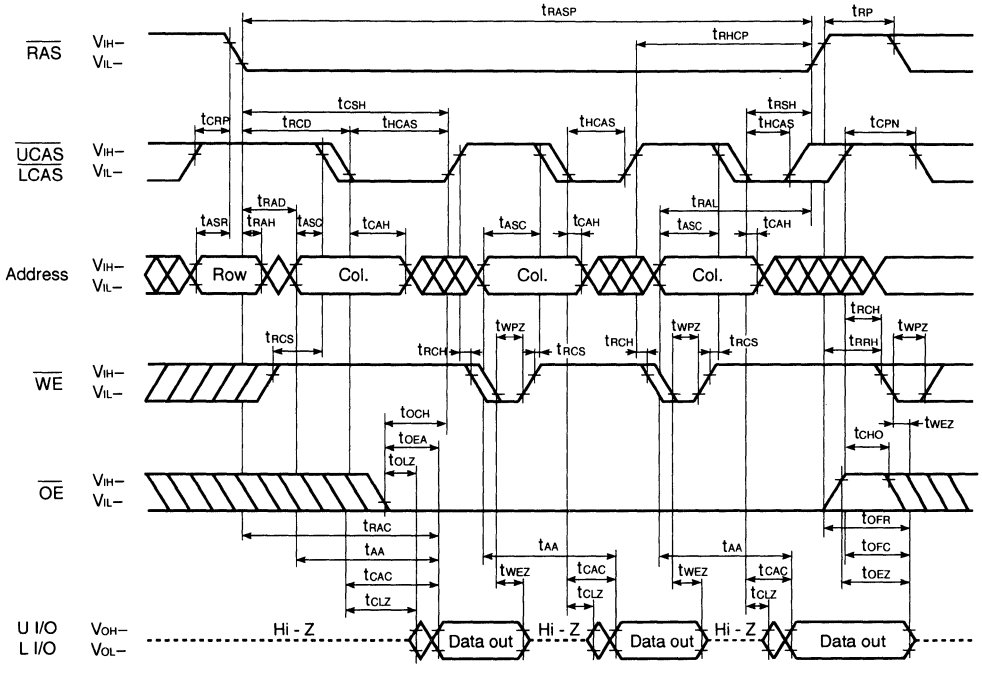
Hyper Page Mode (EDO) Byte Read Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

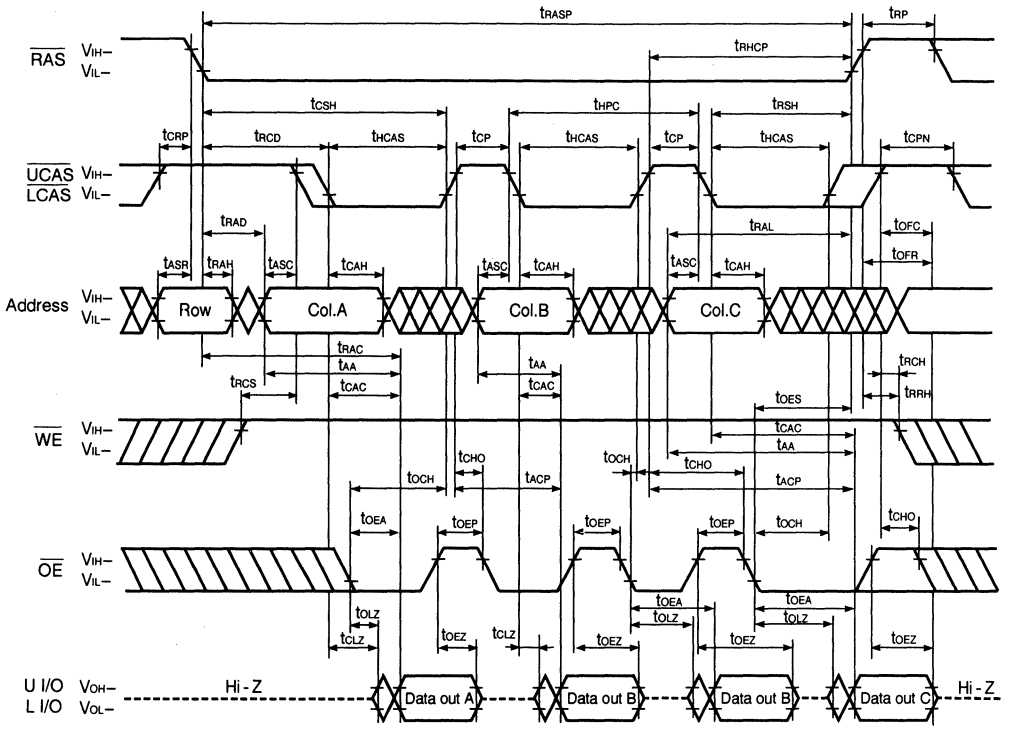
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



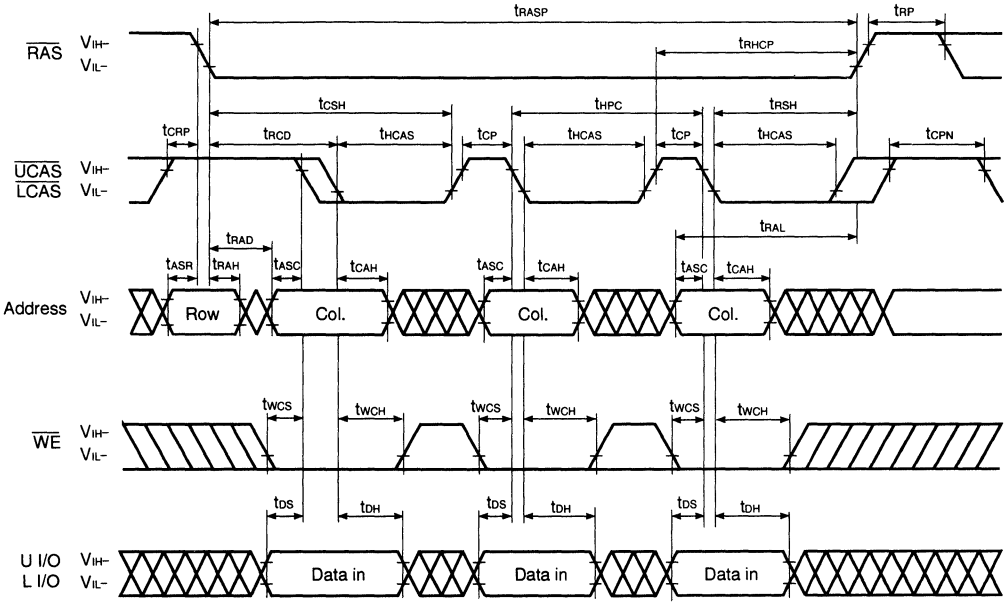
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

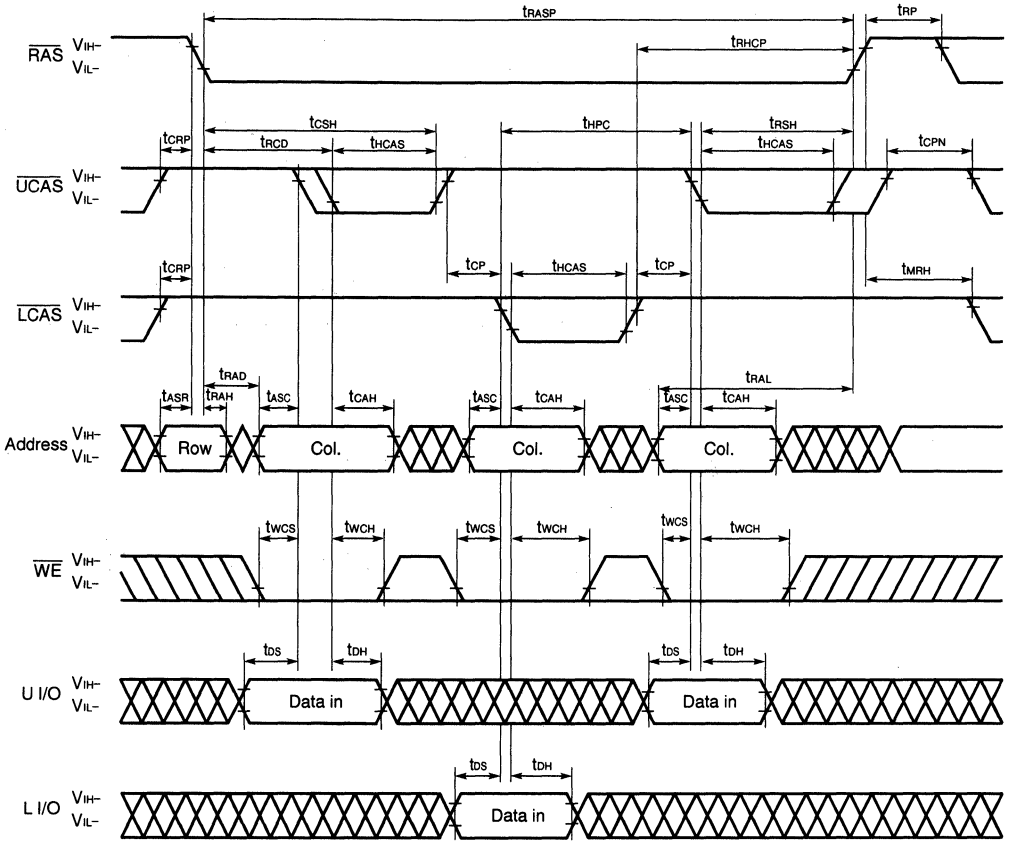
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

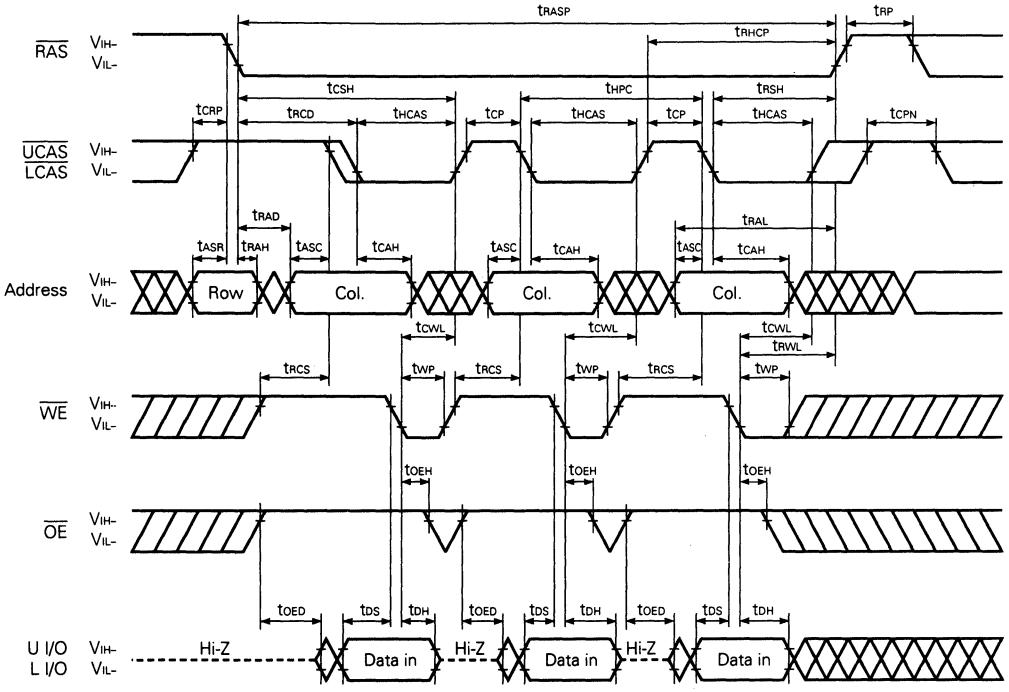
Hyper Page Mode (EDO) Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

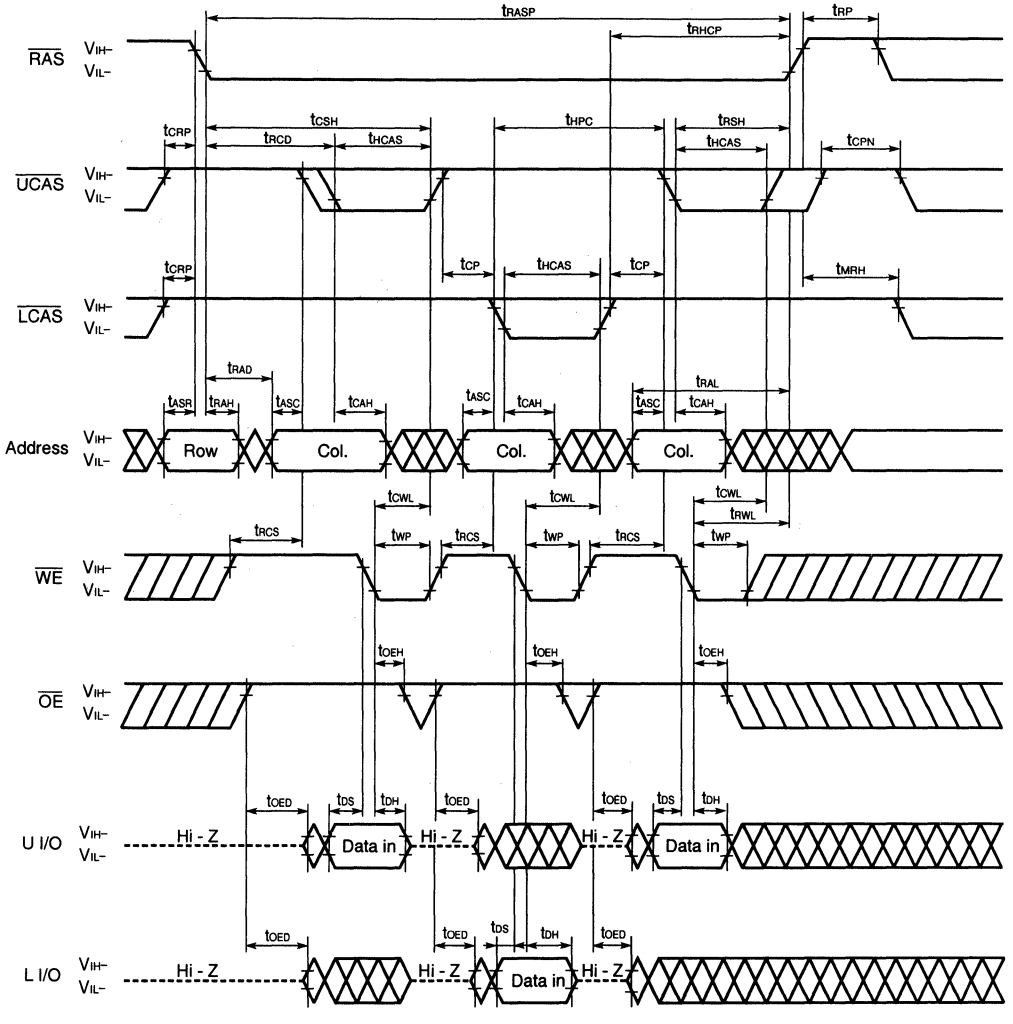
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

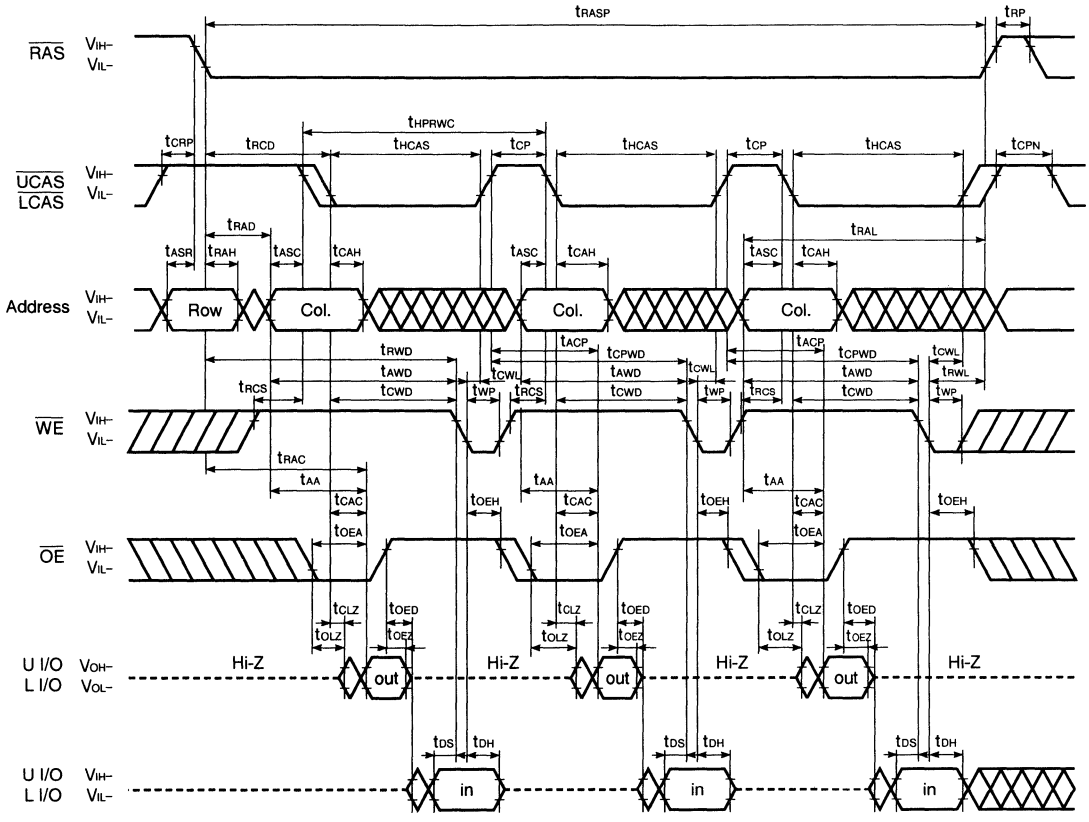
Hyper Page Mode (EDO) Byte Late Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

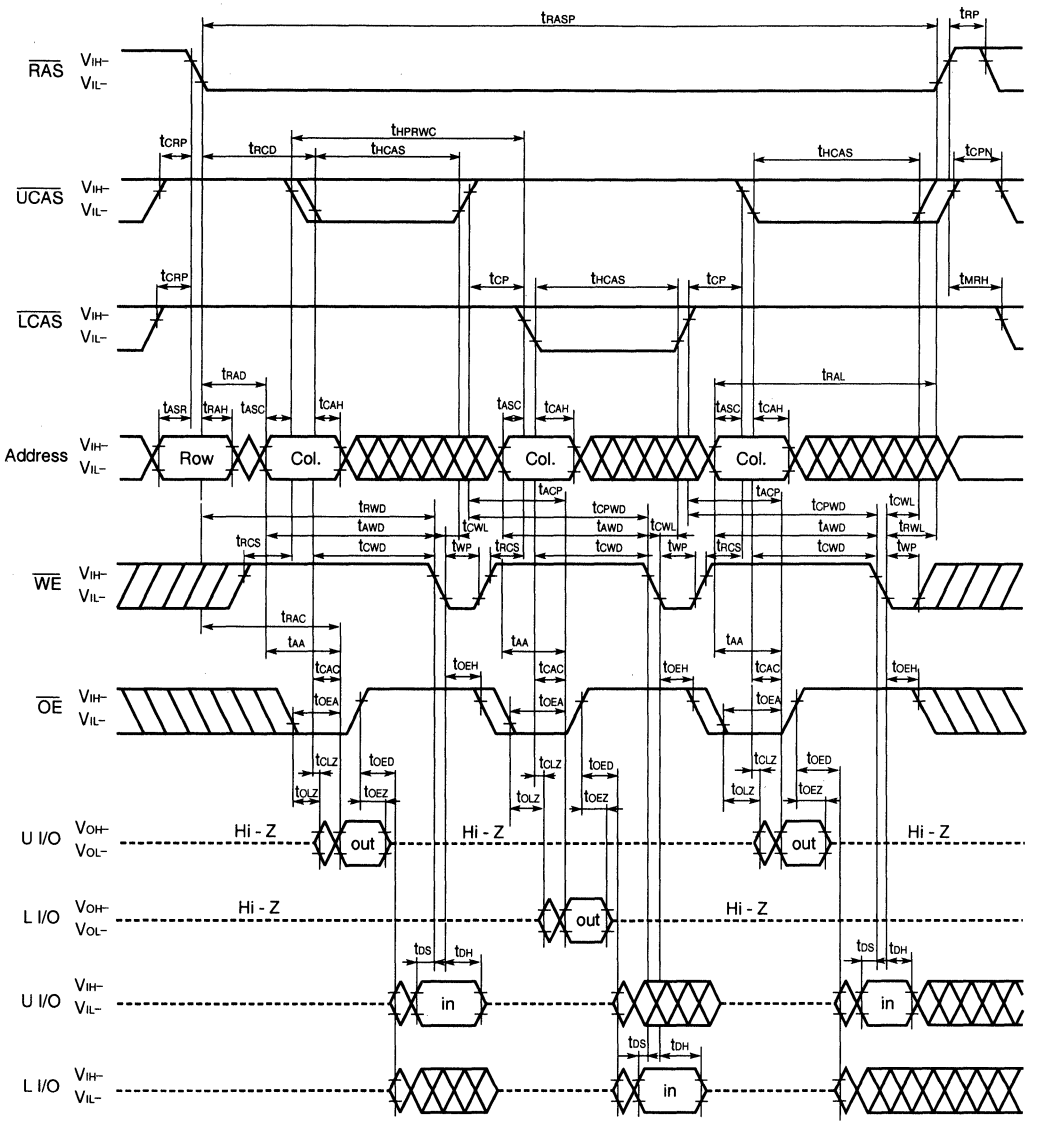
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

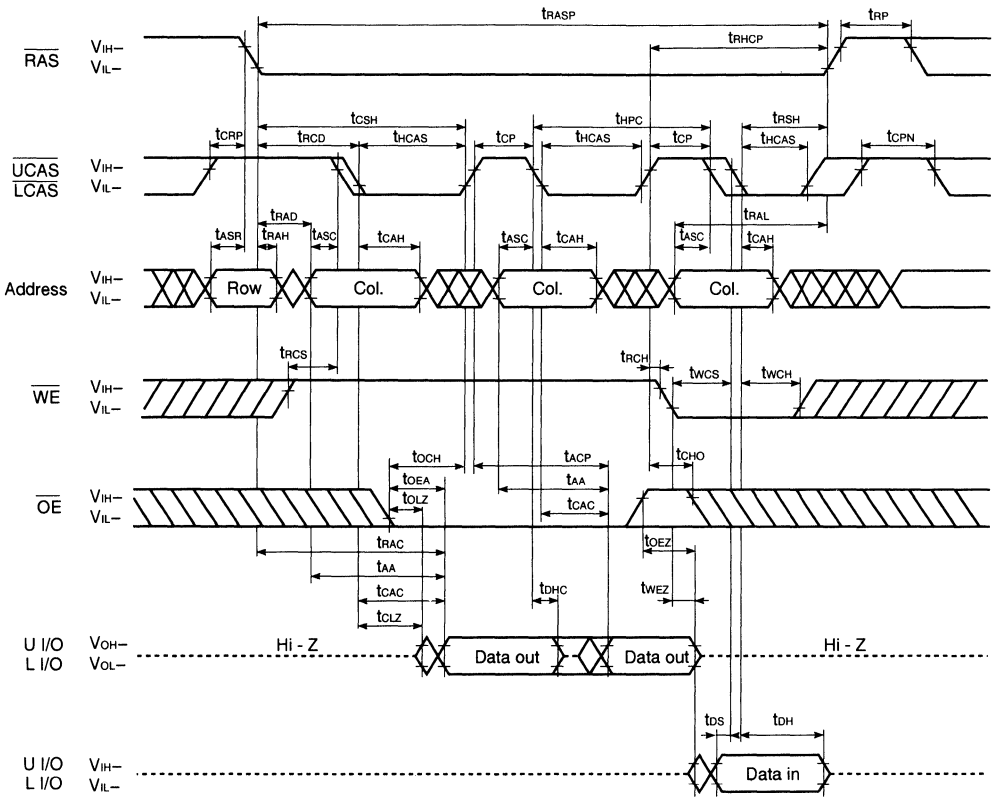
Hyper Page Mode (EDO) Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

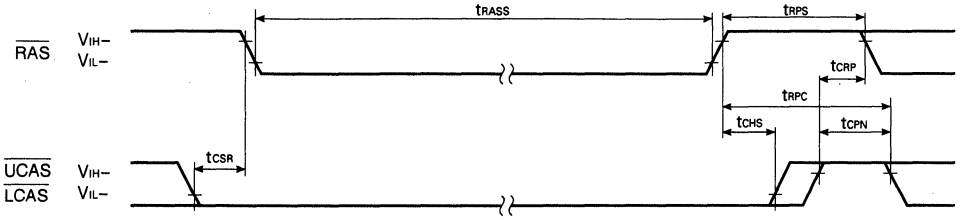
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16165L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

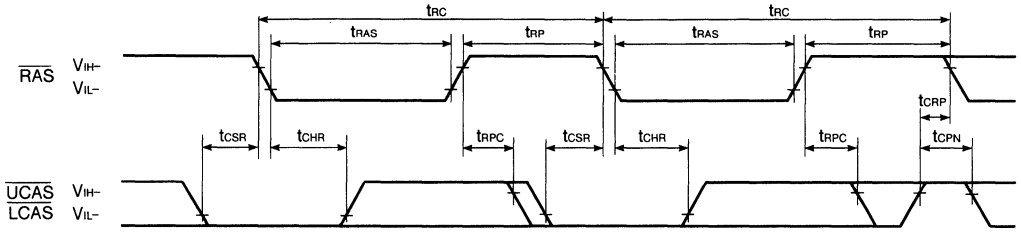
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 4,096 times within a 64 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (4,096/128 ms) should be met.

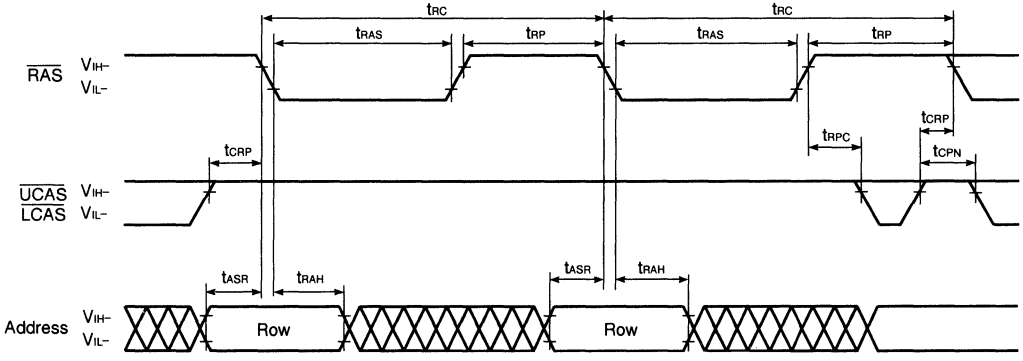
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



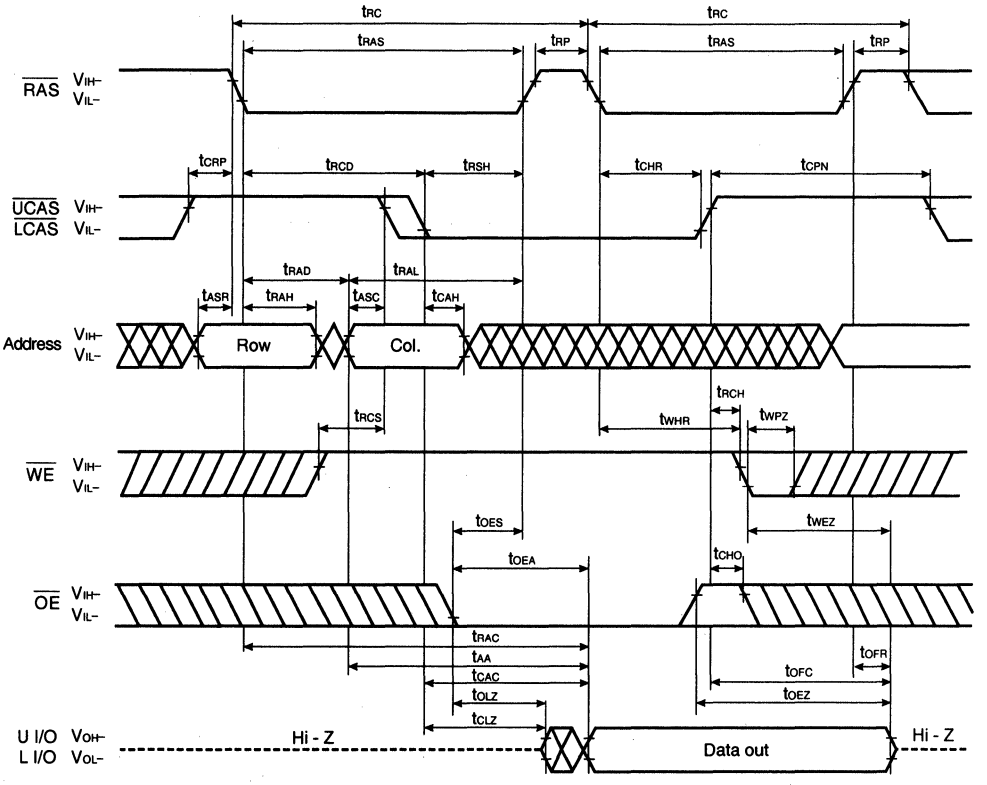
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

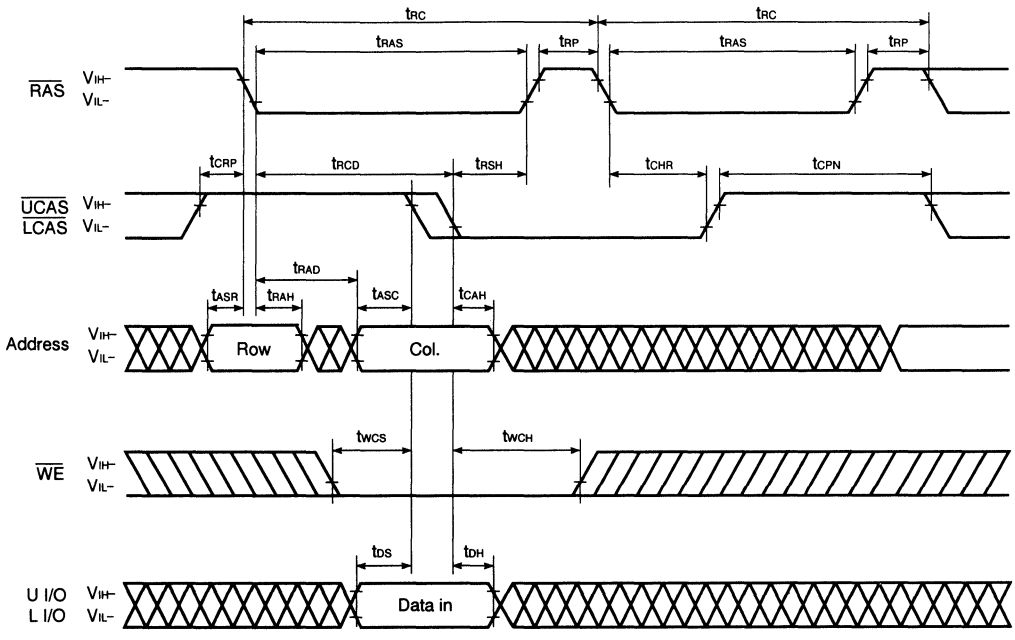


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



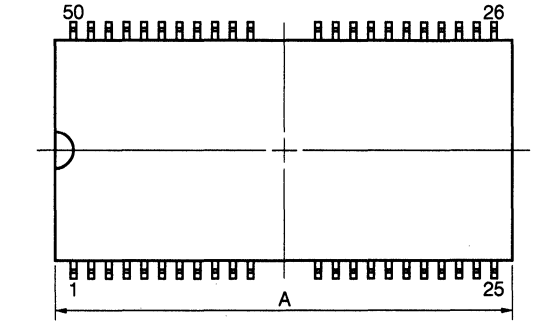
Hidden Refresh Cycle (Write)



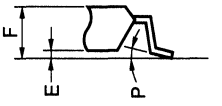
Remark $\overline{OE}$: Don't care

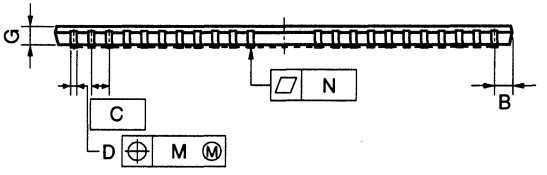
Package Drawings

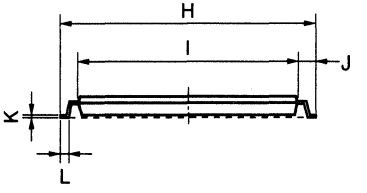
50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







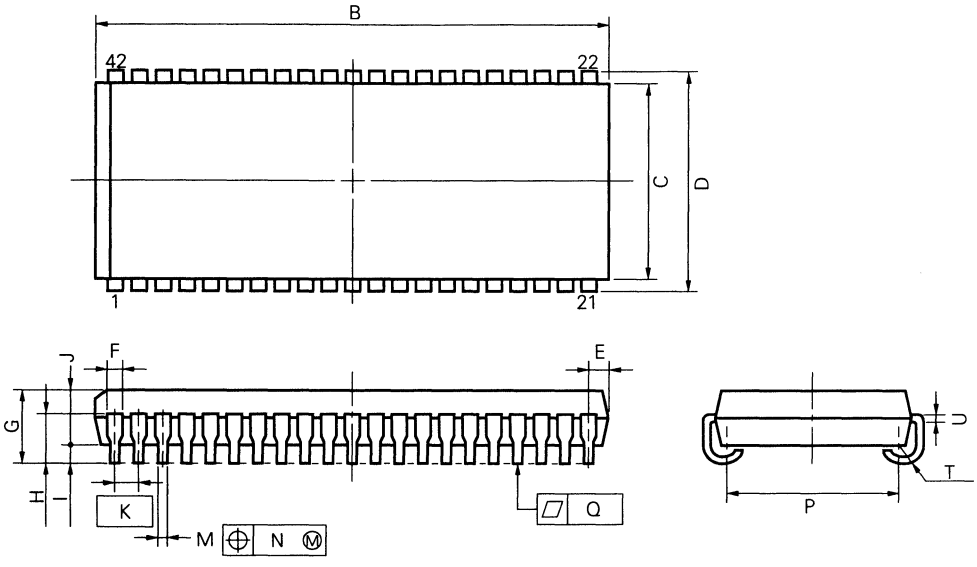
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions must be met for soldering conditions of the μPD42S16165L, 4216165L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16165LG5, 4216165LG5: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16165LLE, 4216165LLE: 42-pin plastic SOJ (400 mil)

Please consult with our sales offices for soldering conditions of the μPD42S16165LLE, 4216165LLE.

NEC

MOS INTEGRATED CIRCUIT

μPD42S18165L, 4218165L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 1 M-WORD BY 16-BIT, HYPER PAGE MODE (EDO), BYTE READ/WRITE MODE

Description

The μPD42S18165L, 4218165L are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S18165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S18165L, 4218165L are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 1,048,576 words by 16 bits organization
- Single +3.3 V ±0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S18165L-A60, 4218165L-A60	540 mW	60 ns	104 ns	25 ns
μPD42S18165L-A70, 4218165L-A70	504 mW	70 ns	124 ns	30 ns

- The μPD42S18165L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

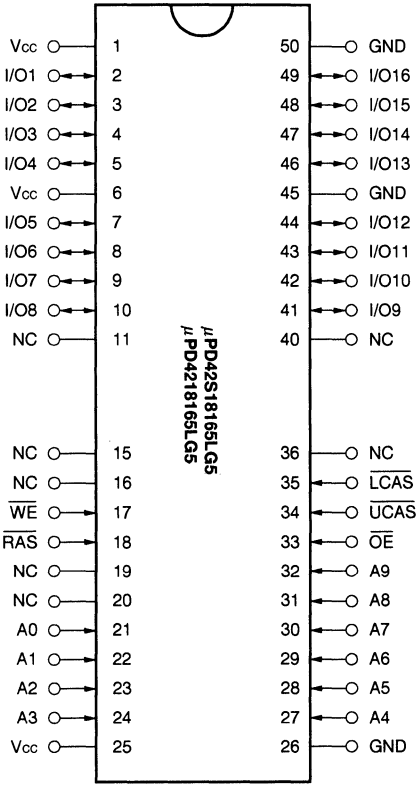
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S18165L	1,024 cycles / 128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4218165L	1,024 cycles / 16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

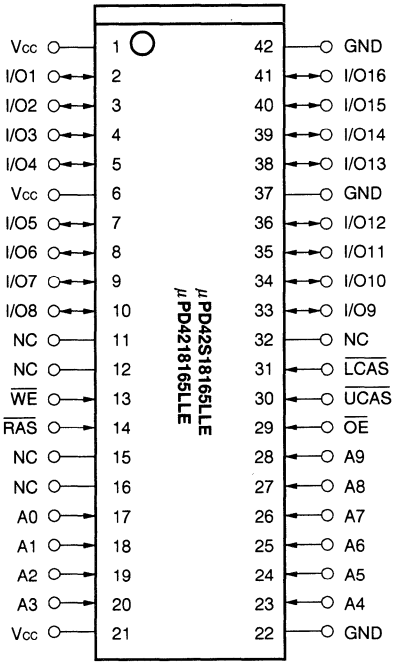
Part number	Access time (MAX.)	Package	Refresh
μPD42S18165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18165LG5-A70	70 ns		
μPD42S18165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD42S18165LLE-A70	70 ns		
μPD4218165LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218165LG5-A70	70 ns		
μPD4218165LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD4218165LLE-A70	70 ns		

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

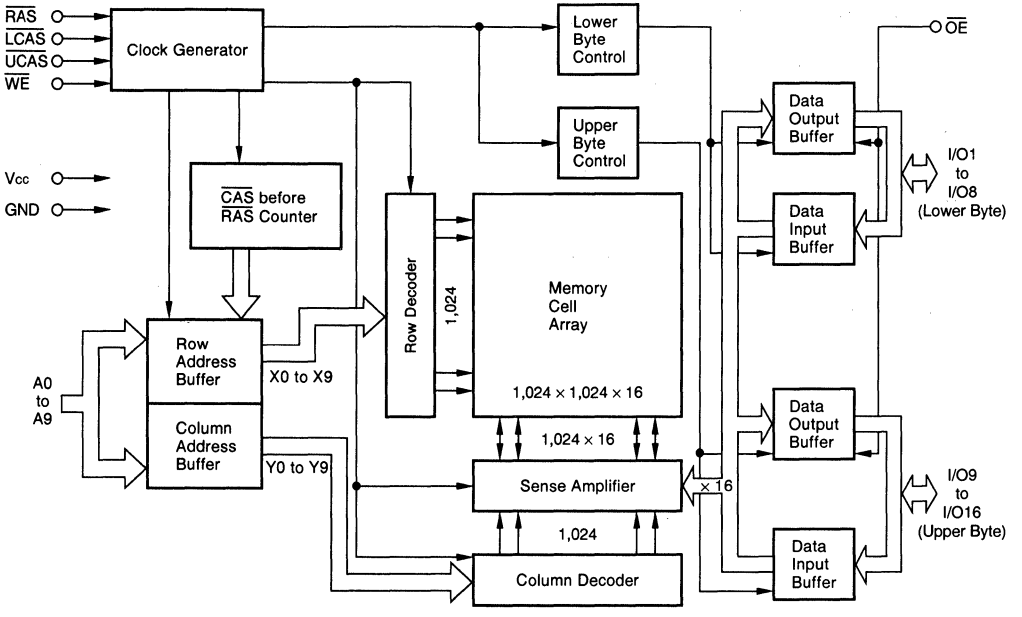


42-pin Plastic SOJ (400 mil)



A0 to A9	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S18165L, 4218165L have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

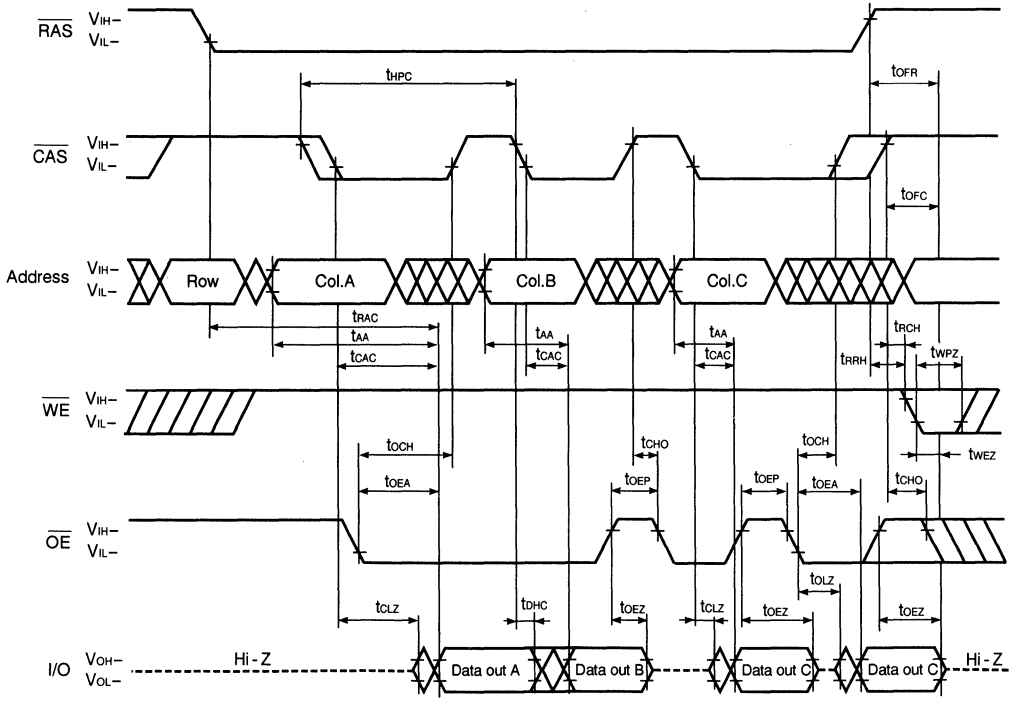
The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. **Data output time is extended.**
   In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**
   In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		150	mA	1, 2, 3
			t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		140		
Standby current	μPD42S18165L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4218165L		$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$	t_{RAC} = 60 ns		150	mA	1, 2, 3, 4
			t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		140		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		110	mA	1, 2, 5
			t_{HPC} = $t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		150	mA	1, 2
			t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18165L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		180	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S18165L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$ and $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$.

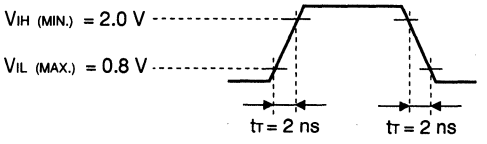
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

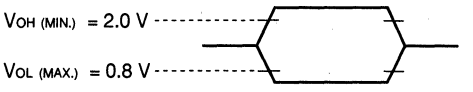
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

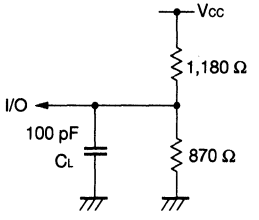
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	104	–	124	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		tRSH	10	–	12	–	ns	
$\overline{CAS}$ hold time		tCSH	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	14	45	14	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		tMRH	0	–	0	–	ns	
Transition time (rise and fall)		tT	1	50	1	50	ns	
Refresh time	μPD42S18165L	tREF	–	128	–	128	ms	4
	μPD4218165L		–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S18165L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	17	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

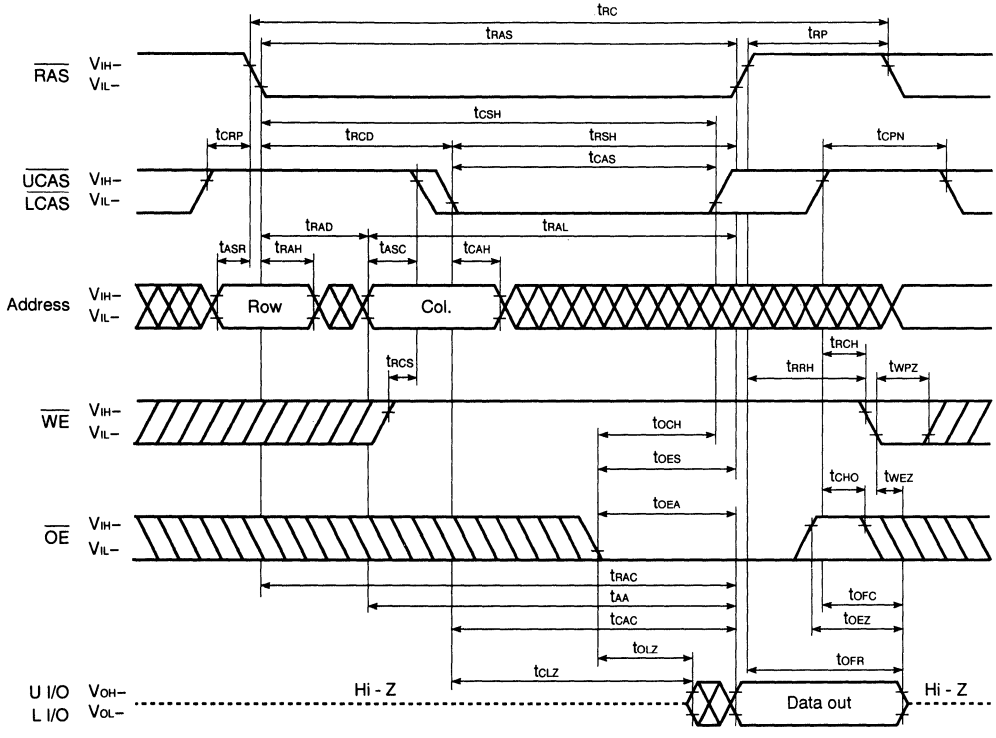
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

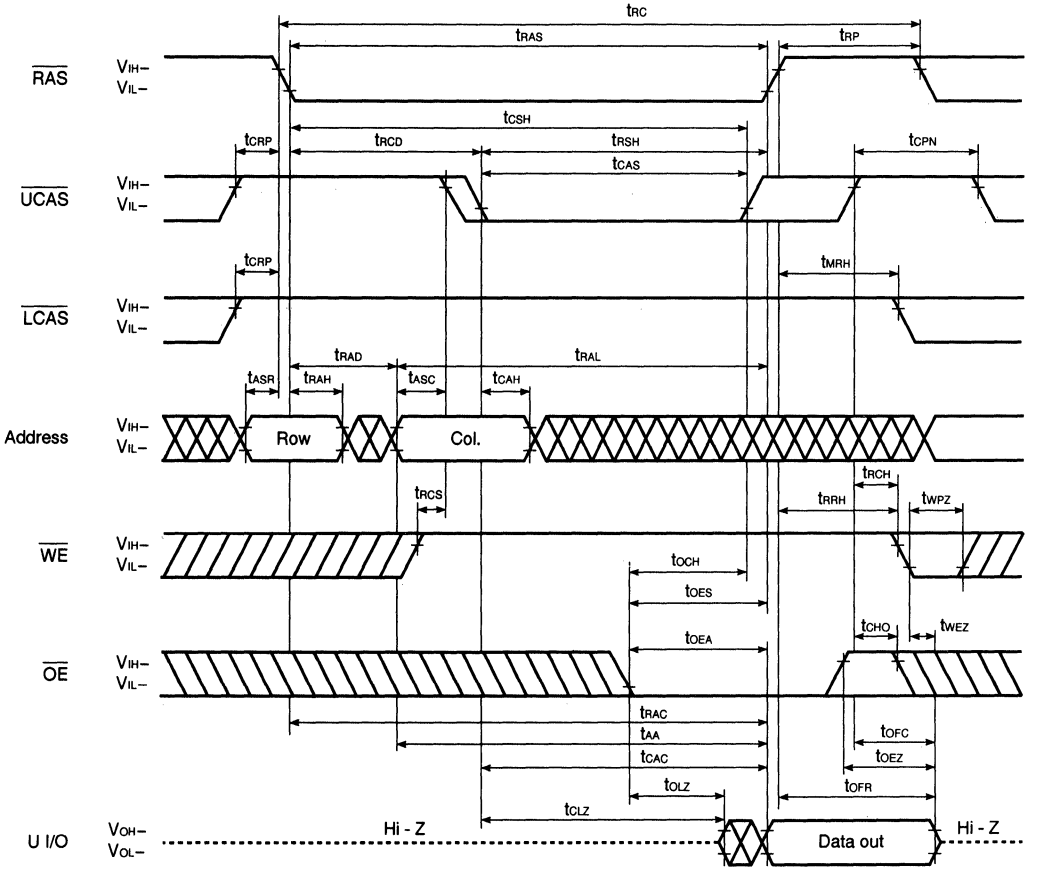
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S18165L.

Read Cycle

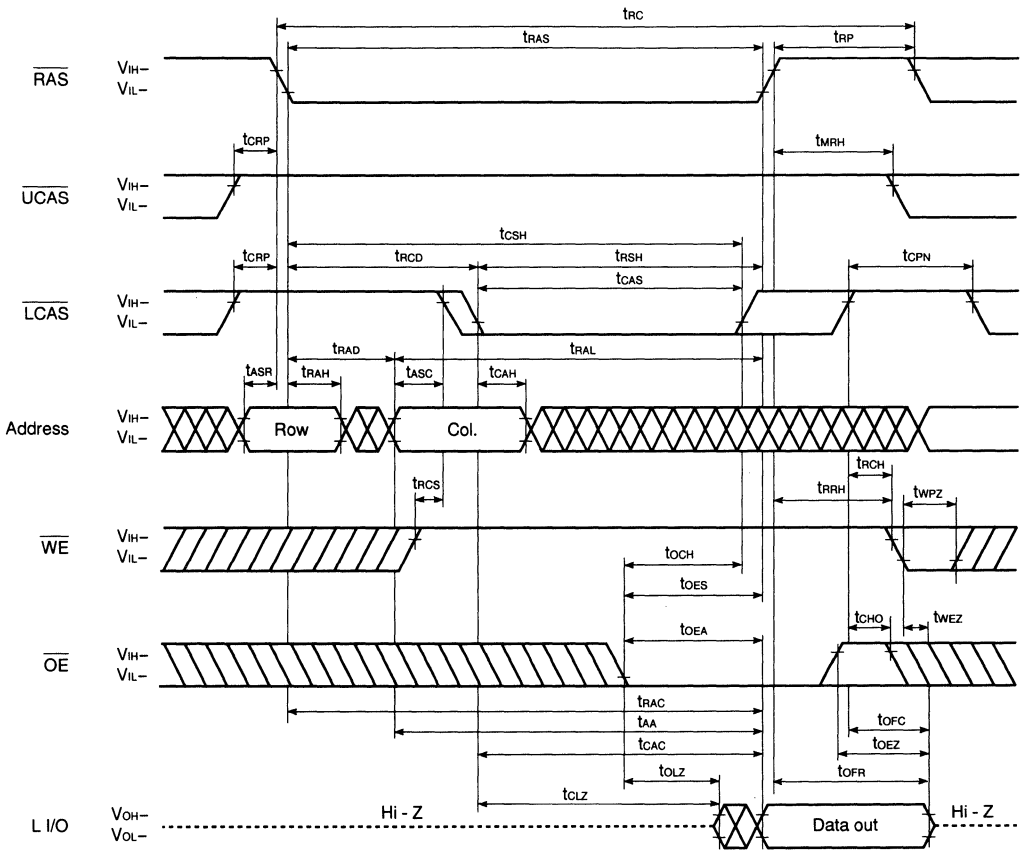

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
OE
tOEA
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



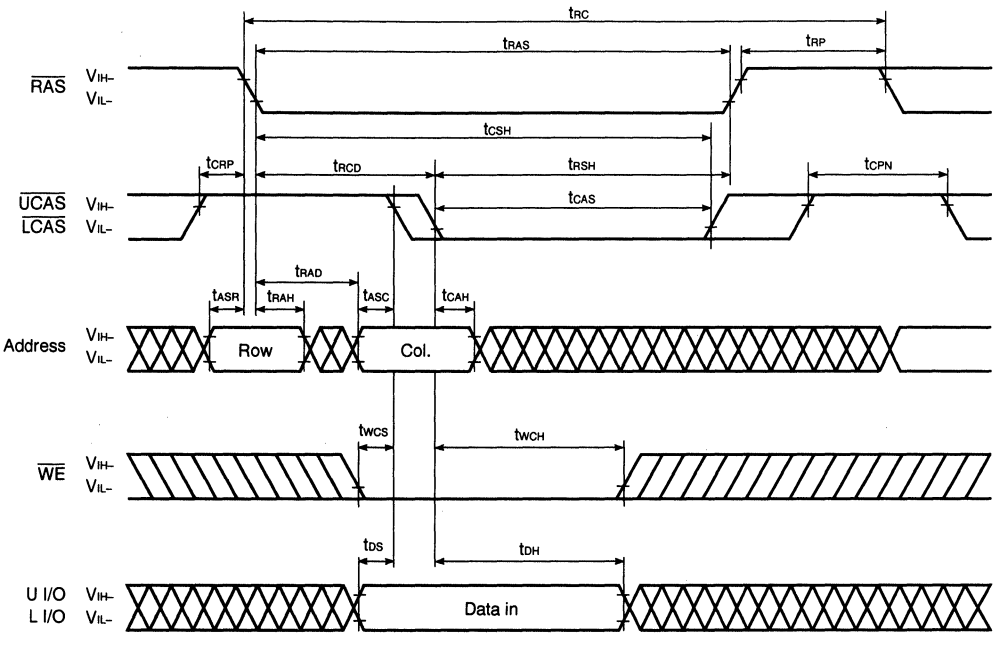
Remark L I/O: Hi-Z

Lower Byte Read Cycle



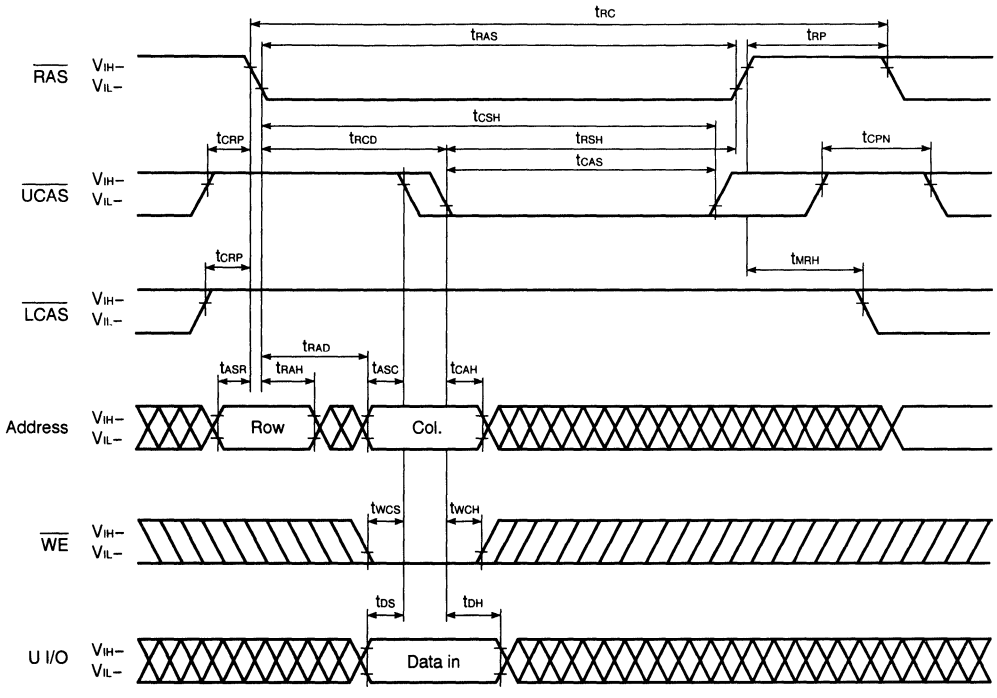
Remark U I/O: Hi-Z

Early Write Cycle



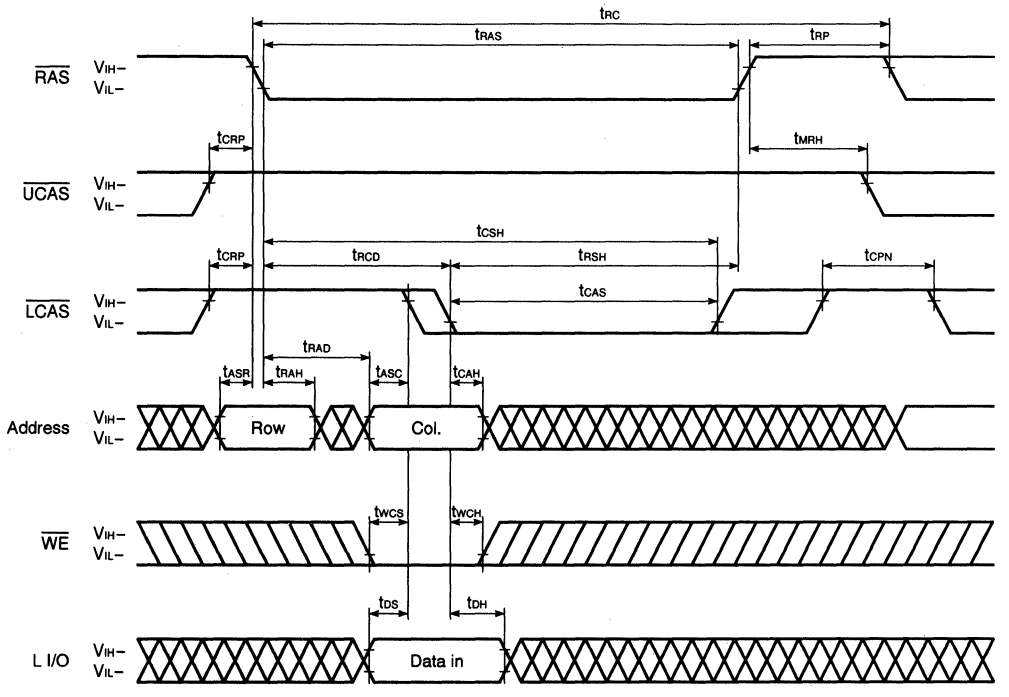
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



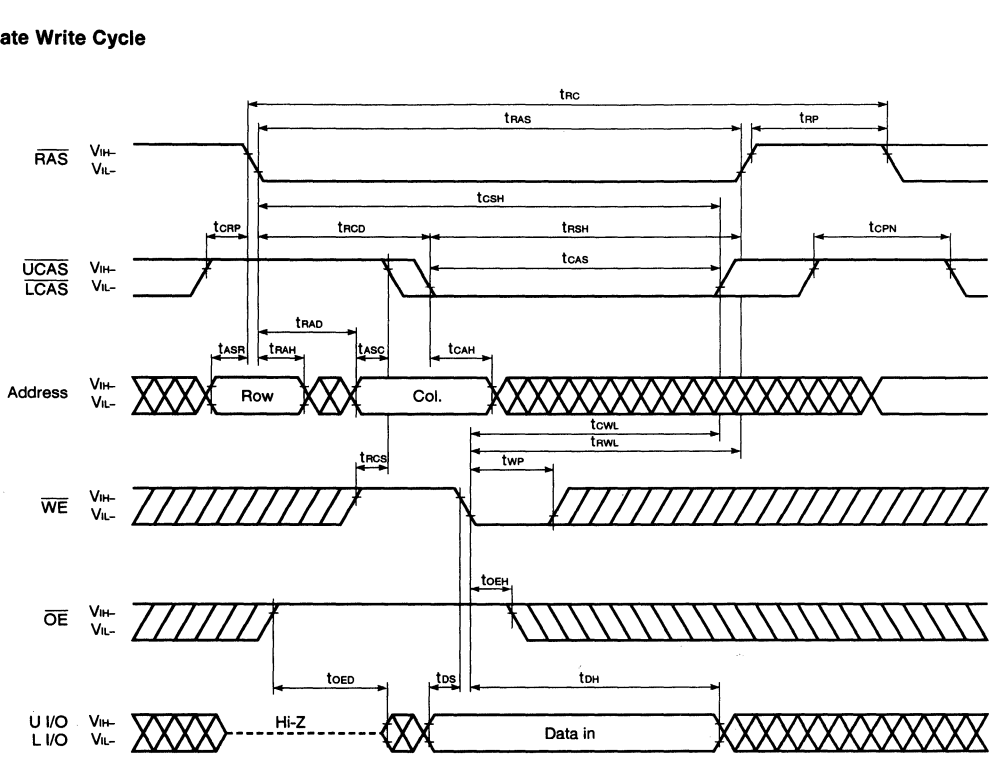
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

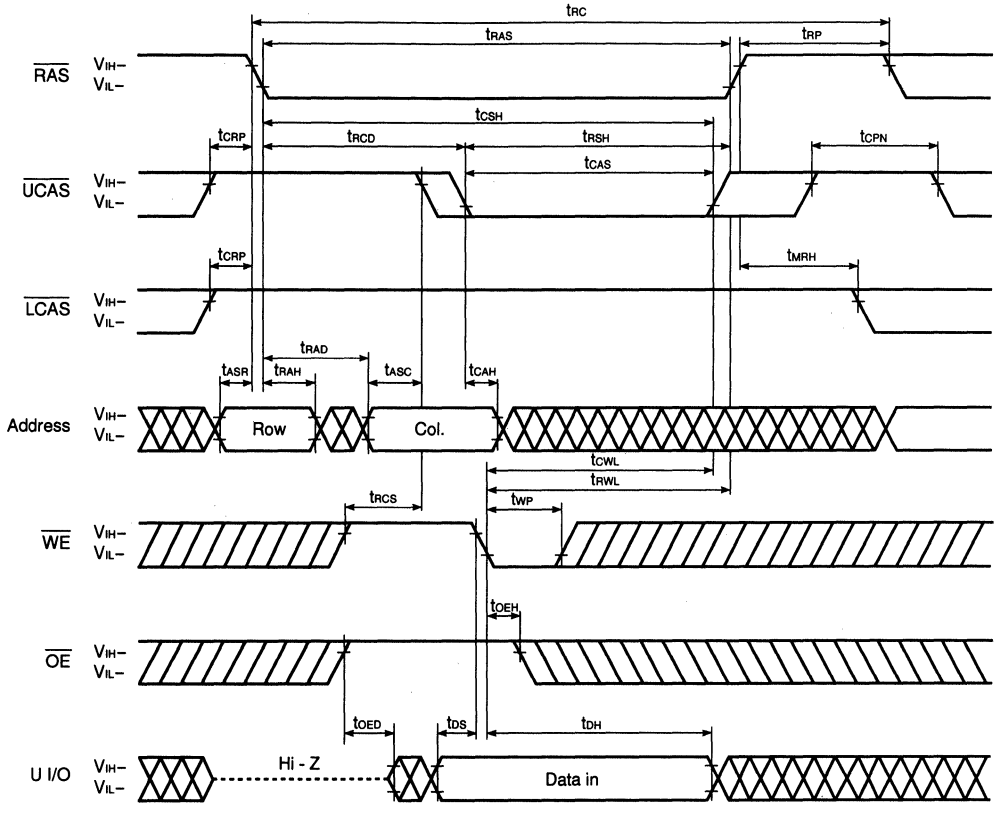


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

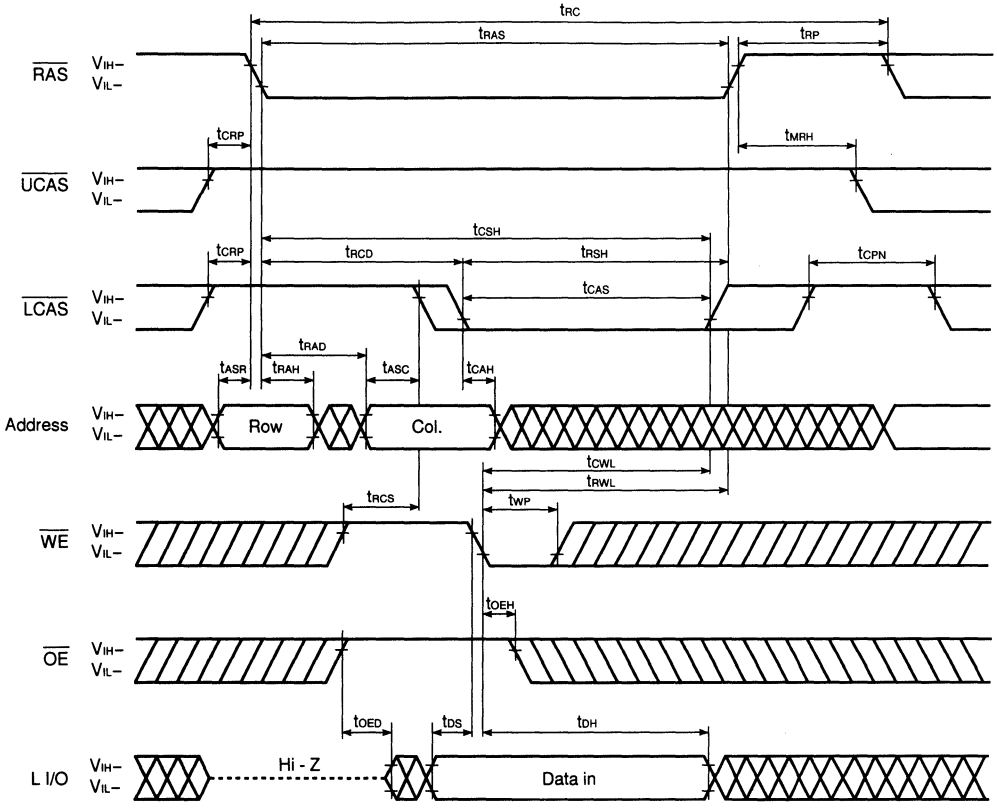


Upper Byte Late Write Cycle



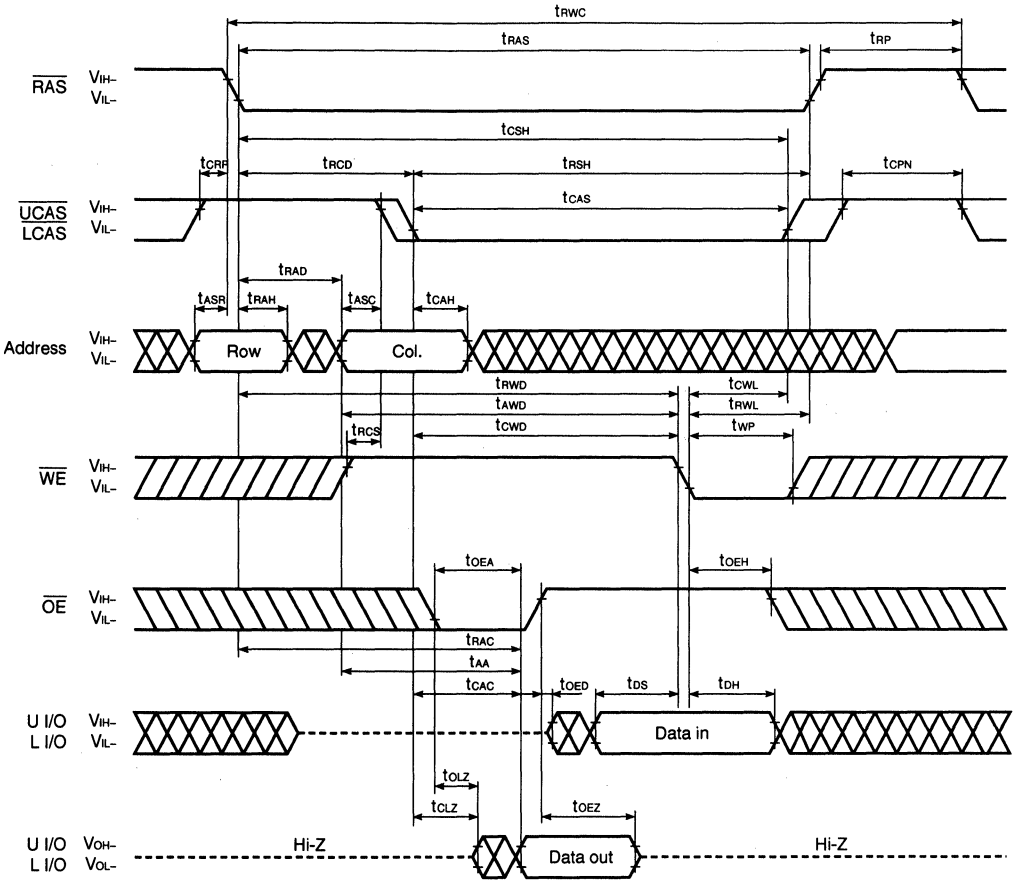
Remark L I/O: Don't care

Lower Byte Late Write Cycle

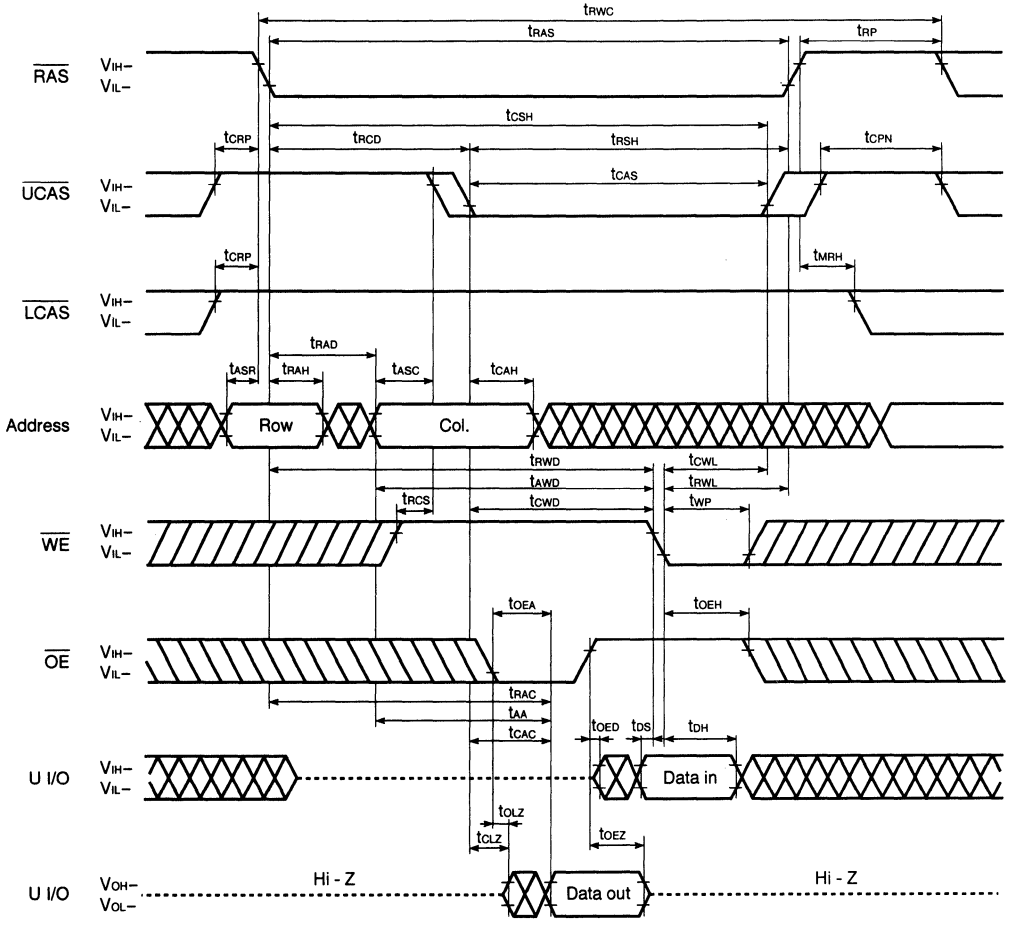


Remark U I/O: Don't care

Read Modify Write Cycle

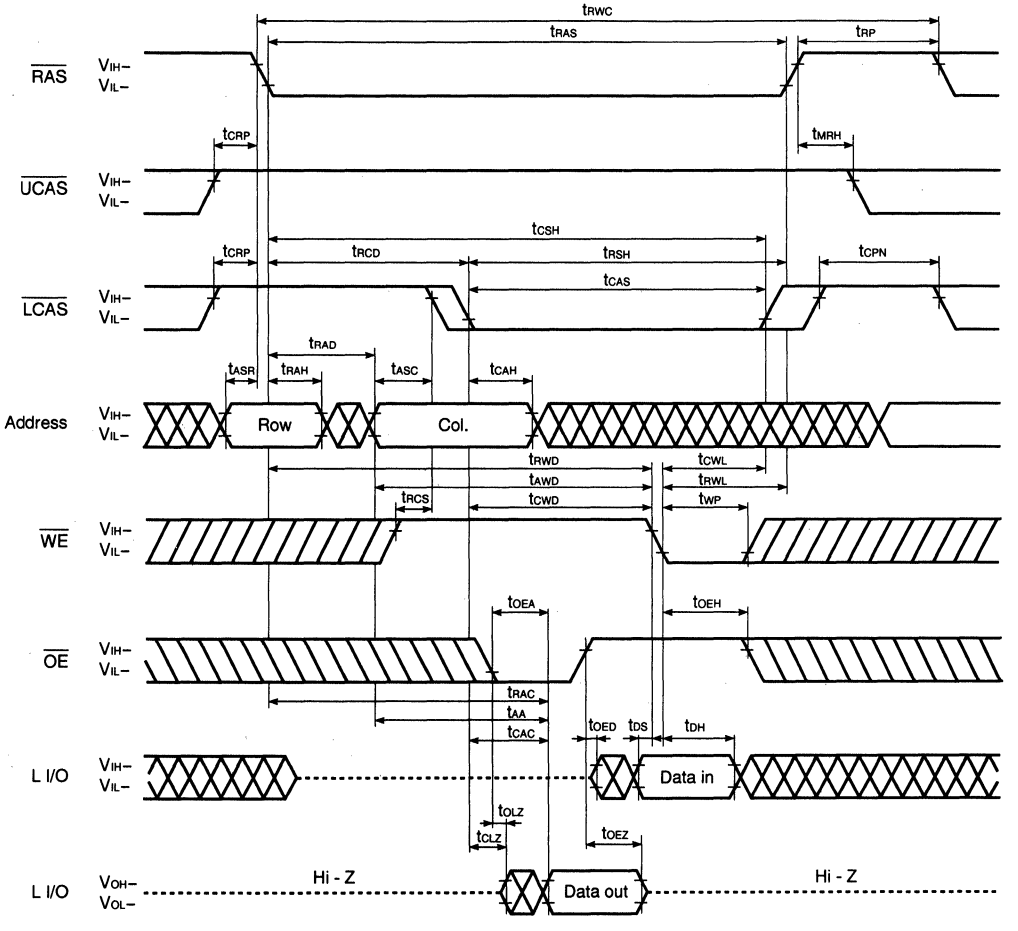


Upper Byte Read Modify Write Cycle



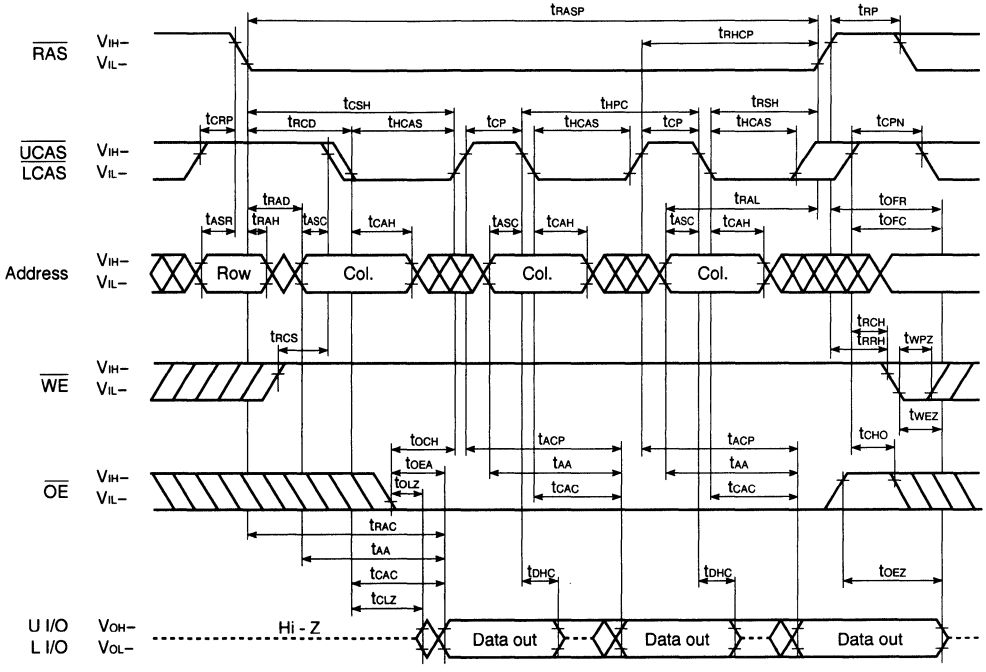
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



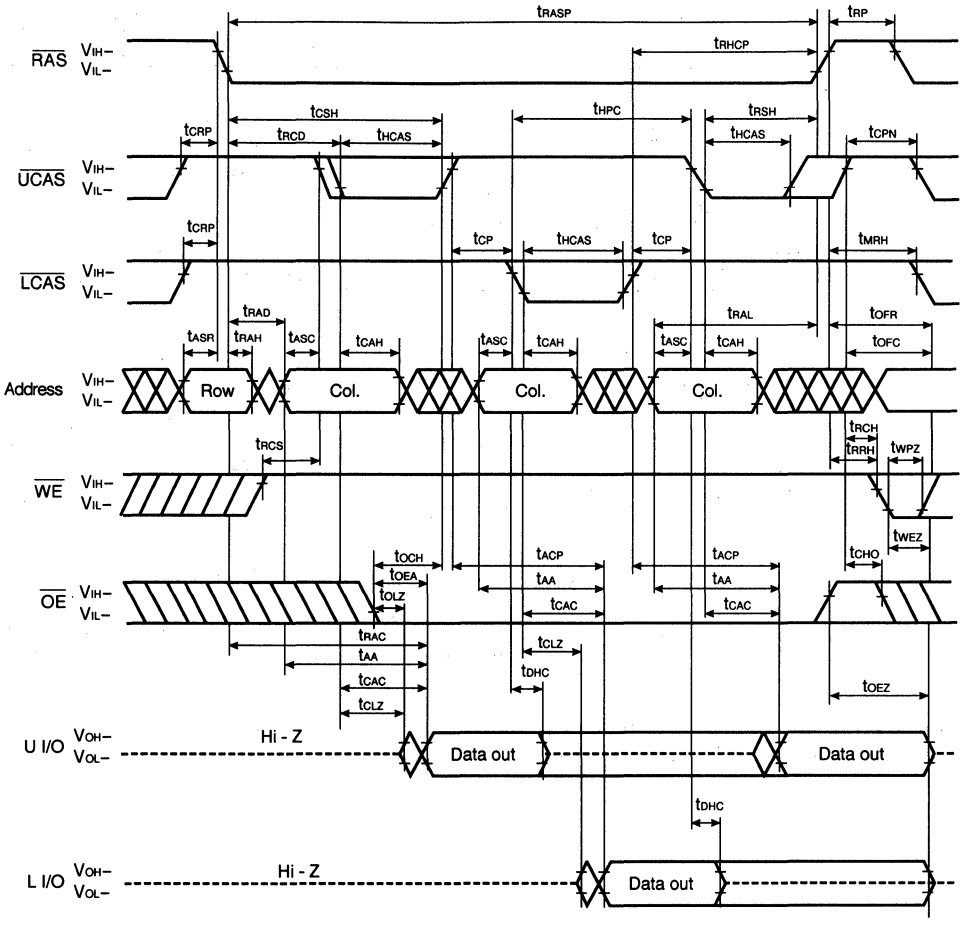
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

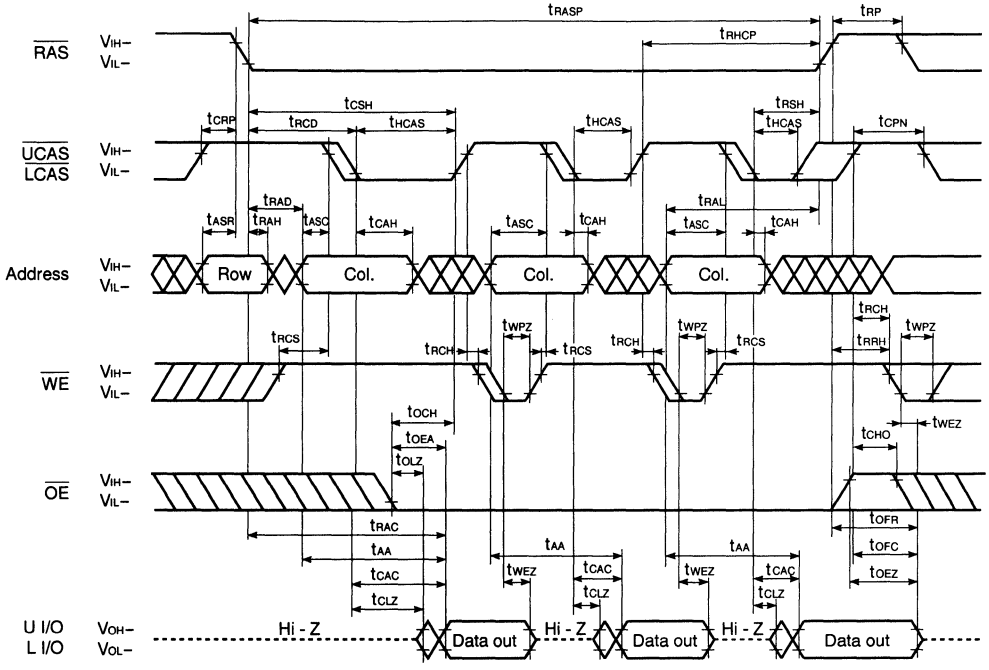
Hyper Page Mode (EDO) Byte Read Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

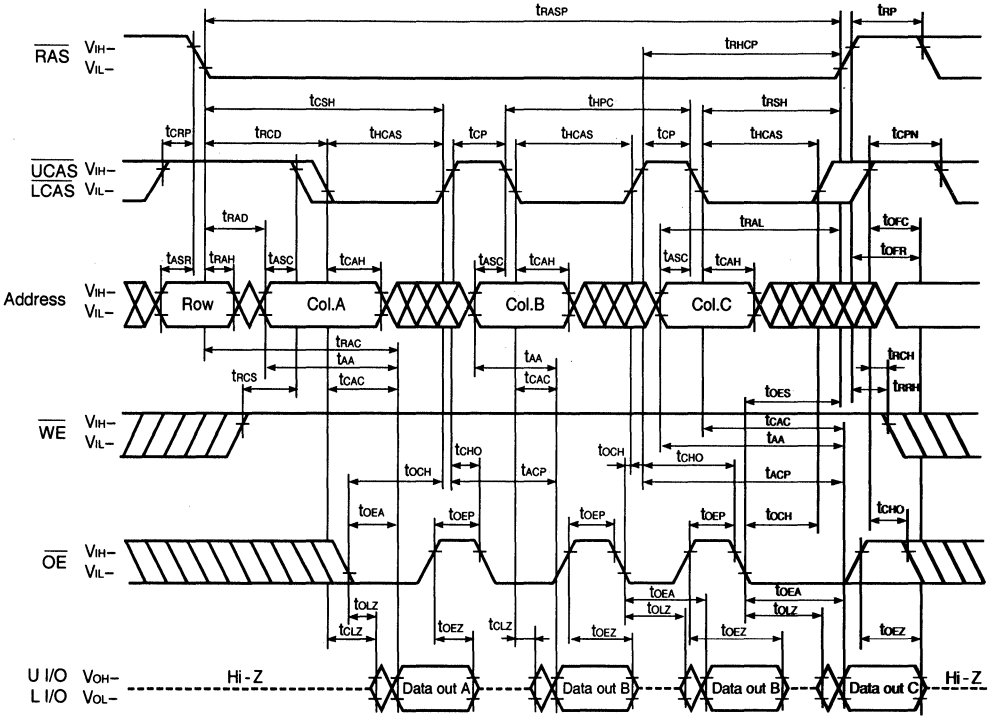
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



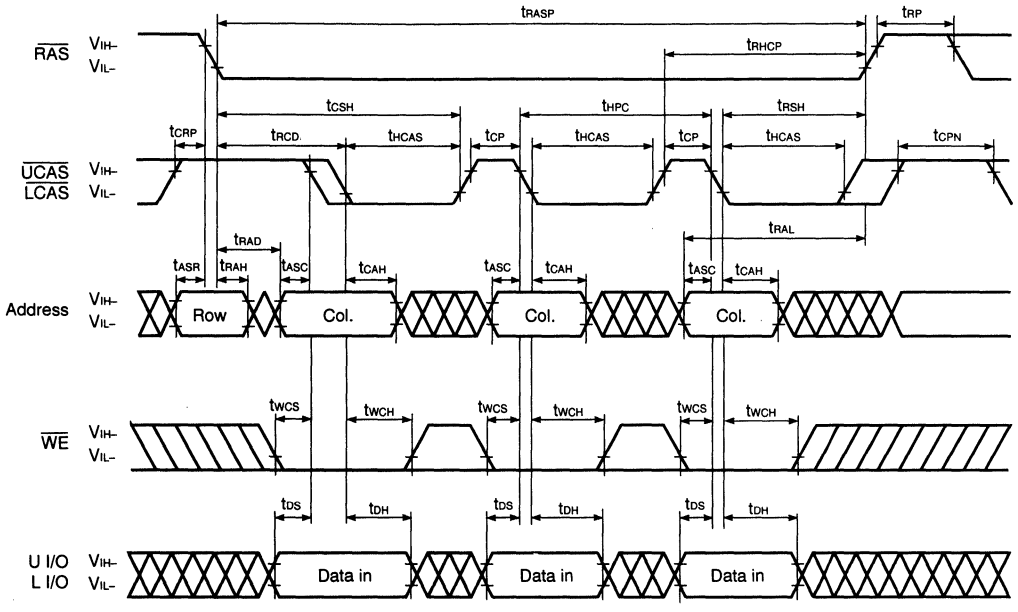
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

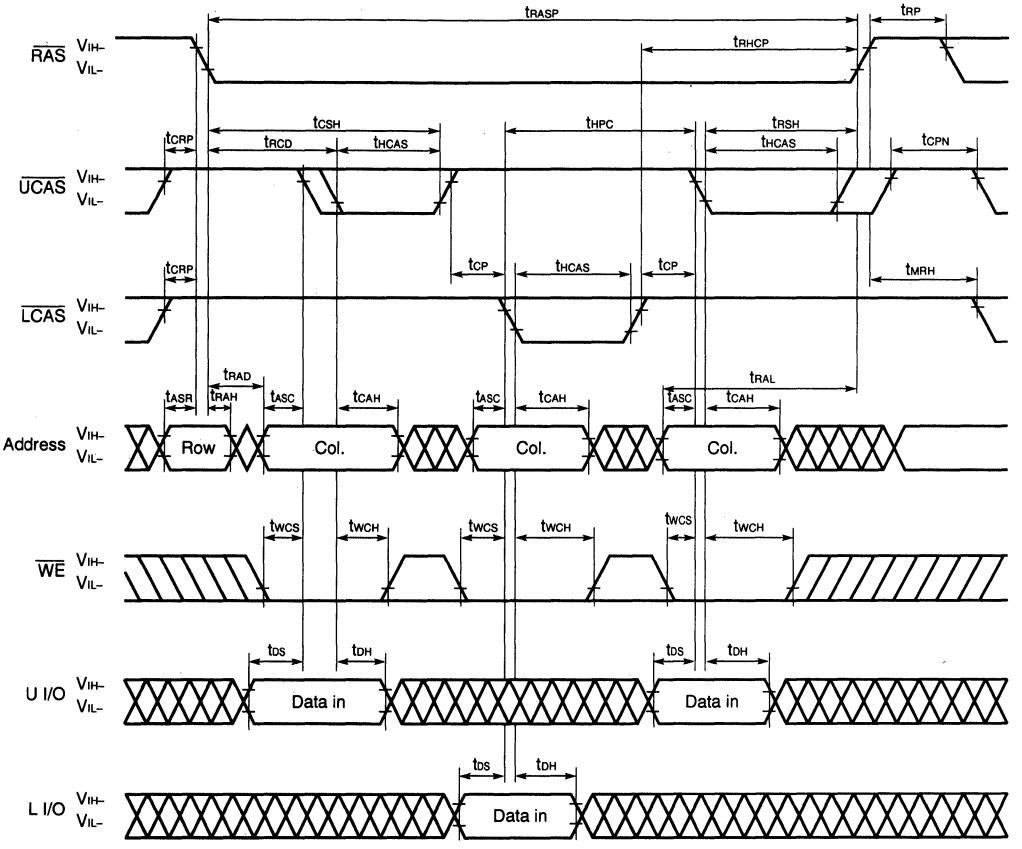
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Byte Early Write Cycle

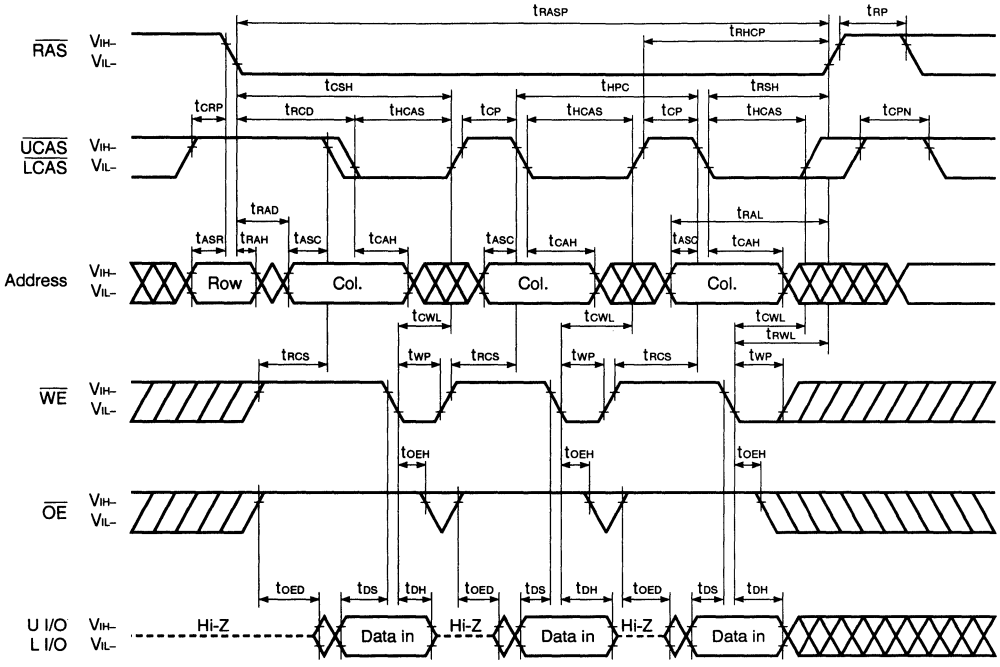


Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

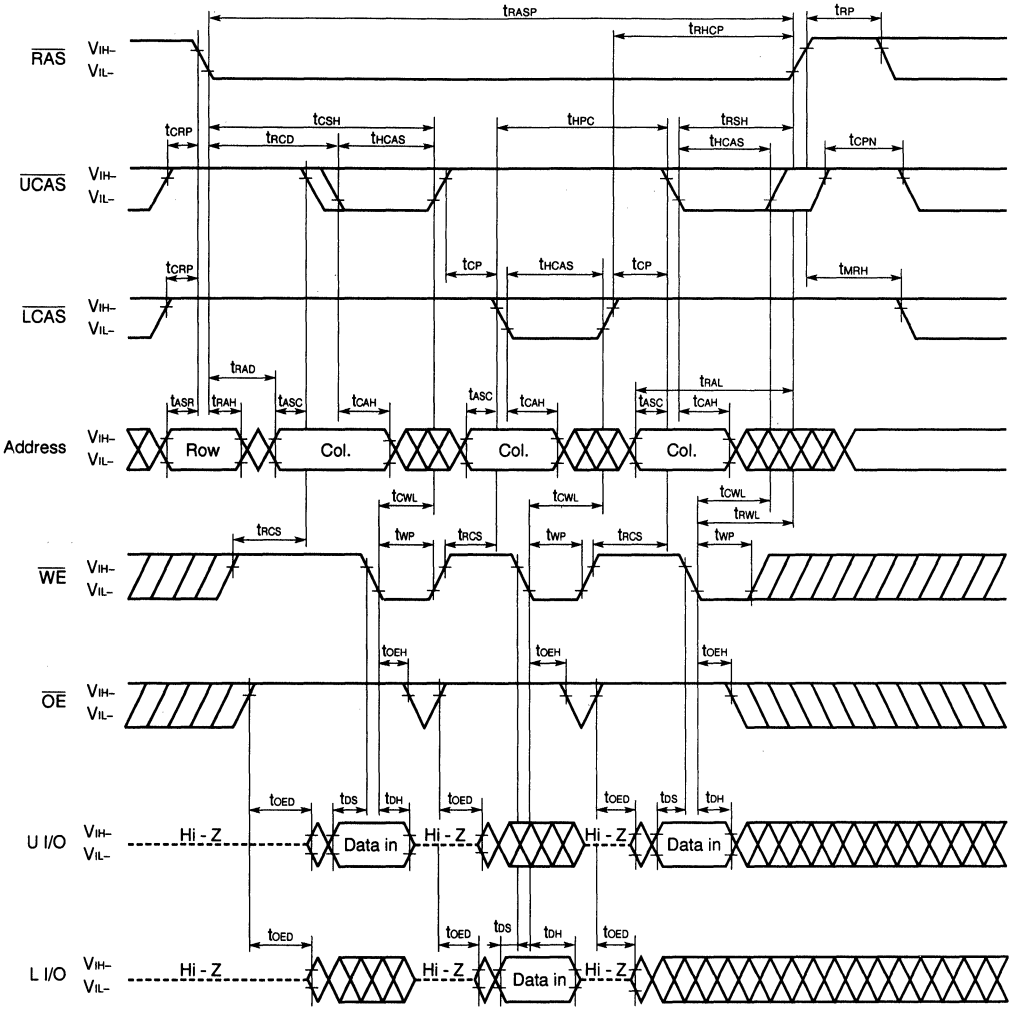
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

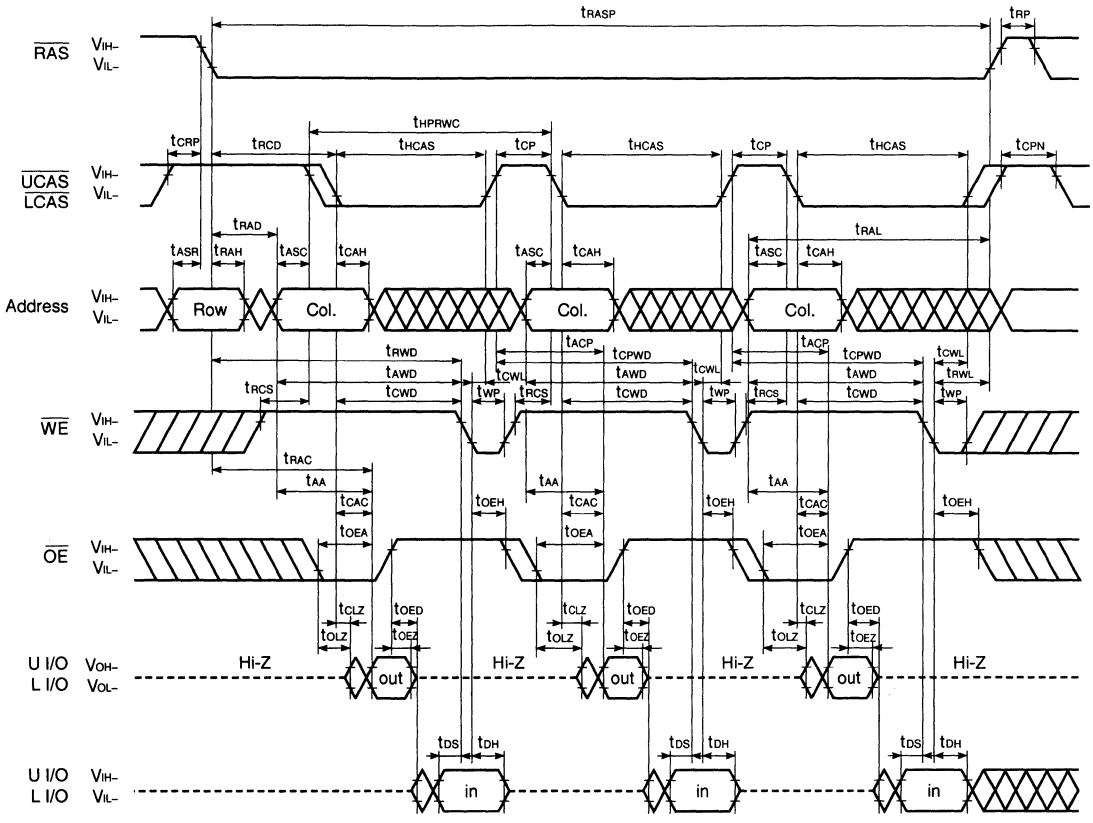
Hyper Page Mode (EDO) Byte Late Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

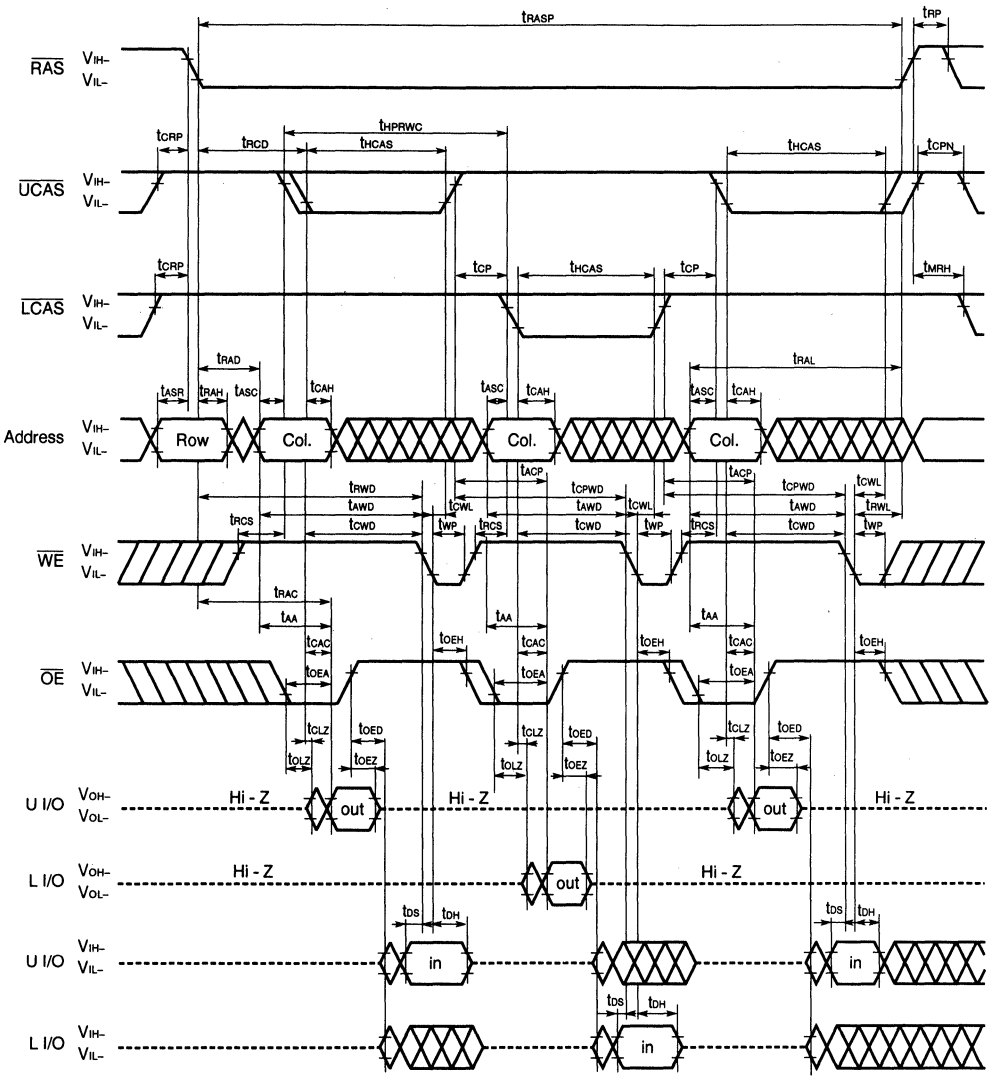
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

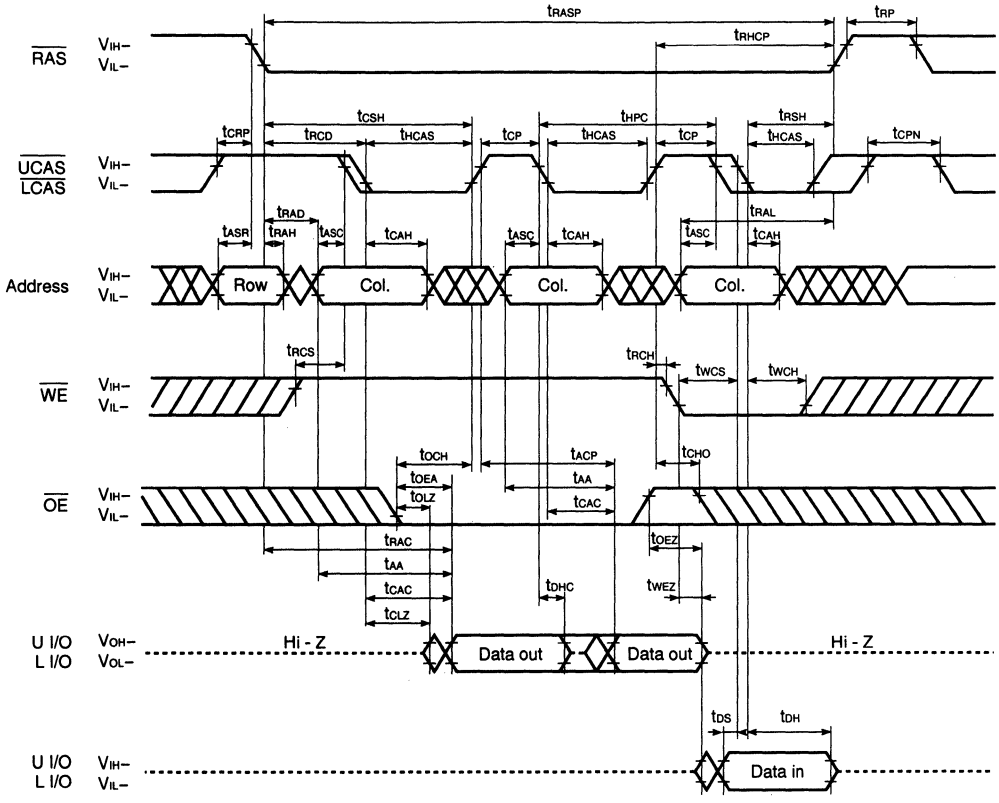
Hyper Page Mode (EDO) Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

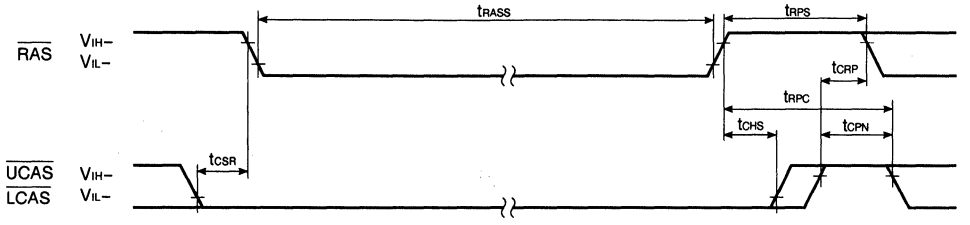
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18165L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

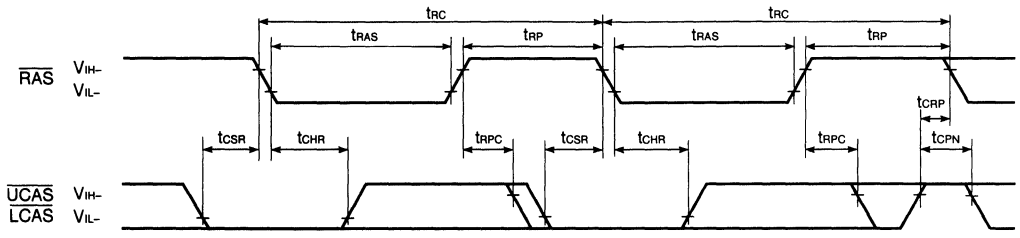
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (1,024/128 ms) should be met.

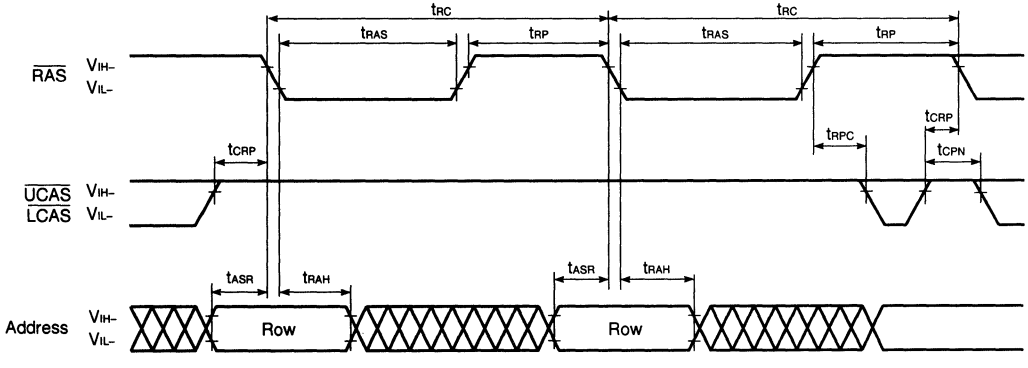
For details, please refer to **How to use DRAM** User's Manual.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



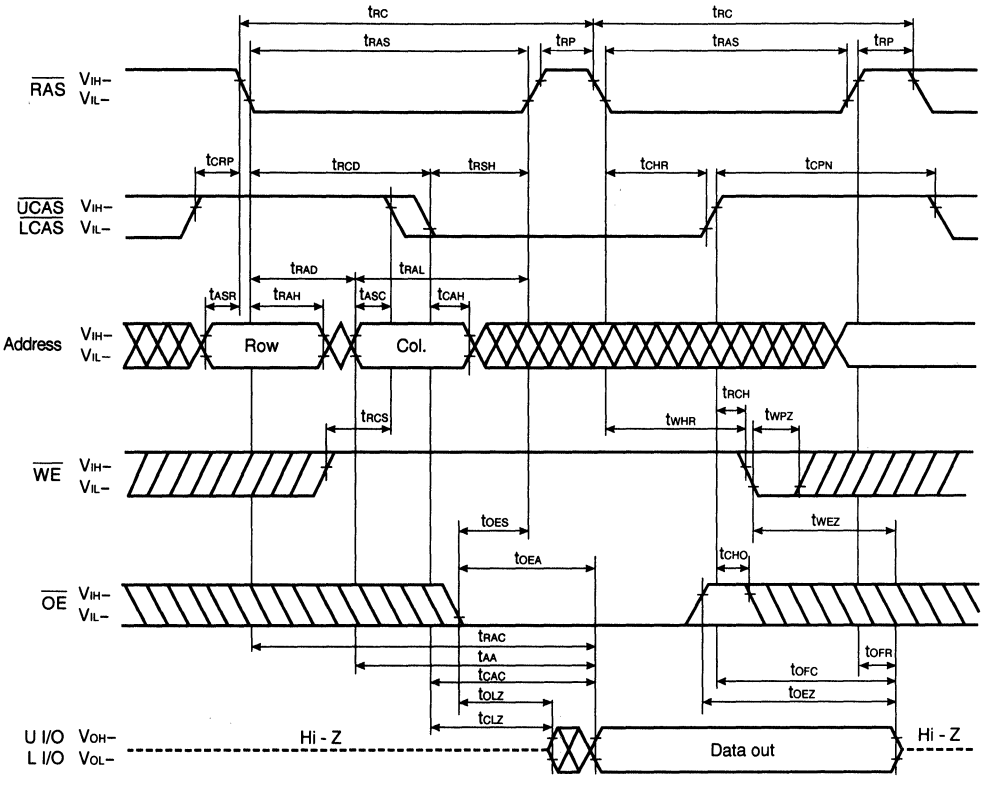
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

$\overline{\text{RAS}}$ Only Refresh Cycle

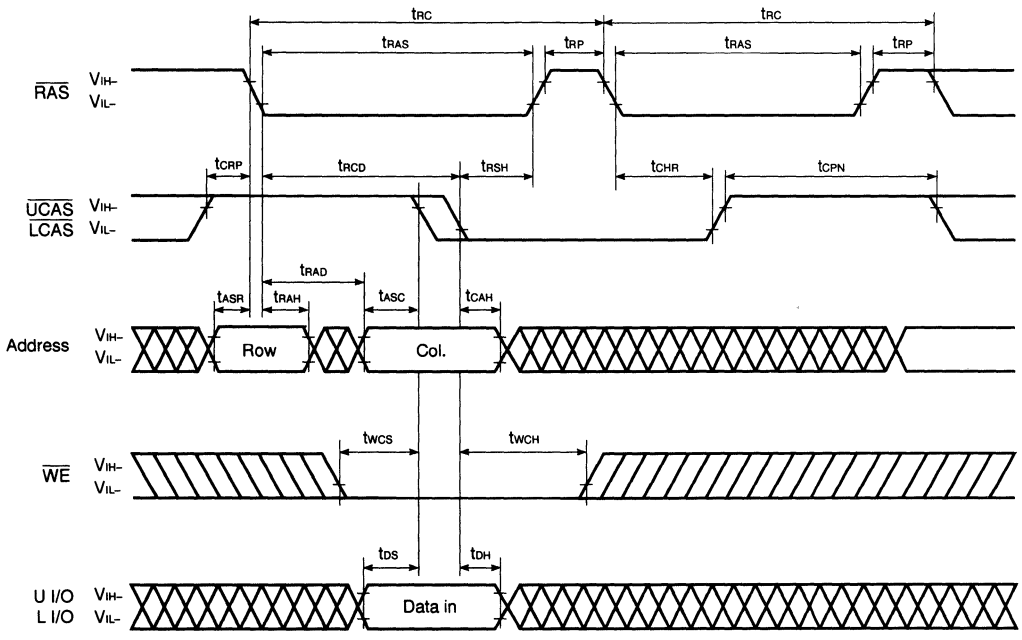


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



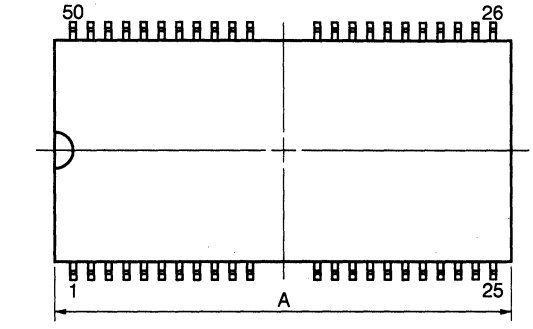
Hidden Refresh Cycle (Write)



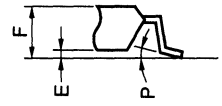
Remark $\overline{OE}$: Don't care

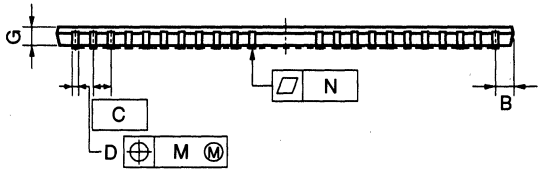
Package Drawings

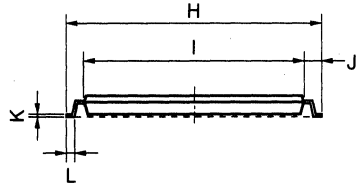
50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







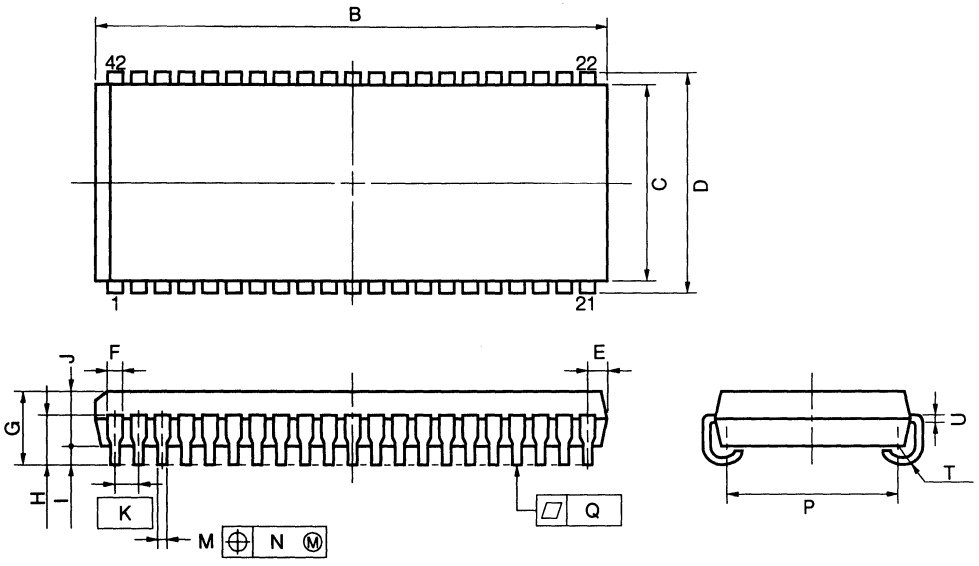
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S18165L, 4218165L.

Types of Surface Mount Device

μPD42S18165LG5, 4218165LG5: 50-pin plastic TSOP (II) (400 mil)
μPD42S18165LLE, 4218165LLE: 42-pin plastic SOJ (400 mil)

Hyper Page Mode (EDO)
4M Dynamic RAM
[5.0V ± 10%]
[5.0V ± 5%]

NEC

MOS INTEGRATED CIRCUIT

μPD42S4210, 424210

4 M-BIT DYNAMIC RAM
256K-WORD BY 16-BIT, HYPER PAGE MODE (EDO),
BYTE READ/WRITE MODE

Description

The μPD42S4210, 424210 are 262,144 words by 16 bits CMOS dynamic RAMs with optional hyper page mode (EDO).

Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S4210 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S4210, 424210 are packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 262,144 words by 16 bits organization
- Single power supply
  +5.0 V ± 10 %: μPD42S4210-60-A, 424210-60-A, 42S4210-70, 424210-70
  +5.0 V ± 5 % : μPD42S4210-60-G, 424210-60-G

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
μPD42S4210-60-A, 424210-60-A	880 mW	60 ns	104 ns	25 ns
μPD42S4210-60-G, 424210-60-G	840 mW	60 ns	104 ns	25 ns
μPD42S4210-70, 424210-70	825 mW	70 ns	124 ns	30 ns

- The μPD42S4210 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

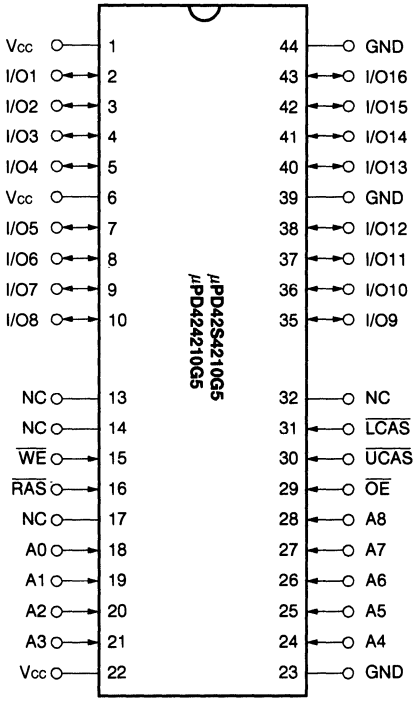
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4210-60-A μPD42S4210-70	512 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.825 mW (CMOS level input)
μPD42S4210-60-G	512 cycles/128 ms		0.7875 mW (CMOS level input)
μPD424210-60-A μPD424210-70	512 cycles/8 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μPD424210-60-G	512 cycles/8 ms		5.25 mW (CMOS level input)

Ordering Information

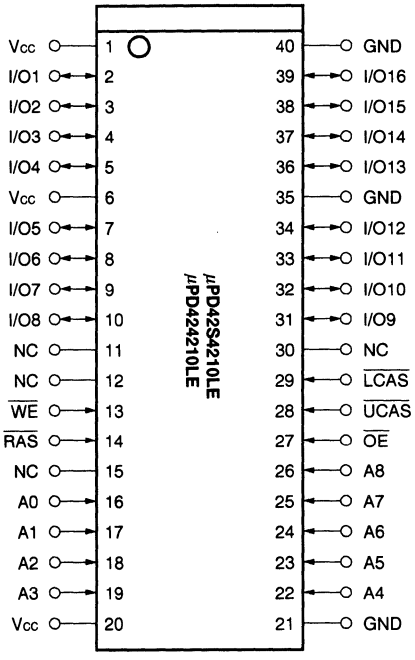
Part number	Access time (MAX.)	Package	Refresh
μPD42S4210G5-60-A	60	44-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S4210G5-60-G	60		
μPD42S4210G5-70	70		
μPD42S4210LE-60-A	60	40-pin plastic SOJ (400 mil)	
μPD42S4210LE-60-G	60		
μPD42S4210LE-70	70		
μPD424210G5-60-A	60	44-pin plastic TSOP(II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424210G5-60-G	60		
μPD424210G5-70	70		
μPD424210LE-60-A	60	40-pin plastic SOJ (400 mil)	
μPD424210LE-60-G	60		
μPD424210LE-70	70		

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II) (400 mil)

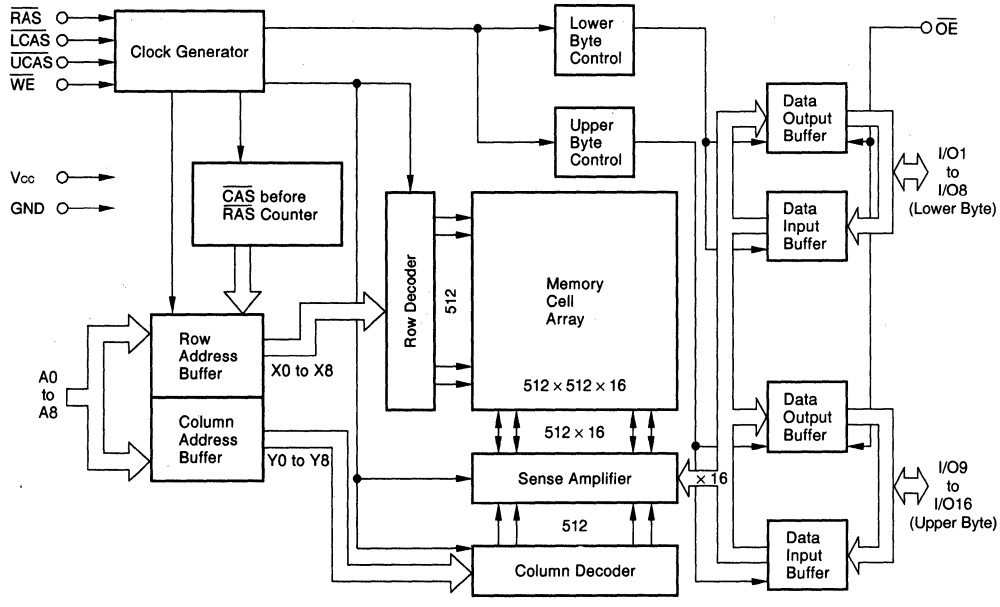


40-pin Plastic SOJ (400 mil)



A0 to A8	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4210, 424210 have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	Address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. Data output time is extended.

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.

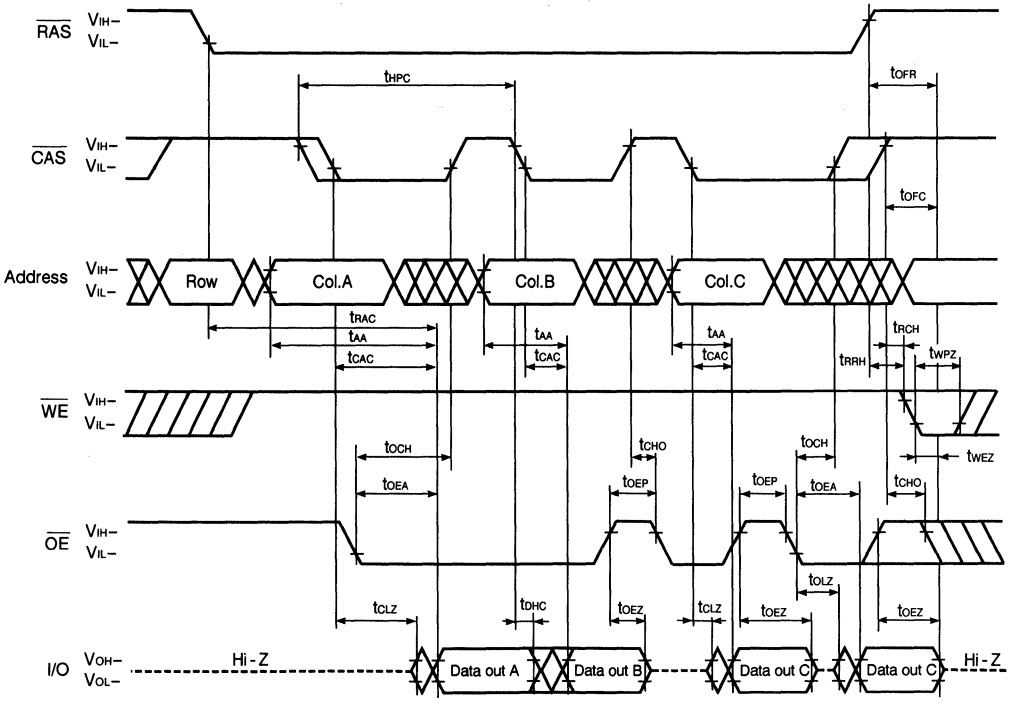
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	μPD42S4210-60-A, 424210-60-A μPD42S4210-70, 424210-70	4.5	5.0	5.5	V
		μPD42S4210-60-G, 424210-60-G	4.75	5.0	5.25	
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		160	mA	1, 2, 3
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		150		
Standby current	μPD42S4210	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.15		
	μPD424210		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$	t_{RAC} = 60 ns		160	mA	1, 2, 3, 4
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		150		
Operating current (Hyper page mode (EDO))		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		160	mA	1, 2, 5
			$t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		150		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		160	mA	1, 2
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		150		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 cycles / 128 ms, only for the μPD42S4210)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 250.0 μs; $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$, 0 V ≤ $V_{IL} \leq$ 0.2 V	$t_{RAS} \leq$ 200 ns		200	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V; Address: V_{IH} or V_{IL}; $\overline{WE}$, $\overline{OE}$: V_{IH}; I_O = 0 mA	$t_{RAS} \leq$ 1 μs		300	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S4210)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms; V_{CC} – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$, 0 V ≤ $V_{IL} \leq$ 0.2 V; I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V	μPD42S4210-60-A, 424210-60-A, μPD42S4210-70, 424210-70	–10	+10	μA	
			V_I = 0 to 5.25 V	μPD42S4210-60-G, 424210-60-G				
			All other pins not under test = 0 V					
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V	μPD42S4210-60-A, 424210-60-A, μPD42S4210-70, 424210-70	–10	+10	μA	
			V_O = 0 to 5.25 V	μPD42S4210-60-G, 424210-60-G				
			Output in disabled (Hi-Z)					
High level output voltage		V_{OH}	I_O = –5.0 mA	μPD42S4210-60-A, 424210-60-A, μPD42S4210-70, 424210-70	2.4		V	
			I_O = –0.1 mA	μPD42S4210-60-G, 424210-60-G				
Low level output voltage		V_{OL}	I_O = +4.2 mA	μPD42S4210-60-A, 424210-60-A, μPD42S4210-70, 424210-70		0.4	V	
			I_O = +0.1 mA	μPD42S4210-60-G, 424210-60-G				

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\,(MAX.)}$ and $\overline{CAS} \geq V_{IH\,(MIN.)}$.

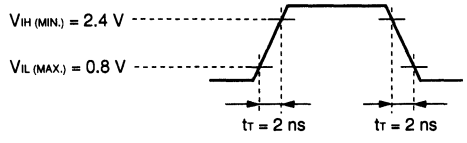
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

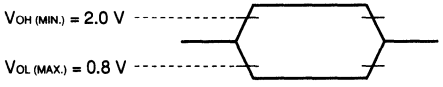
AC Characteristics Test Conditions

(1) Input timing specification

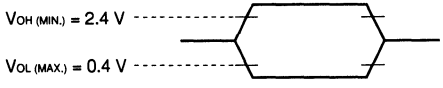


(2) Output timing specification

- μPD42S4210-60-A, 424210-60-A

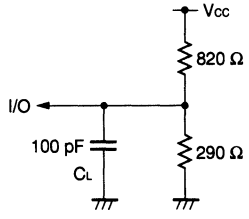


- μPD42S4210-60-G, 424210-60-G
- μPD424210-70, 424210-70

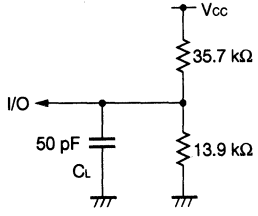


(3) Output loading conditions

- μPD42S4210-60-A, 424210-60-A
- μPD42S4210-70, 424210-70



- μPD42S4210-60-G, 424210-60-G



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t_{RC}	104	–	124	–	ns	
$\overline{RAS}$ precharge time		t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ precharge time		t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ pulse width		t_{RAS}	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		t_{CAS}	10	10,000	12	10,000	ns	
$\overline{RAS}$ hold time		t_{RSH}	10	–	12	–	ns	
$\overline{CAS}$ hold time		t_{CSH}	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_{RCD}	14	45	14	50	ns	2
$\overline{RAS}$ to column address delay time		t_{RAD}	12	30	12	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		t_{CRP}	5	–	5	–	ns	3
Row address setup time		t_{ASR}	0	–	0	–	ns	
Row address hold time		t_{RAH}	10	–	10	–	ns	
Column address setup time		t_{ASC}	0	–	0	–	ns	
Column address hold time		t_{CAH}	10	–	12	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to data setup time		t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to data delay time		t_{OED}	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		t_{MRH}	0	–	0	–	ns	
Transition time (rise and fall)		t_T	1	50	1	50	ns	
Refresh time	μPD42S4210	t_{REF}	–	128	–	128	ms	4
	μPD424210		–	8	–	8	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs ≤ t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S4210.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	10	–	12	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX		
Read modify write cycle time	t_{RWC}	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	–	37	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX		
Read / Write cycle time	t_{HPC}	25	–	30	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	52	–	59	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{HPRWC}	66	–	75	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	13	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	13	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	13	0	15	ns	3,4

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

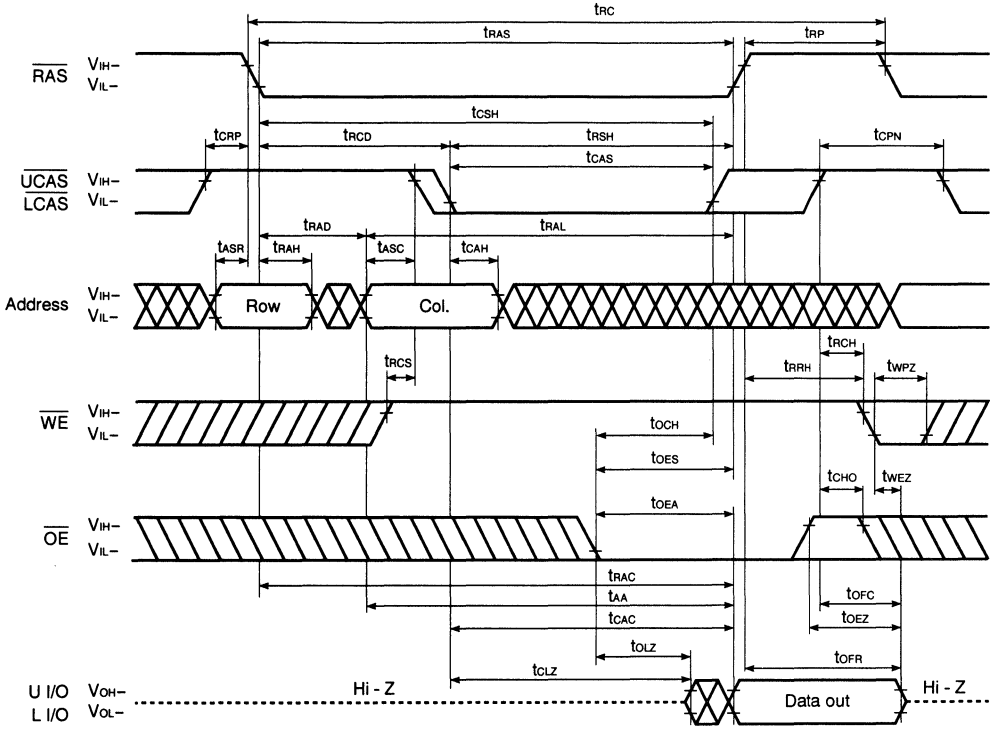
(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Refresh Cycle

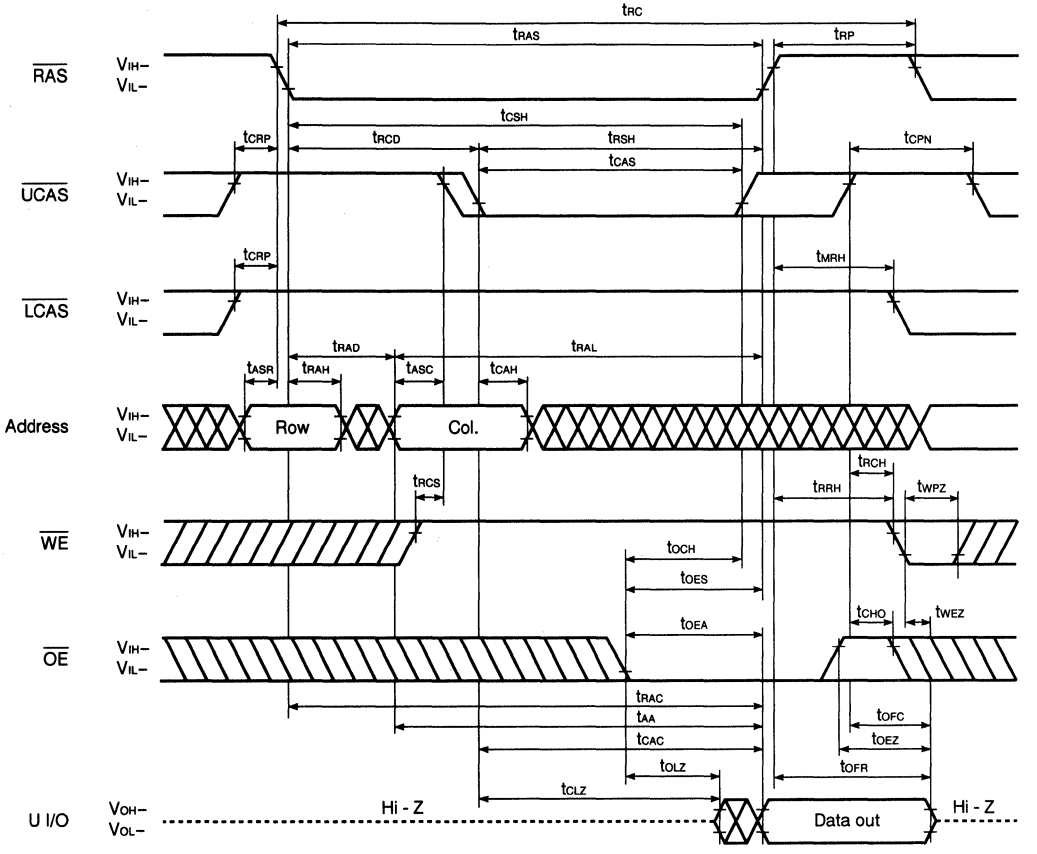
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S4210.

Read Cycle

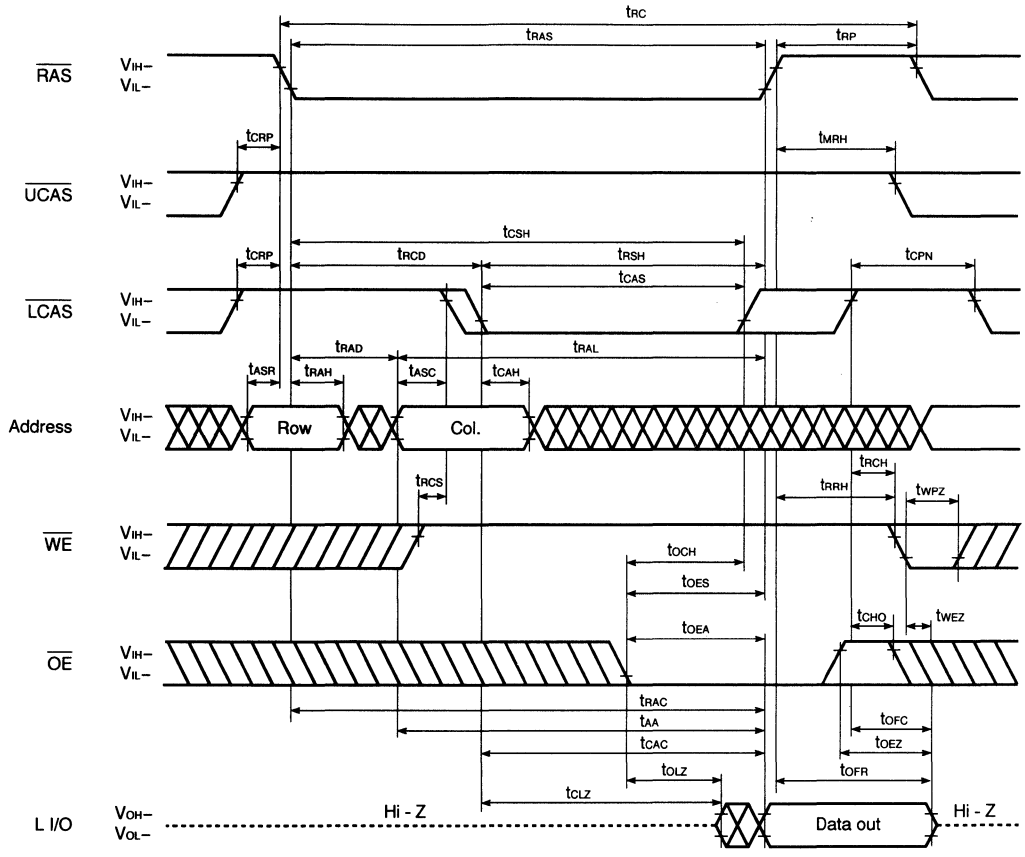

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS VIH– LCAS VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
tOEA
OE VIH– VIL–
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O VOH– L I/O VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



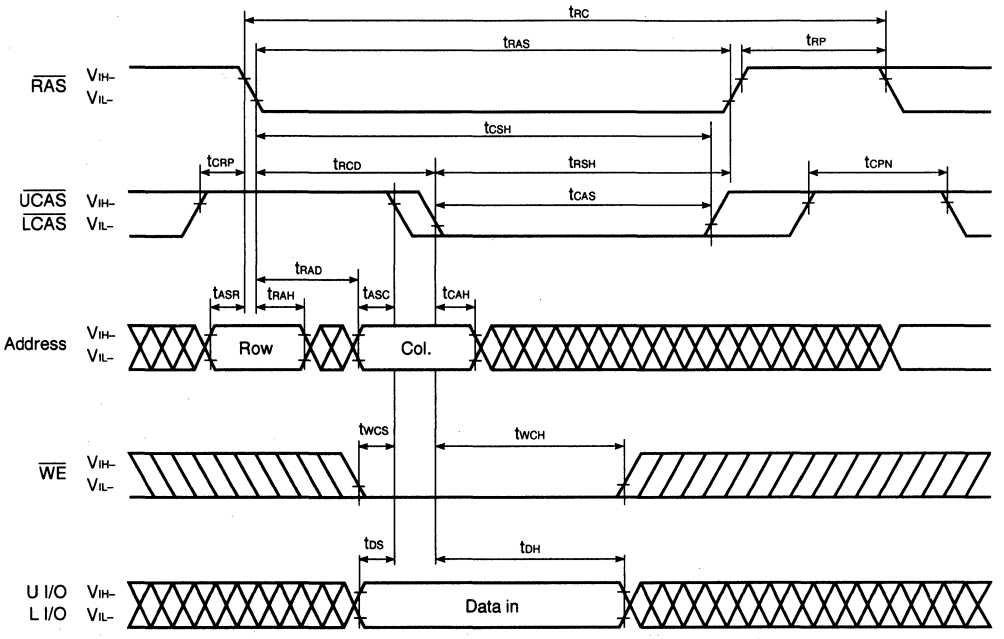
Remark L I/O: Hi-Z

Lower Byte Read Cycle



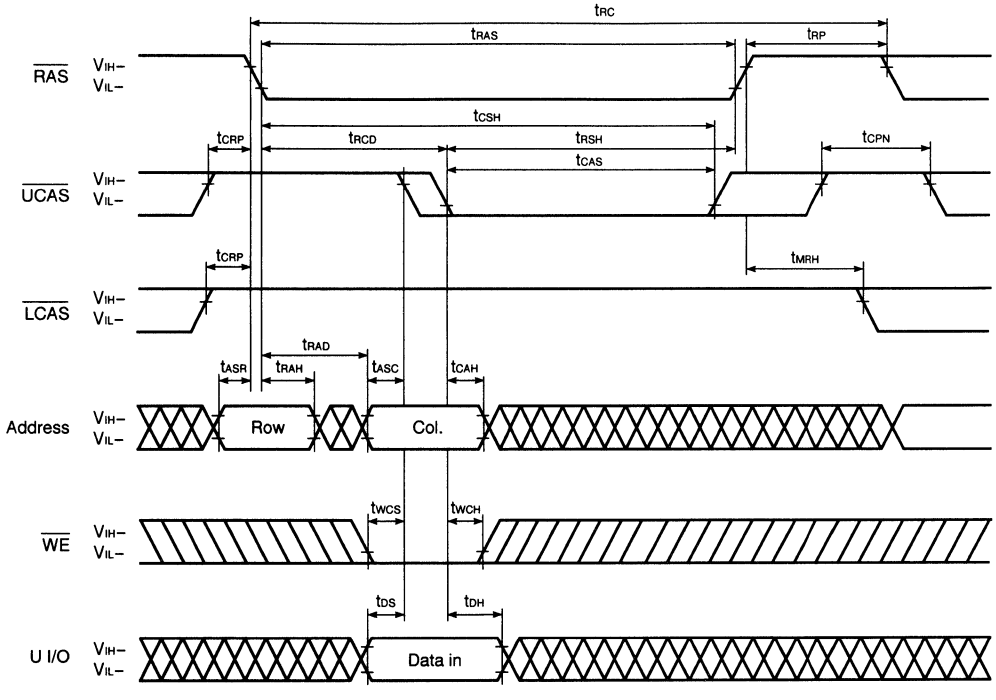
Remark U I/O: Hi-Z

Early Write Cycle



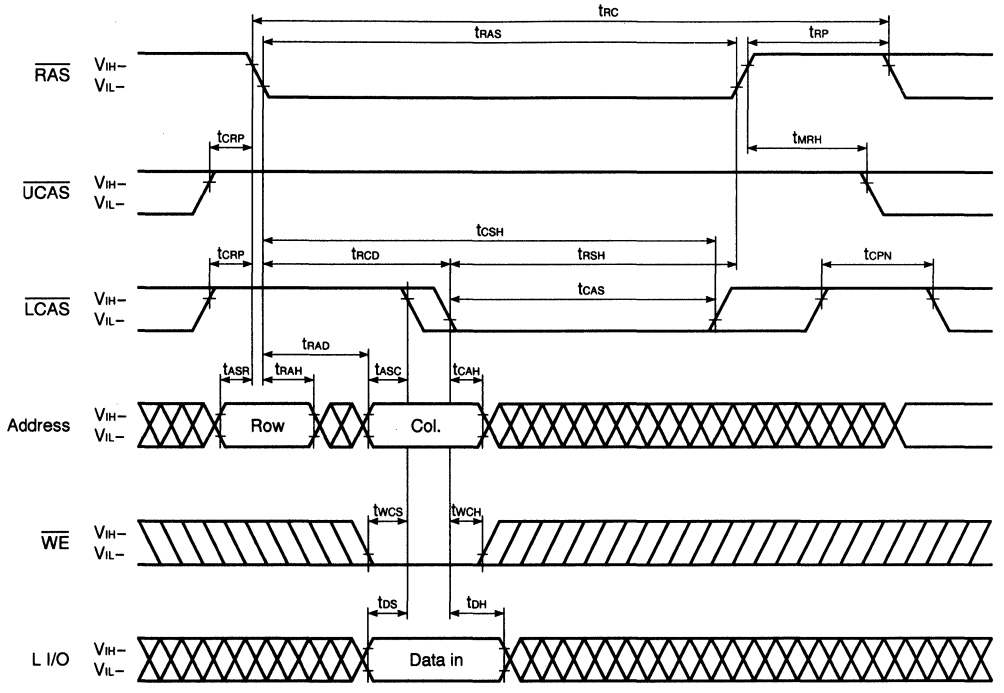
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



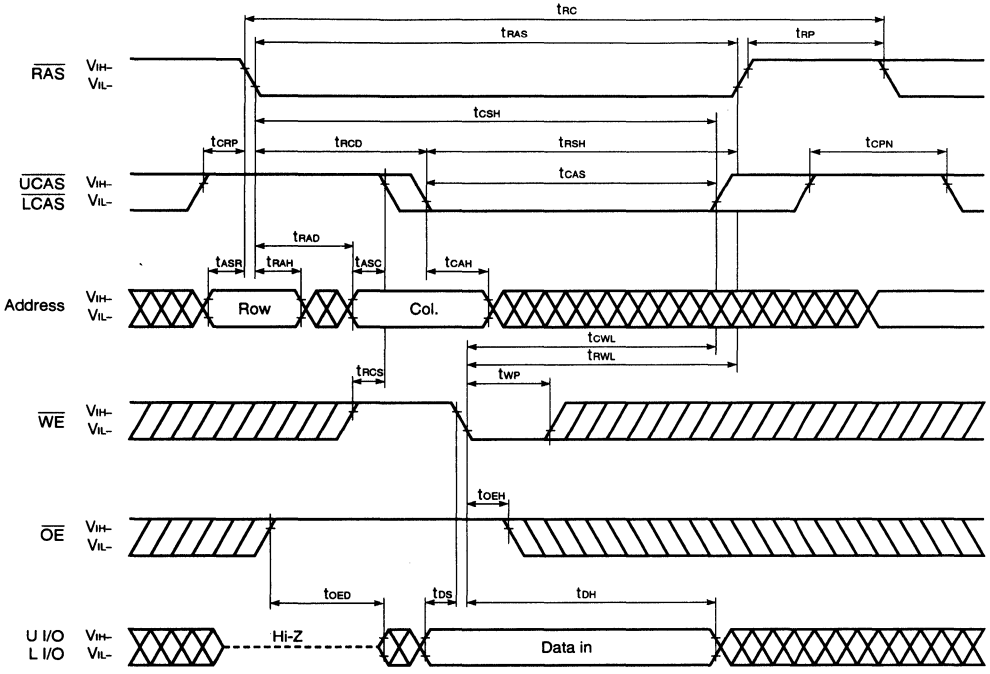
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

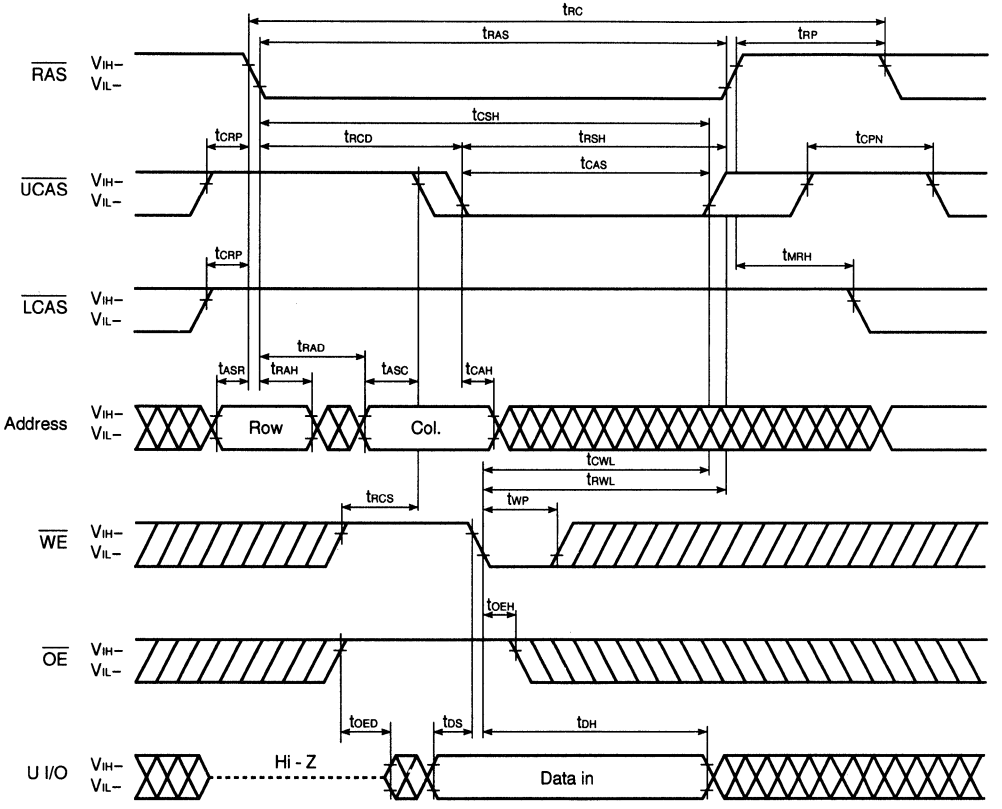


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

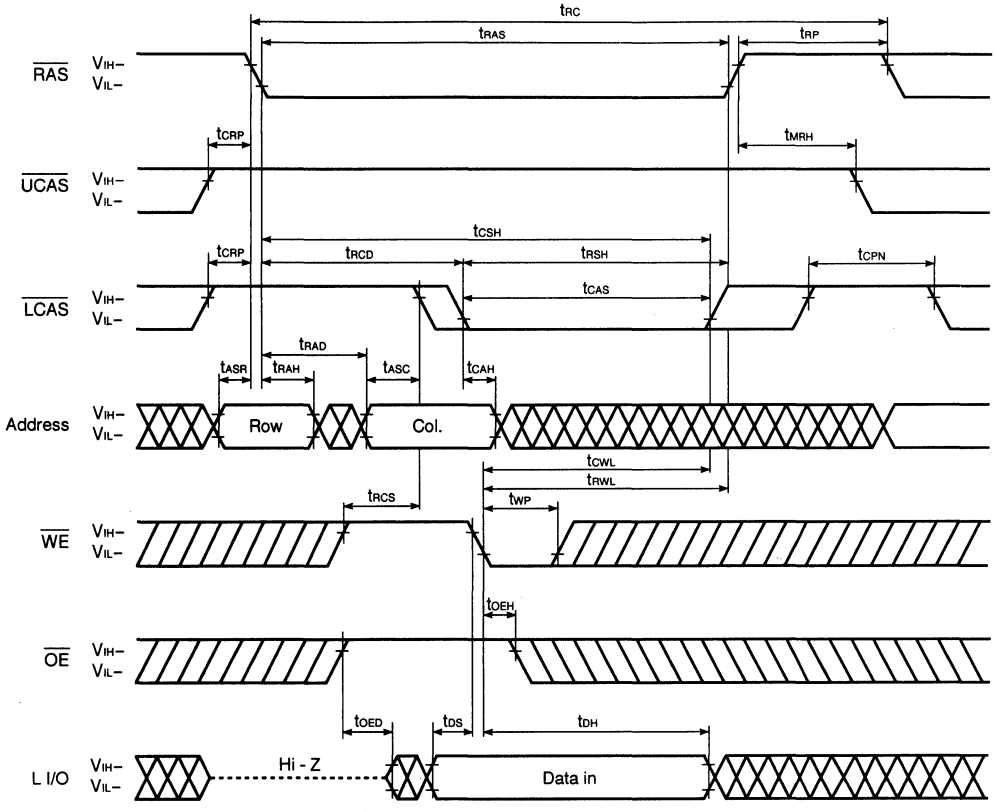


Upper Byte Late Write Cycle



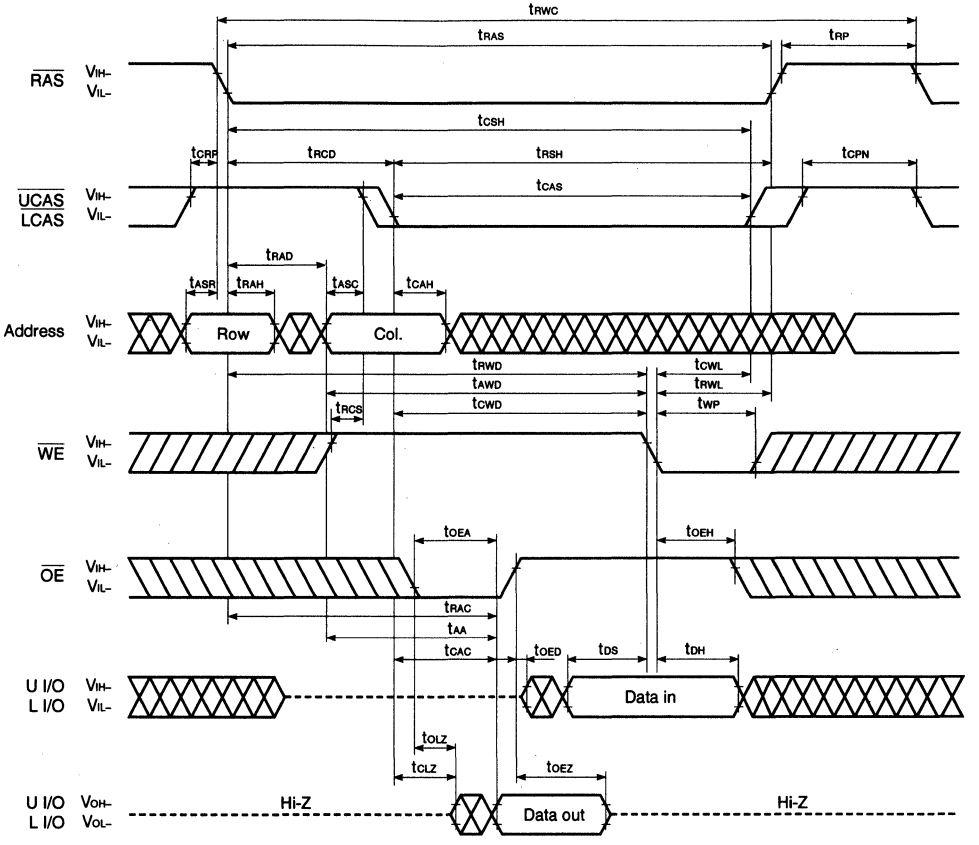
Remark L I/O: Don't care

Lower Byte Late Write Cycle

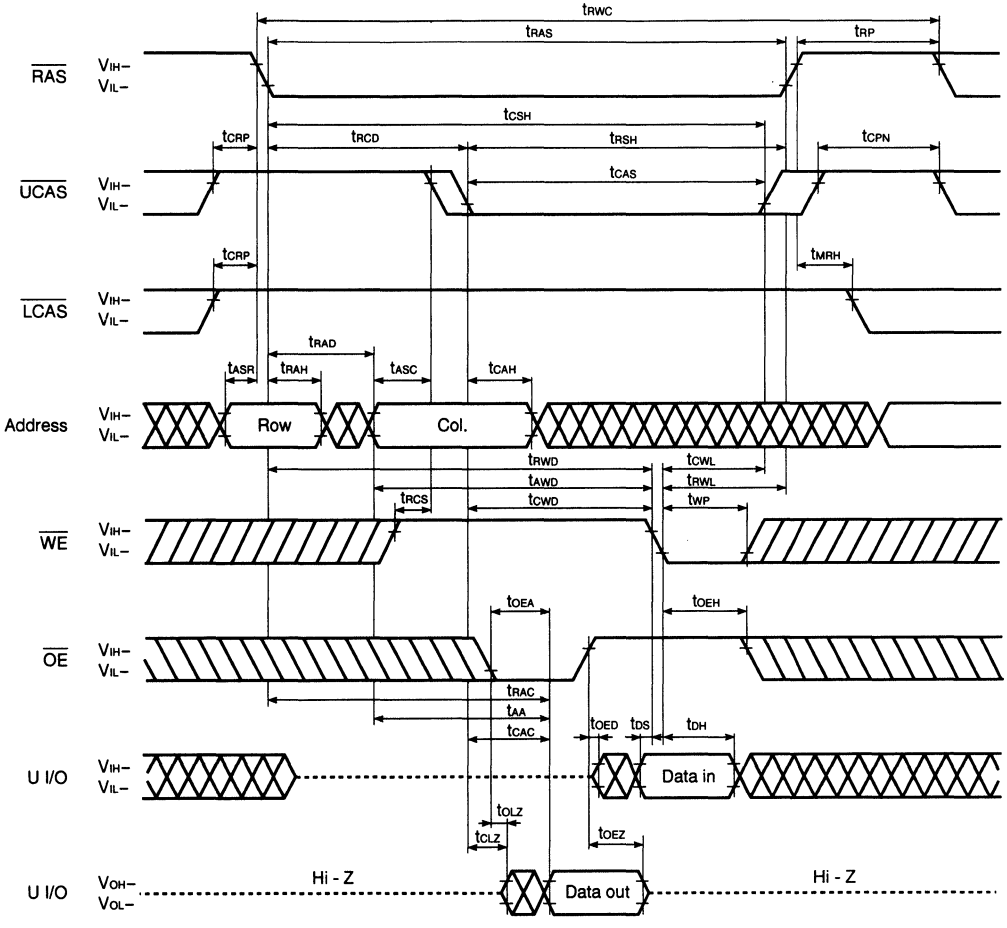


Remark U I/O: Don't care

Read Modify Write Cycle

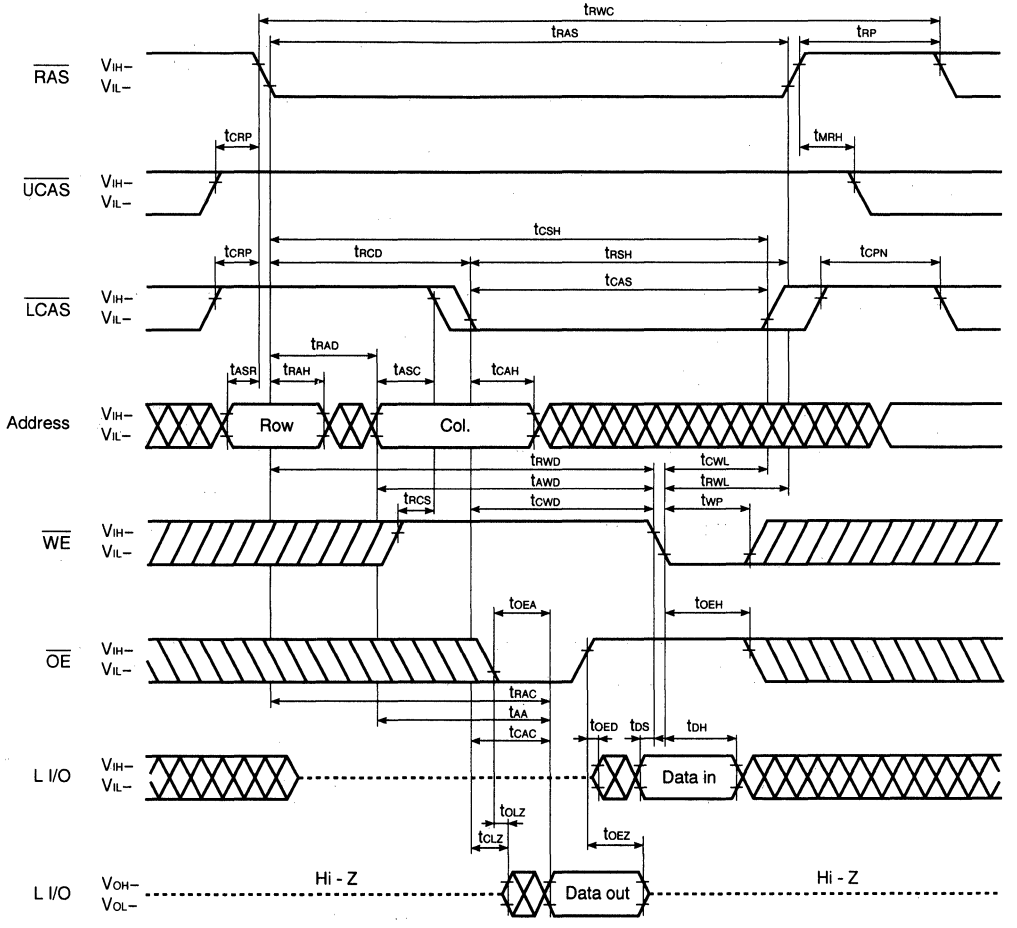


Upper Byte Read Modify Write Cycle



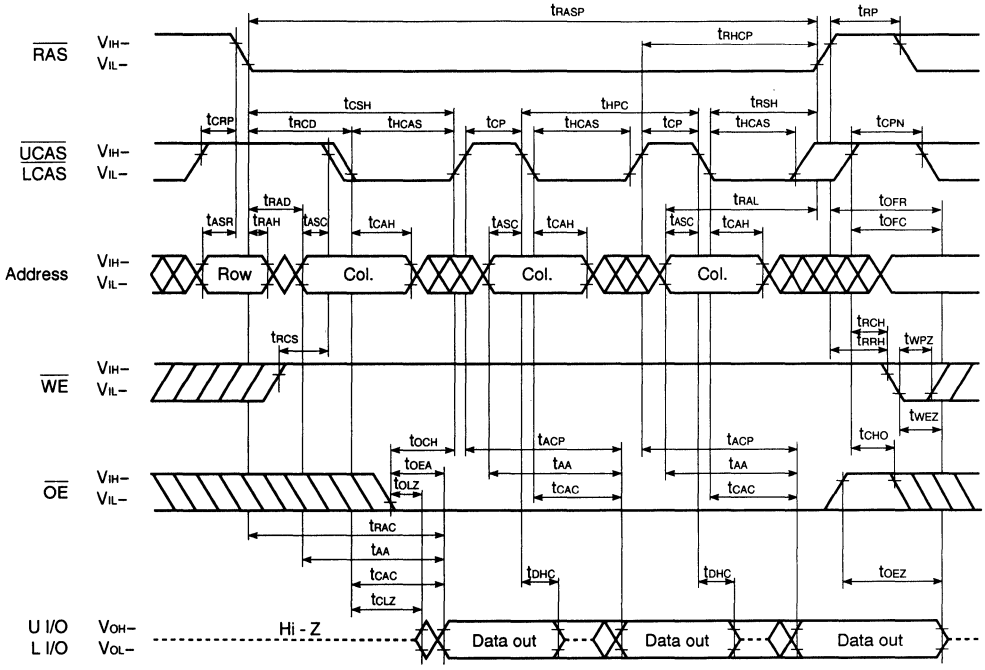
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



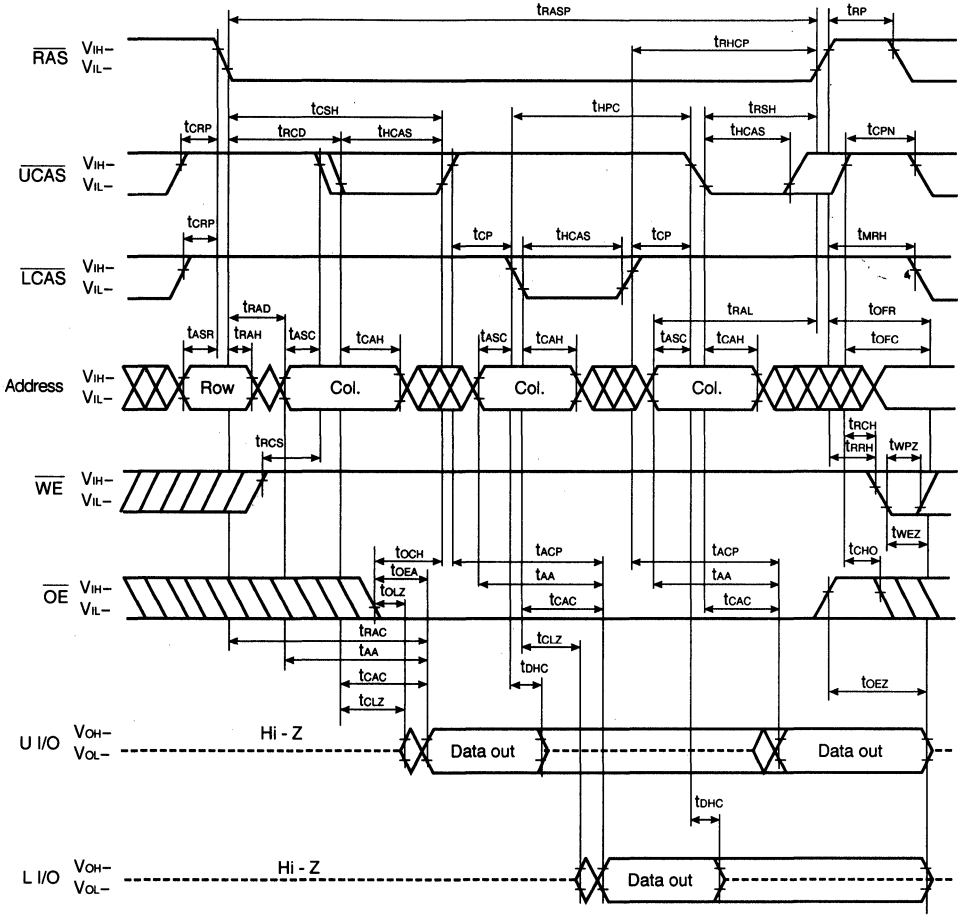
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

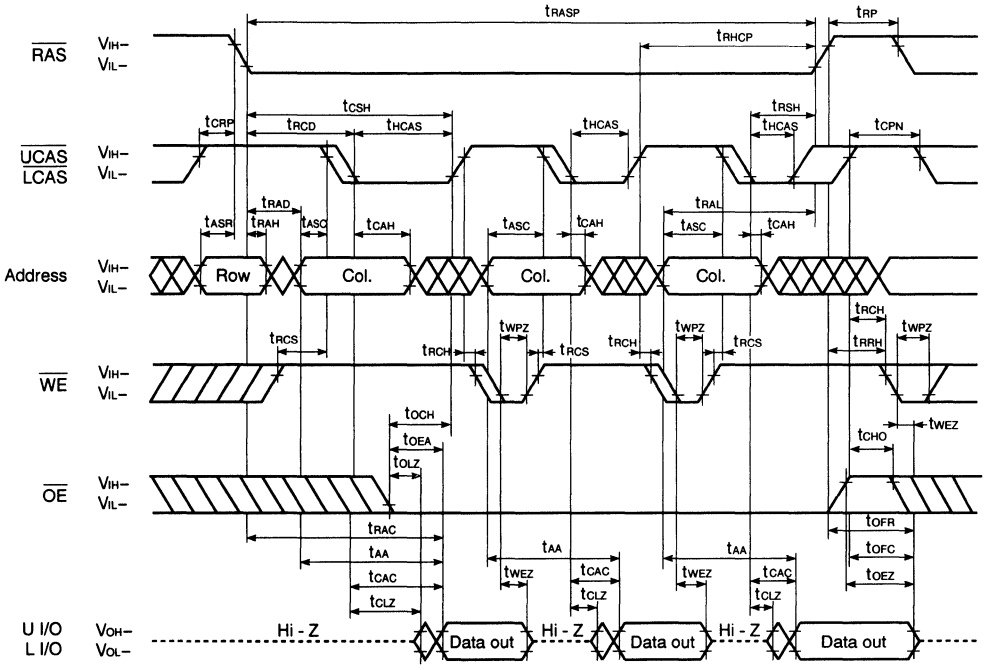
Hyper Page Mode (EDO) Byte Read Cycle



Remark 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

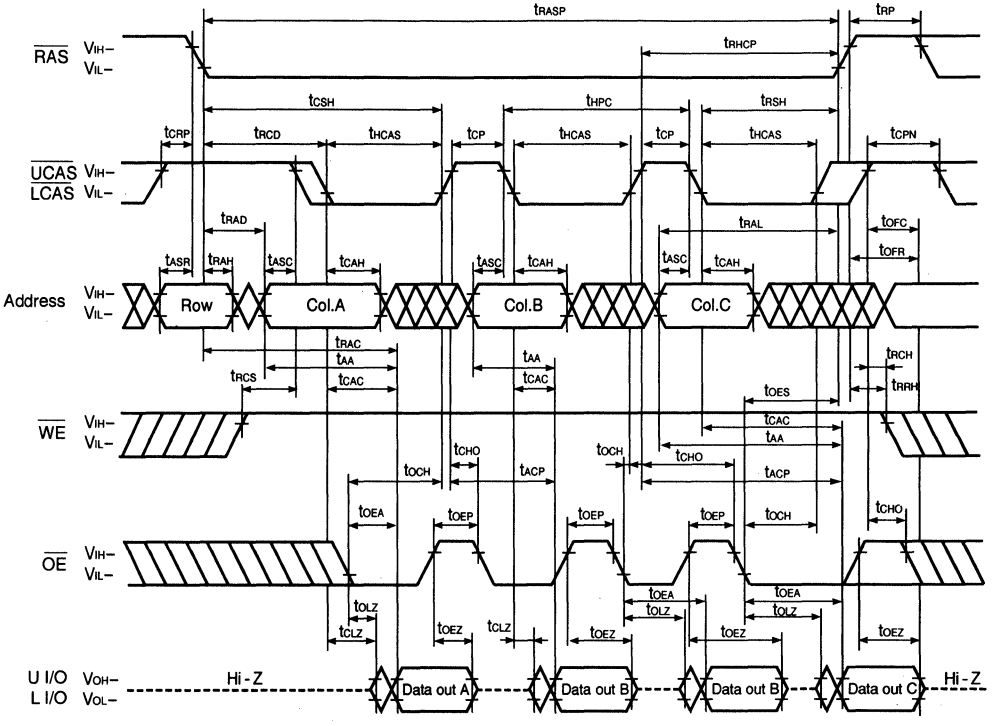
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



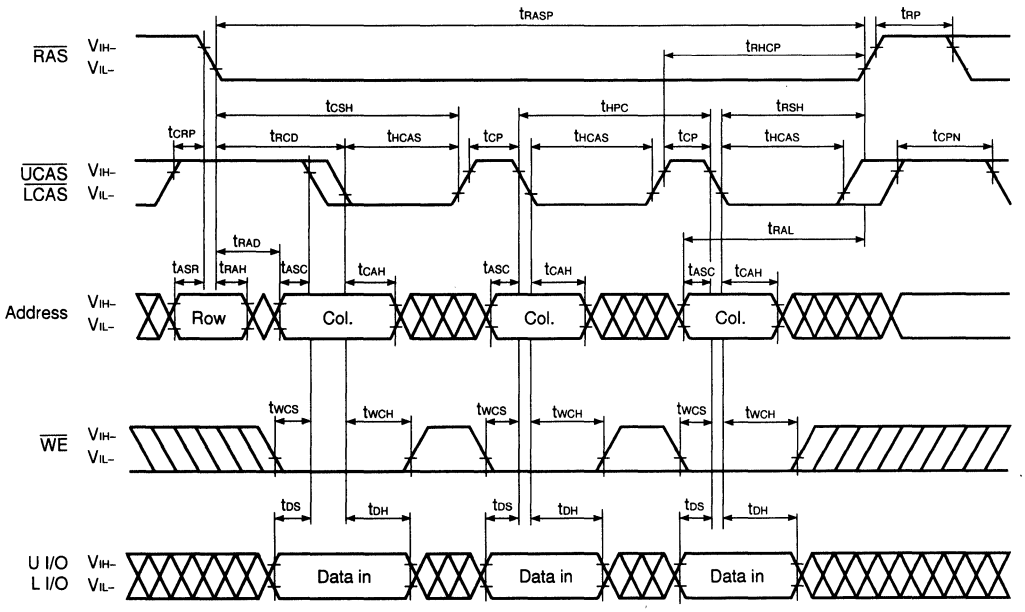
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

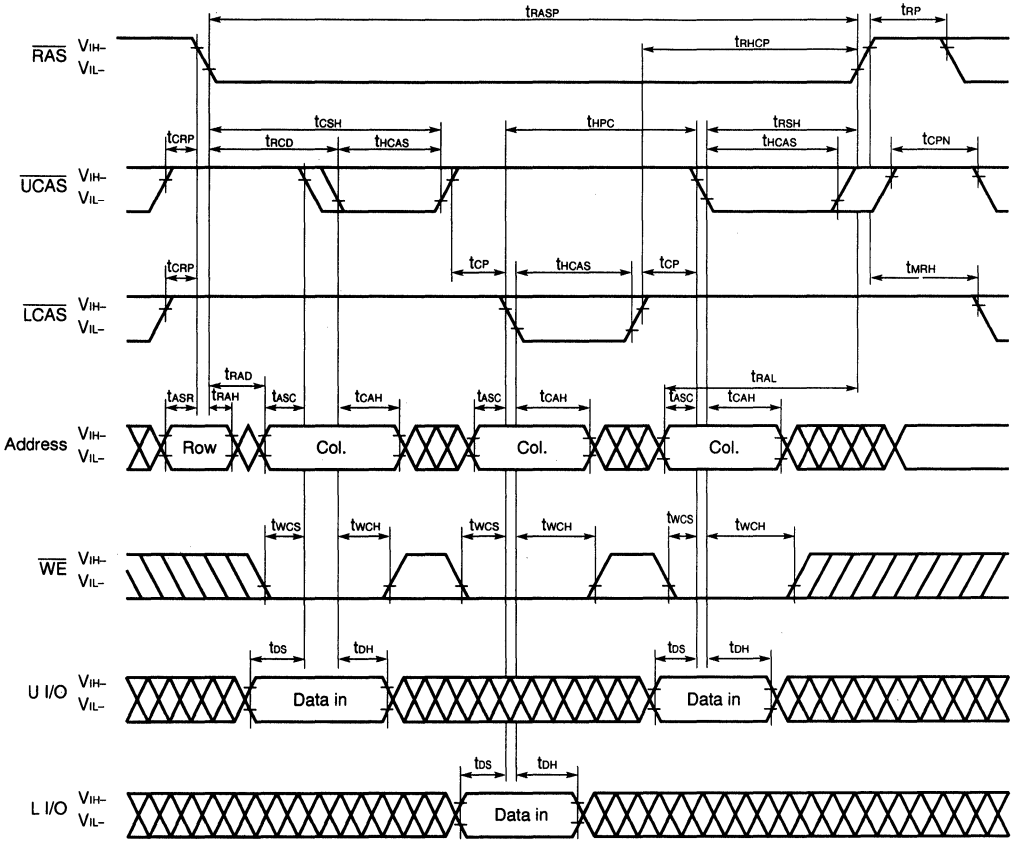
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

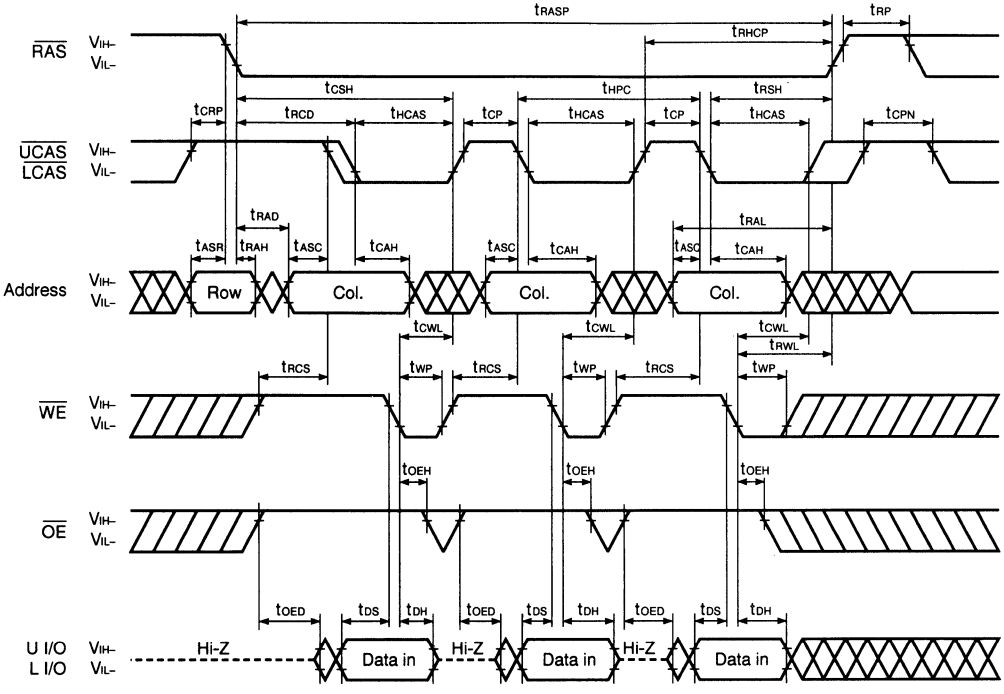
Hyper Page Mode (EDO) Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

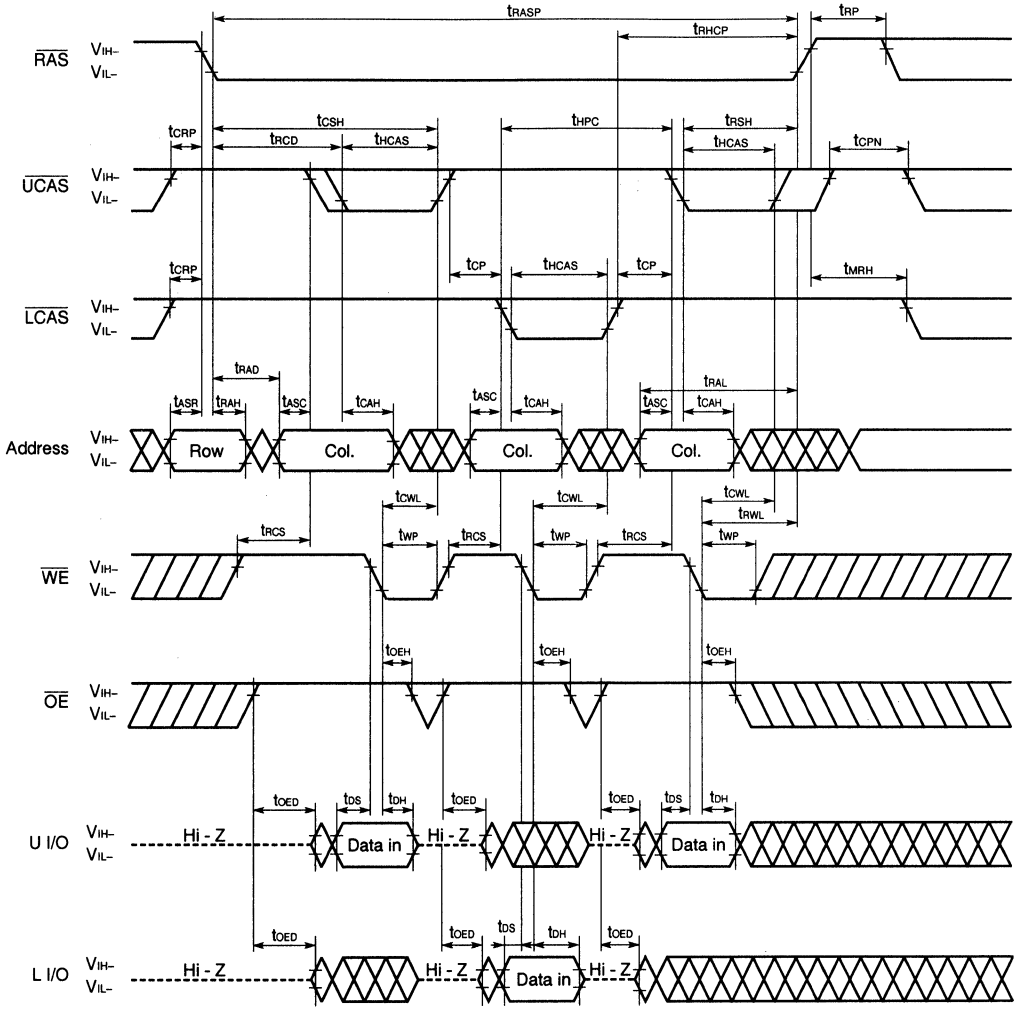
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

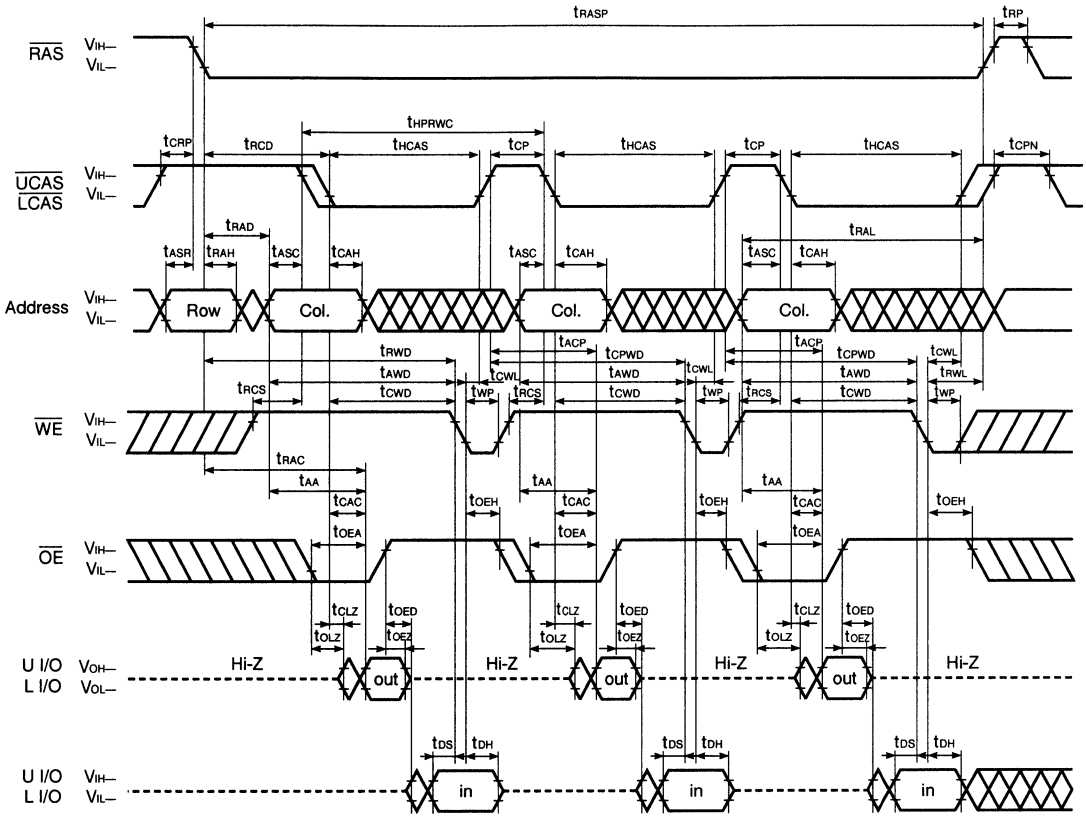
Hyper Page Mode (EDO) Byte Late Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

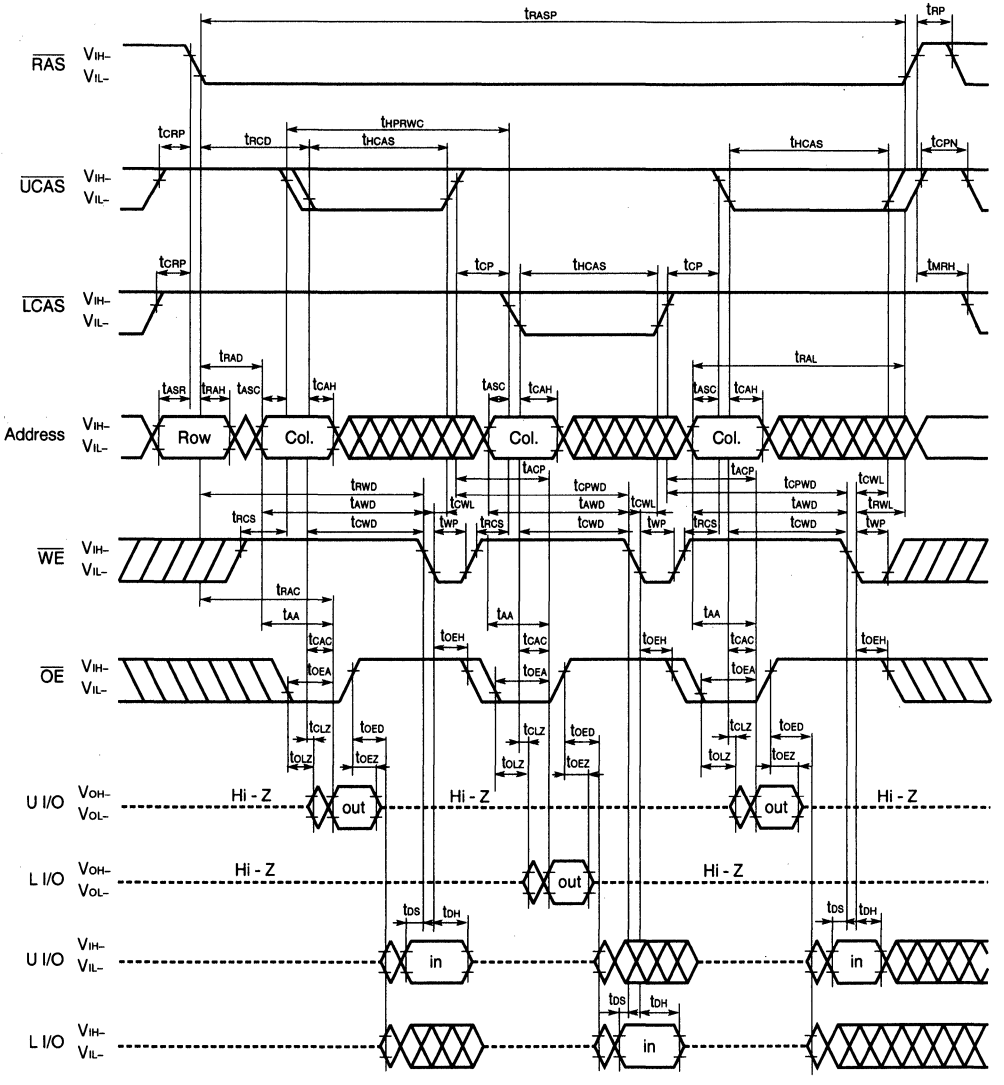
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

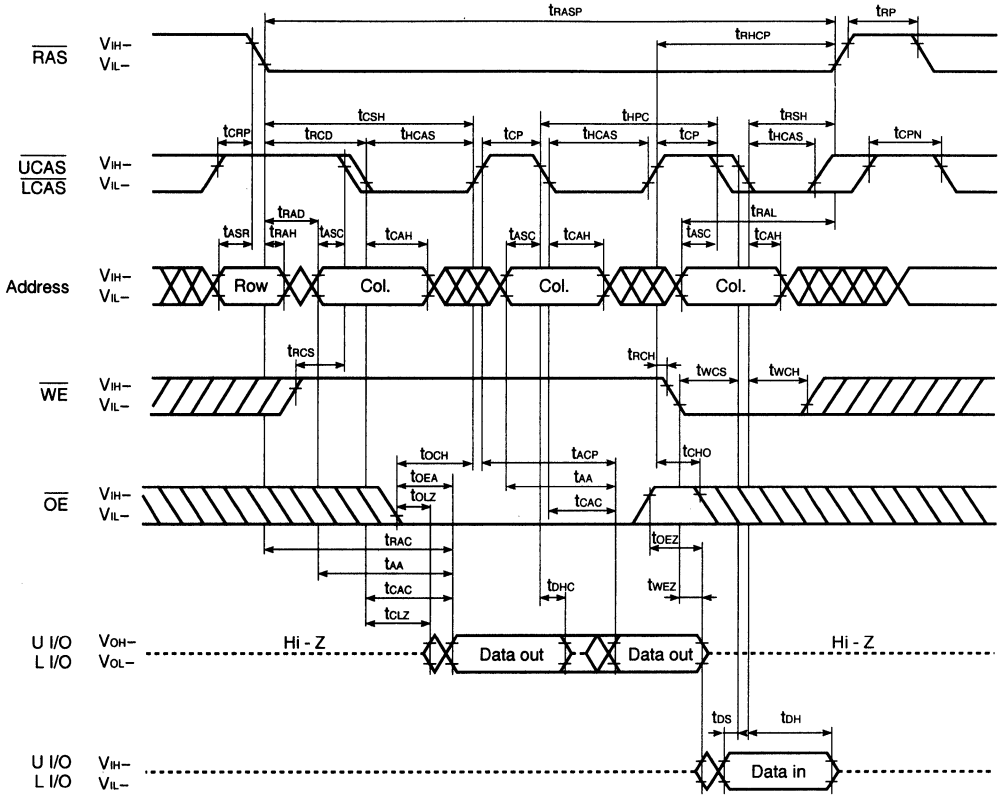
Hyper Page Mode (EDO) Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

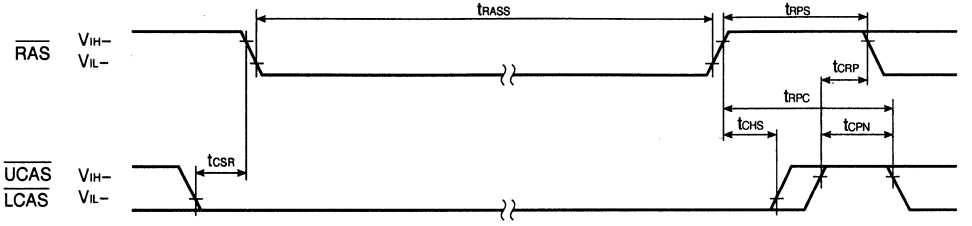
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S4210)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

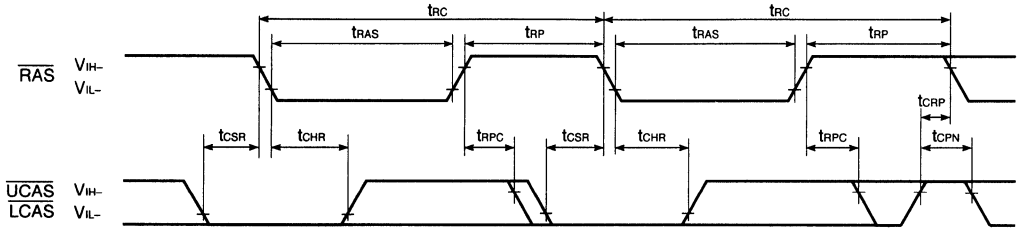
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 512 times within an 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 512 times within an 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100$ μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (512/128 ms) should be met.

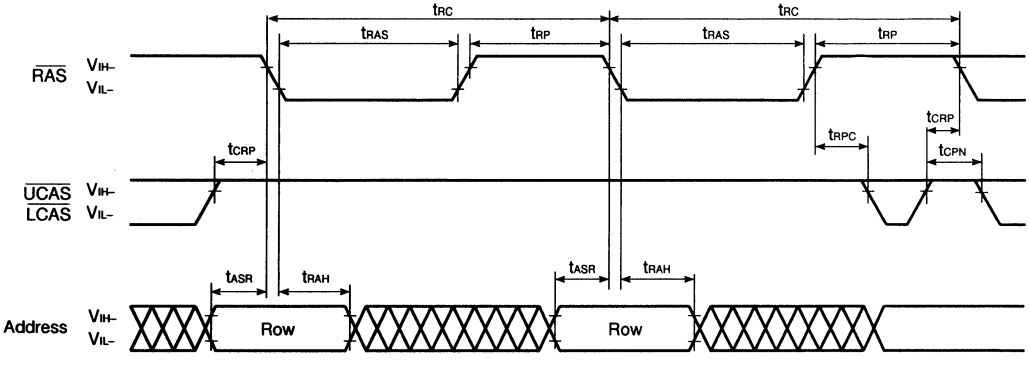
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



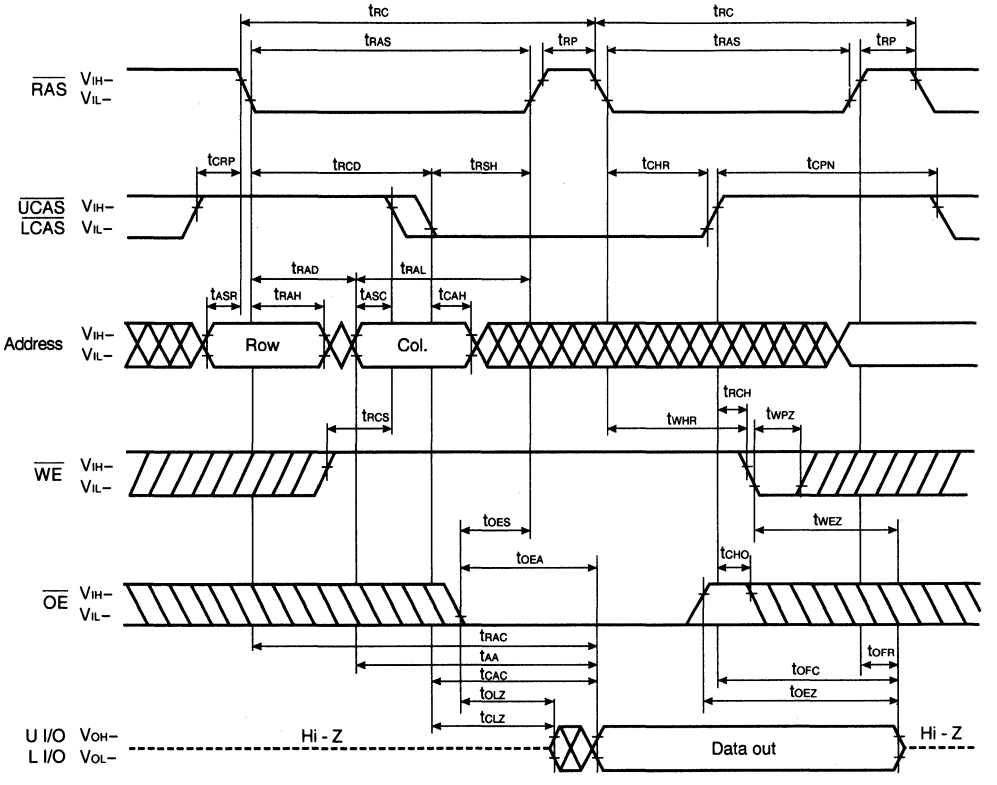
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

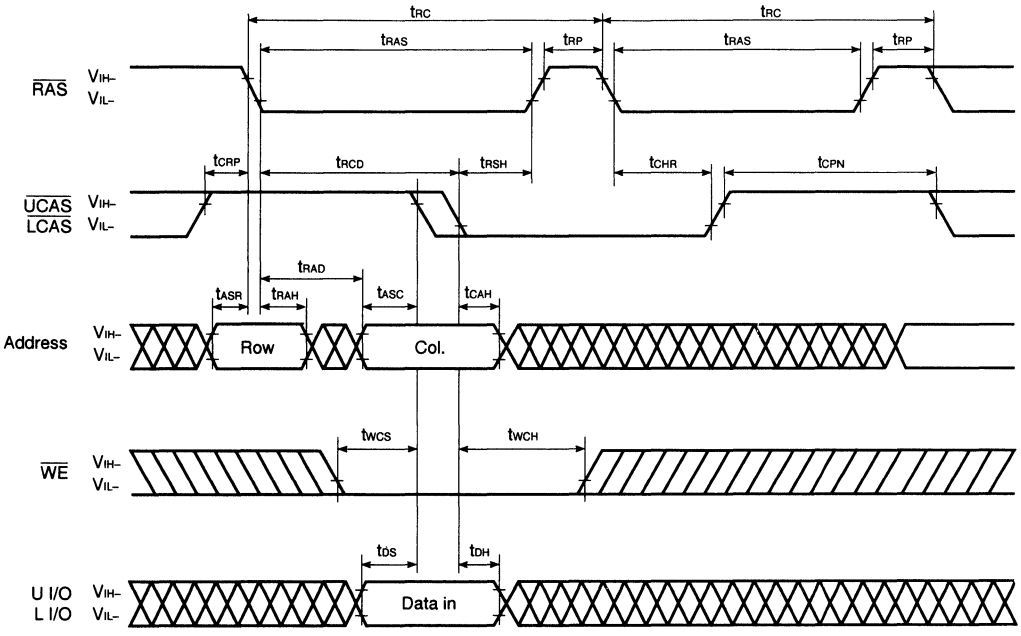


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



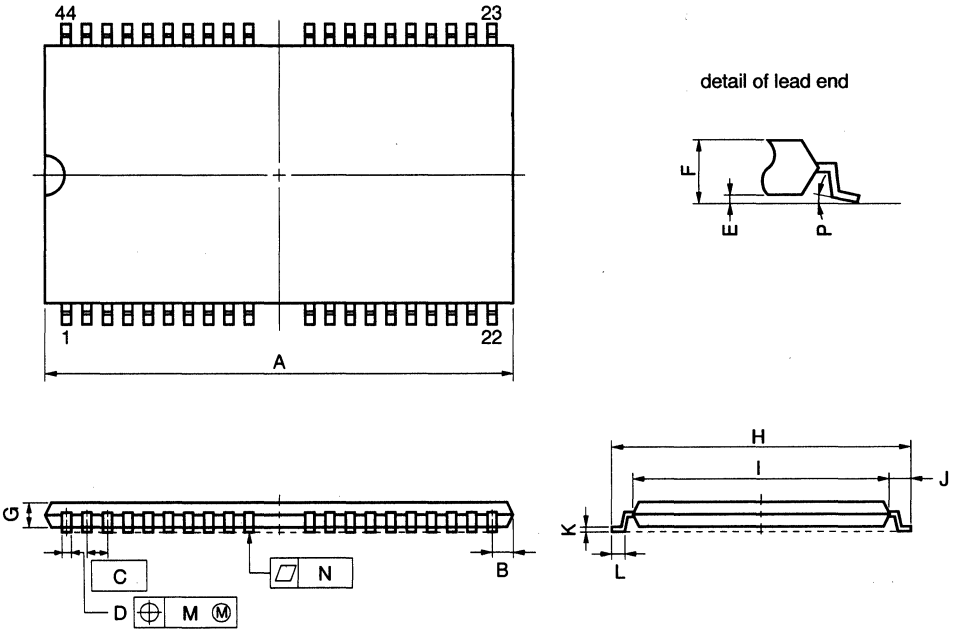
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



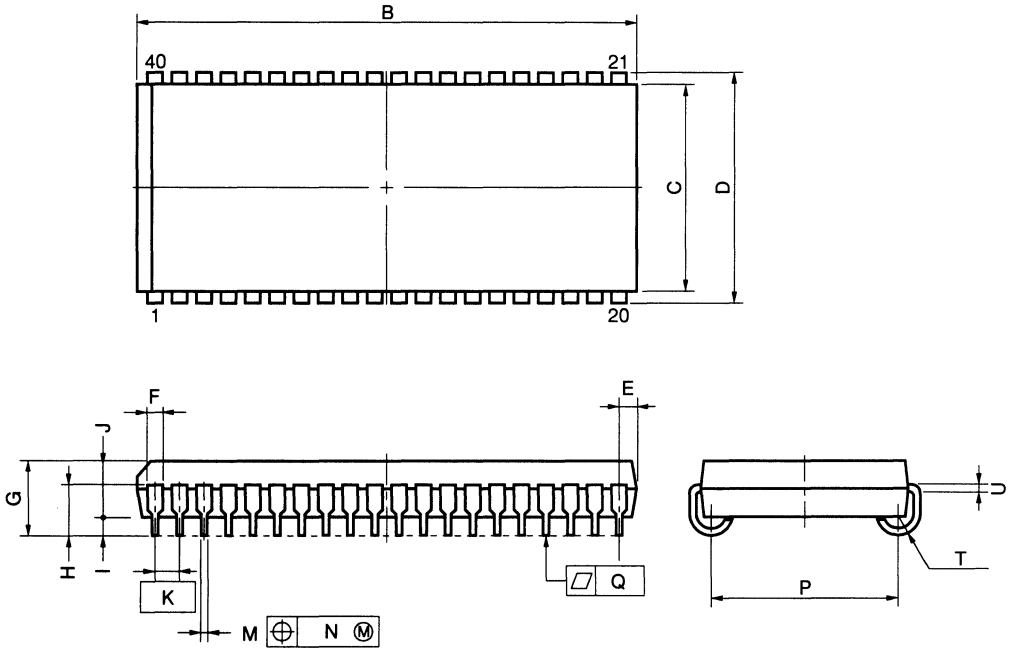
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S44G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P40LE-400A-2

Recommended Soldering Conditions

Types of Surface Mount Device

μPD42S4210G5, 424210G5: 44-pin plastic TSOP (II) (400 mil)
μPD42S4210LE, 424210LE: 40-pin plastic SOJ (400 mil)

Hyper Page Mode (EDO)
1M Dynamic RAM
[5.0V ± 10%]

NEC

MOS INTEGRATED CIRCUIT

μPD421805

1 M-BIT DYNAMIC RAM
128K-WORD BY 8-BIT, HYPER PAGE MODE (EDO)

Description

The μPD421805 is a 131,072 words by 8 bits CMOS dynamic RAM with optional hyper page mode (EDO).
Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.
The μPD421805 is packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 131,072 words by 8 bits organization
- Single +5.0 V ±10 % power supply
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 512 refresh cycles/8 ms

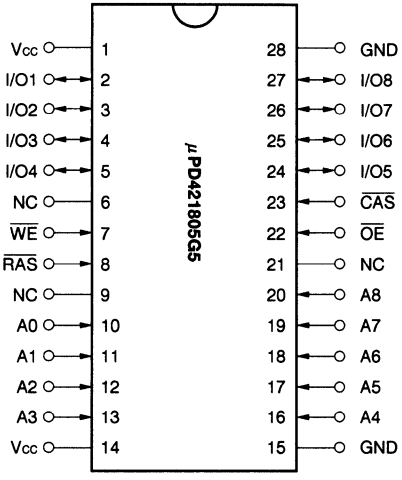
Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
	Active (MAX.)	Standby (MAX.)			
μPD421805-25-A	550 mW	5.5 mW (CMOS level input)	70 ns	124 ns	25 ns
μPD421805-30-A					30 ns
μPD421805-25					25 ns
μPD421805-30					30 ns
μPD421805-35					35 ns

Ordering Information

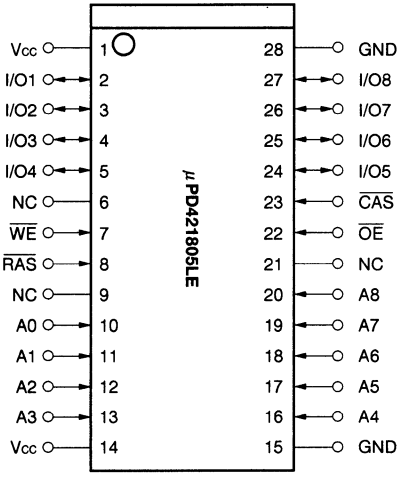
Part number	Access time (MAX.)	Hyper page mode (EDO) cycle time (MIN.)	Package	Refresh
μPD421805G5-25-A	70 ns	25 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD421805G5-30-A	70 ns	30 ns		
μPD421805G5-25	70 ns	25 ns		
μPD421805G5-30	70 ns	30 ns		
μPD421805G5-35	70 ns	35 ns		
μPD421805LE-25-A	70 ns	25 ns	28-pin plastic SOJ (400 mil)	
μPD421805LE-30-A	70 ns	30 ns		
μPD421805LE-25	70 ns	25 ns		
μPD421805LE-30	70 ns	30 ns		
μPD421805LE-35	70 ns	35 ns		

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

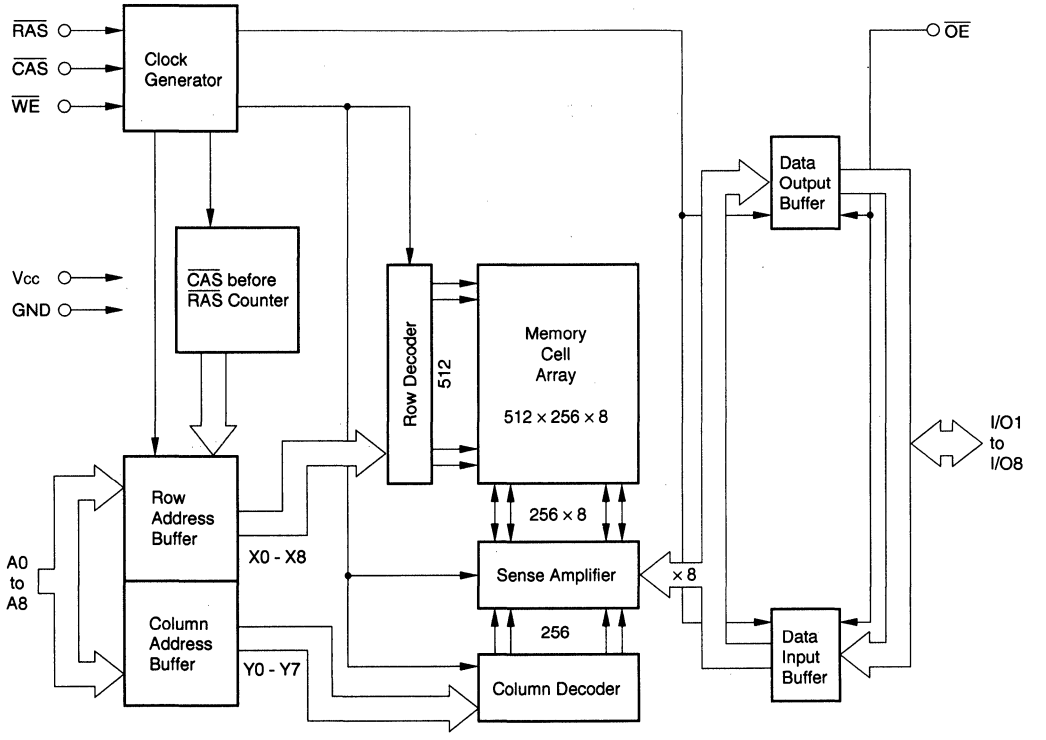


28-pin Plastic SOJ (400 mil)



A0 to A8 : Address Inputs
I/O1 to I/O8: Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Input/Output Pin Functions

The μPD421805 has input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	Address bus. Input total 17-bit of address signal, upper 9-bit and lower 8-bit in sequence (address multiplex method). Therefore, one word is selected from 131,072-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Hyper Page Mode (EDO)

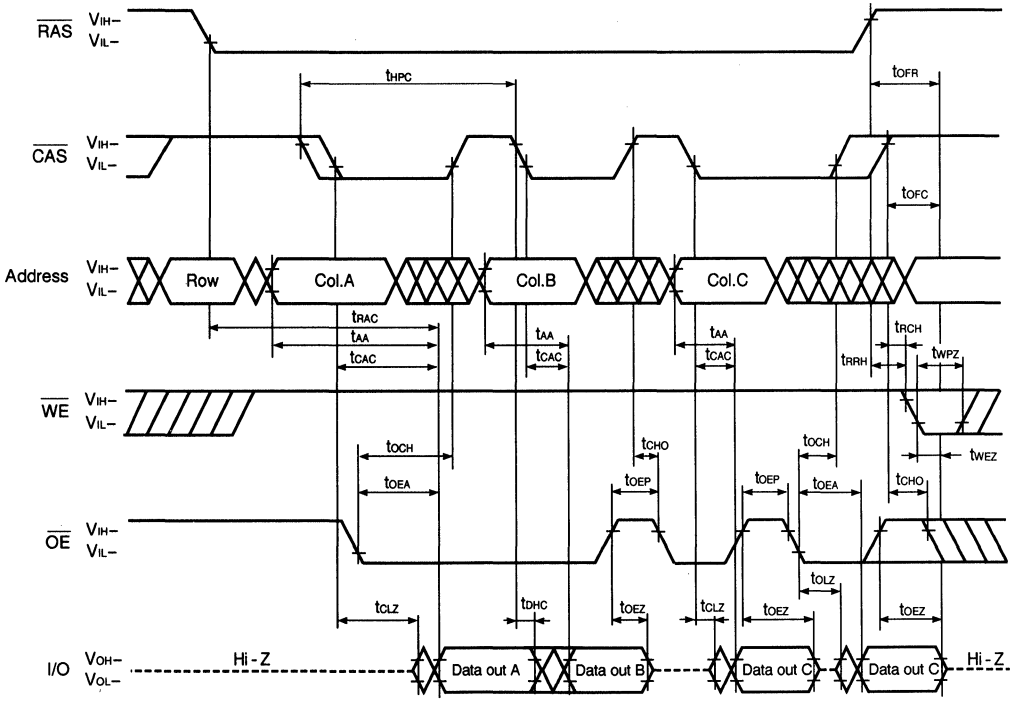
The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. **Data output time is extended.**
   In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**
   In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100	mA	1, 2, 3
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100	mA	1, 2, 3, 4
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{HPC} = 25 ns		100	mA	1, 2, 5
			t_{HPC} = 30 ns		90		
			t_{HPC} = 35 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		100	mA	1, 2
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

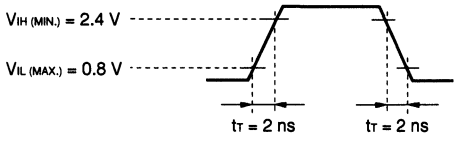
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

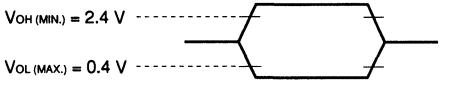
AC Characteristics Test Conditions

(1) Input timing specification

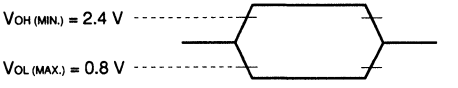


(2) Output timing specification

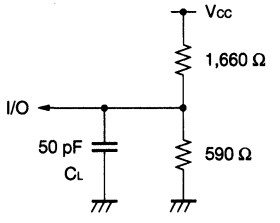
- μPD421805



μPD421805-A



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	124	–	124	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	–	50	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	70	10,000	70	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	12	10,000	15	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	70	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	55	20	52	20	50	ns	1
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	15	35	15	30	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	2
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	12	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	t_{OED}	15	–	15	–	15	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	
Refresh time	t_{REF}	–	8	–	8	–	8	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter		Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$		t_{RAC}	–	70	–	70	–	70	ns	1
Access time from $\overline{CAS}$	μPD421805-A	t_{CAC}	–	20	–	20	–	–	ns	1
	μPD421805		–	15	–	18	–	20		
Access time from column address		t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$		t_{OEA}	–	20	–	20	–	20	ns	
Column address lead time referenced to $\overline{RAS}$		t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time		t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$		t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$		t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$		t_{OEZ}	0	15	0	15	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$		t_{CHO}	5	–	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	12	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	12	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	12	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	165	–	165	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	89	–	89	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	–	37	–	39	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	49	–	54	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	35	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	70	125,000	70	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	15	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	33	–	40	–	45	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	54	–	59	–	64	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{HPRWC}	68	–	75	–	83	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	15	0	15	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	15	0	15	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	15	0	15	0	15	ns	3,4
Access time from previous $\overline{WE}$ (Hyper page mode (EDO) read and write cycle)	t_{AWE}	–	55	–	65	–	75	ns	
Access time from previous $\overline{CAS}$ (Hyper page mode (EDO) write and read cycle)	t_{ACE}	–	55	–	65	–	75	ns	

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

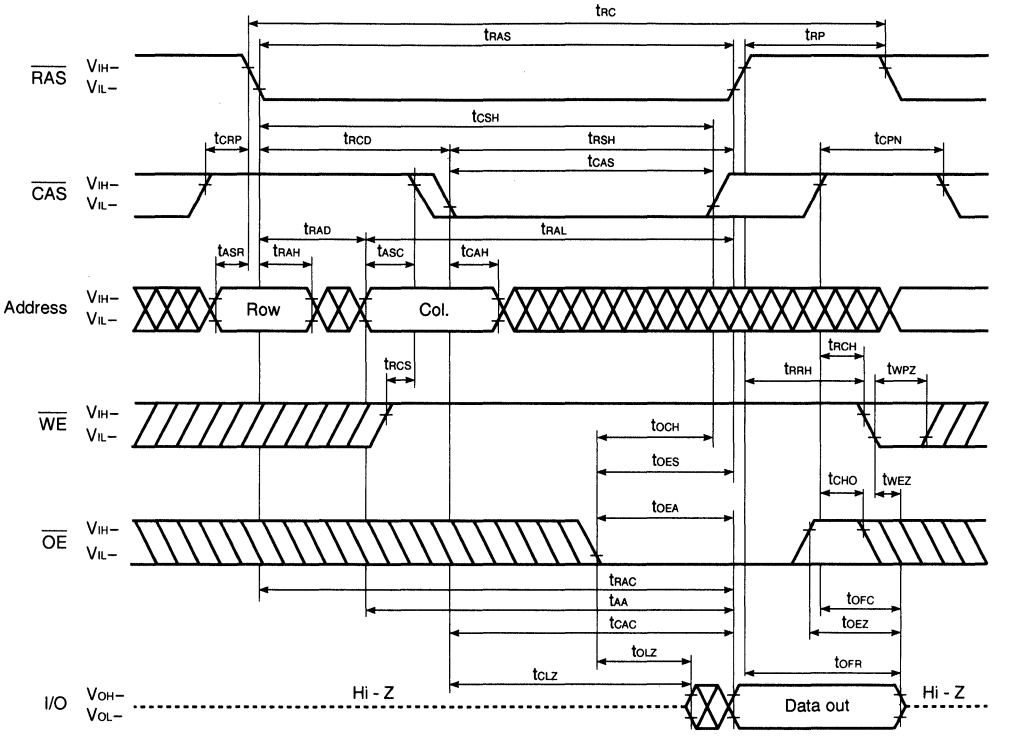
(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

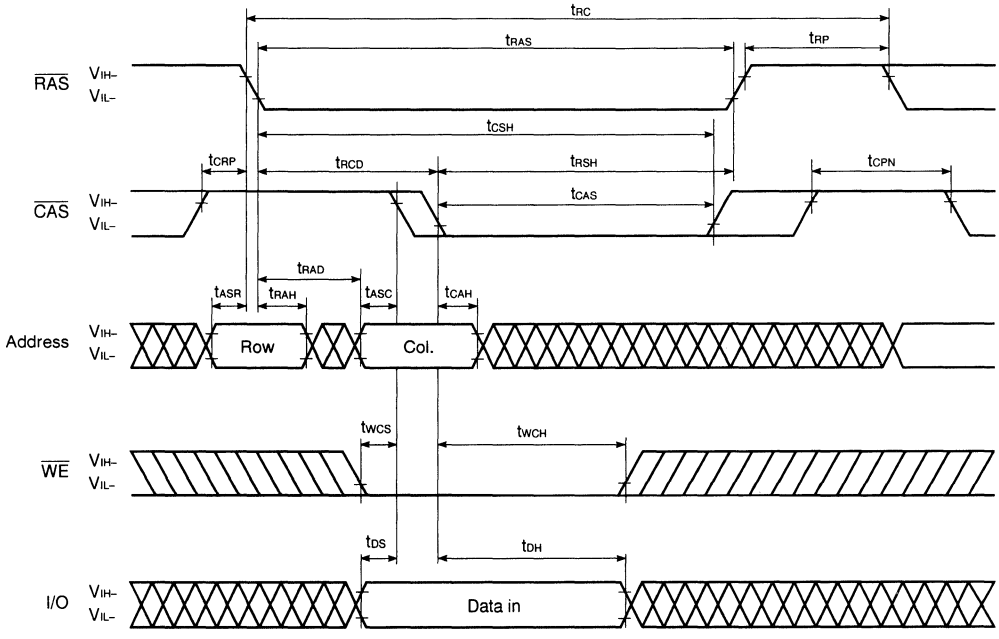
Refresh Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Read Cycle

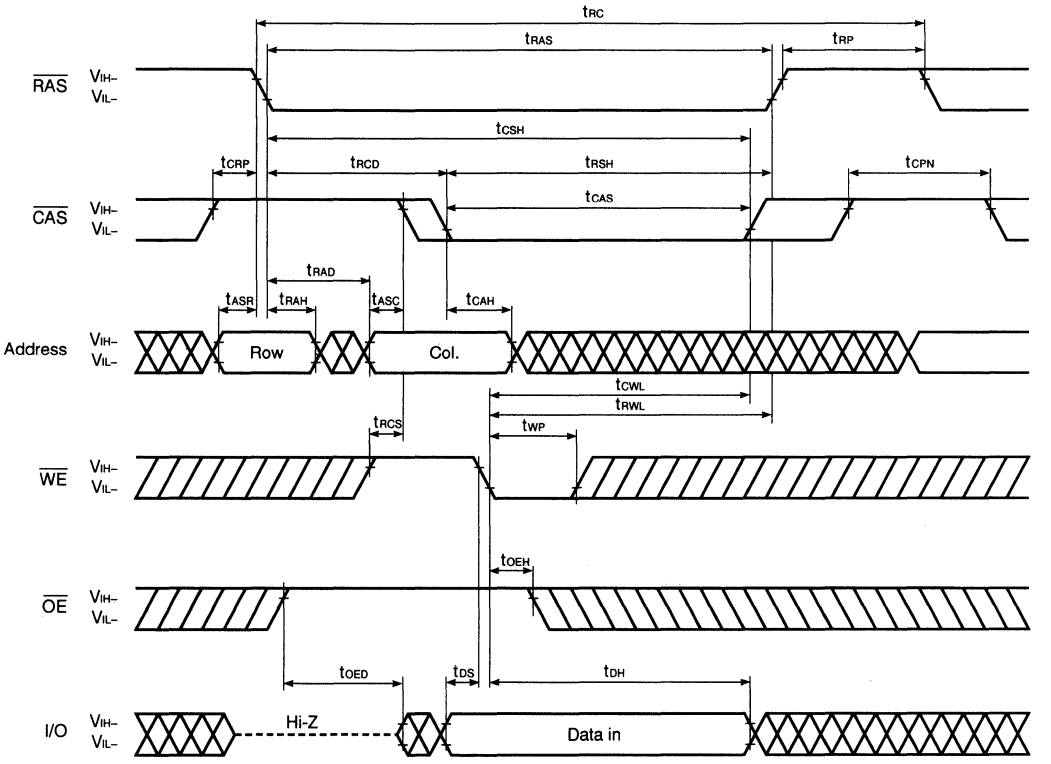

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
tOEA
OE
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Early Write Cycle

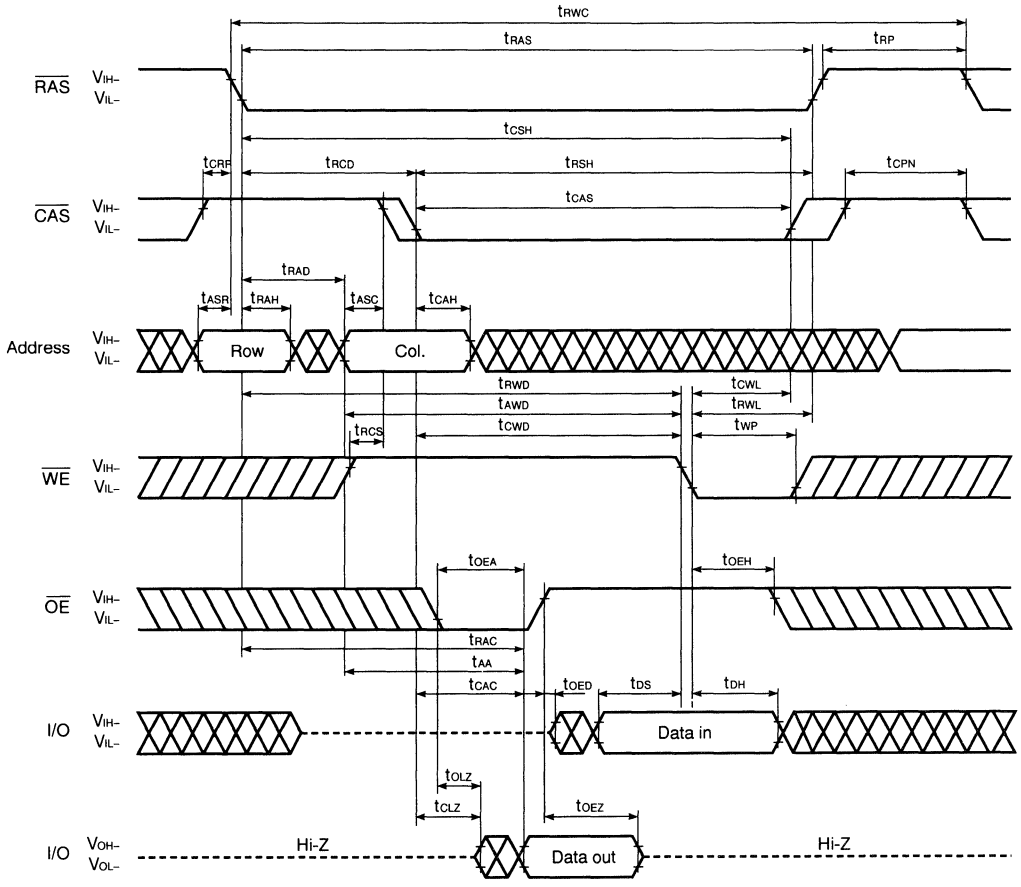


Remark $\overline{OE}$: Don't care

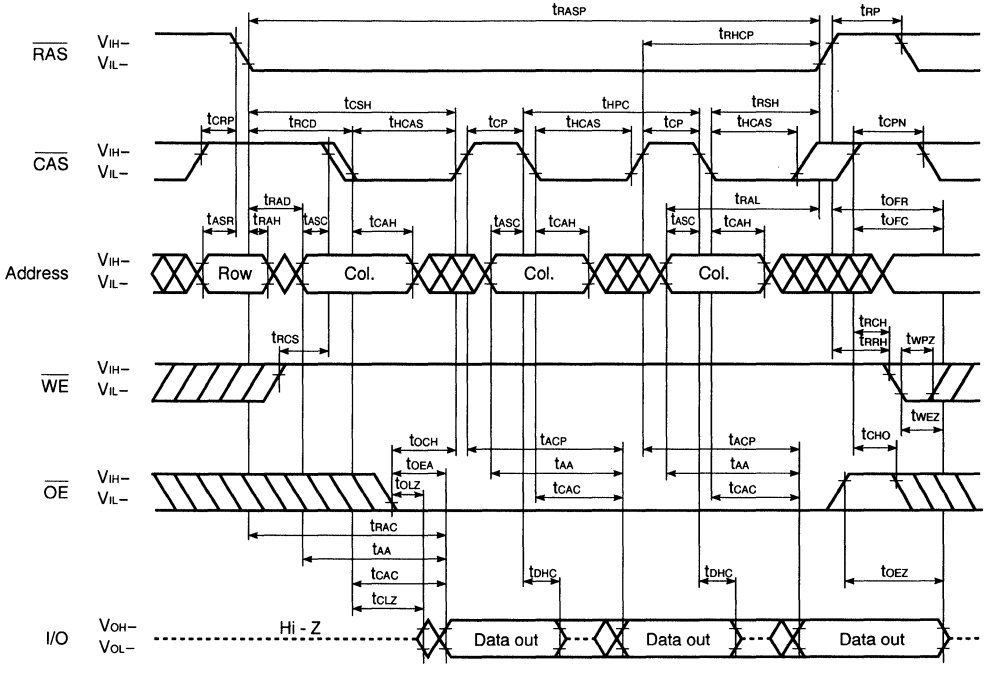
Late Write Cycle



Read Modify Write Cycle

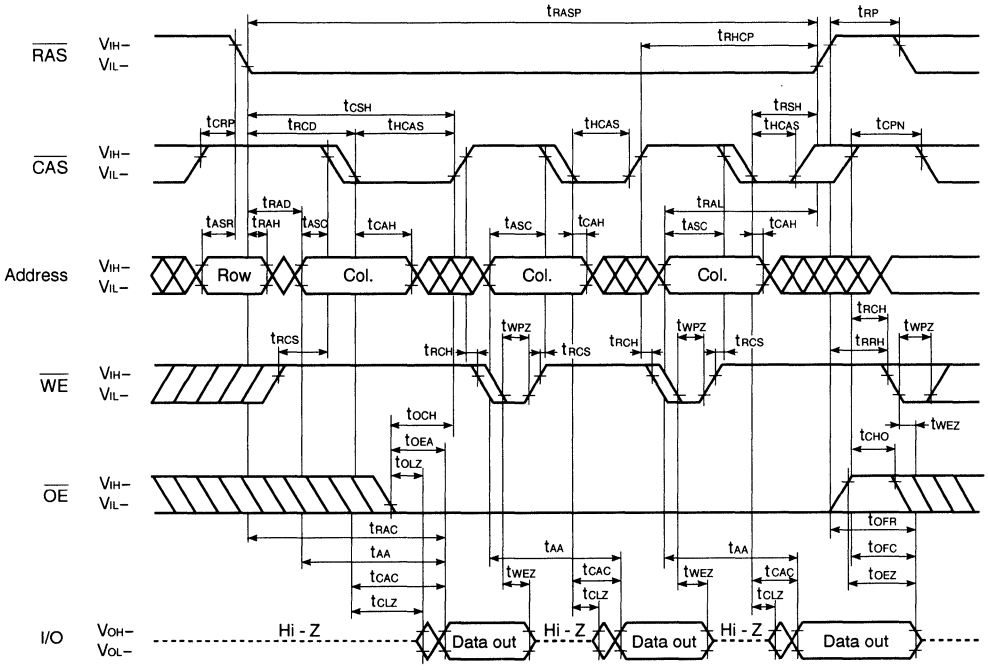


Hyper Page Mode (EDO) Read Cycle



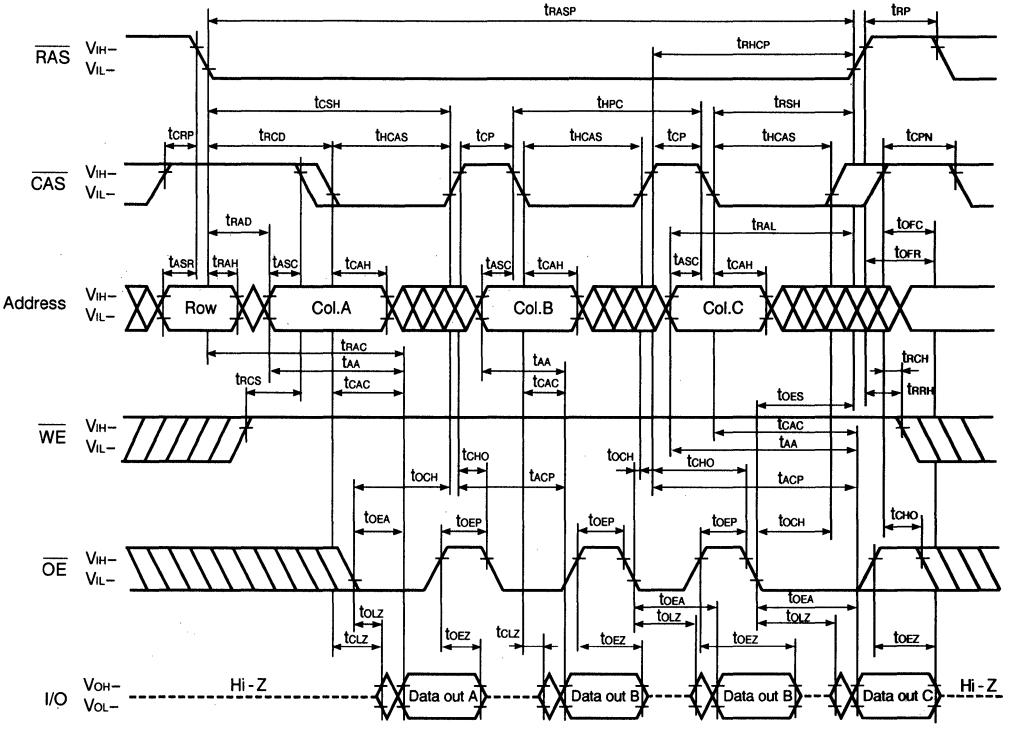
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



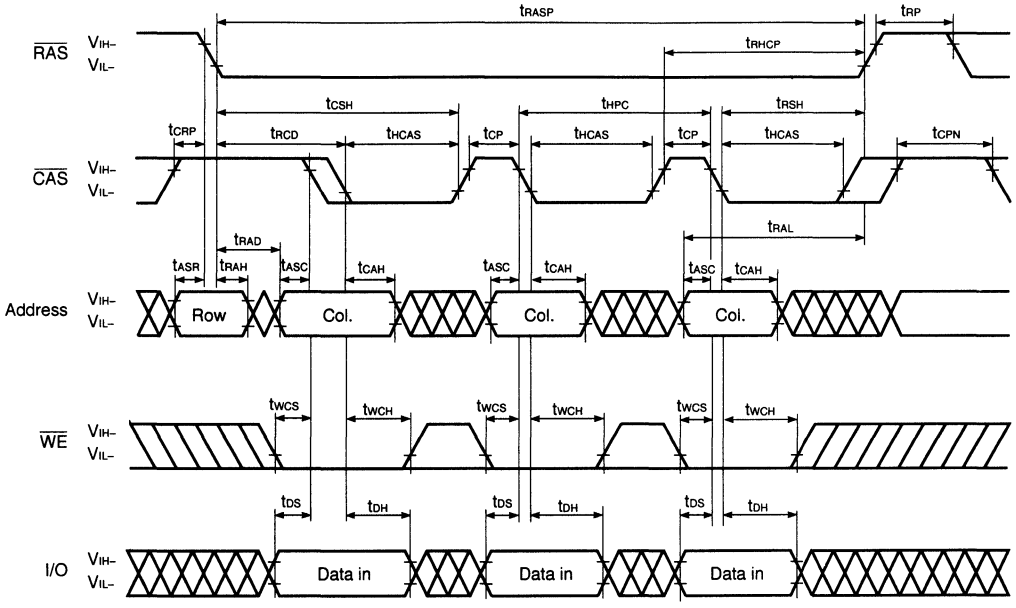
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

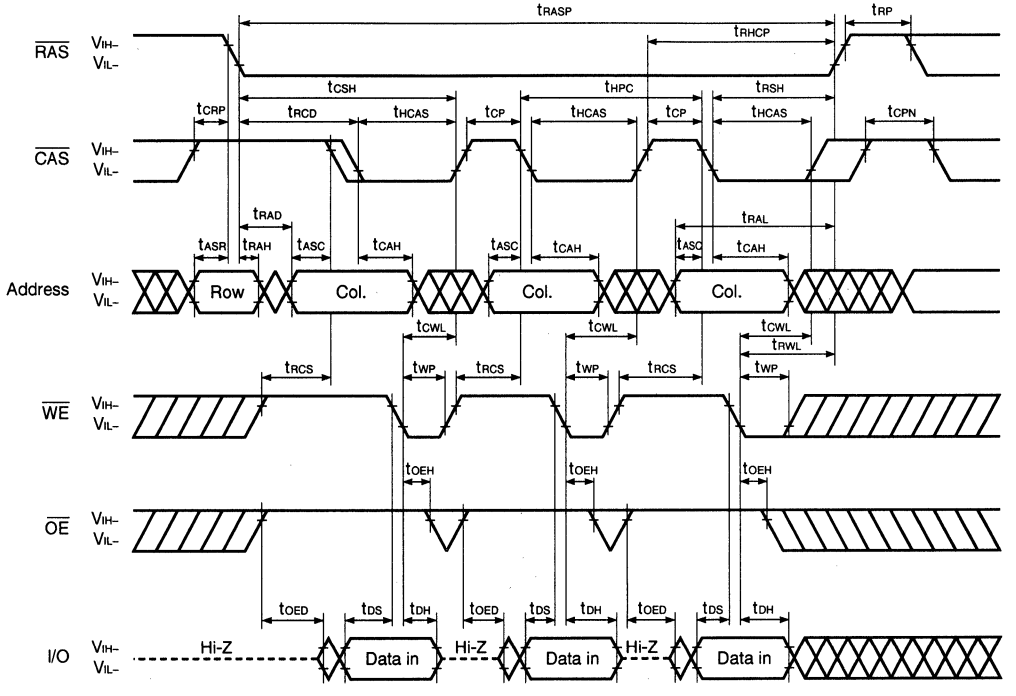
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

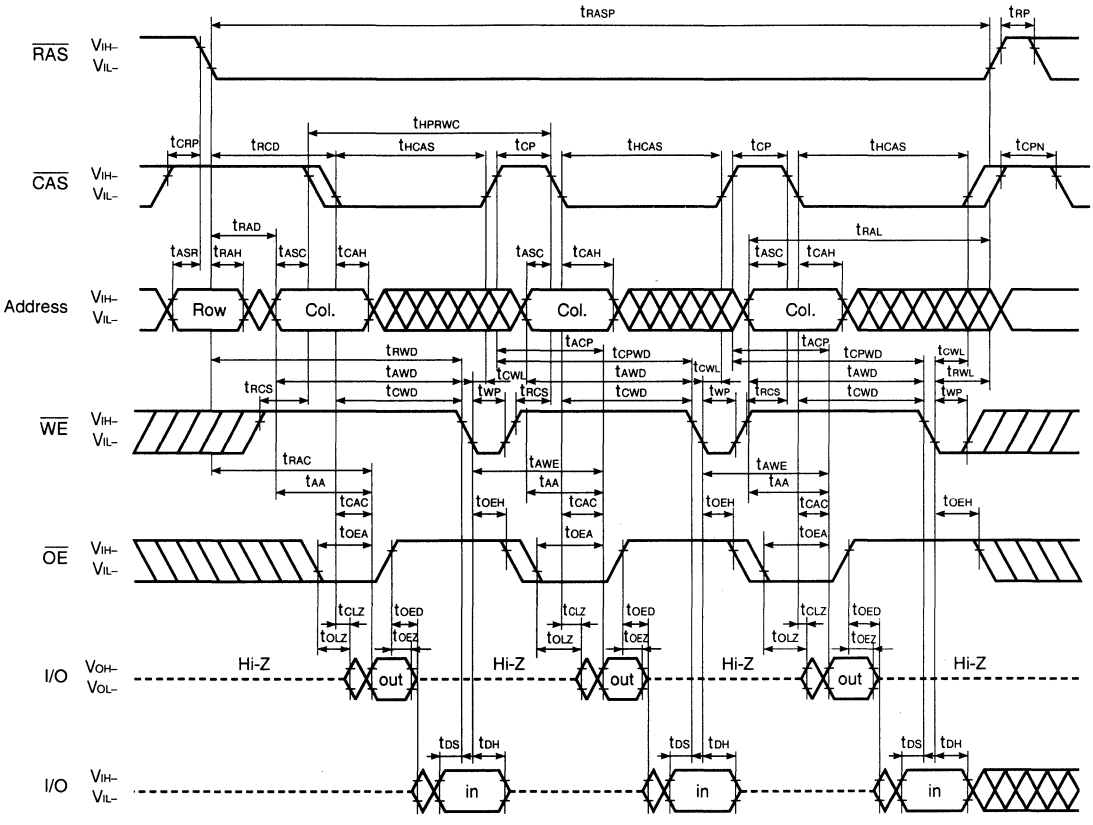
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Late Write Cycle



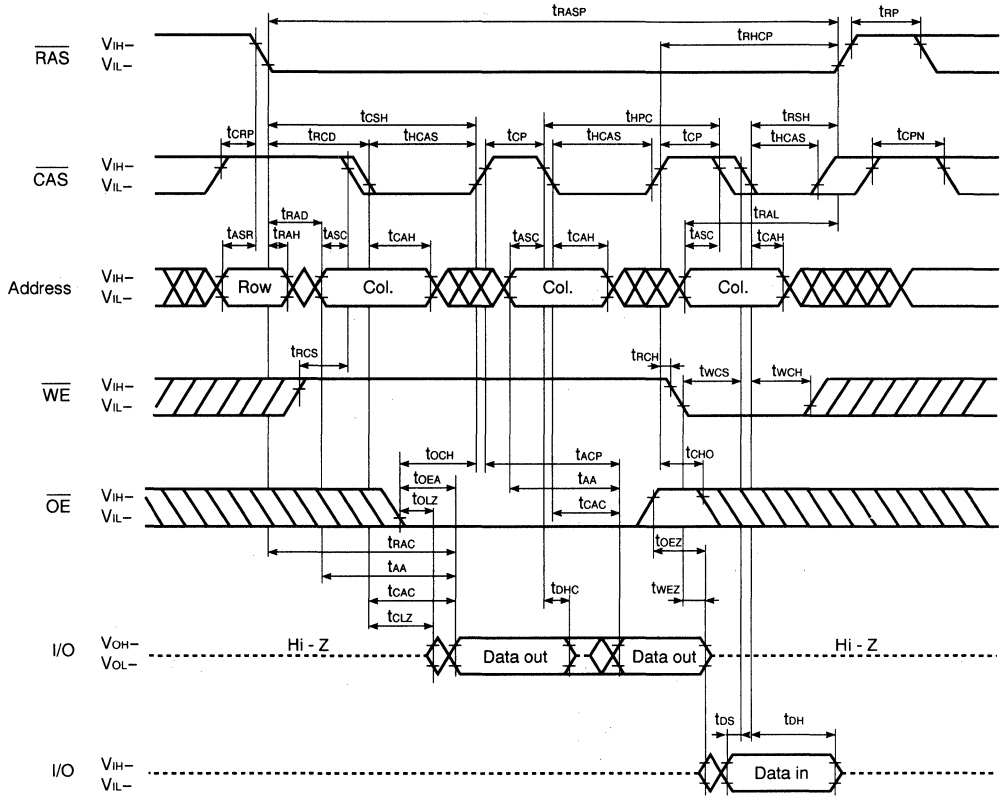
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



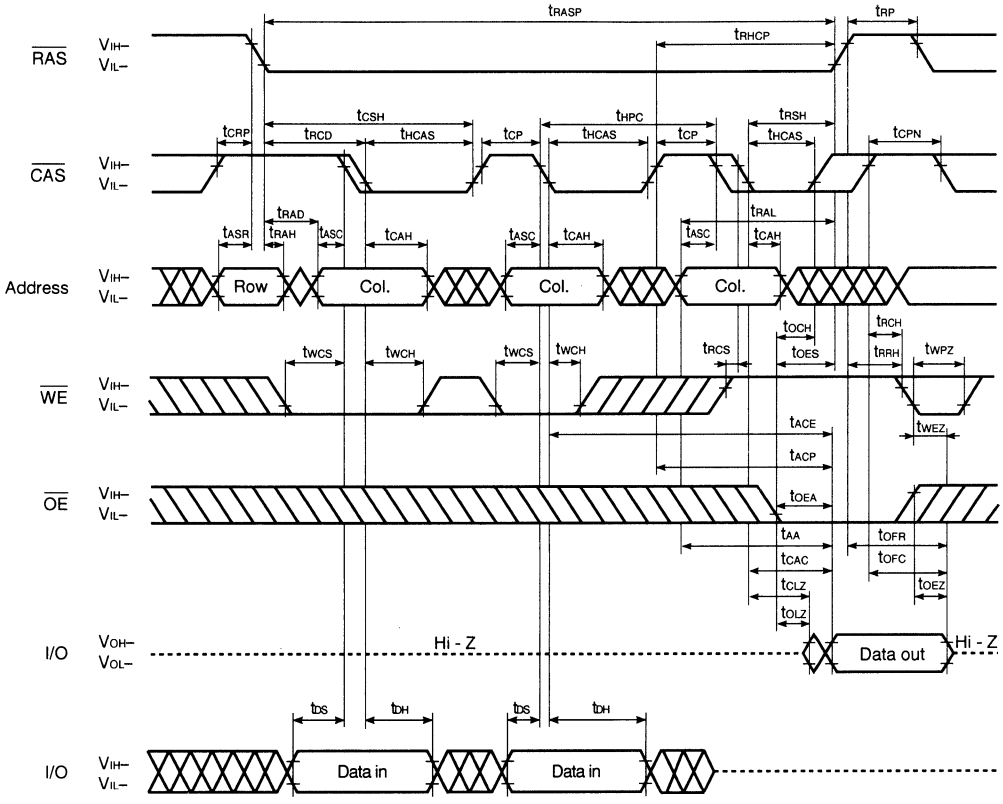
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read and Write Cycle



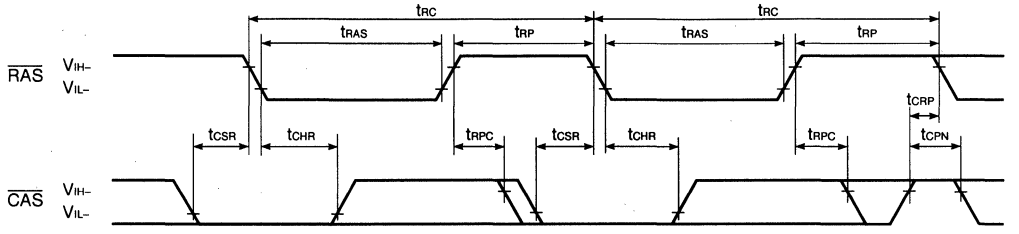
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Write and Read Cycle



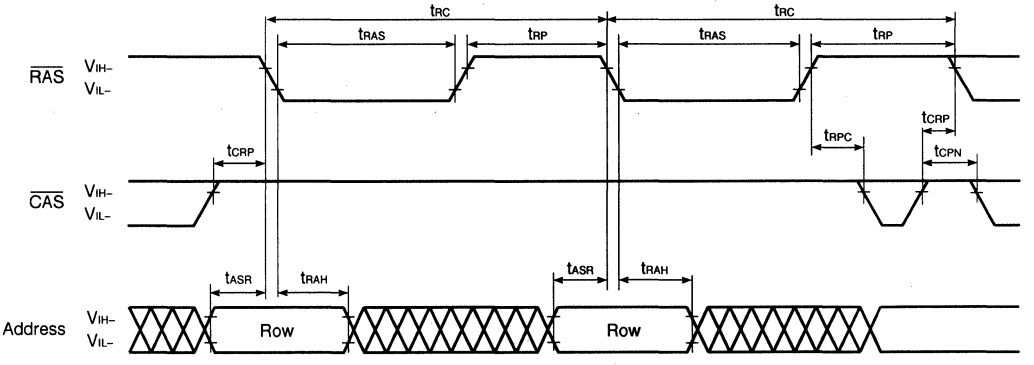
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



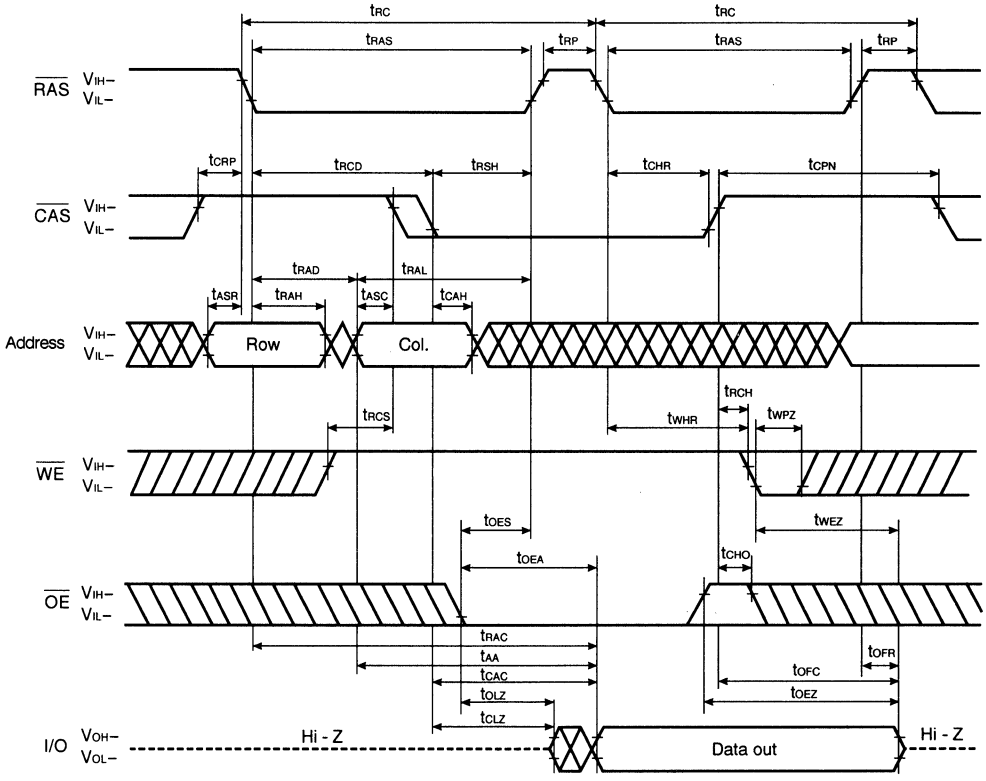
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

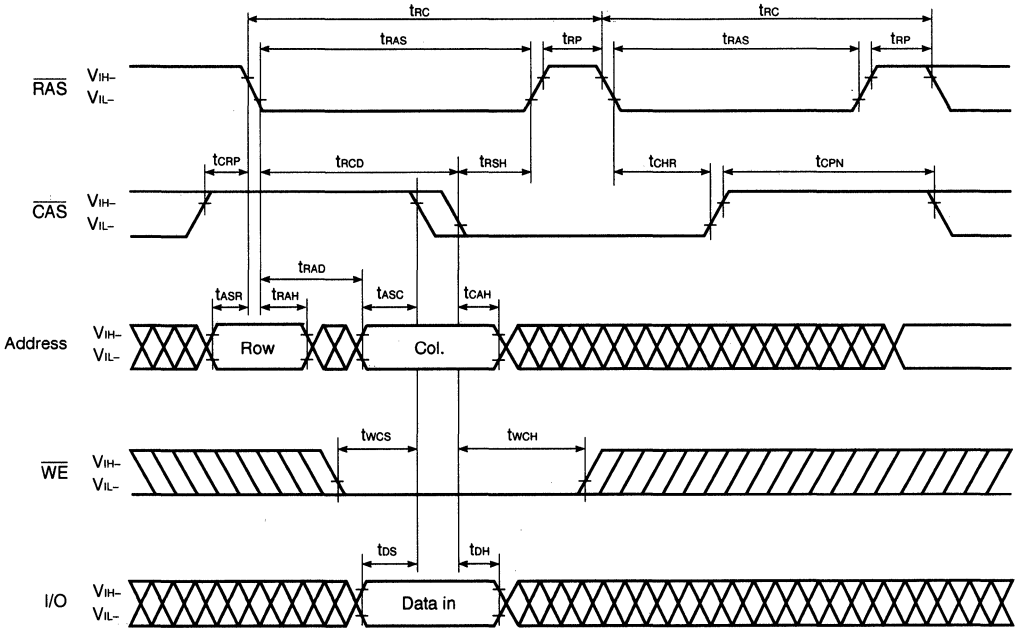


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



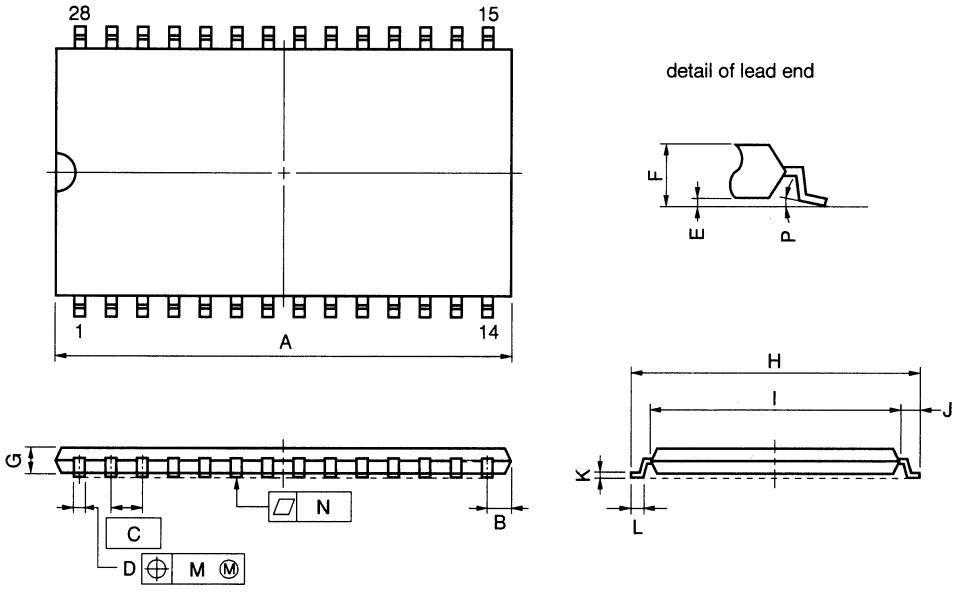
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

28 PIN PLASTIC TSOP(II) (400 mil)



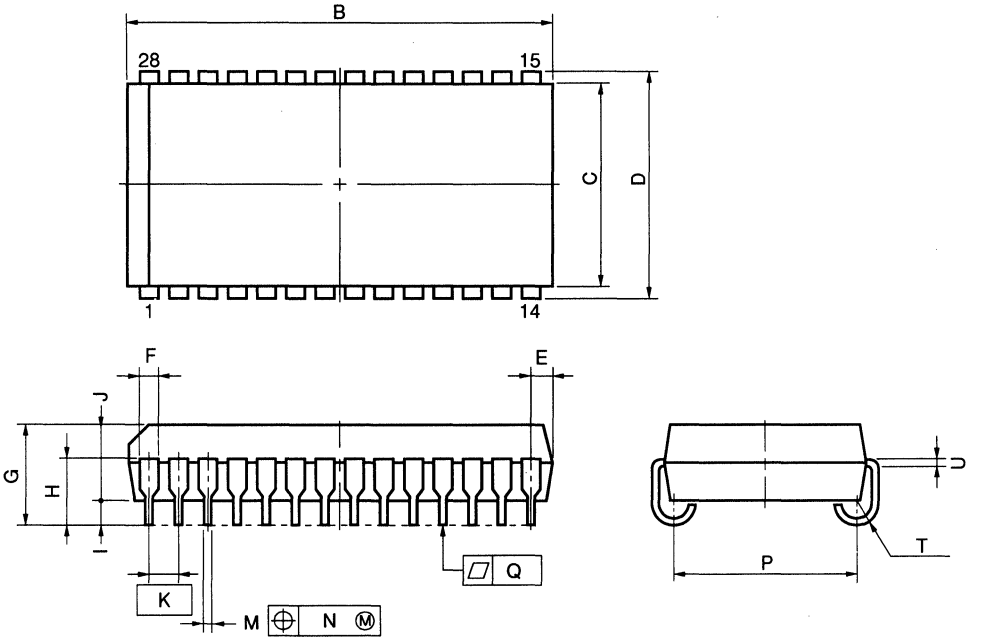
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD5

28 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.4±0.2	$0.094^{+0.008}_{-0.007}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P28LA-400A-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD421805.

Types of Surface Mount Device

μPD421805G5: 28-pin plastic TSOP (II) (400 mil)
μPD421805LE: 28-pin plastic SOJ (400 mil)

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD421165

1 M-BIT DYNAMIC RAM
64K-WORD BY 16-BIT, HYPER PAGE MODE (EDO), BYTE READ/WRITE MODE

Description

The μPD421165 is a 65,536 words by 16 bits CMOS dynamic RAM with optional hyper page mode (EDO).
Hyper page mode (EDO) is a kind of the page mode and is useful for the read operation.
The μPD421165 is packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

Features

- Hyper page mode (EDO)
- 65,536 words by 16 bits organization
- Single +5.0 V ±10 % power supply
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 256 refresh cycles/4 ms

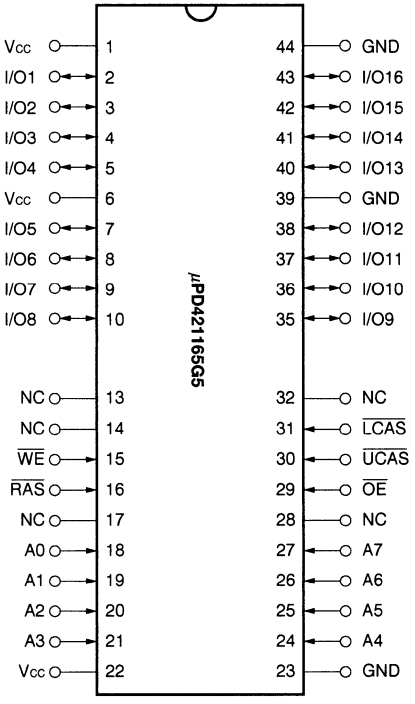
Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)
	Active (MAX.)	Standby (MAX.)			
μPD421165-25-A	632.5 mW	5.5 mW (CMOS level input)	70 ns	124 ns	25 ns
μPD421165-30-A					30 ns
μPD421165-25					25 ns
μPD421165-30					30 ns
μPD421165-35					35 ns

Ordering Information

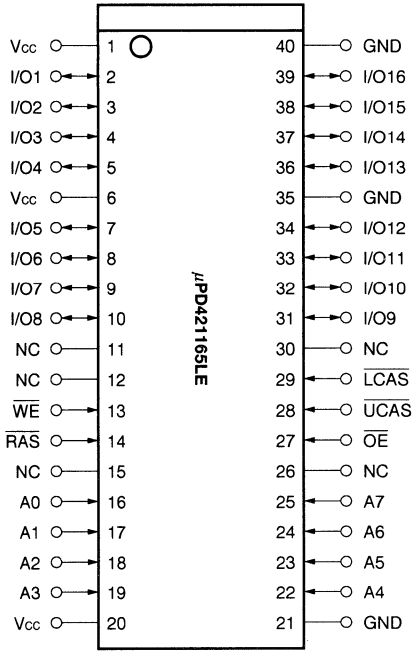
Part number	Access time (MAX.)	Hyper page mode (EDO) cycle time (MIN.)	Package	Refresh
μPD421165G5-25-A	70 ns	25 ns	44-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD421165G5-30-A	70 ns	30 ns		
μPD421165G5-25	70 ns	25 ns		
μPD421165G5-30	70 ns	30 ns		
μPD421165G5-35	70 ns	35 ns		
μPD421165LE-25-A	70 ns	25 ns	40-pin plastic SOJ (400 mil)	
μPD421165LE-30-A	70 ns	30 ns		
μPD421165LE-25	70 ns	25 ns		
μPD421165LE-30	70 ns	30 ns		
μPD421165LE-35	70 ns	35 ns		

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II) (400 mil)

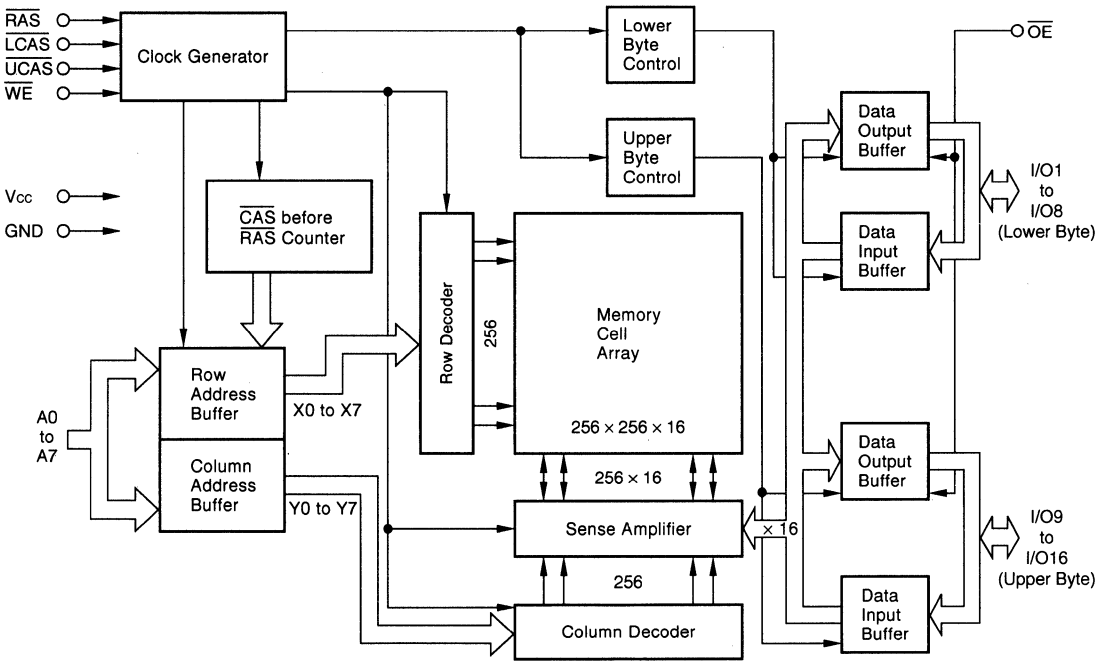


40-pin Plastic SOJ (400 mil)



A0 to A7	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD421165 has input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A7 and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A7 (Address inputs)	Input	Address bus. Input total 16-bit of address signal, upper 8-bit and lower 8-bit in sequence (address multiplex method). Therefore, one word is selected from 65,536-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode (EDO)

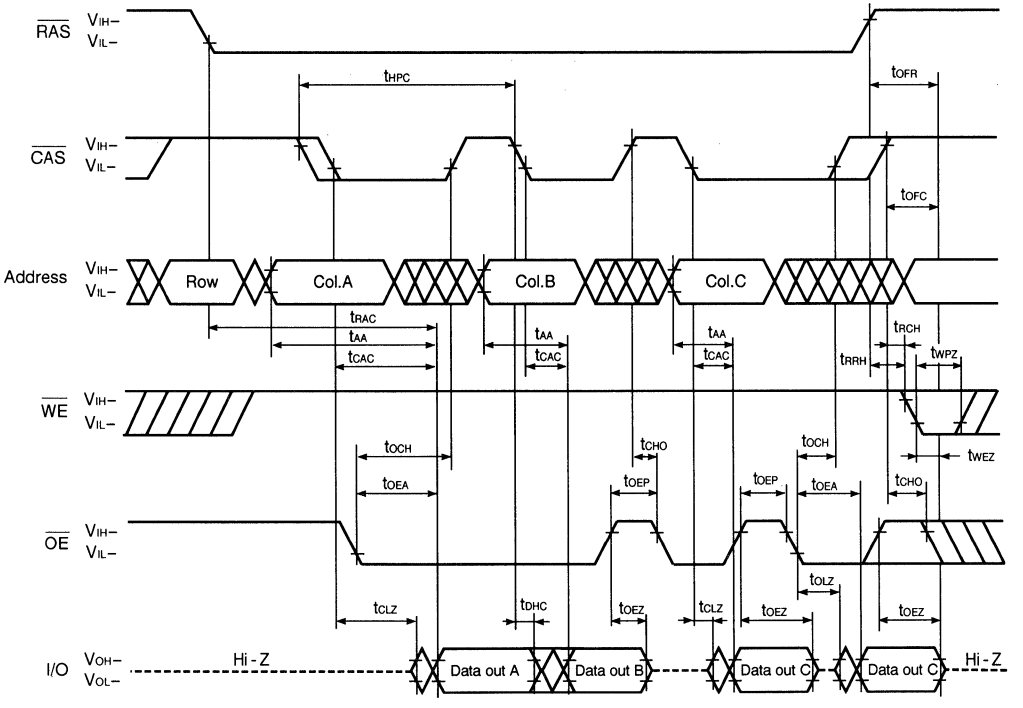
The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

1. **Data output time is extended.**
   In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

2. **The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**
   In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode (EDO) Read Cycle



Cautions when using the hyper page mode (EDO)

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		115	mA	1, 2, 3
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		115	mA	1, 2, 3 ,4
Operating current (Hyper page mode (EDO))	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{HPC} = t_{HPC\ (MIN.)}$, I_O = 0 mA	t_{HPC} = 25 ns		115	mA	1, 2, 5
			t_{HPC} = 30 ns		105		
			t_{HPC} = 35 ns		95		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		115	mA	1, 2
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

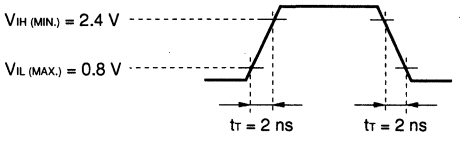
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

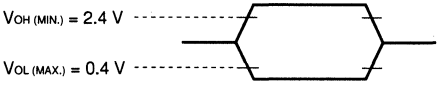
AC Characteristics Test Conditions

(1) Input timing specification

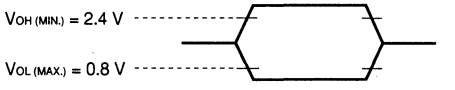


(2) Output timing specification

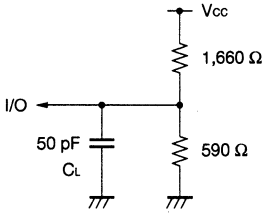
- μPD421165



- μPD421165-A



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	124	–	124	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	–	50	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	70	10,000	70	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	12	10,000	15	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	70	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	55	20	52	20	50	ns	1
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	15	35	15	30	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	2
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	12	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	t_{OES}	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	t_{OLZ}	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	t_{OED}	15	–	15	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$	t_{MRH}	0	–	0	–	0	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	
Refresh time	t_{REF}	–	4	–	4	–	4	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter		Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$		t_{RAC}	–	70	–	70	–	70	ns	1
Access time from $\overline{CAS}$	μPD421165-A	t_{CAC}	–	20	–	20	–	–	ns	1
	μPD421165		–	15	–	18	–	20		
Access time from column address		t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$		t_{OEA}	–	20	–	20	–	20	ns	
Column address lead time referenced to $\overline{RAS}$		t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time		t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$		t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$		t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$		t_{OEZ}	0	15	0	15	0	15	ns	3
$\overline{CAS}$ hold time to $\overline{OE}$		t_{CHO}	5	–	5	–	5	–	ns	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	12	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	12	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	10	–	12	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	12	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	165	–	165	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	89	–	89	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	–	37	–	39	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	49	–	54	–	59	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{HPC}	25	–	30	–	35	–	ns	1
$\overline{RAS}$ pulse width	t_{RASP}	70	125,000	70	125,000	70	125,000	ns	
$\overline{CAS}$ pulse width	t_{HCAS}	10	10,000	12	10,000	15	10,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	33	–	40	–	45	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	54	–	59	–	64	–	ns	2
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{HPRWC}	68	–	75	–	83	–	ns	
Data output hold time	t_{DHC}	5	–	5	–	5	–	ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5	–	5	–	5	–	ns	4
$\overline{OE}$ precharge time	t_{OEP}	5	–	5	–	5	–	ns	
Output buffer turn-off delay from $\overline{WE}$	t_{WEZ}	0	15	0	15	0	15	ns	3,4
$\overline{WE}$ pulse width	t_{WPZ}	10	–	10	–	10	–	ns	4
Output buffer turn-off delay from $\overline{RAS}$	t_{OFR}	0	15	0	15	0	15	ns	3,4
Output buffer turn-off delay from $\overline{CAS}$	t_{OFC}	0	15	0	15	0	15	ns	3,4
Access time from previous $\overline{WE}$ (Hyper page mode (EDO) read modify write cycle)	t_{AWE}	–	55	–	65	–	75	ns	
Access time from previous $\overline{CAS}$ (Hyper page mode (EDO) write and read cycle)	t_{ACE}	–	55	–	65	–	75	ns	

Notes 1. $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.

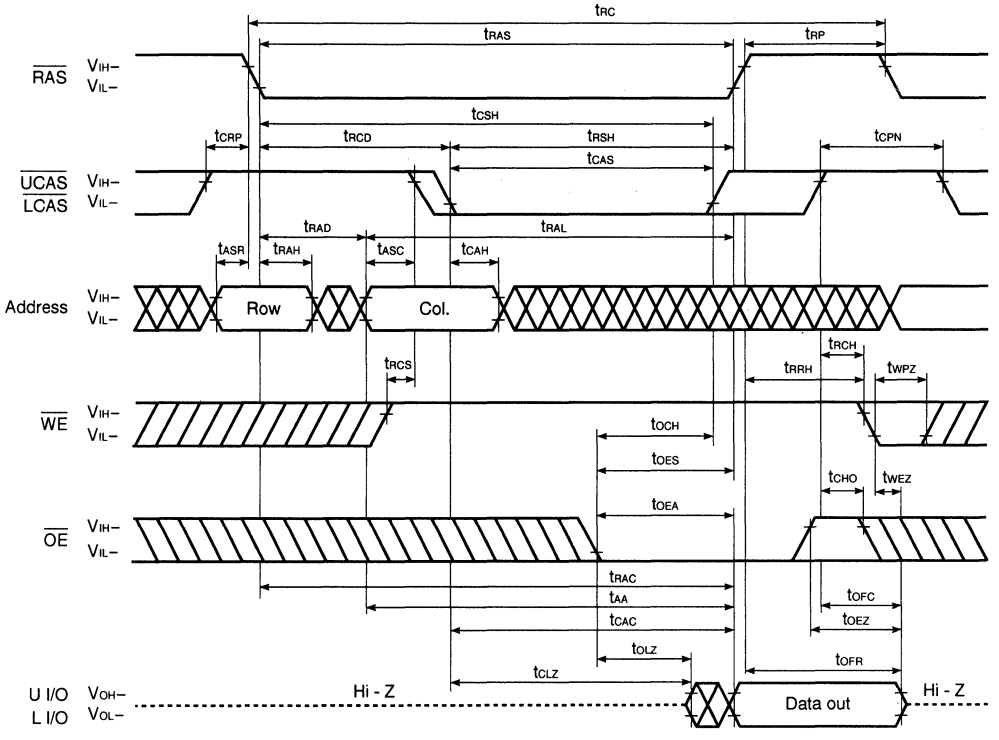
(3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

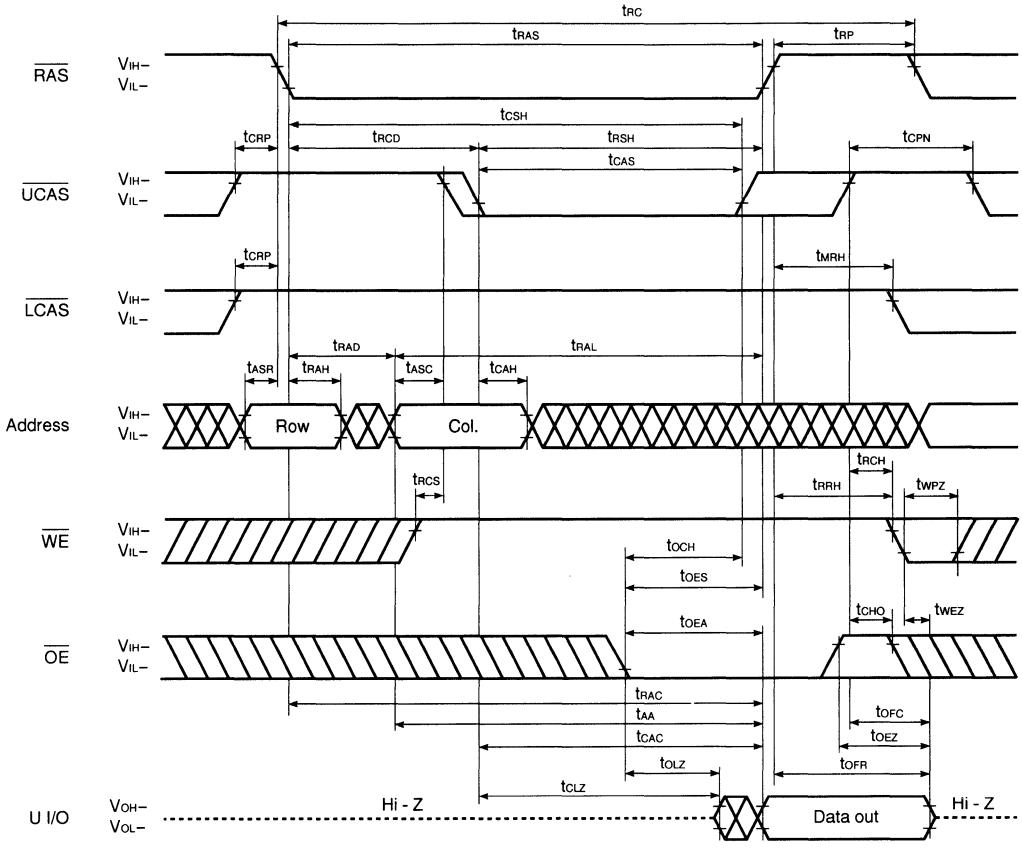
Refresh Cycle

Parameter	Symbol	t_{HPC} = 25 ns		t_{HPC} = 30 ns		t_{HPC} = 35 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Read Cycle

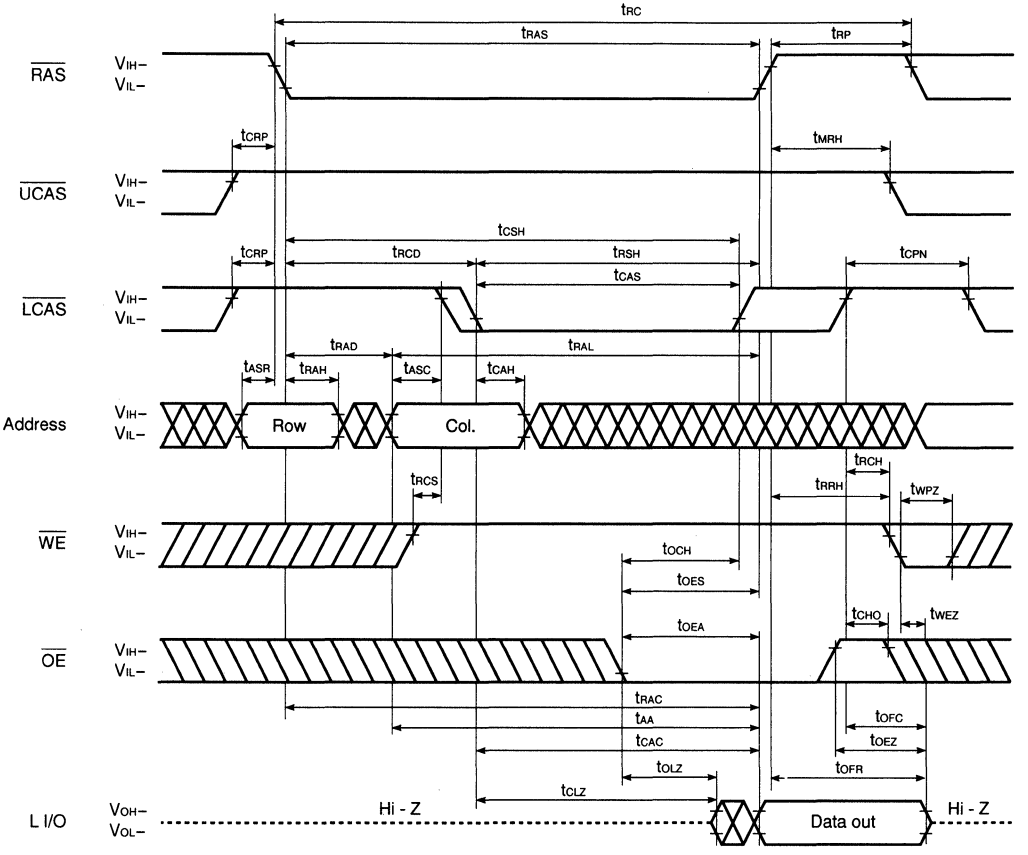

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS VIH–
LCAS VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCH
tRCS
tRRH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
OE VIH– VIL–
tOEA
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O VOH–
L I/O VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



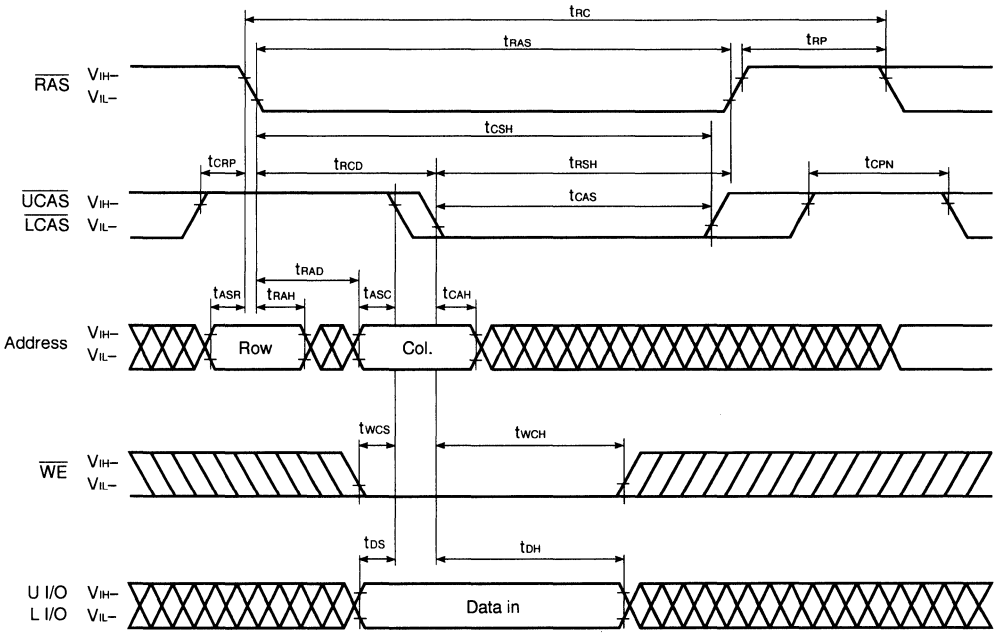
Remark L I/O: Hi-Z

Lower Byte Read Cycle



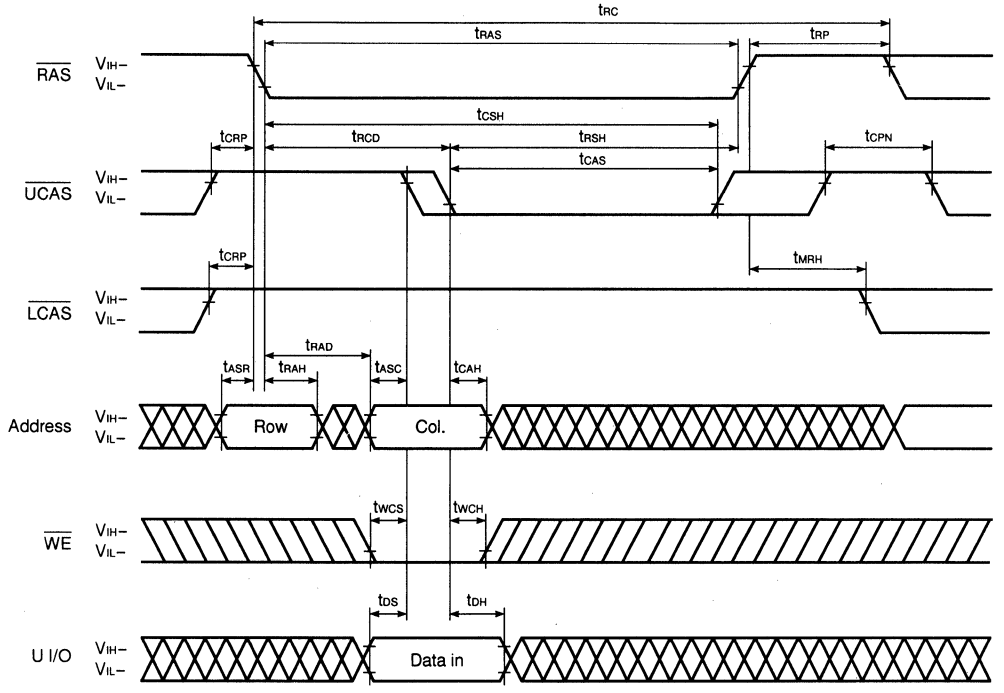
Remark U I/O: Hi-Z

Early Write Cycle



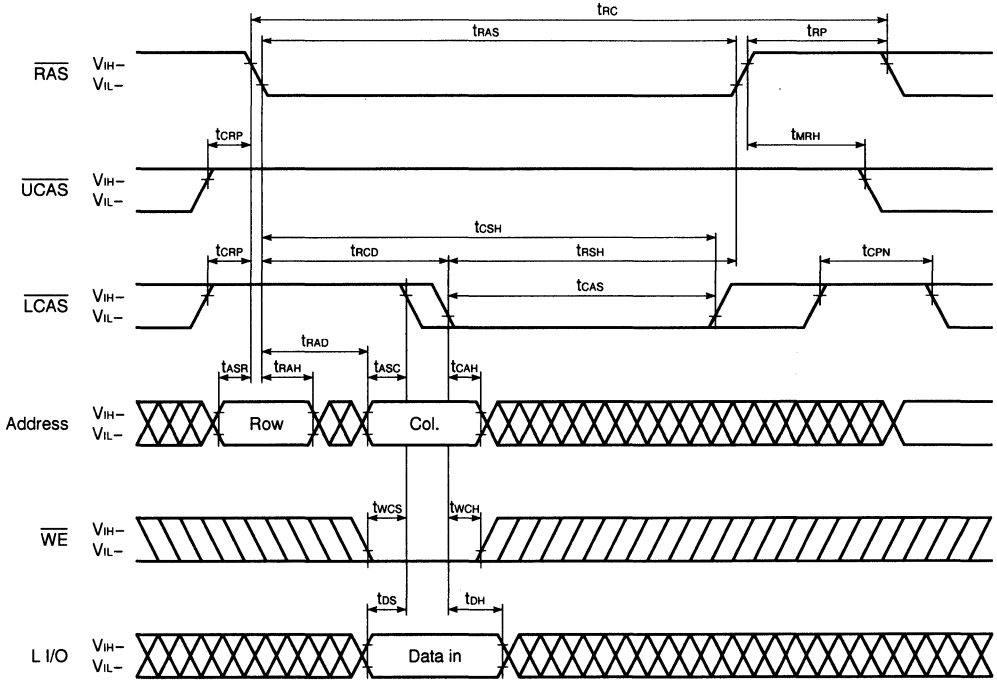
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



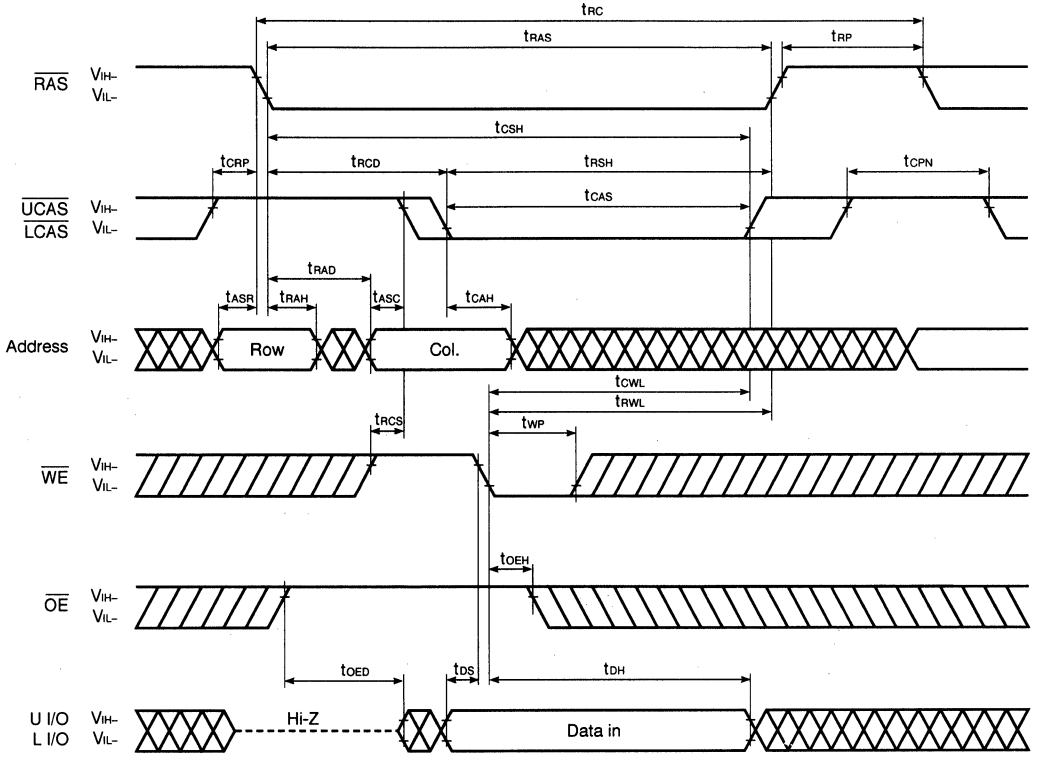
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

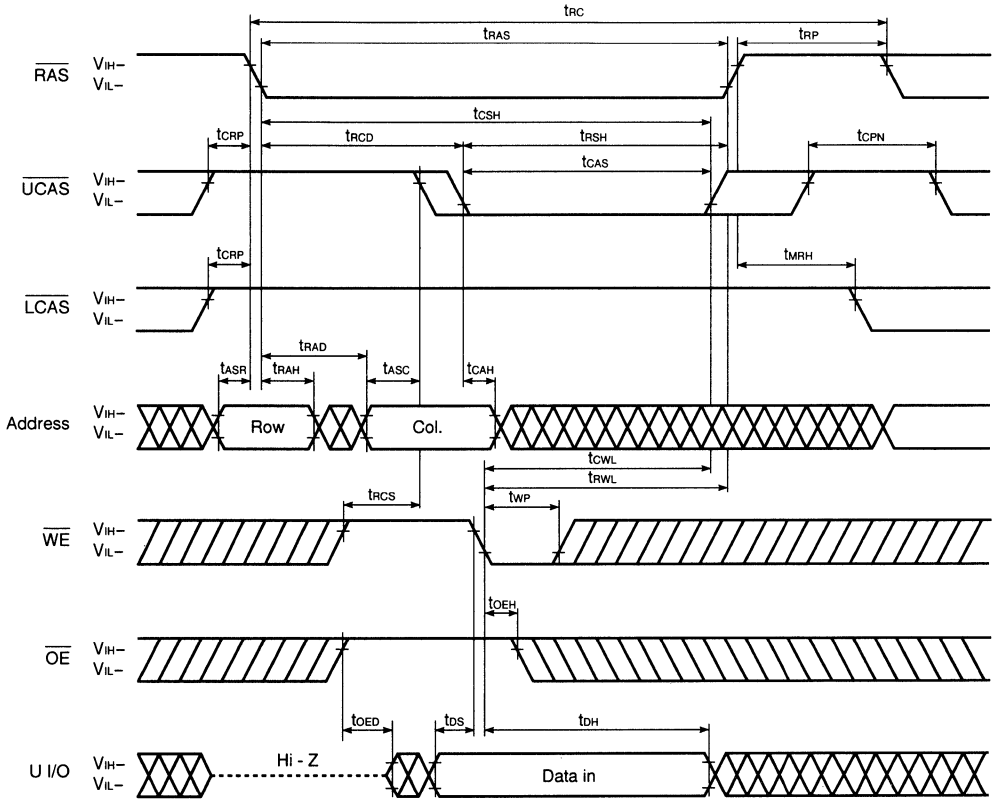


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

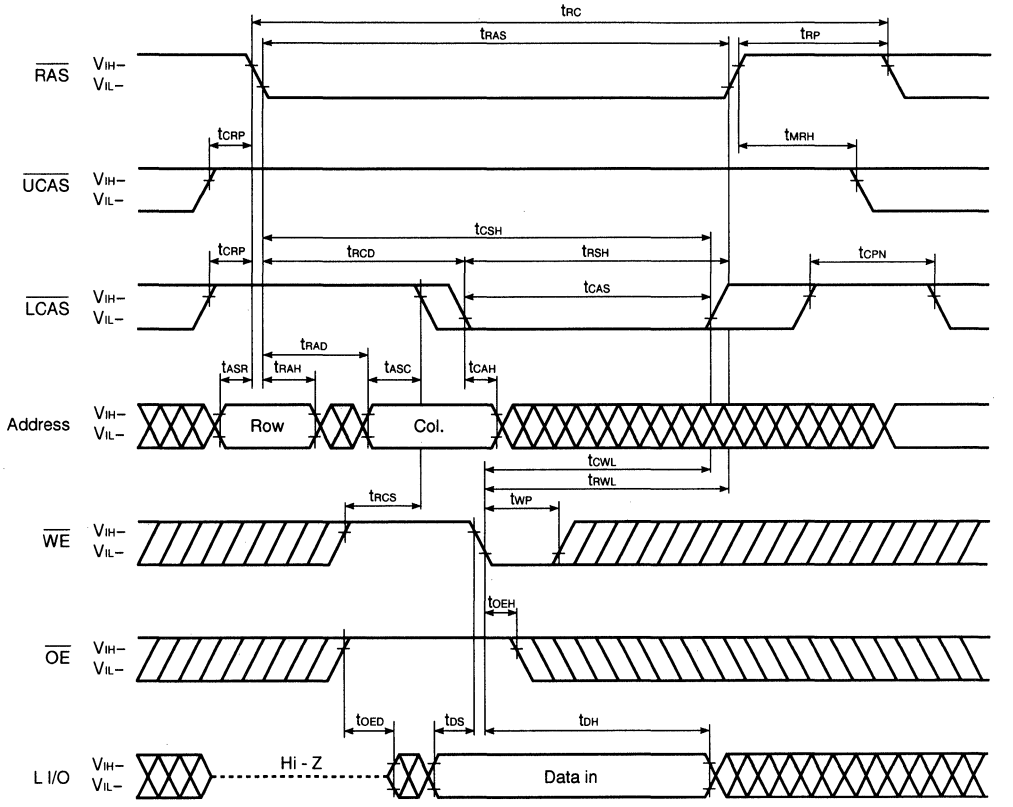


Upper Byte Late Write Cycle



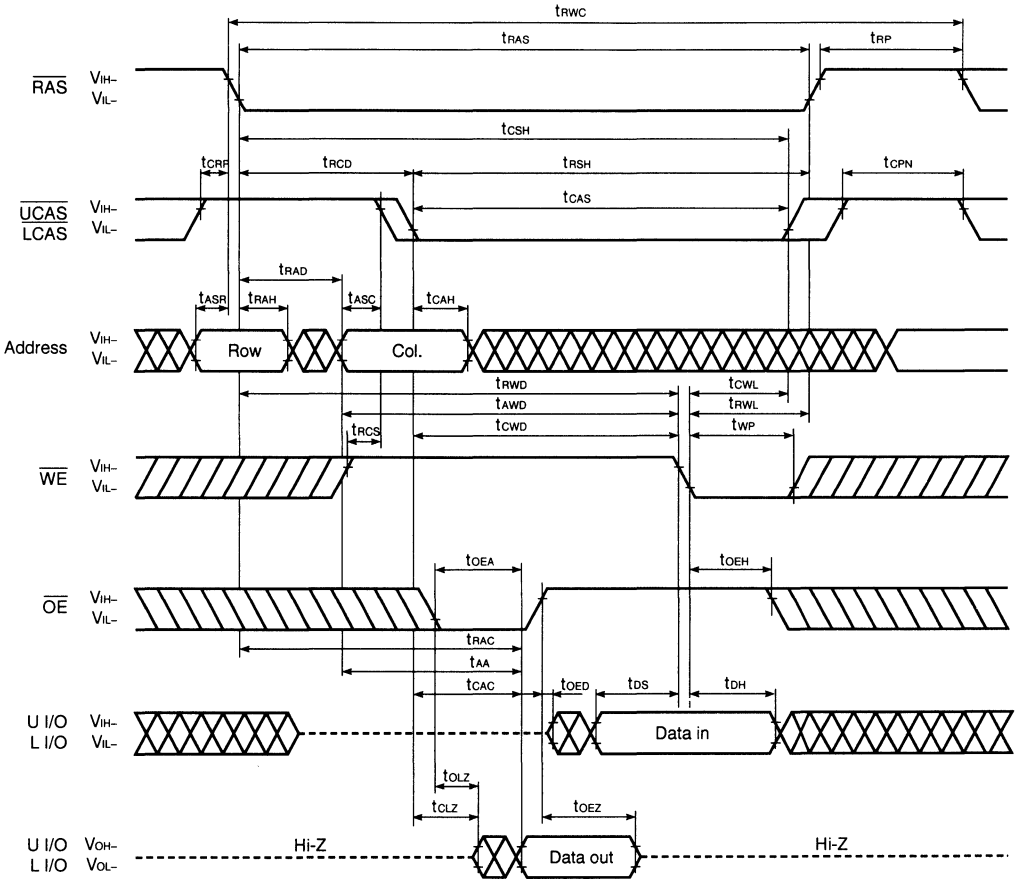
Remark L I/O: Don't care

Lower Byte Late Write Cycle

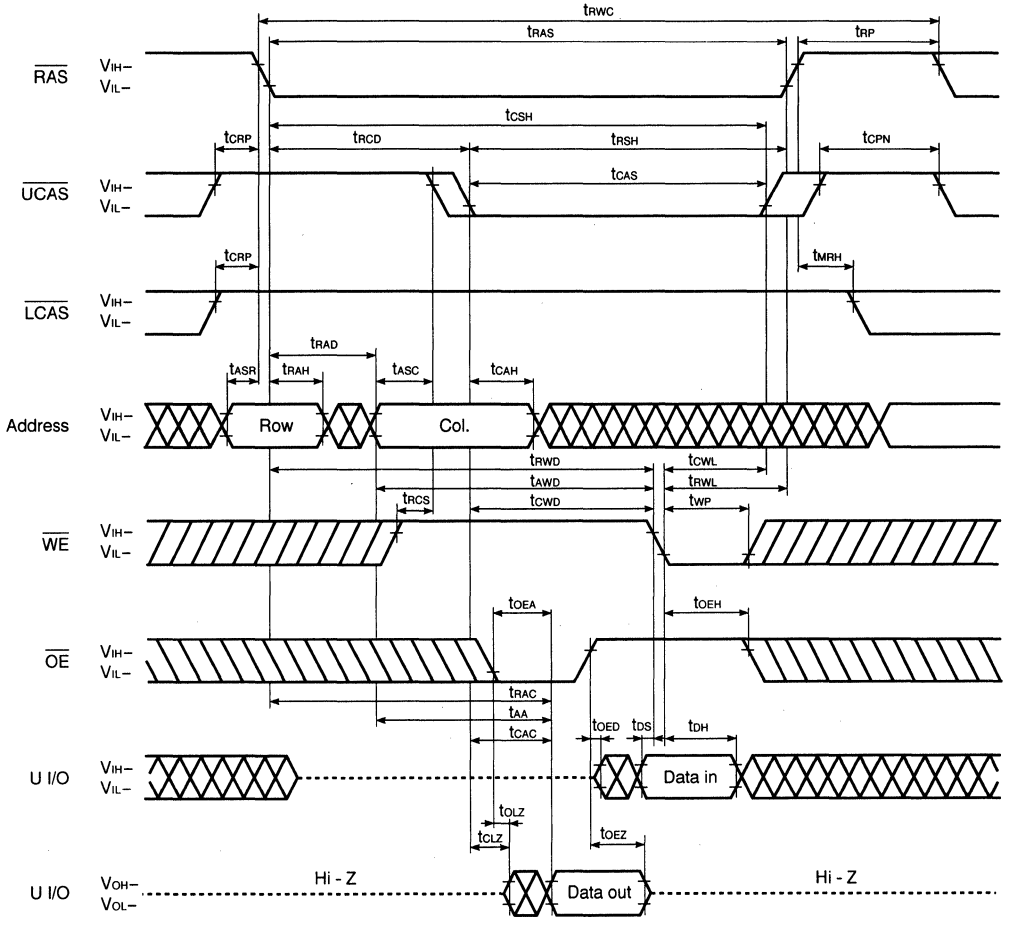


Remark U I/O: Don't care

Read Modify Write Cycle

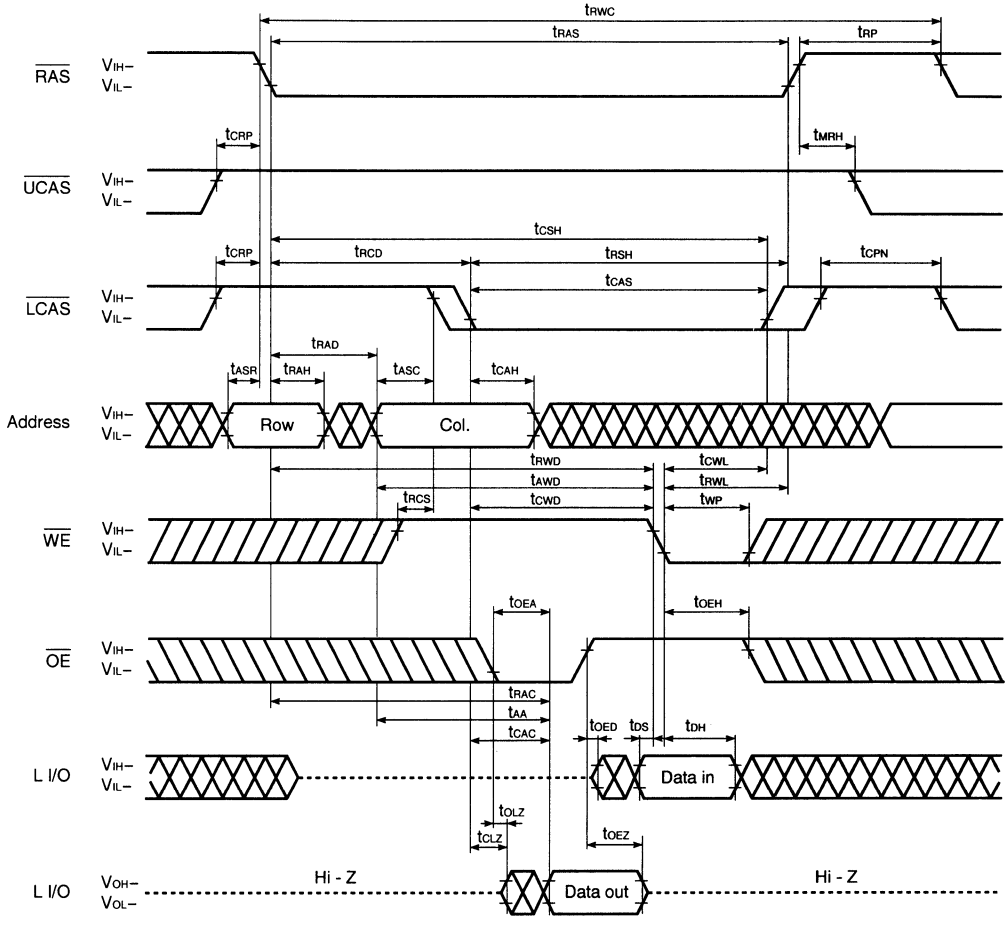


Upper Byte Read Modify Write Cycle



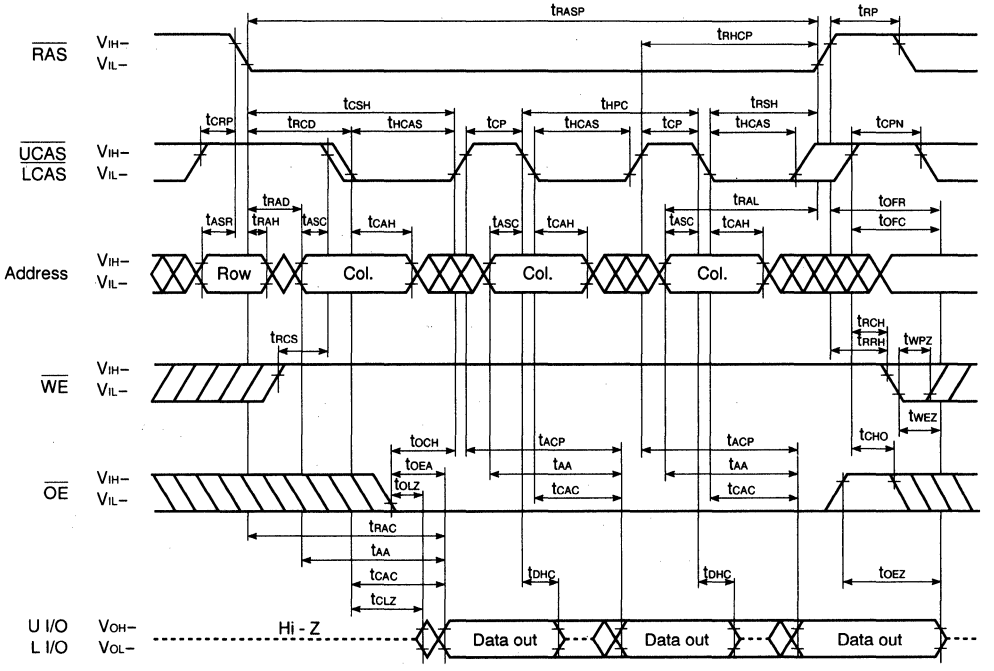
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



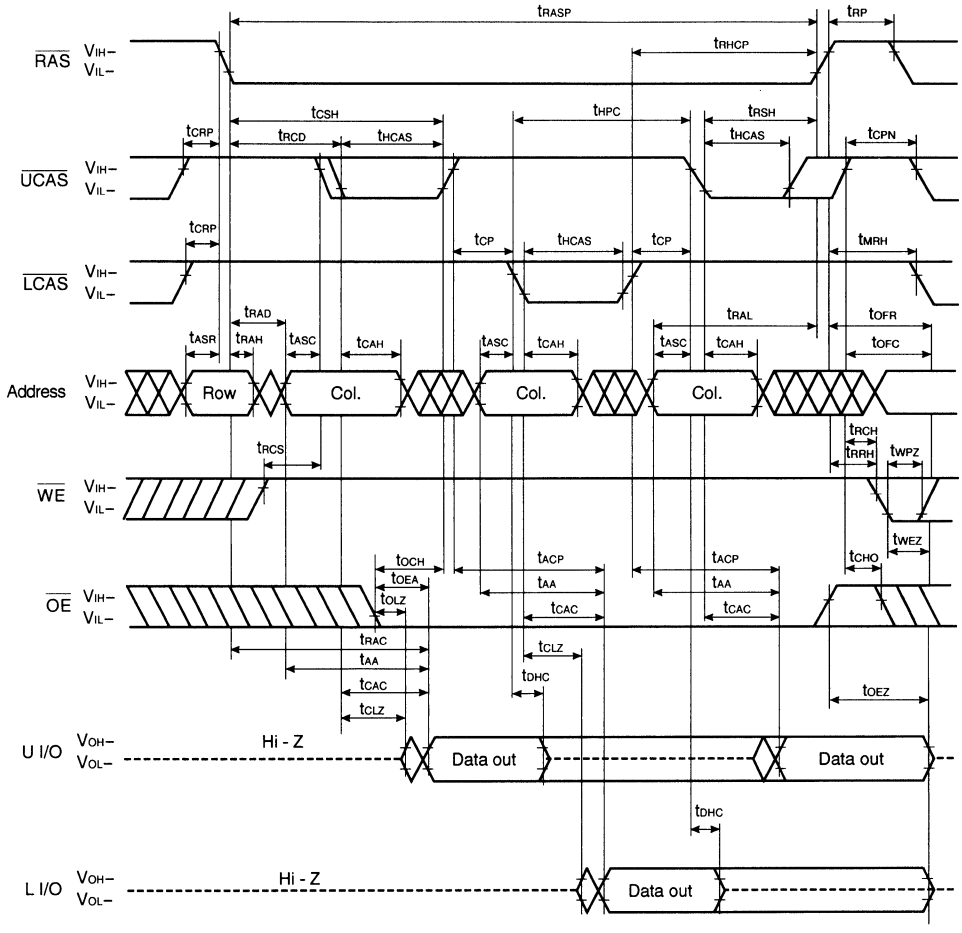
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode (EDO) Read Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

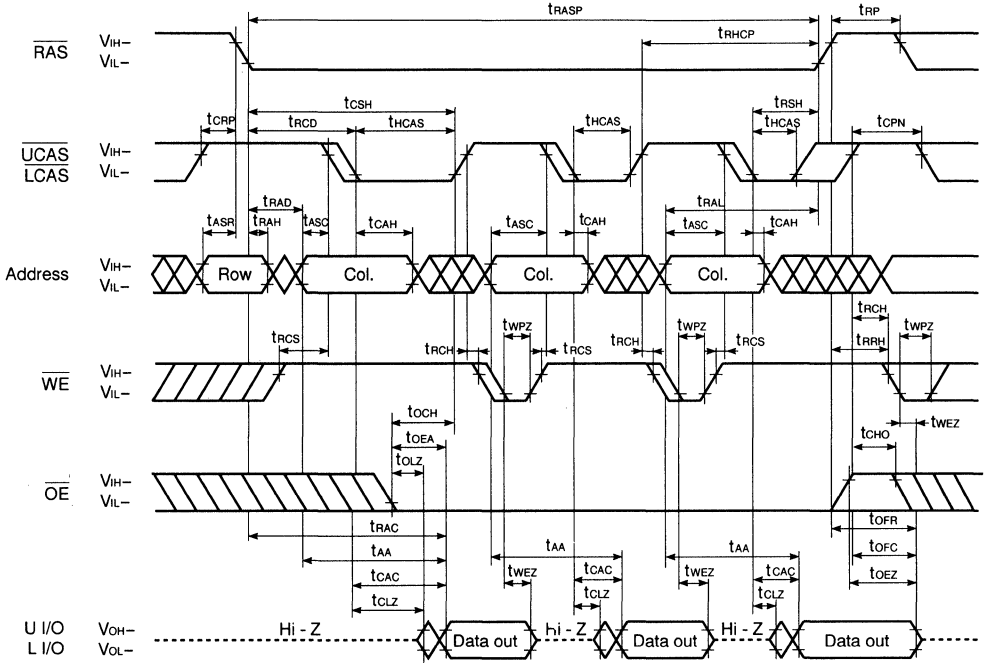
Hyper Page Mode (EDO) Byte Read Cycle



Remark 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

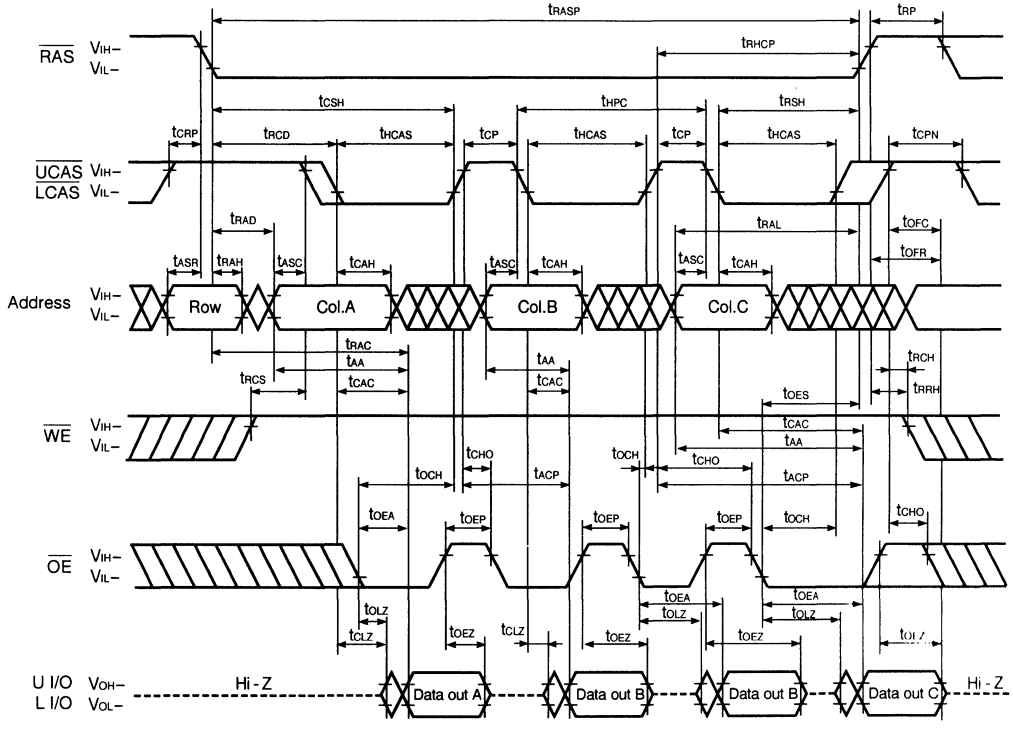
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)



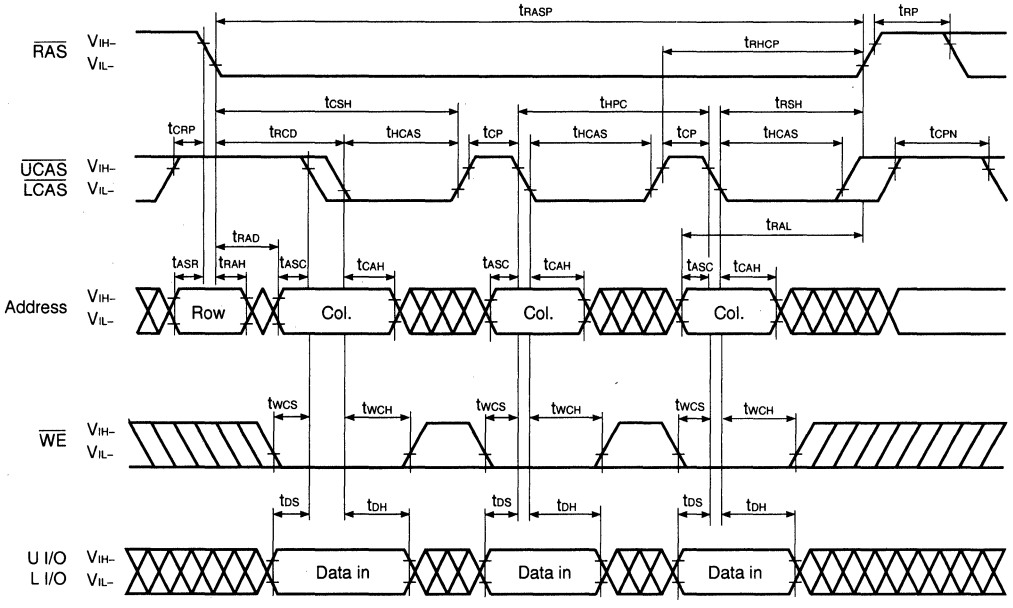
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

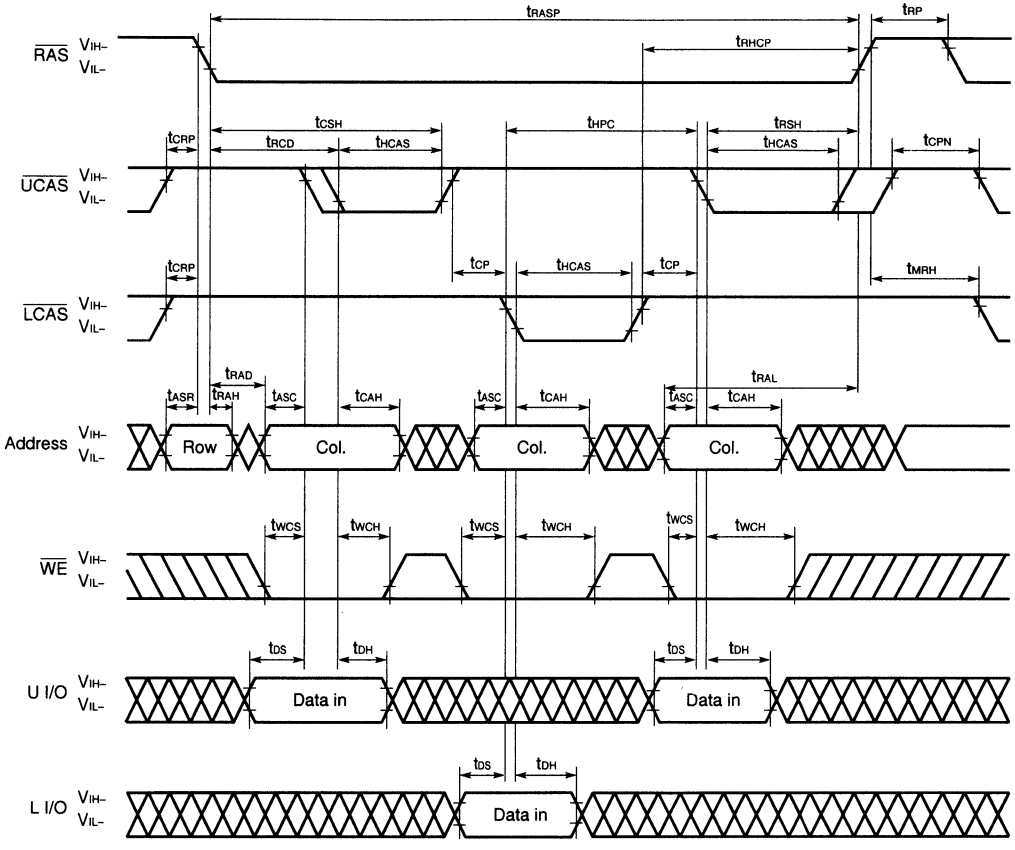
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

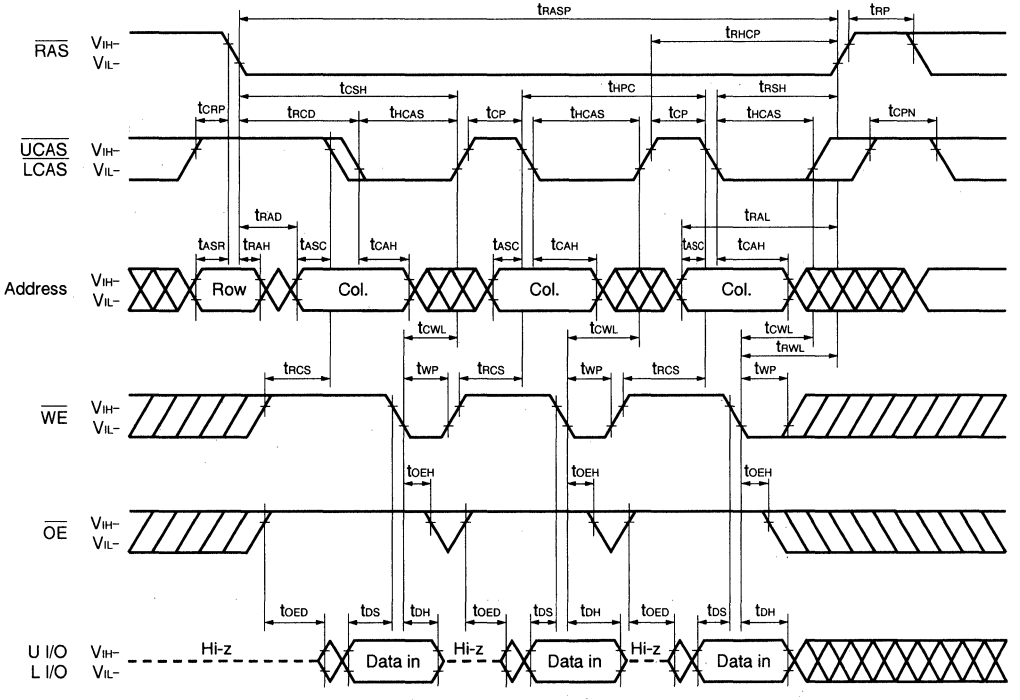
Hyper Page Mode (EDO) Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

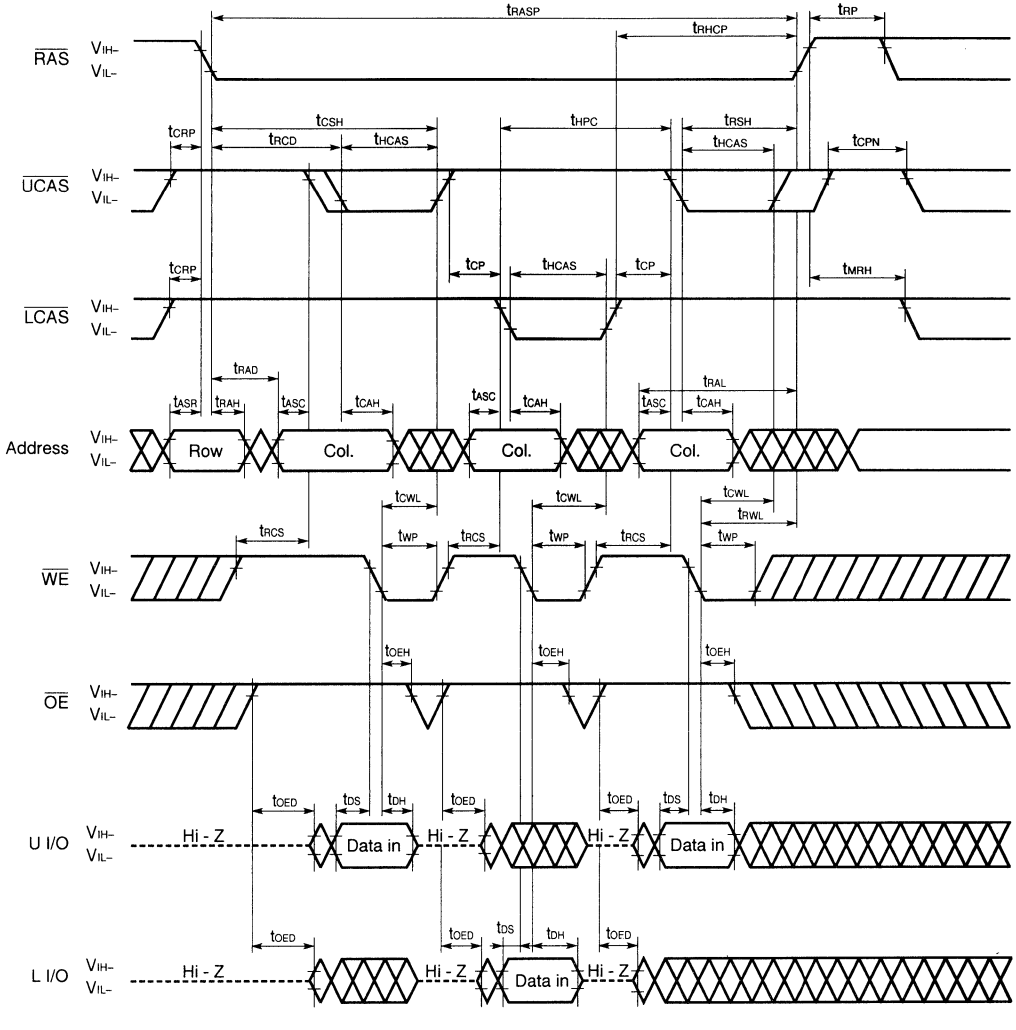
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Late Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

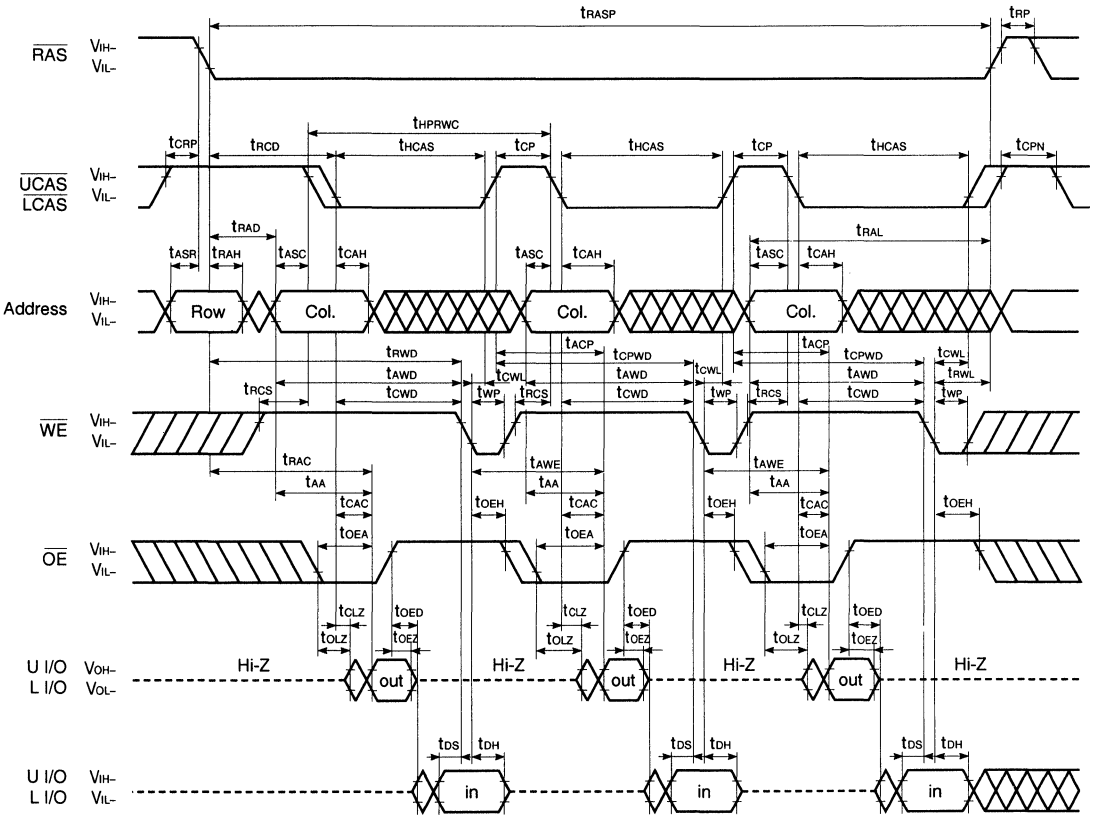
Hyper Page Mode (EDO) Byte Late Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

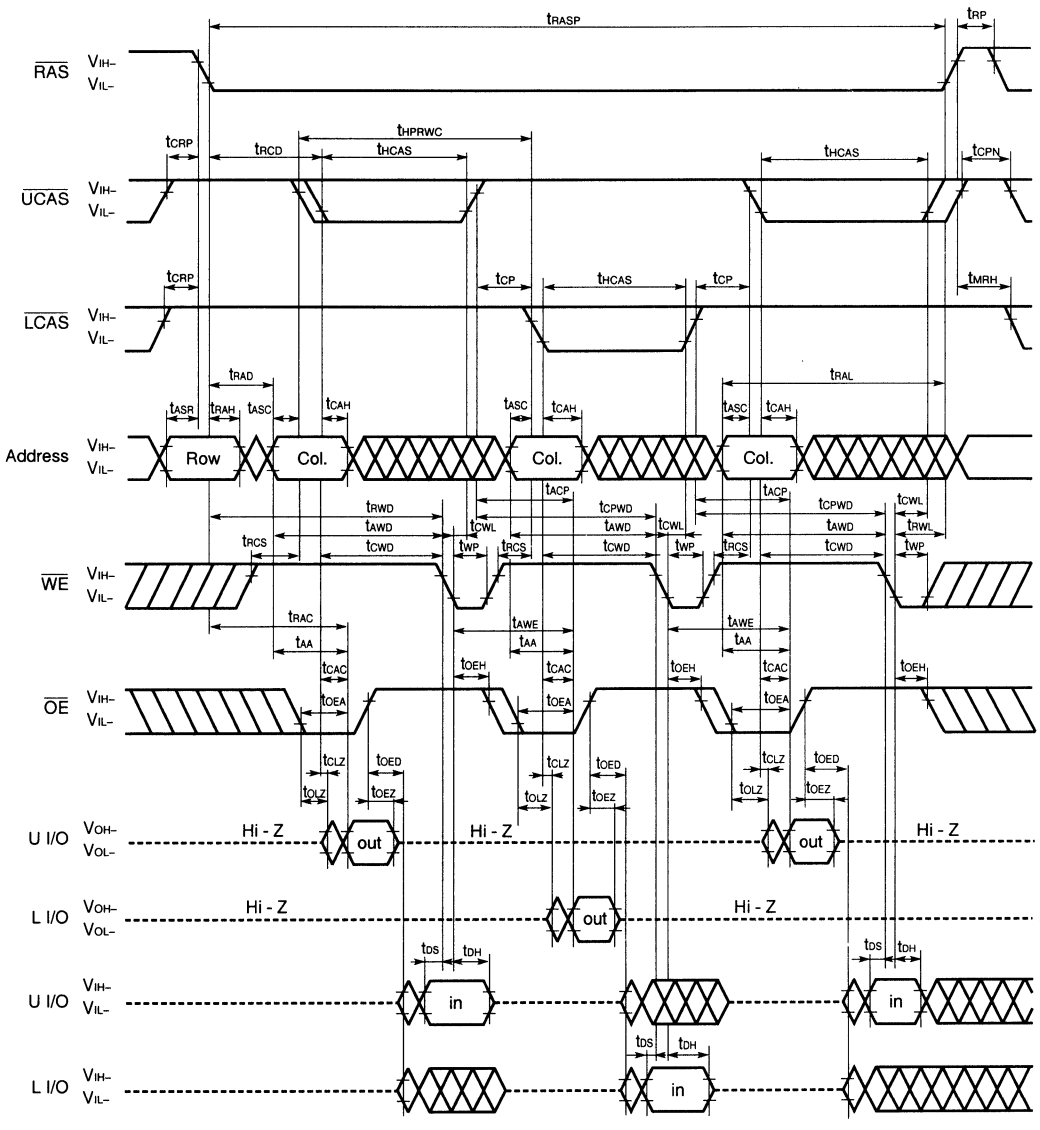
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read Modify Write Cycle



Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

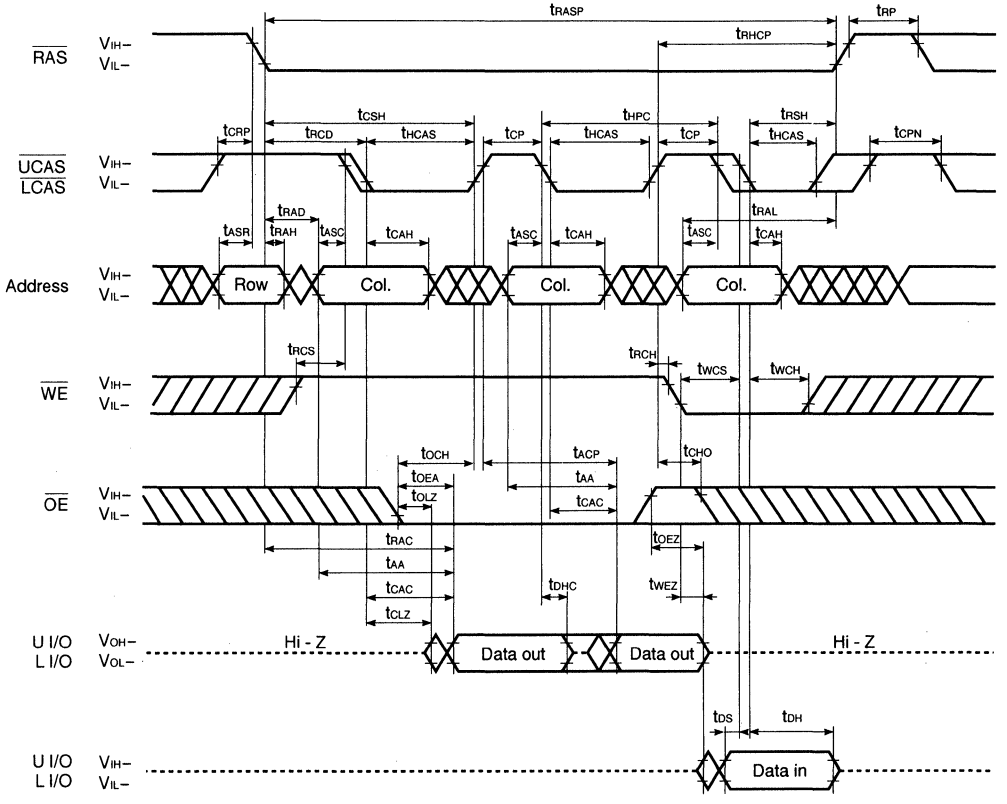
Hyper Page Mode (EDO) Byte Read Modify Write Cycle



Remarks 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

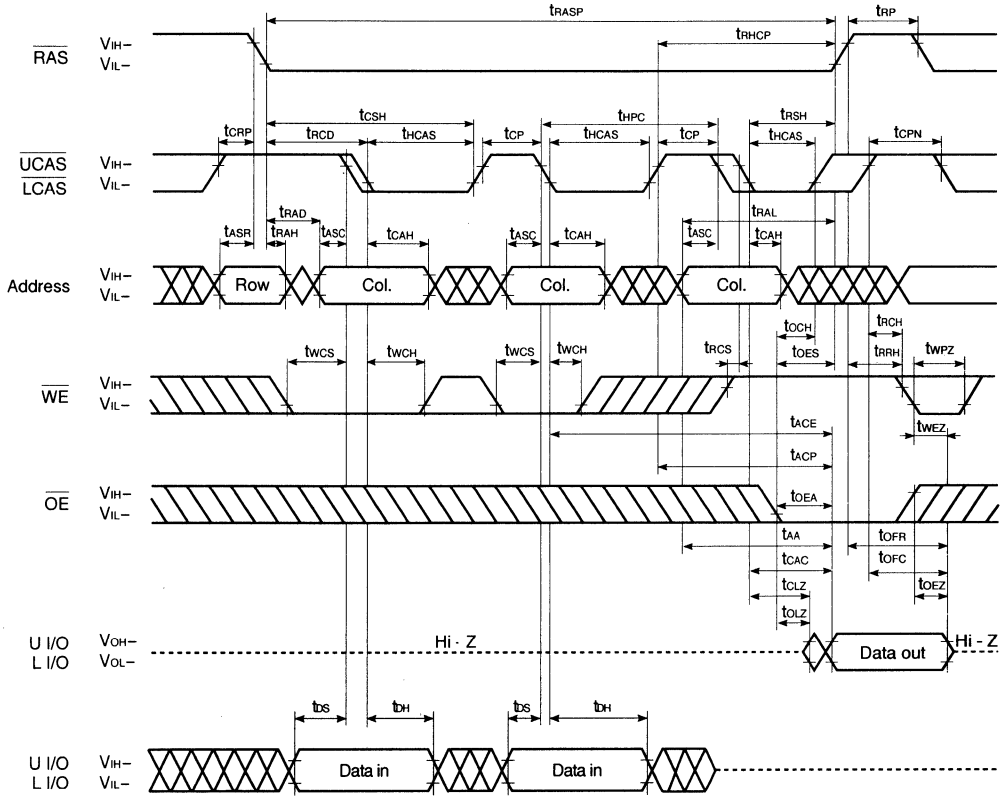
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Hyper Page Mode (EDO) Read and Write Cycle



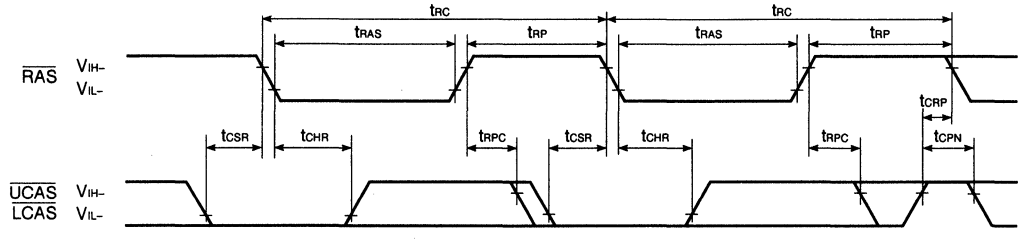
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode (EDO) Write and Read Cycle



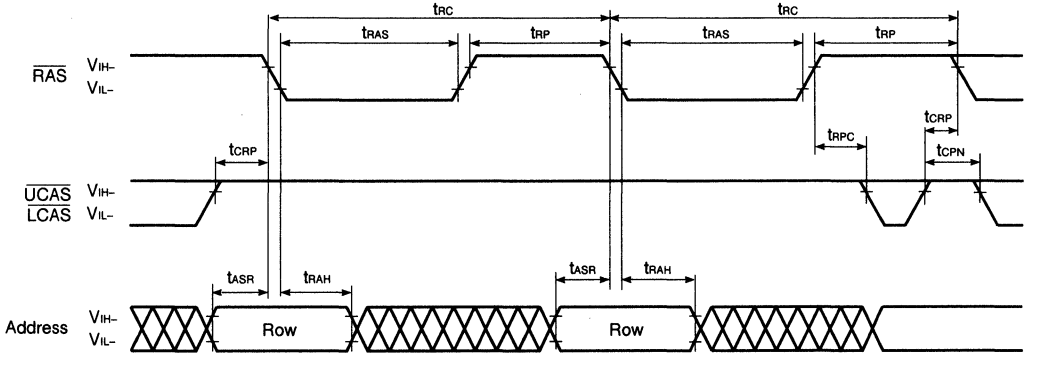
Remark In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



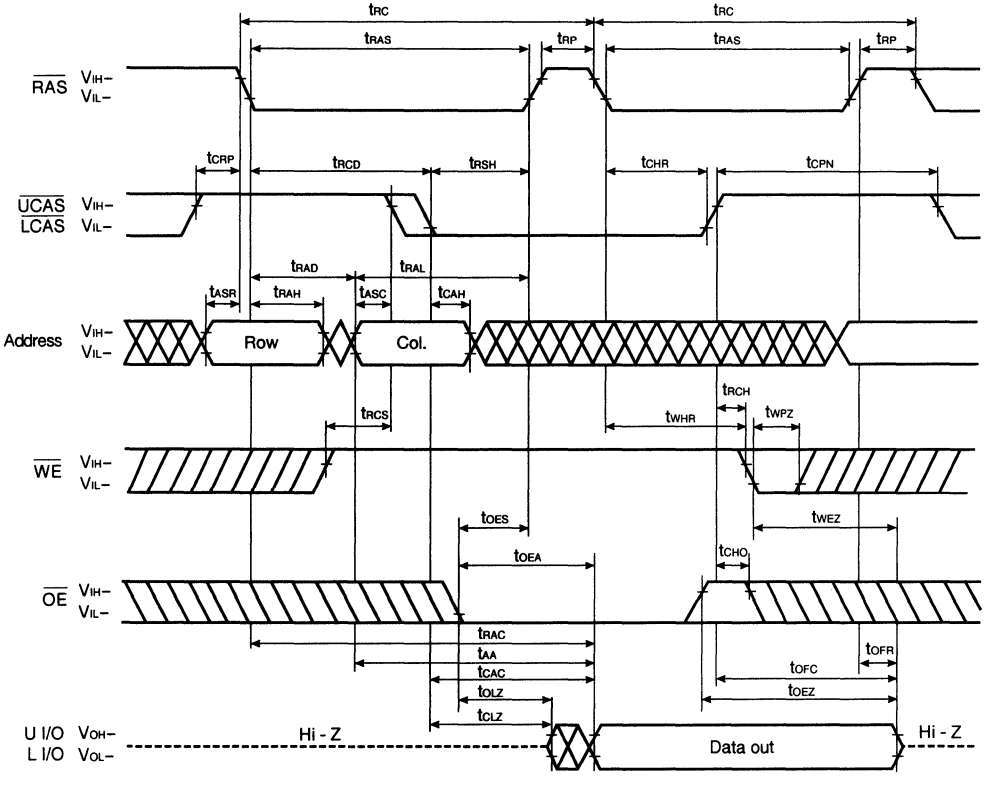
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

$\overline{\text{RAS}}$ Only Refresh Cycle

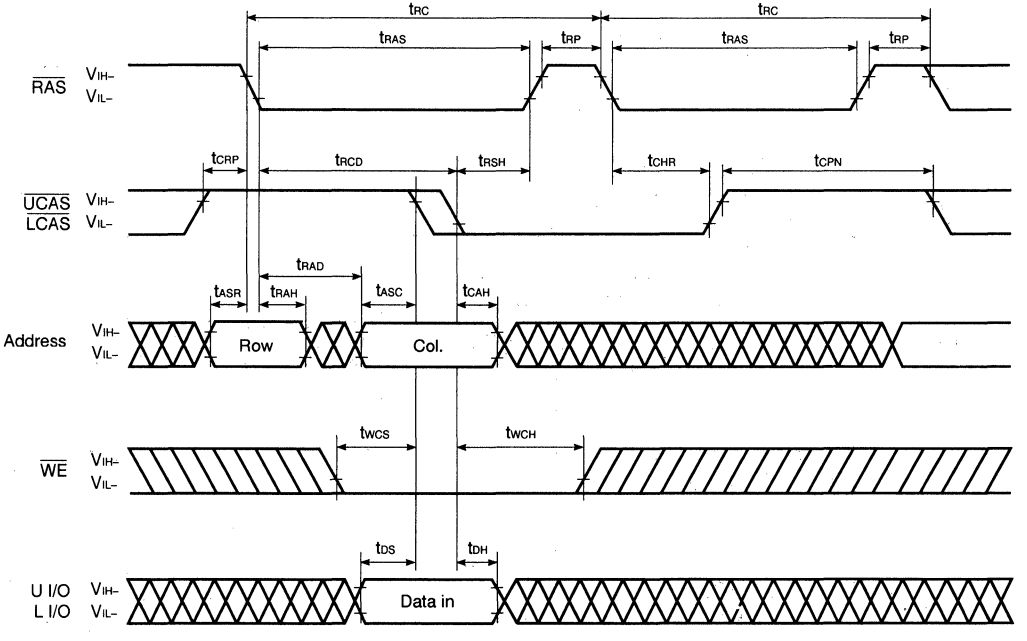


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



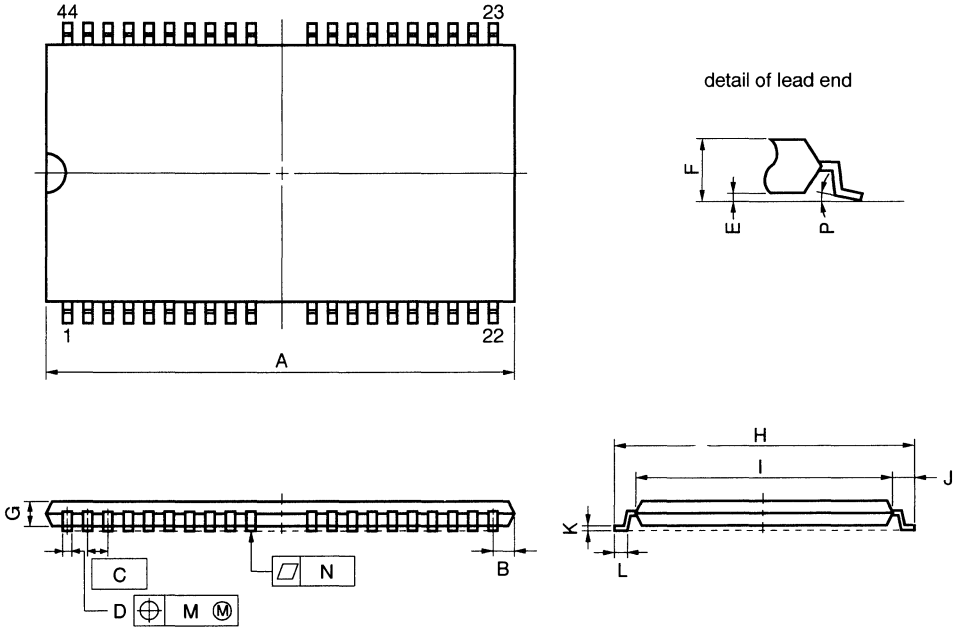
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



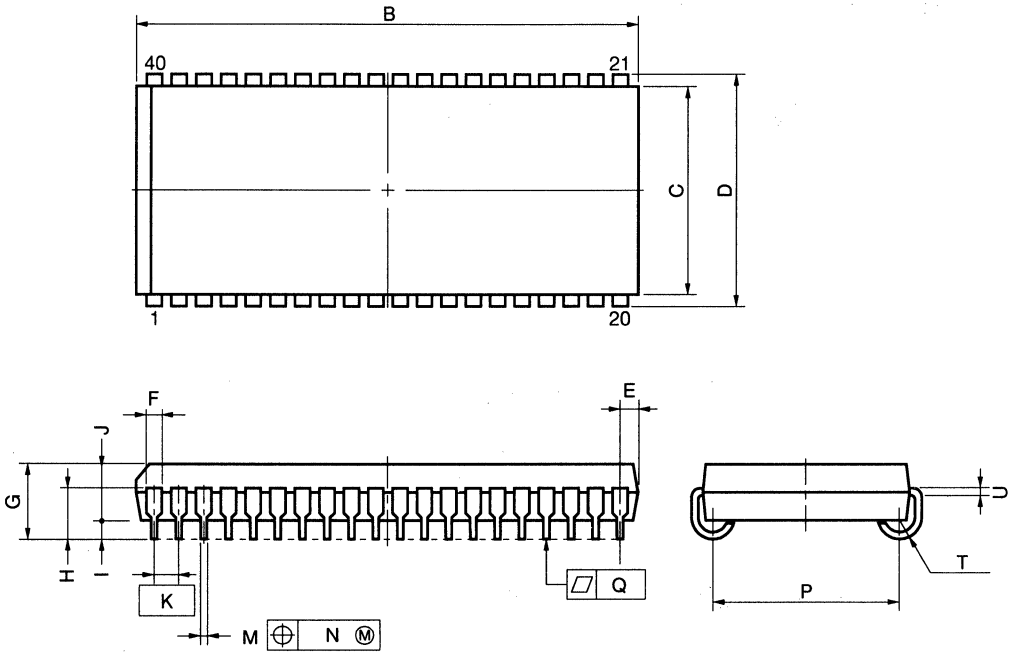
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S44G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P40LE-400A-2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD421165.

Types of Surface Mount Device

μPD421165G5: 44-pin plastic TSOP (II) (400 mil)
μPD421165LE: 40-pin plastic SOJ (400 mil)

[MEMO]

Fast Page Mode
64M Dynamic RAM

NEC

MOS INTEGRATED CIRCUIT

μPD4264400, 4265400

64 M-BIT DYNAMIC RAM
16 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μPD4264400, 4265400 are 16,777,216 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- 16,777,216 words by 4 bits organization
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD4264400-A50	360 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μPD4265400-A50	468 mW				
μPD4264400-A60	324 mW		60 ns	110 ns	40 ns
μPD4265400-A60	396 mW				
μPD4264400-A70	288 mW		70 ns	130 ns	45 ns
μPD4265400-A70	360 mW				
μPD4264400-A80	252 mW		80 ns	150 ns	50 ns
μPD4265400-A80	324 mW				

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

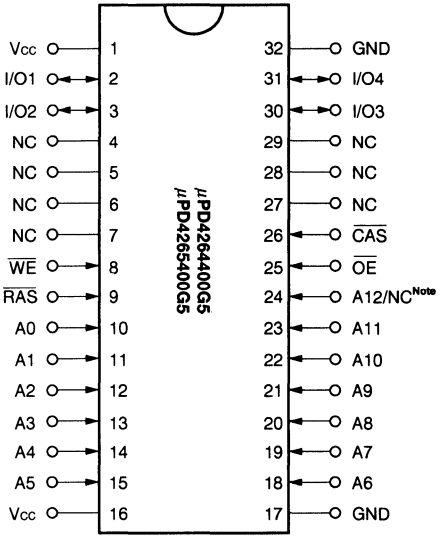
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264400	A0 - A12	A0 - A10	$\overline{RAS}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265400	A0 - A11	A0 - A11	$\overline{RAS}$ only refresh, Normal read/write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms

Ordering Information

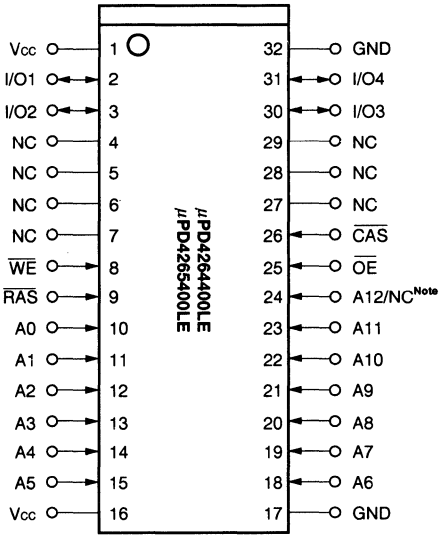
Part number	Access time (MAX.)	Package	Refresh
μPD4264400G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264400G5-A60	60 ns		
μPD4264400G5-A70	70 ns		
μPD4264400G5-A80	80 ns		
μPD4264400LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4264400LE-A60	60 ns		
μPD4264400LE-A70	70 ns		
μPD4264400LE-A80	80 ns		
μPD4265400G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	
μPD4265400G5-A60	60 ns		
μPD4265400G5-A70	70 ns		
μPD4265400G5-A80	80 ns		
μPD4265400LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4265400LE-A60	60 ns		
μPD4265400LE-A70	70 ns		
μPD4265400LE-A80	80 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12 ... μPD4264400
NC ... μPD4265400

A0 to A12	:	Address Inputs
I/O1 to I/O4	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264400, 4265400 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 24-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 16,777,216-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD4264400	A0-A12	13	11
μPD4265400	A0-A11	12	12

Electrical Specifications (Preliminary)

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264400]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		100	mA	1, 2, 3
		$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		90		
		I_O = 0 mA	t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		70		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$	t_{RAC} = 50 ns		100	mA	1, 2, 3, 4
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90		
			t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		70		
Operating current	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		80	mA	1, 2, 5
(Fast page mode)		$t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		70		
			t_{RAC} = 70 ns		60		
			t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1, 2
refresh current		$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265400]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1, 2, 3
		$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$	t_{RAC} = 50 ns		130	mA	1, 2, 3 ,4
		$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		110		
			t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
Operating current	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		80	mA	1, 2, 5
(Fast page mode)		$t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		70		
			t_{RAC} = 70 ns		60		
			t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		130	mA	1, 2
refresh current		$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		110		
		I_O = 0 mA	t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

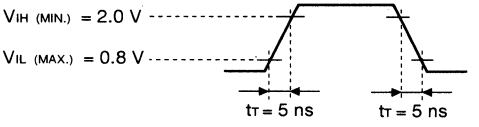
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

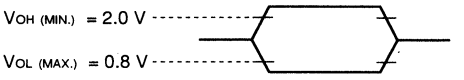
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

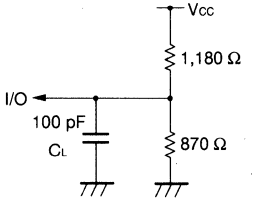
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tRC	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	tRP	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	tCPN	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	tCSH	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	37	20	45	20	52	25	60	ns	1
$\overline{RAS}$ to column address delay time	tRAD	13	25	15	30	15	35	17	40	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	–	5	–	5	–	5	–	ns	2
Row address setup time	tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time	tRAH	8	–	10	–	10	–	12	–	ns	
Column address setup time	tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time	tCAH	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	tOED	10	–	13	–	15	–	15	–	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	
Refresh time	tREF	–	64	–	64	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	128	–	153	–	175	–	195	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	–	38	–	43	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	45	–	53	–	60	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

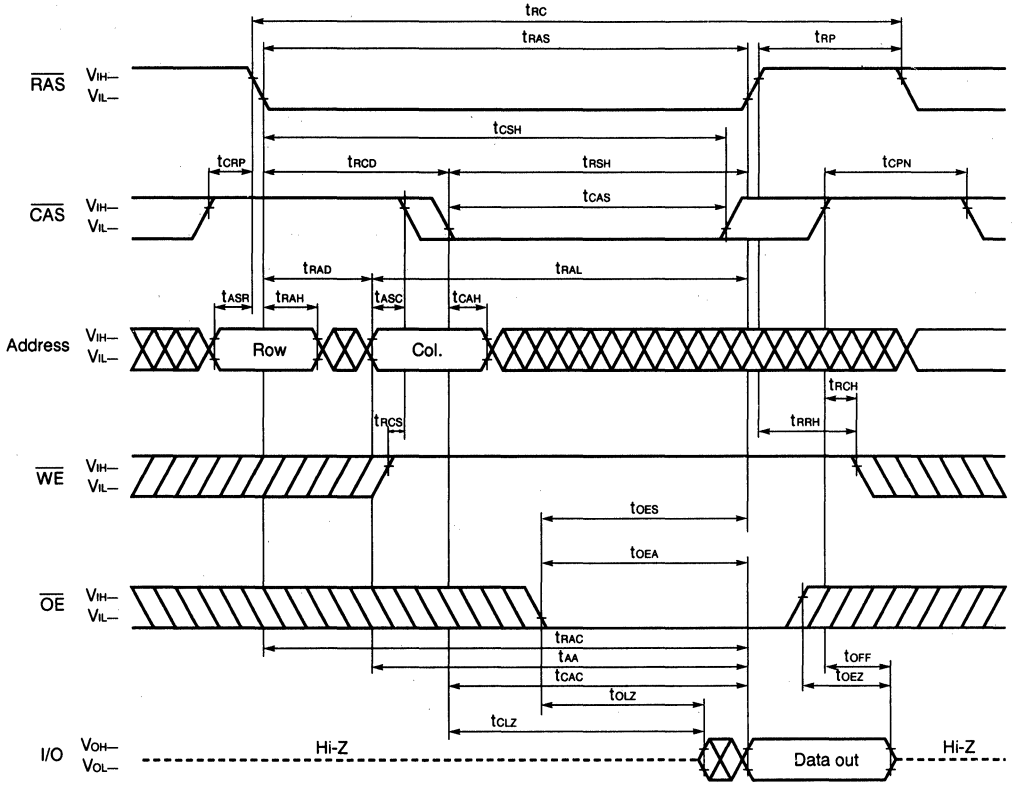
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

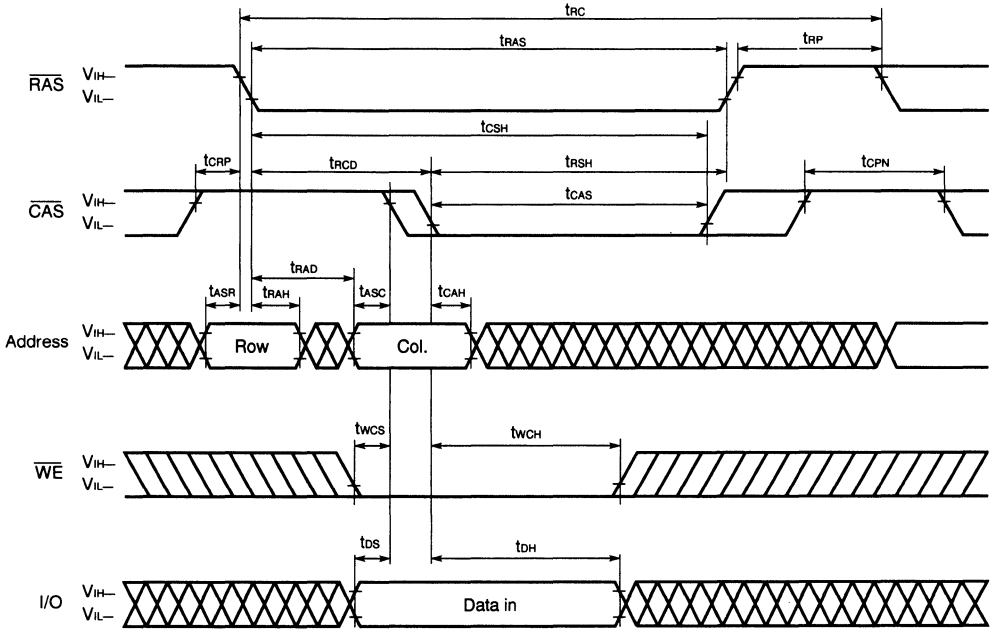
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

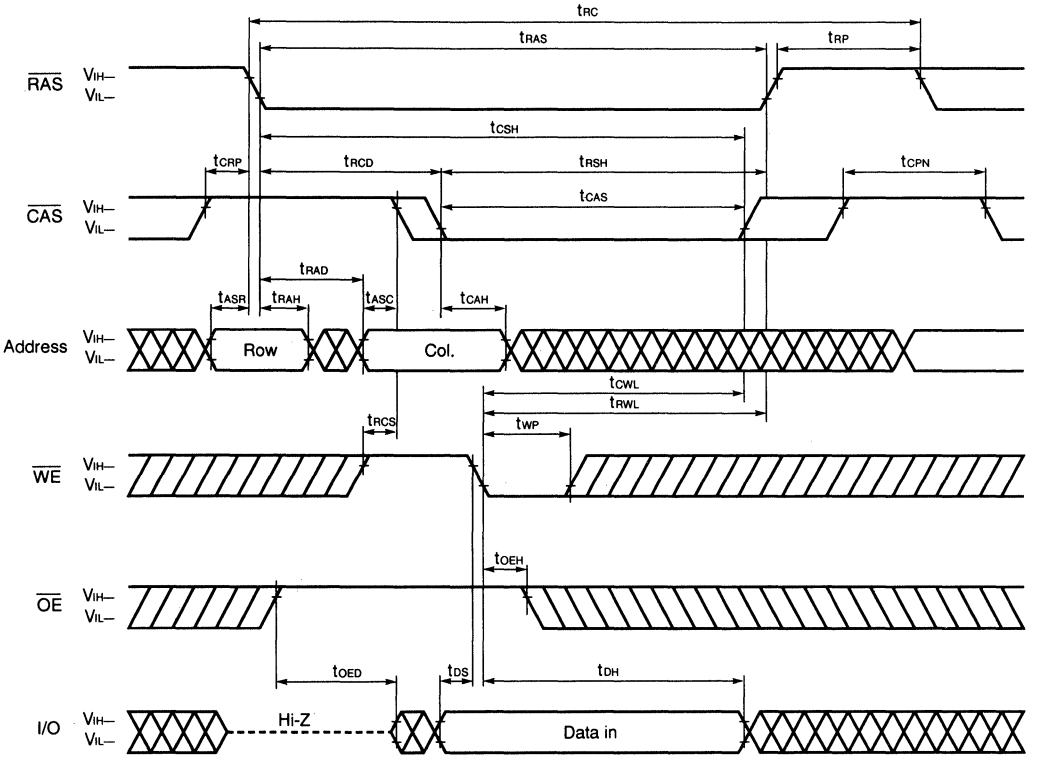

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

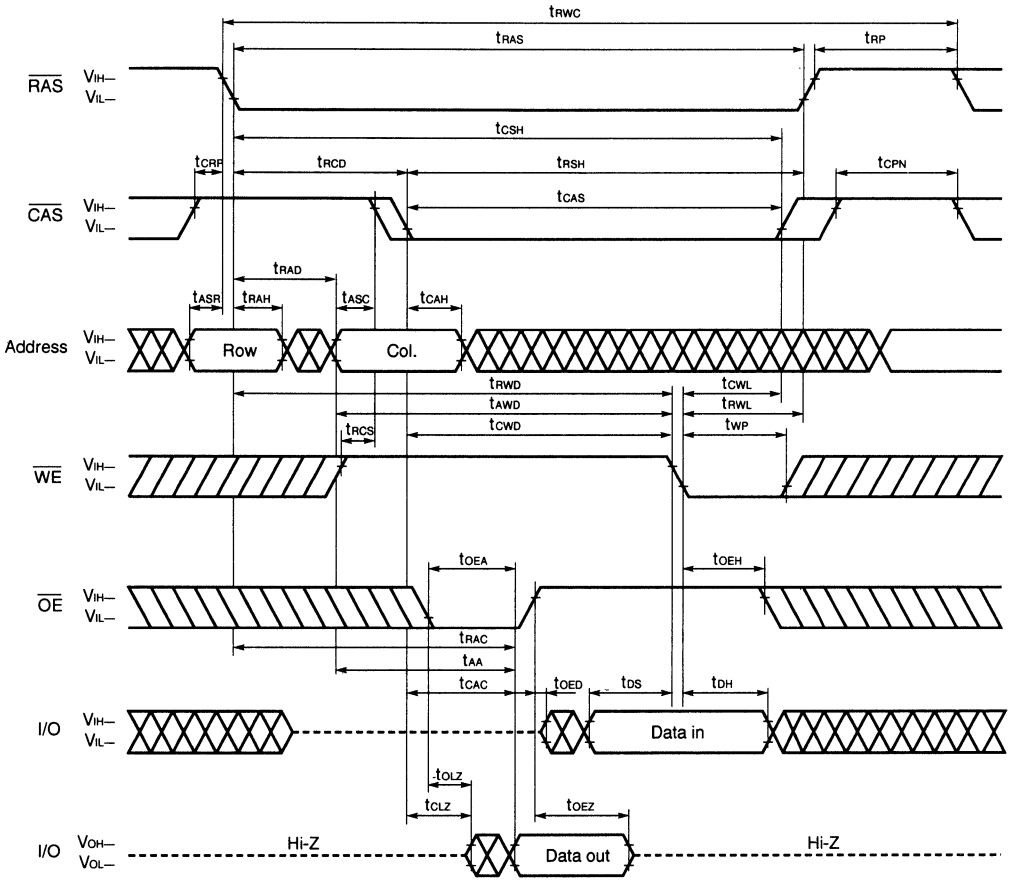


Remark $\overline{OE}$: Don't care

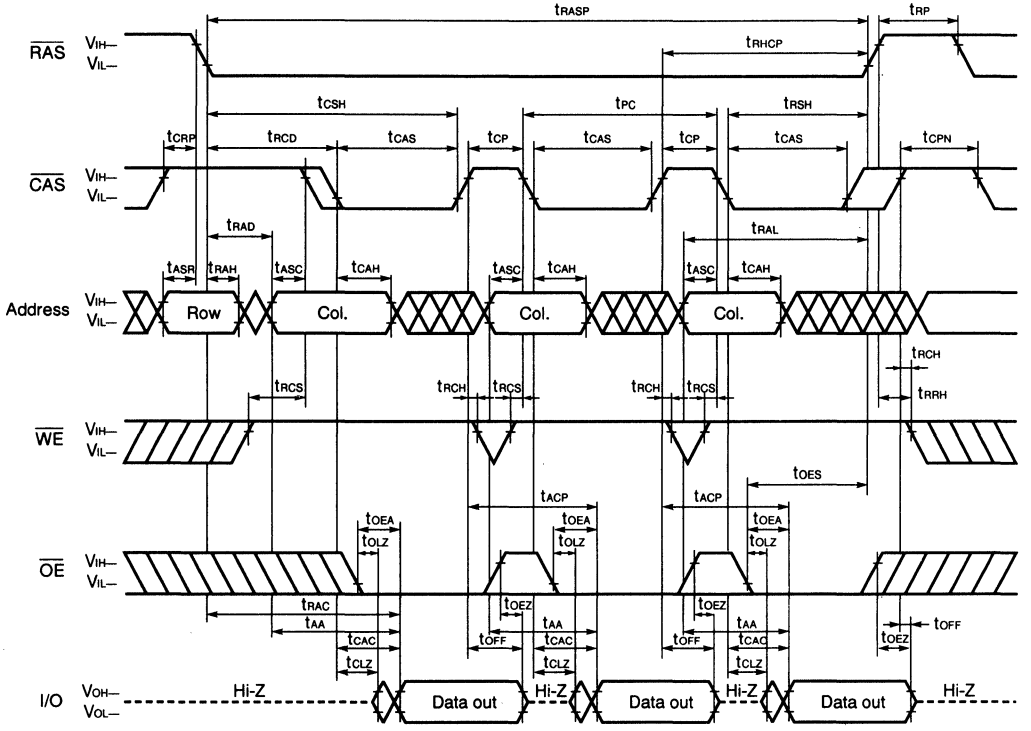
Late Write Cycle



Read Modify Write Cycle

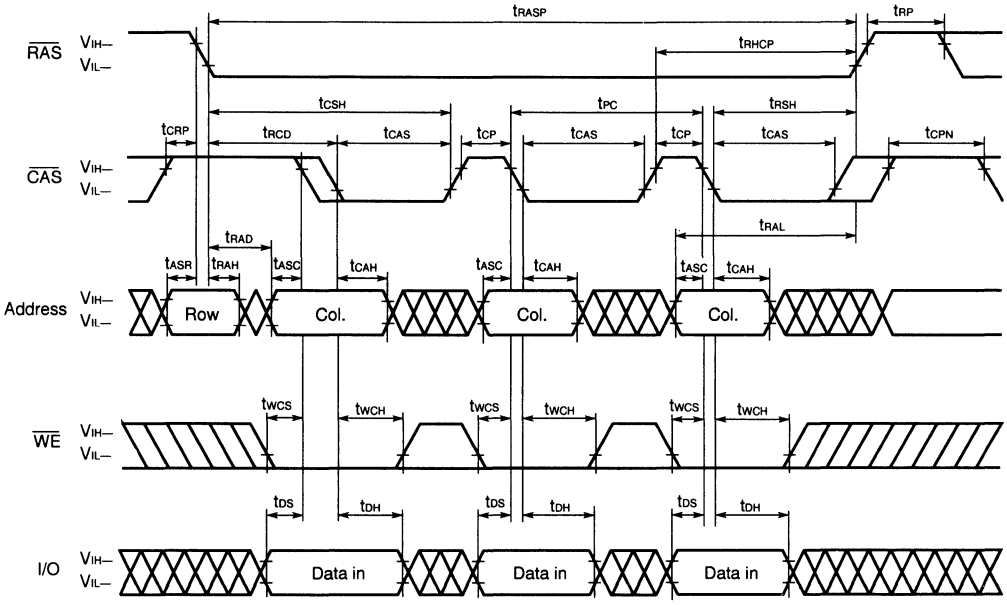


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

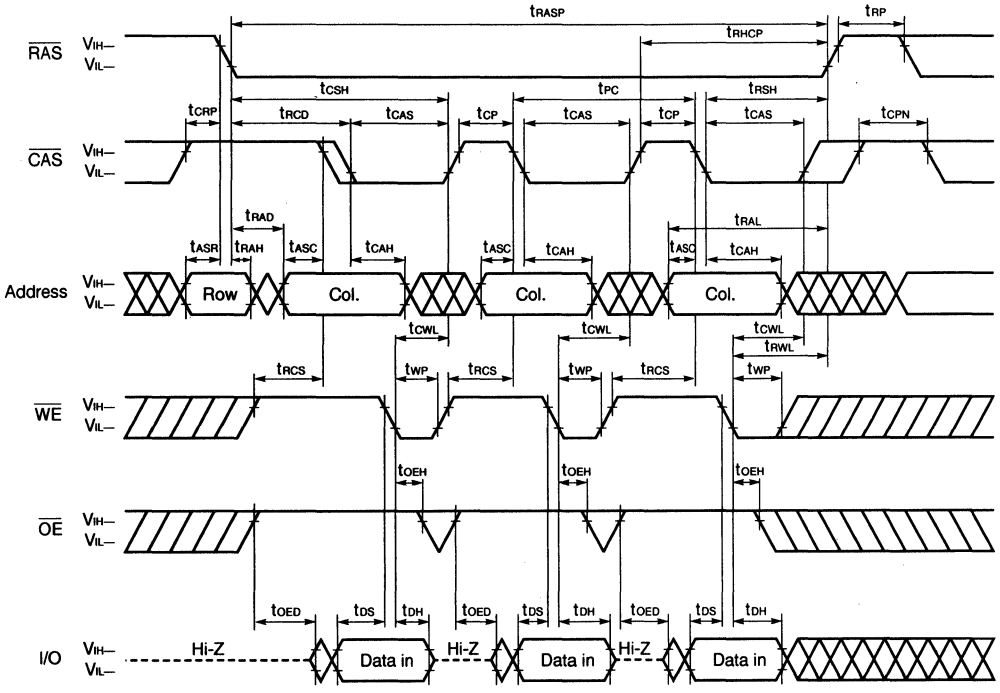
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

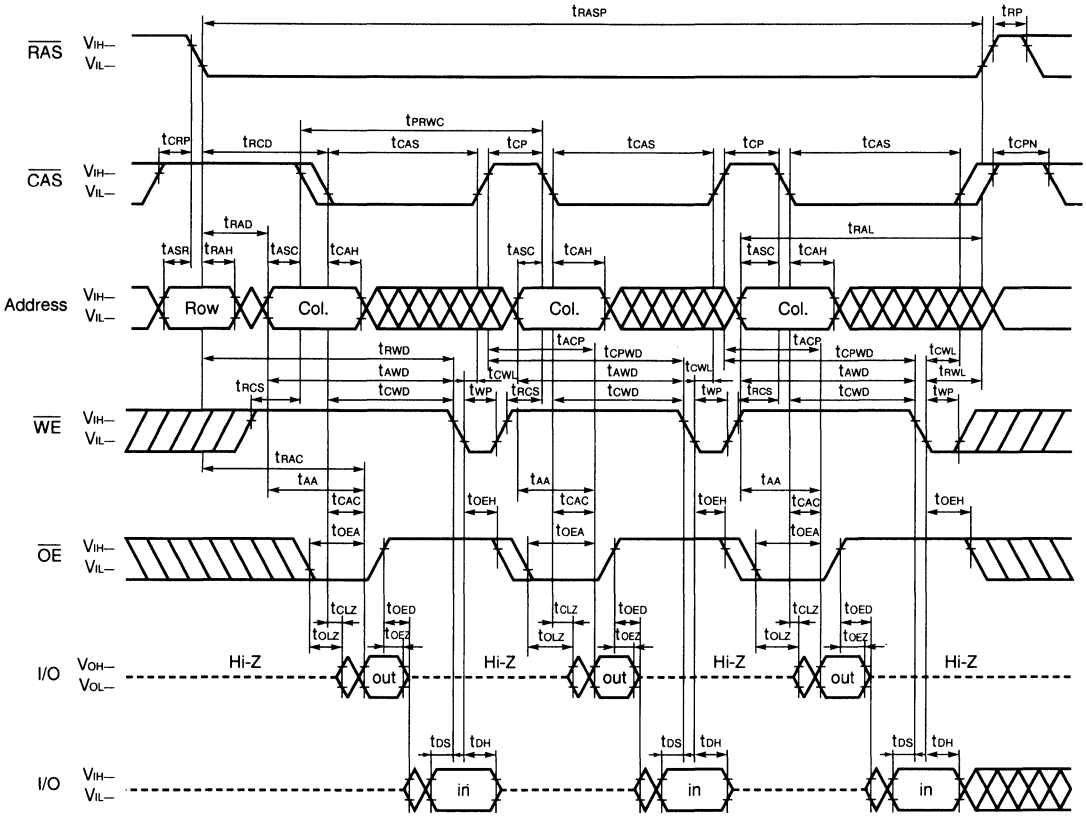
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



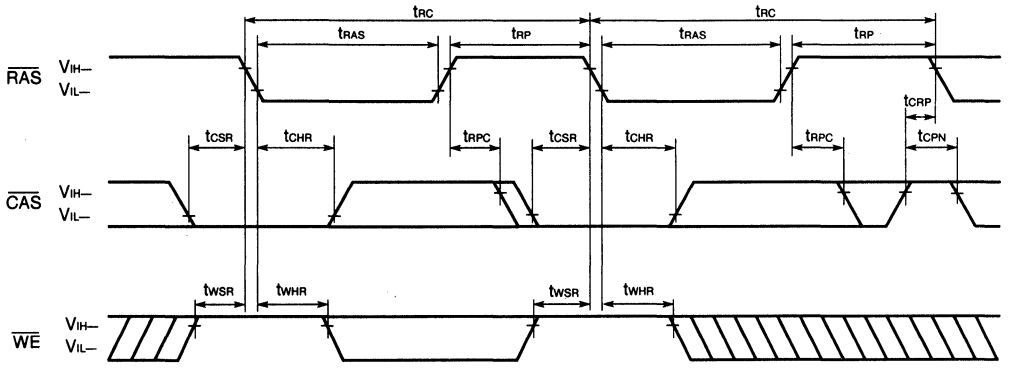
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



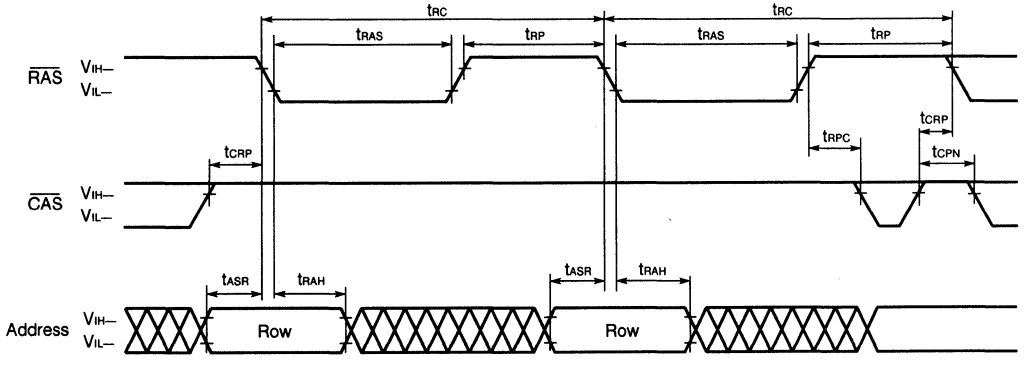
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



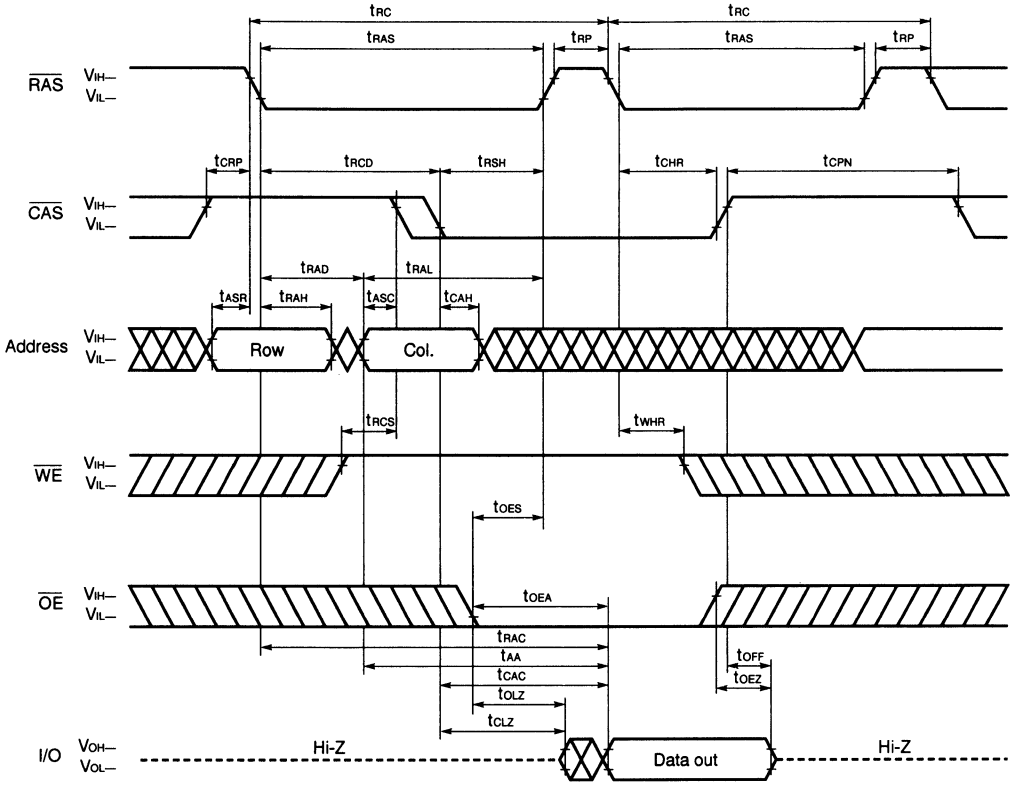
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

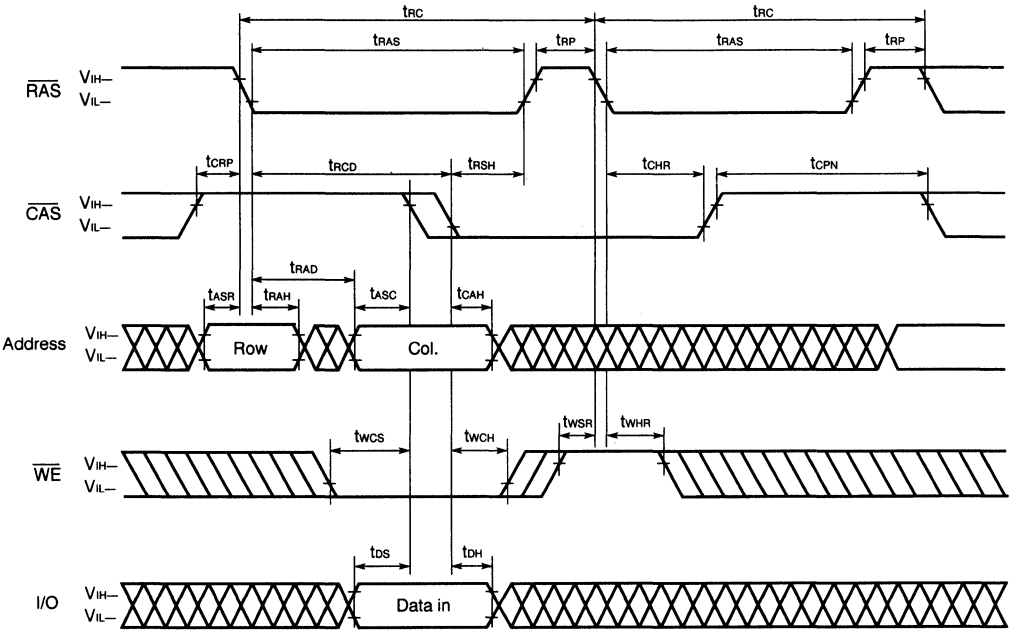


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



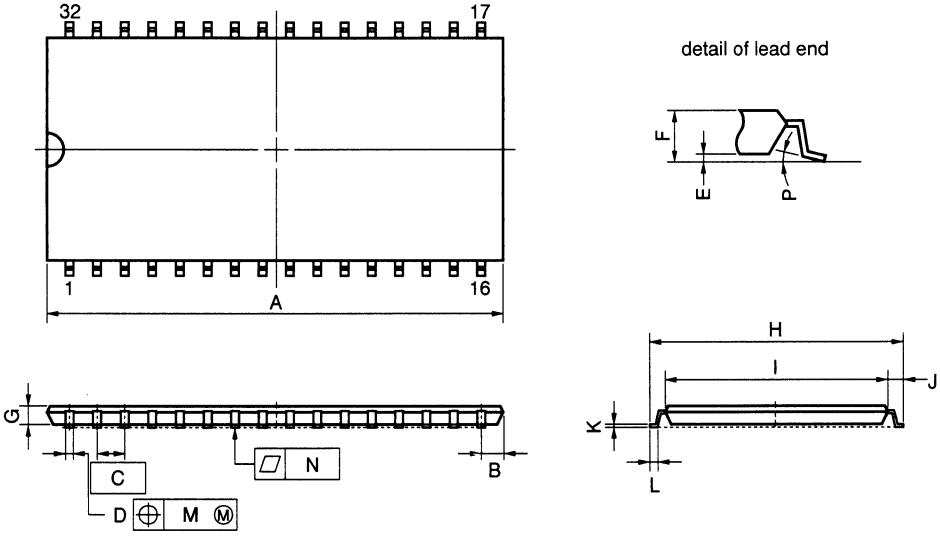
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



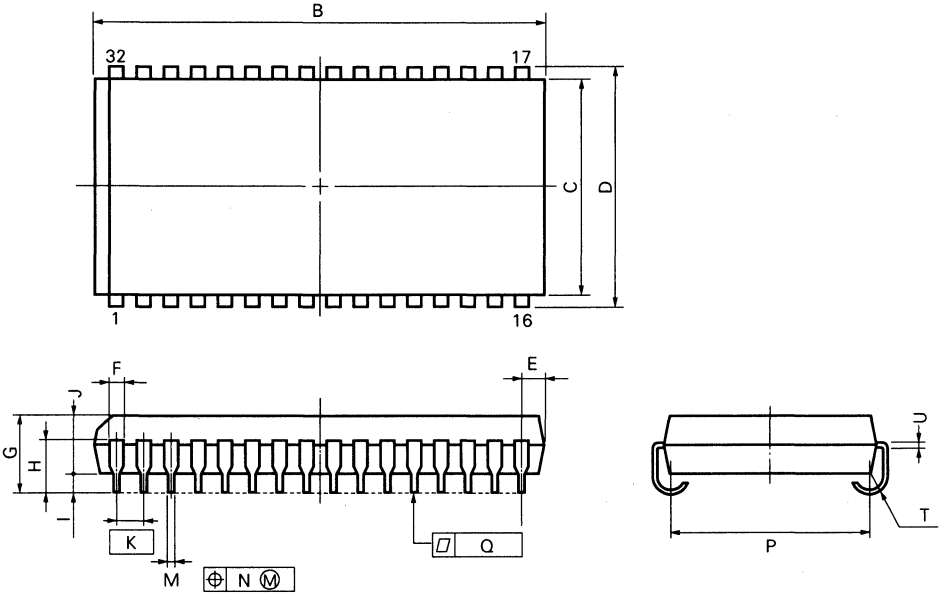
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



P32LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NEC

MOS INTEGRATED CIRCUIT

μPD4264800, 4265800

64 M-BIT DYNAMIC RAM
8 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μPD4264800, 4265800 are 8,388,608 words by 8 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- 8,388,608 words by 8 bits organization
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD4264800-A50	378 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μPD4265800-A50	486 mW				
μPD4264800-A60	342 mW		60 ns	110 ns	40 ns
μPD4265800-A60	414 mW				
μPD4264800-A70	306 mW		70 ns	130 ns	45 ns
μPD4265800-A70	378 mW				
μPD4264800-A80	270 mW		80 ns	150 ns	50 ns
μPD4265800-A80	342 mW				

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

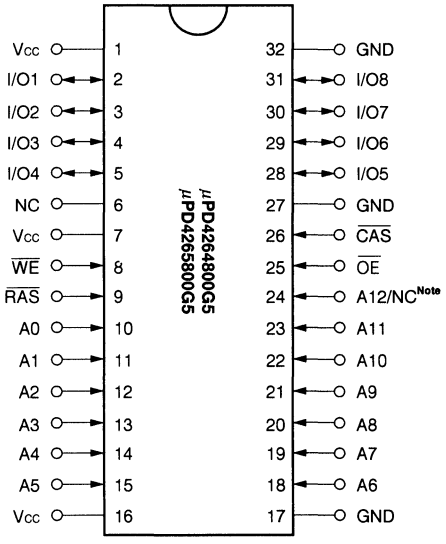
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264800	A0 - A12	A0 - A9	$\overline{RAS}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265800	A0 - A11	A0 - A10	$\overline{RAS}$ only refresh, Normal read/write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms

Ordering Information

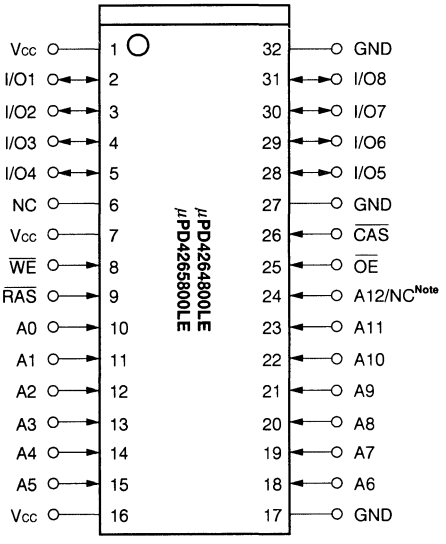
Part number	Access time (MAX.)	Package	Refresh
μPD4264800G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264800G5-A60	60 ns		
μPD4264800G5-A70	70 ns		
μPD4264800G5-A80	80 ns		
μPD4264800LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4264800LE-A60	60 ns		
μPD4264800LE-A70	70 ns		
μPD4264800LE-A80	80 ns		
μPD4265800G5-A50	50 ns	32-pin plastic TSOP (II) (400 mil)	
μPD4265800G5-A60	60 ns		
μPD4265800G5-A70	70 ns		
μPD4265800G5-A80	80 ns		
μPD4265800LE-A50	50 ns	32-pin plastic SOJ (400 mil)	
μPD4265800LE-A60	60 ns		
μPD4265800LE-A70	70 ns		
μPD4265800LE-A80	80 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12 ... μPD4264800
NC ... μPD4265800

A0 to A12 : Address Inputs
I/O1 to I/O8 : Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Input/Output Pin Functions

The μPD4264800, 4265800 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 23-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD4264800	A0-A12	13	10
μPD4265800	A0-A11	12	11

Electrical Specifications (Preliminary)

- All voltages are referenced to GND.
- After power up($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264800]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 50 ns		105	mA	1, 2, 3
		t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		95		
		I_O = 0 mA	t_{RAC} = 70 ns		85		
			t_{RAC} = 80 ns		75		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$	t_{RAC} = 50 ns		105	mA	1, 2, 3 ,4
		t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		95		
			t_{RAC} = 70 ns		85		
			t_{RAC} = 80 ns		75		
Operating current	I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 50 ns		85	mA	1, 2, 5
(Fast page mode)		t_{PC} = $t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		75		
			t_{RAC} = 70 ns		65		
			t_{RAC} = 80 ns		55		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 50 ns		135	mA	1, 2
refresh current		t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
			t_{RAC} = 80 ns		95		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265800]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 50 ns		135	mA	1, 2, 3
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
			t_{RAC} = 80 ns		95		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns		135	mA	1, 2, 3, 4
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		115		
			t_{RAC} = 70 ns		105		
			t_{RAC} = 80 ns		95		
Operating current	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ cycling	t_{RAC} = 50 ns		85	mA	1, 2, 5
(Fast page mode)		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		75		
			t_{RAC} = 70 ns		65		
			t_{RAC} = 80 ns		55		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 50 ns		135	mA	1, 2
refresh current		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
			t_{RAC} = 80 ns		95		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ V_{IL} (MAX.) and $\overline{CAS}$ ≥ V_{IH} (MIN.).

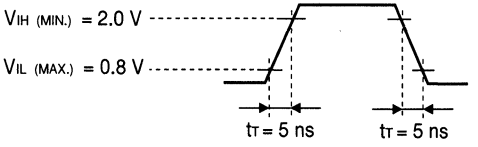
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

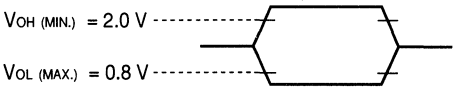
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

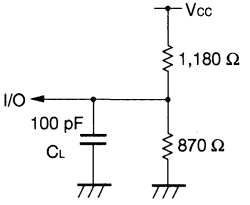
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tRC	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	tRP	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	tCPN	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	tCSH	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	37	20	45	20	52	25	60	ns	1
$\overline{RAS}$ to column address delay time	tRAD	13	25	15	30	15	35	17	40	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	–	5	–	5	–	5	–	ns	2
Row address setup time	tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time	tRAH	8	–	10	–	10	–	12	–	ns	
Column address setup time	tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time	tCAH	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	tOED	10	–	13	–	15	–	15	–	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	
Refresh time	tREF	–	64	–	64	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	128	–	153	–	175	–	195	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	–	38	–	43	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	45	–	53	–	60	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

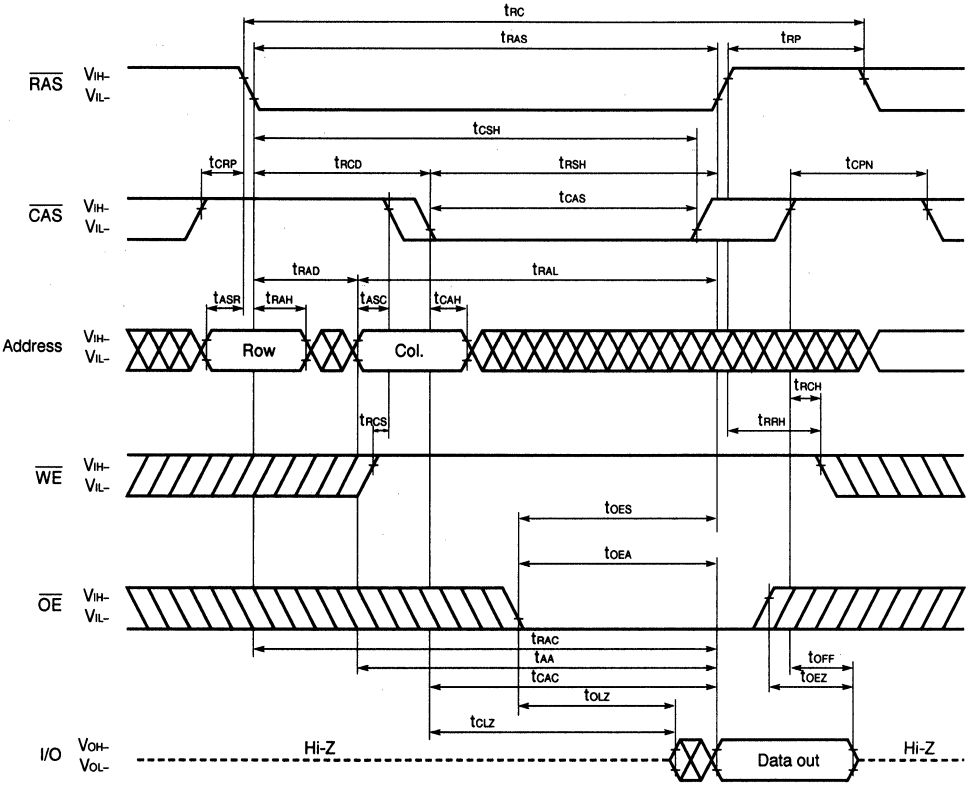
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

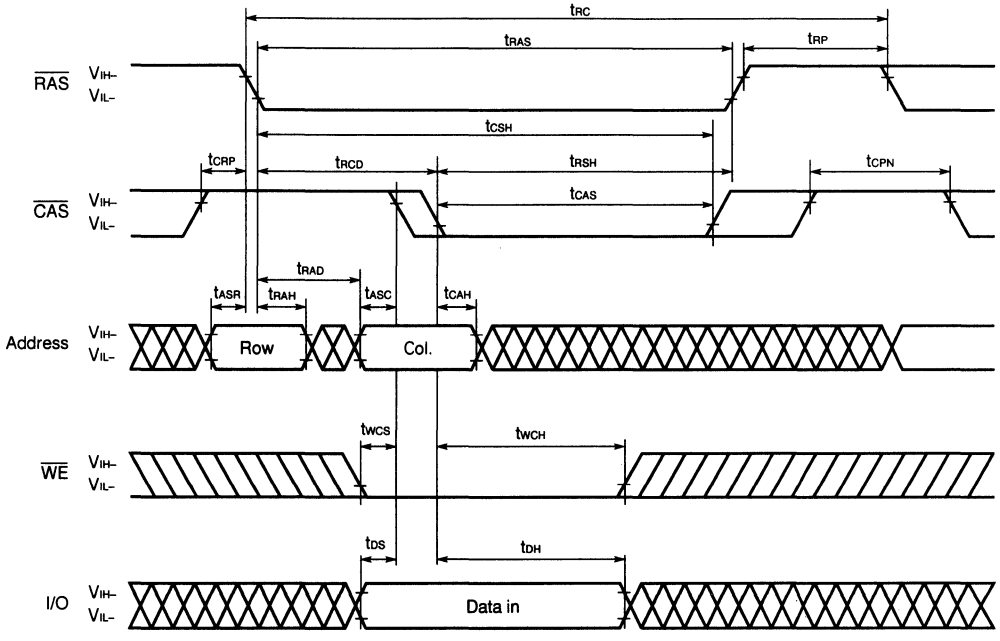
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

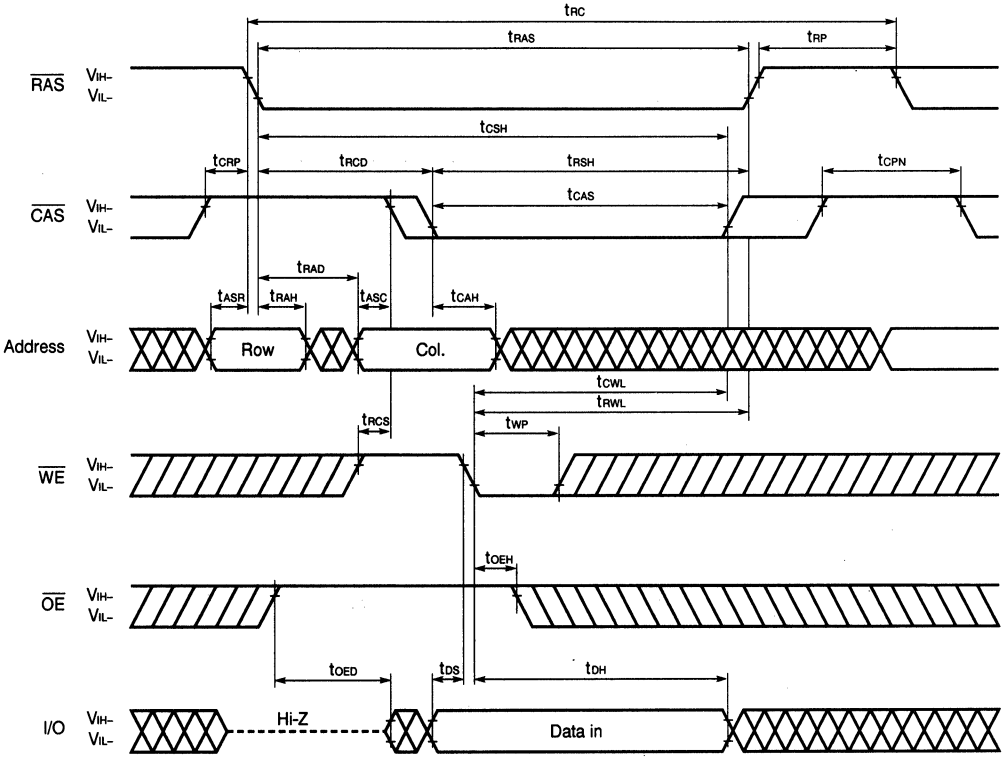

tRC
tRAS
tRP
RAS
VIH-
VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH-
VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

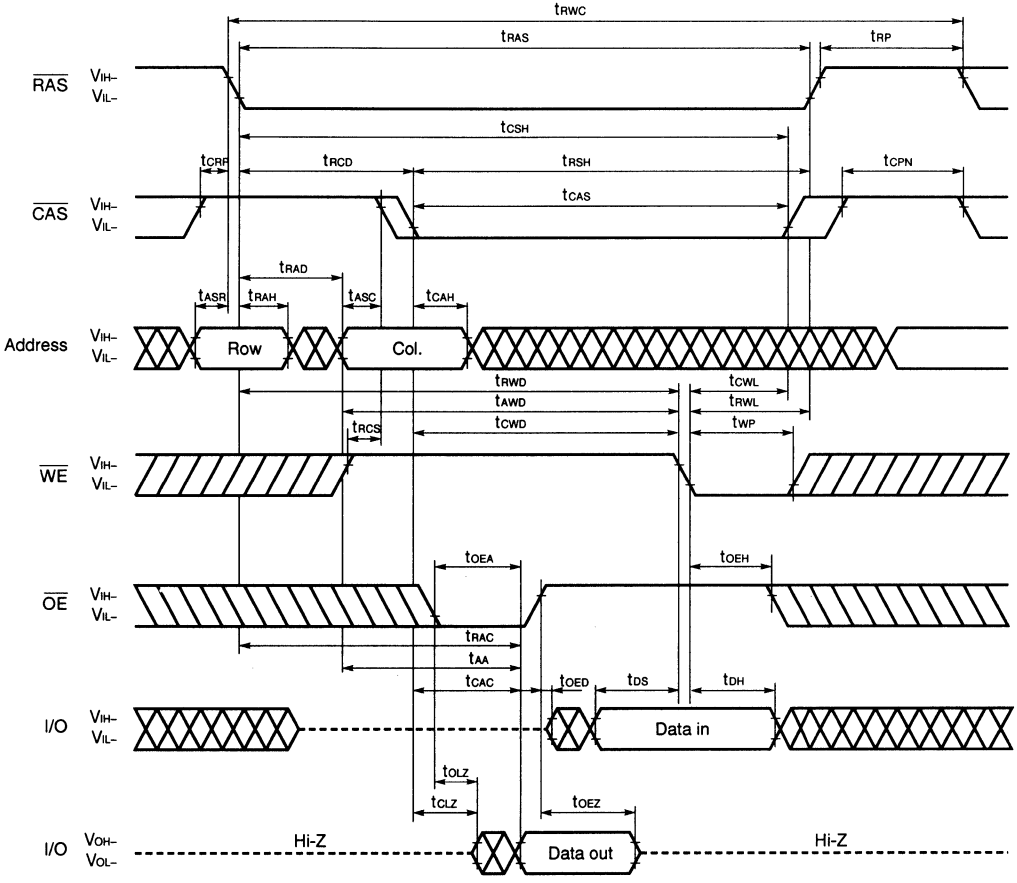


Remark $\overline{OE}$: Don't care

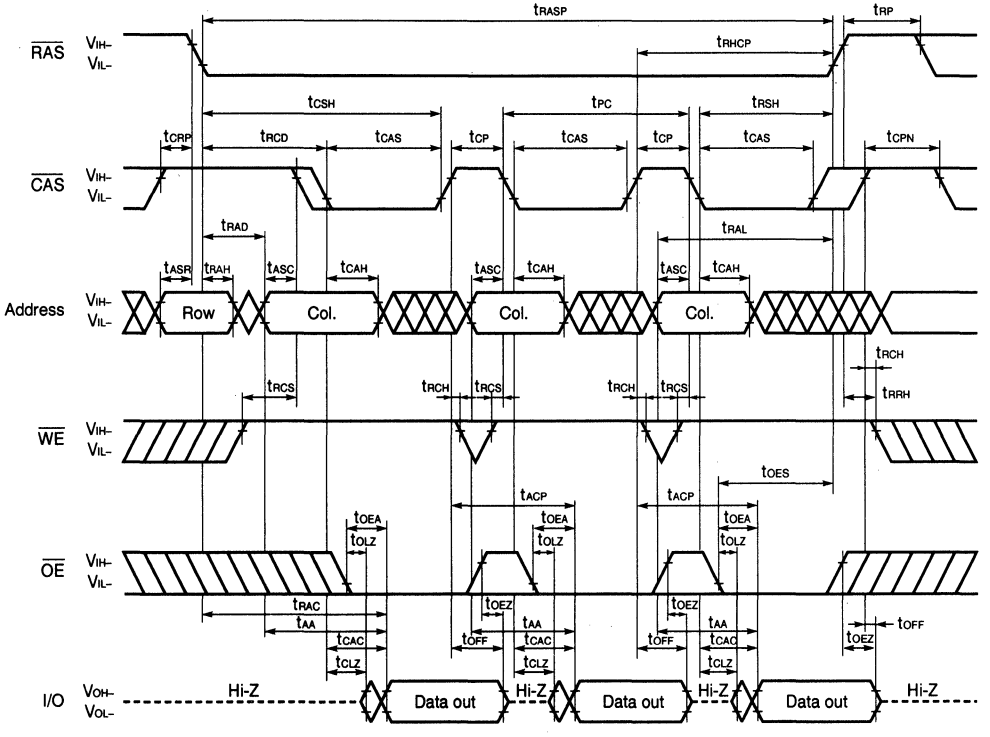
Late Write Cycle



Read Modify Write Cycle

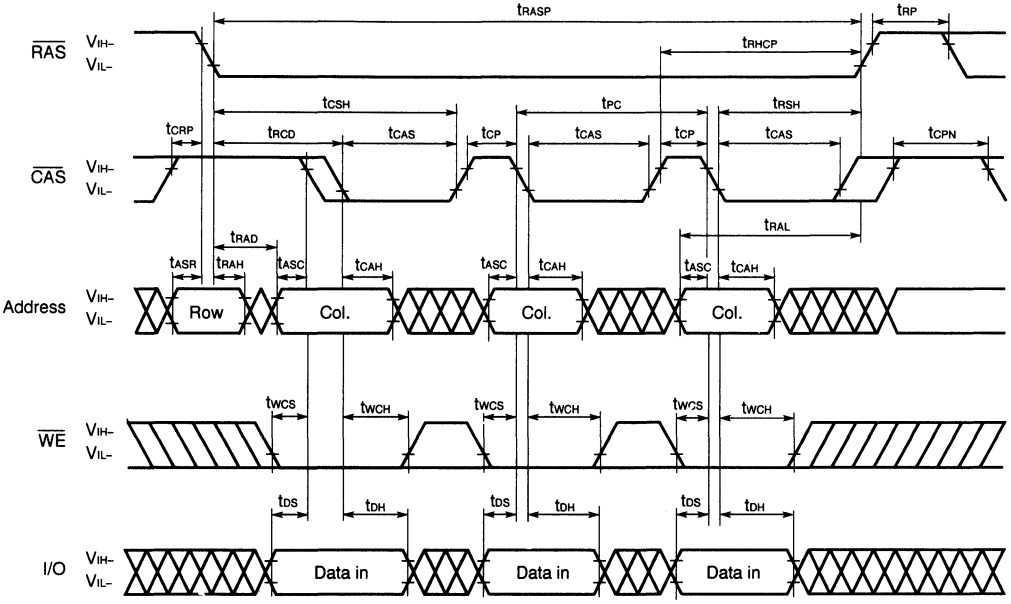


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

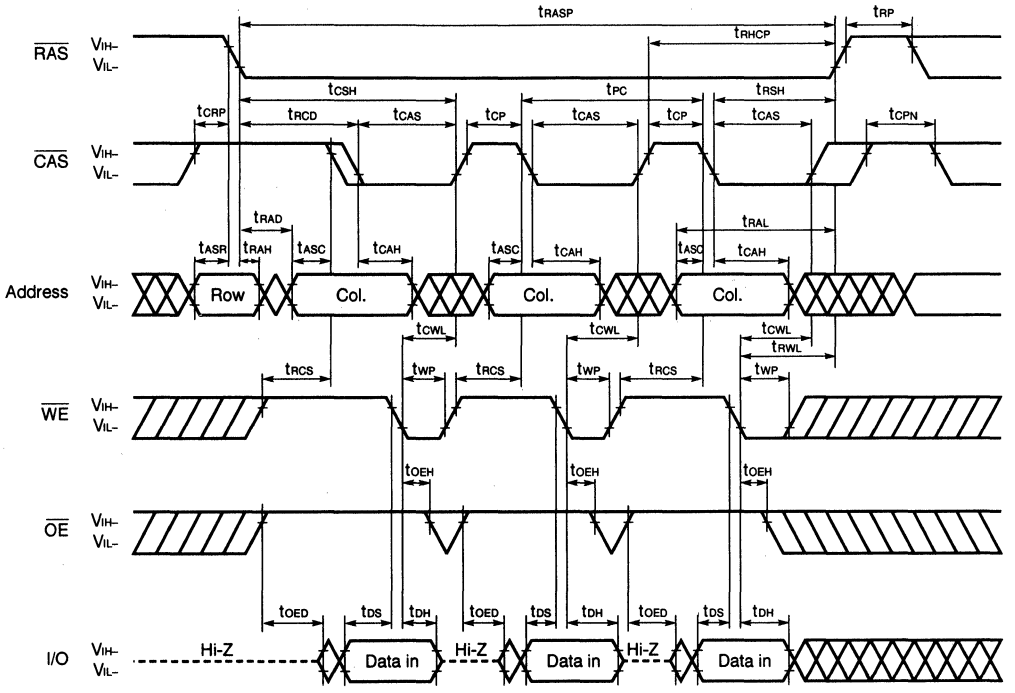
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

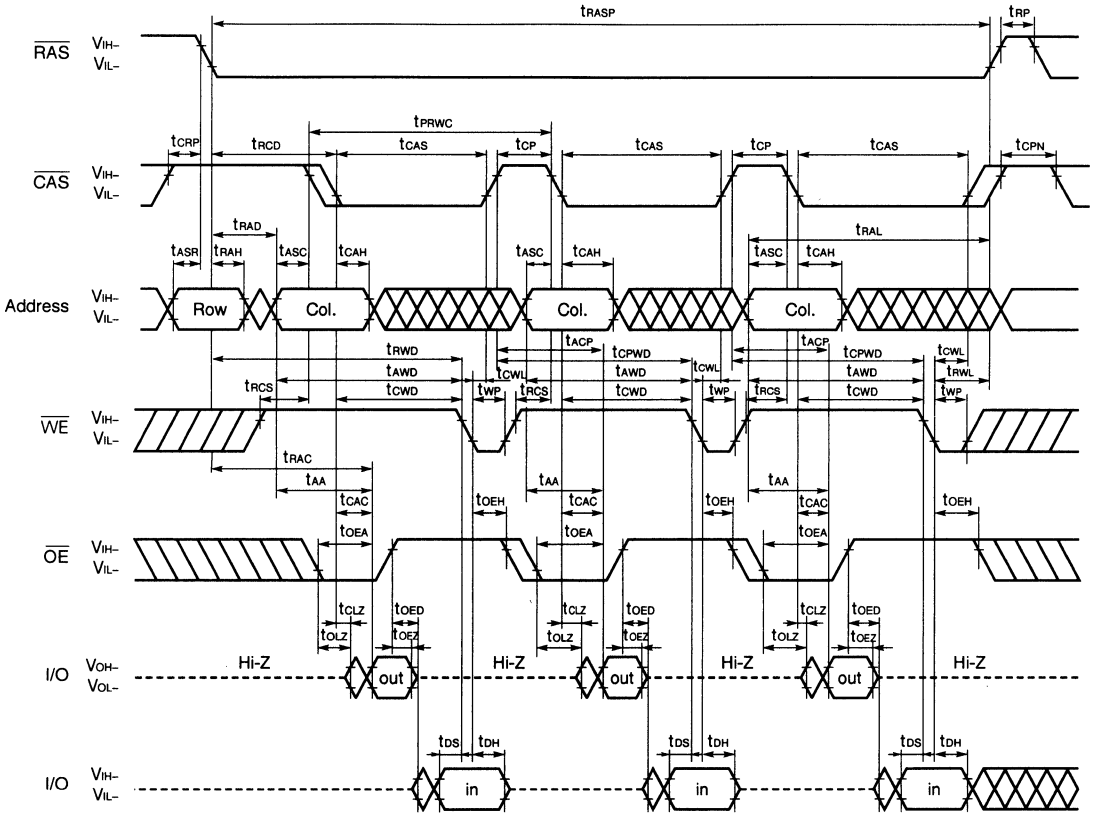
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



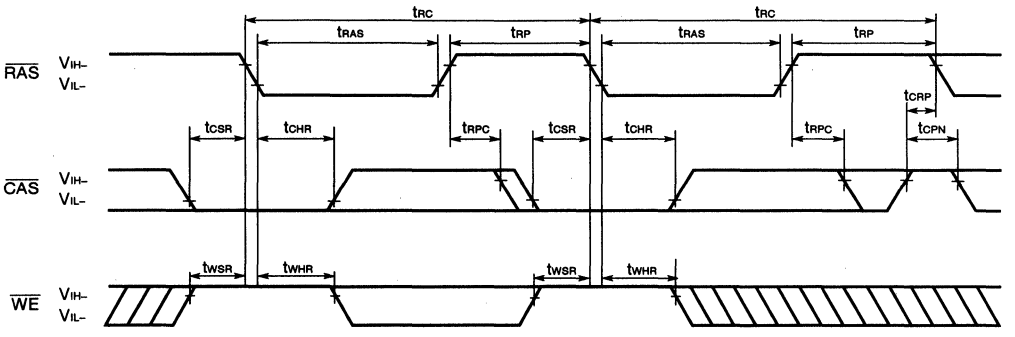
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



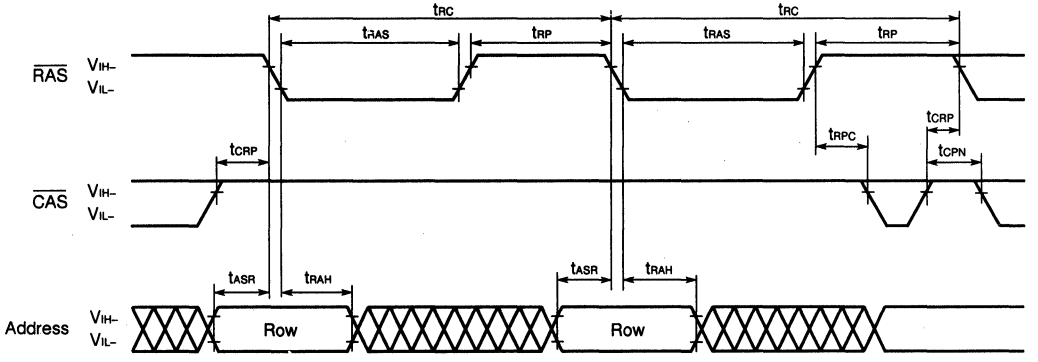
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



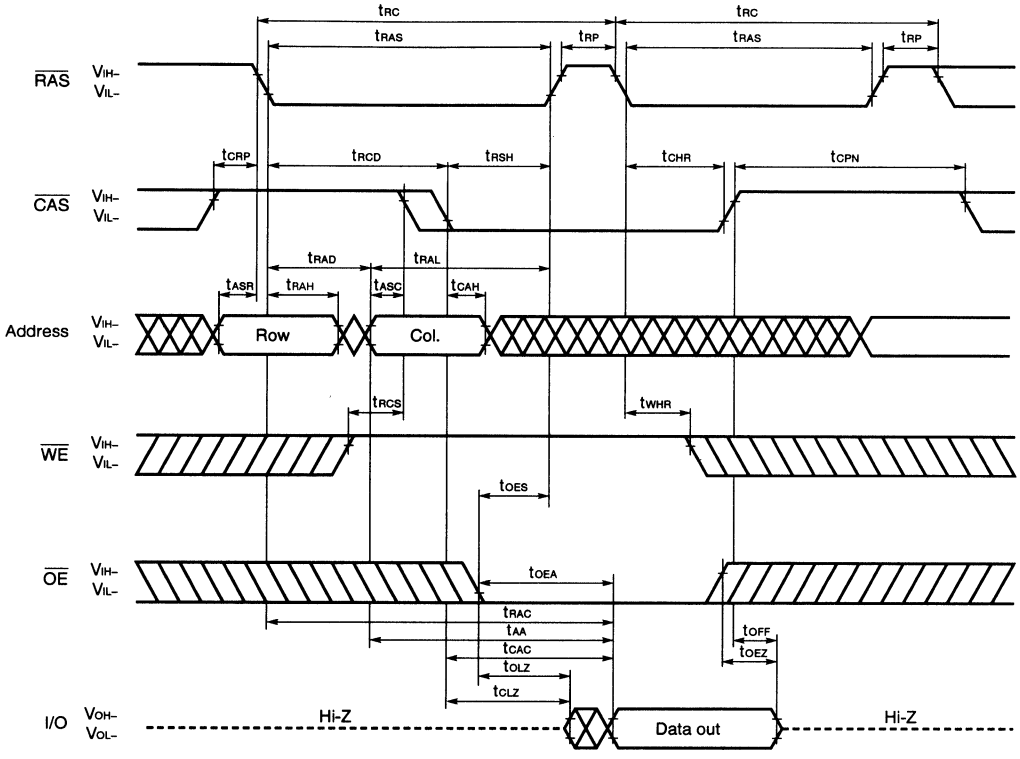
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

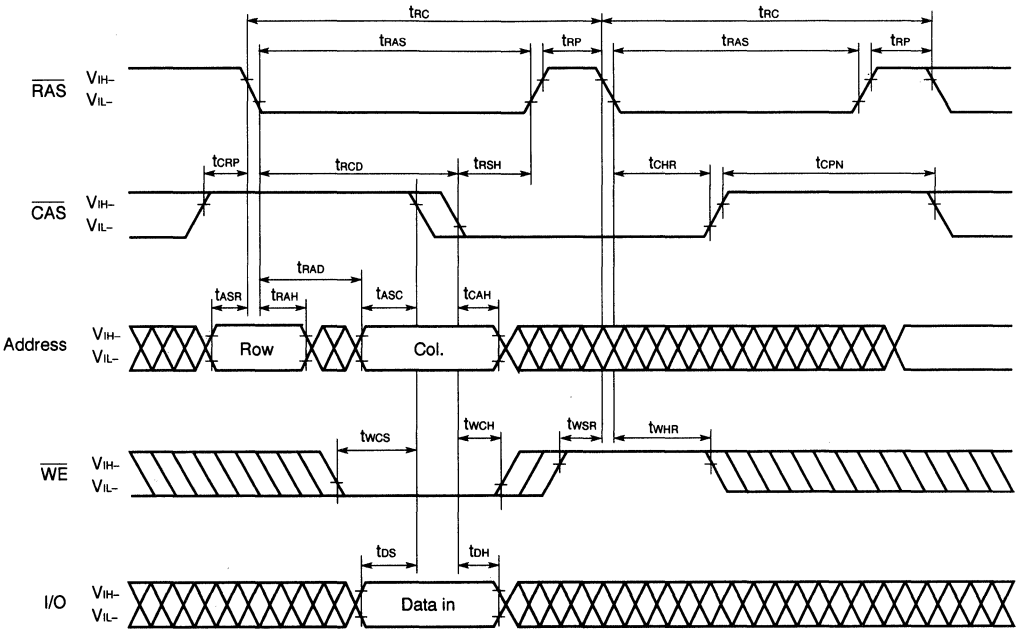


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



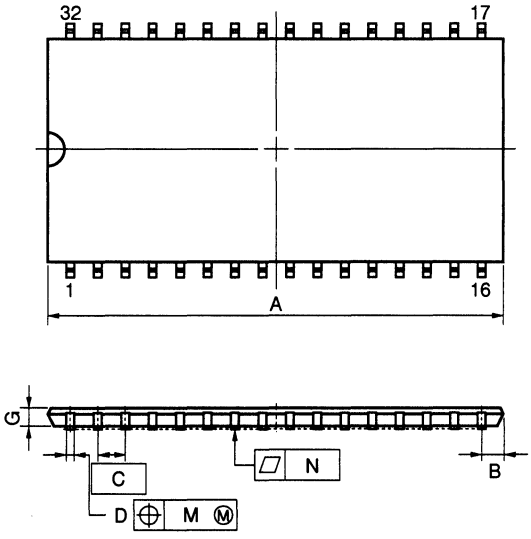
Hidden Refresh Cycle (Write)



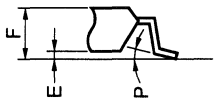
Remark $\overline{OE}$: Don't care

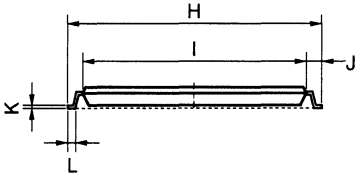
Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



detail of lead end





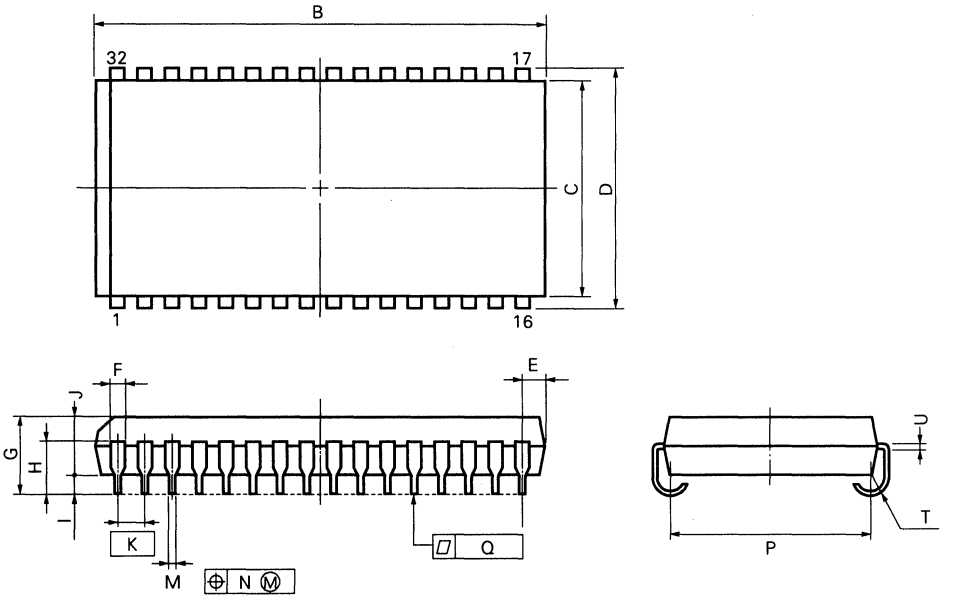
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



P32LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NEC

MOS INTEGRATED CIRCUIT

μPD4264160, 4265160

64 M-BIT DYNAMIC RAM
4 M-WORD BY 16-BIT, FAST PAGE MODE

Description

The μPD4264160, 4265160 are 4,194,304 words by 16 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These are packaged in 50-pin plastic TSOP(II).

Features

- 4,194,304 words by 16 bits organization
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD4264160-A50	396 mW	1.80 mW (CMOS level input)	50 ns	90 ns	35 ns
μPD4265160-A50	504 mW				
μPD4264160-A60	360 mW		60 ns	110 ns	40 ns
μPD4265160-A60	432 mW				
μPD4264160-A70	324 mW		70 ns	130 ns	45 ns
μPD4265160-A70	396 mW				
μPD4264160-A80	288 mW		80 ns	150 ns	50 ns
μPD4265160-A80	360 mW				

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

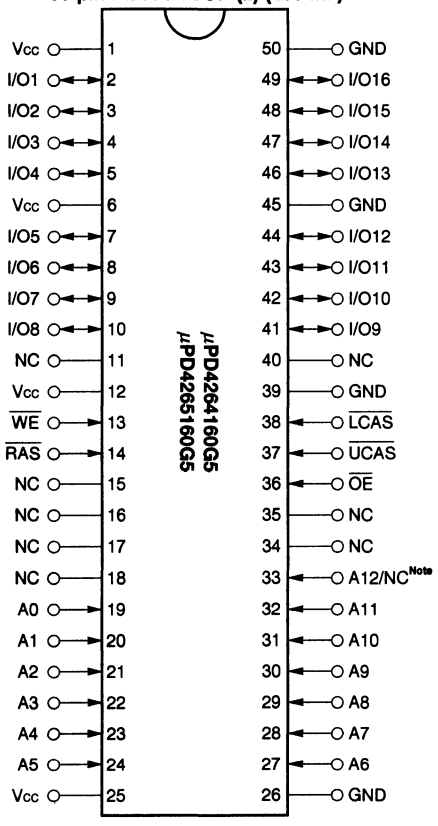
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264160	A0 - A12	A0 - A8	$\overline{RAS}$ only refresh, Normal read/write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265160	A0 - A11	A0 - A9	$\overline{RAS}$ only refresh, Normal read/write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD4264160G5-A50	50 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264160G5-A60	60 ns		
μPD4264160G5-A70	70 ns		
μPD4264160G5-A80	80 ns		
μPD4265160G5-A50	50 ns		
μPD4265160G5-A60	60 ns		
μPD4265160G5-A70	70 ns		
μPD4265160G5-A80	80 ns		

Pin Configuration (Marking Side)

50-pin Plastic TSOP (II) (400 mil)



Note A12 ... μPD4264160
NC ... μPD4265160

A0 to A12	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Upper Byte Column Address Strobe
$\overline{LCAS}$	:	Lower Byte Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264160, 4265160 have input pins $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O16.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{UCAS}$, $\overline{LCAS}$ (Upper, Lower column address strobe)	Input	$\overline{UCAS}$, $\overline{LCAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD4264160	A0-A12	13	9
μPD4265160	A0-A11	12	10

Electrical Specifications (Preliminary)

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[μPD4264160]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		110	mA	1, 2, 3
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		100		
		I_O = 0 mA	t_{RAC} = 70 ns		90		
			t_{RAC} = 80 ns		80		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns		110	mA	1, 2, 3, 4
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		100		
			t_{RAC} = 70 ns		90		
			t_{RAC} = 80 ns		80		
Operating current	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		90	mA	1, 2, 5
(Fast page mode)		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns		80		
			t_{RAC} = 70 ns		70		
			t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2
refresh current		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265160]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2, 3
		t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$	t_{RAC} = 50 ns		140	mA	1, 2, 3 ,4
		t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		120		
			t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		90	mA	1, 2, 5
		t_{PC} = $t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		80		
			t_{RAC} = 70 ns		70		
			t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		140	mA	1, 2
		t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		120		
		I_O = 0 mA	t_{RAC} = 70 ns		110		
			t_{RAC} = 80 ns		100		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$ and $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$.

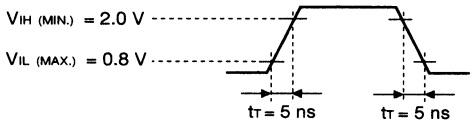
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

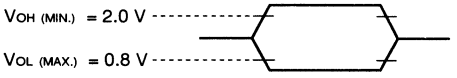
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

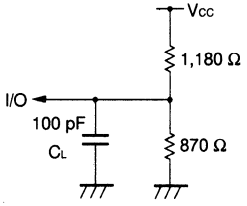
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tRC	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	tRP	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	tCPN	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{CAS}$ pulse width	tCAS	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	tCSH	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	37	20	45	20	52	25	60	ns	1
$\overline{RAS}$ to column address delay time	tRAD	13	25	15	30	15	35	17	40	ns	1
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	–	5	–	5	–	5	–	ns	2
Row address setup time	tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time	tRAH	8	–	10	–	10	–	12	–	ns	
Column address setup time	tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time	tCAH	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	tOED	10	–	13	–	15	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$	tMRH	0	–	0	–	0	–	0	–	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	
Refresh time	tREF	–	64	–	64	–	64	–	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	128	–	153	–	175	–	195	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	83	–	95	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	–	38	–	43	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	45	–	53	–	60	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

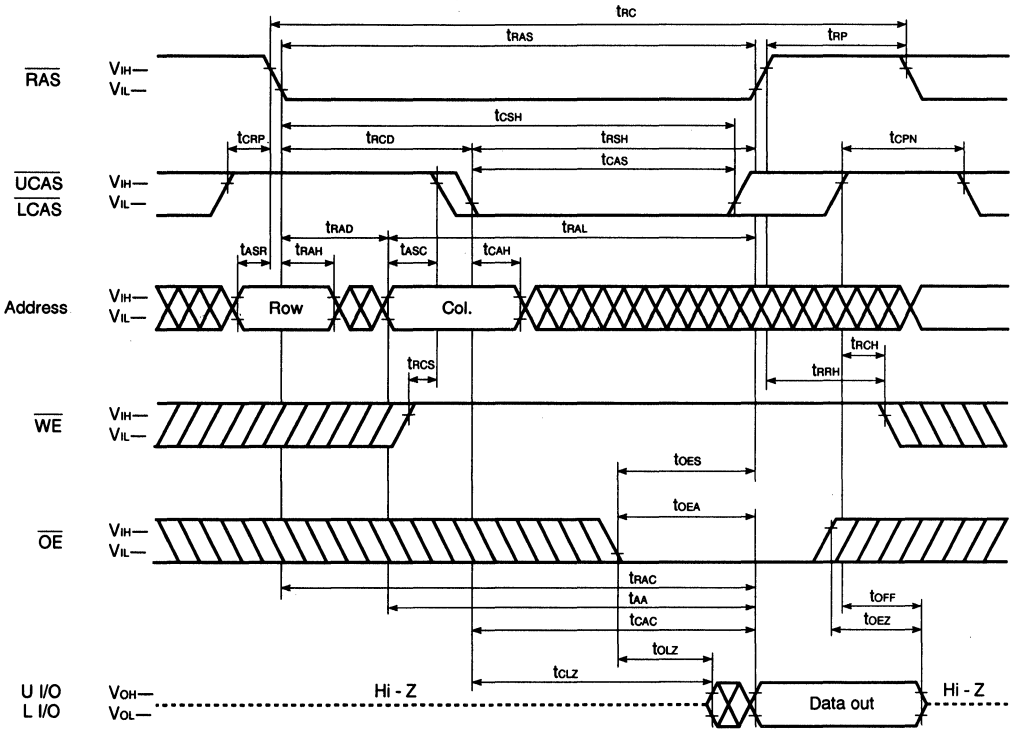
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

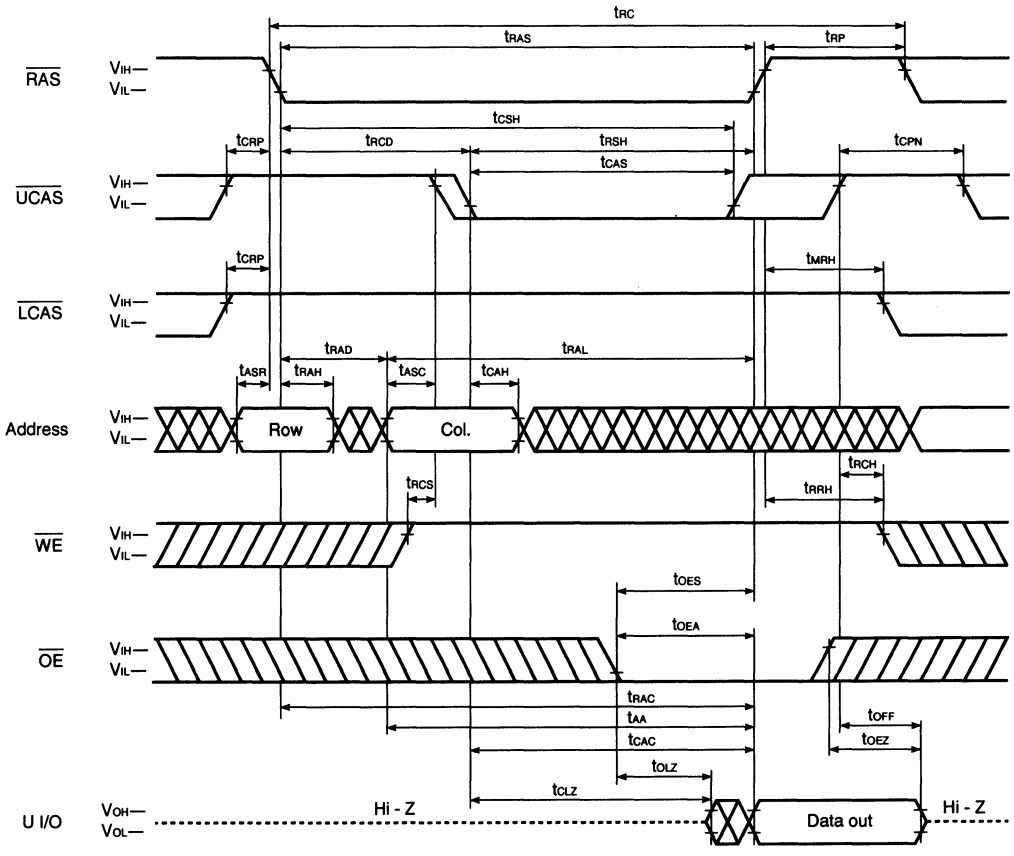
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

Read Cycle

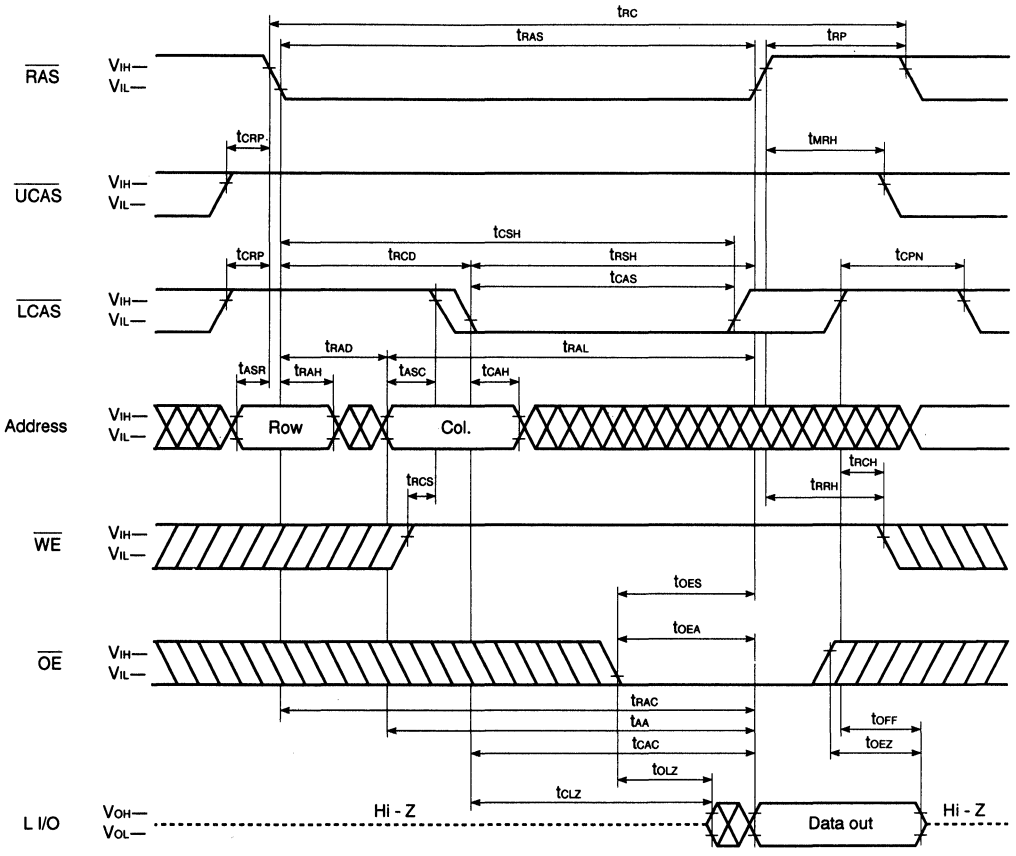

tRC
tRAS
tRP
RAS
VIH—
VIL—
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
U I/O
L I/O
VOH—
VOL—
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



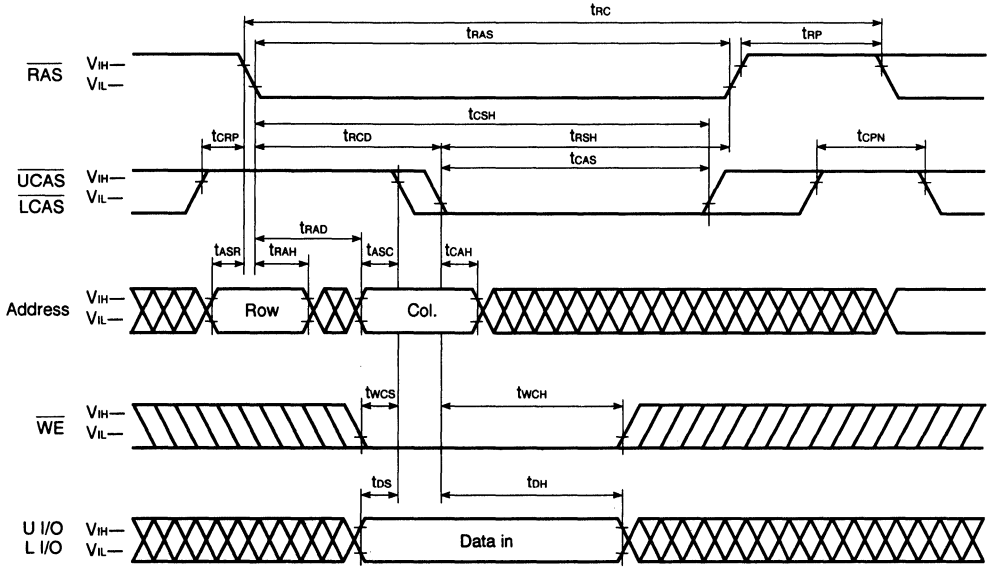
Remark L I/O: Hi-Z

Lower Byte Read Cycle



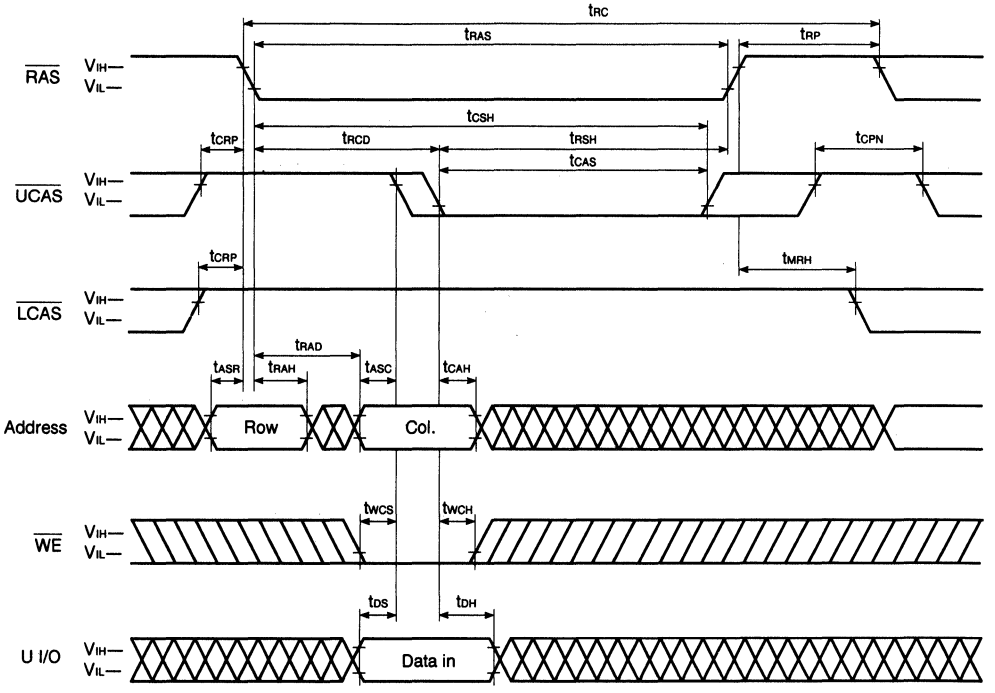
Remark U I/O: Hi-Z

Early Write Cycle



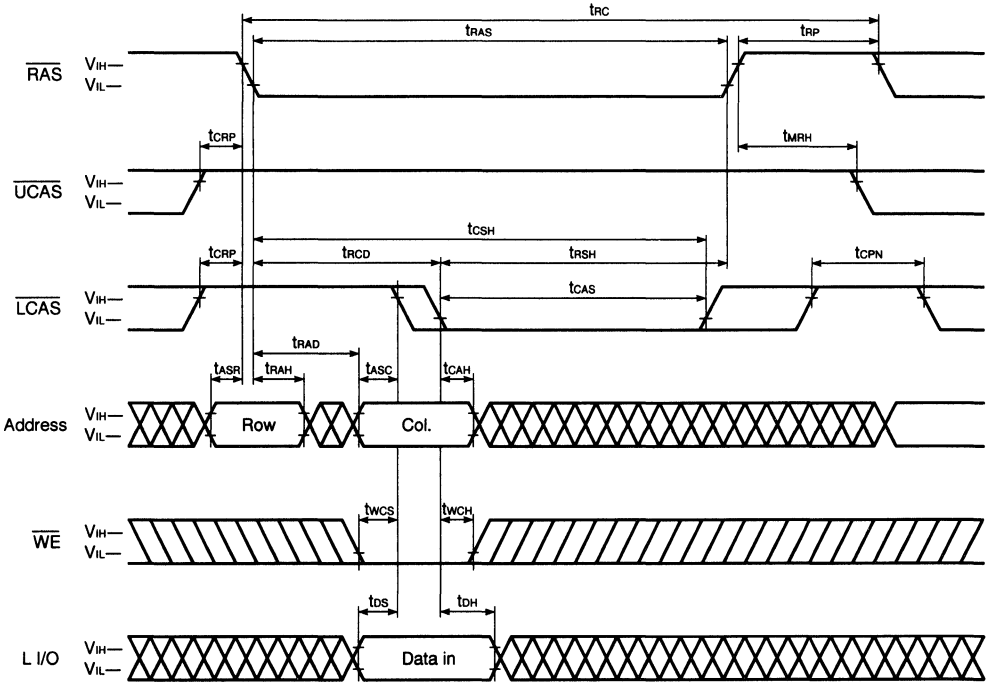
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



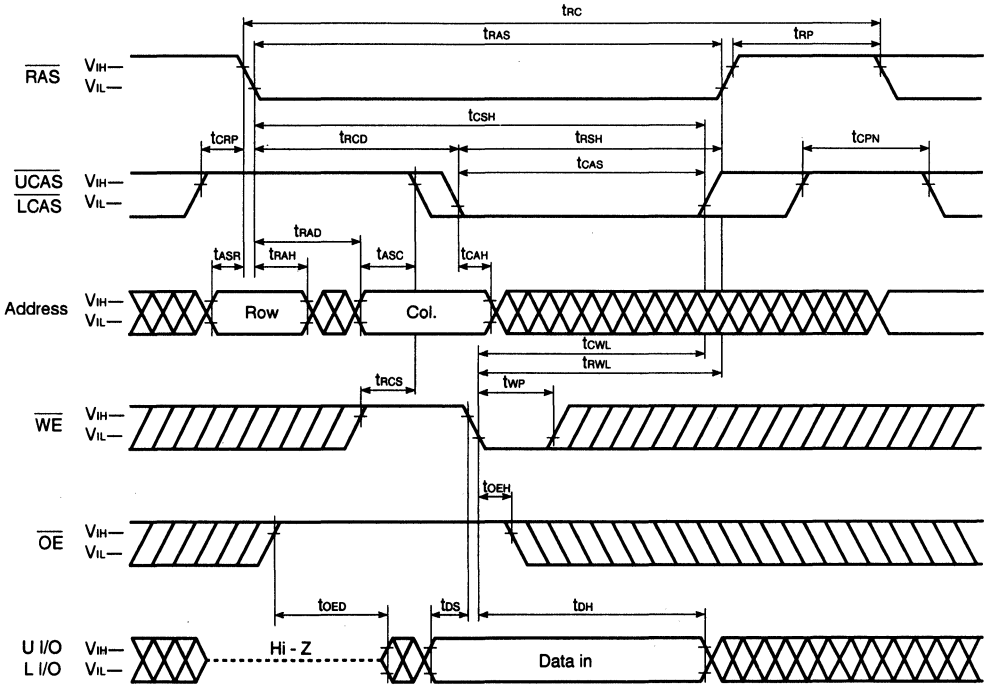
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

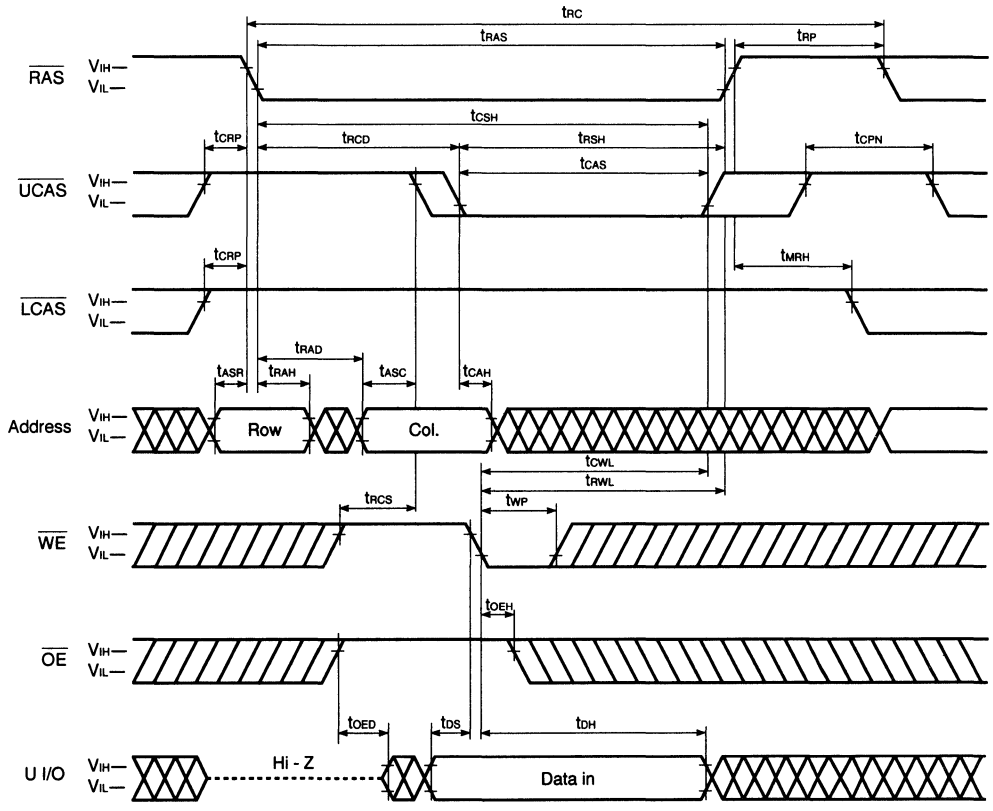


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

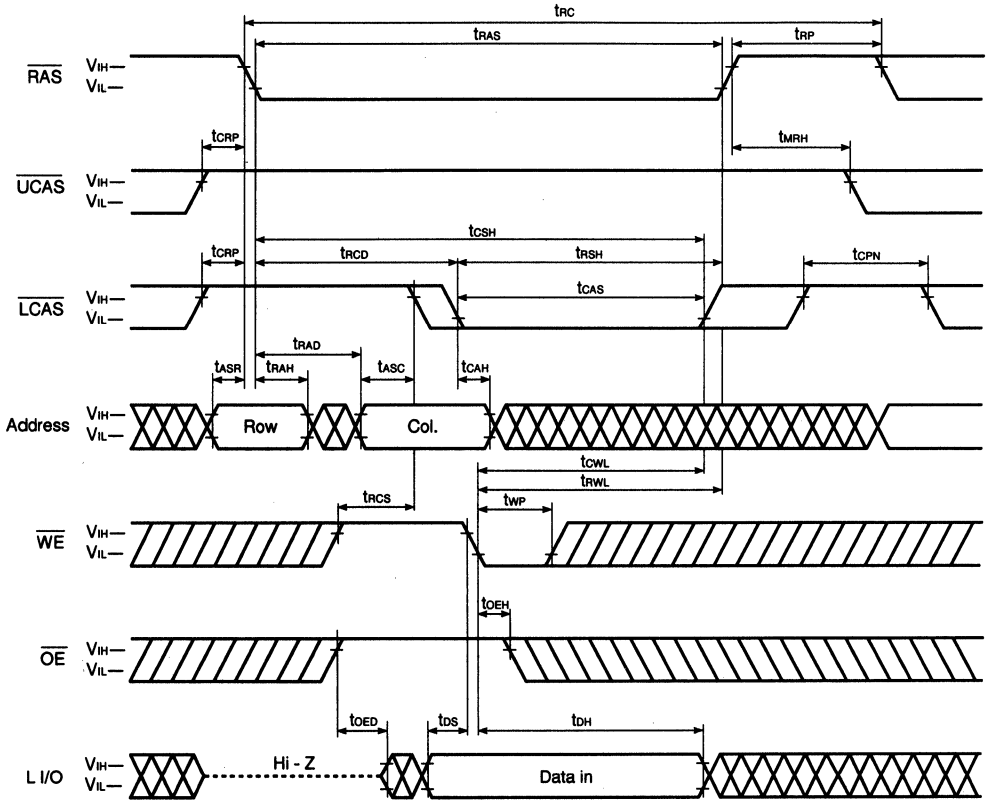


Upper Byte Late Write Cycle



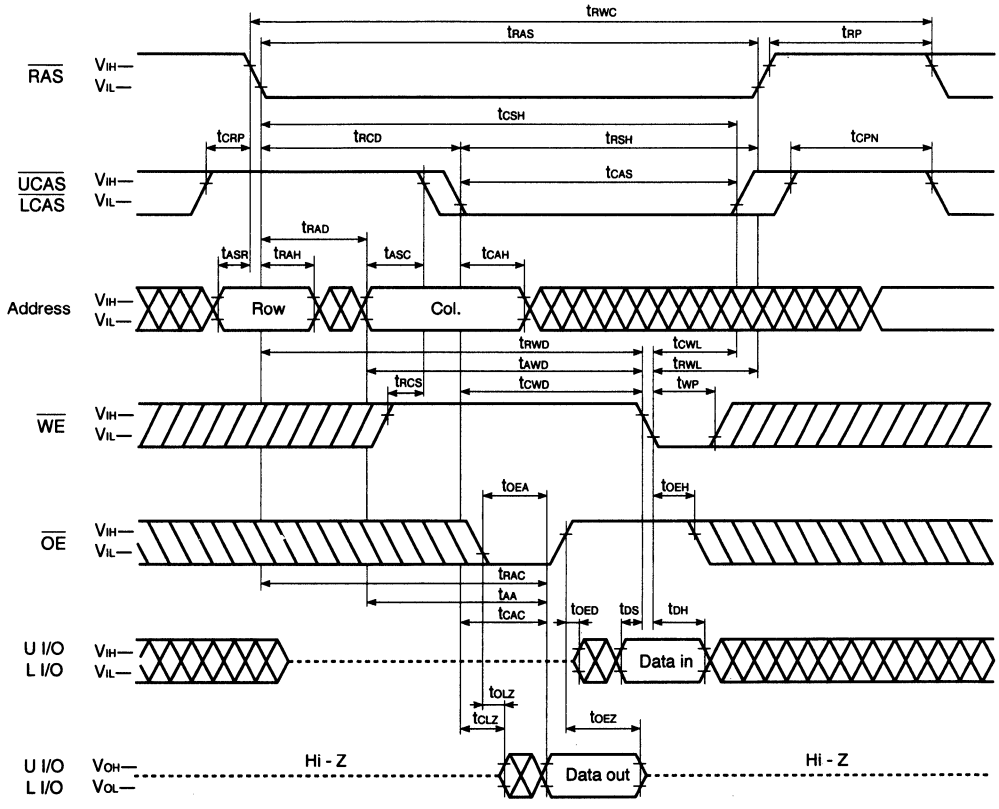
Remark L I/O: Don't care

Lower Byte Late Write Cycle

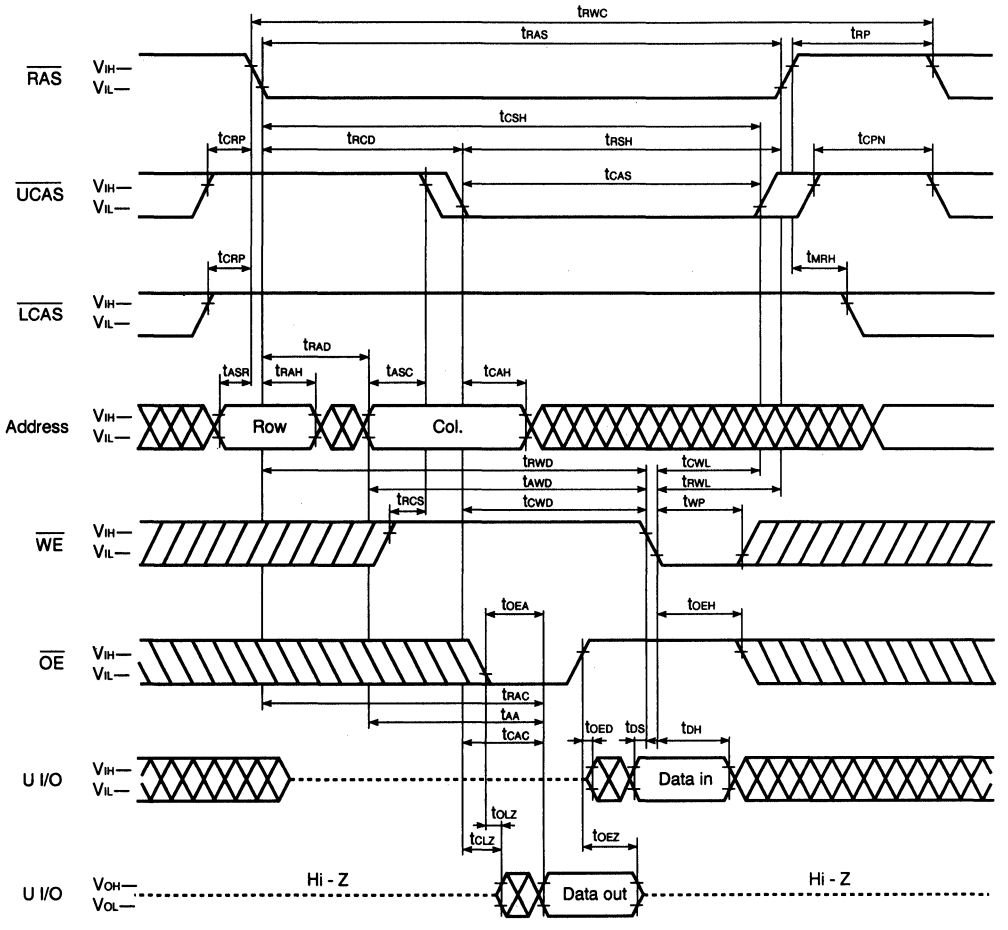


Remark U I/O: Don't care

Read Modify Write Cycle

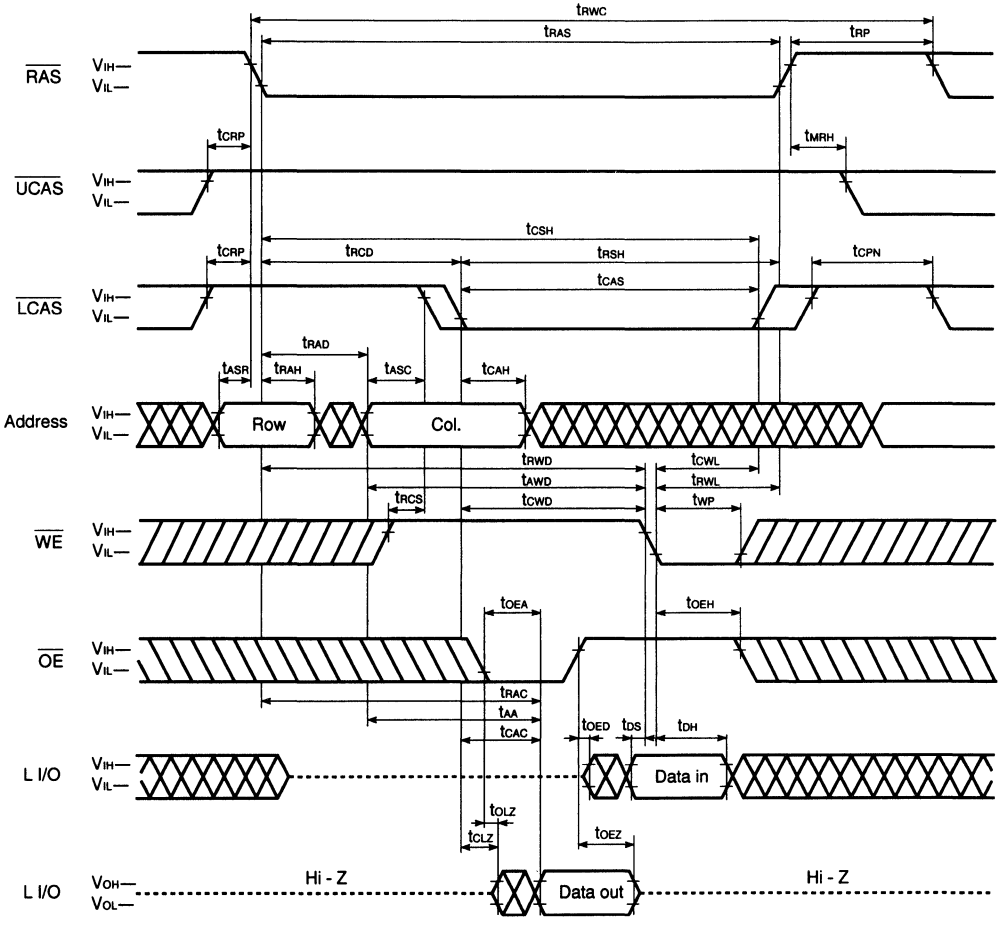


Upper Byte Read Modify Write Cycle



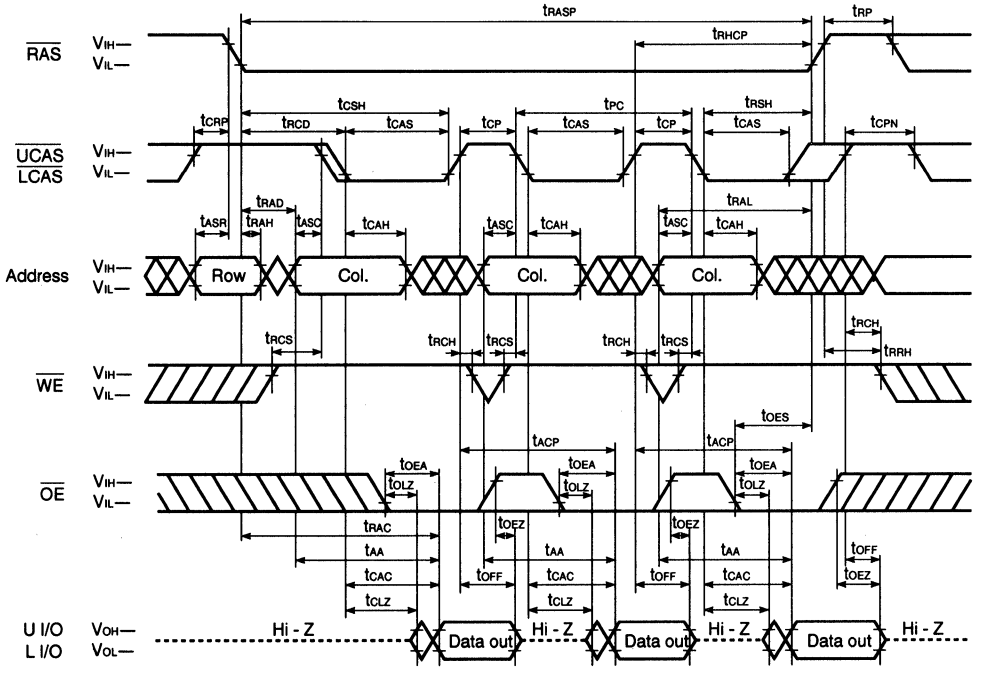
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



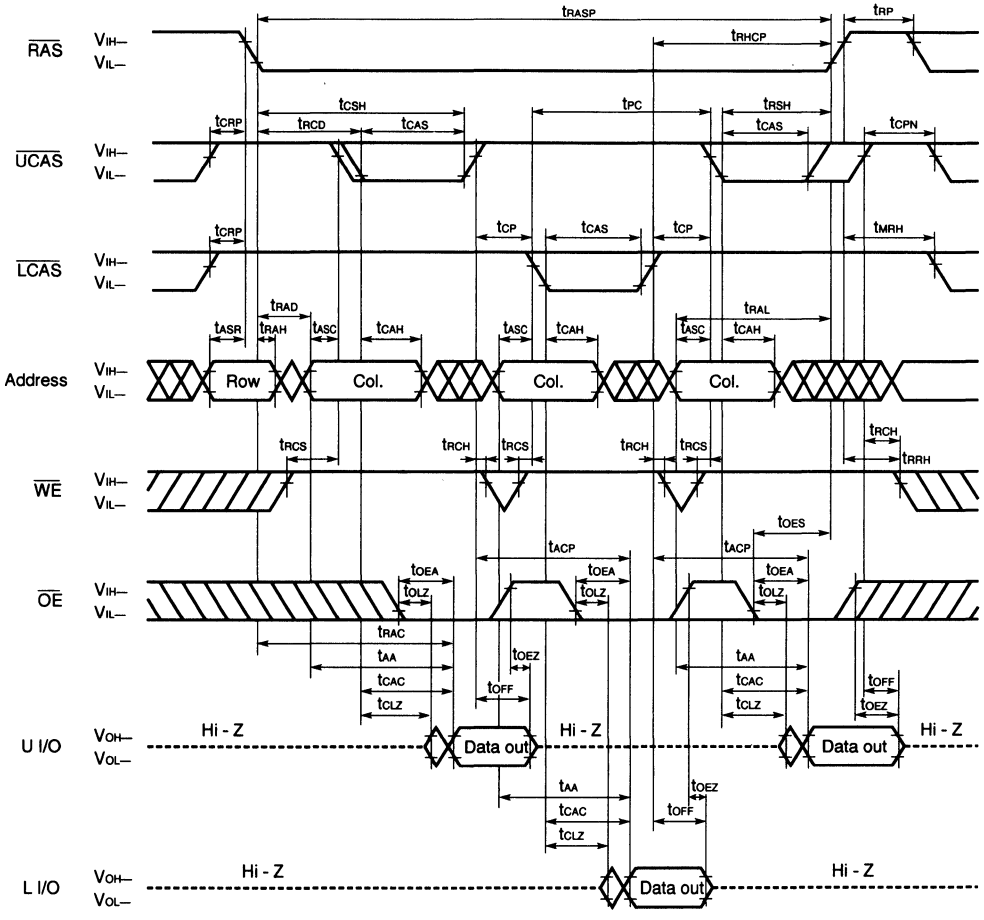
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

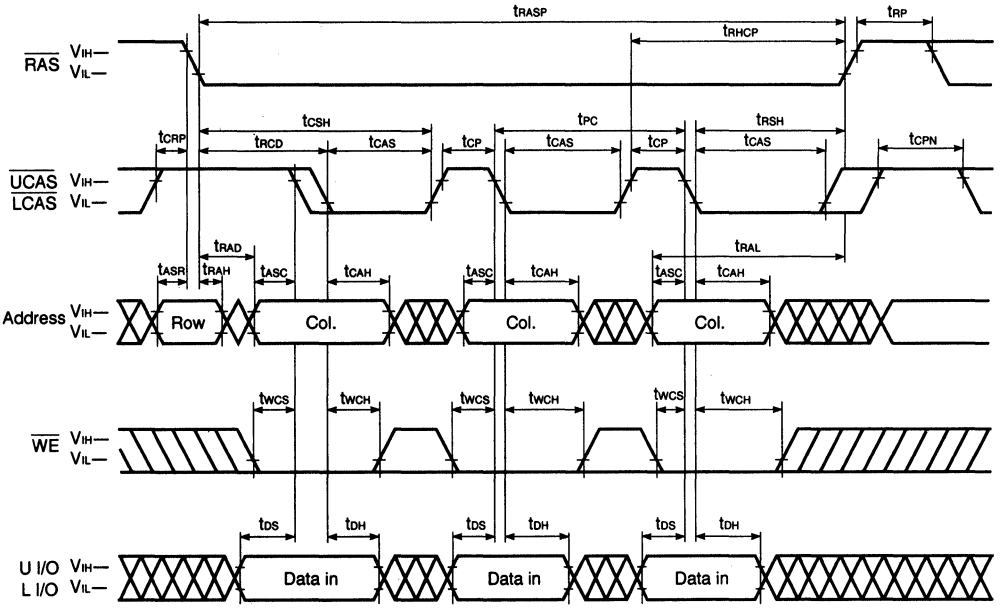
Fast Page Mode Byte Read Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

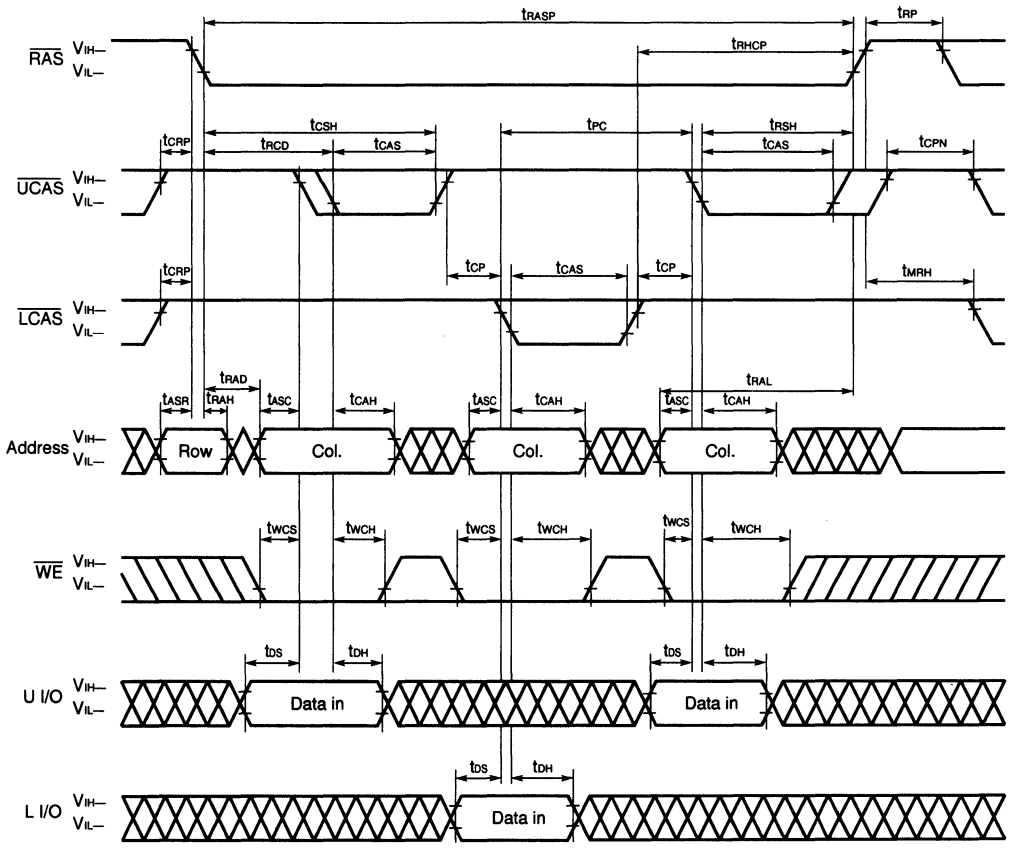
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

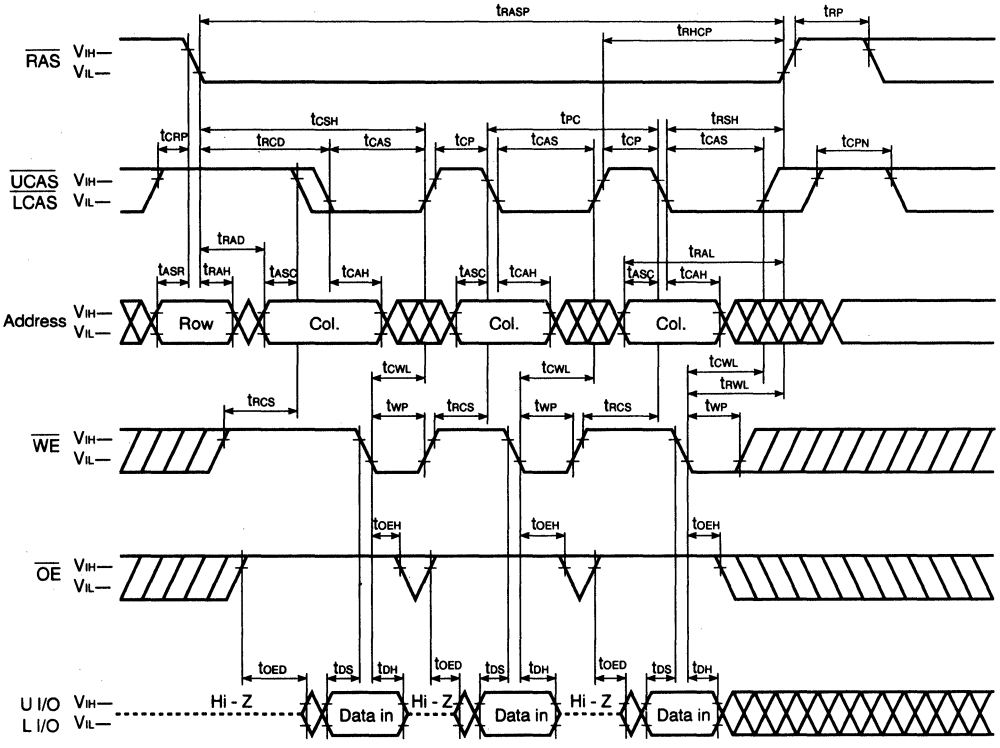
Fast Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

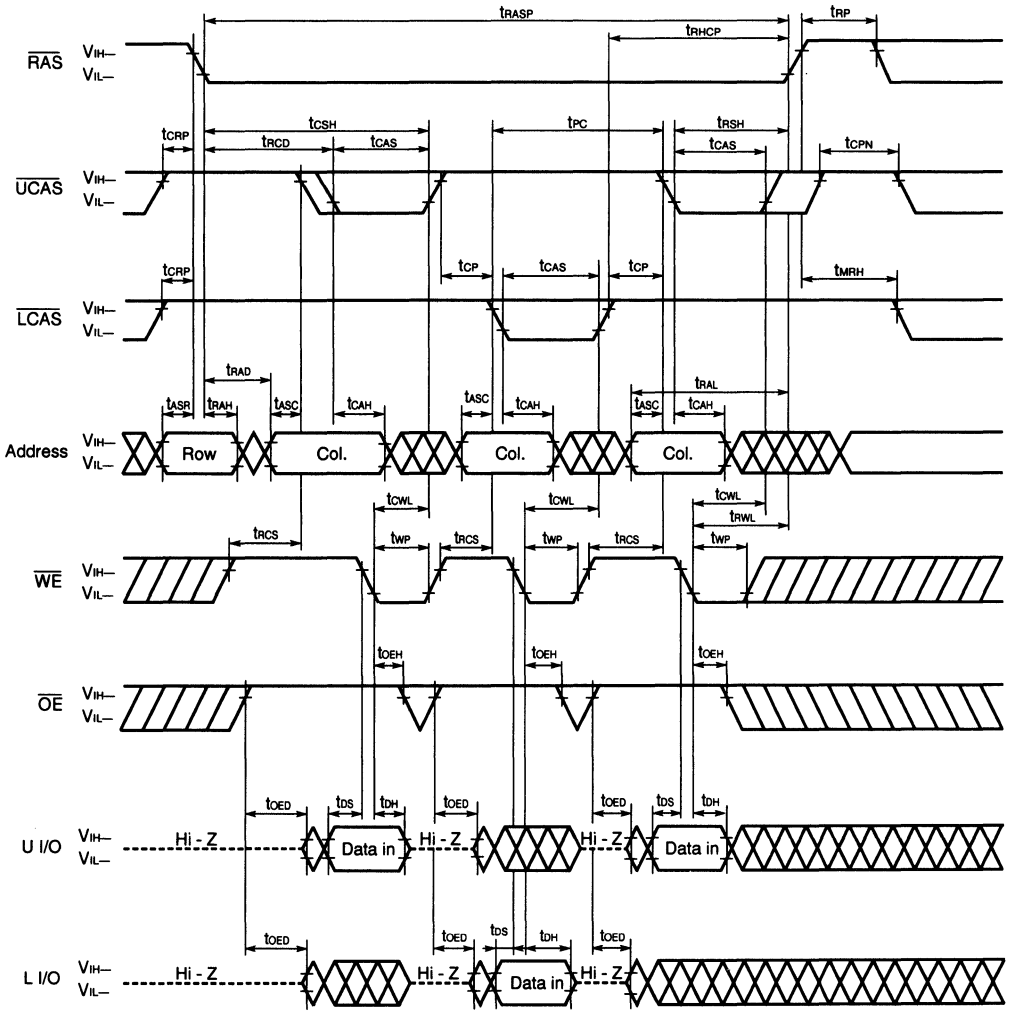
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

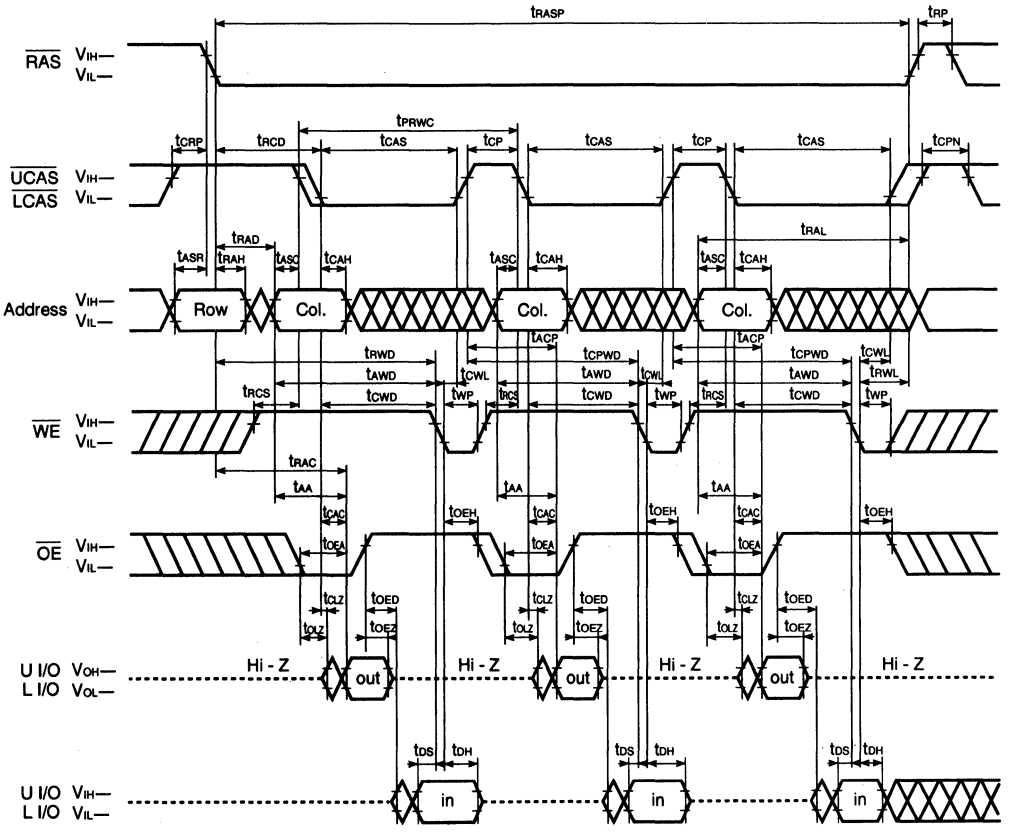
Fast Page Mode Byte Late Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

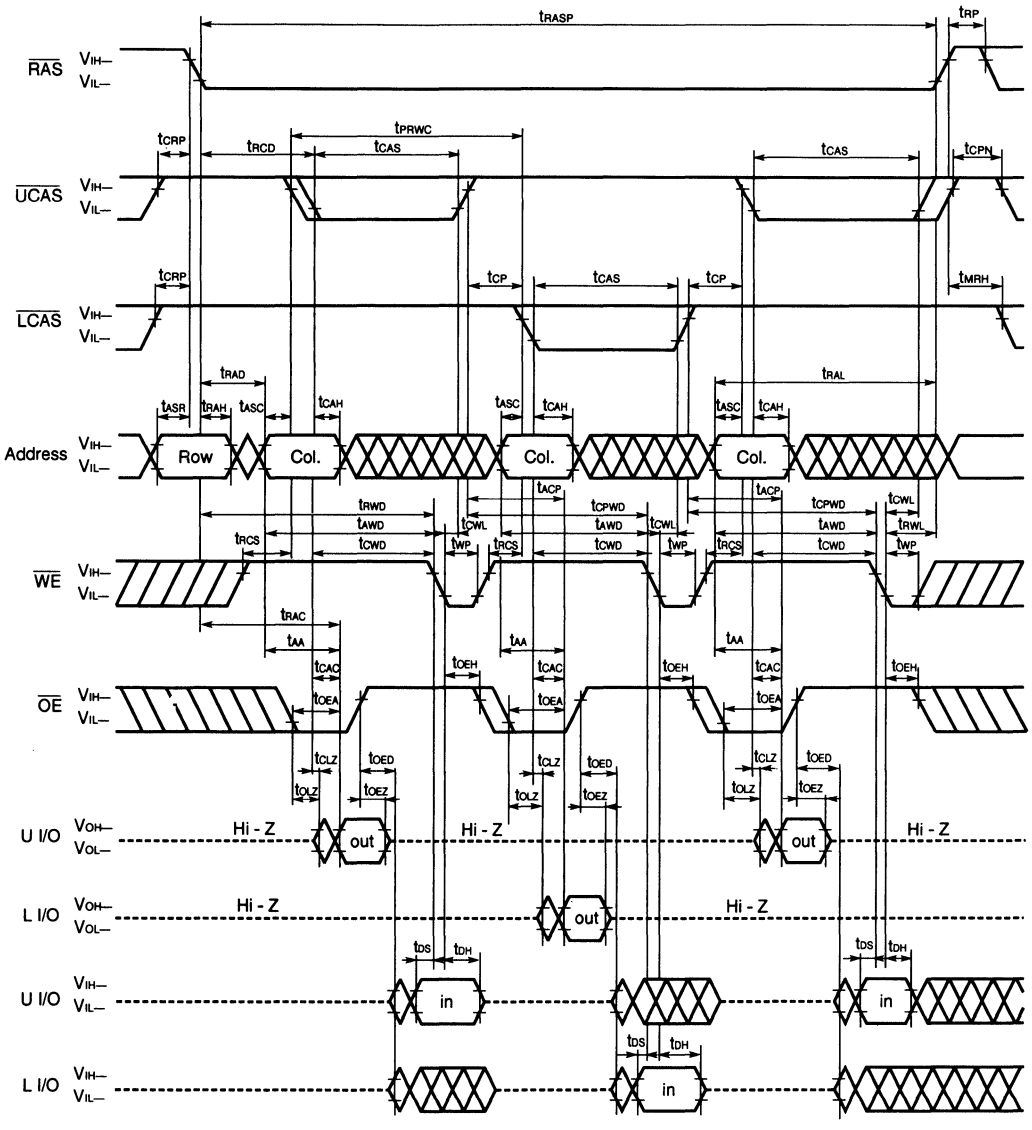
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

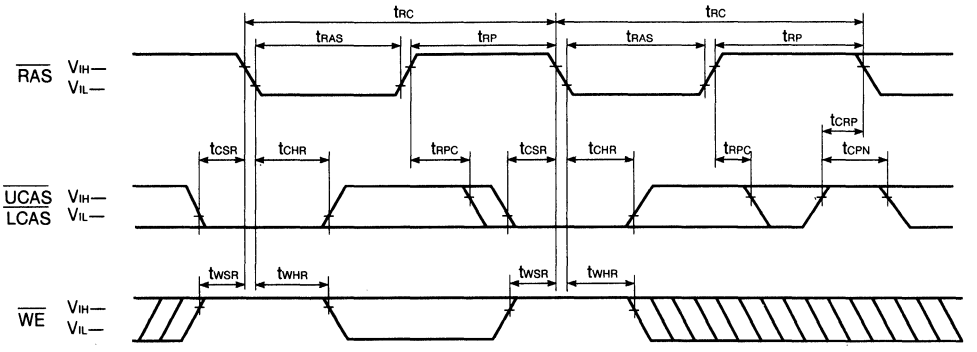
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

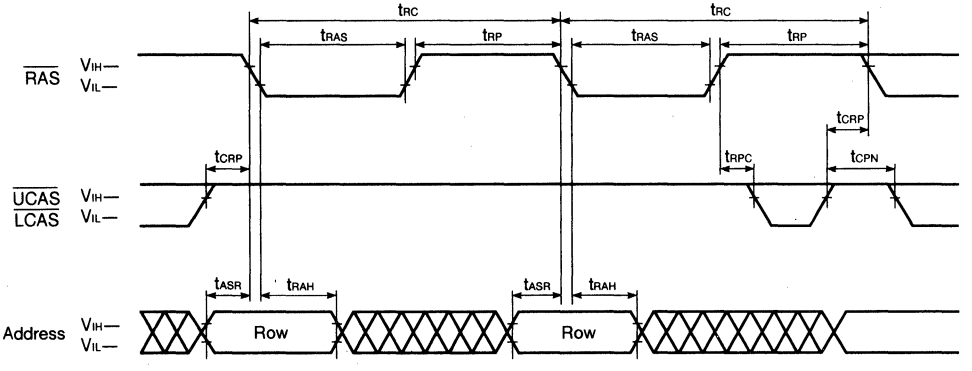
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



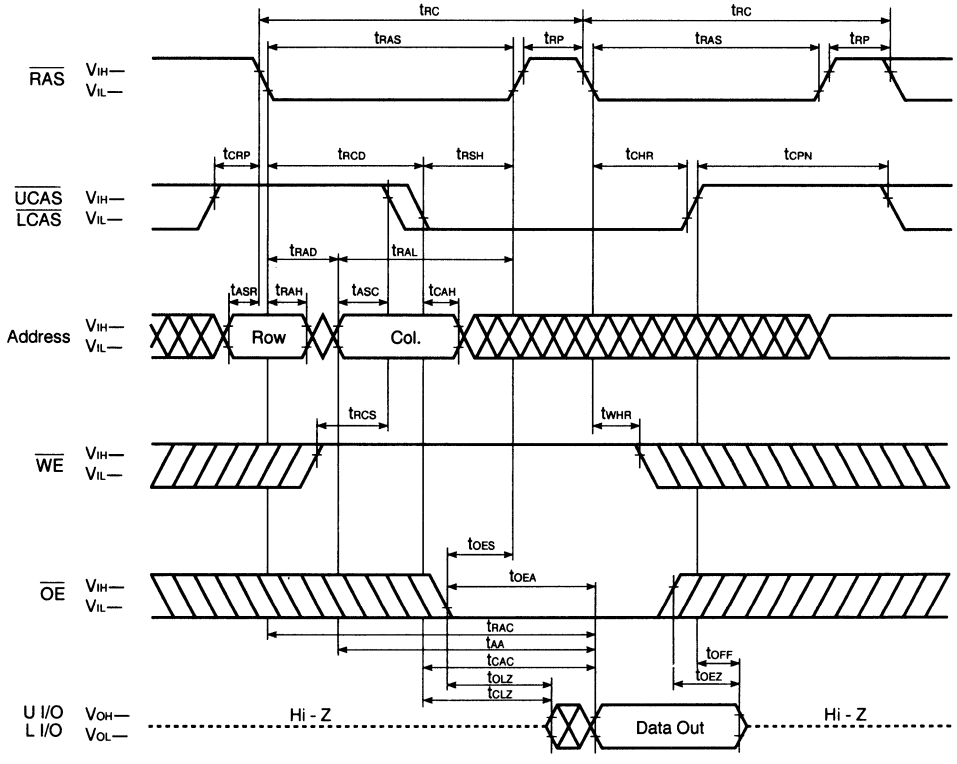
Remark Address, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

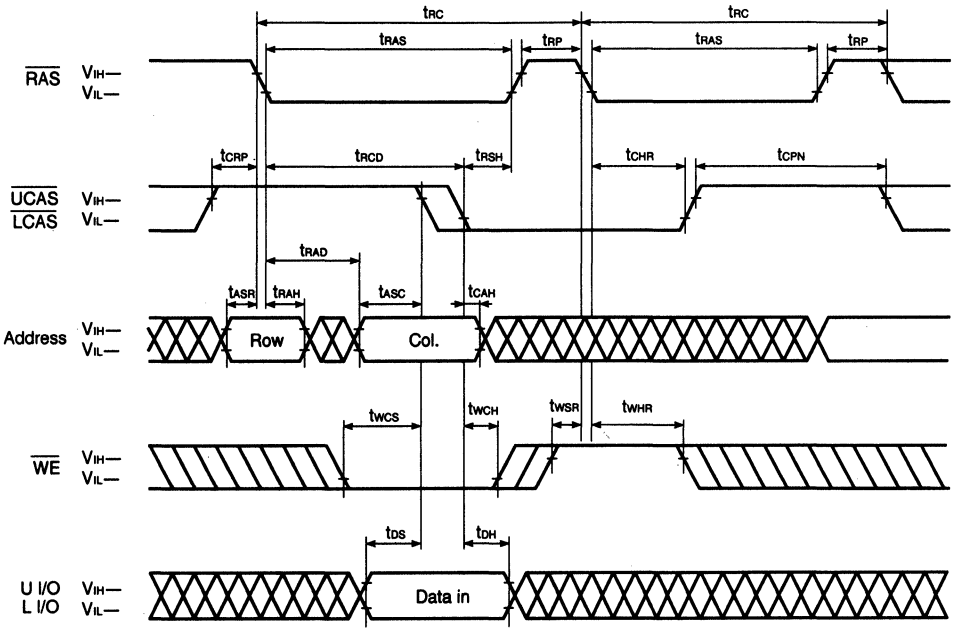


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



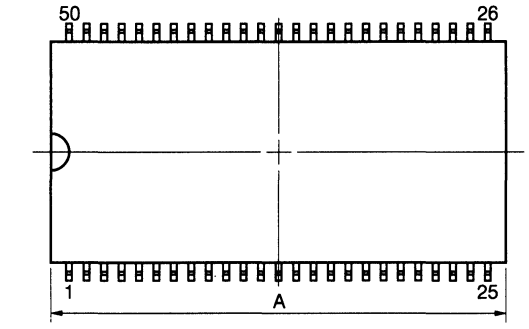
Hidden Refresh Cycle (Write)



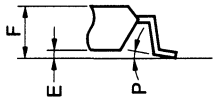
Remark $\overline{OE}$: Don't care

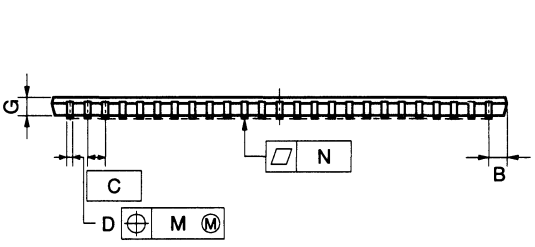
Package Drawing

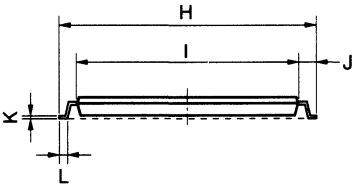
50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF3

[MEMO]

Fast Page Mode
16M Dynamic RAM
[5.0V ± 10%]

NEC

MOS INTEGRATED CIRCUIT

μPD42S16400,4216400,42S17400,4217400

16 M-BIT DYNAMIC RAM
4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μPD42S16400, 4216400, 42S17400, 4217400 are 4,194,304 words by 4 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S16400, 42S17400 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 26-pin plastic TSOP(II) and 26-pin plastic SOJ.

Features

- 4,194,304 words by 4 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S16400-50, 4216400-50	550 mW	50 ns	90 ns	35 ns
μPD42S17400-50, 4217400-50	660 mW			
μPD42S16400-60, 4216400-60	495 mW	60 ns	110 ns	40 ns
μPD42S17400-60, 4217400-60	605 mW			
μPD42S16400-70, 4216400-70	440 mW	70 ns	130 ns	45 ns
μPD42S17400-70, 4217400-70	550 mW			
μPD42S16400-80, 4216400-80	385 mW	80 ns	150 ns	50 ns
μPD42S17400-80, 4217400-80	495 mW			

- The μPD42S16400, 42S17400 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

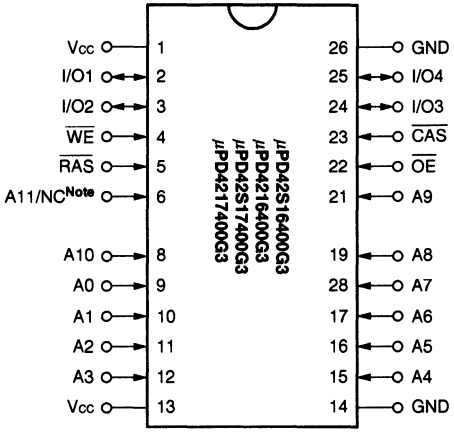
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16400	4,096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μPD42S17400	2,048 cycles/128 ms		
μPD4216400	4,096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
μPD4217400	2,048 cycles/32 ms		

Ordering Information

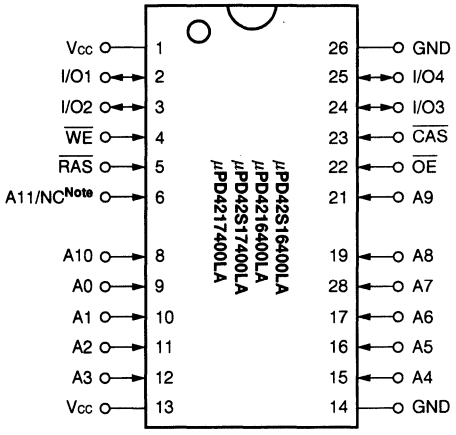
Part number	Access time (MAX.)	Package	Refresh
μPD42S16400G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17400G3-50			
μPD42S16400G3-60	60 ns		
μPD42S17400G3-60			
μPD42S16400G3-70	70 ns		
μPD42S17400G3-70			
μPD42S16400G3-80	80 ns		
μPD42S17400G3-80			
μPD42S16400LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD42S17400LA-50			
μPD42S16400LA-60	60 ns		
μPD42S17400LA-60			
μPD42S16400LA-70	70 ns		
μPD42S17400LA-70			
μPD42S16400LA-80	80 ns		
μPD42317400LA-80			
μPD4216400G3-50	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217400G3-50			
μPD4216400G3-60	60 ns		
μPD4217400G3-60			
μPD4216400G3-70	70 ns		
μPD4217400G3-70			
μPD4216400G3-80	80 ns		
μPD4217400G3-80			
μPD4216400LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD4217400LA-50			
μPD4216400LA-60	60 ns		
μPD4217400LA-60			
μPD4216400LA-70	70 ns		
μPD4217400LA-70			
μPD4216400LA-80	80 ns		
μPD4217400LA-80			

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)



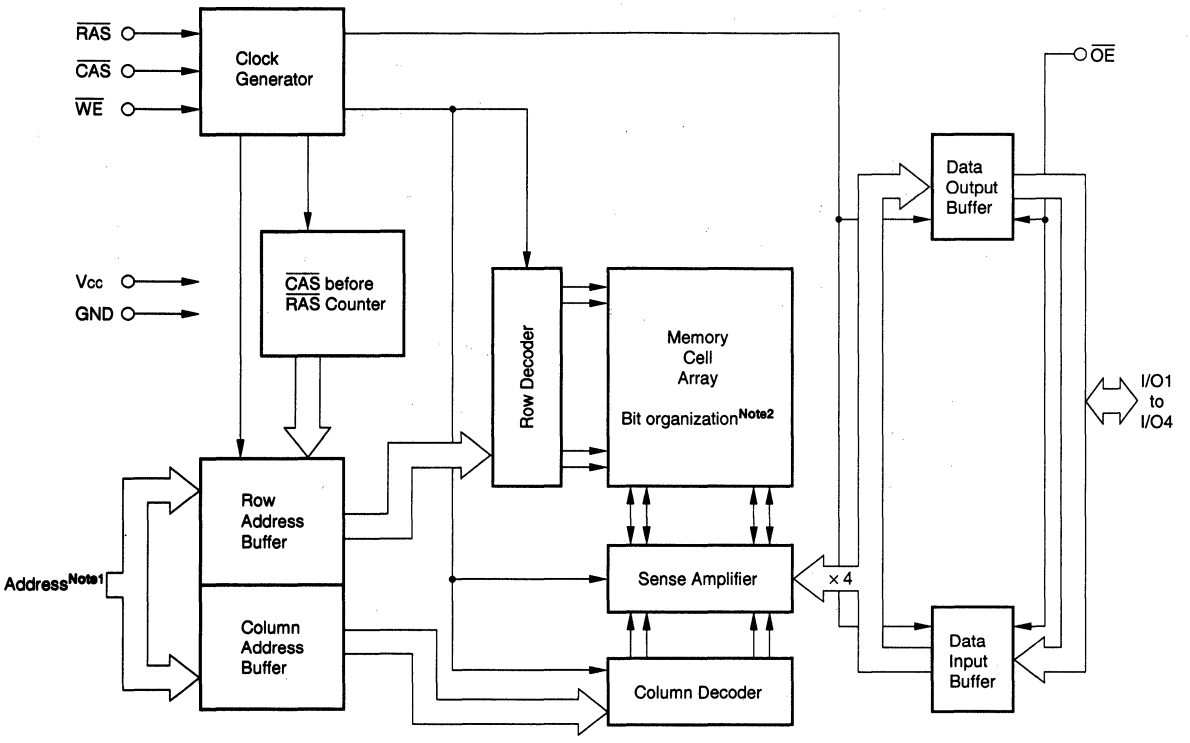
26-pin Plastic SOJ (300 mil)



Note A11 ... μPD42S16400, 4216400
NC μPD42S17400, 4217400

A0 to A11 : Address Inputs
I/O1 to I/O4 : Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground
NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16400, 4216400	A0 – A11	A0 – A9
μPD42S17400, 4217400	A0 – A10	A0 – A10

2. μPD42S16400, 4216400 ... 4,096 × 1,024 × 4 μPD42S17400, 4217400 ... 2,048 × 2,048 × 4

Input/Output Pin Functions

The μPD42S16400, 4216400, 42S17400, 4217400 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax [Note] (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD42S16400, 4216400	A0 – A11	12	10
μPD42S17400, 4217400	A0 – A10	11	11

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)
[μPD42S16400, 4216400]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 3
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
Standby current	μPD42S16400	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.25		
	μPD4216400		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2, 3, 4
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		80	mA	1, 2, 5
				t_{RAC} = 60 ns		70		
				t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns		100	mA	1, 2
				t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16400)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V	$t_{RAS} \leq 300$ ns		450	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		600	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16400)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH(MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

[μPD42S17400, 4217400]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2, 3
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		90		
Standby current	μPD42S17400	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.25		
	μPD4217400		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2, 3, 4
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		90		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns		80	mA	1, 2, 5
				t_{RAC} = 60 ns		70		
				t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns		120	mA	1, 2
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		90		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17400)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2$ V	$t_{RAS} \leq 300$ ns		400	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		500	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17400)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH(MAX.)}$ $0\ V \leq V_{IL} \leq 0.2$ V I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

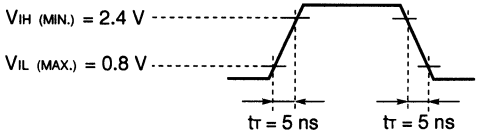
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

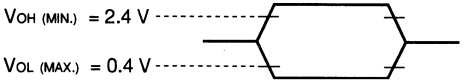
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

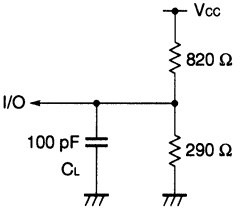
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	90	–	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time		tRP	30	–	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time		tCPN	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	13	10,000	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		tRSH	13	–	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time		tCSH	50	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	18	37	20	45	20	52	25	60	ns	2
$\overline{RAS}$ to column address delay time		tRAD	13	25	15	30	15	35	17	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time		tRAH	8	–	10	–	10	–	12	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time		tCAH	13	–	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	10	–	15	–	15	–	20	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	3	50	3	50	ns	
Refresh time	μPD42S16400, 42S17400	tREF	–	128	–	128	–	128	–	128	ms	4
	μPD4216400		–	64	–	64	–	64	–	64		
	μPD4217400		–	32	–	32	–	32	–	32		

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16400, 42S17400.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	10	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	10	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	18	–	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	133	–	160	–	180	–	205	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	–	85	–	95	–	110	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	–	40	–	43	–	50	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	45	–	55	–	60	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	30	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	73	–	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	50	–	58	–	65	–	70	–	ns	1

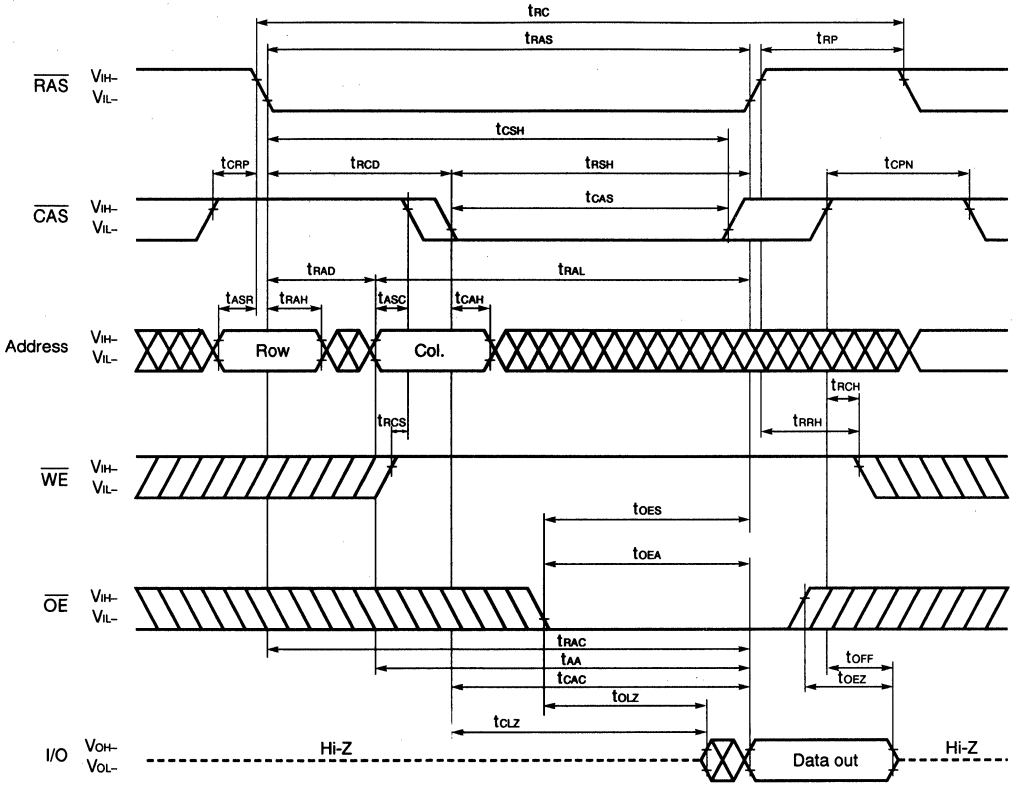
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

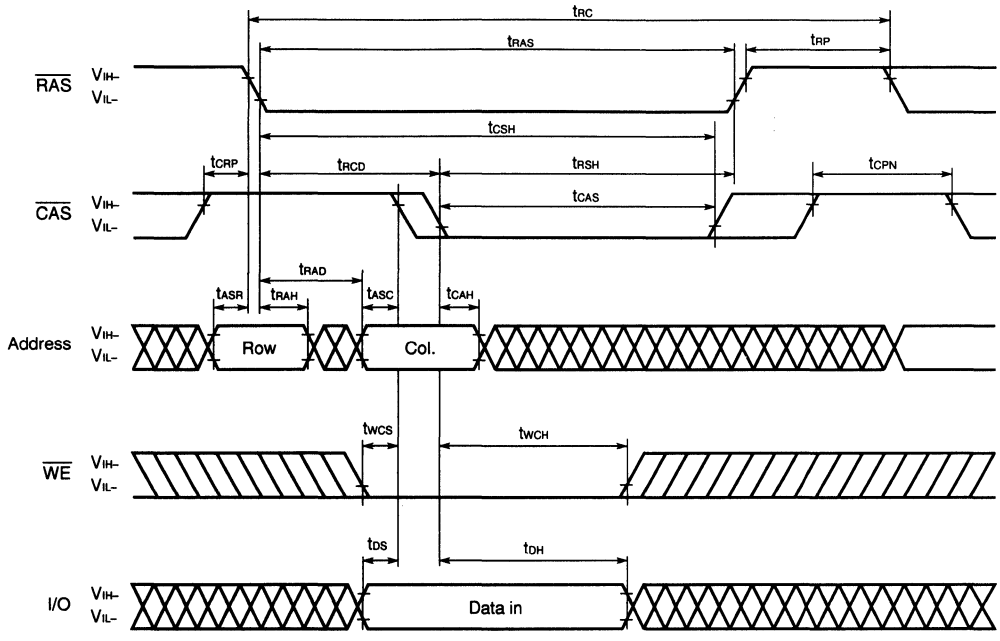
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	90	–	110	–	130	–	150	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	−50	–	−50	–	−50	–	−50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16400, 42S17400.

Read Cycle

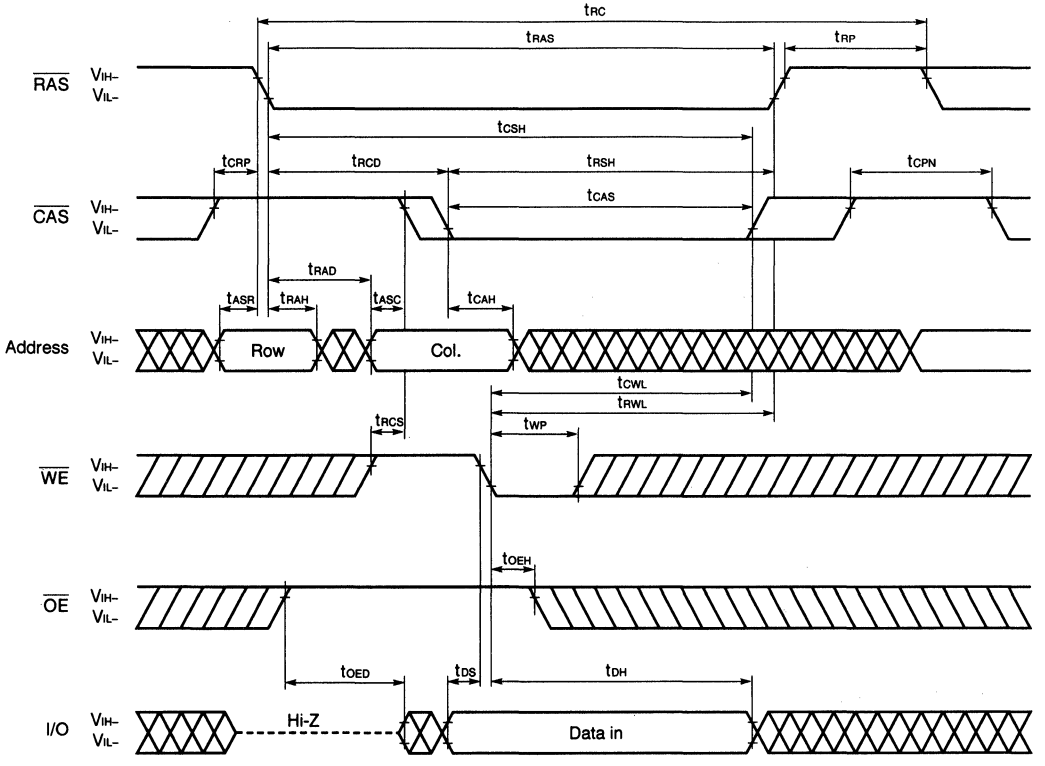

tRC
tRAS
tRP
RAS VIH- VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS VIH- VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH- VIL-
Row
Col.
tRCH
tRCS
tRRH
WE VIH- VIL-
tOES
tOEA
OE VIH- VIL-
tRAC
tAA
tCAC
tOLZ
tOFF
tOEZ
tCLZ
I/O VOH- VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

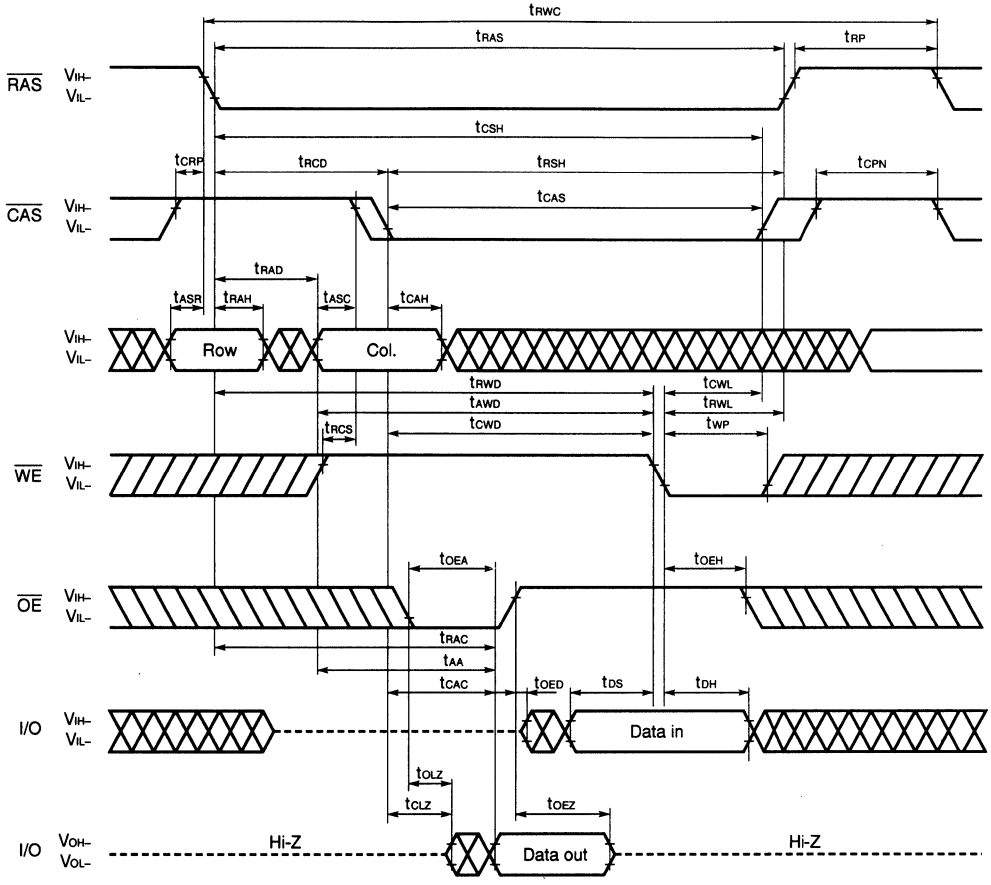


Remark $\overline{OE}$: Don't care

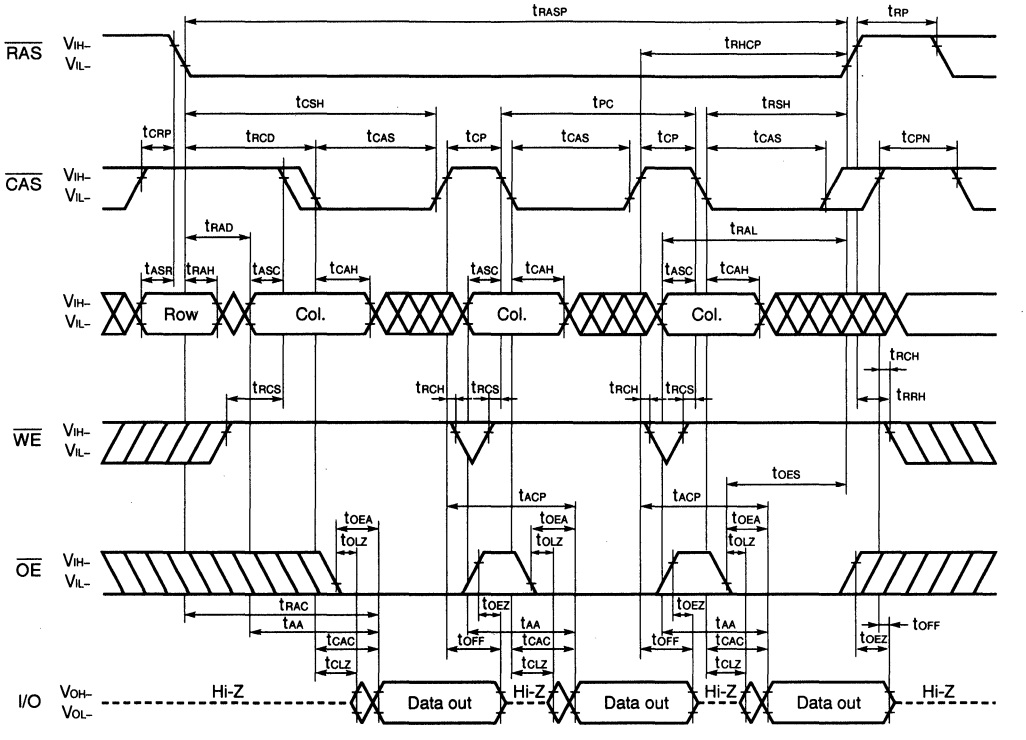
Late Write Cycle



Read Modify Write Cycle

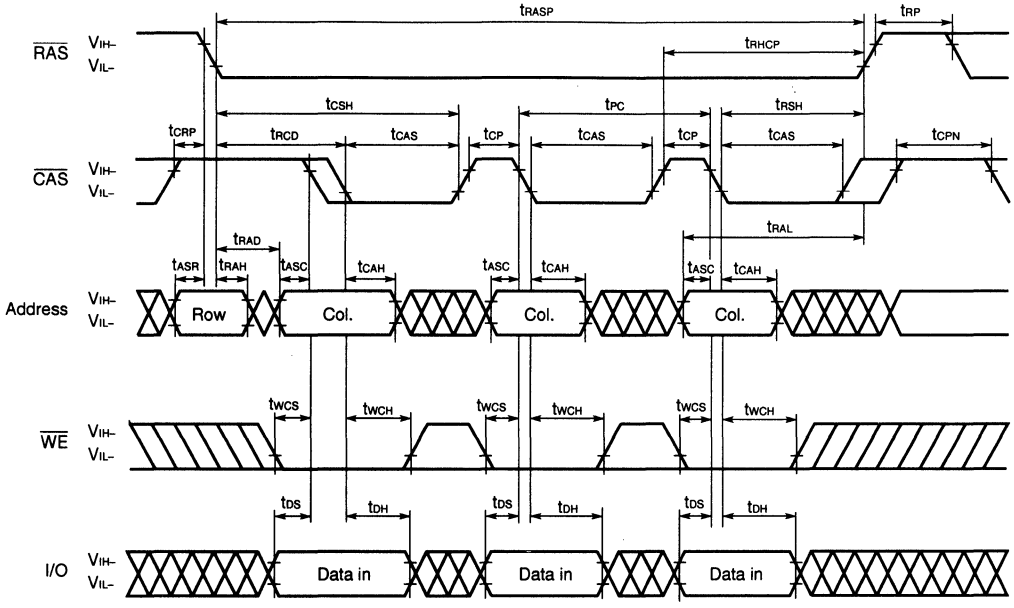


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

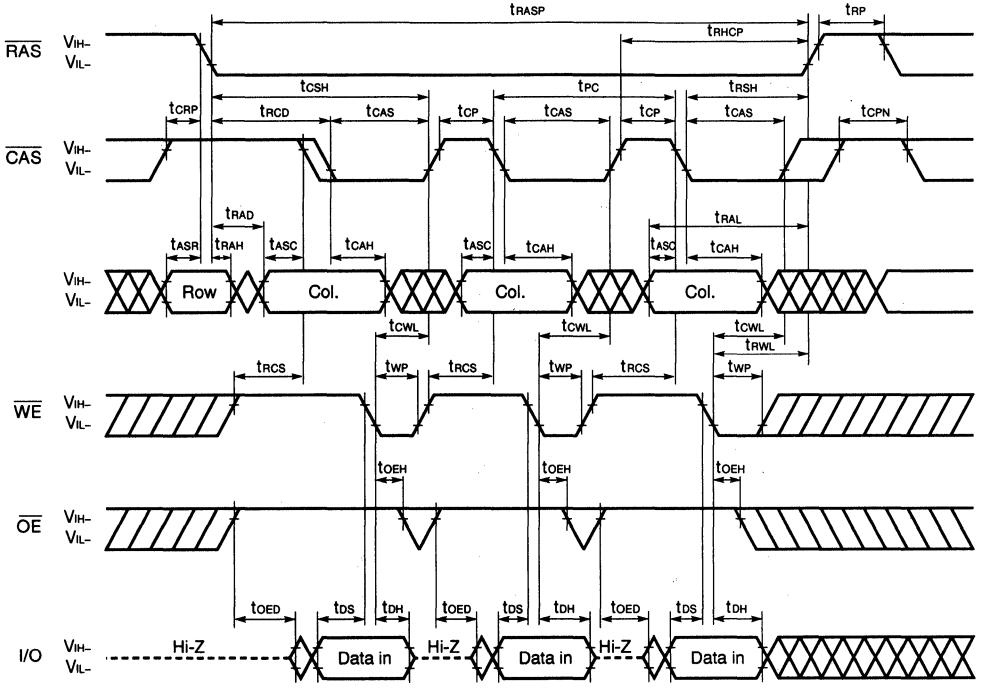
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

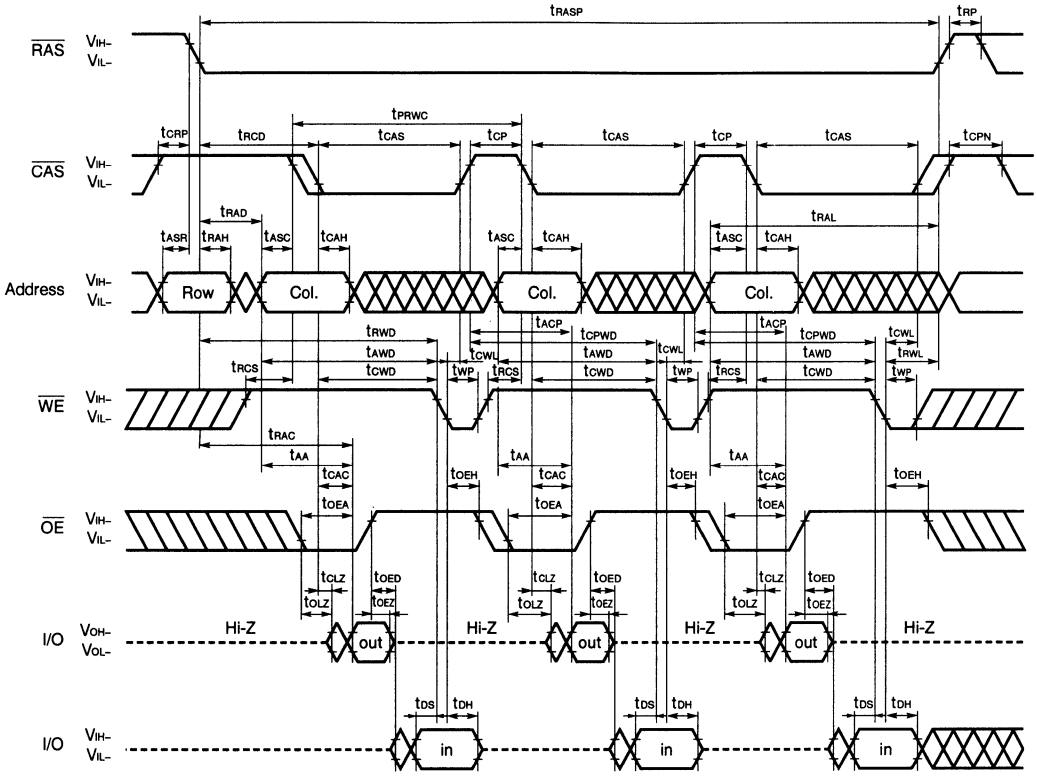
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



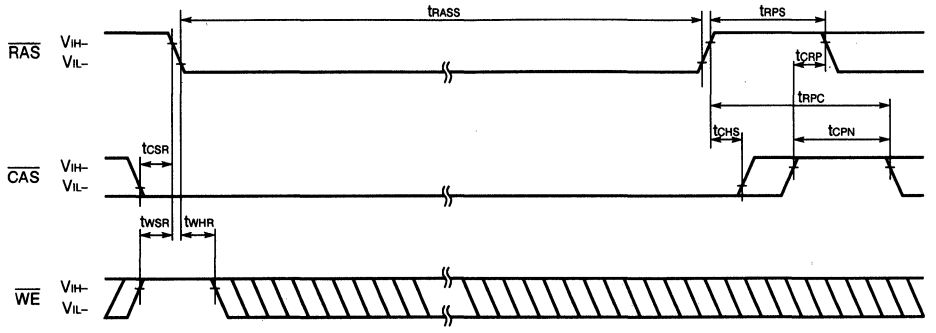
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16400, 42S17400)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S16400: 4,096 times within a 64 ms interval
μPD42S17400: 2,048 times within a 32 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

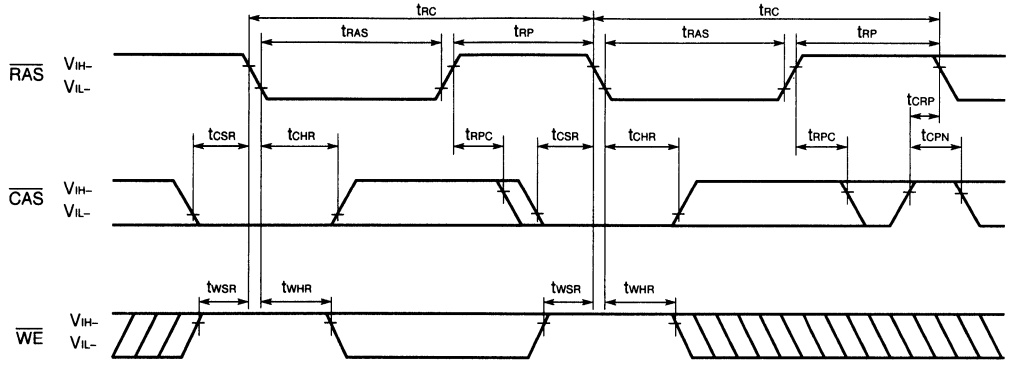
μPD42S16400: 4,096 times within a 64 ms interval
μPD42S17400: 2,048 times within a 32 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S16400: 4,096 times within a 128 ms interval
μPD42S17400: 2,048 times within a 128 ms interval

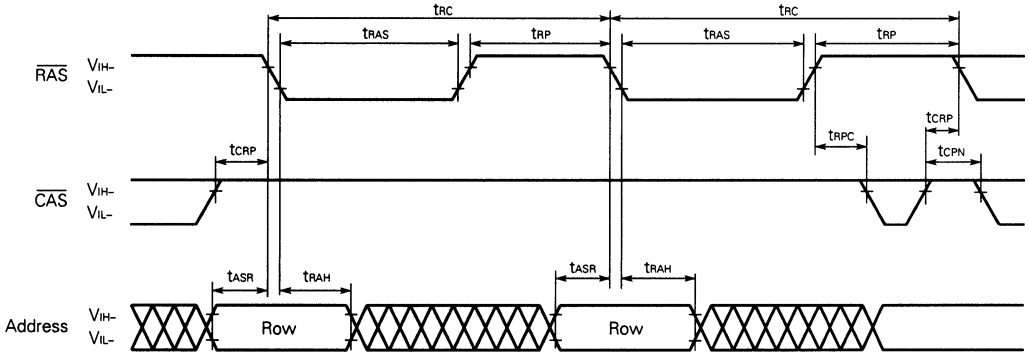
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



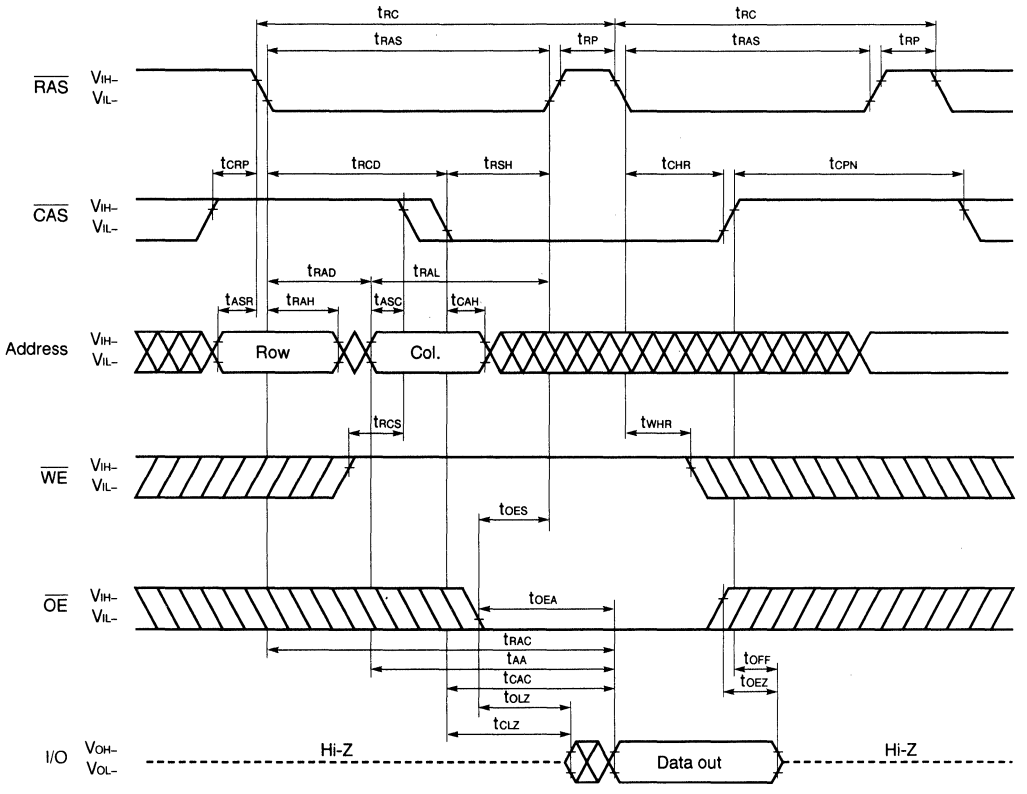
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

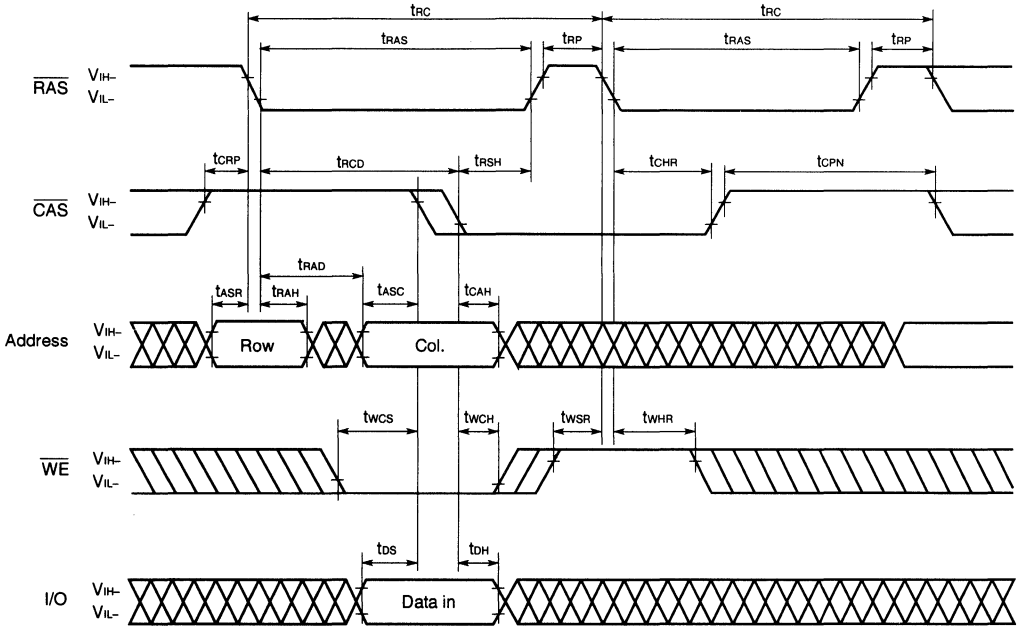


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

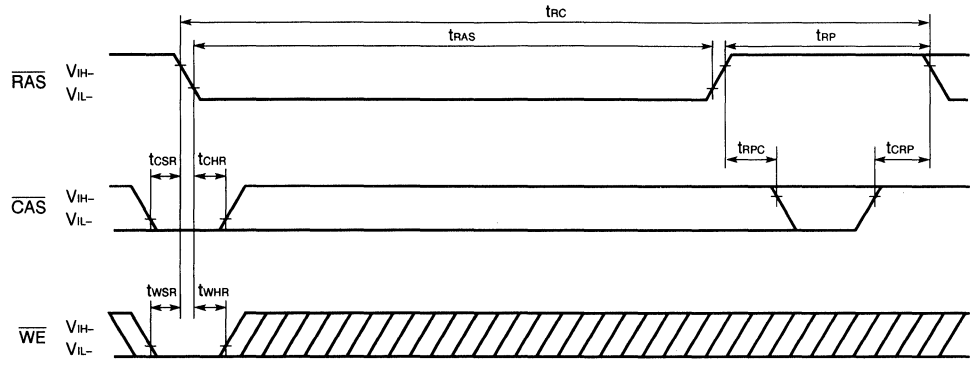


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

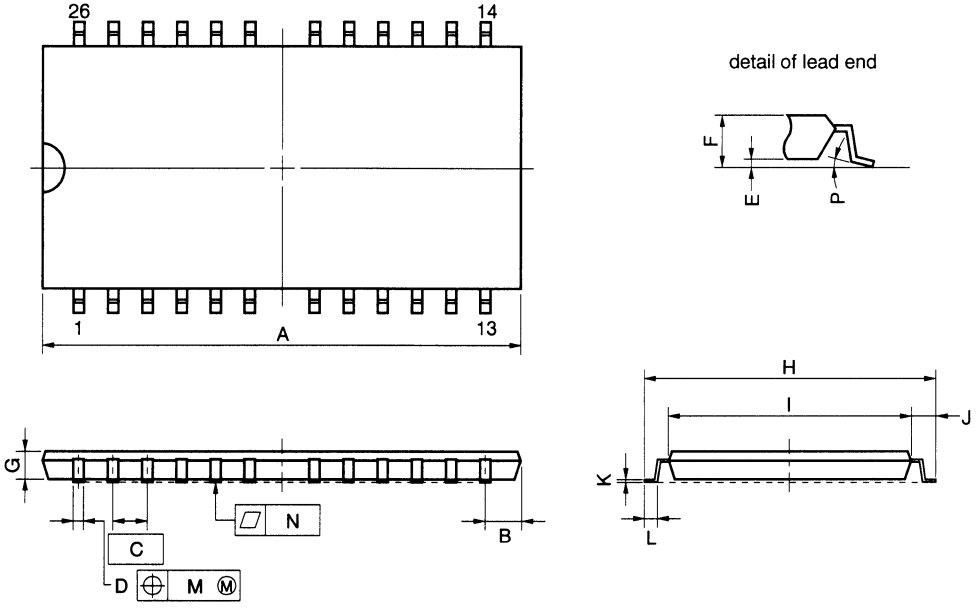
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



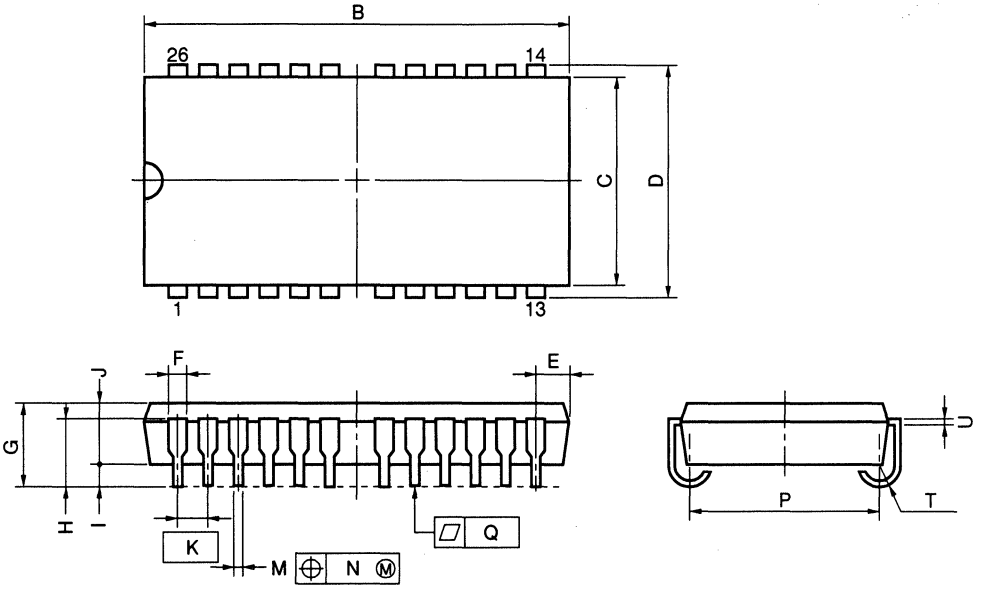
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16400, 4216400, 42S17400, 4217400.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400G3, 4216400G3, 42S17400G3, 4217400G3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16400LA, 4216400LA, 42S17400LA, 4217400LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S17800,4217800

16 M-BIT DYNAMIC RAM
2 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μPD42S17800, 4217800 are 2,097,152 words by 8 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S17800 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- 2,097,152 words by 8 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S17800-60, 4217800-60	605 mW	60 ns	110 ns	40 ns
μPD42S17800-70, 4217800-70	550 mW	70 ns	130 ns	45 ns

- The μPD42S17800 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

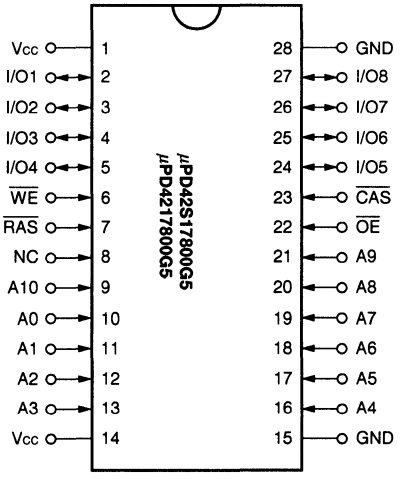
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17800	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μPD4217800	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

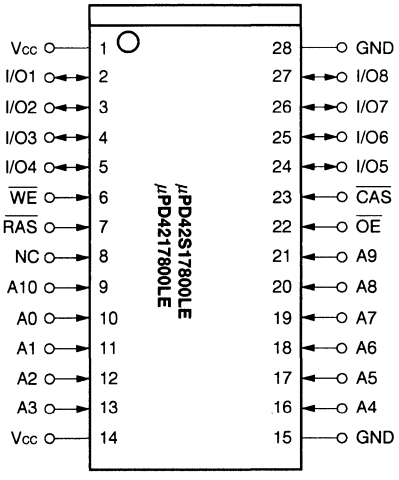
Part number	Access time (MAX.)	Package	Refresh
μPD42S17800G5-60 μPD42S17800G5-70	60 ns 70 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17800LE-60 μPD42S17800LE-70	60 ns 70 ns	28-pin plastic SOJ (400 mil)	
μPD4217800G5-60 μPD4217800G5-70	60 ns 70 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217800LE-60 μPD4217800LE-70	60 ns 70 ns	28-pin plastic SOJ (400 mil)	

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

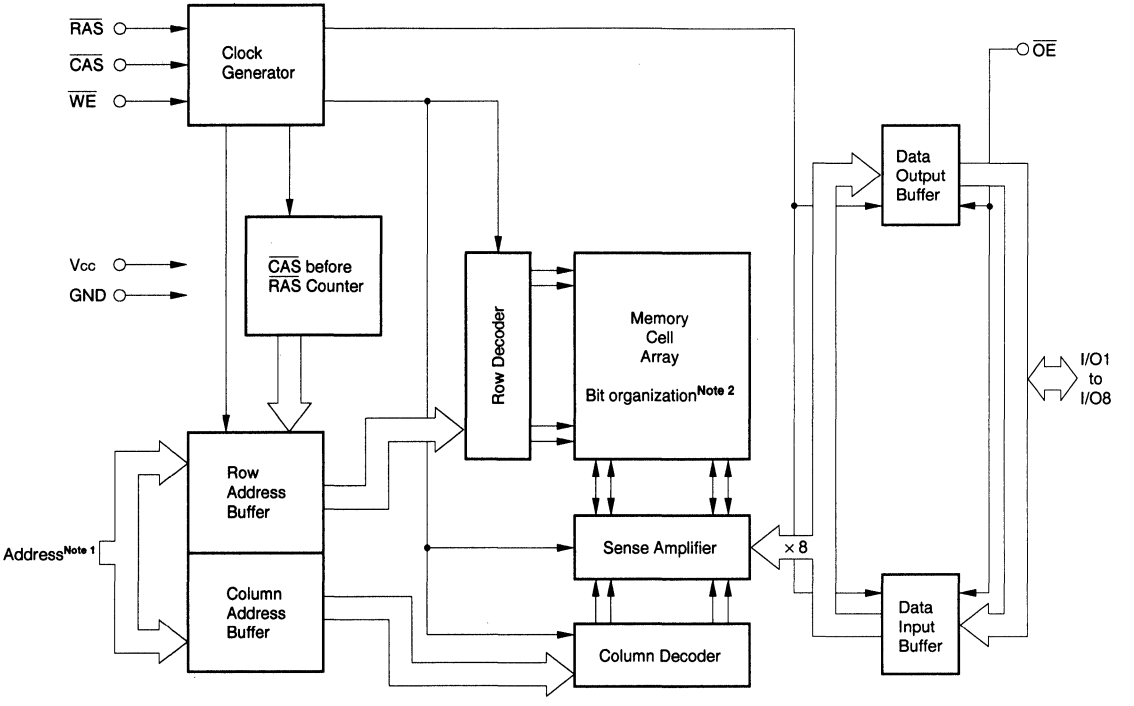


28-pin Plastic SOJ (400 mil)



A0 to A10 : Address inputs
I/O1 to I/O8: Data Inputs/Outputs
$\overline{RAS}$: Row address strobe
$\overline{CAS}$: Column address strobe
$\overline{WE}$: Write enable
$\overline{OE}$: Output enable
Vcc : Power Supply
GND : Ground
NC : No connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S17800, 4217800	A0 – A10	A0 – A9

2. μPD42S17800, 4217800...2,048×1,024×8

Input/Output Pin Functions

The μPD42S17800, 4217800 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 21-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 2,097,152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD42S17800, 4217800	A0 – A10	11 bits	10 bits

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\ (MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

[MEMO]

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA				mA	1, 2, 3
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Standby current	μPD42S17800	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.25		
	μPD4217800		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA				mA	1, 2, 3, 4
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA				mA	1, 2, 5
				t_{RAC} = 60 ns		70		
				t_{RAC} = 70 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA				mA	1, 2
				t_{RAC} = 60 ns		110		
				t_{RAC} = 70 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17800)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V	$t_{RAS} \leq$ 300 ns		400	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq$ 1 μs		500	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17800)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH(MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

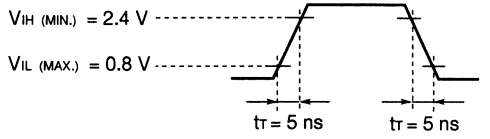
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

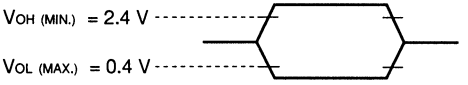
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

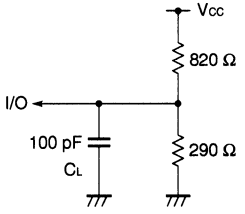
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	18	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	18	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	ns	
Refresh time	μPD42S17800	tREF	–	128	–	128	ms	
	μPD4217800		–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	158	–	180	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83	–	95	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	38	–	43	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	53	–	60	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	ns	1

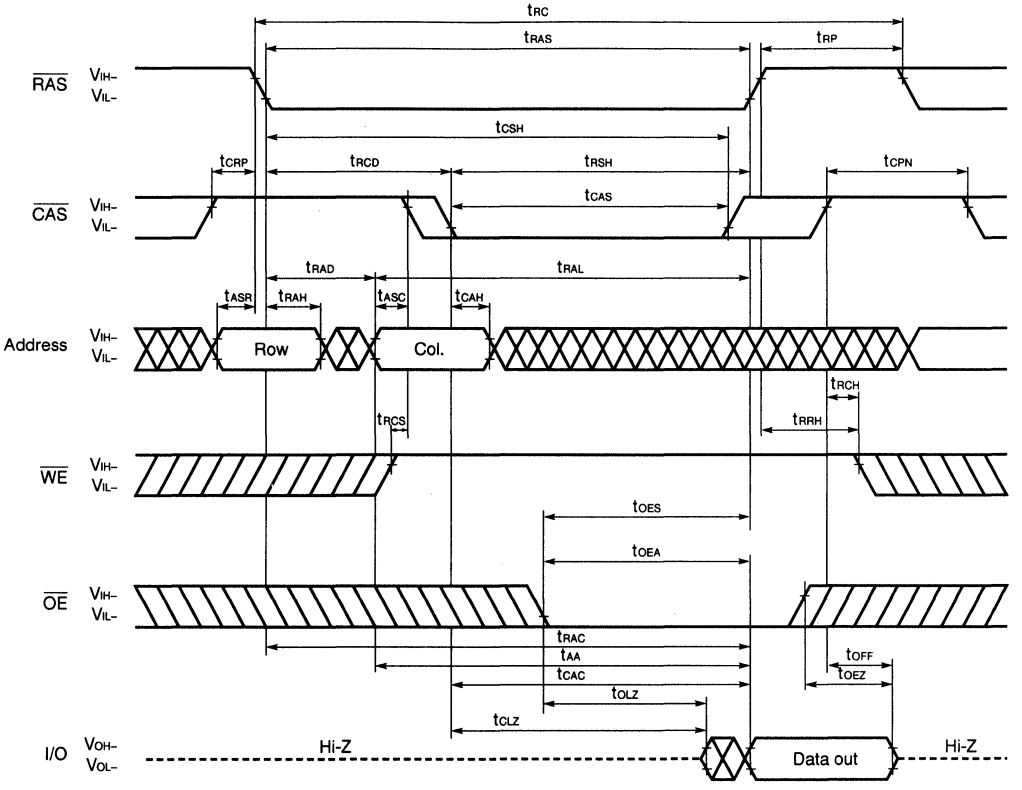
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

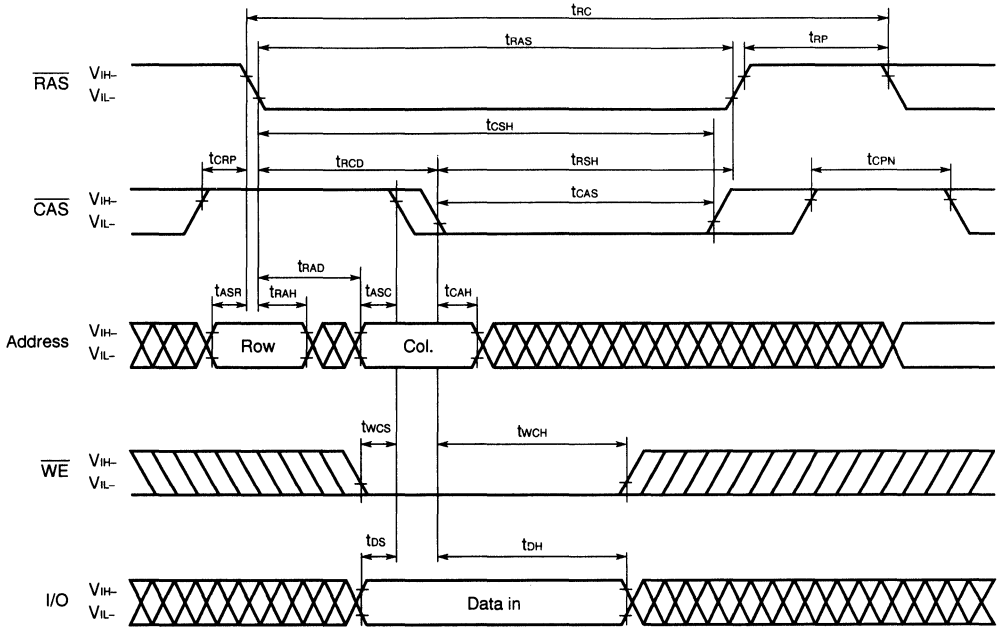
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17800.

Read Cycle

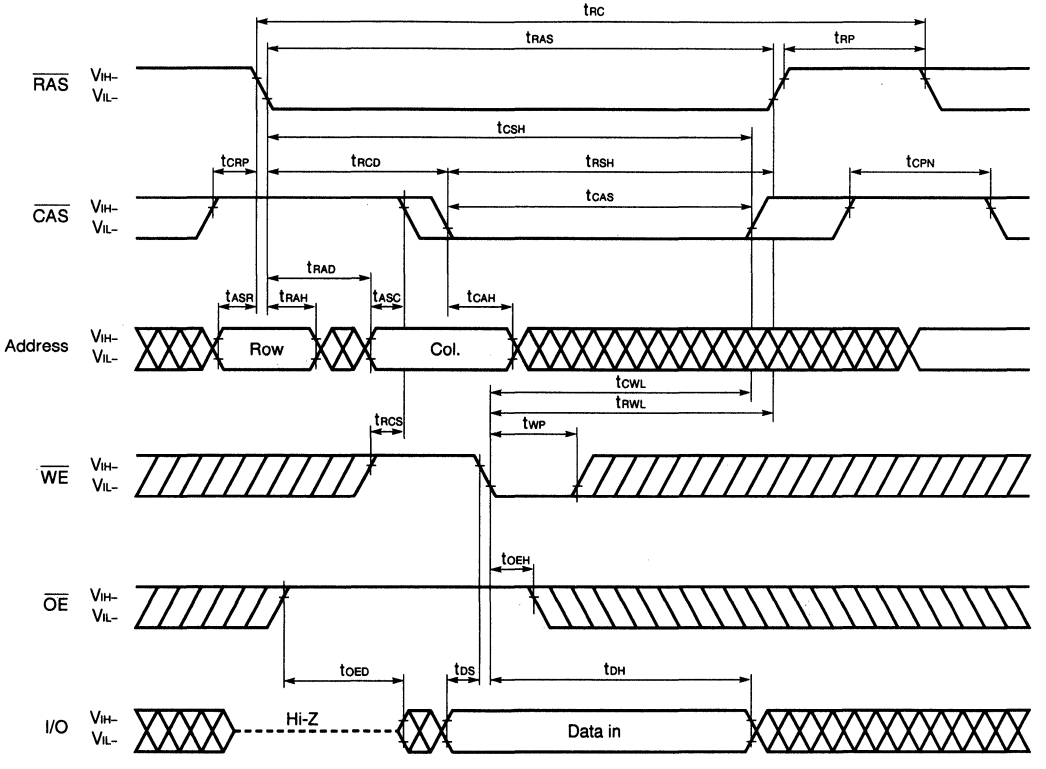

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tCAC
tOFF
tOEZ
tOLZ
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

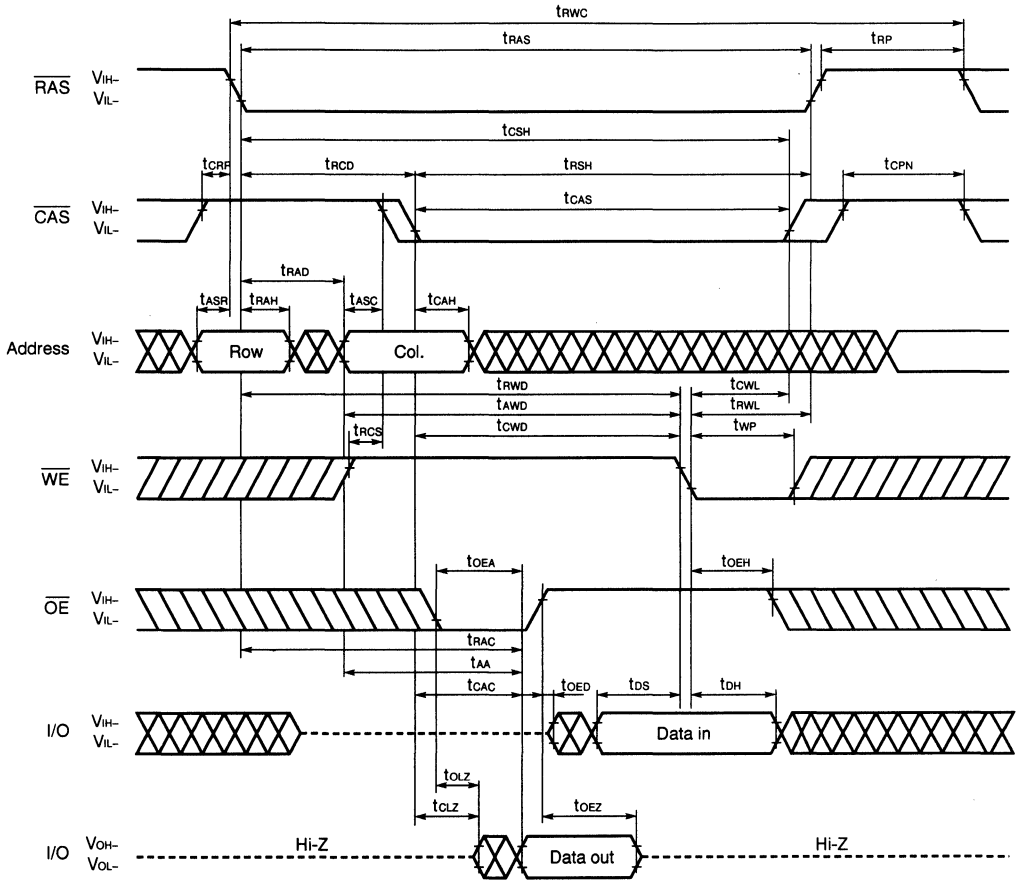


Remark $\overline{OE}$: Don't care

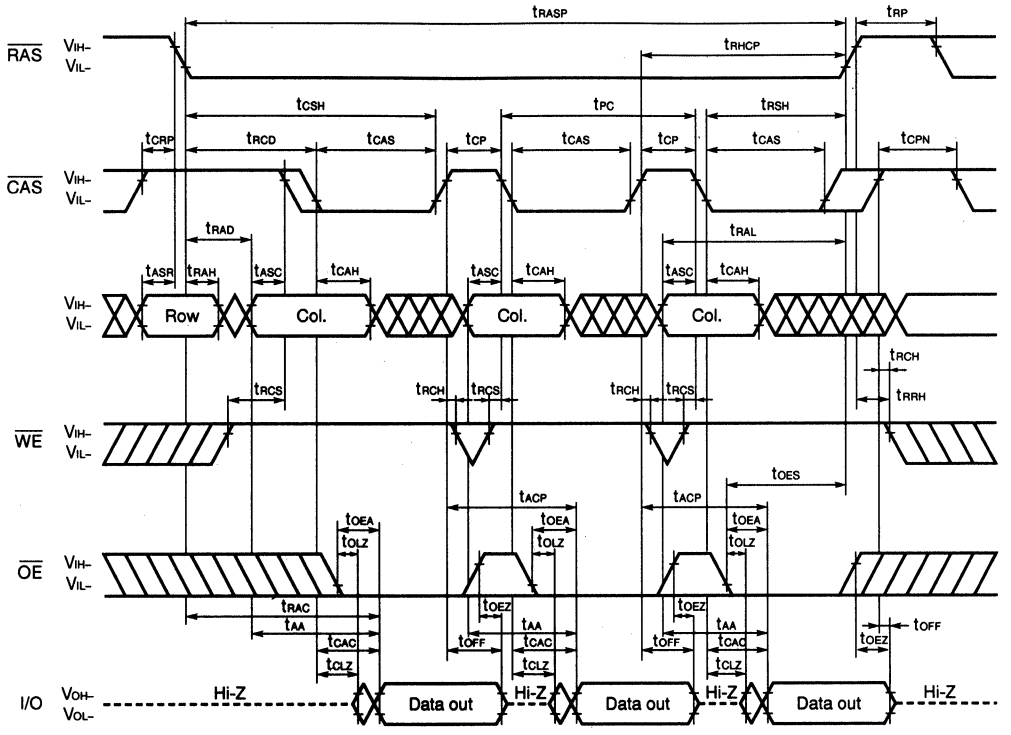
Late Write Cycle



Read Modify Write Cycle

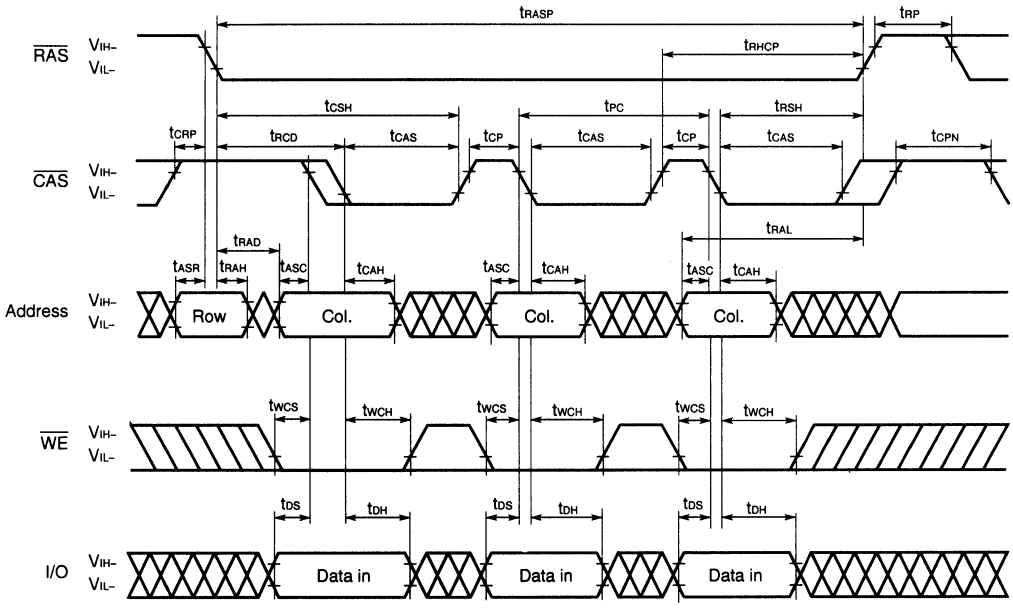


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

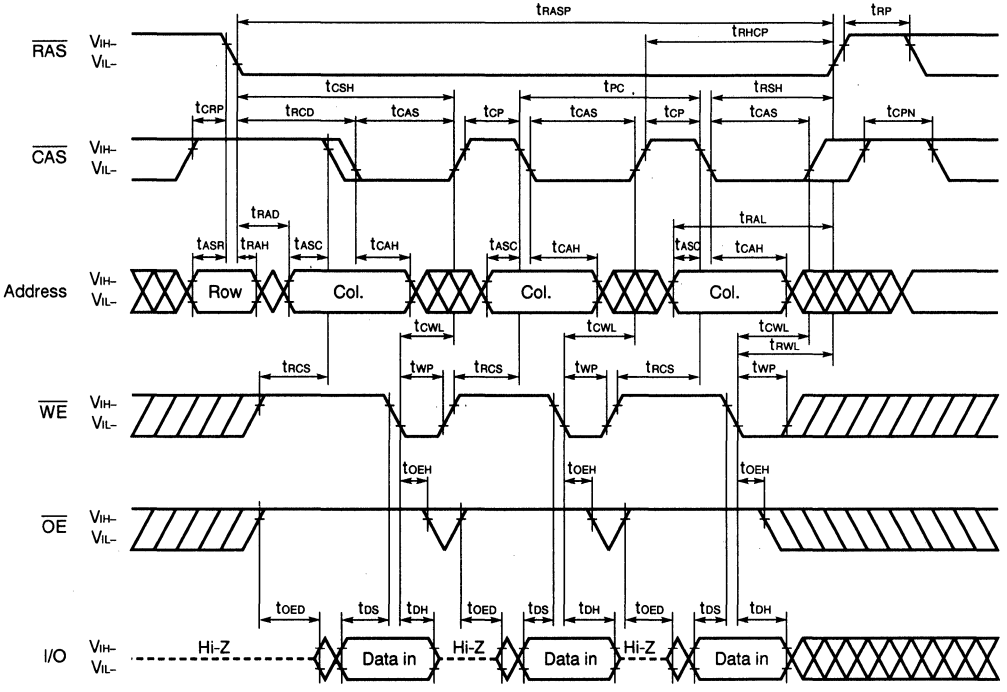
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

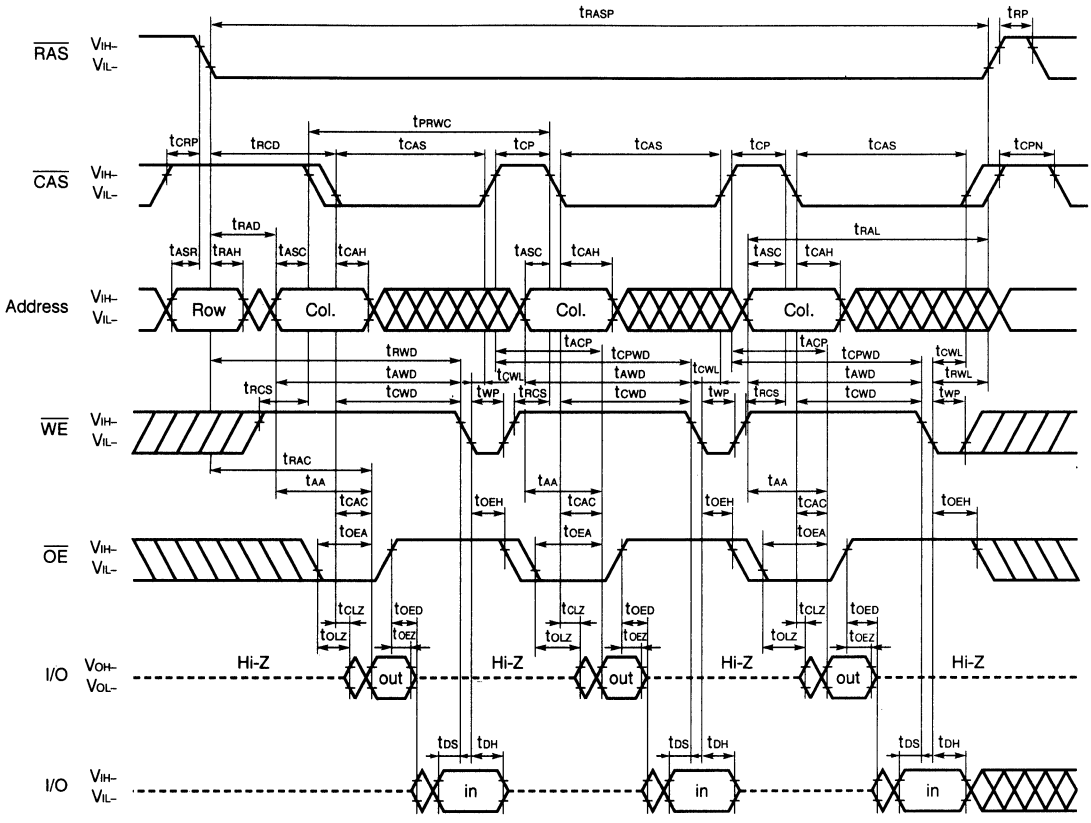
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



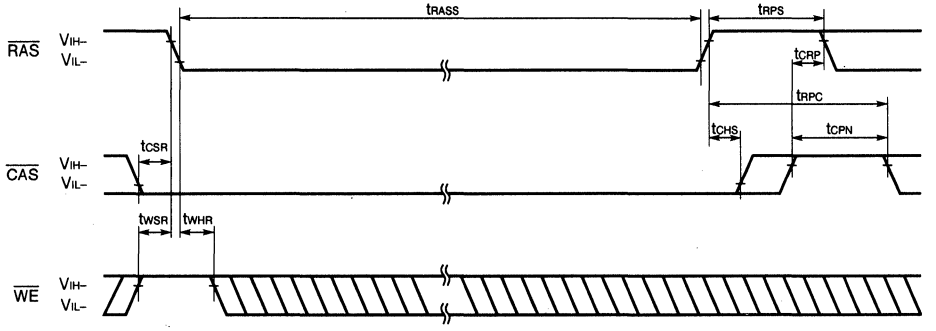
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17800)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S17800: 2,048 times within a 32 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

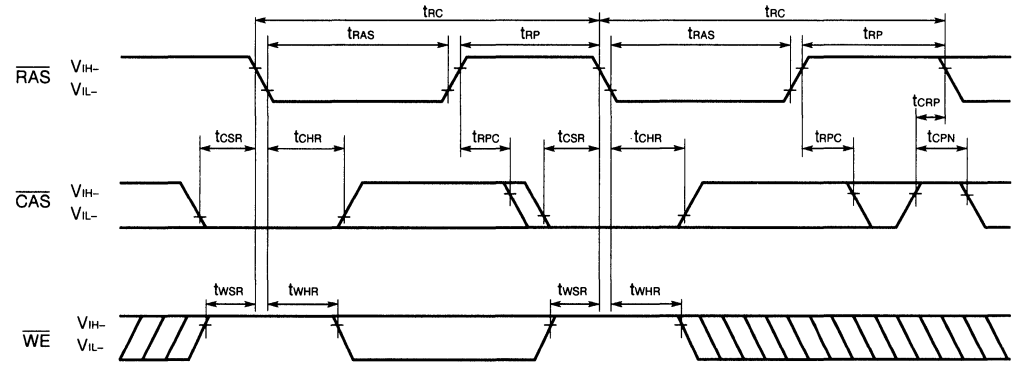
μPD42S17800: 2,048 times within a 32 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S17800: 2,048 times within a 128 ms interval

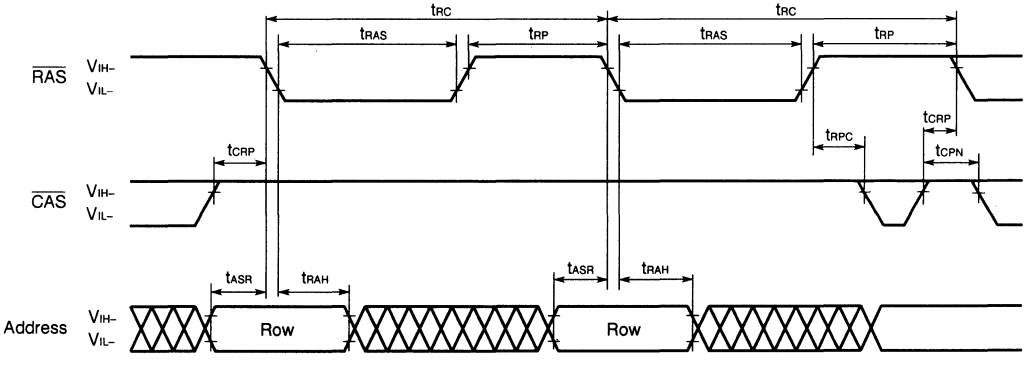
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



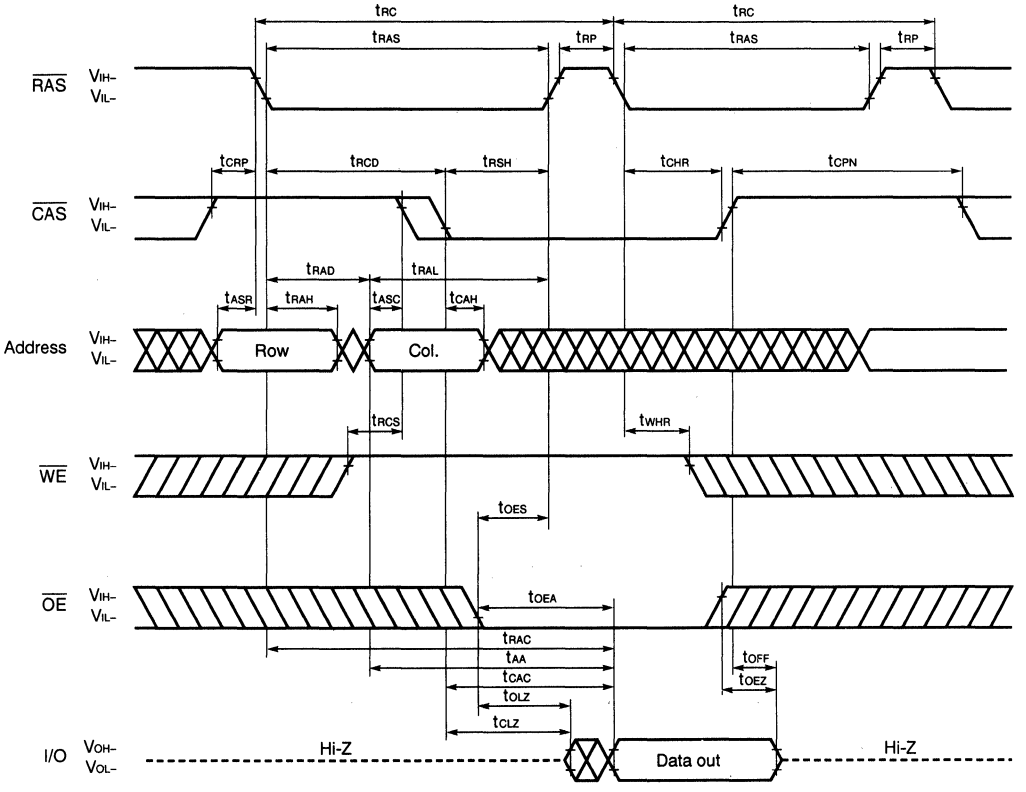
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

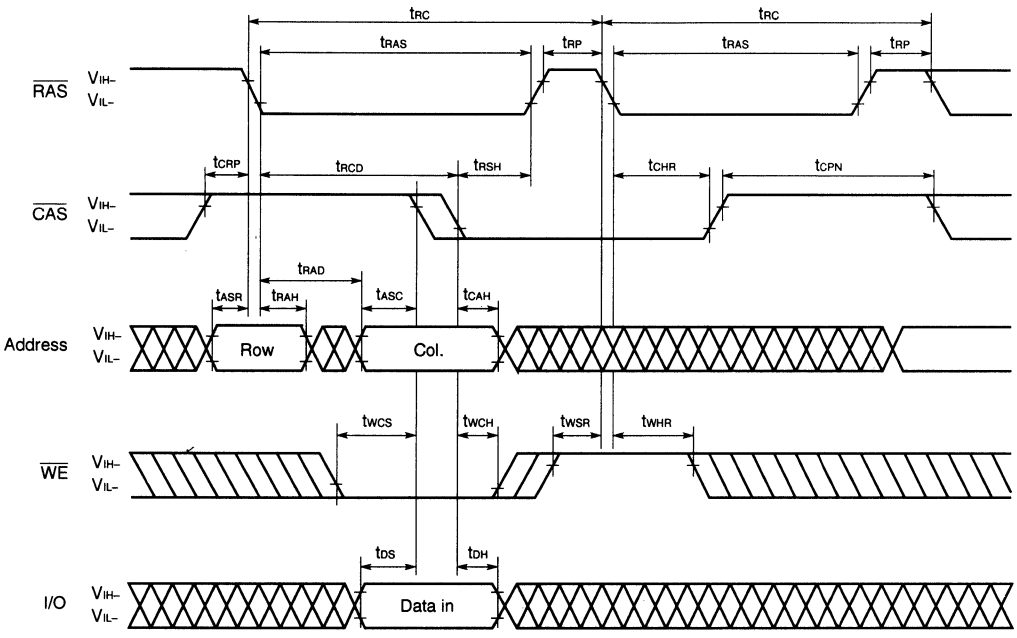


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

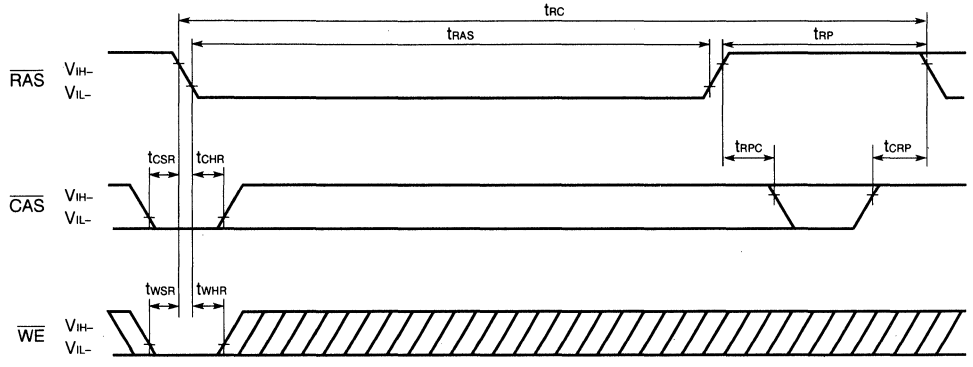


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input level of the $\overline{CAS}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

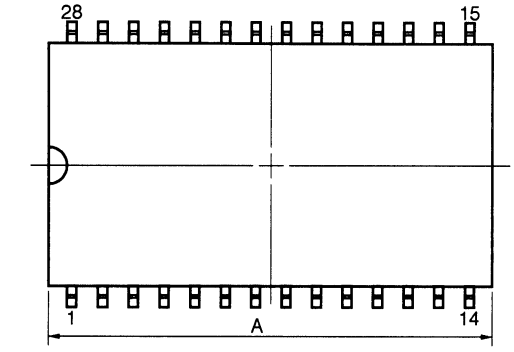
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

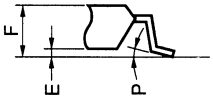
The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

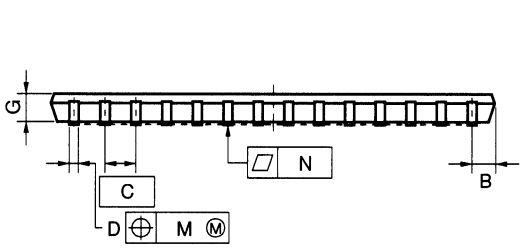
Package Drawings

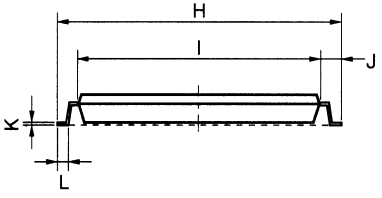
28PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







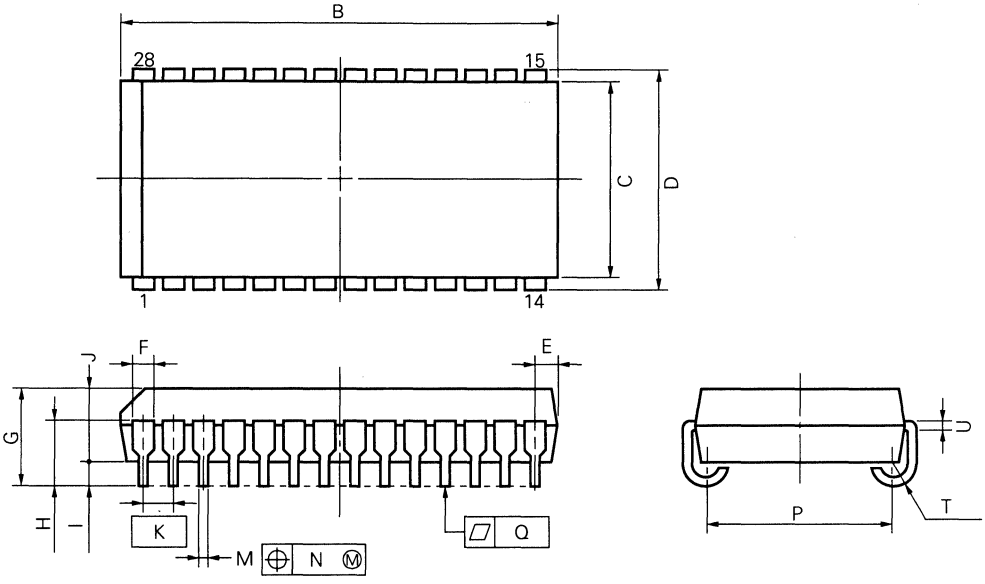
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17800, 4217800.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17800G5, 4217800G5: 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S17800LE, 4217800LE: 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S18160, 4218160

16 M-BIT DYNAMIC RAM
1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S18160, 4218160 are 1,048,576 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S18160 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

Features

- 1,048,576 words by 16 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S18160-60, 4218160-60	880 mW	60 ns	110 ns	40 ns
μPD42S18160-70, 4218160-70	825 mW	70 ns	130 ns	45 ns

- The μPD42S18160 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

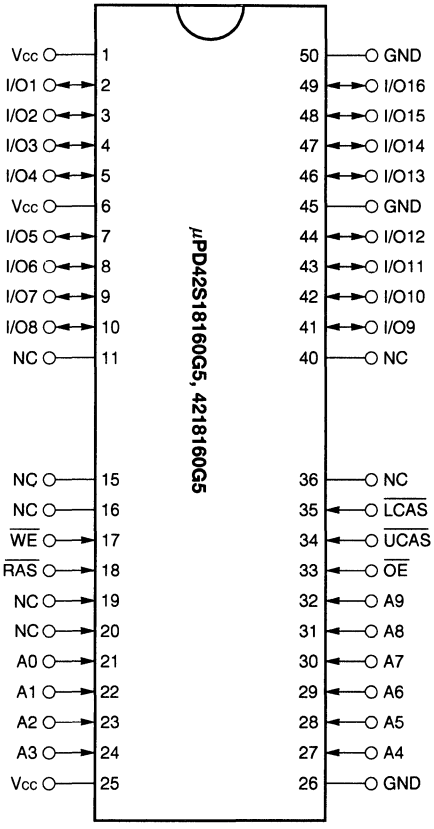
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S18160	1,024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
μPD4218160	1,024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

Ordering Information

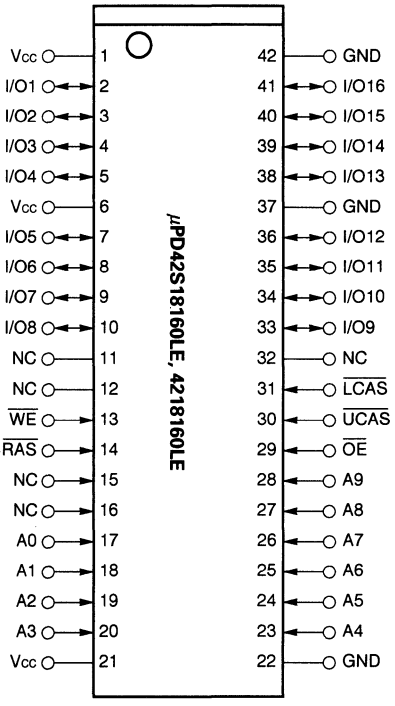
Part number	Access time (MAX.)	Package	Refresh
μPD42S18160G5-60 μPD42S18160G5-70	60 ns 70 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18160LE-60 μPD42S18160LE-70	60 ns 70 ns	42-pin plastic SOJ (400 mil)	
μPD4218160G5-60 μPD4218160G5-70	60 ns 70 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218160LE-60 μPD4218160LE-70	60 ns 70 ns	42-pin plastic SOJ (400 mil)	

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II)(400 mil)

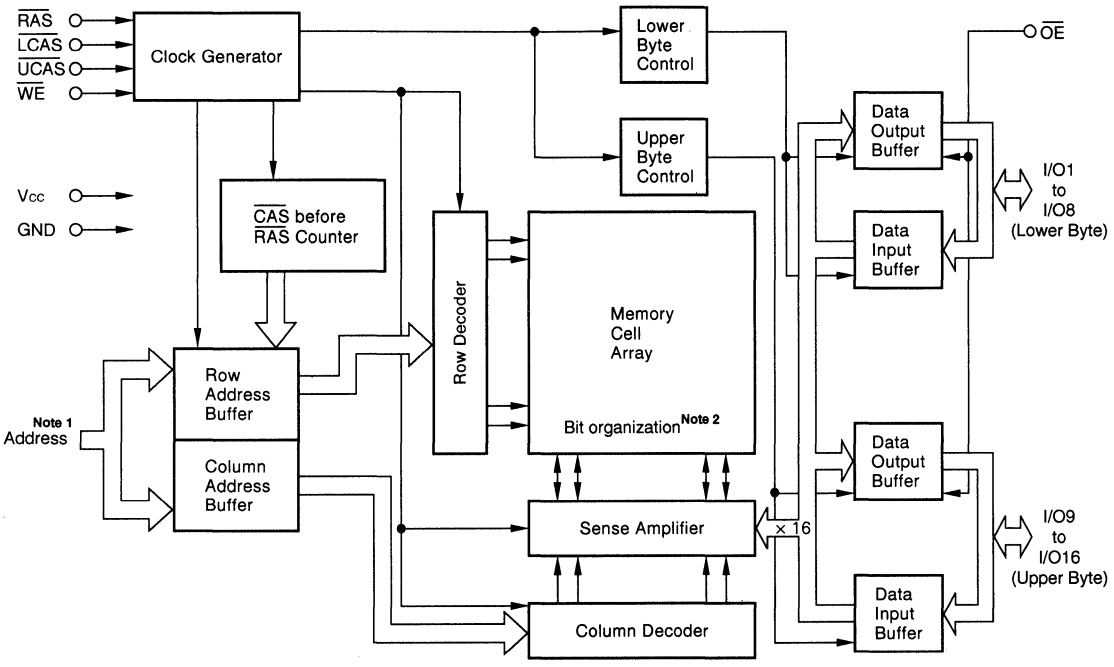


42-pin Plastic SOJ (400 mil)



A0 to A9	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S18160, 4218160	A0 - A9	A0 - A9

2. μPD42S18160, 4218160 ··· 1,024 × 1,024 × 16

Input/Output Pin Functions

The μPD42S18160, 4218160 have input pins $\overline{RAS}$, $\overline{CAS}$[Note 1], $\overline{WE}$, $\overline{OE}$, Address[Note 2] and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9[Note 2] (Address input)	Input	Address bus. Input total 20-bit of address signal, upper bits and lower bits[Note 2] in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/ output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2.

Part number	Address inputs	Upper bits	Lower bits
μPD42S18160, 4218160	A0 - A9	10 bits	10 bits

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

[MEMO]

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling				mA	1, 2, 3
			$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		160		
			I_O = 0 mA	t_{RAC} = 70 ns		150		
Standby current	μPD42S18160	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			0.25		
	μPD4218160		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$				mA	1, 2, 3, 4
			$t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		160		
				t_{RAC} = 70 ns		150		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling				mA	1, 2, 5
			$t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90		
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling				mA	1, 2
			$t_{RC} = t_{RC\ (MIN.)}$	t_{RAC} = 60 ns		160		
			I_O = 0 mA	t_{RAC} = 70 ns		150		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18160)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs; $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V	$t_{RAS} \leq$ 300 ns		350	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V; Address: V_{IH} or V_{IL}; $\overline{WE}$, $\overline{OE}$: V_{IH}; I_O = 0 mA	$t_{RAS} \leq$ 1 μs		400	μA	1, 2
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μPD42S18160)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V; I_O = 0 mA			250	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V; All other pins not under test = 0 V		–10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V; Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.1 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

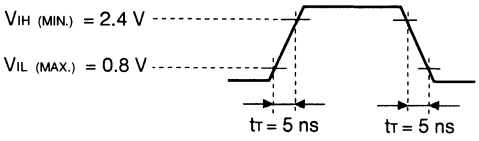
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

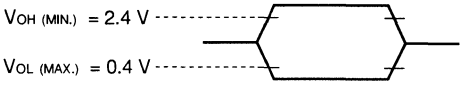
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

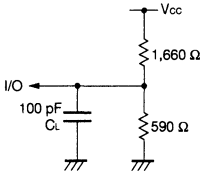
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	18	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	50	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		tMRH	0	–	0	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	ns	
Refresh time	μPD42S18160	tREF	–	128	–	128	ms	
	μPD4218160		–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	158	–	180	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83	–	95	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	38	–	40	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	53	–	60	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	ns	1

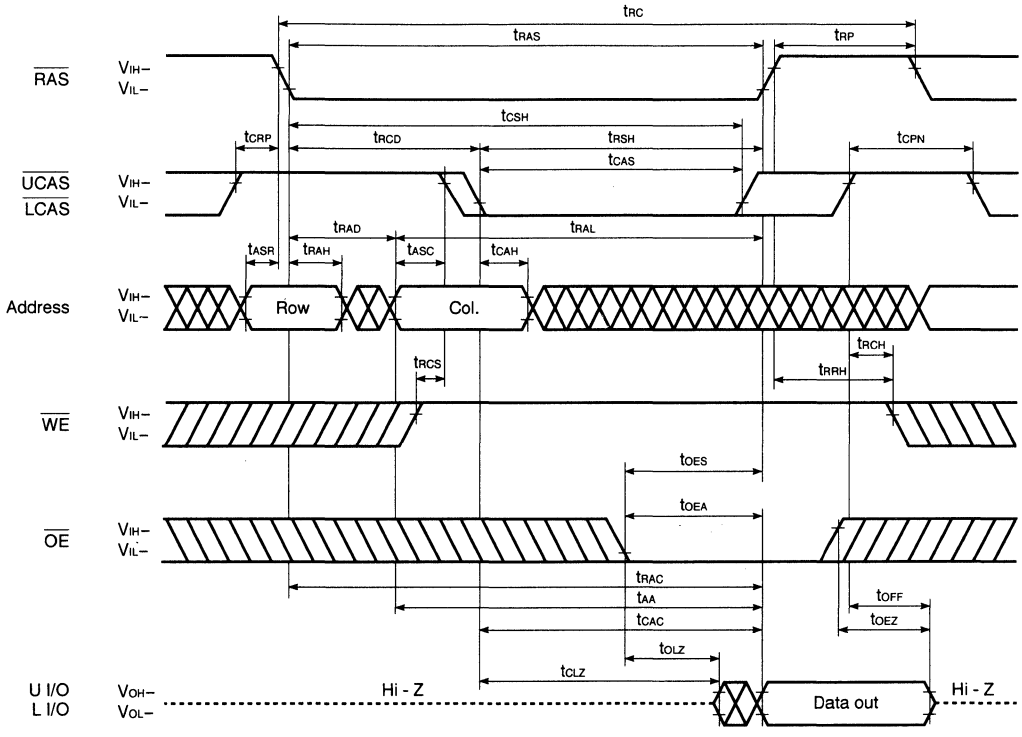
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

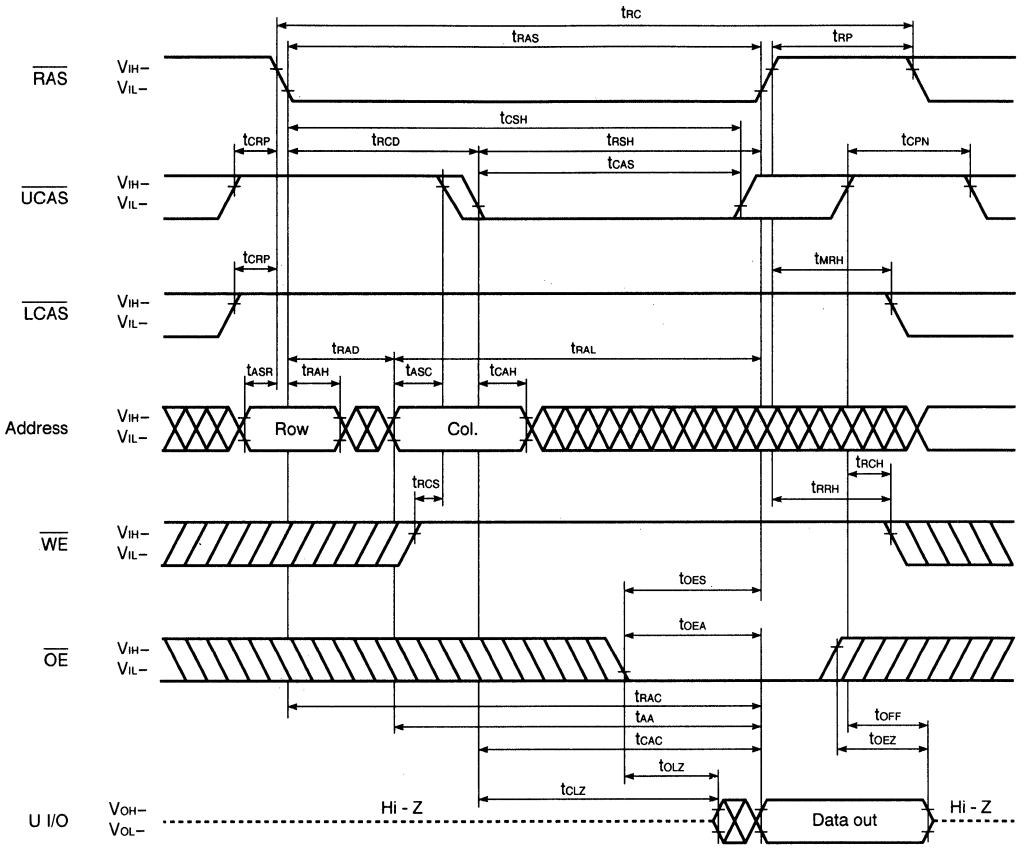
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S18160.

Read Cycle

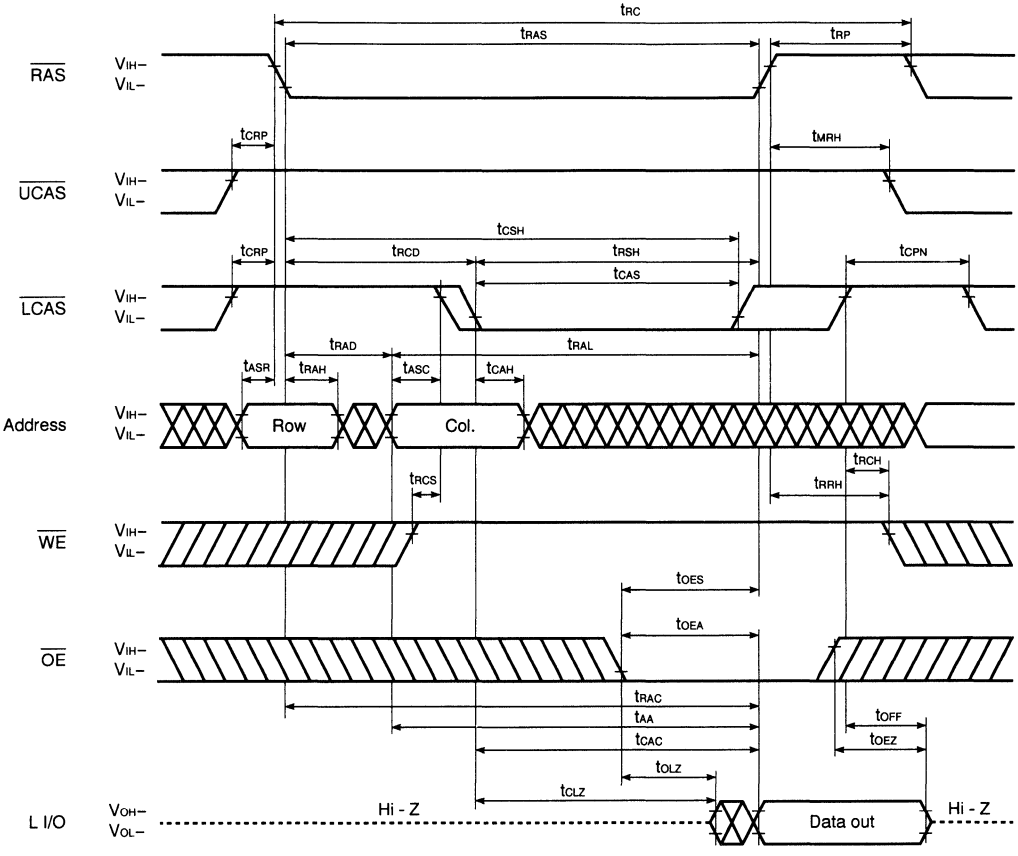

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tOEZ
tCAC
tOLZ
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



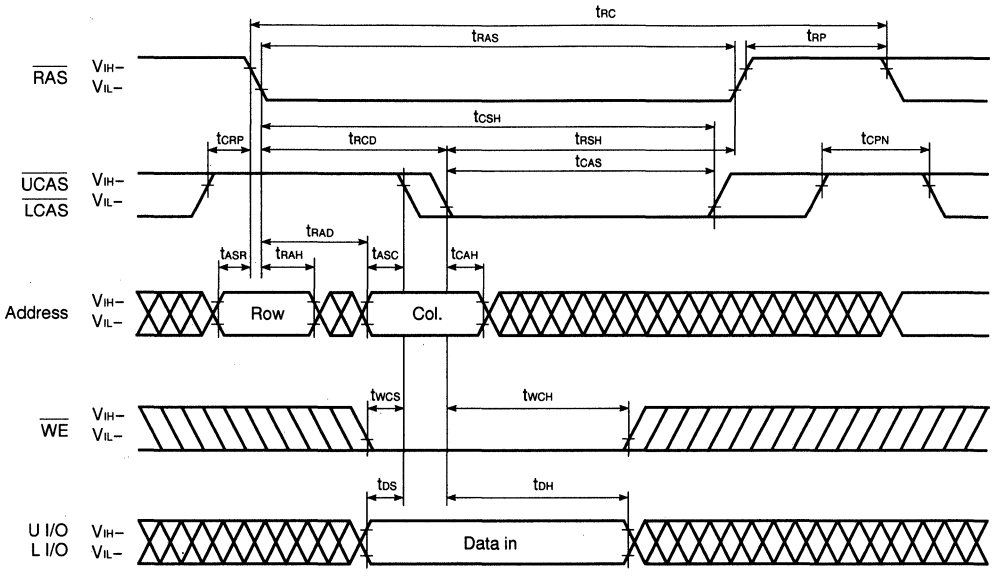
Remark L I/O: Hi-Z

Lower Byte Read Cycle



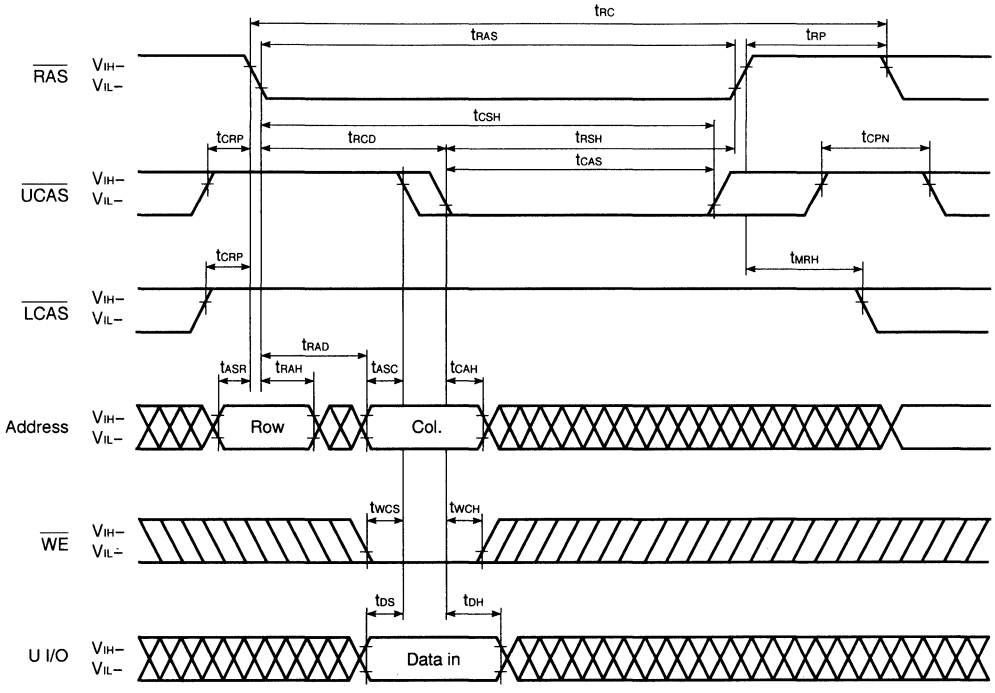
Remark U I/O: Hi-Z

Early Write Cycle



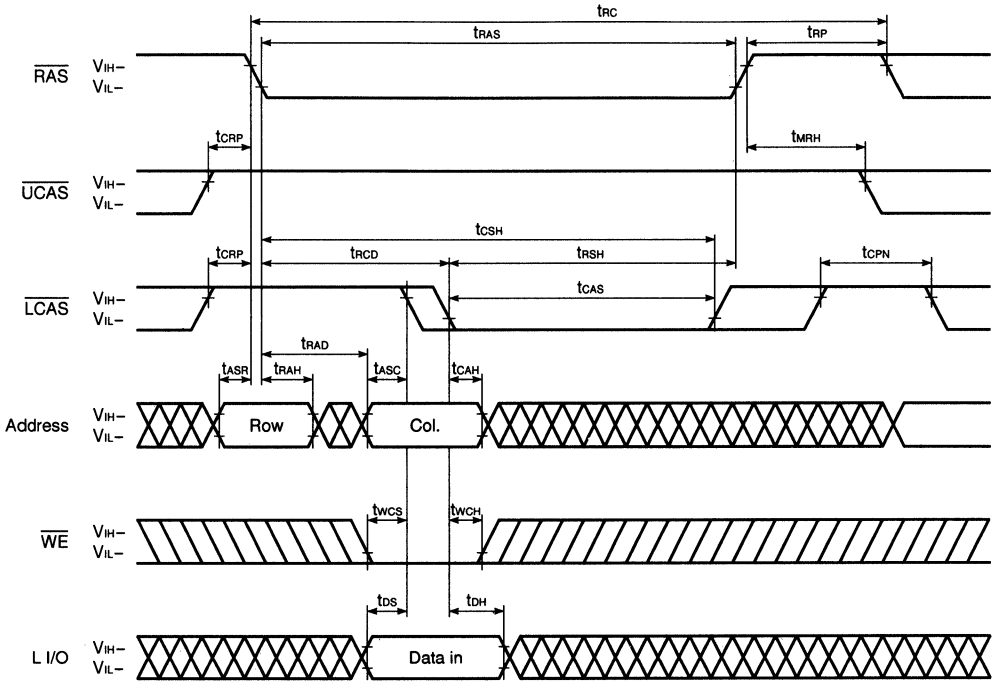
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



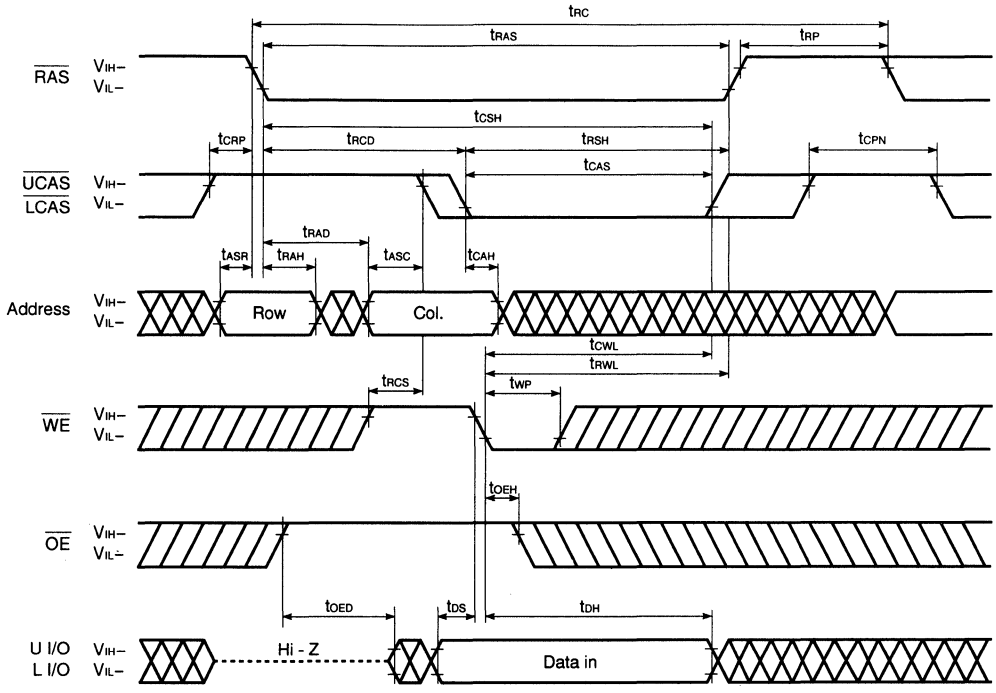
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

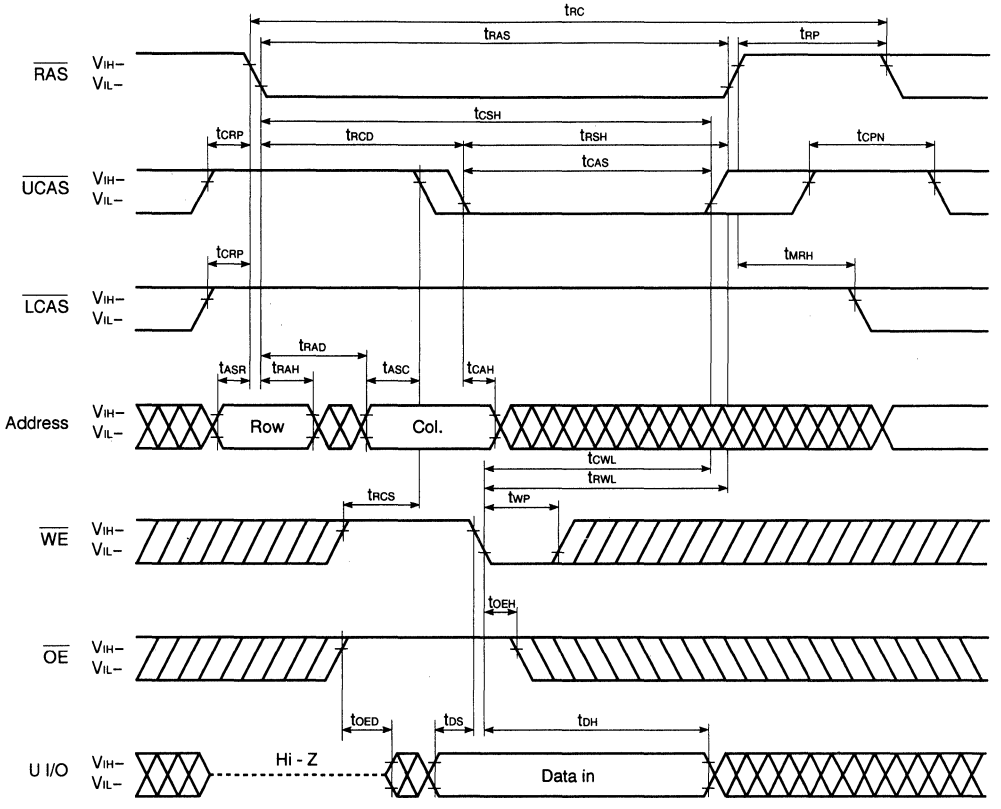


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

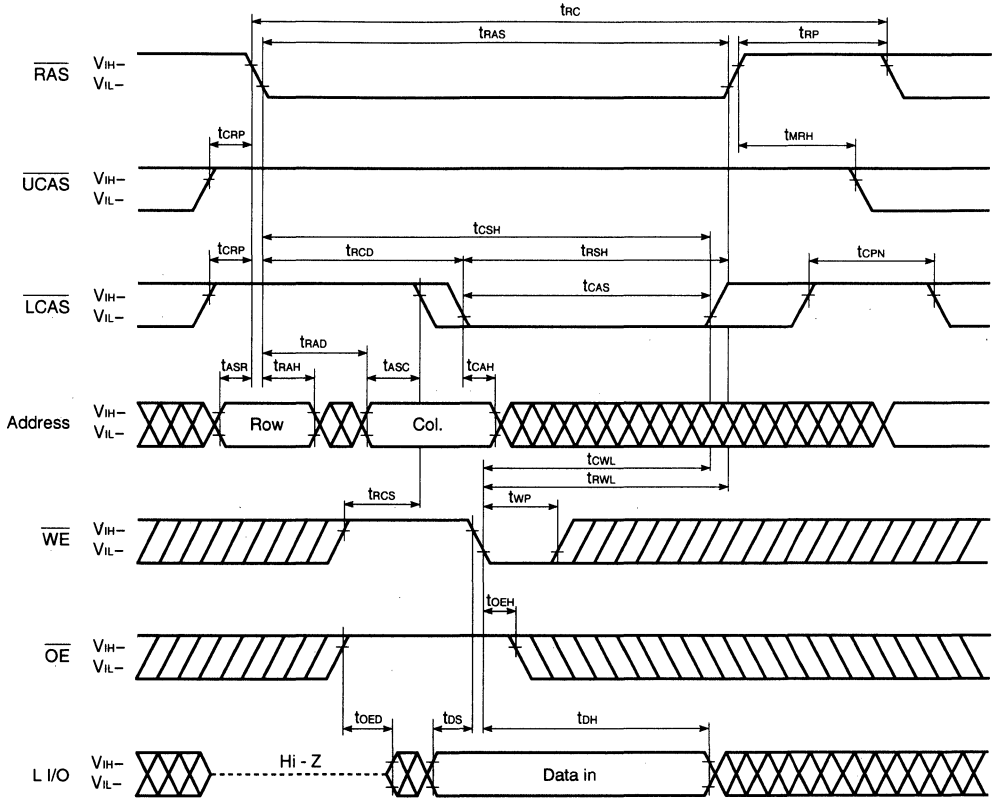


Upper Byte Late Write Cycle



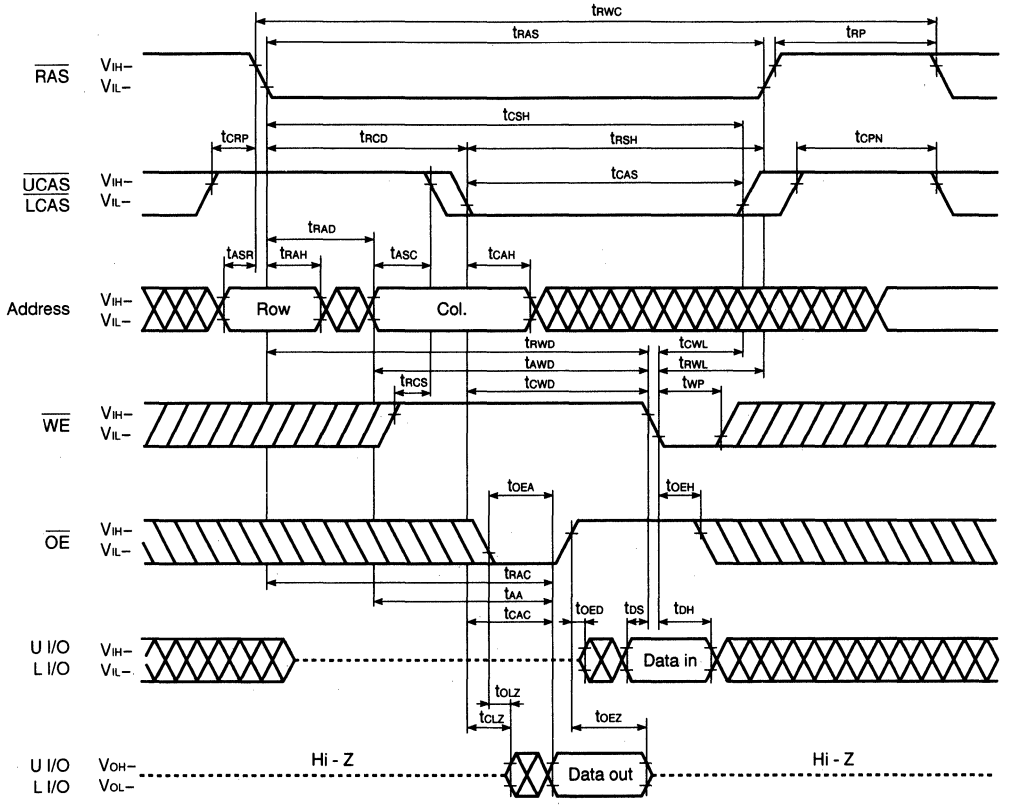
Remark L I/O: Don't care

Lower Byte Late Write Cycle

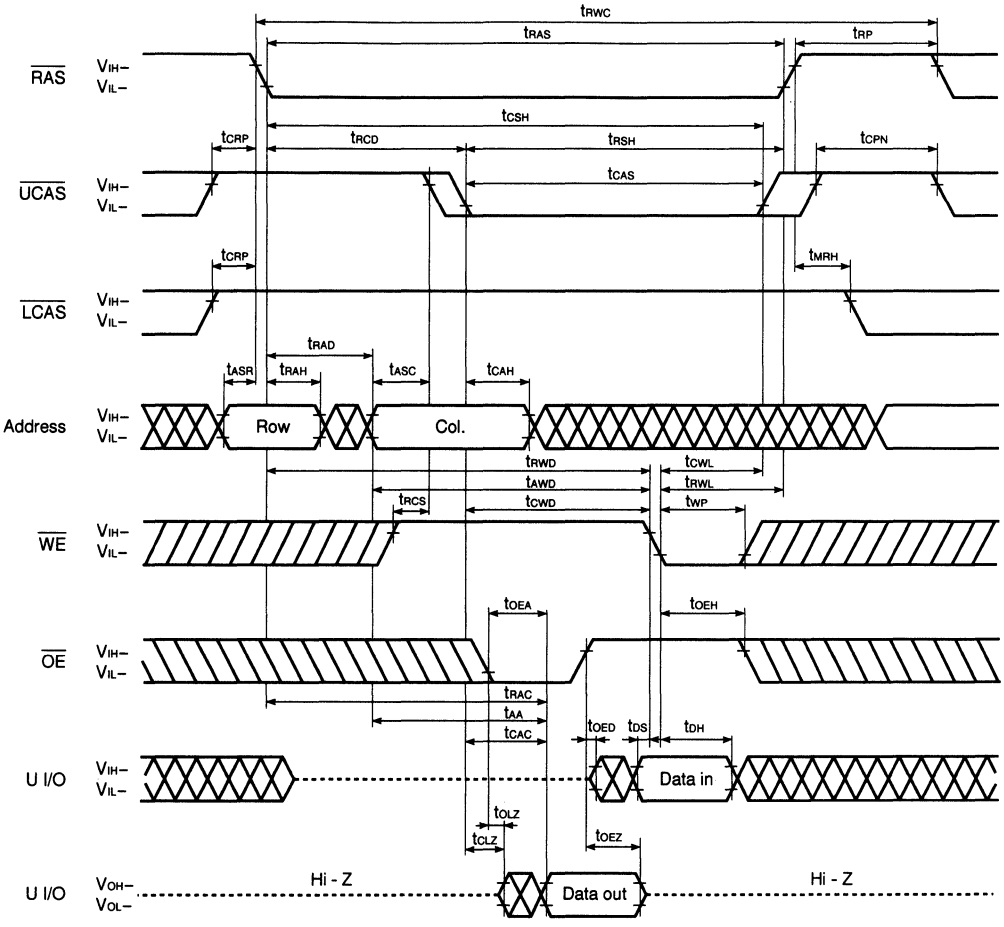


Remark U I/O: Don't care

Read Modify Write Cycle

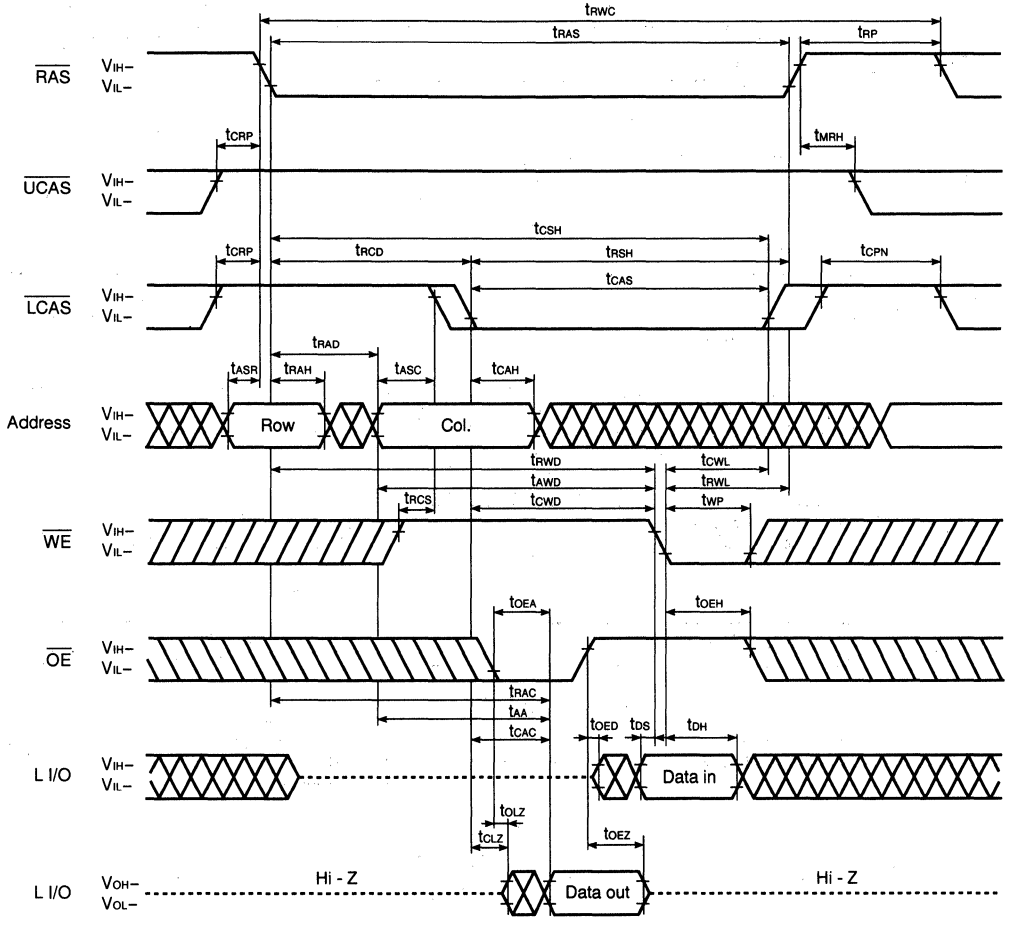


Upper Byte Read Modify Write Cycle



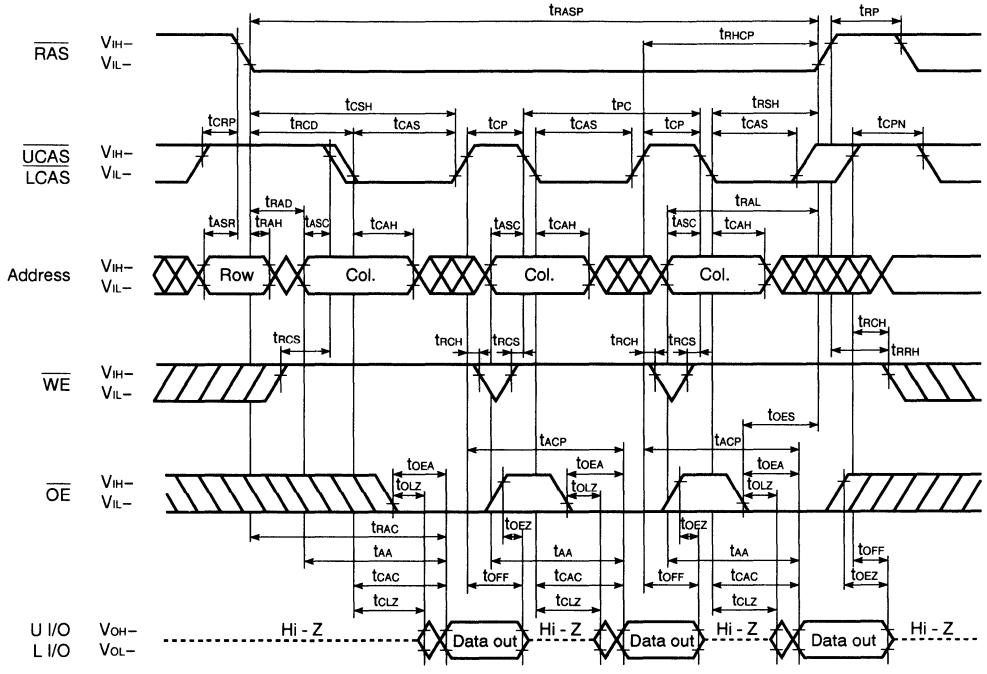
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



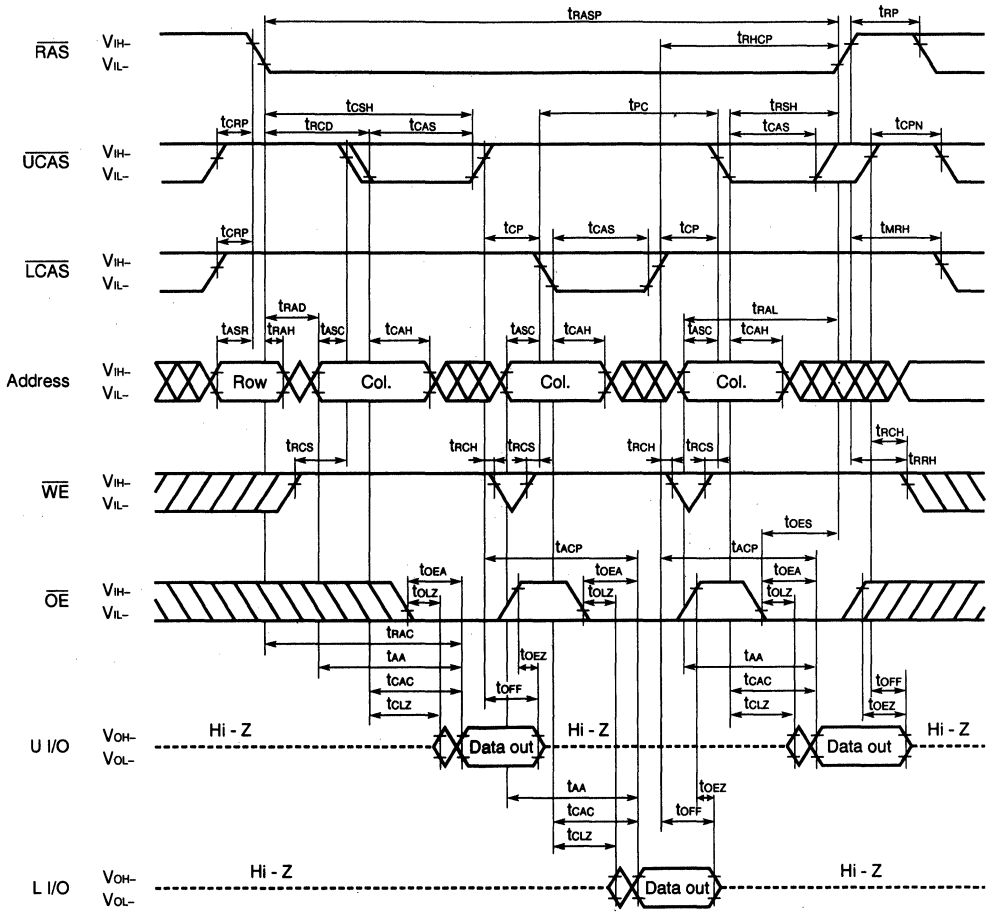
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

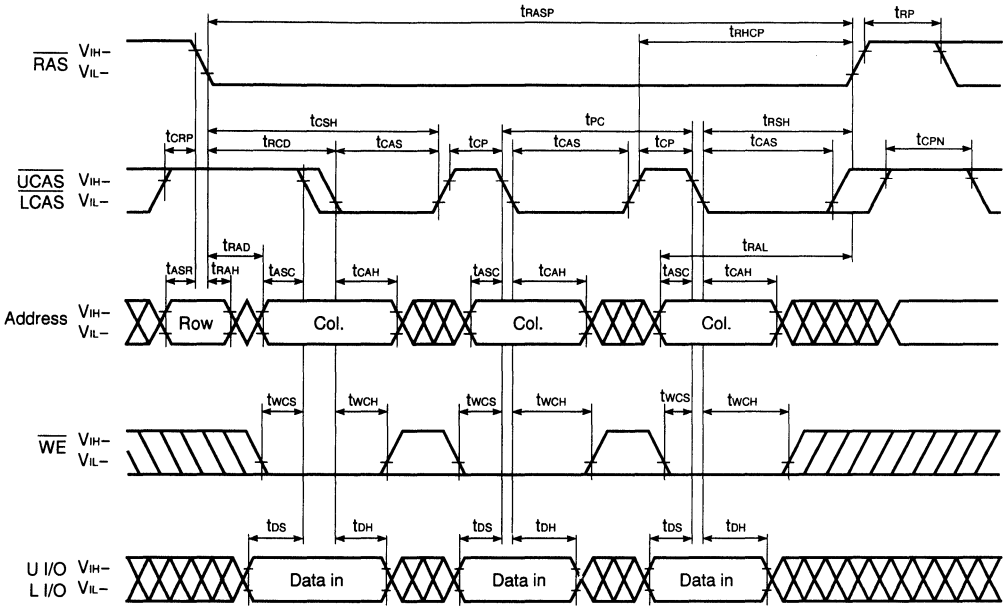
Fast Page Mode Byte Read Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

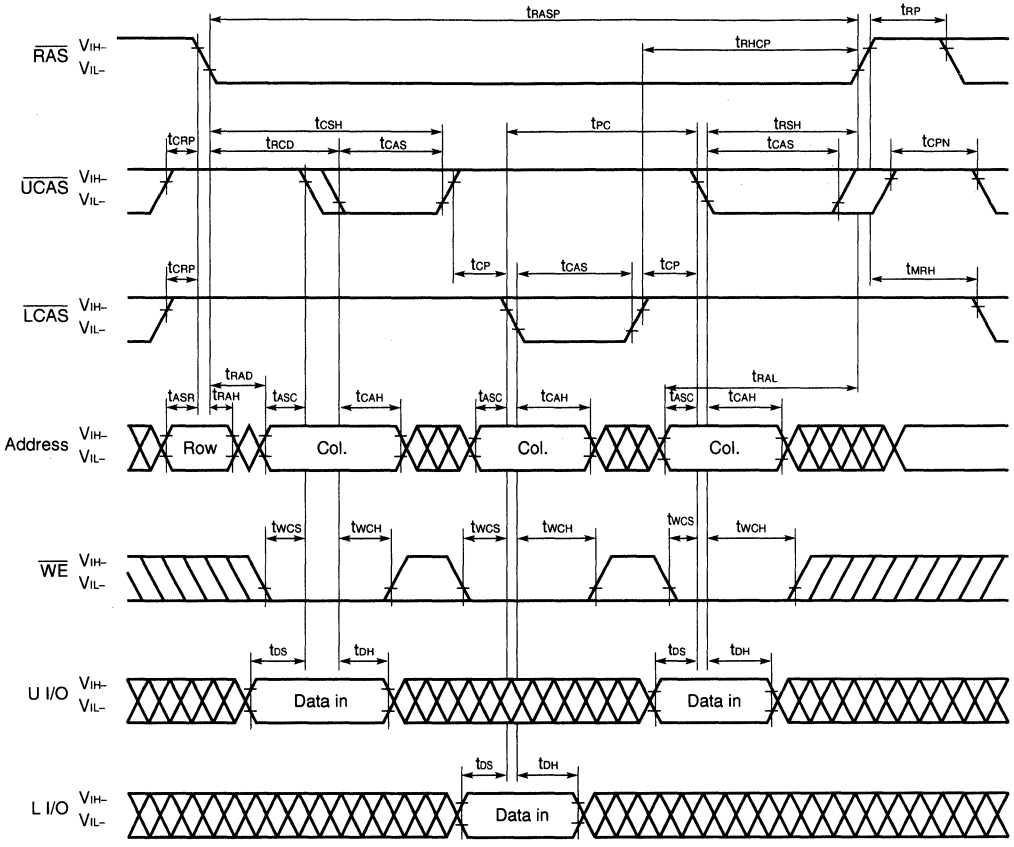
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

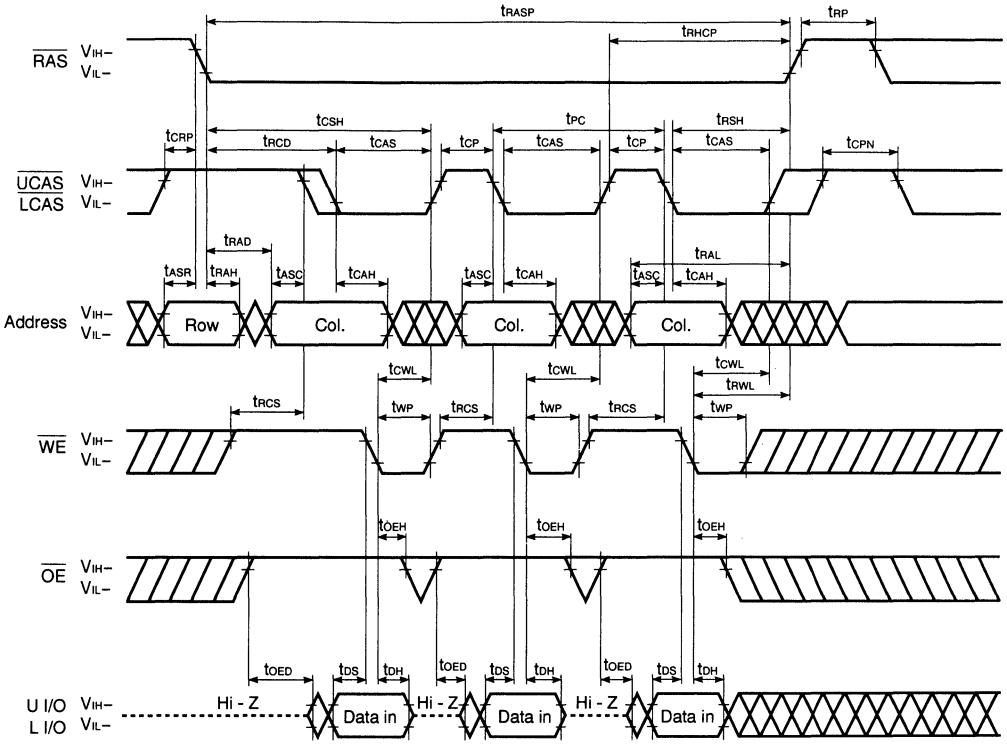
Fast Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

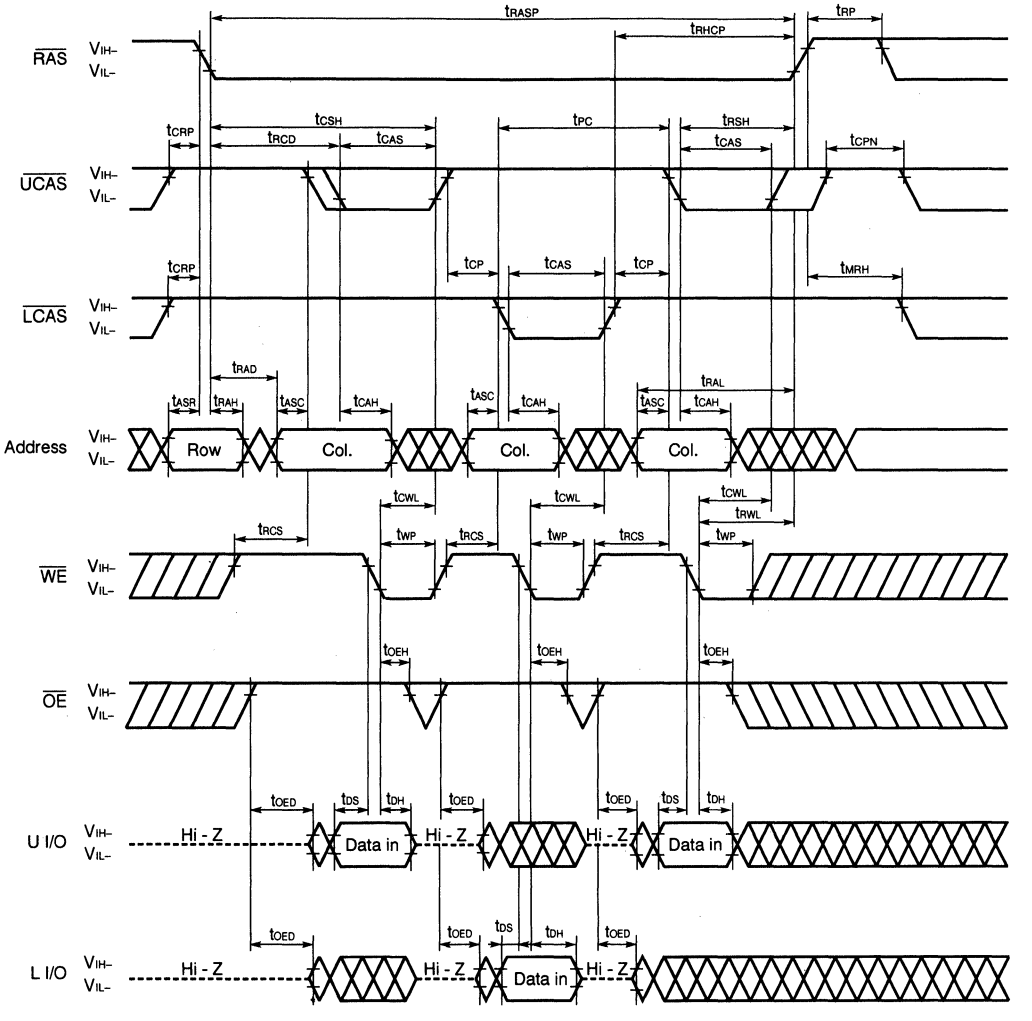
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

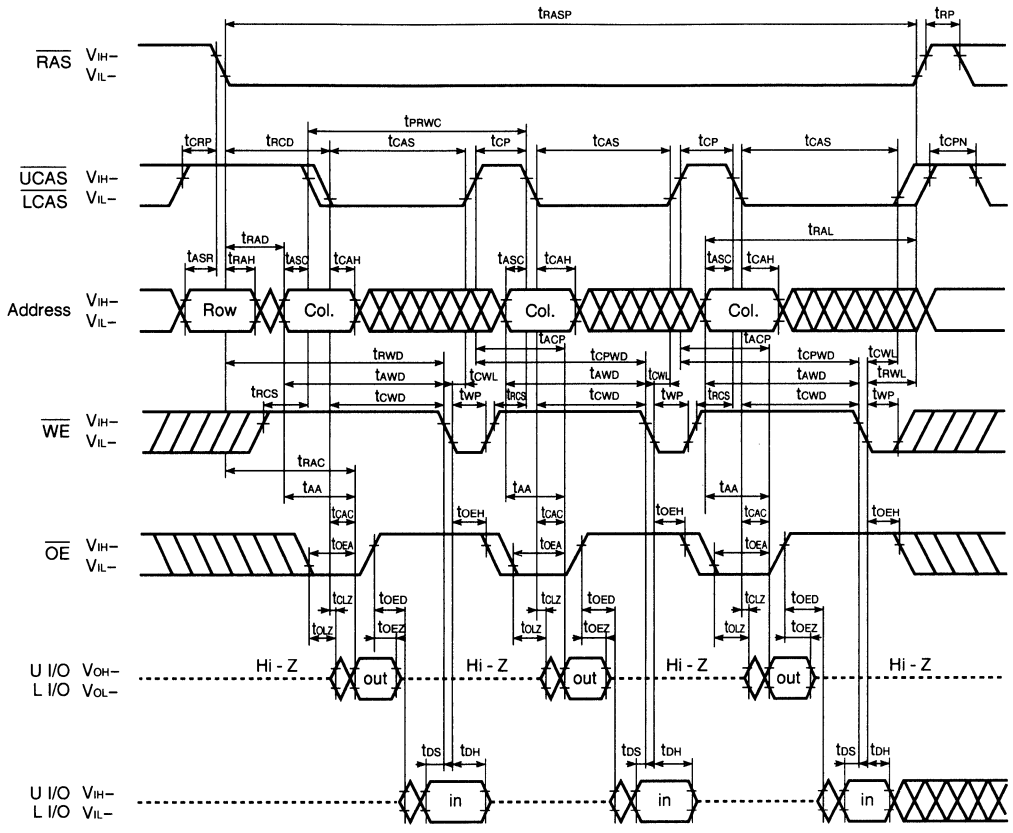
Fast Page Mode Byte Late Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

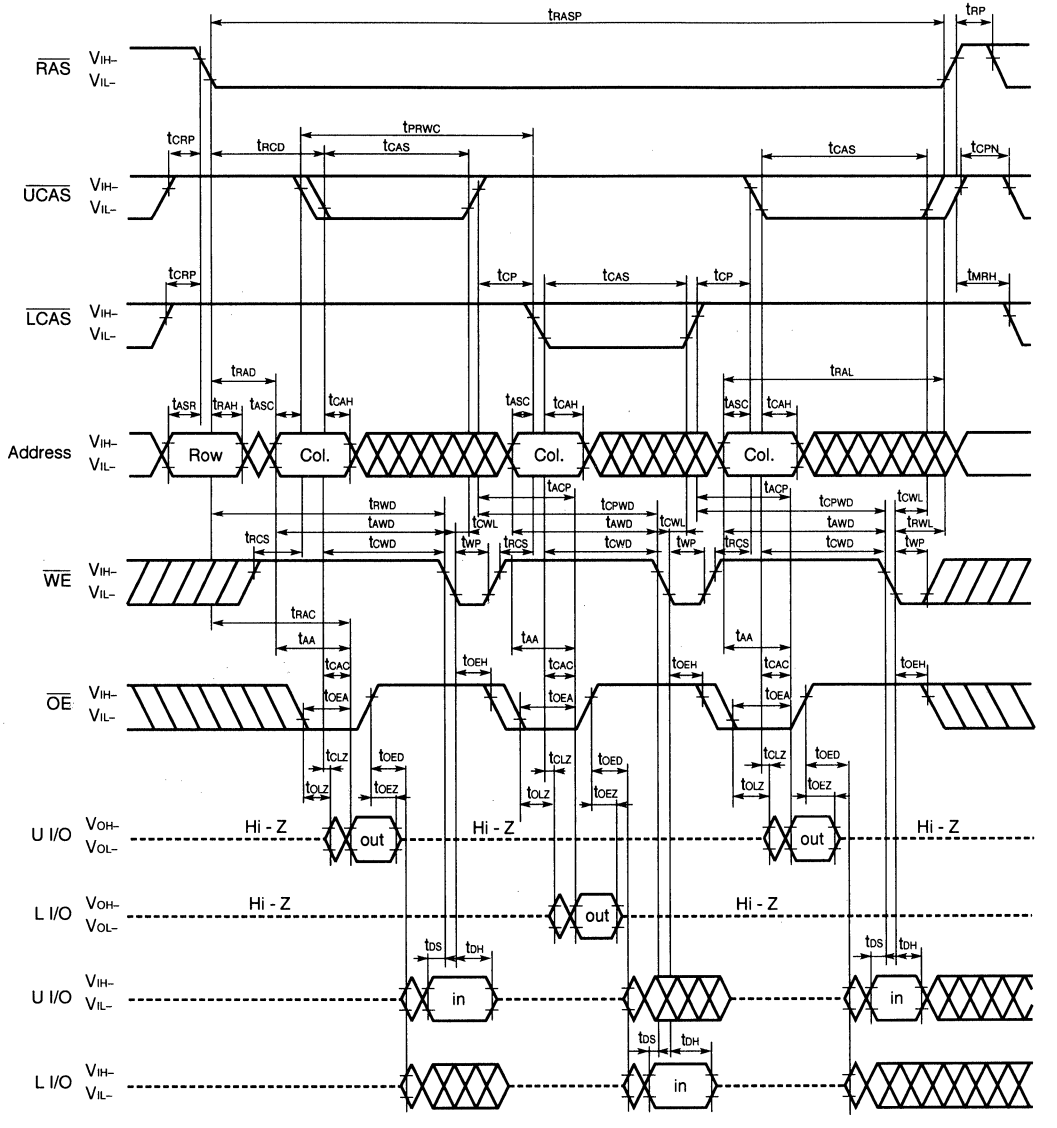
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

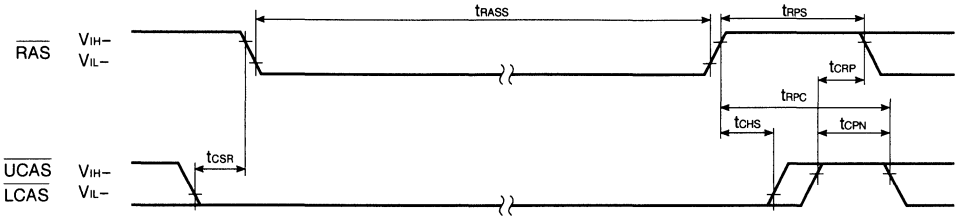
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

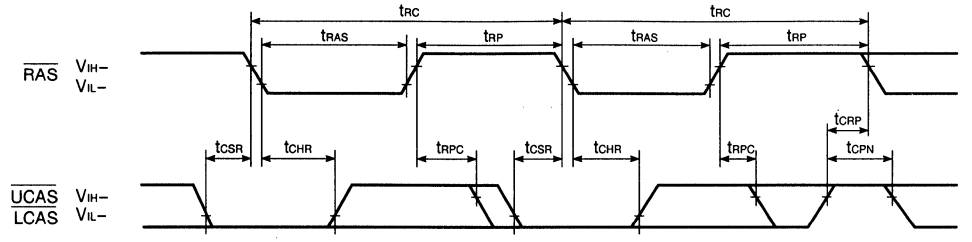
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

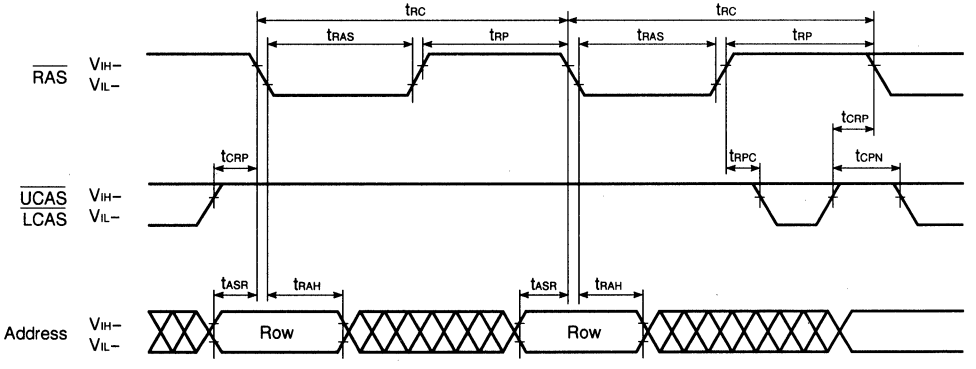
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



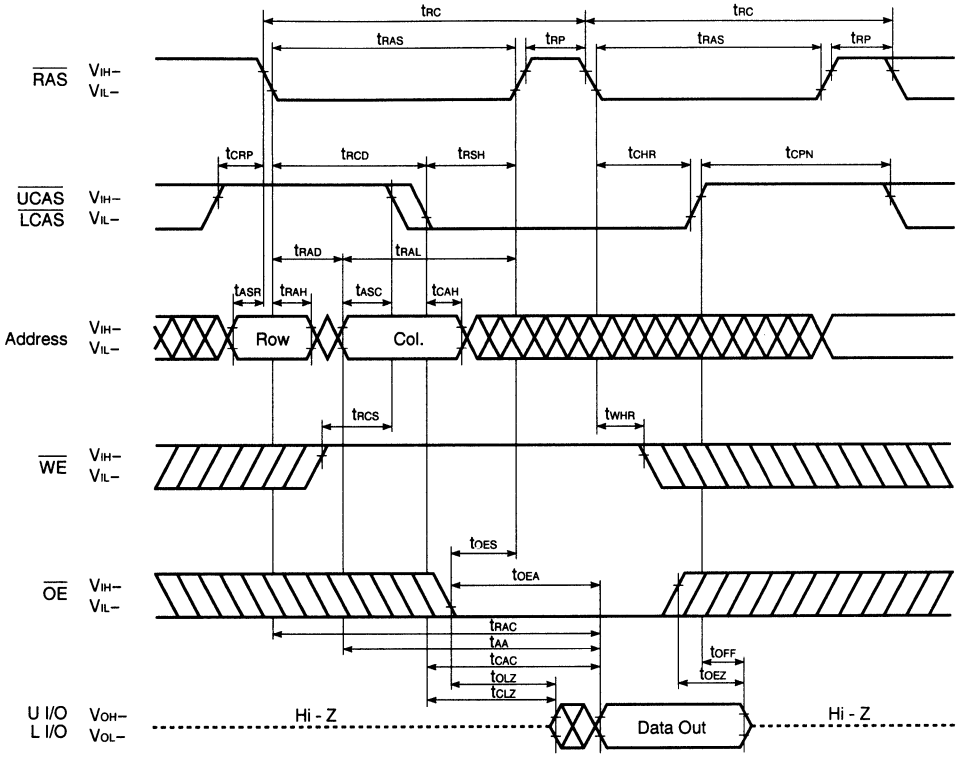
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

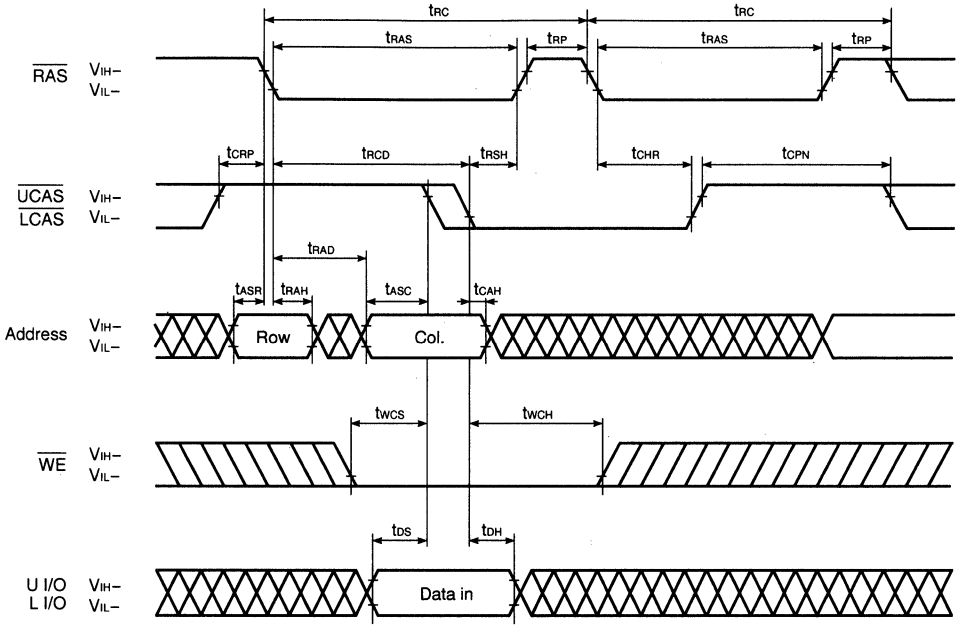


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



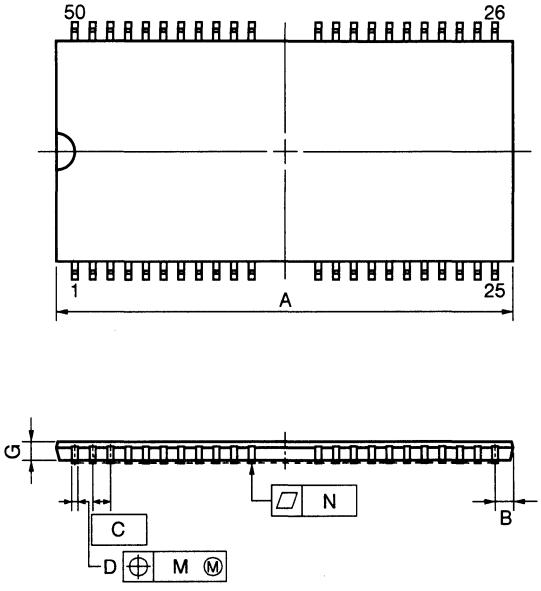
Hidden Refresh Cycle (Write)



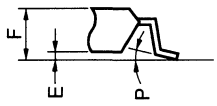
Remark $\overline{OE}$: Don't care

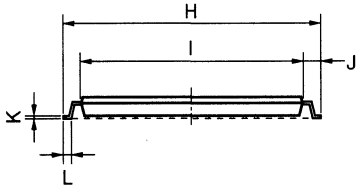
Package Drawings

50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end





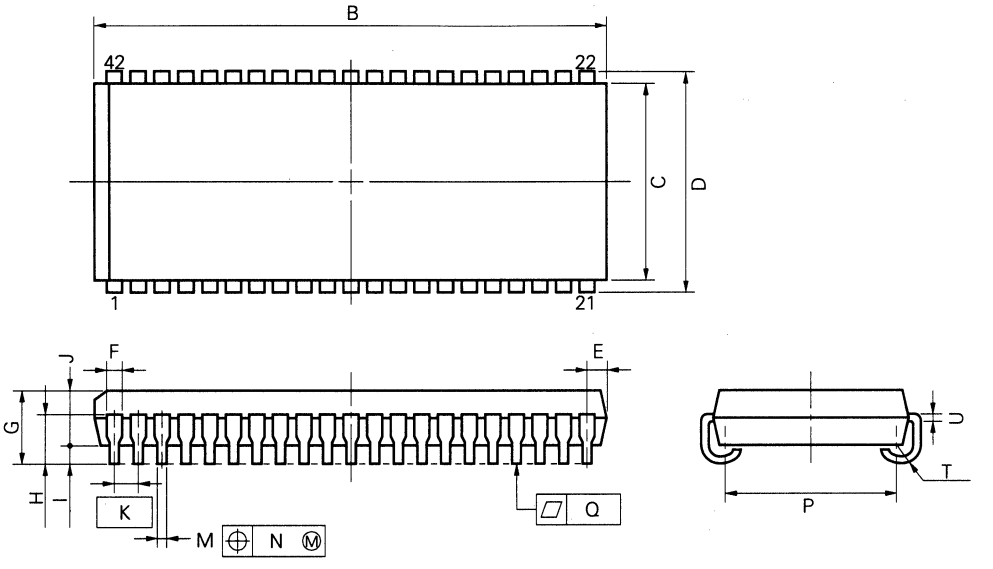
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S18160, 4218160.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S18160G5, 4218160G5: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S18160LE, 4218160LE: 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Fast Page Mode
16M Dynamic RAM
[3.3V ± 0.3V]

NEC

MOS INTEGRATED CIRCUIT

μPD42S16400L, 4216400L, 42S17400L, 4217400L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μPD42S16400L, 4216400L, 42S17400L, 4217400L are 4,194,304 words by 4 bits dynamic CMOS RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycles and the μPD42S16400L, 42S17400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 26-pin plastic TSOP(II) and 26-pin plastic SOJ.

Features

- 4,194,304 words by 4 bits organization
- Fast page mode
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIM.)
μPD42S16400L-A60, 4216400L-A60	288 mW	60 ns	110 ns	40 ns
μPD42S17400L-A60, 4217400L-A60	360 mW			
μPD42S16400L-A70, 4216400L-A70	252 mW	70 ns	130 ns	45 ns
μPD42S17400L-A70, 4217400L-A70	324 mW			
μPD42S16400L-A80, 4216400L-A80	216 mW	80 ns	150 ns	50 ns
μPD42S17400L-A80, 4217400L-A80	288 mW			

- The μPD42S16400L, μPD42S17400L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

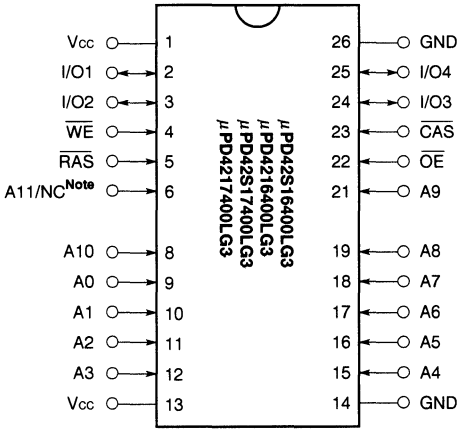
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16400L	4,096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh. $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD42S17400L	2,048 cycles/128 ms		
μPD4216400L	4,096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)
μPD4217400L	2,048 cycles/32 ms		

Ordering Information

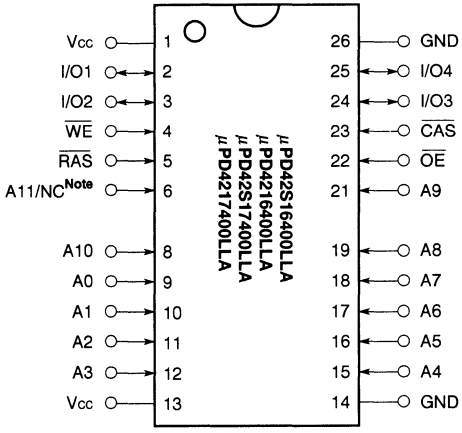
Part number	Access time (MAX.)	Package	Refresh
μPD42S16400LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17400LG3-A60			
μPD42S16400LG3-A70	70 ns		
μPD42S17400LG3-A70			
μPD42S16400LG3-A80	80 ns		
μPD42S17400LG3-A80			
μPD42S16400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD42S17400LLA-A60			
μPD42S16400LLA-A70	70 ns		
μPD42S17400LLA-A70			
μPD42S16400LLA-A80	80 ns		
μPD42S17400LLA-A80			
μPD4216400LG3-A60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217400LG3-A60			
μPD4216400LG3-A70	70 ns		
μPD4217400LG3-A70			
μPD4216400LG3-A80	80 ns		
μPD4217400LG3-A80			
μPD4216400LLA-A60	60 ns	26-pin plastic SOJ (300 mil)	
μPD4217400LLA-A60			
μPD4216400LLA-A70	70 ns		
μPD4217400LLA-A70			
μPD4216400LLA-A80	80 ns		
μPD4217400LLA-A80			

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)



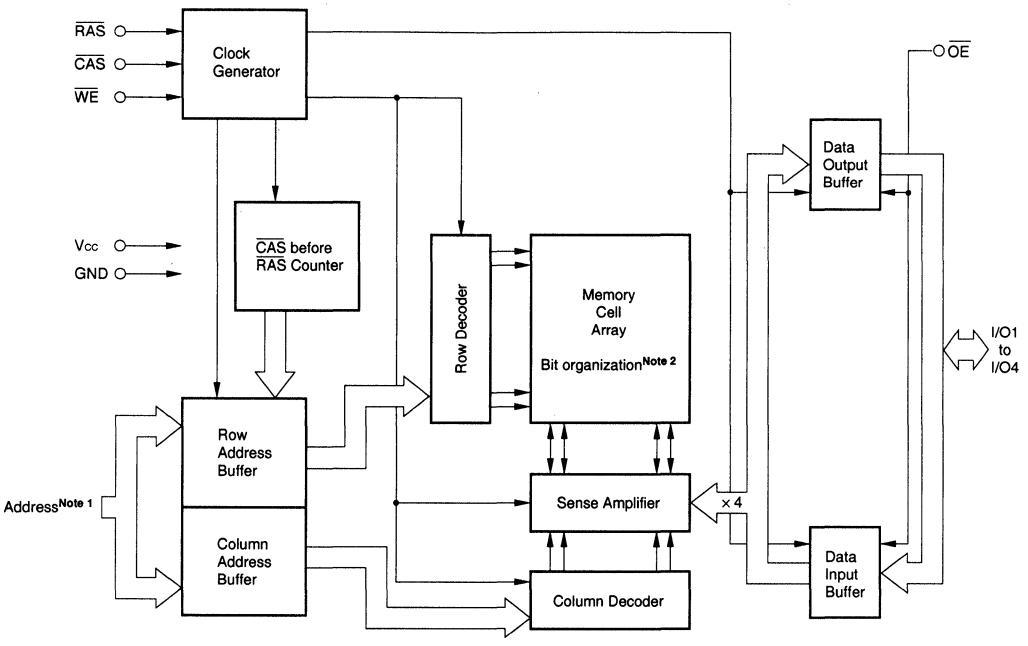
26-pin Plastic SOJ (300 mil)



Note A11 ··· μPD42S16400L, 4216400L
NC ··· μPD42S17400L, 4217400L

A0 to A11	:	Address Inputs
I/O1 to I/O4	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16400L, 4216400L	A0 - A11	A0 - A9
μPD42S17400L, 4217400L	A0 - A10	A0 - A10

2. μPD42S16400L, 4216400L ··· 4,096 × 1,024 × 4 μPD42S17400L, 4217400L ··· 2,048 × 2,048 × 4

Input/Output Pin Functions

The μPD42S16400L, 4216400L, 42S17400L, 4217400L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to Ax[Note] (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD42S16400L, 4216400L	A0 - A11	12 bits	10 bits
μPD42S17400L, 4217400L	A0 - A10	11 bits	11 bits

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)
[μPD42S16400L, 4216400L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		80	mA	1, 2, 3
			t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 70 ns		70		
			I_O = 0 mA	t_{RAC} = 80 ns		60		
Standby current	μPD42S16400L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4216400L		$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$	t_{RAC} = 60 ns		80	mA	1, 2, 3 ,4
			t_{RC} = $t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		70		
				t_{RAC} = 80 ns		60		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		70	mA	1, 2, 5
			t_{PC} = $t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		80	mA	1, 2
			t_{RC} = $t_{RC\ (MIN.)}$	t_{RAC} = 70 ns		70		
			I_O = 0 mA	t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the μPD42S16400L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 31.3 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V Standby : $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs		220	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S16400L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH(MAX.)}$, 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD42S17400L, 4217400L]

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling	t_{RAC} = 60 ns		100	mA	1, 2, 3
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		90		
			I_O = 0 mA	t_{RAC} = 80 ns		80		
Standby current	μPD42S17400L	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.15		
	μPD4217400L		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 60 ns		100	mA	1, 2, 3, 4
			t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		90		
				t_{RAC} = 80 ns		80		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ cycling	t_{RAC} = 60 ns		70	mA	1, 2, 5
			t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 70 ns		60		
				t_{RAC} = 80 ns		50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling	t_{RAC} = 60 ns		100	mA	1, 2
			t_{RC} = t_{RC} (MIN.)	t_{RAC} = 70 ns		90		
			I_O = 0 mA	t_{RAC} = 80 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17400L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 62.5 μs; $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH} (MAX.), 0 V ≤ V_{IL} ≤ 0.2 V; Standby : $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V; Address : V_{IH} or V_{IL}; $\overline{WE}$, $\overline{OE}$: V_{IH}; I_O = 0 mA	t_{RAS} ≤ 1 μs		200	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17400L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms, V_{CC} – 0.2 V ≤ V_{IH} ≤ V_{IH}(MAX.), 0 V ≤ V_{IL} ≤ 0.2 V; I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V; All other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 3.6 V; Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ V_{IL} (MAX.) and $\overline{CAS}$ ≥ V_{IH} (MIN.).

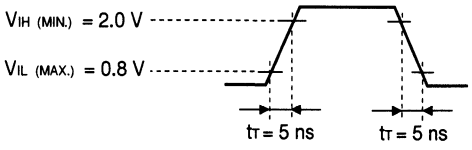
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

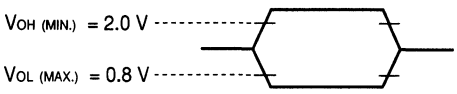
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

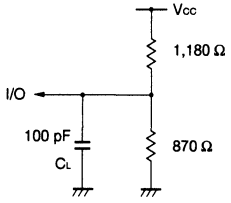
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	52	25	60	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	17	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	12	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	15	–	15	–	20	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	3	50	ns	
Refresh time	μPD42S16400L, 42S17400L	tREF	–	128	–	128	–	128	ms	4
	μPD4216400L		–	64	–	64	–	64	ms	
	μPD4217400L		–	32	–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	160	–	180	–	205	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	–	95	–	110	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	–	43	–	50	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	55	–	60	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	70	–	ns	1

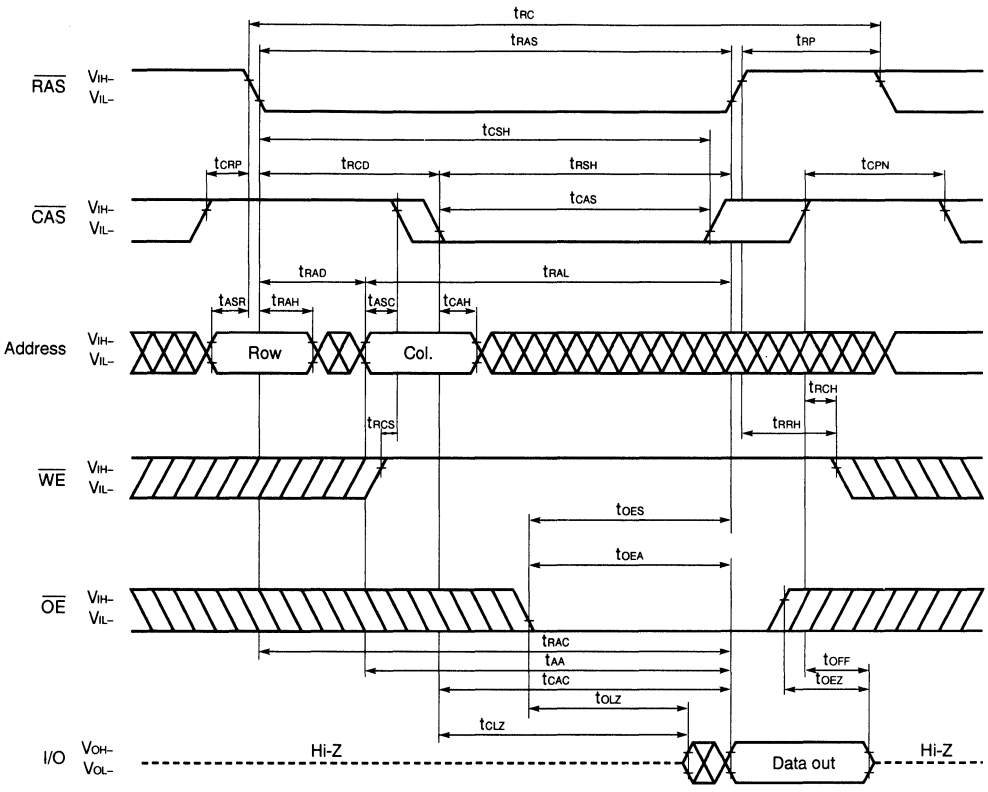
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

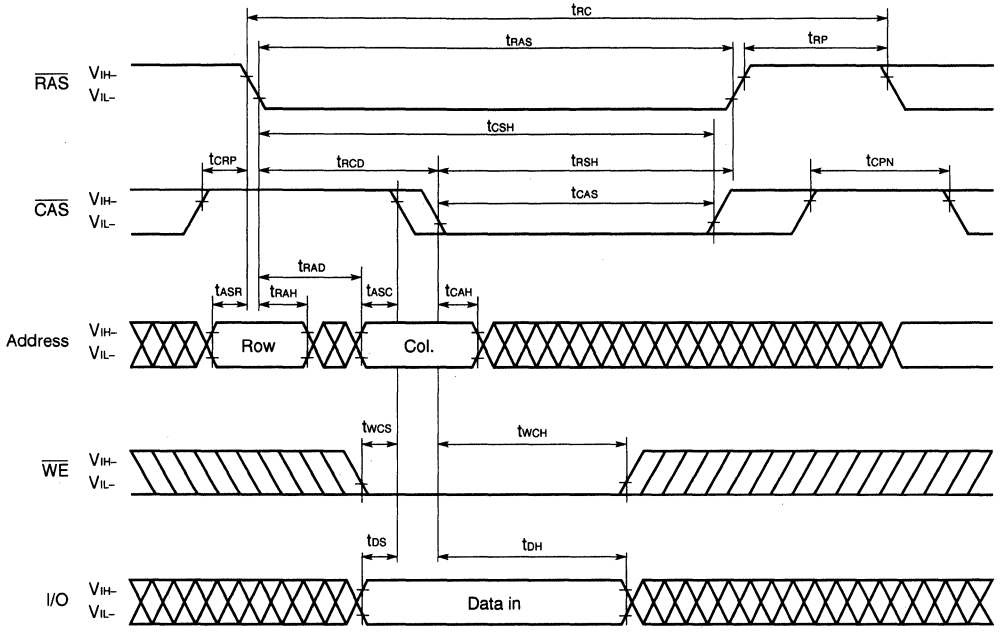
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	150	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

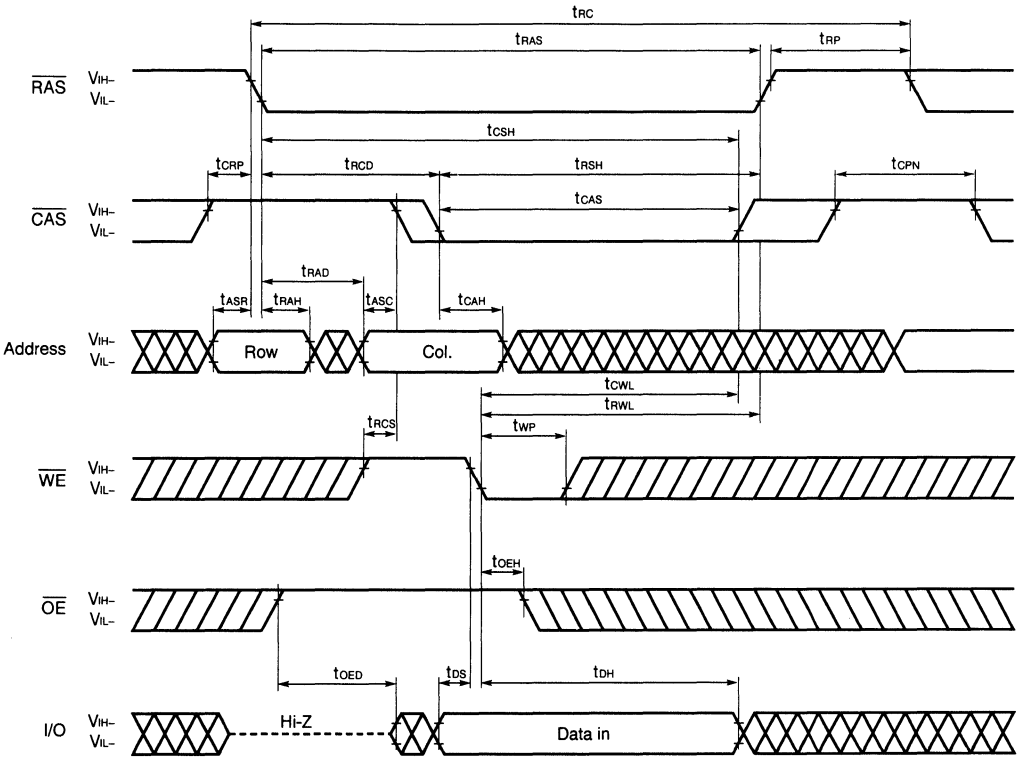

tRC
tRAS
tRP
RAS VIH- VIL-
tCSH
tCRP
tRCD
tRSH
tCPN
CAS VIH- VIL-
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH- VIL-
Row
Col.
tRCH
tRCS
tRRH
WE VIH- VIL-
tOES
tOEA
OE VIH- VIL-
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O VOH- VOL-
Hi-Z
Data out
Hi-Z

Early Write Cycle

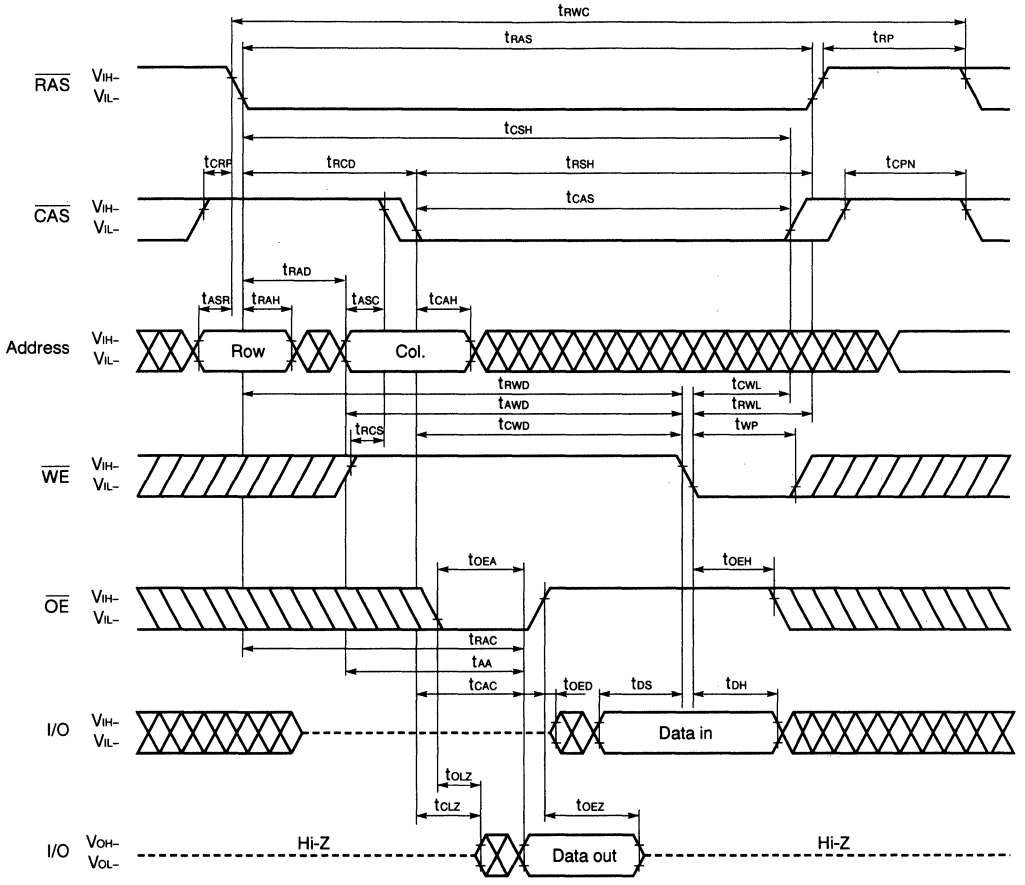


Remark $\overline{OE}$: Don't care

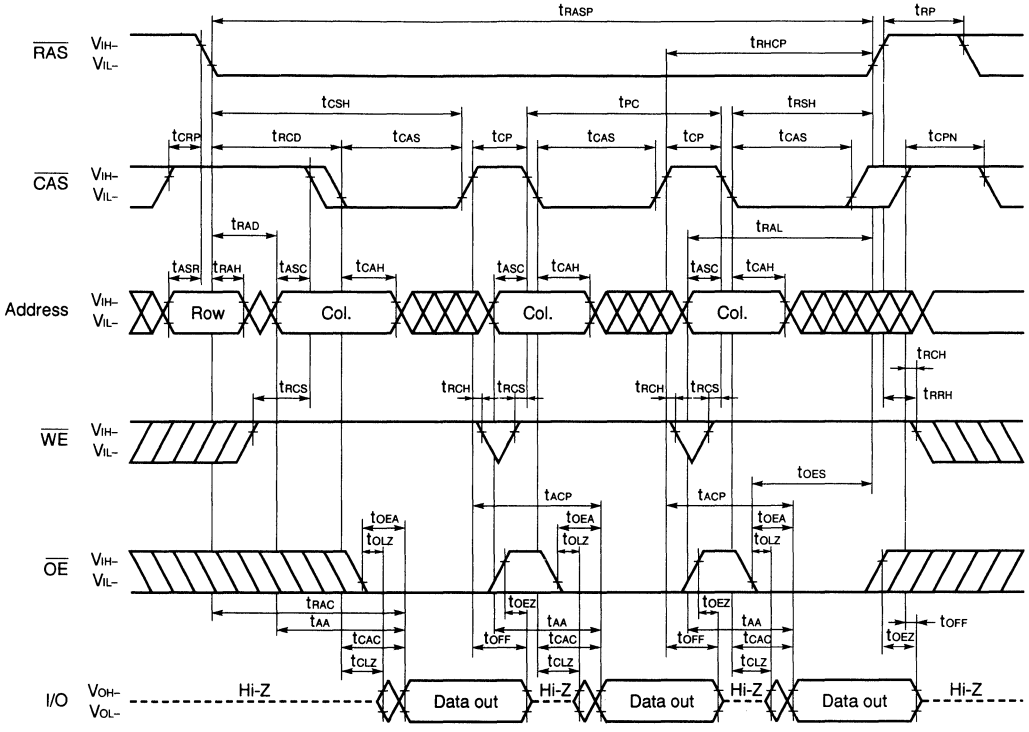
Late Write Cycle



Read Modify Write Cycle

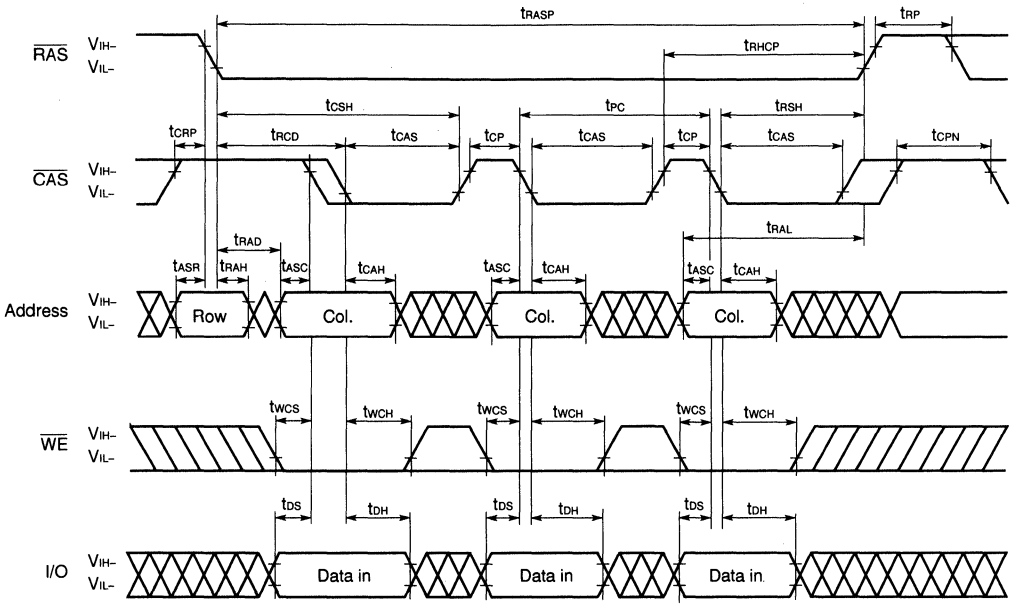


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

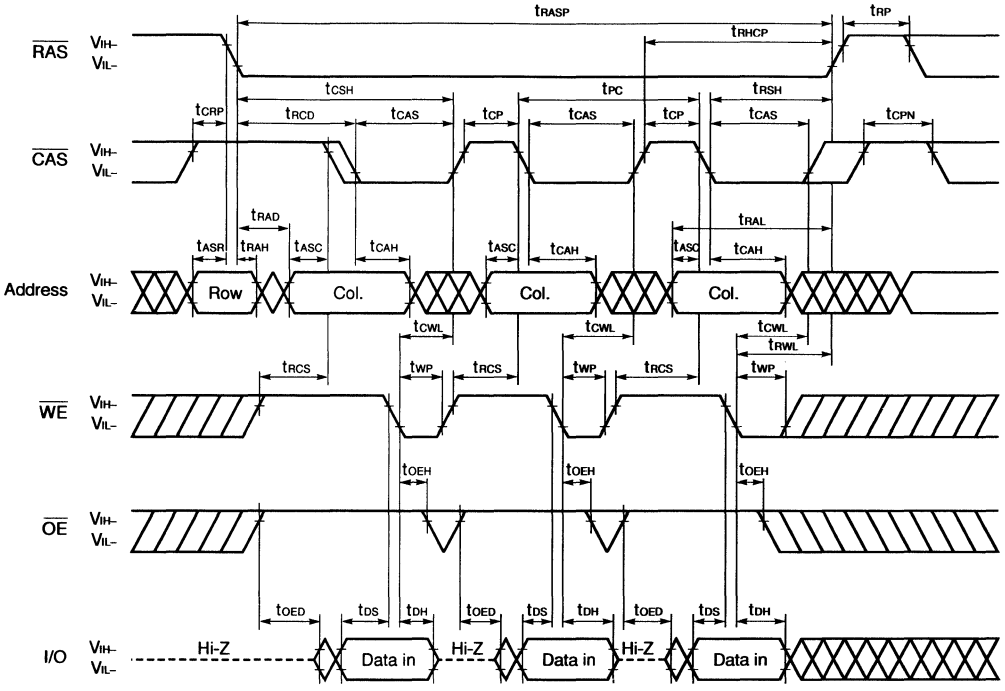
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

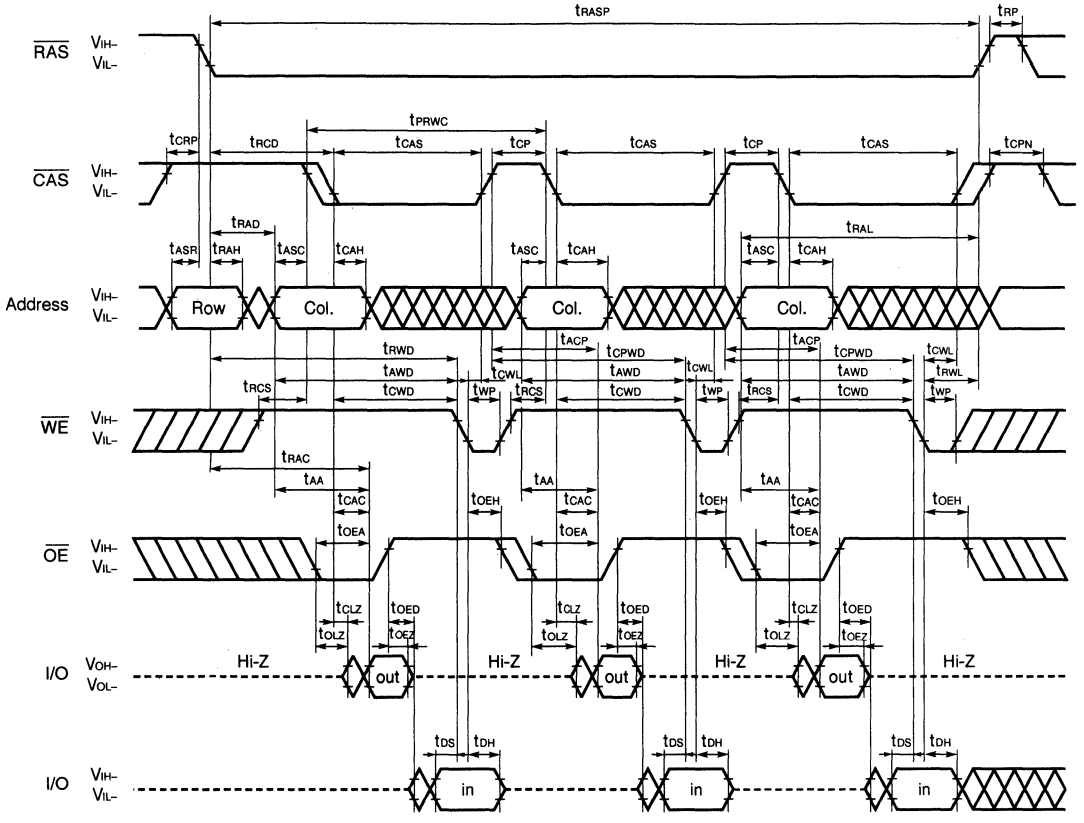
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



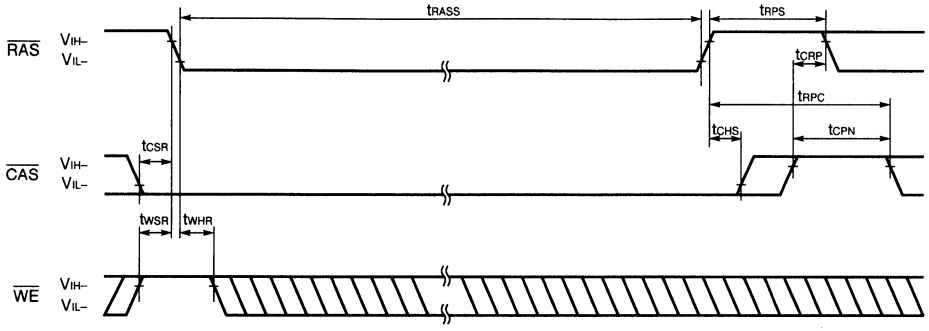
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S16400L, 42S17400L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S16400L : 4,096 times within a 64 ms interval
μPD42S17400L : 2,048 times within a 32 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

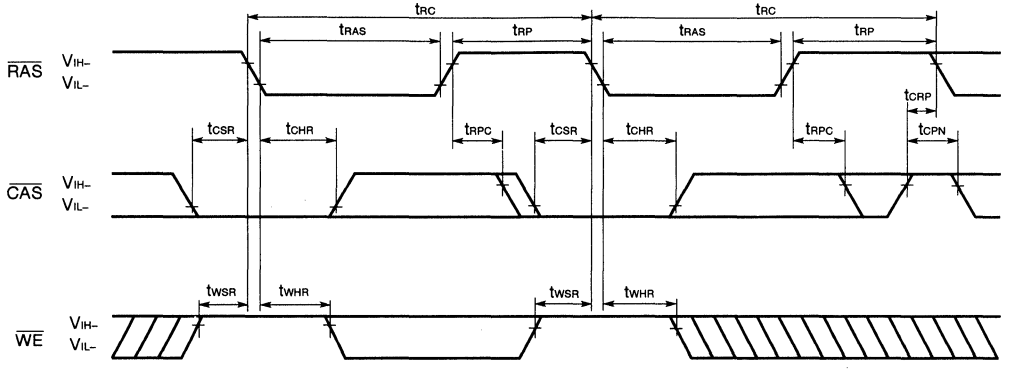
μPD42S16400L : 4,096 times within a 64 ms interval
μPD42S17400L : 2,048 times within a 32 ms interval

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100$ μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S16400L : 4,096 times within a 128 ms interval
μPD42S17400L : 2,048 times within a 128 ms interval

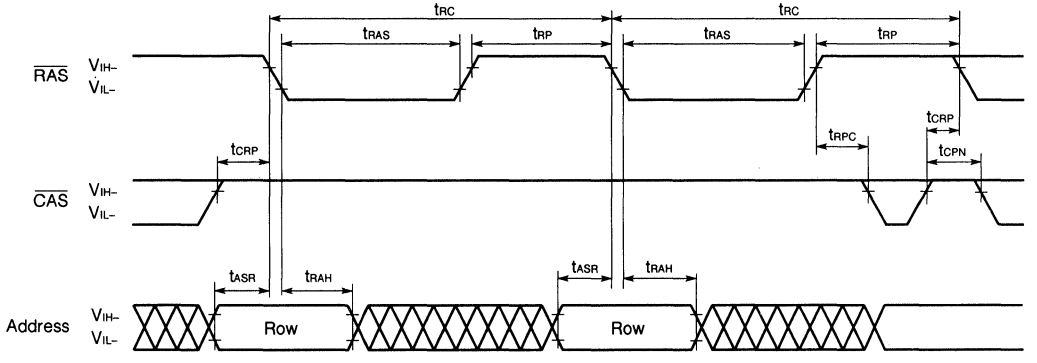
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



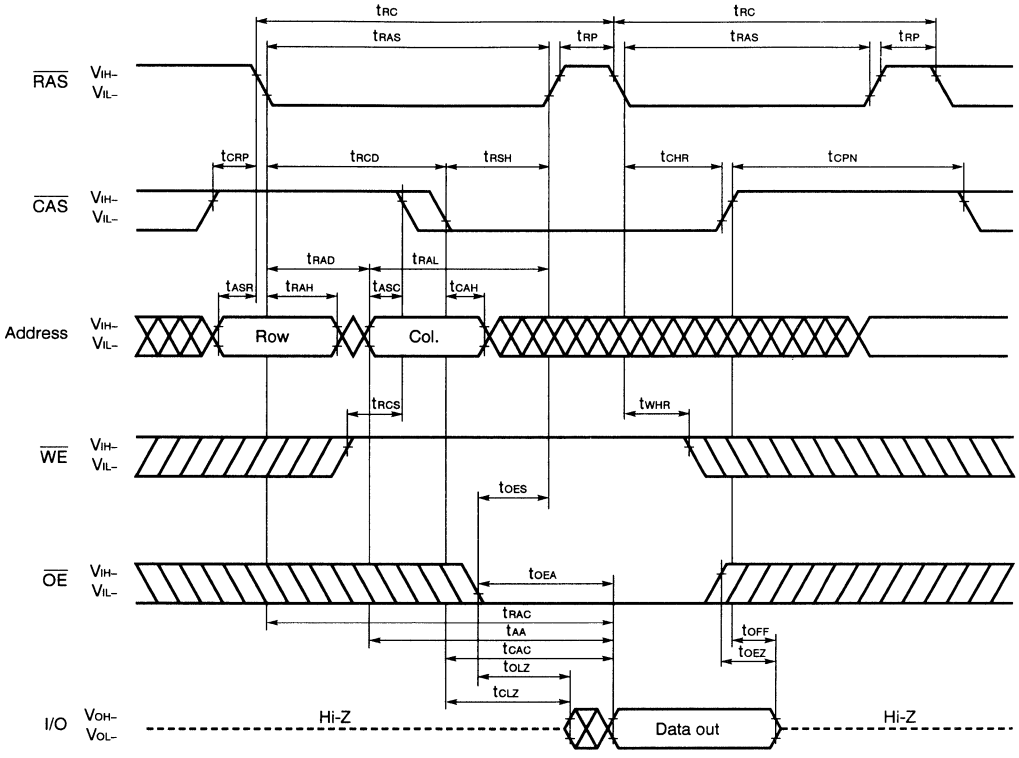
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

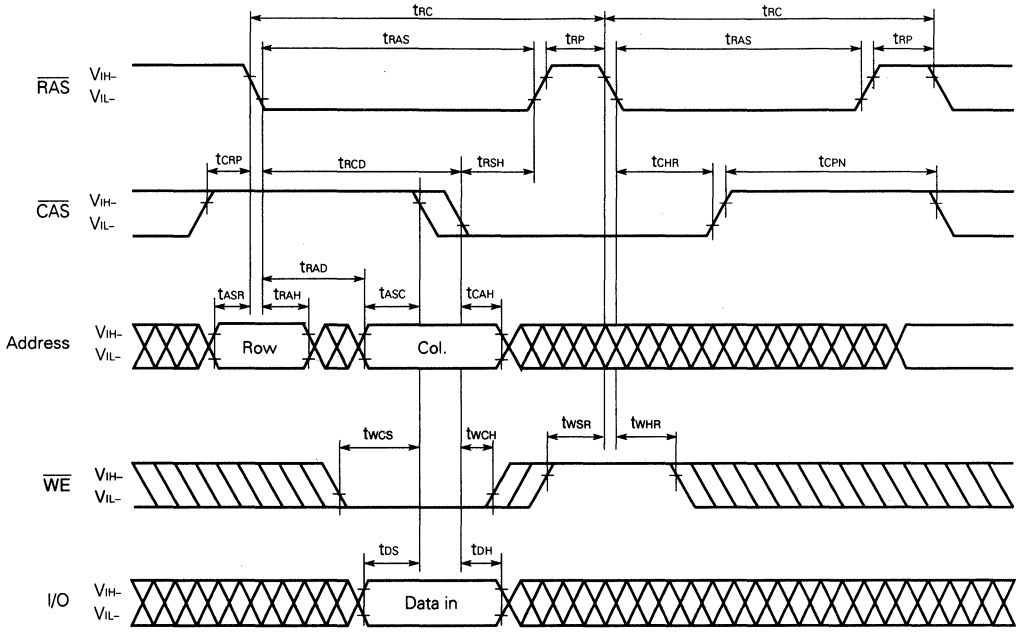


Remark $\overline{WE}$, $\overline{OE}$: Don't care, I/O: Hi-Z

Hidden Refresh Cycle (Read)

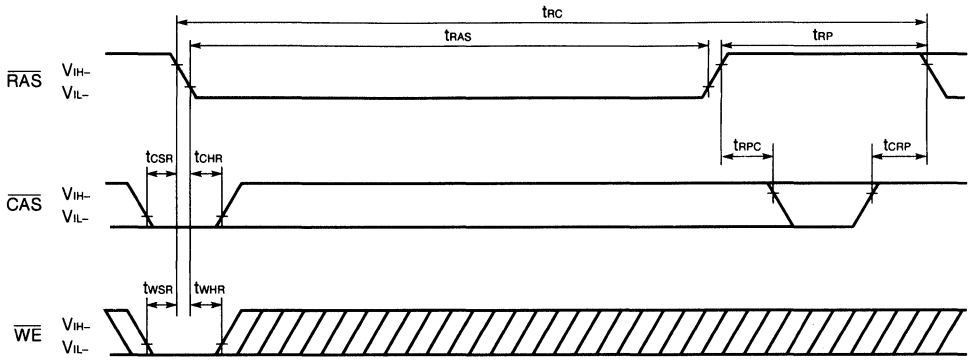


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

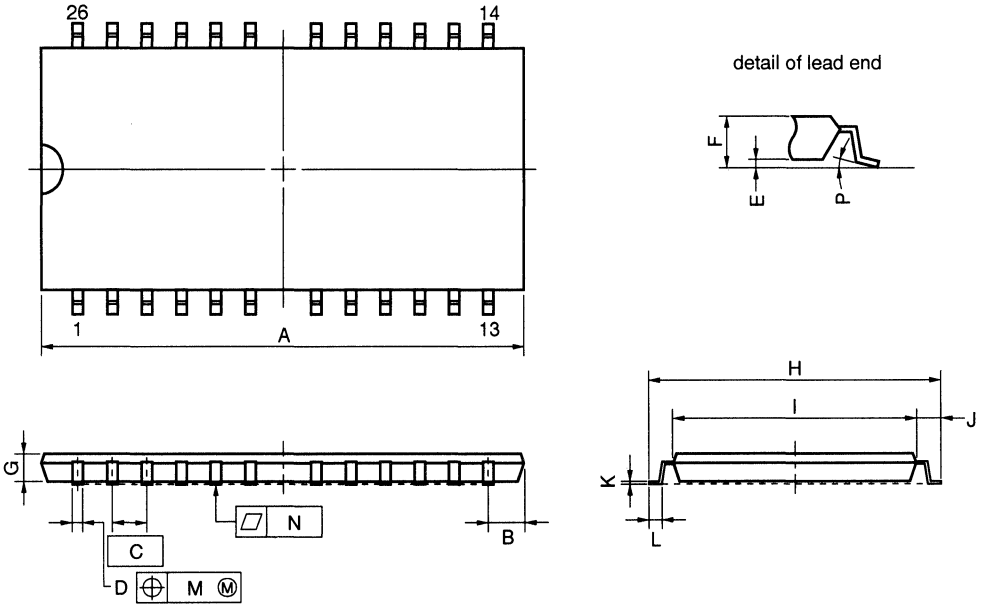
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



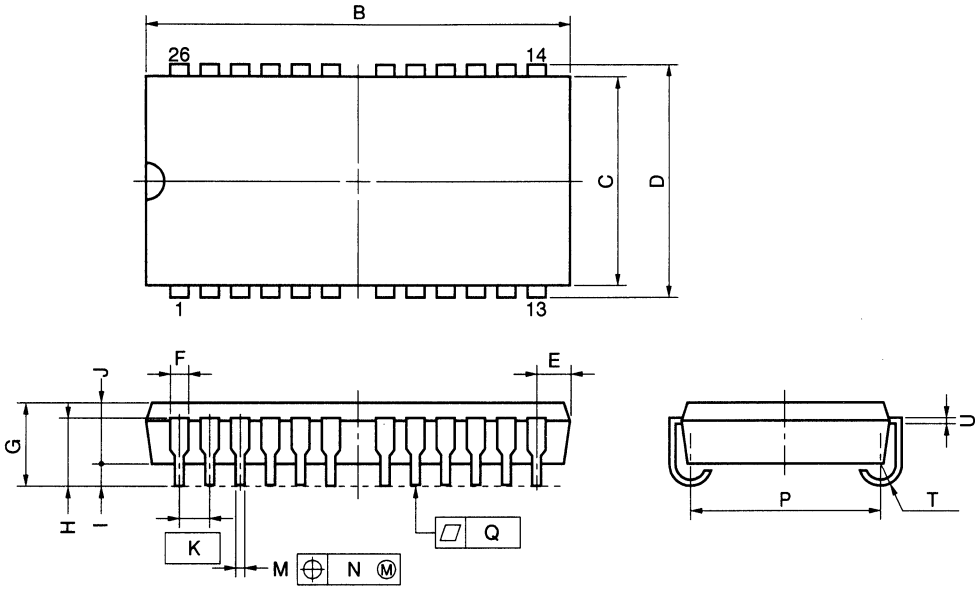
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.3^{+0.20}_{-0.25}$	$0.681^{+0.008}_{-0.010}$
C	7.62	0.300
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.03±0.15	$0.041^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

S26LA-300A-1

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16400L, 4216400L, 42S17400L, 4217400L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400LG3, 4216400LG3, 42S17400LG3, 4217400LG3: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limi: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S16400LLA, 4216400LLA, 42S17400LLA, 4217400LLA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD42S17800L, 4217800L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 2 M-WORD BY 8-BIT, FAST PAGE MODE

Description

The μPD42S17800L, 4217800L are 2,097,152 words by 8 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S17800L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 28-pin plastic TSOP (II) and 28-pin plastic SOJ.

Features

- 2,097,152 words by 8 bits organization
- Fast page mode
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S17800L-A60, 4217800L-A60	360 mW	60 ns	110 ns	40 ns
μPD42S17800L-A70, 4217800L-A70	324 mW	70 ns	130 ns	45 ns

- The μPD42S17800L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

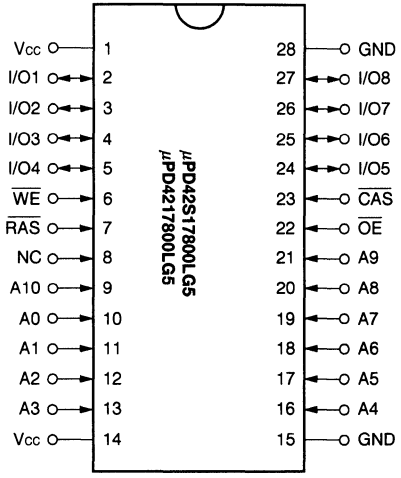
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S17800L	2,048 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4217800L	2,048 cycles/32 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

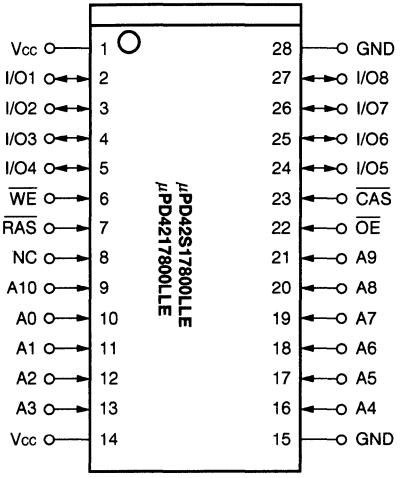
Part number	Access time (MAX.)	Package	Refresh
μPD42S17800LG5-A60 μPD42S17800LG5-A70	60 ns 70 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S17800LLE-A60 μPD42S17800LLE-A70	60 ns 70 ns	28-pin plastic SOJ (400 mil)	
μPD4217800LG5-A60 μPD4217800LG5-A70	60 ns 70 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4217800LLE-A60 μPD4217800LLE-A70	60 ns 70 ns	28-pin plastic SOJ (400 mil)	

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

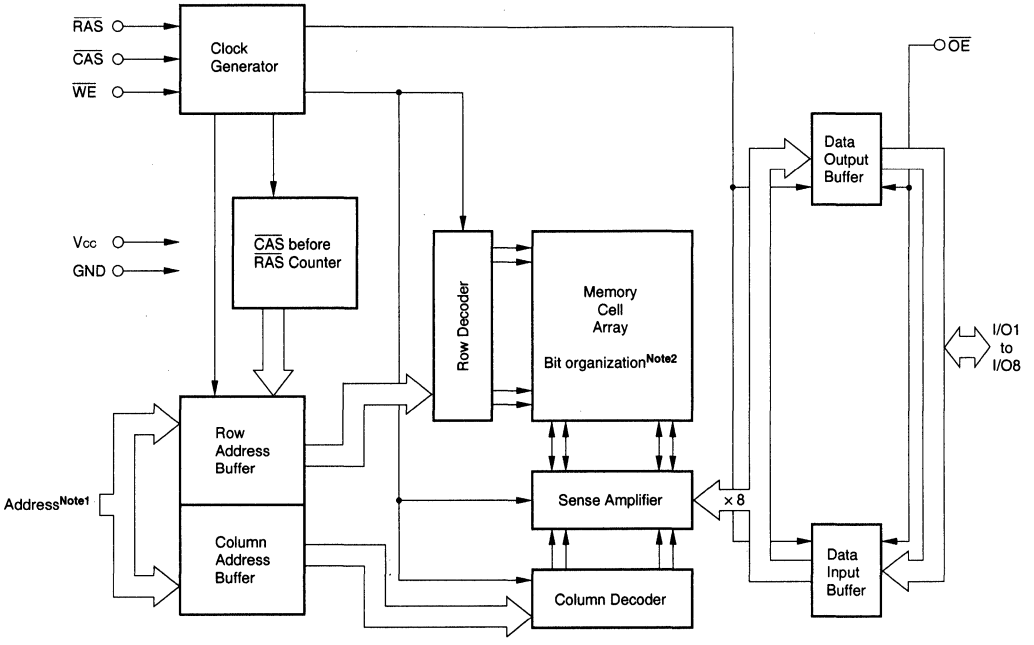


28-pin Plastic SOJ (400 mil)



A0 to A10	:	Address Inputs
I/O1 to I/O8	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Note 1.

Part number	Row address	Column address
μPD42S17800L, 4217800L	A0 - A10	A0 - A9

2. μPD42S17800L, 4217800L ... 2,048 × 1,024 × 8

Input/Output Pin Functions

The μPD42S17800L, 4217800L have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note] and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address inputs)	Input	Address bus. Input total 21-bit of address signal, upper bits and lower bits[Note] in sequence (address multiplex method). Therefore, one word is selected from 2,097,152-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note

Part number	Address inputs	Upper bits	Lower bits
μPD42S17800L, 4217800L	A0 - A10	11 bits	10 bits

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

[MEMO]

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns t_{RAC} = 70 ns		100 90	mA	1, 2, 3
Standby current	μPD42S17800L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.15		
	μPD4217800L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns t_{RAC} = 70 ns		100 90	mA	1, 2, 3, 4
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns t_{RAC} = 70 ns		70 60	mA	1, 2, 5
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns t_{RAC} = 70 ns		100 90	mA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17800L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2$ V Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		200	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17800L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH(MAX.)}$ $0\ V \leq V_{IL} \leq 0.2$ V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

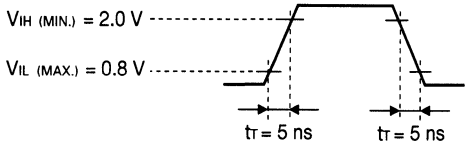
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

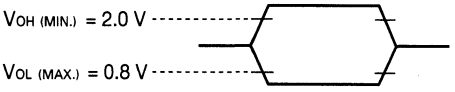
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

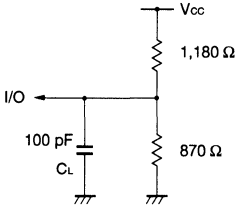
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	18	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	18	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	52	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	13	–	15	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	ns	
Refresh time	μPD42S17800L	tREF	–	128	–	128	ms	
	μPD4217800L		–	32	–	32	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	18	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	158	–	180	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83	–	95	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	38	–	43	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	53	–	60	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	ns	1

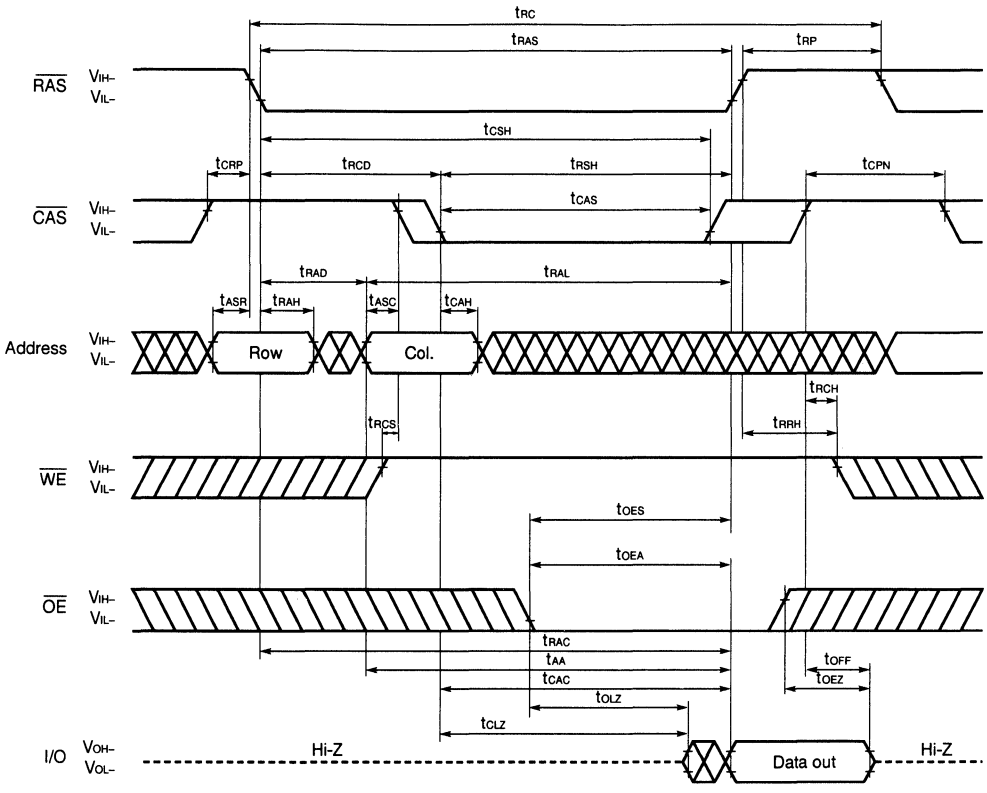
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

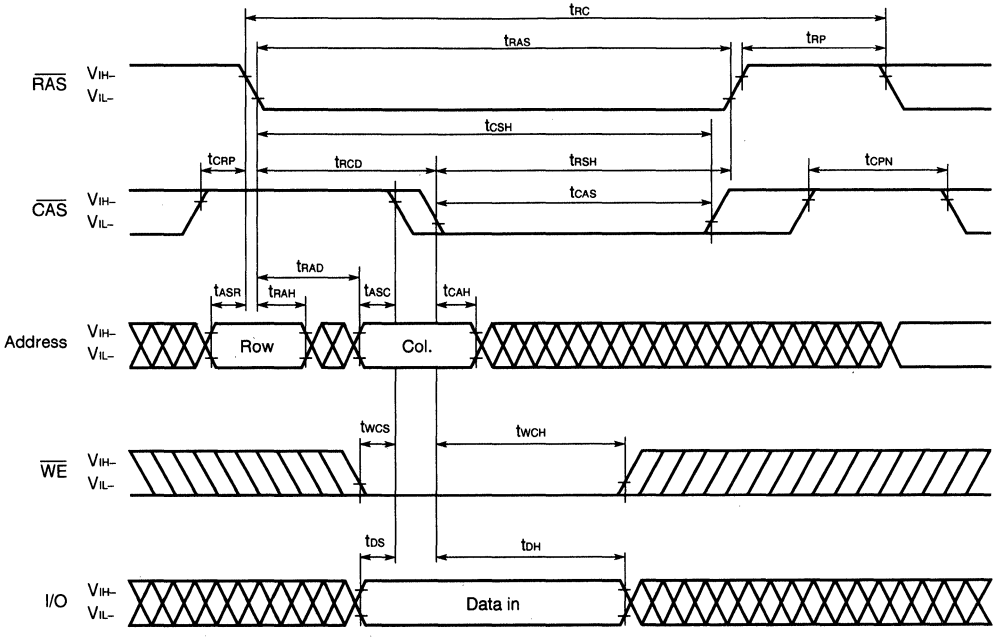
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S17800L.

Read Cycle

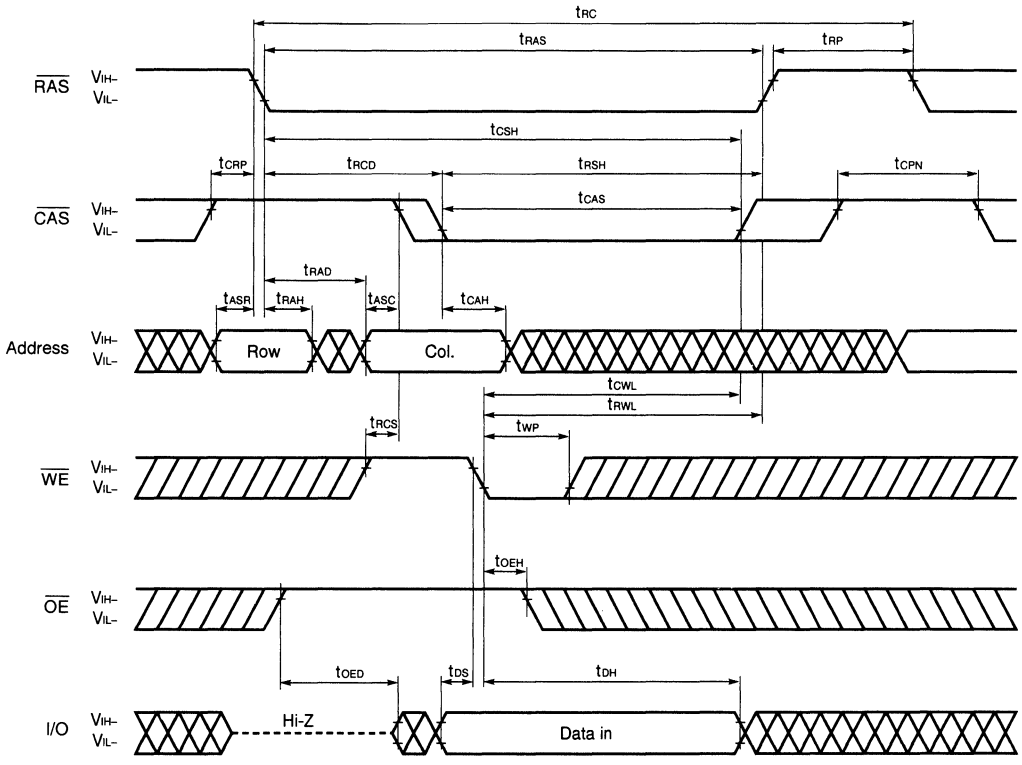

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

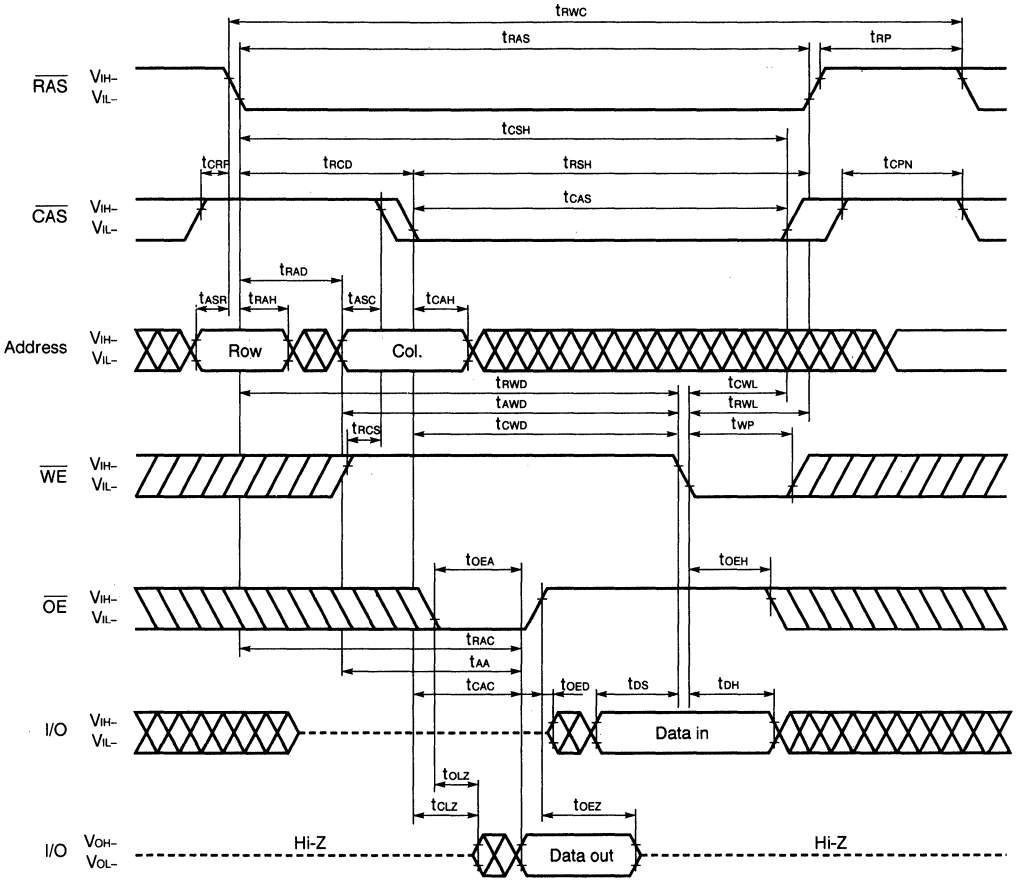


Remark $\overline{OE}$: Don't care

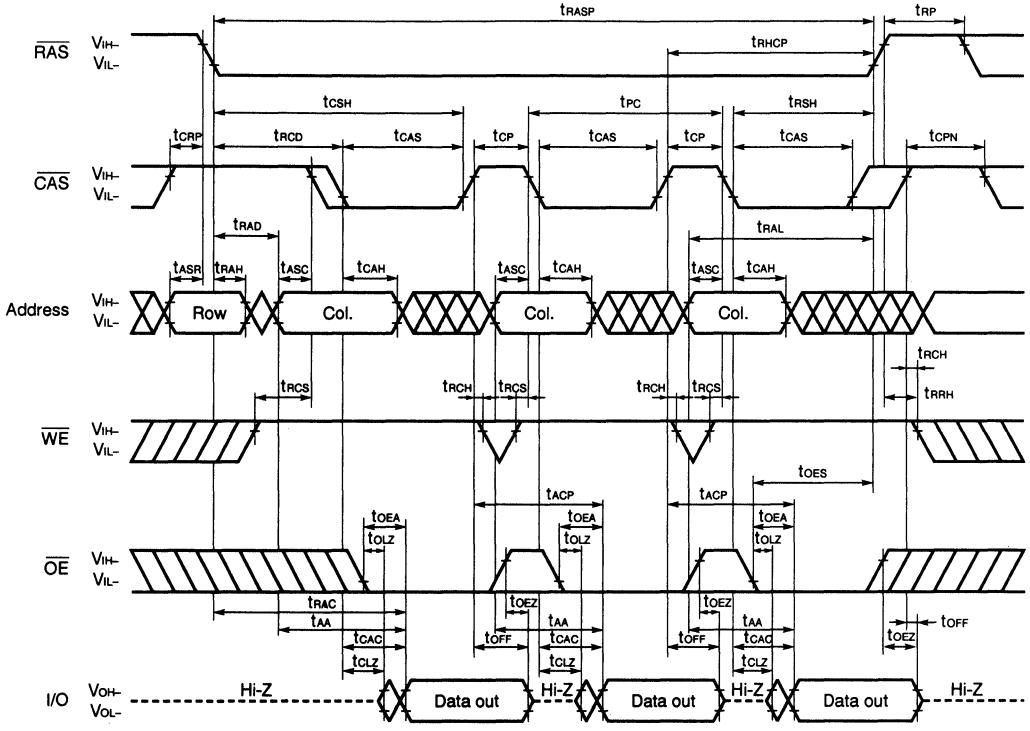
Late Write Cycle



Read Modify Write Cycle

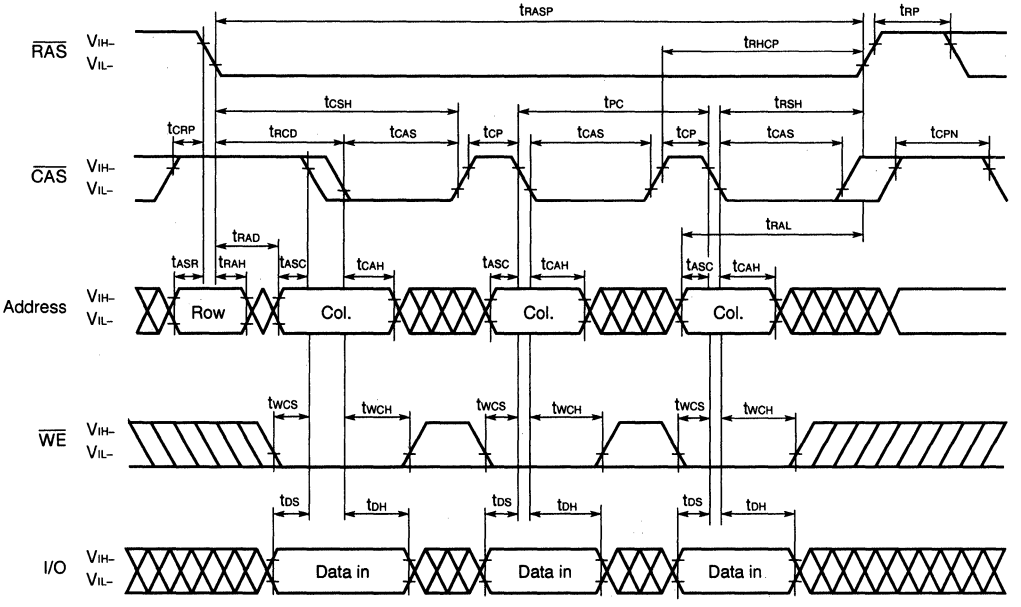


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

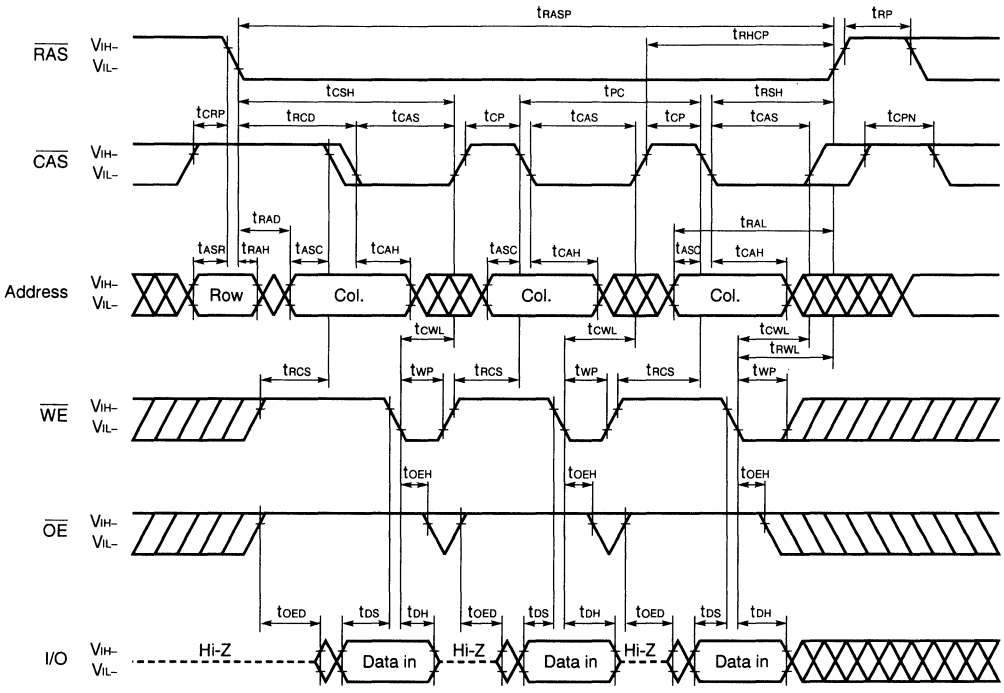
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

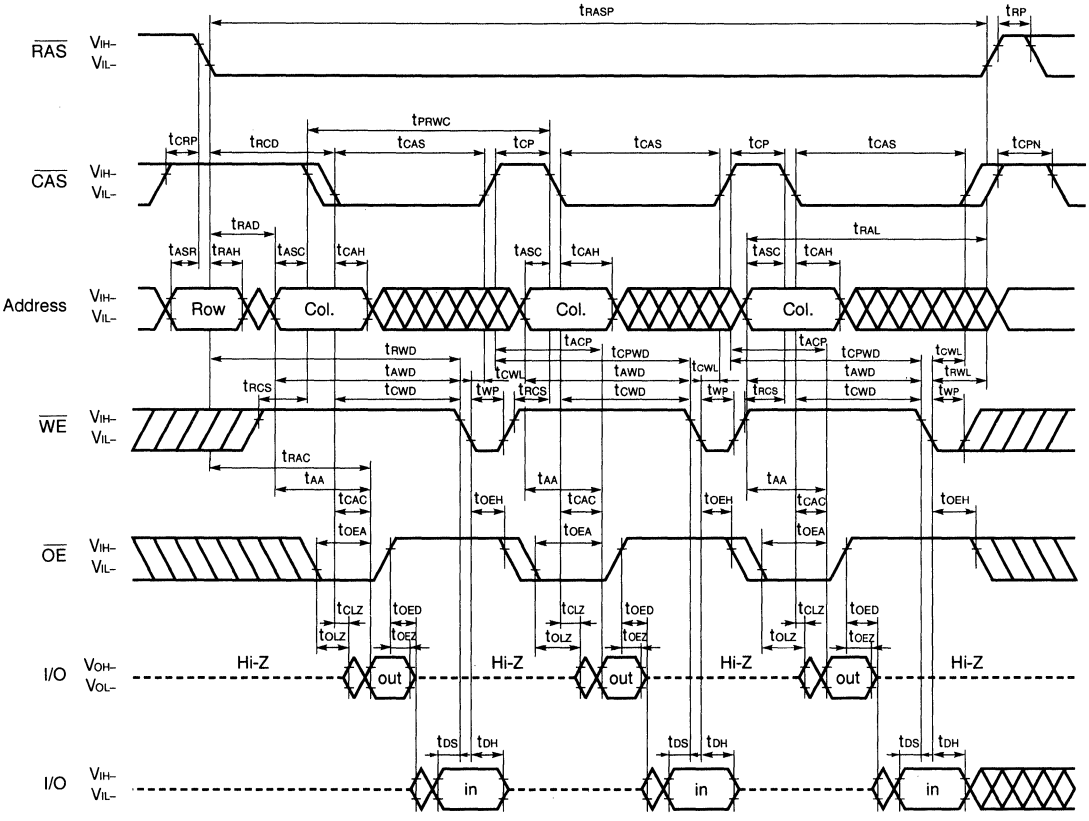
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



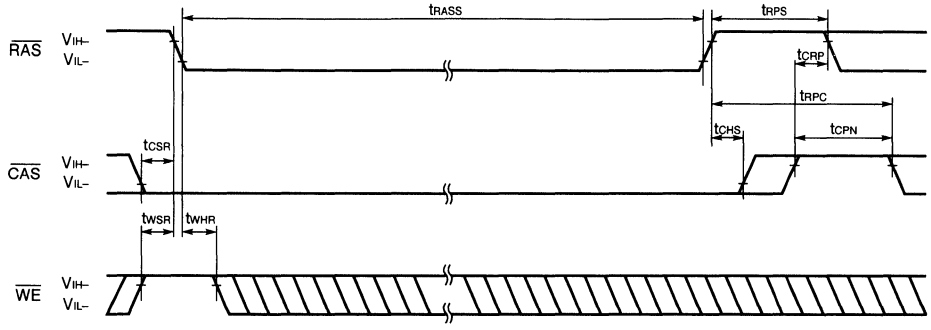
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S17800L)



Remark Address, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S17800L : 2,048 times within a 32 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

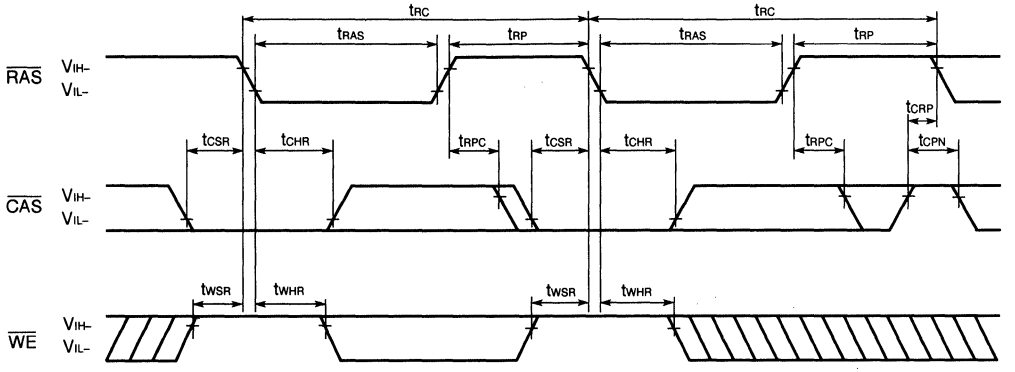
μPD42S17800L : 2,048 times within a 32 ms interval

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S17800L : 2,048 times within a 128 ms interval

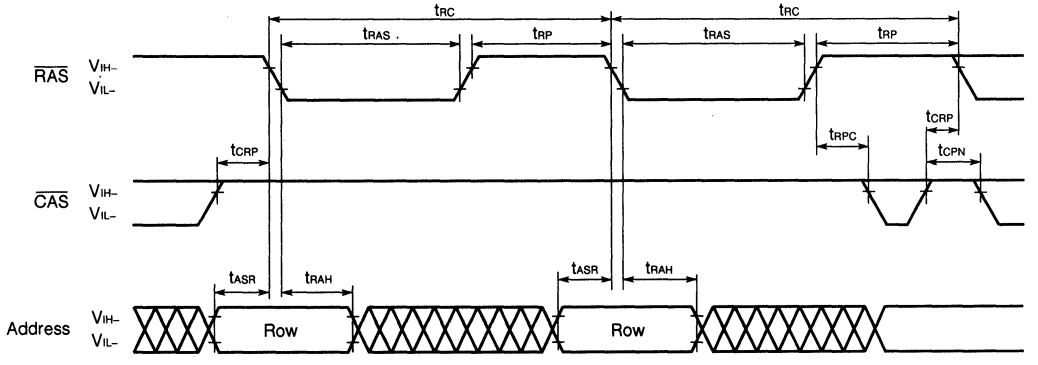
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



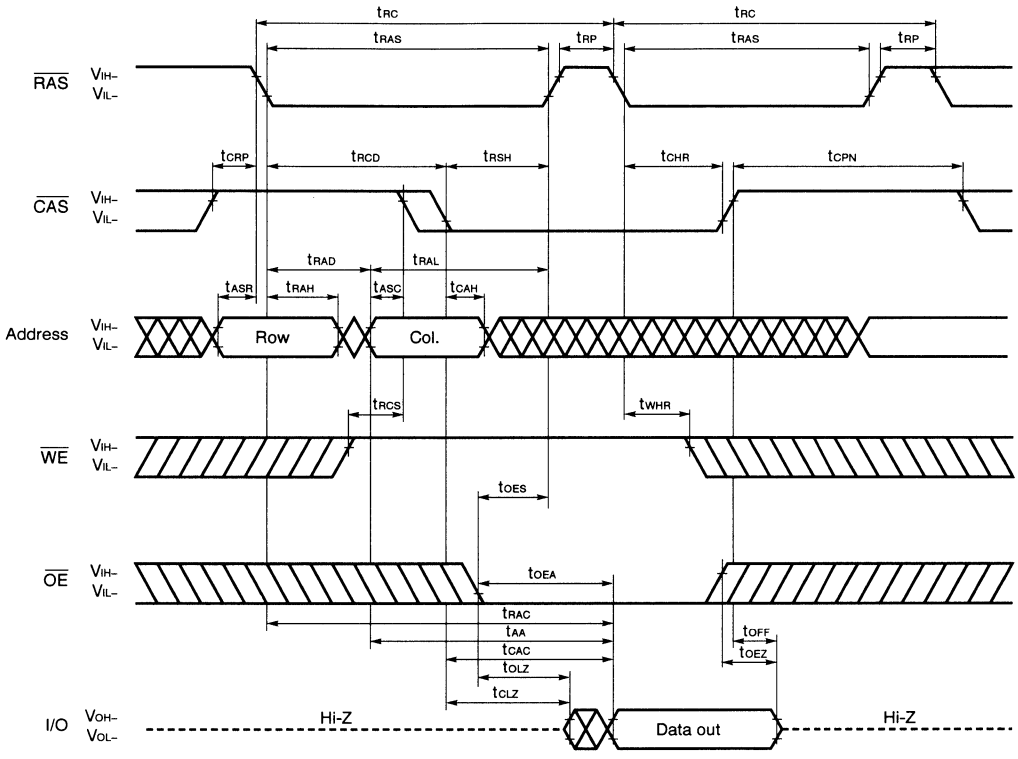
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

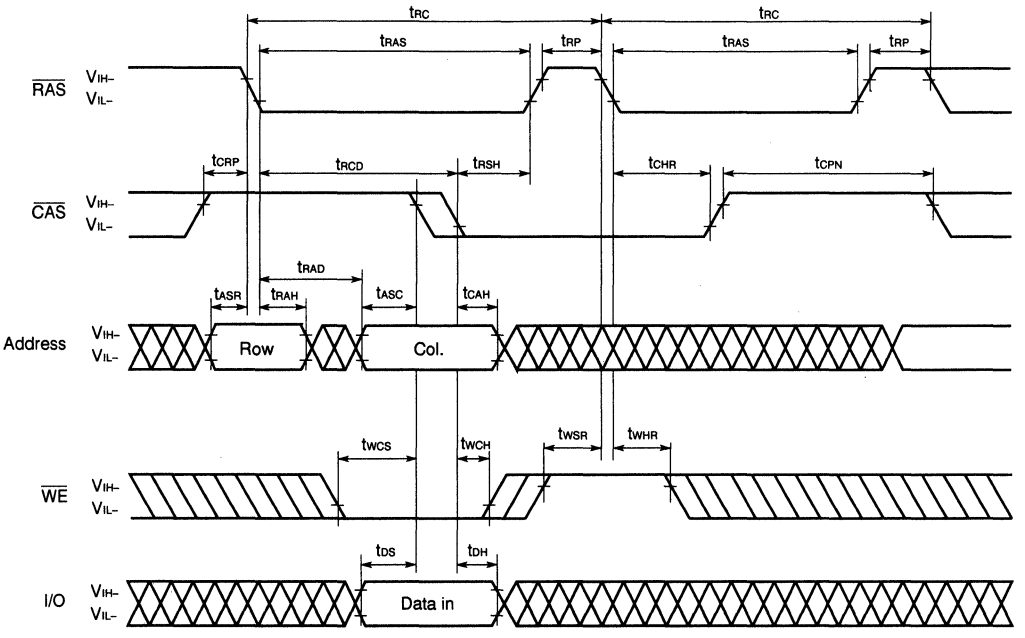


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

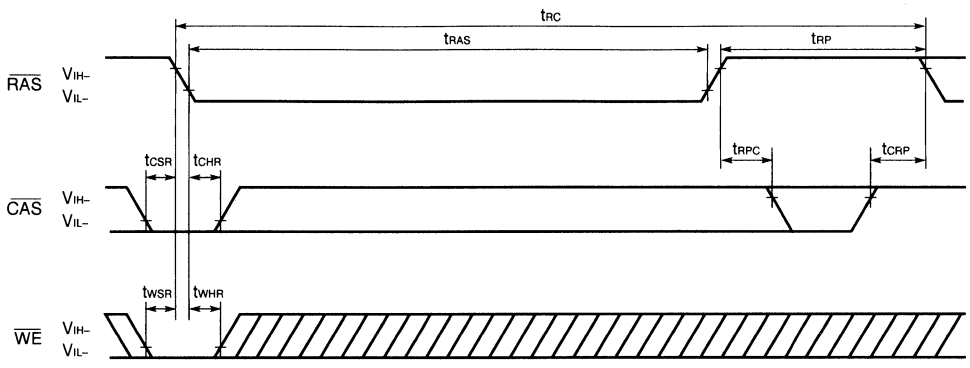


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 16-bit organization during test mode. Don't care about the input level of the $\overline{CAS}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

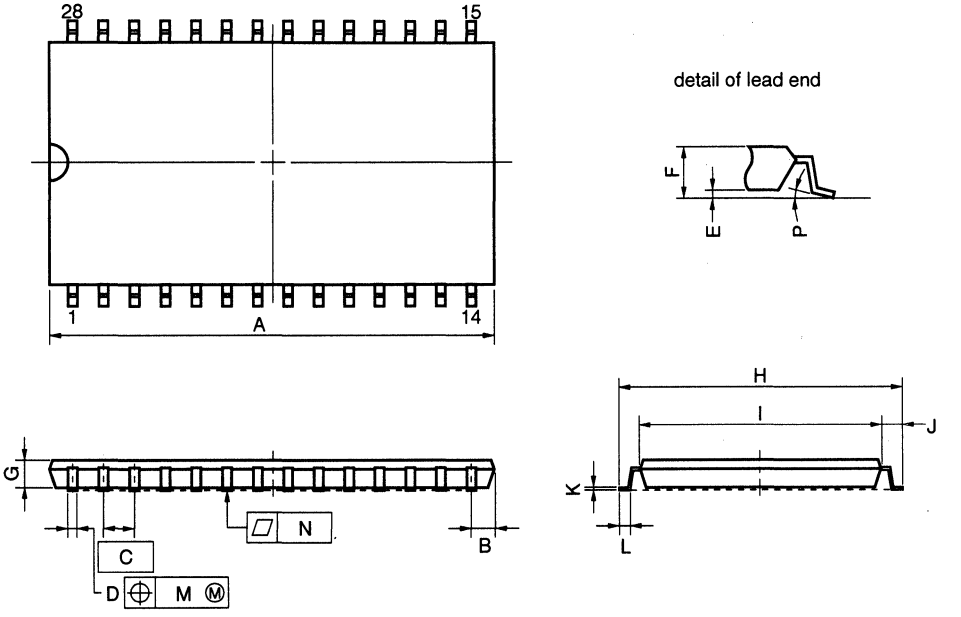
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

28PIN PLASTIC TSOP(II) (400 mil)



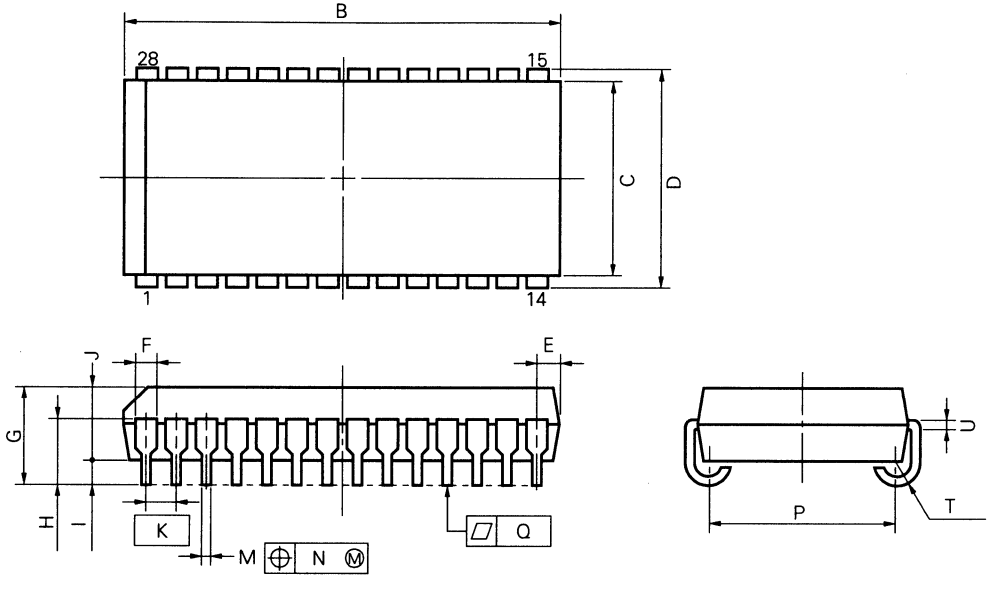
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD3

28 PIN PLASTIC SOJ (400 mil)



P28LE-400A1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S17800L, 4217800L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S17800LG5, 4217800LG5: 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S17800LLE, 4217800LLE: 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD42S18160L, 4218160L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM
1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S18160L, 4218160L are 1,048,576 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 50-pin plastic TSOP (III) and 42-pin plastic SOJ.

Features

- 1,048,576 words by 16 bits organization
- Fast page mode
- Fast access and cycle time
- Single +3.3 V ± 0.3 V power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S18160L-A60, 4218160L-A60	540 mW	60 ns	110 ns	40 ns
μPD42S18160L-A70, 4218160L-A70	504 mW	70 ns	130 ns	45 ns

- The μPD42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

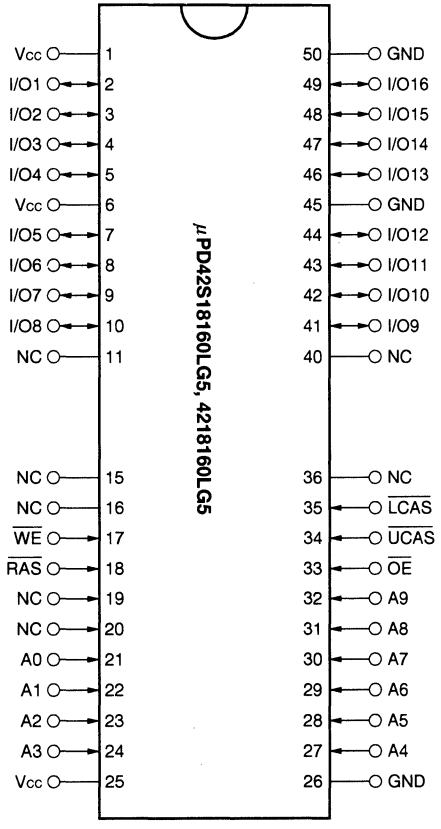
Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S18160L	1,024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.54 mW (CMOS level input)
μPD4218160L	1,024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	1.8 mW (CMOS level input)

Ordering Information

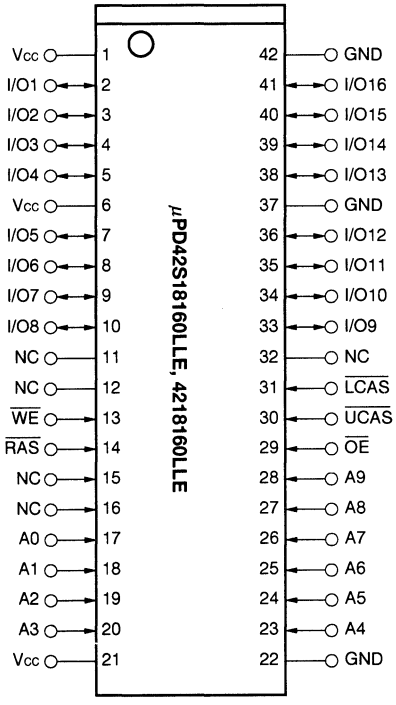
Part number	Access time (MAX.)	Package	Refresh
μPD42S18160LG5-A60 μPD42S18160LG5-A70	60 ns 70 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18160LLE-A60 μPD42S18160LLE-A70	60 ns 70 ns	42-pin plastic SOJ (400 mil)	
μPD4218160LG5-A60 μPD4218160LG5-A70	60 ns 70 ns	50-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218160LLE-A60 μPD4218160LLE-A70	60 ns 70 ns	42-pin plastic SOJ (400 mil)	

Pin Configurations (Marking Side)

50-pin Plastic TSOP (II) (400 mil)

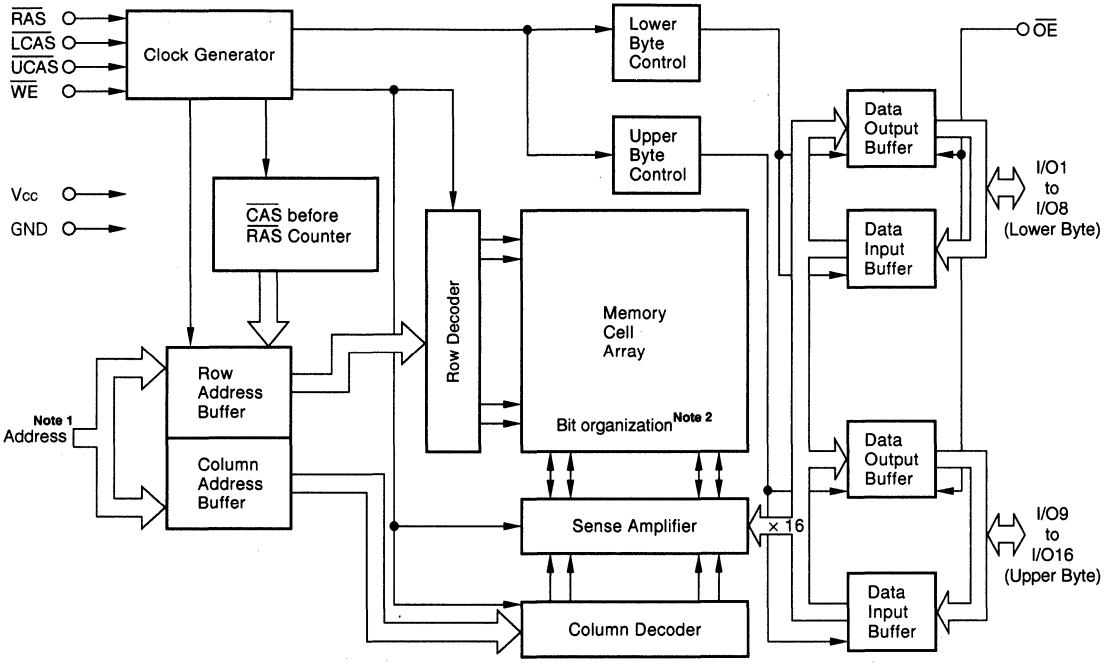


42-pin Plastic SOJ (400 mil)



A0 to A9	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S18160L, 4218160L	A0 - A9	A0 - A9

2. μPD42S18160L, 4218160L ··· 1,024 × 1,024 × 16

Input/Output Pin Functions

The μPD42S18160L, 4218160L have input pins $\overline{RAS}$, $\overline{CAS}$[Note 1], $\overline{WE}$, $\overline{OE}$, Address[Note 2] and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)	Input	Address bus. Input total 20-bit of address signal, upper bits and lower bits[Note 2] in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/ output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2.

Part number	Address inputs	Upper bits	Lower bits
μPD42S18160L, 4218160L	A0 - A9	10 bits	10 bits

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−0.5 to +4.6	V
Supply voltage	V_{CC}		−0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low level input voltage	V_{IL}		−0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

[MEMO]

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1, 2, 3
				t_{RAC} = 70 ns		140		
Standby current	μPD42S18160L	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			0.5	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.15		
	μPD4218160L		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1, 2, 3, 4
				t_{RAC} = 70 ns		140		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 5
				t_{RAC} = 70 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	1, 2
				t_{RAC} = 70 ns		140		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18160L)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ μs		180	μA	1, 2
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μPD42S18160L)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		−5	+5	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		−5	+5	μA	
High level output voltage		V_{OH}	I_O = −2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

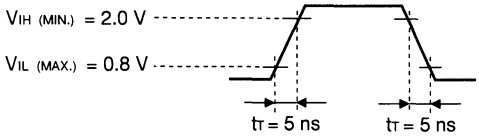
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

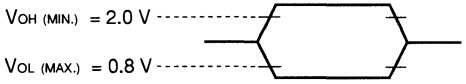
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

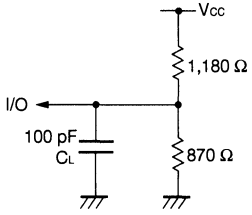
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		t_{RC}	110	–	130	–	ns	
$\overline{RAS}$ precharge time		t_{RP}	40	–	50	–	ns	
$\overline{CAS}$ precharge time		t_{CPN}	10	–	10	–	ns	
$\overline{RAS}$ pulse width		t_{RAS}	60	10,000	70	10,000	ns	1
$\overline{CAS}$ pulse width		t_{CAS}	15	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		t_{RSH}	15	–	18	–	ns	
$\overline{CAS}$ hold time		t_{CSH}	60	–	70	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		t_{RCD}	20	45	20	50	ns	2
$\overline{RAS}$ to column address delay time		t_{RAD}	15	30	15	35	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		t_{CRP}	5	–	5	–	ns	3
Row address setup time		t_{ASR}	0	–	0	–	ns	
Row address hold time		t_{RAH}	10	–	10	–	ns	
Column address setup time		t_{ASC}	0	–	0	–	ns	
Column address hold time		t_{CAH}	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		t_{OES}	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		t_{CLZ}	0	–	0	–	ns	
$\overline{OE}$ to data setup time		t_{OLZ}	0	–	0	–	ns	
$\overline{OE}$ to data delay time		t_{OED}	13	–	15	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		t_{MRH}	0	–	0	–	ns	
Transition time (rise and fall)		t_T	3	50	3	50	ns	
Refresh time	μPD42S18160L	t_{REF}	–	128	–	128	ms	
	μPD4218160L		–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	158	–	180	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83	–	95	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	38	–	40	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	53	–	60	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	ns	
Read modify write cycle time	t_{PRWC}	83	–	90	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	58	–	65	–	ns	1

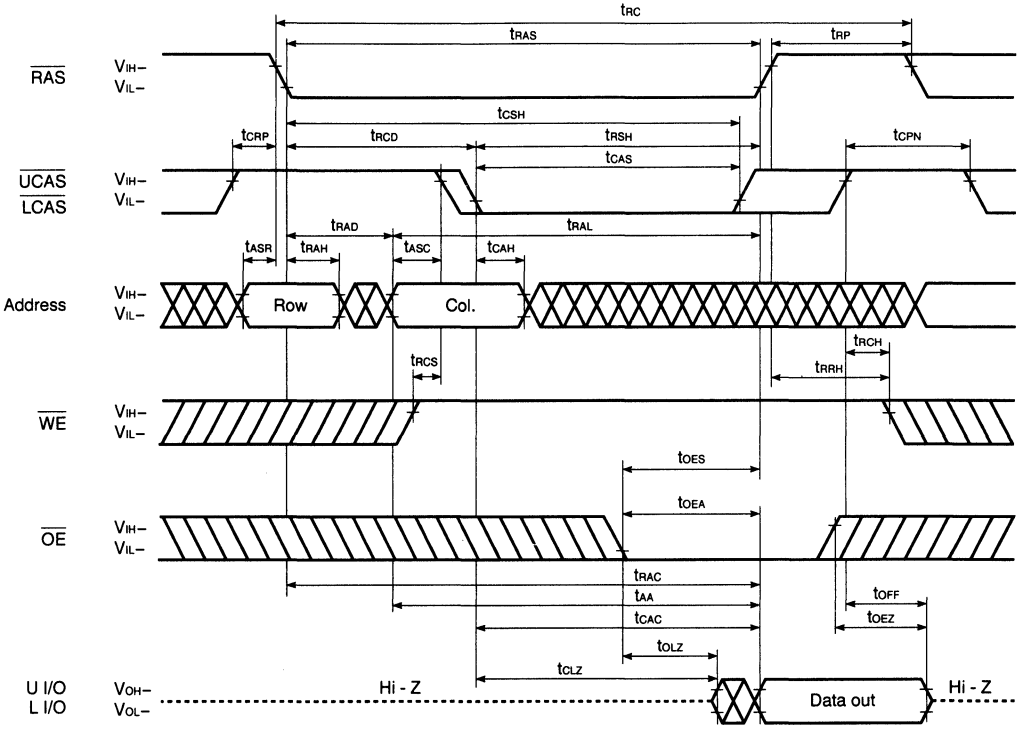
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

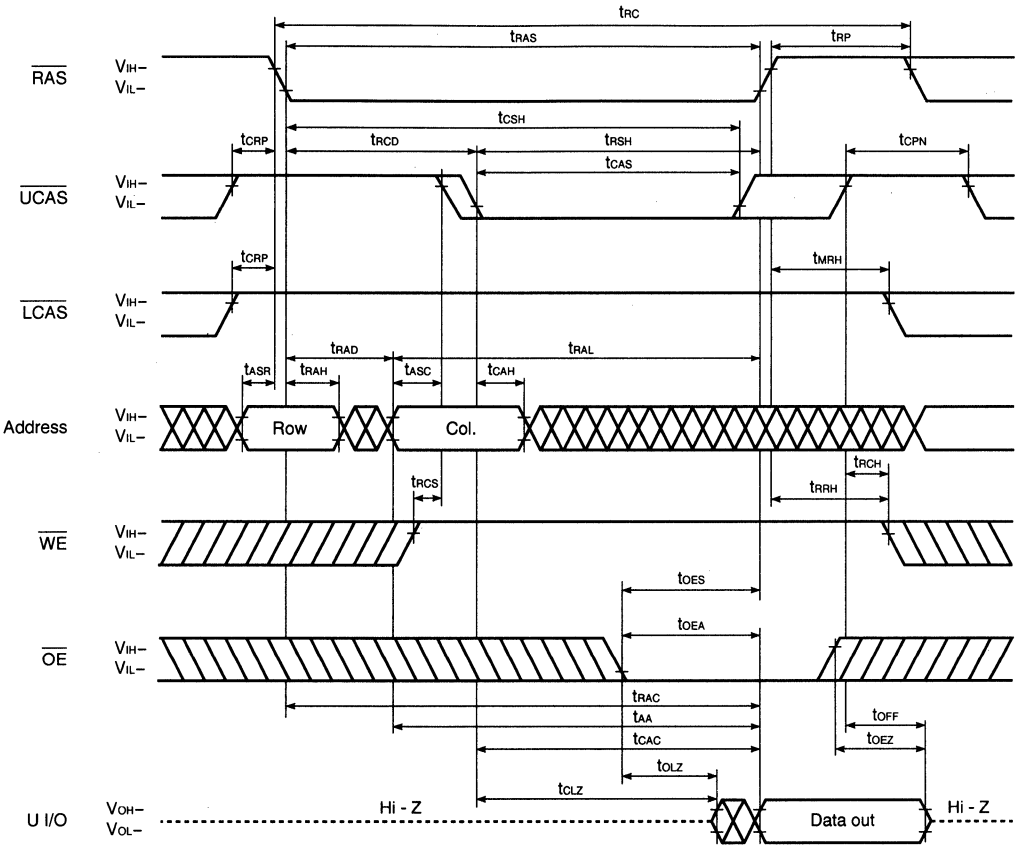
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S18160L.

Read Cycle

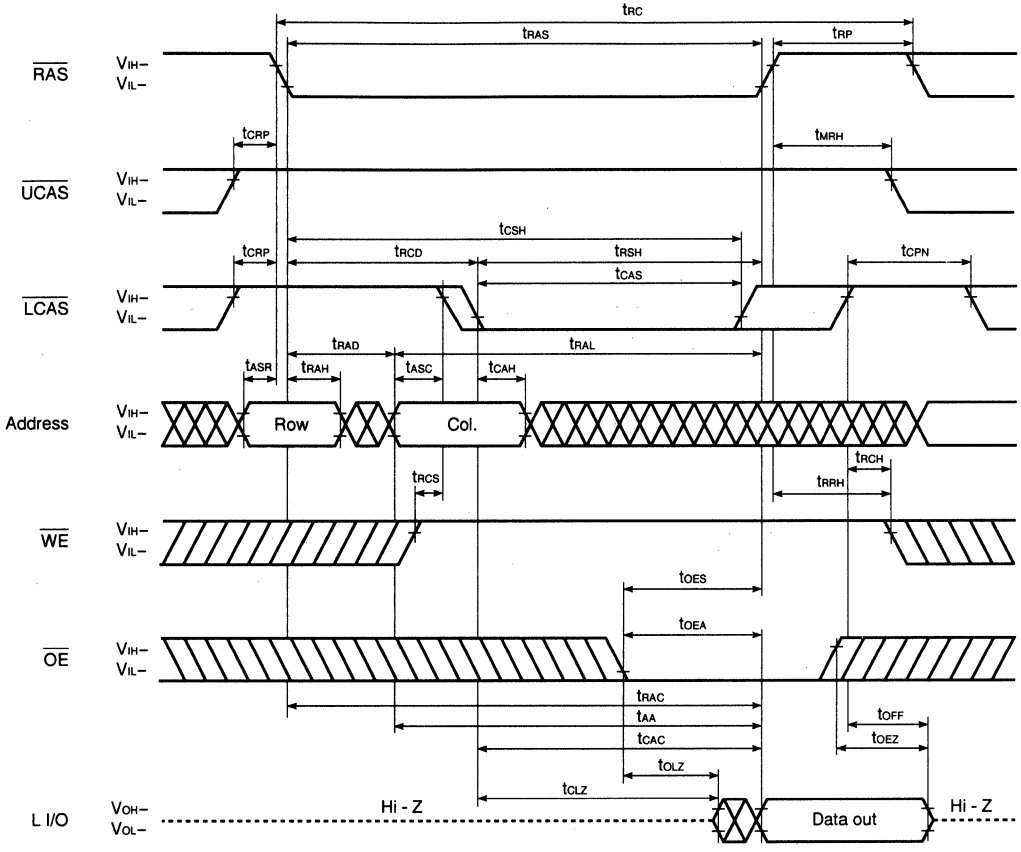

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tOEZ
tCAC
tOLZ
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



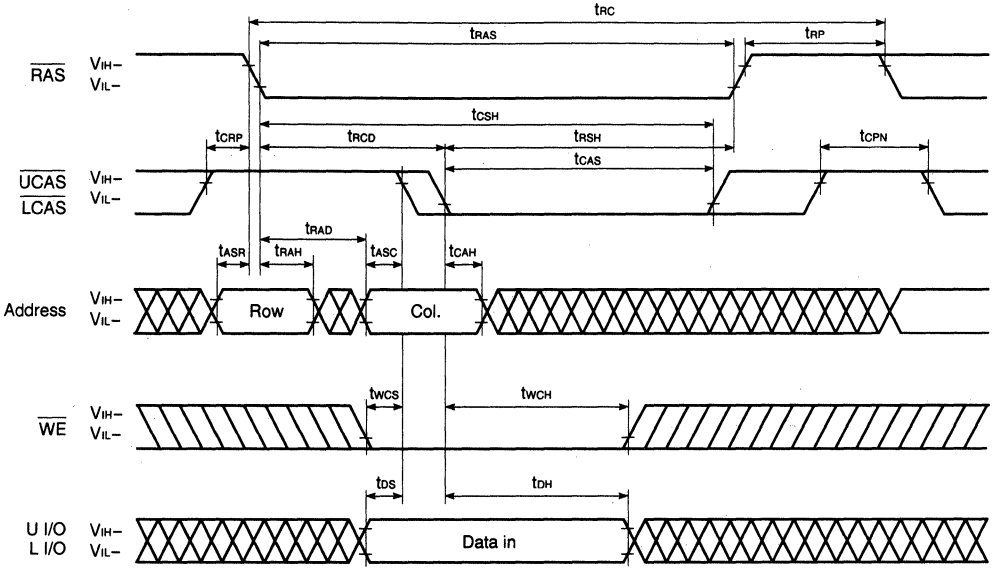
Remark L I/O: Hi-Z

Lower Byte Read Cycle



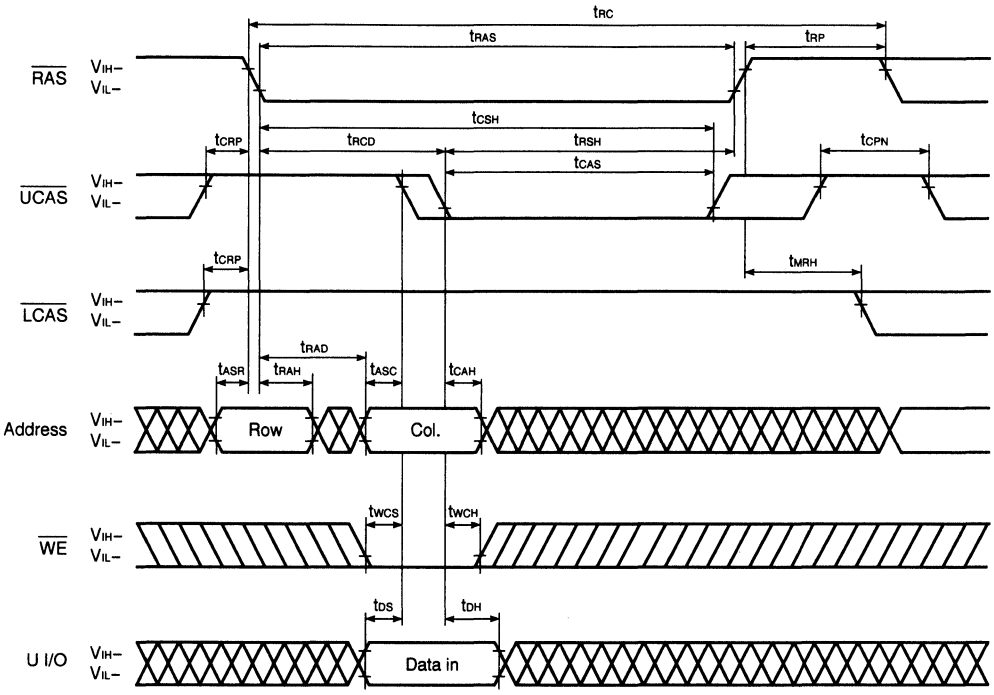
Remark U I/O: Hi-Z

Early Write Cycle



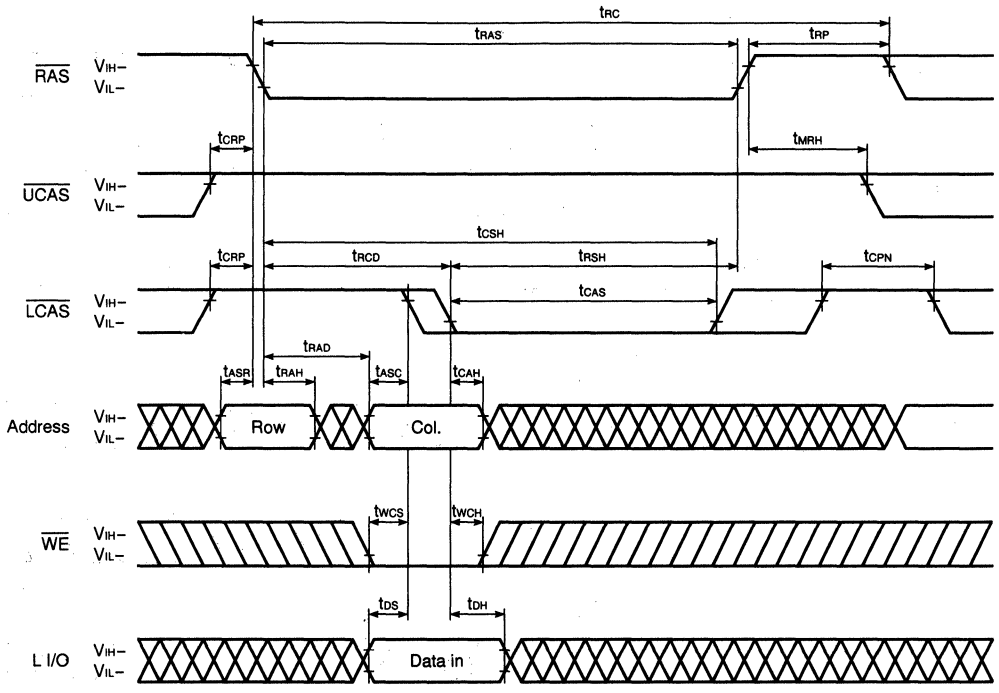
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



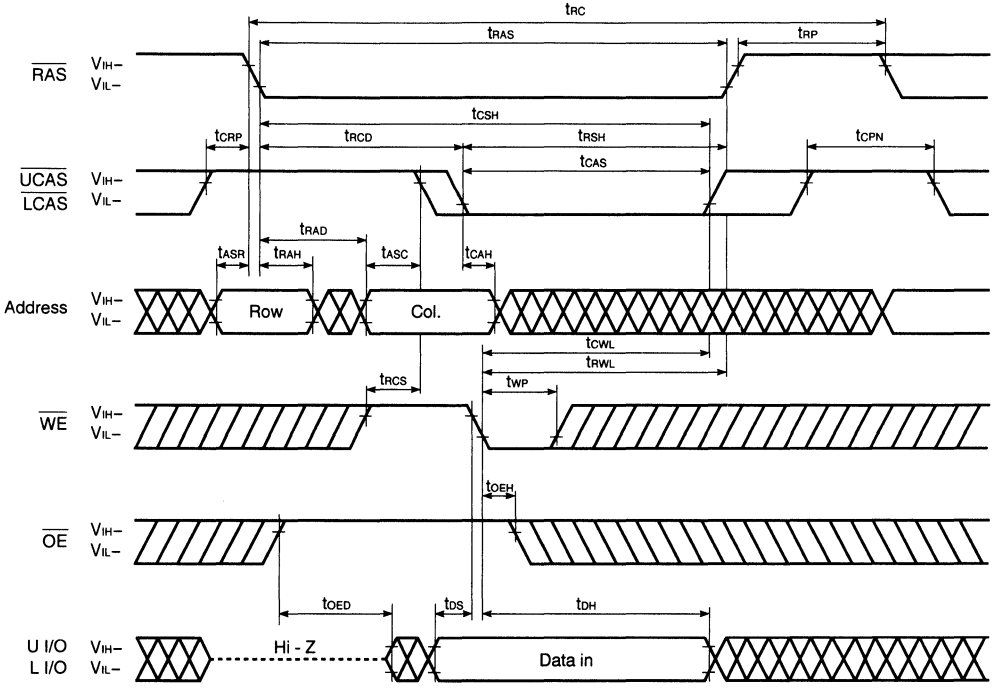
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

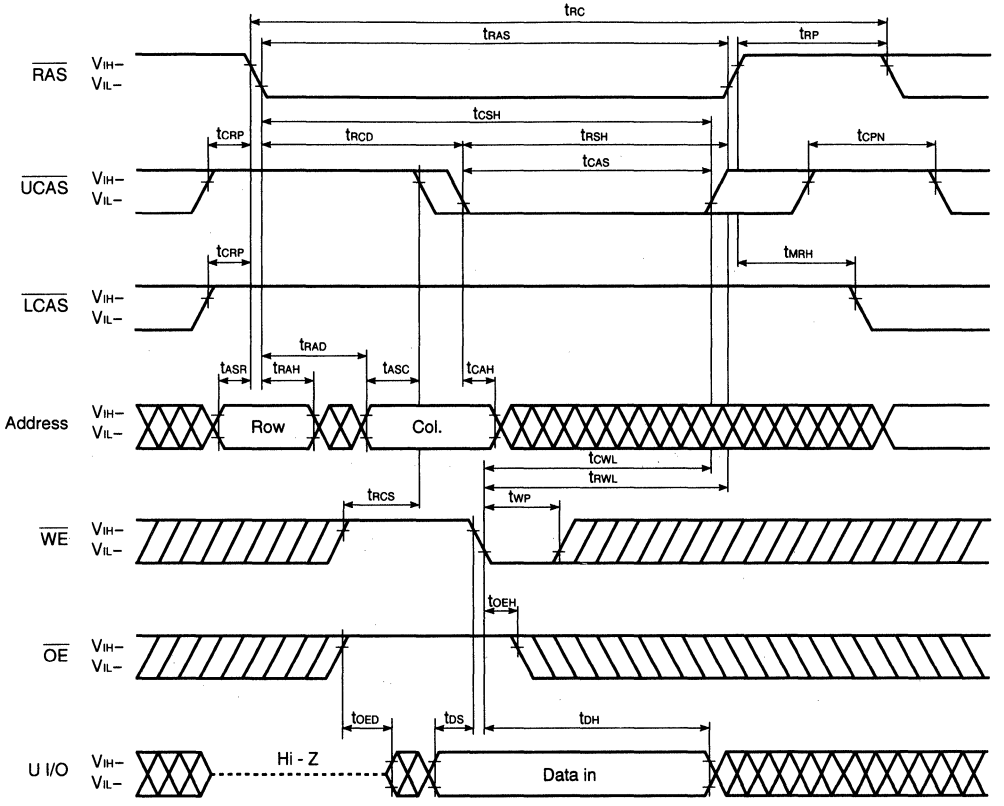


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

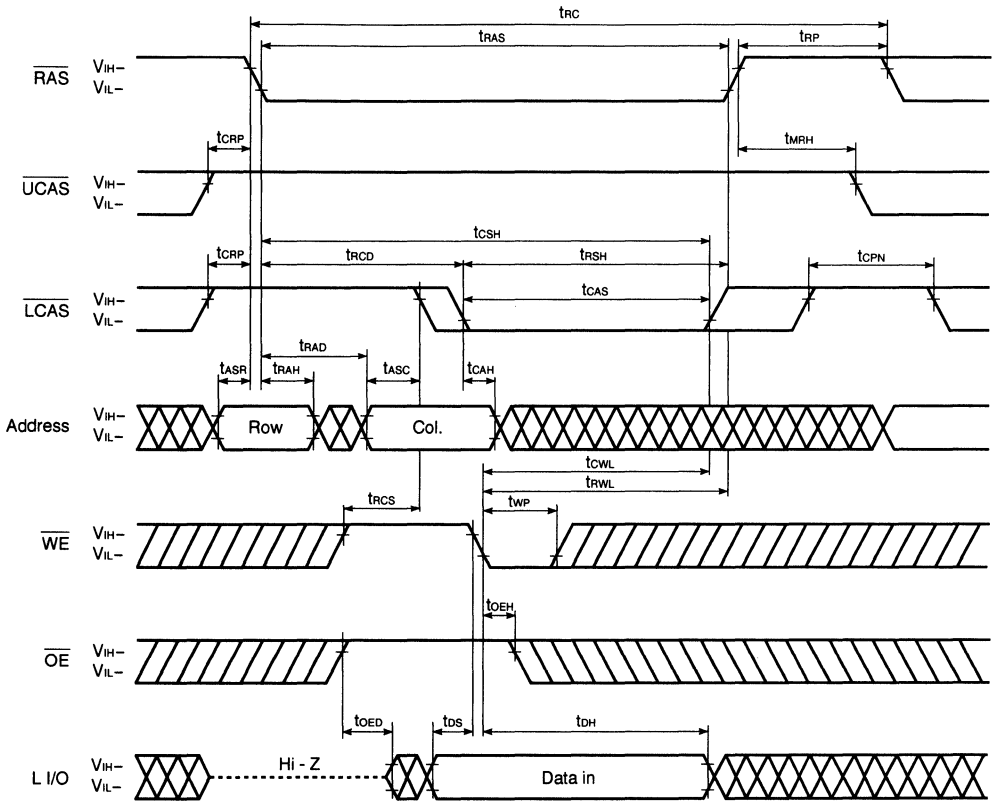


Upper Byte Late Write Cycle



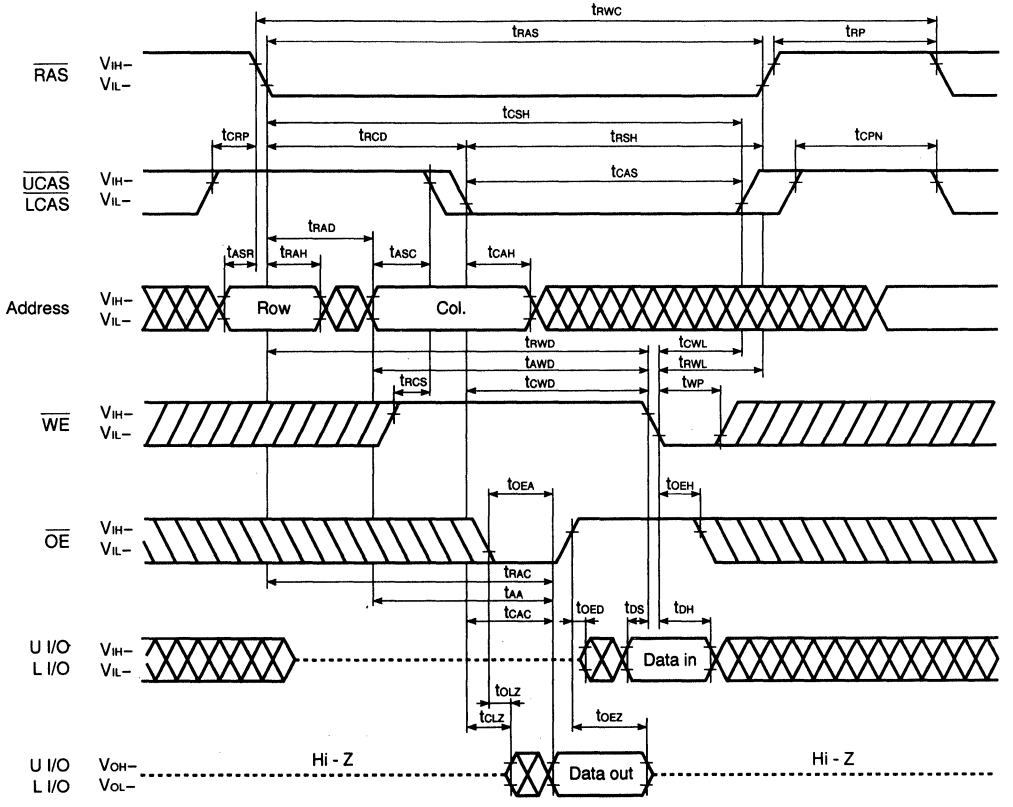
Remark L I/O: Don't care

Lower Byte Late Write Cycle

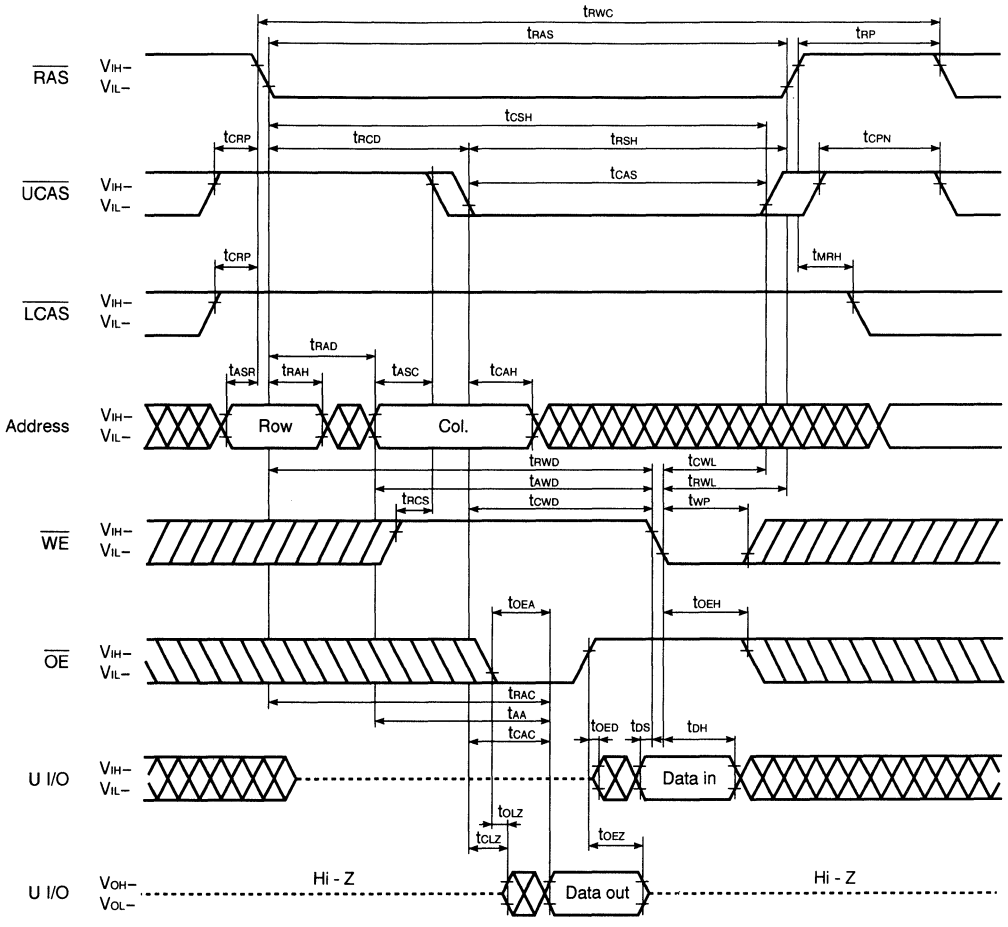


Remark U I/O: Don't care

Read Modify Write Cycle

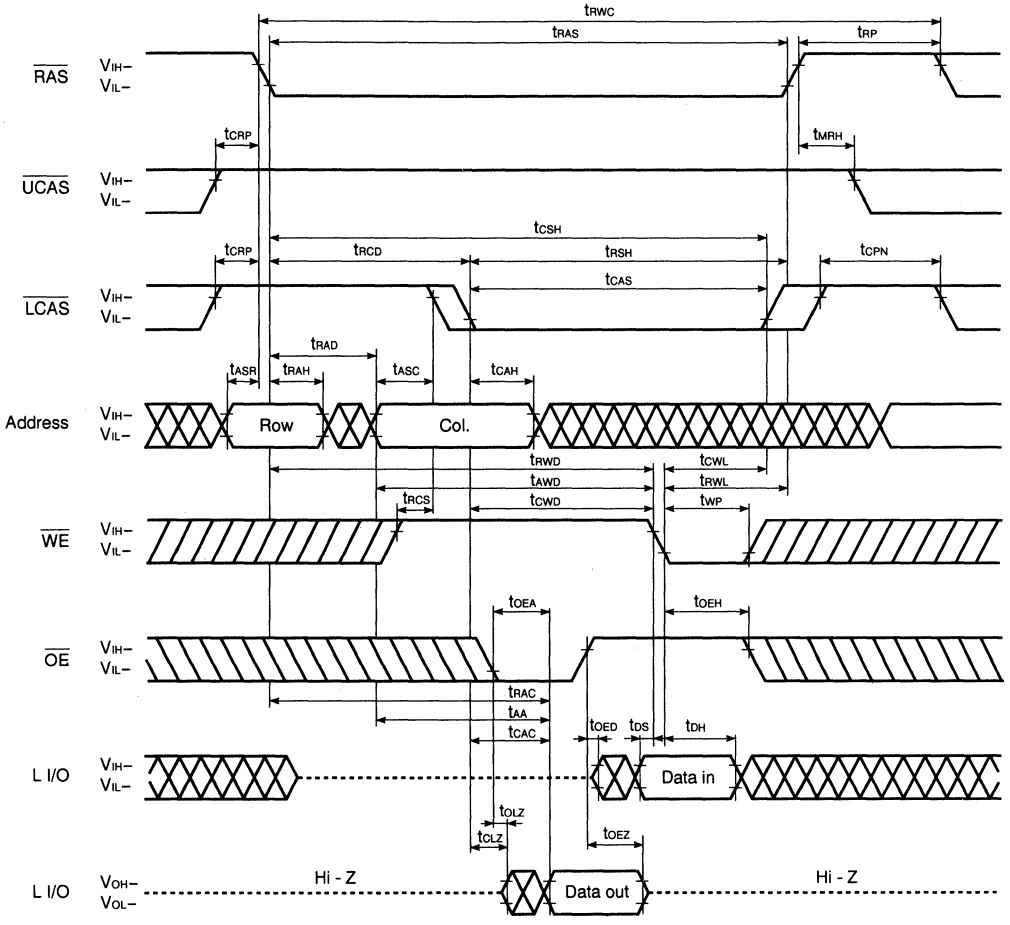


Upper Byte Read Modify Write Cycle



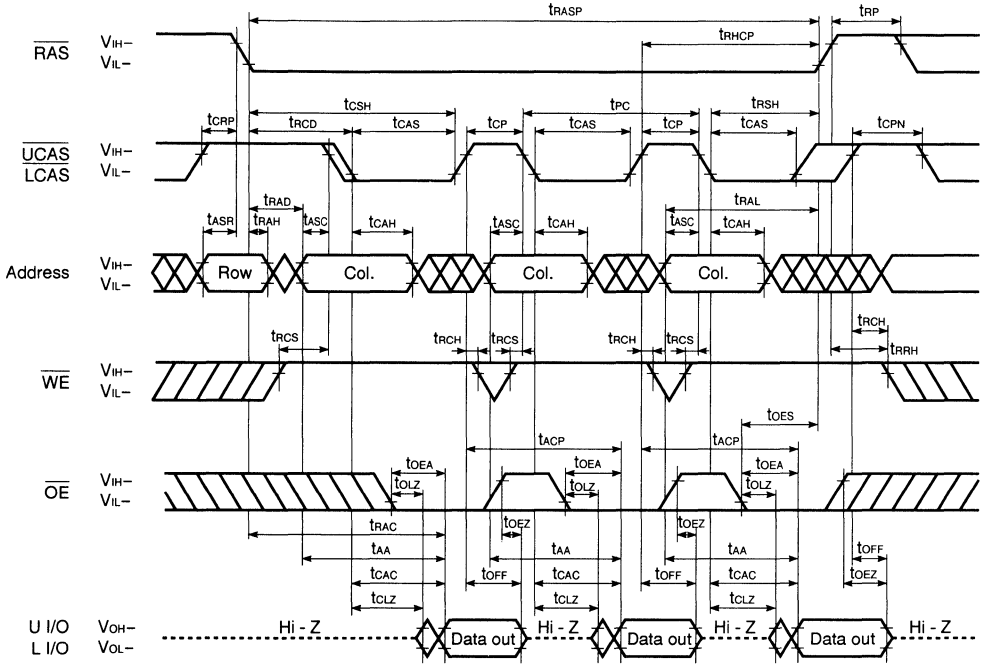
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



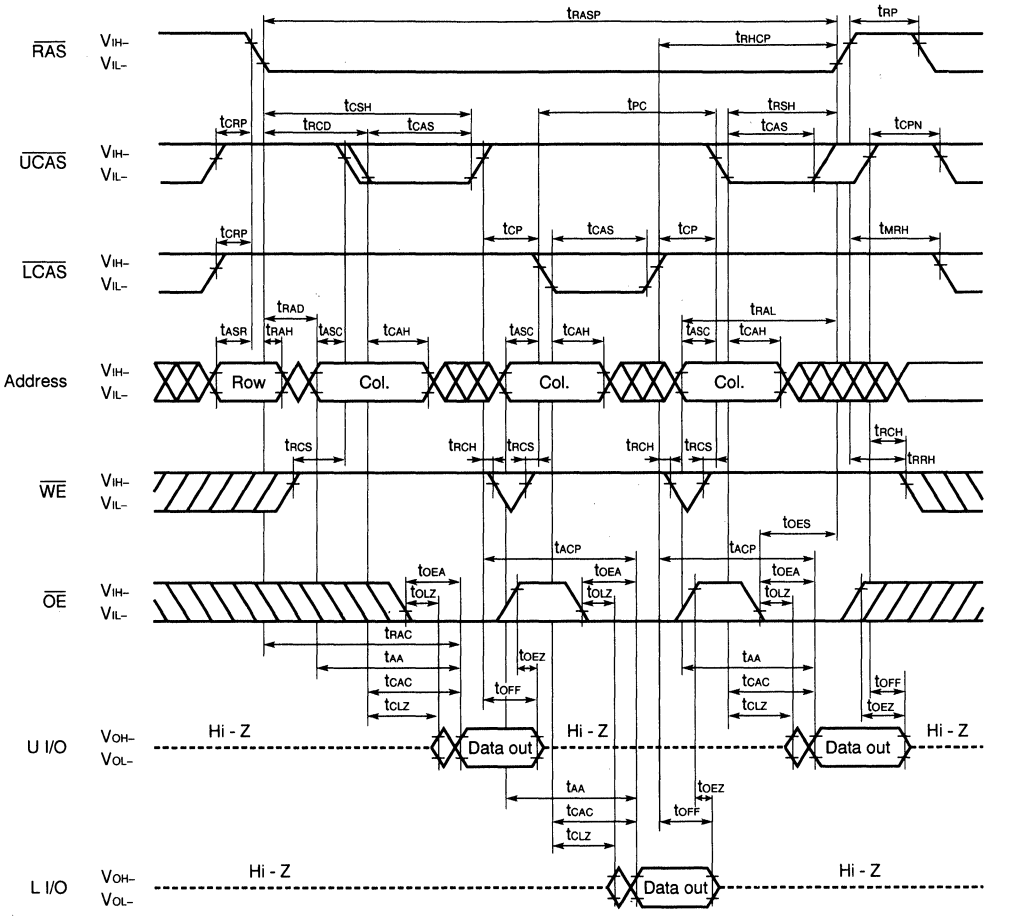
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

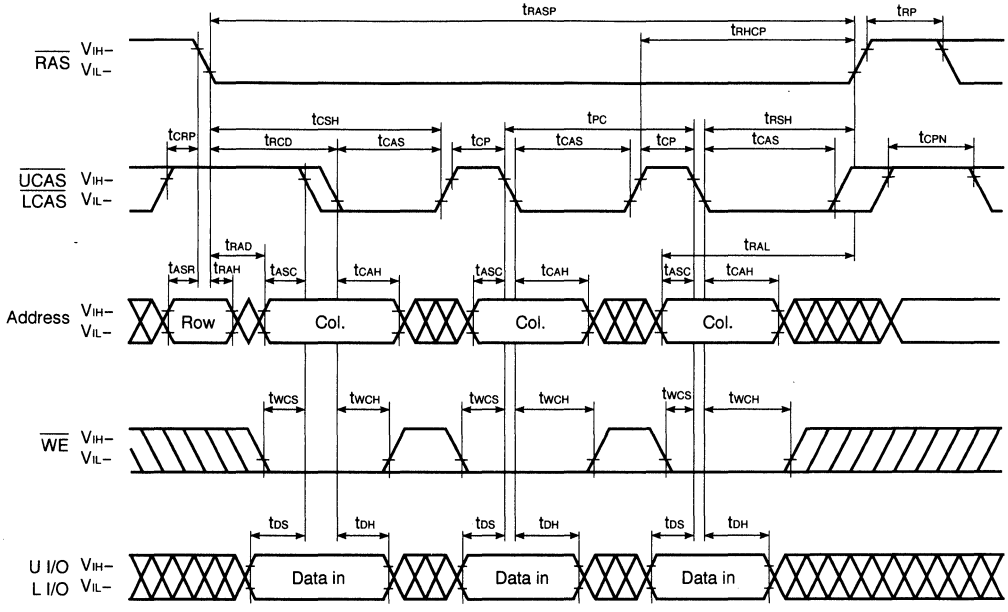
Fast Page Mode Byte Read Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

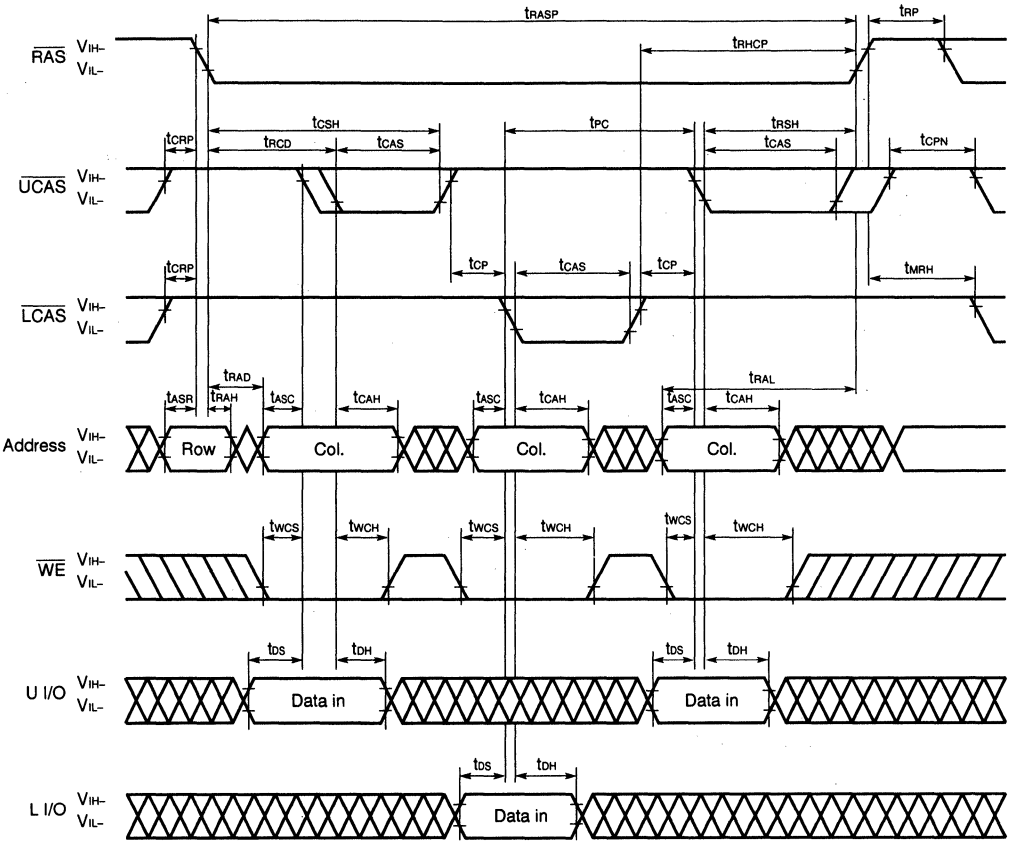
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

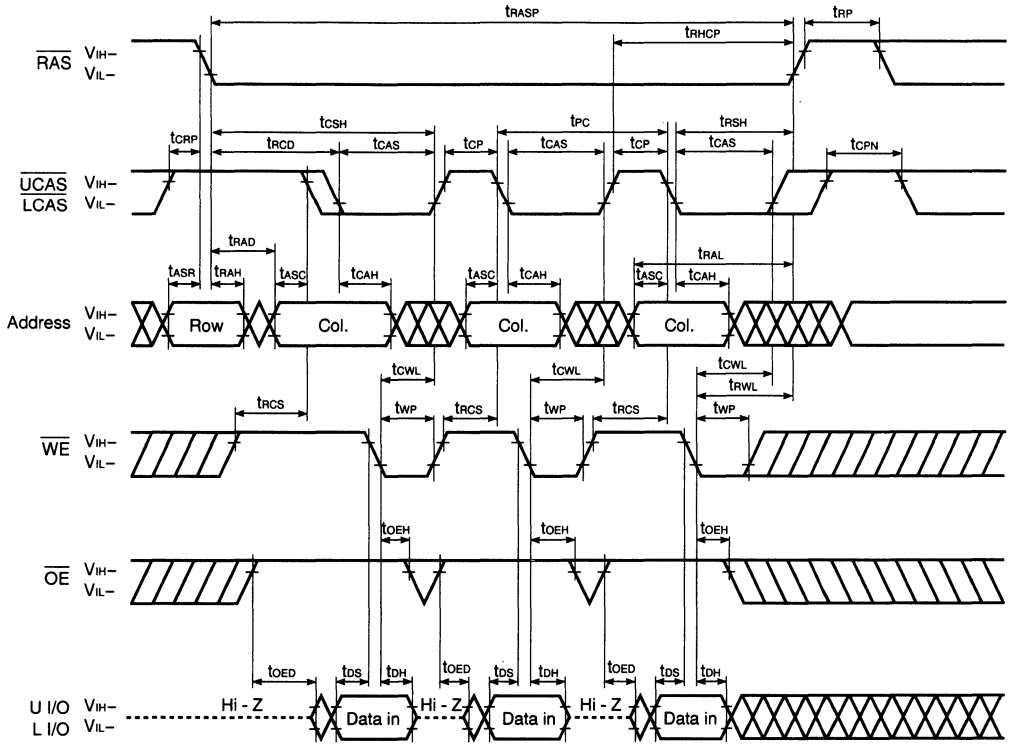
Fast Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

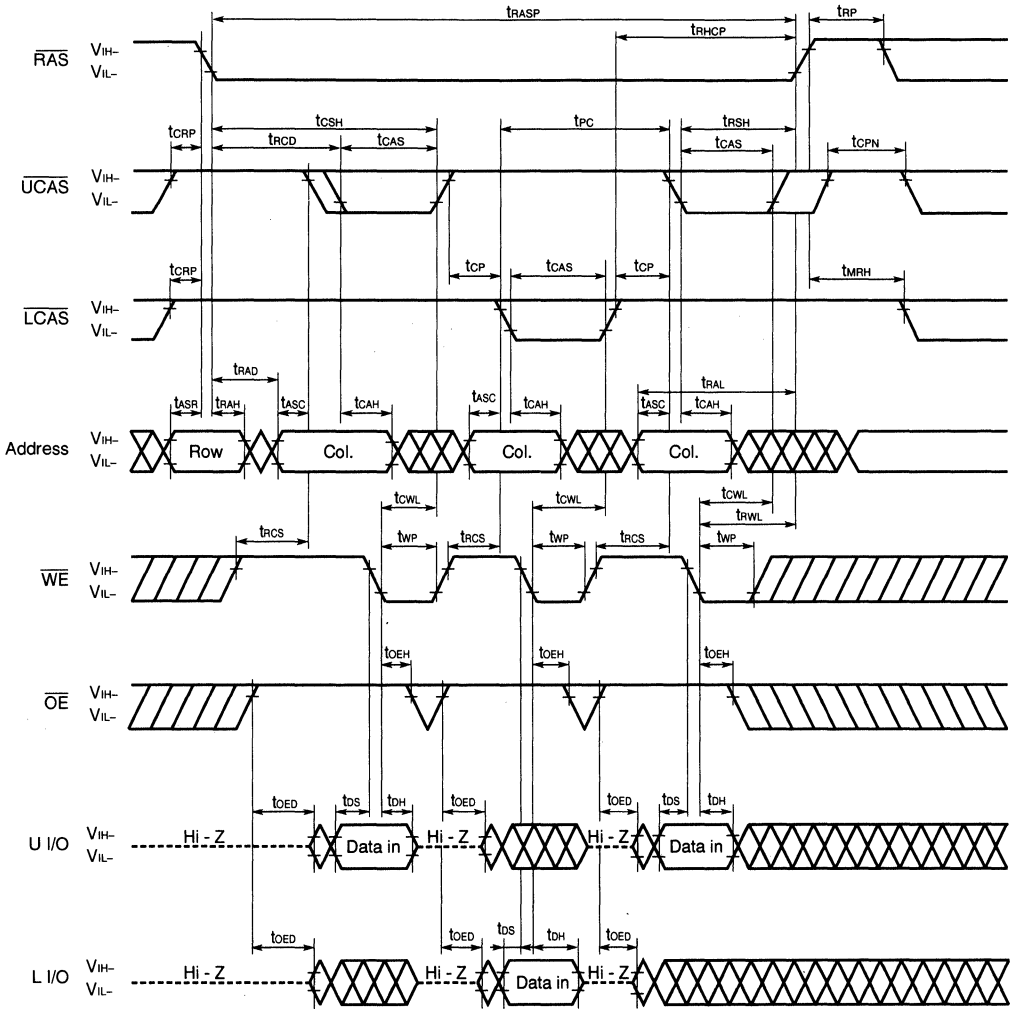
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

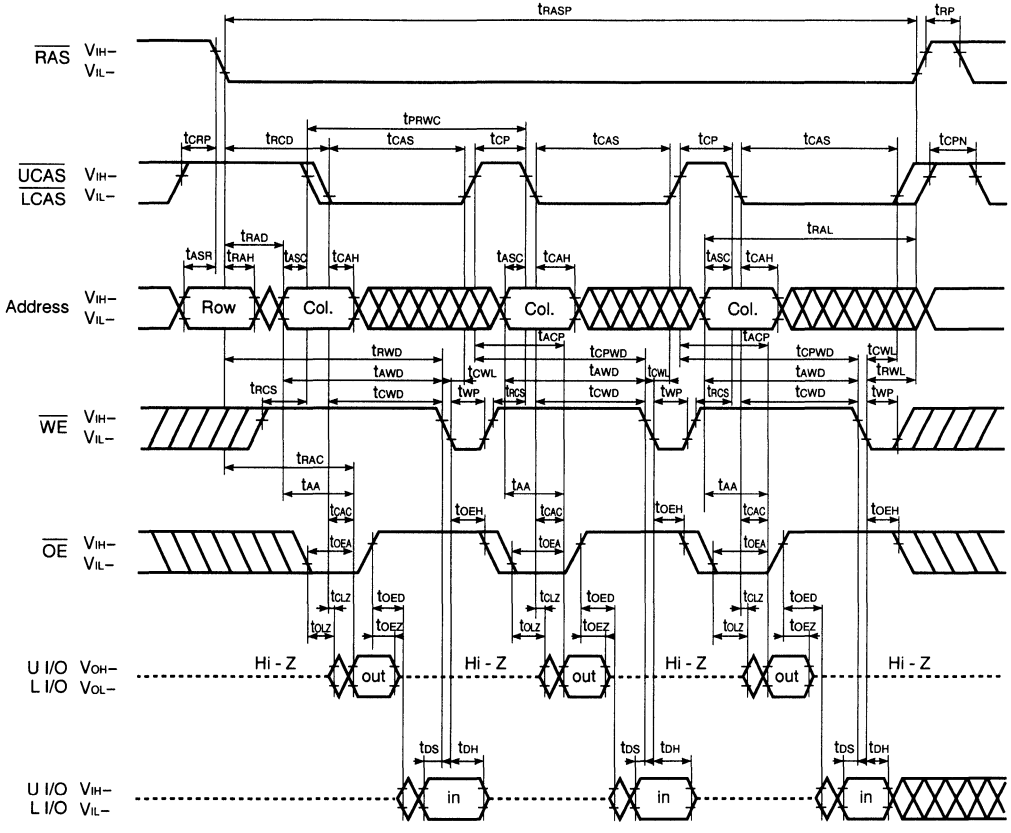
Fast Page Mode Byte Late Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

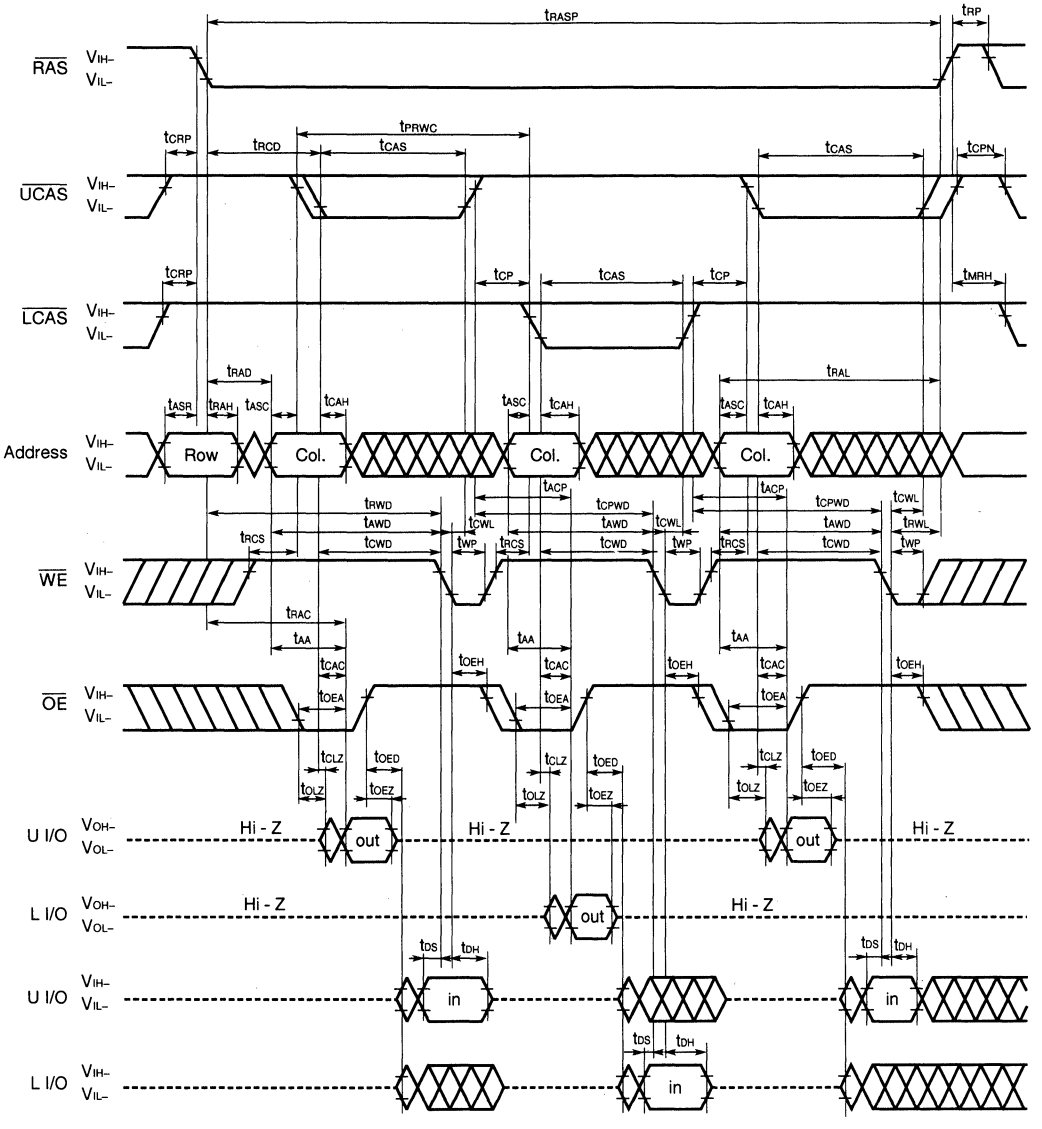
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

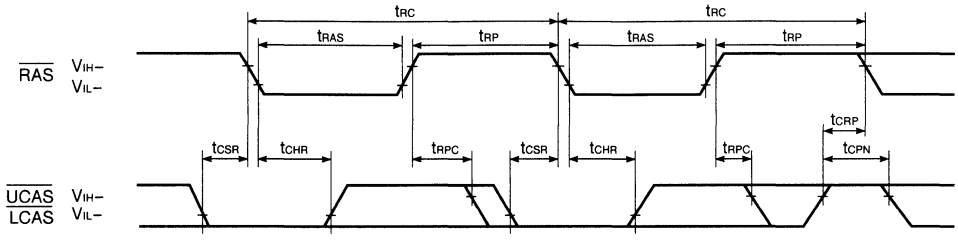
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160L)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160L: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

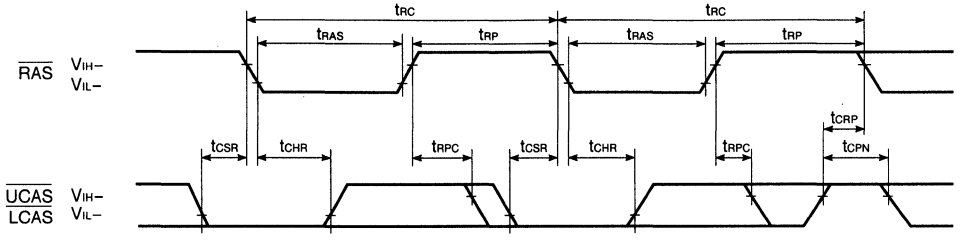
μPD42S18160L: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160L: 1,024 times within a 128 ms interval

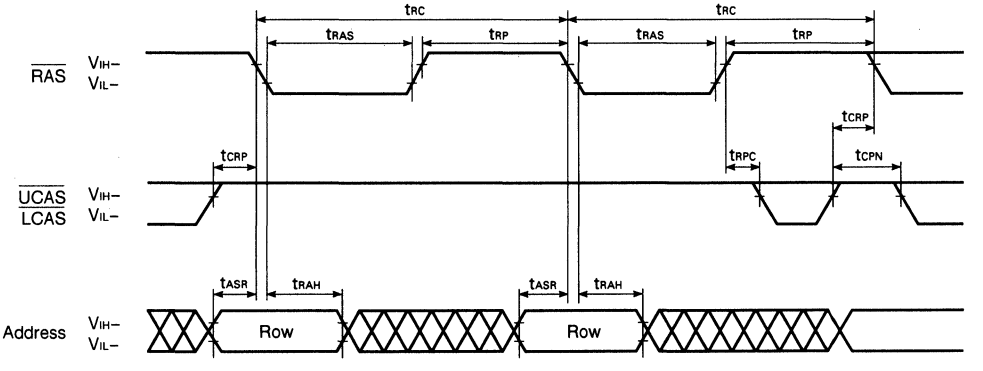
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



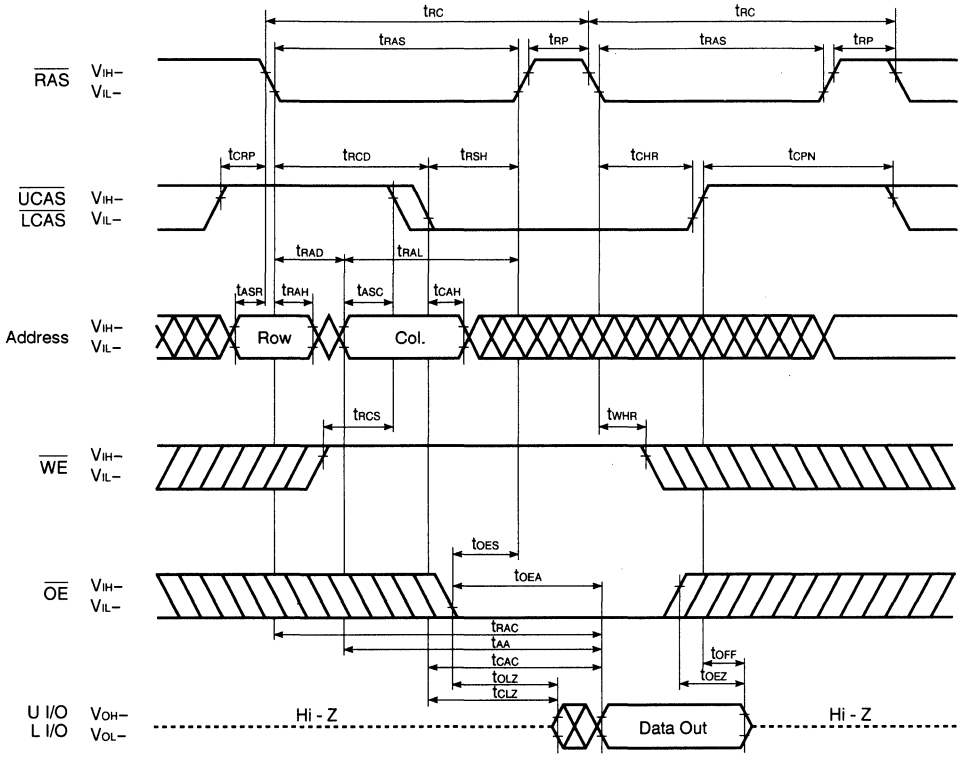
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

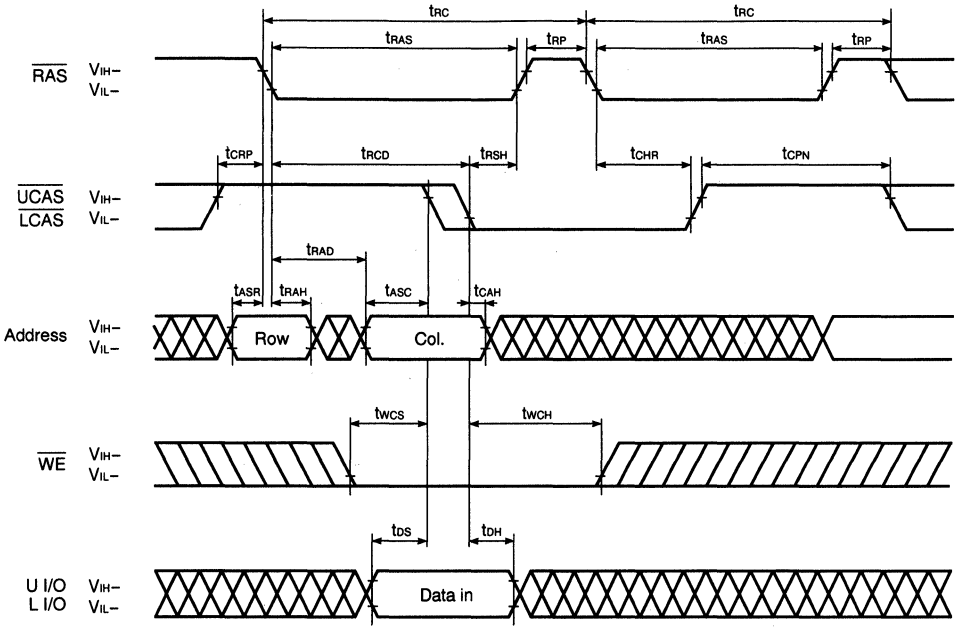


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



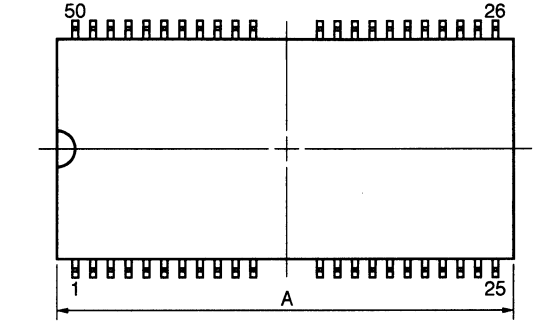
Hidden Refresh Cycle (Write)



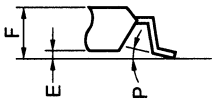
Remark $\overline{OE}$: Don't care

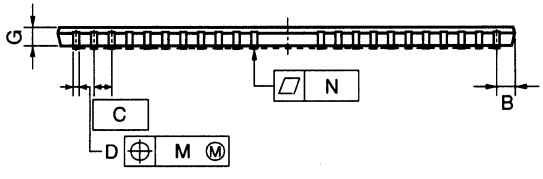
Package Drawings

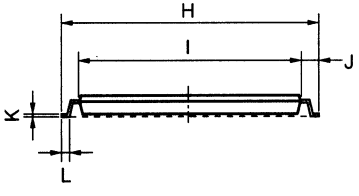
50PIN PLASTIC TSOP(II) (400 mil)



detail of lead end







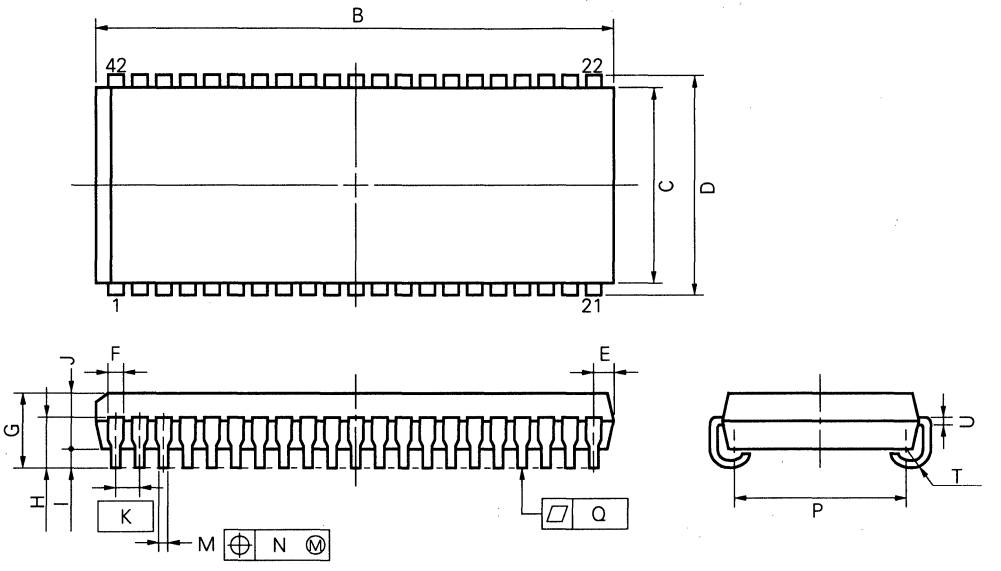
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S50G5-80-7JF4

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S18160L, 4218160L.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S18160LG5, 4218160LG5: 50-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S18160LLE, 4218160LLE: 42-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

Fast Page Mode
4M Dynamic RAM
[5.0V ± 10%]

NEC

MOS INTEGRATED CIRCUIT

μPD424400

4 M-BIT DYNAMIC RAM
1 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μPD424400 is a 1,048,576 words by 4 bits CMOS dynamic RAM. The fast page mode capability realizes high speed access and low power consumption.

The device is packaged in 26-pin plastic TSOP (II) and 26-pin plastic SOJ.

Features

- 1,048,576 words by 4 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD424400-60	495 mW	60 ns	120 ns	40 ns
μPD424400-70	440 mW	70 ns	140 ns	45 ns
μPD424400-80	440 mW	80 ns	160 ns	50 ns

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD424400	1,024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

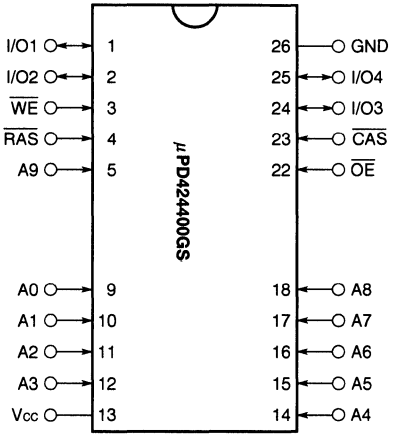
- Multiplexed address inputs ····· Row address: A0 - A9, Column address: A0 - A9

Ordering Information

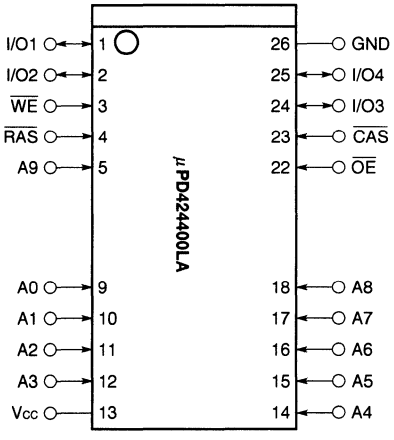
Part number	Access time (MAX.)	Package	Refresh
μPD424400GS-60	60 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424400GS-70	70 ns		
μPD424400GS-80	80 ns		
μPD424400LA-60	60 ns	26-pin plastic SOJ (300 mil)	
μPD424400LA-70	70 ns		
μPD424400LA-80	80 ns		

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)

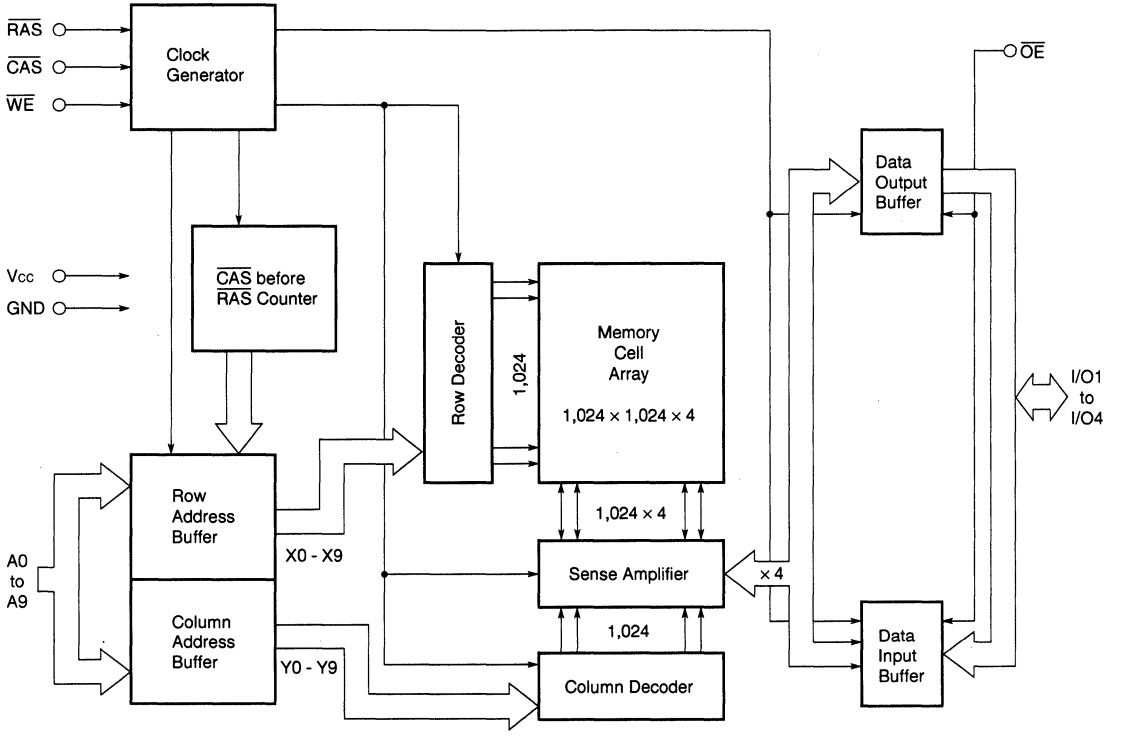


26-pin Plastic SOJ (300 mil)



A0 to A9 : Address Inputs
I/O1 to I/O4 : Data Inputs/Outputs
$\overline{RAS}$: Row Address Strobe
$\overline{CAS}$: Column Address Strobe
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
Vcc : Power Supply
GND : Ground

Block Diagram



Input/Output Pin Functions

The μPD424400 has input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/04.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)	Input	Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1,048,576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 3
			t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		80		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, I_O = 0 mA			1.0		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2, 3 ,4
			t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		80		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		70	mA	1, 2, 5
			t_{RAC} = 70 ns		60		
			t_{RAC} = 80 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	1, 2
			t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		80		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{PC}).

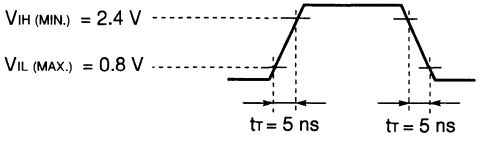
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

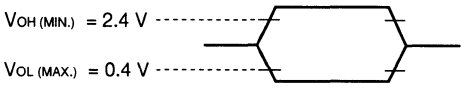
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

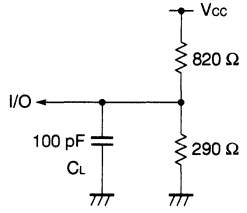
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	tRC	110	–	130	–	160	–	ns	
$\overline{RAS}$ precharge time	tRP	40	–	50	–	70	–	ns	
$\overline{CAS}$ precharge time	tCPN	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	tRSH	15	–	20	–	20	–	ns	
$\overline{CAS}$ hold time	tCSH	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	25	60	ns	2
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	17	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10	–	10	–	10	–	ns	3
Row address setup time	tASR	0	–	0	–	0	–	ns	
Row address hold time	tRAH	10	–	10	–	12	–	ns	
Column address setup time	tASC	0	–	0	–	0	–	ns	
Column address hold time	tCAH	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$	tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time	tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time	tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time	tOED	15	–	15	–	20	–	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	
Refresh time	tREF								
		–	16	–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs. If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	10	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	15	–	15	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	15	–	15	–	15	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	150	–	175	–	210	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	90	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	–	40	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	55	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

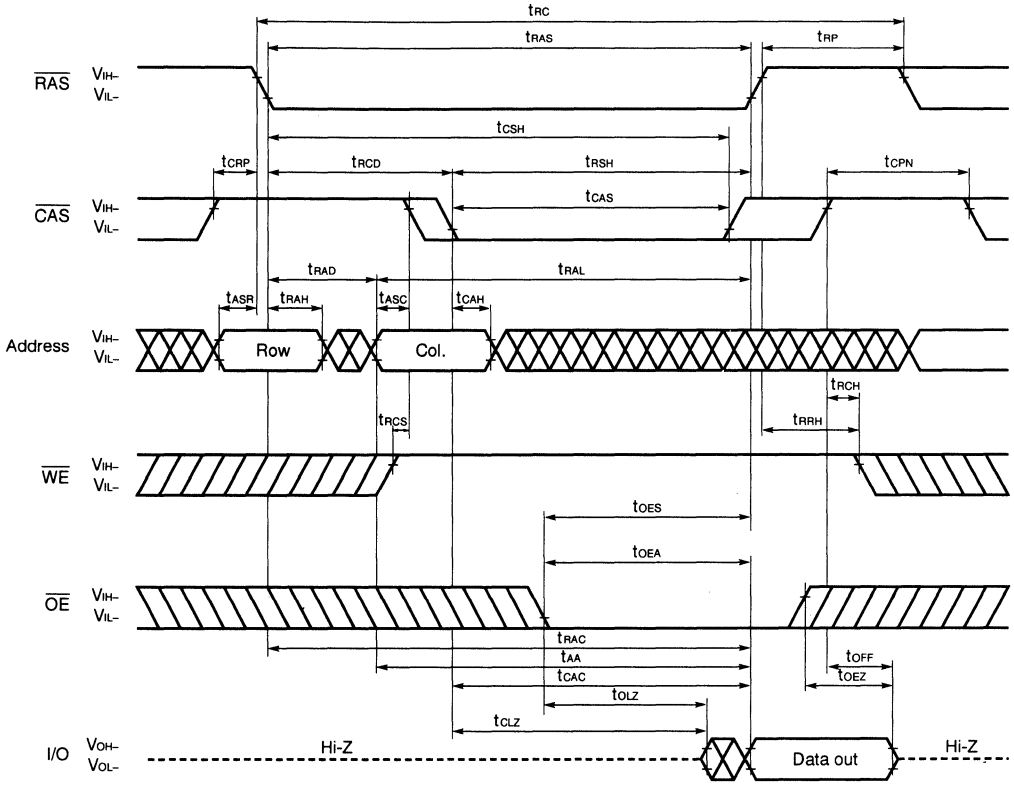
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	80	–	85	–	95	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55	–	60	–	70	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

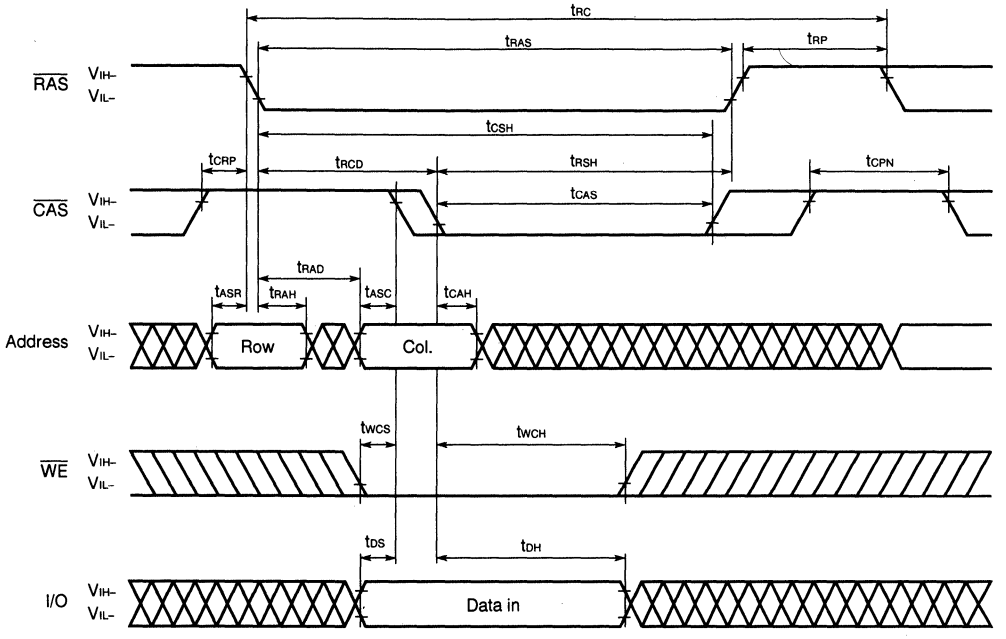
Refresh Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	15	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{WE}$ setup time	t_{WSR}	0	–	0	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	10	–	10	–	15	–	ns	

Read Cycle

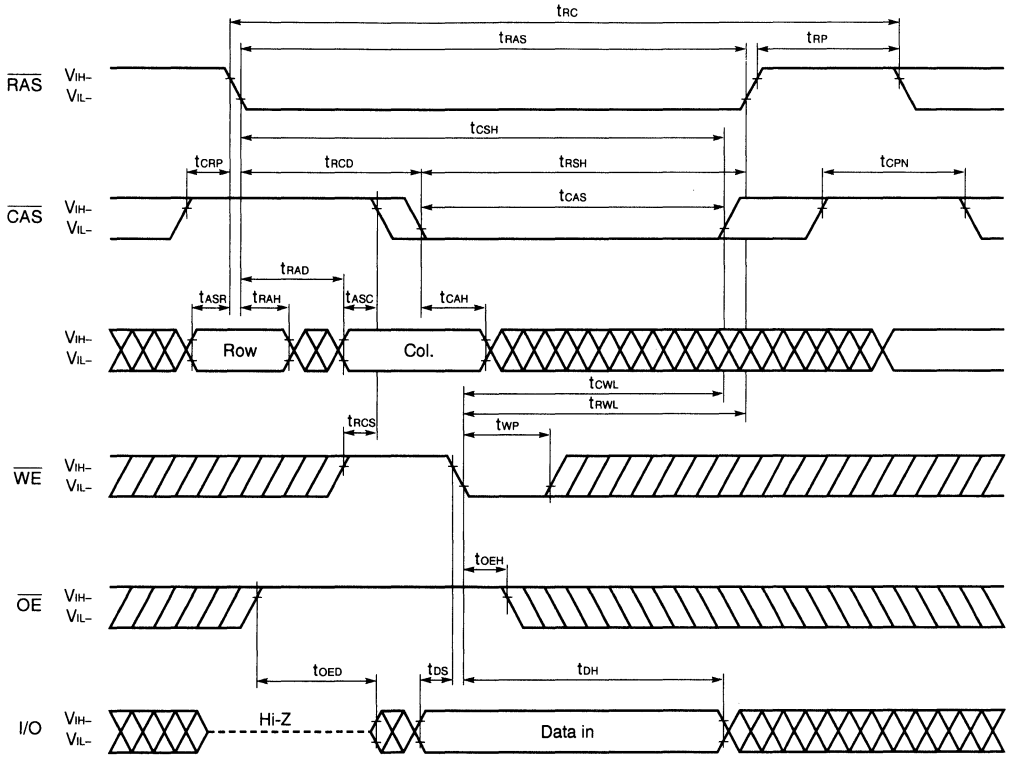

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tCAC
tOEZ
tOLZ
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

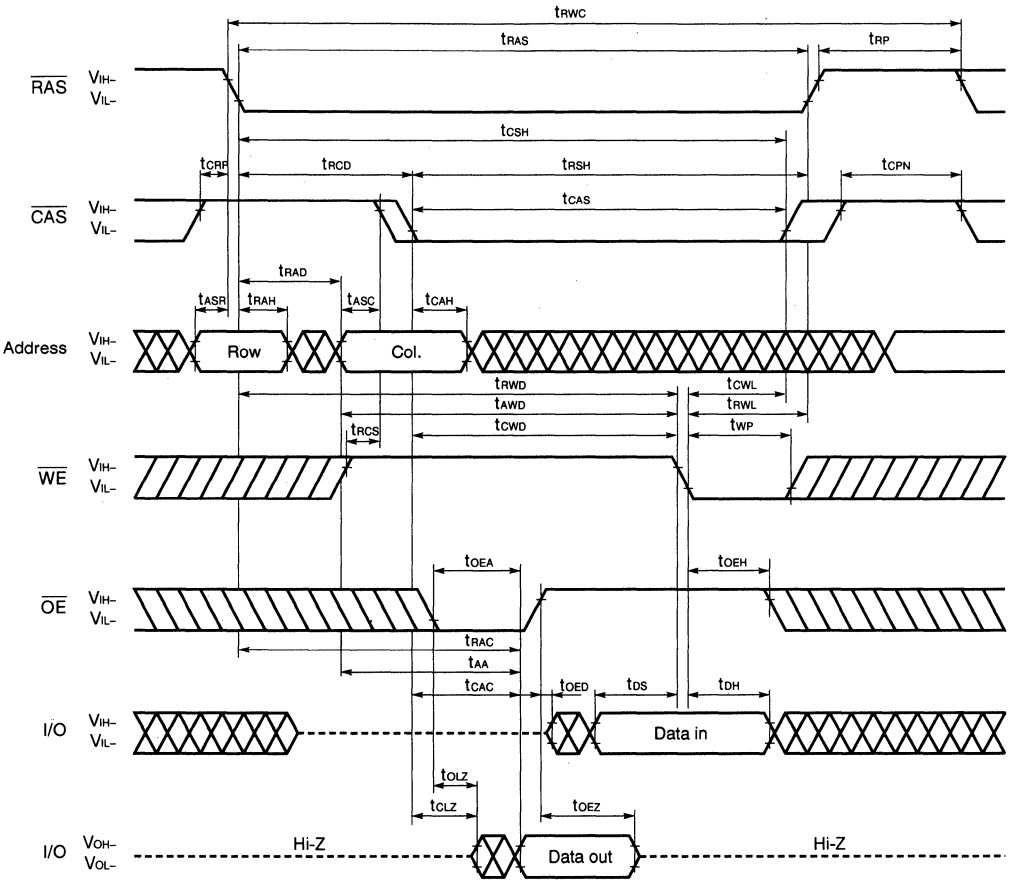


Remark $\overline{OE}$: Don't care

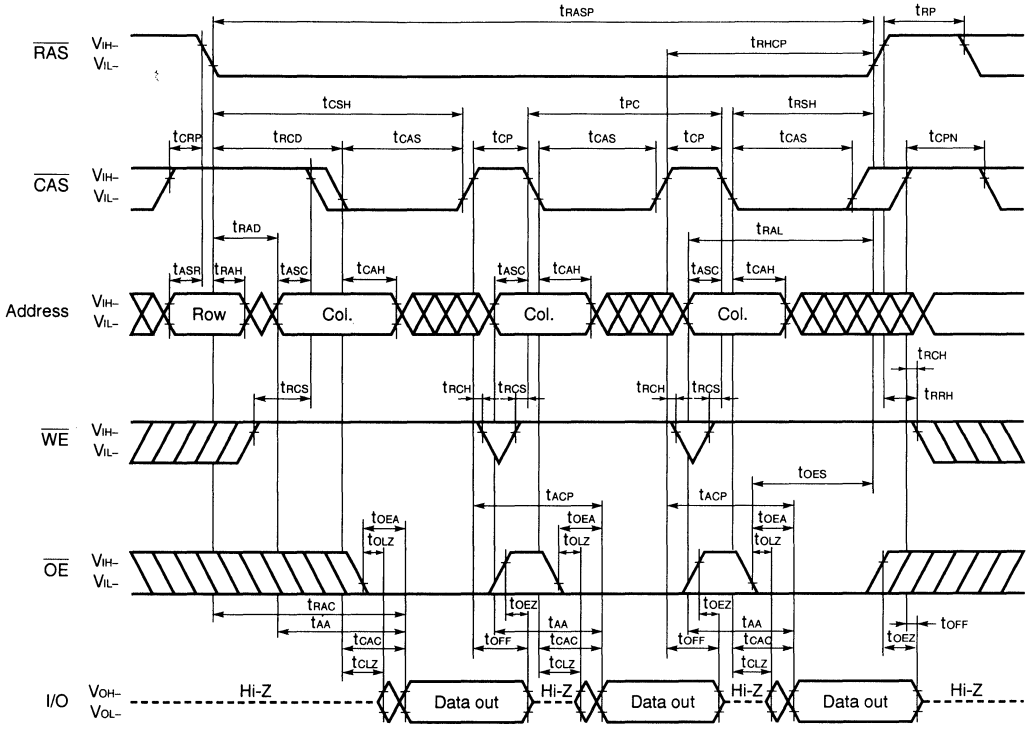
Late Write Cycle



Read Modify Write Cycle

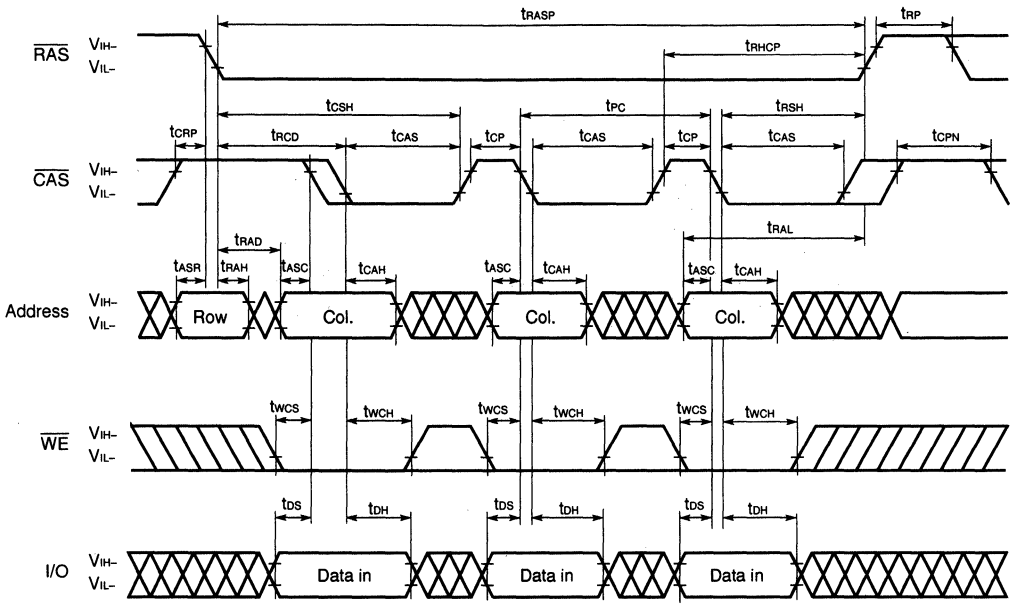


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

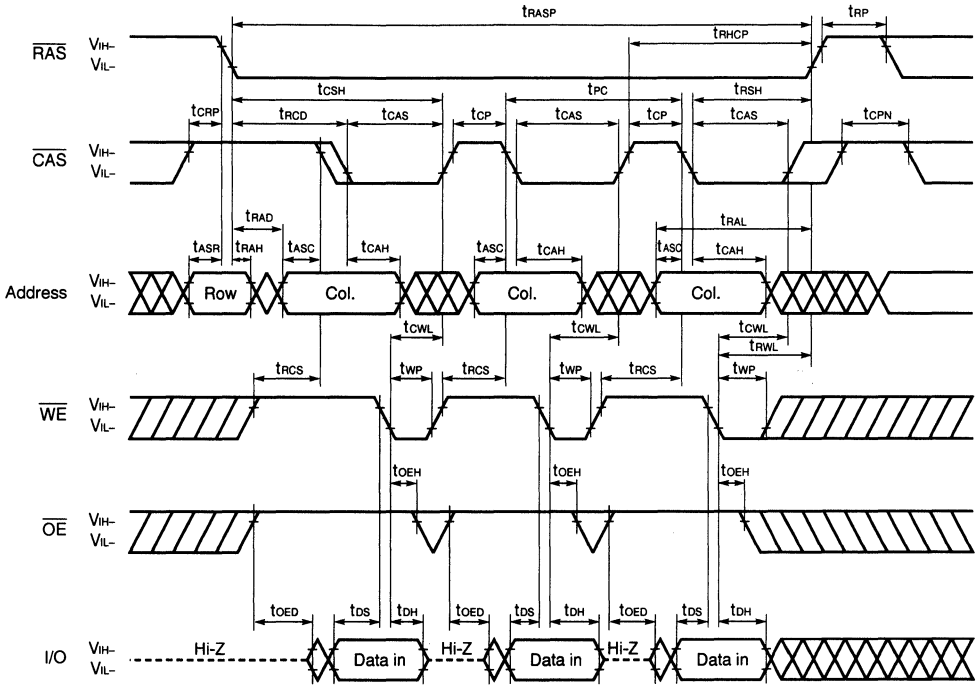
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

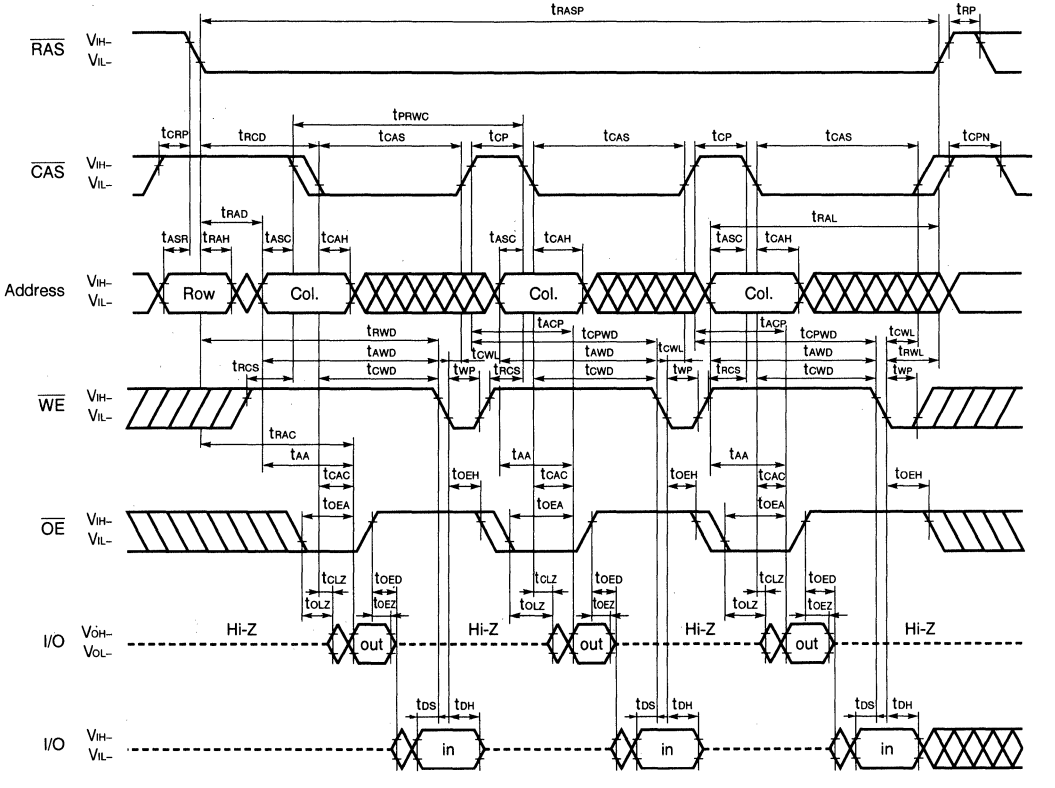
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

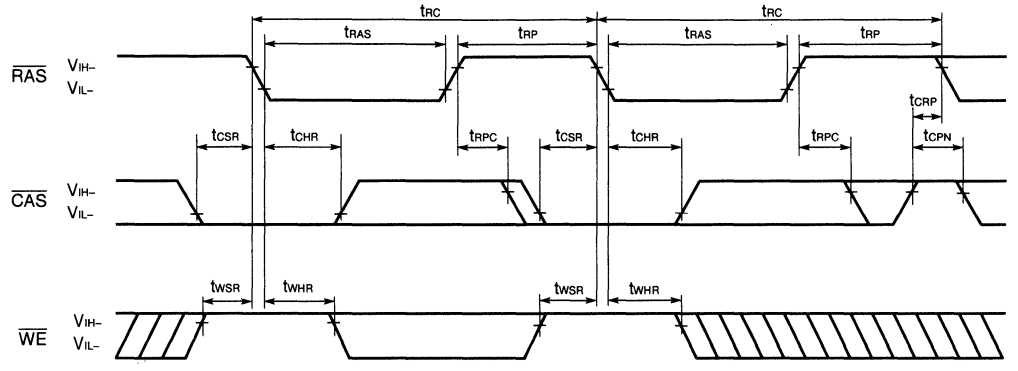
Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

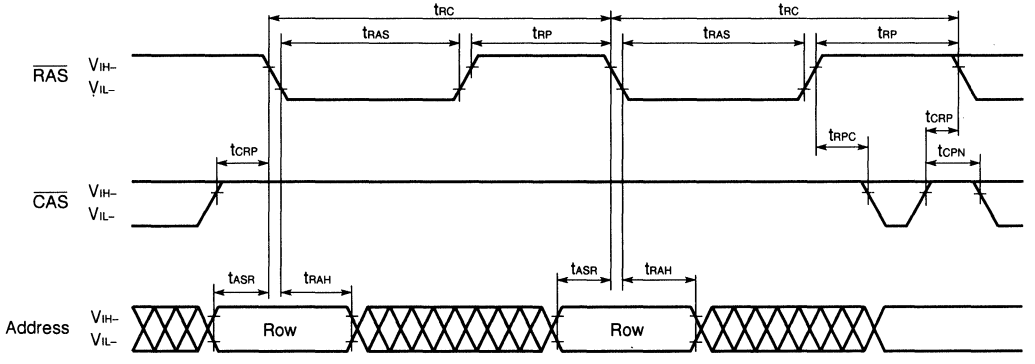
[MEMO]

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



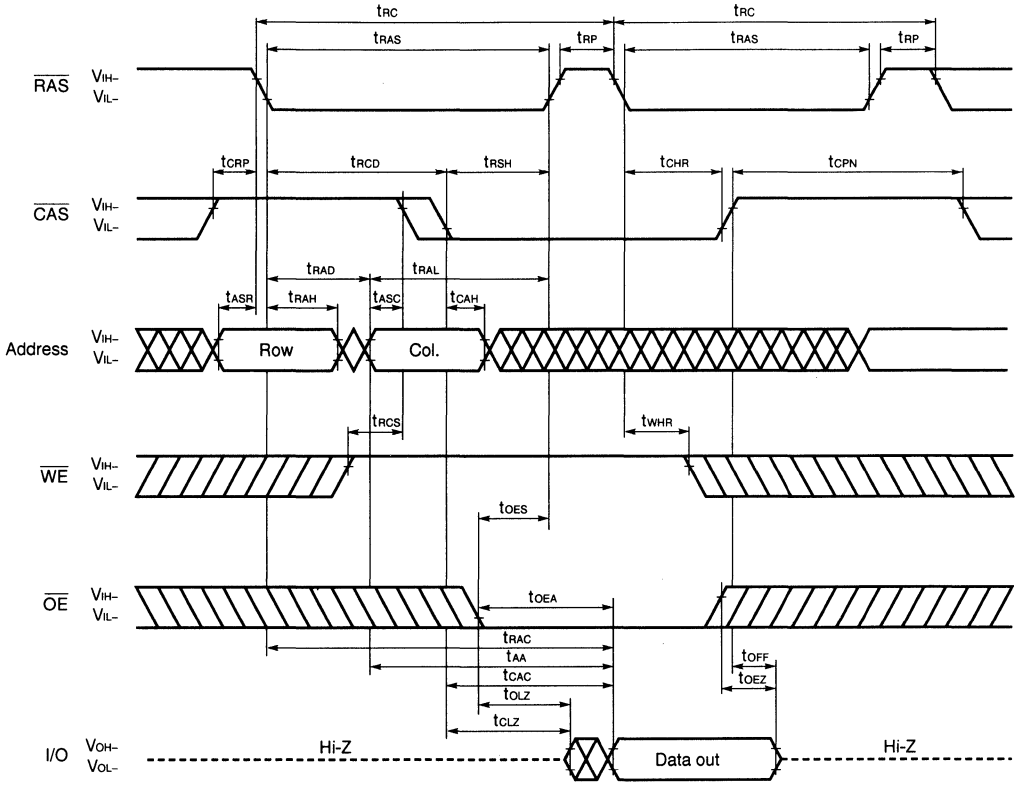
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

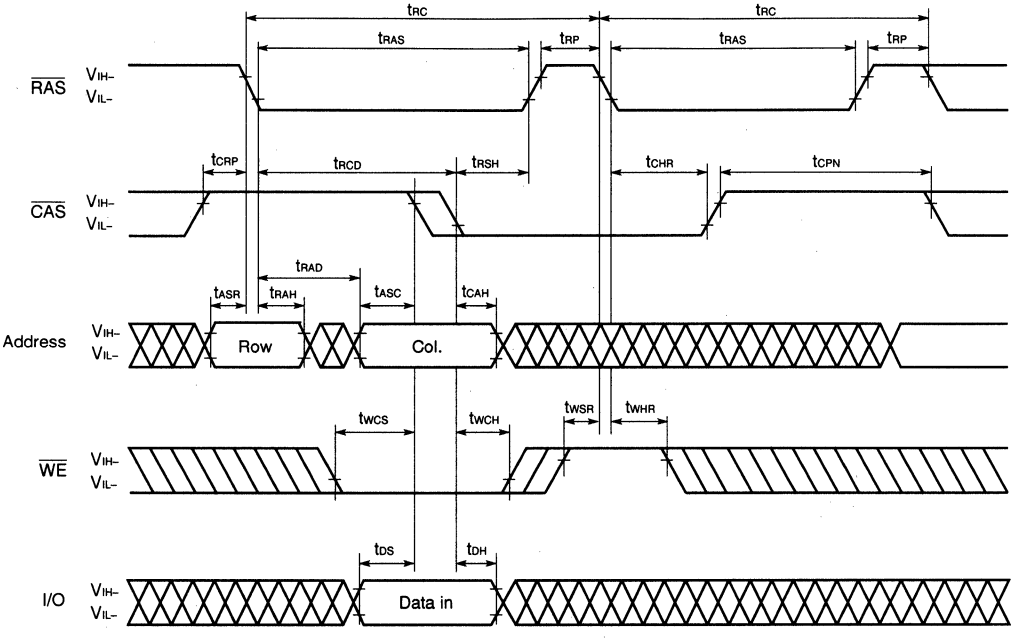


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

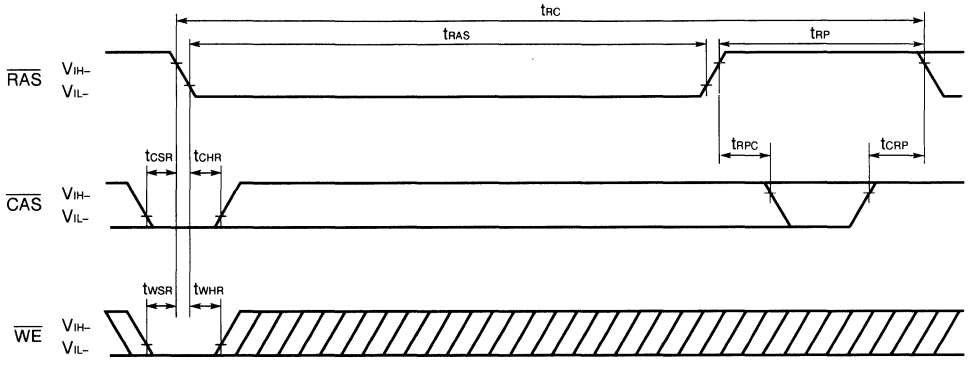


Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Test Mode Set Cycle ($\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)



Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the × 8-bit organization during test mode. Don't care about the input level of the $\overline{CAS}$ input A0.

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 8 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)
Output = "0": Abnormal write

(3) Refresh

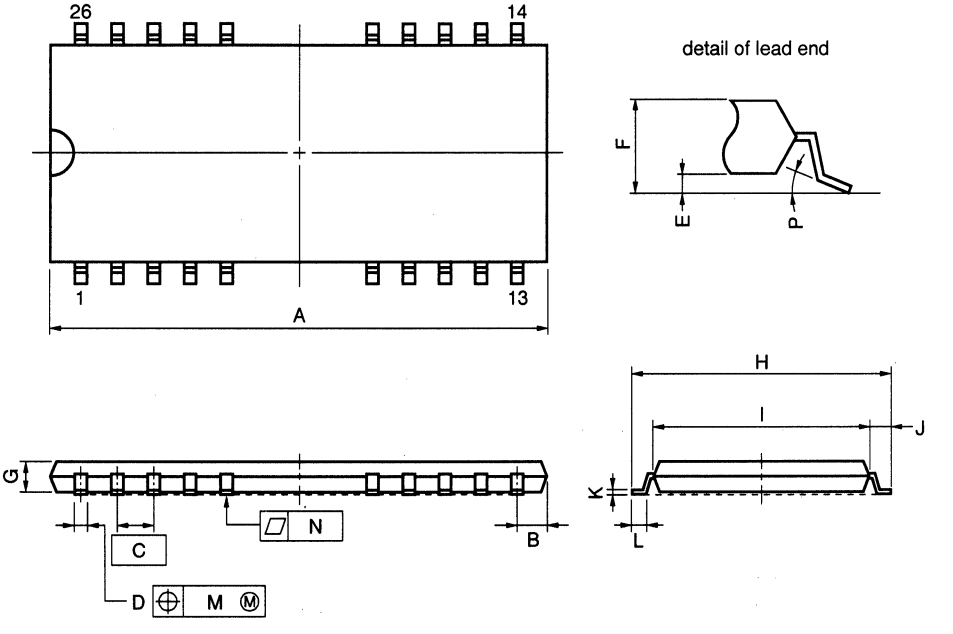
Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

Package Drawings

26 PIN PLASTIC TSOP (II) (300 mil)



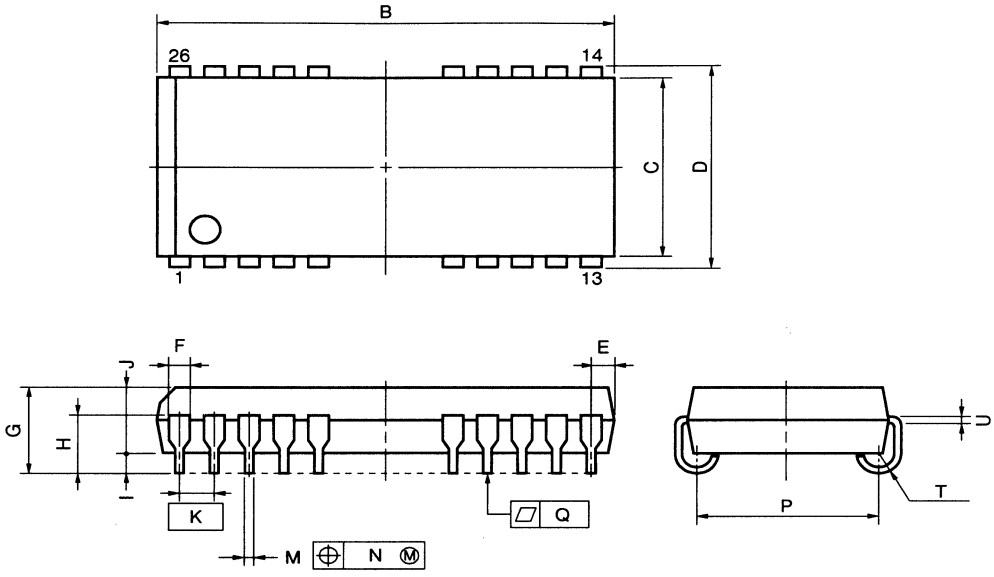
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0	0.039
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S26G3-50-9JD

26 PIN PLASTIC SOJ (300 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.4^{+0.2}_{-0.35}$	$0.685^{+0.008}_{-0.013}$
C	7.57	0.298
D	8.47±0.2	$0.333^{+0.009}_{-0.008}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	6.73±0.20	0.265±0.008
Q	0.15	0.006
T	R 0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P26LA-50A-2

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424400.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD424400GS: 26-pin plastic TSOP (II) (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424400LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]

NEC

MOS INTEGRATED CIRCUIT

μPD42S4800, 424800

4 M-BIT DYNAMIC RAM
512 K-WORD BY 8-BIT, FAST PAGE MODE

Description

The μPD42S4800, 424800 are 524,288 words by 8 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

Besides, the μPD42S4800 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 28-pin plastic TSOP(II) and 28-pin plastic SOJ.

Features

- 524,288 words by 8 bits organization
- Fast page mode
- Fast access and cycle time
- Single +5.0 V ± 10 % power supply

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4800-60, 424800-60	577.5 mW	60 ns	110 ns	40 ns
μPD42S4800-70, 424800-70	550.0 mW	70 ns	130 ns	45 ns
μPD42S4800-80, 424800-80	522.5 mW	80 ns	150 ns	50 ns
μPD42S4800-10, 424800-10	440.0 mW	100 ns	180 ns	60 ns

- The μPD42S4800 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4800	1,024 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.825 mW (CMOS level input)
μPD424800	1,024 cycles/16 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

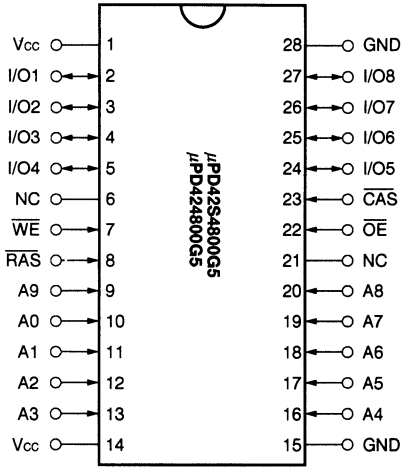
- Multiplexed address inputs ····· Row address: A0-A9, Column address: A0-A8

Ordering Information

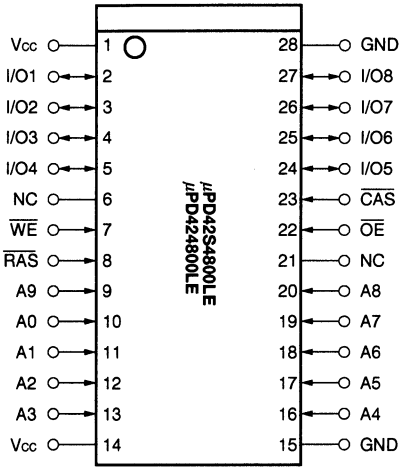
Part number	Access time (MAX.)	Package	Refresh
μPD42S4800G5-60	60 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S4800G5-70	70 ns		
μPD42S4800G5-80	80 ns		
μPD42S4800G5-10	100 ns		
μPD42S4800LE-60	60 ns	28-pin plastic SOJ (400 mil)	
μPD42S4800LE-70	70 ns		
μPD42S4800LE-80	80 ns		
μPD42S4800LE-10	100 ns		
μPD424800G5-60	60 ns	28-pin plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424800G5-70	70 ns		
μPD424800G5-80	80 ns		
μPD424800G5-10	100 ns		
μPD424800LE-60	60 ns	28-pin plastic SOJ (400 mil)	
μPD424800LE-70	70 ns		
μPD424800LE-80	80 ns		
μPD424800LE-10	100 ns		

Pin Configurations (Marking Side)

28-pin Plastic TSOP (II) (400 mil)

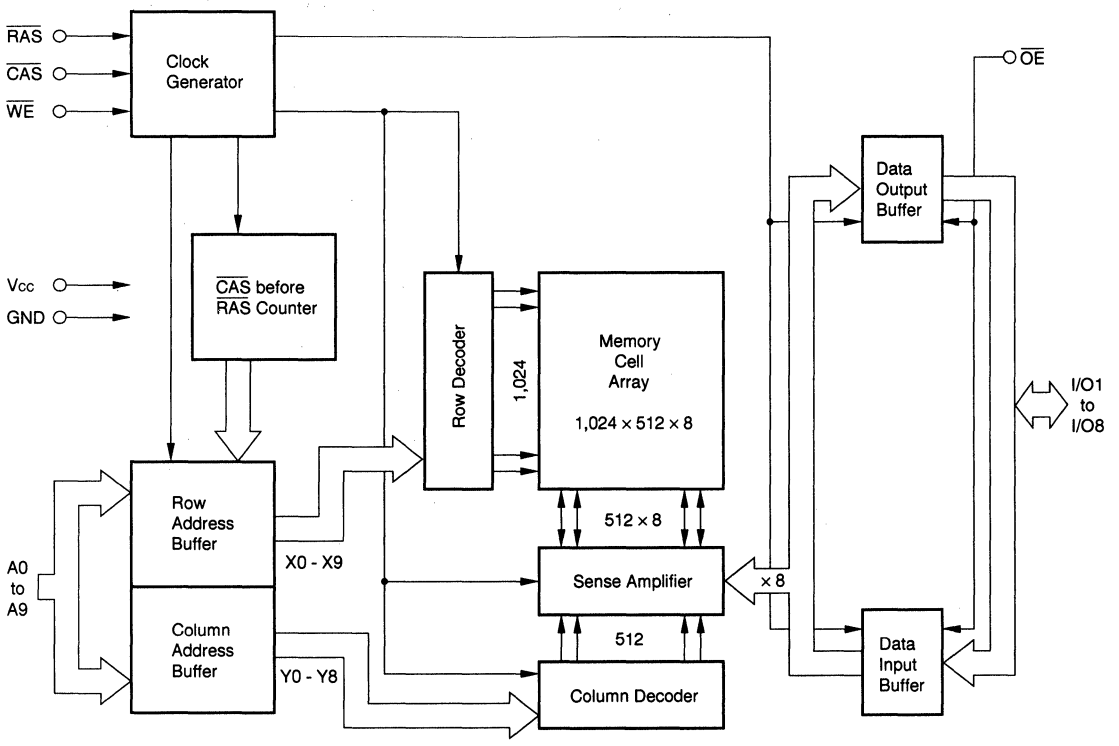


28-pin Plastic SOJ (400 mil)



A0 to A9	:	Address Inputs
I/O1 to I/O8	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4800, 424800 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O8.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address inputs)	Input	Address bus. Input total 19-bit of address signal, upper 10-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 524,288-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} + 1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		105	mA	1, 2, 3
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		95		
				t_{RAC} = 100 ns		80		
Standby current	μPD42S4800	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2	mA	
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			0.15		
	μPD424800		$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, I_O = 0 mA			2		
			$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, I_O = 0 mA			1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		105	mA	1, 2, 3, 4
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		95		
				t_{RAC} = 100 ns		80		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		80	mA	1, 2, 5
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
				t_{RAC} = 100 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		105	mA	1, 2
				t_{RAC} = 70 ns		100		
				t_{RAC} = 80 ns		95		
				t_{RAC} = 100 ns		80		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S4800)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : t_{RC} = 125.0 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V	$t_{RAS} \leq$ 200 ns		200	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq$ 1 μs		300	μA	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S4800)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH(MAX.)}$ 0 V ≤ $V_{IL} \leq$ 0.2 V I_O = 0 mA			150	μA	2
Input leakage current		$I_{I\ (L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		−10	+10	μA	
Output leakage current		$I_{O\ (L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage		V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = +4.2 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

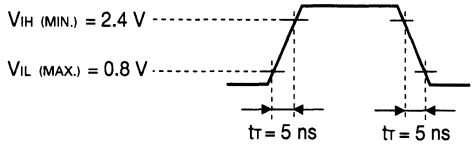
2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

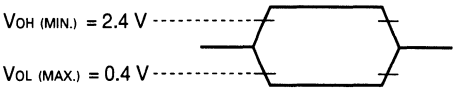
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

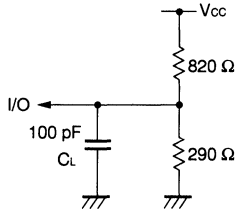
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time		tRC	110	–	130	–	150	–	180	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	60	–	70	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	80	10,000	100	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	20	–	20	–	25	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	50	25	60	25	75	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	17	40	17	50	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	5	–	5	–	5	–	5	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	12	–	12	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	15	–	20	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	15	–	15	–	15	–	20	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	3	50	3	50	ns	
Refresh time	μPD42S4800	tREF	–	128	–	128	–	128	–	128	ms	4
	μPD424800		–	16	–	16	–	16	–	16	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

3. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S4800.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	–	100	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	–	20	–	25	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	–	50	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	–	20	–	25	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	50	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.

3. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	15	–	20	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	10	–	15	–	20	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	20	–	20	–	25	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	15	–	20	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	15	–	15	–	15	–	20	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	150	–	175	–	200	–	240	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	90	–	105	–	130	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	–	40	–	45	–	55	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	55	–	65	–	80	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	60	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	–	55	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	100	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	55	–	ns	
Read modify write cycle time	t_{PRWC}	80	–	85	–	95	–	115	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55	–	60	–	70	–	85	–	ns	1

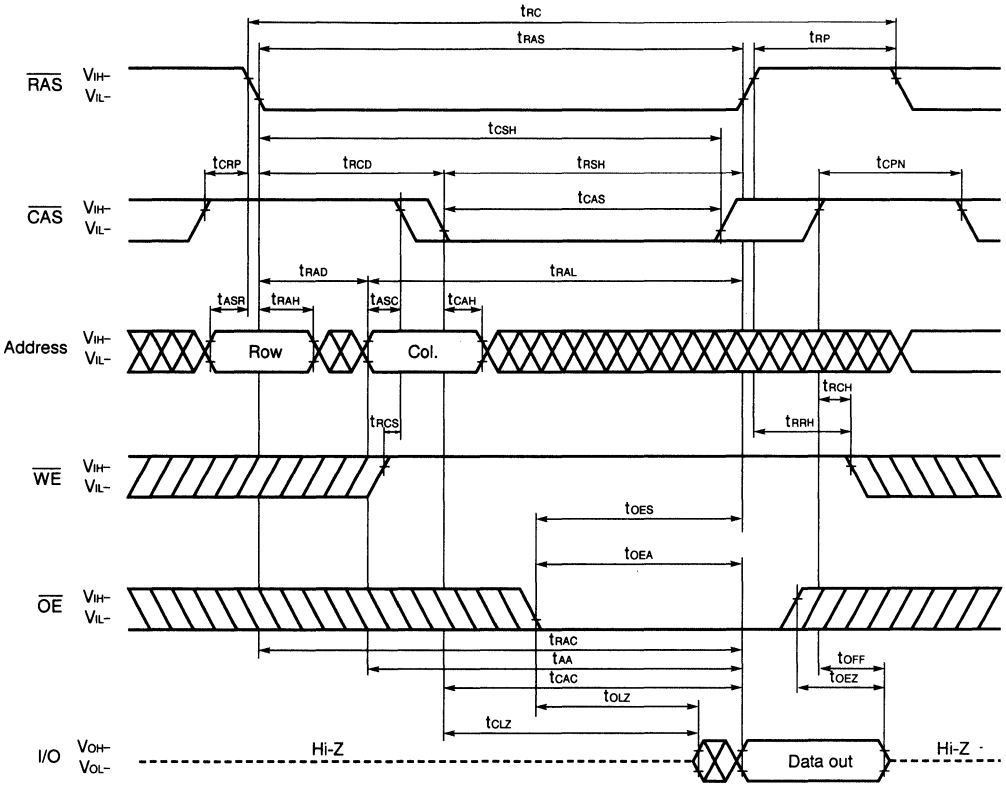
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

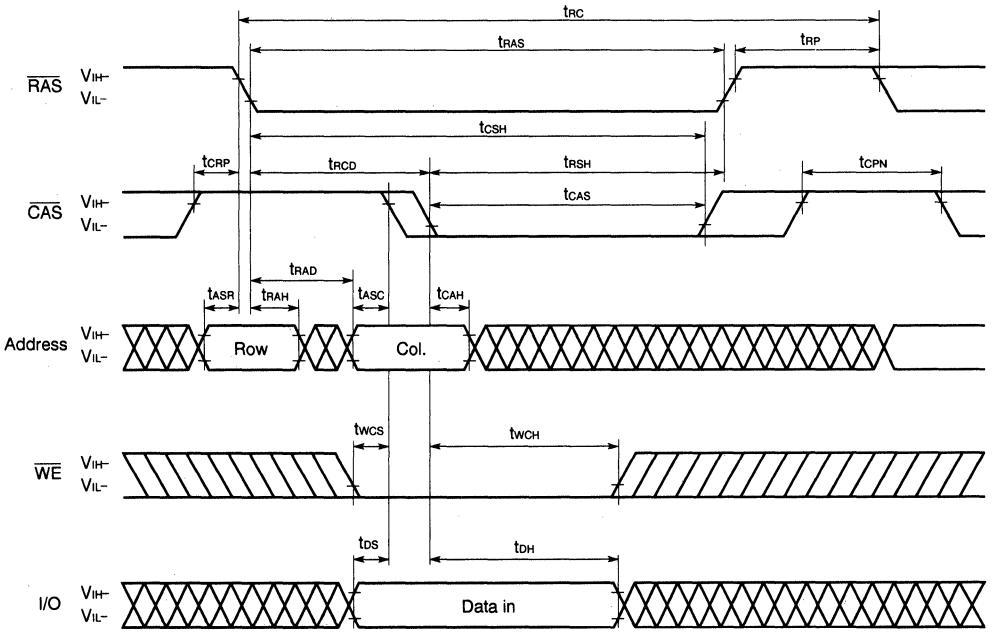
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	150	–	180	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ hold time	t_{WHR}	10	–	15	–	15	–	20	–	ns	

Note 1. This specification is applied only to the μPD42S4800.

Read Cycle

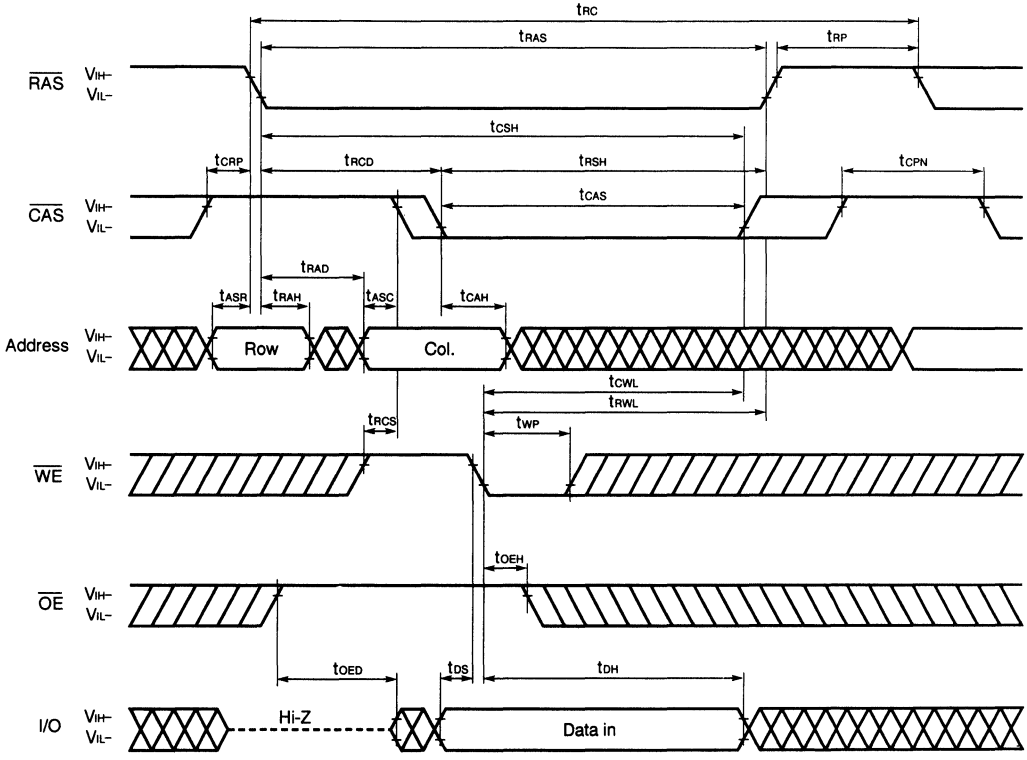

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tCAC
tOFF
tOEZ
tOLZ
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

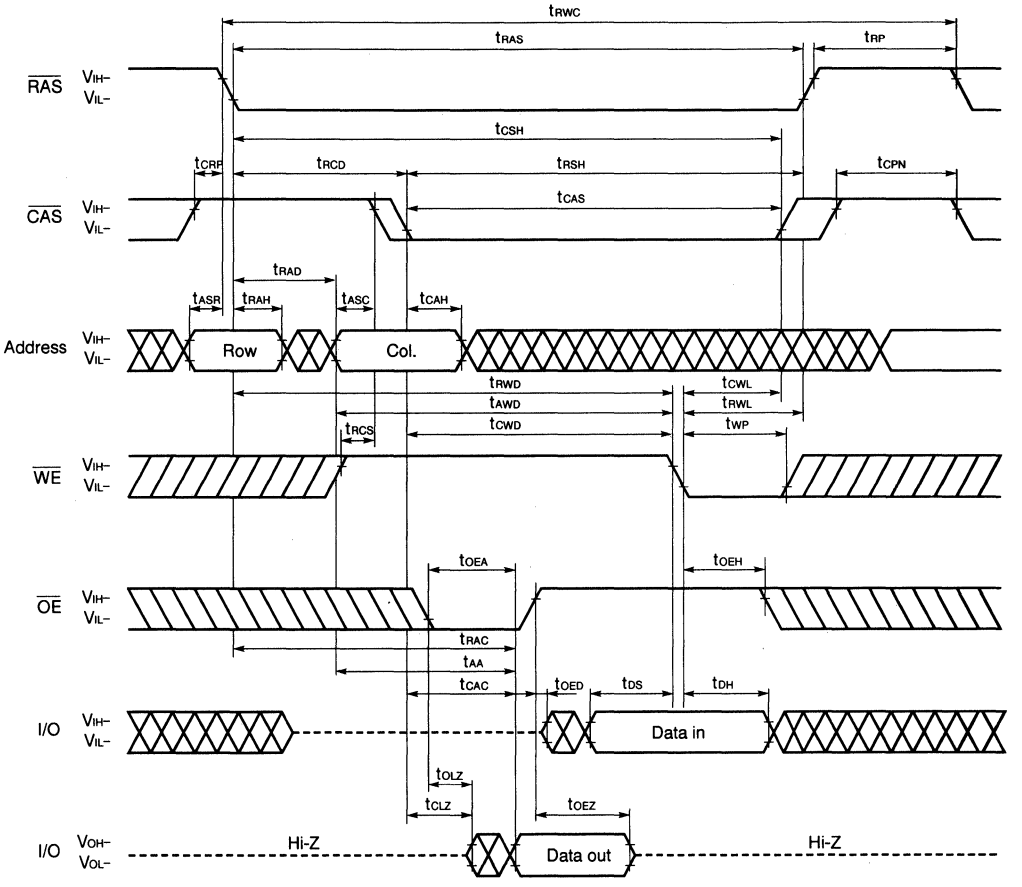


Remark $\overline{OE}$: Don't care

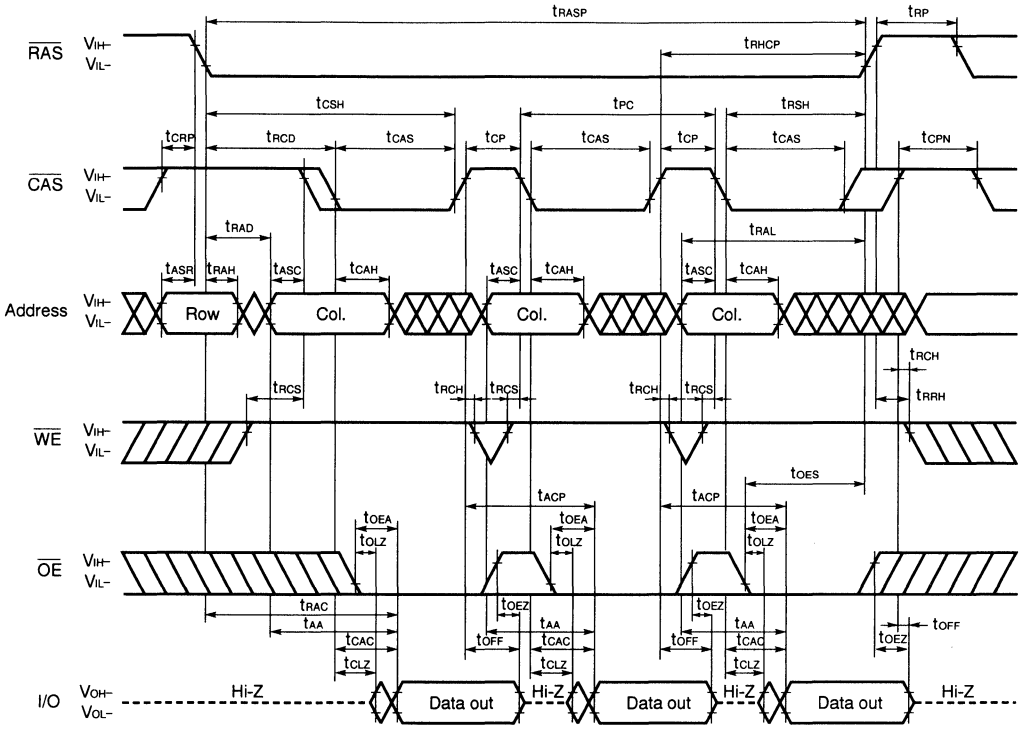
Late Write Cycle



Read Modify Write Cycle

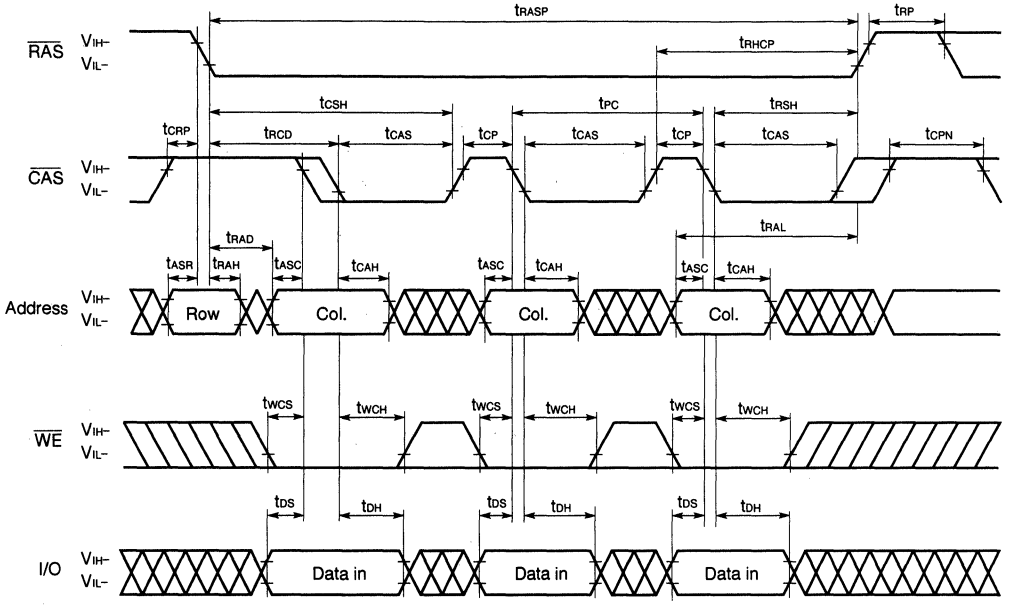


Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

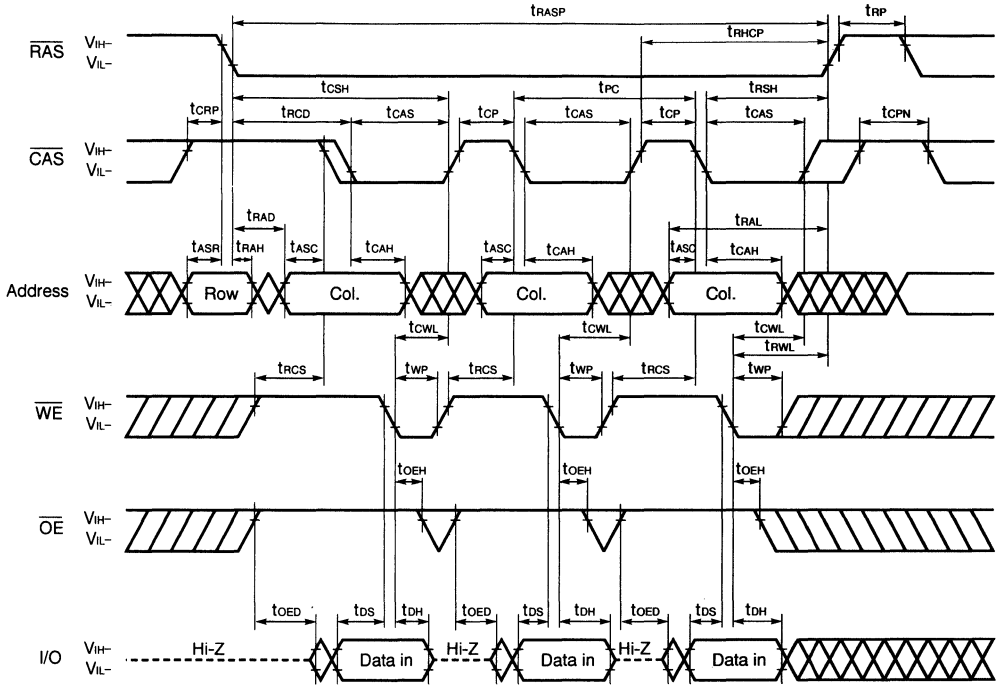
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

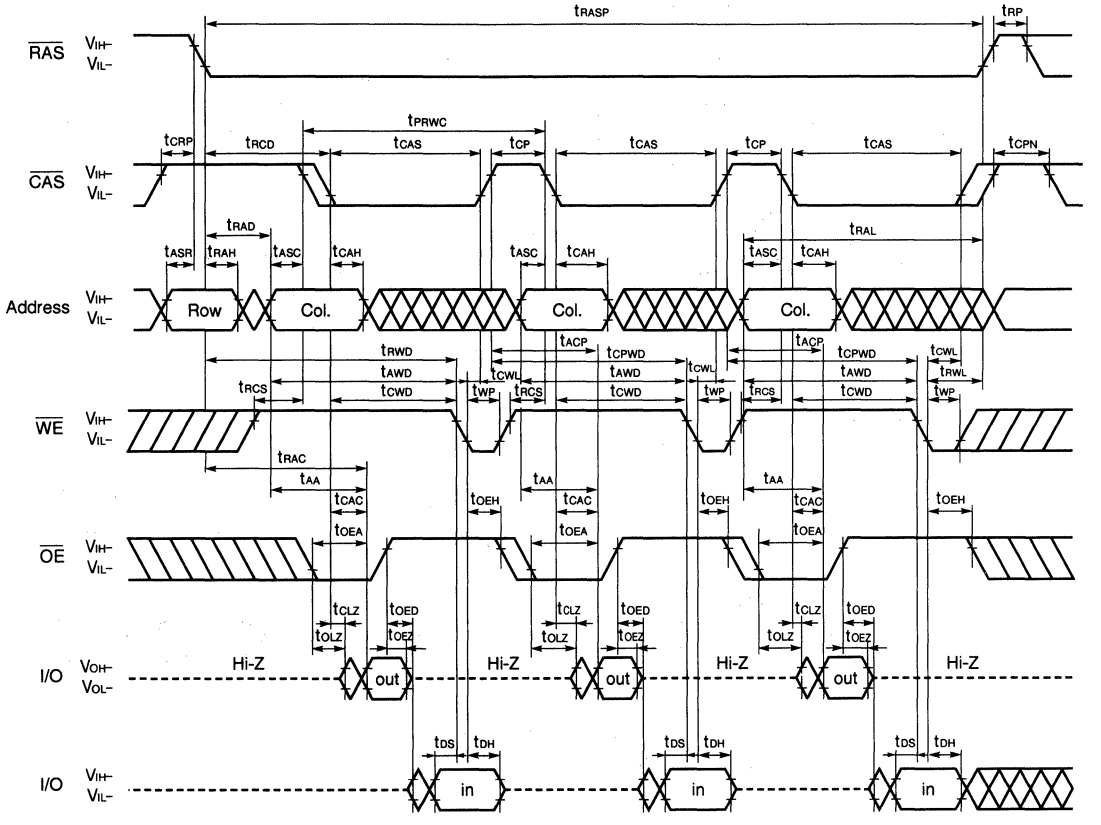
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Late Write Cycle



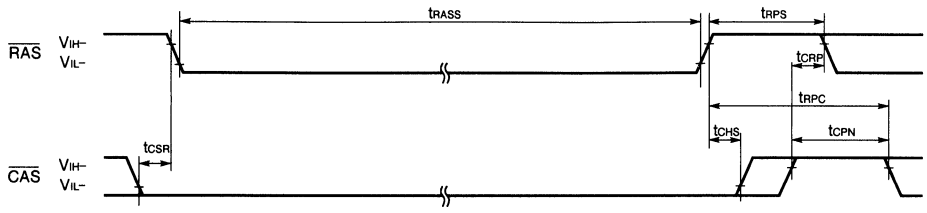
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S4800)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

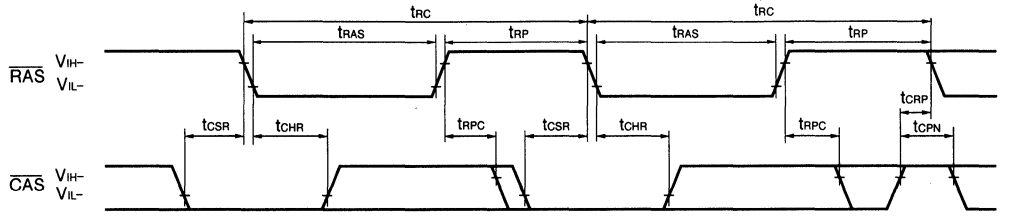
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (1,024/128 ms) should be met.

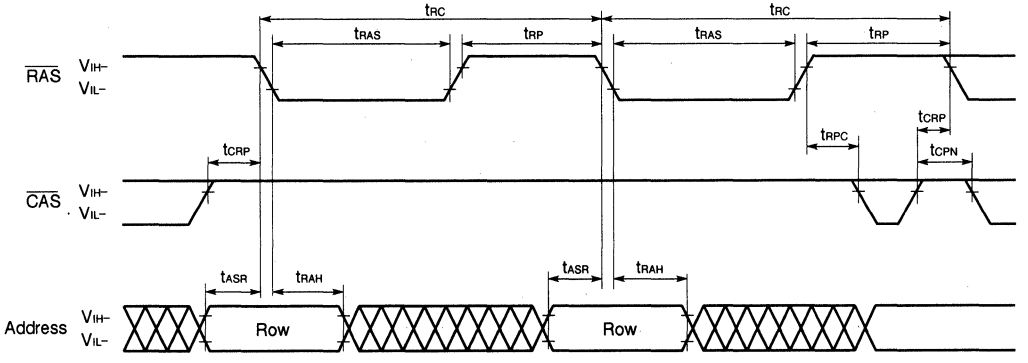
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



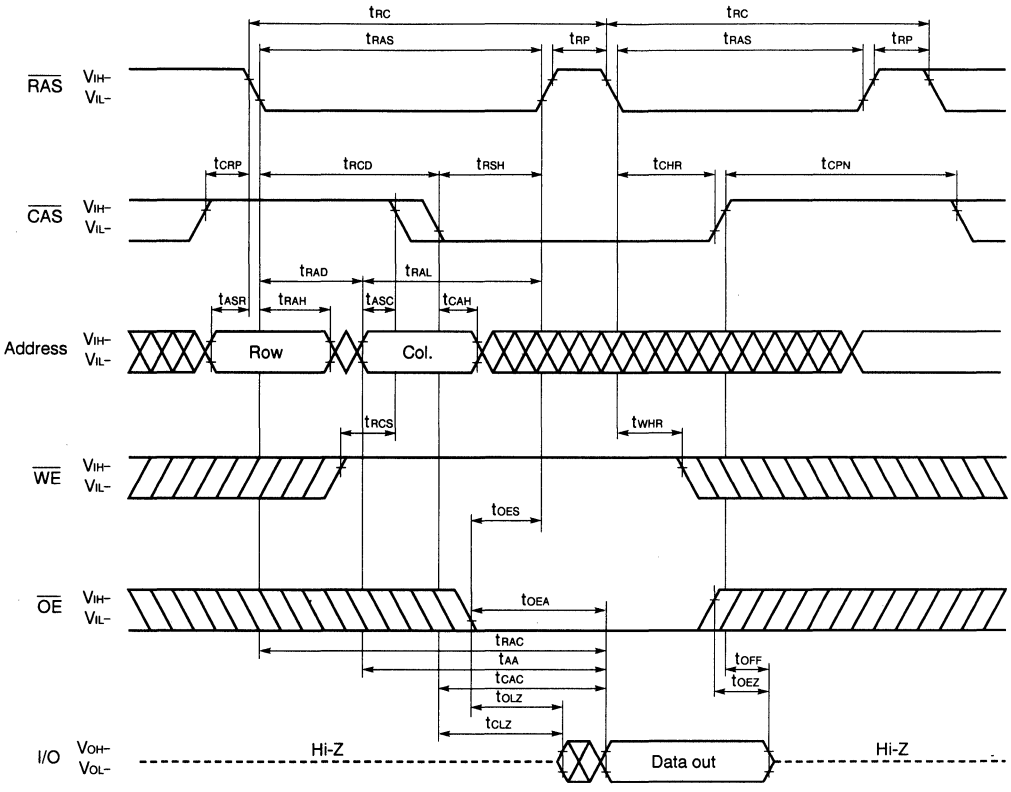
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

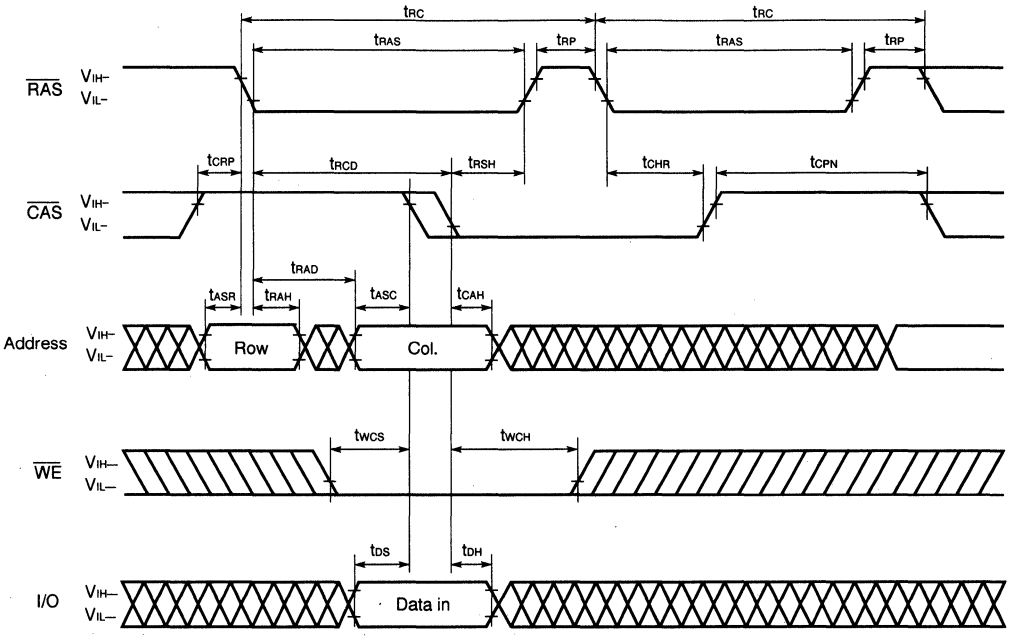


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



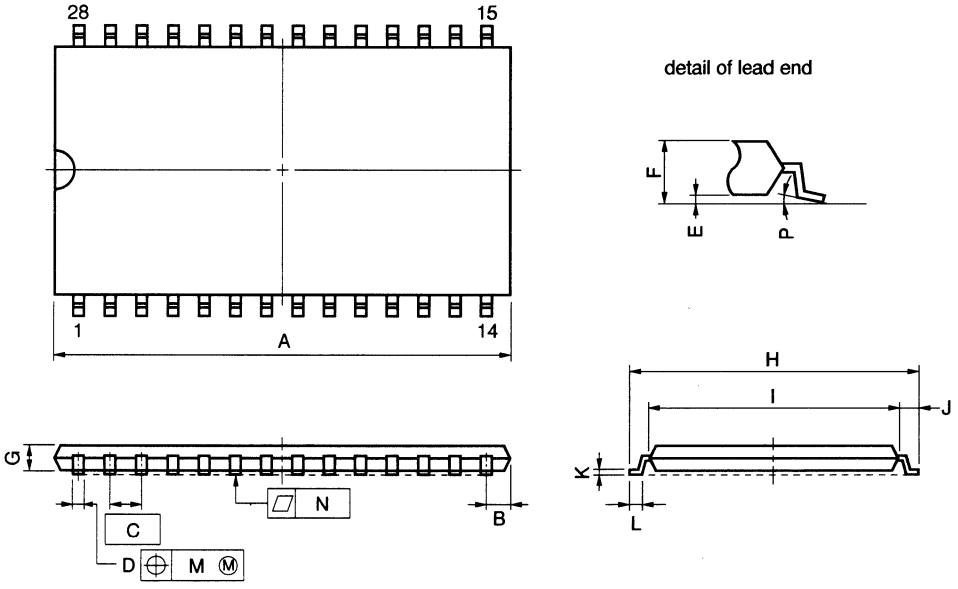
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

28 PIN PLASTIC TSOP(II) (400 mil)



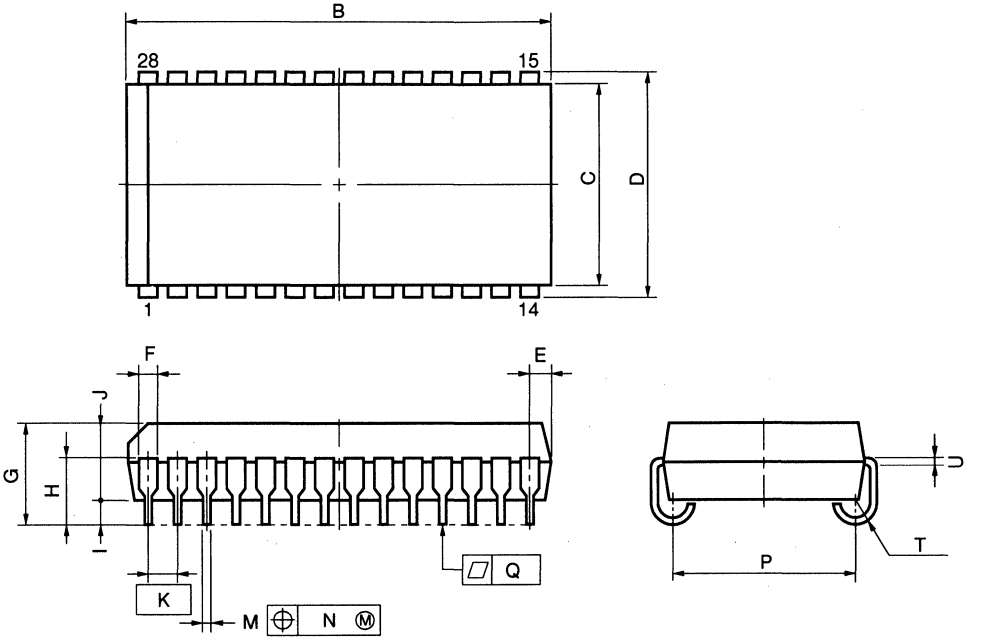
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S28G5-50-7JD5

28 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	11.18±0.2	$0.440^{+0.008}_{-0.007}$
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	3.5±0.2	$0.138^{+0.008}_{-0.007}$
H	2.4±0.2	$0.094^{+0.008}_{-0.007}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	$0.370^{+0.008}_{-0.007}$
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P28LA-400A-2

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S4800, 424800.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4800G5, 424800G5: 28-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4800LE, 424800LE: 28-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit :7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NEC

MOS INTEGRATED CIRCUIT

μPD42S4260, 424260

4 M-BIT DYNAMIC RAM
256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S4260, 424260 are 262,144 words by 16 bits dynamic CMOS RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

Besides, the μPD42S4260 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 44-pin plastic TSOP (II) and 40-pin plastic SOJ.

Features

- 262,144 words by 16 bits organization
- Single +5.0 V ±10 % power supply
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4260-60, 424260-60	880.0 mW	60 ns	110 ns	40 ns
μPD42S4260-70, 424260-70	880.0 mW	70 ns	130 ns	45 ns
μPD42S4260-80, 424260-80	797.5 mW	80 ns	150 ns	50 ns

- The μPD42S4260 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S4260	512 cycles / 128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	0.825 mW (CMOS level input)
μPD424260	512 cycles / 8 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)

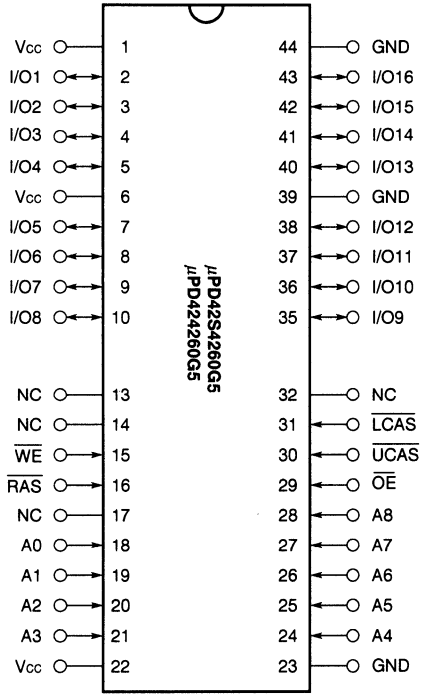
- Multiplexed address inputs ... Row address: A0 to A8, Column address: A0 to A8

Ordering Information

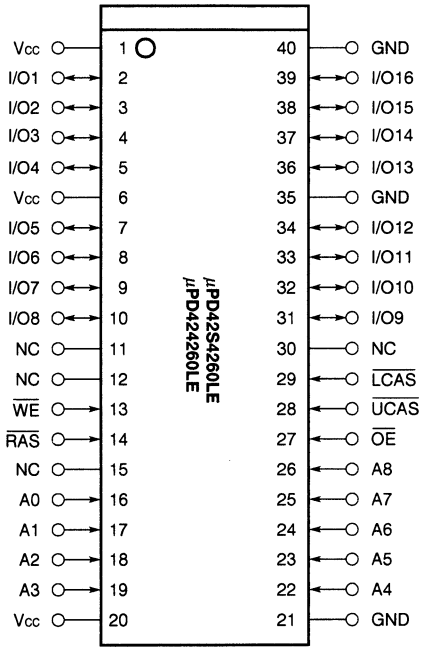
Part number	Access time (MAX.)	Package	Refresh
μPD42S4260G5-60	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S4260G5-70	70 ns		
μPD42S4260G5-80	80 ns		
μPD42S4260LE-60	60 ns	40-pin Plastic SOJ (400 mil)	
μPD42S4260LE-70	70 ns		
μPD42S4260LE-80	80 ns		
μPD424260G5-60	60 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424260G5-70	70 ns		
μPD424260G5-80	80 ns		
μPD424260LE-60	60 ns	40-pin Plastic SOJ (400 mil)	
μPD424260LE-70	70 ns		
μPD424260LE-80	80 ns		

Pin Configurations (Marking Side)

44-pin Plastic TSOP (II)
(400 mil)

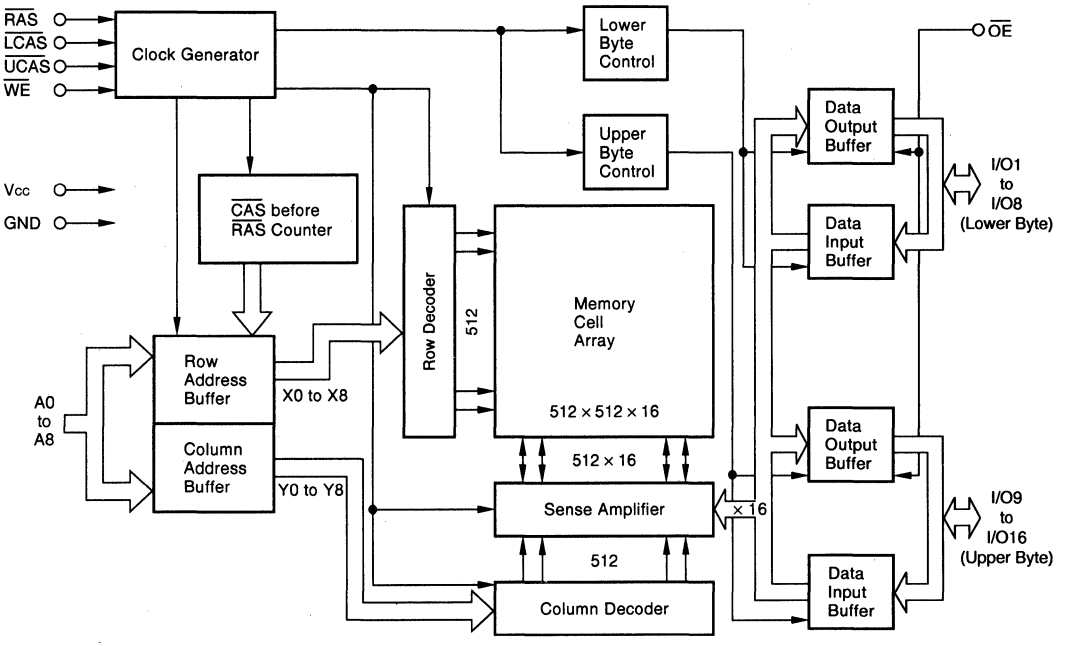


40-pin Plastic SOJ
(400 mil)



A0 to A8	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4260, 424260 have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address (A0 to A8) and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address (A0 to A8). It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address (A0 to A8) and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address input)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word (16-bit) is selected from 262,144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating RAS, CAS and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/ output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC\,(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test condition		MIN.	TYP.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			160	mA	1, 2, 3
				t_{RAC} = 70 ns			160		
				t_{RAC} = 80 ns			145		
Standby current	μPD42S4260	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA				2	mA	
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA				0.15		
	μPD424260		$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$, I_O = 0 mA				2		
			$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA				1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			160	mA	1, 2, 3, 4
				t_{RAC} = 70 ns			160		
				t_{RAC} = 80 ns			145		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			140	mA	1, 2, 5
				t_{RAC} = 70 ns			140		
				t_{RAC} = 80 ns			130		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns			160	mA	1, 2
				t_{RAC} = 70 ns			160		
				t_{RAC} = 80 ns			145		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 cycles / 128 ms, only for the μPD42S4260)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} = 250.0 μs $\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH(MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V	t_{RAS} ≤ 200 ns			200	μA	1, 2
			Standby: $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Address: V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	t_{RAS} ≤ 1 μs			300	μA	1, 2
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μPD42S4260)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms V_{CC} – 0.2 V ≤ V_{IH} ≤ $V_{IH\ (MAX.)}$ 0 V ≤ V_{IL} ≤ 0.2 V I_O = 0 mA				150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10		+10	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10		+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4			V	
Low level output voltage		V_{OL}	I_O = +2.1 mA				0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≤ $V_{IL\ (MAX.)}$ and $\overline{CAS}$ ≥ $V_{IH\ (MIN.)}$.

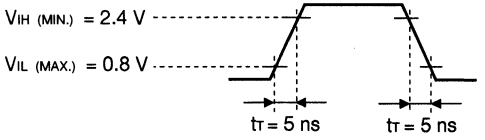
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

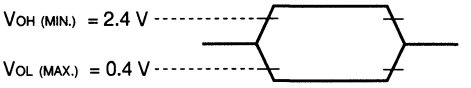
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

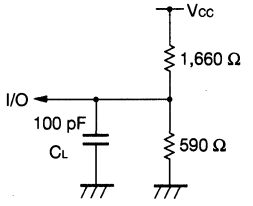
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 60 ns		tRAC = 70 ns		tRAC = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write cycle time		tRC	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time		tRP	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time		tCPN	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width		tRAS	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width		tCAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ hold time		tRSH	15	–	20	–	20	–	ns	
$\overline{CAS}$ hold time		tCSH	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time		tRCD	20	45	20	50	20	60	ns	2
$\overline{RAS}$ to column address delay time		tRAD	15	30	15	35	15	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time		tCRP	10	–	10	–	10	–	ns	3
Row address setup time		tASR	0	–	0	–	0	–	ns	
Row address hold time		tRAH	10	–	10	–	10	–	ns	
Column address setup time		tASC	0	–	0	–	0	–	ns	
Column address hold time		tCAH	15	–	15	–	15	–	ns	
$\overline{OE}$ lead time referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to data setup time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data setup time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to data delay time		tOED	15	–	15	–	20	–	ns	
Masked byte write hold time referenced to $\overline{RAS}$		tMRH	0	–	0	–	0	–	ns	
Transition time (rise and fall)		tT	3	50	3	50	3	50	ns	
Refresh time	μPD42S4260	tREF	–	128	–	128	–	128	ms	4
	μPD424260		–	8	–	8	–	8	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS\ (MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

4. This specification is applied only to the μPD42S4260.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	20	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	ns	1
Access time from $\overline{OE}$	t_{OEA}	–	15	–	20	–	20	ns	
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	15	0	15	0	20	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	15	–	15	–	15	–	ns	1
$\overline{WE}$ pulse width	t_{WP}	10	–	15	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t_{RWL}	15	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t_{CWL}	15	–	15	–	20	–	ns	
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	3

Notes 1. $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t_{RWC}	150	–	175	–	200	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	90	–	105	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	–	40	–	45	–	ns	1
Column address to $\overline{WE}$ delay time	t_{AWD}	50	–	55	–	65	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	
Read modify write cycle time	t_{PRWC}	80	–	85	–	100	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}	55	–	60	–	70	–	ns	1

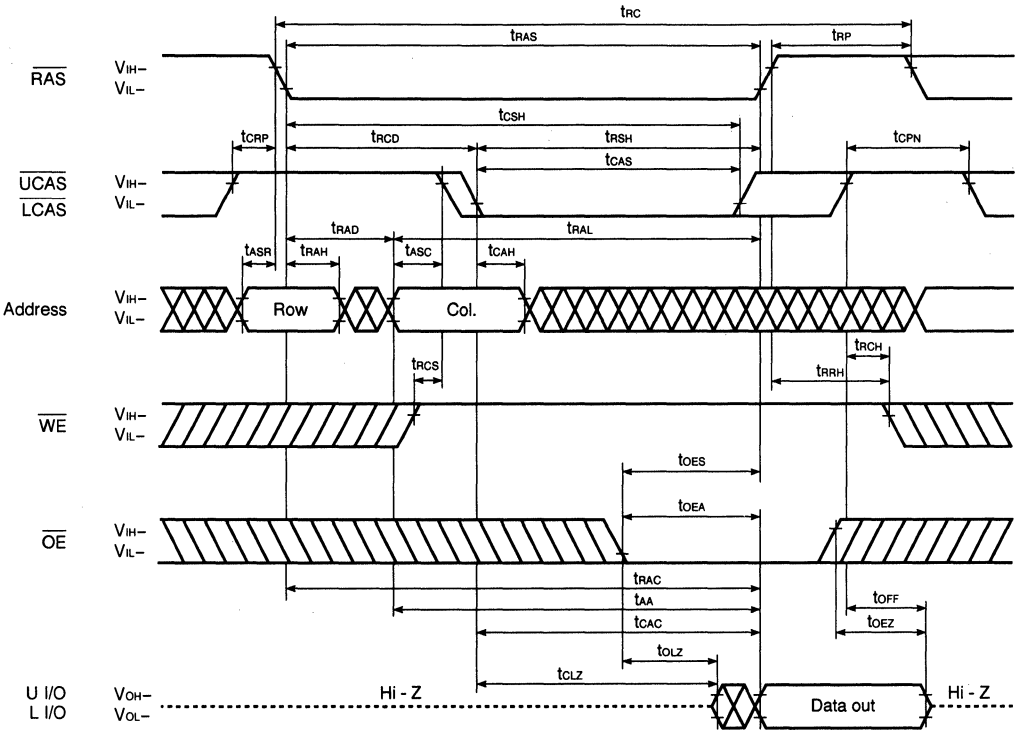
Note 1. If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

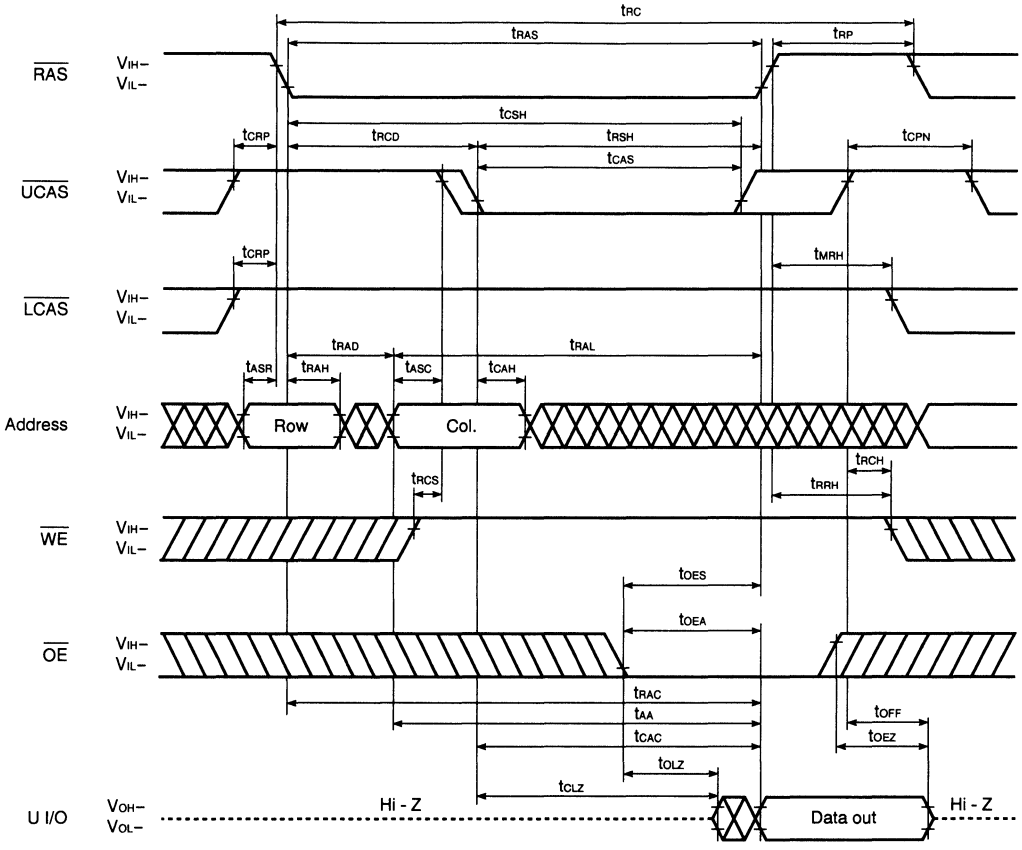
Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	15	–	15	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh cycle)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh cycle)	t_{RPS}	110	–	130	–	150	–	ns	1
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh cycle)	t_{CHS}	–50	–	–50	–	–50	–	ns	1
$\overline{WE}$ hold time (hidden refresh cycle)	t_{WHR}	10	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S4260.

Read Cycle

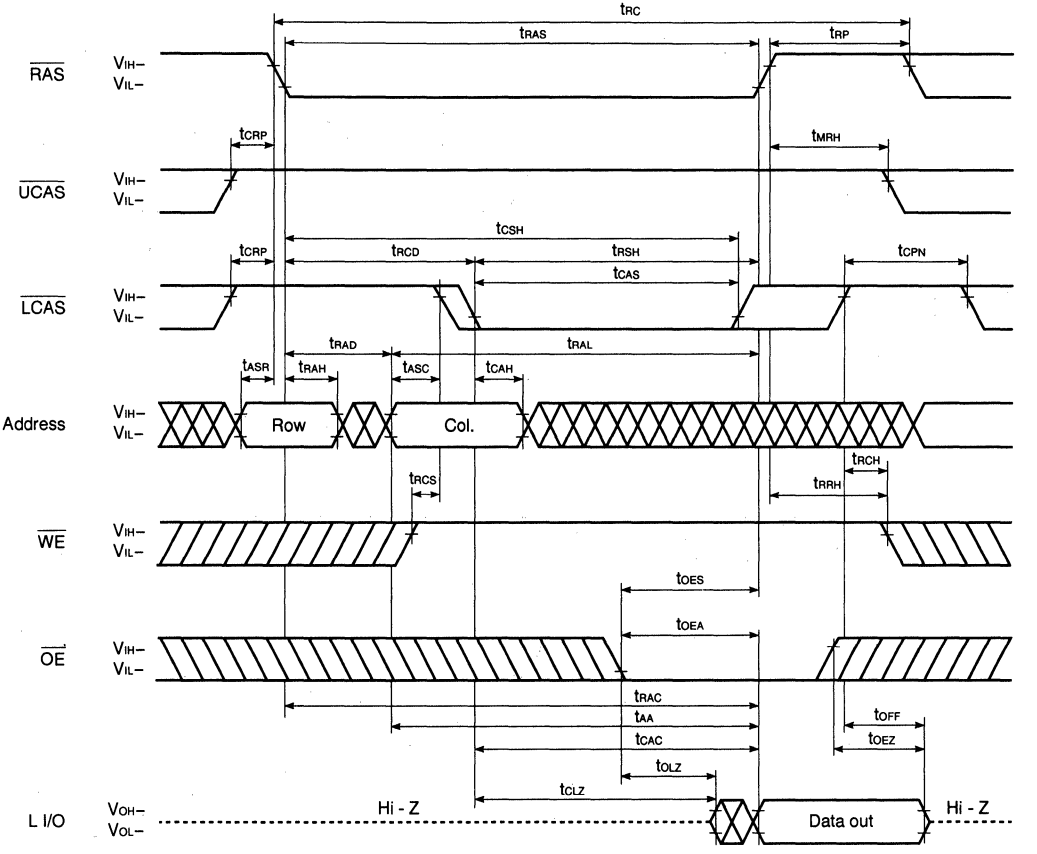

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tOFF
tOEZ
tCAC
tOLZ
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

Upper Byte Read Cycle



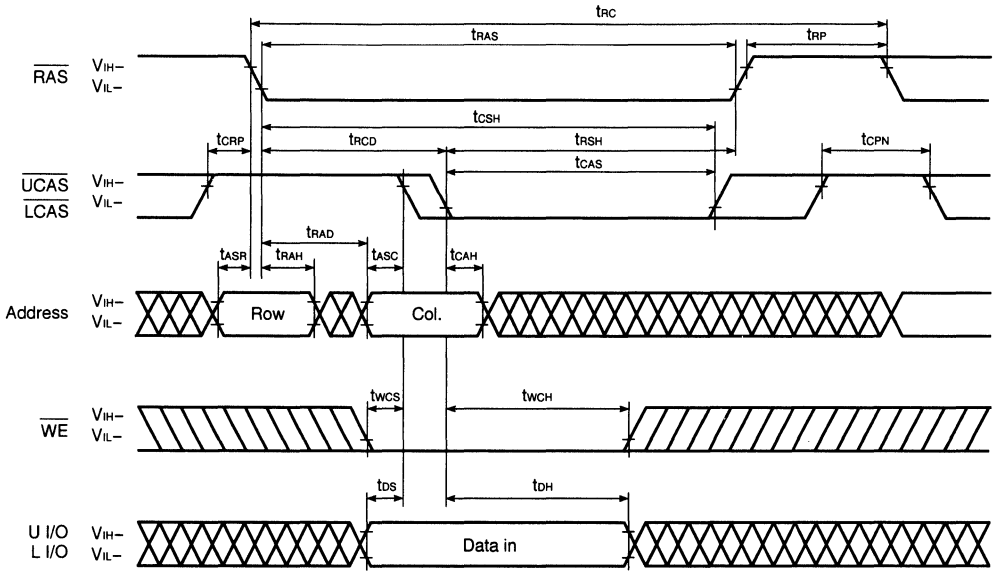
Remark L I/O: Hi-Z

Lower Byte Read Cycle



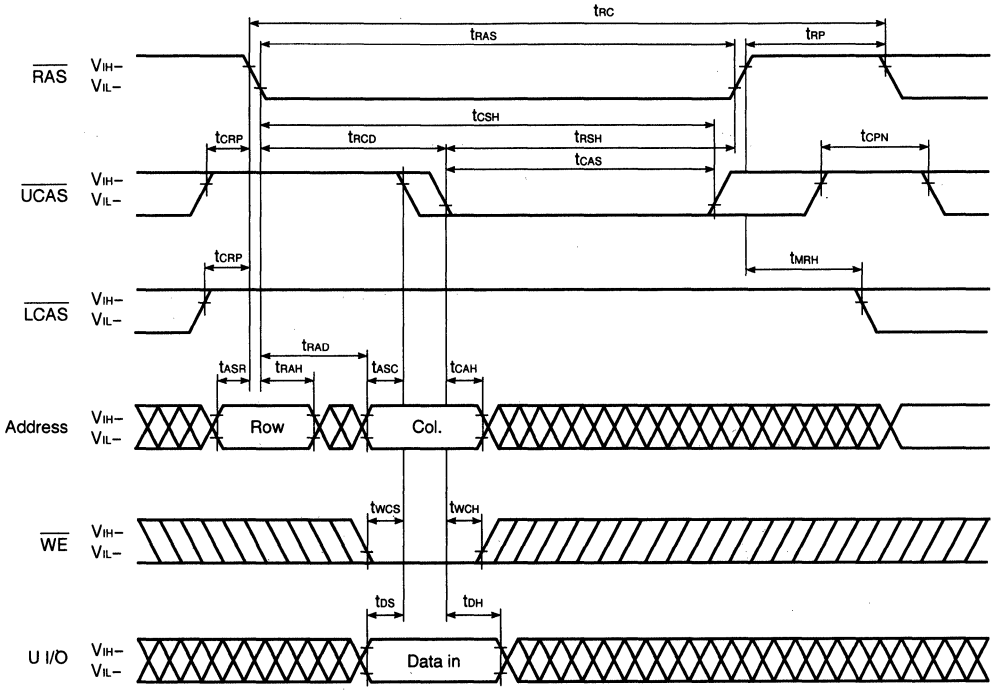
Remark U I/O: Hi-Z

Early Write Cycle



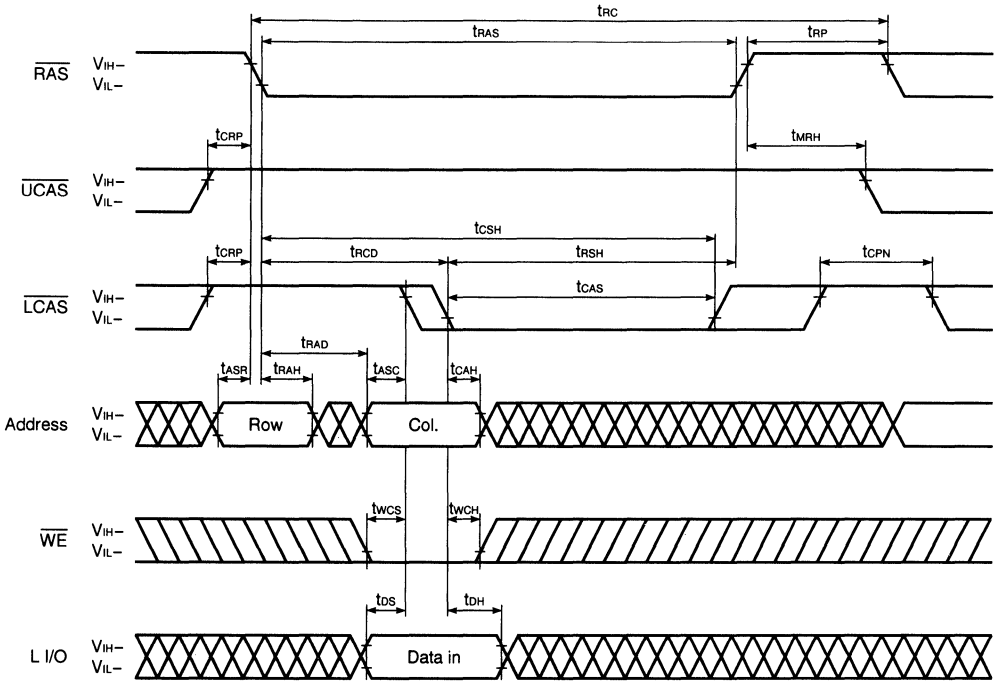
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



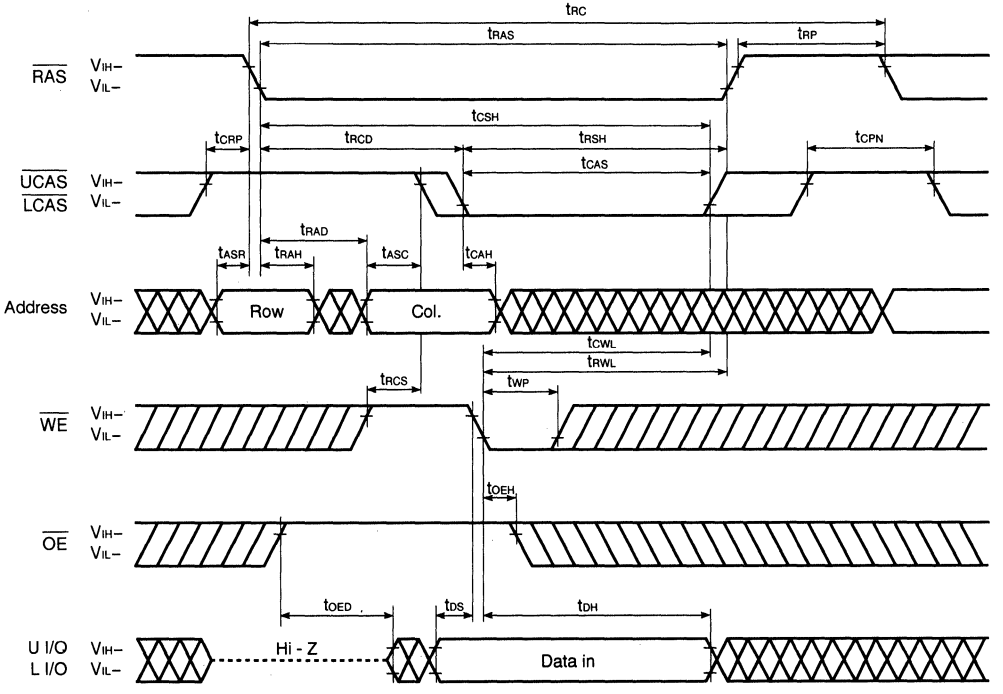
Remark $\overline{OE}$, L I/O: Don't care

Lower Byte Early Write Cycle

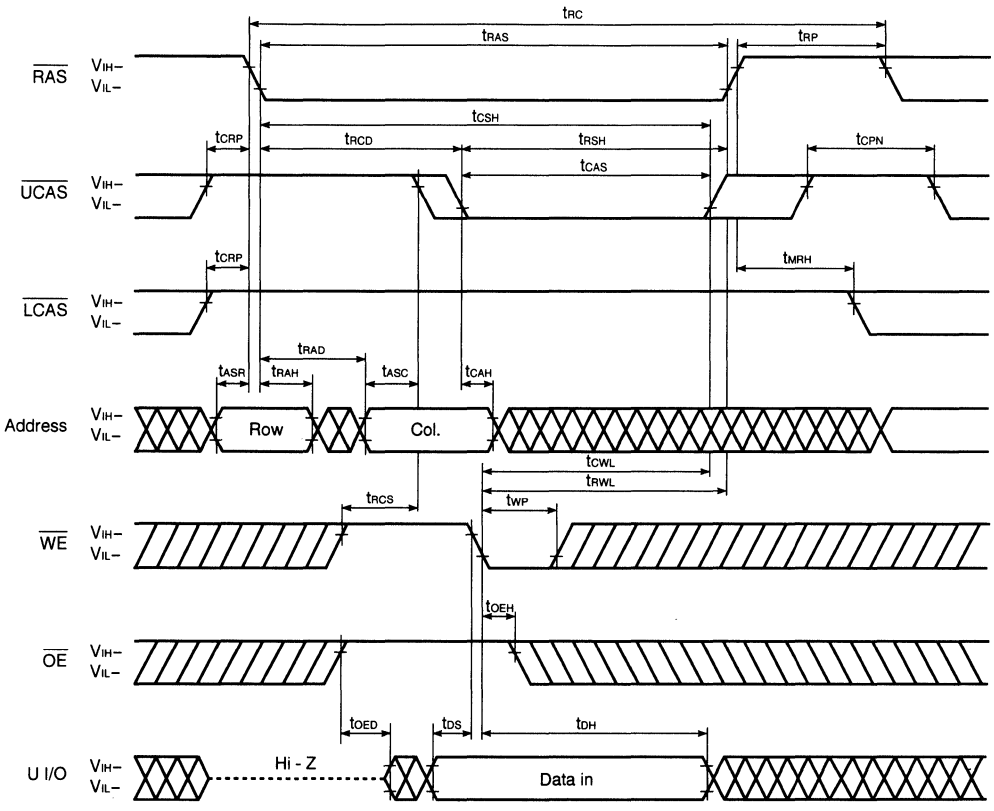


Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

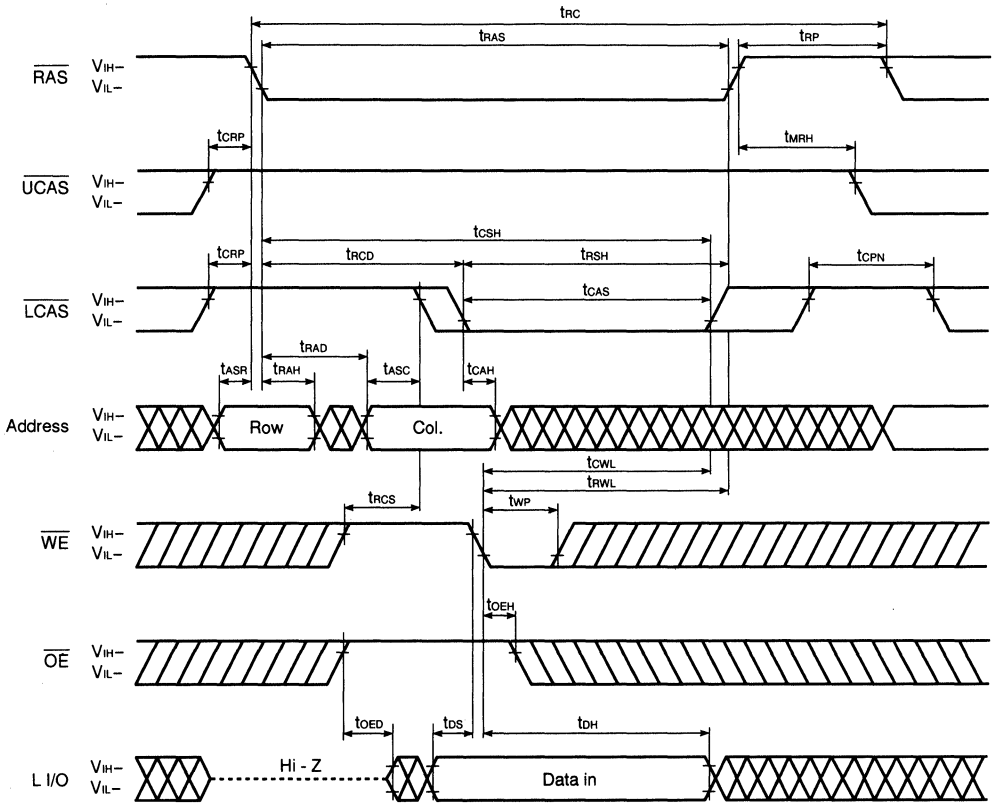


Upper Byte Late Write Cycle



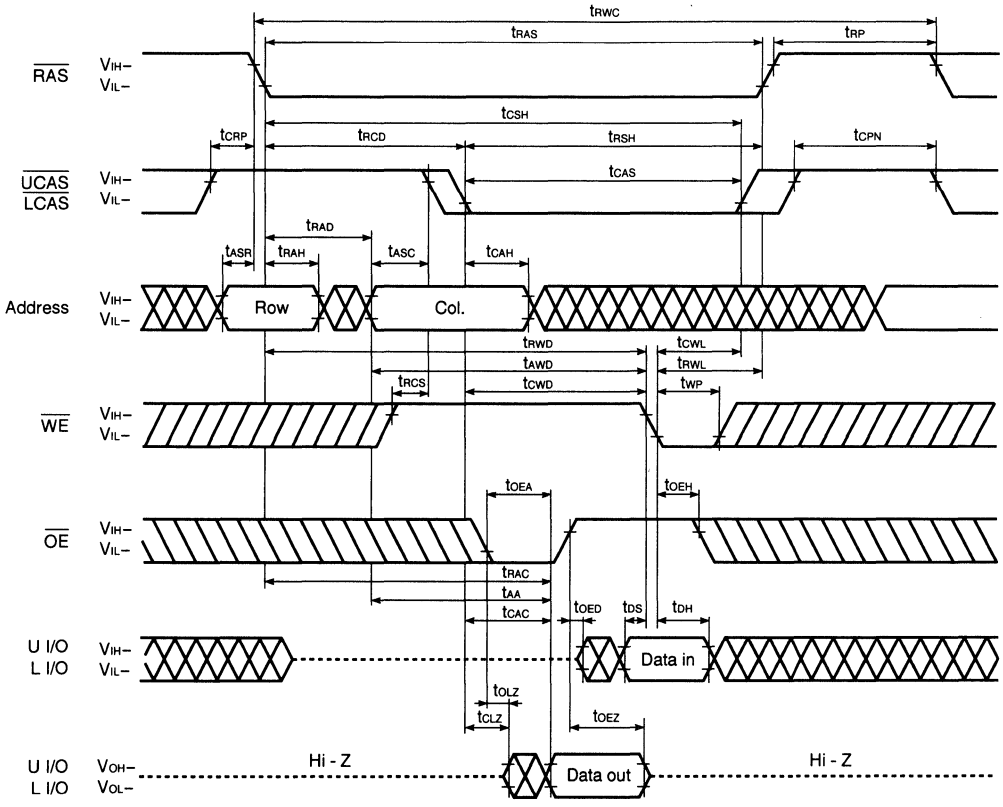
Remark L I/O: Don't care

Lower Byte Late Write Cycle

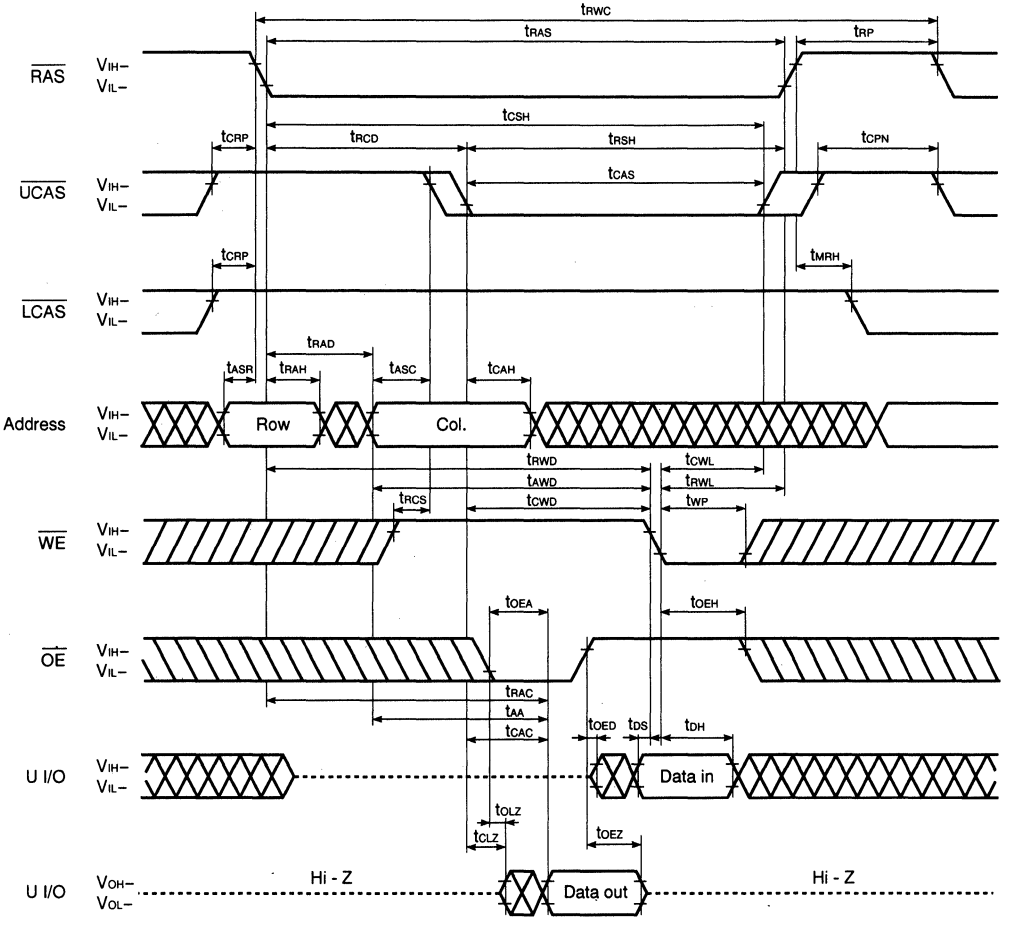


Remark U I/O: Don't care

Read Modify Write Cycle

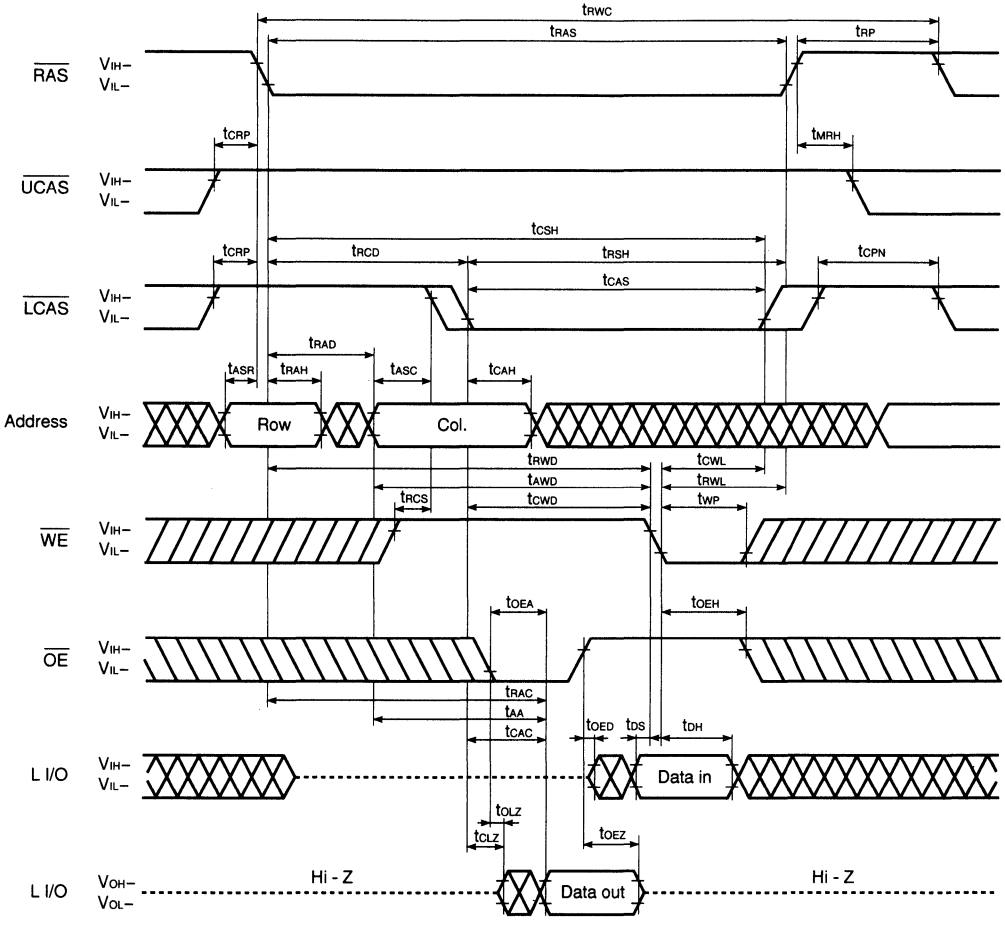


Upper Byte Read Modify Write Cycle



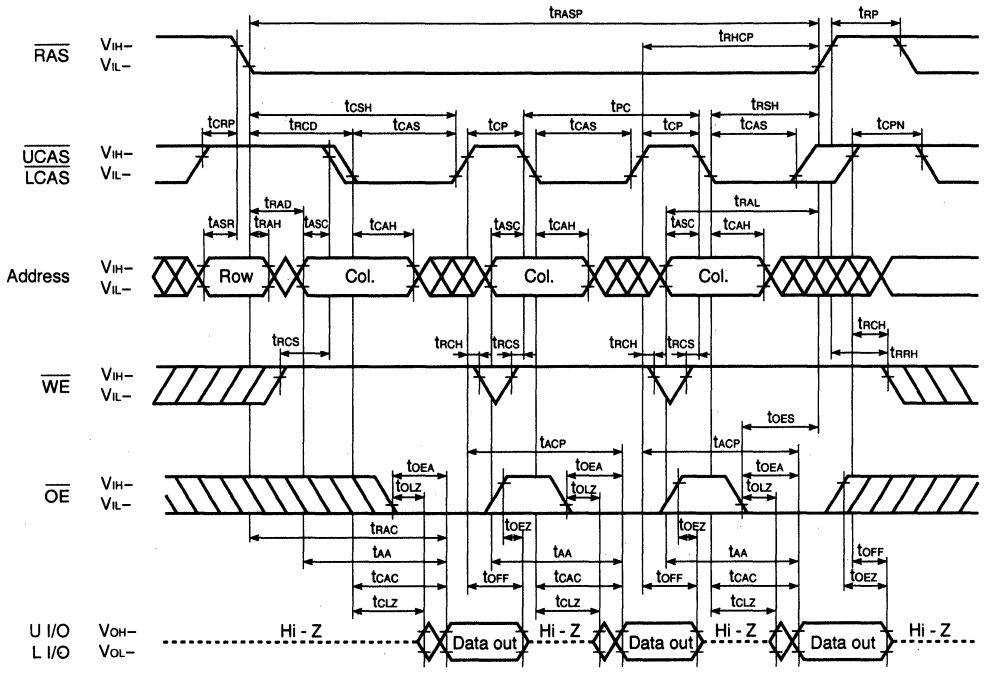
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle



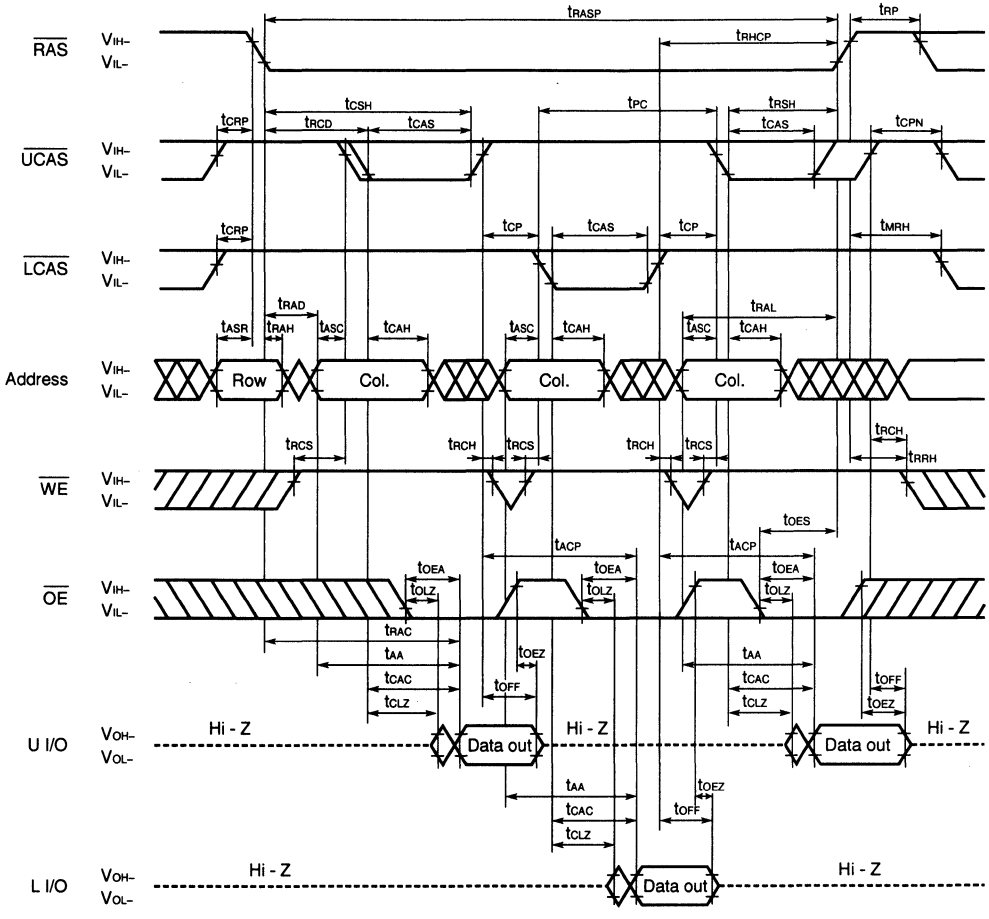
Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Fast Page Mode Read Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

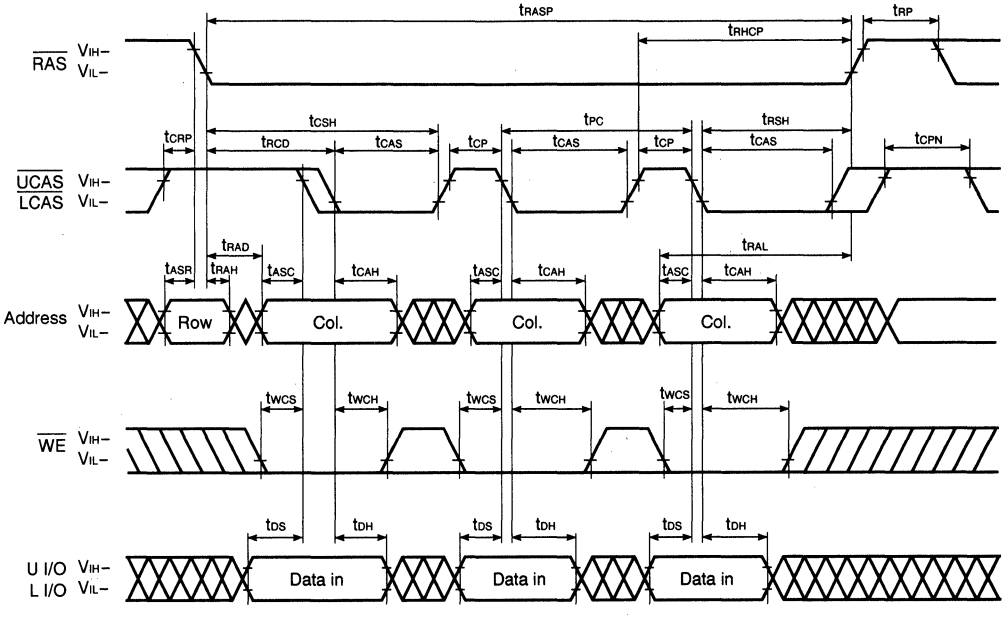
Fast Page Mode Byte Read Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

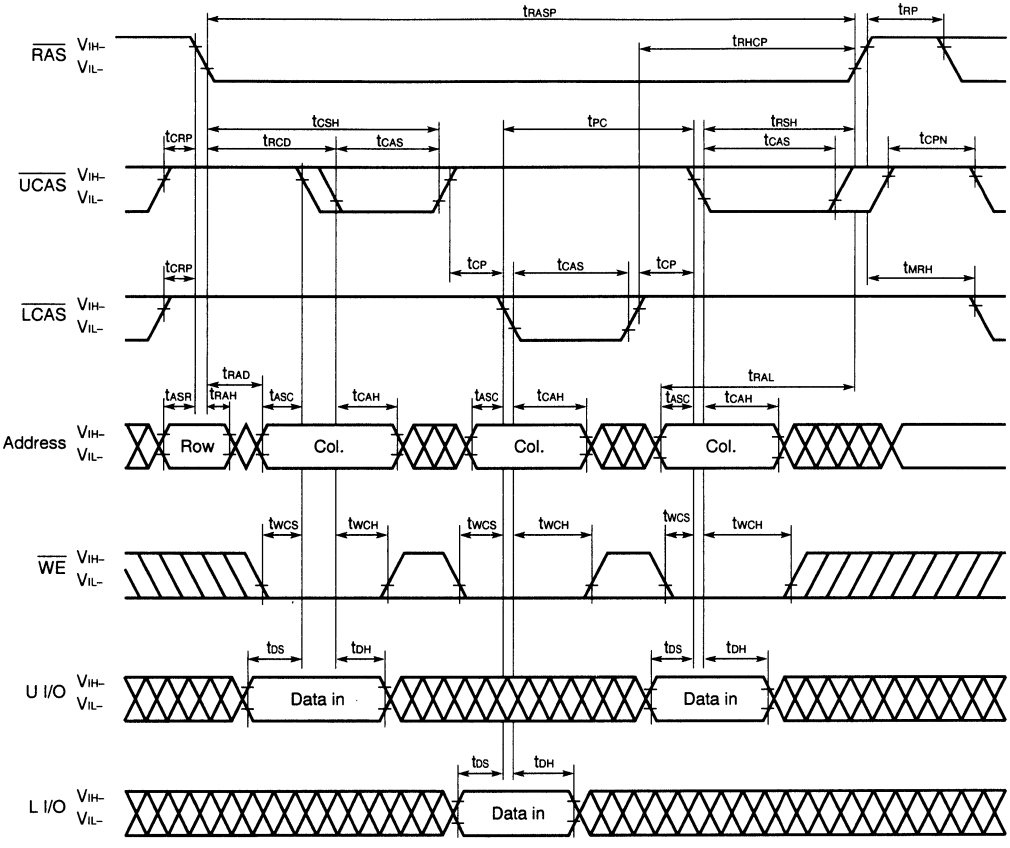
Fast Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

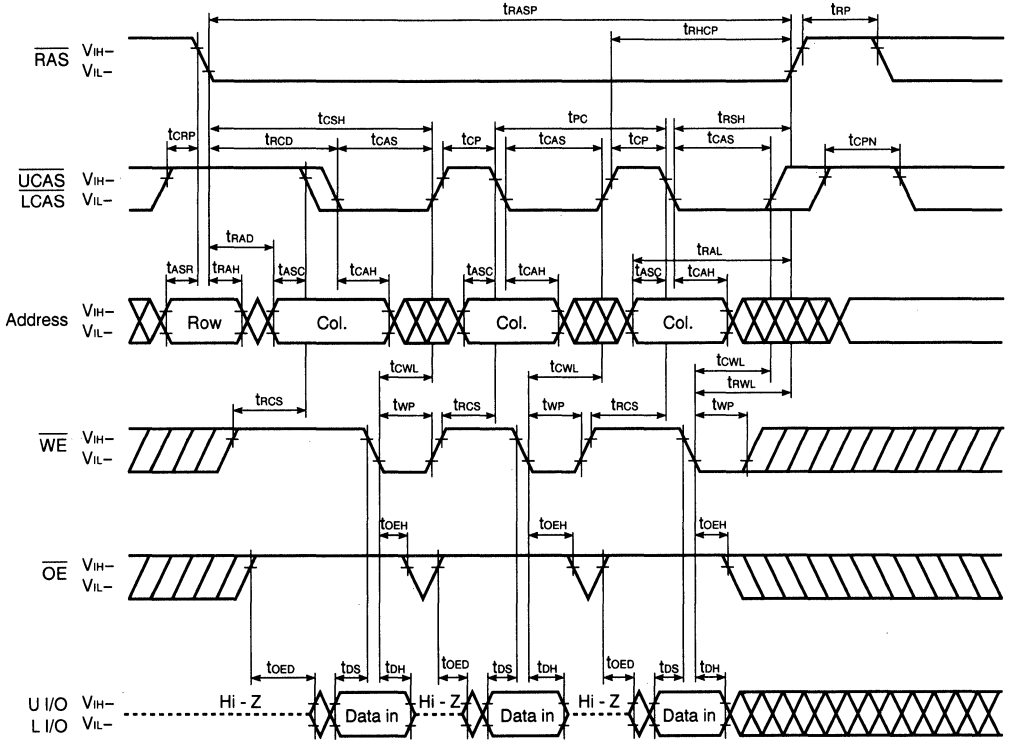
Fast Page Mode Byte Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

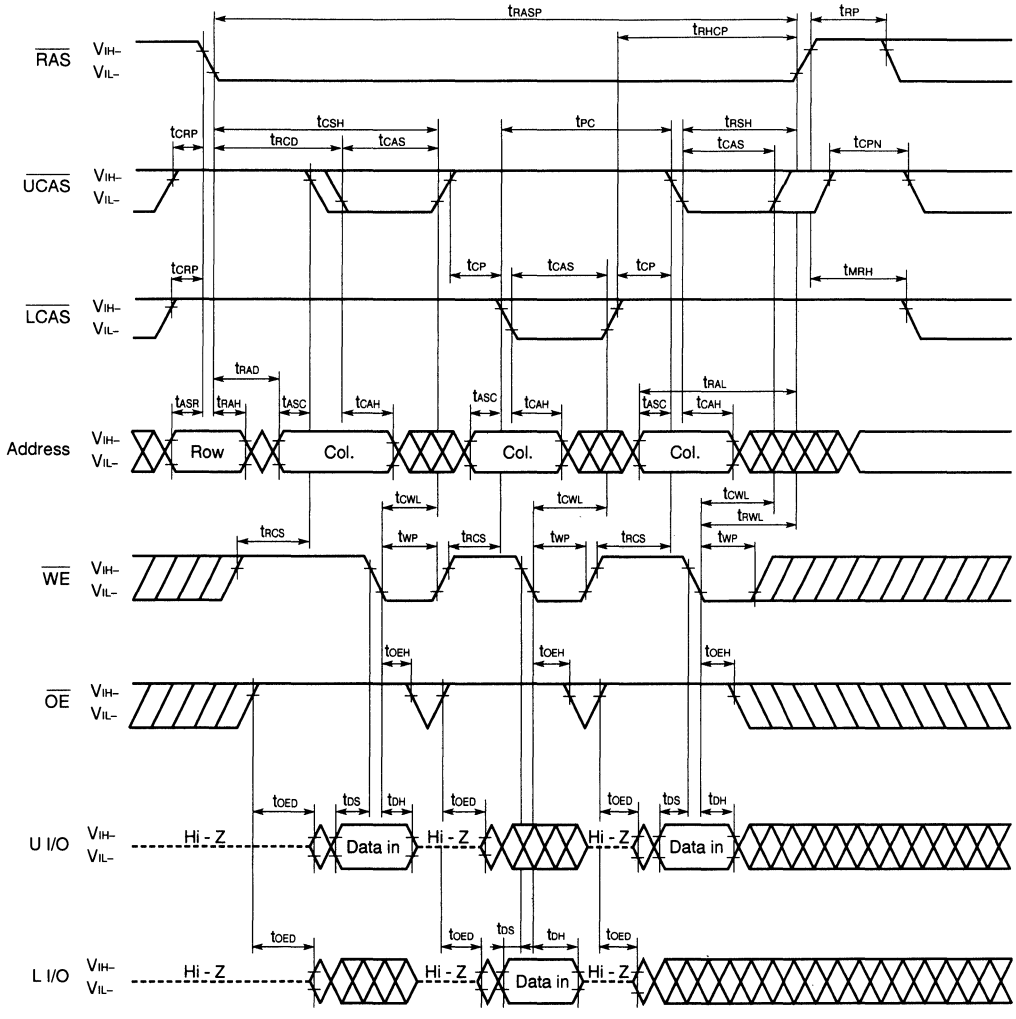
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Late Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

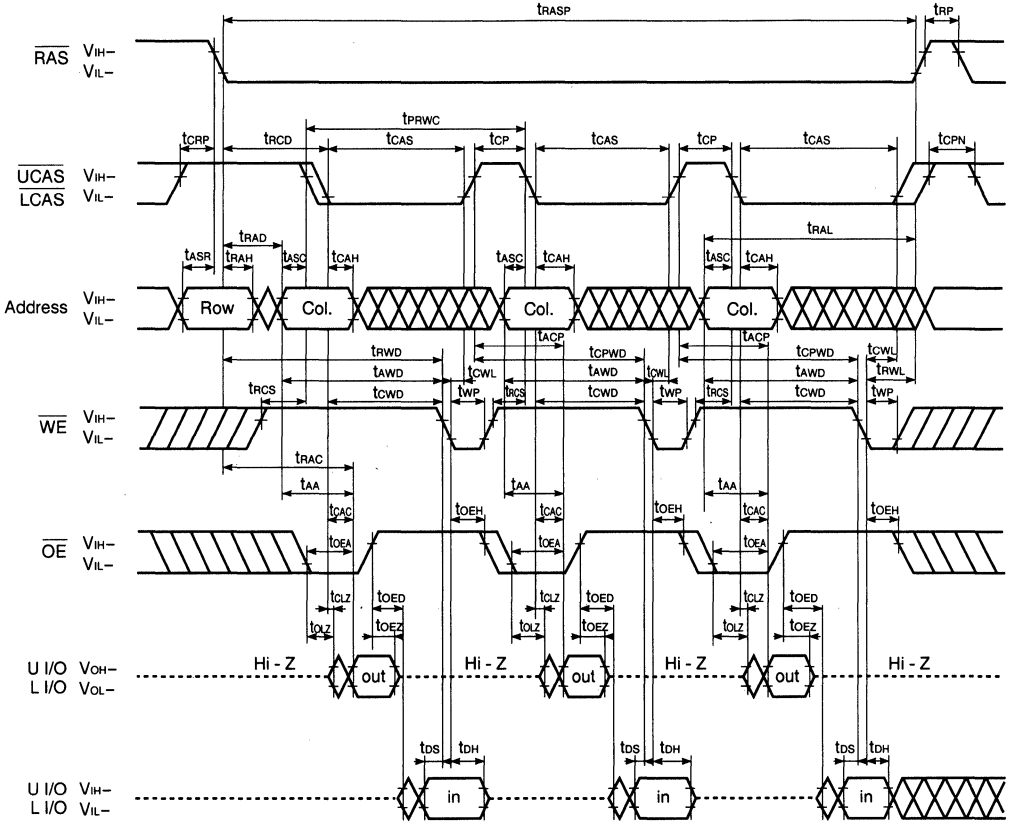
Fast Page Mode Byte Late Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

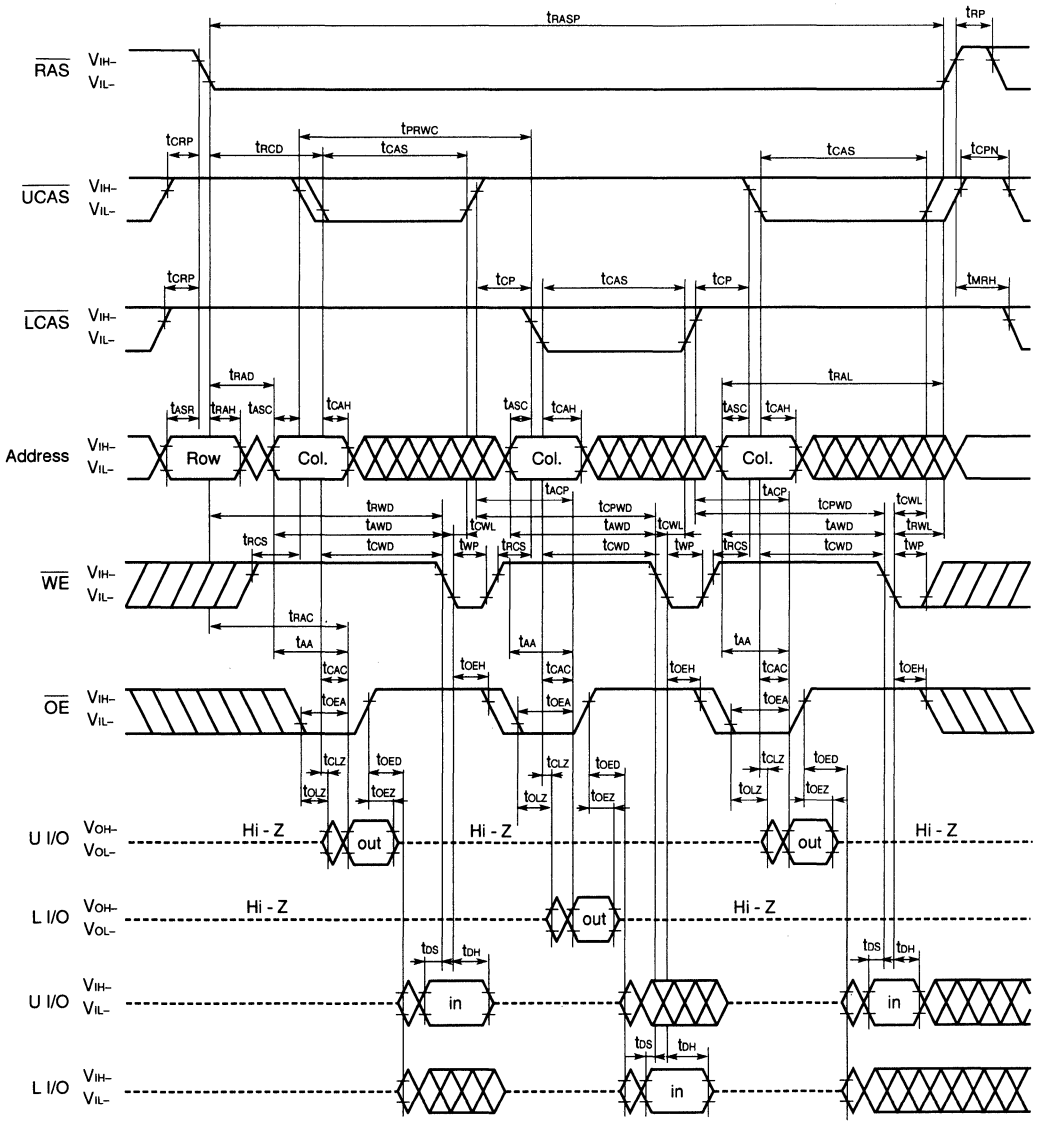
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

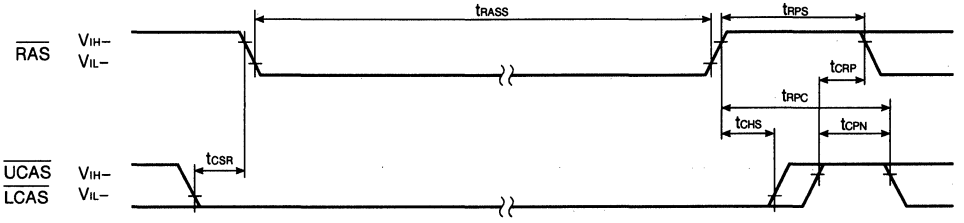
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S4260)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

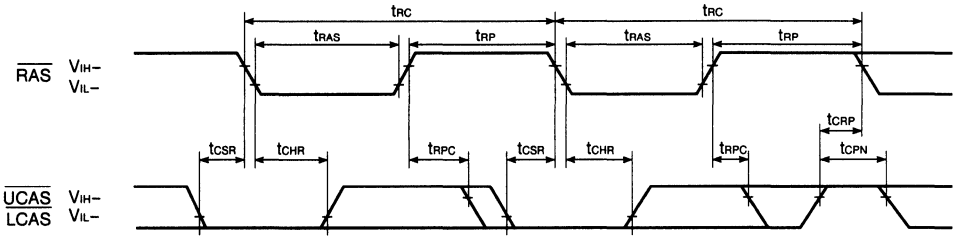
(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 512 times within an 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 512 times within an 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (512/128 ms) should be met.

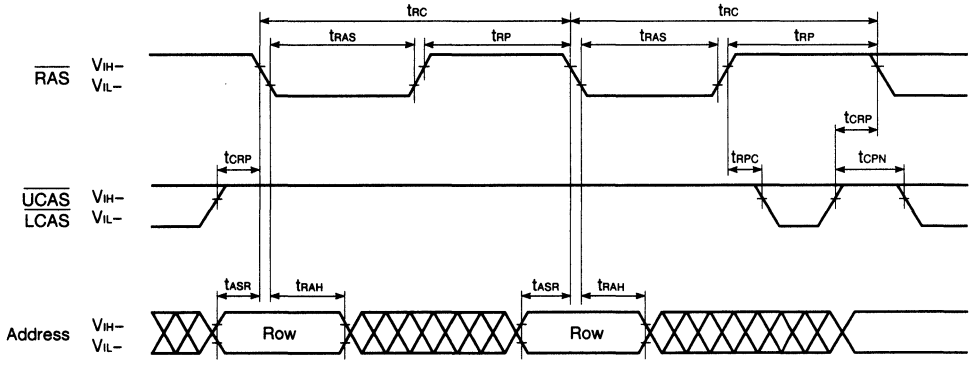
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



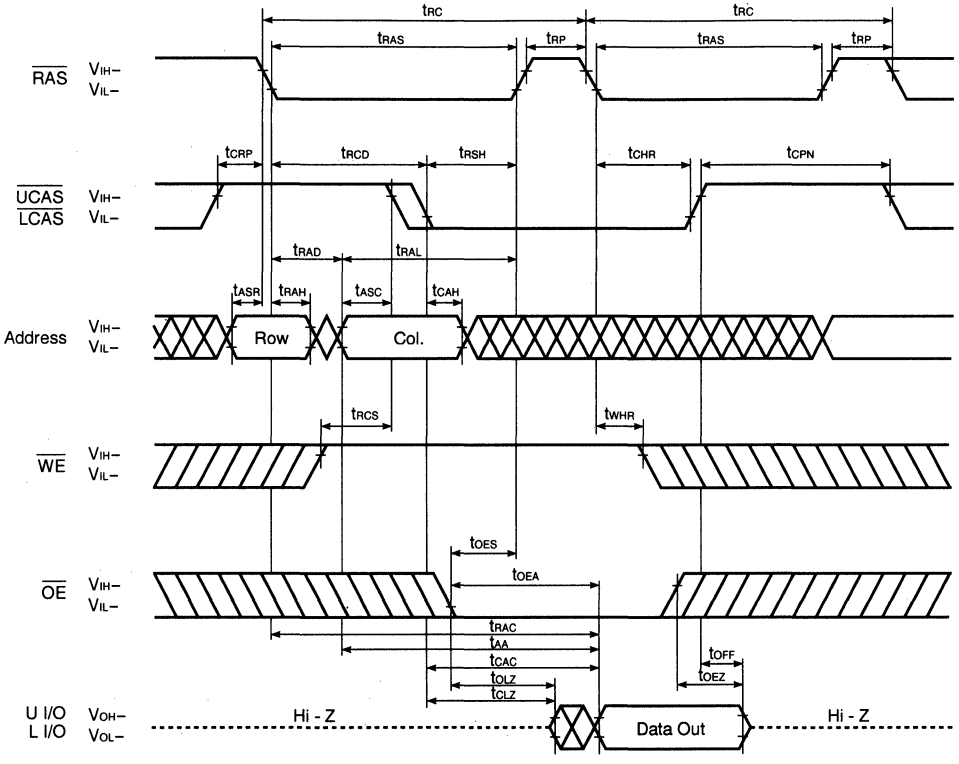
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

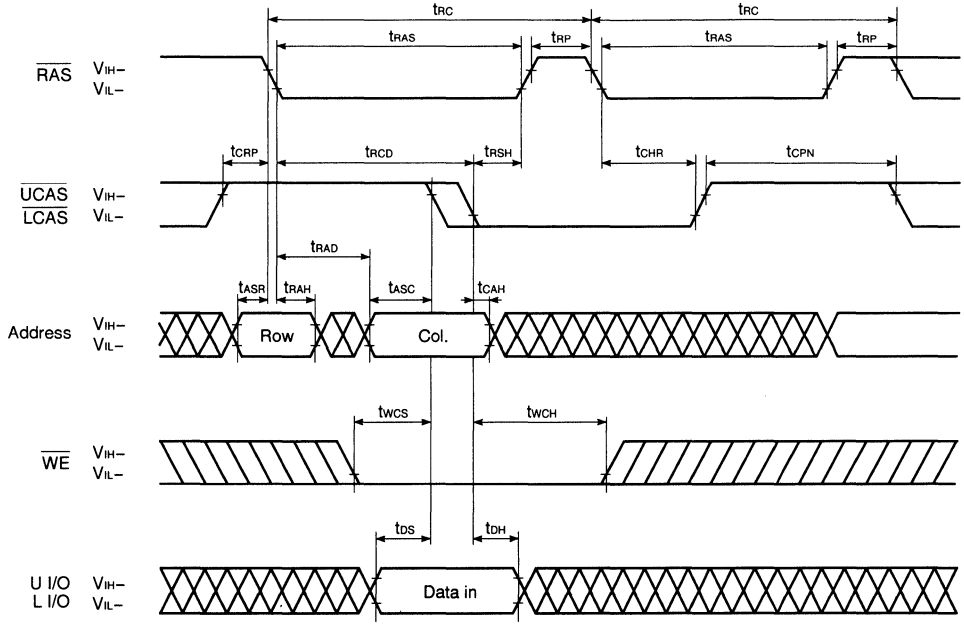


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)



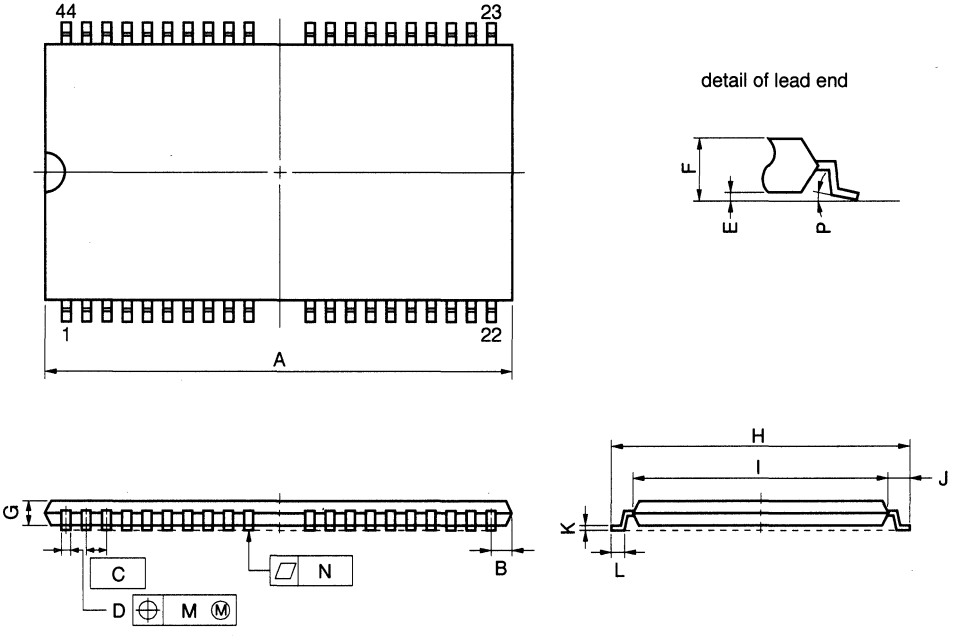
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



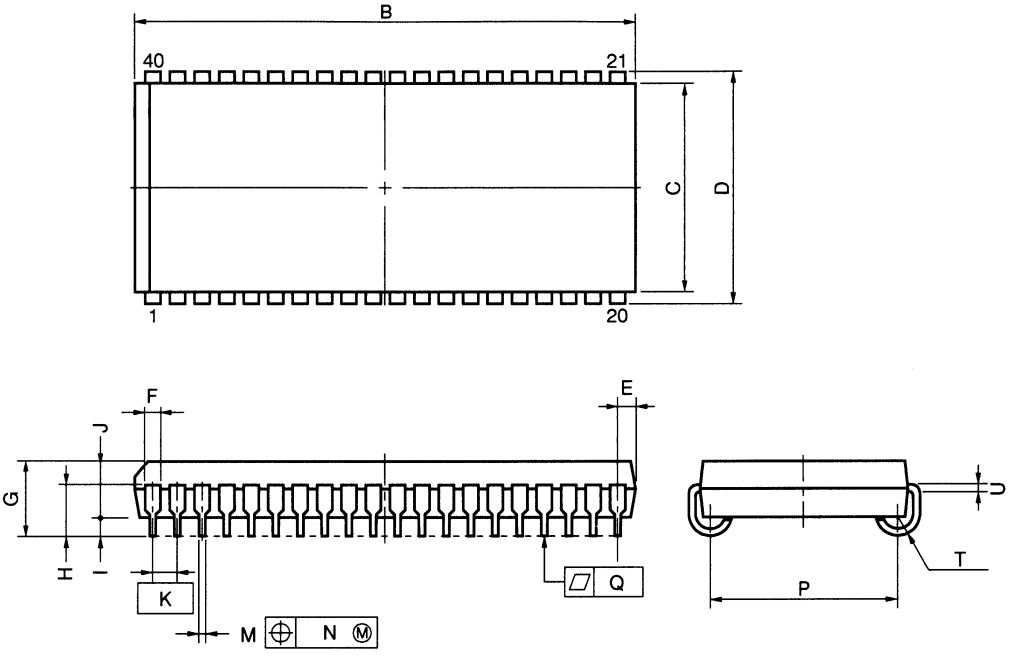
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.63 MAX.	0.734 MAX.
B	0.93 MAX.	0.037 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	0.013±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S44G5-80-7JF4

40 PIN PLASTIC SOJ (400 mil)



NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5±0.2	0.138±0.008
H	2.4±0.2	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.40±0.20	0.370±0.008
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

P40LE-400A-2

Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S4260, 424260.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S4260G5, 424260G5: 44-pin plastic TSOP (II) (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD42S4260LE, 424260LE: 40-pin plastic SOJ (400 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days[Note] (20 hours pre-baking is required at 125 °C afterwards) **Cautions** **1. After the first reflow process, cool the package down to room temperature, then start the second reflow process.** **2. After the first reflow process, do not use water to remove residual flux (water can be used in the second process).**	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	—

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

[MEMO]

Synchronous DRAM

NEC

MOS INTEGRATED CIRCUIT

μPD4516421, 4516821, 4516161

16M-bit Synchronous DRAM

Description

The μPD4516421, 4516821, 4516161 are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152×4×2, 1,048,576×8×2 and 524,288×16×2 (word×bit×bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs compatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) (×4, ×8) and 50-pin TSOP (II) (×16).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 Full Page)
- Programmable wrap sequence (Sequential/Interleave)
- Programmable $\overline{\text{CAS}}$ latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- ×4, ×8, ×16 organization
- Single +3.3±0.3 V power supply
- LVTTL compatible
- Byte control (×16) by LDQM and UDQM
- 2,048 refresh cycles/32ms
- Burst termination by Burst Stop command and Precharge command

Please contact your NEC sales representative if you need a complete data sheet.

Ordering Information

Part number	Organization (word x bit x bank)	Clock frequency MHz (MAX.)	Package
μPD4516421G5-A10	2Mx4x2	100	44-pin Plastic TSOP(II) (400mil)
4516421G5-A12		83	
4516421G5-A13		77	
4516421G5-A15		66	
μPD4516821G5-A10	1Mx8x2	100	44-pin Plastic TSOP(II) (400mil)
4516821G5-A12		83	
4516821G5-A13		77	
4516821G5-A15		66	
μPD4516161G5-A10	512Kx16x2	100	50-pin Plastic TSOP(II) (400mil)
4516161G5-A12		83	
4516161G5-A13		77	
4516161G5-A15		66	

NEC

MOS INTEGRATED CIRCUIT
μPD4516421-PC, 4516821-PC, 4516161-PC

16M-bit Synchronous DRAM for PC
SDRAM Lite

Description

The μPD4516421-PC, 4516821-PC, 4516161-PC are high-speed 16,777,216-bit synchronous dynamic random-access memories, organized as 2,097,152x4x2, 1,048,576x8x2 and 524,288x16x2 (wordxbitxbank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture.

All inputs and outputs are synchronized with the positive edge of the clock.

The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).

The synchronous DRAMs are packaged in 44-pin TSOP (II) (x4, x8) and 50-pin TSOP (II) (x16).

Features

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A11 (Bank Select)
- Burst-length : 1, 2, 4
- Programmable wrap sequence (Sequential/Interleave)
- $\overline{\text{CAS}}$ latency : 2, 3
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- x4, x8, x16 organization
- Single +3.3±0.3 V power supply
- LVTTL compatible
- Byte control (x16) by LDQM and UDQM
- 2,048 refresh cycles/32ms
- Burst termination by Precharge command

Please contact your NEC sales representative if you need a complete data sheet.

Ordering Information

Part number	Organization (word x bit x bank)	Clock frequency (MHz)	Package
μPD4516421G5-A83-PC	2Mx4x2	83	44-pin Plastic TSOP(II) (400mil)
4516421G5-A75-PC		75	
4516421G5-A67-PC		67	
4516421G5-A60-PC		60	
μPD4516821G5-A83-PC	1Mx8x2	83	44-pin Plastic TSOP(II) (400mil)
4516821G5-A75-PC		75	
4516821G5-A67-PC		67	
4516821G5-A60-PC		60	
μPD4516161G5-A83-PC	512Kx16x2	83	50-pin Plastic TSOP(II) (400mil)
4516161G5-A75-PC		75	
4516161G5-A67-PC		67	
4516161G5-A60-PC		60	

How to Use DRAM

USER'S MANUAL

NEC

HOW TO USE DRAM

Document No. M10339EJ2V0UMU1

INTRODUCTION

Purpose

This manual is intended for users who understand DRAM functions and design application systems using DRAMs.

Readers

This manual explains the basic properties of DRAM and their use.

How to read this manual

It is assumed that readers of this manual have general knowledge in the fields of electricity, logic circuits, and memory. For further details on the functions of each device, please refer to their data sheets.

DRAM devices can be divided into 5.0-V and low-voltage operation devices. This manual concentrates on 5.0-V operation devices (For information on low-voltage operation devices, see **CHAPTER 10 LOW VOLTAGE OPERATION**).

This manual uses the following abbreviations for refresh functions:

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	→ CRB refresh
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh	→ CBR long refresh
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh	→ CBR self refresh
$\overline{\text{RAS}}$ only refresh	→ ROR
Long $\overline{\text{RAS}}$ only refresh	→ Long ROR

Legend

Active low	: $\overline{\text{XXX}}$ (top bar over pin or signal name)
Note	: Footnote
Caution	: Points to be noted
Remark	: Supplementary explanations for main text
Numeric representations	: decimal ... xxxx

Related documents

Document related to the μPD4216100

- μPD4216100, 4217100 Data Sheet (IC-2923)

Document related to the μPD4216400

- μPD42S16400, 4216400, 42S17400, 4217400 Data Sheet (IC-2922)

Document related to the μPD42S16160, 4216160, 42S18160

- μPD42S16160, 4216160, 42S18160, 4218160 Data Sheet (IC-3217)

Document related to the μPD42S16160L

- μPD42S16160L, 4216160L, 42S18160L, 4218160L Data Sheet (IC-3218)

Document related to the Hyper Page Mode (HPM)

- μPD4216165 Data Sheet (IC-3378)

[MEMO]

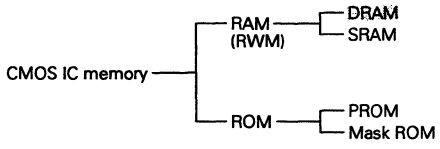
CHAPTER 1 DEFINITION OF DRAM

1.1 Classification of IC Memory

The CMOS IC memory can be divided into two main categories, namely RAM (RWM) and ROM (Read Only Memory).

Figure 1-1 shows the classification of the CMOS IC memory.

Figure 1-1. CMOS IC Memory Classification



(1) RAM (Random Access Memory)...RWM (Read Write Memory)

The RAM can be broadly divided into DRAM and SRAM (See **1.2 DRAM Features**). The RAM memory freely enables high-speed reading and writing.

The ROM also enables reading freely but the RAM generally enables both reading and writing freely. All data in the RAM are lost by turning off the power.

The DRAM can be further divided into conventional DRAM and high-speed DRAM. High-speed DRAM refers to synchronous DRAM and Rambus™ DRAM operating in synchronization with a clock and page access time enabling as compared with conventional DRAMs. This user's manual describes conventional DRAMs. See each user's manual for the details on the synchronous DRAM and Rambus DRAM.

(2) ROM (Read Only Memory)

The ROM can be broadly divided into PROM and mask ROM. It is a memory exclusively used for reading only. Data contained in ROM are retained even if the power is turned off.

As its name indicates, the ROM (Read Only Memory), once written, can be read only and hence cannot be generally rewritten. However, some PROM (Programmable ROM) can be rewritten.

1.2 DRAM Features

The DRAM has the following features:

(1) Memory cell structure = 1 transistor + 1 capacitor → Large density easily provided
(2) Refreshing required
(3) Address multiplex method

The following explains the features (1) to (3) of DRAM in comparison with the SRAM.

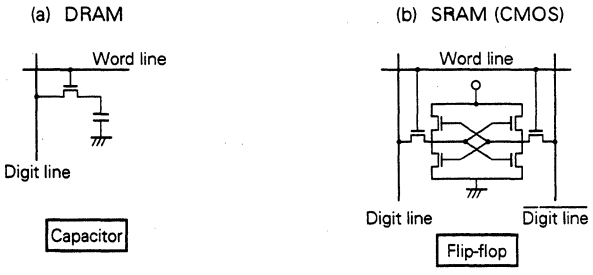
(1) Memory cell structure

The memory cell stores one-bit data. One 16M DRAM has 16,777,216 (2^{24}) memory cells. Figure 1-2 shows the memory cell structure of DRAM and SRAM.

The DRAM memory cell consists of one transistor and one capacitor and hence is highly integrated as compared with the SRAM in 6-transistor configuration.

The SRAM memory cell consists of flip-flops (in 6-transistor configuration) and does not use any capacitors.

Figure 1-2. Memory Cell



(2) Refresh operation

The DRAM uses capacitors in memory cells and hence must be refreshed.

The electric charge accumulated in DRAM capacitors tends to discharge little by little (leak) when left as it is. Therefore, data cannot be saved simply by providing power supply voltage.

Let us call the condition of a cell filled with electric charge as a "high level". If such a cell is left as is, the electric charge contained in the cell will be lost through leakage and the cell will change to the low level. The high level must always be maintained to retain data. Refreshing is the operation for constantly amplifying electric charge to retain data.

The SRAM does not use capacitors and hence does not require refreshing.

Caution For some cells, the condition of a cell filled with electric charge is called "low level" and refreshing is also required for those cells to maintain the low level for the same reason explained above.

(3) Address multiplex method

Figure 1-3 shows a diagram of the address multiplex method.

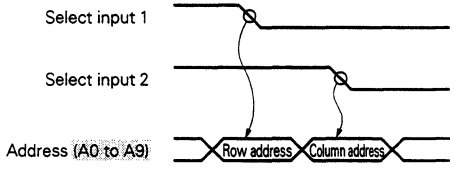
The address multiplex method uses two select inputs. For example, if an address line requires 20 bits, these 20 bits are read in two packets of 10 bits each. By thus reducing in half the number of address pins, high integration and package miniaturization can be achieved.

The DRAM uses this address multiplex method. For this reason, it can be packaged more compactly than SRAM for an equal memory density.

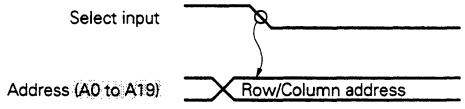
Although the SRAM does not use the address multiplex method, it enables easier timing design than DRAM as data can be transferred using one select input only.

Figure 1-3. Address Multiplex Method (for address line requiring 20 bits)

(a) DRAM type (address multiplex method)



(b) SRAM type (address non-multiplex method)



A comparison of DRAM features and other types of memories is shown in the table below.

Table 1-1. IC Memory Features

Feature \ Type	DRAM	SRAM	Mask ROM	EPROM	Flash Memory
Large density	◎	△	◎	○	◎
Compact package	◎	△	△	△	△
Data-retention capability	△	○	◎	◎	◎
Bit unit cost	◎	△	◎	△	○
Access time	○	◎	○	○	○

◎: excellent ○: very good △: lacking

[MEMO]

CHAPTER 2 WORD AND BIT ORGANIZATIONS

This chapter describes word and bit organizations using an example of 16M DRAM.

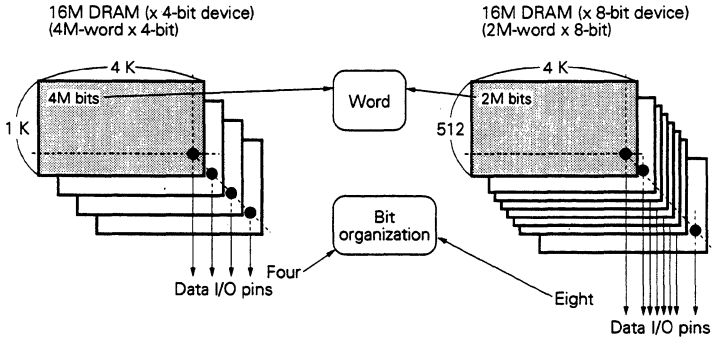
The word means a memory density controlled by one data I/O pin.

The bit organization means the number of data whose I/O can be controlled at one time. The x 4-bit device has four data I/O pins and can control I/O of four bits at one time. The x 8-bit device has eight data I/O pins and can control I/O of 8-bit data at one time. Therefore, word x bit organization forms an entire memory density.

For example, the memory density of 4M words x 1 bit is 4M bits and that of 4M words x 4 bits is 16M bits. The word x bit organization may be different for the same memory density.

The word and bit organization may be called depth and width, respectively, when Figure 2-1 is viewed from the side.

Figure 2-1. Simplified Block Diagram



When a certain address is defined, 4-bit and 8-bit data are selected for x 4-bit and x-8 bit organizations, respectively. Therefore, if there are address pins available for defining all words (x 4-bit device: 4M bits, x 8-bit device: 2M bits), the data of all addresses of memory can be selected.

Table 2-1. Number of Memory Cells and Number of Address Pins

Items / DRAM type	X axis		Y axis	
	Number of memory cells	Number of address pins	Number of memory cells	Number of address pins
16M DRAM (x 4-bit device)	4 K	12	1 K	10
16M DRAM (x 8-bit device)	4 K	12	512	9

Because the DRAM uses the address multiplex method, the number of address pins is 12 for both DRAMs in x 4-bit and x 8-bit organizations.

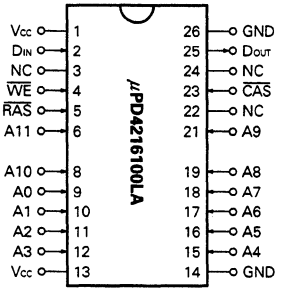
[MEMO]

CHAPTER 3 PIN FUNCTIONS

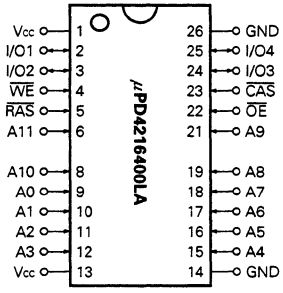
This chapter describes DRAM pin functions based on the μPD4216100 (16M-word x 1-bit device) and μPD4216400 (4M-word x 4-bit device).

3.1 Pin Configurations

(a) μPD4216100LA
(26-pin Plastic SOJ (300 mil))



(b) μPD4216400LA
(26-pin Plastic SOJ (300 mil))



3.2 Pin Functions (common to μPD4216100 and μPD4216400)

Pin name	I/O	Pin functions	Remark
$\overline{RAS}$: Row Address Strobe	In	Signal that activates chip and fetches row address	
$\overline{CAS}$: Column Address Strobe	In	Signal that fetches column address	
$\overline{WE}$: Write Enable	In	Signal enabling write	
Vcc : Power Supply	–	Power supply voltage pin	
GND : Ground	–	Ground pin	
A0-A11 : Address	In	Address input pin	
DIN : Data Input	In	Data input pin	μPD4216100 only
DOUT : Data Output	Out	Data output pin	
$\overline{OE}$: Output Enable	In	Signal enabling output	μPD4216400 only
I/O1-I/O4 : Data Inputs/Outputs	I/O	Data I/O pin	
NC : No Connection	–	Not connected to internal memory	

3.3 Pin Function Explanation

The pin functions of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ are explained below.

3.3.1 $\overline{RAS}$: Row address strobe

This is a signal that activates chips. When the $\overline{RAS}$ is activated, DRAM operation begins. When the $\overline{RAS}$ is activated, a row address is latched, the corresponding word line is selected, and the sense amplifier circuit is activated.

The sense amplifier circuit is used to amplify signals in the capacitor.

The $\overline{RAS}$ is activated when it is low. The " $\overline{\ }$ " (bar) indicates that this signal is activated when it is low.

3.3.2 $\overline{CAS}$: Column address strobe

This signal fetches a column address, selects the digit line connected to the sense amplifier, and activates the data I/O circuit.

3.3.3 $\overline{WE}$: Write enable

When $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are activated, write operation is enabled. Write operation is divided into two major groups.

- Early write : $\overline{WE}$ is activated before or at the same time $\overline{CAS}$ is activated.
- Late write : $\overline{WE}$ is activated after $\overline{CAS}$ is activated.

3.3.4 $\overline{OE}$: Output enable

This signal is used to switch between data input and output (for devices with multiple-bit organization only). The DRAM is divided as shown in Table 3-1 depending on the word and bit organization.

Table 3-1. DRAM Word x Bit Organization

	4M DRAM	16M DRAM
x1-bit device	4 M x 1	16 M x 1
Multiple-bit device	1 M x 4, 512 K x 8, 256 K x 16 etc.	4 M x 4, 2 M x 8, 1 M x 16 etc.

In multiple-bit devices, the I/O pin serve both as the input and output pins and therefore I/O switching signal (=$\overline{OE}$ signal) is required. In x 1-bit devices, $\overline{OE}$ is not required because the data input pins and data output pins are separate. The data I/O pins used for multiple-bit devices and x 1-bit devices are shown in Table 3-2.

Table 3-2. Data I/O Pins

	x 1-bit device	Multiple-bit device
Input pin	DIN	I/O1-I/On **Note**
Output pin	DOUT	

Note n = 4 : x 4-bit device
= 8 : x 8-bit device
= 16 : x 16-bit device

In multiple-bit devices, read operation is enabled when $\overline{OE}$ and then $\overline{RAS}$ and $\overline{CAS}$ are activated. At this time, when $\overline{WE}$ is activated, $\overline{OE}$ changes to 'don't care' in the memory and read operation is disabled. Therefore, read/write operation is enabled only through the control of $\overline{WE}$, with $\overline{OE}$ held active.

Remark In the read modify write cycle, data are output and input once each in one cycle. For details, see **4.3 Read Modify Write Cycle**.

3.4 Block Diagram

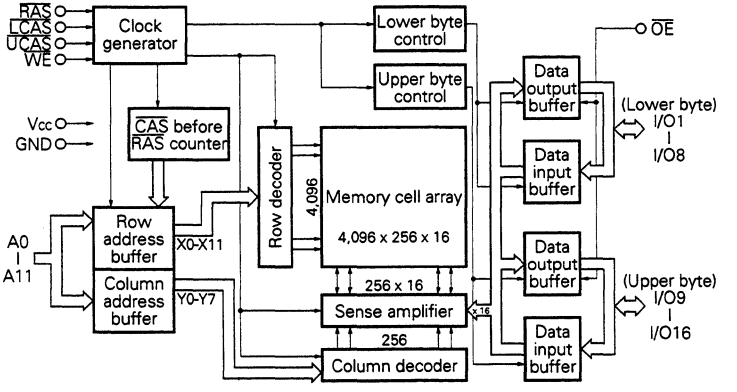
The following two types of DRAM block diagrams are shown.

μPD42S16160 (1M-word x 16-bit, 4,096 refresh)

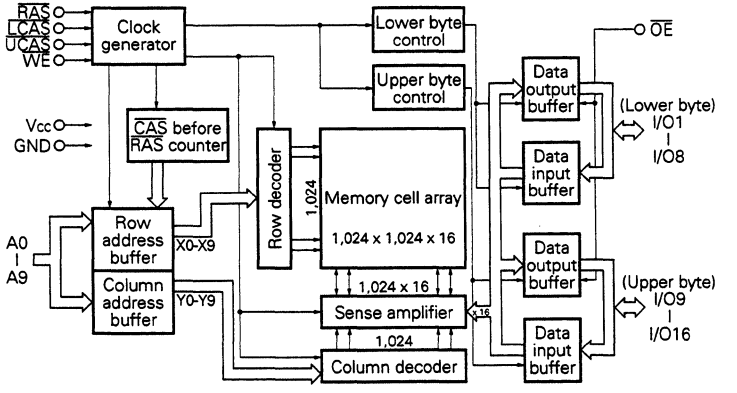
μPD42S18160 (1M-word x 16-bit, 1,024 refresh)

Figure 3-1. Block Diagram

(a) μPD42S16160 (1M-word x 16-bit, 4,096 refresh)



(b) μPD42S18160 (1M-word x 16-bit, 1,024 refresh)



3.4.1 Block diagram explanation

The block diagram is explained below.

(1) When $\overline{RAS}$ is activated:

When $\overline{RAS}$ is activated, the signal travels to the row decoder, latches a row address, selects the corresponding word line, and activates the sense amplifier. The $\overline{RAS}$ also enables activation of $\overline{CAS}$ (Signal priority is: $\overline{RAS}$>$\overline{CAS}$>$\overline{WE}$>$\overline{OE}$).

(2) When $\overline{CAS}$ is activated:

When $\overline{CAS}$ is activated, the signal travels to the column decoder, latches a column address, selects the corresponding digit line, and enables data I/O. The $\overline{CAS}$ also enables activation of $\overline{WE}$ and $\overline{OE}$.
The $\overline{UCAS}$ and $\overline{LCAS}$ control the upper and lower bytes, respectively, thus achieving control in units of bytes (See **CHAPTER 8 BYTE CONTROL**).
Also, when the $\overline{CAS}$ is activated before $\overline{RAS}$, the $\overline{CAS}$ before $\overline{RAS}$ counter is activated, thus automatically generating a row address.

(3) When $\overline{WE}$ is activated:

When $\overline{WE}$ is activated, data are input.

(4) When $\overline{OE}$ is activated:

When $\overline{OE}$ is activated and $\overline{WE}$ is inactivated, data are output.

[MEMO]

CHAPTER 4 OPERATION MODES

Operation modes can be generally divided into read and write. Read consists in extracting effective data from memory and write consists in inputting effective data into memory.

In this manual, a series of operations required for read operations is called read cycle and a series of operations for write operations is called write cycle. Before each operation mode is explained, legends used in timing charts are provided in Table 4-1.

Signal names listed higher in timing charts have precedence over ones listed lower ($\overline{RAS}$ > $\overline{CAS}$ > $\overline{WE}$ > $\overline{OE}$). If $\overline{WE}$ is low, $\overline{OE}$ is "don't care" in memory.

Table 4-1. Legend

Notation	Meaning
	Low or high level can be input and level can be changed from high to low or vice versa at any time. Input of undefined levels (neither high nor low) is prohibited.
	High level can be input and level can be changed from high to low at any time. However, low-to-high transition is prohibited.
	Low level can be input and level can be changed from low to high at any time. However, high-to-low transition is prohibited.
Don't care	Signals of all levels can be input. (Low, high, and undefined levels)
Hi-Z (High Impedance)	The output state is neither high nor low level.

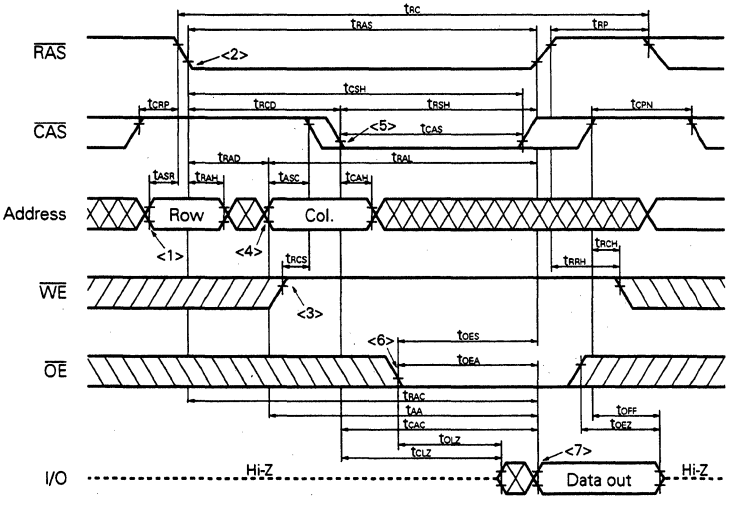
4.1 Read Operation

4.1.1 Read cycle

Read cycle is executed by activating $\overline{RAS}$ and then $\overline{CAS}$ while $\overline{WE}$ is not activated and $\overline{OE}$ is activated. The $\overline{RAS}$ latches row addresses and $\overline{CAS}$ latches column addresses.

Figure 4-1 shows the timing chart for the read cycle.

Figure 4-1. Read Cycle



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Inactivates $\overline{WE}$ to select read mode.
<4> Defines column address.
<5> Activates $\overline{CAS}$ to latch column address.
<6> Activates $\overline{OE}$ to enable output buffer.
<7> Start of data output.

$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Inactive
$\overline{OE}$	Active
I/O	Output

4.1.2 Access time

The effective access time in the read cycle varies depending on the conditions as shown in Table 4-2.

Table 4-2. Access Time in Read Cycle

	Input Conditions	Access Time	Access Time from $\overline{RAS}$
(1)	$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
(2)	$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
(3)	$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

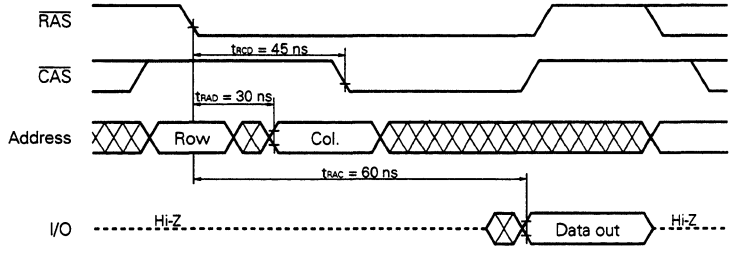
The $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA}, or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

Assuming that the specification is as shown in Table 4-3, an example for Table 4-2 is shown below.

Table 4-3. Specification of a Certain Device (for read cycle)

	MIN.	MAX.	Unit
t_{RAD}	12	30	ns
t_{RCD}	14	45	
t_{RAC}	–	60	
t_{AA}	–	30	
t_{CAC}	–	15	

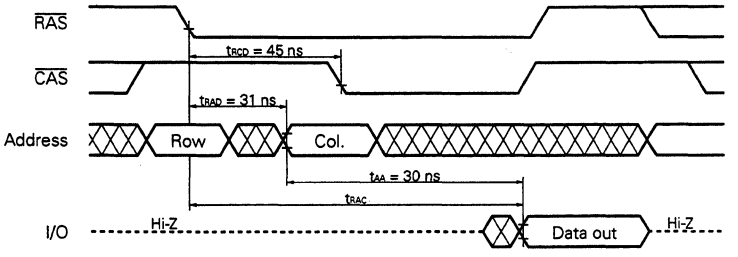
(1) When t_{RAC} becomes valid ($\overline{RAS}$ access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

When t_{RAD} is equal to 30 ns and t_{RCD} is equal to 45 ns, t_{RAC} becomes valid. Data are output in 60 ns after the $\overline{RAS}$ is activated.

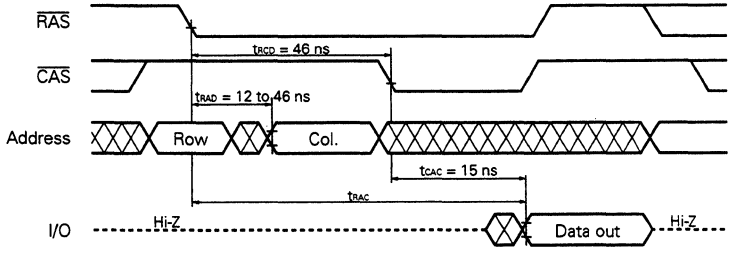
(2) When t_{AA} becomes valid (address access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

When t_{RAD} is equal to 31 ns ($t_{RAD} > t_{RAD\ (MAX.)}$) and t_{RCD} is equal to 45 ns, t_{AA} becomes valid.
Therefore, data are output in 61 ns after $\overline{RAS}$ is activated.
The access time from $\overline{RAS}$ becomes ($t_{RAD} + t_{AA}$) and is delayed from $\overline{RAS}$ access.

(3) When t_{CAC} becomes valid ($\overline{CAS}$ access):



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

The t_{CAC} becomes valid regardless of the value of t_{RAD} when t_{RCD} is equal to 46 ns ($t_{RCD} > t_{RCD\ (MAX.)}$) (the value of $t_{RAD\ (MIN.)}$ and address setup time need to be observed).
Therefore, data are output in 61 ns after $\overline{RAS}$ is activated.
The access time from $\overline{RAS}$ becomes ($t_{RCD} + t_{CAC}$) and is delayed from $\overline{RAS}$ access.

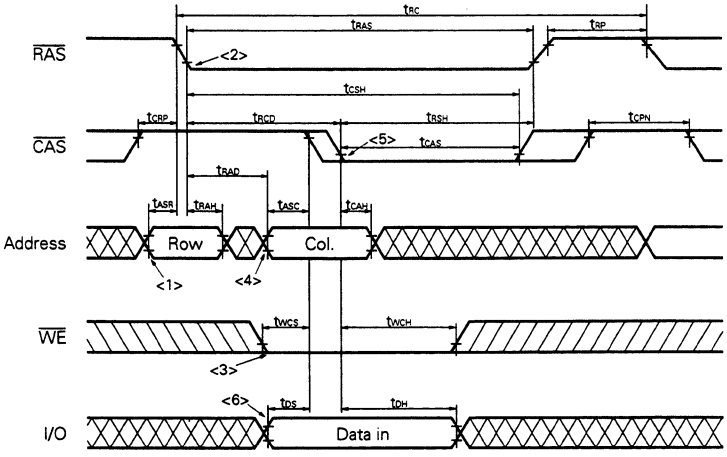
4.2 Write Operation

Write operation is enabled by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$.

4.2.1 Early write cycle

The early write cycle is executed by activating $\overline{WE}$ before or at the same time when $\overline{CAS}$ is activated.

Figure 4-2. Early Write Cycle



Remark $\overline{OE}$: don't care

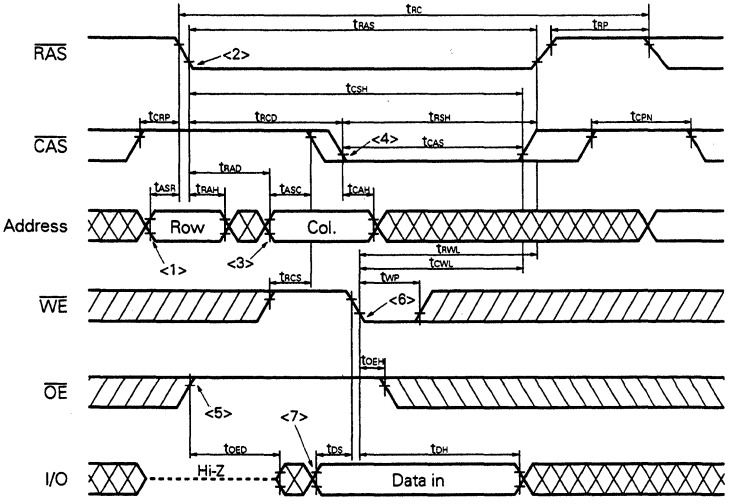
<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Activates $\overline{WE}$ to enable input buffer.
<4> Defines column address.
<5> Activates $\overline{CAS}$ to latch column address.
<6> Sets input data.

$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Active
$\overline{OE}$	Don't care
I/O	Input

4.2.2 Late write cycle

The late write cycle is executed by activating $\overline{WE}$ after activating $\overline{CAS}$.

Figure 4-3. Late Write Cycle



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Inactivates $\overline{OE}$ to select write mode.
<6> Activates $\overline{WE}$ to enable input buffer.
<7> Sets input data.

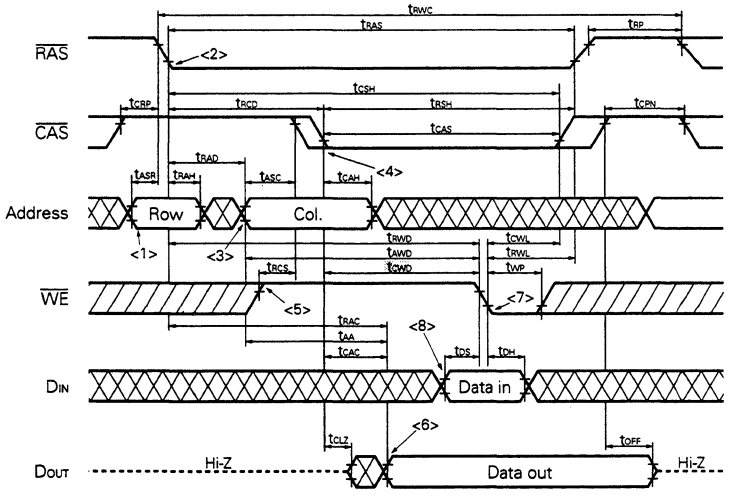
$\overline{RAS}$	Active
$\overline{CAS}$	Active
$\overline{WE}$	Active
$\overline{OE}$	Don't care
I/O	Input

4.3 Read Modify Write Cycle

Read modify write cycle is a cycle that outputs and inputs data from/to the same address during one cycle ($\overline{RAS}$/$\overline{CAS}$ cycle). Write is enabled by activating $\overline{WE}$ while $\overline{RAS}$ and $\overline{CAS}$ are active. Read is enabled by activating $\overline{OE}$ while $\overline{RAS}$ and $\overline{CAS}$ are active. Because x 1-bit devices do not have $\overline{OE}$, write and read operations are controlled by activating or inactivating $\overline{WE}$.

The timing charts of the read modify write cycles of x 1-bit and multiple-bit devices are shown in Figure 4-4 and Figure 4-5, respectively. In either case, if $\overline{WE}$ is activated after a delay from $\overline{CAS}$ that exceeds $\overline{CAS}$-$\overline{WE}$ delay time ($t_{CWD\ (MIN.)}$), the read modify write operation is enabled.

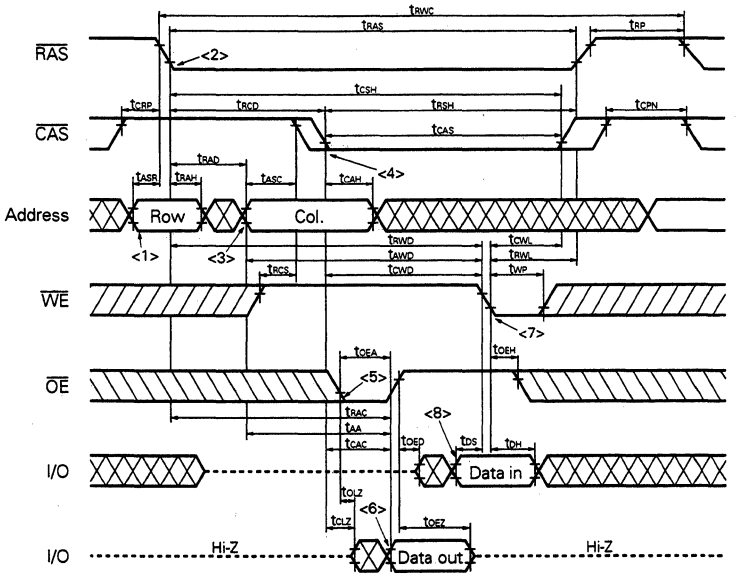
Figure 4-4. Read Modify Write Cycle of x1-Bit Device



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Inactivates $\overline{WE}$ to enable output buffer.
<6> Start of data output.
<7> Activates $\overline{WE}$ to enable input buffer.
<8> Sets input data.

$\overline{RAS}$	Active	
$\overline{CAS}$	Active	
$\overline{WE}$	Inactive	Active
DATA	Output	Input

Figure 4-5. Read Modify Write Cycle of Multiple-Bit Device



<1> Defines row address.
<2> Activates $\overline{RAS}$ to latch row address.
<3> Defines column address.
<4> Activates $\overline{CAS}$ to latch column address.
<5> Activates $\overline{OE}$ to enable output buffer.
<6> Start of data output.
<7> Activates $\overline{WE}$ to enable input buffer.
<8> Sets input data.

$\overline{RAS}$	Active	
$\overline{CAS}$	Active	
$\overline{WE}$	Inactive	Active
OE	Active	Don't care
I/O	Output	Input

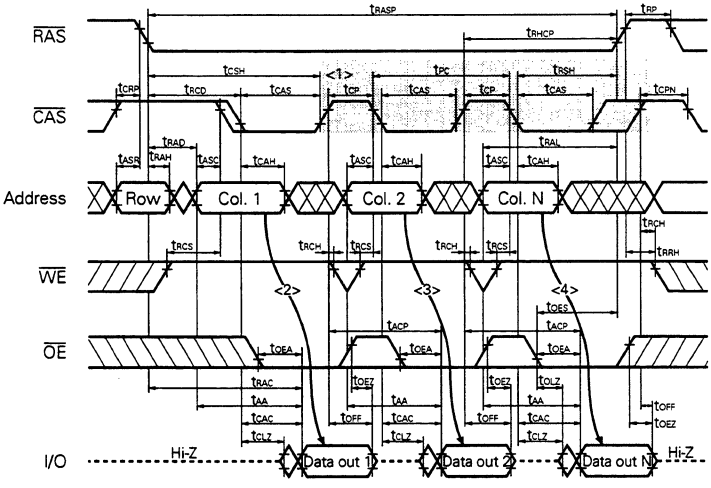
4.4 Page Mode

4.4.1 Fast page mode (FPM)

In the fast page mode (FPM), column addresses are latched by repeatedly activating and inactivating $\overline{CAS}$ after $\overline{RAS}$ has been activated and the row address has been latched. This mode is available for read/write or read modify write operations and allows the simultaneous use of read and write operations.

Taking the read operation as an example, during normal read operations, data can be output only once during each $\overline{RAS}$ cycle, while in the fast page mode, data can be output repeatedly. For this reason, during read operation in the fast page mode, the access time of the data output first (data output 1) is the same as the access time of normal read cycles, but the access time of the second and later data output (data output 2, data output N) becomes successively faster.

Figure 4-6. Fast Page Mode Read Cycle



<1> ▒▒▒▒: $\overline{CAS}$ toggle operation (operation to repeat activating and inactivating)
<2> Data output 1 corresponding to column address 1
<3> Data output 2 corresponding to column address 2
<4> Data output N corresponding to column address N

4.4.2 Access time in fast page mode

The access time in the fast page mode varies depending on the conditions shown in Table 4-4.

Table 4-4. Access Time in Fast Page Mode Read Cycle

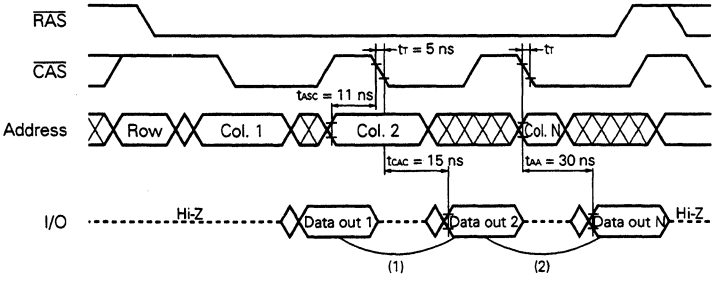
	Conditions	Valid access time
(1)	$t_{ASC} \geq (t_{AA\ (MAX.)} - t_T - t_{CAC\ (MAX.)})$	$t_{CAC\ (MAX.)}$
(2)	$t_{ASC\ (MIN.)} \leq t_{ASC} < (t_{AA\ (MAX.)} - t_T - t_{CAC\ (MAX.)})$	$t_{AA\ (MAX.)}$

Assuming that the specification in Table 4-5, an example in Table 4-4 is shown below (t_T = 5 ns).

Table 4-5. Specification of a Certain Memory (for fast page mode)

	MIN.	MAX.	Unit
t_{AA}	–	30	ns
t_{CAC}	–	15	
t_{ASC}	0	–	

Figure 4-7. $\overline{CAS}$ Access and Address Access



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

(1) When t_{CAC} becomes valid ($\overline{CAS}$ access):

Data are output in 31 ns ($t_{ASC} + t_T + t_{CAC}$) after the column address is defined and in 15 ns after $\overline{CAS}$ is activated.

(2) When t_{AA} becomes valid (address access):

Data are output in 30 ns after column address is defined and in 25 ns ($t_{AA} - t_T$) after $\overline{CAS}$ is activated (in the case of t_{ASC} = 0 ns).

4.4.3 Hyper page mode (HPM)

Hyper page mode (HPM) is one type of page modes and is equivalent to EDO. The following describes main features of hyper page mode in relation to how it differs from the fast page mode (FPM).

(1) Data output time is extended

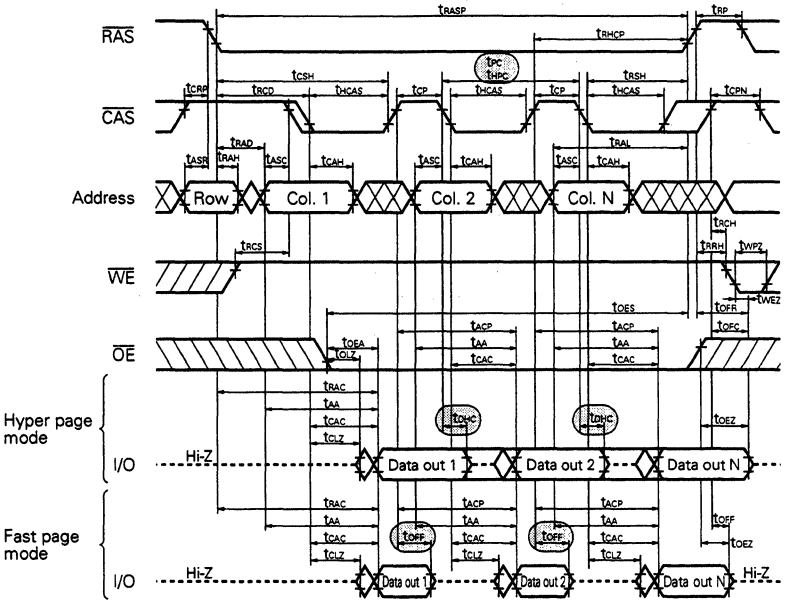
In hyper page mode, output data are held until the falling of the next $\overline{CAS}$ cycle rather than the rising of $\overline{CAS}$ to extend data output time (extended data out function). In normal fast page mode, data output time is reduced when $\overline{CAS}$ cycle time is shortened. However, in hyper page mode, the extended data out function increases the timing margin at the reading side even if the $\overline{CAS}$ cycle time becomes shorter.

(2) Further shortening in $\overline{CAS}$ cycle time (t_{HPC}) as compared with fast page mode

According to (1) above, the $\overline{CAS}$ cycle time can be further shortened in the hyper page mode as compared with the fast page mode if the timing margin at the reading side is the same. For example, the $\overline{CAS}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns for a device with t_{RAC} = 60 ns.

In hyper page mode, read operation (data output) and write operation (data input) can be repeatedly executed during one $\overline{RAS}$ cycle as in fast page mode. The read and write operations can exist at the same time with the performance being equivalent to that of the fast page mode.

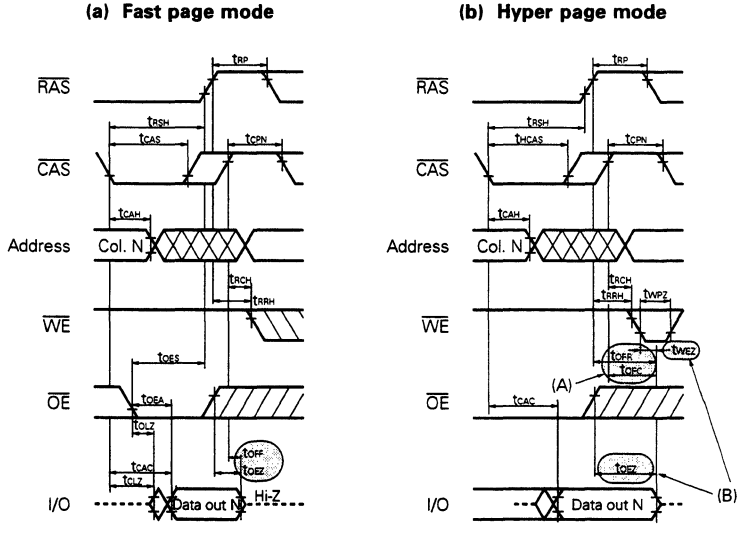
Figure 4-8. Hyper Page Mode Read Cycle



4.4.4 I/O Hi-Z state

In page mode, when I/O is set to Hi-Z state in read cycle, valid signal specifications differ as shown below.

Figure 4-9. I/O Hi-Z State



(1) Fast page mode:

The t_{OFF} and t_{OEZ} are applied to set I/O to Hi-Z state and the faster becomes effective.

(2) Hyper page mode:

The $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ need to be controlled as follows to set I/O to Hi-Z state. Valid signal specifications differ depending on the state of each signal.

- Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
  $\overline{WE}$: inactive, $\overline{OE}$: active
  t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
  t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
- Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
  $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
- Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
  $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
- $\overline{WE}$: inactive (in read cycle)
  $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
  $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

In short,

(A) The slower of t_{OFR} and t_{OFC} becomes effective.

(B) The faster of t_{WEZ} and t_{OEZ} becomes effective.

Please note that I/O will not become Hi-Z state even if $\overline{CAS}$ changes from active to inactive in case of hyper page mode with $\overline{RAS}$: active, $\overline{WE}$: inactive and $\overline{OE}$: active.

4.4.5 Access time in hyper page mode

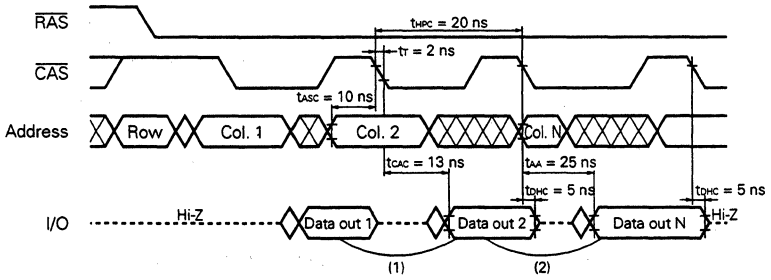
When t_{AA} is applied in the hyper page mode, t_{HPC} cannot be operated at the minimum value (See **4.4.2 Access time in fast page mode** for $\overline{CAS}$ access and address access).

Assuming that the specification in Table 4-6, an example in Figure 4-10 is shown below (t_T = 2 ns).

Table 4-6. Specification of a Certain Memory (for hyper page mode)

	MIN.	MAX.	Unit
t_{HPC}	20	–	ns
t_{AA}	–	25	
t_{CAC}	–	13	
t_{ASC}	0	–	
t_{DHC}	5	–	

Figure 4-10. $\overline{CAS}$ Access and Address Access (for hyper page mode)



Remark $\overline{WE}$: inactive, $\overline{OE}$: active

(1) When t_{CAC} becomes valid ($\overline{CAS}$ access):

Data output time is equal to 10 ns when t_{HPC} is set to the minimum value.

Data output time: $(t_{HPC} - t_T - t_{CAC}) + t_{DHC} = (20 - 2 - 13) + 5 = 10$ ns

(2) When t_{AA} becomes valid (address access):

Data output time is equal to 0 ns when t_{HPC} is set to the minimum value and hence 10 ns cannot be secured.

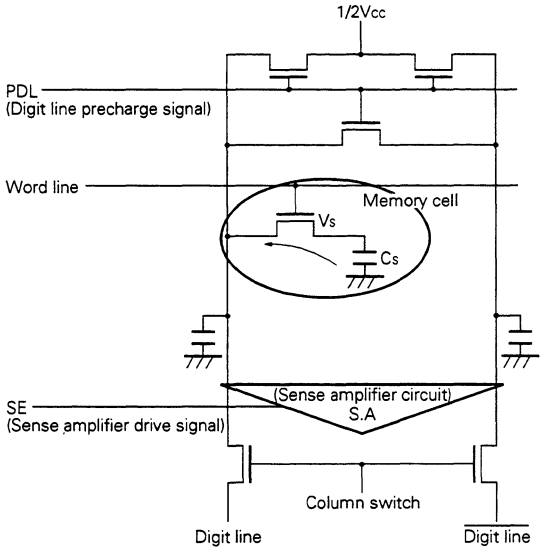
Data output time: $(t_{HPC} - t_{AA}) + t_{DHC} = (20 - 25) + 5 = 0$ ns

Therefore, t_{HPC} needs to be set to 30 ns (address access) or t_{ASC} needs to be set to 10 ns ($\overline{CAS}$ access) to secure 10 ns data output time.

CHAPTER 5 INTERNAL MEMORY OPERATION

This chapter describes the internal operation of memory devices, taking read cycles as an example.

Figure 5-1. Simplified Diagram of Internal Memory



Let us assume that the high level (= 5.0 V) is held by the capacitor in the memory cell and is to be output to the outside of the memory (read operation). When $\overline{RAS}$ is not activated, PDL (digit line precharge) is activated and the digit lines and $\overline{\text{digit lines}}$ are at half of Vcc potential.

Assuming that the word line is selected with the row address, activating $\overline{RAS}$ makes PDL and the word line inactive and active, respectively, followed by SE (sense amplifier drive) being activated with some delay time. When PDL is inactivated, the digit lines and $\overline{\text{digit lines}}$ are separated.

When the word line is activated, the transistor (Vs) is turned on, transferring electric charges in the capacitor (Cs) to the digit line. Then, the potential of the digit line becomes 1/2 Vcc + α, resulting in some voltage difference (=α) between the digit lines and $\overline{\text{digit lines}}$. The difference is amplified by the sense amplifier to 5.0 V and 0 V. When the capacitor (Cs) holds the low level (= 0 V), the reverse operation is performed (i.e., Digit line = 1/2 Vcc – α and $\overline{\text{Digit lines}}$ = 1/2 Vcc. The potential difference is amplified). The column switch is controlled with $\overline{\text{CAS}}$.

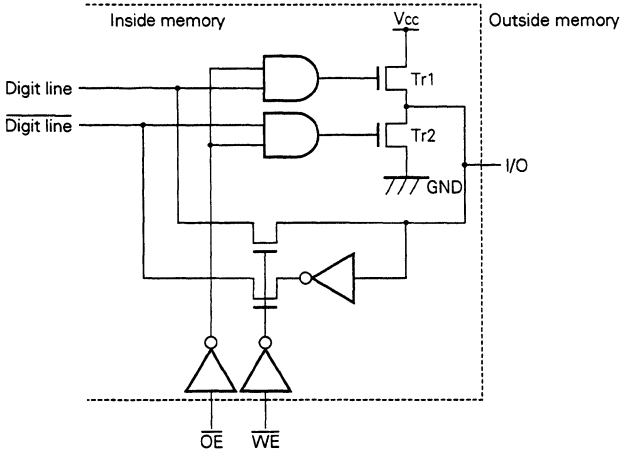
When $\overline{\text{CAS}}$ is inactivated, the column switch is inactivated. When $\overline{\text{RAS}}$ is inactivated, the transistor (Vs) is turned off, SE is inactivated, and PDL is activated. The digit lines and $\overline{\text{digit lines}}$ amplified by the sense amplifier to 5.0 V and 0 V gradually reach 1/2 Vcc.

The time it takes for the digit lines and $\overline{\text{digit lines}}$ to change from 5.0 V and 0 V to 1/2 Vcc at this time is the $\overline{\text{RAS}}$ precharge time (t_{RP}). When the $\overline{\text{RAS}}$ precharge time runs short, the sense amplifier may malfunction because the next operation (the transistor (Vs) is turned on) is made without causing the digit lines and $\overline{\text{digit lines}}$ to reach 1/2 Vcc.

Digit lines are connected to the transistors at the output stage. The transistors are controlled with $\overline{\text{OE}}$ ($\overline{\text{WE}}$ in write operation).

- When Tr1 = ON and Tr2 = OFF, the high level is output.
- When Tr1 = OFF and Tr2 = ON, the low level is output.

Figure 5-2. Simplified Diagram of Memory Output Stage



CHAPTER 6 REFRESH

This chapter describes the refresh operation, taking the μPD42S16160 (1M words x 16 bits) as an example.

6.1 Refresh Cycles and Distributed/Burst Refresh

The refresh cycle of the μPD42S16160 is 4,096/128 ms.

This expression means that 4,096 refresh cycles are required during each 128 ms interval. The requirement should be strictly observed, otherwise data stored in memory may be destroyed.

Refresh can be executed in two ways.

(1) Distributed refresh:

Refresh cycles are executed at intervals. In the case of the μPD42S16160, refresh cycles are executed every 31.3 μs (128 ms/4,096).

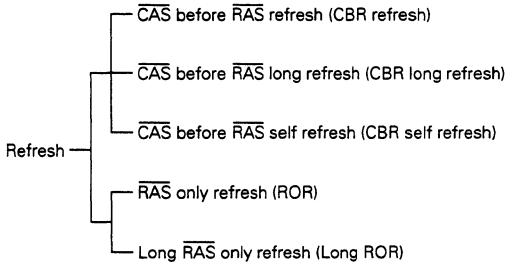
(2) Burst refresh:

Refresh cycles are executed in succession. In the case of the μPD42S16160, 4,096 refresh cycles are executed in succession.

6.2 Refresh Types

Refresh can be categorized into two main types and further into five sub-types as shown below.

Figure 6-1. Refresh Types



In normal (read/write) mode, CBR refresh, CBR long refresh, ROR, or long ROR are generally used; in data retain (with battery backup) mode, CBR self refresh is generally used.

6.3 Refresh Operation

This section describes refreshes used for DRAM. The control method for these refreshes and refresh cycle ratings are shown in Tables 6-1 and 6-2.

(1) CBR refresh:

Refresh is executed with (memory) external clock and (memory) internal address signals. In this case, the refresh cycle rating is 4,096/64 ms.

Addresses are generated by an internal counter which counts automatically. Therefore, 4,096 different addresses are generated automatically.

(2) CBR long refresh:

Refresh is executed with external clock and internal address signals. In this case, the refresh cycle rating is 4,096/128 ms. Compared with the CBR refresh (64 ms), the refresh period is longer (128 ms). Therefore, the number of refresh times per time interval is smaller than in the case of the CBR refresh, resulting in lower power consumption (lower average current consumption per time interval).

(3) ROR and long ROR:

Refresh is executed with external clock and external address signals. In this case, the refresh cycle rating is 4,096/64 ms (4,096/128 ms for long ROR). 4,096 different addresses must be created outside the memory.

(4) CBR self refresh:

Refresh is executed with internal clock and internal address signals. Memory executes refresh automatically under control of the internal clock (no refresh cycle). Therefore, CBR self refresh cannot be used when read and write operations are executed together and cannot be controlled externally.

Memories that can assure CBR self refresh can also assure CBR refresh, CBR long refresh, ROR, and long ROR.

Table 6-1. Refresh Control Methods

	Clock	Address
CBR refresh	External Clock	Internal Address
CBR long refresh		
ROR	External Clock	External Address
Long ROR		
CBR self refresh	Internal Clock	Internal Address

Table 6-2. Refresh Cycle Ratings

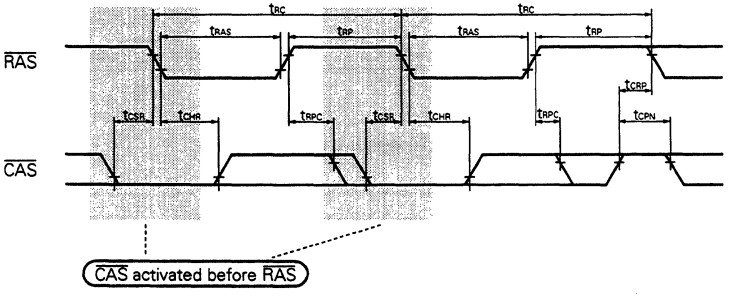
	DRAM with self refresh	DRAM without self refresh
Refresh cycle	4,096/128 ms	4,096/64 ms
CBR refresh	○	○
CBR long refresh	○	×
ROR	○	○
Long ROR	○	×
CBR self refresh	○	×

Remark ○: Assured, ×: Not assured

6.4 CBR Refresh, CBR Long Refresh Cycle

By activating $\overline{RAS}$ after $\overline{CAS}$ has been activated, the internal counter is activated and a row address is generated automatically. One row address is refreshed through this operation (in Figure 6-2, refresh is executed twice). Refresh is executed with the external clock and internal address signals.

Figure 6-2. CBR Refresh Cycle



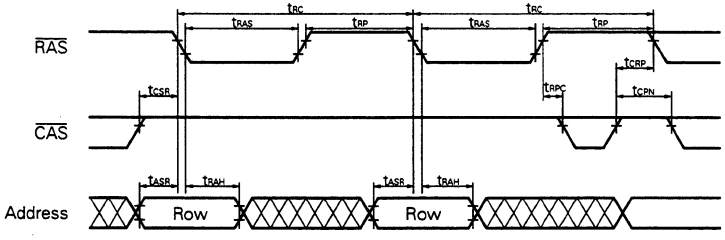
Remark Address, $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

Although the refresh period for the CBR long refresh cycle is longer than that of the CBR refresh cycle, its operation is exactly the same.

6.5 ROR and Long ROR Cycles

After $\overline{RAS}$ has been activated, the row address is latched and refresh is executed. Through this operation, refresh is completed for one row address.

Figure 6-3. ROR Cycle



Remark $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

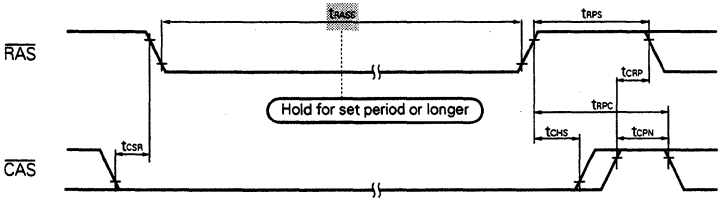
Although the refresh period for the long ROR refresh cycle is longer than that of the ROR refresh cycle, its operation is exactly the same.

6.6 CBR Self Refresh Cycle

6.6.1 Executing CBR self refresh

In the same way as for the CBR refresh cycle, after activating $\overline{CAS}$, activate $\overline{RAS}$. By keeping $\overline{RAS}$ activated for a set period ($t_{RASS\ (MIN.)}$ = 100 μs) or longer, the internal clock and the internal counter are activated and the memory repeatedly refreshes itself.

Figure 6-4. CBR Self Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: don't care I/O: Hi-Z

6.6.2 Cautions on use of CBR self refresh

CBR self refresh can be used independently when used in combination with distributed CBR long refresh; However, used in combination with burst CBR long refresh or with long ROR (both distributed and burst), the following cautions must be observed (For information on distributed and burst refresh, see **6.1 Refresh Cycles and Distributed/Burst Refresh**). The μPD42S16160 is used in the following example.

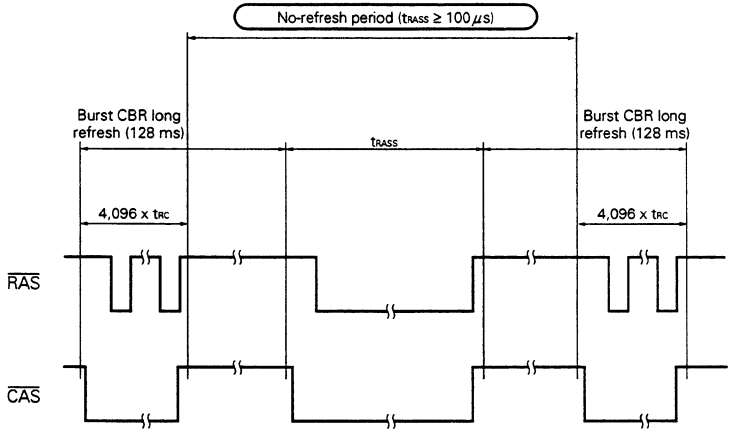
(1) Normal Combined Use of CBR Self Refresh and Burst CBR Long Refresh

Let us assume that CBR long refresh is used as shown in Figure 6-5. The $\overline{RAS}$ must be kept activated (= t_{RASS}) for 100 μs or longer to execute CBR self refresh (See **6.6.1 Executing CBR self refresh**).

In the CBR self refresh, it is not known how many seconds are required to refresh all memory cells. Therefore, if the CBR self refresh is stopped without refreshing all memory cells, an inactive period of up to approximately 2 t_{REF} occurs, the t_{REF} (= refresh time) requirement cannot be satisfied and data may be destroyed.

To prevent this from occurring, normally, when CBR self refresh and burst CBR long refresh are used in combination, execute CBR refresh for 4,096 times within 64 ms just before and after setting CBR self refresh. Through this CBR refresh, the period when any refresh is not executed will be within the t_{REF} requirement.

Figure 6-5. Example of Burst CBR Refresh Use

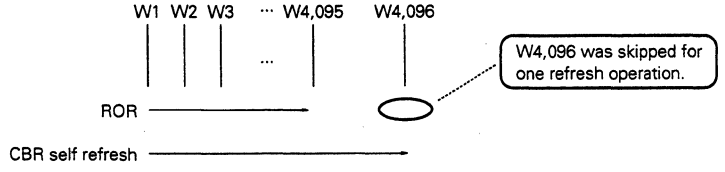


(2) Normal Combined Use of CBR Self Refresh and Burst Long ROR

The address control method for ROR and CBR refresh differ (ROR: Control from outside memory; CBR refresh: Control from inside memory).

Let us suppose that refresh is executed in the subsequence word line 1 (W1) to word line 2 (W2) with ROR. When refresh has been executed up to word line 4,095 (W4,095), CBR self refresh begins. At this time, if the internal counter (it cannot be controlled from the outside) happens to be set at word line 1 (W1), the refresh operation is executed in the subsequence word line 1 (W1) to word line 2 (W2). Under these conditions, an inactive period of up to approximately 2 tREF occurs for the word line 4,096 (W4,096) (See **CHAPTER 5 INTERNAL MEMORY OPERATION** and **6.8 Internal Memory Operation During Refresh**). Execute ROR 4,096 times within an interval of 64 ms or less just before entering or exiting CBR self refresh to satisfy the tREF requirement.

Figure 6-6. Example of ROR Use



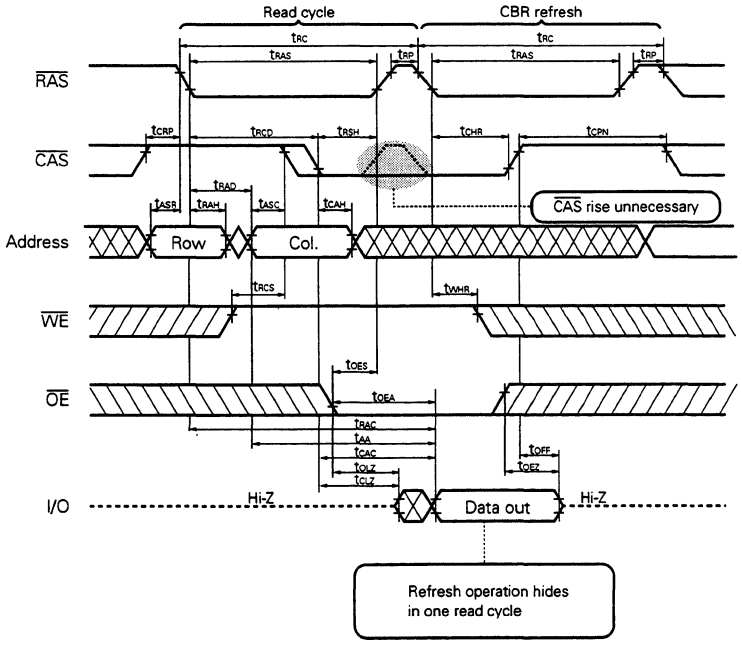
Remark W: Word line

6.7 Hidden Refresh Cycle

If CBR refresh cycle is started after a read/write cycle or read modify write cycle operation, it is possible to enter CBR refresh cycle with $\overline{CAS}$ activated.

Hidden refresh read cycle is shown in Figure 6-7 as an example.

Figure 6-7. Hidden Refresh Read Cycle



6.8 Internal Memory Operation During Refresh

This section explains how the memory operates during refresh using Figure 6-8 as an example.

As explained in **CHAPTER 5 INTERNAL MEMORY OPERATION**, when $\overline{RAS}$ is activated, a word line is selected and activated. The charge in the memory cell connected with this word line is transmitted to the digit line. The signal voltage difference generated at this time is amplified by the sense amplifier. Refresh consists of the above sequence of actions.

Figure 6-8. Simplified Circuit Diagram of 16-bit DRAM

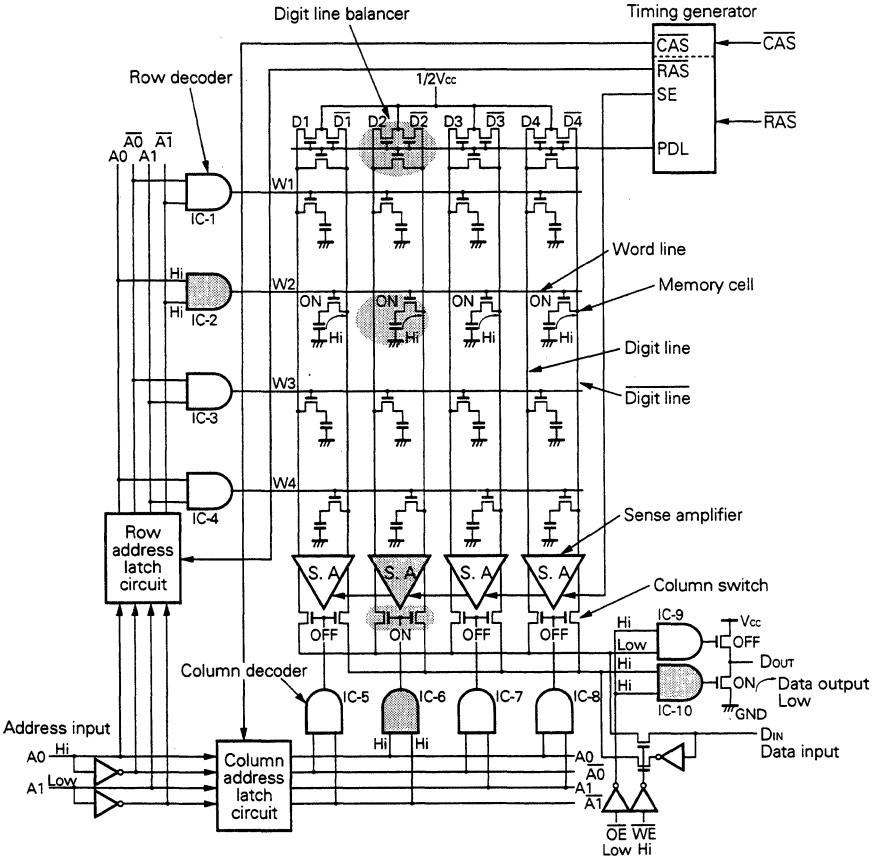


Figure 6-8 shows 16-bit DRAM (DRAM with 16 memory cells).

Let us suppose that the high level and the low level are input to the addresses A0 and A1, respectively, to select the word line (W2) while the high level is retained for all memory cells. Then, the IC-2 becomes the high level, the word line 2 (W2) is selected and activated, and all memory cells connected to it are refreshed (Because the output of the IC-6 is also at the high level, the column switch connected to the digit line 2 (D2, $\overline{D2}$) is activated. However, because the column address latch circuit is inactivated by refresh, all column switches are off.). Therefore, all memory cells are refreshed by selecting all word lines.

In a memory device with 4,096/128 ms refresh cycle, execution of read/write cycle at 4,096 different kinds of addresses is equivalent to refresh.

6.8.1 Not cell and true cell

Even if data within a memory cell are read after refresh fails and all data are destroyed, they are not always at the low level. The following provides an any explanation.

There are two types of memory cells, namely Not cell and True cell.

(1) Not Cell

The Not cell causes the data retention state of a memory cell to be reversed from the data input from the outside of memory or output to the outside of memory.

In Figure 6-8, when the output of the IC-2 and IC-6 reaches the high level, the column switches connected to the word line 2 (W2) and digit lines 2 (D2, $\overline{D2}$) becomes active, and digit line and $\overline{\text{digit line}}$ become the low level and high level, respectively. For read operation, the output of IC-10 becomes the high level, the transistor at the ground side is turned on, and hence a low-level signal is output from DOUT although the memory cell retains the high level because $\overline{WE}$ is inactive and $\overline{OE}$ is active.

Therefore, the output becomes the low level when the Not cell retains the high level at the memory cell and the high level when it retains the low level. The same applies to write operation. When a low level signal is input, the memory cell retains the high level. On the other hand, when the high level is input, it retains the low level.

(2) True Cell

The True cell causes the data retention state of a memory cell to be equal to the data input from the outside of memory or output to the outside of memory. The True cell causes the output to be the high level when the high level is retained at the memory cell and to be the low level when the low level is retained. The same applies to write operation.

In Figure 6-8, the memory cell connected to the word lines 2 and 4 (W2, W4) is Not cell and that connected to the word lines 1 and 3 (W1, W3) is True cell. The following table summarizes the I/O data state and data retention state of memory cell of Not and True cells.

Table 6-3. I/O Data State and Memory Cell Data Retention State

	I/O Data State	Data Retention State of Memory Cell
Not Cell	High level	Low level
	Low level	High level
True Cell	High level	High level
	Low level	Low level

According to the above, even if data are destroyed without observing refresh cycle (tREF) and electric charge is lost from the memory cell, the data output from the inside of the memory is not always at the low level. Also, the high level cannot always be retained even if a high level signal is input from the outside of memory to all memory cells.

The above is designed to minimize the interference between adjacent memory cells. In an actual device, the True and Not cells are aligned carefully, namely the True and Not cells are not always aligned alternately. See **CHAPTER 5 INTERNAL MEMORY OPERATION** for basic internal memory operation.

6.9 DRAM Refresh Cycles

Various DRAM refresh cycles are shown in the table below.

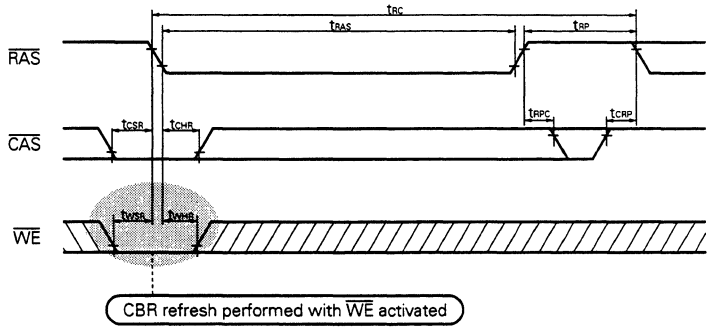
Table 6-4. Various DRAM Refresh Cycles

Density	Bit Organization	DRAM with Self Refresh Function	DRAM without Self Refresh Function
1 M	x 1	———	512/8 ms
	x 4		
4 M	x 1	1,024/128 ms	1,024/16 ms
	x 4		
	x 8		
	x 16	512/128 ms	512/8 ms
16 M	x 1	4,096/128 ms	4,096/64 ms
	x 4	2,048/128 ms	2,048/32 ms
	x 8		
	x 16	4,096/128 ms	4,096/64 ms
		1,024/128 ms	1,024/32 ms

CHAPTER 7 TEST MODE

By using the test mode, the test time can be reduced. The reason for this is that, in the case of 16M DRAM for example, the memory emulates the x 16-bit organization during test mode (In the case of 4M DRAM, the memory emulates the x 8-bit organization).

Figure 7-1. Test Mode Set Cycle ($\overline{WE}$, CBR Refresh Cycle)



Remark Address, $\overline{OE}$: don't care I/O: Hi-Z

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, CBR refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, in the case of 16M DRAM, the data are written to 16 bits of memory cell and in the case of 4M DRAM, the data is written to 8 bits of memory cell (independent data can be written to any input pin). The case of 16M DRAM is illustrated in the example below.

Write Operation during Test Mode for 16M DRAM

- x 1-bit devices: "0" or "1" input from D_{IN} is written sequentially to all 16 bits of memory cells.
- x 4-bit devices: "0" or "1" input from I/O1-I/O4 is written sequentially to all 16 bits of memory cells in four-bit units.

Next, when the data are read from the output pin at the same address, the memory cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

Refresh in the test mode must be performed with read/write cycle (See **6.8 Internal Memory Operation During Refresh**) or with the $\overline{WE}$, CBR refresh cycle. The $\overline{WE}$, CBR refresh cycle use the same counter as the CBR refresh's internal counter (See **6.3 Refresh Operation**).

(4) Mode Cancellation

The test mode is canceled by executing one cycle of ROR cycle or CBR refresh cycle.

[MEMO]

CHAPTER 8 BYTE CONTROL

Concerning DRAMs with x 16 bits or more, controlling I/O data in byte (8 bits) units is called byte control. The byte control mode can be used for read, write, or read modify write operation.

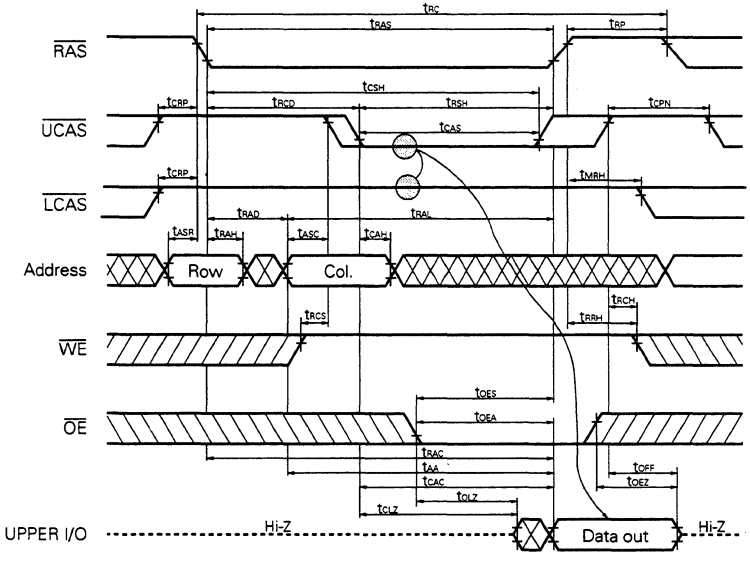
8.1 Byte Read/Write Mode

It is possible to read and write in byte units. Byte control is executed by the following two $\overline{\text{CAS}}$s.

- $\overline{\text{LCAS}}$ ($\overline{\text{LOWER CAS}}$) : Controls read/write operations for I/O1 to I/O8 (Lower I/O).
- $\overline{\text{UCAS}}$ ($\overline{\text{UPPER CAS}}$) : Controls read/write operations for I/O9 to I/O16 (Upper I/O).

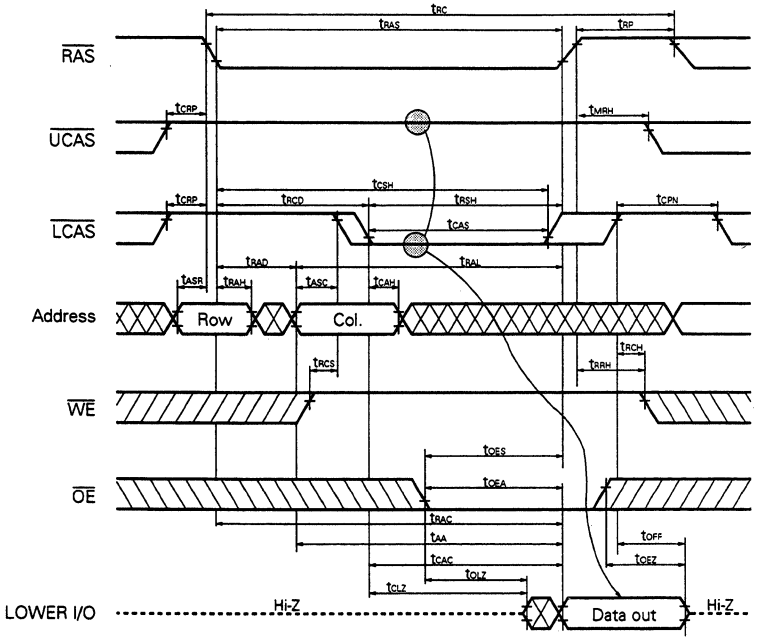
Figures 8-1 and 8-2 show examples controlled by $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$, respectively.

Figure 8-1. Upper Byte Read Cycle



Remark LOWER I/O: Hi-Z

Figure 8-2. Lower Byte Read Cycle



Remark UPPER I/O: Hi-Z

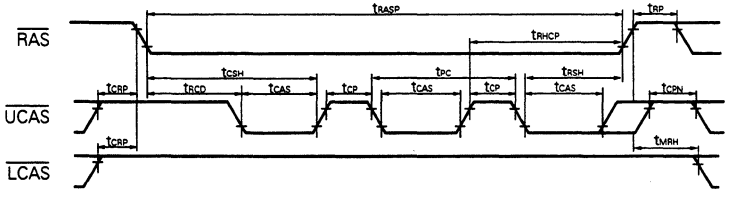
8.2 Page Mode of Byte Read/Write Mode

In the page mode, there are the following four types of control methods of I/O data according to the toggle operation (repeated operation of activation/inactivation) of $\overline{CAS}$ signal.

Table 8-1. Method for Controlling Byte Read/Write Mode

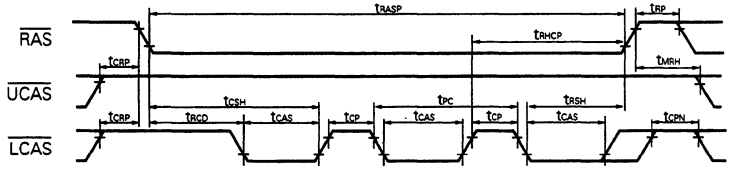
	$\overline{UCAS}$	$\overline{LCAS}$	I/O Data Control
(1)	Toggle operation	Inactive	8 bits
(2)	Inactive	Toggle operation	8 bits
(3)	Toggle operation	Toggle operation	16 bits
(4)	Toggle operation	Toggle operation	8 bits

(1) UPPER I/O Control



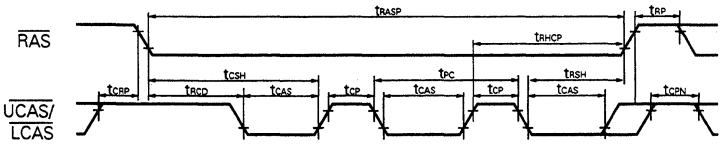
The $\overline{UCAS}$ is toggled while $\overline{LCAS}$ is inactive to control the UPPER I/O 8-bit data.

(2) LOWER I/O Control



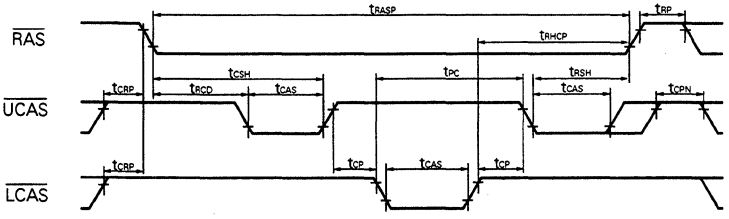
The $\overline{LCAS}$ is toggled while $\overline{UCAS}$ is inactive to control the LOWER I/O 8-bit data.

(3) All I/O Control



The $\overline{UCAS}$ and $\overline{LCAS}$ are toggled simultaneously to control UPPER I/O and LOWER I/O (all I/Os) 16-bit data.

(4) Mixed Control of UPPER I/O and LOWER I/O



The $\overline{UCAS}$ and $\overline{LCAS}$ are toggled in a mix to control each 8-bit data of UPPER I/O and LOWER I/O (No alternate control is required).

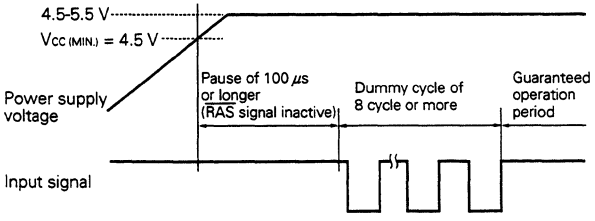
Remark In the page mode, read, write, and read modify write can be used in a mix by continuing $\overline{CAS}$ signal during the same $\overline{RAS}$ cycle.

CHAPTER 9 INITIALIZING

After turning on, the state of internal DRAM circuits is not known. It is therefore necessary to initialize them to ensure normal operation.

When turning on power, allow a 100-μs or longer pause ($\overline{RAS}$ signal inactive) and then be sure to execute eight or more ROR or CBR refresh cycles as dummy cycles to initialize the internal circuits.

Figure 9-1. Initializing



Remark This dummy cycle of 8 cycles or more is just a dummy cycle and does not guarantee refresh operation.

Unless initializing is executed accurately, the memory may not operate properly even during guaranteed operation period.

[MEMO]

CHAPTER 10 LOW VOLTAGE OPERATION

DRAM are divided into 5.0-V operation devices and low-voltage operation devices. The main differences between 5.0-V and low-voltage operation devices are shown in Table 10-1 using 16M DRAM (X 16-bit device) as an example.

Table 10-1. Main Differences between 5.0-V and Low-Voltage Operation Devices

	5.0-V Operation Devices	Low-voltage Operation Devices
Part number	μPD42S16160-60	μPD42S16160L-A60
Power supply voltage	5.0 V ± 10 % (4.5 V to 5.5 V)	3.3 V ± 0.3 V (3.0 V to 3.6 V)
Input voltage	V_{IH} = 2.4 V to V_{CC} + 1.0 V V_{IL} = −1.0 V to +0.8 V	V_{IH} = 2.0 V to V_{CC} + 0.3 V V_{IL} = −0.3 V to +0.8 V
Output voltage	V_{OH} = 2.4 V/V_{OL} = 0.4 V	V_{OH} = 2.4 V/V_{OL} = 0.4 V
Operating current	100 mA	90 mA
CBR self refresh current (data-retention current)	250 μA	150 μA
Pin configuration	Same	

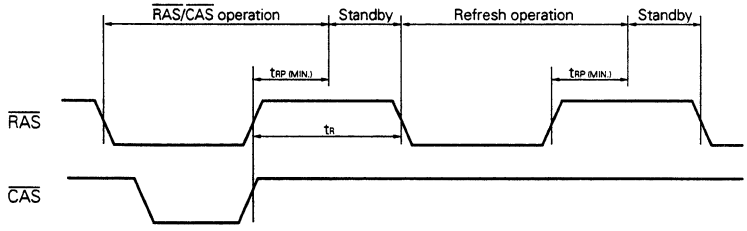
The 5.0-V operation devices of 16M DRAM all adopt an internal voltage-drop circuit. The internal voltage-drop circuit causes the power supply voltage (5.0 V) supplied to the memory externally to be dropped inside the memory and 5.0-V operation devices also operate on 3.3 V inside the memory. Therefore, there is almost no difference between the current consumption of the 5.0-V operation device and that of the low-voltage operation device. The low-voltage operation device of 16M DRAM does not adopt any internal voltage-drop circuit.

[MEMO]

CHAPTER 11 CURRENT CONSUMPTION CALCULATION

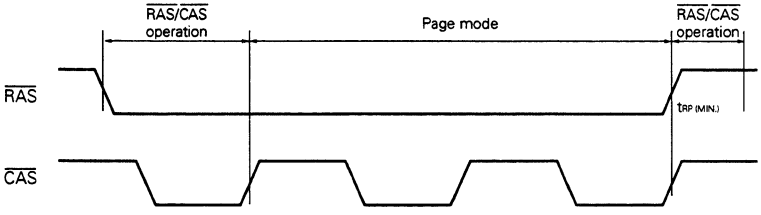
The following examples explains an approximate current consumption calculation according to timing.

(1) Example 1



In the example 1, after $\overline{RAS}/\overline{CAS}$ operation (read, write, or read modify write cycle) is executed first, refresh (ROR) is executed. When the $\overline{RAS}$ precharge time ($t_{RP\,(MIN.)}$) exceeds the specification ($t_R > T_{RP\,(MIN.)}$), standby current is applied.

(2) Example 2



The example 2 executes the page mode. In the first $\overline{CAS}$ cycle, $\overline{RAS}/\overline{CAS}$ operation is applied and the page mode is applied from the second $\overline{CAS}$ cycle or thereafter. The $\overline{RAS}$ precharge time ($t_{RP\,(MIN.)}$) when the page mode ends becomes the precharge of $\overline{RAS}/\overline{CAS}$ operation. Therefore, the $\overline{RAS}/\overline{CAS}$ operation is obtained by merging the first $\overline{RAS}$ active period and the $\overline{RAS}$ precharge period when the page mode ends.

When the timing shown in the example satisfies the conditions shown in Table 11-1 (extracted from data sheet), each current consumption (per unit time) is added.

Table 11-1. μPD4216160 DC Characteristics

Parameter	Symbol	Test Condition		MIN.	TYP.	MAX.	Unit
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns			100	
		I_O = 0 mA	t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} (MIN.), I_O = 0 mA				2	mA
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, I_O = 0 mA				1	
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} (MIN.)	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns			100	
			t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS}$ ≤ V_{IL} (MAX.), $\overline{CAS}$ Cycling	t_{RAC} = 50 ns			100	mA
		t_{PC} = t_{PC} (MIN.), I_O = 0 mA	t_{RAC} = 60 ns			90	
			t_{RAC} = 70 ns			80	
			t_{RAC} = 80 ns			70	
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns			110	mA
		t_{RC} = t_{RC} (MIN.)	t_{RAC} = 60 ns			100	
		I_O = 0 mA	t_{RAC} = 70 ns			90	
			t_{RAC} = 80 ns			80	
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10		+10	μA
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10		+10	μA
High level output voltage	V_{OH}	I_O = –2.5 mA		2.4			V
Low level output voltage	V_{OL}	I_O = +2.1 mA				0.4	V

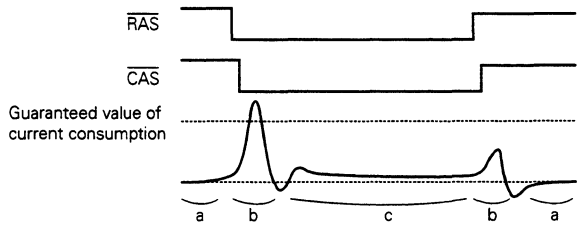
Current consumption varies depending on operating conditions (See **CHAPTER 12 MAIN DRAM CHARACTERISTICS** for the details). Appendix A shows the ratio and compensation which is required for each operating condition.

CHAPTER 12 MAIN DRAM CHARACTERISTICS

12.1 Current Consumption Waveform Diagram

In DRAM, as its name implies, consumption current flows more dynamically as compared with other memories. There is actually a peak current as shown in Figure 12-1.

Figure 12-1. Current Consumption Waveform Simplified Diagram of $\overline{RAS}/\overline{CAS}$ Cycle



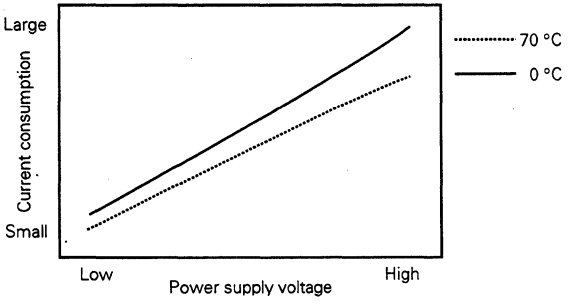
Period	Signal State	Current Consumption
a	$\overline{RAS}/\overline{CAS}$ = inactive	Almost 0
b	$\overline{RAS}/\overline{CAS}$ = from inactive to active or vice versa	Peak current
c	$\overline{RAS}/\overline{CAS}$ = inactive	Slight

When $\overline{RAS}$ changes from inactive to active state, the sense amplifier becomes active and hence current consumption is maximized at that instant (peak current). The guaranteed value indicates an average current consumption and hence the peak current may exceeds the guaranteed value.

As $\overline{RAS}/\overline{CAS}$ cycle becomes longer, the average current consumption becomes smaller.

12.2 Current Consumption Dependence on Power Supply Voltage

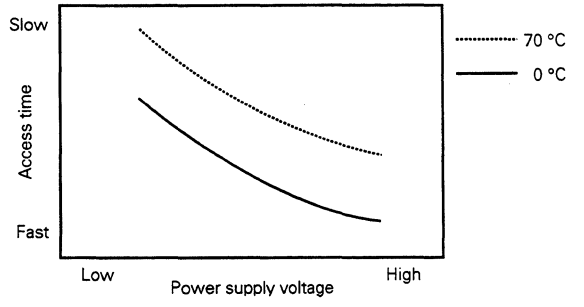
Figure 12-2. Current Consumption - Power Supply Voltage Characteristics



Current consumption decreases when the power supply voltage is reduced, and increases when the ambient temperature decreases. As ambient temperature decreases, resistance decreases and internal memory operation speeds up, resulting in increase in current consumption. The current consumption should be roughly estimated when the power supply voltage is higher (the worst case).

12.3 Access Time Dependence on Power Supply Voltage

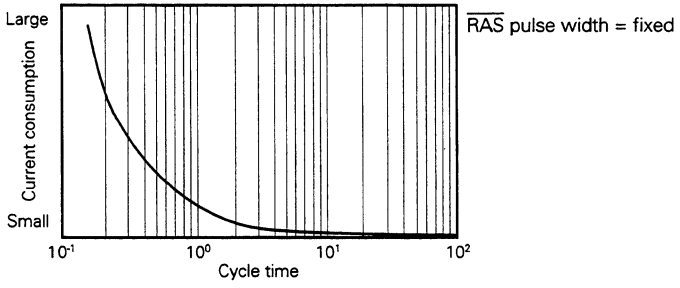
Figure 12-3. Access Time - Power Supply Voltage Characteristics



The access time is slower when the power supply voltage decreases, and is faster when the ambient temperature decreases. The access time should be roughly estimated when the power supply voltage is lower.

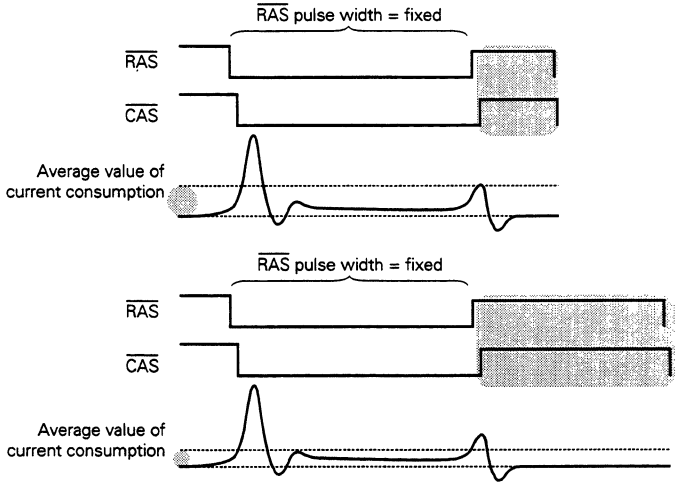
12.4 Current Consumption Dependence on $\overline{RAS}$ Cycle

Figure 12-4. Current Consumption - Cycle Time Characteristics



The current consumption per unit time is reduced as the cycle time becomes slower.

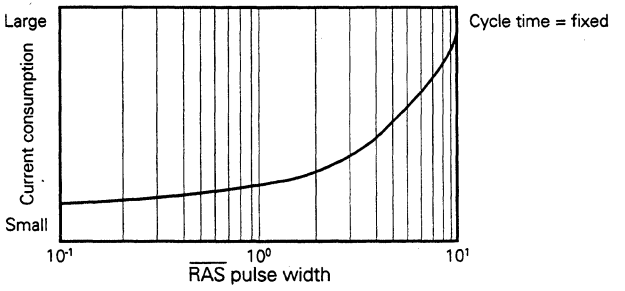
Figure 12-5. Average Current Consumption on Fixed $\overline{RAS}$ Pulse Width



Fixing the $\overline{RAS}$ pulse width and increasing the cycle time result in increasing the $\overline{RAS}$ precharge time. As the $\overline{RAS}$ precharge time becomes longer, the inactive time of $\overline{RAS}$ is extended and hence the average current consumption is reduced.

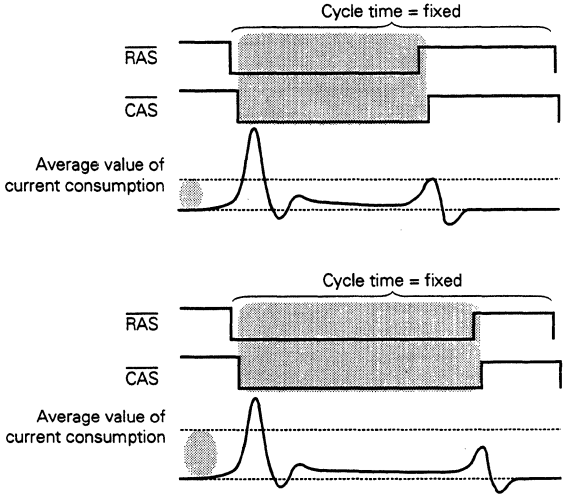
12.5 Current Consumption Dependence on $\overline{RAS}$ Pulse Width

Figure 12-6. Current Consumption - $\overline{RAS}$ Pulse Width Characteristics



As the $\overline{RAS}$ pulse width becomes longer, current consumption per unit time increases.

Figure 12-7. Average Current Consumption in Fixed Cycle Time

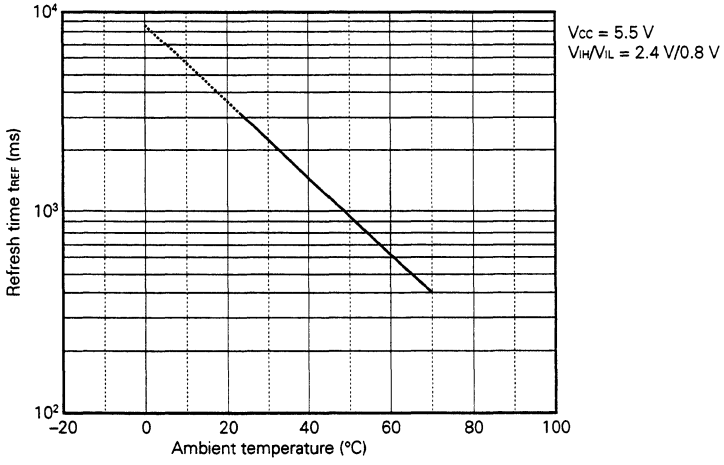


Fixing the cycle time and increasing the $\overline{RAS}$ pulse width result in reduction in the $\overline{RAS}$ precharge time. As the $\overline{RAS}$ pulse width is increased, the inactive time of $\overline{RAS}$ decreases and hence the average current consumption becomes larger.

12.6 Refresh Time Dependence on Ambient Temperature

Figure 12-8 shows the duration for which a high level can be read, supposing that the high level has been written and no refresh operation is performed.

Figure 12-8. Refresh Time - Ambient Temperature Characteristics



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

As ambient temperature rises, the leak in the capacitor tends to increase. In Figure 12-8, all memory cells (16,777,216 cells for 16M DRAM) are targeted rather than only one memory cell.

Therefore, the above figure indicates a point out of all memory cells where one or more data are destroyed.

12.7 Soft Error Rate (SER)

A memory can fail in the following two ways:

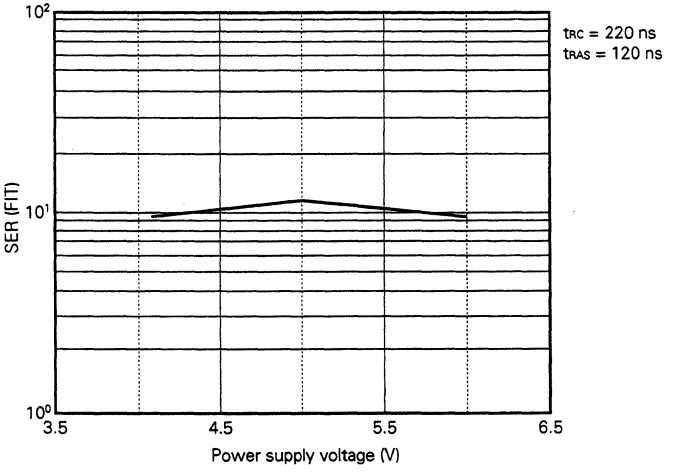
(1) The memory itself (hard) breaks due to application of some kind of stress.
(2) Data (soft) retained in the memory cell breaks.

Generally, a memory failure is due to (2) above.
Such a failure is called a soft error. Data are broken by alpha rays in the physical world. Data breakdown due to specification violation (any one of specifications listed in the data sheet is violated) is not included in category 2.

The soft error rate (SER) indicates the extent that data are broken under the above conditions and is normally expressed by FIT (Failure In Time). The FIT indicates the probability for failure per unit time, and 1 FIT is equal to 1×10^{-9} failures/time.

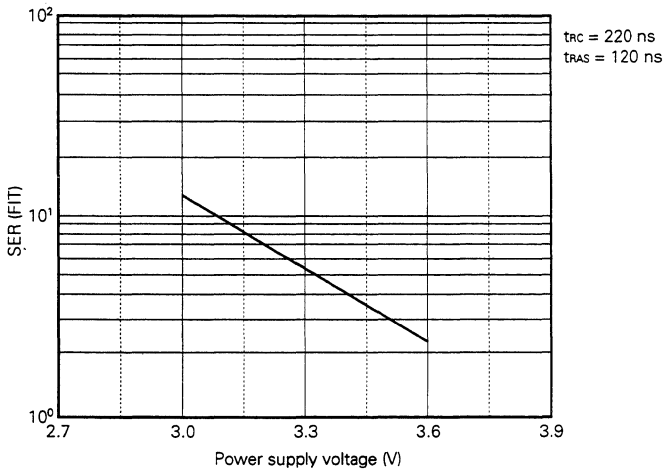
The FIT is a predicted value and varies depending on the memory usage conditions such as power supply voltage and access time and used environment such as ambient temperature.

Figure 12-9. Power Supply - SER Characteristics (5.0-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Figure 12-10. Power Supply - SER Characteristics (3.3-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Figure 12-11. $\overline{RAS}$ Cycle Time - SER Characteristics (5.0-V device)

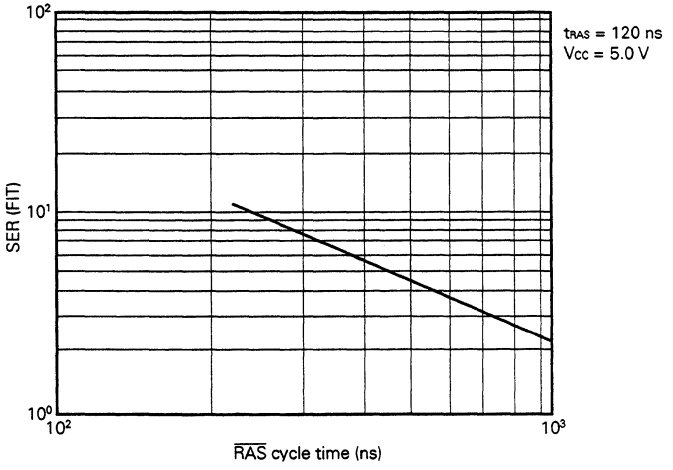
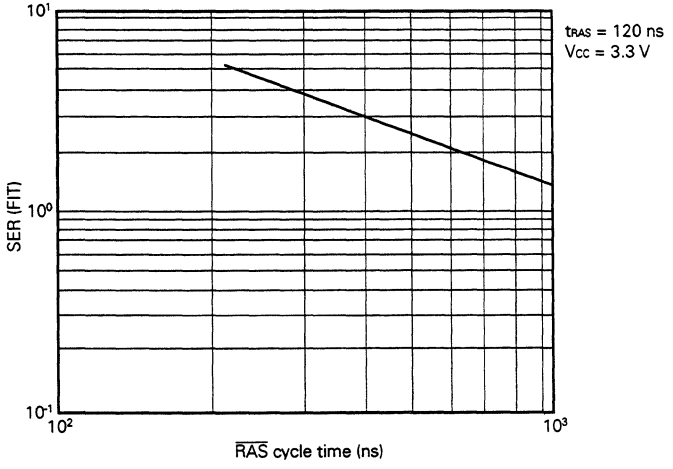


Figure 12-12. $\overline{RAS}$ Cycle Time - SER Characteristics (3.3-V device)



Remark The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

APPENDIX A DRAM DATA COLLECTION

The following shows the main characteristics of DRAM using 16M DRAM as an example.

The data were obtained by measurement using a sample extracted from a specific lot and do not indicate entire characteristics (they are not the assured values). Use them only for designing reference.

Normalization indicates the ratio of a value with a certain another value as 1.0.

A.1 Current Consumption Dependence on Power Supply Voltage

Figure A-1. I_{CC1}-V_{CC} Characteristics (3.3-V device)

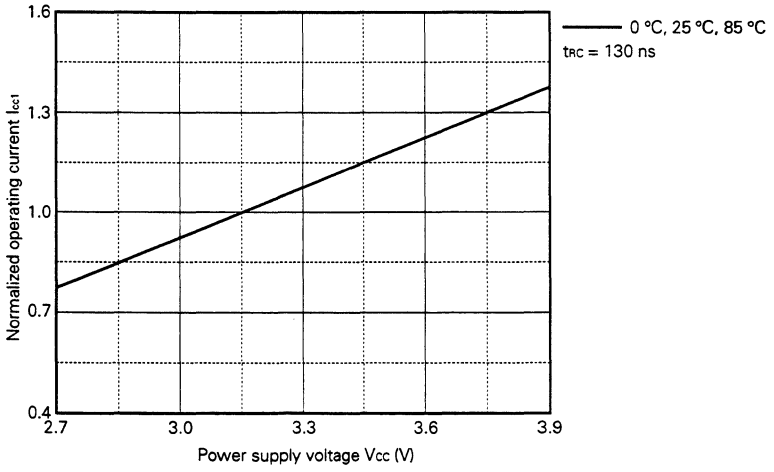
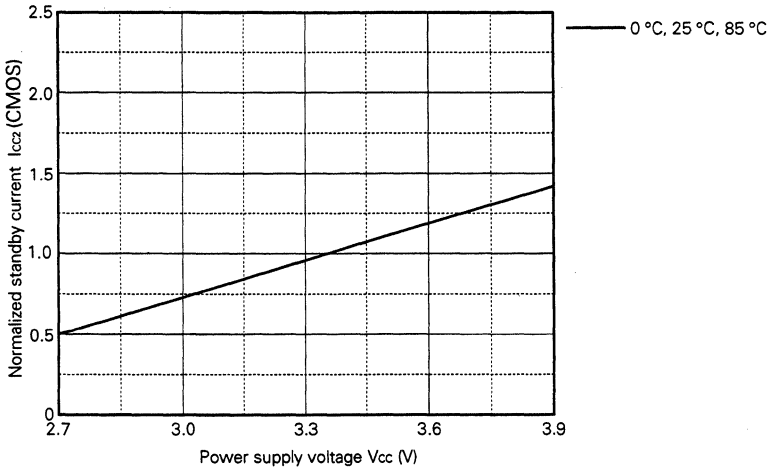


Figure A-2. I_{CC2}-V_{CC} Characteristics (3.3-V device)



Remark Standby refers to the memory condition where no operation is possible ($\overline{RAS}/\overline{CAS}$ inactive). Because, in the case of DRAM, refresh is required for retaining data, data cannot be retained in the standby mode.

Figure A-3. I_{CC3}-V_{CC} Characteristics (3.3-V device)

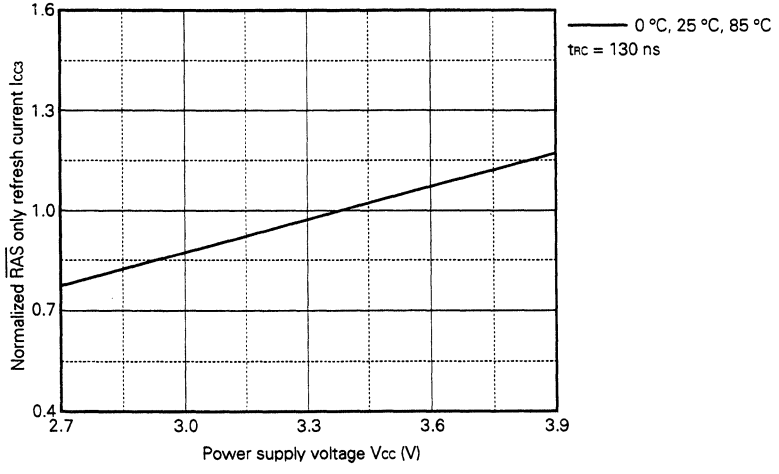


Figure A-4. I_{CC4}-Vcc Characteristics (3.3-V device)

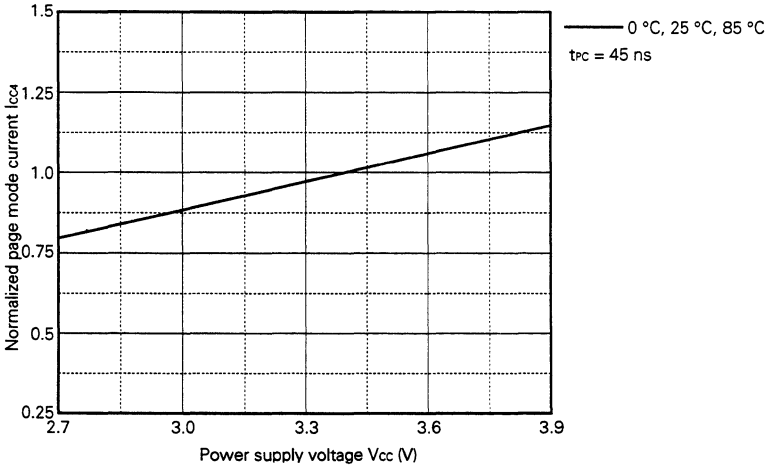


Figure A-5. I_{CC5}-Vcc Characteristics (3.3-V device)

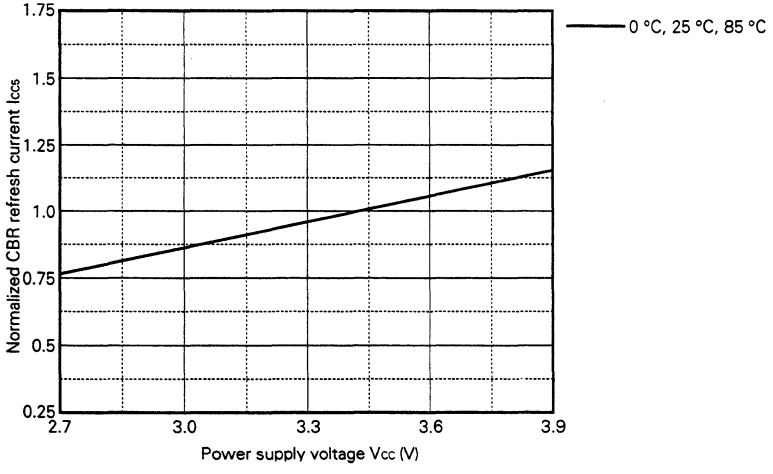


Figure A-6. I_{CC6}-V_{CC} Characteristics (3.3-V device)

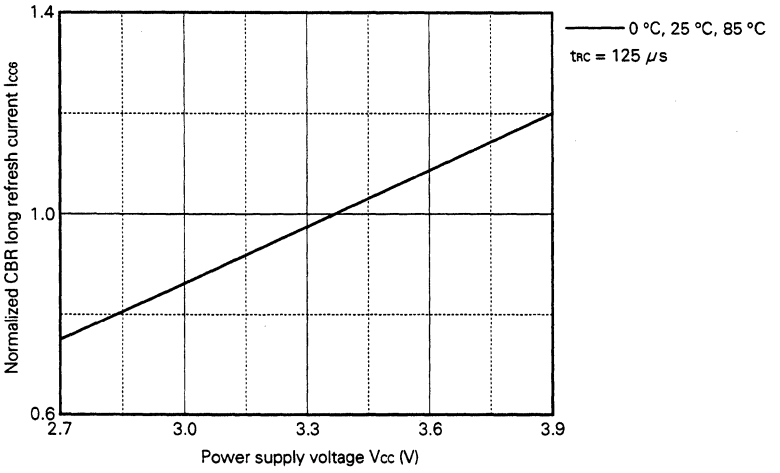


Figure A-7. I_{CC7}-V_{CC} Characteristics (3.3-V device)

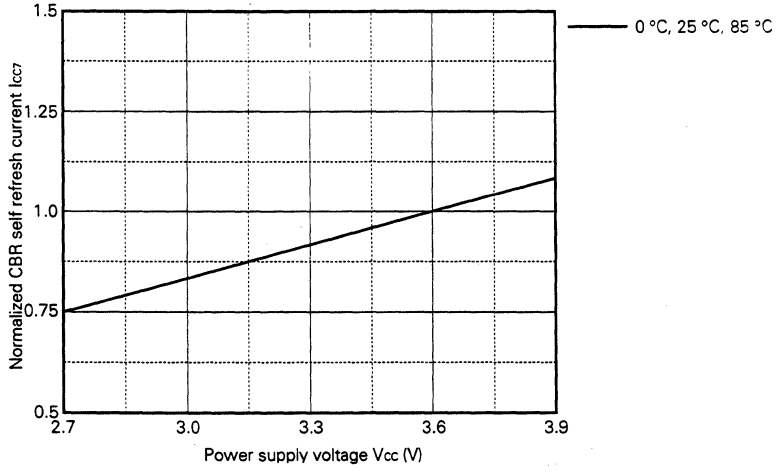


Figure A-8. I_{CC1}-Vcc Characteristics (5.0-V device)

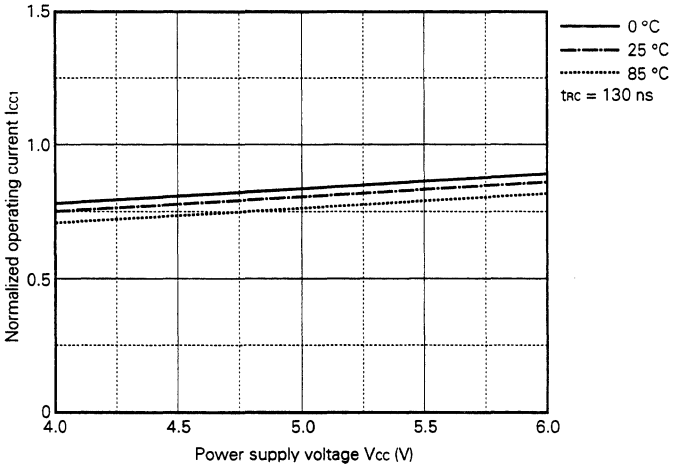
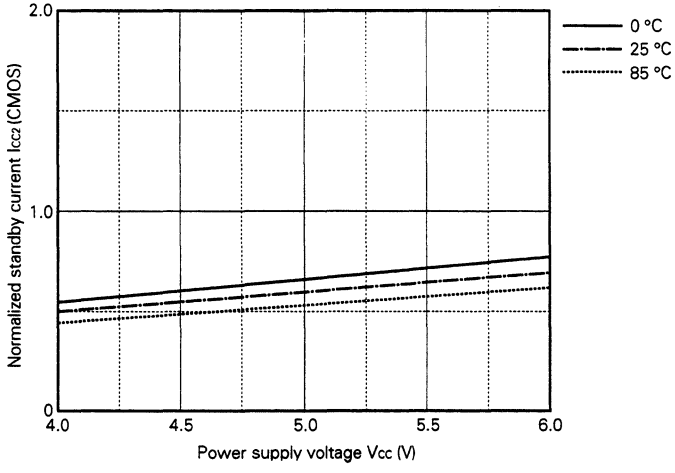


Figure A-9. I_{CC2}-Vcc Characteristics (5.0-V device)



Remark Standby refers to the memory condition where no operation is possible ($\overline{RAS}/\overline{CAS}$ inactive). Because, in the case of DRAM, refresh is required for retaining data, data cannot be retained in the standby mode.

Figure A-10. I_{CC3}-Vcc Characteristics (5.0-V device)

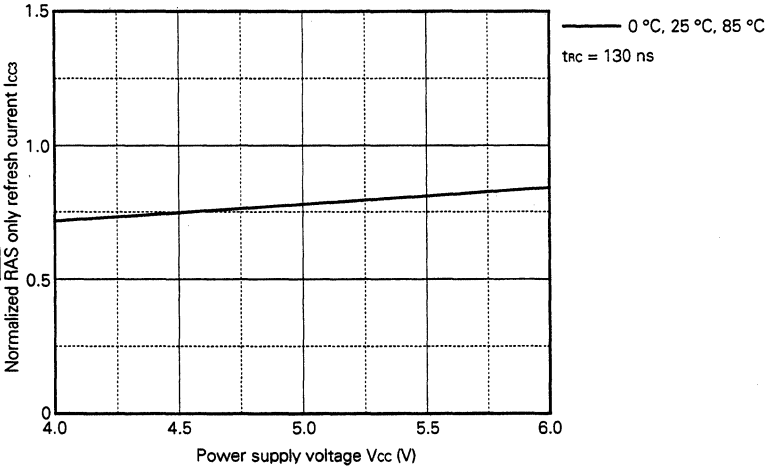


Figure A-11. I_{CC4}-Vcc Characteristics (5.0-V device, fast page mode)

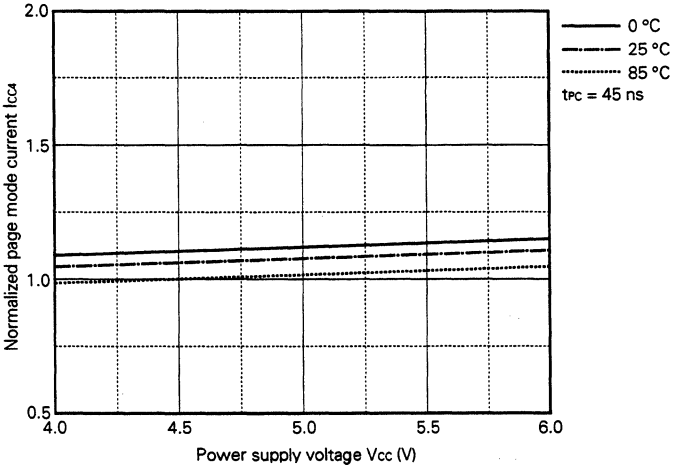


Figure A-12. I_{CC4}-V_{CC} Characteristics (5.0-V device, hyper page mode)

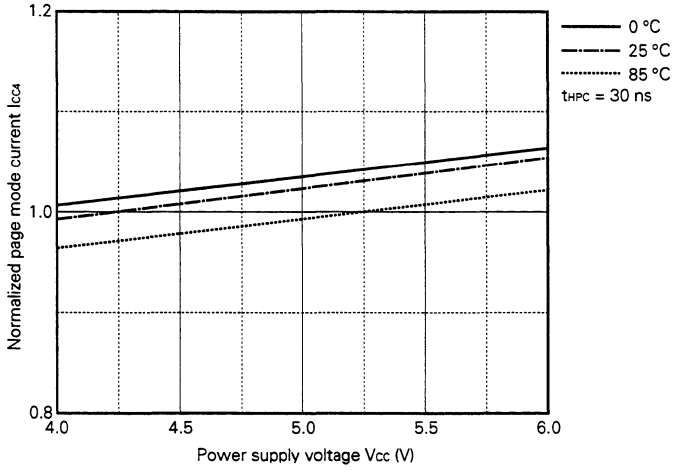


Figure A-13. I_{CC5}-V_{CC} Characteristics (5.0-V device)

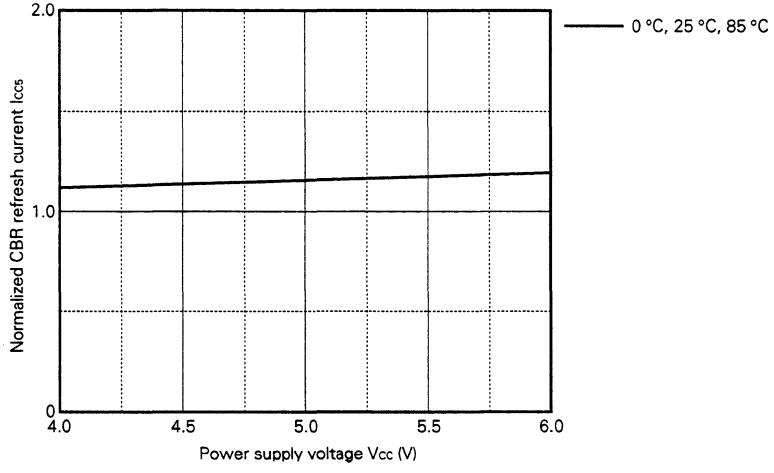


Figure A-14. I_{CC6}-Vcc Characteristics (5.0-V device)

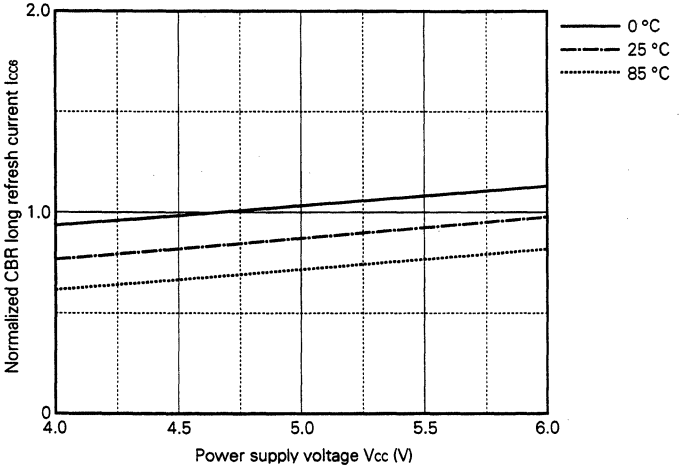
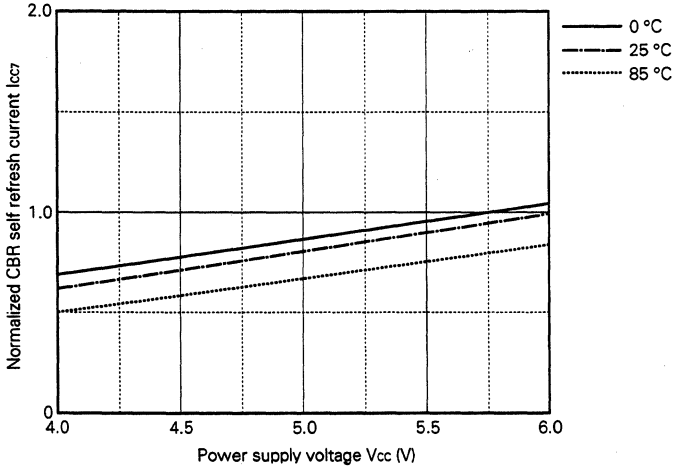


Figure A-15. I_{CC7}-Vcc Characteristics (5.0-V device)



A.2 Access Time Dependence on Power Supply Voltage

Figure A-16. V_{CC}-t_{RAC} Characteristics (3.3-V device)

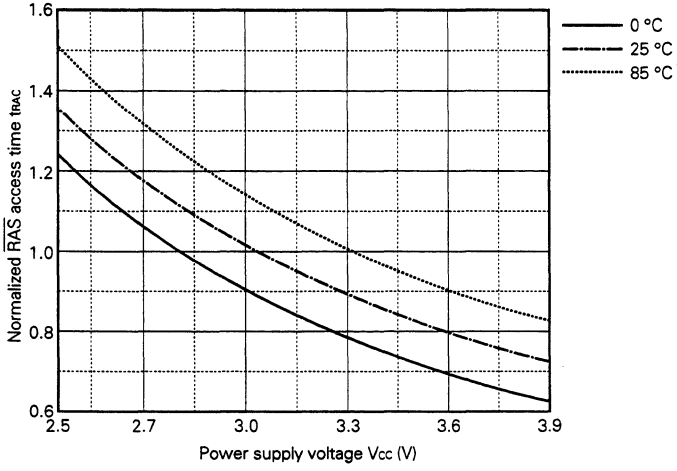


Figure A-17. V_{CC}-t_{CAC} Characteristics (3.3-V device)

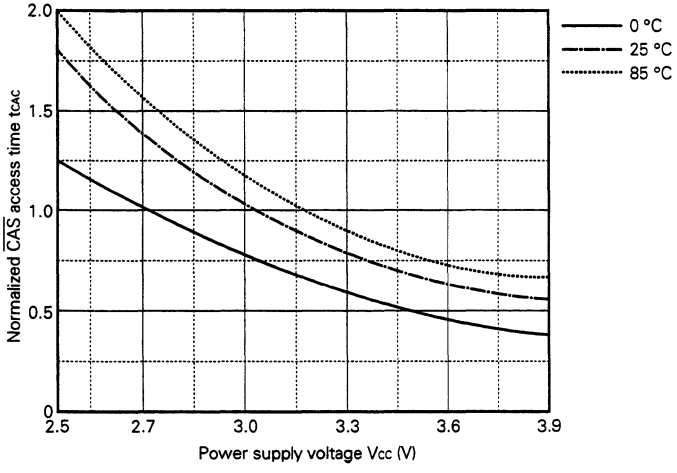


Figure A-18. Vcc-tAA Characteristics (3.3-V device)

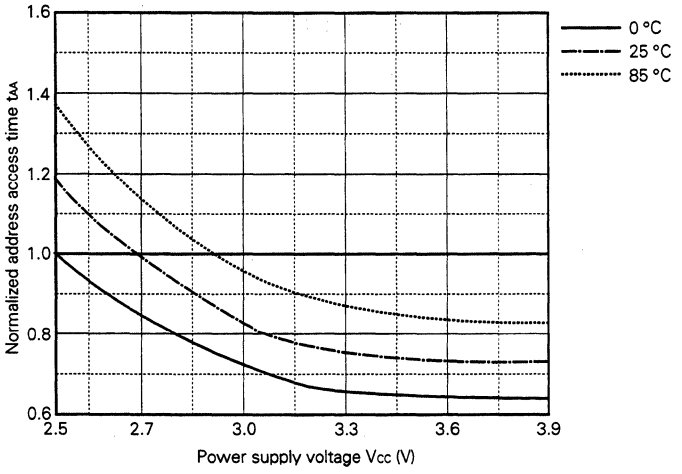


Figure A-19. Vcc-tACP Characteristics (3.3-V device)

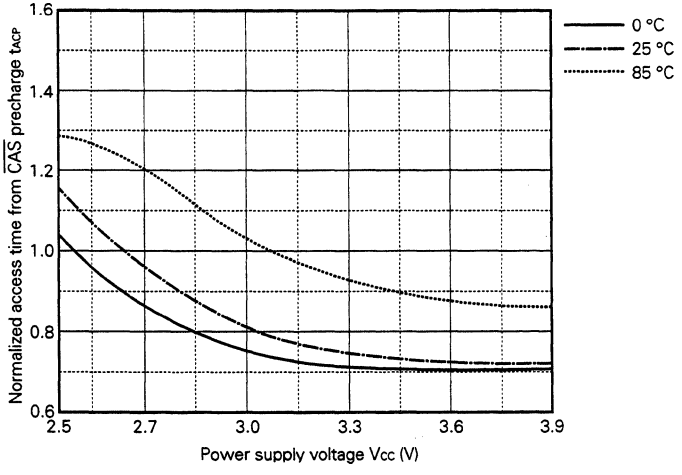


Figure A-20. V_{CC}-t_{OEA} Characteristics (3.3-V device)

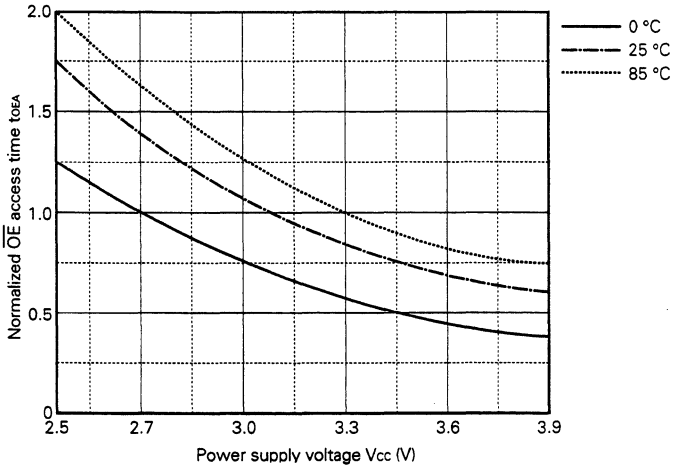
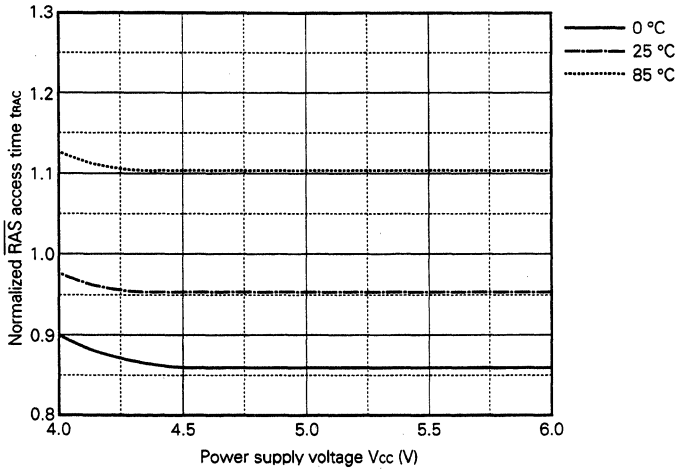


Figure A-21. V_{CC}-t_{RAC} Characteristics (5.0-V device)



The 5.0-V operation devices of 16M DRAM all adopt an internal voltage-drop circuit.

The internal voltage-drop circuit causes the power supply voltage (5.0 V) supplied to the memory externally to be dropped inside the memory and 5.0-V operation devices also operate on 3.3 V inside the memory. Therefore, there is almost no difference between the current consumption of a 5.0-V operation device and that of a low-voltage operation device. The low-voltage operation device of 16M DRAM does not adopt any internal voltage-drop circuit.

Figure A-22. V_{CC}-t_{CAC} Characteristics (5.0-V device)

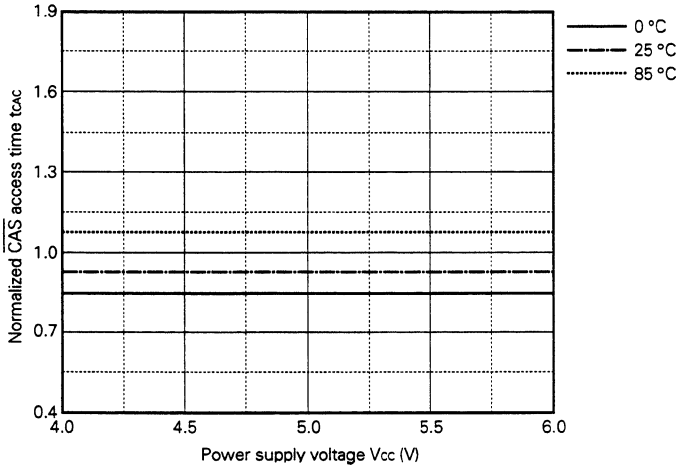


Figure A-23. V_{CC}-t_{AA} Characteristics (5.0-V device)

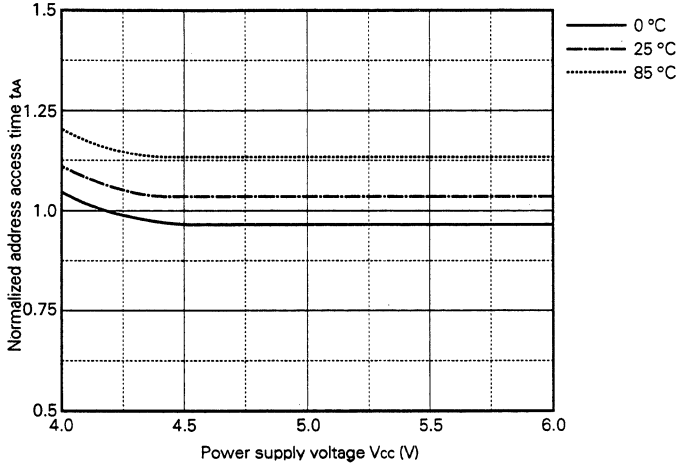


Figure A-24. V_{CC}-t_{ACP} Characteristics (5.0-V device)

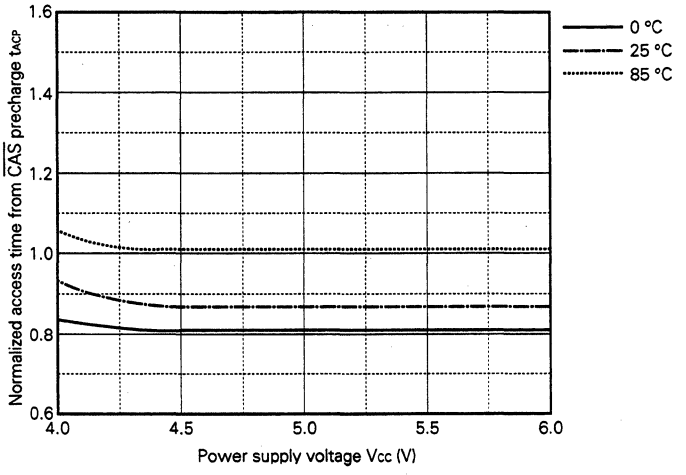
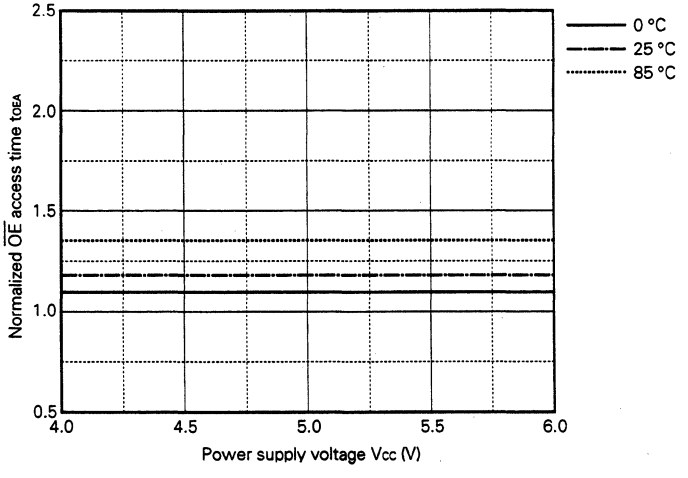


Figure A-25. V_{CC}-t_{OEA} Characteristics (5.0-V device)



A.3 Current Consumption Dependence on Cycle Time

Figure A-26. I_{CC1}-t_{RC} Characteristics (5.0-V device)

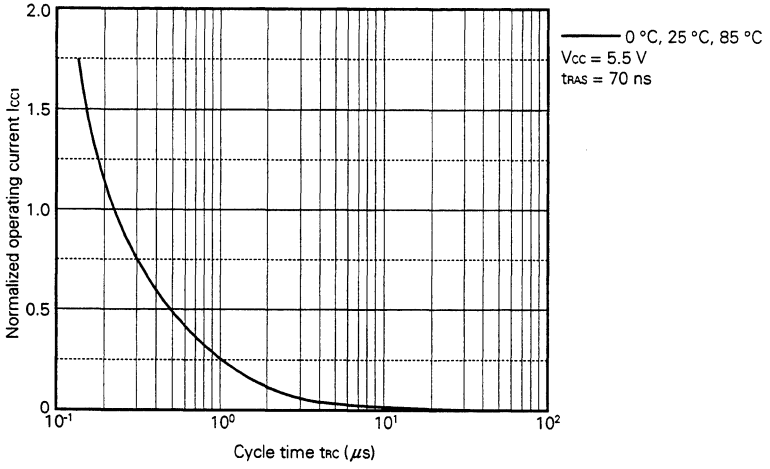


Figure A-27. I_{CC3}-t_{RC} Characteristics (5.0-V device)

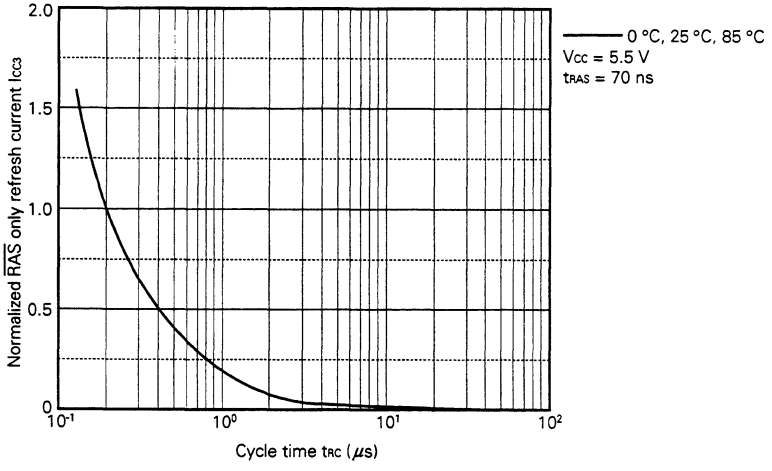


Figure A-28. I_{CC4}-t_{PC} Characteristics (5.0-V device)

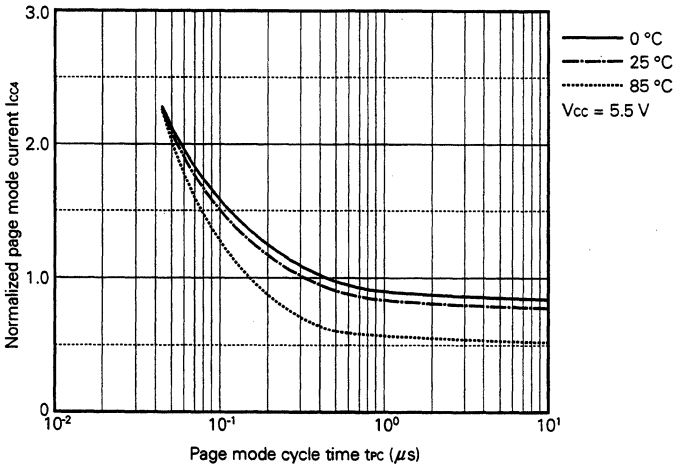


Figure A-29. I_{CC4}-t_{HPC} Characteristics (5.0-V device)

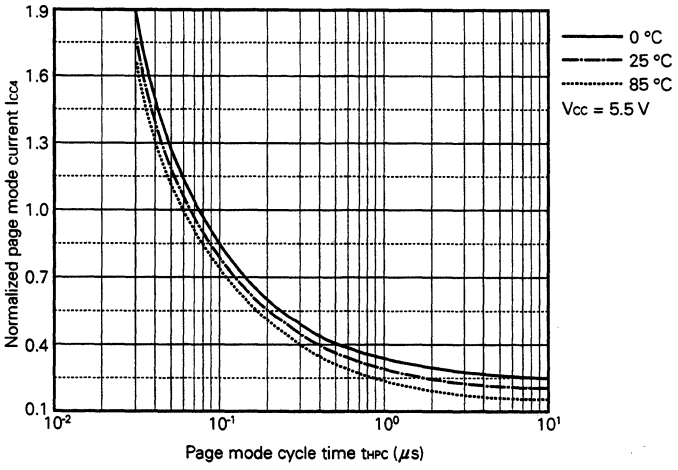


Figure A-30. I_{CC6}-t_{RC} Characteristics (5.0-V device)

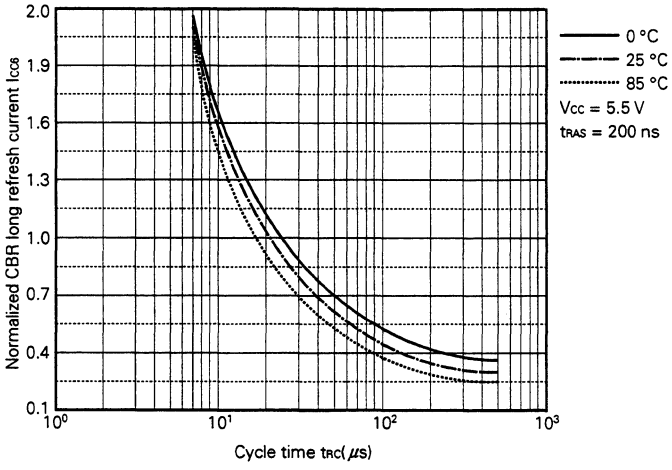


Figure A-31. I_{CC1}-t_{RAS} Characteristics (5.0-V device)

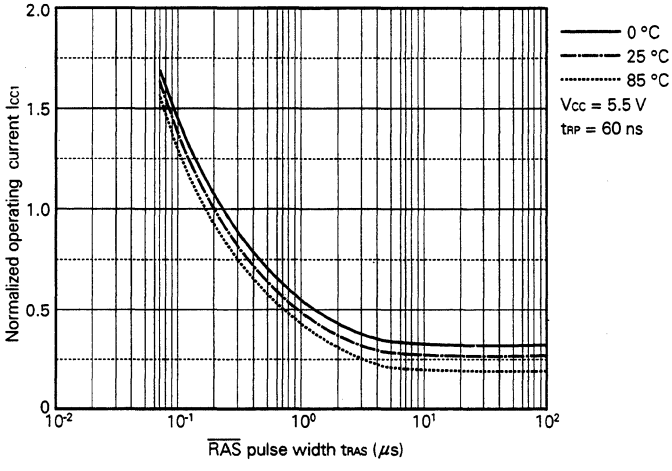


Figure A-32. I_{CC3}-t_{RAS} Characteristics (3.3-V device)

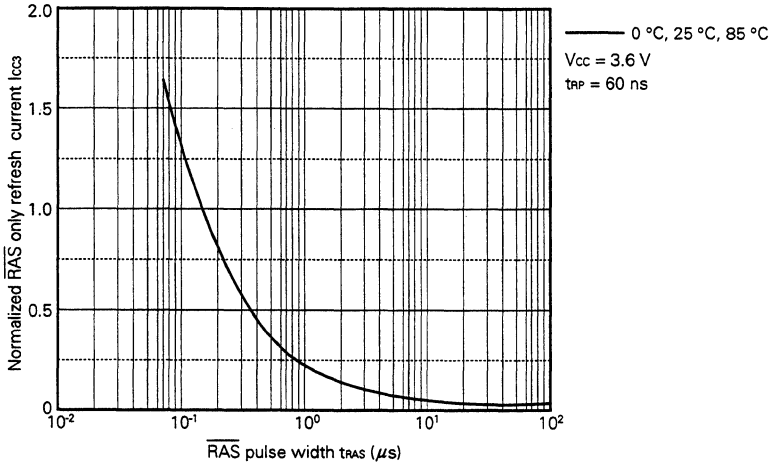


Figure A-33. I_{CC3}-t_{RAS} Characteristics (5.0-V device)

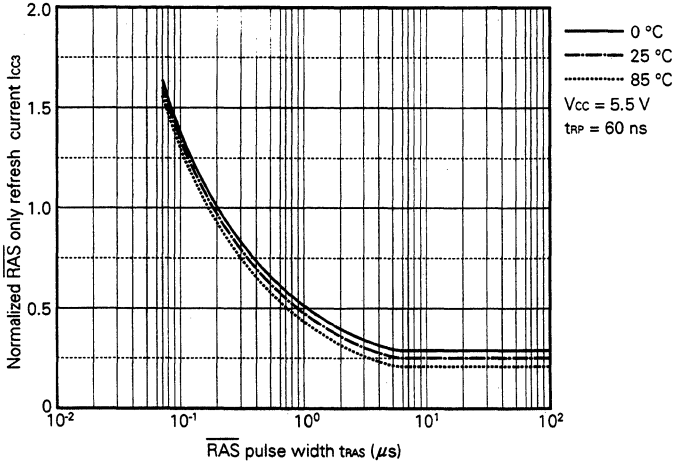
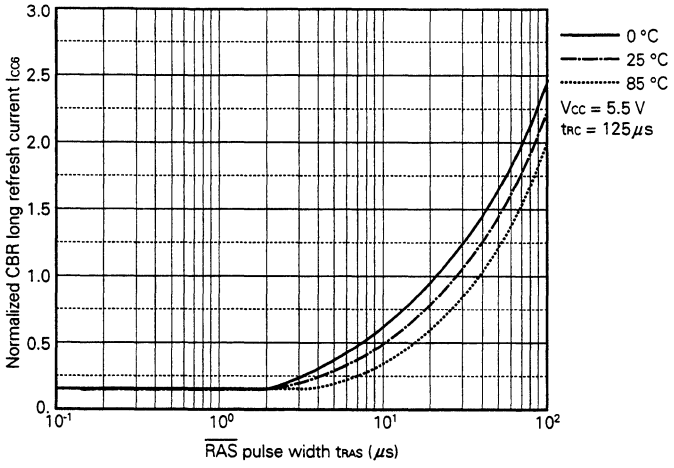


Figure A-34. I_{CC6}-t_{RAS} Characteristics (5.0-V device)

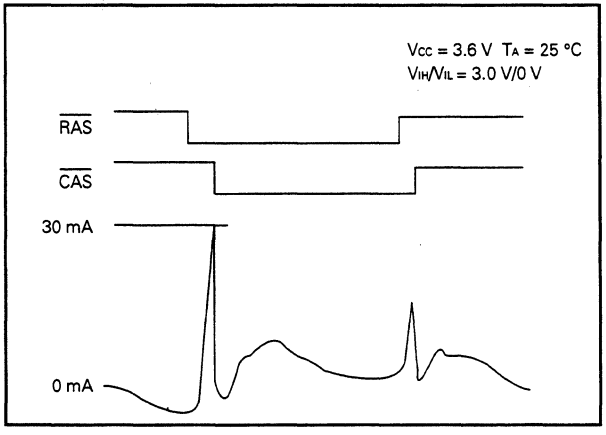


A.4 Current Consumption Waveform

When $\overline{RAS}$ is activated, the sense amplifier is also activated and hence current consumption is maximized at that instant (peak current).

The data in Figures A-1 through A-34 indicate the average current consumption. In reality, however, there is a current consumption peak, as shown in Figure A-35.

Figure A-35. $\overline{RAS}$/$\overline{CAS}$ Cycle Current Consumption Waveform



NEC Semiconductor Device Reliability/Quality Control System

INFORMATION

NEC

NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM

MICROCOMPUTER LSI

MEMORY IC

GATE ARRAY

LOGIC LSI

Document No. C10983EJ3V0IFU1

1. BASIC PRINCIPLES OF RELIABILITY/QUALITY CONTROL SYSTEM

NEC's reliability/quality control of semiconductors is based on the thorough integration of the reliable management in market analysis, development and design of the products meeting users' needs, and manufacturing process design, on one hand, and, quality control in materials and parts supply, each and every manufacturing process, direct and reliable assurance of thorough examination and reliability test of the products, and shipment and after-sale service management, on the other. It is our pleasure and pride to serve our customers best through a product-specific efficient management system to realize reliable quality and reasonable prices to the satisfaction of the users.

As the semiconductor application fields expand and develop, the amount used in those areas is increasing tremendously. The needs of our customers for higher and higher product quality are inevitable results of the development of the electronic industry.

To meet such users' needs, the NEC concentrates on the following three key points:

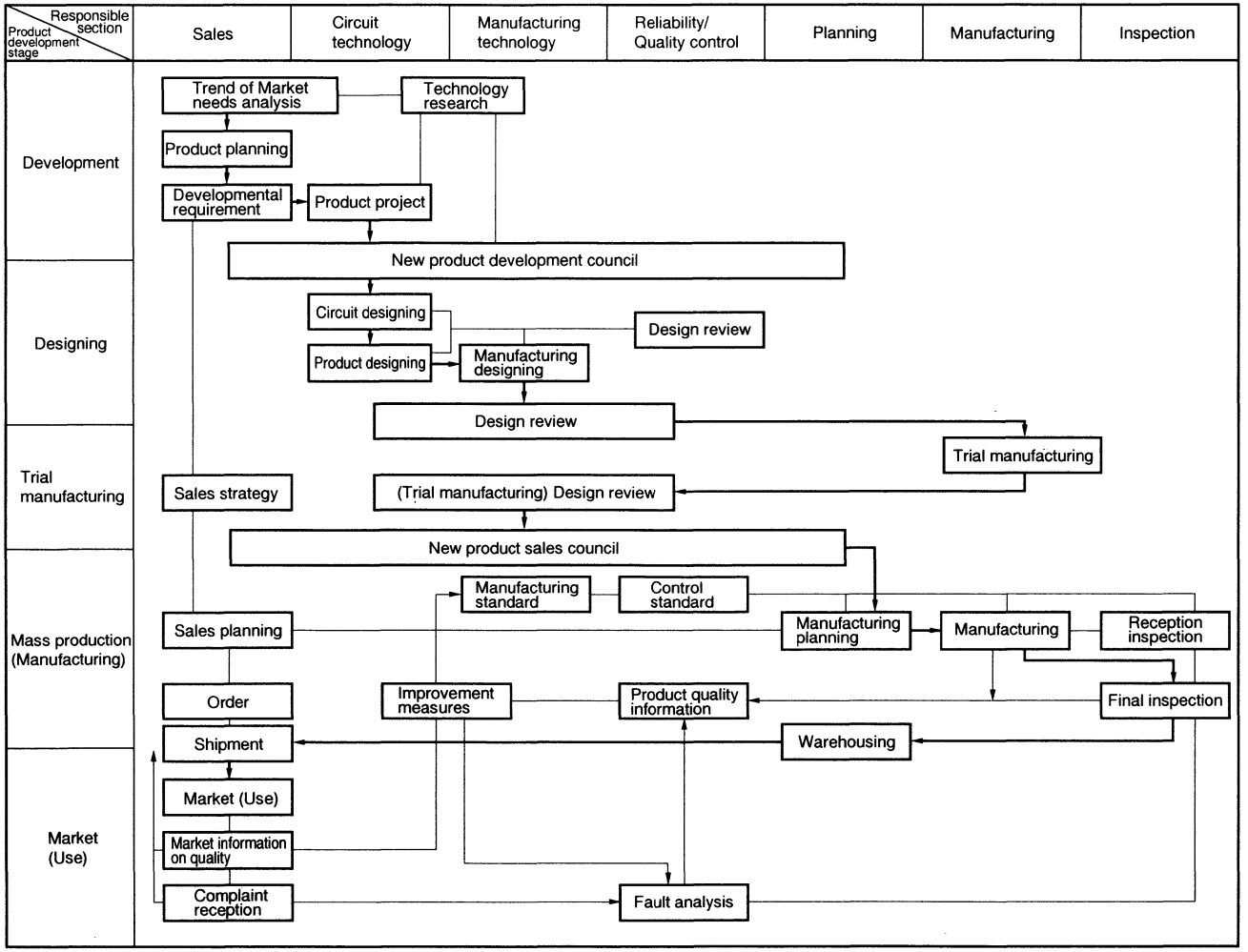
(1) Master design of key aspects of the product characteristics
(2) Quality control system built in the manufacturing process
(3) Removal of fault products through inspection of the products

The followings are our routine practices assure high quality products:

(a) Standardized designing practices to built reliability in to the developed products.
(b) Thorough examination of potential factors that may cause fault products at the design examination stage.
(c) Exhaustive and thoroughgoing evaluation of the characteristics and reliability test of the test products.
(d) Automated manufacturing equipment to reduce variability in the product quality.
(e) Quality control at each and every manufacturing process meeting the process-specific requirements.
(f) Built-in learning process to increase workers' awareness of the importance of the product quality through small group activities such as the ZD (Zero-defect) groups or QC circles.
(g) Product-specific screening, inspection, and reliability tests.
(h) Analysis of quality information, including the field data, and feed back/forward of the analysis results.

Through these effective measures, we believe that NEC can satisfy users' needs for its high quality products. It is not, however, the end of our efforts: we still try our best to improve the quality of our products. Figure 1 diagrammatically describes, our quality (Q) and reliability (R) control.

Fig. 1 Q and R System Diagram



2. MANUFACTURING PROCESS QUALITY CONTROL

NEC manufactures and sells its semiconductor products under the management policy of "Reliability Quality Control" based on an accurate understanding of customers' needs and operating conditions realized in the product designs.

To secure the intended reliability and quality in the product design, possible causes of off-grade products in the manufacturing processes must be eliminated in each step of the production line through qualified manufacturing management.

For the purpose, we carefully control the quality of the parts, materials and related goods, manufacturing equipment and environment. In addition, inspection processes are inserted in the manufacturing process to check the semifinal-final products by referring to key control items at proper sampling frequency.

The above-described quality control system is explained in detail referring to the flow chart Fig. 2 - Fig. 6.

The following is a brief explanation of the material/parts control system.

First, parts, materials, chemicals, highly pure gases, and other related goods are purchased from specific manufacturers authorized by NEC.

The results of the inspection are monitored and, when necessary, corrective measures are requested to the identified suppliers or the plants are audited by the purchase division to maintain quality of the purchased items.

Fig. 2 Manufacturing Process Control Flow Chart:
Example of Plastic Molded DIP, SOP, SOJ and QFJ (PLCC)

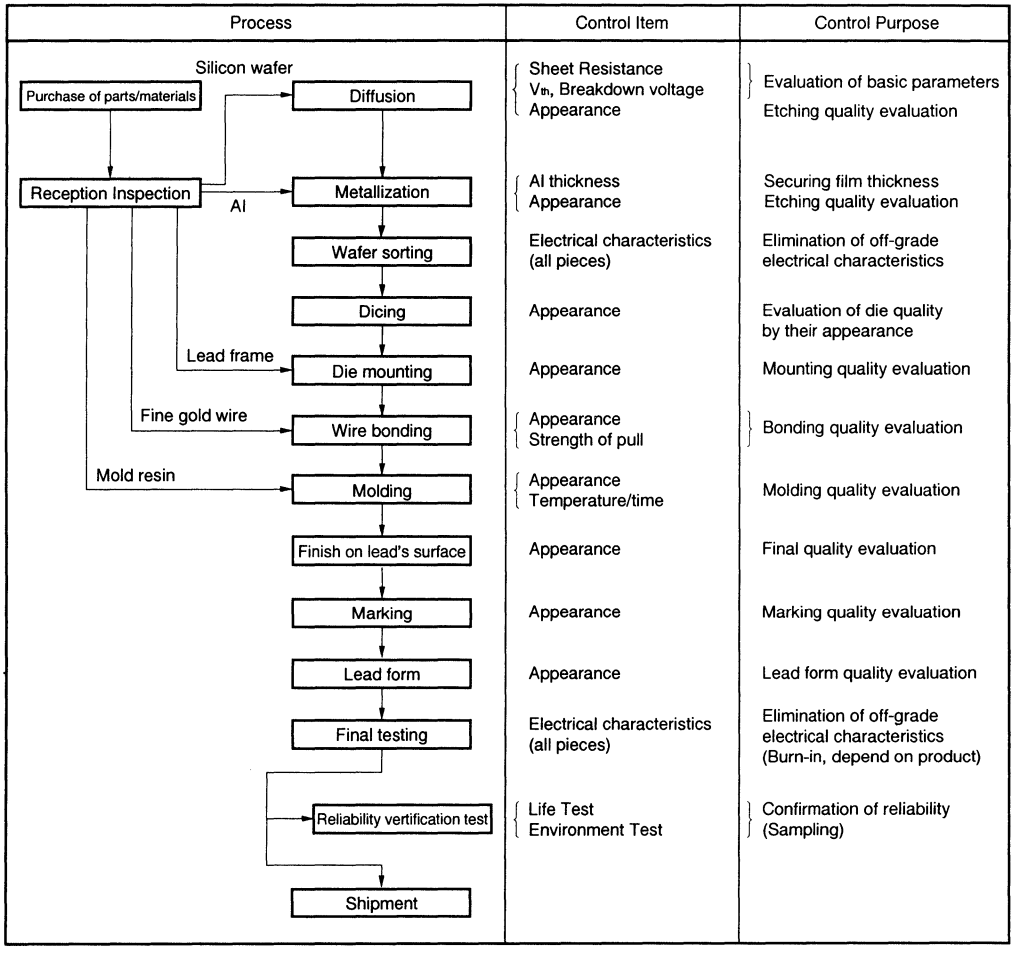


Fig. 3 Manufacturing Process Control Flow Chart: Example of Plastic Molded QFP and TSOP

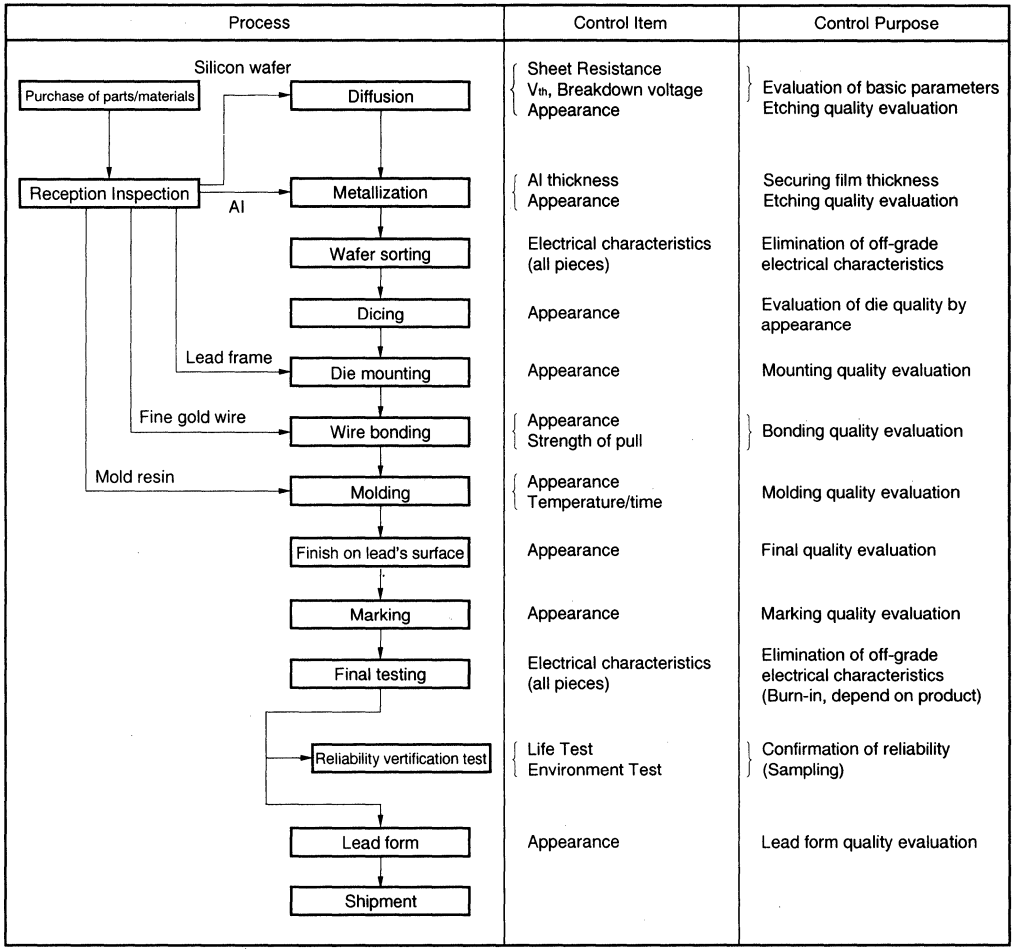


Fig. 4 Manufacturing Process Control Flow Chart: Example of PPGA

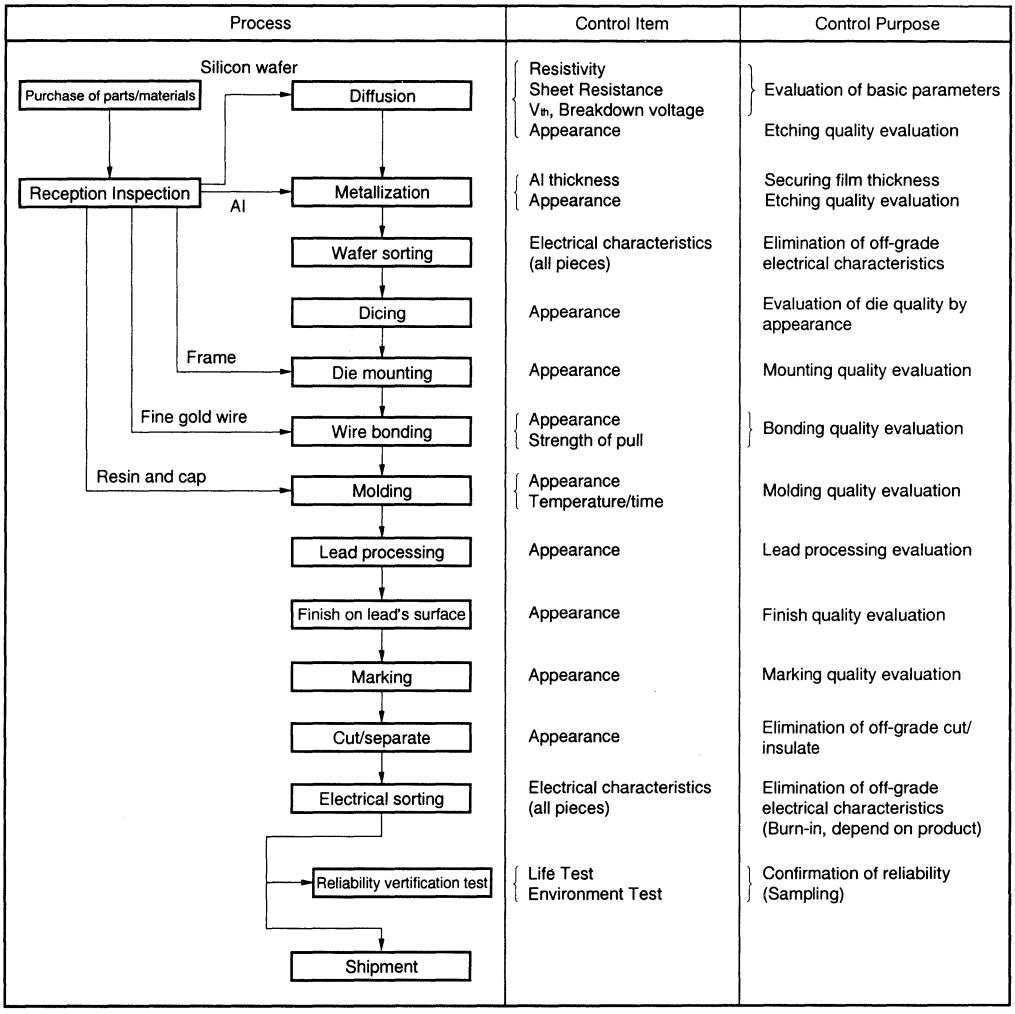


Fig. 5 Manufacturing Process Control Flow Chart: Example of Ceramic DIP (CERDIP)

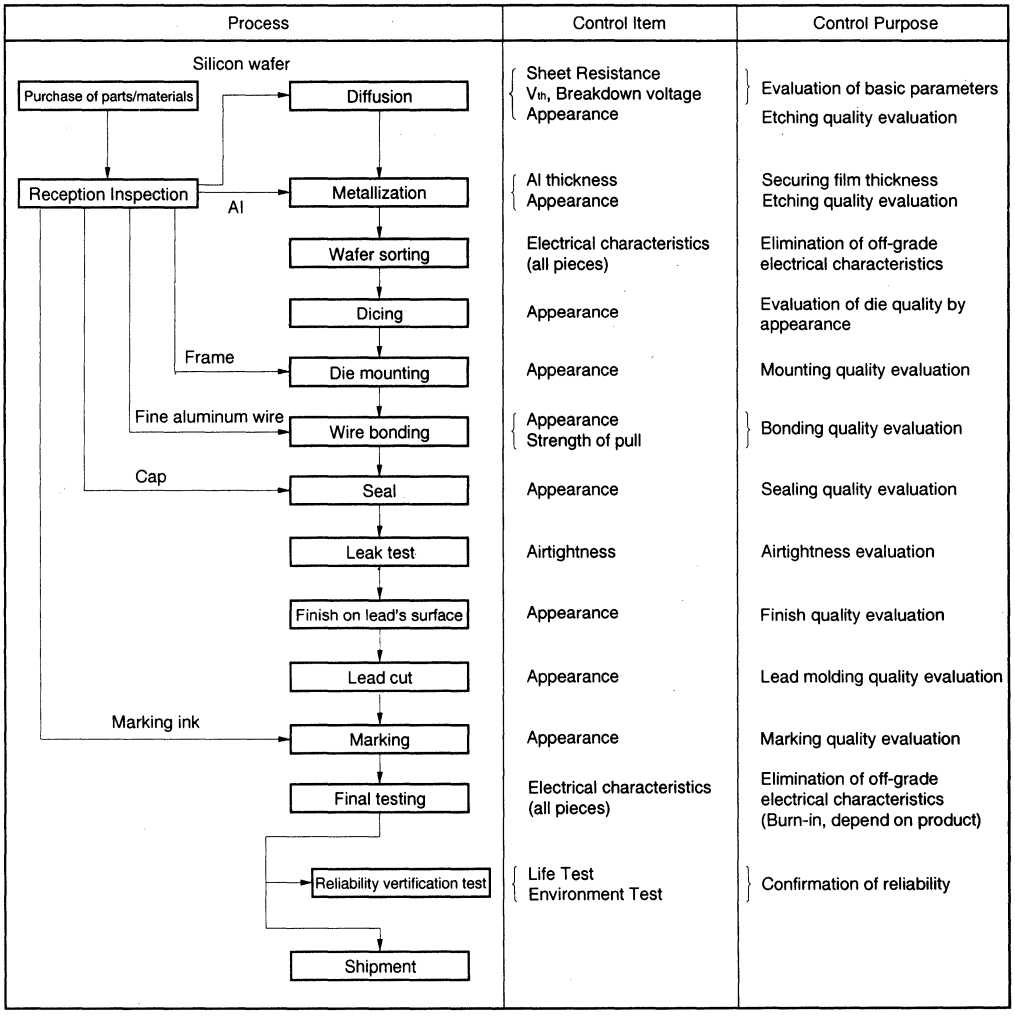
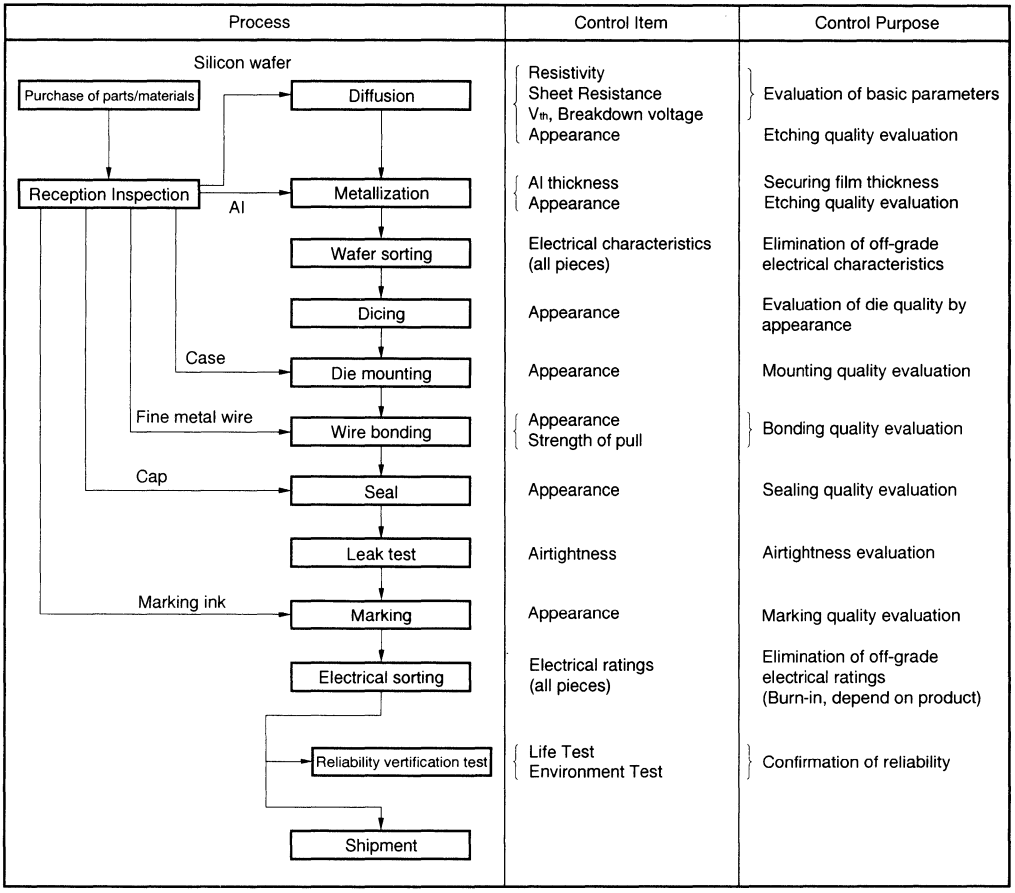


Fig. 6 Manufacturing Process Control Flow Chart:
Example of Ceramic DIP (SEAM WELD), Ceramic QFN (LCC), and Ceramic PGA



3. RELIABILITY TEST

NEC's reliability test is conducted periodically, considering various standards such as JIS C 7022, MIL-STD-883, and other standards.

The following, section 3.1 describes an example of the reliability test, and section 3.2, fault evaluation criteria in the reliability test.

3.1 DESCRIPTION OF THE RELIABILITY TEST

Reliability Test: Example of Plastic Packages

Test Item		Test Condition	Sample Size	Equipment Test Method	
				JIS C 7022	MIL-STD-883
Resistance to Soldering Heat*1		Soak the product in melted solder at 260 ±5 °C with no flux from 10 seconds. 1.6 ±0.8 mm deep from the product or its tab-stud.	18	A-1 Condition A	—
Temperature Cycle		Soak the product in a low temperature (T_{stg} min.) bath for 30 minutes then another 30 minutes in a high-temperature (T_{stg} max.) bath. Repeat this cycle 10 times.		A-4	1010 Condition C
Thermal Shock		Soak the product in a prescribed liquid at 100 °C for at least 5 minutes. Then, within 10 seconds, soak it in a prescribed liquid at 0 °C for at least 5 minutes. Repeat this cycle 15 times.		A-3 Condition A Method II	1011 Condition A
Solderability		Soak the device in noncorrosive flux up to 1.27 mm deep from the product for 5 to 10 seconds then in flux of melt solder at 230 ±5 °C with a soaking speed of 25.4 ±6.3 mm/s, again up to 1.27 mm deep from the device for 5 seconds. Wash away the flux in alcohol and examine the soldered area of the device.	5	A-2	2003
Terminal Strength	Bending*1	Apply a weight*2 to the lead of the product in a vertical direction of the axis of the lead without causing twist in it until the lead bends by 90 degrees, then release it. Repeat this operation three times. Apply this operation separately to 3 randomly chosen terminals.	5	—	2004 Condition B2
High-Temperature Storage		Conduct the left test in an environment atmosphere at 150 °C for 1000 hours.	18	B-3	1008
High-Temperature Bias		In an environmental atmosphere at 125 °C, apply the upper limit supply voltage of the recommended operating conditions for 1000 hours to conduct the bias life test.	24	B-1	1005 Condition A,B, and C
High-Temperature/ Humidity Storage		Conduct the life test in an atmosphere with relative humidity of 85 % at temperature of 85 °C for 1000 hours.	26	B-5 Condition B	—
PCT		Expose the device to vapor having a pressure of 2.3×10^5 Pa (2.3 barometric pressure) in an atmosphere at 125 °C for 96 hours.	18	—	—

***1)** PLCC is not subjected to this test.

***2)** The DIP and PPGA weight 250 grams; the SOP, QFP and QUIP weight 125 grams each.

Reliability Test: Example of Ceramic Packages

Test Item		Test Condition	Sample Size	Equipment Test Method	
				JIS C 7022	MIL-STD-883
Resistance to Soldering Heat*3		Soak the product in melted solder at 260 ±5 °C with no flux from 10 seconds. 1.6 ±0.8 mm deep from the product or its tab-stud.	18	A-1 Condition A	—
Temperature Cycle		Soak the product in a low temperature (T_{stg} min.) bath for 30 minutes, then another 30 minutes in a high-temperature (T_{stg} max.) bath. Repeat this cycle 10 times.		A-4	1010 Condition C
Thermal Shock		Soak the product in a prescribed liquid at 100 °C for at least 5 minutes. Then, within 10 seconds, soak it in a prescribed liquid at 0 °C for at least 5 minutes. Repeat this cycle 15 times.		A-3 Condition A Method II	1011 Condition A
Variable Frequency Oscillation		Fix the product on a vibrator and apply sine wave oscillation in the X, Y, and Z directions that logarithmically changes in the range between 10 to 2000, then 2000 to 10 Hz in 4 minutes, with a peak acceleration of 20 G.	18	A-10	2007 Condition A
Mechanical Shock		Mount the product on a shock tester and subject it to a shock of 1500 G (500 G*1) in acceleration and 0.5 ms in the pulse width, in the X, Y, and Z directions 3 times each.		A-7 Condition F, D	2002 Condition B, A
Constant Acceleration		Fix the product on the tester and subject it to a centrifugal acceleration of 20000 G (5000 G*2) is applied in the X, Y, and Z directions for 1 minute in each.		A-9 Condition C, A	2001 Condition A
Solderability		Soak the device in noncorrosive flux up to 1.27 mm deep from the product for 5 to 10 seconds, then in flux of melted solder at 230 ±5 °C at a soaking speed of 25.4 ±6.3 mm/s, again up to 1.27 mm deep from the device for 5 seconds. Wash away the flux in alcohol and examine the soldered area of the device.	5	A-2	2003
Terminal Strength	Bending*3	Apply a prescribed weight to the lead of the product in a vertical direction of the axis of the lead without causing twist in it until the lead bends by 90 ±5 degrees, then release it. Repeat this three times. Apply this separately to 3 randomly chosen terminals.	5	—	2004 Condition B2
High-Temperature Storage		Conduct the life test in an environmental atmosphere at 150 °C for 1000 hours.	18	B-3	1008
High-Temperature Bias		In an environmental atmosphere at 125 °C, apply the upper limit supply voltage of the recommended operating conditions for 1000 hours to conduct the bias life test.	24	B-1	1005 Condition A,B, and C

***1)** Glass-windowed products. ***2)** Glass-windowed products and products with heat sink.

***3)** The LCC is not subjected to this test.

3.2 FAULT EVALUATION CRITERIA IN RELIABILITY TEST

Example of Plastic Package Product

Testing Item	Fault Evaluation Criterion	
Resistance to Soldering Heat* Temperature Cycle Thermal Shock* High-Temperature Storage High-Temperature Bias High-Temperature/Humidity/Storage PCT	Within tolerance of the electrical characteristics	
Terminal Strength (Bending)*	Lead appearance	No breaking/Loosening
Solderability	Lead appearance	Above 95 % Solder Coverage of Tested Surface

*The PLCC is not subjected to this test.

Example of Ceramic Package Product

Testing Item	Fault Evaluation Criterion	
Resistance to Soldering Heat* Temperature Cycle Thermal Shock Variable Frequency Oscillation Mechanical Shock Constant Acceleration High-Temperature Storage High-Temperature Bias	Within tolerance of the electrical characteristics	
Terminal Strength (Bending)*	Lead appearance	No breaking/Loosening
Solderability	Lead appearance	Above 95 % Solder Coverage of Tested Surface

*The LCC is not subjected to this test.

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