

## OTI-040 286/386SX Core Logic Subsystem

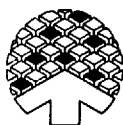
### Features

- Supports 286 and 386SX CPU for 8 MHz to 25 MHz system speed.
  - Highly integrated design
  - On-chip Address & Data path
  - EMS 4.0 Hardware support with 2 maps of 60 registers each
  - 287 support with 386SX
  - Async/Sync AT Bus
  - Selectable memory cycle
  - 82385SX support
  - PAGE and NO PAGE mode support
  - Peripheral chip select signals
  - Fast RESET & GATE 20
  - In-circuit test mode
- Reduced inventory, same design for 286 & 386SX systems.*  
*OTI-041, OTI-042, I/O Controller, 8042, 1 TTL*  
*no external buffers*  
*high-performance EMS driver*  
  
*low cost floating point solution*  
*flexible bus speed*  
*supports many vendor's DRAMs*  
*cache system support*  
*increases performance*  
*no external decode logic for HDD, FDD, Video, Keyboard, Parallel port & two serial ports*  
*optimized for OS/2 support*  
*simplifies board level testing*

### Laptop/Notebook designs

#### Features

- Support for local bus VGA
  - On-chip RTC with 128 bytes RAM
  - 8-bit BIOS ROM
  - Decoupled slow Refresh
  - Cartridge ROM support
  - O/S independent Power Management
  - CPU speed control
  - Activity Monitors
  - Programmable bidirectional I/O pins
  - Automatic Wake Up
- excellent graphics performance*  
*power management programmability*  
*saves board space*  
*reduces power consumption*  
*lightweight notebook design*  
*hardware configure power savings mode, to support power management*  
*no need for additional BIOS development*  
*reduces CPU clock speed with on-going memory refresh*  
*intelligent peripheral controller triggers power savings mode automatically by monitoring INTERRUPT, DMA & I/O activities*  
*pre-programmed pins to power on/off peripheral devices upon receiving signals from the activity monitors.*  
*well suited for Remote Data Acquisition type of applications*



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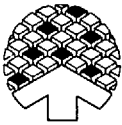
Product Overview  
December 1991

## General Description

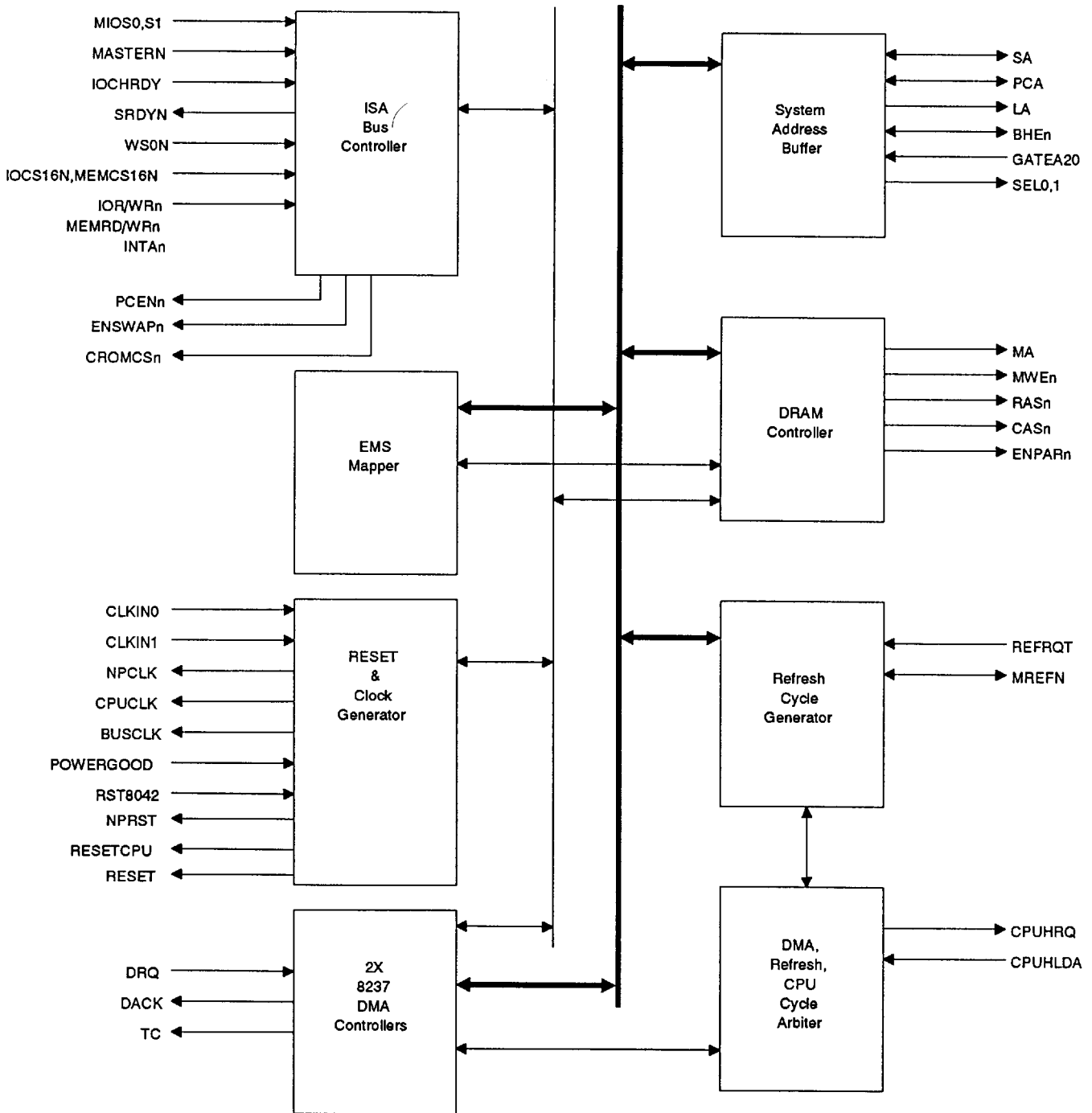
The OTI-040 system chipset is a highly integrated, semi-custom chipset designed for 80286 and 80386SX systems with clock speeds ranging from 8 MHz to 25 MHz. This chipset consists of the System Controller (OTI-041) and the Intelligent Peripheral Controller (OTI-042). Both chips are implemented with 1.2 micron HCMOS technology. The OTI-041 is packaged in a 160-pin PQFP, and the OTI-042 is packaged in a 144-pin PQFP.

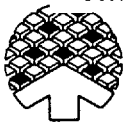
The OTI-040 chipset brings to systems designers an optimal solution for implementing a low cost, high performance PC/AT system. With the tightly-coupled local bus support provided by the OTI-040 for the Oak Technology LCD VGA Controller, the system designer can achieve outstanding graphics performance without the addition of any external TTL components. The 2/4-way interleaving and page-mode addressing scheme of the OTI-040 allows system designers to achieve very high system performance without the need for a complicated cache system design. For those users who require the utmost performance, the OTI-040 chipset does support an external 82385SX cache controller. To implement a full function PC/AT system, all that is required would be the OTI-041, OTI-042, CPU, ROM, RAM, 8042, I/O Controller, graphics controller, and one 7406. This system provides an amazing PC board area savings. The single-chip AT solutions normally require a lot of external TTL components to complete the system design.

With the OTI-040 chipset, there is no need for any extensive BIOS development to implement your power management scheme for laptop/notebook designs. The O/S Independent Power Management Scheme and the Activity Monitors inside the OTI-040 chipset can bring the laptop/notebook system into power savings modes automatically, without any BIOS intervention.



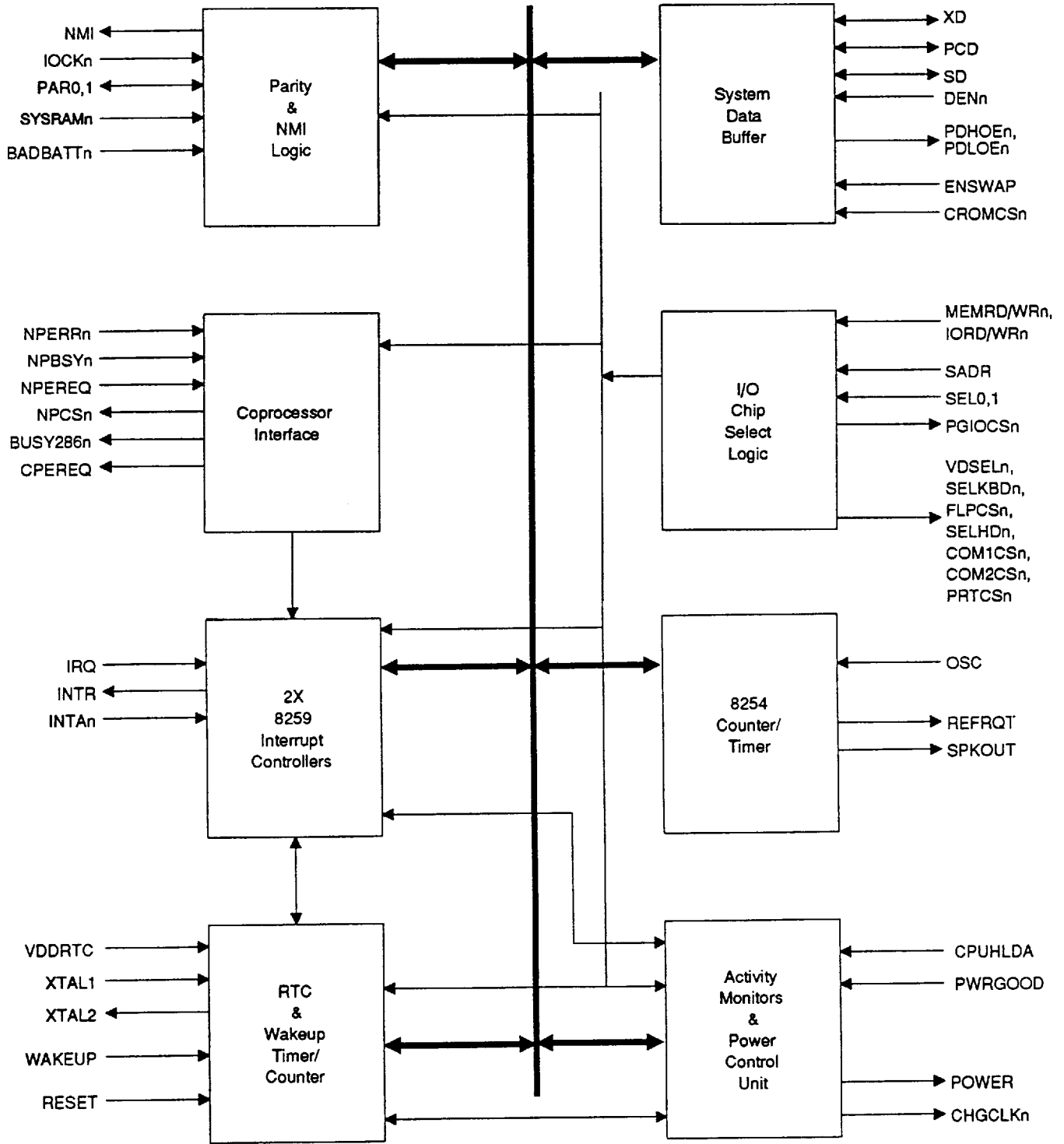
### OTI-041 Chip Block Diagram

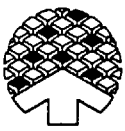




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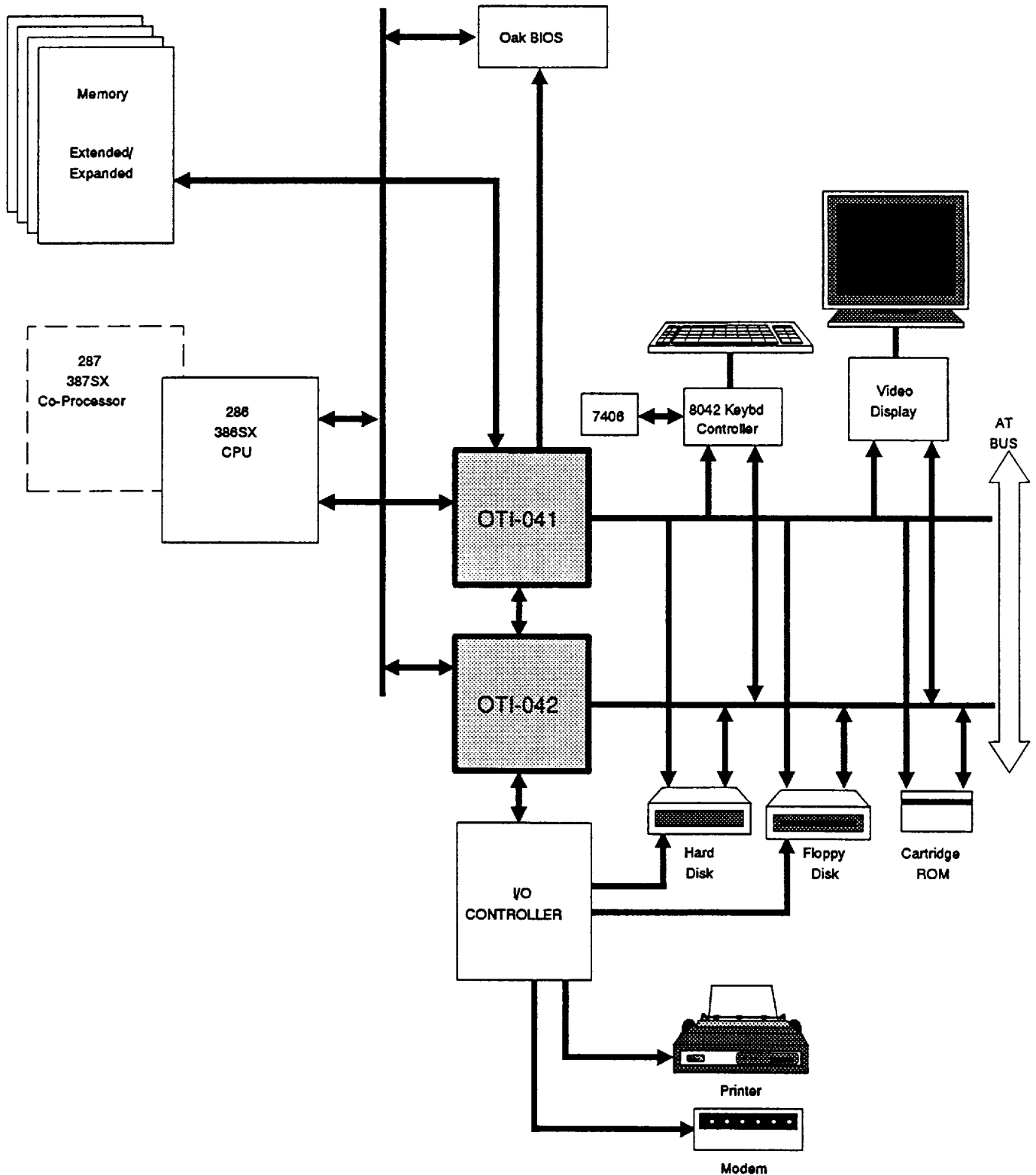
### OTI-042 Chip Block Diagram

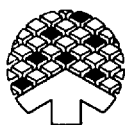




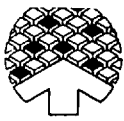
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### System Block Diagram



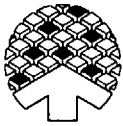
**OTI-041 Pin Description**

Pin Name	Pin Number	Pin Type	Description
<b>CPU Interface</b>			
SA[23:0]	TBA	I	CPU ADDRESS BUS
BHE <sub>n</sub>	TBA	I	BYTE HIGH ENABLE. An active-low signal used to enable data on to the most significant half of the data bus (D15 - D8).
RESETCPU	TBA	O	RESET CPU. An active-high output to reset the CPU.
NPRST	TBA	O	CO-PROCESSOR RESET. An active-high signal to reset the numerical co-processor.
ADSn	TBA	I	ADDRESS STROBE. An active-low signal coming from 80386SX. This input is also used to detect the presence of 386SX. This pin should be pulled low with a 20K-ohm resistor.
S1 - S0	TBA	I	BUS CYCLE STATUS. These signals together with M/IO and COD/INTA <sub>n</sub> are used to decode different bus cycles. S0 and S1 are connected to W/R <sub>m</sub> and D/C <sub>m</sub> , respectively.
M/IO <sub>n</sub>	TBA	I	MEMORY OR I/O CYCLE. An input signal from CPU indicating whether the present cycle is memory or I/O access.
CPUCLK	TBA	O	CPU CLOCK. A MOS driven clock signal to the 80286/80386SX CPU. The frequency is programmable through index port 0003H.
NPCLK	TBA	O	CO-PROCESSOR CLOCK. Clock signal for 80287 or 80387SX. This clock can be programmed to stop if co-processor is not used.
SRDY <sub>n</sub>	TBA	O	SYSTEM READY. An active-low signal to acknowledge the CPU that the data transfer for either memory or I/O is complete.
<b>DMA Interface</b>			
DRQ0-3 DRQ5-7	TBA	I	DMA REQUEST. These are asynchronous active-high channel request inputs used by peripheral devices to obtain DMA service.
DACK0-3 DACK5-7	TBA	O	DMA ACKNOWLEDGE. These are active-low signals to notify the individual peripheral that it has been granted a DMA cycle.
CPUHRQ	TBA	O	HOLD REQUEST. An active-high signal connected directly to HOLD of the CPU. This signal is used by the chip to request the bus from the CPU.
CPUHLDA	TBA	I	HOLD ACKNOWLEDGE. An active-high signal connected directly to HLDA of CPU. This signal is used by the chip to determine if the bus request has been granted by the CPU.
TC	TBA	O	TERMINAL COUNT. An active-high output pulse signal when the terminal count for any DMA channel is reached.



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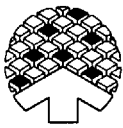
Pin Name	Pin Number	Pin Type	Description
<b>Bus Interface</b>			
PCA[19:0]	TBA	I/O	PC BUS ADDRESS (19-0). These are the latched version of SA(0-19) and become input during MASTER mode.
LA[23:17]	TBA	I/O	UNLATCHED ADDRESS (23-17). These are the unlatched version of SA(23-17). The bus become input when MASTER <sub>n</sub> is active.
PBHE <sub>n</sub>	TBA	I/O	I/O CHANNEL BYTE HIGH ENABLE. An active-low signal on the I/O channel. It is a latched version of BHE <sub>n</sub> . When MASTER <sub>n</sub> is low, it becomes input.
WS0 <sub>n</sub>	TBA	I	ZERO WAIT STATE. An active-low signal indicating the present cycle can be completed without any more wait state.
IOCS16 <sub>n</sub>	TBA	I	16-BIT I/O CHIP SELECT. An active-low input that indicates to the system that the present data transfer is a 1 wait-state, 16-bit I/O cycle.
MEMCS16 <sub>n</sub>	TBA	I	16-BIT MEMORY CHIP SELECT. An active-low input that indicates to the system that the present data transfer is a 1 wait-state, 16-bit memory cycle.
PCALE	TBA	O	PC ADDRESS LATCH ENABLE. An active-high pulse signal during phase 2 of TS(T1p or T2 for 80386SX) of any bus cycle and is always high when the CPU is held. It is synchronized to BUSCLK.
IOCHRDY	TBA	I	I/O CHANNEL READY. An active-high ready signal from an I/O channel. It is pulled low by a memory or I/O device to lengthen memory or I/O cycles.
IORD <sub>n</sub>	TBA	I/O	I/O READ COMMAND. An active-low command to instruct the I/O device to drive its data onto the data bus. It is input when MASTER <sub>n</sub> is active.
IOWR <sub>n</sub>	TBA	I/O	I/O WRITE COMMAND. An active-low command to instruct the I/O device to read the data present on the data bus. It is input when MASTER <sub>n</sub> is active.
MEMRD <sub>n</sub>	TBA	I/O	MEMORY READ COMMAND. An active-low signal to instruct the memory subsystem to drive its data onto the data bus. It is input when MASTER <sub>n</sub> is active.
MEMWR <sub>n</sub>	TBA	I/O	MEMORY WRITE COMMAND. An active-low signal to instruct the memory subsystem to store the data present on the data bus. It is input when MASTER <sub>n</sub> is active.
BUSCLK	TBA	O	PC-BUS CLOCK. An MOS driven clock signal for the I/O channel.



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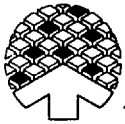
Pin Name	Pin Number	Pin Type	Description															
<b>System Interface</b>																		
INTAn/WAKEUPn	TBA	I/O	INTERRUPT ACKNOWLEDGE. An active-low signal to enable the interrupt controller's interrupt-vector data onto the data bus. It is input during shutdown/sleep mode as wakeup signal for the OTI-041.															
GATEA20	TBA	I	GATE A20. An active-high signal from the 8042 used to gate address A20.															
RST8042n	TBA	I	RESET FROM 8042. An active-low signal from the 8042 to reset the CPU.															
CHKCLKn	TBA	I	CHANGE SYSTEM SPEED. An active-low input signal from the OTI-042 indicating change of system speed.															
PCENn	TBA	O	PC DATA BUS ENABLE. An active-low control signal to enable the data buffer between CPU and PC data bus. PCENn is active low if: <ol style="list-style-type: none"> <li>1. CPU I/O read/write cycle, except co-processor I/O.</li> <li>2. CPU memory read/write cycle, except onboard RAM and ROM.</li> <li>3. Interrupt acknowledge cycle (INTAn active).</li> </ol>															
ENSWAPn	TBA	O	ENABLE DATA SWAP. An output to control the output enable of the byte swapping data buffer.															
ROMCSn	TBA	O	ROM CHIP SELECT. An active-low output signal used to enable the ROM BIOS to output data onto the data bus.															
CROMCSn	TBA	O	CARTRIDGE ROM CHIP SELECT. An active-low output signal used to access the cartridge ROM.															
SEL0	TBA	I/O	SELECT FUNCTION 0. One of the two address encoding signals.															
SEL1	TBA	O	SELECT FUNCTION 1. Together with SEL0, encodes the following address ranges: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SEL1</th> <th>SEL0</th> <th>FUNCTION</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Nothing selected</td> </tr> <tr> <td>0</td> <td>1</td> <td>A15 - A10 = 0 (I/O) or onboard video RAM</td> </tr> <tr> <td>1</td> <td>0</td> <td>onboard video ROM</td> </tr> <tr> <td>1</td> <td>1</td> <td>I/O channel memory but within 1M</td> </tr> </tbody> </table>	SEL1	SEL0	FUNCTION	0	0	Nothing selected	0	1	A15 - A10 = 0 (I/O) or onboard video RAM	1	0	onboard video ROM	1	1	I/O channel memory but within 1M
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PWRGOOD	TBA	I	POWER GOOD. An active-high signal from the power supply after DC power level is stable.															
XD[7:0]	TBA	I/O	XDATA BUS. A bidirectional data lines for accessing this chip.															
REFRQT	TBA	I	MEMORY REFRESH REQUEST. The memory refresh request input signal from 8254 Timer channel 1 which comes from the OTI-042.															
MREFn	TBA	I/O	MEMORY REFRESH. An active-low signal indicating that refresh cycle is going on.															





## OAK TECHNOLOGY, INC.

Pin Name	Pin Number	Pin Type	Description
<b>System Interface (Continued)</b>			
ENPAR <sub>n</sub>	TBA	O	ENABLE MEMORY PARITY. An active-low output signal indicating that onboard RAM is being accessed.
RMRD <sub>n</sub>	TBA	I/O	ROM/RAM READ. An active-low signal indicating that onboard ROM or RAM is being read. It is an input representing the signal NPBSY <sub>n</sub> when accessing 80287 operation code for 80386SX CPU.
<b>Memory Interface</b>			
MA[11:1]	TBA	I/O	MEMORY ADDRESS (1-11). During memory cycles, this is a time multiplexed memory address bus for 1M memory type (for 256K memory type MA(10,11) is not used).
RAS0 <sub>n</sub> - RAS3 <sub>n</sub>	TBA	O	ROW ADDRESS STROBE (0 - 3). These are active-low control signals to the onboard DRAM to strobe the row address.
CASH0-3 <sub>n</sub> - CASL0-3 <sub>n</sub>	TBA	O	COLUMN ADDRESS STROBE (High & Low). These are active low control signals to on board DRAM to strobe the column address: CASH <sub>n</sub> for odd bytes D(15-8) and CASL <sub>n</sub> for even bytes D(7-0).
MWEn	TBA	O	MEMORY WRITE ENABLE. An active-low output used to control memory read/write cycles.
<b>Miscellaneous</b>			
CLKIN0	TBA	I	CLOCK INPUT 0. A 32 MHz TTL clock input with 50% duty cycle. It is used for: the CPU clock generation with CPU running at 8 or 16 MHz, asynchronous bus clock generation, and memory refresh time.
CLKIN1	TBA	I	CLOCK INPUT 1. An optional 20/25/40/50 MHz CMOS clock input with 50% duty cycle. It is used for CPU clock generation with CPU running at 10, 12.5, 20, and 25 MHz.
VDD	TBA	I	POWER: +5 V supply.
VSS	TBA	I	GROUND:

**OTI-042 Pin Description**

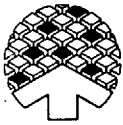
Pin Name	Pin Number	Pin Type	Description
<b>CPU Interface</b>			
CPUHLDA	TBA	I	CPU HOLD ACKNOWLEDGE. This input signal is active when the CPU releases the control of the bus.
SD[15:0]	TBA	I/O	CPU DATA BUS (0-15). The CPU data bus.
<b>System Interface</b>			
DEN <sub>n</sub>	TBA	I	DATA BUFFER ENABLE. An active-low input control signal to enable/disable the internal data transceiver between SD(0-15) and PCD(0-15).
PDLDIR <sub>n</sub>	TBA	O	EXTERNAL DATA BUFFER OUTPUT ENABLE. An active-low output control signal to enable output for the external data transceiver between PCD(0-7) and slot data bus(0-7).
PDHDIR <sub>n</sub>	TBA	O	EXTERNAL DATA BUFFER OUTPUT ENABLE. An active-low output control signal to enable output for the external data transceiver between PCD(8-15) and slot data bus(8-15).
ENSWAP <sub>n</sub>	TBA	I	ENABLE DATA SWAP. An active-low input signal used for enabling the byte swapping data buffer.
XD[7:0]	TBA	I/O	XD BUS. Bidirectional data lines to/from the XD bus for accessing onboard peripherals.
IORD <sub>n</sub>	TBA	I	I/O READ COMMAND. An active-low input command to instruct the I/O device to drive its data onto the data bus.
IOWR <sub>n</sub>	TBA	I	I/O WRITE COMMAND. An active-low input command to instruct the I/O device to read the data present on the data bus.
MEMRD <sub>n</sub>	TBA	I	MEMORY READ COMMAND. An active-low input signal to instruct the memory sub-system to drive its data onto the data bus.
MEMWR <sub>n</sub>	TBA	I	MEMORY WRITE COMMAND. An active-low input signal to instruct the memory sub-system to read the data present on the data bus.
REFRQT	TBA	O	REFRESH REQUEST. Indicates to the arbiter in the OTI-041 that DRAM needs refreshing.
CROMCS <sub>n</sub>	TBA	I	CARTRIDGE ROM CHIP SELECT. An active-low input signal from the OTI-041 indicating cartridge ROM is being accessed.
SEL0	TBA	I/O	SELECT FUNCTION 0. One of the two address encoding signals. It is output during refresh period as TURBO signal for the OTI-041.



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Product Overview  
December 1991

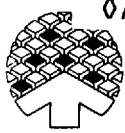
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ROMCS <sub>n</sub>	TBA	I	ROM CHIP SELECT. An active-low signal used to enable the ROM BIOS to output data on to the data bus.															
VDPMSSEL <sub>n</sub>	TBA	O	VIDEO ROM CHIP SELECT. The chip select signal for on board video ROM.															
VDSEL/VGAEN	TBA	O	VIDEO CHIP SELECT/VGA ENABLE. The chip select signal for on board video I/O and RAM address space, special for OAK VGA OTI-037. If IBM compatible VGA is used, this pin becomes VGA enable signal.															
<b>82385SX Support</b>																		
FGA20	TBA	O	FAST GATE A20															
FLUSH	TBA	O	FLUSH CACHE. This pin acts as cache flush when EMS mapper is updated.															
<b>Bus Interface</b>																		
PCMEMRD <sub>n</sub>	TBA	O	MEMORY READ COMMAND. An active-low signal to instruct the memory sub-system within 1M on the I/O channel to drive its data onto the data bus.															
PCMEMWR <sub>n</sub>	TBA	O	MEMORY WRITE COMMAND. An active-low signal to instruct the memory sub-system within 1M on the I/O channel to store the data present on the data bus.															
PCAEN	TBA	O	ADDRESS ENABLE. A signal to de-gate the I/O devices from the I/O channel and allow DMA transfers to take place.															
MASTER <sub>n</sub>	TBA	I	MASTER. This signal is used together with a DRQ line to gain control of the system.															
PCD[15:0]	TBA	I/O	I/O CHANNEL DATA BUS (0-15). The I/O channel data bus. There are two sets of data transceivers that are connected internally, (i.e., between SD(0-7) and PCD(0-7) and between SD(8-15) and PCD(8-15)).															
SADR[9:0]	TBA	I	ADDRESS BUS. The I/O channel address bus.															
PBHE <sub>n</sub>	TBA	I	BYTE HIGH ENABLE.															
MREF <sub>n</sub>	TBA	I	MEMORY REFRESH CYCLE. An active-low signal indicating that the system is in the memory refresh cycle.															



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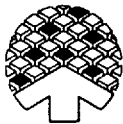
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Pin Name	Pin Number	Pin Type	Description
<b>Real Time Clock</b>			
XTAL1	TBA	I	XTAL INPUT FOR RTC. The crystal input for the built-in real time clock.
XTAL2	TBA	O	XTAL OUTPUT FOR RTC. The crystal output for the built-in real time clock.
VDDRTC	TBA	I	POWER. Battery power for the built-in Real Time Clock.
<b>Reset Generation</b>			
PWRGOOD	TBA	I	POWER GOOD. PWRGOOD comes from the power supply to indicate that power is stable.
RESET	TBA	O	RESET. An active-high signal synchronized to the CPU clock to reset the system.
<b>Timer Counter</b>			
SPKOUT	TBA	O	SPEAKER DATA OUTPUT. Speaker output data, to be connected to a speaker driver to drive the speaker or beeper.
<b>Interrupt Controller</b>			
IRQ1, IRQ3-7 IRQ9-12, IRQ14-15	TBA	I	INTERRUPT REQUEST INPUTS. asynchronous interrupt request inputs to the internal 8259 controllers.
INTR	TBA	O	INTERRUPT REQUEST. Interrupt request to the CPU and is generated whenever a valid IRQ is received.
INTAn	TBA	I/O	INTERRUPT ACKNOWLEDGE. An active-low signal from the OTI-041 indicating that an interrupt acknowledge cycle is in progress. It is output during shutdown/sleep mode to pass the wakeup signal to the OTI-041, either from WAKEUP pin or from wakeup timer or from INTR signal.
<b>Keyboard and Mouse Interface</b>			
SELKBDn	TBA	O	SELECT KEYBOARD. An active-low signal indicating that the keyboard controller is selected.
<b>Floppy Disk Controller</b>			
FLPCSn	TBA	O	FLOPPY SELECT. An active-low signal used to select the floppy disk controller. This pin is multiplexed with POFF4n.
DACK2n	TBA	I	DMA ACKNOWLEDGE. An active-low signal indicating that the floppy disk controller has been granted a DMA cycle.
<b>Hard Disk Controller</b>			
SELHDK1n	TBA	O	HARD DISK SELECT2. When Conner's hard disk is installed, this pin is used as one of the chip select signal decoding addresses 3F6H & 3F7H. This pin is multiplexed with POFF3n.
SELHDK0n	TBA	O	HARD DISK SELECT1. An active-low signal to select on-board hard disk drive. This pin is multiplexed with POFF2n.



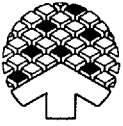
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Pin Name	Pin Number	Pin Type	Description
<b>Co-processor Interface</b>			
NPERR <sub>n</sub>	TBA	I	NUMERICAL PROCESSOR ERROR. An active-low input indicating that an unmasked exception has occurred during numeric instruction execution when the co-processor interrupt is enabled.
NPBSY <sub>n</sub>	TBA	I	NUMERICAL PROCESSOR BUSY. An active-low input connected directly to the BUSY signal of the co-processor.
NPCS <sub>n</sub>	TBA	O	NUMERICAL PROCESSOR CHIP SELECT. An active-low output to select the co-processor.
BUSY286 <sub>n</sub>	TBA	O	BUSY TO CPU. An active-low output connected directly to the BUSY input of the CPU.
NPPREQ	TBA	I	NUMERICAL PROCESSOR REQUEST. An active-high input indicating that the co-processor is requesting an operand transfer. This pin comes from the PEREQ output of the co-processor.
CPEREQ	TBA	O	CPU REQUEST. An active-high output to the CPU indicating to the CPU that the co-processor is requesting an operand transfer.
<b>NMI Generation</b>			
IOCK <sub>n</sub>	TBA	I	I/O CHANNEL CHECK. An active-low input indicating that an I/O channel error condition is detected.
PAR0 - PAR1	TBA	I/O	PARITY BIT (0 - 1). The memory parity bits for even and odd bytes of the memory bank. Each parity bit is generated and written during the memory write operation. Each is checked and reported on an error to the system at the end of memory read cycle. PAR0 is memory parity bit for even byte, PAR1 is the memory parity bit for odd byte.
SYSRAM <sub>n</sub>	TBA	I	ENABLE MEMORY PARITY. An active-low input indicating that onboard RAM is being accessed.
RMRD <sub>n</sub>	TBA	I/O	ROM/RAM READ. An active-low signal indicating that onboard ROM or RAM is being read. RMRD <sub>n</sub> is an output equal to NPBSY <sub>n</sub> signal when I/O address F8H is selected.
NMI	TBA	O	NON-MASKABLE INTERRUPT. An active-high output to the CPU indicating that an error has occurred in one of the following areas: memory parity error or I/O channel check signal.
<b>Chip Select Signals</b>			
PGIOCS0 <sub>n</sub>	TBA	O	PROGRAMMABLE I/O CHIP SELECT 0. An active-low I/O chip select signal with a programmable I/O address space.
COM1CS <sub>n</sub>	TBA	O	SERIAL PORT 1 CHIP SELECT. An active-low I/O chip select signal for the serial port 1. This pin is multiplexed with POF7 <sub>n</sub> .



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Pin Name	Pin Number	Pin Type	Description
<b>Chip Select Signals (Continued)</b>			
COM2CS <sub>n</sub>	TBA	O	SERIAL PORT 2 CHIP SELECT. An active-low I/O chip select signal for the serial port 2. This pin is multiplexed with POFF8 <sub>n</sub> .
PRTCS <sub>n</sub>	TBA	O	PRINTER PORT CHIP SELECT. An active-low I/O chip select signal for the printer port. This pin is multiplexed with POFF6 <sub>n</sub> .
PRTOE <sub>n</sub>	TBA	O	PRINTER PORT OUTPUT ENABLE. An active-low bidirectional printer port output enable signal. This pin is multiplexed with POFF5 <sub>n</sub> .
<b>Power Control Signals</b>			
POFF0 <sub>n</sub>	TBA	I/O	PROGRAMMABLE BIDIRECTIONAL CONTROL SIGNALS. I/O signals to control power to peripherals or as status input to system.
POFF1 <sub>n</sub> -POFF8 <sub>n</sub>	TBA	I/O	PROGRAMMABLE BIDIRECTIONAL CONTROL SIGNALS. I/O signals to control power to peripherals or as status input to system. These pins are multiplexed with Chip Select signals.
HDDPWR	TBA	O	HARD DISK POWER. An active-high output that controls power to the hard disk.
LCDPWR	TBA	O	LCD BACKLIGHT POWER. An active-high output that controls power to LCD backlight.
LCDMODE0,1	TBA	O	LCD POWER SAVINGS MODES CONTROL. An active-high output that controls LCD standby mode.
SYSPWR	TBA	O	SYSTEM POWER CONTROL. An active-high output that controls power to the entire system.
<b>Miscellaneous</b>			
TURBO <sub>n</sub>	TBA	I	TURBO SPEED SELECTION INPUT. When high (inactive), forces CPUCLK to be 8MHZ. When active low, CPUCLK will be controlled by the speed control register. This pin is multiplexed with POFF1 <sub>n</sub> .
<b>Miscellaneous</b>			
WAKEUP <sub>n</sub>	TBA	I	WAKEUP PIN. When active high, triggers internal wakeup counter. When the wakeup counter down-counts to zero, the system is resumed from sleep or shutdown mode.
BADBATT <sub>n</sub>	TBA	I	BAD BATTERY INPUT. An active-low input indicating that a bad battery status has been detected. This signal level can be readable and it can be optionally enabled to generate NMI.
PWRDOWN	TBA	I	POWER DOWN. An active-high external input to trigger power-down mode.
CHGCLK <sub>n</sub>	TBA	O	CHANGE SYSTEM SPEED. An active-low output to OTI-041 for changing system clock frequency.
OSC	TBA	I	14.318 MHz OSCILLATOR OUTPUT. A 14.318 MHz TTL level clock signal to generate the clock for on-chip 8254.

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December 1991

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Pin Name	Pin Number	Pin Type	Description
<b>Miscellaneous (Continued)</b>			
GND	TBA	I	GROUND: 0V
VCC	TBA	I	POWER: +5V