OKI

'94 VOICE SYNTHESIS LSI DATA BOOK

OKI

'94 Data Book for VOICE SYNTHESIS LSI

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OKI
VOICE SYNTHESIS LSI DATA BOOK 1994

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INTRODUCTION

1. VOICE SYNTHESIS LSI PRODUCTS

OKI SPEECH LSI PRODUCTS

·SYNTHESIZER

Internal Mask-ROM -MSM6375 FAMILY-	MSM6372	128Kbit	Internal Mask-ROM -MSM6650 FAMILY-	MSM6652	288Kbit
	MSM6373	256Kbit		MSM6653	544Kbit
	MSM6374	512Kbit		MSM6654	1.0Mbit
	MSM6375	1Mbit		MSM6655	1.5Mbit
				MSM6656	2.0Mbit

Internal OTP	MSM63P74	6375 Family
	MSM66P54	6650 Family
	MSM6379 , MSM6378A	for Voice Card

External ROM	MSM6376	6375 Family
	MSM6650	6650 Family
	MSM6295	4 channel mixing

Prototype	MSM5205
	MSM6585

·RECORDER

Special memory Type	MSM6388	4 bit ADPCM
	MSM6588	3 or 4bit ADPCM
	MSM6688	3 or 4bit ADPCM
	MSM6788	SBC

Special memory for MSM6388 , MSM6588 , MSM6688 , MSM6788

Serial Voice Register	MSM6586	256Kbit
	MSM6587	512Kbit
Serial Voice ROM	MSM6389	1Mbit
	MSM6684	4Mbit
	MSM6685	8Mbit
	MSM6595	1Mbit
	MSM6596	2Mbit
	MSM6597	3Mbit

Standard memory Type	MSM6258
	MSM6310

Prototype	MSM5218

·PITCH CONTROL

MSM6322
MSM6722

·SPEAKER AMP

MSC1191
MSC1192

·DEVELOPMENT SUPPORT TOOL

Analysis/Editing Tool	AR761	Working on PC9801 Japanese
	AR76-202	Working on IBM-PC English

Support Tool for M6378A	Anawriter
	Buckup Unit
	Parawriter

Demonstration Board

2. PRODUCTS AND TYPICAL CHARACTERISTICS

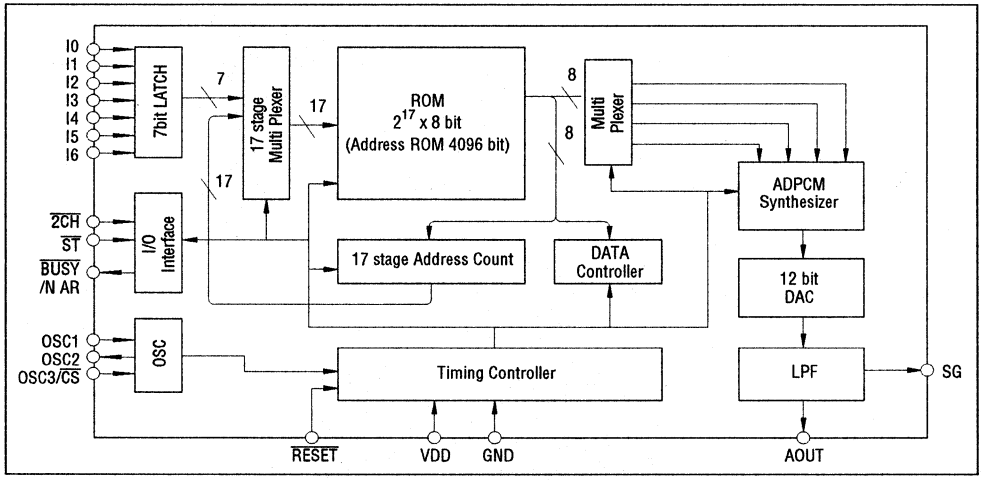
2-1) VOICE SYNTHESIS LSI PRODUCTS (Fixed message type)

There are various types of voice synthesizer's suitable for a large number of applications, such as: A) Built-in ROM synthesizers tailored for mass production of "fixed messages". B) An OTP(One Time Programmable) device which adds versatility in applications where low volume, multiple messages, and field programmability are needed. C) Voice synthesizers using external memory for extended playback requirements.

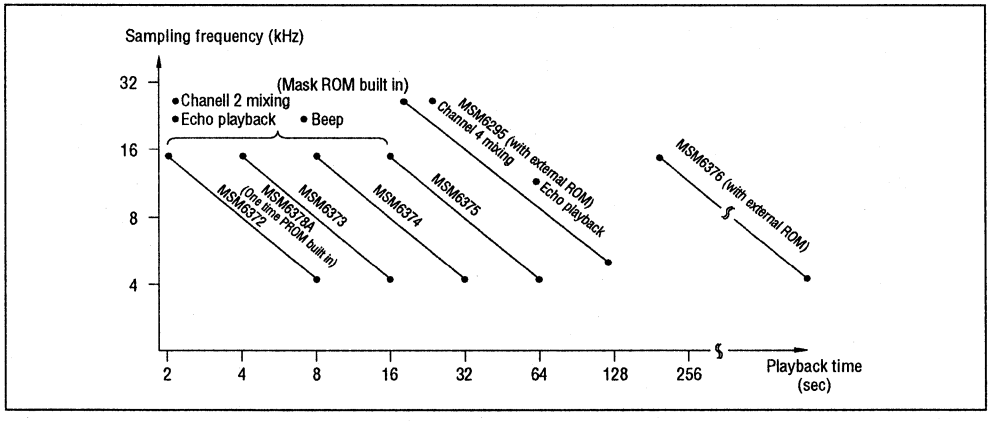
Oki's voice synthesizers have many common characteristics, such as the ADPCM method, internal D/A converters, a wide range of sampling rates to choose from, and excellent sound fidelity.

Furthermore, the mask ROM synthesizers contain a LPF (Low Pass Filter), 2-channel mixing capability, echo reproduction, and variable Beep Tone functions.

MSM6375 Block Diagram

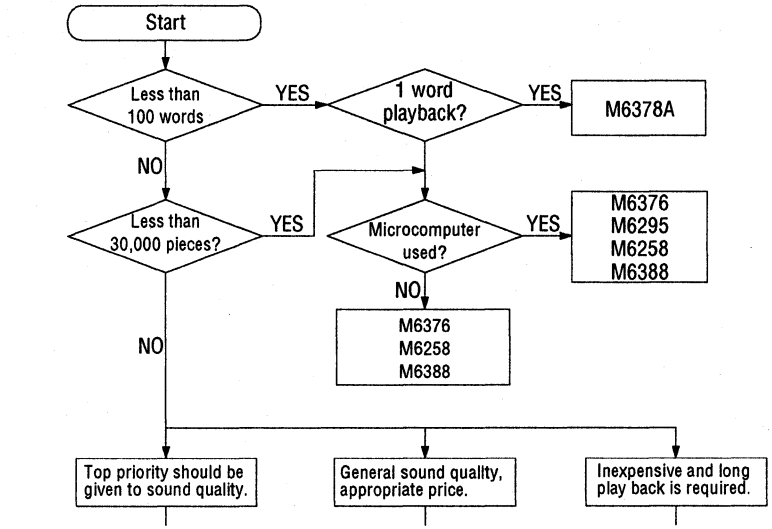


PRODUCT CONFIGURATION



Product name	MSM6372	MSM6373	MSM6374	MSM6375	MSM63P74	MSM6378A	MSM6376	MSM6295	MSM5205	MSM6585
Coding	4-bit ADPCM method								3/4-bit ADPCM	4-bit ADPCM
ROM type	Mask ROM built-in				Built-in OPT		External		—	—
ROM capacity	128K bits	256K bits	512K bits	1M bits	512K bits	256K bits	Up to 16M bits	Up to 2M bits	—	—
Synthesis time (sampling frequeny)	8 sec (4kHz) 5sec (6.4kHz) 2 sec (16kHz)	16 sec (4kHz) 10 sec (6.4kHz) 4 sec (16kHz)	32 sec (4kHz) 20 sec (6.4kHz) 8 sec (16kHz)	64 sec (4kHz) 40 sec (6.4kHz) 16 sec (16kHz)	32 sec (4kHz) 20 sec (6.4kHz) 8 sec (16kHz)	16 sec (4kHz) 8 sec (8kHz) 4 sec (16kHz)	17 min (4kHz) 10 min (6.4kHz) 256 sec (16kHz)	128 sec (4kHz) 16 sec (32kHz)	By external circuit	
Sampling frequency	4.0, 6.4, 8.0kHz (f_{OSC} = 64kHz) 8.0, 12.8, 16.0kHz(f_{OSC} = 128kHz)					4.0kHz ~ 16.0 kHz	4.0kHz ~ 32.0 kHz	8.0kHz ~ 32.0 kHz	4.0, 6.0 8.0 kHz	4.0, 8.0 16.0, 32.0kHz
Clock frequency	64 ~ 128kHz (LPF selected) 64 ~ 256kHz (DAC selected)					64 ~ 256kHz (RC oscillation)	64 ~ 128kHz	1 ~ 4MHz	384kHz	640kHz
D-A converter	12-bit								10-bit	12-bit
Low-pass filter	–24dB/oct							None	None	–40dB/oct
Supply voltage	2.4 ~ 5.5V (DAC selected) 2.7 ~ 5.5V (LPF selected, f_{OSC} = 64kHZ)				2.7 ~ 5.5V	2.4 ~ 5.5V	4.5 ~ 5.5V		3.0 ~ 6.0V	4.5 ~ 5.5V
Operating current	10mA				20mA		10mA		4mA	10mA
Standby current	10µA				100µA	10µA		—	—	—
Package	Chip, 18-pin DIP 24-pin SOP				20-pin DIP	16-pin DIP	64-pin QFP	44-pin QFP 40-pin DIP	18-pin DIP	
Voice analysis tool	AR76-202					ANA WRITER AR76-202	AR76-202			
Other characteristics	Channel 2 mixing, echo playback beep tones					Power ON start	MSM6373/74/75 evaluation	4 Channel mixing, echo playback	—	—

SELECTION GUIDE



- SAMPLING FREQUENCY
  fs=8-16kHz
- High quality music or voice playback
  Less than 2 sec: M6372
  Less than 4 sec: M6373,M6652
  Less than 8 sec: M6374,M6653
  Less than 16 sec: M6375,M6654
  More than 16 sec: M6376,M6655 M6258,M6656 M6295 M6388

- fs=6.4kHz
- High quality playback or voice
  Less than 5 sec: M6372
  Less than 10 sec: M6373,M6652
  Less than 20 sec: M6374,M6653
  Less than 40 sec: M6375,M6654
  More than 40 sec: M6376,M6655 M6258,M6656 M6295 M6388

- fs=4.0kHz
- Playback of low frequency
  Less than 8 sec: M6372
  Less than 16 sec: M6373,M6652
  Less than 32 sec: M6374,M6653
  Less than 64 sec: M6375,M6654
  More than 64 sec: M6376,M6655 M6258,M6656 M6295 M6388

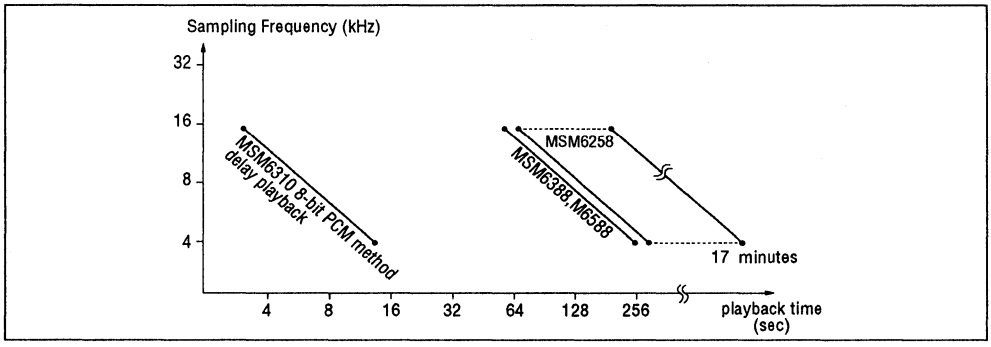
2-2) RECORDING AND PLAYBACK LSI LINE-UP

GENERAL DESCRIPTION

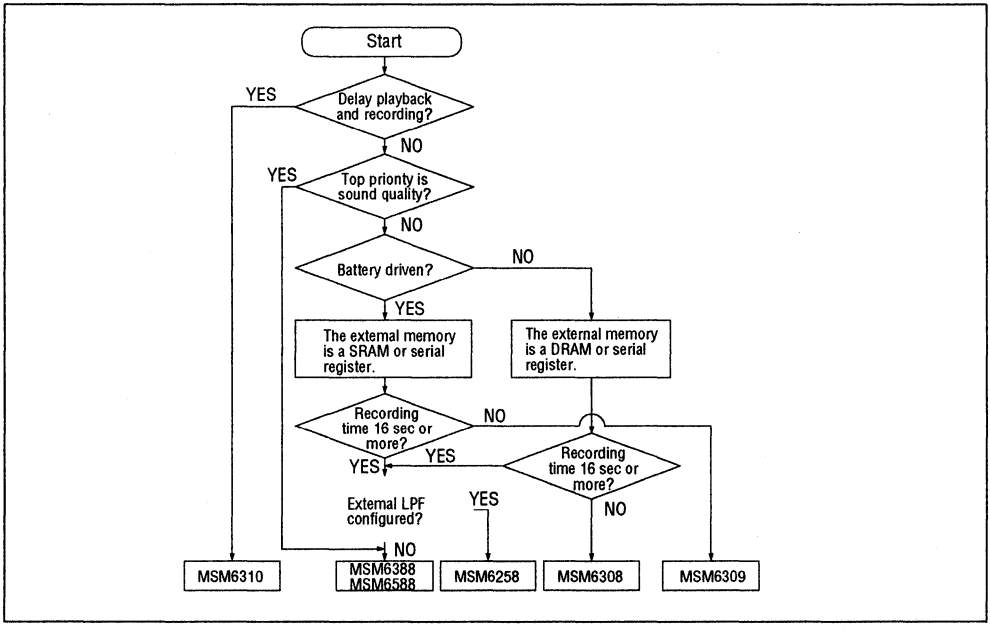
There are two basic types of record/playback devices which use external memory for data storage, LSI's using ADPCM processing, and LSI's using PCM processing.

The ADPCM processors incorporate an A/D and D/A of up to 12-bits, LPF (Low Pass Filter) up to –40dB/octave (outband attenuator) for input and output, and microphone and line amplification. These devices directly address from 256-bits to 16Mega bits of external memory. Under processor control and with additional external circuitry, almost any external memory requirement can be met.

PRODUCT CONFIGURATION



SELECTION GUIDE



TYPICAL CHARACTERISTICS

Product name	MSM6258 (V)	MSM6388	MSM6588	MSM6310	MSM5218
Coding	3/4-bit ADPCM	4-bit ADPCM method	3/4-bit ADPCM	8-bit PCM	3/4-bit ADPCM
Memory type to be connected (capacity)	DRAM (16Mb) SRAM (4Mb)	Serial Voice register Serial Voice ROM (4Mb)		DRAM (512Kb)	–
Maximum recording time (sampling frequency)	DRAM 17 min (4kHz) SRAM 256 sec (4kHz)	256 sec (4kHz) 128 sec (8kHz)	256 sec (5.3kHz x 3bit) 170 sec (8kHz x 3bit)	16 sec (4kHz) 8 sec (8kHz)	By external circuit
Number of words/phrases	7 words *1	8 words *1		1 word (Delay playback)	Determined by external circuity
Sampling frequency	4.0kHz ~ 15.6kHz	4.0kHz ~ 16.0kHz		4.0kHz ~ 16.0kHz	4.0, 6.0 8.0kHz
Clock frequency	4MHz ~ 8MHz	1.5MHz ~ 4MHz	4MHz ~ 8.192MHz	4MHz ~ 8.2MHz	384kHz
Microphone/line amplifier	External	Built-in		Built in Line amplifier	None
A-D converter	8 bits	12 bits		8 bits	None
D-A converter	10 bits	12 bits		8 bits	10 bits
Low-pass filter	None	–40dB/oct		–24dB/oct	None
Supply voltage	3.5 ~ 6.0V	3.5 ~ 5.5V		4.5 ~ 5.5V	3.0 ~ 6.0V
Operating current	4mA	10mA			6mA
Standby current	10µA	10µA			–
Package	40-pin DIP 44-pin QFP 60-pin QFP 44-pin PLCC 68-pin PLCC	44-pin QFP			24-pin DIP

*1 During MCU or microprocessor control, the number of words depends on the MCU and its associated circuity driving the speech chip.

2-3) VOICE PITCH CONTROL LSI

GENERAL DESCRIPTION

MSM6322 is a voice pitch control LSI providing a voice pitch changer function. This LSI provides a 17-step voice pitch conversion function using the PCM method. This single chip solution contains all necessary functions to realize a voice changer, such as A-D conversion, D-A conversion, LPF, microphone amplification, and line amplification.

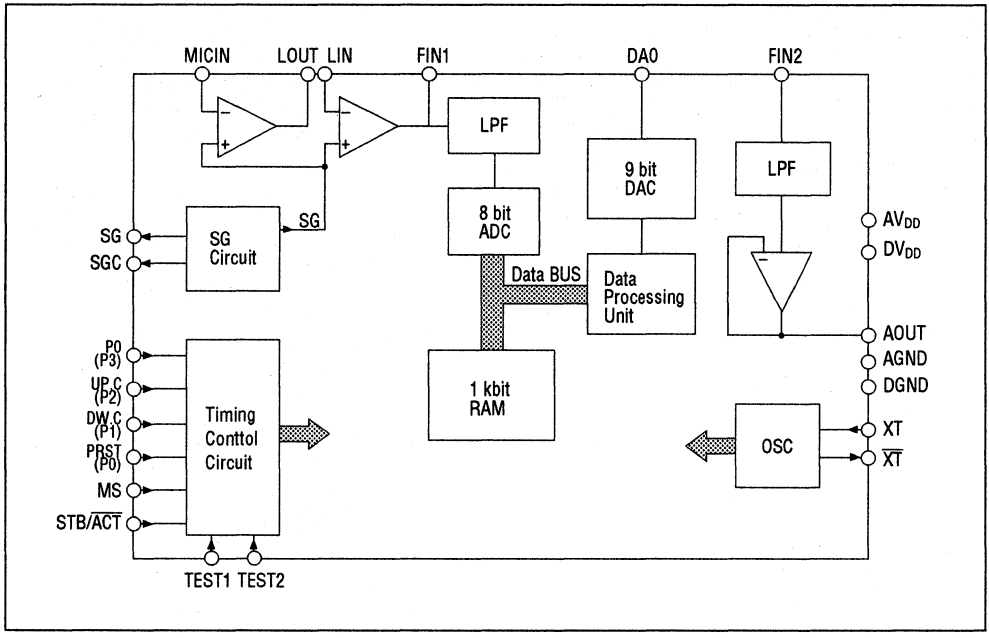
FEATURES

- 17-step voice pitch conversion using the 8-bit PCM method
- Sampling frequency: Input 8 kHz, output 4 to 16 kHz
- 8-bit A-D converter, 9-bit D-A converter, LPF, microphone amplifier, and line amplifier built-in
- 24-pin flat package

VOICE PITCH CONTROL LSI

Product name	MSM6322
Function	17-step voice pitch conversion
Coding method	8-bit PCM method
Sampling frequency	Input 8kHz, Output 4k~16kHz
Clock frequency	4MHz
Built-in analog circuit	8-bit A-D converter, 9-bit D-A converter, LPF, microphone amplifier, line amplifier
Supply voltage	4.0-6.0V
Operating current	10mA
Standby current	10μA
Package	24-pin flat

MSM6322 BLOCK DIAGRAM



2-4) DIRECT DRIVE SPEAKER AMPLIFIER

GENERAL DESCRIPTION

MSC 1191/1192 is a speaker drive amplifier IC for Oki's voice LSIs. This is a power amplifier with low consumption at a low voltage, and directly drives a speaker without a coupling capacitor.

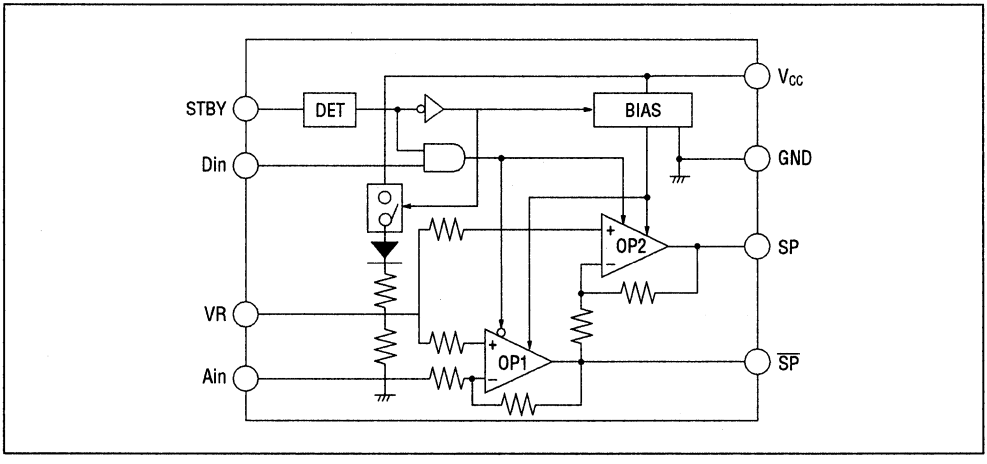
FEATURES

- Operating at a low voltage
- A voice analog signal input pin and a digital signal input pin such as an alarm signal is provided
- The speaker can be directly connected between the differential output pins.
- Standby function provided

DIRECT DRIVE SPEAKER AMPLIFIER

Product name	MSC1191/MSC1192
Function	Speaker drive amplifier
Supply voltage	2.0 ~ 6.0V
Maximum output current	250mA
No-load operating current	1.5mA (TYP)
Standby current	1mA (MAX)
Package	Chip, 8-pin DIP, 8-pin SOP

MSC1191/1192 BLOCK DIAGRAM



Note: MSC1191: Standby mode is activated by "H" level to the input STBY
MSC1192: Standby mode is activated by "L" level to the input STBY

Features of Oki Voice Synthesis LSIs

The major features of Oki voice synthesis LSIs are summarized below.

(1) Quality of Synthesis

(i) Good quality sound with a high degree of naturalness.

(ii) Synthesis of sound effects, musical instruments, and animal sounds also possible.

(2) Hardware

(i) Easy to handle (built-in ROM) SINGLE-chip devices ready for simple application.

(ii) A range of voice synthesis LSIs with various built-in ROM sizes to meet diversified market needs.

(iii) Low power requirements due to CMOS with low fundamental oscillating frequency–ideal also for battery operated applications.

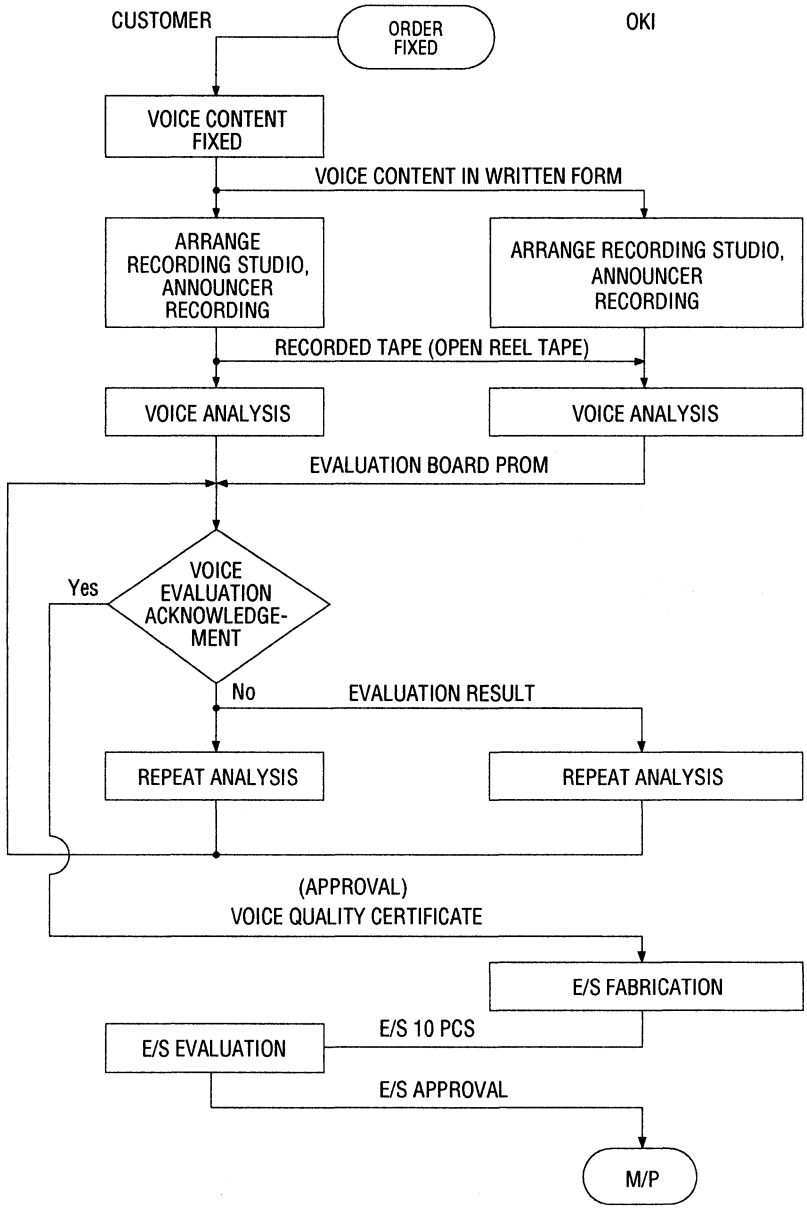
(3) Software

(i) Simple and precise analysis for any customized sound/voice.

Because of the fine sound quality achieved for a wide range of applications, Oki voice synthesis LSIs are used worldwide by a large number of client in numerous applications.

3. FLOWCHART FOR BUILT-IN ROM VOICE SYNTHESIS DEVELOPMENT

(MSM6372, MSM6373, MSM6374, MSM6375, and MSM6376)



4. USER ANALYSIS SUPPORT TOOLS

4-1) SPEECH DEVELOPMENT SYSTEM

OUTLINE OF AR76-202

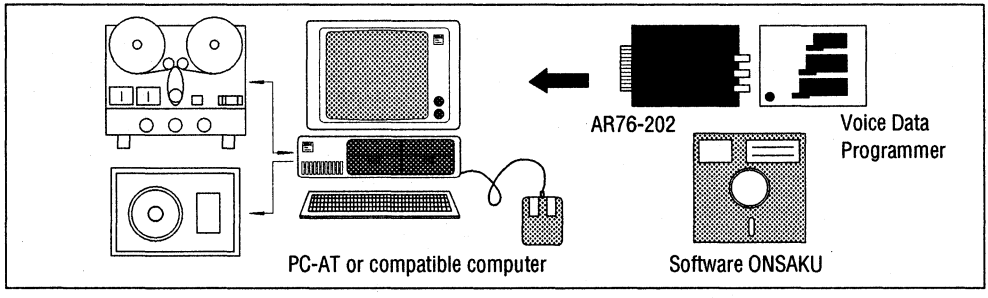
AR76-202 is fully PC supported. Included with the shipment is a standard 16-bit PC slot card, an EPROM programmer, a software driver and an English manual.

The host environment should consist of a PC-AT® or 100% compatible machine equipped with a harddisk, VGA® graphic adaptor and serial mouse. A printer is useful but not essential. The driver software runs under DOS 3.2 and higher on a 640K machine. However, for speech phrases of more than 15 seconds, EMS expansions are strongly recommended in order to record long phrases in one piece without concatenations. A tape deck or cassette player is needed as an analog source which can be connected directly to the installed board as well as a loudspeaker.

TARGET LSIs

MSM6372/73/74/75	MSM6585	MSM6378A	MSM6595
MSM6376	MSM6295	MSM5205	MSM6596
MSM63P74	MSM6258		

SYSTEM CONFIGURATION



PERFORMANCE

What AR76-202 does for you comprises all essentially demanded functions from recording all the way up to EPROM programming, plus a few extras. In detail:

- Recording into host memory through an audio line input
- Playback of a recording from host memory via speaker
- Editing of a recorded voice file, including
  - -Amplitude manipulation
  - -Silencing/Silence insertion
  - -Fading/Cut/Copy/Paste
- HEX-file or BIN-file generation
- EPROM/OTP programming
- EPROM duplication
- Random access playback of speech files
- Covers all OKI speech LSIs, including OTP synthesizers
- Makes full use of Expanded Memory System

HARDWARE

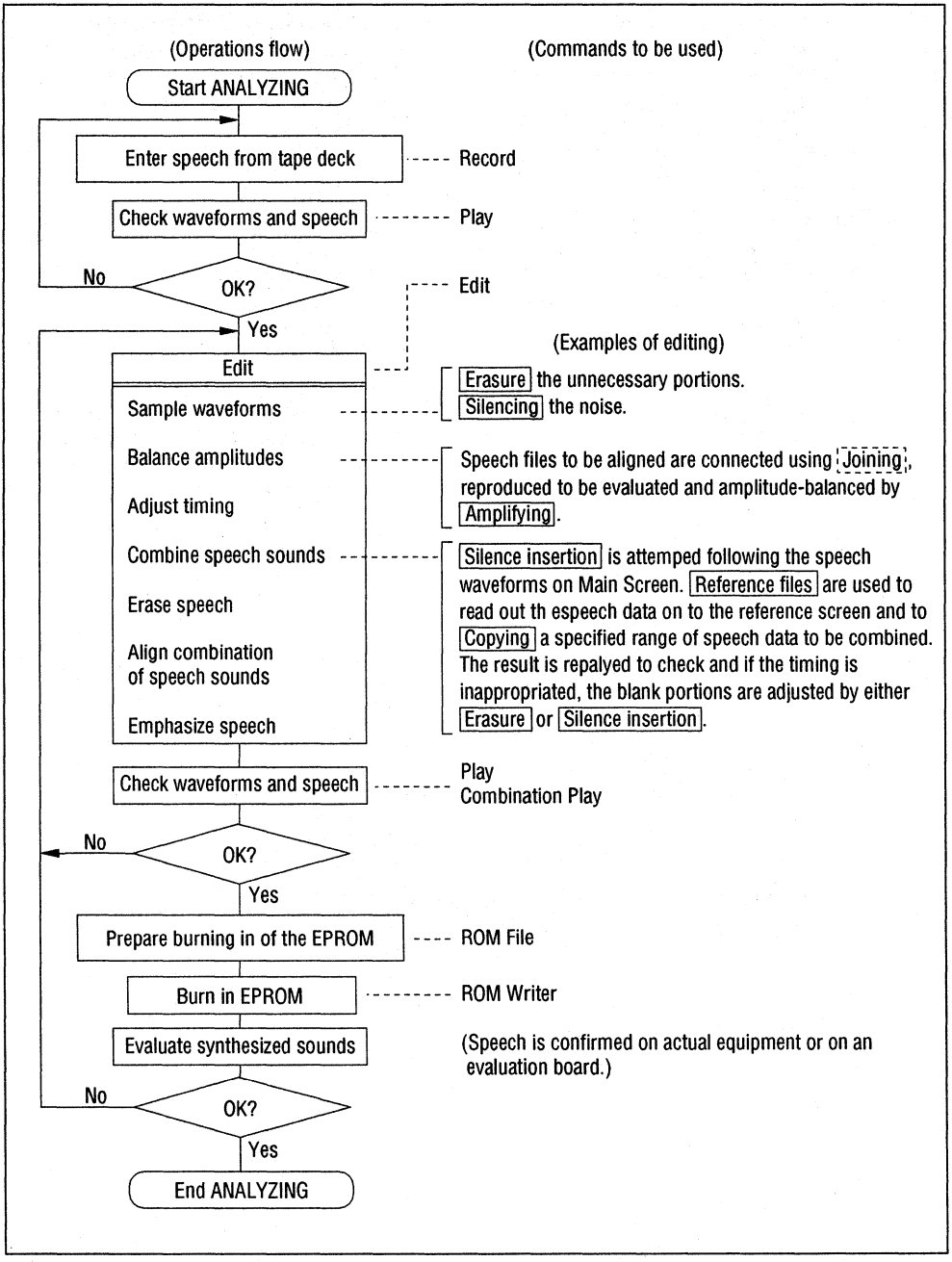
Measuring approximately 284(L) x 107(W) mm, the slot card is designed around OKI Electric's MSM5218 speech recorder LSI in connection with external 12-bit converters plus low pass filter featuring –48dB attenuation per octave. Both analog and digital circuits are provided through to analog inputs and outputs for direct connection of a tape deck and a speaker. Likewise, the external EPROM/OTP writer is linked to the card's interface.

SOFTWARE

The software driver, "ONSAKU", is fully graphics oriented and operable with keys or preferably with a mouse. The primary application of the software is for editing raw speech recordings. This includes amplitude amplification and attenuation, cutting, copying and insertion of selected excerpts. Additionally, the auto-face in/fade out function helps to save time. Using this software is like using a modern wordprocessor. A recorded waveform is displayed on the graphic screen in three scales allowing for precise editing at any point.

"ONSAKU" can be started with a variety of option switches in order to adjust operating parameters for more convenience and easier further processing.

GENERAL FLOW OF OPERATIONS



4-2) ANAWRITER, PARAWRITER, BACK-UP SYSTEM (FOR MSM6378A)

ANAWRITER 6378 MARK II

GENERAL DESCRIPTION

The ANAWRITER 6378 MARK II is a tool dedicated to voice analysis for the Oki MSM6378A 256 Kbit OTP (one-time programmable device.)

It can run on 90 to 250 V AC. Therefore, it can be used in any country without voltage modifications.

It has two input jacks: microphone input (with built-in ALC) and line input jacks.

Programming time in a MSM6378A is 8 seconds, including time for verify.

A ROM (EPROM) master can be made by preparing a backup using an external I/F. If a PARAWRITER is used with the master ROM, write and verify for ten MSM6378A can be simultaneously completed within 11 seconds.

FEATURES

- Voice analysis: Oki ADPCM MSM6378A
- Microphone input: 600 Ω, with built-in ALC
- Line input: 10KΩ, -10dB
- Recording monitor: Input level is displayed on a bar graph LED
- Play monitor: Reproduced sound can be heard from a built-in speaker
- Functions: REC, PLAY, WRITE, PLAYBACK FROM PROGRAMMED MSM6378A
- Options: Backup (master ROM generation tool), PARAWRITER (ten-ROM parallel writing tool)
- Supply voltage: 90 ~ 250V AC
- Write and verify time: 8.0 seconds for one device, 11.0 seconds (PARAWRITER) for ten devices.

RECORDING TIME

Sampling frequency (kHz)	Recording time (sec)
4	15.6
6	10.4
8	7.8
10	6.2
12	5.2
14	4.5
16	3.9

OPERATION

a. Power-on

Connect the AC power supply (1), and turn on the power switch (2).

- The power lamp (11) is lit up.
- "88" is displayed on the indicator (14). Then, it is changed to "4".
- The sampling lamp (9) is lit.

b. Switching of sampling frequency

- Pressing the sampling frequency selector switch (15) selects another sampling frequency.
- The indicator (14) shows the selected sampling frequency.
- Each time the sampling frequency switch (15) is pressed, the sampling frequency changes as follows:

$$\rightarrow 4 \rightarrow 6 \rightarrow 8 \rightarrow 10 \rightarrow 12 \rightarrow 14 \rightarrow 16 \rightarrow$$

- While a sampling frequency is indicated on the sampling indicator (14), the sampling lamp remains on.

c. Recording

Insert the microphone connector into the microphone input jack (6), or set a sound source to the input jack (7). When sound is entered, the level meter (4) works.

Pressing the record switch (16) starts recording.

At the same time, ADPCM analysis is performed.

- The lamp for the record switch (16) is lit.
- During recording, the lamp (10) remains on.
- The indicator (14) shows the residual recording time.

When recording is complete, the indicator (14) shows a sampling frequency again.

d. Play (checking of recorded voice)

Pressing the switch (17) begins voice reproduction. Sound volume can be adjusted using the monitor control (5). During play, the lamp for the play switch (17) is lit.

e. Writing to 6378

Check the direction of 6378 with the lever of TEXTOOL® (20) raised. Place the 6378 in TEXTOOL® socket, and lower the lever.

Make sure that 6378 is placed horizontally.

Pressing the 6378 write switch starts writing.

During writing, the 6378 busy lamp (12), and write lamp (18) are lit. In eight seconds, write and verify are completed.

If the error lamp (13) comes on when writing is over, it means writing has not been done normally.

In this case, the indicator (14) shows an error code.

E0: 6378 is not in the TEXTOOL® socket, or is not in the socket correctly.

E3: An error occurred during writing. So, writing was aborted.

Any other error :
May mean a failure has occurred with the ANAWRITER.

If any key is pressed when the indicator (14) is displaying an error, the display is changed to a sampling frequency.

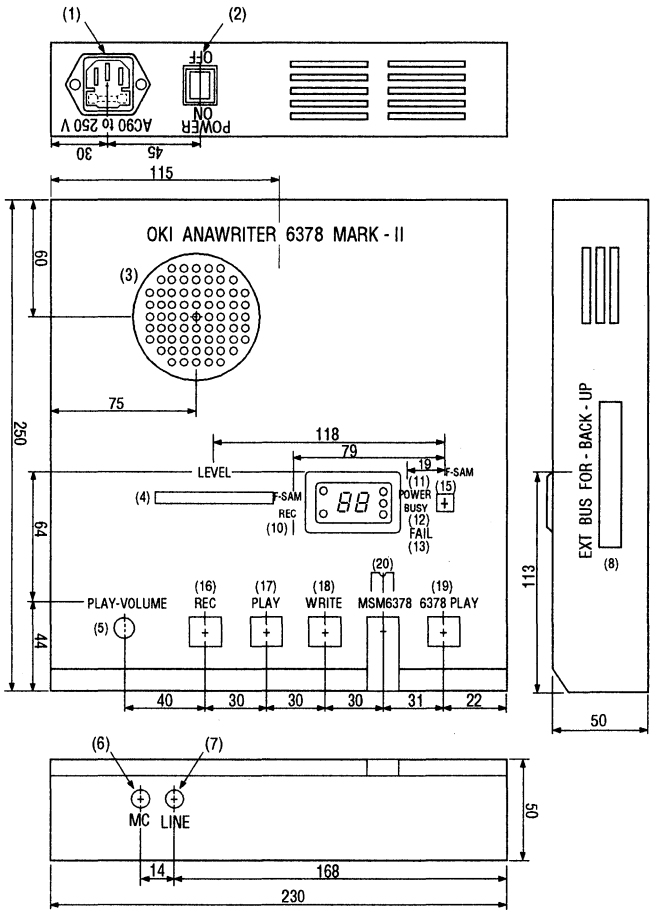
f. Reproduction from 6378

Check the direction of the 6378 with the lever of TEXTOOL®(20) raised. Place it in TEXTOOL® socket, and lower the lever to fix it.

Sound volume can be adjusted using the monitor control (5) in play.

During voice reproduction, the lamp for the 6378 play switch (19) and the 6378 busy lamp (12) are lit.

MECHANICAL DIMENSION



PARAWRITER

GENERAL DESCRIPTION

The PARAWRITER writes data for up to ten MSM6378As at a time using a master EPROM (27256), which is prepared with the EPROM BACKUP writer.

SPECIFICATIONS

Master ROM : 27C256 or 27256

Programmable device : MSM6378A

Writing time : 11 seconds (with data written to ten MSM6378As simultaneously)

Function keys : LOAD Reads data from EPROM.
WRITE Writes data to MSM6378A
RESET Resets an error lamp.

Buzzer	:	
	Write error	Beep
	Normal end of writing	Beep
	Upon loading	Beep
	Upon resetting	Beep

FUNCTION KEYS

LOAD key	Loads data from a master EPROM (27256) to PARAWRITER.
WRITE key	Writes data to up to ten MSM6378As simultaneously.
RESET key	Resets any error lamp 1 through 10.

FUNCTION LAMP

BUSY lamp Lit during loading/writing.

LAMPS 1 THROUGH 10

Any of the lamps 1 through 10 is lit if in MSM6378A is not placed in the 16-pin TEXTOOL socket, or if a write error occurs. More precisely, a lamp for the position where the MSM6378A is not placed is lit upon completion of writing.

If an error occurs during writing to the MSM6378A, the lamp for the position where the error has occurred is lit. Pressing the RESET switch turns off the lamp.

BACK-UP UNIT

GENERAL DESCRIPTION

BACKUP is an EPROM writer for a 27256 EPROM. It loads the EPROM with voice and other data, which are generated using the ANAWRITER 6378 MARK II. BACKUP is connected to the 6378 ANAWRITER through a 40-pin flat cable.

FEATURES

- Applicable EPROMs: 27C256 or 27256
- Functions switches : LOAD
  PLAY
  BLANK Blank check
  WRITE EPROM write
  VERIFY EPROM verify
- Function lamps : BUSY
  FAIL

FUNCTION SWITCHES CONTINUED

LOAD Loads data from EPROM to 6378 ANAWRITER.

PLAY Reproduces voice data loaded into 6378 ANAWRITER. The switch has the same function as the 6378 play switch.

BLANK Used for blank check of EPROM (27256).

WRITE Write voice data generated in 6378 to EPROM (27256). This switch invokes three modes: blank, write, and verify modes.

VERIFY Compares data in 6378 ANAWRITER with those in EPROM for verification.

FUNCTION LAMPS CONTINUED

BUSY lamp : It is lit during LOAD, BLANK, WRITE, and VERIFY.
It is not lit during PLAY.

FAIL lamp : If this lamp is lit, an error lamp is also lit.

- Upon blank check, the data in the EPROM was found not to be blank.
- A write error occurred during writing.
- A verify error occurred during verify.

5. PACKAGING

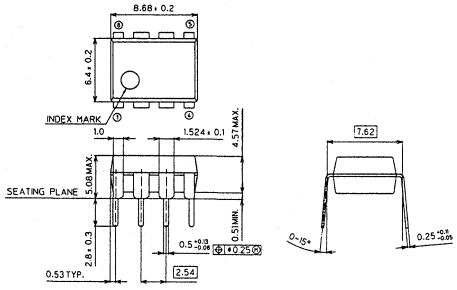
Product name	No. of Pins	Die Form	DIP	SOP/QFP				QFJ(PLCC)
			RS	MS-K	GS-K	GS-VK	GS-V1K	JS
MSM5205	18		○					
MSM6585	18		○					
MSM6295	42		○					
	44				○		○	
MSM6376	64						○	
MSM6372	18		○					
	24					○		
MSM6373	18		○					
	24					○		
MSM6374	18		○					
	24					○		
MSM6375	18		○					
	24					○		
MSM63P74	20		○					
MSM6378A	16		○					
MSM6379	16		○					
MSM6652	18		○					
	24					○		
MSM6653	18		○					
	24					○		
MSM6654	18		○					
	24					○		
MSM6655	18		○					
	24					○		
MSM6656	18		○					
	24					○		
MSM66P54	20		○					
	24					○		
MSM6650	64						○	
MSM5218	24		○					
MSM6258	60				○	○		
	68							○
MSM6258V	40		○					
	44				○		○	○

Product name	No. of Pins	Die Form	DIP	SOP/QFP				QFJ(PLCC)
			RS	MS-K	GS-K	GS-VK	GS-V1K	JS
MSM6310	44				○			
MSM6388	44						○	
MSM6588	44						○	
MSM6688	56						○	
MSM6788	80						○	
MSM6389	16		○					
	18							○
MSM6586	18							○
MSM6587	18							○
MSM6595	18		○					○
	24					○		
MSM6596	18		○					○
	24					○		
MSM6597	24					○		
MSM6690	42		○					
	44					○		
MSM6691	44					○		
MSM6791	44					○		
MSM6322	24				○			
MSM6722	24					○		
MSC1191	8	○	○	○				
MSC1192	8	○	○	○				

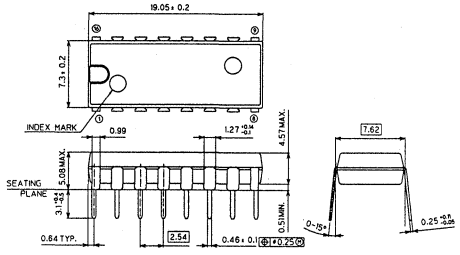
PACKAGE OUTLINES AND DIMENSIONS

• PLASTIC STANDARD DIP

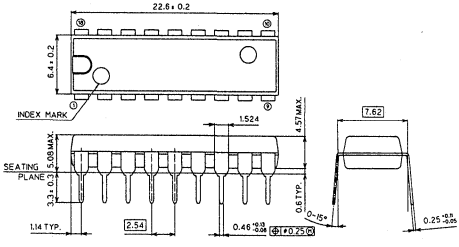
8PIN	DIP8-P-300



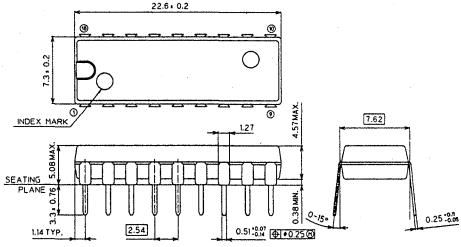
16PIN	DIP16-P-300-W1



18PIN	DIP18-P-300

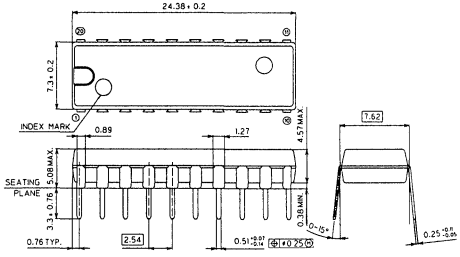


18PIN	DIP18-P-300-W1

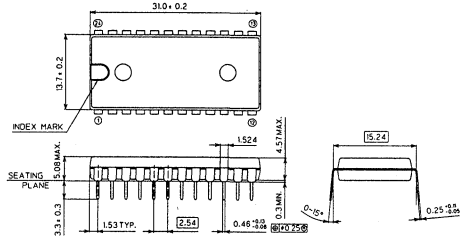


• PLASTIC STANDARD DIP

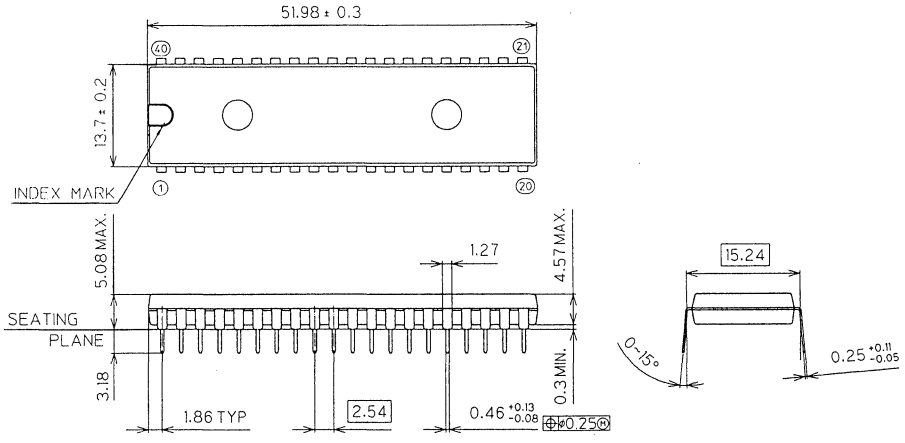
20PIN	DIP20-P-300-W1



24PIN	DIP24-P-600

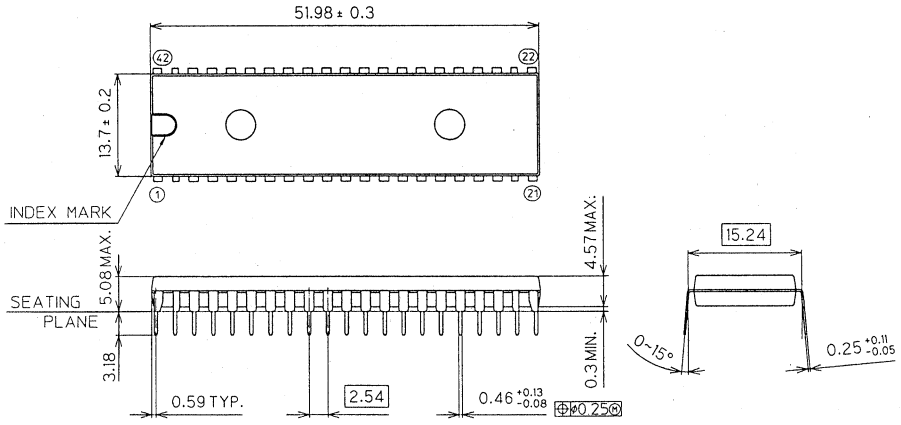


40PIN	DIP40-P-600



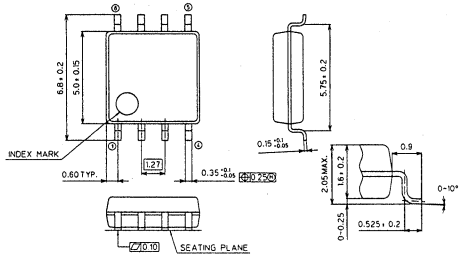
• PLASTIC STANDARD DIP

42PIN	DIP42-P-600

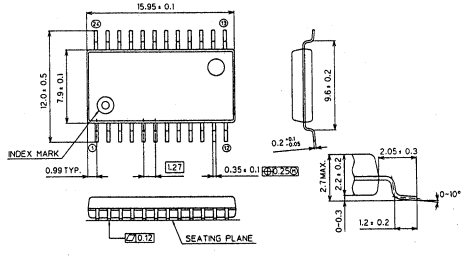


• PLASTIC SOP

8PIN	SOP8-P-250-K

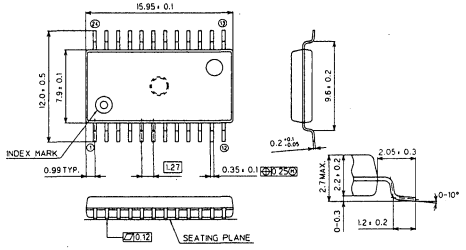


24PIN	SOP24-P-430-K



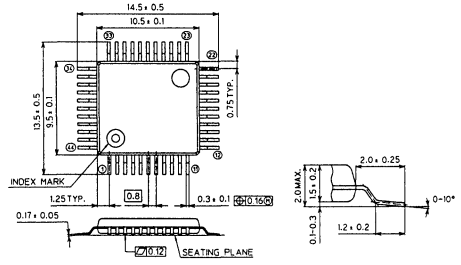
• PLASTIC SOP

24PIN	SOP24-P-430-VK

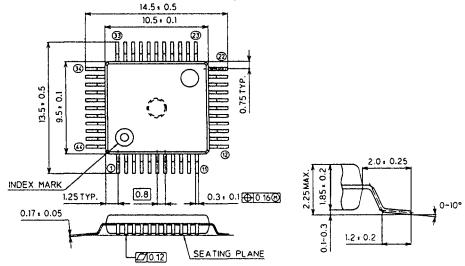


• PLASTIC QFP

44PIN	QFP44-P-910-K

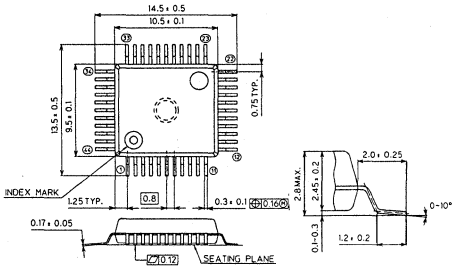


44PIN	QFP44-P-910-VK

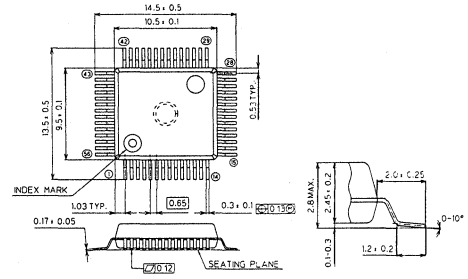


• PLASTIC QFP

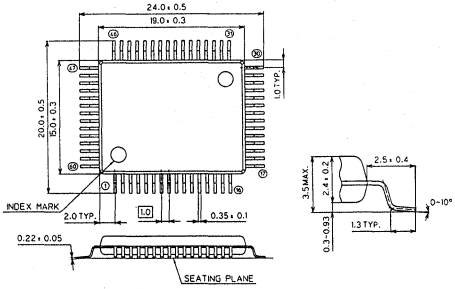
44PIN	QFP44-P-910-V1K



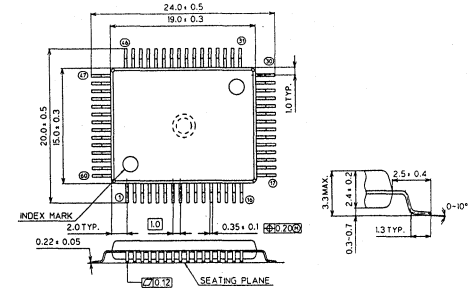
56PIN	QFP56-P-910-V1K



60PIN	QFP60-P-1519-K

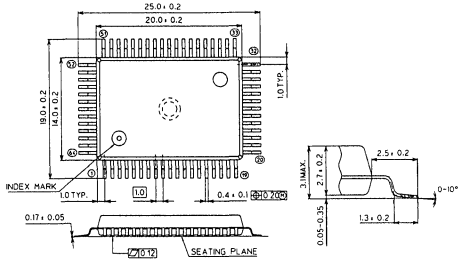


60PIN	QFP60-P-1519-VK

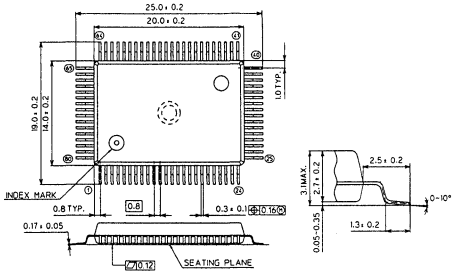


• PLASTIC QFP

64PIN	QFP64-P-1420-V1K

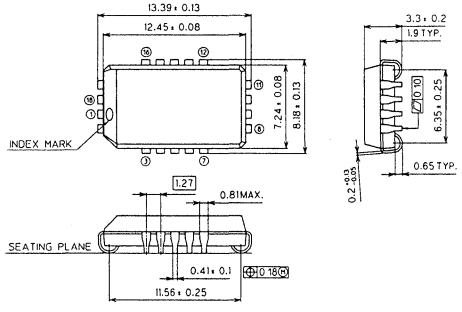


80PIN	QFP80-P-1420-V1K

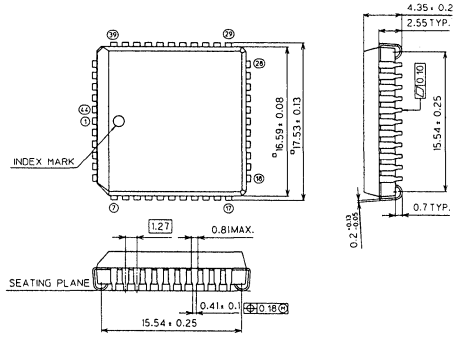


• PLASTIC QFJ (PLCC)

18PIN	QFJ18-P-R290

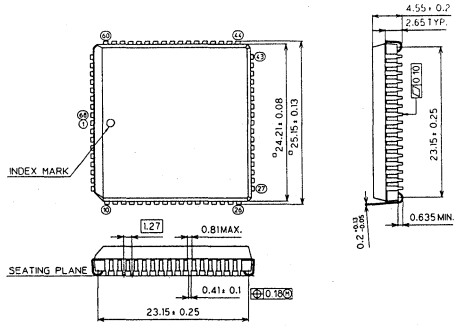


44PIN	QFJ44-P-S650



• PLASTIC QFJ (PLCC)

68PIN	QFJ68-P-S950



6. RELIABILITY

1. GENERAL DESCRIPTIONS FOR RELIABILITY

Refer to "QUALITY/RELIABILITY HANDBOOK FOR INTEGRATED CIRCUITS" on the General Descriptions of Reliability Information.

DATA SHEETS

Voice Synthesis

OKI Semiconductor

MSM5205

ADPCM SPEECH SYNTHESIS LSI

TO CUSTOMERS FOR NEW CIRCUIT DESIGN

For a new circuit design, it is recommended to use the MSM6585 as described later. The MSM5205 has a 10-bit DA converter and does not have a built-in low-pass filter. On the other hand, the MSM6585 has a 12-bit DA converter and includes a -40dB/oct low-pass filter. The sampling frequency can also be selected up to 32kHz. Therefore, the MSM6585 can realize a high quality voice.

GENERAL DESCRIPTION

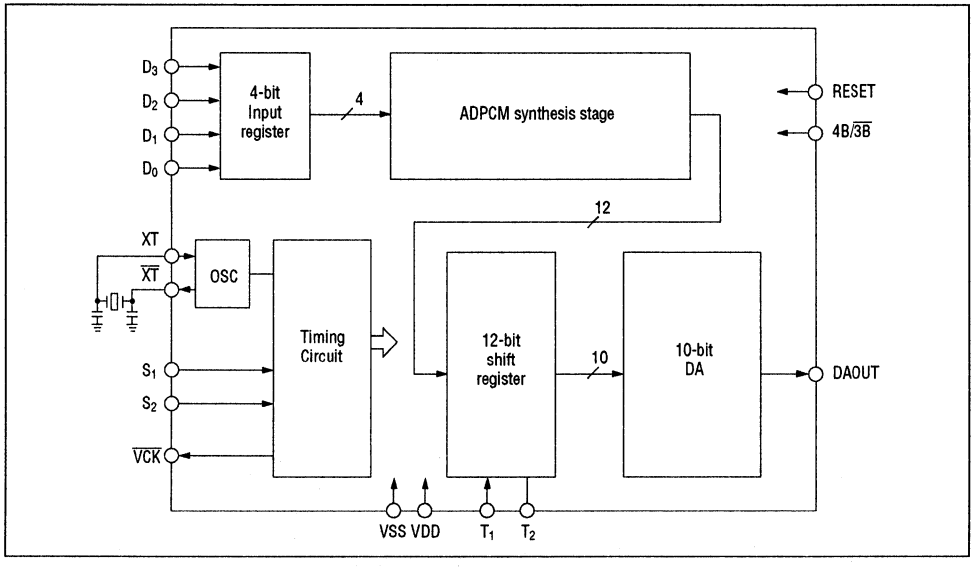
The MSM5205 is a speech synthesis integrated circuit which accepts Adaptive Differential Pulse Code Modulation (ADPCM) data. The circuit consists of synthesis stage which expands the 3- or 4-bit ADPCM data to 12-bit Pulse Code Modulation (PCM) data and a D/A stage which reproduces analog signals from the PCM data.

The MSM5205 is fabricated using Oki's advanced CMOS process which enables low-power consumption. The single power supply requirement and its availability in 18-pin molded DIP allow the MSM5205 to be ideally suited for various applications.

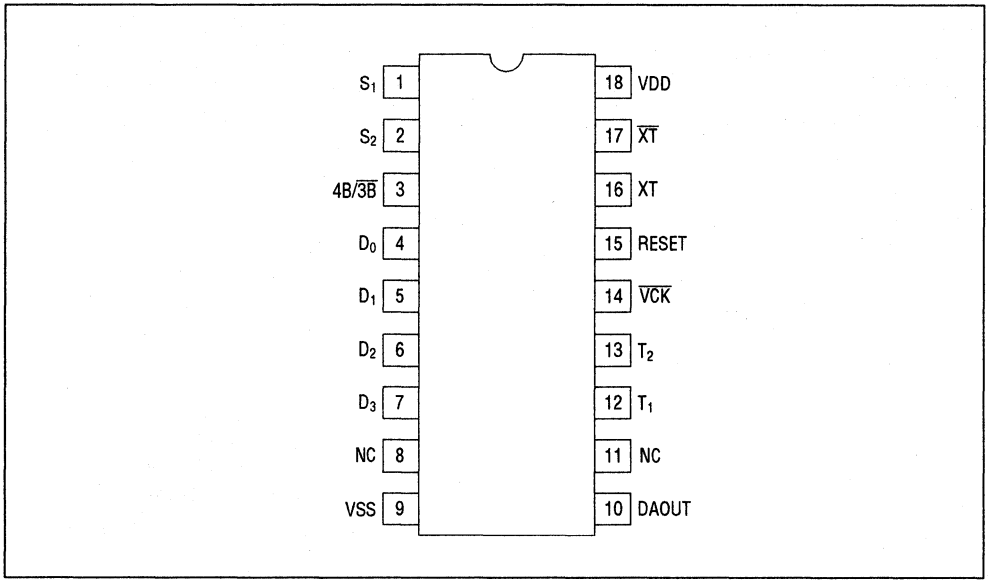
FEATURES

- 3 or 4-bit ADPCM system
- On-chip 10-bit D/A converter
- Low power consumption (10 mW typical)
- Single +5V supply
- Wide operating temperature (Ta = -30°C ~ +70°C)
- 18-pin Plastic DIP (DIP 18-P-300)

BLOCK DIAGRAM



PIN CINFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	T_a = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ VDD	V
Power dissipation	P_D	T_a = 25°C	200 max	mW
Storage temperature	T_{stg}	–	−55 ~ + 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	–	+3 ~ +6	V
Operating temperature	Top	–	−30 ~ +70	°C
Oscillator Frequency	f_{OSC}	Specified Oscillator	384 ~ 768	kHz

D.C./A.C. CHARACTERISTICS

(VDD = 5V±5%; Ta = −30°C ~ +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except T_1, T_2	4.2	–	VDD+0.3	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	V_{SS}−0.3	–	0.8	V
Input High Current	I_{IH}	V_{IN} = VDD	–	–	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V	–	–	−1	µA
Output High Current	I_{OH}	$\overline{VCK}$ pin: V_O = 4.2V	−50	–	–	µA
Output Low Current	I_{OL}	$\overline{VCK}$ pin: V_O = 0.4V	+50	–	–	µA
Operating Current	I_{DD}	f_{osc} = 384 kHz VDD = 5V	–	2	4	mA
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale; VDD = 5V	–	±4	–	LSB
DAOUT Output Impedance	V_{OR}	–	–	100	–	kΩ

PIN DESCRIPTION

Pin Name	Terminal Number	I/O
S_1	1	I
S_2	2	I

These inputs select the sampling data according to Figure 1.

4B/$\overline{3B}$	3	I

Specifies whether 3-bit or 4-bit ADPCM data is to be processed. "H" level input is 4-bit (ADPCM). "L" level input is 3-bit (ADPCM).

D_0	4	I
D_1	5	I
D_2	6	I
D_3	7	I

ADPCM data inputs. For 3-bit ADPCM data, D_0 input is not used and should be connected to ground.

VSS	9	—

Ground (0 V)

DAOUT	10	O

Output for synthesized analog signal. Peak-to-peak swing is proportional to VDD. Typical method of connection is shown Figure 2.

T_1	12	I
T_2	13	I

IC test pins used at the factory for testing purposes only. During normal operations, T_1 is grounded and T_2 is left open.

$\overline{VCK}$	14	O

This pin outputs a signal whose frequency is equal to the sampling frequency selected by the S_1, S_2 inputs. See the figure1.

PIN DESCRIPTION (continued)

Pin Name	Terminal Number	I/O
RESET	15	I

An active high input which initializes the internal circuitry. Internally, the reset pulse is synchronized with the $\overline{VCK}$ signal. To be effective, it must be true for at least twice $\overline{VCK}$ time.

XT	16	I
$\overline{XT}$	17	O

Oscillator input and output for a crystal or ceramic resonator (Figure 3).

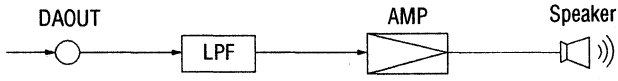
VDD	18	—

Power supply pin (Typical +5V)

S1	S2	Sampling Frequency (f_{OSC}=384kHz)
L	L	4 kHz (f_{OSC}/96)
L	H	6 kHz (f_{OSC}/64)
H	L	8 kHz (f_{OSC}/48)
H	H	Prohibited See Note *1

Note: *1 A 384kHz oscillator can be used to select 4kHz, 6kHz or 8kHz. A 768kHz oscillator can be used to select 8kHz, 12kHz or 16kHz.

Figure 1



Cut off frequency (f_{CUT}) of LPF should be related to the selected sampling frequency (f sample) by,

$$(f_{CUT}) = f\ sample/2 \times 0.85$$

Sound quality is strongly dependent on the characteristic of the low pass filter.

* If the MSM5205 is sent a stream of ADPCM data that causes greater than full scale output, the D/A output will wrap around: from the most positive rail (+5V) to the most negative rail (0.0V)

Figure 2

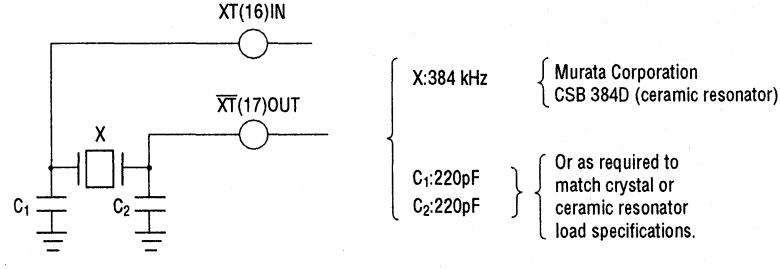


Figure 3

DA converter SN ratio improvement method

The accuracy near center of the voice waveform of this LSI may be worse due to the configuration of the DA converter. Therefore, the SN ratio can be improved by shifting the waveform center up or down. This is an extremely effective method for improving the SN ratio of a small signal or improving residual noise during silence (between 2 speech patterns.)

To put it concretely, by adding data before or after the current ADPCM data (voice data), the waveform center can be shifted as shown in Figure 4.

Adding data is as follows:

(A) section	(B) section	
0 0 0 0	1 0 0 0	
0 0 0 0	1 0 0 0	100 data
⋮	⋮	

(The ADPCM bit length is 4-bit.)

Since an offset of about 5 mV can be obtained for each 2 samples of data, it is recommended that about 100 samples of data be entered to shift the waveform center about 250 mV.

For 3-bit data, an offset of about 5 mV can be obtained for each data. Therefore, about 50 samples of data is required to be entered to shift the waveform center about 250 mV.

In the (A) section, the waveform center should be shifted up. In the (B) section, the waveform center should be shifted down. The number of data in the (A) section should be the same as that in the (B) section.

When (A) is added before voice data and (B) is added after the voice data, the output waveform is as shown in Figure 4.

Since the dynamic range is narrowed by the shifted area, some data may overflow, causing the voice to be distorted.

If this occurs, decrease the sound level about 20% and analyze the data once again. (For an overflow, see the precautions for ADPCM data creation on the next page.)

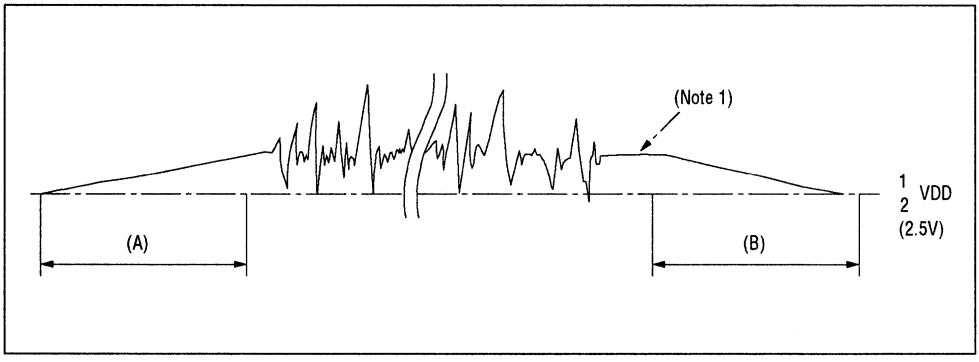


Figure 4 Waveform the DA Converter

Note 2: Voice data should be sufficiently small just prior to (B). For voice editing, insert a silence of about 10msec.

Precaution for ADPCM data creation

When voice is synthesized by the MSM5205 using ADPCM data analyzed by the MSM5218, noise may be generated in the synthesized voice.

The MSM5205 is not equipped with an overflow protection unit in the internal operation circuit even though the MSM5218 is. Therefore, although the MSM5218 produces normal voice, the MSM5205 may cause noise in the composite voice due to an overflow in the data. If this occurs, analyze and create the ADPCM data once again.

An example of a waveform when an overflow occurs and the overflow protection method is as follows :

(1) Waveform when an overflow occcurs

The observation of the output waveform from the DA converter of the MSM5205 on an oscilloscope shows that an overflowed waveform is looped as shown in Figure 5.

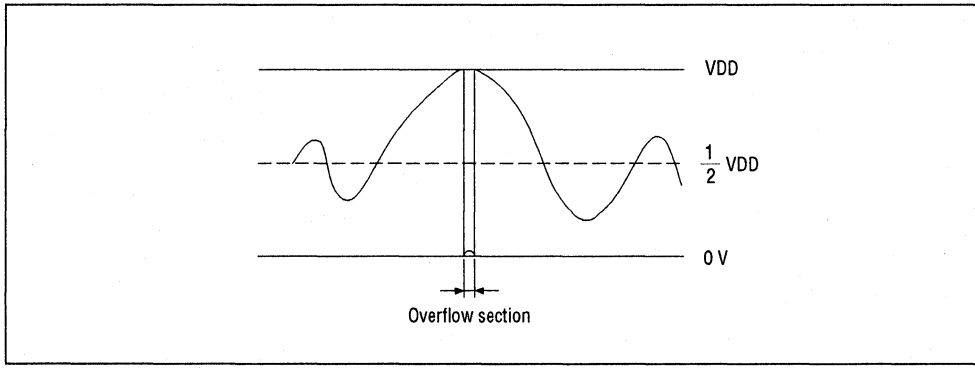


Figure 5 Output Waveform When an Overflow Occurs

(2) Overflow protection method

Even if an input waveform is not beyond the dynamic range when the ADPCM data is analyzed by the MSM5218, the output waveform may overflow due to an internal operation error.

Therefore, if the maximum amplitude level of the input waveform when the ADPCM data is analyzed by the MSM5218, is controlled to about 80% of the dynamic range or less (see Figure 6), the output waveform of the MSM5205 will not overflow, causing no noise in the composite voice.

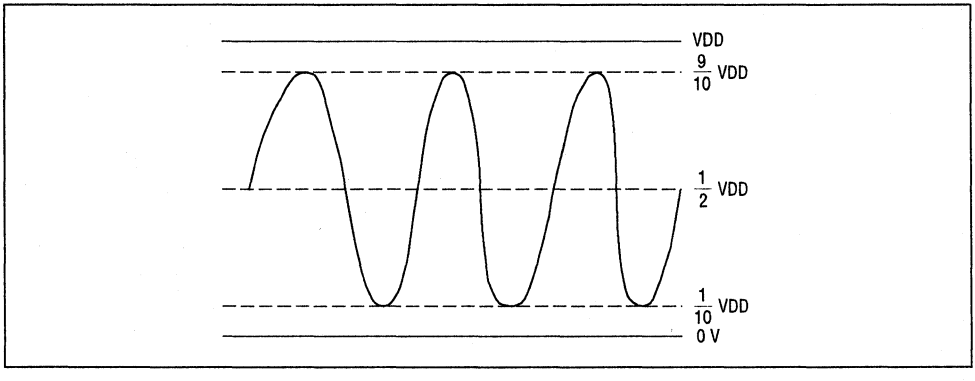
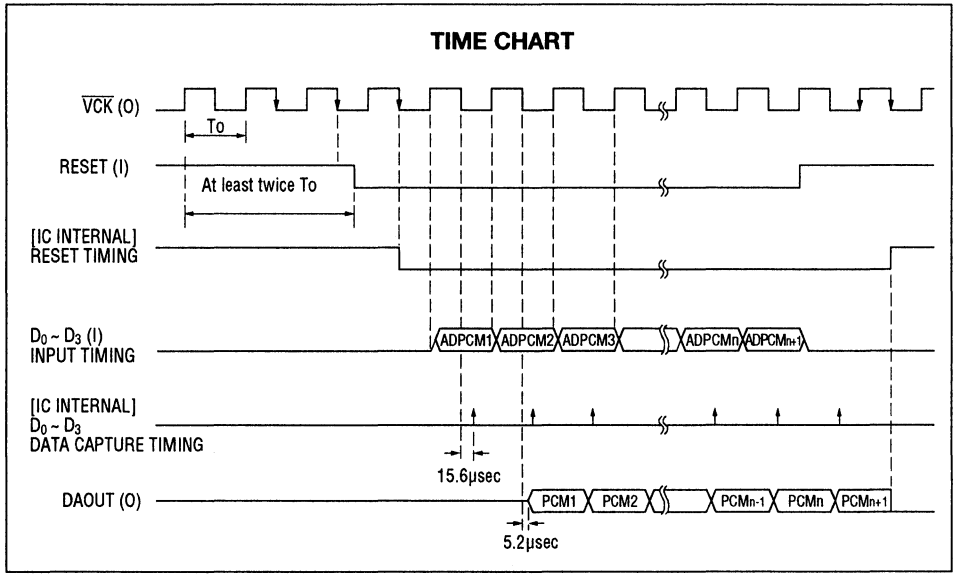


Figure 6 Waveform When the Maximum Amplitude Level of the Input Waveform is about 80% of the Dynamic Range.

Figure 7 shows the time chart for MSM5205.



Note 3: See the RESET pin description about RESET timing of the IC internal.

Figure 7

THE FOLLOWING TIMING SHOWS HOW TO APPLY THE RESET

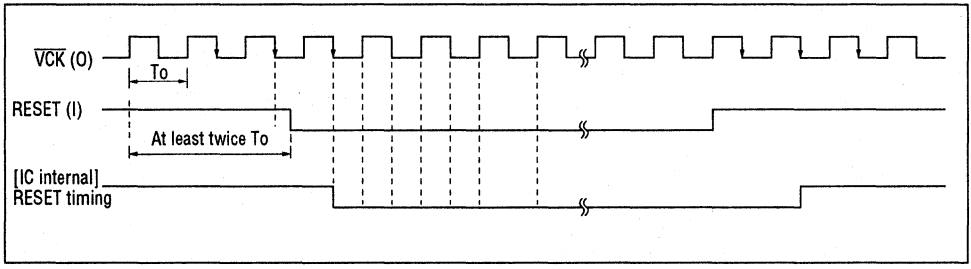


Figure 8 MSM5205 Reset Timing

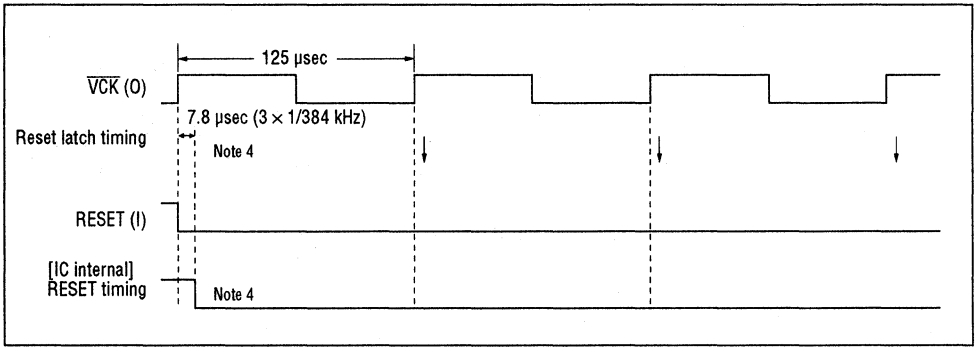


Figure 9 MSM5218 Reset Timing (8 kHz Sampling Example)

Note 4: The reset signal is latched within the LSI by the reset latch timing. Analysis is commenced by switching the external reset signal from H to L before this timing. Switching is probably best achieved by the leading edge of the VCK signal.

DISTINCTION BETWEEN MSM5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method, however, with the exception that MSM5218 is equipped with an overflow protection.

In other words, when all 12-bit PCM become '1' any further exceeding analog input would cause a data overflow which is caught and re-routed as the MSB in case of MSM5218.

MSM5205 returns to 'all bits zero' when a data overflow occurs.

Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the AD converter should be limited to 80% of the converters maximum input range.

The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

TYPICAL APPLICATION
MSM5205 TO CENTRONICS INTERFFACE CIRCUITS (f_{SAM} = 8kHz)

Figure 10 shows the MSM5205 to centronics interface circuit (f_{SAM} = 8kHz), and Figure 11 shows that timing chart.

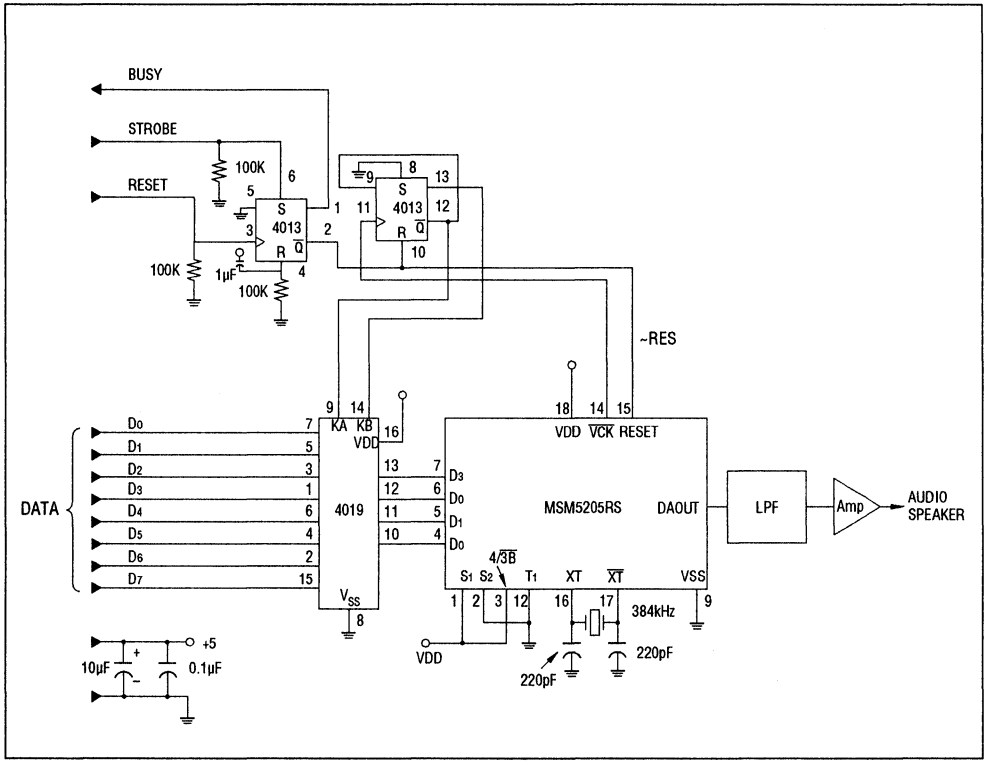


Figure 10

MSM5205 to Centronics Timing Diagram

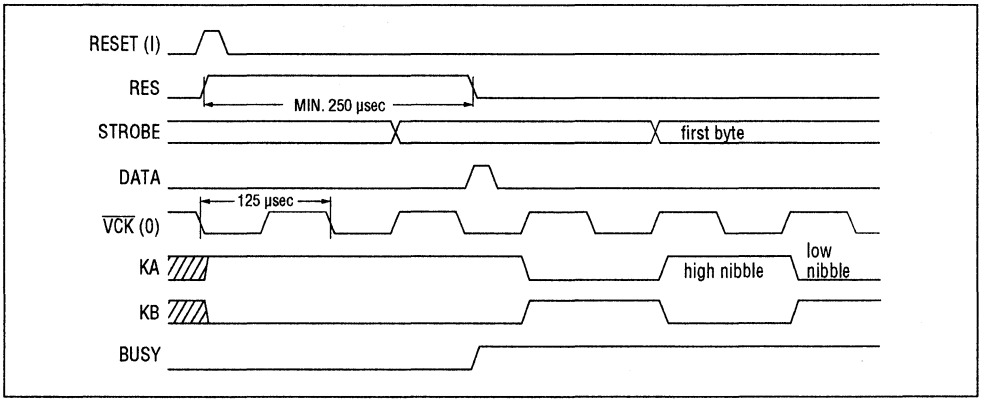


Figure 11

- **MSM5205 VOICE SYNTHESIS CIRCUIT EXAMPLE**

An example where 256k-bit EPROM are used linked together is shown in Figure 12. The timing chart for this example is provided in Figure 13.

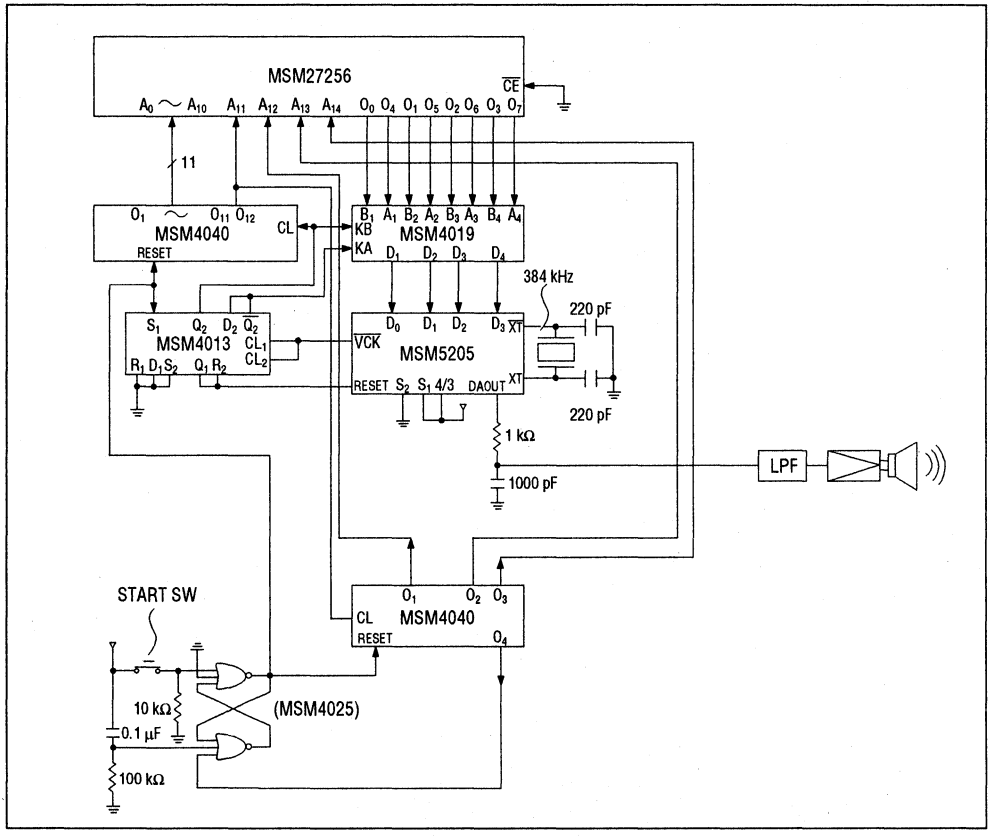


Figure 12

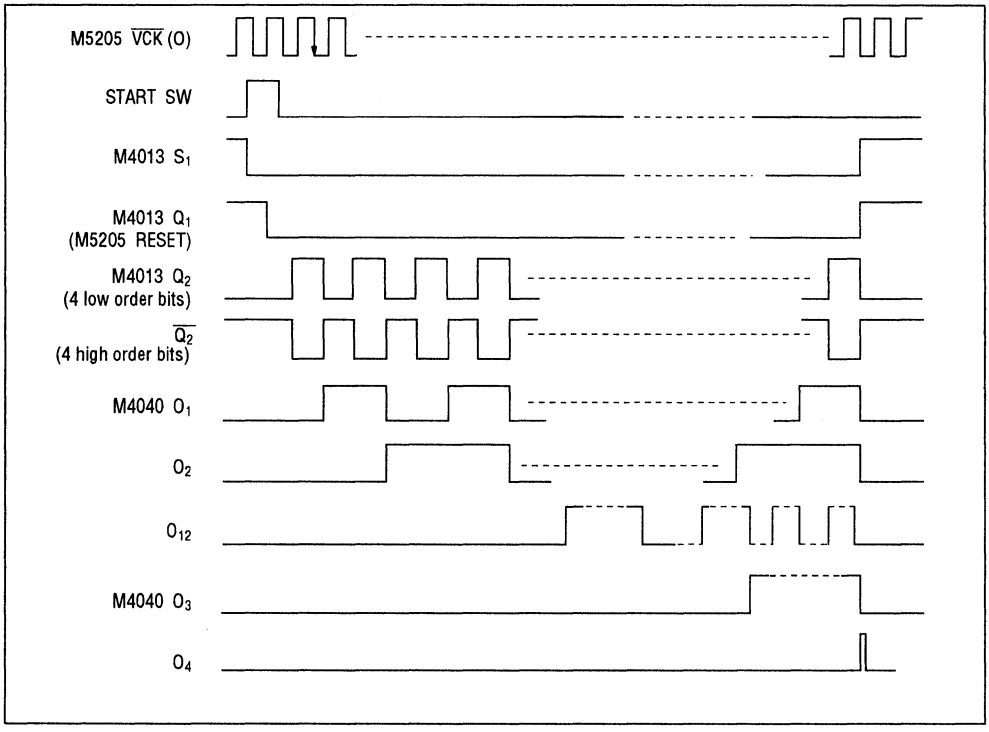

M5205 $\overline{VCK}$ (O)
START SW
M4013 S_1
M4013 Q_1
(M5205 RESET)
M4013 Q_2
(4 low order bits)
$\overline{Q_2}$
(4 high order bits)
M4040 O_1
O_2
O_{12}
M4040 O_3
O_4

Figure 13

OKI Semiconductor

MSM6585

ADPCM SPEECH SYNTHESIS LSI

GENERAL DESCRIPTION

The MSM6585 is an upversion product of the MSM5205 voice synthesis LSI. Mainly improved points are improvement for the precision of an internal DA converter, a built-in low-pass filter, and expansion on the sampling frequency. The MSM6585 does not include a control circuit to drive an external memory similar to the MSM5205. Therefore, the MSM6585 can be connected with not only semiconductor memories, but other memory media (CD-ROM, etc.) by the control of CPU.

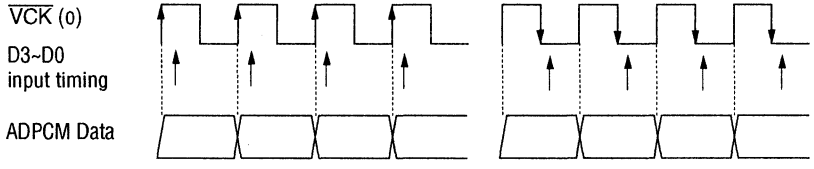
FEATURES

- 4-bit ADPCM system
- Built-in 12-bit DA converter
- Built-in LPF (-40dB/oct)
- Sampling frequencies:
  4k/8k/16k/32kHz
- Original oscillation frequency
  (ceramic oscillator): 640kHz
- Package : 18-pin DIP (DIP 18-P-300)
- Voice data synthesis :
  Support by voice analysis editing tool AR76-202

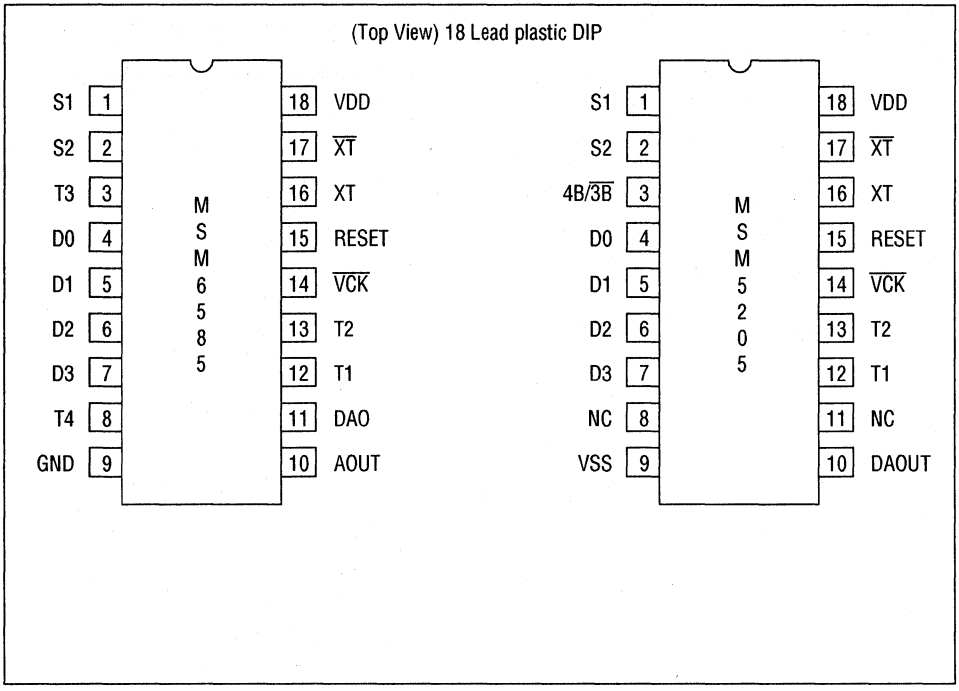
DEFFERENCES BETWEEN MSM6585 AND MSM5205

	MSM6585	MSM5205
• Original oscillation frequency:	640kHz	348kHz
• Sampling frequency:	4k/8k/16k/32kHz	4K/6K/8kHz
• ADPCM bit length:	4-bit	3-bit/4-bit
• DA Converter:	12-bit	10-bit
• Low pass filter:	Included (-40dB/oct)	Not included
• Overflow preventing circuit:	Included	Not included
• Power supply voltage:	4.5 ~ 5.5V	3.0 ~ 6.0V
• Operating current consumption:	10mA	4mA
• Operating temperature:	-40 ~ +85°C	-30 ~+70°C

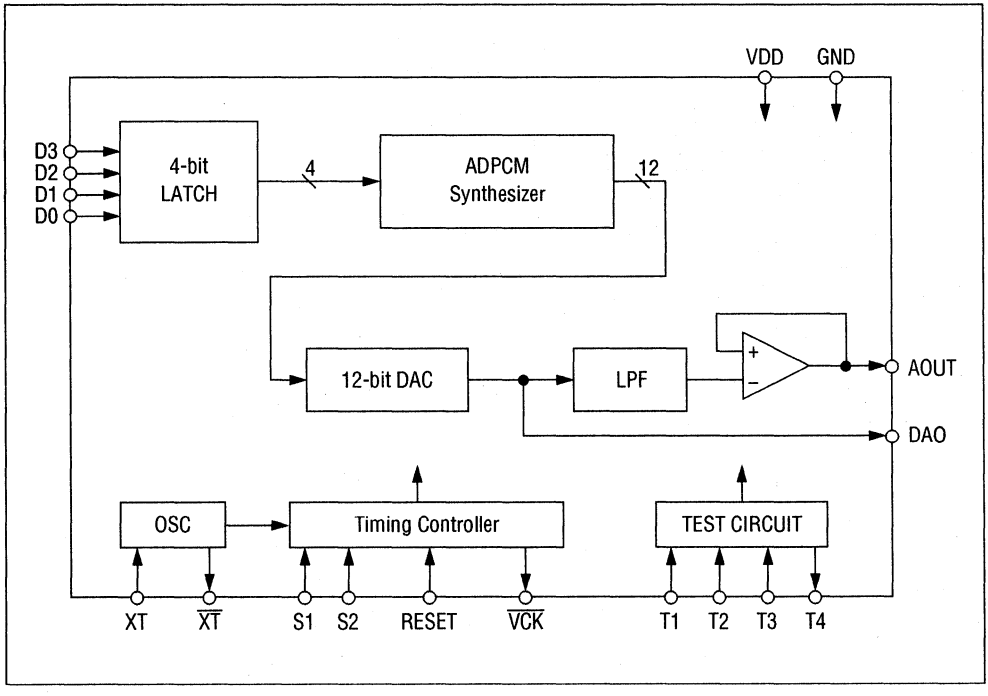
- D3 to D0 input timing



PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Absolute Maximum Ratings

(GND = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	Tstg	—	−55~ +150	°C

Operating Conditions

(GND = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	—	+4.5 ~ +5.5	V
Operating temperture	T_{OP}	—	−40 ~ +85	°C
Original oscillation frequency	f_{OSC}	oscillator connection	640	kHz

DC Chracteristics

(VDD= 4.5 ~ 5.5V, GND = 0V, Ta = −40 ~ +85°C)

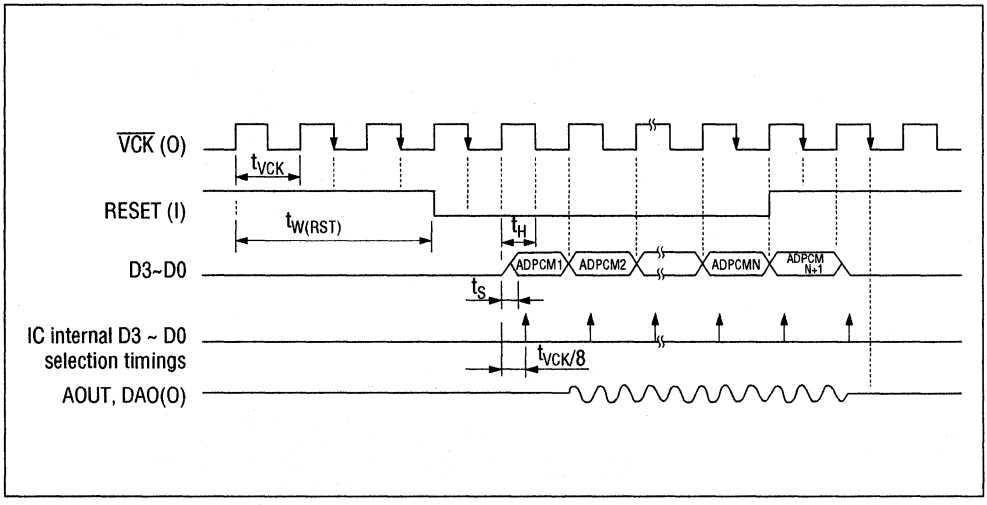
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8×VDD	—	VDD+0.1	V
"L" input voltage	V_{IL}	—	−0.1	—	0.2×VDD	V
"H" output voltage	V_{OH}	VCK: I_{OH} = −40μA	VDD −0.4	—	—	V
"L" output voltage	V_{OL}	VCK: I_{OL} = 40μA	—	—	0.4	V
"H" input current	I_{IH1}	T1, T2, RESET: V_{IH} = VDD	20	150	400	μA
"H" input current	I_{IH2}	S1,S2, D0~D3, T3: V_{IH} = VDD	—	—	10	μA
"H" input current	I_{IH3}	XT: V_{IH} = VDD	—	—	20	μA
"L" input current	I_{IL1}	T3: V_{IL} = 0V	−400	−120	−20	μA
"L" input current	I_{IL2}	S1,S2, D0~D3, T1, T2, RESET: V_{IL} = 0V	−10	—	—	μA
"L" input current	I_{IL3}	XT: V_{IL} = 0V	−20	—	—	μA
Current consumption	I_{DD}	f_{OSC} = 640kHz, No load	—	5	10	mA
DA output relative error	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
DA output impedance	R_{DAO}	—	10	—	40	kΩ
LPF load resistance	R_{AOUT}	—	50	—	—	kΩ

AC Characteristics

Prameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Original oscillation duty cycle	f_{duty}	—	40	50	60	%
RESET input pulse width	$t_{W(RST)}$	f_{SAM} = 4kHz ··· t_{VCK} = 250µs	$2 \times t_{VCK}$	—	—	µs
Data setup time	t_S	= 8kHz ··· = 125µs	—	—	3	µs
Data hold time	t_H	=16kHz··· = 62.5µs =32kHz··· = 31.25µs	$t_{VCK}/2$	—	—	µs

When the MSM5205 and data are commonly used, note that the D3 to D0 selection timings of the MSM6585 and MSM5205 are different. (Refer to DEFFERENCES BETWEEN MSM6585 AND MSM5205.)

TIMING CHART



PIN DESCRIPTION

Pin Name	I/O	Function
S1, S2	I	Pins to determine the sampling frequency. The sampling frequencies of 32k, 16k, 8k, and 4kHz can be selected by combinations. (See the sampling frequencies of the functional description on the selection of combinations.)
T3	I	Pin to test the internal circuit. Set this pin to a high level or make it open because it has a built-in pull-up resistor.
D0~D3	I	Input pin for ADPCM data.
T4	O	Pin to test the internal circuit. Make this pin open.
GND	—	Ground pin
AOUT	O	Pin to output the analog voice from the low-pass filter. Connect a 0.01 µF capacitor to this pin. (See the AOUT connecting circuit of the functional description on the connecting circuit.)
DAO	O	Pin to output the analog voice form the DA converter.
T1, T2	I	Pins to test the internal circuit. Set these pins to a low level or make them open because pull-down resistors are included.
$\overline{VCK}$	O	This pin outputs the sampling frequency selected by the combinations of S1 and S2. The voice synthesis starts or stops by synchronizing with $\overline{VCK}$.
RESET	I	Reset pin. The voice synthesis circuit is initialized by synchronizing with $\overline{VCK}$. If this pin is set to a high level, the D0 to D3 data inputs are disabled by synchronizing with $\overline{VCK}$. The AOUT and DA0 pins output 1/2 VDD and become the state of no voice.
XT	I	Pin to connect an oscillator. When the external clock is used, input it from this pin.
$\overline{XT}$	O	Pin to connect an oscillator. When the external clock is used, make this pin open.
VDD	—	Power supply pin.

FUNCTIONAL DESCRIPTION

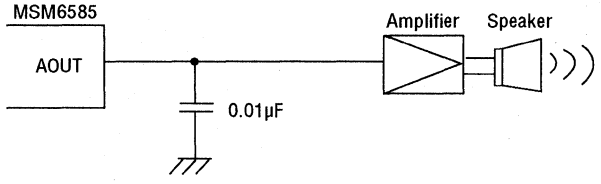
1. Sampling Frequency

The relationship of the sampling frequencies on S1 and S2, and the cutoff frequencies are listed below.

S1	S2	Sampling frequency (f_{SAM})	Cutoff frequency (f_{CUT})
L	L	4 kHz	1.6 kHz
H	L	8 kHz	3.2 kHz
L	H	16 kHz	6.4 kHz
H	H	32 kHz	12.8 kHz

2. AOUT Connecting Circuit

Connect a 0.01uF capacitor to the AOUT pin. The circuit diagram is as shown below.



Even when the DAO pin is used, connect a 0.01μF capacitor to the AOUT pin. This capacitor is used for the improvement of a voice quality.

3. Voice Output

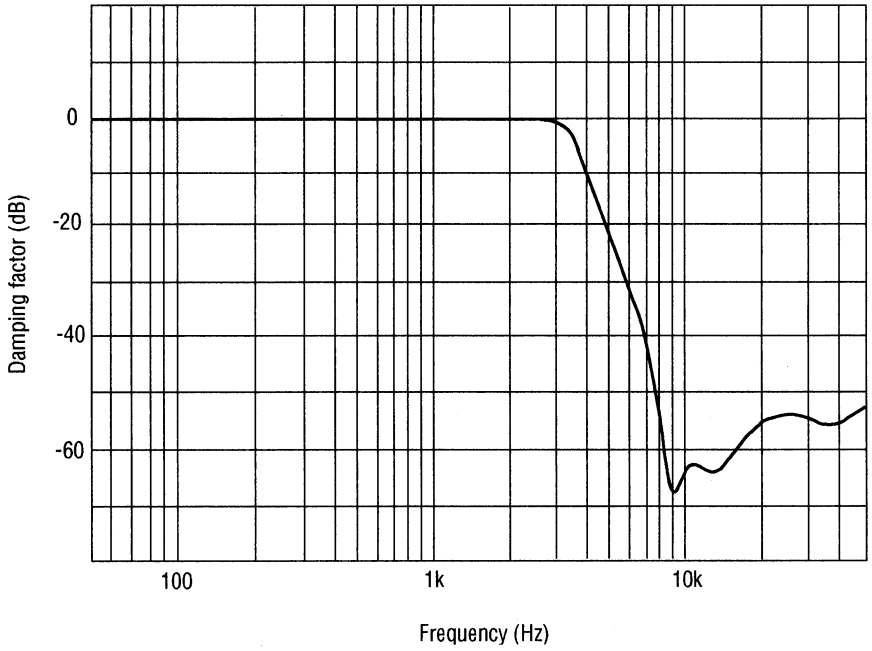
The MSM6585 has two voice output pins. The DAO is direct output pin from the internal DA converter. The AOUT is a pin to output a voice after which the DAO output passed a built-in LPF.

3-1. DA Converter Output Waveform

The output amplitude from the DA converter is max. (4095/4096) ×VDD and becomes a stair step waveform synchronized with the sampling frequency. The DAO output impedance varies in the ranges from 10kΩ to 40kΩ Therefore, determine the filter constant so that the resistor variation does not have influence on the cutoff frequency of the filter.

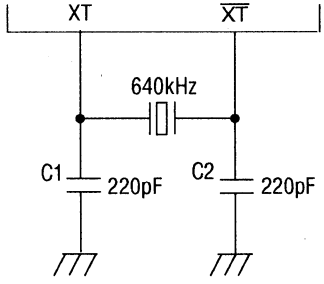
3-2. Low-pass Filter Output

The cutoff frequency of the low-pass filter varies in proportion to the sampling frequency. The following figure shows the low-pass filter characteristics in the sampling frequency 8kHz.



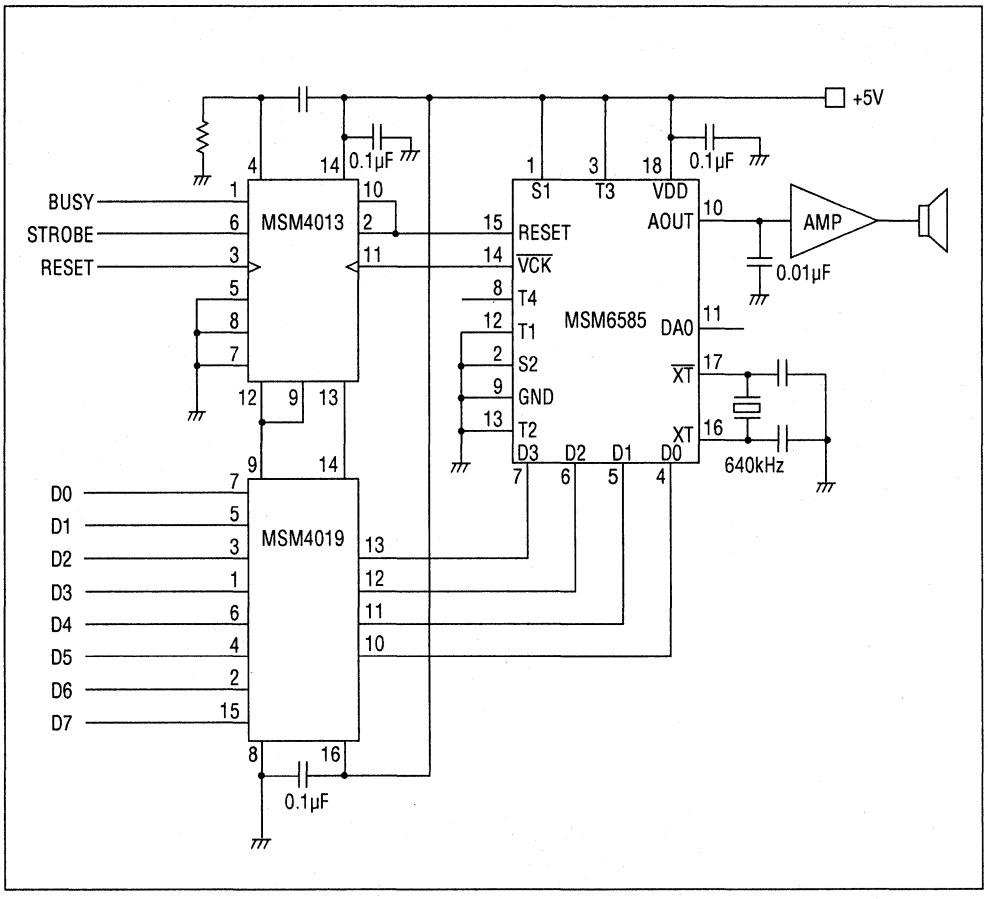
4. Oscillation

The external circuit that used a ceramic oscillator KBR-640B (640kHz) of Kyosera, manufacture is as shown below.

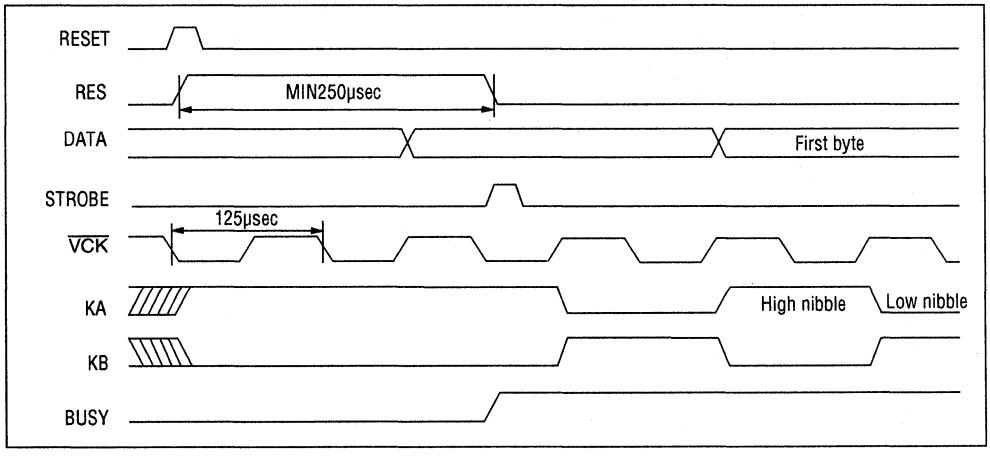


TYPICAL APPLICATION DIAGRAM

Centronics Interface Circuit (sampling frequency 8kHz)

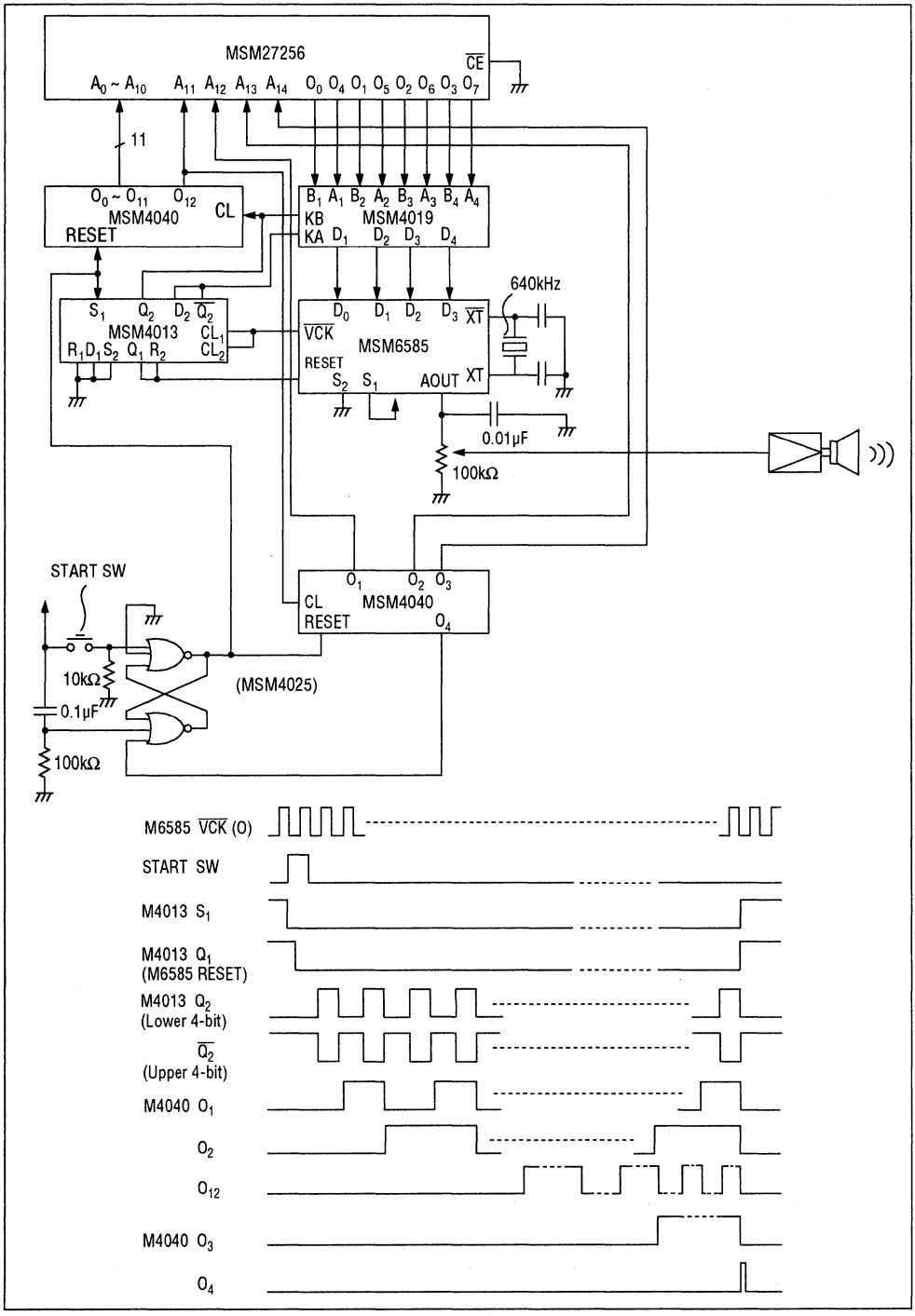


Centronics Timing Chart



Example of Interface Circuit with 256Kbit EPROM

The circuit example and timing chart that used the 256K-bit EPROM are shown below.



OKI Semiconductor

MSM6295

4-CHANNEL MIXING ADPCM VOICE SYNTEHSIS LSI

GENERAL DESCRIPTION

The Oki MSM6295 is a 4-channel mixing ADPCM voice synthesis LSI which is fabricated using Oki's low power CMOS silicon gate technology.

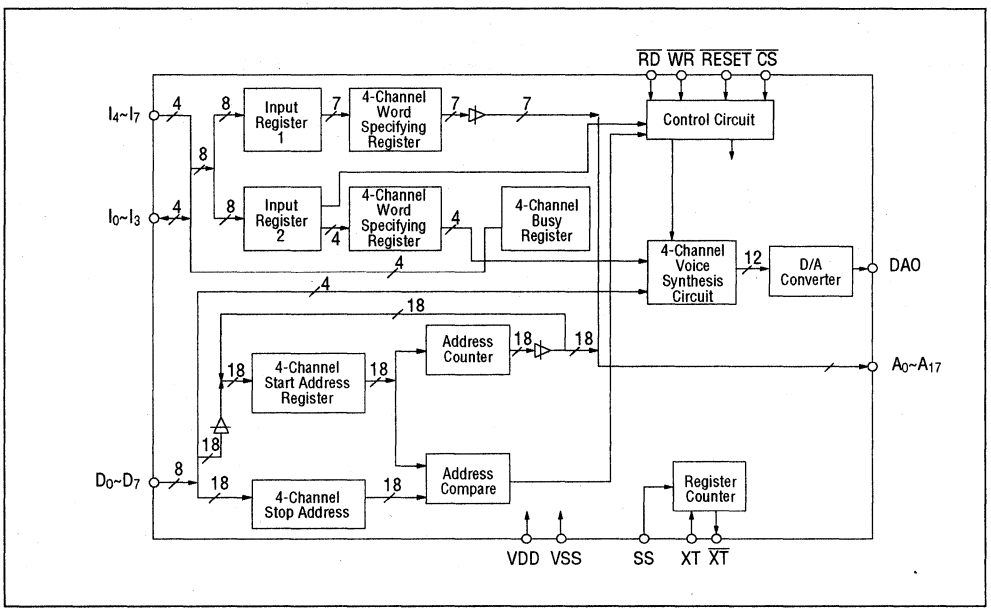
The MSM6295 can access an external ROM, where speech or sound effects data is stored. The maximum external ROM size is 256K bytes.

The MSM6295 has a 4-channel synthesis stage which allows the simultaneous playback of four different channels. It is used to have a voice with BGM (Back Ground Music) effect, instrumental sound, echo etc.

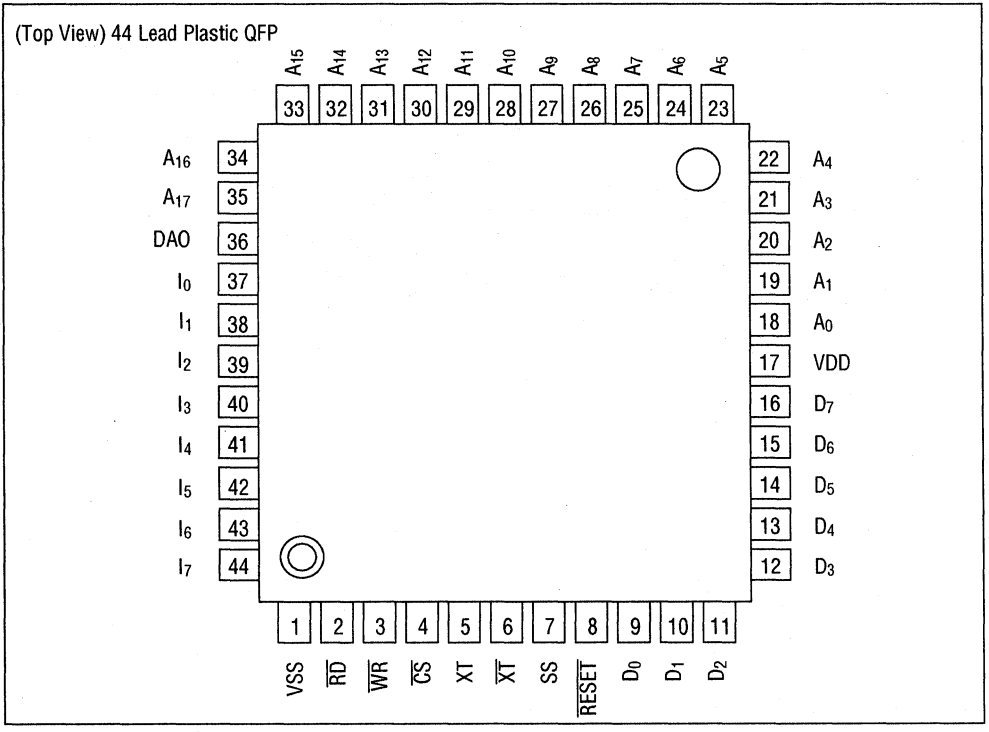
FEATURES

- Oki straight ADPCM algorithm
- Number of bits/sample: 4
- 18 address lines for external ROM
- 8-bit control bus for mode setting
- External memory capacity 2Mbit
- Interface with common CPU and MPU
- Clock frequency: 1 MHz to 5 MHz
- Sampling frequency:
  6.5 kHz and 8 kHz
  (@1.056 MHz clock)
  25.6 kHz and 32 kHz
  (@4.224 MHz clock)
- Number of words: 127 maximum
- Vocalization time: 60 sec maximum
  (@8 kHz, straight)
- Built-in DA converter: 12-bit
- DA output format: A-class
- Voice level attenuation: 0dB ~ –24dB
  on each channel (9 steps)
  –3dB/step
- Low power CMOS process
- 5 V single power supply
- 44-pin plastic QFP (QFP44-P-910-V1K)
  (QFP44-P-910-K)
- 42-pin plastic DIP (DIP42-P-600)

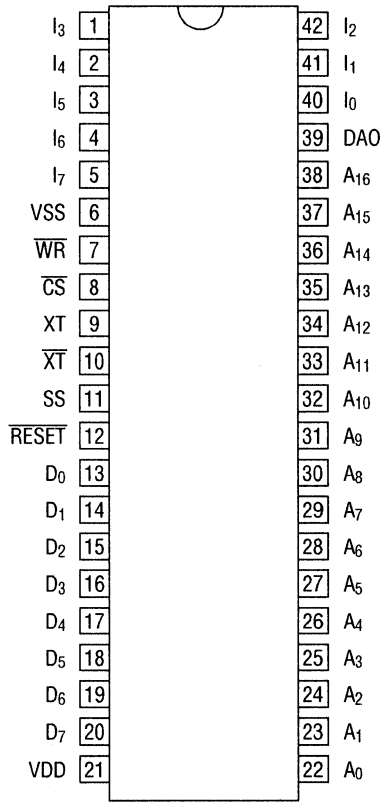
BLOCK DIAGRAM



PIN CONFIGURATION



(Top View) 42 Lead Plastic DIP



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Recommended Operating Conditions

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	VSS = 0V	4.5 ~ +5.5	V
Operating temperature	T_{op}	VSS = 0V	−40 ~ +85	°C
Oscillation frequency	f_{OSC}	VSS = 0V	1 ~ 5	MHz

• DC Characteristics

(VDD = 4.5~5.5V, VSS = 0V, Ta = −40 ~ +85°C)

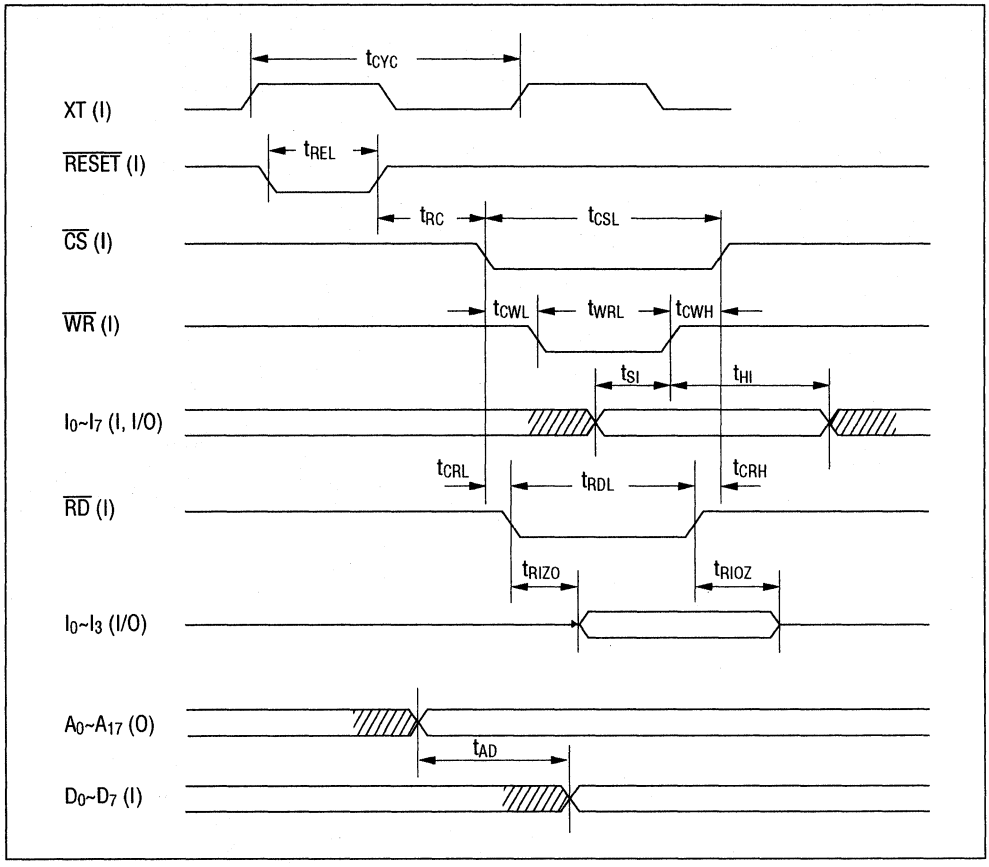
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
"L" input current	I_{IL}	V_{IL} = VSS	−10	—	—	µA
"H" input current	I_{IH}	V_{IH} = VDD	—	—	10	
"L" input voltage	V_{IL}	—	—	—	0.8	V
"H" input voltage	V_{IH}	—	2.4	—	—	
"L" output voltage	V_{OL}	I_{OL} = 0.8 mA	—	—	0.45	V
"H" output voltage	V_{OH}	I_{OH} = −40 µA	3.7	—	—	
Output leakage current	I_{LO}	VSS ≦ V_{OUT} ≦ VDD	−10	—	10	µA
Operating current	I_{DD}	f_{OSC} = 5.0MHz	—	5	10	mA
DA output relative error	$\|V_{DAE}\|$	No load	—	—	20	mV
DA output impedance	R_{DAOUT}	—	—	15	—	kΩ

• AC Characteristics

(VDD = 4.5~5.5V, VSS = 0V, Ta = −40 ~ +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock cycle	t_{CYC}	200	–	–	ns
Clock duty cycle	f_{DUTY}	40	50	60	%
$\overline{RESET}$ pulse width	t_{REL}	100	–	–	ns
$\overline{CS}$ pulse width	t_{CSL}	250	–	–	ns
$\overline{WR}$ pulse width	t_{WRL}	200	–	–	ns
$\overline{RD}$ pulse width	t_{RDL}	300	–	–	ns
$\overline{RESET}$ fall to $\overline{CS}$ fall	t_{RC}	250	–	–	ns
$\overline{CS}$ fall to $\overline{WR}$ fall	t_{CWL}	50	–	–	ns
$\overline{WR}$ raise to $\overline{CS}$ raise	t_{CWH}	0	–	–	ns
Data set up time of I_0-I_7 in respect to $\overline{WR}$ raise	t_{SI}	80	–	–	ns
Data hold time of I_0-I_7 in respect to $\overline{WR}$ raise	t_{HI}	80	–	–	ns
$\overline{RD}$ fall to stable output of I_0-I_3	t_{RIZO}	–	–	120	ns
$\overline{RD}$ raise to flow status output of I_0-I_3	t_{RIOZ}	0	–	120	ns
$\overline{CS}$ fall to $\overline{RD}$ fall	t_{CRL}	20	–	–	ns
$\overline{RD}$ raise to $\overline{CS}$ raise	t_{CRH}	0	–	–	ns
Address stable (A_0-A_{17}) to data input of D_0-D_7	t_{AD}	–	–	$5 \cdot t_{CYC}+90$	ns

• Timing Chart



PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
I_0	37	I/O	Instruction bus and condition outputs
I_1	38	I/O	These pins are inputs for phrase specification. Maximum number
I_2	39	I/O	of phrases is 127. I_0~I_3 pins are also outputs of the operating
I_3	40	I/O	state, busy state, for channels 1~4 and are further used to select the
I_4	41	I	channel attenuation rate.
I_5	42	I	
I_6	43	I	
I_7	44	I	
$\overline{WR}$	3	I	Write enable input Data is written on the data bus of I_0~I_7. The data is written when $\overline{WR}$ goes low.
$\overline{RD}$	2	I	Read enable input The output busy state of channels 1~4 on the data bus of I_0~I_3. Can be read using this input. A high level indicates busy.
$\overline{CS}$	4	I	Chip select input Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input.
$\overline{RESET}$	8	I	Reset input Reset condition is available by inputting "L" level. All functions are suspended during reset.
A_0	18	I	Address outputs
〃	〃	〃	These pins are to address the external ROM in which voice data
A_{17}	35	I	is stored.
D_0	9	I	Voice data inputs
〃	〃	〃	
D_7	16	I	
SS	7	I	Sampling frequency select input When oscillation frequency is 1.056 MHz or 4.224 MHz, the following choices are available by inputting "H" level or "L" level to SS.

	SS = "H"	SS = "L"
Oscillation frequency 1.056 MHz	8 kHz	6.5 kHz
Oscillation frequency 4.224 MHz	32 kHz	25.6 kHz

DAO	36	O	Voice synthesis output Voice synthesized analog signal is output from this pin.
XT	5	I	Crystal oscillator pin
$\overline{XT}$	6	O	Crystal oscillator pin
VDD	17	–	Power supply pin
VSS	1	–	Ground

FUNCTION EXPLANATION

1. Phrase Selection

Phrases are specified and read into the 2 byte data which consists of I_0~I_7 data bus.

The phrase selection data is latched when $\overline{WR}$ goes high while $\overline{CS}$ is low (L).

The format of the phrase specification input is as follows.

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1st Byte	1	Phrase selection data						
2nd Byte	Channel specification				Reduction specification			

As shown in the above chart, I_7 of the first 1 data byte is always 1. I_0 ~I_6 of the first 1 data byte specifies the phrase. Phrase selection data has a selection of 127 phrases which corresponds to 0000001~1111111. The phrase selection data is used for to A_3~A_9 address outputs, and they specify both start and stop address which are stored in the external ROM.

Relation between Phrase Selection Data and ROM Address

Phrase selection data	–	I_6	I_5	I_4	I_3	I_2	I_1	I_0	–	–	–
External ROM address	A_{17}~A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Selection											
Not valid	0~0	0	0	0	0	0	0	0	0	0	0
Phrase 1	0~0	0	0	0	0	0	0	1	0	0	0
Phrase 2	0~0	0	0	0	0	0	1	0	0	0	0
Phrase 3	0~0	0	0	0	0	0	1	1	0	0	0
Phrase 127	0~	1	1	1	1	1	1	1	0	0	0

* Phrases cannot be specified with all inputs = "0"

The second byte of data specifies the synthesis operation channel as well as specific channel reduction of the synthesized playback. The channel selection format is shown below.

It is not possible to specify multiple channels at the same time. For example, it is not possible to specify channel 1 and channel 3 simultaneously.

Channel Specification

Channel	I_7	I_6	I_5	I_4
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

REDUCTION SELECTION

All 0's is considered as 0 dB of the analyzed sound itself. The reduction is made through 9 levels from about 0 dB to - 24 dB with the steps of about - 3 dB. Reduction format is shown below.

Reduction Specification

Attenuation level	I_3	I_2	I_1	I_0
0 dB	0	0	0	0
–3.2 dB	0	0	0	1
–6.0 dB	0	0	1	0
–9.2 dB	0	0	1	1
–12.0 dB	0	1	0	0
–14.5 dB	0	1	0	1
–18.0 dB	0	1	1	0
–20.5 dB	0	1	1	1
–24.0 dB	1	0	0	0

2. Voice Synthesis Channel Suspension

Voice synthesis operation of any channel can be suspended. Channel suspension is controlled by bits I_3~I_6 of data bytes I_0~I_7. To suspend a channel, make I_7=0, while I_3~I_6 represent the channels which should be suspended.

Channel suspension occurs even if multiple channels are selected. For example, if I_3~I_6 are all 1 and I_7=0, then channels 1~4 are suspended simultaneously.

Suspended channel	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1	0	0	0	0	1	X	X	X
2	0	0	0	1	0	X	X	X
3	0	0	1	0	0	X	X	X
4	0	1	0	0	0	X	X	X

3. Data ROM

1) ADDRESS DATA

This specifies start and stop address of ADPCM speech data. One phrase start and end address consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty.

By selecting the first address in which the start address is stored, the selected speech data is played back.

Address	
0	SA_1
1	SA_2
2	SA_3
3	EA_1
4	EA_2
5	EA_3
6	EMPTY
7	EMPTY

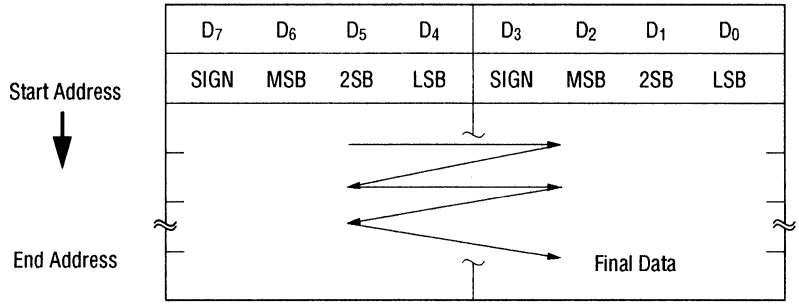
Start addresses (SA_1~SA_3) and stop addresses (EA_1~EA_3) are stored according to the chart shown below.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_1/EA_1	0	0	0	0	0	0	A_{17}	A_{16}
SA_2/EA_2	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
SA_3/EA_3	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

2) ADPCM SPEECH DATA

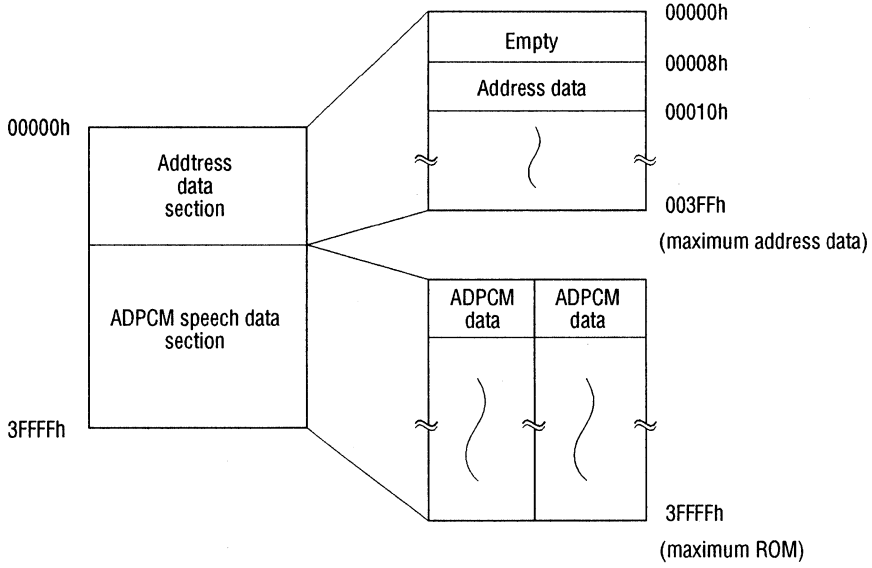
ADPCM speech data consists of (2) 4-bit samples. So, 1 byte stores 2 samples. Data arrangement proceeds from higher rank bits (D_4~D_7) to lower rank bits (D_0~D_3). The storage of speech data should always be ended with the lower rank bit. So, always store an even number of samples.

Speech data is produced by Speech Development Tool AR76-202.



3) DATA ROM STRUCTURE

The following chart shows the memory map of the source data ROM.



When the maximum 127 phrases are selected in address data section, the data is written up to ROM address 003FFh.

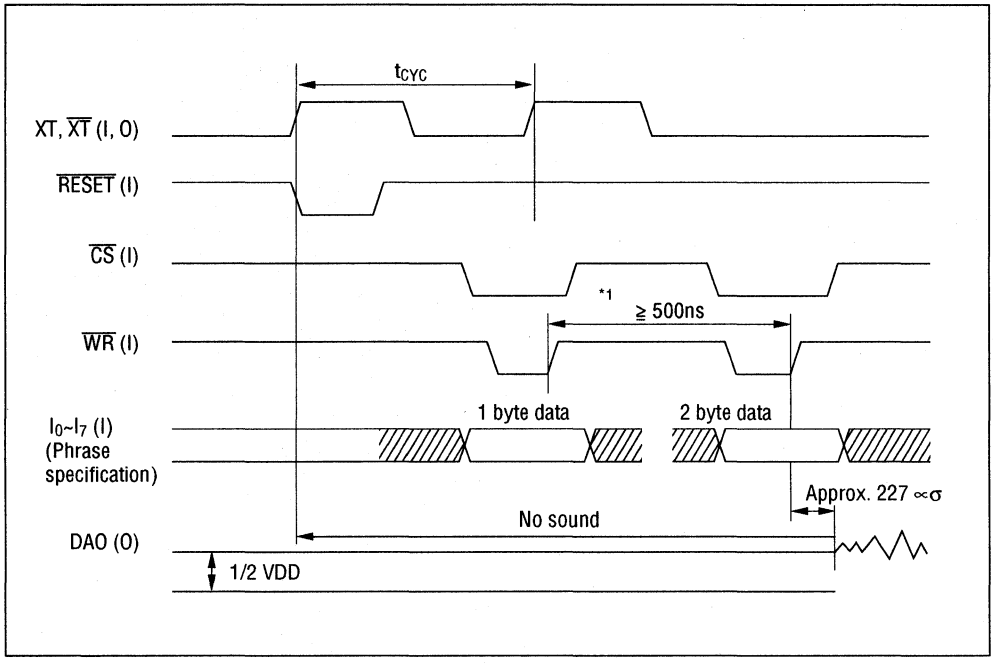
When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, and the rest is used as the ADPCM data section.

FUNCTIONAL DESCRIPTION

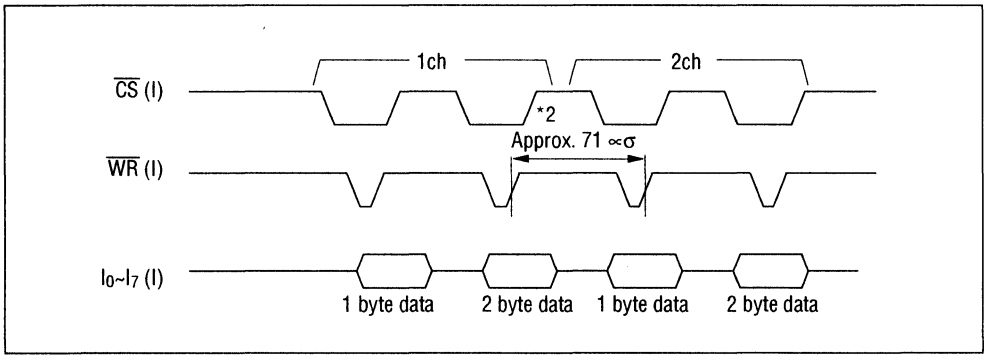
1. Phrase Selection Input

This procedure is to input phrase selection data onto the data bus inputs I_0~I_7. The data is latched internally when $\overline{WR}$ rises from "L" to "H", while $\overline{CS}$ remains "L".

Voice synthesis operation does not start till the second byte is fully latched.



Note: Phrase selection is from channel 1 to channel 4 continuously.
*1 An interval of 75 T_{CYC} (max.) is needed between phrases.

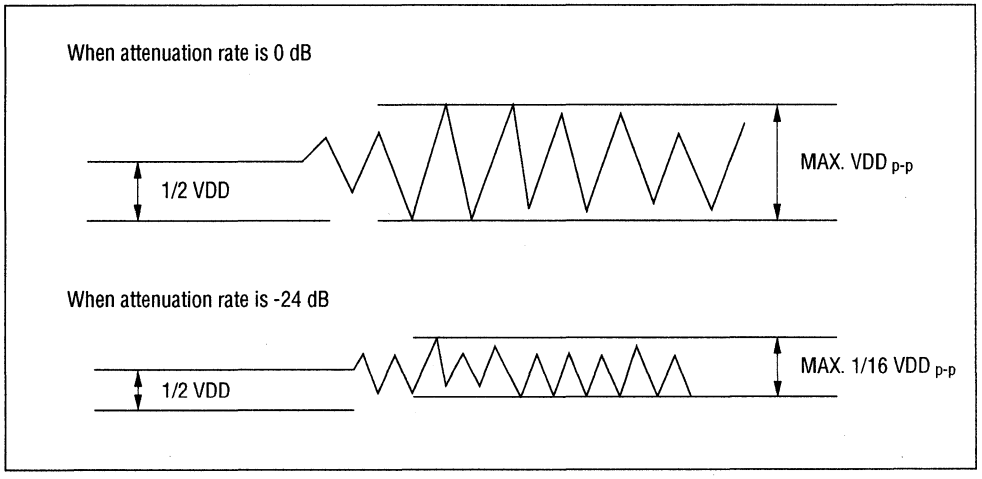


Note: *2 Oscillation frequency = 1.056 MHz SS = "L"

Voice synthesis playback can be started from any channel, 1 to 4. The arrangement of each channel can be in any order.

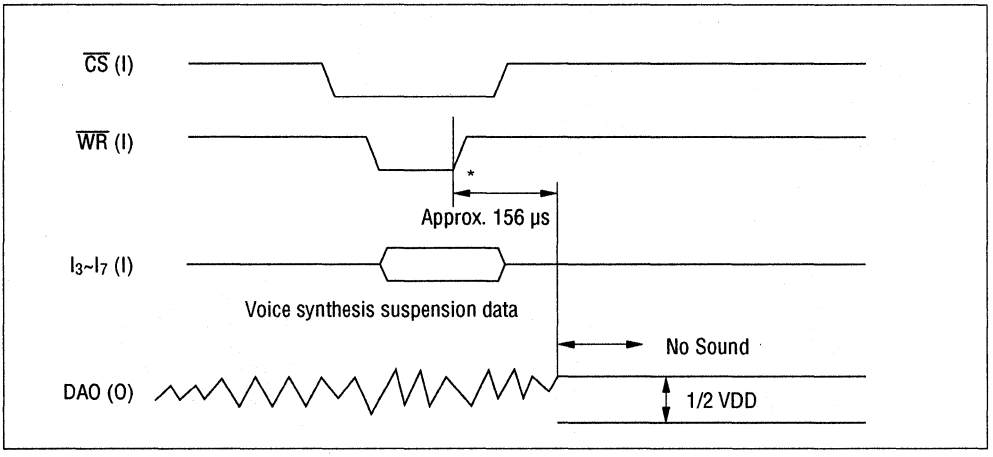
The second byte of the phrase selection data contains the phrase attenuation data in bits D0 - D3. Synthesized data is attenuated in –3 dB steps from 0 dB to –24 dB.

2. Attenuation of Synthesized Speech



3. Speech Synthesis Channel Suspension

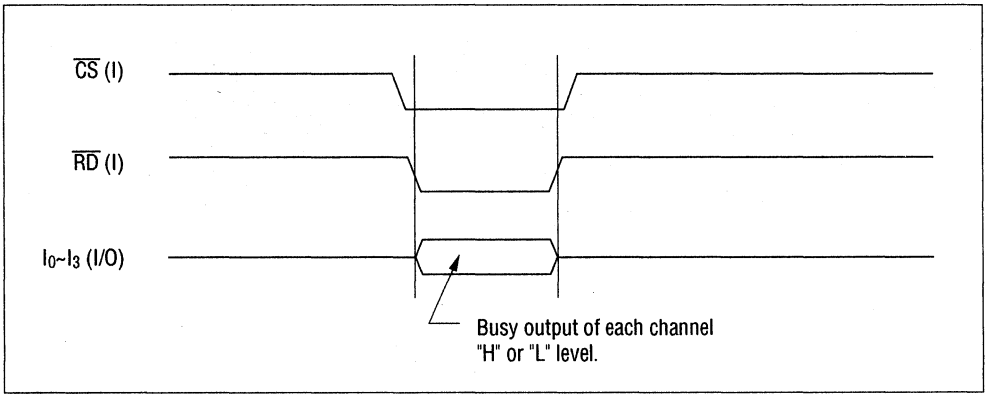
This is accomplished by writting synthesis channel suspension data onto data bus inputs I_3~I_7. The data is latched internally when $\overline{WR}$ goes from "L" to "H" while $\overline{CS}$ remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after the rising edge of $\overline{WR}$. Multiple channels can be specified, making it possible to suspend channels 1~4 simultaneously.



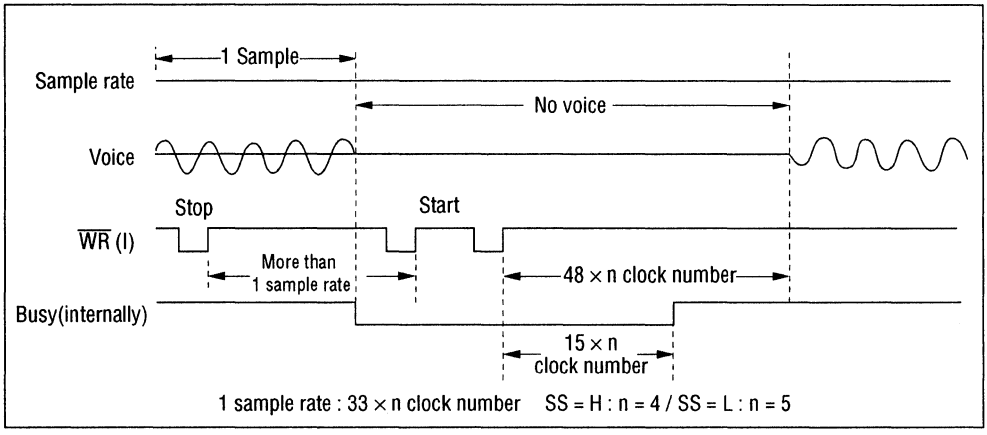
Note: * Oscillation frequency = 1.056 MHz SS = "L"

4. Reading the Busy Status

While $\overline{CS}$ is "L" and $\overline{RD}$ is "L", each operation state, the busy state of channels 1~4 is output on I_0~I_3. "H" is output during synthesized playback.



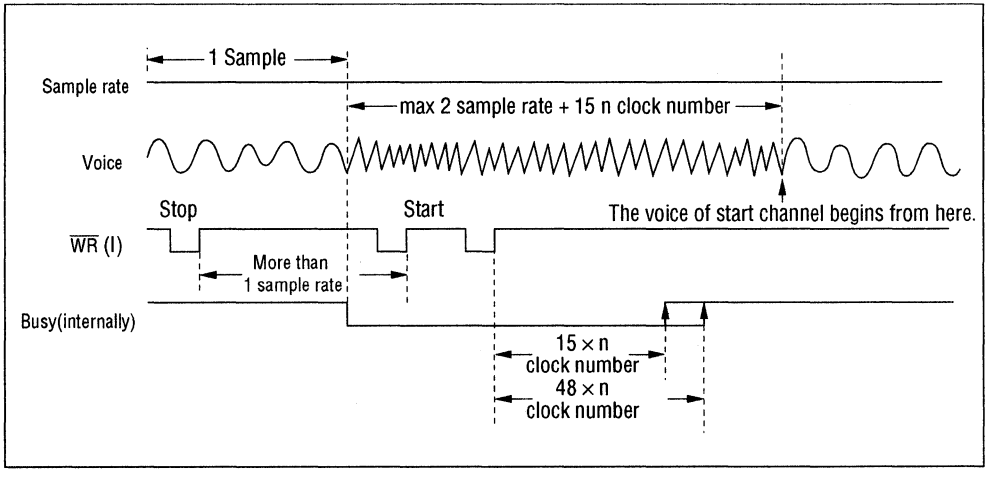
5. Start and Stop of 1 Channel



Start and Stop of Signal Channel

When a single channel (either of channels 1-4) starts again after it has stopped, the first write for start must be input with a delay of more than one sample rate from the stop write as shown in the figure above. When stop is entered, voice playback stops all the next sample and BUSY becomes "L".

When start is entered again, voice is output after 48 x n clock from the second byte write. BUSY becomes "H" after 15 x n clock internally.



Start and Stop in Plural Channels

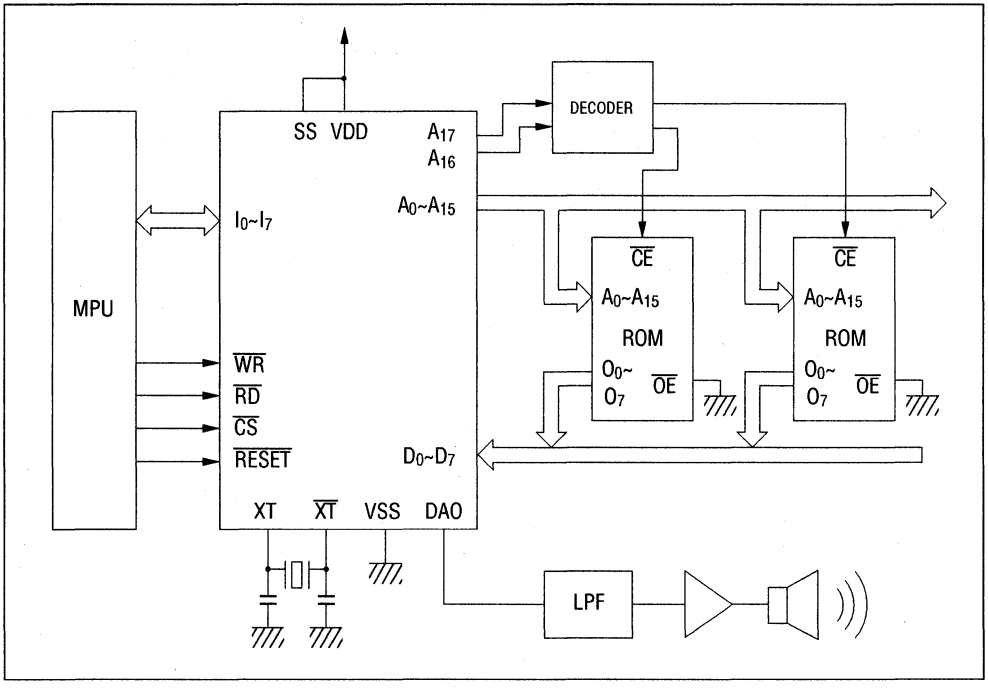
When channels are operating, the first byte write for start must be input with a delay of more than one sample rate from stop write.

The channel where stop was input, stops at every sample.

Voice off the channel where stop was again input is output after a maximum 2 samples = 15 x n clocks from the preceding sample point.

BUSY becomes "H" during the 48 x n clock time.

6. Application Circuit



OKI Semiconductor

MSM6375/4/3/2-XXX

1M-bit/512K-bit/256K-bit/128K-bit MASK ROM SPEECH SYNTHESIZER

GENERAL DESCRIPTION

The MSM6375 series is an ADPCM speech synthesis LSI utilizing a CMOS speech processor circuit in conjunction with a built-in MASK ROM for speech data storage. Since it has a built-in 12-bit DA converter and low pass filter, speech output can easily be accomplished by connecting an external power amplifier and speaker. Two sounds can be synthesized and reproduced simultaneously making applications with BGM (Background Music) and voice with echo possible. Additionally 8 beep tones are available at four selectable durations for use as prompts into a message.

The MSM6376 is an evaluation LSI for the MSM637X series.

FEATURES

Device	ROM size	Speech period		
		fs=4.0kHz	fs=6.4kHz	fs=8.0kHz
MSM6375-XXX	1M-bit	64 sec	40 sec	32 sec
MSM6374-XXX	512K-bit	32 sec	20 sec	16 sec
MSM6373-XXX	256K-bit	16 sec	10 sec	8 sec
MSM6372-XXX	128K-bit	8 sec	5 sec	4 sec

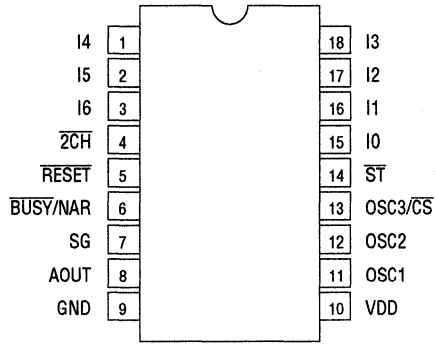
(Note) fs=Sampling frequency

- Single-chip CMOS
- ROM Custom
- 4-bit ADPCM system
- Echo or 2-channel mixing functions
- Maximum number of words: 111-word
- Built-in 12-bit DA converter
- Built-in LPF
- Standby function
- Oscillation: RC or crystal
- Packages: 18-pin DIP (DIP 18-P-300)
  24-pin SOP
  (SOP 24-P-430-VK)Chip

fosc [kHz]	fs [kHz]	fCUT [kHz]	Beep Tone	LPF Voltage	DAC Voltage
64	4.0	1.5	1kHz & 2kHz	2.7V ~ 5.5V	2.4V ~ 5.5V
	6.4	3.0			
	8.0	3.0			
128	8.0	3.0	2kHz & 4kHz	4.5V ~ 5.5V	
	12.8	6.0			
	16.0	6.0			
256	16.0	–	4kHz & 8kHz	–	
	25.6	–			
	32.0	–			

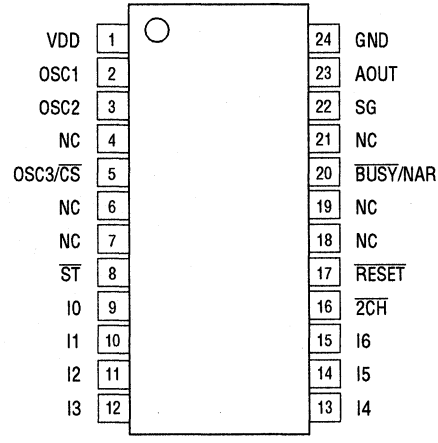
PIN CONFIGURATION (Top View)

18 Lead Plastic DIP



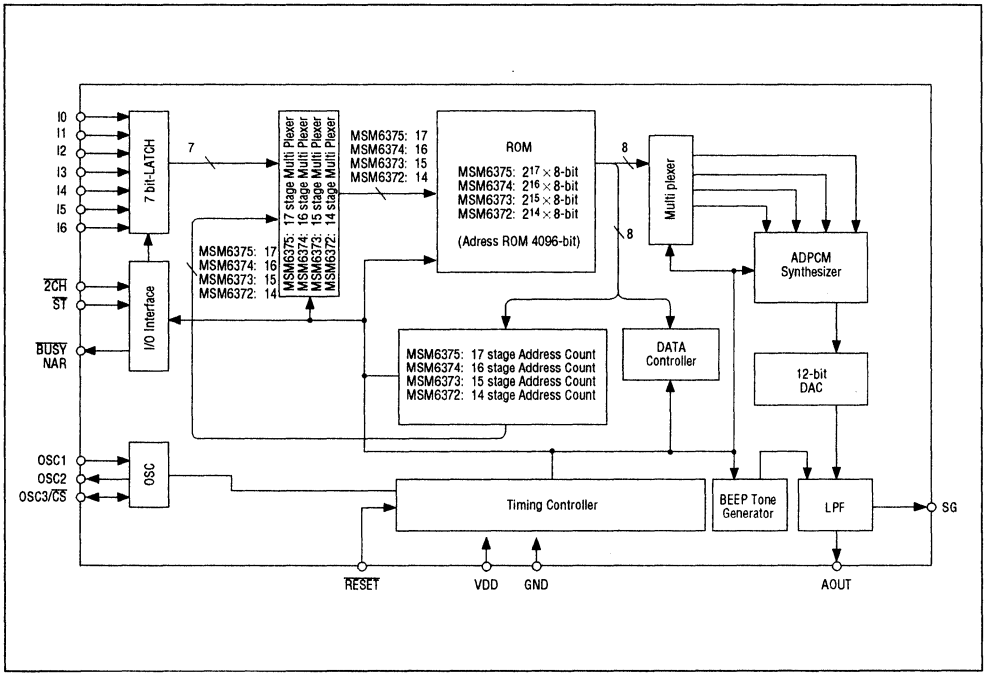
Note: Applicable to the MSM6375-XXX-RS, MSM6374-XXX-RS, MSM6373-XXX-RS, MSM6372-XXX-RS

24 Lead Plastic SOP



Note: Applicable to the MSM6375XXXGS-VK, MSM6374XXXGS-VK, MSM6373XXXGS-VK, MSM6372XXXGS-VK.

MSM6375/MSM6374/MSM6373/MSM6372 BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

(GND=0V)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}		−0.3 ~ VDD + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Ranges

(GND=0V)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	VDD	DAC output		+2.4~ +5.5	V
		LPF output	40kHz ≦ f_{osc} ≦ 140kHz	+4.5 ~ +5.5	
			f_{osc} ≦ 80kHz	+2.7 ~ +5.5	
Operating temperature	T_{op}	—		−40 ~ +85	°C
Master oscillation frequency (Note 1)	f_{osc1}	LPF output		40 ~ 140	kHz
Master oscillation frequency (Note 1)	f_{osc2}	DAC output		40 ~ 256	kHz

Note 1: The precision of the osclation frequency with the optional RC oscillator depends heavily on the precision of external C and R.

• DC Characteristics

(VDD=5.0V, GND=0V, Ta=−40~+85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	4.2	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.8	V
"H" output voltage	V_{OH}	I_{OH} = −40 µA	4.6	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" input current	I_{IH}	V_{IH} = VDD	—	—	10	µA
"L" input current	I_{IL}	V_{IH} = OV	−10	—	—	µA
Operating current consumption	I_{DD}	—	—	4	10	mA
Standby current consumption	I_{DS}	—	—	—	10	µA
Relative precision of DA	$\|V_{DAE}\|$	No load	—	—	40	mV
DA output impedance	R_{DAO}	—	15	25	35	kΩ
LPF load impedance	R_{AOUT}	—	50	—	—	kΩ

• DC Characteristics

(VDD = 3.1V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	2.6	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.5	V
"H" output voltage	V_{OH}	I_{OH} = −10 µA	2.7	—	—	V
"L" output voltage	V_{OL}	I_{OL} = −10 µA	—	—	0.4	V
"H" input current	I_{IH}	V_{IH} = VDD	—	—	1	µA
"L" input current	I_{IL}	V_{IL} = 0V	−1	—	—	µA
Operating current consumption	I_{DD}	—	—	1.5	4	mA
Standby current consumption	I_{DS}	—	—	—	1	µA
Relative precision of DA output	$\|V_{DAE}\|$	No load	—	—	20	mV
DA output impedance	R_{DAO}	—	15	25	35	kΩ
LPF load impedance	R_{AOUT}	—	50	—	—	kΩ

• AC Characteristics (VDD = 5V, Ta = –40 ~ 85°C, f_{OSC} = 64 kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µs
$\overline{ST}$ input pulse width (Note 3)	$t_{W(\overline{ST})}$	—	0.35	–	350	µs
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µs
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µs
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µs
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µs
Data set time	t_{DW}	—	10	–	–	µs
Data hold time	t_{WD}	—	10	–	–	µs
$\overline{CS}$ setup time (Note 1)	t_{CS}	—	10	–	–	µs
$\overline{CS}$ hold time (Note 1)	t_{SC}	—	10	–	–	µs
Selectable sampling frequency	f_{S1}	$f_{osc}/8$	–	8.0	–	kHz
	f_{S2}	$f_{osc}/10$	–	6.4	–	kHz
	f_{S3}	$f_{osc}/16$	–	4.0	–	kHz
$\overline{BUSY}$ output time (1) (Note 5)	t_{SBS}	—	–	–	10	µs
$\overline{BUSY}$ output time (2) (Note 2)	t_{BN}	At f_s = 8 kHz	350	375	400	µs
$\overline{BUSY}$ output time (3) (Notes 2 and 6)	t_{BF}	At master frequency=64 kHz	–	–	64	ms
$\overline{BUSY}$ output time (4) (Note 3)	t_{BA}	At f_s=8 kHz	350	375	400	µs
NAR output time (1) (Note 5)	t_{SNS}		–	–	10	µs
NAR output time (2)	t_{NN}	—	–	–	500	ns
NAR output time (3) (Note 4)	t_{NAA}	At f_s=8 kHz	350	375	400	µs
NAR output time (4) (Note 4)	t_{NAB}	At f_s=8 kHz	350	375	400	µs
NAR output time (5) (Note 4)	t_{NAC}	At f_s=8 kHz	350	–	550	µs
D/A converter transition time	t_{DAR}, t_{DAF}	At master frequency=64 kHz	60	64	68	ms
LPF stabilizing time (Note 5)	t_L	At master frequency=64 kHz	12	16	20	ms
Standby transition time (at end of speech output)	t_{STB}	At master frequency=64 kHz	2.9	3.0	3.1	sec
$\overline{ST}$– $\overline{2CH}$ pulse interval	t_{S2CH}	At master frequency=64 kHz	1.0	–	–	ms
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µs

Note 1: When crystal oscillation is selected as an option.
Note 2: When $\overline{BUSY}$ is selected as an option. The duration is proportional to f_s.
Note 3: When the CPU interface is selected as an option, the MAX value is proportional to f_s. The MAX value when playing one word (using the SW interface) is equal to the speech cycle time.
Note 4: When NAR is selected as an option. The duration is proportional to f_s. (When f_s is high, the cycle is shortened.)
Note 5: Applicable at the start of oscillation.
Note 6: When playback occurs during the standby transition period (t_{DAF}).

• AC Characteristics (VDD = 5V, Ta = –40 ~ 85°C, f_{OSC1} = 40 ~ 140 kHz, f_{OSC2} = 40 ~ 256 kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µs
$\overline{ST}$ input pulse width (Note 2)	$t_{W(\overline{ST})}$	—	0.35	–	a	µs
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µs
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µs
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µs
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µs
Data set time	t_{DW}	—	10	–	–	µs
Data hold time	t_{WD}	—	10	–	–	µs
$\overline{CS}$ setup time (Note 1)	t_{CS}	—	10	–	–	µs
$\overline{CS}$ hold time (Note 1)	t_{SC}	—	10	–	–	µs
Selectable sampling frequency	f_{S1}	—	–	f_{osc}/8	–	kHz
	f_{S2}	—	–	f_{osc}/10	–	kHz
	f_{S2}	—	–	f_{osc}/16	–	kHz
$\overline{BUSY}$ output time (1) (Note 3)	t_{SBS}	—	–	–	10	µs
$\overline{BUSY}$ output time (2)	t_{BN}	—	a	b	c	µs
$\overline{BUSY}$ output time (3) (Notes 4)	t_{BF}	—	–	–	e	ms
$\overline{BUSY}$ output time (4)	t_{BA}	—	a	b	c	µs
NAR output time (1) (Note 3)	t_{SNS}	—	–	–	10	µs
NAR output time (2)	t_{NN}	—	–	–	500	ns
NAR output time (3)	t_{NAA}	—	a	b	c	µs
NAR output time (4)	t_{NAB}	—	a	b	c	µs
NAR output time (5)	t_{NAC}	—	a	–	d	µs
D/A converter transition time (Note 3)	t_{DAR}, t_{DAF}	—	e-4	e	e+4	ms
LPF stabilizing time	t_L	—	f-4	f	f+4	ms
Standby transition time (at end of speech output)	t_{STB}	—	g-0.1	g	g+0.1	sec
$\overline{ST}$–$\overline{2CH}$ pulse interval	t_{S2CH}	—	h	–	–	ms
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µs

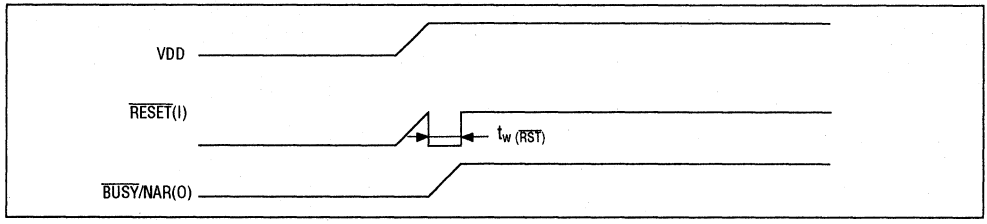
$$a = 350 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad b = 375 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad c = 400 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad d = 550 \times \frac{8\ (kHz)}{f_S\ (kHz)}$$

$$e = 64 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad f = 16 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad g = 3.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad h = 1.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)}$$

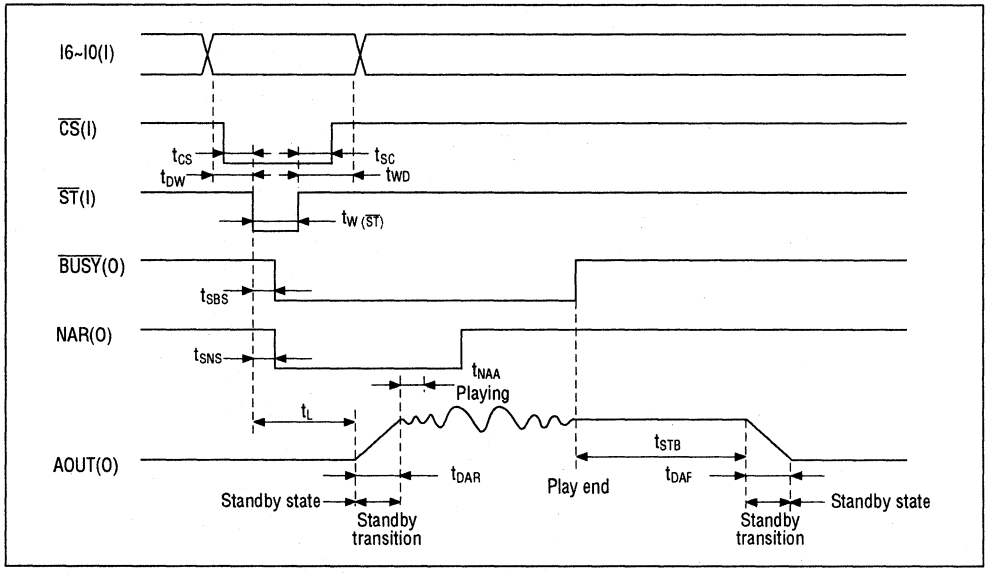
Note 1: When crystal oscillation is selected as an option.
Note 2: When the CPU interface is selected as an option, the MIN value when playing one word (using the SW interface) is 0.35µS and the MAX value is equal to the speech cycle time.
Note 3: Applicable at the start of oscillation.
Note 4: When playback occurs during the standby transition period (t_{DAF}).

TIMING DIAGRAMS

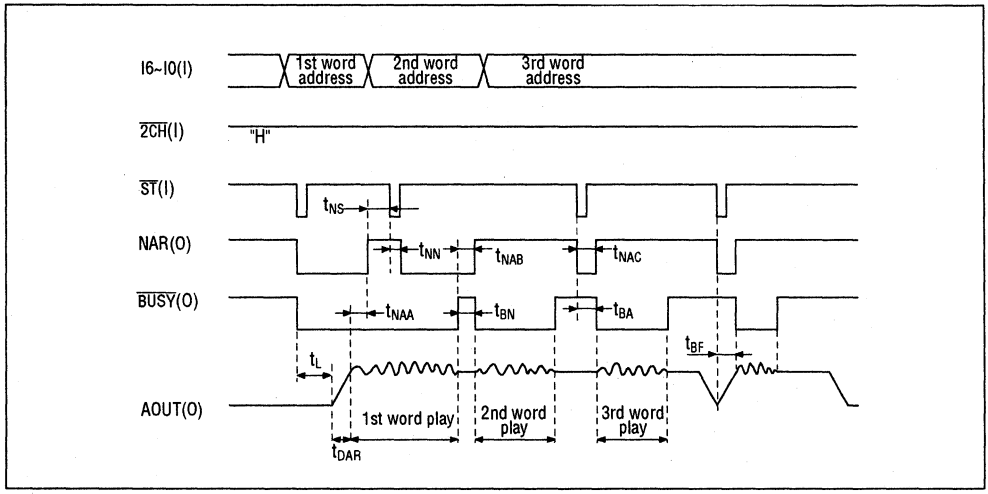
1. At power-on



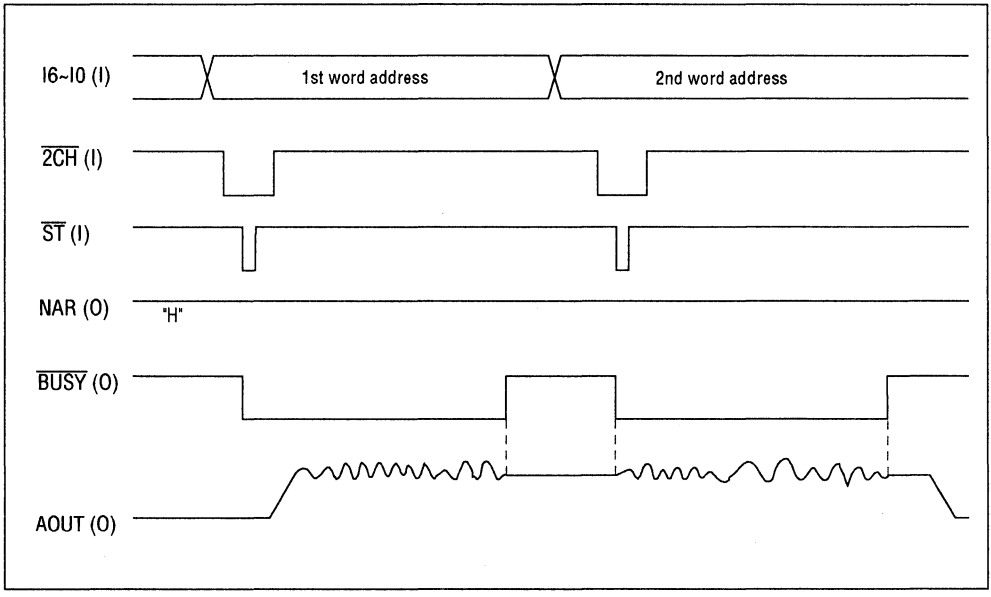
2. At LSI startup and in standby state



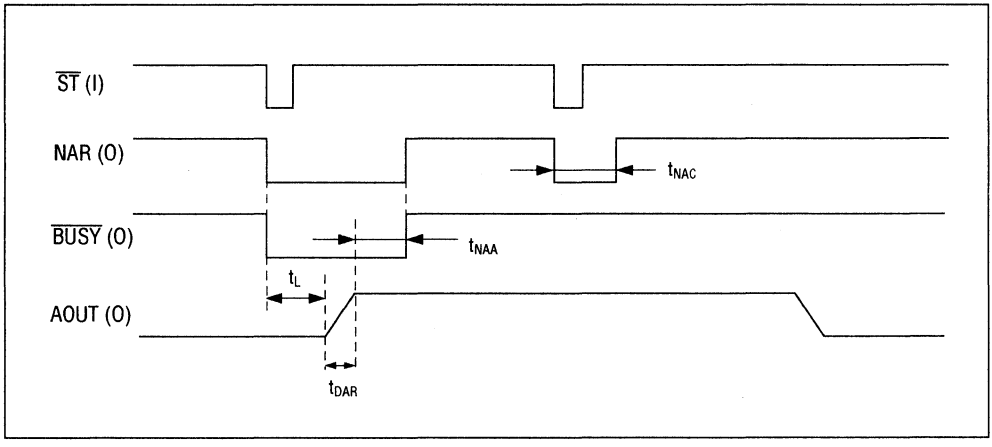
3. Operation in channel 1 only (CPU input interface)



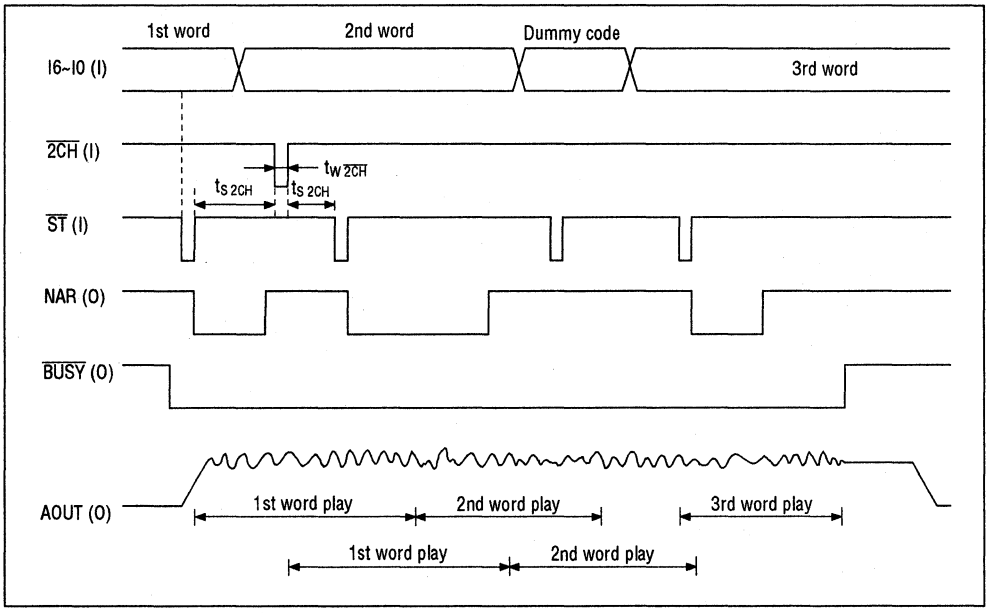
4. Operation in Channel 2 Only (CPU input interface)



5. Operation in Address Designation with No Sound



6. Timing Diagram of Echo Playback in Channel 1



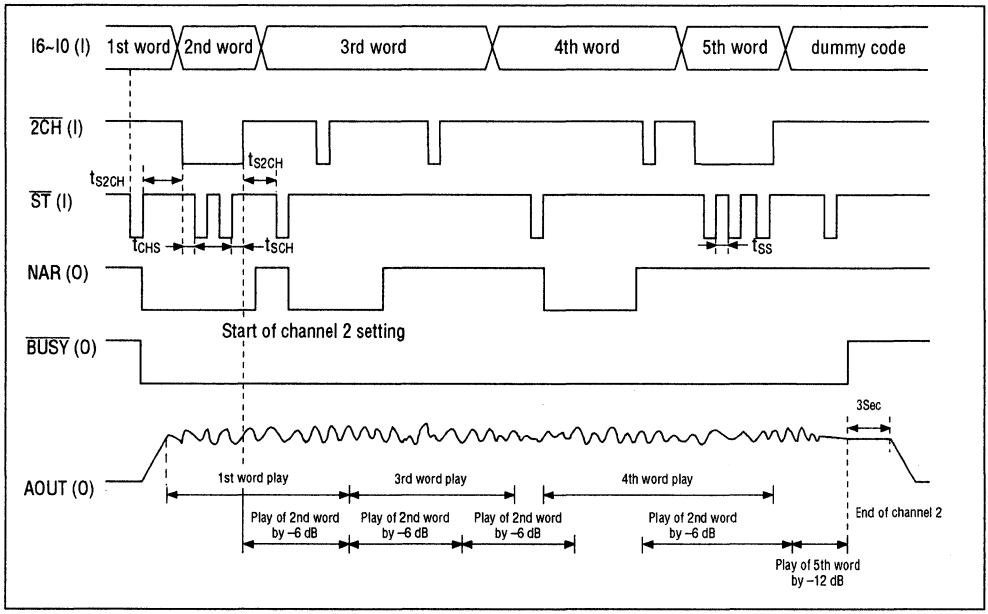
1. Input of the $\overline{2CH}$ pulse without lowering $\overline{ST}$ starts echo playback. Echo playback is canceled unless play is continuous.

2. During echo playback, the waveform is a combination of the playback of channel 1 by the $\overline{ST}$ pulse and a–6 DB playback of channel 2 by the $\overline{2CH}$ pulse.

3. In continuous play, the echo is applied to the next word (continuous play means playback of another word during a single word vocalization.)

4. Input an unused code as a dummy code from the user selectable code at the end of echo playback. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of playback when the standby option is selected.

7. Timing Diagram of Simultaneous Playback in Channel 1 and Channel 2



1. Channel 2 starts playing when the $\overline{ST}$ pulse is input and $\overline{2CH}$="L". The sound volume can be changed by the number of the $\overline{ST}$ pulses using the table below.

2. Channel 2 plays a pre-set word each time the $\overline{2CH}$ pulse is input with the same sound volume until the LSI goes to the standby state or until channel 2 is reset.

3. Please input an unused code as a dummy code from the user selectable codes at the end of playback of channel 2. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of play when the standby option is selected.

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation
2	–6dB attenuation
3	–12dB attenuation

PIN FUNCTIONS

Pin name	Input/output	Function
I0~I6	Input	The user designation word corresponding to the vocalized sound is selected and input to this pin. The code when the $\overline{ST}$ pulse is at the "L" level is input and latched at the rising edge of the $\overline{ST}$ pulse.
$\overline{2CH}$	Input	This pin is used for echo reproduction or simultaneous reproduction of two audible signals. When only the $\overline{2CH}$ pulse is input in 1-channel operation, echo reproduction occurs. The echo delay time can be changed by changing the $\overline{2CH}$ pulse input timing. Inputting the $\overline{ST}$ pulse when $\overline{2CH}$=L causes simultaneous reproduction in 2-channel.
SG	Output	Connect a capacitor of about 1μF to this pin when the LPF output is selected as an option. Capacitor connection to this terminal improves the SN ratio of the LPF. Leave this pin open when the LPF output is not selected.
AOUT	Output	This is the analog voice output pin. Output of the DA converter or output through the LPF can be selected as an option.
$\overline{BUSY}$/NAR (Next Address Request)	Output	Output of the $\overline{BUSY}$ signal or NAR signal can be selected as an option. If $\overline{BUSY}$ is selected, the level of this pin is "L" while speech synthesis is carried out in the LSI. If NAR is selected, the $\overline{ST}$ input for channel 1 is valid when this pin is at the H level.
$\overline{RESET}$	Input	The LSI is set to the standby state when the input to this pin is at the "L" level. In this state, the oscillation stops and the AOUT is set to the GND level for initialization. This LSI has a built-in power on reset circuit. For normal functioning of power on reset, the power supply shall rise within 1ms. If 1ms rise time is unsuitable, apply the $\overline{RESET}$ pulse at the time of power on.
GND	—	Ground terminal
VDD	—	Power supply terminal
OSC1	Input	This pin becomes the crystal oscillator connecting pin when crystal oscillation is selected, and becomes the CR connecting pin when CR oscillation is selected.

Pin name	Input/output	Function
OSC2	Output	This pin becomes the crystal oscillator connecting pin when crystal oscillation is selected, and becomes the RC connecting pin when RC selected.
OSC3/$\overline{CS}$	Input/Output	This pin becomes the RC connecting pin when RC oscillation is selected. If crystal oscillation is selected, it becomes the $\overline{CS}$ pin to enable $\overline{ST}$ input when the $\overline{CS}$ is "L". If the $\overline{CS}$ is unnecessary, fix $\overline{CS}$ at the "L" level.
$\overline{ST}$	Input	When the ST is "L", the signals at I_0 to I_6 are input to the LSI and latched at the rising edge of the $\overline{ST}$. The address input for channel 1 is valid when NAR is "H". For reproduction in channel 2, the sound volume for channel 2 can be varied by the number of $\overline{ST}$ pulses when the $\overline{2CH}$ is "L". If the SW input interface is selected, repeated synthesis occurs when the $\overline{ST}$ is fixed at the "L" level.

FUNCTION DESCRIPTION

1. Voice Code Selection

User selectable words (phrases) are maximum 111-word/phrases. The setting of I0~I6 is as follows:

Table 1 List of User Selected Words

I0~I6	Code explanation
0000000	STOP code
0000001 ↕ 1101111	User selectable codes (111-word)
1110000 ↕ 1110111	BEEP codes
1111000 ↕ 1111111	Test codes (do not use)

2. Non-Usable Range of Built-in ROM

The last two bytes of the built-in ROM are in the non-usable range. Do not use these bytes when analyzing speech.

Built-in ROM Configuration and Non-usable Area

ROM configuration

Speech data control area
Speech data area
Non-usable area

Address list for each area per devices

Device	Speech data area	Non-usable area
MSM6372	00220 ~ 03FFD	03FFE, 03FFF
MSM6373	00220 ~ 07FFD	07FFE, 07FFF
MSM6374	00220 ~ 0FFFD	0FFFE, 0FFFF
MSM6375	00220 ~ 1FFFD	1FFFE, 1FFFF

3. CPU Interface and SW Input Interface

Select either the CPU interface or the SW input interface as an option for the input interface.

3-1 CPU Interface

If the CPU interface is selected, the $\overline{ST}$ pulse becomes valid when the NAR pin is "H". User selected words are then fetched internally and vocalized. This interface is effective for playback of several words continuously. Please note that when the $\overline{ST}$ pulse is kept at the "L" level for longer than 800 µs, one word is played twice (at 8 kHz sampling).

When the $\overline{ST}$ pulse width is between 350 µs and 800 µs, a single word is played once or twice. However, when the $\overline{ST}$ pulse is input from the standby state, a single word is played only once if within 80 µs.

When a $\overline{ST}$ pulse width of longer than 350 µs (master frequency is 64 kHz) is input and the

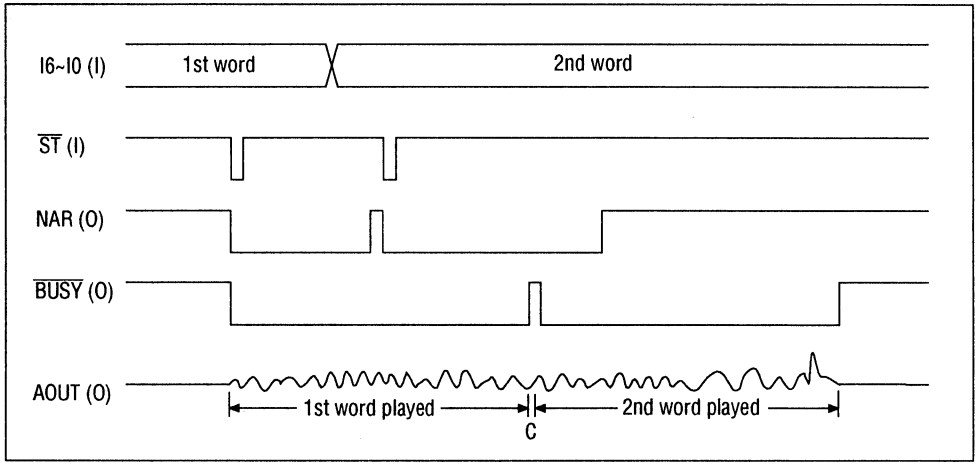


Figure 1 Timing of CPU Interface ($\overline{ST} \leqq 350$ µs)

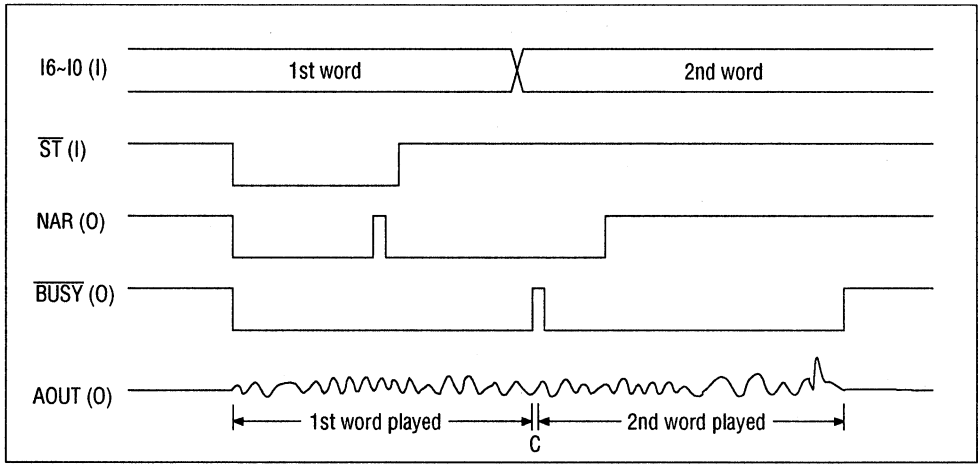


Figure 2 Timing of CPU Interface (800 µs < $\overline{ST}$)

$\overline{BUSY}$ option has been selected, make sure the $\overline{ST}$ pulse is within 800 µs after the rise of $\overline{BUSY}$ pin.

3-2 SW Input Interface

If the SW input interface is selected, the specified word is played repeatedly when $\overline{ST}$ is "L" at the end of play of the specified word and is finished when it is "H".

For example, when this LSI is operated using a push switch, the same word is played repeatedly as long as the switch is pressed and when the switch is released, playback stops when the currently playing word is finished.

When playing different words continuously, change the code of I_0~I_6 and maintain $\overline{ST}$ at the "L" level before the playback is completed.

However, note that the playing is interrupted if the input level of I_6~I_0 becomes "L" instantly when switching the address.

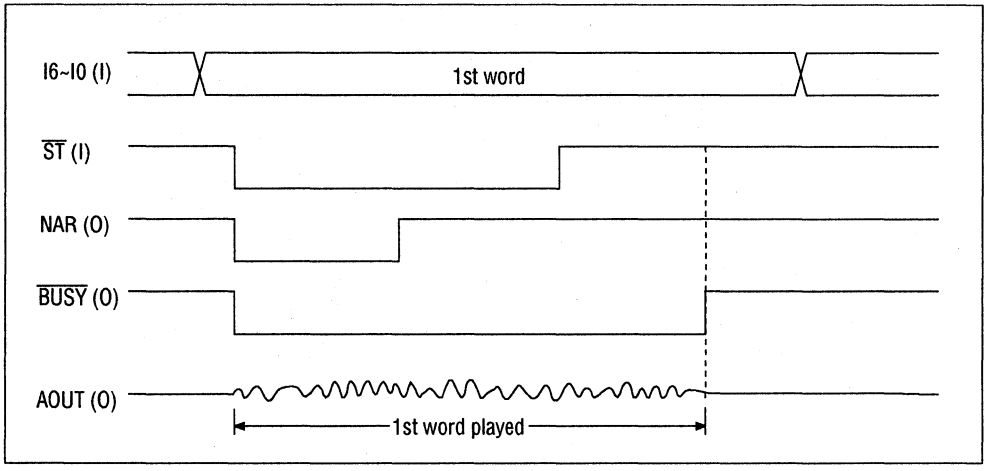


Figure 3 Timing of SW Input Interface (playing one word)

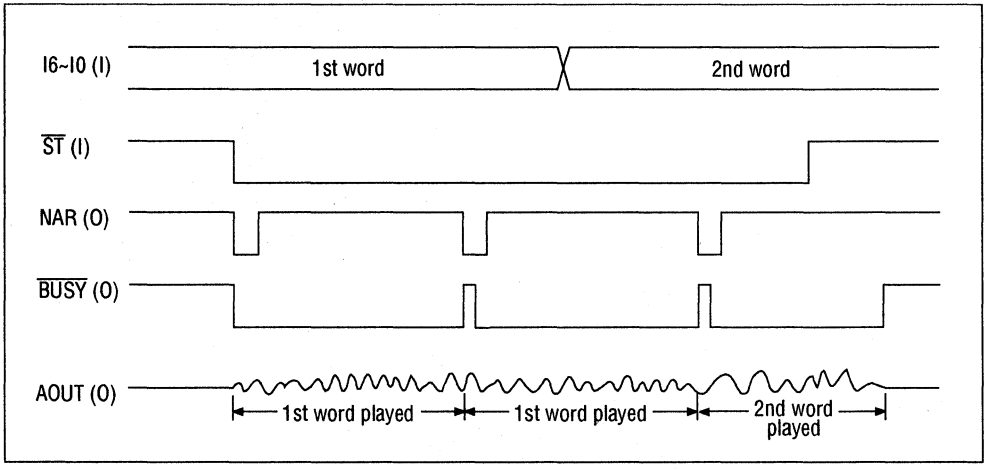


Figure 4 Timing of SW Input Interface (repeated play)

In SW input interface, playback of the 1st and 2nd channels simultaneously is not possible. Neither 2-channel mixing nor echo playback is possible in this interface.

4. BEEP Tone Generation

Since this LSI has an on-chip circuit to generate BEEP tones, the BEEP tones are selected using I_6~I_0. Depending on the word code, the frequency and duration can be changed. The amplitude is approximately 1/4 VDD.

The NAR/$\overline{\text{BUSY}}$ pin outputs a "L" level during BEEP tone play regardless of either NAR or /BUSY is selected as the option. Figure 5 shows such timing.

Neither the STOP code (explained later) nor 2-channel playback is valid during the playback of BEEP tone. The following table shows the relationship between the BEEP tones and addresses when the oscillation frequency is 64 kHz.

Table 2 Relationship between BEEP Tones and Addresses

I6	I5	I4	I3	I2	I1	I0	BEEP tone frequency	Generating duration (sec)
1	1	1	0	0	0	0	2.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500
				1	0	0	1.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500

When the code for a BEEP tone is input while playing either the 1st channel or the 2nd channel, the BEEP tone is generated after the completion of play. The reverse case also holds true.

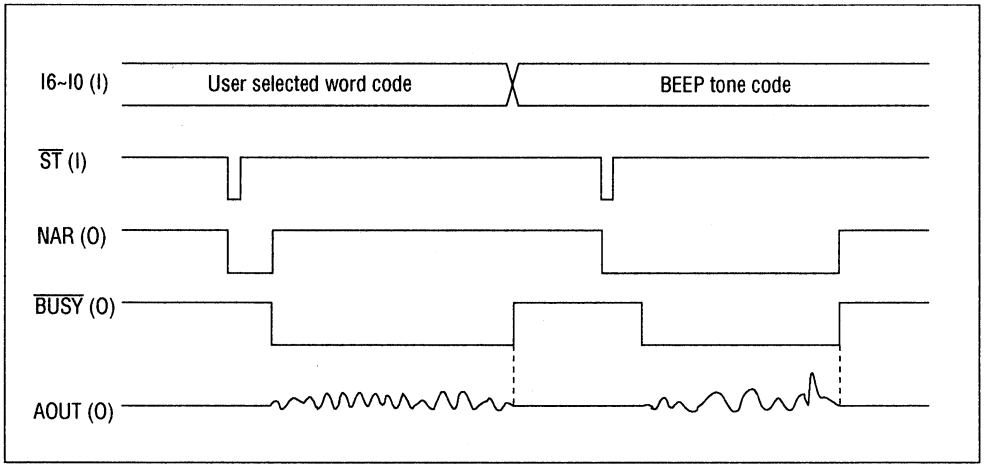


Figure 5 Timing at BEEP Tone Generation

5. Stop Code

Speech playing is finished when the $\overline{ST}$ pulse is input by setting I6~I0 to "0000000" during play. The DA converter becomes 1/2 VDD.

The input method of the $\overline{ST}$ pulse is subject to the AC characteristics when the NAR output is "H". When the NAR output is at the "L" level, the STOP code is valid by setting the $\overline{ST}$ pulse to the "L" level longer than 1 msec (f_{OSC}=64 kHz) or by the timing shown in Figure 6.

The STOP code is not valid during the generation of BEEP tone. When the STOP code is input, only playback is stopped while the oscillation and the analog circuitry are still operating.

When the $\overline{RESET}$ pulse is input, all operations are halted.

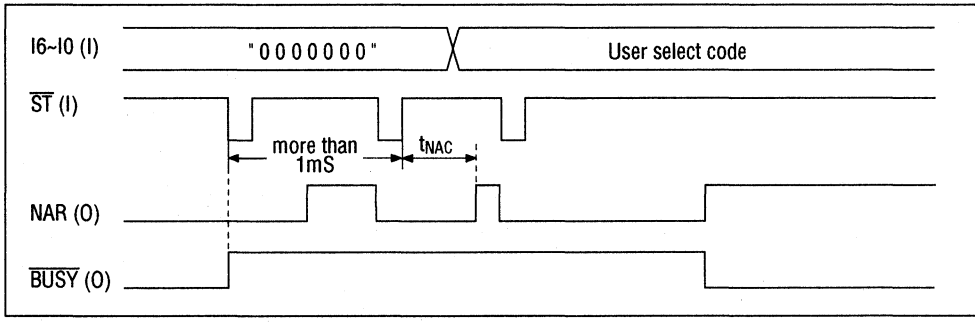


Figure 6 Example of STOP Code Input Timing

6. Sampling Frequencies

Sampling frequencies can be specified for each word in the speech data of the built-in ROM. When the 1st and the 2nd channels are simultaneously played back, the sampling frequency of the 1st channel has priority.

Three types of sampling frequencies can be selected during speech data analysis. The relationship between the master frequency, f_{OSC}, and the sampling frequency, f_S is as follows:

Selection 1	$f_{S1}=f_{OSC}/8$
Selection 2	$f_{S2}=f_{OSC}/10$
Selection 3	$f_{S3}=f_{OSC}/16$

7. Echo Playback and Channel 2 Playback

By using the $\overline{2CH}$ input, echo or 2-channel playback is possible. Because both echo and 2-channel playback use the $\overline{2CH}$ pin, switch between modes by returning the LSI to the standby state.

This function is not available in the SW input interface or during generation of BEEP tones.

7-1 Echo Playback

Echo playback is performed by combining a speech waveform of the 1st channel with a delayed speech waveform with –6 dB attenuation (half the amplitude of the channel 1 speech waveform).

The echo delay time is the time until the $\overline{2CH}$ pulse is input from the start of play of channel 1.

However, when starting this operation from the standby state, pop noise suppression time is not counted as delay time.

In echo playback, echo is applied to all the words during continuous play of channel 1 (continuous play means playback of the next word during playback.)

7-2 2-Channel Mixing Playback

Using 2-channel mixing playback, a different word can be played during the play of channel 1. This has a wide range of application such as BGM (back ground music) and combinations of instruments. Speech data on channel 2 can remain the same while the sound volume may be changed to 1, 1/2 and 1/4 according to channel 1. The change in sound volume is determined by the number of $\overline{ST}$ pulses when starting the 2nd channel.

Once 2-channel mixing is set, it is maintained until the standby state or until channel 2 is reset. Because of this, restart can be accomplished by the input of the $\overline{2CH}$ pulse only.

Table 3 Number of $\overline{ST}$ Pulses and Attenuation

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation (100% of speech data)
2	–6dB attenuation (1/2 of speech data)
3	–12dB attenuation (1/4 of speech data)

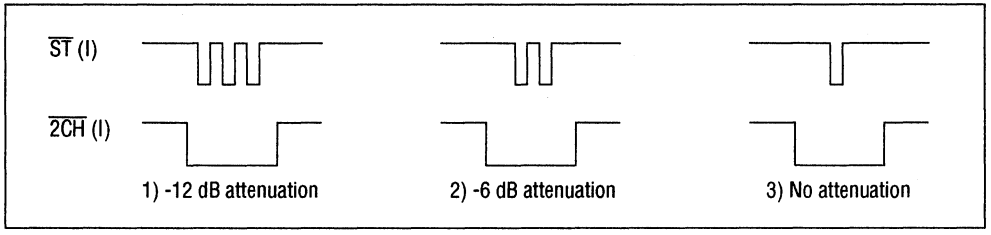


Figure 7 Input Timing of 2 Channel Mixing

8. Standby Transition

When standby transition is enabled as an option, the LSI changes to the standby state and halts all operations unless another word is played within 3 seconds of the completion of playback of a signal word. For this reason, it takes approximately 100mS before the next playback is started as the LSI needs activates the pop noise suppression circuitry.

When standby transition is disabled as an option, the LSI does not go into the standby mode even when playback is completed. At this time, the output from AOUT is approximately 1/2 VDD and the LSI still draws current as oscillation is continued. When restarted, the next playback begins after approximately 350 μS.

If disabling standby transition is disabled as an option, the $\overline{RESET}$ pulse must be input to set to the standby state. Pop noise may be generated at the input of the $\overline{RESET}$ pulse as the output level from AOUT becomes GND level instantly.

9. Voice Output

The voice output pin can be selected by the output of the DA converter either directly or through the built-in low-pass filter.

9-1 Output Waveform of DA Converter

The output amplitude from the DA converter is maximum 4095/4096 × VDD of a square wave that synchronizes with a sampling frequency. When selecting the DA output, addition of an external low-pass filter is highly recommended.

Because the output impedance of DAO varies between 15 kΩ and 35 kΩ, determine the filter constant so that the resistance variation does not influence the cut-off frequency of the low-pass filter.

Table 4 shows the output level from the AOUT pin when selecting an optional DA output.

Table 4 Output Level from DA Converter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	$\frac{1}{4}$VDD	$\frac{1}{2}$VDD	$\frac{3}{4}$VDD	V
2-channel mixing	0.0	$\frac{1}{2}$VDD	VDD	V
BEEP tone playback	$\frac{3}{8}$VDD	$\frac{1}{2}$VDD	$\frac{3}{8}$VDD	V

9-2 Low-pass Filter Output

Since the low-pass filter is composed of switch capacitors, the cut-off frequency varies proportional to the master clock frequency.

When the sampling frequency (f_S) is 1/8 and 1/10 of the master clock frequency, the cut-off frequency, f_{CUT}, is f_{CUT}=3/64 f_{OSC} and is f_{CUT}=3/128 when f_S is 1/16. Table 5 shows the relationship between the sampling frequencies and the cut-off frequencies.

Table 5 Cut-off Frequency of Low-pass Filter

Sampling frequency (f_S)	Master clock frequency (f_{OSC})	Cut-off frequency (f_{cut})
4.0 kHz	64 kHz	1.5 kHz
6.4 kHz	64 kHz	3.0 kHz
8.0 kHz	64 kHz	3.0 kHz
12.8 kHz	128 kHz	6.0 kHz
16.0 kHz	128 kHz	6.0 kHz

The low-pass filter characteristics when the sampling frequency is 8 kHz are shown in Figure 8. Table 6 shows the output level from AOUT when selecting the low-pass filter option.

Table 6 Output Level of Low-pass Filter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	$\frac{1}{4}$VDD	$\frac{1}{2}$VDD	$\frac{3}{4}$VDD	V
2-channel mixing	0.7	$\frac{1}{2}$VDD	VDD–0.7	V
BEEP tone playback	$\frac{3}{8}$VDD	$\frac{1}{2}$VDD	$\frac{3}{8}$VDD	V

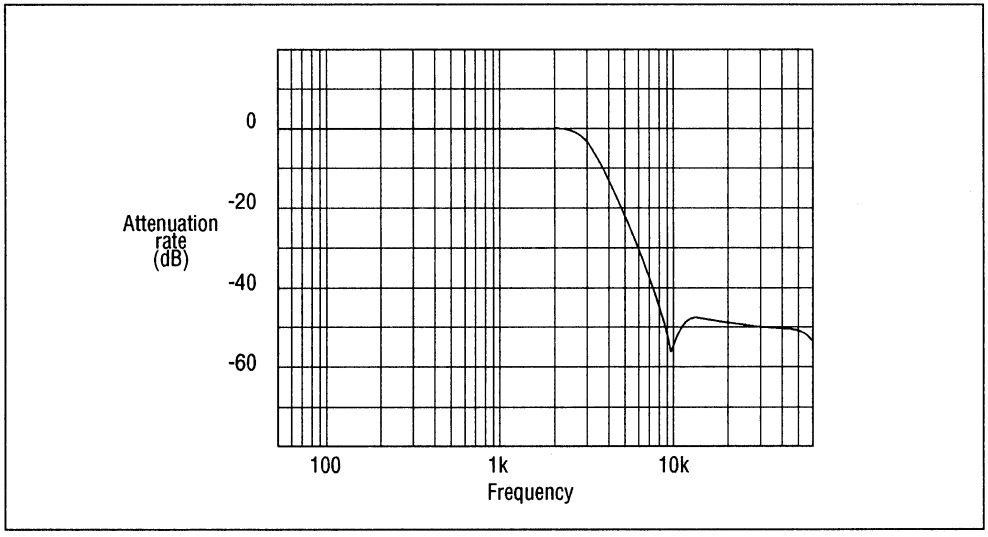


Figure 8 Low-pass Filter Characteristics (f_S=8 kHz)

9-3 Pop Noise Low-Pass Filter Output

Although this LSI has a built-in pop noise suppression circuit, the voltage of the circled portion in the figure below may be changed abruptly by approximately 0.7 V when selecting the low-pass filter output and may generate a "pop" sound.

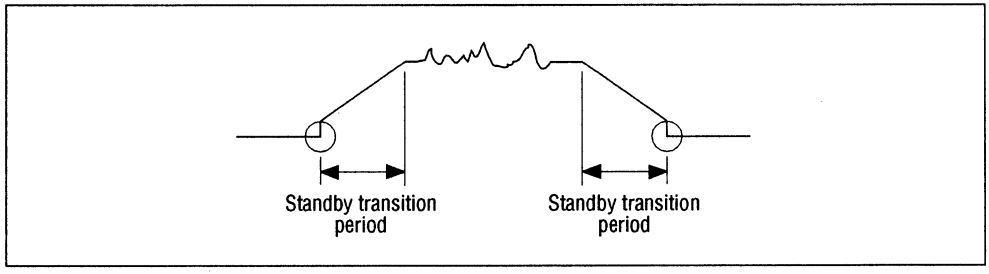


Figure 9 Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the "pop" sound can be reduced. Figure 10 shows the circuit.

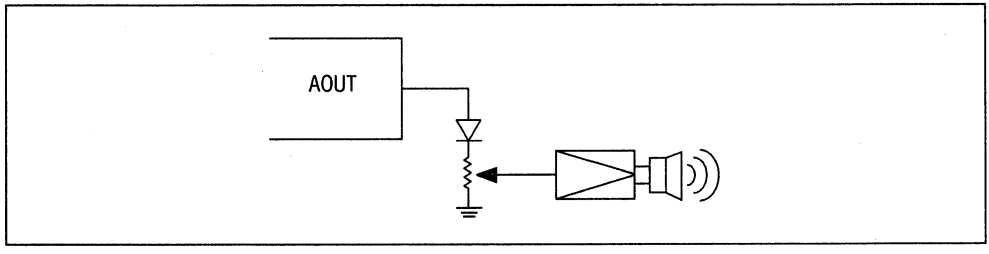


Figure 10 Pop Noise Suppression Circuit

10. RC Oscillation

The external circuit diagram for RC oscillation is shown below:

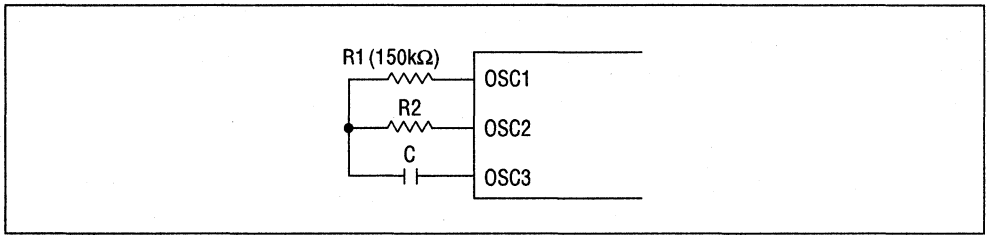


Figure 11 RC Oscillation Connection Circuit

10-1 Determination of RC Constant

The RC oscillation frequency characteristics are shown in Figure 12. If f_{OSC} is set to 64 kHz, choose the appropriate values for C and R_2 using the following as a reference:

C=100 pF, R1=150 kΩ, R2=50 kΩ

10-2 Fluctuation of RC Oscillation Frequencies

When choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R2 as well as the process variations of the LSI.

When using a 50 kΩ R2, the error due to process variations of the LSI is maximum ±4% so that the fluctuation of the RC oscillation frequency when using a capacitance (C) of ±1% accuracy and a resistance (R2) of ±2% accuracy is maximum ±7% approximately.

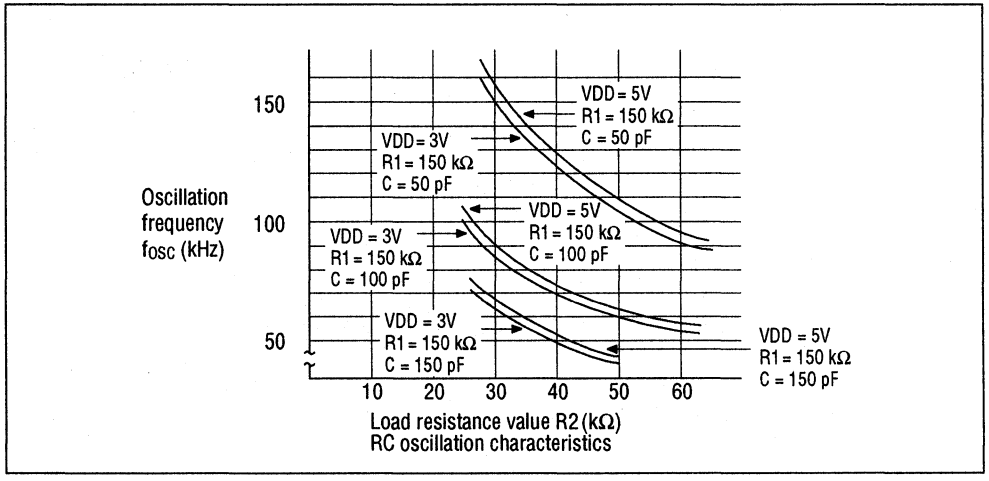


Figure 12 RC Oscillation Frequency

11. Crystal Oscillation

Figure 13 shows an external circuit using a crystal oscillator, KF-38S4-PO102 (64 kHz), made by Kyocera.

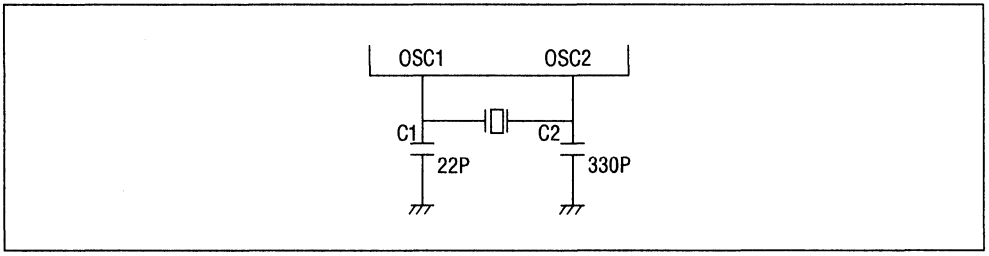


Figure 13 Circuit Diagram of Crystal Oscillator Connection

12. Connection with MSC 1191/1192

When using an MSC1191 and an MSC1192, connect the STBY pin to the OSC3/$\overline{CS}$ pin and the OSC2 pin, respectively. When connecting with an MSC1191/1192, set C and R after mounting it to the board as the oscillation characteristics may change.

13. Option Item List

No.	Item	Center level		Remarks
1	Oscillation circuit	Crystal oscillation	RC oscillation	Crystal oscillation : OSC3/$\overline{CS}$ is a $\overline{CS}$ pin. R_{FB} is built-in. RC oscillation : OSC3/$\overline{CS}$ is a OSC3 pin.
2	Selection of $\overline{BUSY}$ or NAR	$\overline{BUSY}$	NAR	
3	AOUT output	DA output	LPF output	
4	Transition to standby	Yes	No	If the next user-specified word is not input within 3 seconds after playback is finished when "Standby" is selected, the LSI enters the standby state.
5	Input interface	SW input interface	CPU interface	

14. Code Option

There are 13 types of options for the MSM6375 family as shown below. Select one of them.

MSM6375 Family						MSM63P74
Option name	**RC/XT**	**BUSY/NAR**	**DA/LPF**	**Standby**	**CPU/SW**	**Code option**
Option A	RC	NAR	LPF	None	CPU	—
Option B	RC	BUSY	LPF	Available	SW	02
Option C	XT	NAR	LPF	None	CPU	—
Option D	RC	BUSY	LPF	None	SW	—
Option E	XT	NAR	LPF	Available	CPU	05
Option F	XT	NAR	DA	None	CPU	—
Option G	RC	NAR	LPF	Available	CPU	07
Option H	RC	BUSY	LPF	None	CPU	—
Option I	RC	BUSY	DA	Available	CPU	—
Option J	RC	NAR	DA	Available	CPU	—
Option K	XT	BUSY	LPF	None	CPU	—
Option L	RC	BUSY	LPF	Available	CPU	12
Option M	XT	NAR	DA	Available	CPU	—

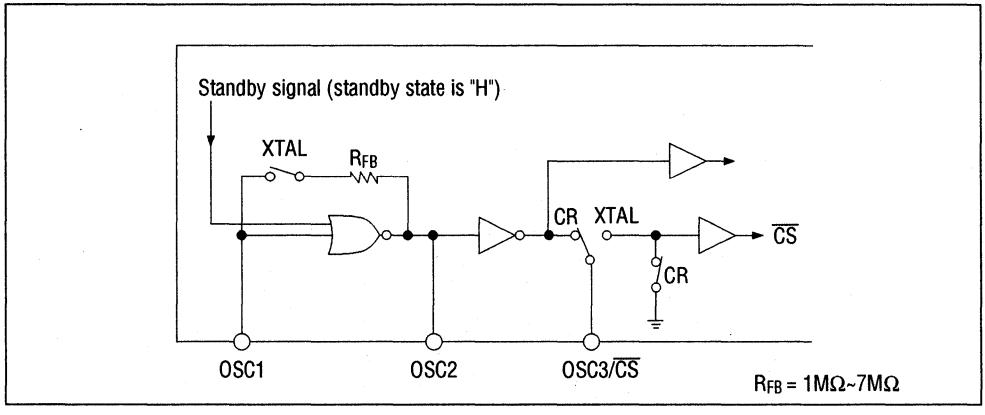


Figure 14 Internal Oscillation Circuit
(The switches in the diagam select RC oscillation)

APPLICATION CIRCUIT EXAMPLE

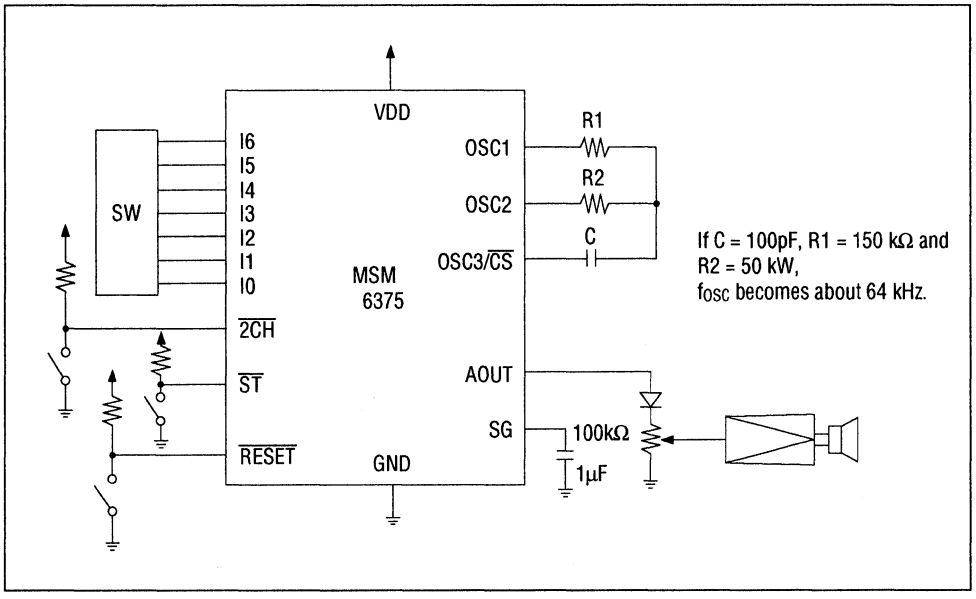


Figure 15 Application Circuit Example in the Case of Selecting RC, LPF and SW in Option

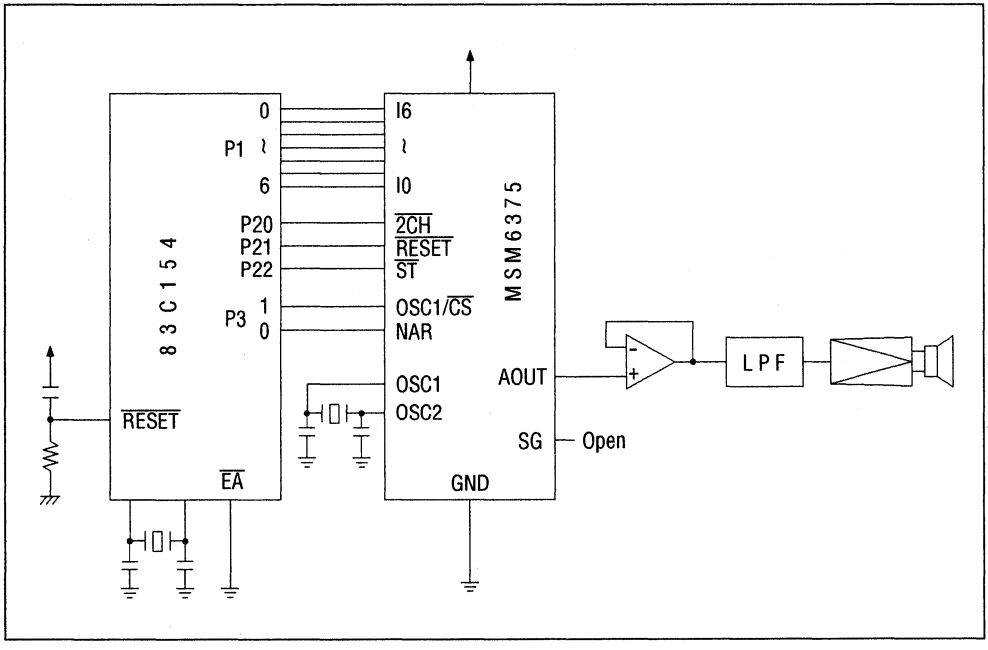


Figure 16 Application Circuit Example in the Case of Selecting XT, DAC and CPU in Option

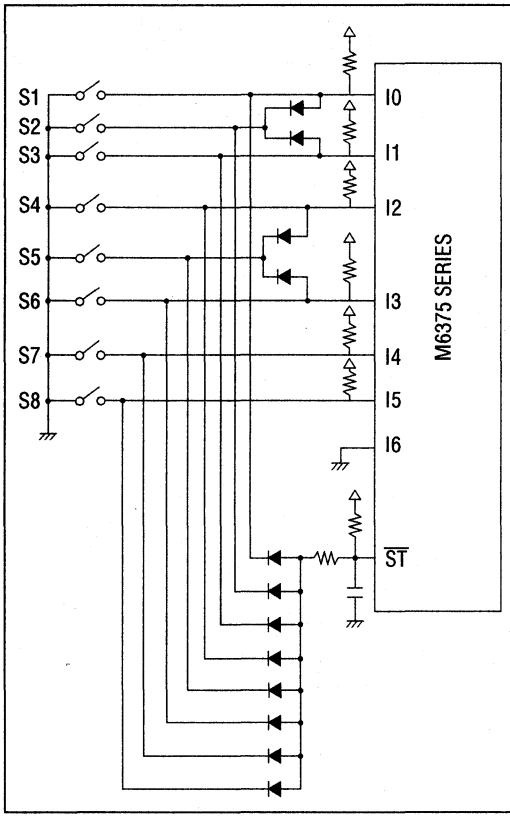
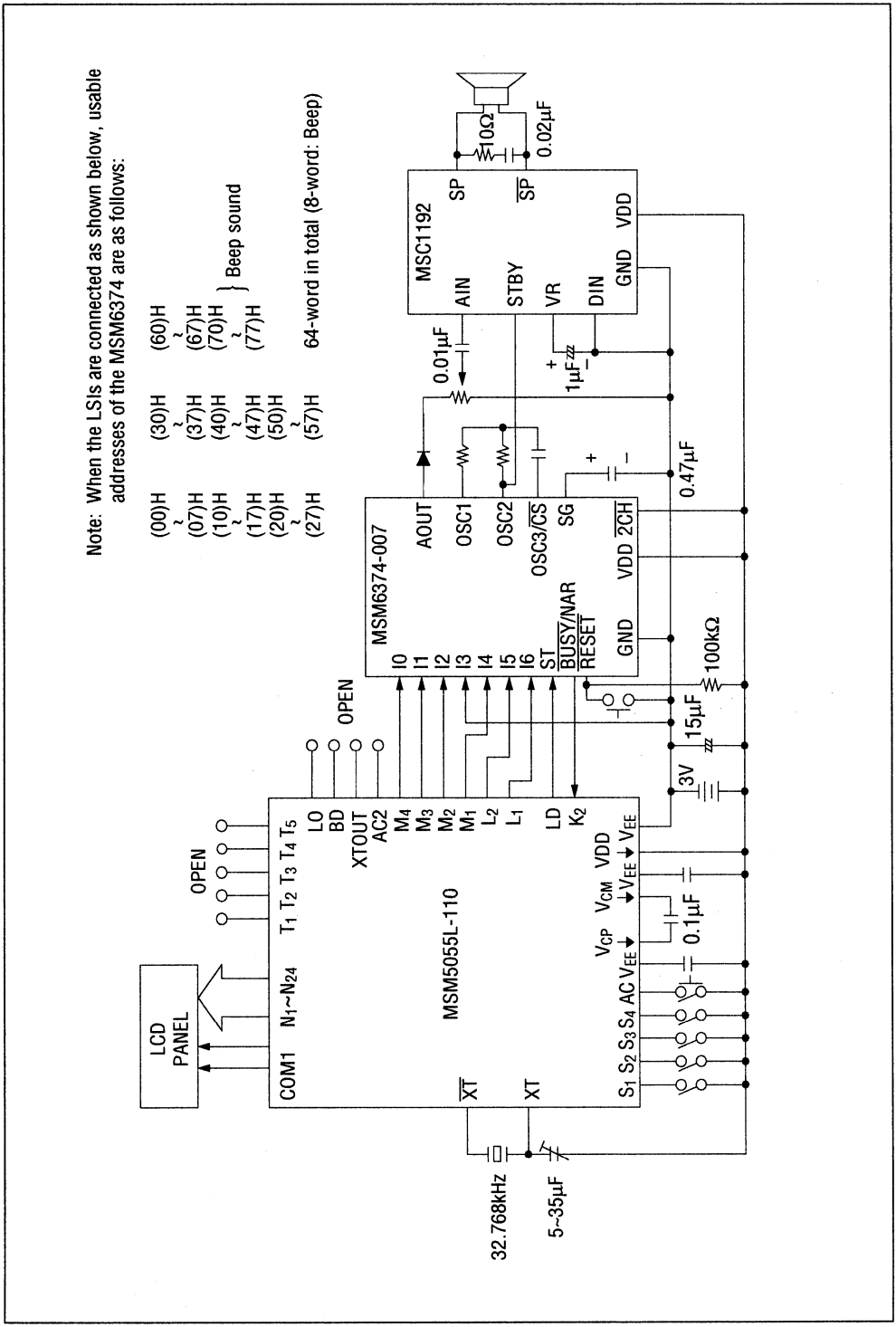


Table for voice address vs. switch

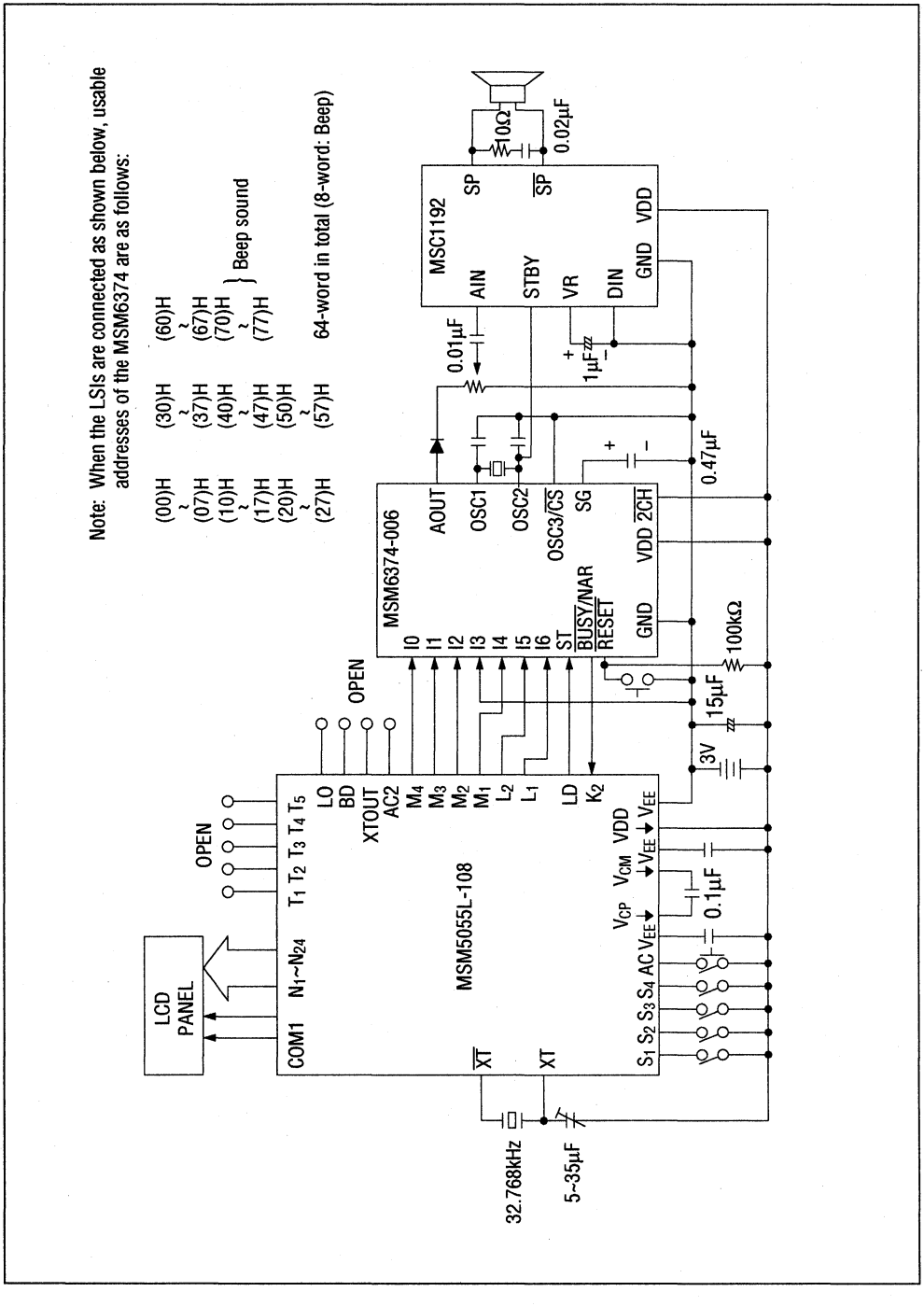
	I6	I5	I4	I3	I2	I1	I0	ADR
S1	0	1	1	1	1	1	0	3 E
S2	0	1	1	1	1	0	0	3 C
S3	0	1	1	1	1	0	1	3 D
S4	0	1	1	1	0	1	1	3 B
S5	0	1	1	0	0	1	1	3 3
S6	0	1	1	0	1	1	1	3 7
S7	0	1	0	1	1	1	1	2 F
S8	0	1	1	1	1	1	1	1 F

Figure 17 Application Circuit Example to Output the Voice of 8 Words by Switch Interface

Application's Circuit: MSM5055L-xx, MSM6374-007, and MSC1192



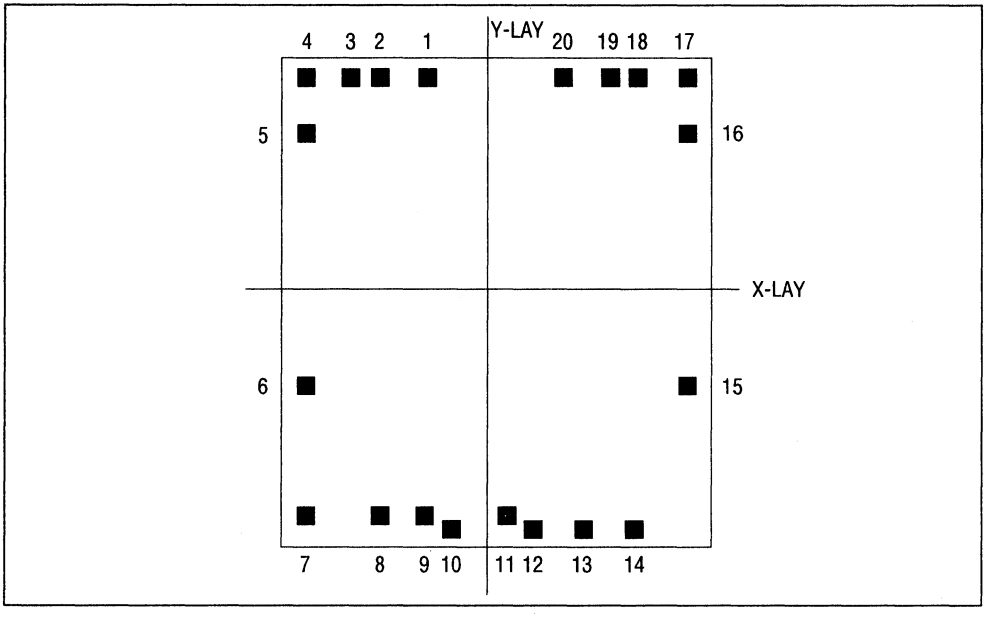
Application's Circuit: MSM5055L-xx, MSM6374-006, and MSC1192



PAD LAYOUT

Product name	MSM6372-XXX
Function	128K-bit ROM built-in voice synthesis LSI
Die size	3.49 × 4.00 (mm²)
Die thickness	350μm±30μm
Pad size	110μm²
Substrate voltage	GND

Pad location diagram

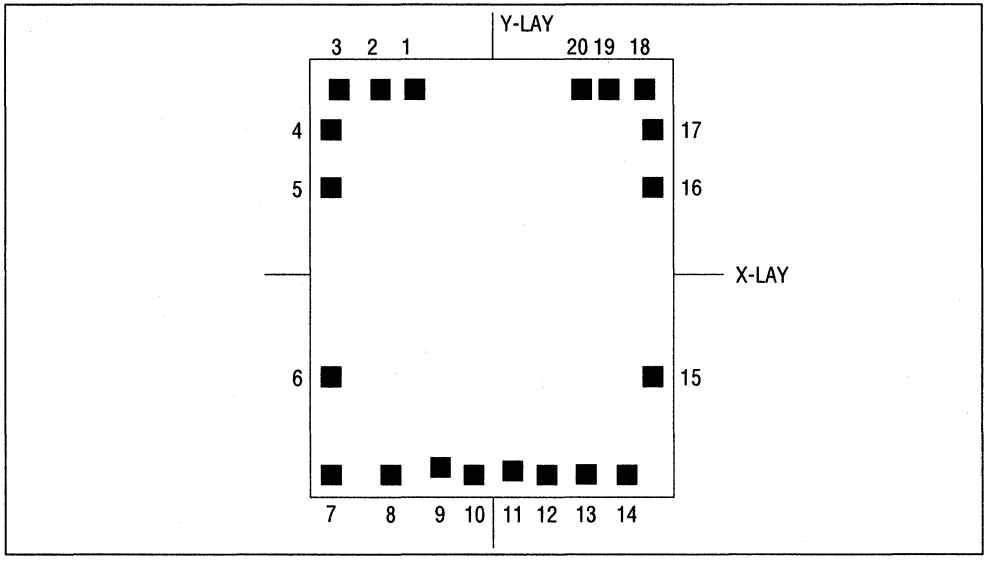


Pad Position (the die center is located at X=0, Y=0) (Unit: μm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−555	1830	11	AVDD	107	−1754
2	I5	−960	1830	12	DVDD	353	−1830
3	I6	−1140	1830	13	OSC1	766	−1829
4	$\overline{2CH}$	−1545	1830	14	OSC2	1180	−1829
5	$\overline{RESET}$	−1590	1421	15	OSC3/$\overline{CS}$	1590	−644
6	$\overline{BUSY}$/NAR	−1590	−650	16	$\overline{ST}$	1590	1421
7	SG	−1509	−1751	17	I0	1545	1830
8	AOUT	−921	−1752	18	I1	1140	1830
9	AGND	−513	−1720	19	I2	960	1830
10	DGND	−281	−1830	20	I3	555	1830

Product name	MSM6373-XXX
Function	256K-bit ROM built-in voice synthesis LSI
Die size	3.49 × 4.70 (mm²)
Die thickness	350µm±30µm
Pad size	110µm²
Substrate voltage	GND

Pad location diagram

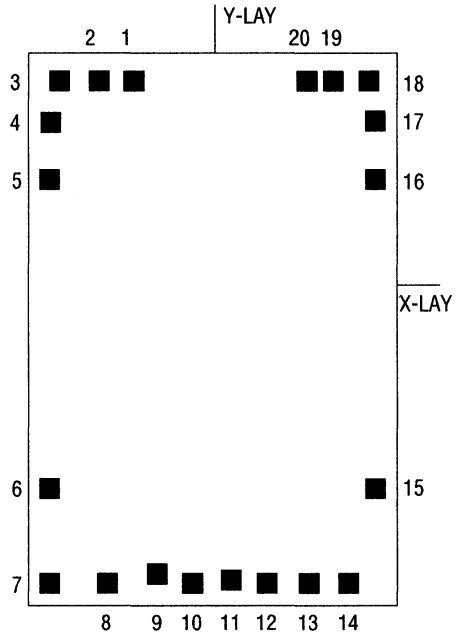


Pad Position (the die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	2180	11	AVDD	107	−2104
2	I5	−1135	2180	12	DVDD	353	−2180
3	I6	−1545	2180	13	OSC1	766	−2179
4	2CH	−1590	1791	14	OSC2	1180	−2179
5	$\overline{\text{RESET}}$	−1590	1235	15	OSC3/$\overline{\text{CS}}$	1590	−994
6	$\overline{\text{BUSY}}$/NAR	−1590	−1024	16	$\overline{\text{ST}}$	1590	1225
7	SG	−1509	−2101	17	I0	1590	1791
8	AOUT	−921	−2102	18	I1	1545	2180
9	AGND	−513	−2070	19	I2	1135	2180
10	DGND	−281	−2180	20	I3	955	2180

Product name	MSM6374-XXX
Function	512K-bit ROM built-in voice synthesis LSI
Die size	3.52 × 6.17 (mm²)
Die thickness	350μm±30μm
Pad size	110μm²
Substrate voltage	GND

Pad location diagram

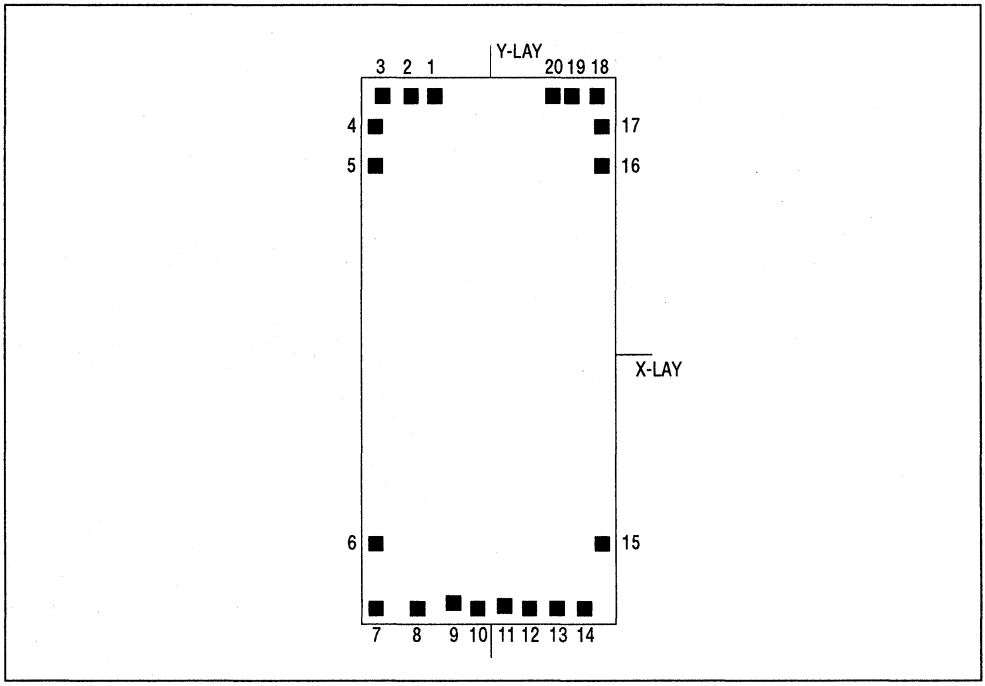


Pad Position (the die center is located at X=0, Y=0) (Unit: μm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	2930	11	AVDD	107	−2854
2	I5	−1135	2930	12	DVDD	353	−2930
3	I6	−1545	2930	13	OSC1	766	−2929
4	$\overline{2CH}$	−1590	2541	14	OSC2	1180	−2929
5	$\overline{RESET}$	−1590	1985	15	OSC3/$\overline{CS}$	1590	−1744
6	$\overline{BUSY}$/NAR	−1590	−1774	16	$\overline{ST}$	1590	1975
7	SG	−1509	−2851	17	I0	1590	2541
8	AOUT	−921	−2852	18	I1	1545	2930
9	AGND	−513	−2820	19	I2	1135	2930
10	DGND	−281	−2930	20	I3	955	2930

Product name	MSM6375-XXX
Function	1M-bit ROM built-in voice synthesis LSI
Die size	3.52 × 9.16 (mm²)
Die thickness	350µm±30µm
Pad size	110µm²
Substrate voltage	GND

Pad location diagram



Pad Position (the die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	4425	11	AVDD	107	−4349
2	I5	−1135	4425	12	DVDD	353	−4425
3	I6	−1545	4425	13	OSC1	766	−4424
4	$\overline{2CH}$	−1590	4036	14	OSC2	1180	−4424
5	$\overline{RESET}$	−1590	3480	15	OSC3/$\overline{CS}$	1590	−3239
6	$\overline{BUSY}$/NAR	−1590	−3269	16	$\overline{ST}$	1590	3470
7	SG	−1509	−4346	17	I0	1590	4036
8	AOUT	−921	−4347	18	I1	1545	4425
9	AGND	−513	−4315	19	I2	1135	4425
10	DGND	−281	−4425	20	I3	955	4425

MSM6375 SERIES GENERAL CODE LIBRARY

ROM built-in voice synthesis LSI is based on customer's order by user's request and voice products for general use are ready as standard.

The standard products are as follows.

Code Name	Application	Language	Sex	fs	Option
MSM6373-329	For an answer phone, a clock	English	Male	4.0kHz	G
MSM6374-007	For an answer phone, a clock	English	Female	6.4kHz	G
MSM6374-544	For an answer phone, a clock	English	Female	6.4kHz	G
MSM6374-545	For an answer phone, a clock	Chinese	Female	6.4kHz	G
MSM6373-308	For an answer phone, a clock	Japanese	Female	4.0kHz	A
MSM6374-519	For an answer phone, a clock	Japanese	Female	5.3kHz	A
MSM6374-006	For an answer phone, a clock	Japanese	Female	6.4kHz	E
MSM6374-553	For an answer phone, a clock	Japanese	Female	6.4kHz	G
MSM6372-119	For a facsimile	Japanese	Female	6.4kHz	L
MSM6372-100	Irasshaimase . Arigatougozaimashita.	Japanese	Female	6.4/8.0kHz	B

Refer to next page and after.

MSM6373-329 Voice Word Address Corresponding List (for English Time Signal)

Specification: F_{OSC} = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	SIX	4.0
01	ONE	4.0	21	SEVEN	4.0
02	TWO	4.0	22	EIGHT	4.0
03	THREE	4.0	23	NINE	4.0
04	FOUR	4.0	24	TWENTY	4.0
05	FIVE	4.0	25	THIRTY	4.0
06	SIX	4.0	26	FORTY	4.0
07	SEVEN	4.0	27	FIFTY	4.0
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	EIGHT	4.0	30	OH	4.0
11	NINE	4.0	31	AM	4.0
12	TEN	4.0	32	PM	4.0
13	ELEVEN	4.0	33	SUN-	4.0
14	TWELVE	4.0	34	MON-	4.0
15	THIR-	4.0	35	TUES-	4.0
16	FOUR-	4.0	36	WEDNES-	4.0
17	FIF-	4.0	37	THURS-	4.0
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	FRI-	4.0	60		
41	SATUR-	4.0	61		
42	-DAY	4.0	62		
43	-TEEN	4.0	63		
44	Set the DAY and TIME	4.0	64		
45	No Voice 30m sec	4.0	65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71	↓	
52			72		
53			73		
54			74		
55			75		
56			76		
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E		
5F			7F	↓	

MSM6374-007 Voice Word Address Corresponding List (for English Time Signal)

Specification: Fosc = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	TY-FOUR	6.4
01	Alarm	6.4	21	TY-FIVE	6.4
02	Setting	6.4	22	TY-SIX	6.4
03	ON	6.4	23	TY-SEVEN	6.4
04	OFF	6.4	24	TY-EIGHT	6.4
05	Hour	6.4	25	TY-NINE	6.4
06	Minute	6.4	26	-TY	6.4
07	Second	6.4	27	-TEEN	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	NINE	6.4	30	ONE	6.4
11	TEN	6.4	31	TWO	6.4
12	ELEVEN	6.4	32	THREE	6.4
13	TWELVE	6.4	33	FOUR	6.4
14	ZERO-	6.4	34	FIVE	6.4
15	TWEN-	6.4	35	SIX	6.4
16	THIR-	6.4	36	SEVEN	6.4
17	FIF-	6.4	37	EIGHT	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	O'CLOCK	6.4	60		
41	SIX-	6.4	61		
42	SEVEN-	6.4	62		
43	EIGHT-	6.4	63		
44	NINE-	6.4	64		
45	TY-ONE	6.4	65		
46	TY-TWO	6.4	66		
47	TY-THREE	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	OH	6.4	70	BEEP Sound Code	
51	FOR-	6.4	71	↓	
52	To Go	6.4	72	↓	
53	It's	6.4	73	↓	
54	No Voice 50ms	6.4	74	↓	
55	No Voice 200ms	6.4	75	↓	
56	AM	6.4	76	↓	
57	PM	6.4	77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6374-544 Voice Word Address Corresponding List (for English Time Signal)

Specification: Fosc = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	-TY	6.4
01	ONE	6.4	21	TY-ONE	6.4
02	TWO	6.4	22	TY-TWO	6.4
03	THREE	6.4	23	TY-THREE	6.4
04	FOUR	6.4	24	TY-FOUR	6.4
05	FIVE	6.4	25	TY-FIVE	6.4
06	SIX	6.4	26	TY-SIX	6.4
07	SEVEN	6.4	27	TY-SEVEN	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	EIGHT	6.4	30	TY-EIGHT	6.4
11	NINE	6.4	31	TY-NINE	6.4
12	TEN	6.4	32	OH	6.4
13	ELEVEN	6.4	33	TEEN	6.4
14	TWELVE	6.4	34	TEEN	6.4
15	ZERO	6.4	35	No Voice 200ms	6.4
16	No Voice 50ms	6.4	36	No Voice 200ms	6.4
17	No Voice 50ms	6.4	37	No Voice 200ms	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	EIGHT-	6.4	60	SUN-	6.4
41	NINE-	6.4	61	MON-	6.4
42	TWEN-	6.4	62	TUES-	6.4
43	THIR-	6.4	63	WEDNES-	6.4
44	FOR-	6.4	64	THURS-	6.4
45	FIF-	6.4	65	FRI-	6.4
46	SIX-	6.4	66	SATUR-	6.4
47	SEVEN-	6.4	67	-DAY	6.4
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	IT'S	6.4	70	BEEP Sound Code	
51	O'CLOCK	6.4	71	↓	
52	AM	6.4	72	↓	
53	PM	6.4	73	↓	
54	SET	6.4	74	↓	
55	DATA	6.4	75	↓	
56	TIME	6.4	76	↓	
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6374-545 Voice Word Address Corresponding List (for Chinese Time Signal)

Specification: Fosc = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	1 (分)	6.4
01	1 (時)	6.4	21	2 (分)	6.4
02	2 (時)	6.4	22	3 (分)	6.4
03	3 (時)	6.4	23	4 (分)	6.4
04	4 (時)	6.4	24	5 (分)	6.4
05	5 (時)	6.4	25	6 (分)	6.4
06	6 (時)	6.4	26	7 (分)	6.4
07	7 (時)	6.4	27	8 (分)	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	8 (時)	6.4	30	9 (分)	6.4
11	9 (時)	6.4	31		
12	10 (時)	6.4	32	0 (分)	6.4
13	11 (時)	6.4	33	10 (分、例如1×分)	6.4
14	12 (時)	6.4	34	2 (分、例如2×分)	6.4
15			35	3 (分、例如3×分)	6.4
16			36	4 (分、例如4×分)	6.4
17	點 (時)	6.4	37	5 (分、例如5×分)	6.4
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	無聲音 200ms	4.0	60		
41	無聲音 50ms	4.0	61		
42	無聲音 30ms	4.0	62		
43			63		
44	早上	6.4	64		
45	上手	6.4	65		
46			66		
47	分	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	鐘聲	6.4	70	BEEP Sound Code	
51			71	↓	
52			72	↓	
53			73	↓	
54			74	↓	
55			75	↓	
56			76	↓	
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6373-308 Voice Word Address Corresponding List (for Japanese Time Signal)

Specification: Fosc = 64kHz, Option A

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	Stop Code	—	20	いっ (分)	4.0
01	いち (時)	4.0	21	さん (分)	4.0
02	に (時・分)	4.0	22	よん (分)	4.0
03	さん (時)	4.0	23		
04	よ (時)	4.0	24	ろっ (分)	4.0
05	ご (時・分)	4.0	25		
06	ろく (時)	4.0	26		
07	なな (時・分)	4.0	27	きゅう (分)	4.0
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	はち (時・分)	4.0	30	無音 200 (ms)	4.0
11	く (時)	4.0	31	じゅっ (分)	4.0
12	じゅう (時)	4.0	32	にじゅっ (分)	4.0
13	じゅういち (時)	4.0	33	さんじゅっ (分)	4.0
14	じゅうに (時)	4.0	34	よんじゅっ (分)	4.0
15			35	ごじゅっ (分)	4.0
16	ぜろ (件)	4.0	36		
17	時	4.0	37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	無音 30 (ms)	4.0	60	シャープ	4.0
41	じゅう	4.0	61	スター	4.0
42	にじゅう	4.0	62	ポーズ	4.0
43	さんじゅう	4.0	63		
44	よんじゅう	4.0	64	日 (にち)	6.4
45	ごじゅう	4.0	65		
46	伝言	4.0	66		
47	件	4.0	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	無音 50 (ms)	4.0	70	Beep Sound Code	
51	午前	4.0	71	↓	
52	午後	4.0	72	↓	
53	ぷん	4.0	73	↓	
54	ふん	4.0	74	↓	
55	です	4.0	75	↓	
56			76	↓	
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6374-519 Voice Word Address Corresponding List (for JapaneseTime Signal)

Specification: Fosc = 53kHz, Option A

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	無音 100 (ms)	3.3
01	いち (月、日、時、秒)	5.3	21	じゅっ (10分、件)	5.3
02	に (時、2分、件)	5.3	22	に (20分/秒)	5.3
03	さん (時)	5.3	23		
04	よ (時)	5.3	24		
05	ご (月、日、時、分、秒、件)	5.3	25	ご (50分/秒)	5.3
06	ろく (月、日、時、秒)	5.3	26	じゅっ (20、30、40分)	5.3
07	なな (月、日、時、分、秒、件)	5.3	27	じゅう (20、30、40秒)	5.3
08	はち (月、日、時、分、秒、件)	5.3	28	午前	5.3
09	く (月、日、時)	5.3	29	午後	5.3
0A	じゅう (月、日、10時、10秒)	5.3	2A	時	5.3
0B	じゅういち (月、日、時、秒)	5.3	2B	ぶん	5.3
0C	じゅうに (月、日、時、分、秒、件)	5.3	2C	ふん	5.3
0D			2D	秒	5.3
0E			2E	です	5.3
0F			2F		
10	れい (時、分、秒)	5.3	30	無音 30 (ms)	3.3
11	いっ (分、件)	5.3	31	じゅう～ (11-19分/件)	5.3
12			32	に (月、日、21-29分/秒、2秒)	5.3
13	さん (月、日、3、13、23、30-39分/秒、件)	5.3	33		
14	よん (日、4、14、24、40-49分/秒、件)	5.3	34		
15			35	ごじゅう～ (51-59分/秒)	5.3
16	ろっ (分、件)	5.3	36	じゅう-(21-29、31-39、41-49分/秒)	5.3
17			37		
18			38		
19	きゅう (分、秒、件)	5.3	39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40	日	5.3	60	BEEP音(64mSec, 883Hz)	5.3
41	月	5.3	61	BEEP音(128mSec, 883Hz)	5.3
42	火	5.3	62		
43	水	5.3	63		
44	木	5.3	64		
45	金	5.3	65		
46	土	5.3	66		
47	曜日	5.3	67		
48	シャープ	5.3	68		
49	アスター	5.3	69		
4A	ポーズ	5.3	6A		
4B	PB	5.3	6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50	無音 50 (ms)	3.3	70	BEEP Sound Code	
51	ぜろ (件)	5.3	71	↓	
52	伝言	5.3	72	↓	
53	件	5.3	73	↓	
54	し (月)	5.3	74	↓	
55	月 (がつ)	5.3	75	↓	
56	日 (にち)	5.3	76	↓	
57	しち (月)	5.3	77	↓	
58			78	Test Code	
59			79	↓	
5A	只今留守にしております	5.3	7A	↓	
5B	後ほどおかけ直し下さい	5.3	7B	↓	
5C	ピーという音の後にお話し下さい	5.3	7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6374-006 Voice Word Address Corresponding List (for JapaneseTime Signal)

Specification: Fosc = 64kHz, Option E

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	いっ (分)	6.4
01	いち (時)	6.4	21	さん (分)	6.4
02	に (時・分)	6.4	22	よん (分)	6.4
03	さん (時)	6.4	23	ご (分)	6.4
04	よ (時)	6.4	24	ろっ (分)	6.4
05	ご (時)	6.4	25	なな (分)	6.4
06	ろく (時)	6.4	26	はっ (分)	6.4
07	なな (時)	6.4	27	きゅう (分)	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	はち (時)	6.4	30		
11	く (時)	6.4	31	じゅっ (分)	6.4
12	じゅう (時)	6.4	32	にじゅっ (分)	6.4
13	じゅういち (時)	6.4	33	さんじゅっ (分)	6.4
14	じゅうに (時)	6.4	34	よんじゅっ (分)	6.4
15	れい (時)	6.4	35	ごじゅっ (分)	6.4
16			36		
17	時	6.4	37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41	じゅう	6.4	61		
42	にじゅう	6.4	62		
43	さんじゅう	6.4	63		
44	よんじゅう	6.4	64		
45	ごじゅう	6.4	65		
46			66		
47	件	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51	午前	6.4	71	↓	
52	午後	6.4	72	↓	
53	ぷん	6.4	73	↓	
54	ふん	6.4	74	↓	
55	です	6.4	75	↓	
56			76	↓	
57	メモ	6.4	77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6374-553 Voice Word Address Corresponding List (for JapaneseTime Signal)

Specification: Fosc = 64kHz, Option G

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20	いっ (分)	6.4
01	いち (時)	6.4	21	さん (分)	6.4
02	に (時、分)	6.4	22	よん (分)	6.4
03	さん (時)	6.4	23	ご (分)	6.4
04	よ (時)	6.4	24	ろっ (分)	6.4
05	ご (時)	6.4	25	なな (分)	6.4
06	ろく (時)	6.4	26	はっ (分)	6.4
07	なな (時)	6.4	27	きゅう (分)	6.4
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10	はち (時)	6.4	30		
11	く (時)	6.4	31	じゅっ (分)	6.4
12	じゅう (時)	6.4	32	にじゅっ (分)	6.4
13	じゅういち (時)	6.4	33	さんじゅっ (分)	6.4
14	じゅうに (時)	6.4	34	よんじゅっ (分)	6.4
15	れい (時)	6.4	35	ごじゅっ (分)	6.4
16			36		
17	時	6.4	37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41	じゅう	6.4	61		
42	にじゅう	6.4	62		
43	さんじゅう	6.4	63		
44	よんじゅう	6.4	64		
45	ごじゅう	6.4	65		
46			66		
47	件	6.4	67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51	午前	6.4	71	↓	
52	午後	6.4	72	↓	
53	ぶん	6.4	73	↓	
54	ふん	6.4	74	↓	
55	です	6.4	75	↓	
56			76	↓	
57	メモ	6.4	77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM6372-119 Voice Word Address Corresponding List
(for telephone and facsimile switchable guidance in Japanese)
Specification: Fosc = 64kHz, Option L

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	STOP Code	—	20		
01	電話を呼び出しております	6.4	21		
02	ファクシミリにつながります	6.4	22		
03	送信ボタンを押して下さい	6.4	23		
04			24		
05			25		
06			26		
07			27		
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41			61		
42			62		
43			63		
44			64		
45			65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71	↓	
52			72		
53			73		
54			74		
55			75		
56			76		
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A		
5B			7B		
5C			7C		
5D			7D		
5E			7E		
5F			7F	↓	

MSM6372-100 Voice Word Address Corresponding List
(for telephone and facsimile switchable guidance in Japanese)
Specification: Fosc = 64kHz, Option B

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
00	Stop Code	—	20		
01	いらっしゃいませ	8.0	21		
02	いらっしゃいませ	6.4	22		
03	ありがとうございました	8.0	23		
04	ありがとうございました	6.4	24		
05			25		
06			26		
07			27		
08			28		
09			29		
0A			2A		
0B			2B		
0C			2C		
0D			2D		
0E			2E		
0F			2F		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
1A			3A		
1B			3B		
1C			3C		
1D			3D		
1E			3E		
1F			3F		

Address	Voice Word	fs(kHz)	Address	Voice Word	fs(kHz)
40			60		
41			61		
42			62		
43			63		
44			64		
45			65		
46			66		
47			67		
48			68		
49			69		
4A			6A		
4B			6B		
4C			6C		
4D			6D		
4E			6E		
4F			6F		
50			70	BEEP Sound Code	
51			71	↓	
52			72	↓	
53			73	↓	
54			74	↓	
55			75	↓	
56			76	↓	
57			77	↓	
58			78	Test Code	
59			79	↓	
5A			7A	↓	
5B			7B	↓	
5C			7C	↓	
5D			7D	↓	
5E			7E	↓	
5F			7F	↓	

MSM63P74-02/05/07/12

512Kbit OTP BUILT-IN VOICE SYNTHESIS LSI

GENERAL DESCRIPTION

The MSM63P74 is a single-chip CMOS ADPCM speech synthesizer LSI that has a on-chip OTP (One time PROM) for speech data storage. This LSI is compatible with the MSM6375 family. In addition to on-chip programmable ROM, it contains, a 12bit DA converter, LPF, 2-channel mixing function, and beep tone generation. Speech analysis and speech data programming can be easily performed by the user by means of the development tool, AR76-202 from OKI.

This LSI is suitable for applications where programming flexibility is needed for multiple voice codes, further more for medium or small quantities and for minimum turn around times.

If mass production becomes feasible as your application matures, our MSM6375 family with on-chip mask ROM provides you with the proper compatibility.

FEATURES

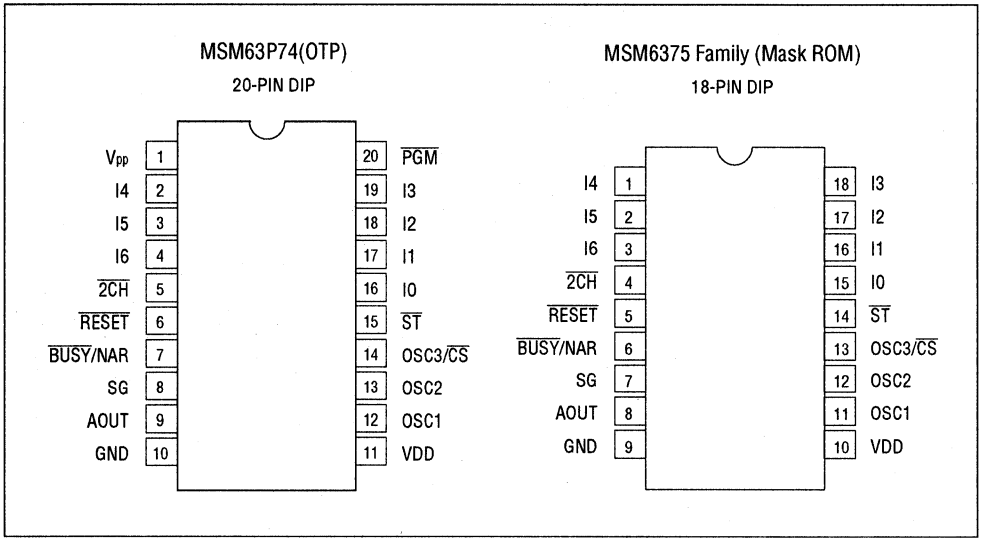
- Built-in 512Kbit OTP
- Single-chip CMOS
- 4bit ADPCM algorithm
- Echo or 2 channel mixing functions
- Maximum number of words: 111-word
- Built-in 12bit DA converter
- Built-in LPF
- Standby function
- Oscillation: RC or crystal
- Data write time (when using AR76-202)
  Write and verify approx. 55 seconds
  Verify only approx. 15 seconds
- Data retention time: 10 years min.
- Package 20pin DIP (DIP20-P-300-W1)

fosc [kHz]	fsam [kHz]	fcut [kHz]	Output Time (sec)	BEEP TONE	VDD for the use of internal LPF
64	4.0	1.5	32	1kHz	2.7V
	6.4	3.0	20	&	〃
	8.0	3.0	16	2kHz	5.5V
128	8.0	3.0	16	2kHz	4.5V
	12.8	6.0	10	&	〃
	16.0	6.0	8	4kHz	5.5V

PIN CONFIGURATION (TOP VIEW)

The pin layout of the MSM63P74 basically matches with that of the on-chip mask ROM family but the MSM63P74 has two more pins than the MSM6375 family for the programming function.

These two pins (V_{PP}, $\overline{PGM}$) may be left open during playback after programming.

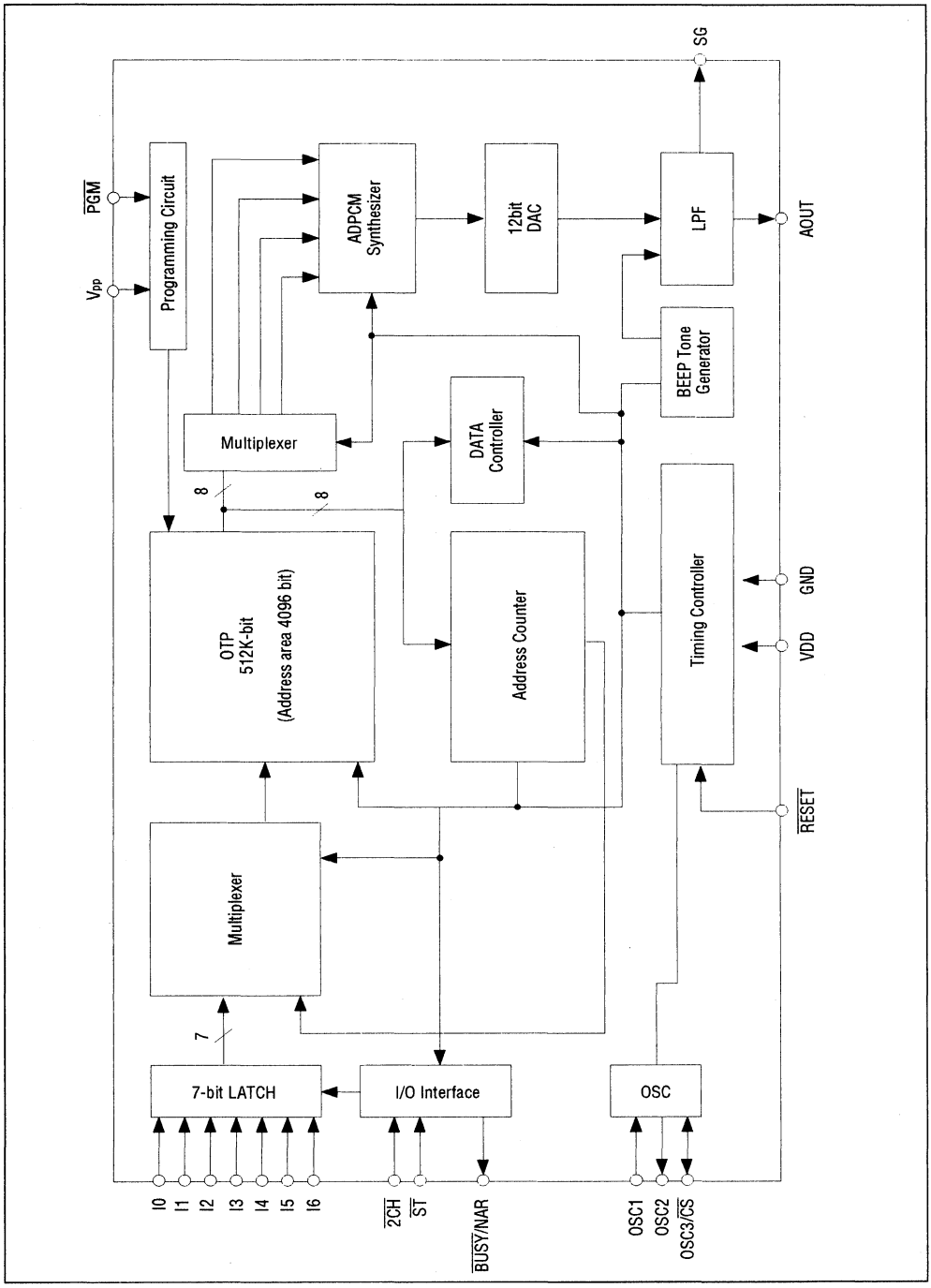


DIFFERENCES BETWEEN THE MSM63P74 AND THE MSM6375 FAMILY

- Built-in memory (OTP)
- DC characteristics
- External C and R values at RC oscillation (partially)
- Mask bonding options (02/05/07/12) Refer to CODE OPTION.
- Pin layout (additional programming pins)
- Maximum sampling frequency 16kHz
- 20pin DIP

BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings (GND = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_I	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Range (GND = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage	VDD	LPF selection	64kHz < f_{osc}	+4.5 ~ +5.5	V
			$f_{osc} \leqq$ 64kHz	+2.7 ~ +5.5	V
Operating temperature	T_{op}	—		−40 ~ +85	°C
Master oscillation frequency (Note 1)	f_{osc}	LPF output		40 ~ 140	kHz

Note 1: The precision of the oscillation frequency with the optional RC oscillator depends strongly on the precision of external C and R.

• DC Characteristics (VDD= 5.0V, GND = 0V, Ta = -40 ~ +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH}	—	4.2	—	—	V
"L" level input voltage	V_{IL}	—	—	—	0.8	V
"H" level output voltage	V_{OH}	I_{OH} = −40 µA	4.6	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" level input current 1	I_{IH1}	V_{IH} = VDD	—	—	10	µA
"H" level input current 2	I_{IH2}	V_{IN} = V_{DD} (applied to $\overline{PGM}$ pin)	150	—	450	µA
"L" level input current	I_{IL}	V_{IL} = 0V	−10	—	—	µA
Operating current consumption	I_{DD}	—	—	6	20	mA
Standby current consumption	I_{DS}	—	—	0.1	100	µA
Relative precision of DA	$\lvert V_{DAE} \rvert$	no load	—	—	40	mV
LPF load resistance	R_{AOUT}	—	50	—	—	kΩ

- **DC Characteristics (VDD = 3.1V, GND = 0V, Ta = –40 ~ 85°C)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH}	—	2.6	—	—	V
"L" level input voltage	V_{IL}	—	—	—	0.5	V
"H" level output voltage	V_{OH}	I_{OH} = 10 µA	2.7	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 10 µA	—	—	0.4	V
"H" level input current 1	I_{IH1}	V_{IH} = VDD	—	—	1	µA
"H" level input current 2	I_{IH2}	V_{IN} = VDD (applied to $\overline{PGM}$ pin)	100	—	300	µA
"L" level input current	I_{IL}	V_{IL} = 0V	–1	—	—	µA
Operating current consumption	I_{DD}	—	—	3	6	mA
Standby current consumption	I_{DS}	—	—	0.1	100	µA
Relative precision of DA	$\lvert V_{DAE} \rvert$	no load	—	—	20	mV
LPF load resistance	R_{AOUT}	—	50	—	—	kΩ

• AC Characteristics (V_{DD} = 5V, Ta = –40 ~ 85°C, f_{OSC} = 64 kHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µs
$\overline{ST}$ input pulse width (Note 3)	$t_{W(\overline{ST})}$	—	0.35	–	350	µs
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µs
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µs
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µs
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µs
Data set time	t_{DW}	—	10	–	–	µs
Data hold time	t_{WD}	—	10	–	–	µs
$\overline{CS}$ setup time (Note 1)	t_{CS}	—	10	–	–	µs
$\overline{CS}$ hold time (Note 1)	t_{SC}	—	10	–	–	µs
Selectable sampling frequency	fsam1	f_{osc}/8	–	8.0	–	kHz
	fsam2	f_{osc}/10	–	6.4	–	kHz
	fsam3	f_{osc}/16	–	4.0	–	kHz
$\overline{BUSY}$ output time (1)	t_{SBS}	—	–	–	10	µs
$\overline{BUSY}$ output time (2) (Note 2)	t_{BN}	At fsam = 8 kHz	350	375	400	µs
$\overline{BUSY}$ output time (3) (Notes 2 and 6)	t_{BF}	At master frequency=64 kHz	–	–	64	ms
$\overline{BUSY}$ output time (4) (Note 2)	t_{BA}	At fsam=8 kHz	350	375	400	µs
NAR output time (1) (Note 5)	t_{SNS}	–	–	–	10	µs
NAR output time (2)	t_{NN}	–	–	–	500	ns
NAR output time (3) (Note 4)	t_{NAA}	At fsam=8 kHz	350	375	400	µs
NAR output time (4) (Note 4)	t_{NAB}	At fsam=8 kHz	350	375	400	µs
NAR output time (5) (Note 4)	t_{NAC}	At master	350	–	550	µs
D/A converter transition time	t_{DAR}, t_{DAF}	frequency=64 kHz At master	60	64	68	ms
LPF stabilizing time (Note 5)	t_L	frequency=64 kHz At master	12	16	20	ms
Standby transition time (at end of speech output)	t_{STB}	frequency=64 kHz At master	2.9	3.0	3.1	S
$\overline{ST}$-$\overline{2CH}$ pulse interval	t_{S2CH}	frequency=64 kHz —	1.0	–	–	ms
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µs

Note 1: When crystal oscillation is selected as an option.
Note 2: When $\overline{BUSY}$ is selected as an option. The duration is proportional to fsam.
Note 3: When the CPU interface is selected as an option, the MAX value is proportional to fsam. The MAX value when playing one word (using the SW interface) is equal to the speech cycle time.
Note 4: When NAR is selected as an option. The duration is proportional to fsam. (When fsam is high, the cycle is shortened.)
Note 5: Applicable at the start of oscillation.
Note 6: When playback occurs during the standby transition period (t_{DAF}).

- **AC Characteristics (VDD = 5V, Ta = –40 ~ 85°C, f_{OSC} = 40 - 140 kHz)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µs
$\overline{ST}$ input pulse width (Note 2)	$t_{W(\overline{ST})}$	—	0.35	–	a	µs
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µs
$\overline{ST}$-$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µs
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µs
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µs
Data set time	t_{DW}	—	10	–	–	µs
Data hold time	t_{WD}	—	10	–	–	µs
$\overline{CS}$ setup time (Note 1)	t_{CS}	—	10	–	–	µs
$\overline{CS}$ hold time (Note 1)	t_{SC}	—	10	–	–	µs
Selectable sampling frequency	f_{sam1}	—	–	$f_{osc}/8$	–	kHz
	f_{sam2}	—	–	$f_{osc}/10$	–	kHz
	f_{sam2}	—	–	$f_{osc}/16$	–	kHz
$\overline{BUSY}$ output time (1) (Note 3)	t_{SBS}	—	–	–	10	µs
$\overline{BUSY}$ output time (2)	t_{BN}	—	a	b	c	µs
$\overline{BUSY}$ output time (3) (Note 4)	t_{BF}	—	–	–	e	ms
$\overline{BUSY}$ output time (4)	t_{BA}	—	a	b	c	µs
NAR output time (1) (Note 3)	t_{SNS}	—	–	–	10	µs
NAR output time (2)	t_{NN}	—	–	–	500	ns
NAR output time (3)	t_{NAA}	—	a	b	c	µs
NAR output time (4)	t_{NAB}	—	a	b	c	µs
NAR output time (5)	t_{NAC}	—	a	–	d	µs
D/A converter transition time (Note 3)	t_{DAR}, t_{DAF}	—	e-4	e	e+4	ms
LPF stabilizing time	t_L	—	f-4	f	f+4	ms
Standby transition time (at end of speech output)	t_{STB}	—	g-0.1	g	g+0.1	sec
$\overline{ST}$-$\overline{2CH}$ pulse interval	t_{S2CH}	—	h	–	–	ms
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µs

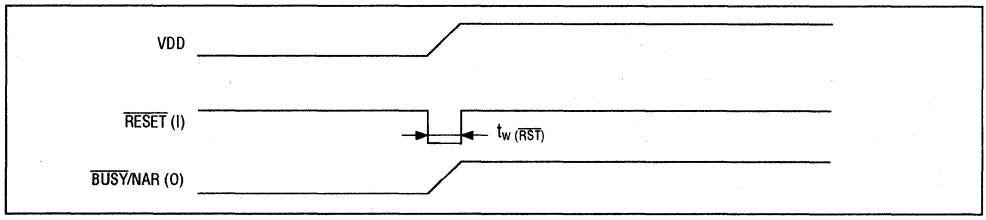
$$a = 350 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad b = 375 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad c = 400 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad d = 550 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)}$$

$$e = 64 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad f = 16 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad g = 3.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad h = 1.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)}$$

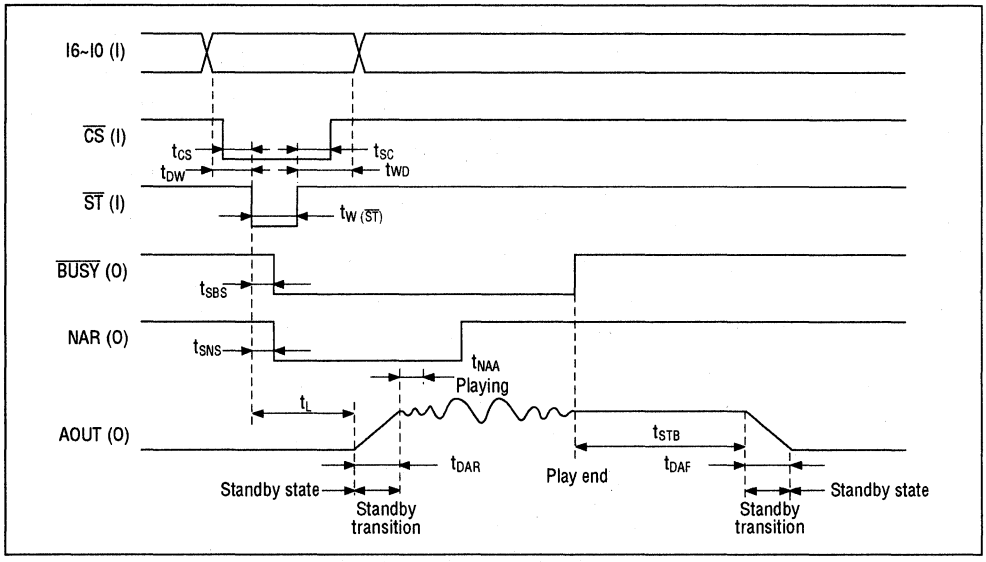
Note 1: When crystal oscillation is selected as an option.
Note 2: When the CPU interface is selected as an option, the MIN value when playing one word (using the SW interface) is 0.35µS and the MAX value is equal to the speech cycle time.
Note 3: Applicable at the start of oscillation.
Note 4: When playback occurs during the standby transition period (t_{DAF}).

TIMING DIAGRAMS

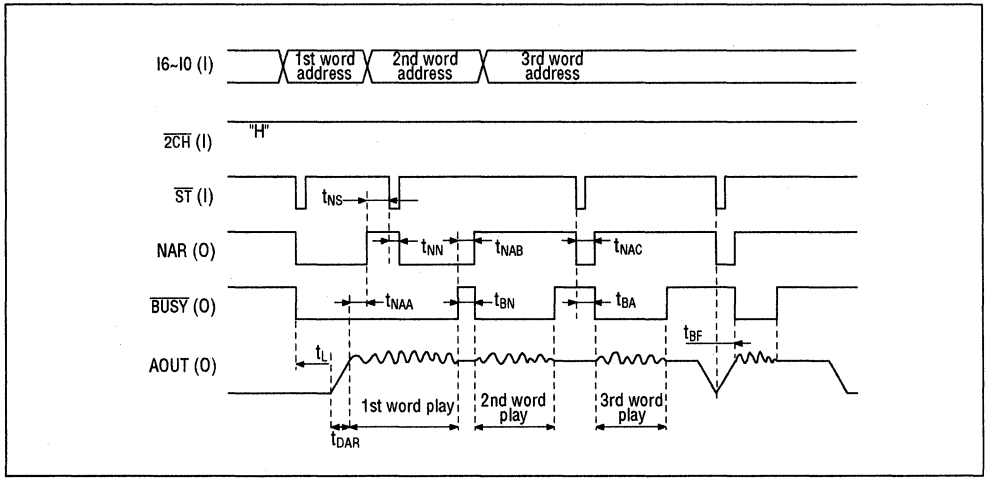
1. At power-on



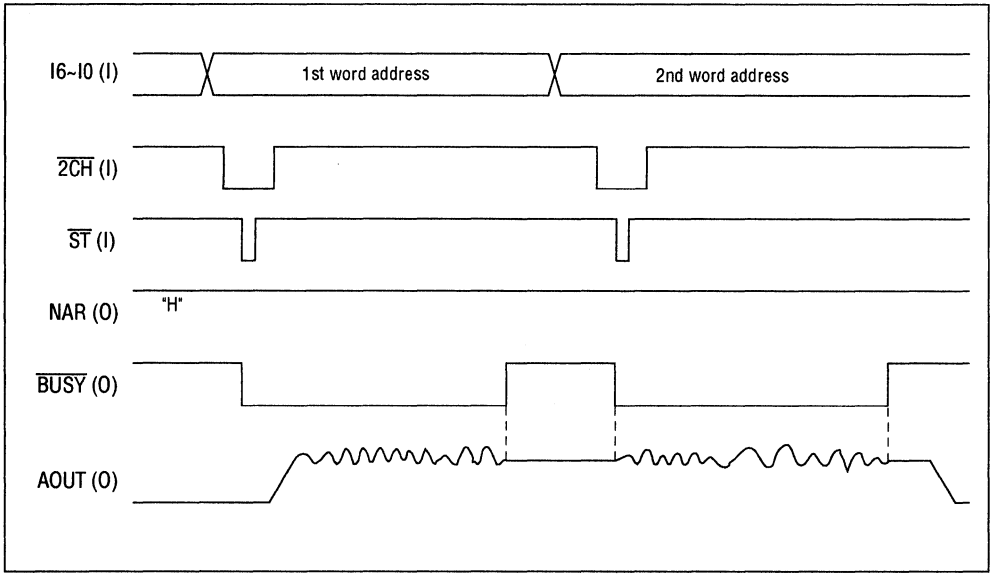
2. At LSI startup and in standby state



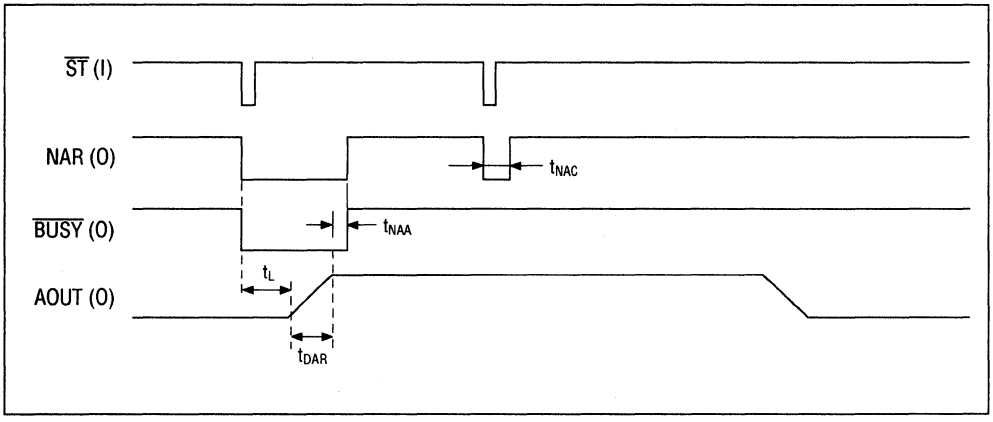
3. Operation in channel 1 only (CPU input interface)



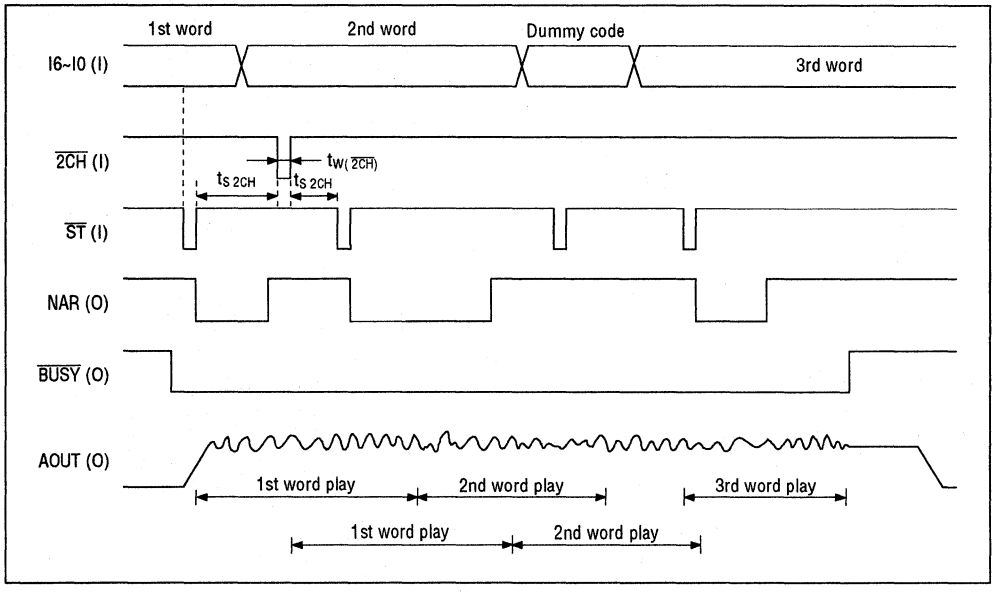
4. Operation in Channel 2 Only (CPU input interface)



5. Operation in Address Designation With no Voice



6. Timing Diagram of Echo Playback in Channel 1



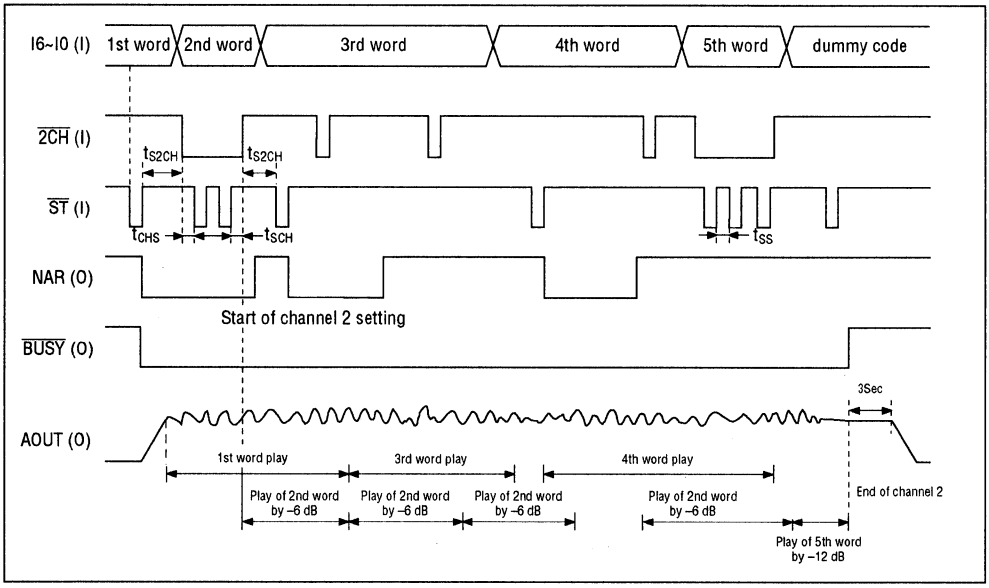
1. Input of the $\overline{2CH}$ pulse without lowering $\overline{ST}$ starts echo playback. Echo playback is canceled unless play is continuous.

2. During echo playback, the waveform is a combination of the playback of channel 1 by the $\overline{ST}$ pulse and a-6 DB playback of channel 2 by the $\overline{2CH}$ pulse.

3. In continuous play, the echo is applied to the next word (continuous play means playback of another word during a shingle word vocalization.)

4. Input unused code as a dummy code from the user selectable code at the end of echo playback. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of playback.

7. Timing Diagram of Simultaneous Playback in Channel 1 and Channel 2



1. Channel 2 starts playing when the $\overline{ST}$ pulse is input and $\overline{2CH}$ = "L". The sound volume can be changed by the number of the $\overline{ST}$ pulses using the table below.

2. Channel 2 plays a pre-set word each time the $\overline{2CH}$ pulse is input with the same sound volume until the LSI goes to the standby or until channel 2 is reset.

3. Input unused code as a dummy code from the user selectable codes at the end of playback of channel 2. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of playback.

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation
2	-6dB attenuation
3	-12dB attenuation

PIN DESCRIPTION

Pin Name	I/O	Function
I0 ~ I6	I	These are the phrase address inputs by which a designed phrase can be selected for playback. The code at I0~I6 when the $\overline{ST}$ pulse goes "L" level is input and latched at the rising edge.
$\overline{2CH}$	I	This pin is used for echo playback and for simultaneous playback of two phrase/words. Input of only the $\overline{2CH}$ pulse in 1-channel operation starts the echo playback mode. The echo delay time can be changed by the timing of the $\overline{2CH}$ pulse input. Input of the $\overline{ST}$ pulse when $\overline{2CH}$ is "L" causes 2-channel playback.
SG	O	A 1µF capactior is connected between this pin and the GND pin to stabilize the voltage. By connecting the capacitor to this pin, the SN ratio of the internal LPF is improved.
AOUT	O	Analog voice output pin that passed the LPF.
$\overline{BUSY}$/NAR (Next Address Request)	O	Can select either the NAR signal output or the $\overline{BUSY}$ signal output. When selecting $\overline{BUSY}$, this pin maintains a "L" level during playback. When selecting NAR, the $\overline{ST}$ input in channel 1 at the "H" level becomes valid.
$\overline{RESET}$	I	The LSI enters the standby state upon a "L" input. At this time, the oscillation stops, the LPF output (AOUT) is set to GND level and the LSI is reset. This LSI has a built-in power-on-reset circuit but for normal operation with power-on-reset, apply the power within 1 mS up to VDD. If the power cannot be applied within 1 mS, input the $\overline{RESET}$ pulse during power-on.
GND	—	Ground pin
VDD	—	Power supply pin
OSC1	I	This pin is connected to a crystal oscillator when choosing crystal oscillation as an option. This pin becomes a RC connection pin when choosing RC oscillation. OSC1 is also suitable for an external clock input.

Pin Name	I/O	Function
OSC2	O	This pin is connected to a crystal oscillator when choosing crystal oscillation as an option. This pin becomes a RC connection pin when choosing RC oscillation. This pin outputs a "L" level in the standby mode. Leave this pin open when using an external clock.
OSC3/$\overline{CS}$	I/O	This pin becomes a RC connection pin when choosing RC oscillation and outputs the "H" level in the standby mode. This pin becomes a $\overline{CS}$(CHIP SELECT) pin when choosing the crystal oscillation and the ST input is fetched internally. Leave $\overline{CS}$ to "L" when not needed.
$\overline{ST}$	I	Speech synthesis playback is started with the falling edge of $\overline{ST}$ and addresses I0~I6 are fetched when $\overline{ST}$ is "L" level. The addresses are latched internally at the rising edge of $\overline{ST}$. Input the address of channel 1 when NAR is "H". When playing back in channel 2, it is possible to change the sound volume of channel 2 by the number of $\overline{ST}$ pulses while $\overline{2CH}$ is "L". When selecting the SW input interface, repeated playback can be done by fixing $\overline{ST}$ to the "L" level.
V_{pp}	—	This pin is a programming power supply pin for the built-in OTP. When playing back, set V_{pp}=VDD or leave this pin open.
$\overline{PGM}$	I	An interface pin to the dedicated writer, AR76-201 with OTP adapter or AR76-202. Set this pin to "L" or leave the pin open when playing back. This pin has a built-in pull-down resistance.

FUNCTION DESCRIPTION

1. Voice code Selection

User selectable words (phrases) are maximum 111-word/phrases. The setting of I0~I6 is as follows:

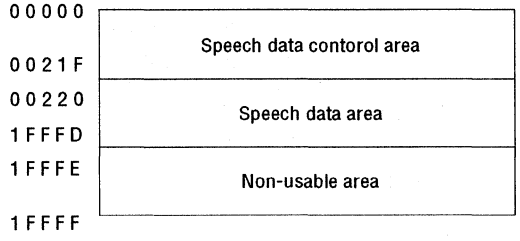
Table 1 List of User Selected Words

I0~I6	Code explanation
0000000	STOP code
0000001 ↕ 1101111	User selectable code (111-word)
1110000 ↕ 1110111	BEEP tone code
1111000 ↕ 1111111	Test codes (do not use)

2. Non-Usable Rrange of Built-in ROM

The last two bytes of the built-in ROM are in the non-usable range. Do not use these bytes when analyzing speech.

ROM Configuration



3. CPU Interface and SW Input Interface

Select either the CPU interface of the SW input interface as an option for the input interface.

3-1 CPU Interface

If the CPU interface is selected, the $\overline{ST}$ pulse becomes valid when the NAR pin is "H". User selected words are then fetched internally and vocalized. This interface is effective for playback of several words continuously. Please note that when the $\overline{ST}$ pulse is kept at the "L" level for longer than 800µs, one word is played twice (at 8kHz sampling).

When the $\overline{ST}$ pulse width is between 350µs and 800µs, a single word is played once or twice. However, when the $\overline{ST}$ pulse is input from the standby state, a single word is played only once if within 80ms.

When a $\overline{ST}$ pulse width of longer than 350µs (master frequency is 64kHz) is input and the $\overline{BUSY}$ option has been selected, make sure the $\overline{ST}$ pulse is within 800µs after the rise of $\overline{BUSY}$ pin.

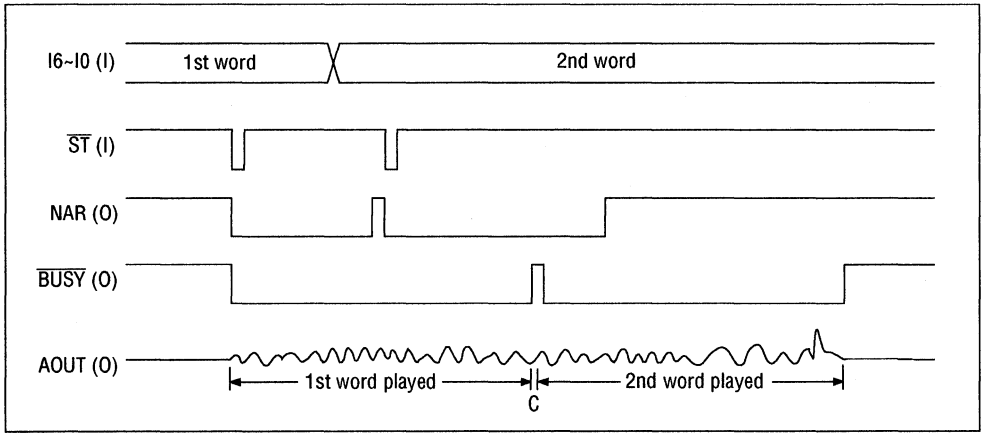


Figure 1 Timing of CPU Interface ($\overline{ST}$≦ 350µs)

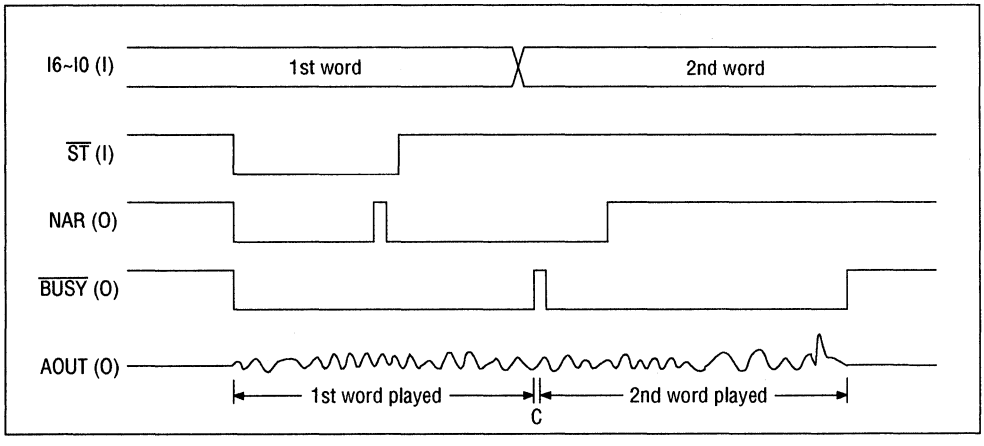


Figure 2 Timing of CPU Interface (800µs < $\overline{ST}$)

3-2 SW Input Interface

If the SW input interface is selected, the specified word is played repeatedly when $\overline{ST}$ is "L" at the end of play of the specified word and is finished when it is "H"level.

For example, when this LSI is operated using a push switch, the same word is played repeatedly as long as the switch is pressed and when the switch is released, playback stops when the currently playing word is finished.

When playing different words continuously, change the code of I6~I0 and maintain $\overline{ST}$ at the "L" level before the playback is completed.

However, note that the playing is interrupted if the input level of I6~I0 becomes "L" instantly when switching the address.

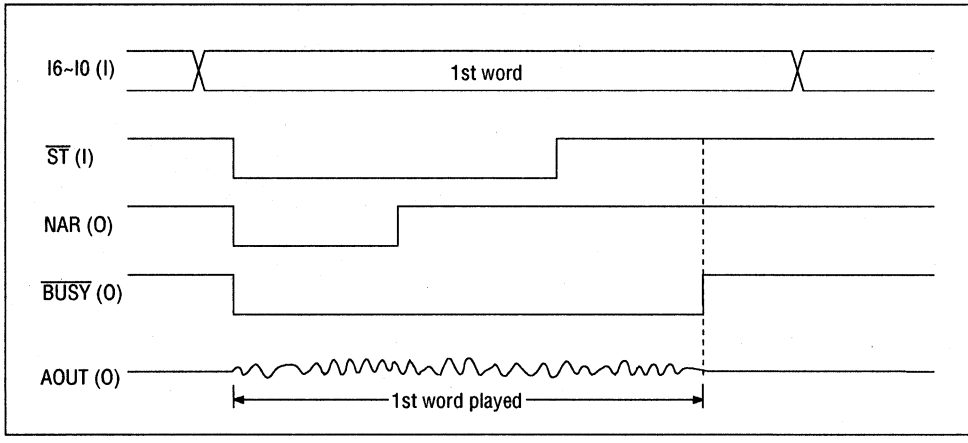


Figure 3 Timing of SW Input Interface (playing one word)

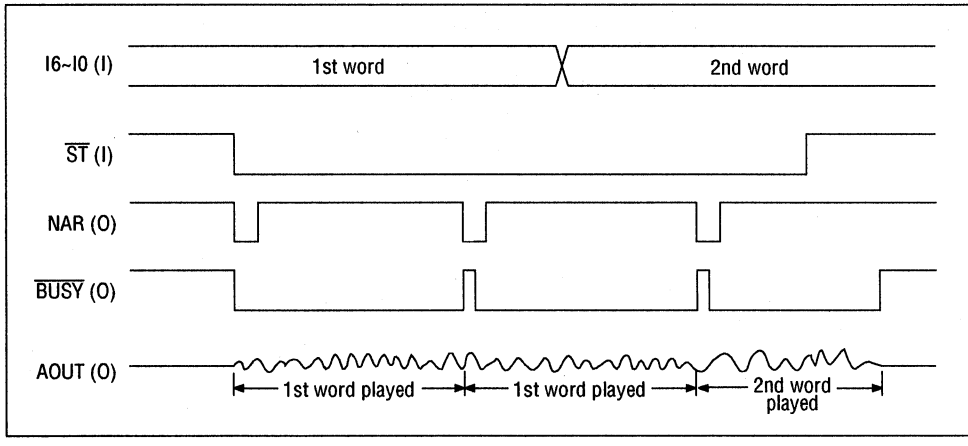


Figure 4 Timing of SW Input Interface (repeated play)

In SW input interface, playback of the 1st and 2nd channels simultaneously is not possible.

Neither 2-channel mixing nor echo playback is possible in this interface.

4. BEEP Tone Generation

Since this LSI has an on-chip circuit to generate BEEP tones, the BEEP tones are selected using I6~I0. Depending on the word code, the frequency and duration can be changed. The amplitude is approximately 1/4 VDD.

The NAR/$\overline{\text{BUSY}}$ pin outputs a "L" level during BEEP tone play regardless of either NAR or $\overline{\text{BUSY}}$ is selected as the option. Figure 5 shows such timing. Neither the STOP code (explained later) nor 2 -channel playback is valid during the playback of BEEP tone. The following table shows the relationship between the BEEP tones and addresses when the oscillation frequency is 64kHz.

Table 3 Relationship between BEEP Tones and Addresses

I6	I5	I4	I3	I2	I1	I0	BEEP tone frequency	Generating duration (sec)
1	1	1	0	0	0	0	2.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500
				1	0	0	1.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500

When the code for a BEEP tone is input while playing either the 1st channel or the 2nd channel, the BEEP tone is generated after the completion of play. The reverse case also holds true.

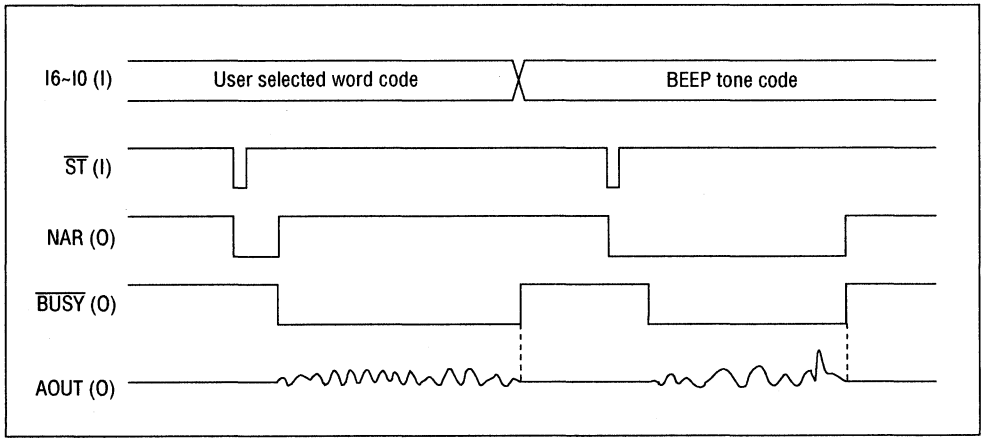


Figure 5 Timing at BEEP Tone Generation

5. Stop Code

Speech playing is finished when the $\overline{ST}$ pulse is input by setting I6~I0 to "0000000" during play. The DA converter becomes 1/2 VDD.

The input method of the $\overline{ST}$ pulse is subject to the AC characteristics when the NAR output is "H"level. When the NAR output is at the "L" level, the STOP code is valid by setting the $\overline{ST}$ pulse to the "L" level longer than 1 msec (f_{osc}=64kHz) or by the timing shown in Figure 6.

The STOP code is not valid during the generation of BEEP tone. When the STOP code is input, only playback is stopped while the oscillation and the analog circuitry are still operating. When the $\overline{RESET}$ pulse is input, all operations are halted.

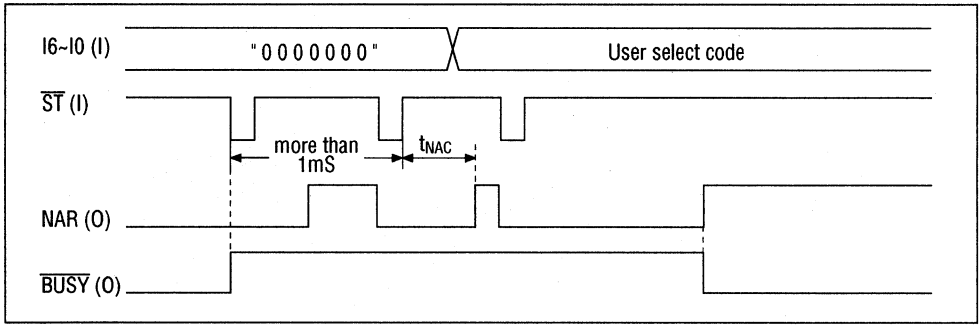


Figure 6 Example of STOP Code Input Timing

6. Sampling Frequencies

Sampling frequencies can be specified for each word in the speech data of the built-in ROM. When the 1st and the 2nd channels are simultaneously played back, the sampling frequency of the 1st channel has priority.

Three types of sampling frequencies can be selected during speech data analysis. The relationship between the master frequency, fosc, and the sampling frequency, fsam, is as follows:

Selection 1	$fsam_1 = fosc/8$
Selection 2	$fsam_2 = fosc/10$
Selection 3	$fsam_3 = fosc/16$

7. Echo Playback and Channel 2 Playback

By using the $\overline{2CH}$ input, echo or 2-channel playback is possible. Because both echo and 2-channel playback use the $\overline{2CH}$ pin, switch between modes by returning the LSI to the standby state.

This function is not available in the SW input interface or during generation of BEEP tones.

7-1 Echo Playback

Echo playback is performed by combining a speech waveform of the 1st channel with a delayed speech waveform with-6 dB attenuation (half the amplitude of the channel 1 speech waveform).

The echo delay time is the time until the $\overline{2CH}$ pulse is input from the start of play of channel 1.

However, when starting this operation from the standby state, pop noise suppression time is not counted as delay time.

In echo playback, echo is applied to all the words during continuous play of channel 1 (continuous play means playback of the next word during playback.)

7-2 2-Channel Mixing Playback

Using 2-channel mixing playback, a different word can be played during the play of channel 1. This has a wide range of application such as BGM (back ground music) and combinations of instruments. Speech data on channel 2 can remain the same while the sound volume may be changed to 1, 1/2 and 1/4 according to channel 1. The change in sound volume is determined by the number of $\overline{ST}$ pulses when starting the 2nd channel.

Once 2-channel mixing is set, it is maintained until the standby state or until channel 2 is reset. Because of this, restart can be accomplished by the input of the $\overline{2CH}$ pulse only.

Table 4 Number of $\overline{ST}$ Pulses and Attenuation

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation (100% of speech data)
2	-6dB attenuation (1/2 of speech data)
3	-12dB attenuation (1/4 of speech data)

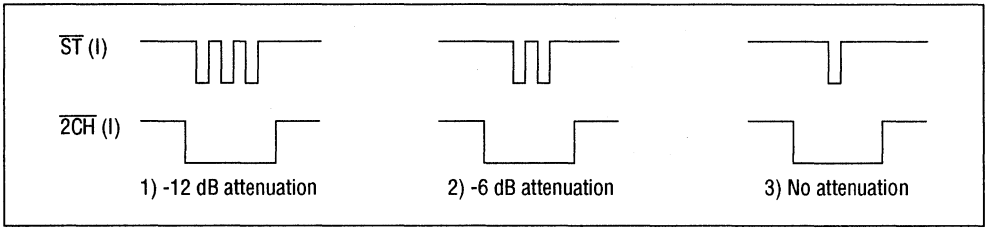


Figure 7 Input Timing of 2-Channel Mixing

8. Standby Transition

The LSI changes to the standby state and halts all operations unless another word is played within 3 seconds of the completion of playback of a single word. For this reason, it takes approximately 100 mS before the next playback is started as the LSI needs to activate the pop noise suppression circuitry.

The standby state can be obtained by inputting the $\overline{RESET}$ pulse, but if the $\overline{RESET}$ pulse is input, Popnoise is generated so that the output level from AOUT becomes GND level instantly.

9. Voice Output

The voice is output at the AOUT pin through the built-in low-pass filter.

9-1 Output Waveform of DA Converter

The output amplitude from the DA converter is maximum 4095/4096 × VDD of a square wave that synchronizes with a sampling frequency.

Table 5 shows the output level from the DA converter.

Table 5 Output Level from DA Converter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	$\frac{1}{4}$VDD	$\frac{1}{2}$VDD	approx. $\frac{3}{4}$VDD	V
2-channel mixing	0.0	$\frac{1}{2}$VDD	VDD	V
BEEP tone playback	approx. $\frac{3}{8}$VDD	$\frac{1}{2}$VDD	approx. $\frac{3}{8}$VDD	V

9-2 Low-passFilter Output

Since the low-pass filter is composed of switch capacitors, the cut-off frequency varies proportional to the master clock frequency.

When the sampling freq. (fsam) is 1/8 and 1/10 of the master clock frequency, the cut-off frequency, fcut is fcut=3/64 fosc and is fcut=3/128 when fsam is 1/16. Table6 shows the relationship between the sampling frequencies and the cut-off frequencies.

Table 6 Cut-off Frequency of Low-pass Filter

Sampling frequency (fsam)	Master clock frequency (fosc)	Cut-off frequency (fcut)
4.0 kHz	64 kHz	approx 1.5 kHz
6.4 kHz	64 kHz	approx 3.0 kHz
8.0 kHz	64 kHz	approx 3.0 kHz
12.8 kHz	128 kHz	approx 6.0 kHz
16.0 kHz	128 kHz	approx 6.0 kHz

The low-pass filter characteristics when the sampling frequency is 8kHz are shown in Figure 8.

Table 7 shows the output level from AOUT when selecting the low-pass filter option.

Table 7 Output Level of Low-pass Filter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	approx. $\frac{1}{4}$VDD	approx. $\frac{1}{2}$VDD	approx. $\frac{3}{4}$VDD	V
2-channel mixing	approx. 0.7	approx. $\frac{1}{2}$VDD	approx. VDD–0.7	V
BEEP tone playback	approx. $\frac{3}{8}$VDD	approx. $\frac{1}{2}$VDD	approx. $\frac{3}{8}$VDD	V

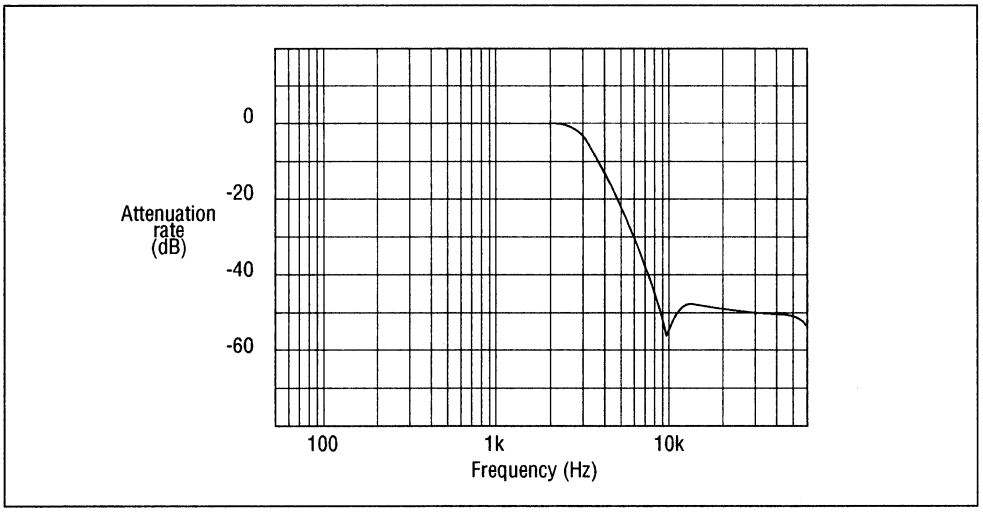


Figure 8 Low-pass Filter Characteristics (fsam=8kHz)

9-3 Pop Noise of Low-pass Filter Output

Although this LSI has a built-in pop noise suppression circuit, the voltage of the circled portion in Figure 9 may be changed abruptly by approximately 0.7V when selecting the low-pass filter output and may generate a "pop" sound.

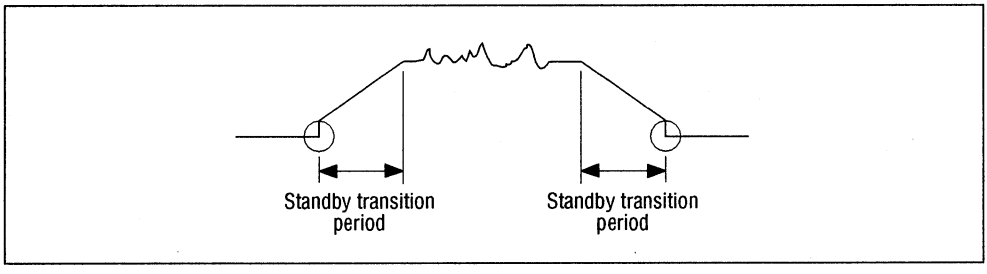


Figure 9 Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the "pop" sound can be reduced. Figure 10 shows the circuit.

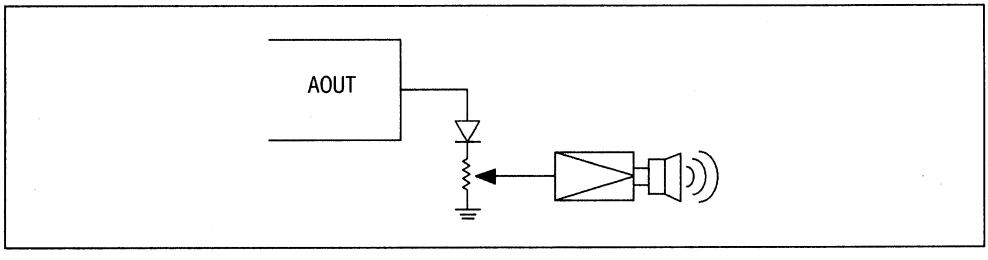


Figure 10 Pop Noise Suppression Circuit

10. RC Oscillation

The external circuit diagram for RC oscillation is shown below:

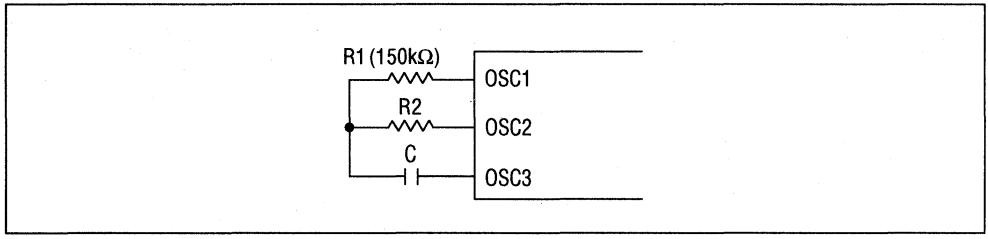


Figure 11 RC Oscillation Connection Circuit

10-1 Determination of RC Constant

The RC oscillation frequency characteristics are shown in Figure 12. If fosc is set to 64 kHz, choose the appropriate values for C and R2 using the following as a reference:

C=100 pF, R1=150KΩ, R2=50KΩ.

10-2 Fluctuation of RC Oscillation Frequencies

When choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R2 as well as the process variations of the LSI.

When using a 50kΩ R2 the error due to process variations of the LSI is maximum ±4% so that the fluctuation of the RC oscillation frequency when using a capacitance (C) of ±1% accuracy and a resistance (R2) of ±2% accuracy is maximum ±7% approximately.

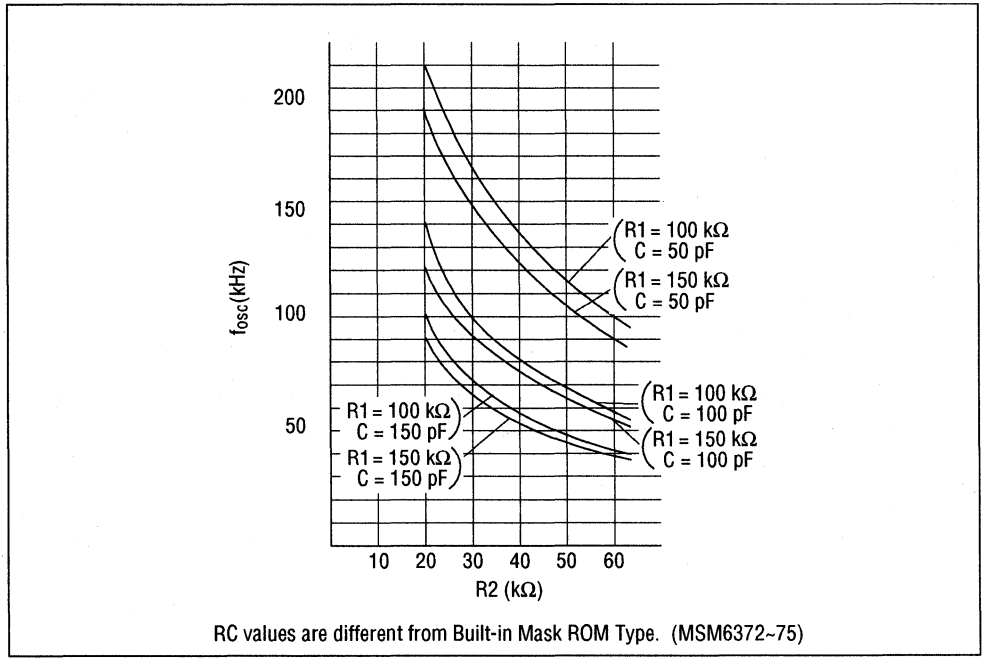


Figure 12 RC Oscillation Frequency

11. Crystal Oscillation

Figure 13 shows an external circuit using a crystal oscillator, KF-38S4-13PO102 (64kHz), made by Kyocera.

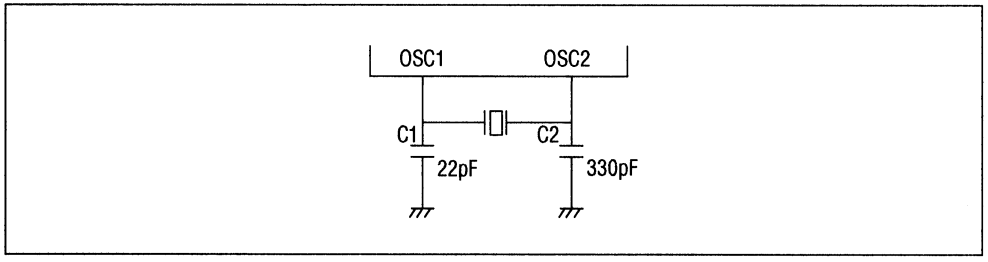


Figure 13 Circuit Diagram of Crystal Oscillator Connection

12. Connection with MSC1191/1192

When using an MSC1191 and an MSC1192, connect the STBY pin to the OSC3/$\overline{CS}$ pin and the OSC2 pin, respectively. When connecting with an MSC1191/1192, set C and R after mounting it to the board as the oscillation characteristics may change.

CODE OPTION

There are 13 types of options for the MSM6375 family as shown below. The MSM63P74 is corresponds to 4 options (option B, E, G, L) in this table (example: type name MSM63P74-02).

MSM6375 Family						MSM63P74
Option name	**RC/XT**	**BUSY/NAR**	**DA/LPF**	**Standby**	**CPU/SW**	**Code option**
Option A	RC	NAR	LPF	None	CPU	—
Option B	**RC**	**BUSY**	**LPF**	**Available**	**SW**	**02**
Option C	XT	NAR	LPF	None	CPU	—
Option D	RC	BUSY	LPF	None	SW	—
Option E	**XT**	**NAR**	**LPF**	**Available**	**CPU**	**05**
Option F	XT	NAR	DA	None	CPU	—
Option G	**RC**	**NAR**	**LPF**	**Available**	**CPU**	**07**
Option H	RC	BUSY	LPF	None	CPU	—
Option I	RC	BUSY	DA	Available	CPU	—
Option J	RC	NAR	DA	Available	CPU	—
Option K	XT	BUSY	LPF	None	CPU	—
Option L	**RC**	**BUSY**	**LPF**	**Available**	**CPU**	**12**
Option M	XT	NAR	DA	Available	CPU	—

EXAMPLE OF APPLICATION CIRCUITS

As the MSM63P74 is functionally compatible with the MSM6375 family, refer to the users manual of MSM6375 family for application circuits.

OKI Semiconductor

MSM6376

ADPCM SPEECH SYNTHESIZER WITH EXTERNAL ROM

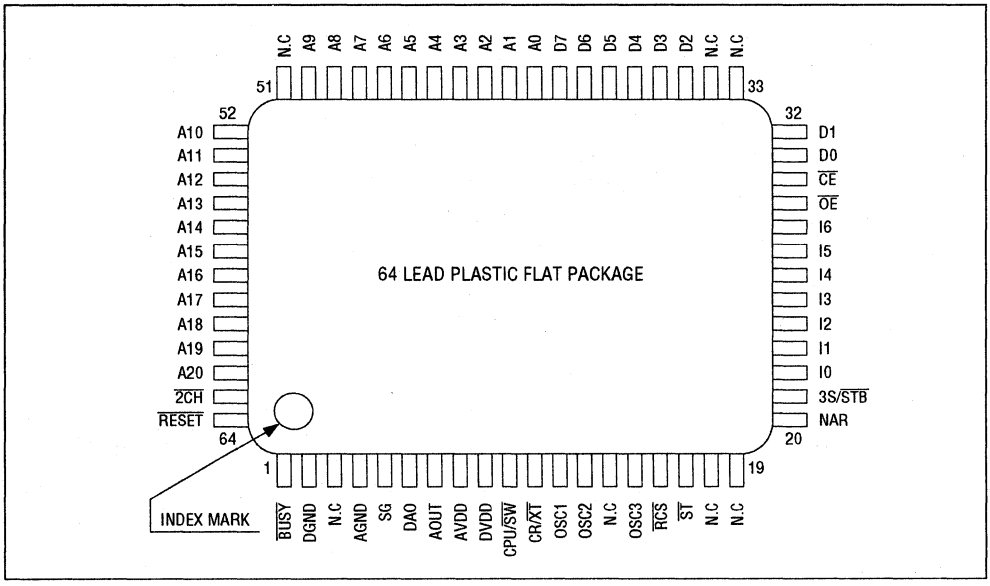
GENERAL DESCRIPTION

MSM6376 is a two-channel mixing ADPCM speech synthesizer LSI using up to 16 M-bit external speech data storage, such as ROM, and EPROM. Since it has a built-in 12-bit DA converter and low pass filter, a speech data output system can easily be configured by connecting an external power amplifier and speaker. MSM6376 is best suited to the evaluation of MSM6372, MSM6373, MSM6374, and MSM6375, which are used as speech synthesizer LSIs with built in ROM, because the MSM6376 has the same circuit configuration as those LSIs.

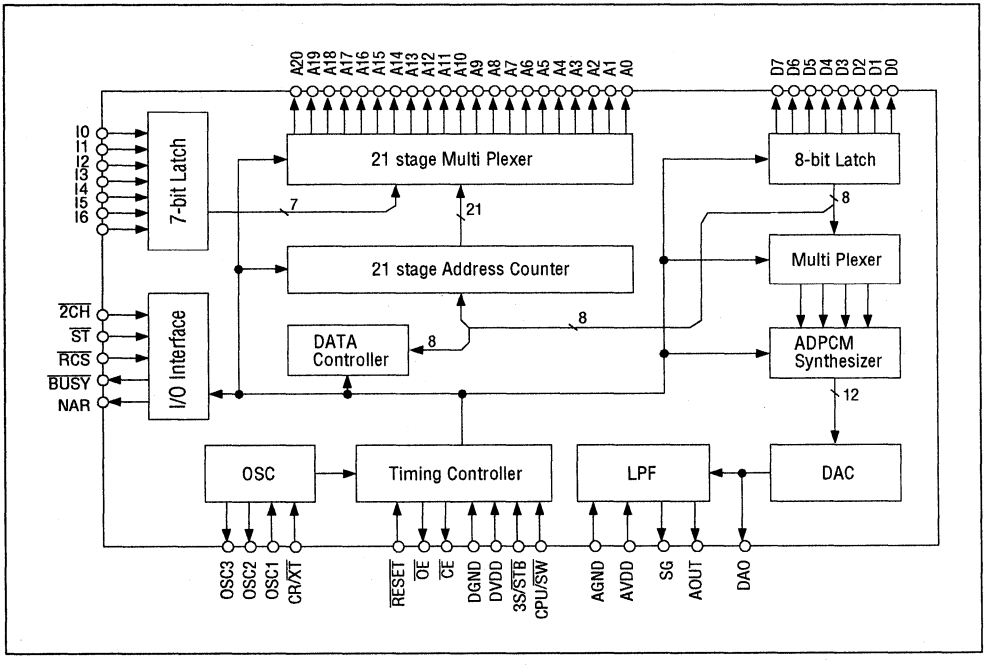
FEATURES

- External memory capacity 16 M-bit ROM
- 4-bit straight ADPCM method
- Echo reproduction and simultaneous output of two audible tones (sound volume variation for one tone in three stages)
- Output of either of two built-in BEEP tones (1 kHz and 2 kHz) by designation code (when oscillation is 64 kHz)
- Sampling frequency 4.0, 6.4 and 8.0 kHz (at oscillation of 64 kHz) up to 32 kHz is possible.(at selected DA output)
- Maximum speech period of 10.9 minutes (at sampling frequency of 6.4 kHz) with 16 M-bit ROM
- Maximum number of words:
  111-word
- Built-in 12-bit D/A converter of class A voltage type (with built-in pop noise suppression circuit)
- Built-in LPF with attenuation factor of -24 dB/oct
  Note) fcut=cutoff frequency
- Standby function to stop oscillation and all functions during the standby state
- Oscillation selectable between RC oscillation and crystal oscillation
- Master oscillation frequency:
  40 to 140 kHz (LPF output)
  40 to 256 kHz (DAC output)
- Supply voltage:
  4.5 to 5.5V
- 64-pin-V1 plastic QFP
  (QFP64-P-1420-V1K)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

(DGND = AGND = 0V)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}		−0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Ranges

(DGND = AGND = 0V)

Parameter	Symbol	Conditions	Range	Unit
Power supply voltage	V_{DD}	–	+4.5 ~ +5.5	V
Operating temperature	T_{op}	–	−40 ~ +85	°C
Master oscillation frequency	f_{OSC1}	LPF output	40 ~ 140	kHz
Master oscillation frequency	f_{OSC2}	DAC output	40 ~ 256	kHz
DAO output level	V_{OD}	No load	0 ~ V_{DD}	V

• DC Characteristics

(DVDD = AVDD = 4.5~5.5V, DGND = AGND = 0V, Ta=−40~85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.84×VDD	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.16×VDD	V
"H" output voltage	V_{OH}	I_{OH} = −40 µA	VDD-0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" input current	I_{IH}	V_{IH} = V_{DD}	—	—	10	µA
"L" input current	I_{IL}	V_{IL} = 0V	−10	—	—	µA
Output leak current	I_{LO}	0 ≦ V_{OUT} ≦ V_{DD}	−10	—	10	µA
Operating current consumption	I_{DD}	—	—	4	10	mA
Standby current consumption	I_{DS}	—	—	—	10	µA
Relative precision of DA output	$\|V_{DAE}\|$	no load	—	—	40	mV
DA output impedance	R_{DAO}	—	15	25	35	kΩ
LPF load impedance	R_{AOUT}	—	50	—	—	kΩ

• AC Characteristics (VDD = 5V, Ta = –40 ~ 85°C, f_{OSC} = 64 kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µS
$\overline{ST}$ input pulse width (Note 1)	$t_{W(\overline{ST})}$	CPU interface	0.35	–	350	µS
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µS
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µS
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µS
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µS
Data set time	t_{DW}	—	10	–	–	µS
Data hold time	t_{WD}	—	10	–	–	µS
$\overline{RCS}$ setup time	t_{CS}	—	10	–	–	µS
$\overline{RCS}$ hold time	t_{BC}	—	10	–	–	µS
Selectable sampling frequency	$fsam_1$	$f_{(osc1)}/8$	–	8.0	–	kHz
	$fsam_2$	$f_{(osc1)}/10$	–	6.4	–	kHz
	$fsam_3$	$f_{(osc1)}/16$	–	4.0	–	kHz
NAR output time (1) (Note 4)	t_{SNS}		–	–	10	µS
NAR output time (2)	t_{NN}	—	–	–	500	nS
NAR output time (3) (Note 2)	t_{NAA}	At fsam=8 kHz	350	375	400	µS
NAR output time (4) (Note 2)	t_{NAB}	At fsam=8 kHz	350	375	400	µS
NAR output time (5) (Note 2)	t_{NAC}	At fsam=8 kHz	350	–	550	µS
$\overline{BUSY}$ output time (1) (Note 4)	t_{SBS}	—	–	–	10	µS
$\overline{BUSY}$ output time (2) (Note 2)	t_{BN}	At fsam = 8 kHz	350	375	400	µS
$\overline{BUSY}$ output time (3) (Note 5)	t_{BF}	At master frequency=64 kHz	–	–	64	mS
$\overline{BUSY}$ output time (4) (Note 2)	t_{BA}	At fsam=8 kHz	350	375	400	µS
D/A converter transition time (Note 3)	t_{DAR}, t_{DAF}	At master frequency=64 kHz	60	64	68	mS
LPF stabilizing time (Note 4)	t_L	At master frequency=64 kHz	12	16	20	mS
Standby transition time (Note 3) (at end of speech output)	t_{STB}	At master frequency=64 kHz	2.9	3.0	3.1	S
$\overline{ST}$ - $\overline{2CH}$ pulse interval	t_{S2CH}	At master frequency=64 kHz	1.0	–	–	mS
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µS

Note 1: The MAX value is proportional to fsam.
Note 2: The duration is proportional to fsam.
Note 3: The duration is proportional to f_{OSC}.
Note 4: Applicable at the start of oscillation.
Note 5: When playback occurs during the standby transition period (t_{DAF}).

- **AC Characteristics**
  (VDD = 5V, Ta = –40 ~ 85°C, f_{OSC1} = 40 ~140 kHz, f_{OSC2} = 40 ~ 256kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{\text{RESET}}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µS
$\overline{\text{ST}}$ input pulse width	$t_{W(\overline{ST})}$	CPU interface	0.35	–	a	µS
$\overline{\text{2CH}}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µS
$\overline{\text{ST}}$–$\overline{\text{ST}}$ pulse interval	t_{SS}	—	0.35	–	–	µS
$\overline{\text{2CH}}$ setup time	t_{CHS}	—	0.35	–	–	µS
$\overline{\text{2CH}}$ hold time	t_{SCH}	—	0.35	–	–	µS
Data set time	t_{DW}	—	10	–	–	µS
Data hold time	t_{WD}	—	10	–	–	µS
$\overline{\text{RCS}}$ setup time	t_{CS}	—	10	–	–	µS
$\overline{\text{RCS}}$ hold time	t_{BC}	—	10	–	–	µS
Selectable sampling frequency	$fsam_1$	—	–	$f_{osc}/8$	–	kHz
	$fsam_2$	—	–	$f_{osc}/10$	–	kHz
	$fsam_3$	—	–	$f_{osc}/16$	–	kHz
NAR output time (1) (Note 1)	t_{SNS}	—	–	–	10	µS
NAR output time (2)	t_{NN}	—	–	–	500	nS
NAR output time (3)	t_{NAA}	—	a	b	c	µS
NAR output time (4)	t_{NAB}	—	a	b	c	µS
NAR output time (5)	t_{NAC}	—	a	–	d	µS
$\overline{\text{BUSY}}$ output time (1) (Note 1)	t_{SBS}	—	–	–	10	µS
$\overline{\text{BUSY}}$ output time (2)	t_{BN}	—	a	b	c	µS
$\overline{\text{BUSY}}$ output time (3) (Notes 2)	t_{BF}	—	–	–	64	mS
$\overline{\text{BUSY}}$ output time (4)	t_{BA}	—	a	b	c	µS
D/A converter transition time	t_{DAR}, t_{DAF}	—	e-4	e	e+4	mS
LPF stabilizing time (Note 1)	t_L	—	f-4	f	f+4	mS
Standby transition time (at end of speech output)	t_{STB}	—	g-0.1	g	g+0.1	S
$\overline{\text{ST}}$–$\overline{\text{2CH}}$ pulse interval	t_{S2CH}	—	h	–	–	mS
$\overline{\text{ST}}$ input wait time	t_{NS}	—	10	–	–	µS

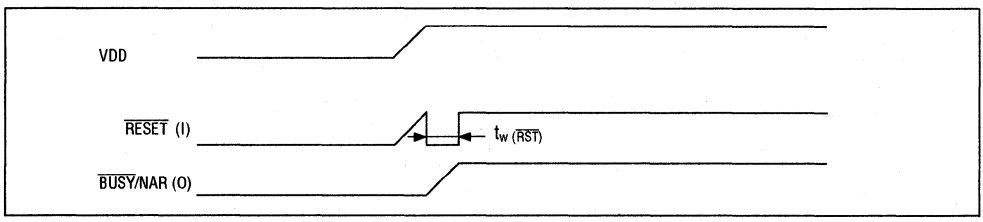
$$a = 350 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad b = 375 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad c = 400 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)} \quad d = 550 \times \frac{8\ (kHz)}{f_{sam}\ (kHz)}$$

$$e = 64 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad f = 16 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad g = 3.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad h = 1.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)}$$

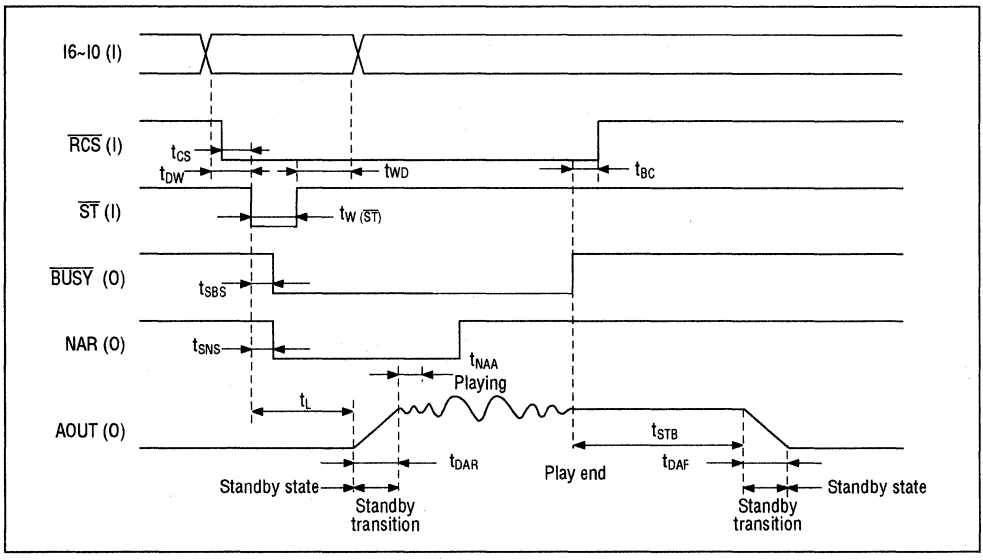
Note 1: Applicable at the start of oscillation.
Note 2: When playback occurs during the standby transition period (t_{DAF}).

TIMING DIAGRAMS

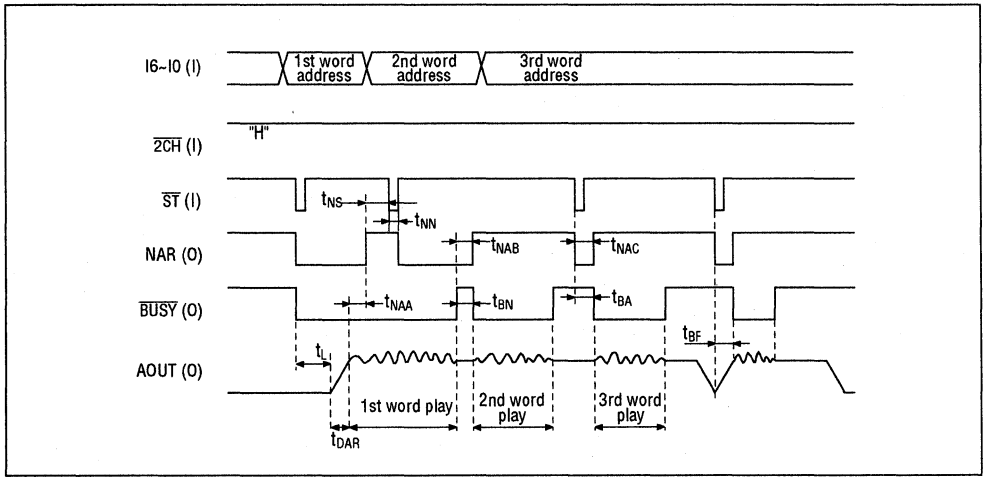
1. At power-on



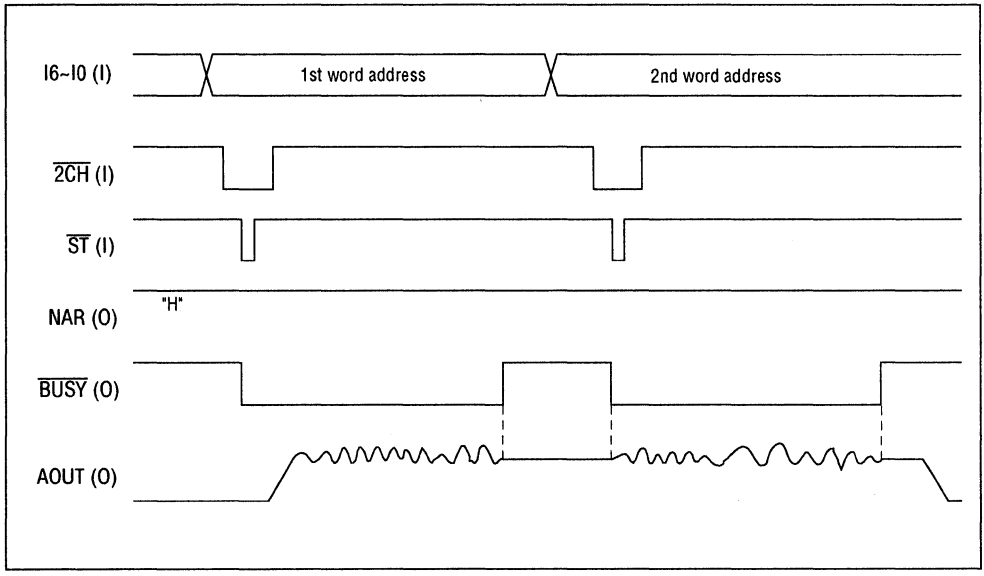
2. At LSI startup and in standby state



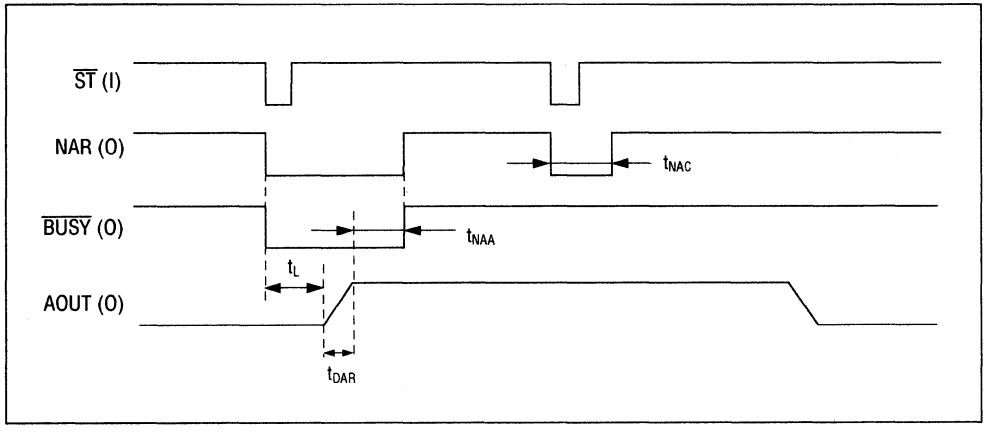
3. Operation in channel 1 only (CPU input interface)



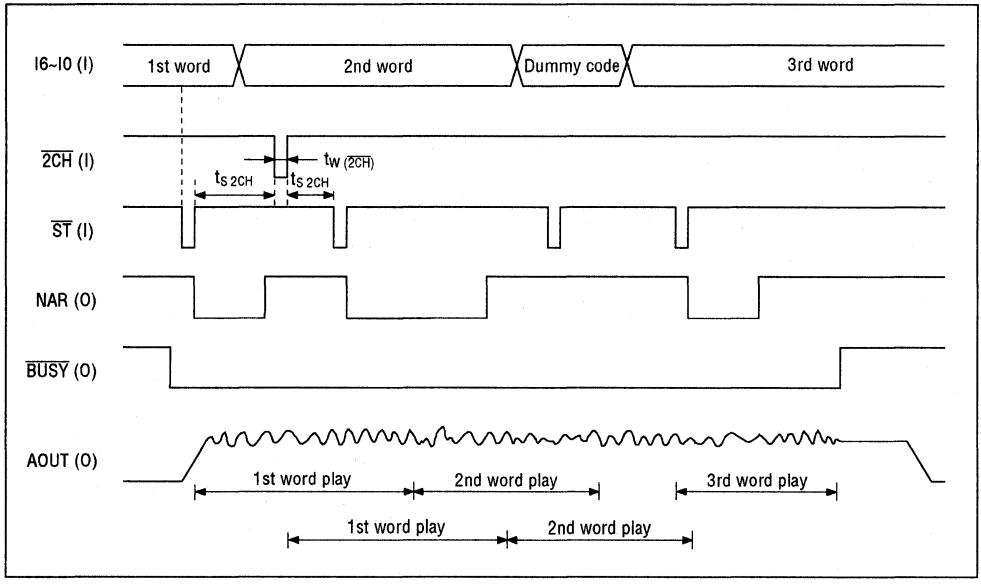
4. Operation in Channel 2 Only (CPU input interface)



5. Operation in Address Designation with noVoice



6. Timing Diagram of Echo Playback in Channel 1



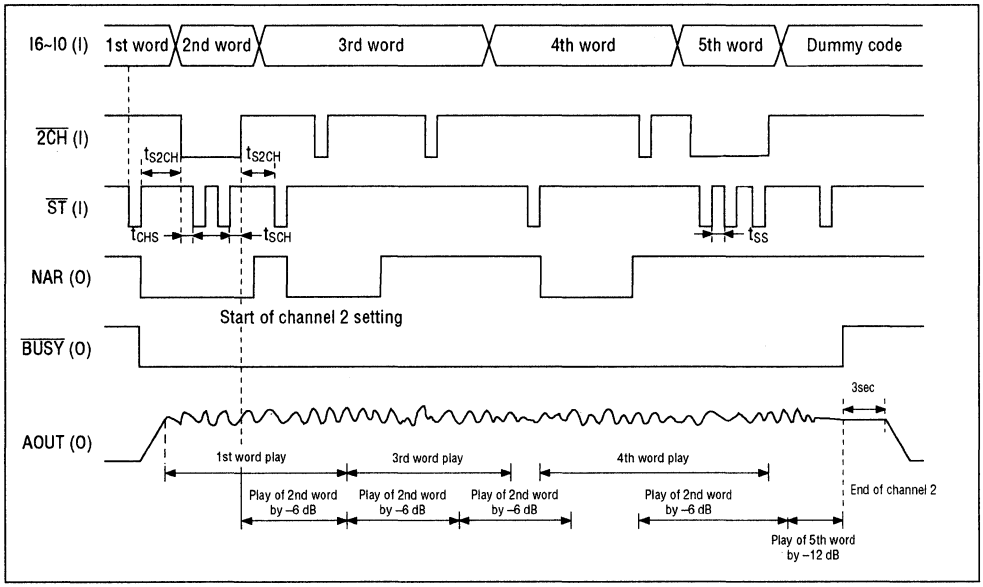
1. Input of the $\overline{2CH}$ pulse without lowering $\overline{ST}$ starts echo playback. Echo playback is canceled unless play is continuous.

2. At echo playback, the waveform is a combination of the playback of channel 1 by the $\overline{ST}$ pulse and a -6dB playback of channel 2 by the $\overline{2CH}$ pulse.

3. In continuous play, the echo is applied to the next word (continuous play means playback of another word during a single word vocalization.)

4. Input unused code as a dummy code from the user selectable code at the end of echo playback. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of playback when the standby option is selected.

7. Timing Diagram of Simultaneous Playback in Channel 1 and Channel 2



1. Channel 2 starts playing when the $\overline{ST}$ pulse is input and $\overline{2CH}$="L". The sounds volume can be changed by the number of the $\overline{ST}$ pulses using the table below.

2 Channel 2 plays a pre-set word each time the $\overline{2CH}$ pulse is input with the same sound volume until the LSI goes to the standby state or until channel 2 is reset.

3 Please input an unused code as a dummy code from the user selectable codes at the end of playback of channel 2. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of play when the standby option is selected.

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation
2	-6dB attenuation
3	-12dB attenuation

PIN FUNCTIONS

Pin Name	I/O	Function
I6~I0	I	Selects and enters a user-specified word corresponding to the vocalized word. The code when the level of the $\overline{ST}$ pulse goes low is read, and latched as the level rises.
A20~A0	O	These are the address terminals for the external connection of memory. The data is output when $\overline{RCS}$ is "L".
D7~D0	I	These are the pins to input the data from external memory. The data is input when $\overline{RCS}$ is "L". Insert a pull-down resistor of about 100 kΩ to pins D7~D0. If these pins are used at an open state, the leakage current of hundreds μA may flow to a power supply pin at a standby state.
$\overline{2CH}$	I	Reproduces echo, or reproduces two different tones simultaneously. If $\overline{2CH}$ pulse is entered during operation in channel 1, echo is reproduced. Delay time for the echo can be changed according to the time of input of $\overline{2CH}$ pulse. If $\overline{ST}$ pulse is entered when the level for CH2 is low, reproduction is performed in channel 2.
$\overline{ST}$	I	Activated at the fall of $\overline{ST}$. Data on I6 through I0 is read when their level is "L", and latched at the rise of $\overline{ST}$. Enter an address for channel 1 when the level of NAR is "H". For reproduction in channel 2, sound volume can be changed according to the number of $\overline{ST}$ pulses when the level of $\overline{2CH}$ is "L". In the case of SW input interface, synthesis is repeated while the level of $\overline{ST}$ is set to "L".
$\overline{RCS}$	I	When the level is "L", this pin enables $\overline{ST}$ pulse to be input and the address from A20~A0, $\overline{OE}$ and $\overline{CE}$ are output. When the level is "H", the address pins of A20~A0, and $\overline{CE}$ and $\overline{OE}$ become high impedance.
$\overline{BUSY}$	O	During playback, "L" level is output.
NAR	O	When the level is "H", the next channel address can be input.
CR/$\overline{XT}$	I	Selects RC oscillation or crystal oscillation. If the level of CR/$\overline{XT}$ is set to "H", OSC1, OSC2, and OSC3 work as RC oscillation pins; if the level of CR/$\overline{XT}$ is set to "L", OSC1 and OSC2 work as crystal oscillation pins, and a resistor with a resistance of about 2 MΩ is inserted between OSC1 and OSC2.

Pin Name	I/O	Function
OSC1	I	Crystal oscillation and RC oscillaito pins.
OSC2	O	To use them for crystal oscillation, leave the OSC3 pin open.
OSC3	O	If an external clock signal is to be used, it should be connected to the OSC1 pin with OSC2 and OSC3 left open.
CPU/$\overline{SW}$	I	Pin for selection between CPU interface and SW input interface. "H" level = CPU interface. "L" level = switch interface Note: If SW input interface is selected, echo reproduction, and 2-channel mixing reproduction cannot be performed.
3S/$\overline{STB}$	I	If the level of the 3S pins is "H", standby state is invoked three seconds after completion of speech synthesis. If the level of the 3S pins is "L", the output from the DA converter remains at 1/2 VDD after completion of speech synthesis.
$\overline{RESET}$	I	If the level of this pins is set to "L", the LSI is put in standby state. Upon $\overline{RESET}$, oscillation is stopped, the output from the DA converter is grounded, and put to the initial state. The M6376 has a built-in power-on reset circuit. To make the power-on resetting function reliably, raise the power supply within 1msec. If this is impossible to do, enter the $\overline{RESET}$ pulse when hte power is turned on.
$\overline{CE}$	O	A timing output pin that controls chip enable of external memory. The signal is output when the level of $\overline{RCS}$ is "L".
$\overline{OE}$	O	A timing output pin that controls reading from external memory. The signal is output when the level of $\overline{RCS}$ is "L".
DAO	O	A pin that outputs analog voice sent from the DA converter.
AOUT	O	A pin for output of analog voice sent from the LPF.
SG	O	A pin that improves SN ratio of LPF. To utilize the outpur from the LPF, connect a capacitor of about 1μF.
AVDD	—	An analog power supply pin.
AGND	—	An analog grounding pin.
DVDD	—	A digital power supply pin.
DGND	—	A digital grounding pin.

FUNCTION DESCRIPTION

1. Voice Code Selection

User selectable words (phrases) are maximum 111-word/phrases. The setting of I0-I6 is as follows:

Table 1 List of User Selected Words

I0~I6	Code explanation
0000000	STOP code
0000001 ↕ 1101111	User selectable codes (111-word)
1110000 ↕ 1110111	BEEP codes
1111000 ↕ 1111111	Test codes (do not use)

2. CPU Interface and Switch Input Interface

The CPU interface and the switch input interface can be selected by the CPU/$\overline{SW}$ pin. When the CPU pin is high, the CPU interface is on. When the CPU pin is low, the switch input interface is on.

2-1 CPU interface

If the CPU interface is selected, the $\overline{ST}$ pulse becomes valid when the NAR pin is "H". User selected words are then fetched internally and vocalized. This interface is effective for playback of several words continuously. Please note that when the $\overline{ST}$ pulse is

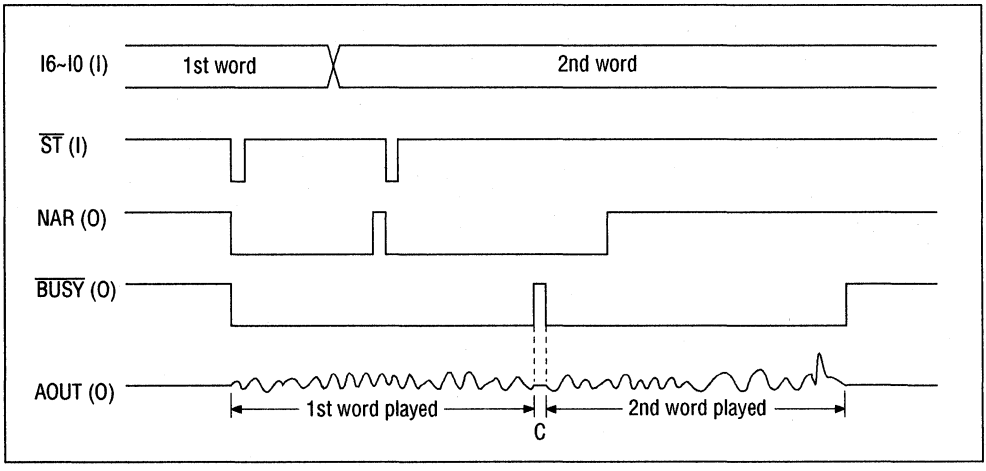


Figure 1 Timing of CPU Interface ($\overline{ST}$ ≤ 350 µS)

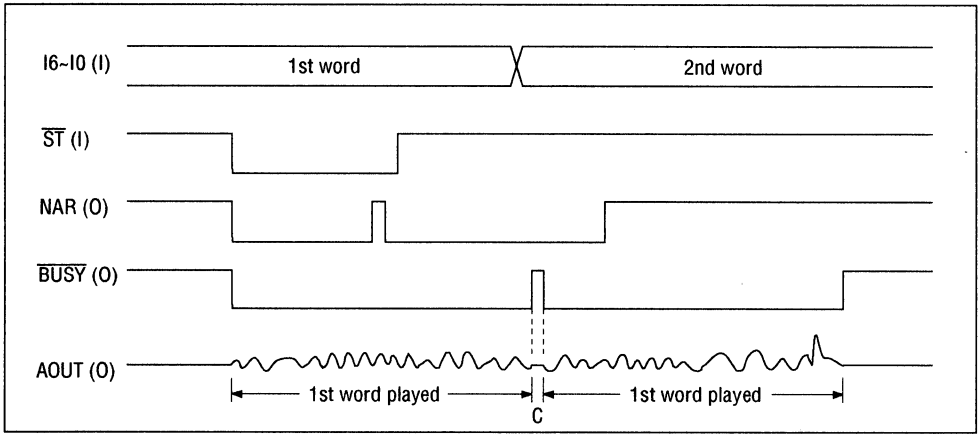


Figure 2 Timing of CPU Interface (ST > 800 µS)

kept at the "L" level for longer than 800µS, one word is played twice (at 8kHz sampling).

When the ST pulse width is between 350µS and 800µS, a single word is played once or twice. However, when the ST pulse is input from the standby state, a single word is played only once if within 80µS.

When a ST pulse width of longer than 350µS (master frequency is 64kHz) is input and the BUSY option has been selected, make sure the ST pulse is within 800 µS after the rise of BUSY pin.

2-2 SW input interface

If the SW input interface is selected, the specified word is played repeatedly when ST is "L"level at the end of play of the specified word and is finished when it is "H"level.

For example, when this LSI is operated using a push switch , the same word is played repeatedly as long as the switch is pressed

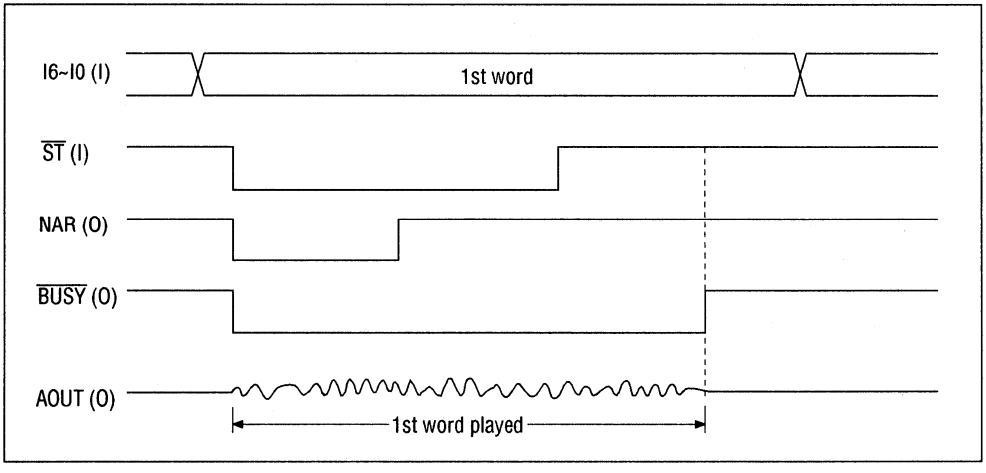


Figure 3 Timing of SW Input Interface (playing one word)

and when the switch is released, playback stops when the currently playing word is finished.

When playing different words continuously, change the code of I0-I6 and maintain $\overline{ST}$ at the "L" level before the play back is completed.

However, note that the playing interrupted if the input level of I6-I0 becomes "L" instantly when switching the address.

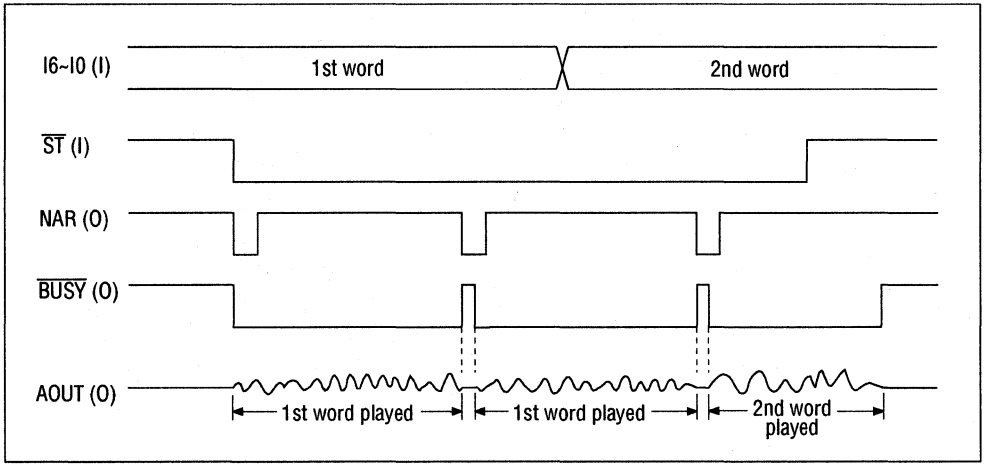


Figure 4 Timing of SW Input Interface (repeated play)

In SW input interface, playback of the 1st and 2nd channels simultaneously is not possible. Neither 2-channel mixing nor echo playback is possible in this interface.

3. BEEP Tone Generation

Since this LSI has an on-chip circuit to generate BEEP tones, the BEEP tones are selected using I6-I0. Depending on the word code, the frequency and duration can be changed. The amplitude is approximately 1/4 VDD.

The NAR/$\overline{\text{BUSY}}$ pin outputs a "L" level during BEEP tone play regardless of either NAR or $\overline{\text{BUSY}}$ is selected as the option. Figure 5 shows such timing.

Neither the STOP code (explained later) nor 2-channel playback is valid during the playback of BEEP tone, The following table shows the relationship between the BEEP tones and addresses when the oscillation frequency is 64kHz.

Table 2 Relationship between BEEP Tones and Addresses

I6	I5	I4	I3	I2	I1	I0	BEEP tone frequency	Generating duration (sec)
1	1	1	0	0	0	0	2.0kHz	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500
				1	0	0	1.0kHz	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500

When the code for BEEP tone is input while playing either the 1st channel or the 2nd channel, the BEEP tone is generated after the completion of play. The reverse case also holds true.

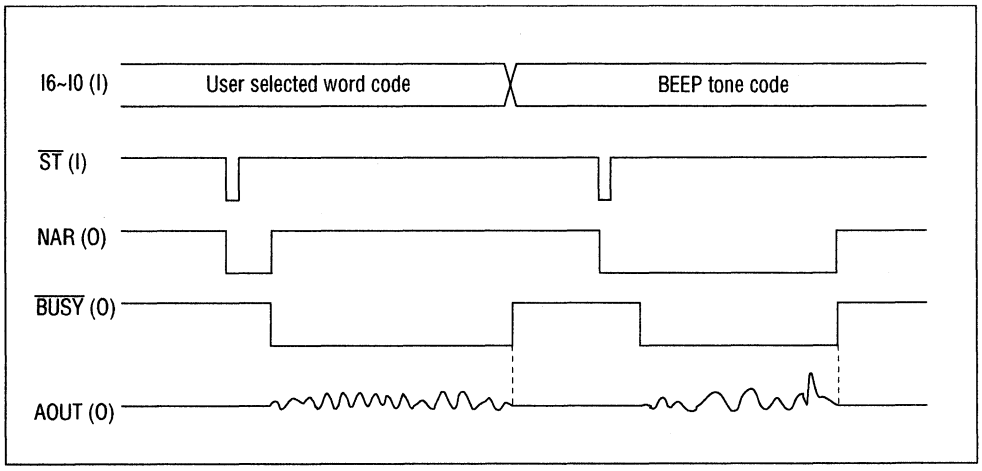


Figure 5 Timing at BEEP Tone Generation

4. Stop Code

Speech playing is finished when the $\overline{ST}$ pulse is input by setting I6-I0 to "0000000" during play. The DA converter becomes 1/2VDD.

The input method of the $\overline{ST}$ pulse is subject to the AC characteristics when the NAR output is "H"level. When the NAR output is at the "L" level, the STOP code is valid by setting the $\overline{ST}$ pulse to the "L" level longer than 1 msec (fOSC=64kHz) or by the timing shown in Figure 6.

The STOP code is not valid during the generation of BEEP tone. When the STOP code is input, only playback is stopped while the oscillation and the analog circuitry are still operating. When the $\overline{RESET}$ pulse is input, all operations are halted.

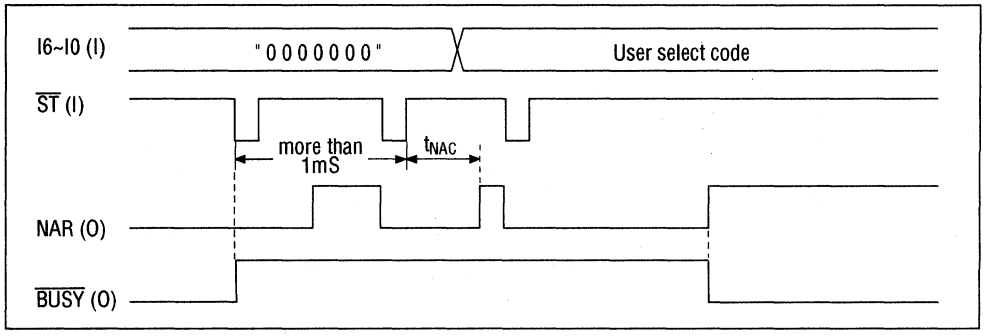


Figure 6 Example of STOP Code Input Timing

5. Sampling Frequencies

Sampling frequencies can be specified for each word in the speech data of the built-in ROM. When the 1st and the 2nd channels are simultaneously played back, the sampling frequency of the 1st channel has priority.

Three types of sampling frequencies can be selected during speech data analysis. The relationship between the master frequency, fosc, and the sampling frequency, fs, is as follows:

Selection 1	f_{sam1}=fose/8
Selection 2	f_{sam2}=fose/10
Selection 3	f_{sam3}=fose/16

6. Echo Playback and Channel 2 Playback

By using the $\overline{2CH}$ input, echo or 2-channel playback is possible. Because both echo and 2-channel playback use the $\overline{2CH}$ pin, switch between modes by returning the LSI to the standby state.

This function is not available in the SW input interface or during generation of BEEP tones.

6-1 Echo Playback

Echo playback is performed by combining a speech waveform of the 1st channel with a delayed speech waveform with -6 dB attenuation (half the amplitude of the channel 1 speech waveform).

The echo delay time is the time until the $\overline{2CH}$ pulse is input from the start of play of channel 1.

However, when starting this operation from the standby state, pop noise suppression time is not counted as delay time.

In echo playback, echo is applied to all the words during continuous play of channel 1 (continuous play means playback of the next word during playback.)

6-2 Channel Mixing Playback

Using 2-channel mixing playback, a different word can be played during the play of channel 1. This has a wide range of application such as BGM (back ground music) and combinations of instruments. Speech data on channel 2 can remain the same while the sound volume may be changed to 1, 1/2 and 1/4 according to channel 1. The change in sound volume is determined by the number of $\overline{ST}$ pulses when starting the 2nd channel.

Table 3 Number of $\overline{ST}$ Pulses and Attenuation

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation (100% of speech data)
2	-6dB attenuation (1/2 of speech data)
3	-12dB attenuation (1/4 of speech data)

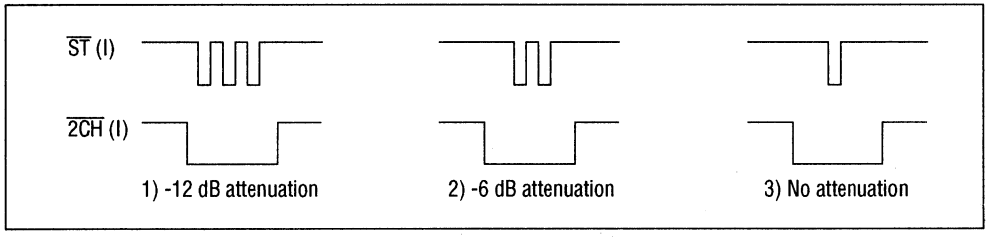


Figure 7 Input Timing of 2 Channel Mixing

Once 2-channel mixing is set, it is maintained until the standby state or until channel 2 is reset. Because of this, restart can be accomplished by the input of the $\overline{2CH}$ pulse only.

7. Standby Transition

When standby transition is enabled as an option, the LSI changes to the standby state and halts all operations unless another word is played within 3 seconds of the completion of playback of a single word. For this reason, it takes approximately 100mS before the next playback is started as the LSI needs to activate the pop noise suppression circuitry.

When standby transition is disabled as an option, the LSI does not go into the standby mode even when playback is completed. At this time, the output from AOUT is approximately 1/2VDD and the LSI still draws current as oscillation is continued. When restarted, the next playback begins after approximately 350μS.

If disabling standby transition as an option, the $\overline{RESET}$ pulse must be input to set to the standby state. Pop noise may be generated at the input of the $\overline{RESET}$ pulse as the output level from AOUT becomes GND level instantly.

8. Voice Input

The voice output pin can be selected by the output of the DA converter either directly or through the built-in low-pass filter.

8-1 Output Waveform of DA Converter

The output amplitude from the DA converter is maximum 4095/4096 ×VDD of a square wave that synchronizes with a sampling frequency. When selecting the DA output, addition of an external low-pass filter is highly recommended.

Because the output impedance of DAO varies between 15KΩ and 35KΩ, determine the filter constant so that the resistance variation does not influence the cut-off frequency of the low-pass filter.

Table 4 shows the output level from the AOUT pin when selecting an optional DA output.

Table 4 Output Level from DA Converter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	$\frac{1}{4}$VDD	$\frac{1}{2}$VDD	$\frac{3}{4}$VDD	V
2-channel mixing	0.0	$\frac{1}{2}$VDD	VDD	V
BEEP tone playback	$\frac{3}{8}$VDD	$\frac{1}{2}$VDD	$\frac{3}{8}$VDD	V

8-2 Low-pass filter output

Since the low-pass filter is composed of switch capacitors, the cut-off frequency varies proportional to the master clock frequency.

When the sampling frequency (f_{sam}) is 1/8 and 1/10 of the master clock frequency, the cut-off frequency, f_{cut}, is $f_{cut}=3/64\ f_{osc}$ and is $f_{cut}=3/128$ when f_{sam} is 1/16. Table 5 shows the relationship between the sampling frequencies and the cut-off frequencies.

Table 5 Cut-off Frequency of Low-pass Filter

Sampling frequency (fsam)	Master clock frequency (fosc)	Cut-off frequency (fcut)
4.0 kHz	64 kHz	Approximately 1.5 kHz
6.4 kHz	64 kHz	Approximately 3.0 kHz
8.0 kHz	64 kHz	Approximately 3.0 kHz
12.8 kHz	128 kHz	Approximately 6.0 kHz
16.0 kHz	128 kHz	Approximately 6.0 kHz

The low-pass filter characteristics when the sampling frequency is 8kHz are shown in figure 8. Table 6 shows the output level from AOUT when selecting the low-pass filter option.

Table 6 Output Level of Low-pass Filter

Condition	Minimum level	Center level	Maximum level	Unit
1-channel playback	$\frac{1}{4}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{4}V_{DD}$	V
2-channel mixing	0.7	$\frac{1}{2}V_{DD}$	V_{DD}–0.7	V
BEEP tone playback	$\frac{3}{8}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{8}V_{DD}$	V

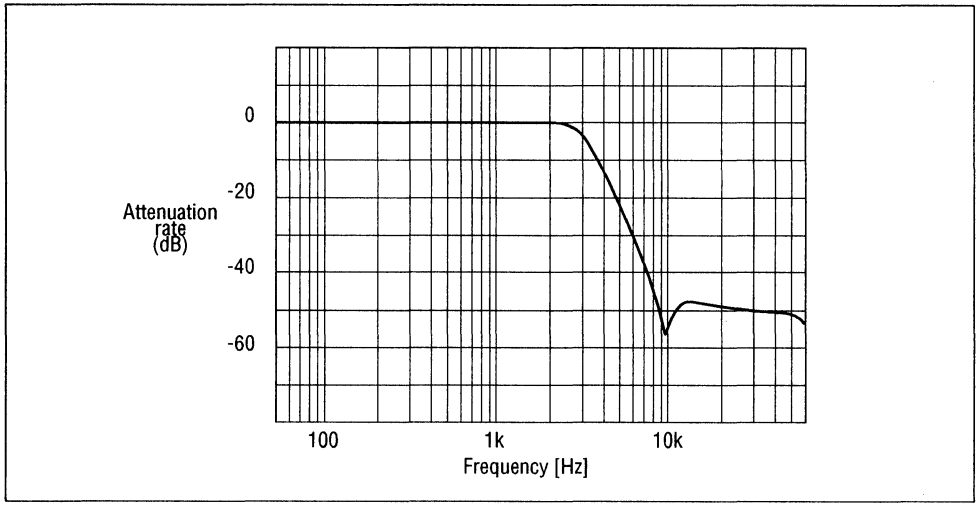


Figure 8 Low-pass Filter Characteristics (f_S=8 kHz)

8-3 Pop Noise of Low-Pass Filter Output

Although this LSI has a built-in pop noise suppression circuit, the voltage of the circled portion in the figure below may be changed abruptly by approximately 0.7V when selecting the low-pass filter output and may generate a "pop" sound.

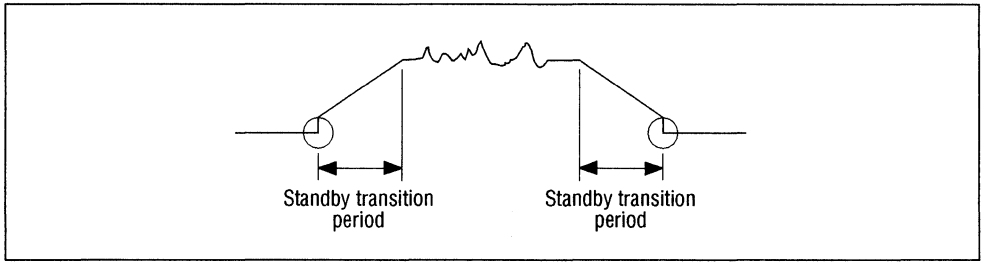


Figure 9 Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the "pop" sound can be reduced. Figure 10 shows the circuit.

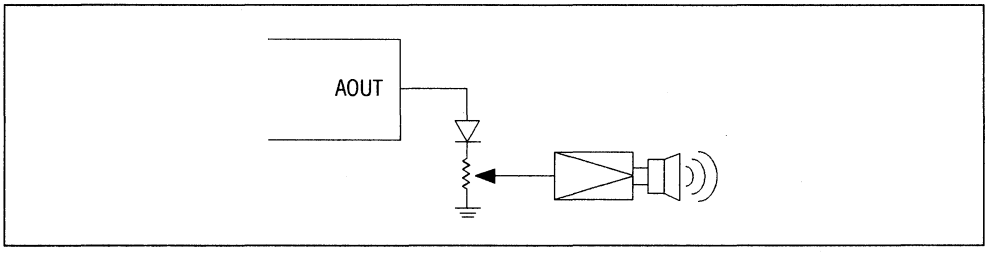


Figure 10 Pop Noise Suppression Circuit

9. RC Oscillation

The external circuit diagram for RC oscillation is shown below:

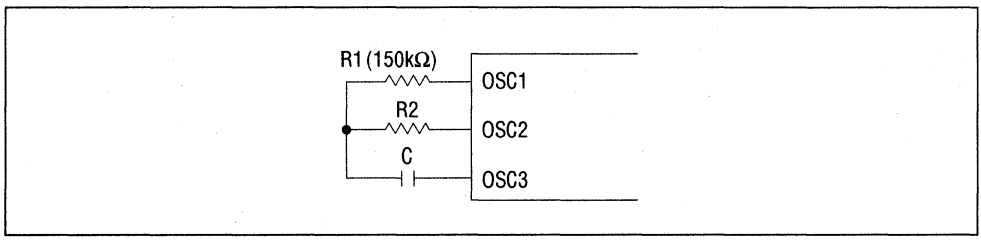


Figure 11 RC Oscillation Connection Circuit

9-1 Determination of RC Constant

The RC oscillation frequency characteristics are shown in Figure 12. If fOSC is set to 64 kHz, choose the appropriate values for C and R2 using the following as a reference:

C=100pF, R1=150KΩ, R2=50KΩ.

9-2 Fluctuation of RC oscillation frequencies

When choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R2 as well as the process variations of LSI.

When using a 50KΩ R2, the error due to process variations of the LSI is maximum ±4% so that the fluctuation of the RC oscillation frequency when using a capacitance (C) of ±1% accuracy and a resistance (R2) of ±2% accuracy is maximum ±7% approximately.

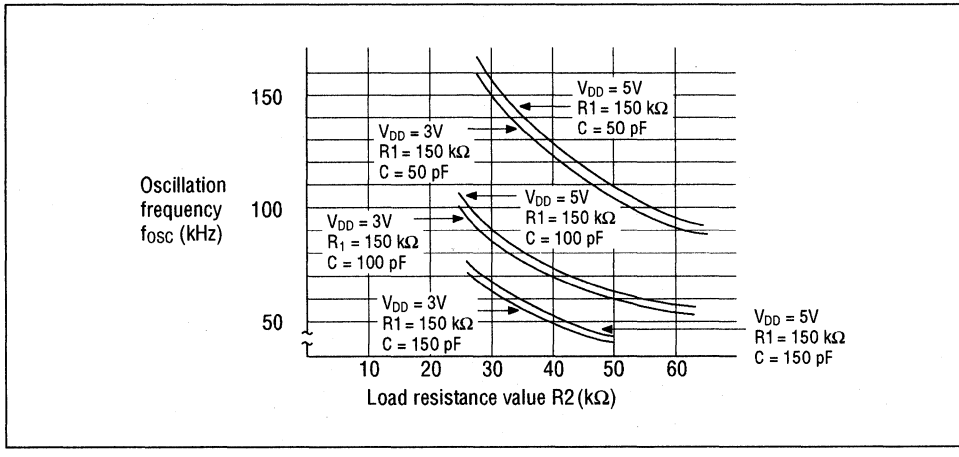


Figure 12 RC Oscillation Frequency Characteristics

10. Crystal Oscillation

Figure 13 shows an external circuit using a crystal oscillator, KF-38S4-13PO102 (64kHz), made by Kyocera.

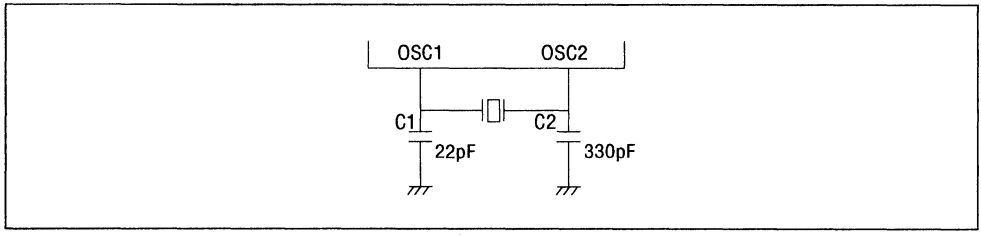


Figure 13 Circuit Diagram of Crystal Oscillator Connection

11. Connection with MSC1191/1192

When using an MSC1191 and an MSC1192, connect the STBY pin to the OSC3/$\overline{CS}$ pin an the OSC2 pin, respectively. When connecting with an MSC1191/1192, set C and R after mounting it to the board as the oscillation characteristics may change.

12. Wiring for Power Supply

Supply the power supply for this LSI from the same power supply as illustrated below and divide into an analog section and a logic section on wiring.

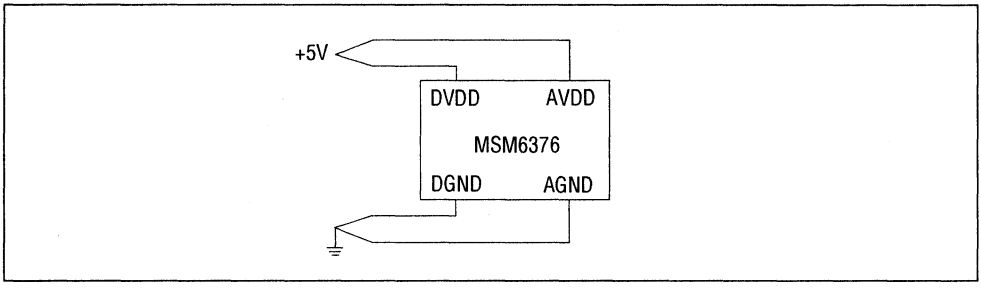


Figure 14

If the analog section and the logic section are supplied from a separate power supply, make sure that the separate power supply is not provided because there is possibility to bring about a latch-up , etc.

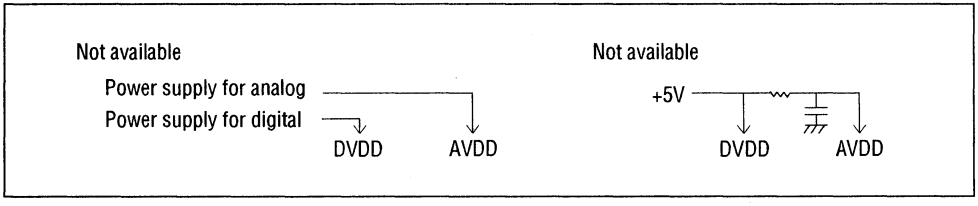
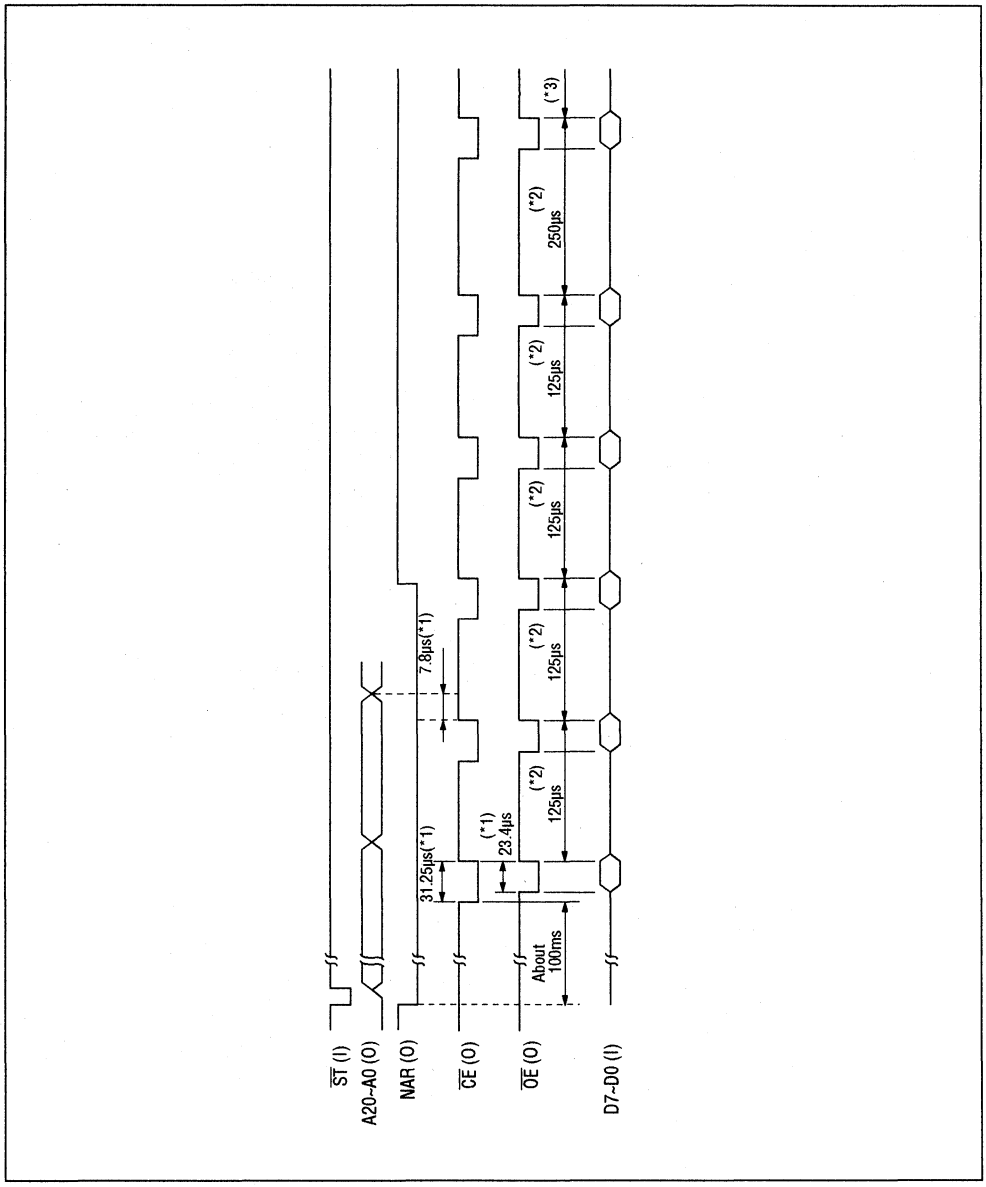


Figure 15

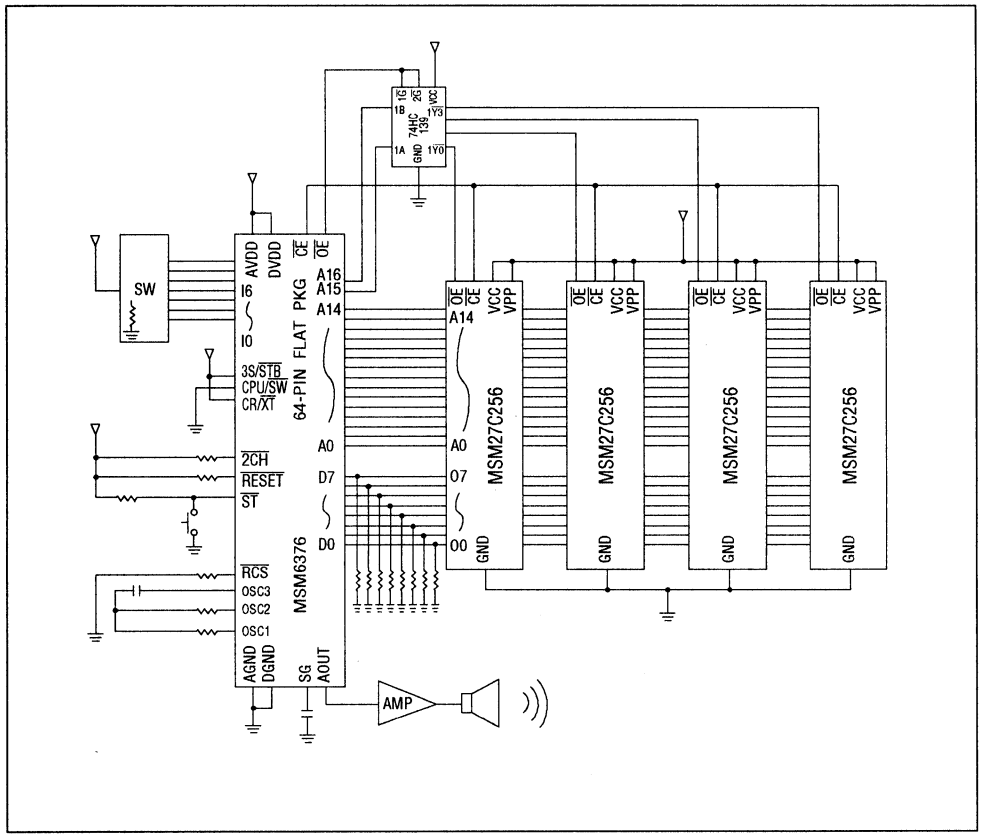
13. External ROM Timing

Figure 16 shows the external ROM driving timing under voice playback at fOSC = 64 kHz and f_{sam} = 8.0kHz.



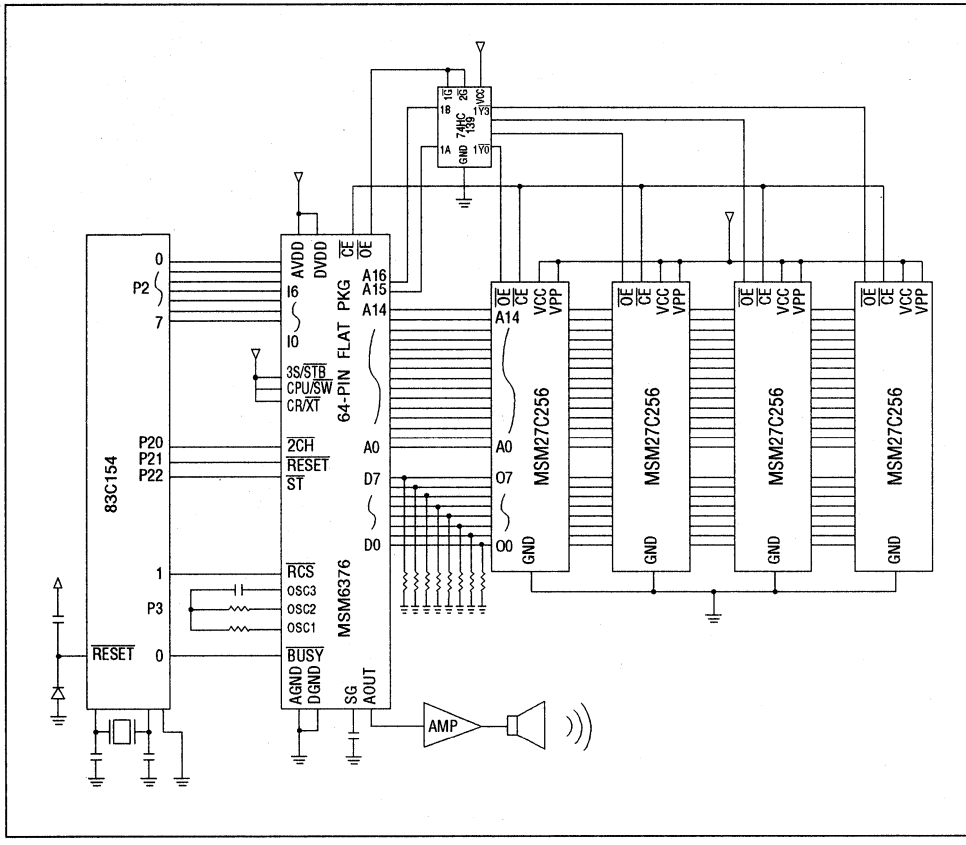
Note *1) This is proportional to fosc
*2) This is proportional to fsam
*3) CE,OE and D0~D7 are input and output at the frequency of 250μs or 125μs hereafter.

Figure 16 External ROM Timing



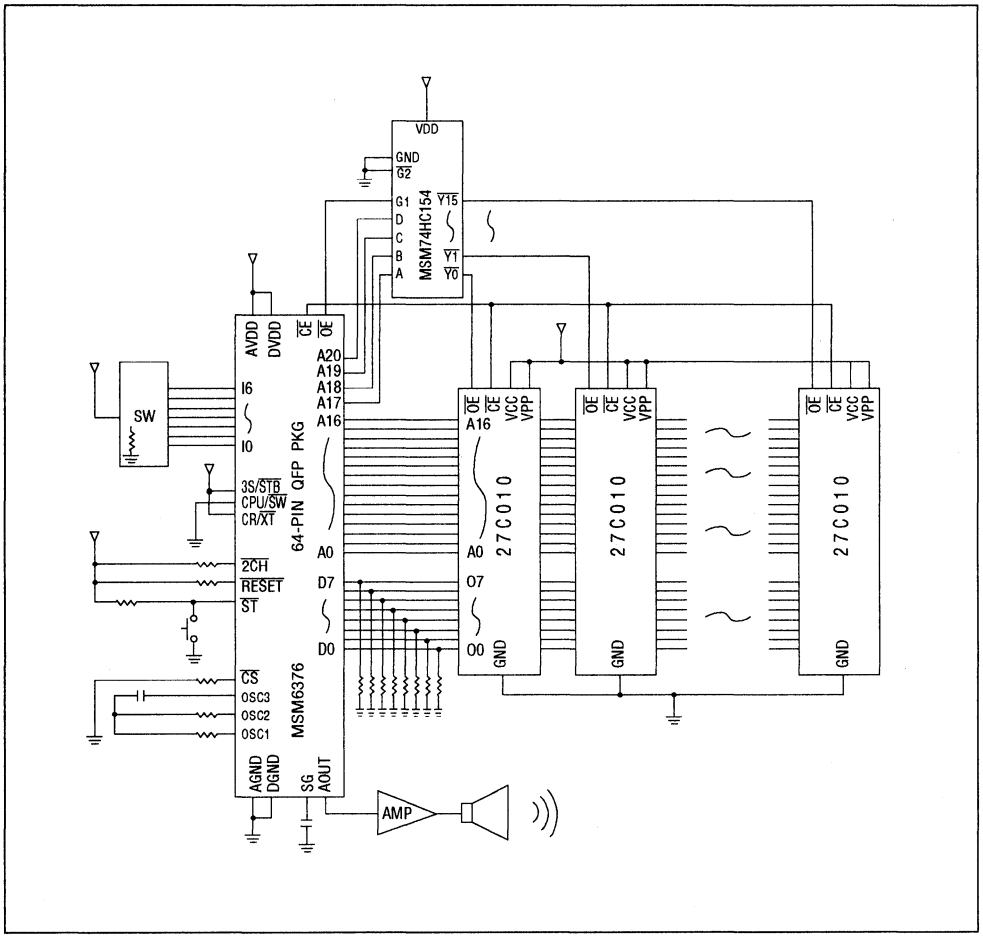
Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, there are some cases where the power voltage variation of the EPROM becomes a source to generate noise.

Figure 17 Example of Interface Using 4pcs. 256Kbit EPROMs



Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, there are some cases where the power voltage variation of the EPROM becomes a source to generate noise.

Figure 18 Example of Applied CPU Interface Circuit



Note: Use a CMOS type 27C010 as an EPROM if possible. If an NMOS type EPPROM is used the power voltage variation of the EPROM becomes a source to generate noise.

Figure 19 Example of Interface Using 16pcs. 1Mbit EPROMs

OKI Semiconductor

MSM6378A/MSM6379

OTP BUILT-IN VOICE SYNTHESIS LSI

GENERAL DESCRIPTION

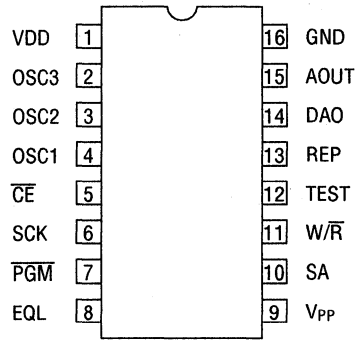
The MSM6378A/MSM6379 is an ADPCM voice synthesis LSI with a built-in one-time PROM (OTP). The MSM6378A/MSM6379 reproduces the speech data, which the user has analyzed and recorded using the "ANAWRITER" for an exclusive use, through a speaker driving AMP and speaker. The MSM6378A/MSM6379 can be used in voice cards, small-quantity multi-product toy line-ups, and personal use devices.

FEATURES

- CMOS
- MSM6379: Built-in 512Kbit OTP (500Kbits for recording)
- MSM6378A: Built-in 256Kbit OTP (244bits for recording)
- 4bit straight ADPCM method
- Built-in low pass filter
- Built-in 12bit DA converter
- Data write time: MSM6379 16 sec.
  MSM6378A 8 sec.
- Oscillation system:
  R/C oscillation or external clock input
- Oscillation frequency: 64 to 256kHz
- Sampling frequency:
  4 to 16kHz (original oscillation frequency/16)
- Activation: Power on start or reactivation after one shot output
- Speech output: one-shot or repeat
- Low current consumption
- Largest speech time:
  MSM6379 32.0 sec. (4kHz sampling)
  MSM6378A 15.6 sec. (4kHz sampling)
- Speech phrase number: One phrase only
- Power supply voltage:
  DAO pin 2.4 to 5.5V
  AOUT pin 2.7 to 5.5V (fsam ≤ 8 kHz)
  3.5 to 5.5V (fsam ≤ 10 kHz)
- Shipping package:
  16pin plastic DIP (DIP 16-P-300W1)
  chip

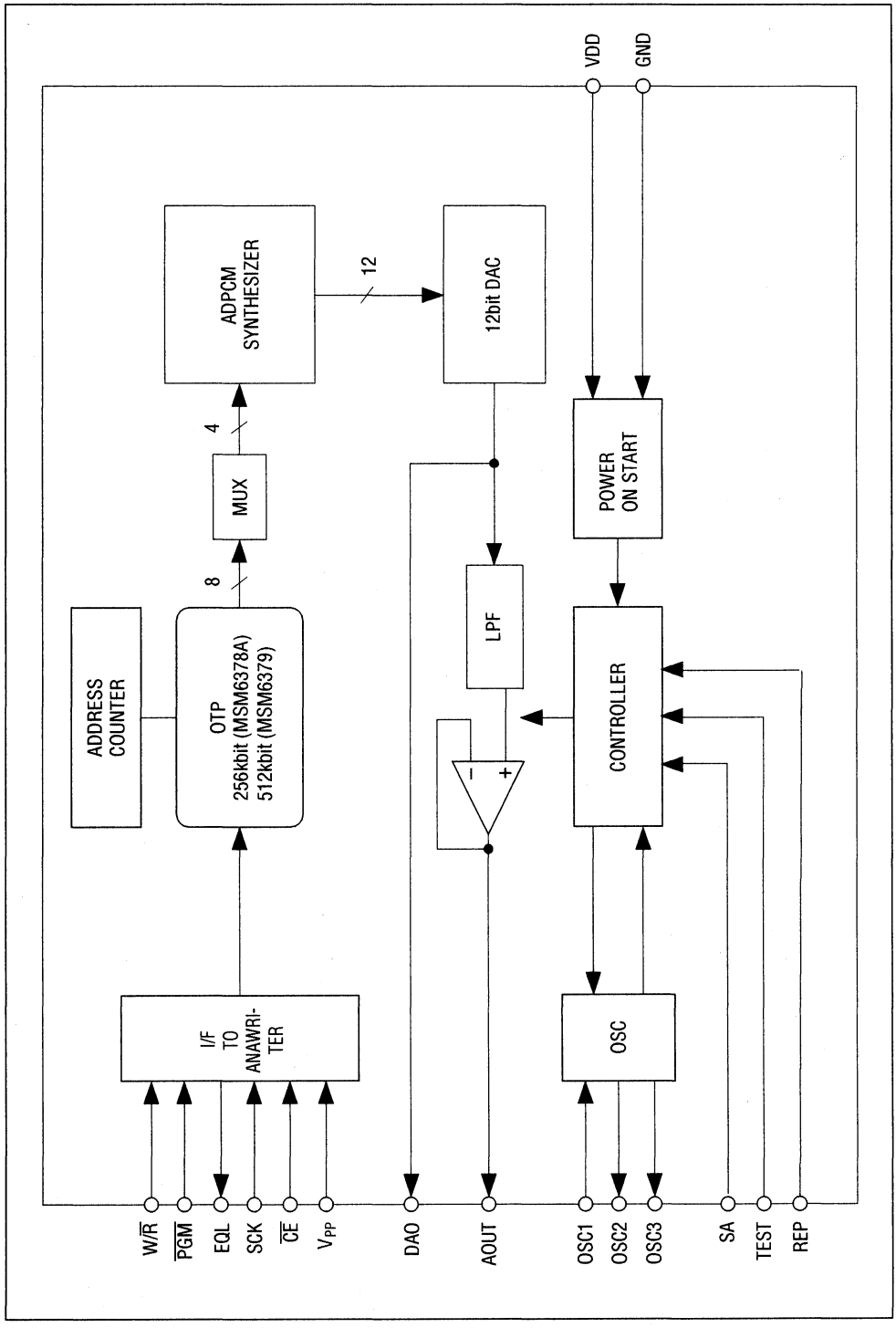
PIN CONFIGURATION

(Top View) 16 Lead Plastic DIP



Note: This is applied to MSM6378ARS and MSM6379RS.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (VPP=VDD at reproduction)

Absolute Maximum Rating

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3~7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3~V_{DD}+0.3	V
Storage temperature	T_{stg}	—	−55~125	°C

Operating Range

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	GND=0V	DAO pin 2.4~5.5 AOUT pin 2.7~5.5 (fs≤8 kHZ) 3.5~5.5 (fs≥10 kHZ)	V
Operating temperature	T_{OP}	—	−10~70	°C
Oscillation frequency	f_{OSC}	—	64~256	kHZ

DC Characteristics

(V_{DD}=4.5~5.5V GND=0V Ta=0~70°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}+0.1	V
"L" input voltage	V_{IL}	—	−0.1	—	0.2×V_{DD}	V
"H" input current 1	I_{IH1}	Applies to $\overline{CE}$, SCK, $\overline{PGM}$, SA,W/$\overline{R}$, and TEST pins	20	—	400	µA
"H" input current 2	I_{IH2}	Applies to OSC1 and REP pins	—	—	10	µA
"L" input current	I_{IL}	—	−10	—	—	µA
Operation current consumption	I_{DD}	—	—	7	20	mA
Standby current consumption	I_{DS}	—	—	0.1	10	µA
DA output relative accuracy	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
DA output impedance	R_{DAO}	—	15	25	35	kΩ
LPF minimum driving resistance	R_{AOUT}	—	50	—	—	kΩ

AC Characteristics

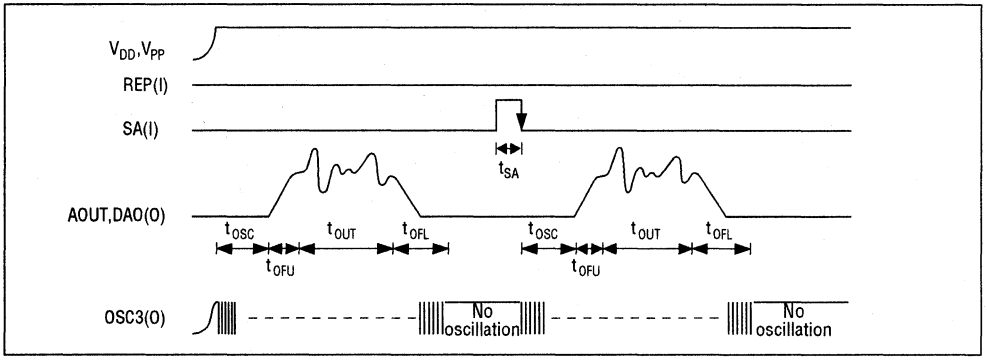
(V_{DD}=4.5~5.5V GND=0V Ta=0~70°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation duty cycle	f_{duty}	—	40	50	60	%
Sampling frequency	f_S	f_{OSC}/16	4	—	16	kHz
Oscillation stabilization time	t_{OSC}	32/f_{OSC}	128	—	512	ms
Upper offset time	t_{OFU}	1K/f_{sam}	64	—	256	ms
Lower offset time	t_{OFL}	2K/f_{sam}	128	—	512	ms
MSM6378A speech output time	t_{OUT1}	244Kbit/(4bit×f_{sam})	3.9	—	15.6	S
MSM6379 speech output time	t_{OUT2}	500Kbit/(4bit×f_{sam})	8.0	—	32.0	S
SA input pulse width	t_{SA}	—	10	—	—	µs
MSM6378A data write time	t_{WR1}	*Use ANAWRITER	—	8	—	S
MSM6379 data write time	t_{WR2}	*Use ANAWRITER	—	16	—	S

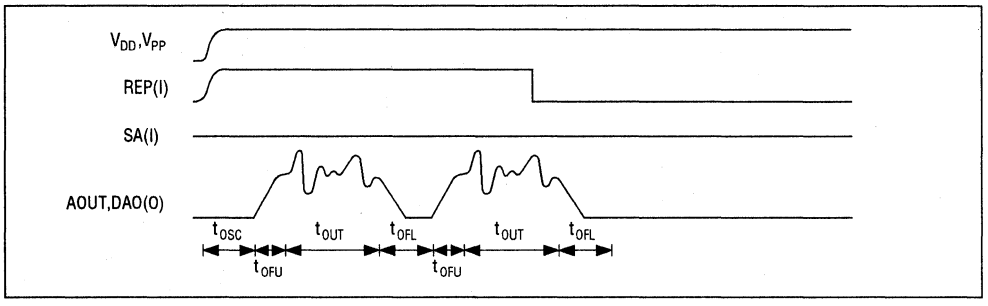
* MSM6378A/6379 guarantees the write only by the ANAWRITER or speech analysis editing tools (AR761 and AR76-202). The anawriter is a registered trademark of Oki Electric Industry Co., Ltd.

TIME CHARTS

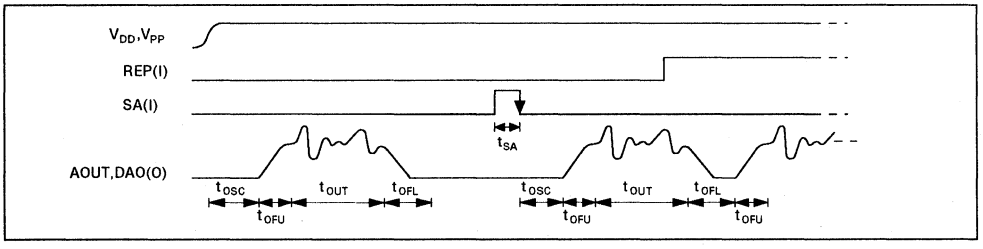
1. Reactivation after One-shot Output



2. One-shot after Repeat

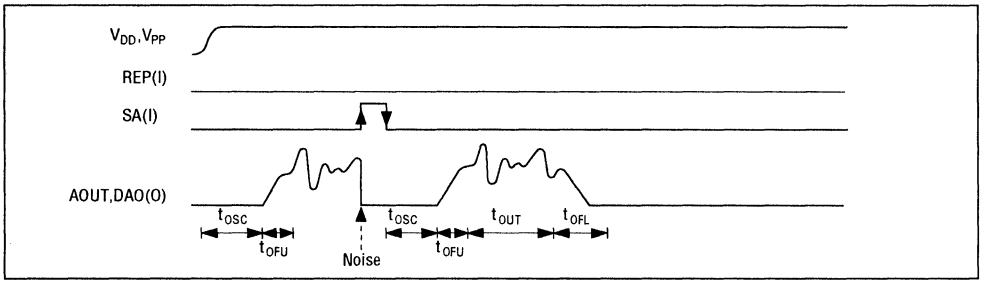


3. Repeat during Speech Output



Note: When REP pin is merely set to "H" level, the speech is not output.

4. Reactivation during Speech Output



Note: When SA pin goes to "H" level during playback, speech is stopped and a noise is output.

PIN DESCRIPTION

Pin Name	I/O	Function
REP	I	Repeat/one-shot selection pin. In power-on or input to SA pin, one-shot is output when REP="L" and repeated speeches are output when REP="H". The speech is not output so long as this pin is merely set to "H" level. This pin does not include pull-down resistance.
SA	I	Pin to be reactivated after one-shot output. When a single pulse is applied to SA pin, the LSI is reactivated on the falling edge. This pin includes pull-down resistance.
W/$\overline{R}$	I	Interface pin for the ANAWRITER for exclusive use. Set to "L" or "open" in playback. This pin includes pull-down resistance.
$\overline{PGM}$	I	Same as above (W/$\overline{R}$).
SCK	I	Same as above (W/$\overline{R}$).
$\overline{CE}$	I	Same as above (W/$\overline{R}$).
EQL	O	Interface pin for the anawriter for exclusive use. Set to "open" in playback.
TEST	I	Internal circuit test pin. Set to "L" or "open" in playback. This pin includes pull-down resistance.
OSC1	I	Oscillation RC connection pin or external clock input pin.
OSC2	O	Oscillation RC connection pin. Set to open to input external clock through the OSC1 pin.
OSC3	O	Same as above (OSC2).
DAO	O	DA converter output pin.
AOUT	O	LPF output pin.
V_{PP}	–	Power voltage pin for writing the built-in OTP. Set to $V_{PP} = V_{DD}$ or "open" in playback.
V_{DD}	–	Power pin.
GND	–	Ground pin.

FUNCTIONS

1. Number of Phrases

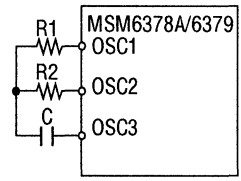
   One word only

2. Relationship Between R, C, Original Oscillation Frequency, and Speech Output Time

C (pF) 3V	C (pF) 5V	R1(kΩ) 3V	R1(kΩ) 5V	R2 (kΩ) 3V	R2 (kΩ) 5V	fosc (kHz)	fsam (kHz)	fcut (kHz)	tout1(sec) MSM6378A	tout2(sec) MSM6379
100	100	200	200	56.5	60.5	64	4	1.5	15.6	32.0
100	100	200	200	34.5	36.5	96	6	2.2	10.4	21.3
100	100	200	200	23	25	128	8	2.9	7.8	16.0
100	100	200	200	16.5	18	160	10	3.6	6.2	12.8
100	100	200	200	12.5	14	192	12	4.4	5.2	10.6
100	100	200	200	9.5	11	224	14	5.1	4.5	9.1
100	100	200	200	7.5	9	256	16	5.8	3.9	8.0

$$* t_{OUT1} = \frac{244Kbit}{4bit \times f_{sam}}$$

$$* t_{OUT2} = \frac{500Kbit}{4bit \times f_{sam}}$$



The values of C, R1, and R2 for the above table are for the MSM6378A 16-pin DIP. The oscillation frequency fluctuates with an external resistance and floating capacity. Therefore, since the oscillation frequency fluctuates when the board wiring and packages are different, determine the constant after check with monitoring fosc at OSC3 pin with reference to the above table.

3. Ceramic Oscillator (fosc=256kHz)

- Figure 3-1 shows an external circuit that used the ceramic oscillator CSB256D made by Murata.
- Figure 3-2 shows an external circuit that used the ceramic oscillator KBR-256B made by Kyosera.

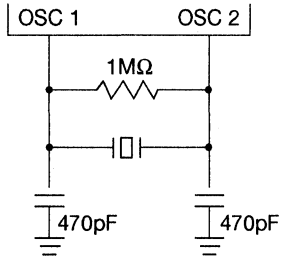


Figure 3-1 Ceramic Oscillator (CSB256D) Connection Circuit

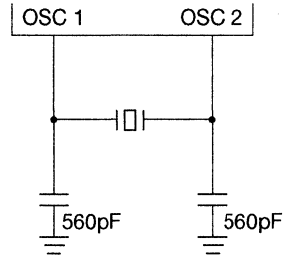


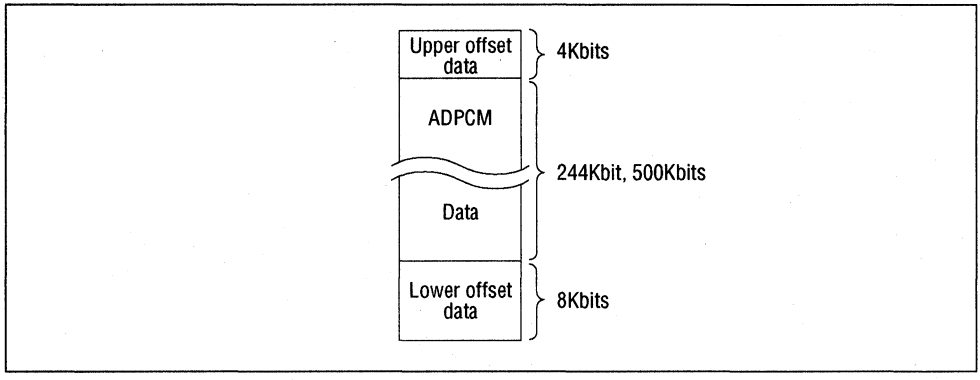
Figure 3-2 Ceramic Oscillator (KBR-256B) Connection Circuit

4. Pop Noise Prevention

To prevent generation of pop noise before and after speech output, the MSM6378A/6379 contains a 12Kbit offset data area in the built-in OTP. The anawriter for exclusive use automatically reads the offset data into the MSM6378A/6379.

5. Activation

The MSM6378A/6379 is activated as soon as the power is turned on (power-on start function). To reactivate from stand-by mode, apply a pulse on the SA pin, and the speech is again output.



6. Repeat

The MSM6378A/6379 repeats when the REP pin is set to "H"level. However, the speech is not output when the REP pin is merely set to "H"level.

7. Standby Mode

When the REP pin is set to "L"level, the MSM6378A/6379 outputs one-shot speech and enters standby mode after the power is turned on or a pulse is applied to the SA pin. While in standby mode, internal oscillation stops and the OSC3 pin is set to "H"level.

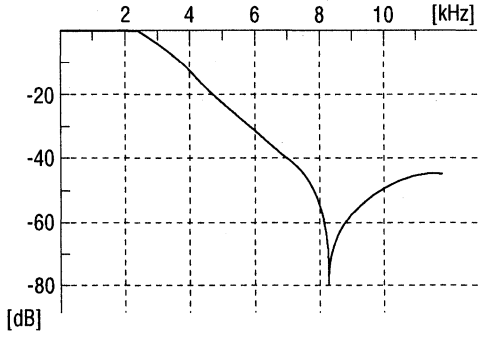
8. Speech Output Pin

The MSM6378A/6379 has two speech output pins. The DAO pin is for internal DA converter output, and the AOUT pin is for DAO output via the LPF.

9. LPF Characteristic

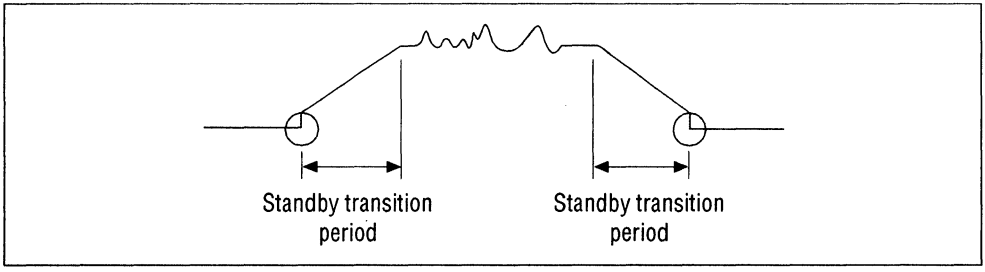
The LPF cut-off frequency (fcut) is always proportional to original oscillation frequency. The following figure shows the LPF characteristic curve at 8kHz sampling frequency (with the original oscillation frequency set to 128kHz).

fosc (kHz)	f_{sam} (kHz)	f_{CUT} (kHz)
64	4	Approx. 1.5
96	6	Approx. 2.2
128	8	Approx. 2.9
160	10	Approx. 3.6
192	12	Approx. 4.4
224	14	Approx. 5.1
256	16	Approx. 5.8



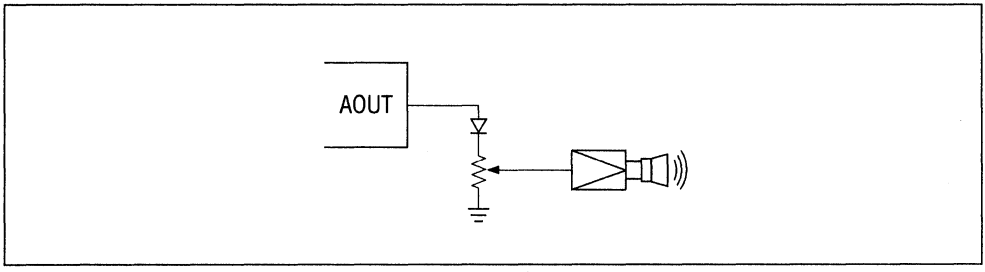
10. Pop Noise of Low-Pass Filter Output

Although the MSM6378A/6379 has a built-in pop noise suppression circuit, the voltage of the circled portion in the figure below may be changed abruptly by approximately 0.7 V when selecting the low-pass filter output and may generate a "pop" sound.



Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the "pop" sound can be reduced. The following figure shows its circuit.

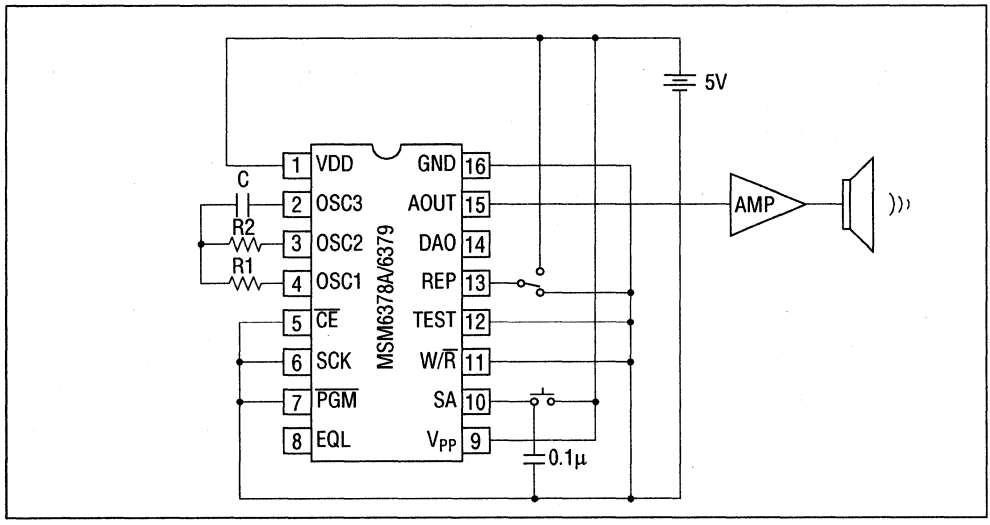


Pop Noise Suppression Circuit

APPLICATION NOTES

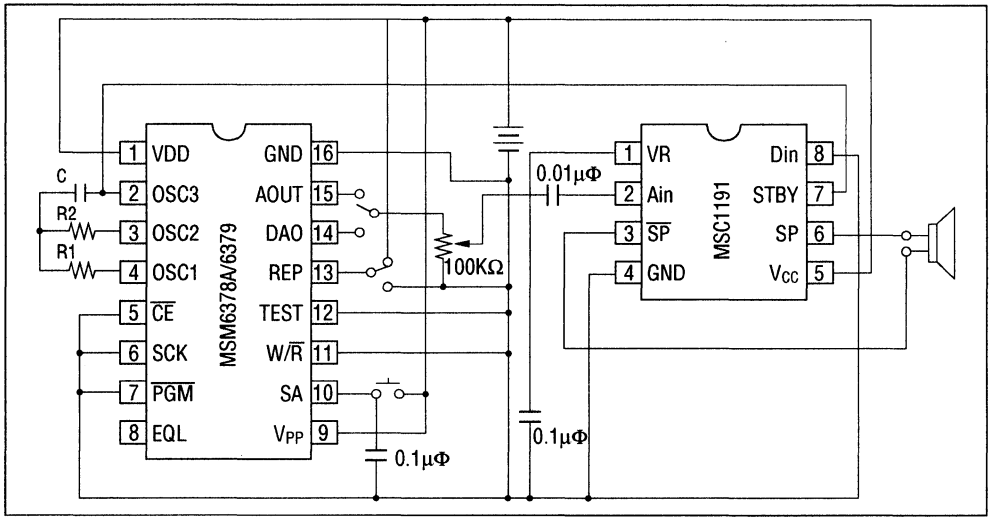
I. Playback

1.1 When Used Standard AMP



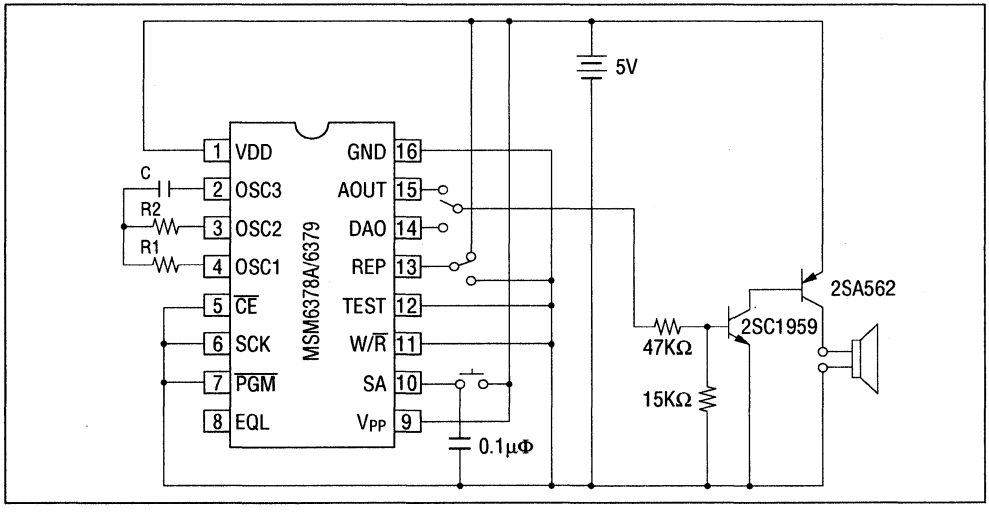
Note: The capacitor connected to the SA pin contributes to noise margin in the case of SA being "open"

1.2 Use of MSC1191 as AMP



Note: * MSC1191 is the most suitable amplifier to drive a speaker for the voice LSI. When MSM6378A terminates the reproduction of speech data, MSC1191 is also put into power save mode automatically.

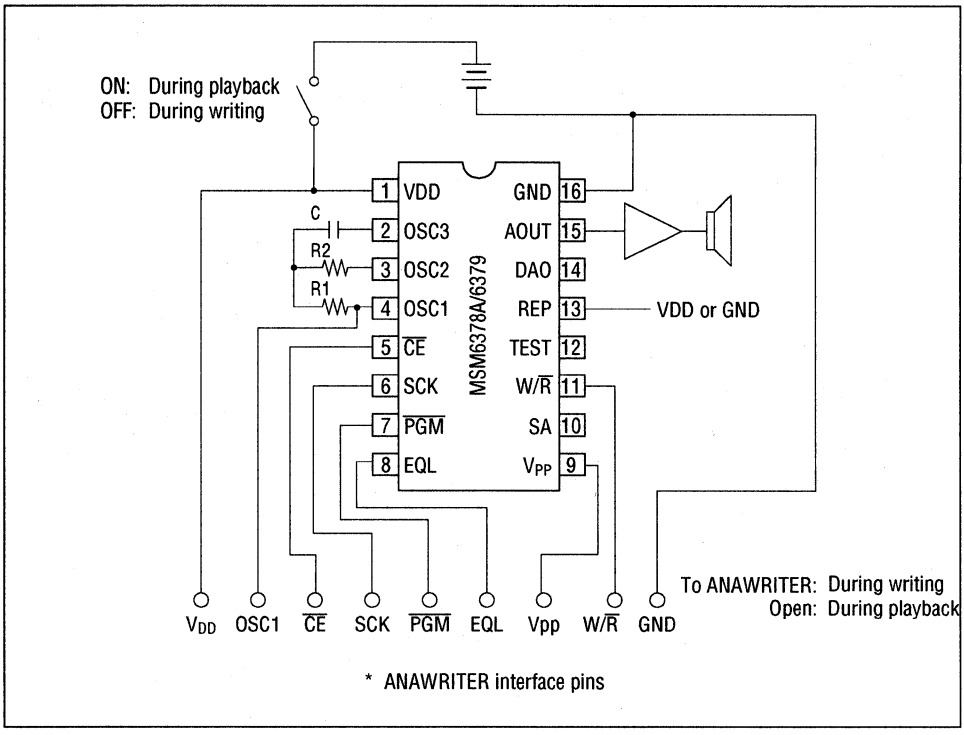
1.3 Use of Tr as AMP



Note: If 5V or less is used, change the constant used to divide the resistor in the output stage.

EXAMPLE OF WRITE CIRCUIT

(equivalent to the playback circuit)



Note: * Be careful about noise margin for input pins that are open during playback.

OKI Semiconductor

MSM6652-XXX/MSM6653-XXX/ MSM6654-XXX/MSM6655-XXX/ MSM6656-XXX

Internal MASK ROM Speech Synthesis LSI

GENERAL DESCRIPTION

The MSM6650 family is a successor to the MSM6375 family that are speech synthesis LSIs with internal mask ROM. Since the PCM Method is added in addition to the ADPCM Method, a 12bit DA converter and a -40dB/oct low pass filter are built in, high quality sound synthesis was made possible.

The conventional "BEEP" tone and a 2-channel mixing function are now easier to use, and a melody function, fadeout function and random vocalization function are now included. External control is easier than before due to the addition of an edit ROM that can form sentences by linking phrases.

As it is possible to select standalone mode or microcomputer interface mode by the mask option, it can handle various applications. Because microcomputer interface mode has serial inputs, it is possible to reduce the number of ports for controlling microcomputers.

We developed an MSM6650 driven by external ROM as an evaluation LSI for the MSM6650 family.

The general differences between the MSM6650 family and the MSM6375 family follow.

	MSM6650 Family	MSM6375 Family
Interface	Standalone/Microcomputer	SW input/CPU input
Speech Synthesis Method	4bit ADPCM / 8bit PCM / Melody PCM	4bit ADPCM
BEEP Tone Output Frequency Duration	0.5 kHz/1.0 kHz/1.6 kHz/2.0 kHz Arbitrary (16 ms~2100 ms)	1.0 kHz/2.0 kHz Fixed (64 ms/128 ms/250 ms/500 ms)
Sampling Frequency (fsam)	4.0 kHz/5.3 kHz/6.4 kHz/8.0 kHz 10.6 kHz/12.8 kHz/16.0 kHz/32.0 kHz	4.0 kHz/6.4 kHz/8.0 kHz (f_{OSC} = 64 kHz) 16.0 kHz/25.6 kHz/32.0kHz (f_{OSC} = 256 kHz)
Original Oscillation Frequency (fosc)	256 kHz (RC)/4.096 MHz (X'tal)	40 kHz ~ 256 kHz
LPF Attenuation Factor	-40 dB/oct	-24 dB/oct
LPF Cutoff Frequency f_{CUT} (kHz)	f_{CUT}: 1.8 | 2.6 | 2.6 | 3.2 | 4.2 | 5.1 | 6.4 | 12.8 f_{sam}: 4.0 | 5.3 | 6.4 | 8.0 | 10.6 | 12.8 | 16.0 | 32.0	f_{CUT}: 1.5 | 3.0 | 3.0 f_{sam}: 4.0 | 6.4 | 8.0
Maximum No. of Phases	127	111
Pullup/Pulldown Resistance	Yes	No
Standby Conversion Time	0.2 sec	3.0 sec
Mask Option	4 types	14 types
Additional Functions	Edit ROM Fadeout Random vocalization Melody regeneration PCM regeneration Serial input/Port output	

See the related Data Book for details on differences.

This LSI is classified roughly into standalone mode and microcomputer interface mode. Because this data sheet explains the two modes separately, please refer to appropriate items by the index below.

Table of Contents

Standalone

Microcomputer Interface

(1) STANDALONE MODE

FEATURES

Type	ROM Capacity	Maximum Vocalization Time			
		fsam = 4.0 kHz	fsam = 6.4 kHz	fsam = 8.0 kHz	fsam = 16.0 kHz
MSM6652	288 Kbit	16.9sec	10.5sec	8.4sec	4.2sec
MSM6653	544 Kbit	31.2sec	19.5sec	15.6sec	7.8sec
MSM6654	1 Mbit	63.8sec	39.9sec	31.9sec	15.9sec
MSM6655	1.5 Mbit	96.5sec	60.3sec	48.2sec	24.1sec
MSM6656	2 Mbit	129.1sec	80.7sec	64.5sec	32.2sec

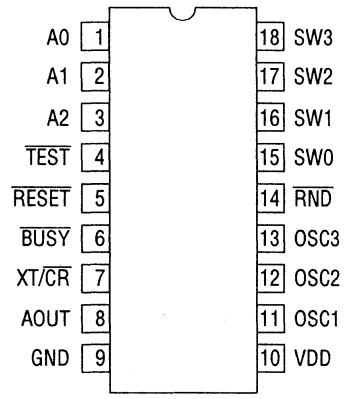
(Actual speech ROM area is less by 22 Kbit)

ROM custom
4-bit ADPCM method/8-bit PCM method
Melody function
Edit ROM function
2-channel mixing function built in
Internal random vocalization function
Fadeout function (4-step change of sound volume)
BEEP tone built in — BEEP tones of 0.5 kHz, 1.0 kHz, 1.6 kHz and 2.0 kHz can be generated by specification code.
Sampling frequencies — 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz 1)
Note 1) 32.0 kHz cannot be selected if RC oscillation is selected.
Maximum number of phrases : 120 Phrases
Internal 12-bit D/A converter
Internal LPF attenuation factor : -40 dB / oct
Standby function
RC oscillation or ceramic oscillation can be selected
Package : 18-pin DIP (DIP18-P-300)
: 24-pin SOP (SOP24-P-430-VK)
: Chip

PIN CONFIGURATION

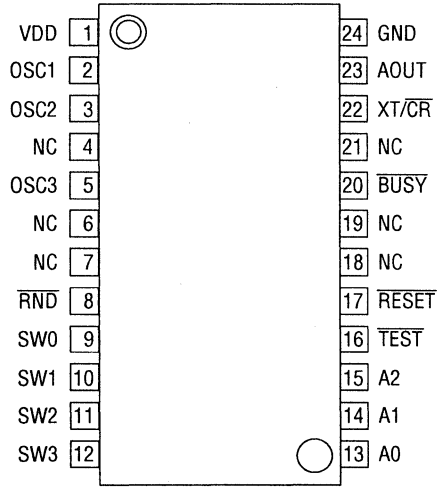
(Top View)

18 Lead Plastic DIP



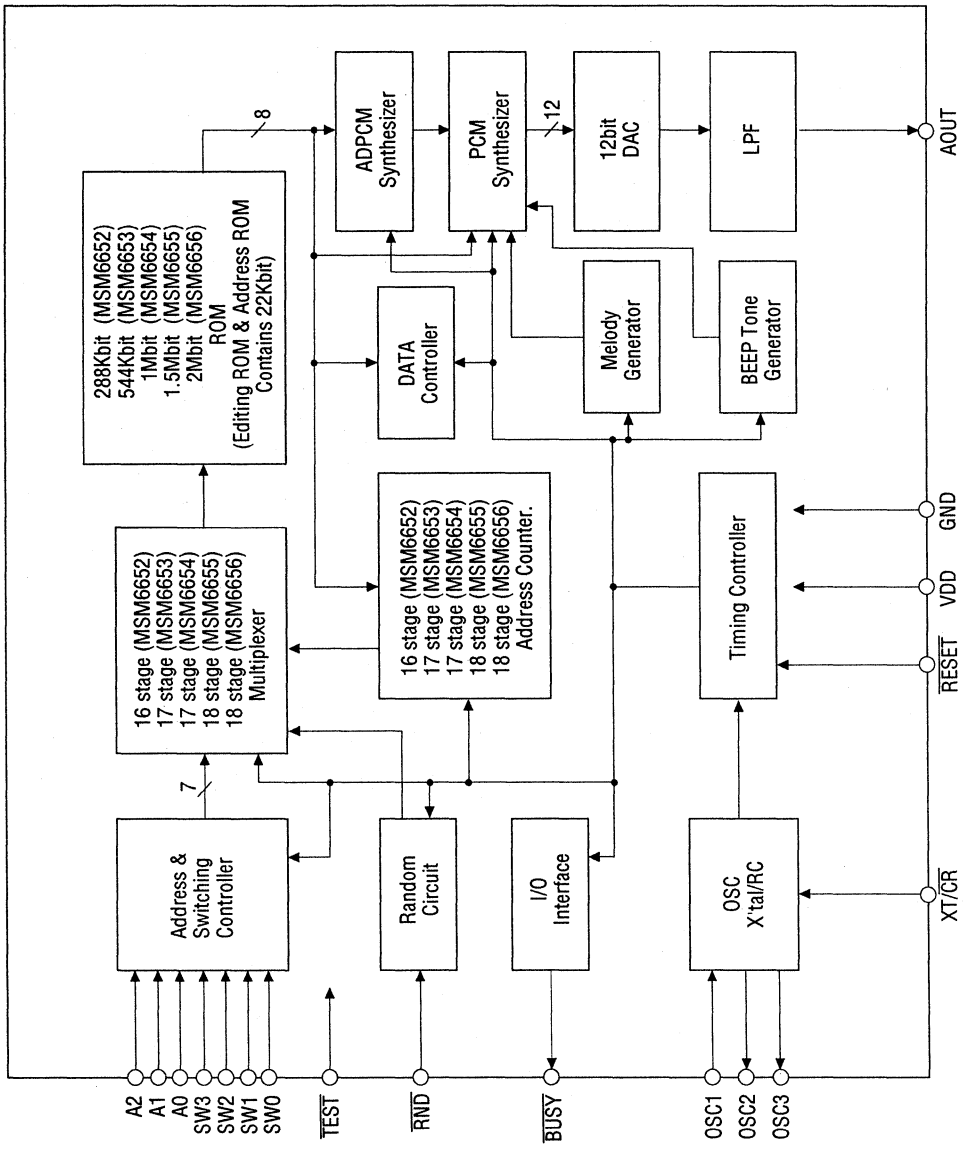
Note: Applicable to MSM6652-XXXRS, MSM6653-XXXRS, MSM6654-XXXRS, MSM6655-XXXRS and MSM6656-XXXRS

24 Lead Plastic SOP



Note: Applicable to MSM6652-XXXGS-VK, MSM6653-XXXGS-VK, MSM6654-XXXGS-VK, MSM6655-XXXGS-VK and MSM6656-XXXGS-VK

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operation Range

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	LPF output	+2.7 ~ +5.5	V
Operating Temperature	T_{op}	–	-40 ~ 85	°C
Original Oscillation Frequency (1)	f_{OSC}	When X'tal selected	3.5 ~ 4.5	MHz
Original Oscillation Frequency (2)	f_{OSC2}	When RC selected[1)]	200 ~ 300	kHz

Note 1: The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the R and C of the external parts.

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance terminal	-200	-90	-30	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2	I_{IL2}	Internal pullup resistance terminal	30	90	200	µA
Operating Current Consumption	I_{DD}	–	–	6	10	mA
Standby Current Consumption	I_{DS}	–	–	–	10	µA
LPF Load Resistance	R_{AOUT}	–	50	–	–	kΩ
LPF Output Impedance	R_{LFP}	I_F = 100µA	–	1	3	kΩ

DC Characteristics

(V_{DD} = 3.1V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	2.7	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	2.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-100	-30	-10	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2	I_{IL2}	Internal pullup resistance pin	10	30	100	µA
Operating Current Consumption	I_{DD}	–	–	4	7	mA
Standby Current Consumption	I_{DS}	–	–	–	1	µA
LPF Load Resistance	R_{AOUT}	–	50	–	–	kΩ
LFP Output Impedance	R_{LPF}	I_F = 100µA	–	1	3	kΩ

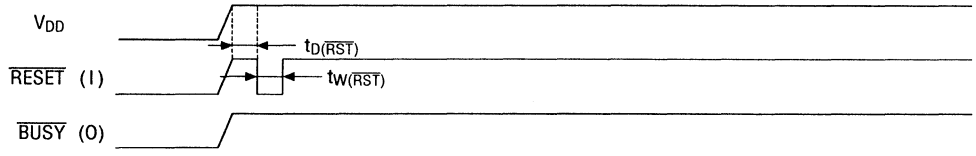
AC CHARACTERISTICS

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

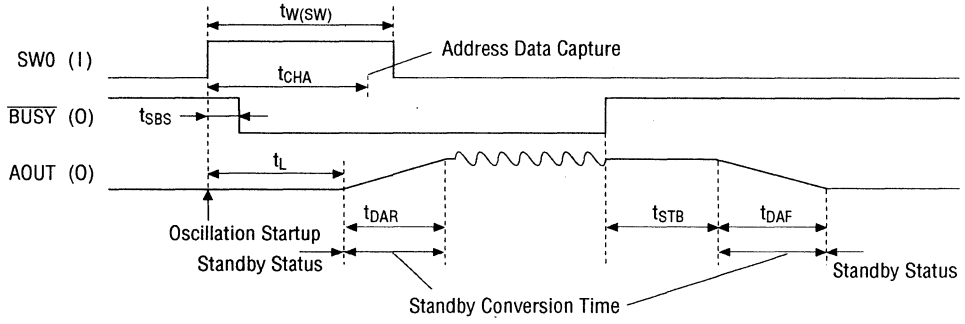
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{W(\overline{RST})}$	–	10	–	–	µS
$\overline{\text{RESET}}$ Input Time after Power on	$t_{D(\overline{RST})}$	–	0	–	–	µS
$\overline{\text{RND}}$ Input Pulse Width	$t_{W(\overline{RAN})}$	Function details 5.2	100	–	–	µS
SW3~SW0 Input Pulse Width	$t_{W(SW)}$	–	16	–	–	mS
$\overline{\text{BUSY}}$ Output Time(1)	t_{SBS}	–	–	–	10	µS
$\overline{\text{BUSY}}$ Output Time(2)	t_{BN}	fsam = 8kHz	350	375	400	µS
Chattering Prevention Time	t_{CHA}	–	14	15	16	mS
DA Converter Change Time	t_{DAR}	–	60	64	68	mS
LPF Stabilization Time	t_L	–	6	8	10	mS
Standby Conversion Time	t_{STB}	–	0.15	0.20	0.25	sec
Capture Random Address Time	t_{RA}	Function details 5.2	16	32	48	µS

TIMING CHART

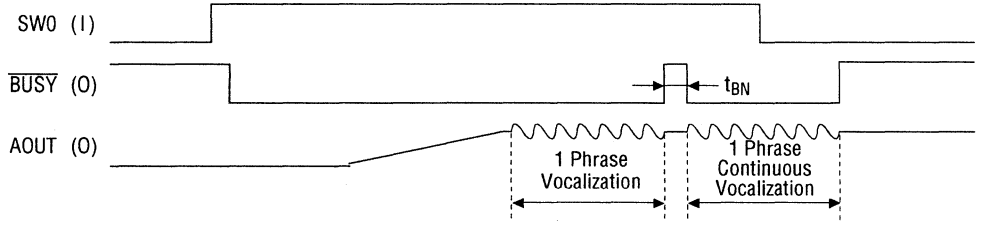
1. When Power is Turned ON



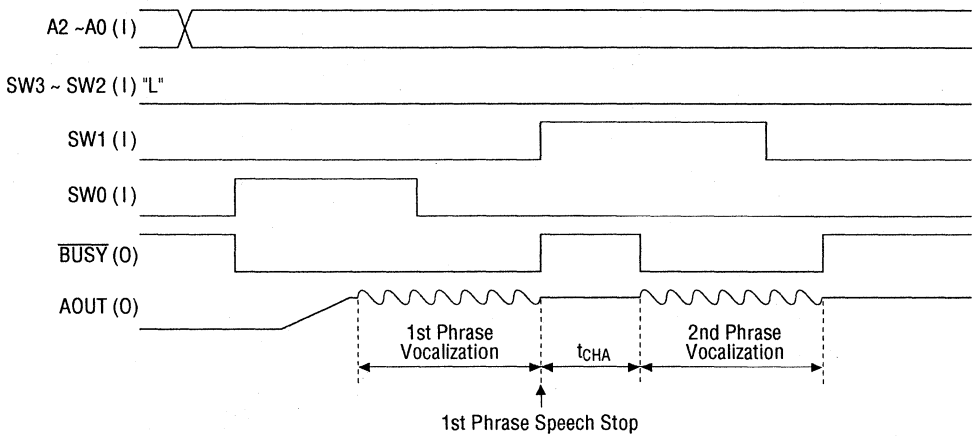
2. When LSI Starts Up and is In Standby Status



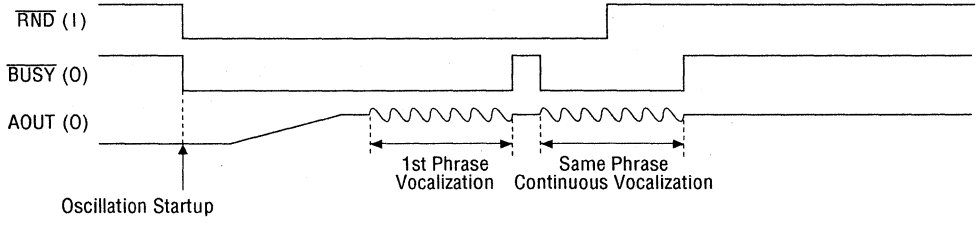
3. Repeat Vocalization Timing Chart



4. Timing Chart When SW 3~SW 0 are Changed During Vocalization



5. Repeat Vocalization Timing Chart of Random Vocalization



PIN DETAILS

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	LSI is in standby status if set to "L". At this time oscillation stops and AOUT output becomes GND, and returns to initial status. LSI has internal power ON reset. To operate power ON reset correctly startup power within 1 mS If not, apply $\overline{\text{RESET}}$ pulse when power is turned ON. This pin has internal pullup resistance.
$\overline{\text{BUSY}}$	O	Outputs "L" level during vocalization. In "H" level when power is turned ON.
XT/$\overline{\text{CR}}$	I	X'tal/RC selectable pin. Set to "H" level if ceramic oscillator is used. Set to "L" level if RC oscillation is used.
AOUT	O	Speech output pin of internal LPF.
GND	–	Ground pin
VDD	–	Power pin
OSC1	I	Ceramic oscillator connection pin when ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic ocsillator connection pin when ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Set to open if external clock is used. Outputs "L" level in standby status.
OSC3	O	Set to open if ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Outputs "H" level in standby status when RC oscillation is selected.
$\overline{\text{RND}}$	I	Random vocalization starts if $\overline{\text{RND}}$ pin is set to "L" level. Captures address from random address generation circuit in LSI at fall of $\overline{\text{RND}}$. Set to "H" level if random vocalization function is not used. This pin has internal pullup resistor.
$\overline{\text{TEST}}$	I	A test pin. Set to "H" level. This pin has internal pullup resistor.
SW3~SW0	I	Phrase input pins corresponding to vocalized sound. If input changes, SW3~SW0 pins capture addresses after 16 mS, and starts speech synthesis. These pins have internal pulldown resistor.
A2~A0	I	Phrase input pins corresponding to vocalized sound. A0 input becomes invalid if the random vocalization function is used.

FUNCTION DETAILS

1. VOCALIZATION CODE SPECIFICATION

The user can specify a maximum of 120 phrases. Table 1.1 shows the settings by A2~A0 and SW3~SW0.

Table 1.1 User Specified Phrase List

A2 ~ A0	SW3 ~ SW0	Code Description
000 ≀ 111	0000	Forbidden Code
	0001 ≀ 1111	User Specified Phrase (120 phrases)

2. INTERNAL ROM USAGE DISABLED AREA

The last 3 bytes of the internal ROM are not to be used as shown in Table 2. Please do not use those 3 bytes when analyzing speech.

For instance, make sure to select only the MSM6652 by analysis tool AR76-202 (do not use MSM6653 for example) when making EPROM for the MSM6652.

Table 2.1 shows the addresses that are not to be used for each model.

Table 2.1 Internal ROM Layout and Usage-Disabled Area

Type	Speech Data Area	Usage-Disabled Area
MSM6652	00B00 ~ 08FFC	08FFD, 08FFE, 08FFF
MSM6653	00B00 ~ 10FFC	10FFD, 10FFE, 10FFF
MSM6654	00B00 ~ 1FFFC	1FFFD, 1FFFE, 1FFFF
MSM6655	00B00 ~ 2FFFC	2FFFD, 2FFFE, 2FFFF
MSM6656	00B00 ~ 3FFFC	3FFFD, 3FFFE, 3FFFF

Note: Addresses are in hex mode.

3. PULLUP/PULLDOWN RESISTANCE

The $\overline{\text{RESET}}$, $\overline{\text{RND}}$ and $\overline{\text{TEST}}$ pins have internal pullup resistors and the SW3~SW0 pins have internal pulldown resistors.

4. OPTION(S)

In standalone mode the XT/$\overline{\text{CR}}$ pin can be used to select the oscillation circuit. If this pin is set to "H" level the circuit is in ceramic oscillation or X'tal, conversely, if set to "L" level, the circuit is in RC oscillation.

In the case of RC oscillation, however, a 32 kHz sampling frequency cannot be used.
An option to move to stand-by mode can be selected when rewriting ROM data.

5. STANDALONE MODE

In standalone mode, the complete SW input interface function and the random vocalization function can be used.

5.1 Complete SW Input Interface

With the complete SW input interface, speech synthesis starts when SW3~SW0 pins have changed. However, to prevent chattering, the address at 16 ms (t_{CHA}) is captured after SW3~SW0 pins have changed. Speech synthesis does not start even if A2~A0 pins have changed.
Set the $\overline{RND}$ pin to "H" level if the random vocalization function is not used.
At the power supply , SW3~SW0 pins are all "L" level.
The complete SW input interface is effective when operating MSM6650 using a push switch. Speech synthesis starts when an address is changed by pressing the push switch. If the push switch is released during vocalization, vocalization stops when the current vocalized phrase ends.

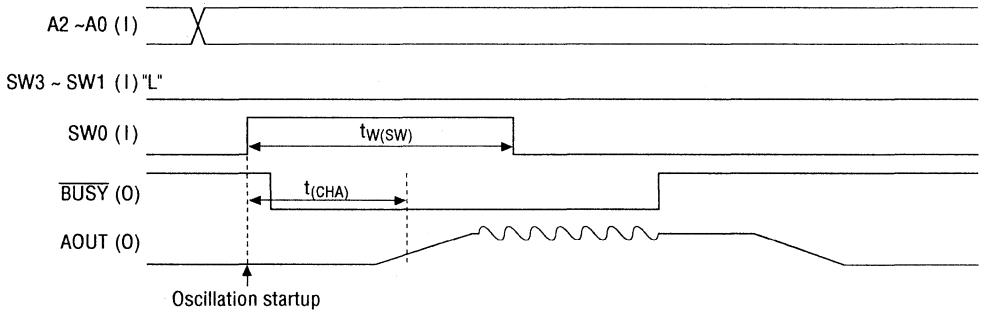


Figure 5.1 Complete SW Input Interface 1 Phrase Vocalization Timing

Figure 5.1 shows one phrase vocalization timing.

If the push switch is continuously pushed, the same phrase vocalization is repeated. Figure 5.2 shows repeat vocalization timing. Figure 5.3 shows vocalization timing when A2~A0 are changed during vocalization.

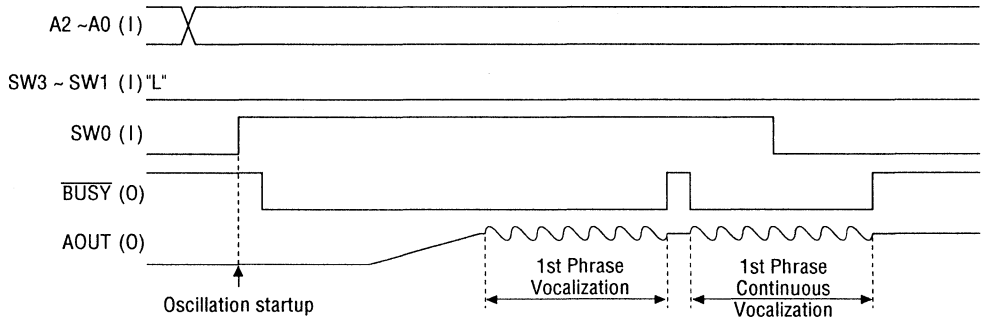


Figure 5.2 Complete SW Input Interface Repeat Vocalization Timing

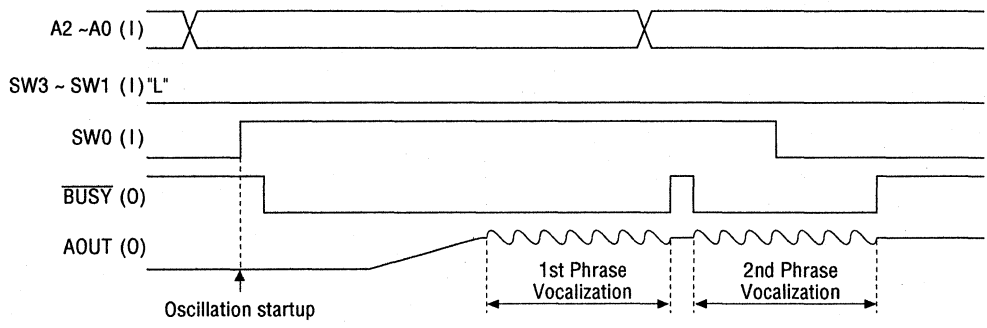


Figure 5.3 Complete SW Input Interface Vocalization Timing

If SW3~SW0 terminals change during vocalization, vocalization stops and the next phrase is vocalized. For the next phrase vocalization, speech is first stopped and is synthesized after 16 mS of chattering prevention.

Figure 5.4 shows vocalization timing when SW3~SW0 are changed during vocalization.

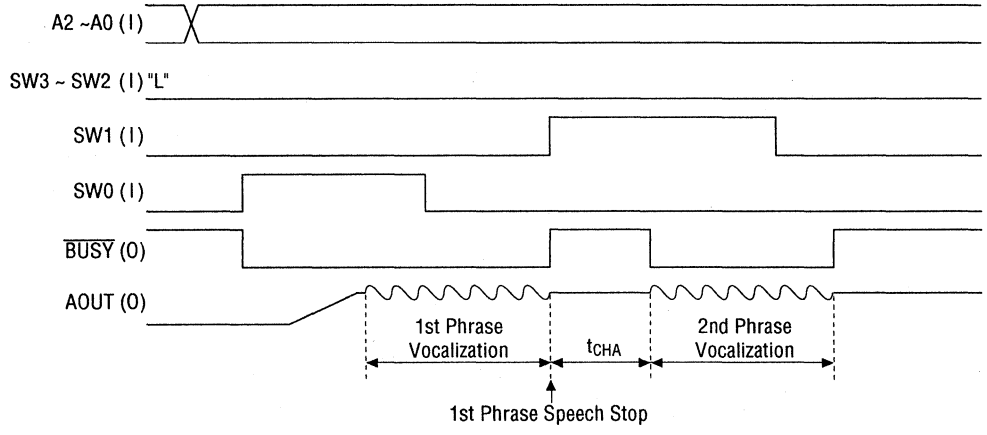


Figure 5.4 Vocalization Timing when SW3~SW0 Are Changed during Vocalization

If speech is started up at a non-used address in the user specified phrase, AOUT reaches 1/2 VDD, but speech is not vocalized. Figure 5.5 shows the timing.

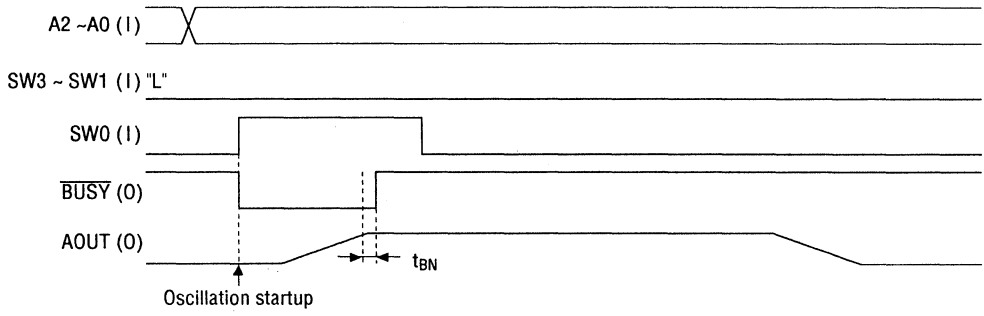


Figure 5.5 Timing when Speech is Started up at an Address except the User-Specified Phrase

In the complete SW interface, addresses (against SW3 ~ SW0) that do not start up exist without fail. When power is turned ON or when inputted to $\overline{\text{RESET}}$, the addresses set from SW3 to SW0 become the addresses that do not start up. Therefore, when the circuit consists of diode matrixes that use push switches, the maximum vocalized phrases become 120 phrases.

Combinations of A2 ~ A0 are 8 kinds.
When addresses of SW3 ~ SW0 that do not start up are 0000;

$2^7 - 8 = 120$ (phrases)

5.2 Random Vocalization Function

The random vocalization function randomly generates 31 types of addresses corresponding to 5 bits of the addresses of A0, and SW3~SW0 pins (except ALL "L") on the LSI, and vocalizes speech.

This means there is no external input to A0, SW3~SW0 pins. Since the A0 pin has no internal pullup/pulldown resistance, permanently set to "L" or "H".

Speech may not be vocalized if a phrase is not set to all 31 types of addresses. Caution is advised when creating ROM data.

For example, when 4 types of phrases, "sunny", "rainy", "cloudy", and "snowy" are vocalized, set the phrases shown in Table 5.1 to 31 types of addresses. The 4 types of phrases are then vocalized at random.

Table 5.1 Random Address Setup Example

A2, A1	A0, SW3 ~ SW0	Phrase
00	00001	Sunny
	00010	Rainy
	00011	Cloudy
	00100	Snowy
	00101	Sunny
	∫	∫
	11110	Rainy
	11111	Snowy

Random vocalization starts when the timing shown in Figure5.6 is input to the $\overline{RND}$ pin. A random address is determined by the "L" level time of the $\overline{RND}$ pin. When the LSI is in oscillation status random address is determined by the "H" level time of the pin. Random address is captured at the fall of the $\overline{RND}$ pin, and speech is vocalized. Therefore when power is turned ON, or when $\overline{RESET}$ is input, the phrase at fixed address "00001" is vocalized while a random counter remains an initial state, and a random phrase is vocalized at a second or later time.

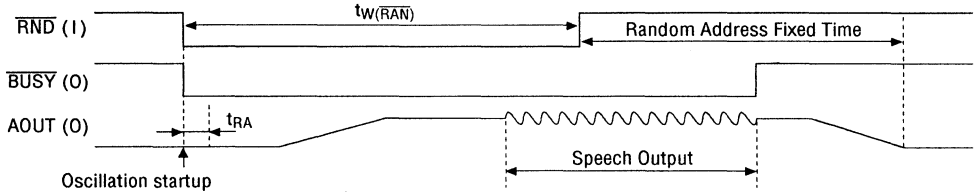


Figure 5.6 Random Address Capture

Table 5.2 Type of Address for Random Vocalization

A2, A1	A0, SW3 ~ SW0 (Note)	Code Description
00	00001 ∫ 11111	Random Vocalization Address (31 Types)
01	Same as above	Same as above
10		
11		

Note: Address(es) corresponding to A0, SW3~SW0 pins.

For a random address, 31 phrases can be set to each "00", "01", "10" and "11" of A2 and A1 respectively.

In random vocalizations, note that the 4 types of "0000000," "0100000", "1000000" and "1100000" in user specified phrases can not be used when ROM data is prepared.

By changing the A2 and A1 pins as in Table 5.2, probabilities or phrase combinations for 4 types of random vocalizations can be changed..

A random address is set by the "H" level time of the $\overline{\text{RND}}$ pin, therefore if the same pulse length is input by microcomputer, the random address fixed time becomes constant, and a random phrase may not be vocalized.

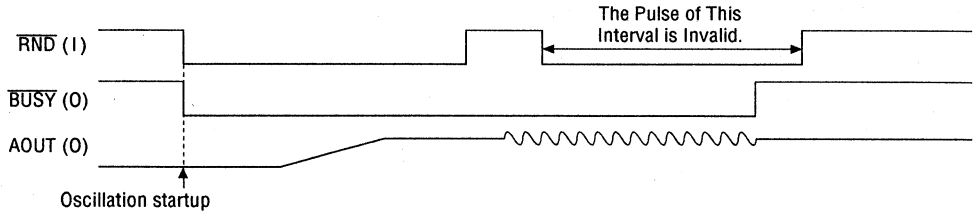


Figure 5.7 Timing when a Pulse is Input to the $\overline{\text{RND}}$ pin during Random Vocalization

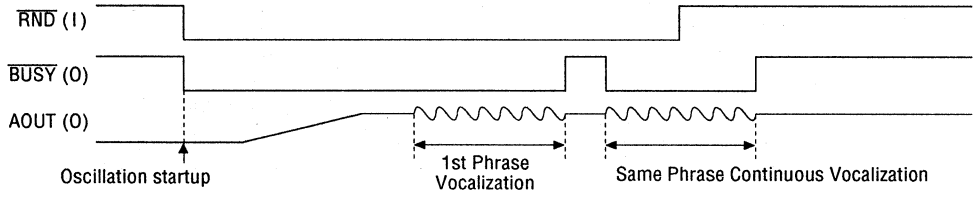


Figure 5.8 Repeat Vocalization Timing of Random Vocalization

As shown in Figure 5.7, if a pulse becomes trailig edge at the $\overline{\text{RND}}$ pin during speech vocalization ($\overline{\text{BUSY}}$ is "L" interval.), input to the $\overline{\text{RND}}$ pin during vocalization becomes invalid. If the $\overline{\text{RND}}$ pin is in "L" level and the $\overline{\text{RND}}$ pin is still in "L" level after the 1st phrase vocalization is over, as shown in Figure 5.8, the same phrase is vocalized repeatedly.

If SW3~SW0 are changed during random vocalization, speech during random vocalization stops, and speech of phrases that correspond to SW3~SW0 is vocalized.

Figure 5.9 shows the timing when SW3~SW0 are changed during random vocalization.

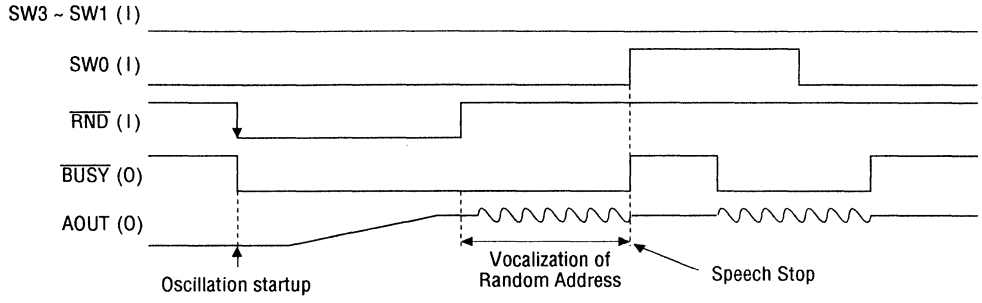


Figure 5.9 Timing when a Pulse is Input to SW0 pin during Random vocalization

Table 5.3 and Figure 5.10 show the address settings that quit random vocalization. These settings also stop vocalization when the "infinite repeat" command is in use under edit ROM.

Table 5.3 Address for Random vocalization and Addresses for Stop

A2, A1	A0, SW3 ~ SW0 (Note)	Code Description
00	00001 ⌇ 11111	Random Vocalization Address (31 Types)
01	00001	Stop Address

Note: Addresses corresponding to A0, SW3~SW0 pins.

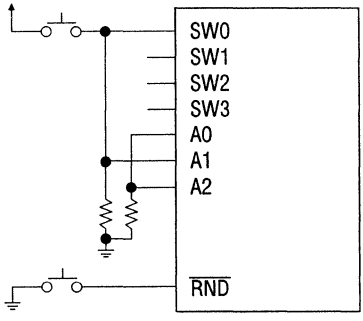


Figure 5.10 Circuit Example to Stop Random Vocalization

For example Table 5.3 shows that addresses other than random vocalization "0100001" are generated to stop vocalization.

A user specified address that is not used is used as a stop address, therefore the status can enter standby without vocalizing speech, also shown in Figure 5.5.

6. SAMPLING FREQUENCY

Sampling frequencies can be specified for each phrase in speech data of internal ROM. For channel synthesis, if channels 1 and 2 are regenerated at the same time, the channel 1 sampling frequency has priority.

For sampling frequency, the following 8 frequencies can be selected when creating speech data.

4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz

In standalone, RC oscillation and ceramic oscillation can be selected. If RC oscillation is selected however, 32.0 kHz can not be selected.

7. SPEECH VOCALIZATION TIME

Table 7.1 shows internal ROM configuration. The actual speech data ROM area is different from the indicated ROM capacity.

The speech data management area shown in Table 7.1 is about 6Kbits, and the edit ROM area includes 16Kbits.

Table 7.1 ROM Configuration

Speech Data Management Area
Editing ROM Area
Speech Data Area
Disabled Area

Use the following formula as a guide to compute speech vocalization time.

$$\text{Vocalization Time} = (\text{ROM Capacity} - 16 - 6) \times 1024 \times 255/256 \div \text{Bit Rate (kbps)}$$

For example, if data was created at a 4.0 kHz sampling using MSM6652 (288Kbit internal ROM), the vocalization time is

$$(288 - 16\text{-}6) \times 1024 \times 255/256 \div 16(\text{kbps}) = 16.9(\text{sec.})$$

8. CHANNEL STATUS

The $\overline{\text{BUSY}}$ pin outputs the status signals. It outputs "L" level when either channel 1 or 2 is synthesizing speech. "H" level is output when power is turned ON.

9. REGENERATION METHOD

The MSM6375 series has only the ADPCM regeneration method, however to support various speech MSM6650 has 3 types of regeneration methods: ADPCM, PCM and melody regeneration. Respective features and how to select are explained below.

9.1 ADPCM Method

With the ADPCM (Adaptive Differential Pulse Code Modulation) method, basic quantization width Δ is adaptively changed for each sampling, and is encoded to 4bit data each time. This further improves the follow-up properties to speech wave forms.

Conversion to ADPDM data is performed by the AR76-202 analysis tool.

If the ADPCM method is used for human voices, animal cries and natural tones, the speech data capacity becomes smaller.

9.2 PCM Method

The PCM method of MSM6650 uses an 8-bit straight binary format. Of the three methods, PCM is the best for follow-up properties to speech wave forms.

This method is appropriate for sound effects where wave forms sharply change, and for pulse shaped wave forms.

9.3 Melody Regeneration Method

The AR76-202 analysis tool supports melody regeneration system. The melody data can be composed by using the AR76-202. Therefore, unique sound can be created.

9.4 Bit Rate of Each Method

The bit rate shows the degree of data compression and the data amount to synthesize for 1 second. The bit rate is determined by the relationship between the sampling frequency and the data-amount-per-sample. The following formula is used.

Bit Rate (kbps) = Sampling Frequency (kHz) × Data-amount-per-sample (bit)

The bit rate of the three methods are compared below when the sampling frequency is 6.4 kHz.

1) ADPCM Method
   Bit Rate (kbps) = 6.4kHz × 4bit = 25.6 kbps

2) PCM Method
   Bit Rate (kbps) = 6.4kHz × 8bit = 51.2 kbps

3) Melody Regeneration Method
   With the melody regeneration method, the bit rate changes depending on each sound. The formula does not determine the bit rate changes. The average bit rate is 4 kbps.

9.5 The Regulations of Channel Synthesis about each Regeneration Methods

Melody regeneration and BEEP tones can not be regenerated in 2 channel side,the regeneration of channel synthesis about each regeneration Methods as follows table 9.1.

Table 9.1 The Regulations of channel Synthesis

1 Channel	2 Channel	Setting
ADPCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
ADPCM(0dB～-18dB)	ADPCM(0dB)	○ Note1)
ADPCM(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
ADPCM(0dB～-18dB)	PCM(0dB)	○ Note1)
ADPCM(0dB)	PCM(0dB～-18dB)	○ Note1)
ADPCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
ADPCM(0dB～-18dB)	SILENCE	○
MELODY(0dB)	ADPCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	ADPCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	MELODY(0dB～-18dB)	×
MELODY(0dB)	PCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	PCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	PCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
MELODY(0dB～-18dB)	SILENCE	○
PCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
PCM(0dB)	PCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
PCM(0dB～-18dB)	SILENCE	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	MELODY(0dB～-18dB)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	SILENCE	○
SILENCE	ADPCM(0dB～-18dB)	○
SILENCE	MELODY(0dB～-18dB)	×
SILENCE	PCM(0dB～-18dB)	○
SILENCE	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
SILENCE	SILENCE	○

Note1) In case of channel synthesis, confirm the voice quality with the MSM6650 evaluation board. Because occasionally there is possibility of straining the voice by recording level and synthsis phrases.

10. EDIT ROM

The role of edit ROM is to link phrases and build sentences, which makes an external microcomputer unnecessary. The conventional MSM6375 family could not link phrases and synthesis channels in standalone mode, but the MSM6650 family can using edit ROM.

For example: The phrase "Today's weather is...." is used to compare the MSM6375 family and MSM6650. With the MSM6375 family, individual data must be stored to phrase ROM (see Table 10.1) to vocalize each phrase in timing of once as "Today's weather is sunny", and "Today's weather is rainy".

On the other hand, the MSM6650 family can vocalize plural phrases at timing of once by having edit ROM functions. This means that "Today's weather is sunny" will be vocalized by merely specifying address [01] of Table 10.3 in the phrase ROM configuration shown in Table 10.3. If address [02] is specified, "Today's weather is rainy" will be vocalized.

Conventionally data must be repeatedly stored to phrase ROM to vocalize "Today's weather is....", but overlapped data is not required as shown in Table 10.2 by using edit ROM functions.

Table 10.1 Conventional Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's weather is sunny.
02	Today's weather is rainy.
03	Today's weather is sunny followed by cloudy, some areas are rainy.
∫	∫
7F	

Table 10.2 Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's
02	weather
03	is
∫	∫
10	sunny
11	cloudy
12	rainy
13	snowy
20	occasional
21	followed by
22	some areas are
∫	∫
7F	

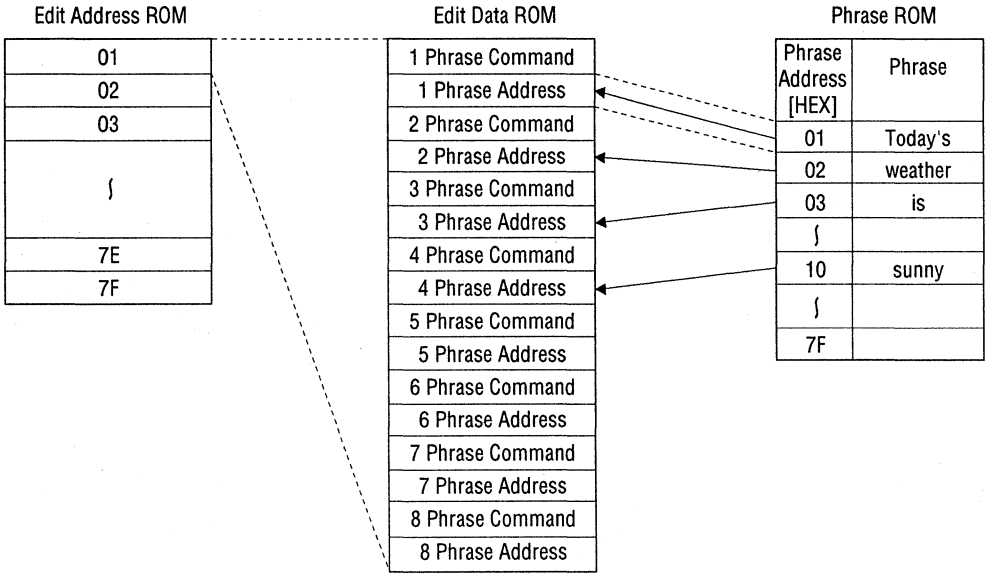
Table 10.3 Edit ROM Configuration

Address [HEX]	Edit Content [Max. 8 Phrases]
01	[01][02][03][10]
02	[01][02][03][12]
03	[01][02][03][10][21][11][22][12]
∫	∫
7F	

Edit ROM makes channel synthesis possible, a feature previously not available in standalone mode with the MSM6375 series. With edit ROM commands, phrase linking, channel synthesis, and "BEEP" tone or "silent" can be set.

A maximum of 8 phrases (16 bytes) can be set in 1 edit. Table 10.3 shows the configuration of edit ROM.

Table 10.4 Edit ROM Configuration



Edit address ROM can process a maximum of 127 user specified phrases. Table 10.4 shows the relationship between phrase ROM, edit data ROM, and edit address ROM.

Phrase ROM cannot be directly accessed if edit ROM is used.

Edit ROM can be setup using the previously mentioned AR76-202 analysis tool. For regeneration using edit ROM, regeneration may not be the one requested. Be certain to check the speech using either the analysis tool or MSM6650 of external ROM.

Figure 10.1 shows the flow chart when creating edit ROM.

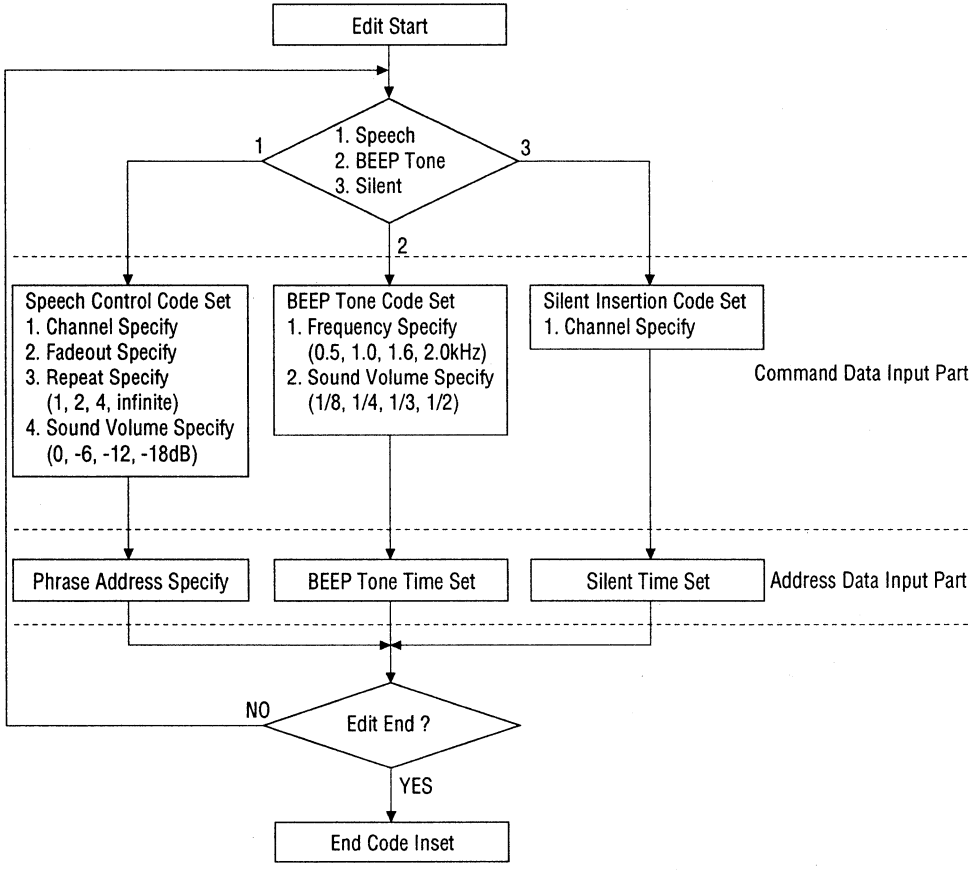


Figure 10.1 Edit Data ROM Creation Flow Chart

10.5 Edit ROM Commands

Table 11 shows the commands that can be set in edit ROM.

Table 10.5 List of Commands that can be Set in Edit ROM

O7	O6	O5	O4	O3	O2	O1	O0	Command
0	0	0	0	0	0	0	0	End Code
ch	0	1	0	0	0	0	0	Silence Insertion Code
1	1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
ch	1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

The commands of the 4 codes shown in Table 10.5 are explained below.

10.1.1 End Code

End code means that one edit data is completed. Although this is necessary at the end of one edit data, since the LSI can recognize the end of editing, it is unnecessary when the maximum number of phrases are used.

10.1.2 Silence Insertion Code

Silence insertion code inserts silence to each channel, reducing speech data.

O7	O6	O5	O4	O3	O2	O1	O0
ch	0	1	0	0	0	0	0

The channel to insert silence is specified in command data, and silence time is set in address data.

The channel to insert silence is set to "O7" command data. If "O7" is "H" channel 1 is set, if "L" channel 2 is set.

Silence time is set at the address settings of phrases shown in Table 10.4.

Minimum Silence Time ... 16.384 ms
Maximum Silence Time ... 2.1 sec.

The formula to set the silence time is shown below.

$t_{MU} = (2^6 \times (O6) + 2^5 \times (O5) + 2^4 \times (O4) + 2^3 \times (O3) + 2^2 \times (O2) + 2^1 \times (O1) + 2^0 \times (O0)) \times 16.384\text{ms}$

Table 10.6 Edit Data Example of Silence Insertion Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	0	1	0	0	0	0	0	Silence Insertion Code
2nd Byte	0	0	0	1	1	0	0	0	Silence Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 10.6, 393 ms of silence is inserted to channel 1.

10.1.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data.

The BEEP tone can be set only at channel 1.

To mix a BEEP tone and channel 2 vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz.

If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

The sound volume is set to O3, O2 and the frequency is set to O1, O0.

O7	O6	O5	O4	O3	O2	O1	O0
1	1	0	0	bl1	bl0	bf1	bf0

Tables 10.7 and 10.8 show the sound volumes and the frequencies that can be set.

Table 10.7 Sound Volume Settings

O3	O2	Sound Volume
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 10.8 Frequency Settings

O1	O0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

The BEEP tone time is set to the address setting of phrases shown in Table 10.4.

Minimum BEEP Tone Time ... 16.384 ms
Maximum BEEP Tone Time ... 2.1 sec.

The formula to set a BEEP tone time is shown below.

$t_{BE} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384ms$

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	0	0	1	1	0	1	BEEP Tone Code
2nd Byte	0	0	0	1	1	0	0	0	BEEP Tone Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 10.9, a 1.0 kHz BEEP tone is vocalized at a 1/2 amplitude sound volume at channel 1 for 393 mS.

10.1.4 Speech Control Code

Speech control code can set repeat and sound volume.

O7	O6	O5	O4	O3	O2	O1	O0
ch	1	1	sm	rp1	rp0	vl1	vl0

The channel is set at "O7". If "O7" is "H", channel 1 is set, if "L" channel, 2 is set. The speech control condition of each channel is set between O4 to O0.

1) Setting Number of Repeats

The number of repeats is set at O3 and O2, and can be selected from 4 types: 1, 2, 4 and infinite. If infinite is selected, repeat can be stopped by switching to another phrase.

Table 10.10 shows the relationship between O3, O2 and the number of repeats.

Table 10.10 Number of Repeats Settings

O3	O2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "O4" is set to "H", sound volume during repeat is attenuated from 1 to 1/2, 1/4 and 1/8. This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at O1 and O0. Table 10.11 shows the correspondence.

Table 10.11 Attenuation Volume Setting

O1	O0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound volume is 1/8 of speech data)

10.2 PCM Regeneration in Edit ROM

For PCM regeneration, edit data is set together with speech control code. All settable items in speech control code (channel, sound volume smoothing during repeat, number of repeats, and sound volume) can be set.

10.3 Melody Regeneration in Edit ROM

For melody regeneration, edit data is set together with speech control code. Channels however cannot be set. Channel 1 is fixed. Channel 2 mixing of melody regeneration/melody regeneration combination is not possible.

All settable items in speech control code can be set except channels.

10.4 Random Vocalization in Edit ROM

If the $\overline{\text{RND}}$ pin is used during random vocalization, the 1st edit phrase (consists of edit data ROM up to 16 bytes) is vocalized and the random vocalization of the 2nd edit phrase then starts continuously.

However, this occurs only when the channel setting of the 1st and 2nd edit phrase are the same, and when echo regeneration and channel 2 regeneration are not performed. For example, if the 1st edit phrase is echo regeneration, and the 2nd edit phrase channel 1 regeneration, as shown in Figure 10.2 (1), 2 edit phrases overlap.

To avoid this, insert silence to channel 1, as shown in Figure 10.2 (2), and set edit data ROM so that channels 1 and 2 end regeneration at the same time.

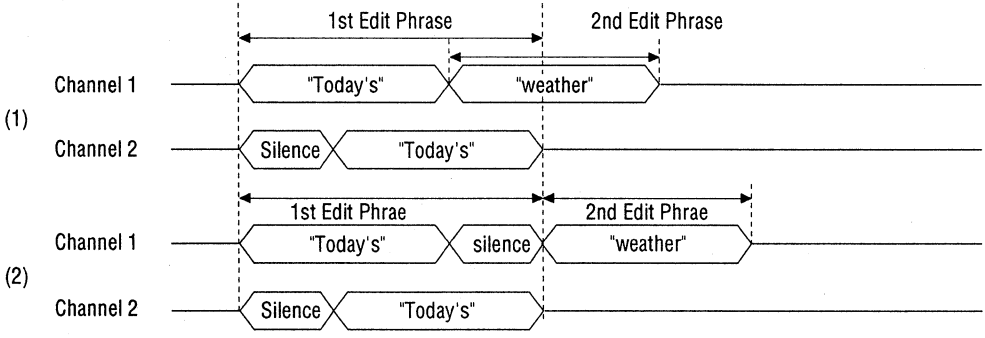


Figure 10.2 Example of Random Vocalization Timing

10.5 Channel 2 Mixing Function in Edit ROM

This function overlaps 2 phrases. By using edit ROM, it is easy to echo a phrase (echo regeneration) and to vocalize a phrase with a musical instrument sound or BGM (channel 2 regeneration).

10.5.1 Echo Regeneration

Echo regeneration delays and overlaps -6 dB attenuation (1/2 amplitude speech wave form of channel 1) to a speech wave form vocalized at channel 1.

Echo Regeneration of 1 Phrase

Using address [02] of phrase ROM, "weather", an echo regeneration edit data example is explained below.

Tabel 10.12 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
7th Byte	0	0	0	0	0	0	0	0	End code

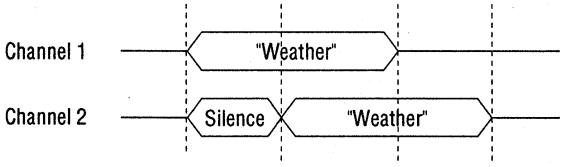
If edit data is set as in Table 10.12, "weather" is vocalized at channel 1, and is overlapped and vocalized from channel 2 with a -6 dB attenuated sound volume 98.3 ms. later.

When 2 phrases overlap set the attenuation of the speech control command with attention to sound volume.

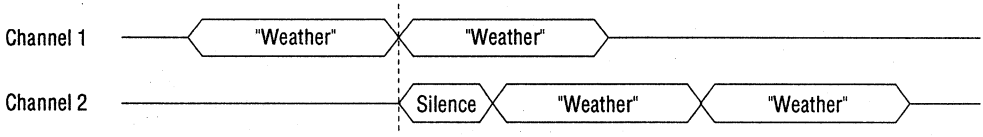
The silence time by silence insertion code is an element that influences the echo quality. Set the silence time so that the desired echo is created.

For channel synthesis in standalone, wave forms may be cramped due to the sound volume of the phrase. Check this with the AR76-202 analysis tool.

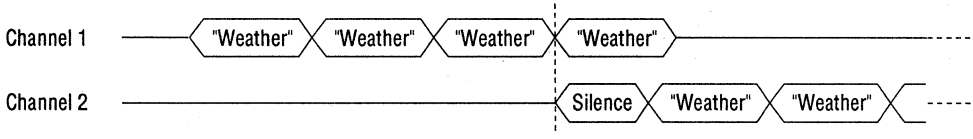
When performing echo regeneration set the number of repeats of the speech control command to 1. If 2, 4 or infinite is set, timing becomes as shown in Figure 10.3. This figure shows that the number of repeats of the 1st and 5th byte of edit data in Table 10.12 have changed.



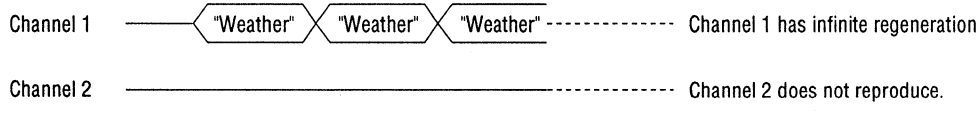
(1) Number of Repeats: 1



(2) Number of Repeats: 2



(3) Number of Repeats: 4



(4) Number of Repeats: infinite

Figure 10.3 Vocalization Timing of Echo Regeneration According to Number of Repeats

The vocalization timing, when the number of repeats of the speech control command is set for an edit data phrase, is explained below.

1 When number of repeats is set to 1

If the same channel is specified for the next phrase, vocalization of the next phrase starts when vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of vocalization.

2 When number of repeats is set to 2

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the second vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the second vocalization after the first vocalization ends.

3 When number of repeats is set to 4

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the fourth vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the fourth vocalization after the 3rd vocalization ends.

4 When number of repeats is set to infinite

The next phrase becomes invalid and is not vocalized regardless the channel specification.

Echo Regenerqation of Multiple Phrases

A maximum of 8 phrases (16 bytes) are set to one edit data ROM. Up to 3 phrases are possible for an echo regeneration with 16 bytes. Set the phrase ROM so that the number of phrases do not exceed four. Using "Today's", "weather" and "is" of the phrase ROM in Table 10.2 as an example, Table 10.13 shows a three phrase echo regeneration edit data example, and Figure 10.4 shows vocalization timing.

Table 19 Three Phrase Echo Regeneration Edit Data Example

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting repeat once, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	0	0	0	1	0	Phrae Address (02H "weather")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
13th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
14th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
15th Byte	1	1	1	0	0	0	1	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
16th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")

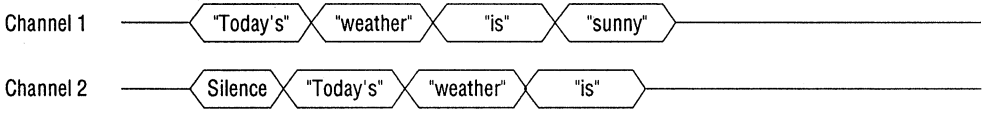


Figure 10.4 Vocalization Timing of a Three Phrase Echo Regeneration

For the echo regeneration of multiple phrases, set so that the sampling frequency of each phrase is the same. If a phrase with a different sampling frequency is mixed, the speech of channel 2 will become fast or slow because the sampling frequency of channel 1 has priority. Figure 10.5 shows the timing.

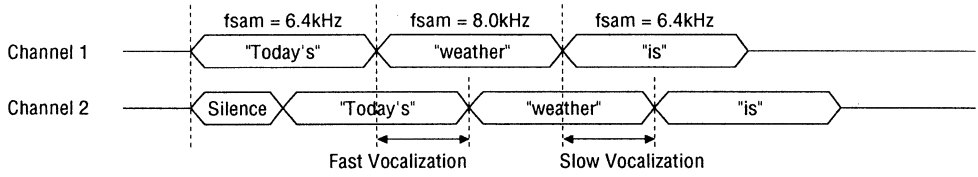


Figure 10.5 Vocalization Timing of Echo Regenerations with Different Sampling Frequencies

Echo Regeneration of an Arbitrary Phrase in Multiple Phrases

Table 10.14 shows an edit data example to apply echo to "is" in the four phrases of "Today's", "weather", "is" and "sunny".

Table 10.14 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	1	1	0	0	0	0	1	Silence Time (1.59 mS)
5th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting repeat once, -6 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (01H "weather")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	1	0	0	0	0	Phrae Address (10H "is")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")
13th Byte	0	0	0	0	0	0	0	0	End Code

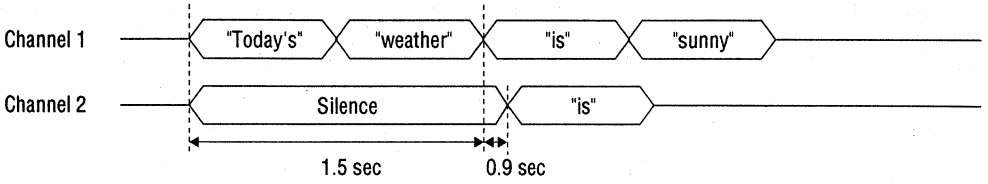


Figure 10.6 Vocalization Timing Using Edit Data of Table 10.14

As shown by the timing in Figure 10.6, "is" is echoed by setting the silence time, which is the addition of the vocalization time for "Today's" and "weather" and the delay time for echo to channel 2. If the silence time exceeds 2.1 sec, it is necessary to add a silence insertion setting to 2 bytes of edit data.

For the echo regeneration of one arbitrary phrase of multiple phrases, a maximum of 6 phrases are possible if the silence insertion setting is 2 bytes.

10.5.2 Two-channel Regeneration

Two-channel regeneration uses PCM, melody and ADPCM methods. Channel synthesis is possible with all combinations except a melody reregeneration/melody reregeneration combination. Melody regeneration is fixed to channel 1. The sampling frequency of phrases to be overlapped must be the same.

Figures 10.7~10.10 show the vocalization timings of two-channel regeneration.

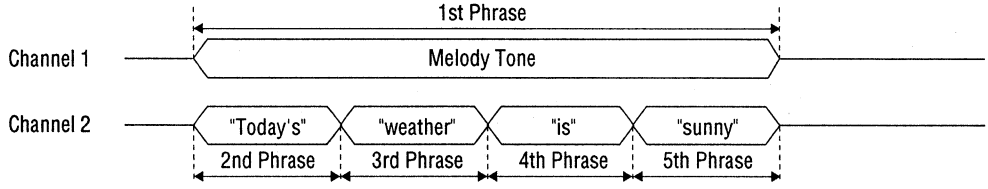


Figure 10.7 Example of Four Phrase Channel Synthesis Timing with Melody Tone as BGM

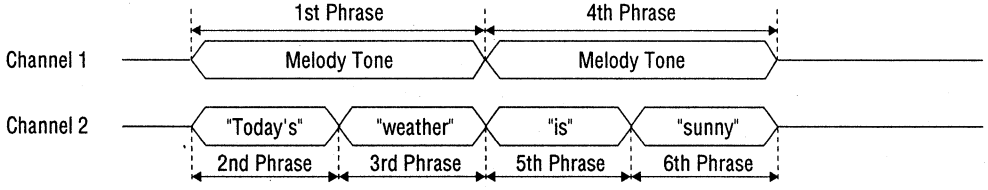


Figure 10.8 Example of Four Phrase Channel Synthesis Timing with Melody Tone and 1st and 4th Phrases as BGM

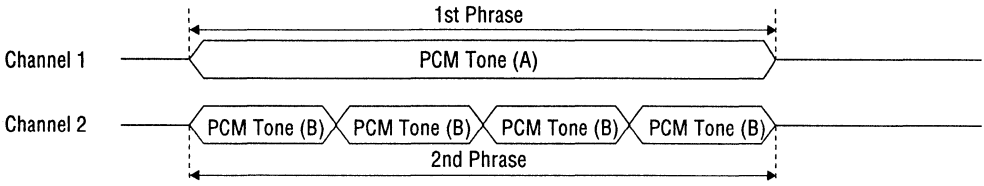


Figure 10.9 Example of Channel Synthesis between PCM Main Melody Tone (A) and PCM Rhythm Tone (B) with 4 Repeats

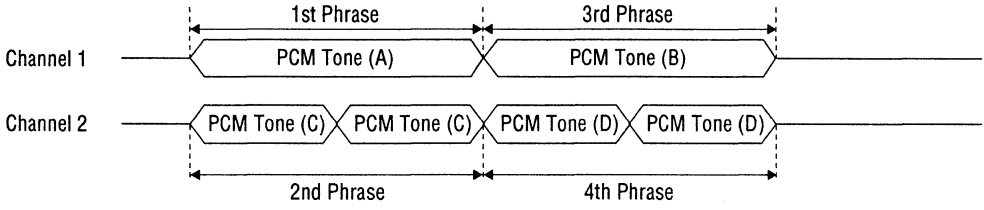


Figure 10.10 Example of Channel Synthesis between PCM Main Melody Tone (A) (B) and PCM Rhythm Tone (C) (D) with 2 Repeats

11. STANDBY CONVERSION

When standby conversion "YES" is selected by the MASK option, if the next phrase is not started up within 0.2 sec. after speech ends, the LSI enters standby status and all operation stops. If restarted, it takes about 100 mS from start up to speech start because the "pop noise" countermeasure circuit is in opration .

If standby conversion "NO" is selected by the MASK option, the LSI does not enter standby status even if speech is over. Current is flowing since AOUT output remains at about 1/2 VDD and oscillation is in operation. If started up speech starts in about 350 µs to enter standby status when standby conversion "NO" is selected, the $\overline{\text{RESET}}$ pulse must be input.

If the $\overline{\text{RESET}}$ pulse is input, the AOUT output level instantaneously changes to GND level, causing pop noises.

12. SPEECH OUTPUT

In standalone mode speech is output via an internal low pass filter. Table 12.1 shows output level of AOUT pin. This filter consists of switched capacitors. Table12.2 shows the relationship between sampling frequencies and cutoff frequencies.

Table 12.1 Output level of AOUT pin

Regeneration Method	Most Lowest Level	Center Level	Most Highest Level
ADPCM	About 0.15 × VDD	About 0.5 × VDD	About 0.95 × VDD
PCM	0.25	0.5	0.75
Melody	0.25	0.5	0.75
BEEP Tone	0.25	0.5	0.75

Table 12.2 Cutoff Frequencies of Low Pass Filter

Sampling Frequency (fsam)	Cutoff Frequency (fcut)
4.0kHz	About 1.8kHz
5.3kHz	About 2.6kHz
6.4kHz	About 2.6kHz
8.0kHz	About 3.2kHz
10.6kHz	About 4.2kHz
12.8kHz	About 5.1kHz
16.0kHz	About 6.4kHz
32.0kHz	About 12.8kHz

13. RC OSCILLATION

Figure 13.1 shows an-external circuit diagram using RC oscillation

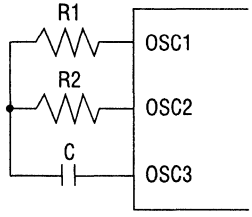


Figure 13.1 RC Oscillation

13.1 Determine of RC Constants

The RC oscillation frequency characteristics are shown in Figure 13.2.If fosc is set to 256 kHz,

R1=100kΩ, R2=30kΩ, C=30pF

when choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R2 as wsll as the process variations of the LSI.

13.2 Fluctuation of RC oscillation frequencies

When using a 30kΩ R2 , the error due to process variations of the LSI is maximum ±4% so flat the fluctuation of RC oscillation frequency when using a capacitance (C) of ±1% accuracy (R2) of ±2% accuracy is maximum±7% apporocimately.

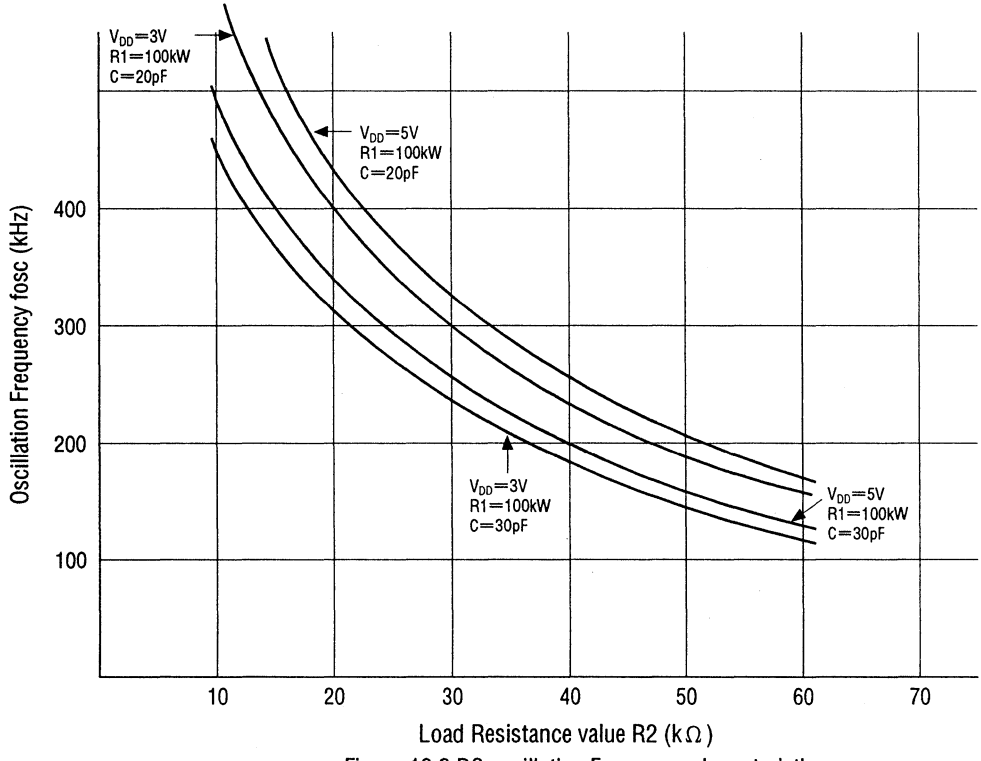


Figure 13.2 RC oscillation Frequency eharacteristics

14. CERAMIC OSCILLATION

Figure 14.1 shows an external circuit diagram using a ceramic oscillaton.

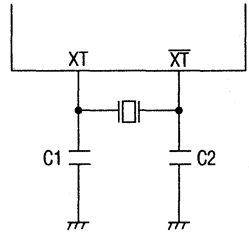


Figure 14.1 External circuit diagram

Figure 14.2 and 14.3 show external circuit diagrams using a cermic oscillator, CSA4.09MGU and CST4.09MGWU made by Murata Seisakusho Co., ltd

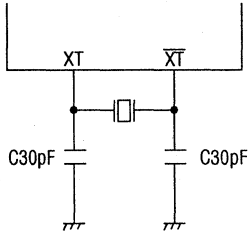


Figure 14.2 CSA4.09MGU

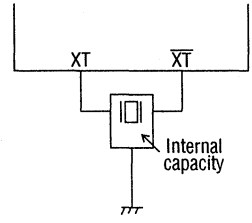


Figure 14.3 CST4.09MGWU

Figure 14.4 shows an extend circuit diagram using a cermic oscillator , PBRC 4.00MSA/MKS/MWS made by Kyocera Co., ltd.

Note) In case of using a oscillator, 4.00MHz, vocalization speed is low about 2% than AR76-202 analysis tool and evaluation board.

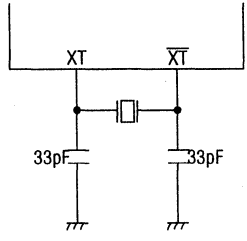
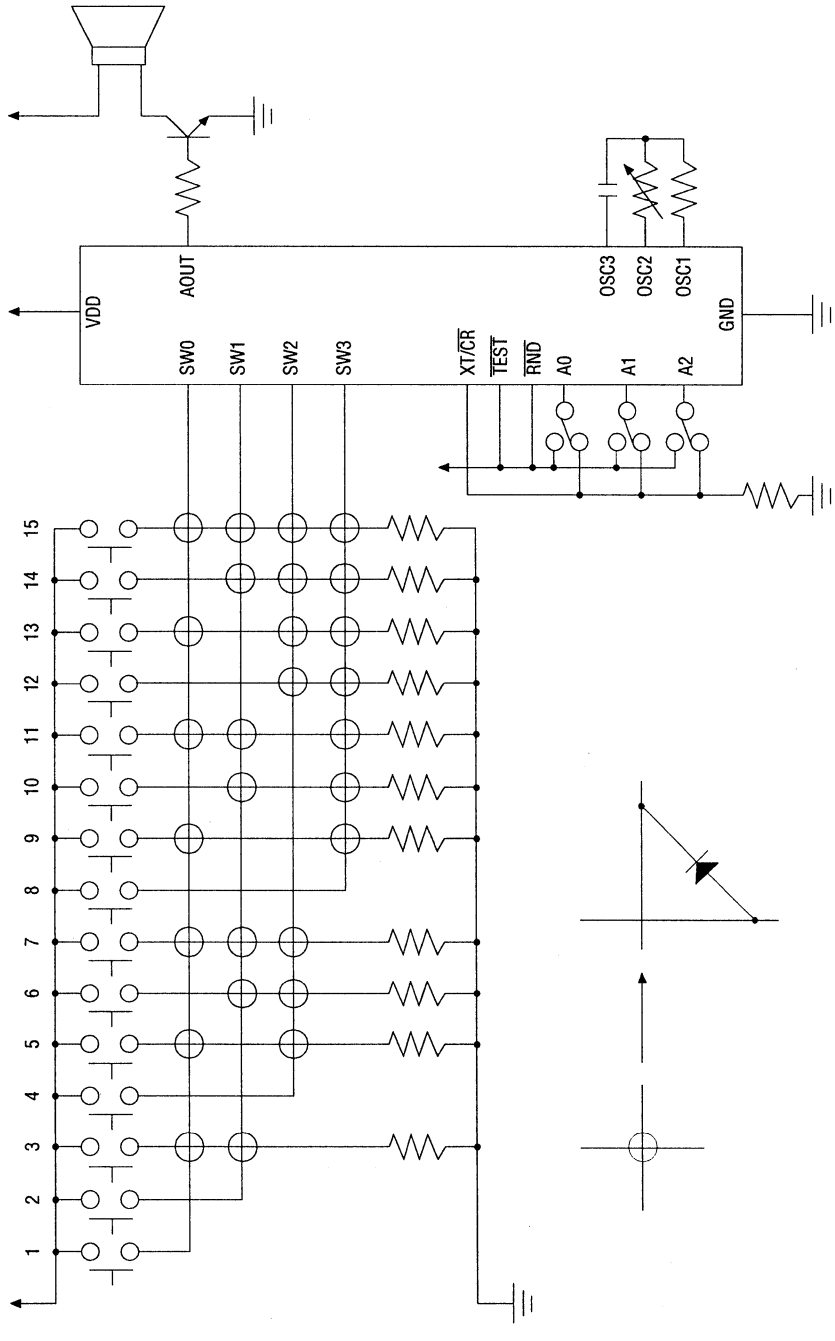
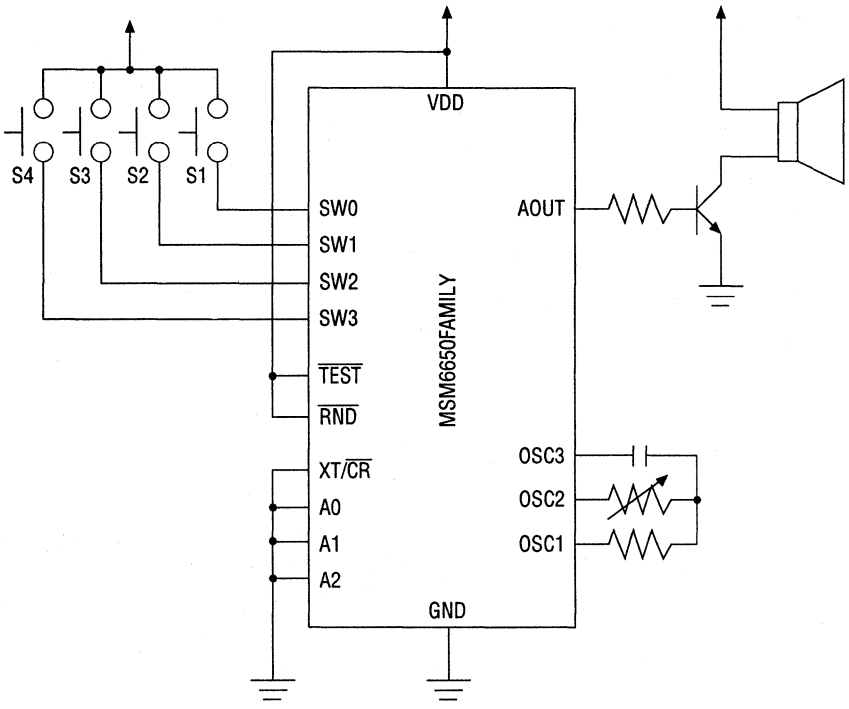


Figure 14.4 PRBC 4.00 MSA/MSK/MWS

APPLICATION CIRCUIT EXAMPLE



Application Circuit Example to Speech-output 15 Phrases by Switching



Example of Application Circuit to Output 4 Phrases by Switch

Corresponding Table between Switches and Sound Generation Addresses

	A2	A1	A0	SW3	SW2	SW1	SW0	ADR
S1	0	0	0	0	0	0	1	01
S2	0	0	0	0	0	1	0	02
S3	0	0	0	0	1	0	0	04
S4	0	0	0	1	0	0	0	08

(2) MICROCOMPUTER INTERFACE

FEATURES

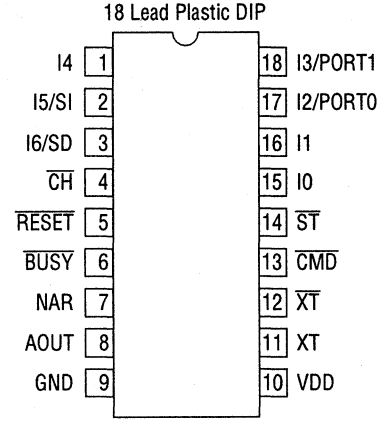
Type	ROM Capacity	Maximum Vocalization Time				
		fs=4.0kHz	fs=6.4kHz	fs=8.0kHz	fs=16.0kHz	fs=32.0kHz
MSM6652	288Kbit	16.9sec	10.5sec	8.4sec	4.2sec	2.1sec
MSM6653	544Kbit	31.2sec	19.5sec	15.6sec	7.8sec	3.9sec
MSM6654	1Mbit	63.8sec	39.9sec	31.9sec	15.9sec	7.9sec
MSM6655	1.5Mbit	96.5sec	60.3sec	48.2sec	24.1sec	12.0sec
MSM6656	2Mbit	129.1sec	80.7sec	64.5sec	32.2sec	16.1sec

(Actual speech ROM area is less 22 Kbit)

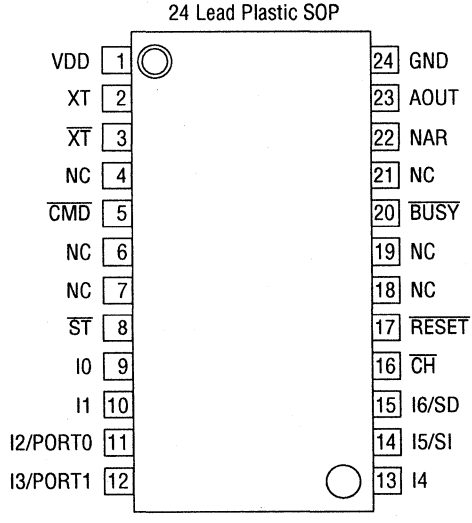
ROM custom
4-bit ADPCM method/8-bit PCM method
Melody function
Edit ROM function
2-channel mixing function
Fadeout function (4-step change of sound volume)
Serial input/parallel input can be selected
Internal BEEP tone : BEEP tones of 0.5 kHz, 1.0 kHz, 1.6 kHz and 2.0 kHz can be generated by specification code.
Sampling frequencies : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0kHz, 32.0kHz
Maximum number of phrases : 127 Phrases
Internal 12-bit D/A converter
Internal LPF attenuation factor : -40 dB/oct
Internal standby function
Package : 18-pin DIP (DIP18-P-300)
: 24-PIN SOP (SOP24-P-430-VK)
: Chip

PIN CONFIGURATION

(Top View)

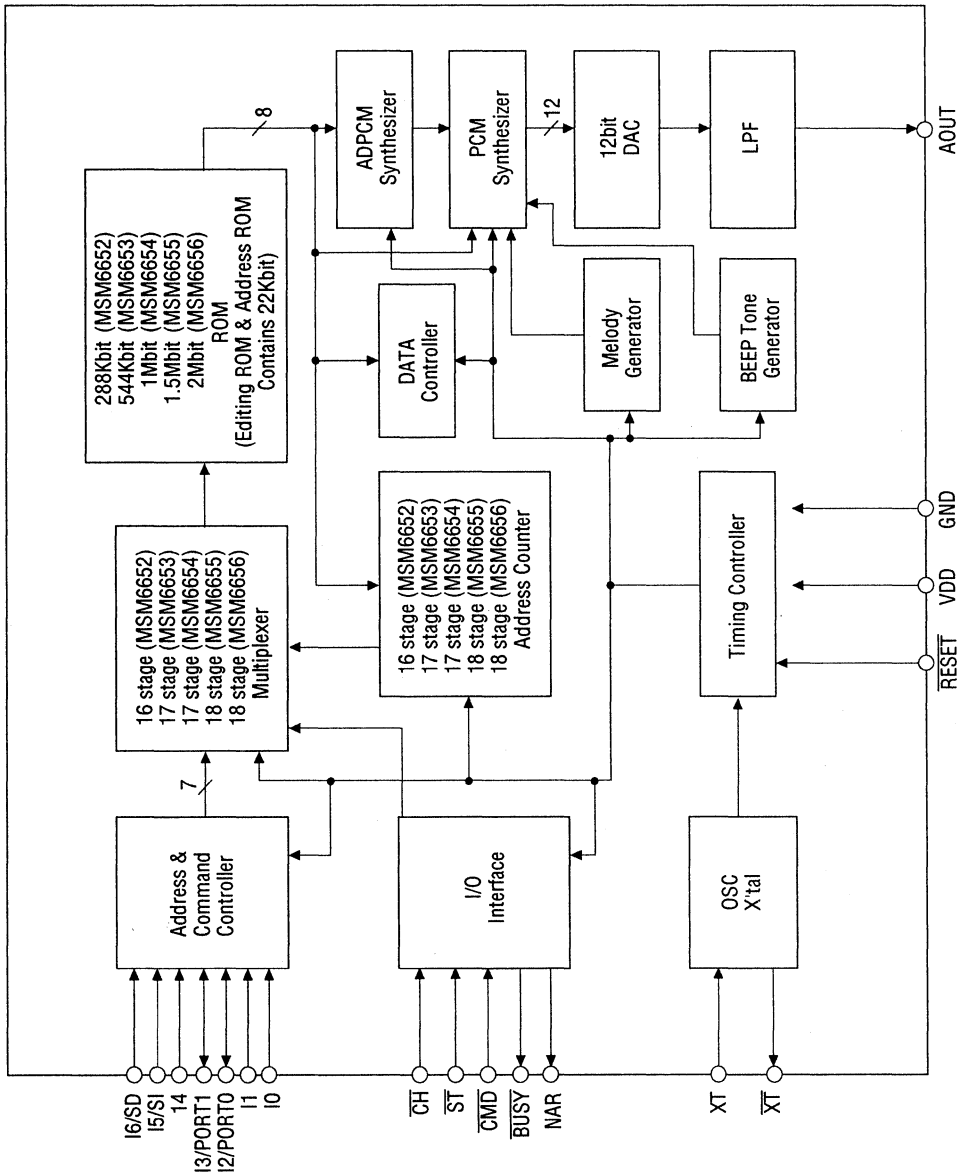


Note: Applicable to MSM6652-XXXRS, MSM6653-XXXRS, MSM6654-XXXRS, MSM6655-XXXRS and MSM6656-XXXRS



Note: Applicable to MSM6652-XXXGS-VK, MSM6653-XXXGS-VK, MSM6654-XXXGS-VK, MSM6655-XXXGS-VK and MSM6656-XXXGS-VK

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operation Range

(GND = 0V)

Parameter	Symbol	Condition	Limits			Unit
Power Supply Voltage	V_{DD}	DAC output	+2.4 ~ +5.5			V
		LPF output	+2.7 ~ +5.5			V
Operating Temperature	T_{op}	–	-40 ~ 85			°C
Original Oscillation Frequency	fosc	–	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-200	-90	-30	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2 (Note)	I_{IL2}	Internal pullup resistance pin	30	90	200	µA
Operating Current Consumption	I_{DD}	–	–	6	10	mA
Standby Current Consumption	I_{DS}	–	–	–	10	µA
DA Output Relative Accuracy	$\lvert V_{DAE} \rvert$	When DA output selected	–	–	40	mV
DA Output Impedance	R_{DAO}	When DA output selected	15	25	35	kΩ
LPF Load Resistance	R_{AOUT}	When LPF output selected	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	When LPF output selected I_F=100µA	–	1	3	kΩ

DC Characteristics

(V_{DD} = 3.1V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	2.7	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	2.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-100	-30	-10	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2 (Note)	I_{IL2}	Internal pullup resistance pin	10	30	100	µA
Operating Current Consumption	I_{DD}	–	–	4	7	mA
Standby Current Consumption	I_{DS}	–	–	–	1	µA
DA Output Relative Accuracy	$\lvert V_{DAE} \rvert$	When DA output selected	–	–	20	mV
DA Output Impedance	R_{DAO}	When DA output selected	15	25	35	kΩ
LPF Load Resistance	R_{AOUT}	When LPF output selected	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	When LPF output selected, I_F=100µA	–	1	3	kΩ

Note: Applicable to $\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{ST}}$ and $\overline{\text{CH}}$ terminals.

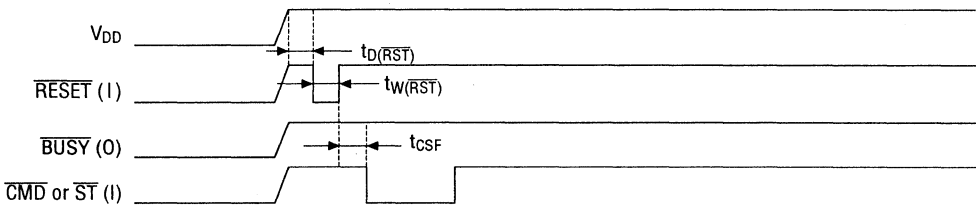
AC CHARACTERISTICS

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

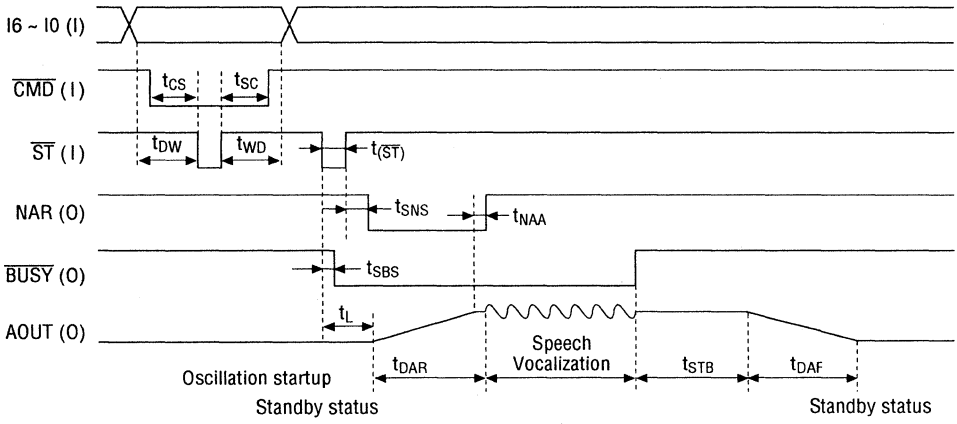
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{W(\overline{RST})}$	–	10	–	–	µS
$\overline{\text{ST}}$ Input Pulse Width	$t_{(\overline{ST})}$	–	0.35	–	2000	µS
Data Set Time	t_{DW}	–	1	–	–	µS
Data Hold Time	t_{WD}	–	1	–	–	µS
$\overline{\text{CMD}}$ Setup Time	t_{CS}	–	1	–	–	µS
$\overline{\text{CMD}}$ Hold Time	t_{SC}	–	1	–	–	µS
$\overline{\text{CH}}$ Setup Time	t_{CHS}	–	1	–	–	µS
$\overline{\text{CH}}$ Hold Time	t_{SCH}	–	1	–	–	µS
Serial Clock Pulse Width	$t_{W(SCK)}$	When using serial input option	0.35	–	–	µS
Serial Data Setup Time	t_{SDS}	When using serial input option	1	–	–	µS
Serial Data Hold Time	t_{SSD}	When using serial input option	1	–	–	µS
$\overline{\text{BYSY}}$ Output Time (1)	t_{SBS}	–	–	–	10	µS
$\overline{\text{BUSY}}$ Output Time (2)	t_{BN}	When fs = 8kHz	350	375	400	µS
$\overline{\text{BUSY}}$ Output Time (3)	t_{BF}	–	–	–	64	mS
NAR Output Time (1)	t_{SNS}	–	–	–	10	µS
NAR Output Time (2)	t_{NAA}	When fs = 8kHz	350	375	400	µS
NAR Output Time (3)	t_{NAB}	When fs = 8kHz	350	375	400	µS
NAR Output Time (4)	t_{NAC}	When fs = 8kHz	350	375	500	µS
DA Converter Change Time	t_{DAR}	–	60	64	68	mS
LPF Stable Time	t_L	–	6	8	10	mS
Standby Conversion Time (after speech ends)	t_{STB}	–	0.15	0.20	0.25	S

TIMING CHART

1.When Power is Turned ON

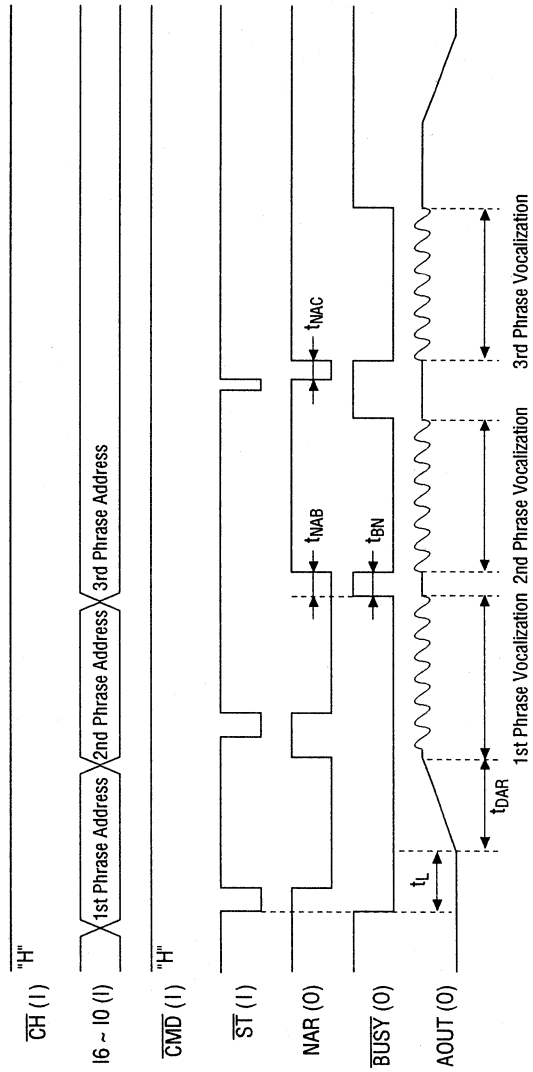


2.When LSI Starts Up and is in Standby Status

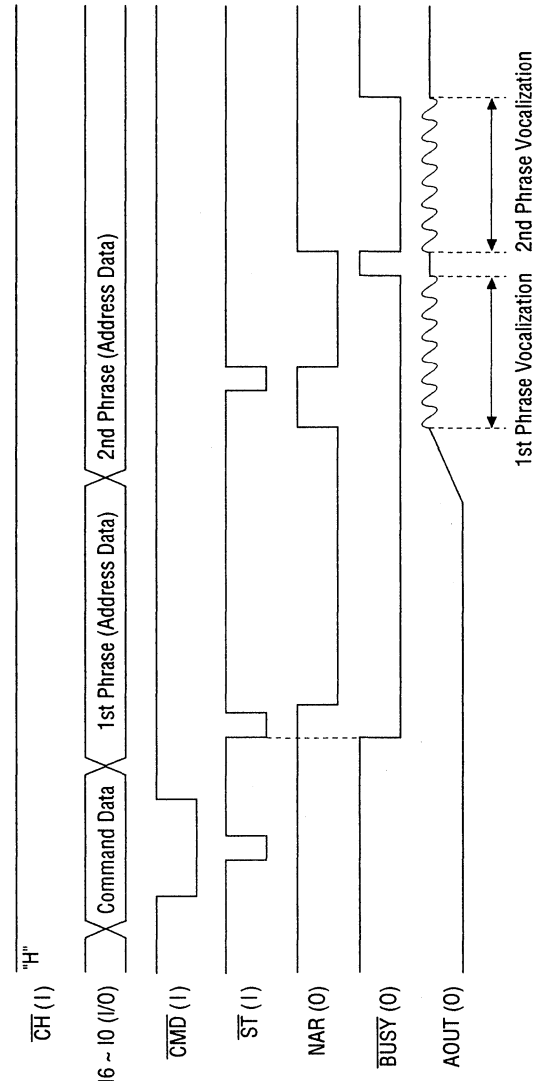


3.Channel 1 Regeneration Timing Chart

when External Command is not used (Parallel Input)

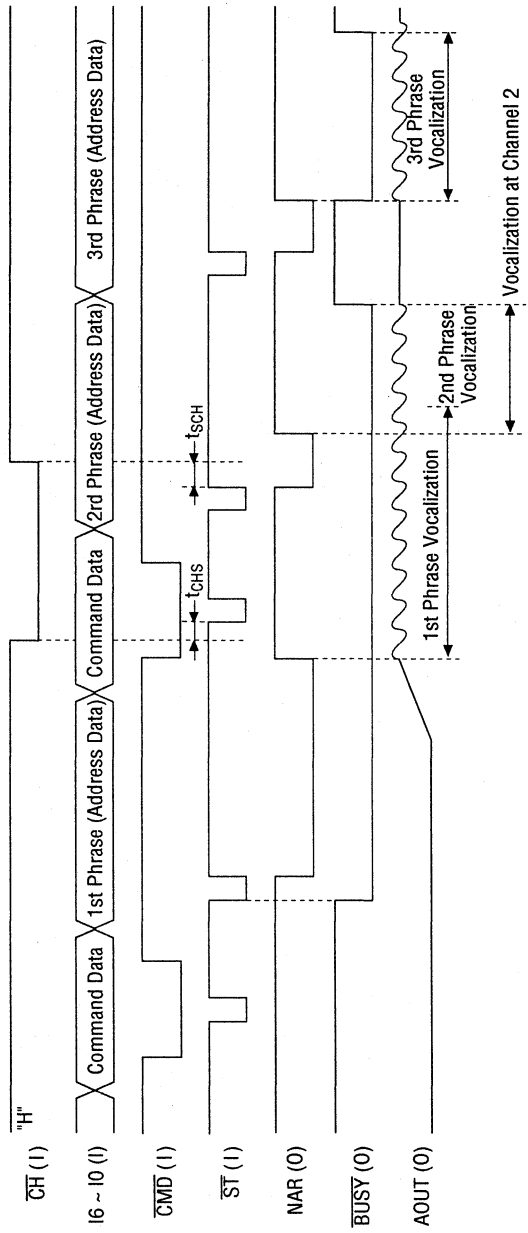


4.Channel 1 Regeneration Timing Chart when External Command is used (Parallel Input)



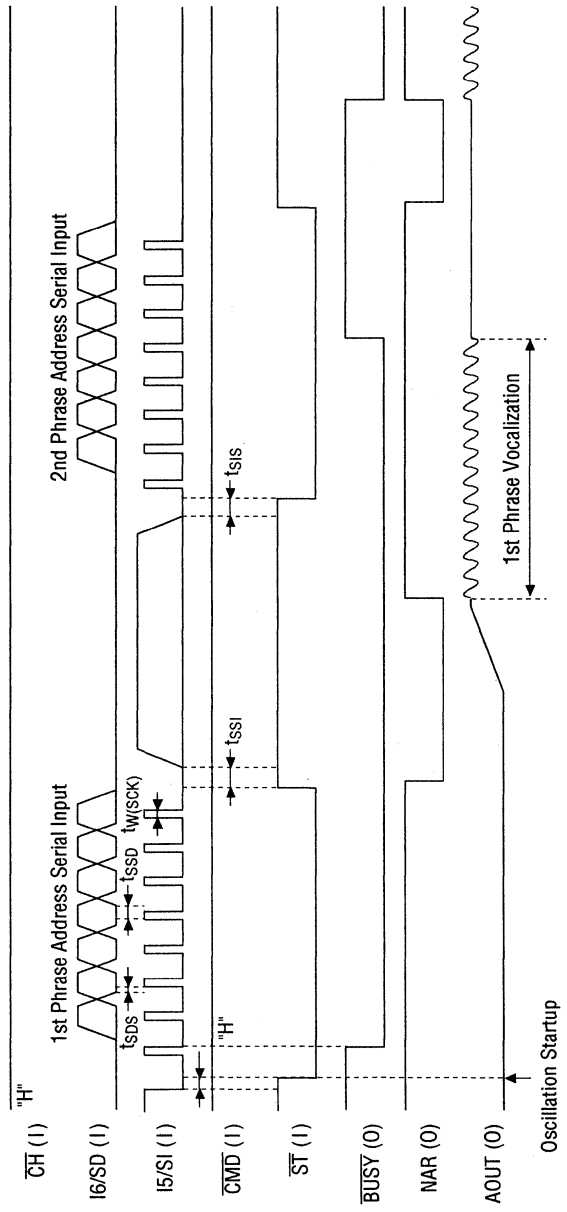
If a command is set externally the status set is maintained until the next command is set. Therefore, if the 1st and 2nd phrases are vocalized at the timing shown above, speech for both phrases is first vocalized in the status set by that command. To vocalize command content that was changed, be certain to input command data before inputting address data. The command input can be continuously set many times until address input. However, the setting of the command inputted last becomes valid (common with 1 and 2 channel regenerations).

5.Channel 1, Channel 2 Regeneration Timing Chart when External Command is used (Parallel Input)



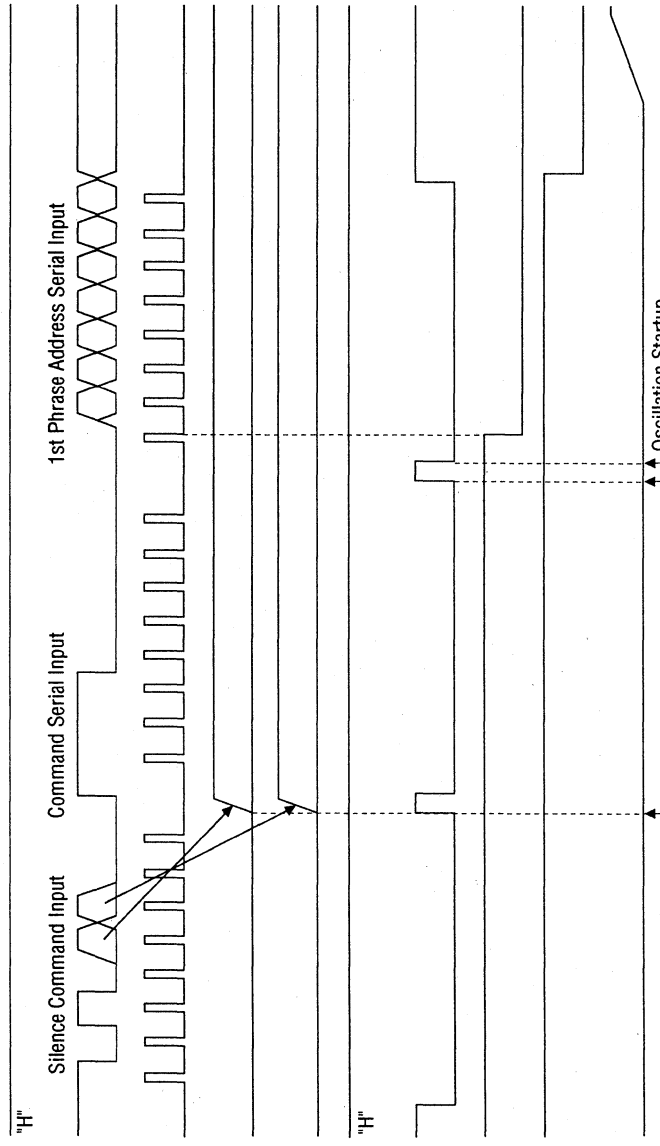
Since command data is maintained independently, If speech is started up at channel 1 without a command setting, speech is vocalized by the same command set at the 1st phrase.

6.Regeneration Timing Chart when External Command is not used (Serial Input)



In serial input, data is transferred to the LSI when the ST signal rises after serial data is input.
SD is captured at the former edge of SI.

7.Regeneration Timing Chart when External Command is used (Serial Input)



In serial input, port output can be set by a command setting. Since a port output command and internal command are shared, if a command is set for port output, set the command for speech again to input address data. If address data is input without setting the command, the LSI recognizes it as silence insertion code. The command input can be continuously set many times until address input. However, the setting of the command inputted last becomes valid (common with 1 and 2 channel regenerations).

PIN DETAILS

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	LSI enters standby status if "L" is input. Oscillation then stops, AOUT output changes to GND, and status returns to intial status. LSI has internal power ON reset. Startup power within 1 mS to operate power ON reset correctly. If not, apply $\overline{\text{RESET}}$ pulse when power is turned ON. This pin has internal pullup resistance.
$\overline{\text{BUSY}}$	O	Outputs "L" during vocalization. At "H" level when power is turned ON.
NAR	O	$\overline{\text{CMD}}$, $\overline{\text{ST}}$ input becomes effective when NAR is at "H" level. If CH pin is in "H" level, NAR becomes a channel 1 status signal. If in "L" level NAR becomes a channel 2 status signal. NAR signal indicates whether resisters I6 to I0 address of address/command controller (see block diagram) is in open status. "H" level indicates open status. NAR is in "H" level when power is turned ON.
AOUT	O	Analog speech output pin. DA converter output or LPF output can be selected by a command input.
GND	–	Ground pin
VDD	–	Power pin
XT	I	Ceramic oscillator connection pin. Pin has internal 0.5 to 5MΩ feedback resistance between XT and $\overline{\text{XT}}$. Input from this pin when using external clock.
$\overline{\text{XT}}$	O	Ceramic oscillator connection pin. Set to open to use external clock.
$\overline{\text{CMD}}$	I	Command input and option setting control pin. Command and option input is enabled if $\overline{\text{ST}}$ pin is set to "L" level when $\overline{\text{CMD}}$ pin is in "L" level. Set to "H"level when $\overline{\text{CMD}}$ is not used and when using serial input interface. This pin has internal pullup resistance.

Pin Name	I/O	Function
$\overline{ST}$	I	Speech synthesis starts at fall of $\overline{ST}$, I6 to I0 addresses are captured at rise of $\overline{ST}$. Input $\overline{ST}$ when NAR of channels 1 and 2 status signals are "H". This pin has internal pullup resistance.
$\overline{CH}$	I	Channel control signal. Channel 1 input is in "H" level, channel 2 input is in "L" level. This pin has internal pullup resistance.
I6/SD	I	Command and user specified phrase input pin when parallel input is optionlly selected. A serial data (command and address) input pin when serial input is optionally selected.
I5/SI	I	Command and user specified phrase input pin when parallel input is optionlly selected. A serial clock input pin when serial input is optionally selected.
I4	I	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, leave this pin at "L" level. This pin has internal pulldown resistance.
I3/PORT1	I/O	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, this pin becomes a port output pin. Output from the port varies by command input from the microcomputer.
I2/PORT0	I/O	Command and user specified phrase input pin. when parallel input is optionally selected. When serial input is optionally selected, this pin. becomes a port output pin. Output from the port varies by command input from the microcomputer.
I1,I0	I	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, leave this pin at "L" level. This pin has internal pulldown resistance.

FUNCTION DETAILS

Parallel input or serial input can be selected for the microcomputer interface. Selection should be done when making ROM data.

1. VOCALIZATION CODE SPECIFICATION

The user can specify a maximum of 127 phrases. Table 1.1 shows the settings by I6 to I0.

Table 1.1 User Specified Phrases

I6 ~ I0	Code Details
0000000	Stop Code
0000001 { 1111111	User Specified Phrase (127 Phrases)

2. INTERNAL ROM USAGE DISABLED AREA

Usage of the last 3 bytes of the internal ROM is disabled as shown in Table 2. Do not use the last 3 bytes accordingly when analyzing speech.

For instance, do not specify those models (i.e. MSM6653) other than the MSM6652 in using the analysis tool AR76-202 when making EPROM of the MSM6652.

Table 2.1 shows the addresses that are disabled.

Table 2.1 Internal ROM Layout and Disabled Area

Type	Speech Data Area	Disabled Area
MSM6652	00B00 ~ 08FFC	08FFD, 08FFE, 08FFF
MSM6653	00B00 ~ 10FFC	10FFD, 10FFE, 10FFF
MSM6654	00B00 ~ 1FFFC	1FFFD, 1FFFE, 1FFFF
MSM6655	00B00 ~ 2FFFC	2FFFD, 2FFFE, 2FFFF
MSM6656	00B00 ~ 3FFFC	3FFFD, 3FFFE, 3FFFF

Note: Addresses are in hex mode.

3. PULLUP/PULLDOWN RESISTANCE

$\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{ST}}$ and $\overline{\text{CH}}$ pins have internal pullup resistance. I6 to I0 pins do not have internal pullup/pulldown resistance.
At serial input option, I4, I1 and I0 pins have internal pulldown resistance.

4. MODE SETTING

In microcomputer interface mode, two option selection methods are available; i.e. the mask option to be set at making ROM data and the command option by command setting.

In mask option, either parallel input or serial input of commands and phrase addresses can be selected. However, when the mask option is selected, no change can be made once the option is selected while making ROM data.

The command option can select three items. Table 4.1 shows selectable options.

Table 4.1 Option Item List

No.	Item	Selection		Remarks
1	Standby Conversion	Yes	No	If standby conversion YES is selcted, status enters standby unless the next user specified phrase is input within 0.2 sec. after speech ends.
2	AOUT Output	LPF Output	DAC Output	
3	Maximum amplitude of 1 phrase	0 ~ VDD	1/4 VDD ~ 3/4 VDD (1/2 amplitude)	Maximum amplitude at 1 phrase

An option is set as in Table 4.2 when power is turned ON.

Table 4.2 Option when Power is Turned ON

Standby Conversion	AOUT Output	Amplitude for 1 Phrase
YES	LPF Output	0 ~ V_{DD}

To change an option that is already set use command again. If the $\overline{\text{RESET}}$ terminal is set to "L" level, the option returns to the status when power was turned ON (Table 4.2).

After setting the option, be certain to input the speech, silence and BEEP tone commands, then startup.

Figures 4.1 and 4.2 show the option setting timing, and Tables 4.3 and 4.4 show the option correspondences.

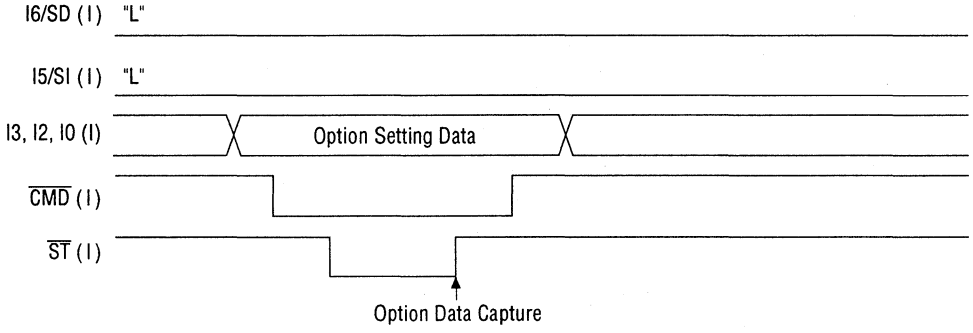


Figure 4.1 Option Setting Timing (during Parallel Input)

Table 4.3 Correspondence between Options and I3, I2, I0

	I3	I2	I0
	AOUT Output	Standby Conversion	Amplitude of 1 Phrase
"0" Data	LPF	YES	0 ~ V_{DD}
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4V_{DD}

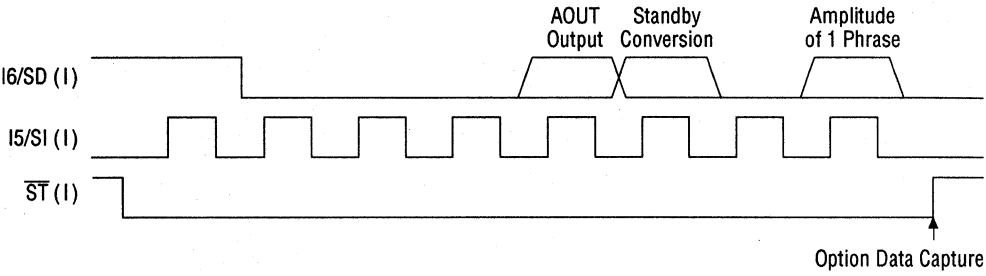


Figure 4.2 Option Setting Timing (during Serial Input)

Table 4.4 Correspondence between Option and Serial Data

	AOUT Output	Standby Conversion	Amplitude of 1 Phrase
"0" Data	LPF	YES	0 ~ V_{DD}
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4V_{DD}

5. MICROCOMPUTER INTERFACE MODE

External command settings are enabled with the microcomputer interface. However, if edit ROM is used, the command settings of channel 1 are disabled.

Figures 5.1 and 5.2 show the command input and address input method when using the microcomputer interface.

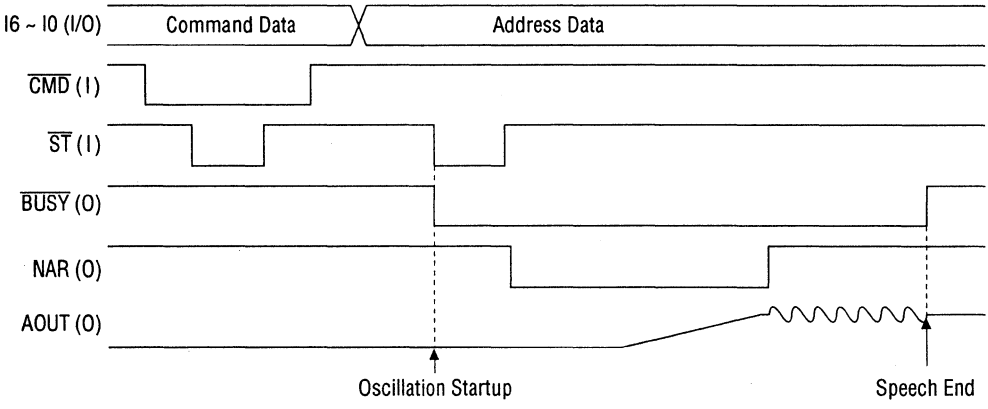


Figure 5.1 Command, Address Input Timing (Parallel Input)

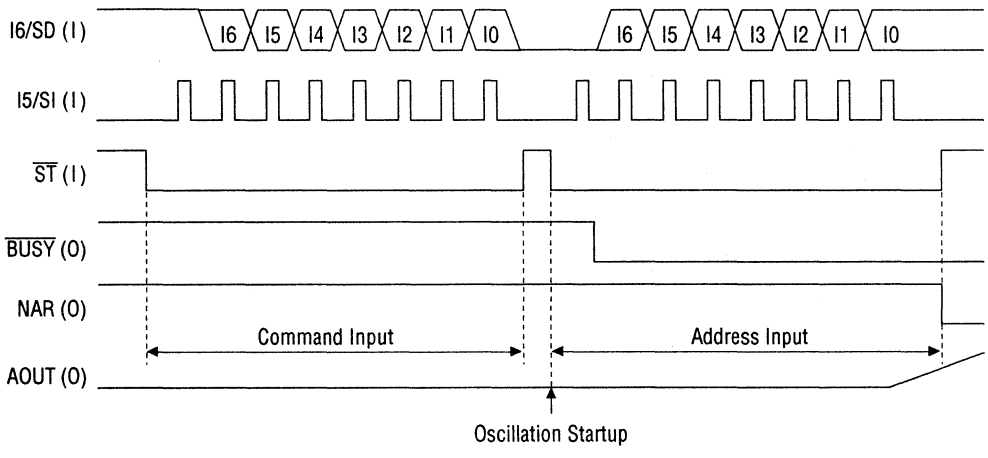


Figure 5.2 Command, Address Input Timing (Serial Input)

In microcomputer interface serial input, command data and address data are distinguished by the initial data input serially. If the initial data is "H", it is judged as command data, if "L", it is judged as address data.

Input command data and address data after inputting the command and address judgment data as initial data. Figures 5.3 , 5.4 and 5.5 show the external input flow.

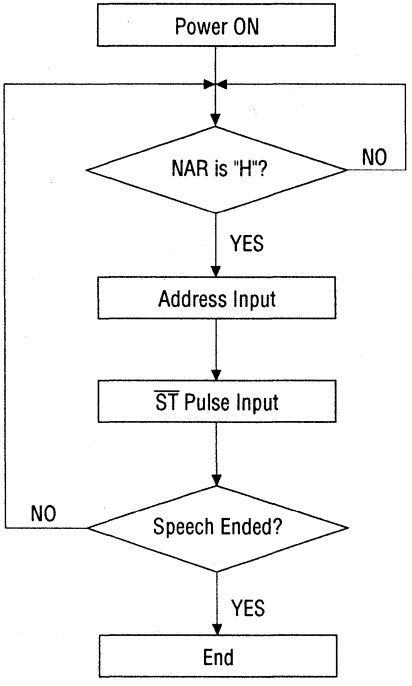


Figure 5.3 Input Flow Chart when Command is not set

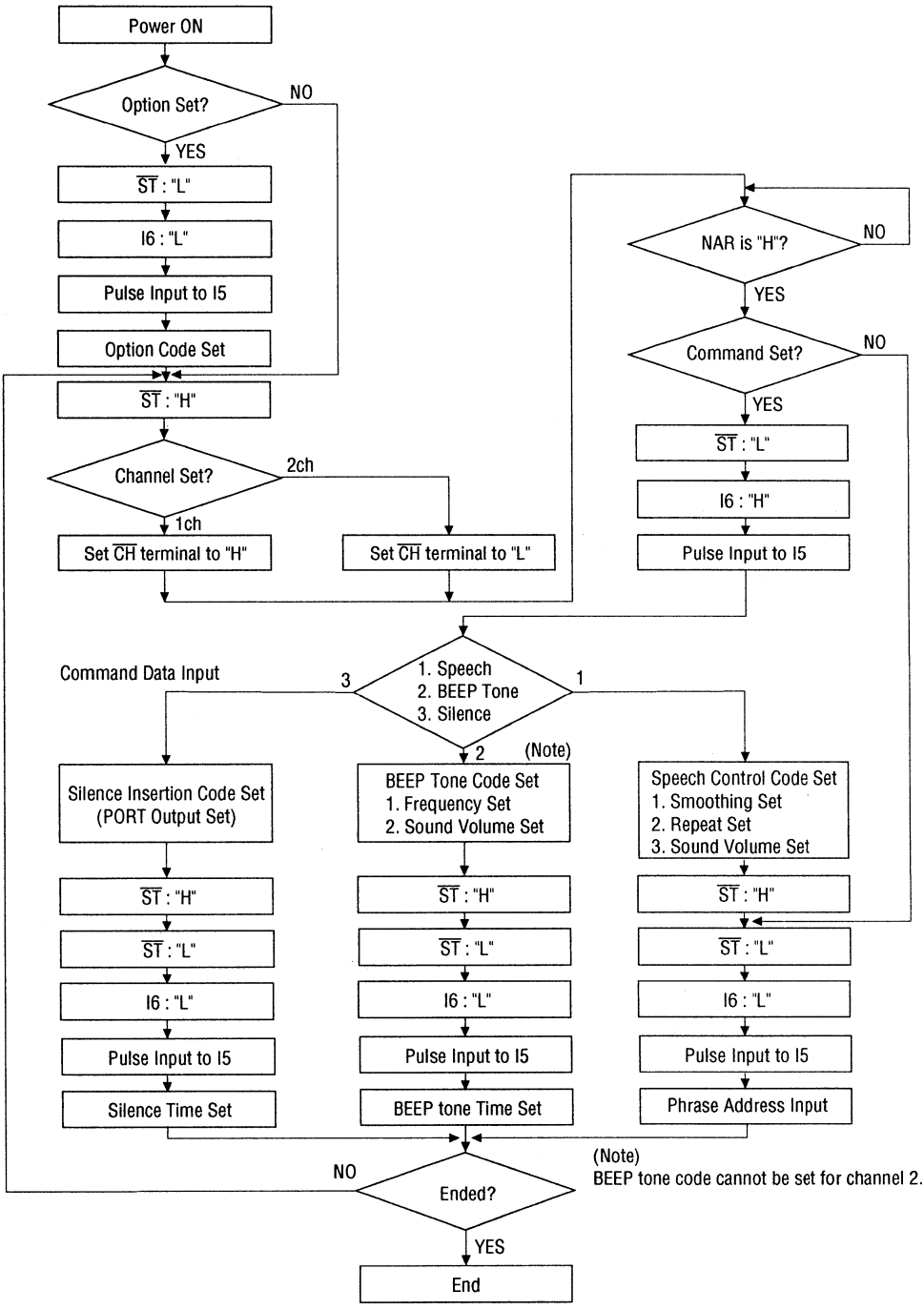


Figure 5.4 Parallel Input Flow Chart when External Command is used.

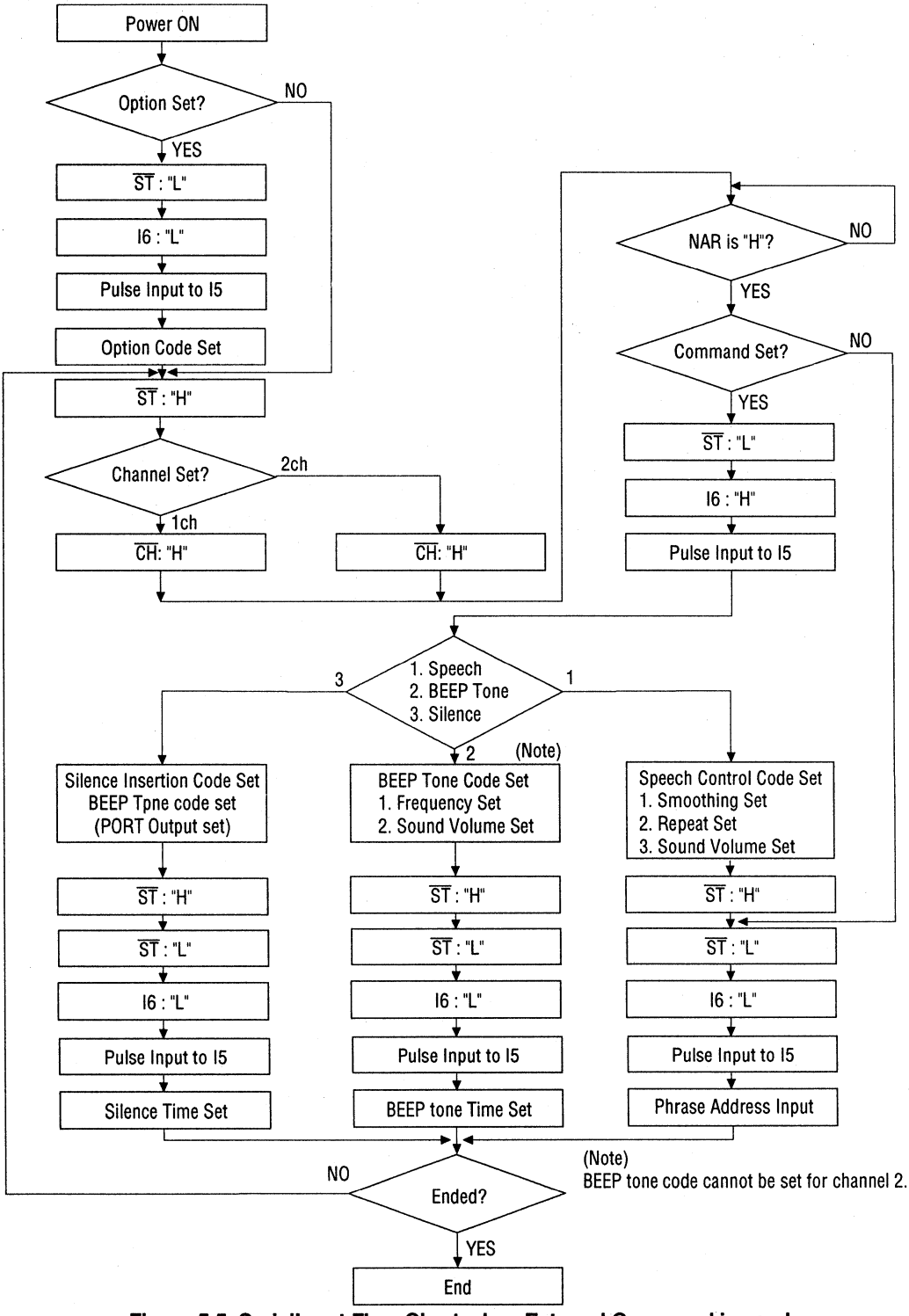


Figure 5.5 SerialInput Flow Chart when External Command is used

6. COMMAND DATA

Table 6.1 shows the conditions that can be set by command data. Command data is set with I6 to I0. In serial input, input data corresponding to I6 to I0 serially as shown in Figure 5.2.

Table 6.1 Command Setting Content List

I6	I5	I4	I3	I2	I1	I0	Command Content
0	0	0	oa	os	0	ov	Option Setting
0	1	0	p1	p0	0	0	Silence Insertion Code
1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

Command data is set to "1100000" when power is turned ON.

6.1 Option Setting Code

An option can be set by command. Since an option is set as in Table 4.2 when power is turned ON, use this command to change an option. Once an option is set, it remains effective either until power is shut OFF or until the $\overline{\text{RESET}}$ signal is input.

When an option is set, input speech, silence and BEEP tone commands again by command input and set address (phrase, silence time and BEEP tone time).

Table 6.2 shows the options that can be set.

Table 6.2 Option Correspondence Table

	I3	I2	I0
	AOUT output	**Standby Conversion**	**Amplitude of 1 Phrase**
"0" Data	LPF	YES	0 ~ VDD
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4 V_{DD}

Show the Figure 4.2 for command option setting timing chart .
Options can be set anytime, but if set during vocalization, AOUT output impedance and acorstic pressure may change .

6.2 Silence Insertion Code

Silence code inserts silence to each channel. Speech data can be reduced by inserting silence externally.

I6	I5	I4	I3	I2	I1	I0	
0	1	X	p1	p0	X	X	X: Don't care

Command data specifies to insert silence, address data sets the silence time. The $\overline{CH}$ terminal inserts silence to either channel 1 or 2.

Silence time is set by address data (I6 to I0).

Minimum Silence Time: ... 16.384 ms
Maximum Silence Time: ... (128 - 1) × 16.384 ms=2.1 sec.

Figure 6.1 shows the channel 1 silence insertion setting timing.

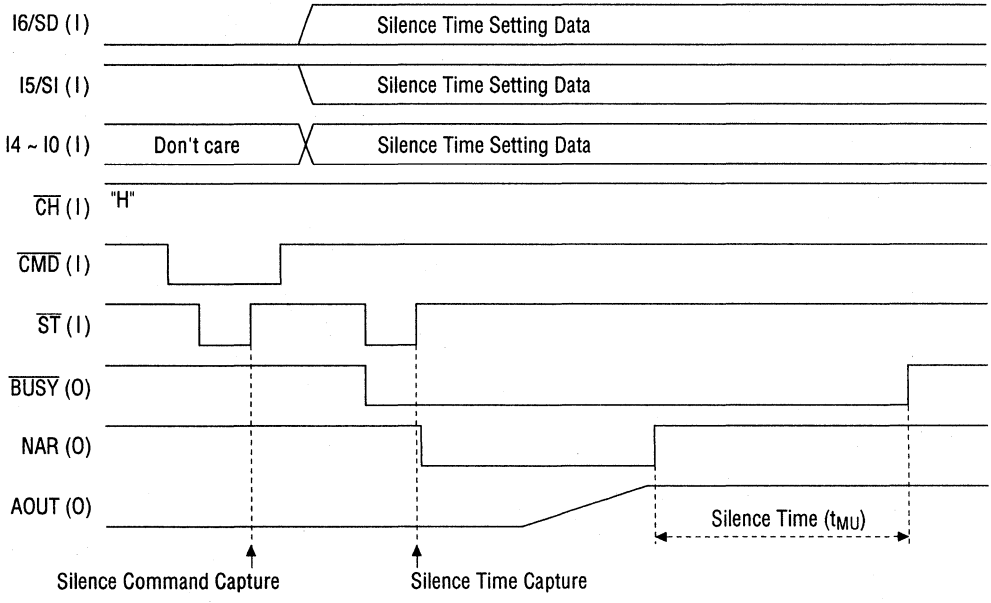


Figure 6.1 Channel 1 Silence Setting Timing (Parallel Input)

For example, if silence time setting data shown in Figure 6.1 is set as (I6 to I0) = ("0011000"), the silence time (t_{MU}) becomes

$$(2^6 \times 0+2^5 \times 0+2^4 \times 1+2^3 \times 1+2^2 \times 0+2^1 \times 0+2^0 \times 0) \times 16.384 \text{ mS} = 393.216 \text{ ms}$$

The formula to set silence time is shown below.

$$t_{MU} = (2^6 \times (I6)+2^5 \times (I5)+2^4 \times (I4)+2^3 \times (I3)+2^2 \times (I2)+2^1 \times (I1)+2^0 \times (I0)) \times 16.384 \text{ ms}$$

The channel 2 silence insertion setting timing becomes as shown in Figure 6.2.

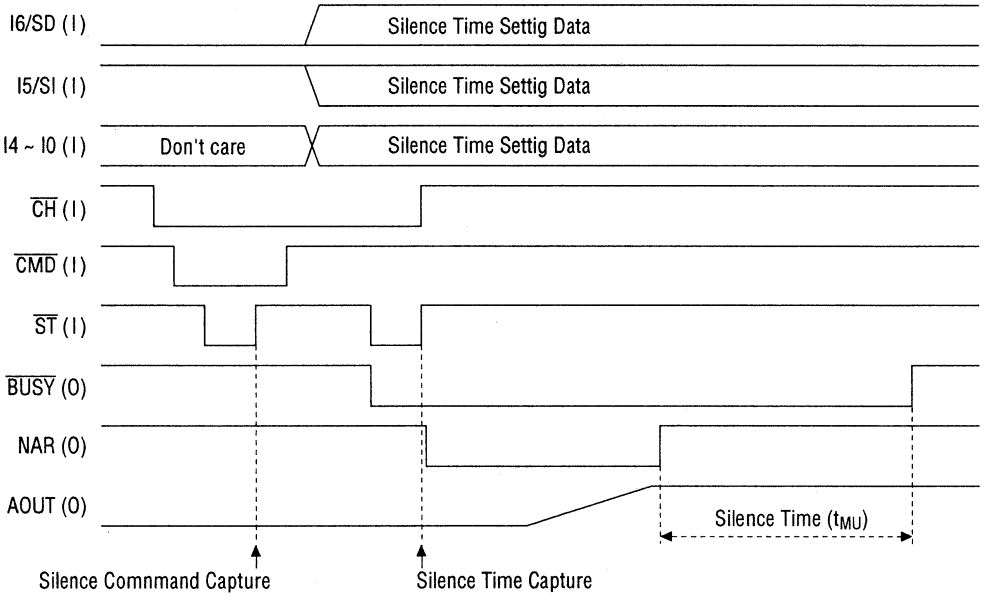


Figure 6.2 Channel 2 Silence Setting Timing (Parallel Input)

In serial input, the port output signals from I3/PORT1, I2/PORT0 terminals is also controlled by silence insertion code. I3/PORT1, I2/PORT0 terminals are in "L" level when power is turned ON, and when the $\overline{\text{RESET}}$ signal is input.

If speech synthesis starts after setting the port output, first set the port output by silence insertion code, then input the speech vocalization code and set the address. Figure 6.3 shows the timing. If it is necessary to set the port again after setting the port, since a port cannot be set continuously, input the BEEP tone code or speech vocalization code after first setting the port, then set the port again.

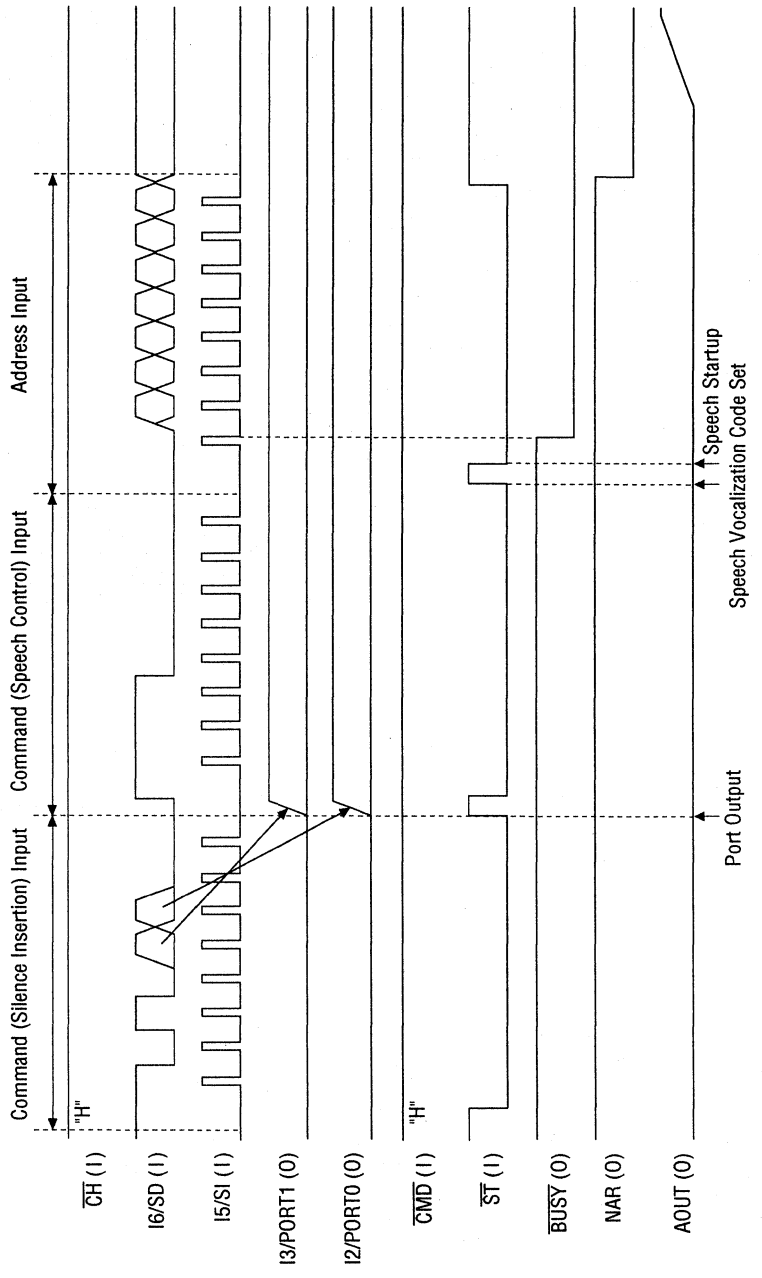


Figure 6.3 Port Output and Command, Address Setting Timing (during Serial Input)

6.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data.

The BEEP tone can be set only at channel 1. Do not select the BEEP tone at channel 2.

To mix a BEEP tone and channel 2, vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz. If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

I6	I5	I4	I3	I2	I1	I0
1	0	0	bl1	bl0	bf1	bf0

The sound volume is set to I3, I2 pins, and the frequency is set to I1, I0 pins. Tables 6.3 and 6.4 show the sound volumes and the frequencies that can be set.

Table 6.3 Sound Volume Settings

I3	I2	Sound Volume (Note 1)
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 6.4 Frequency Settings

I1	I0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

(NOTE1)

If 1/2 amplitude of channel 1 is set, and if the maximum amplitude is set to 1/2 V_{DD} as an option the sound volume of BEEP tone becomes 1/4 V_{DD}.

The BEEP tone time is set by address data (I6 to I0).

Minimum BEEP Tone Time ..... 16.384 ms
Maximum BEEP Tone Time ..... (128 - 1) × 16.384 mS = 2.1 sec.

Figure 6.4 shows BEEP tone setting timing.

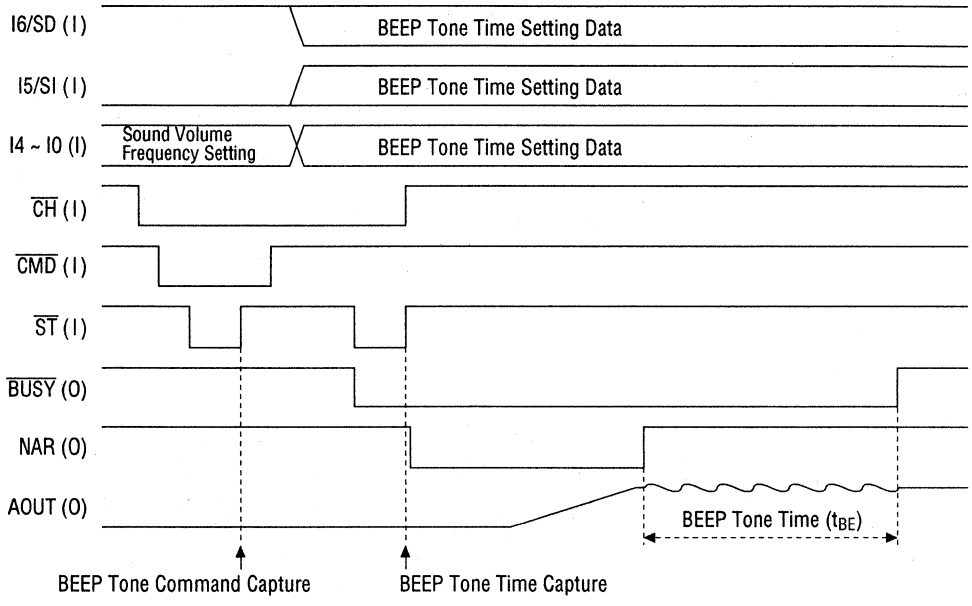


Figure 6.4 BEEP Setting Timing (during Parallel Input)

For example, if the BEEP tone time setting data shown in Figure 6.4 is set as (I6 to I0) = ("0011000"), the BEEP tone time (t_{BE}) becomes

$$(2^6 \times 0+2^5 \times 0+2^4 \times 1+2^3 \times 1+2^2 \times 0+2^1 \times 0+2^0 \times 0) \times 16.384\text{mS} = 393.216 \text{ ms}$$

The formula to set BEEP tone time is shown below.

$$t_{BE} = (2^6 \times (I6)+2^5 \times (I5)+2^4 \times (I4)+2^3 \times (I3)+2^2 \times (I2)+2^1 \times (I1)+2^0 \times (I0)) \times 16.384 \text{ ms}$$

6.4 Speech Control Code

Command data can set repeat and sound volume.

I6	I5	I4	I3	I2	I1	I0
1	1	sm	rp1	rp0	vl1	vl0

Channel 1 is set if $\overline{CH}$ terminal is in "H", channel 2 is set if in "L". Once a command is set, it is maintained as both channels until another command is set. The LSI cannot be maintained command contents as each channels . Conditions of each channel are set by I4 to I0. Three conditions can be set: 1) to 3) .

1) Setting Number of Repeats

The number of repeats is set by I3 and I2 terminals. For the number of repeats 4 types can be selected: 1, 2, 4 and infinite. Input stop code to stop speech when infinite repeat is selected. Table 6.5 shows the correspondence between I3 and I2 terminals, and the number of repeats.

Table 6.5 Selection of Number of Repeats

I3	I2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "I4" is set to "H", sound volume during repeat is automatically attenuated from 1 to 1/2, 1/4 and 1/8 (fadeout function). This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at I1 and I0 terminals.

Table 6.6 shows the correspondence between I1, I0 terminals and sound volume settings.

Table 6.6 Attenuation Volume Setting

I1	I0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound vlume is 1/8 of speech data)

7. ADDRESS DATA

If a user specified phrase is input to I6 to I0 terminals by address data, and if an $\overline{ST}$ signal is then input, speech synthesis starts. Time is set if silence and BEEP tone were set by command. Figure 7.1 shows speech start timing. Figures 7.2 and 7.3 show timing when an address, other than a user phrase, is input.

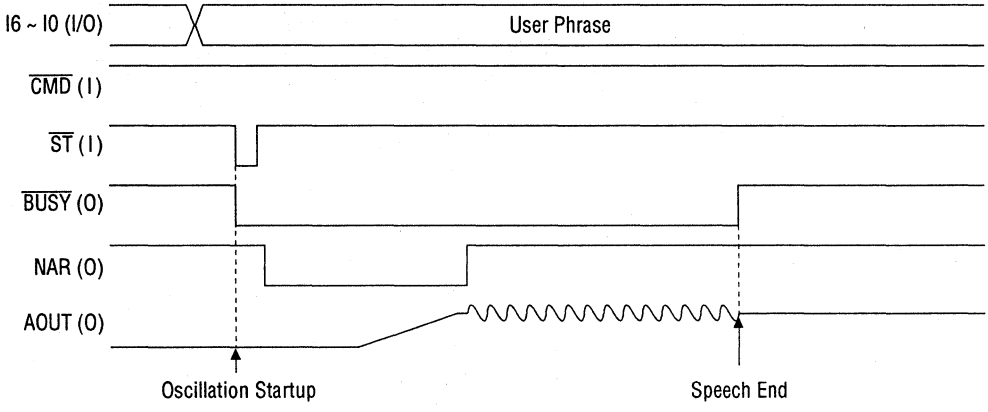


Figure 7.1 Speech Startup Timing

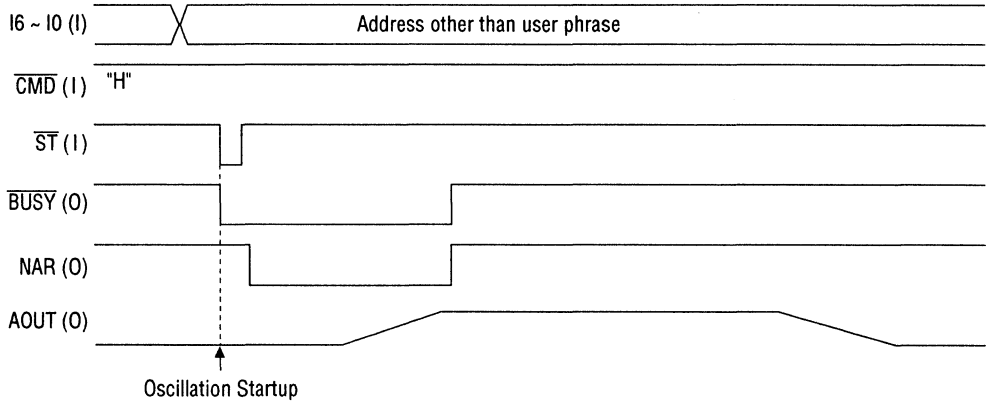


Figure 7.2 Timing when Address, other than User Phrase, is Input in Standby Status

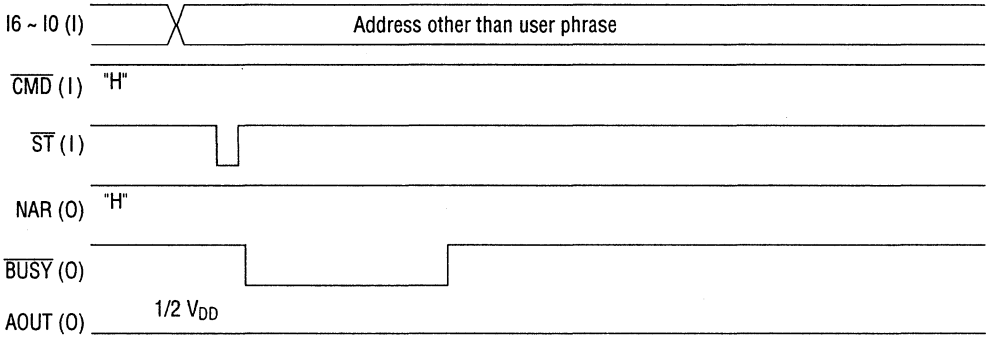


Figure 7.3 Timing when Address, other than User Phrase, is Input in Status that AOUT is 1/2 V_{DD}

8. STOP CODE

If I6 to I0 are set to "0000000" during speech vocalization, and if an $\overline{ST}$ signal is input, vocalization stops and AOUT becomes $1/2\,V_{DD}$. STOP code becomes valid at the leading edge of $\overline{ST}$ (common with parallel and serial inputs).
Use the stop code only at setting "L" $\overline{BUSY}$ pin. The stop code cannot be used in states of standby-mode .

Figure 8.1 shows stop code input timing.

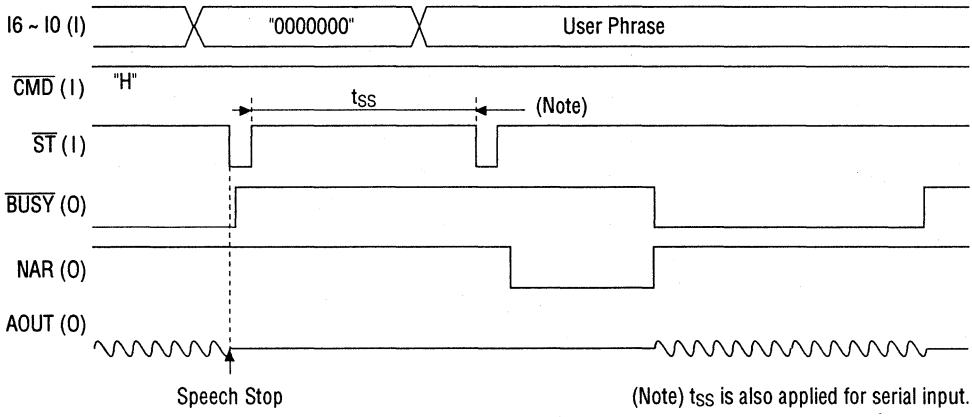


Figure 8.1 Stop Code Input Timing

If an $\overline{ST}$ signal is input by stop code in standby status, NAR stays in "H" level and AOUT becomes 1/2 V_{DD} after standby conversion time, as shown in Figure 8.2. If an $\overline{ST}$ signal is input by stop code in standby status, the status does not follow AC characteristics.

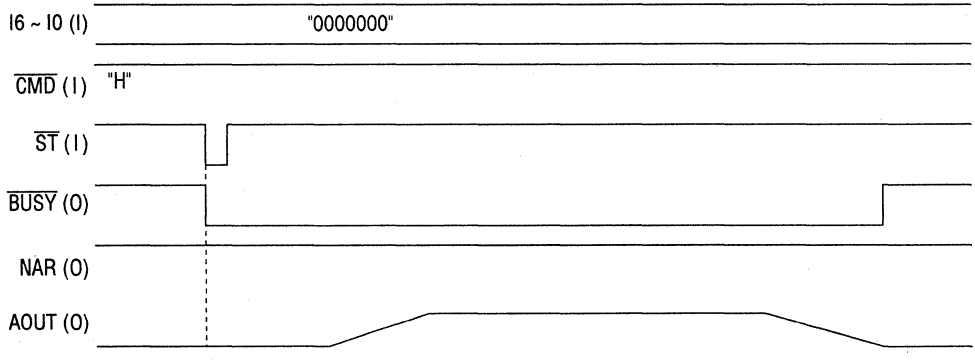


Figure 8.2 Timing when Stop Code is Input in Standby Status

9. SAMPLING FREQUENCY

Sampling frequencies can be specified for each phrase in speech data of internal ROM. For channel synthesis, if channels 1 and 2 are regenerated at the same time, the channel 1 sampling frequency has priority.

For sampling frequency, the following 8 frequencies can be selected when creating speech data.

4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz

10. SPEECH VOCALIZATION TIME

Table 10.1 shows internal ROM configuration. The actual speech data ROM area is different from the indicated ROM capacity.

The speech data management area as shown in Table 10.1 is about 6 Kbits, and the edit ROM area includes 16 Kbits.

Table 10.1 ROM Configuration

Speech Data Management Area
Editing ROM Area
Speech Data Area
Disabled Area

Use the following formula as a guide to compute speech vocalization time.

Vocalization Time = (ROM Capacity - 16 - 6) × 1024 × 255/256 ÷ Bit Rate (kbps)

For example, if data was created at a 4.0 kHz sampling using MSM6652 (288 kbit internal ROM), the vocalization time is

(288 - 16-6) × 1024 × 255/256 ÷ 16(kbps) = 16.9 sec

11. CHANNEL STATUS

The $\overline{BUSY}$ pin and NAR terminal output status signals.

$\overline{BUSY}$ terminal outputs "L" level when either channel 1 or 2 is synthesizing speech. It is in "H" level when power is turned ON.

The NAR terminal is the channel 1 and 2 input status signal (Next Address Request), enabled $\overline{ST}$ signal input when NAR is in "H" level. The channel status is switched by $\overline{CH}$ terminal. If $\overline{CH}$ terminal is in "H" level, the status signal of channel 1 is output, and if in "L" level, the status signal of channel 2 is output.

12. REGENERATION METHOD

The MSM6375 series has only the ADPCM regeneration method, however to support various speech MSM6650 has 3 types of regeneration methods: ADPCM, PCM and melody regeneration.

Respective features and how to select are explained below.

12.1 ADPCM Method

With the ADPCM (Adaptive Differential Pulse Code Modulation) method, basic quantization width Δ is adaptively changed for each sampling, and is encoded to 4bit data. This further improves the follow-up properties to speech wave forms.

Conversion to ADPCM data is performed by the AR76-202 analysis tool.

If the ADPCM method is used for human voices, animal cries and natural tones, the speech data capacity becomes smaller.

12.2 PCM Method

The PCM method of MSM6650 uses an 8-bit straight binary format. Of the three methods, PCM is the best for follow-up properties to speech wave forms.

This method is appropriate for sound effects where wave forms sharply change, and for pulse shaped wave forms.

12.3 Melody Regeneration Method

The AR76-202 analysis tool supports melody regeneration system. The melody data can be composed by using the AR76-202. Therefore, unique sound can be created.

12.4 Bit Rate of Each Method

The bit rate shows the degree of data compression and the data amount to synthesize for 1 second. The bit rate is determined by the relationship between the sampling frequency and the data-amount-per-sample. The following formula is used.

Bit Rate (kbps) = Sampling Frequency (kHz) × Data-amount-per-sample (bit)

The bit rate of the three methods are compared below when the sampling frequency is 6.4 kHz.

1) ADPCM Method

Bit Rate (kbps) = 6.4 kHz × 4 bit = 25.6 kbps

2) PCM Method

Bit Rate (kbps) = 6.4 kHz × 8 bit = 51.2 kbps

3) Melody Regeneration Method

With the melody regeneration method, the bit rate changes depending on each sound. The formula does not determine the bit rate changes. The average bit rate is 4 kbps.

12.5 The regulations of channel synthesis about each regenaration methods

Melody regeneration and BEEP tone cannot be regenarated in 2 channel side . The regulations of channel synthesis about each regeneration methods as follows table 12.1 .

Table 12.1 The Regulations of channel Synthesis

1 Channel	2 Channel	Setting
ADPCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
ADPCM(0dB～-18dB)	ADPCM(0dB)	○ Note1)
ADPCM(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
ADPCM(0dB～-18dB)	PCM(0dB)	○ Note1)
ADPCM(0dB)	PCM(0dB～-18dB)	○ Note1)
ADPCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
ADPCM(0dB～-18dB)	SILENCE	○
MELODY(0dB)	ADPCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	ADPCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	MELODY(0dB～-18dB)	×
MELODY(0dB)	PCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	PCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	PCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
MELODY(0dB～-18dB)	SILENCE	○
PCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
PCM(0dB)	PCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
PCM(0dB～-18dB)	SILENCE	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	MELODY(0dB～-18dB)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	SILENCE	○
SILENCE	ADPCM(0dB～-18dB)	○
SILENCE	MELODY(0dB～-18dB)	×
SILENCE	PCM(0dB～-18dB)	○
SILENCE	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
SILENCE	SILENCE	○

Note1) In case of channel synthesis , confirm the voice quality with the MSM6650 evaluation board. Because , occasionally , there is possible of straining the voice by recording level and synthesis phrases .

13. EDIT ROM

The role of edit ROM is to link phrases and build sentences, making an external microcomputer unnecessary. The conventional MSM6375 family could not link phrases and synthesis channels in standalone mode, but the MSM6650 family can using edit ROM.

For example: The phrase "Today's weather is...." is used to compare the MSM6375 family and MSM6650 family. With the MSM6375 family, individual data must be stored to phrase ROM (see Table 13.1) to vocalize each phrase in timing of once as "Today's weather is sunny", and "Today's weather is rainy".

On the other hand, the MSM6650 family can vocalize plural phrases at timing of once by having edit ROM functions. This means that "Today's weather is sunny" will be vocalized by merely specifying address [01] of Table 13.3 in the phrase ROM configuration shown in Table 13.2. If address [02] is specified, "Today's weather is rainy" will be vocalized.

Conventionally data must be repeatedly stared to phrase ROM to vocalize "Today's weather is....", but overlapped data is not required as shown in Table 13.2 by using edit ROM functions.

Table 13.1 Conventional Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's weather is sunny.
02	Today's weather is rainy.
03	Today's weather is sunny follwed by cloudy, some areas are rainy.
⌇	⌇
7F	

Table 13.2 Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's
02	weather
03	is
∫	∫
10	sunny
11	cloudy
12	rainy
13	snowy
20	occasional
21	followed by
22	some areas are
∫	∫
7F	

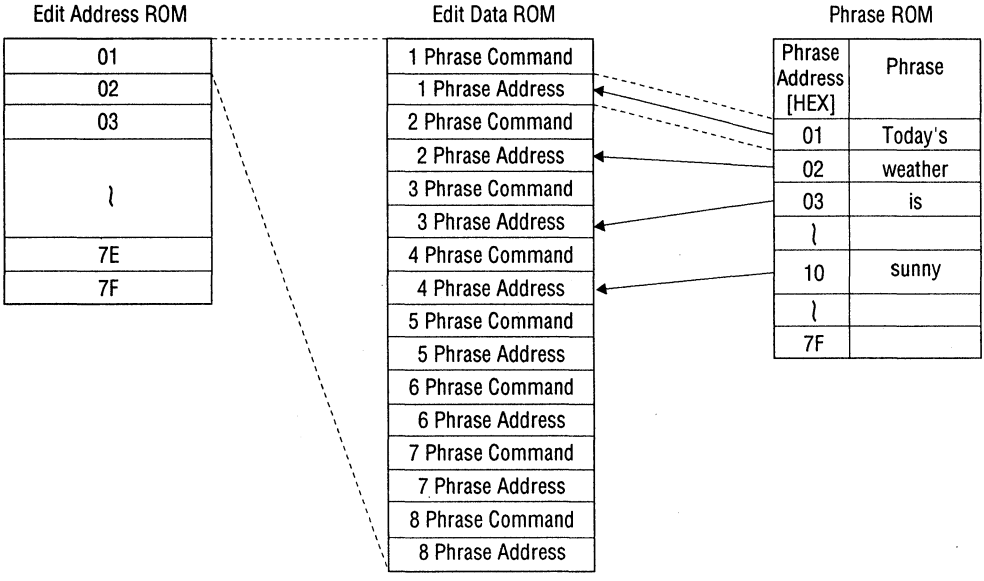
Table 13.3 Edit ROM Configuration

Address [HEX]	Edit Content [Max. 8 Phrases]
01	[01][02][03][10]
02	[01][02][03][12]
03	[01][02][03][10][21][11][22][12]
∫	∫
7F	

In addition, by using the edit ROM, the MSM6375 series can perform channel synthesis in stand alone mode which was not possible before. The edit ROM not only can connect phrases but can also perform channel synthesis and selection of BEEP and mute sound by commands.

A maximum of 8 phrases (16 bytes) can be set in 1 edit. Table 13.4 shows the configuration of edit ROM.

Table 13.4 Edit ROM Configuration



Edit address ROM can process a maximum of 127 user specified phrases. Table 13.4 shows the relationship between phrase ROM, edit data ROM, and edit address ROM.

Phrase ROM cannot be directly accessed if edit ROM is used.

Edit ROM can be setup using the previously mentioned AR76-202 analysis tool. For regeneration using edit ROM, regeneration may not be the one requested. Be certain to check the speech data using either the analysis tool or MSM6650 of external ROM.

Figure 13.1 shows the flow chart when creating edit ROM.

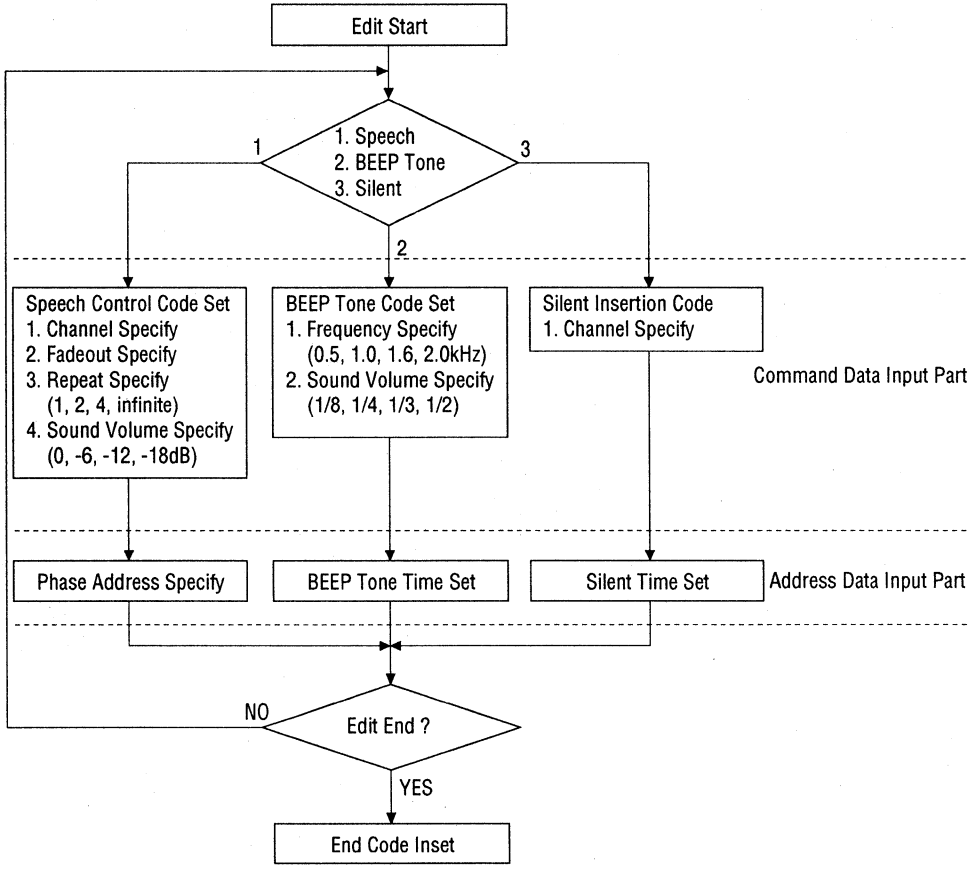


Figure 13.1 Edit Data ROM Creation Flow Chart

13.1 Edit ROM Commands

Table 13.5 shows the commands that can be set in edit ROM.

Table 13.5 List of Commands that Can Be Set in Edit ROM

O7	O6	O5	O4	O3	O2	O1	O0	Command
0	0	0	0	0	0	0	0	End Code
ch	0	1	0	0	0	0	0	Silence insertion Code
1	1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
ch	1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

The commands of the 4 codes shown in Table 13.5 are explained below.

13.1.1 End Code

End code means that one edit data is completed. Although this is necessary at the end of one edit data, since the LSI can recognize the end of editing, it is unnecessary when the maximum number of phrases are used.

13.1.2 Silence Insertion Code

Silence insertion code inserts silence to each channel, reducing speech data.

O7	O6	O5	O4	O3	O2	O1	O0
ch	0	1	0	0	0	0	0

The channel to insert silence is specified in command data, and silence time is set in address data.

The channel to insert silence is set to "O7" command data. If "O7" is "H" channel 1 is set, if "L" channel 2 is set.

Silence time is set at the address settings of phrases shown in Table 13.4.

Minimum Silence Time ... 16.384 ms
Maximum Silence Time ... 2.1 sec.

The formula to set the silence time is shown below.

$t_{MU} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384$ ms

Table 13.6 Edit Data Example of Silence Insertion Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	0	1	0	0	0	0	0	Silence Insertion Code
2nd Byte	0	0	0	1	1	0	0	0	Silence Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 13.6, then 393 ms of silence is inserted to channel 1.

13.1.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data.

The BEEP tone can be set only at channel 1.

To mix a BEEP tone and channel 2 vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz.
If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

O7	O6	O5	O4	O3	O2	O1	O0
1	1	0	0	bl1	bl0	bf1	bf0

The sound volume is set to O3, O2 and the frequency is set to O1, O0. Tables 13.7 and 13.8 show the sound volumes and the frequencies that can be set.

Table 13.7 Sound Volume Settings

O3	O2	Sound Volume
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 13.8 Frequency Settings

O1	O0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

The BEEP tone time is set to the address setting of phrases shown in Table 13.4.

Minimum BEEP Tone Time ... 16.384 ms
Maximum BEEP Tone Time ... 2.1 sec.

The formula to set a BEEP tone time is shown below.

$t_{MU} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384$ ms

Table 13.9 Edit Data Example of BEEP Tone Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	0	0	1	1	0	1	BEEP Tone Code
2nd Byte	0	0	0	1	1	0	0	0	BEEP Tone Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data are set as in Table 13.9, BEEP sound of 1.0kHz is vocalized for 393mS with 1/2 of amplitude of sound volume of Channel 1.

13.1.4 Speech Control Code

Speech control code can set repeat and sound volume.

O7	O6	O5	O4	O3	O2	O1	O0
ch	1	1	sm	rp1	rp0	vl1	vl0

The channel is set at "O7". If "O7" is "H", channel 1 is set, if "L" channel, 2 is set. The speech control condition of each channel is set between O4 to O0.

1) Setting Number of Repeats

The number of repeats is set at O3 and O2, and can be selected from 4 types: 1, 2, 4 and infinite. If infinite is selected, repeat can be stopped by inputting stop code.

Table 13.10 shows the relationship between O3, O2 and the number of repeats.

Table 13.10 Number of Repeats Settings

O3	O2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "O4" is set to "H", sound volume during repeat is attenuated from 1 to 1/2, 1/4 and 1/8. This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at O1 and O0. Table 13.11 shows the correspondence.

Table 13.11 Attenuation Volume Setting

O1	O0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound volume is 1/8 of speech data)

13.2 PCM Regeneration in Edit ROM

For PCM regeneration, edit data is set together with speech control code. All settable items in speech control code (channel, sound volume smoothing during repeat, number of repeats, and sound volume) can be set.

13.3 Melody Regeneration in Edit ROM

For melody regeneration, edit data is set together with speech control code. Channels however cannot be set. Channel 1 is fixed. Channel 2 mixing of melody regeneration / melody regeneration combination is not possible.

All settable items in speech control code can be set except channels.

13.4 Continuous Regeneration in Edit ROM

If at the 2nd edit phrase is input during speech vocalization of the 1st edit phrase (phrase consists of 16 bytes or less of edit data ROM: referred to as edit phrase), speech vocalization starts continuously after 1st edit phrase vocalization ends.

However, this occurs only when the channel setting of the 1st and 2nd edit phrase are the same, and when echo regeneration and channel 2 regeneration are not performed. For example, if the 1st edit phrase is echo regeneration, and the 2nd edit phrase channel 1 regeneration, as shown in Figure 13.2 (1), then 2 edit phrases overlap.

To avoid this, insert silence to channel 1, as shown in Figure 13.2 (2), and set edit data ROM so that channels 1 and 2 end regeneration at the same time.

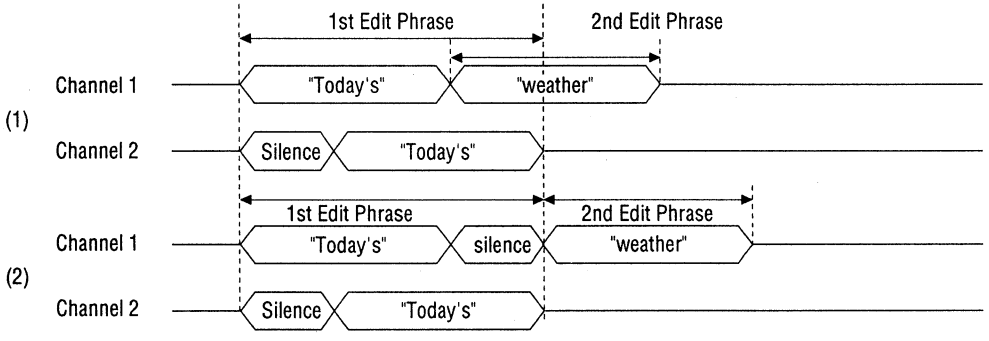


Figure 13.2 Example of Continuous Regeneration Timing

13.5 Channel 2 Mixing Function in Edit ROM

This function overlaps 2 phrases.

By using edit ROM, it is easy to echo a phrase (echo regen-eration) and to vocalize a phrase with a musical instrument sound or BGM (channel 2 regeneration).

13.5.1 Echo Regeneration

Echo regeneration delays and overlaps -6 dB attenuation (1/2 amplitude speech wave form of channel 1) to a speech wave form vocalized at channel 1.

Echo Reproduction of Multiple Phrases

Using address [02] of phrase ROM, "weather", an echo regeneration edit data example in Table 13.2, is explained below.

Table 13.12 Edit Data Example of 1 Phrase Echo Regeneration

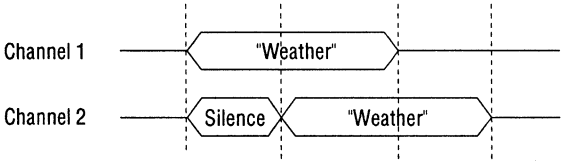
	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat, no attenuation)
2nd Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	0	1	Speech Control Code (2ch setting, repeat, -6 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
7th Byte	0	0	0	0	0	0	0	0	End code

If edit data is set as in Table 13.12 , "weather" is vocalized at channel 1, and is overlapped and vocalized from channel 2 with a -6 dB attenuated sound volume 98.3 mS later.

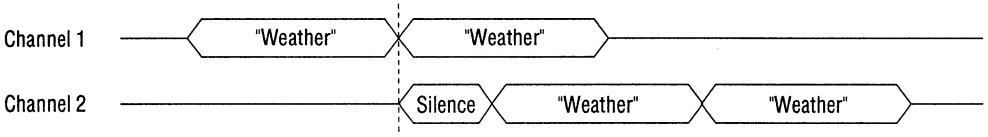
When 2 phrases overlap, set the attenuation of the speech control command with attention to sound volume.

The silence time by silence insertion code is a factor that influences echo quality. Set the silence time so that the desired echo is created.

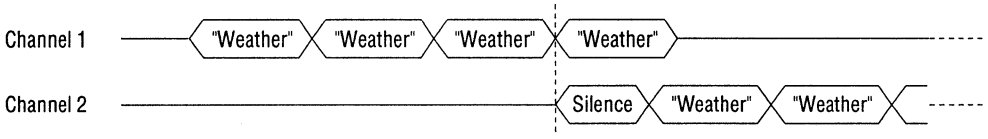
When performing echo regeneration set the number of repeats of the speech control command to 1. If 2, 4 or infinite is set, timing becomes as shown in Figure 13.3. This figure shows that the number of repeats of the 1st and 5th byte of edit data in Table 13.12 have changed.



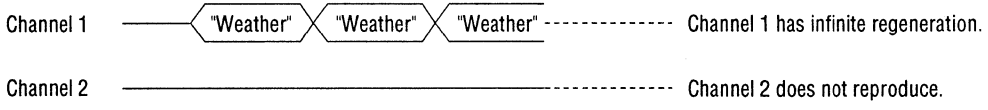
(1) Number of Repeats: 1



(2) Number of Repeats: 2



(3) Number of Repeats: 4



(4) Number of Repeats: infinite

Figure 13.3 Vocalization Timing of Echo Reproduction According to Number of Repeats

The vocalization timing, when the number of repeats of the speech control command is set for an edit data phrase, is explained below.

① When number of repeats is set to 1

If the same channel is specified for the next phrase, vocalization of the next phrase starts when vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of vocalization.

② When number of repeats is set to 2

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the second vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the second vocalization after the first vocalization ends.

③ When number of repeats is set to 4

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the fourth vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the fourth vocalization after the 3rd vocalization ends.

④ When number of repeats is set to infinite

The next phrase becomes invalid and is not vocalized regardless the channel specification.

Echo Reproduction of Multiple Phrases

A maximum of 8 phrases (16 bytes) are set to one edit data ROM. Up to 3 phrases are possible for an echo reproduction with 16 bytes. Set the phrase ROM so that the number of phrases do not exceed four.

Using "Today's", "weather" and "is" of the phrase ROM in Table 13.2 as an example, Table 13.13 shows a three phrase echo regeneration edit data example, and Figure 13.4 shows vocalization timing.

Table 13.13 Three Phrase Echo Regeneration Edit Data Example

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting repeat once, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	0	0	0	1	0	Phrae Address (02H "weather")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
13th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
14th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
15th Byte	1	1	1	0	0	0	1	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
16th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")

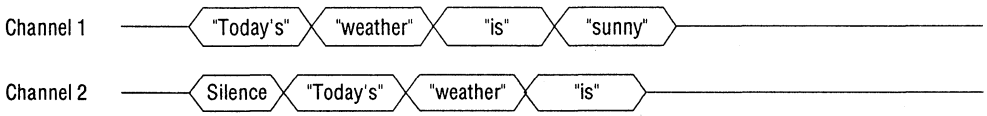


Figure 13.4 Vocalization Timing of a Three Phrase Echo Regeneration

For the echo regeneration of multiple phrases, set so that the sampling frequency of each phrase is the same. If a phrase with a different sampling frequency is mixed, the speech of channel 2 will become fast or slow because the sampling frequency of channel 1 has priority. Figure 13.5 shows the timing.

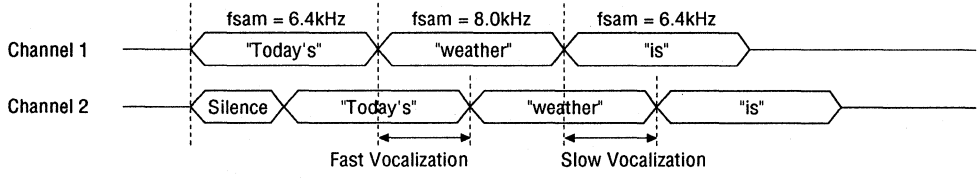


Figure 13.5 Vocalization Timing of Echo Regenerations with Different Sampling Frequencies

Echo Reproduction of an Arbitrary Phrase in Multiple Phrases

Table 13.14 shows an edit data example to apply echo to "is" in the four phrases of "Today's", "weather", "is" and "sunny".

Table 13.14 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	1	1	0	0	0	0	1	Silence Time (1.59 mS)
5th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting repeat once, no attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "tweather")
7th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
8th Byte	0	0	0	1	0	0	0	0	Phrae Address (10H "is")
9th Byte	0	1	1	0	0	0	0	1	Speech Control Code (2ch setting, repeat once, -6 dB attenuation)
10th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
11th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
12th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")
13th Byte	0	0	0	0	0	0	0	0	End Code

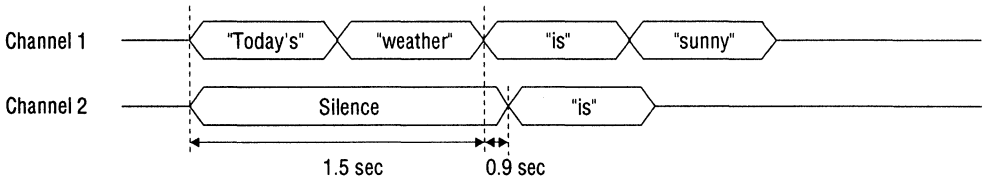


Figure 13.6 Vocalization Timing Using Edit Data of Table 13.14

As shown by the timing in Figure 13.6, "is" is echoed by setting the silence time, which is the addition of the vocalization time for "Today's" and "weather" and the delay time for echo to channel 2. If the silence time exceeds 2.1 sec, it is necessary to add a silence insertion setting to 2 bytes of edit data.

For the echo reproduction of one arbitrary phrase of multiple phrases, a maximum of 6 phrases are possible if the silence insertion setting is 2 bytes.

13.5.2 Two-channel Regeneration

Two-channel regeneration uses PCM, melody and ADPCM methods. Channel synthesis is possible with all combinations except a melody regeneration / melody regeneration combination. Melody regeneration is fixed to channel 1. The sampling frequency of phrases to be overlapped must be the same.

Figures 13.7 to 13.10 show the vocalization timings of two-channel regeneration.

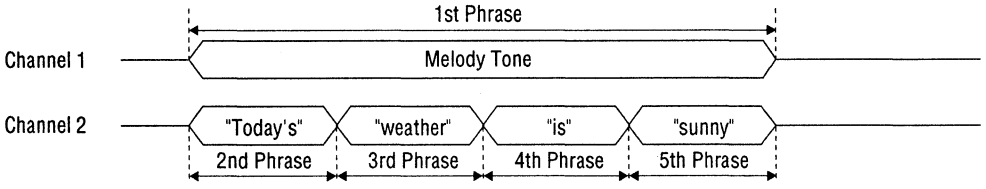


Figure 13.7 Example of Four Phrase Channel Synthesis Timing with Melody Tone as GBM

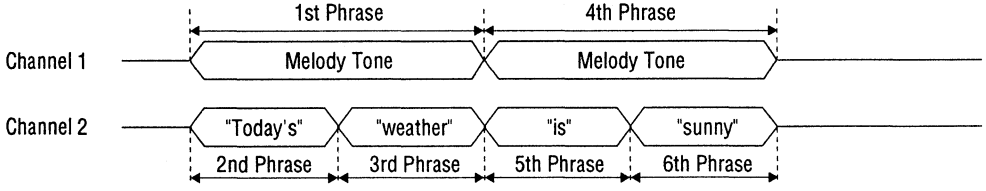


Figure 13.8 Example of Four Phrase Channel Syntehsis Timing with Melody Tone and 1st and 4th Phrases as BGM

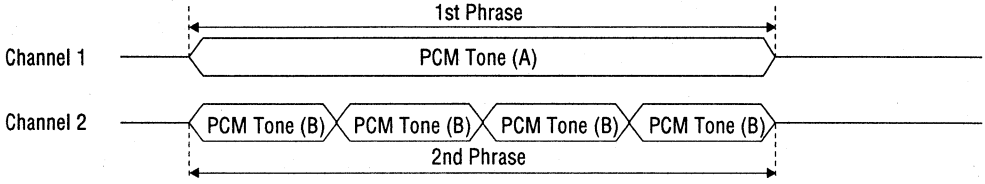


Figure 13.9 Example of Channel Synthesis between PCM Main Melody Tone (A) and PCM Rhythm Tone (B) with 4 Repeats

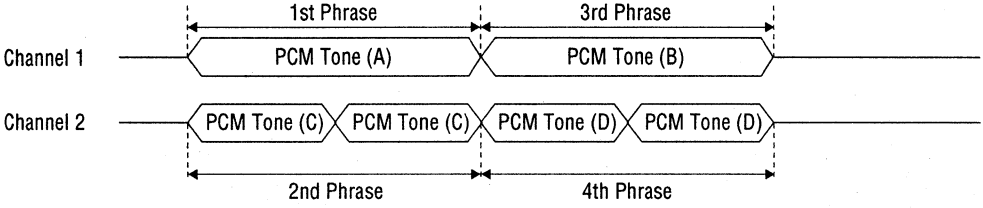


Figure 13.10 Example of Channel Synthesis between PCM Main Melody Tone (A), (B) and PCM Rhythm Tone (C), (D) with 2 Repeats

14. STANDBY CONVERSION

If standby conversion YES is selected by command option, if the next phrase does not startup within 0.2 sec. after vocalization ends, the LSI enters standby status and stops all operations. If restarted it takes about 100 ms until speech starts, since a pop noise countermeasure circuit operates.

If standby conversion NO is selected by command option, the LSI does not enter standby status, even if speech ends, and the output of AOUT becomes about 1/2 VDD. Current is flowing since oscillation is operating. If started up speech starts in about 350 µs.

If standby conversion NO is selected, it is necessary to input an $\overline{\text{RESET}}$ pulse to enter standby status.

If an $\overline{\text{RESET}}$ pulse is input, a pop noise is generated since the AOUT output level instantaneously becomes GND level.

15. SPEECH OUTPUT

For the speech output terminal, a command option can select whether the DA converter output is directly output or output through an internal low pass filter.
Table 15.1 shows output level of AOUT pin.

Table 15.1 Output level of AOUT pin

Regeneration method	Conditions	Most lowest level	Centre level	Most highest level
ADPCM	DA converter output	0	About 0.5 x VDD	About VDD
	LPF output	About 0.15 x VDD	About 0.5 x VDD	About 0.95 x VDD
PCM	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
Melody	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
BEEP Tone	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD

15.1 DA Converter Output Wave Form

The output amplitude from the DA converter becomes a step wave form synchronizing the sampling frequency at a maximum 4095/4096 × VDD.

If DA output is selected, it is recommended to externally attach a low pass filter. Since the output impedance of a DA converter changes between 15 kΩ to 35 kΩ, determine the filter constant so that this resistance change does not affect the cutoff frequency of the low pass filter.

15.2 Low Pass Filter Output

A low pass filter consists of switched capacitors. The attenuation characteristic of the MSM6650 low pass filter is -40 dB/oct. The cutoff frequency changes depending on the sampling frequency.

Table 15.2 shows the relationship between sampling frequency and cutoff frequency.

Table 15.2 Cutoff Frequencies of Low Pass Filter

Sampling Frequency (fsam)	Cut-off Frequency (fcut)
4.0kHz	About 1.8kHz
5.3kHz	About 2.6kHz
6.4kHz	About 2.6kHz
8.0kHz	About 3.2kHz
10.6kHz	About 4.2kHz
12.8kHz	About 5.1kHz
16.0kHz	About 6.4kHz
32.0kHz	About 12.8kHz

16. CERAMIC OSCILLATION

Figure16.1 shows an external circuit diagram using a ceramic oscillator.

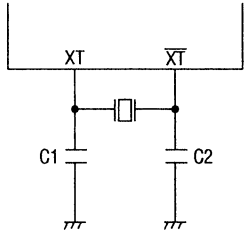


Figure 16.1 External circuit diagram

Figure 16.2 and 16.3 show external circuit diagrams using a cermic oscillator, CSA4.09MGU and CST4.09MGWU made by Murata Seisakusho Co., ltd.

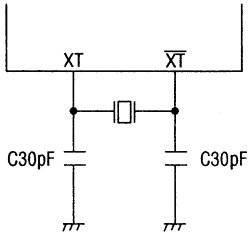


Figure 16.2 CSA4.09MGU

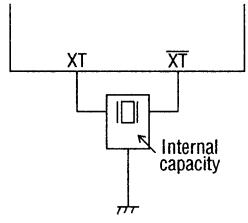


Figure 16.3 CST4.09MGWU

Figure 16.4 shows an external circuit diagram using a cermic oscillator, PBRC4.00MSA/MSK/MWS made by Kyocera Co., ltd.

Note) In case of using a oscillator 4.00MHz, vocalization speed is low about 2% than AR76-202 analysis tool and evaluation board.

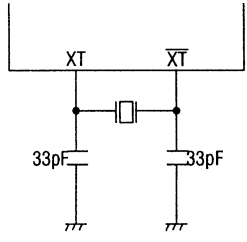
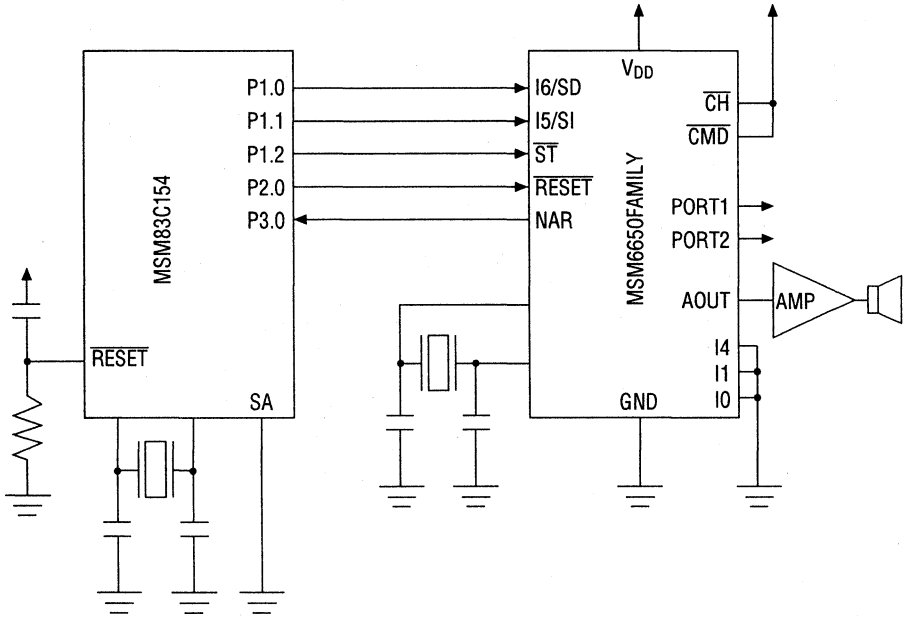
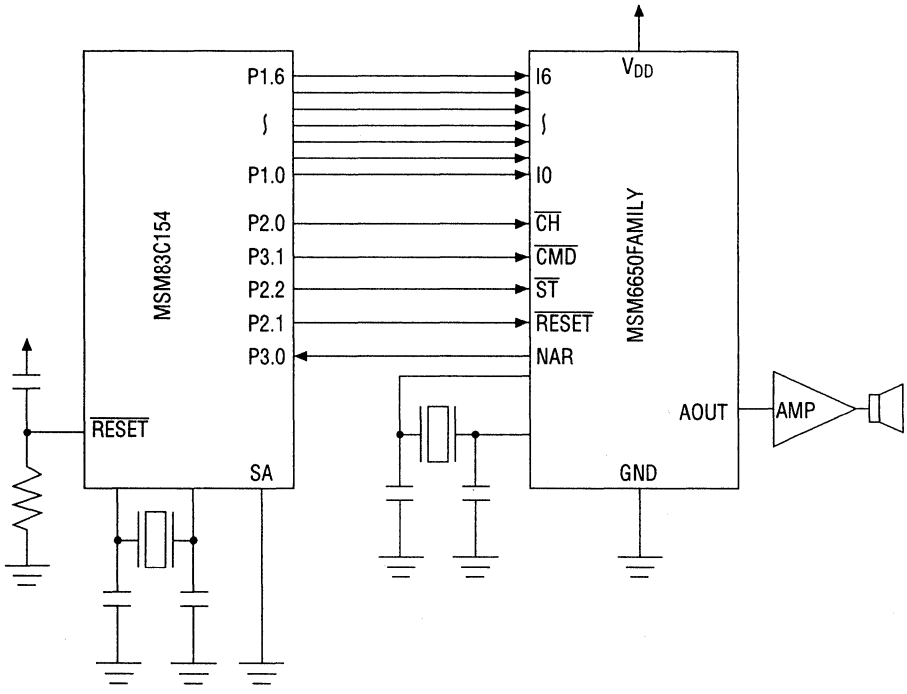


Figure 16.4 PRBC 4.00 MSA/MSK/MWS

APPLICATION CIRCUIT EXAMPLE



Example of Application Circuit at Serial Input Interface



Example of Application Circuit at Parallel Input Interface

OKI Semiconductor

MSM66P54-01/02/03/04

MSM6650 family 1 Mbit OTP Built-in Speech Synthesis LSI

GENERAL DESCRIPTION

The MSM66P54 is a single-chip CMOS speech synthesis LSI that has an on-chip OTP (One Time PROM) for speech data storage. This LSI is the OTP version for on-chip mask ROMs from the MSM6652 to the MSM6656. The MSM66P54 that adds PCM system to ADPCM system provides you a speech synthesis sound of a high quality so that it contains a 12bit DA converter and -40dB/oct low pass filter.

The conventional "BEEP" tone and a 2-channel mixing function are now easier to use, and a melody function, fadeout function and random vocalization function are now included. External control is easier than before due to the addition of an edit ROM that can form sentences by linking phrases.

As it is possible to select standalone mode or microcontroller interface mode by the code (-01~ -04), it can handle various applications. Because MSM66P54-01 has serial inputs, it is possible to reduce the number of ports for controlling microcontrollers.

A speech analysis and speech data can be simply written by using a developed tool AR76-202 at your side. This LSI is suited for applications to the small production of various products and the short delivery that can not correspond to the mask ROM. In case of the mass production, on-chip mask ROMs from the MSM6652 to the MSM6656 are recommended.

This LSI is classified to two kinds of stand-alone and microcontroller interface. Refer to the contains because this description explains these two kinds individually. In addition, see the pages described about on-chip mask ROM products from the MSM6652 to the MSM6656.

Table of Contents

Standalone

Microcontroller Interface

(1) STANDALONE MODE

FEATURES

ROM Capacity	Maximum Vocalization Time			
	fsam = 4.0 kHz	fsam = 6.4 kHz	fsam = 8.0 kHz	fsam = 16.0 kHz
1 Mbit	63.8sec	39.9sec	31.9sec	15.9sec

(Actual speech ROM area is less by 22 kbit)

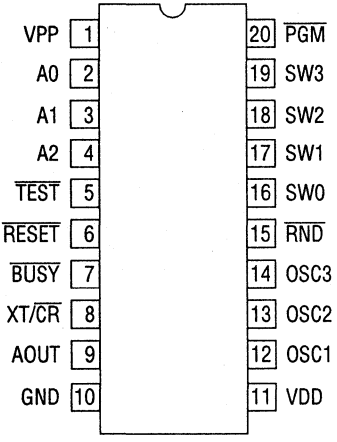
4bit ADPCM method/8bit PCM method
Melody function
Edit ROM function
2-channel mixing function
Internal random vocalization function
Fadeout function (4-step change of sound volume)
BEEP tone built-in BEEP tones of 0.5 kHz, 1.0 kHz, 1.6 kHz and 2.0 kHz can be generated by specification code.
Sampling frequencies 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz 1)
Note 1)32.0 kHz cannot be selected if RC oscillation is selected.
Maximum number of phrases : 120
Internal 12-bit D/A converter
Internal LPF attenuation factor : -40 dB / oct
Standby function
RC oscillation or ceramic oscillation can be selected
Data write time (when using AR76-202.)
Write and verify : approx. 2 minutes
Verify only : approx. 30 seconds
Package : 20-pin DIP (DIP 20-P-300-W1)
24-pin SOP (SOP 24-P-430-VK)
Code option : -03 standalone (shift to standby)
-04 standalone (no shift to standby)
(-01, -02 microcontroller interface)

PIN CONFIGURATION

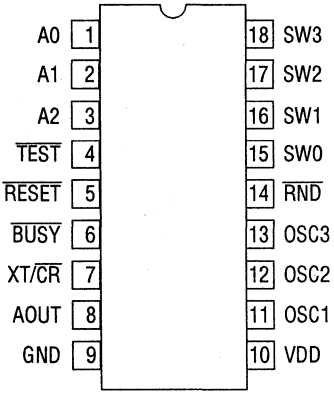
(Top View)

On-chip ROM series and pin layouts are basically fitted, but the MSM66P54 increases further two pins for write than on-chip mask ROMs from the MSM6652 to the MSM6656. These two pins (Vpp and $\overline{PGM}$) allow you to be opened in replay after the write is completed.

MSM66P54 (OTP)
20 Lead Plastic DIP

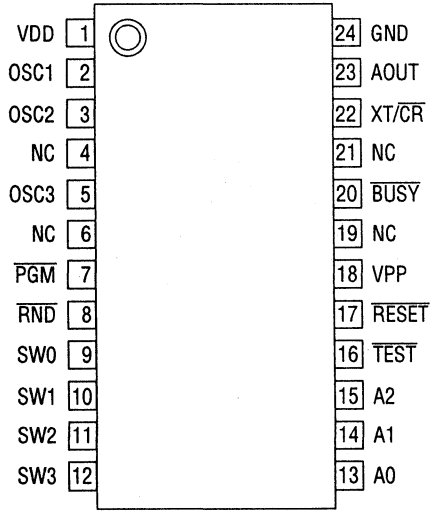


MSM6652~6656 (Mask ROM)
18 Lead Plastic DIP

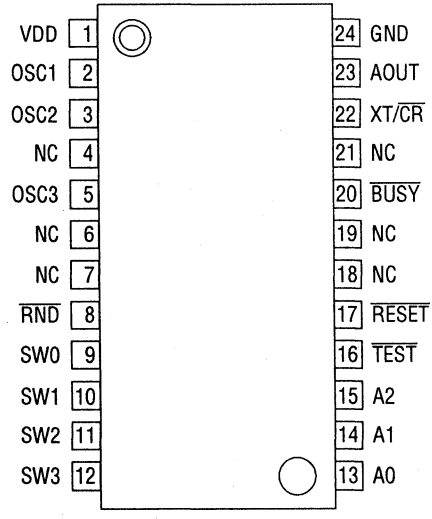


Note: Applicable to MSM66P54-01/02/03/04RS

MSM66P54 (OTP)
24 Lead Plastic SOP

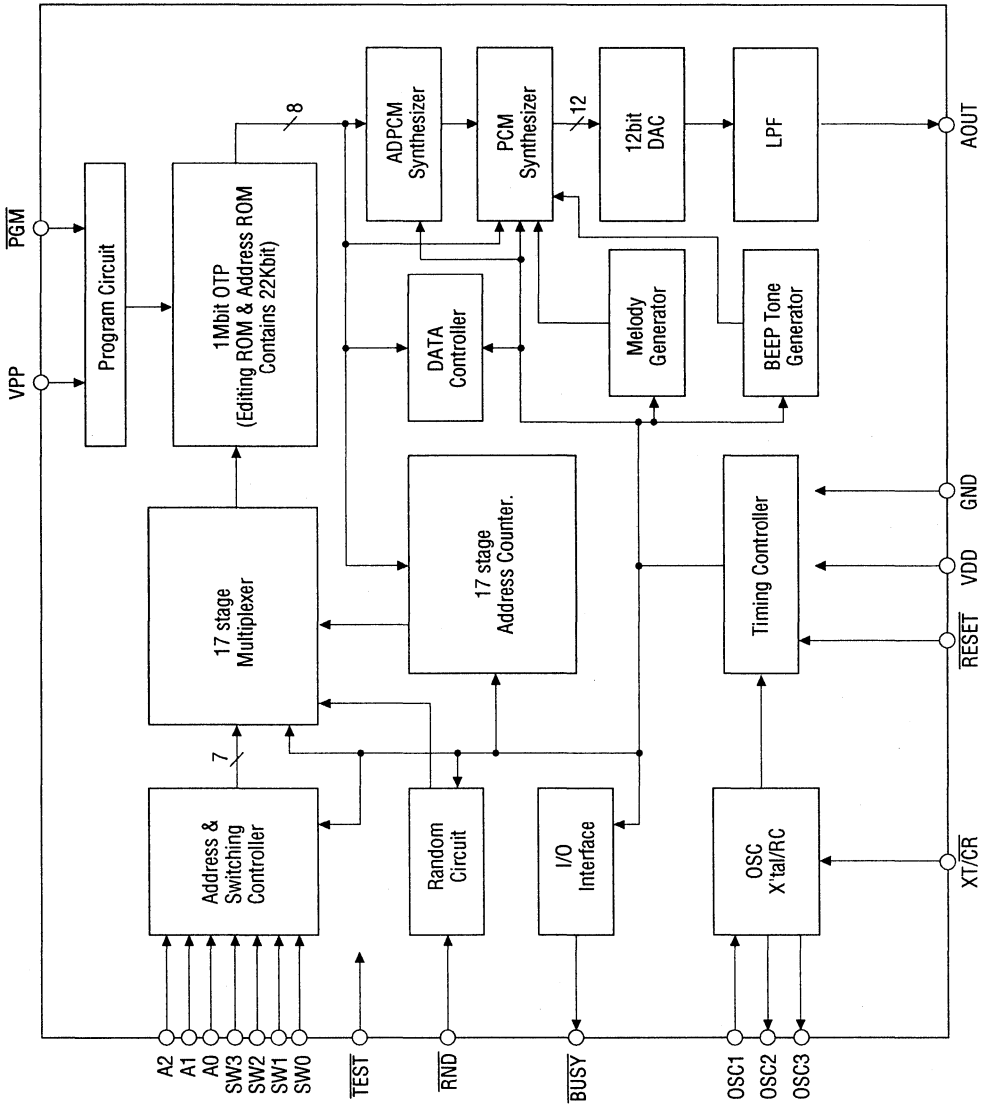


MSM6652~6656 (Mask ROM)
24 Lead Plastic SOP



Note: Applicable to MSM66P54-01/02/03/04GS-VK

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operating Range

(GND = 0V)

Parameter	Symbol	Condition	Limits			Unit
Power Supply Voltage	V_{DD}	LPF output	+3.5 ~ +5.5			V
Operating Temperature	T_{op}	–	-10 ~ 70			°C
Original Oscillation Frequency (1)	f_{OSC1}	When X'tal selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Original Oscillation Frequency (2)	f_{OSC2}	When RC selected	200	256	300	kHz

Note 1: The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the R and C of the external parts.

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -10 ~ 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -40μA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 40μA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	μA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-200	-90	-30	μA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	μA
"L" Input Current 2	I_{IL2}	Internal pullup resistance pin	30	90	200	μA
Operating Current Consumption	I_{DD}	–	–	6	20	mA
Standby Current Consumption	I_{DS}	–	–	–	100	μA
LPF Load Resistance	R_{AOUT}	–	50	–	–	kΩ

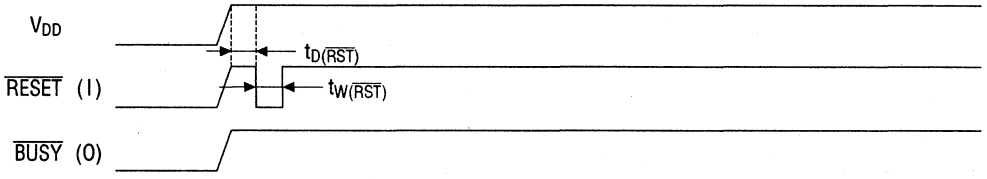
AC CHARACTERISTICS

(V_{DD} = 5.0V, GND = 0V, Ta = -10 ~ 70°C)

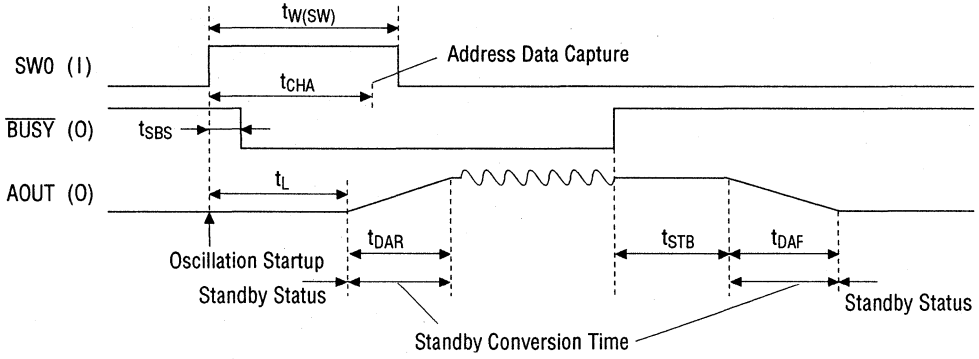
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{W(\overline{RST})}$	–	10	–	–	µS
$\overline{\text{RESET}}$ Input Time after Power on	$t_{D(\overline{RST})}$	–	0	–	–	µS
$\overline{\text{RND}}$ Input Pulse Width	$t_{W(\overline{RAN})}$	–	100	–	–	µS
SW3~SW0 Input Pulse Width	$t_{W(SW)}$	–	32	–	–	mS
$\overline{\text{BUSY}}$ Output Time (1)	t_{SBS}	–	–	–	10	µS
$\overline{\text{BUSY}}$ Output Time (2)	t_{BN}	When fsam = 8kHz	350	375	400	µS
Chattering Prevention Time	t_{CHA}	–	29	30	31	mS
DA Converter Change Time	t_{DAR}, t_{DAF}	–	60	64	68	mS
LPF Stabilization Time	t_L	–	6	8	10	mS
Standby Conversion Time	t_{STB}	–	0.45	0.5	0.55	sec.
Capture Random Address Time	t_{RA}	–	16	32	48	µS

TIMING CHART

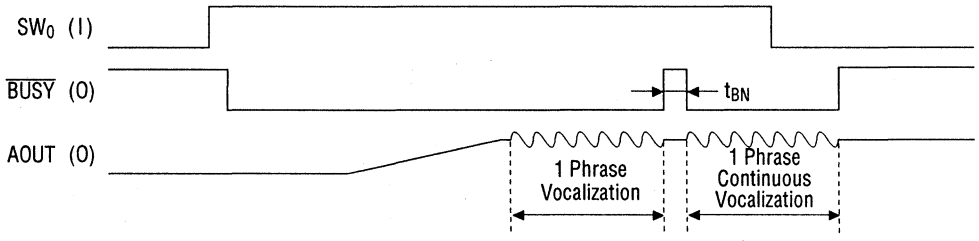
1. When Power is Turned ON



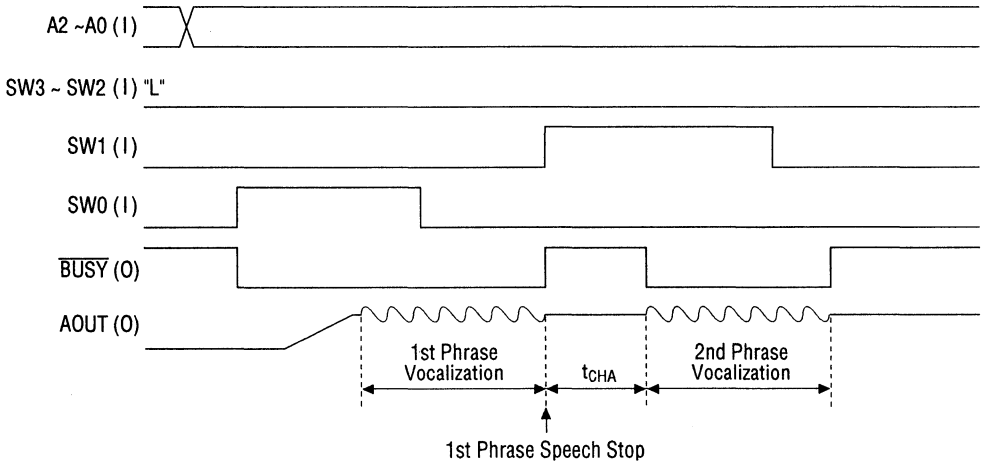
2. When LSI Starts Up and is In Standby Status



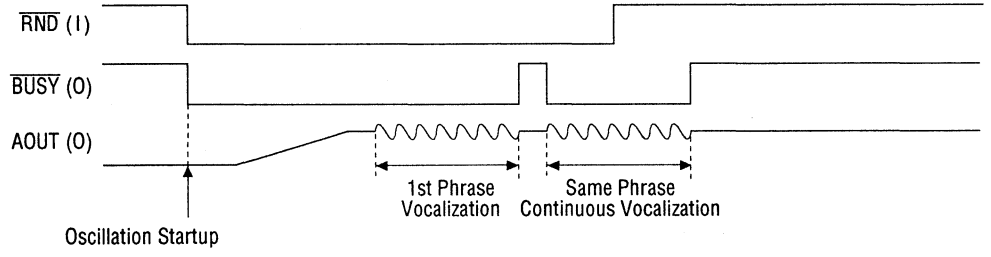
3. Repeat Vocalization Timing Chart



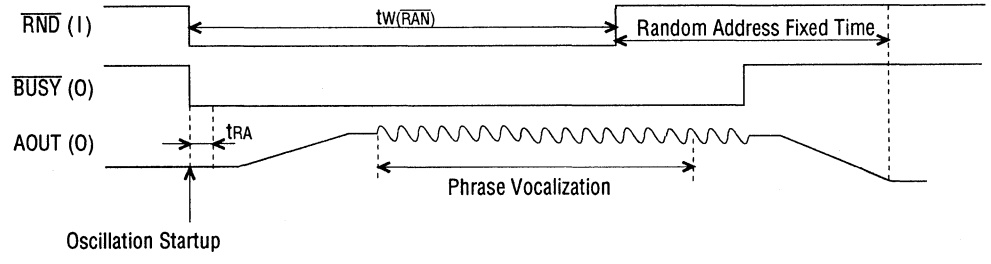
4. Timing Chart When SW3~SW0 are Changed During Vocalization



5. Repeat Vocalization Timing Chart of Random Vocalization



6. Timing Chart of Capturing Random Address



PIN DETAILS

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	LSI is in standby status if set to "L" level. At this time oscillation stops and AOUT output becomes GND, and returns to initial status. LSI has internal power ON reset. To operate power ON reset correctly startup power within 1 mS If not, apply $\overline{\text{RESET}}$ pulse when power is turned ON. This pin has internal pullup resistor.
$\overline{\text{BUSY}}$	O	Outputs "L" level during vocalization. In "H" level when power is turned ON.
XT/$\overline{\text{CR}}$	I	X'tal or RC selectable pin. Set to "H" level if ceramic oscillator is used. Set to "L" level if RC oscillation is used.
AOUT	O	Speech output pin of internal LPF.
GND	–	Ground pin
VDD	–	Power pin
OSC1	I	Ceramic oscillator connection pin when ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	Ceramic ocsillator connection pin when ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Set to open if external clock is used. Outputs "L" level in standby status.
OSC3	O	Set to open if ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Outputs "H" level in standby status when RC oscillation is selected.
$\overline{\text{RND}}$	I	Random vocalization starts if $\overline{\text{RND}}$ pin is set to "L" level. Captures address from random address generation circuit in LSI at fall of $\overline{\text{RND}}$. Set to "H" level if random vocalization function is not used. This pin has internal pullup resistor.
$\overline{\text{TEST}}$	I	A test pin. Set to "H" level. This pin has internal pullup resistor.
SW3~SW0	I	Phrase input pins corresponding to vocalized sound. If input changes, SW3~SW0 pins capture addresses after 16 mS, and starts speech synthesis. These pins have internal pulldown resistor.
A2~A0	I	Phrase input pins corresponding to vocalized sound. A0 input becomes invalid if the random vocalization function is used.
VPP	–	Power supply voltage pin for write in on-chip OTP. Set to "H" or open in replay.
$\overline{\text{PGM}}$	I	Interface pin for speech analysis edition tool AR76-202. Set to "L" or open in reply. This pin has internal pull-down resistor.

Note: See the pages described about on-chip mask ROM products from the MSM6652 to the MSM6656 for more detailed functions. In addition, the values of a R and C mounted externally for a RC oscillation differ a little between on-chip mask ROM products and on-chip OTP products.

(2) MICROCONTROLLER INTERFACE MODE

FEATUERS

ROM Capacity	Maximum Vocalization Time				
	fsam = 4.0 kHz	fsam = 6.4 kHz	fsam = 8.0 kHz	fsam = 16.0 kHz	fsam = 32.0 kHz
1 Mbit	63.8sec	39.9sec	31.9sec	15.9sec	8.0sec

(Actual speech ROM area is less by 22 kbit)

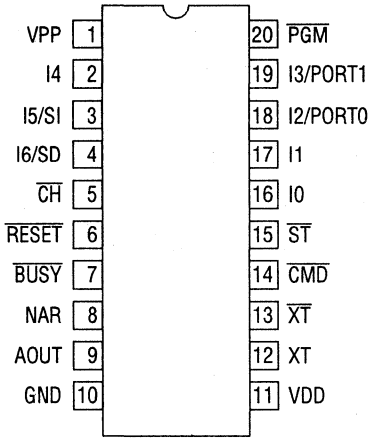
4bit ADPCM method/8bit PCM method
Melody function
Edit ROM function
2-channel mixing function
Fadeout function (4-step change of sound volume)
Serial input/parallel input can be selected
BEEP tone built-in : BEEP tones of 0.5 kHz, 1.0 kHz, 1.6 kHz and 2.0 kHz can be generated by specification code.
Sampling frequencies : 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0kHz, 32.0kHz
Maximum number of phrases : 127 Phrases
Internal 12-bit D/A converter
Internal LPF attenuation factor : -40 dB/oct
Standby function
Data write time (When using AR76-202.)
Write and verify : approx. 2 minutes
Verify only : approx. 30 seconds
Package : 20-pin DIP (DIP 20-P-300-W1)
24-pin SOP (SOP 24-P-430-VK)
Code option : -01 serial input microcontroller interface
-02 parallel input microcontroller interface
(-03, -04 standalone)

PIN CONFIGURATION

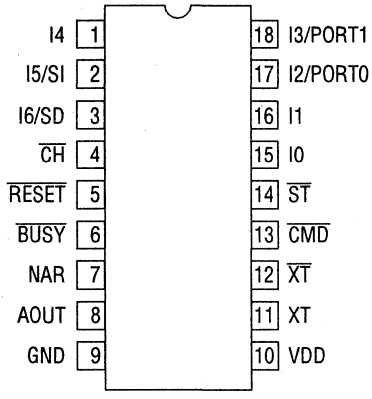
(Top View)

On-chip ROM series and pin layouts are basically fitted, but the MSM66P54 increases further two pins for write than on-chip mask ROMs from the MSM6652 to the MSM6656. These two pins (Vpp and $\overline{PGM}$) allow you to be opened in replay after the write is completed.

MSM66P54 (OTP)
20 Lead Plastic DIP

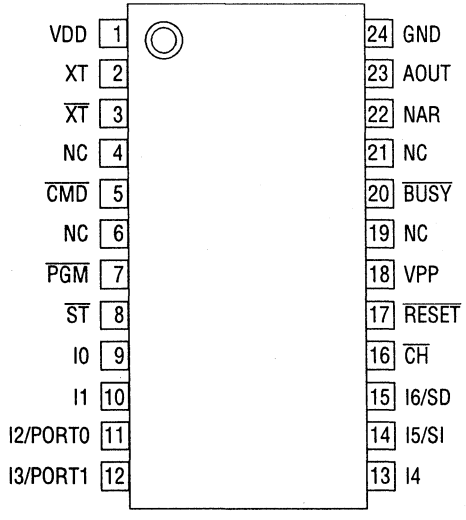


MSM6652~6656 (Mask ROM)
18 Lead Plastic DIP

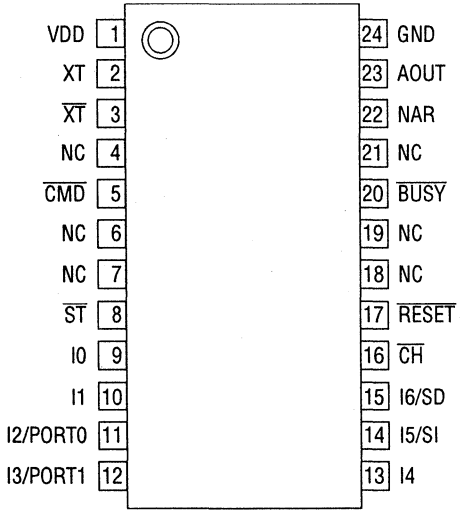


Note: Applicable to MSM66P54-01/02/03/04RS

MSM66P54 (OTP)
24 Lead Plastic SOP

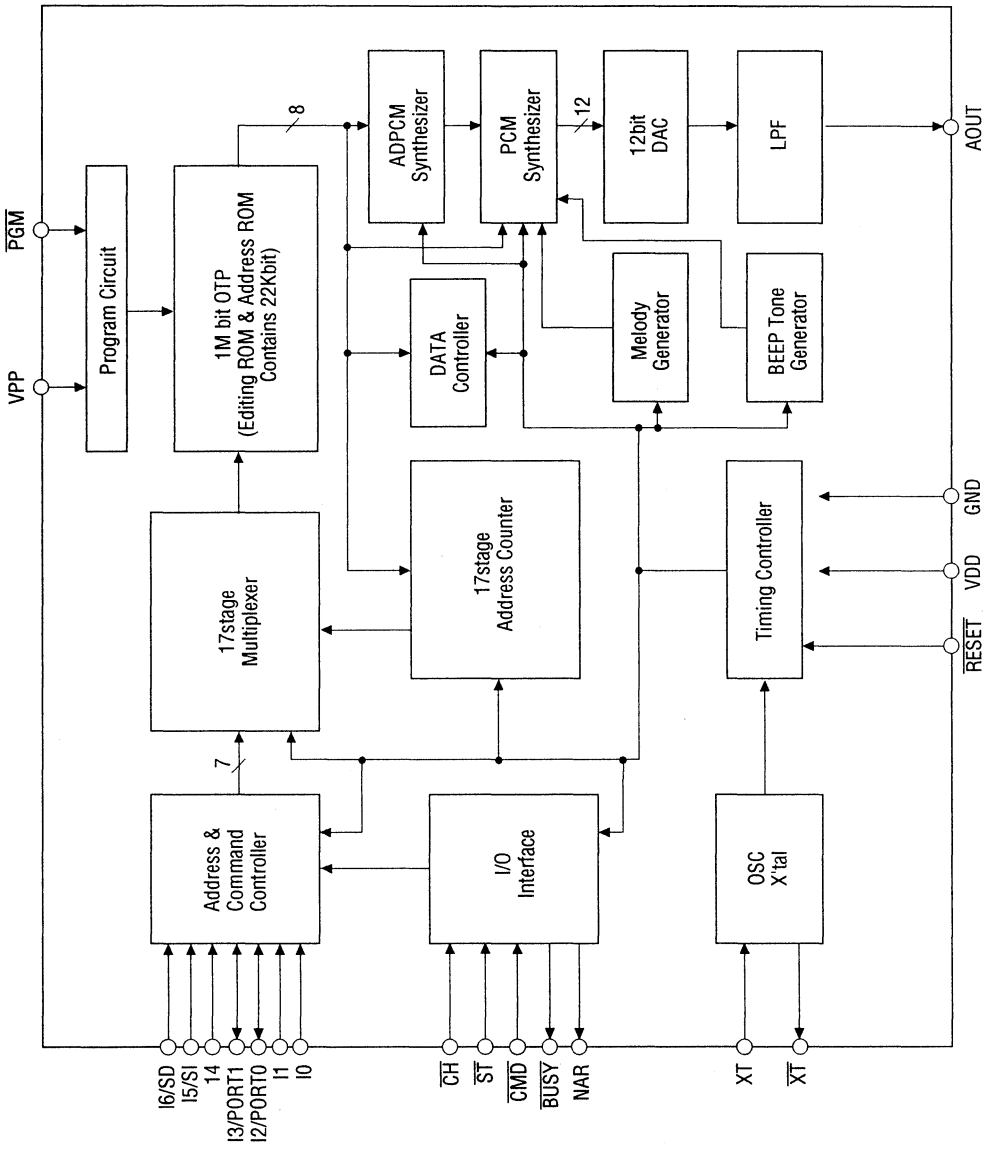


MSM6652~6656 (Mask ROM)
24 Lead Plastic SOP



Note: Applicable to MSM66P54-01/02/03/04GS-VK

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operation Range

(GND = 0V)

Parameter	Symbol	Condition	Limits			Unit
Power Supply Voltage	V_{DD}	—	+3.5 ~ +5.5			V
Operating Temperature	T_{op}	—	-10 ~ 70			°C
Original Oscillation Frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -10 ~ 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -40μA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 40μA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	μA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-200	90	-30	μA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	μA
"L" Input Current 2	I_{IL2}	Internal pullup resistance pin	30	90	200	μA
Operating Current Consumption	I_{DD}	–	–	6	20	mA
Standby Current Consumption	I_{DS}	–	–	–	100	μA
DA Output Relative Accuracy	$\lvert V_{DAE} \rvert$	When DA output selected	–	–	40	mV
DA Output Impedance	R_{DAO}	When DA output selected	15	30	45	kΩ
LPF Load Resistance	R_{AOUT}	When LPF output selected	50	–	–	kΩ

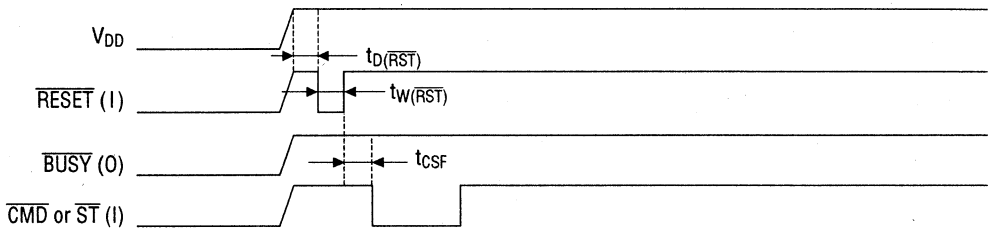
AC CHARACTERISTICS

(V_{DD} = 5.0V, GND = 0V, Ta = -10 ~ 70°C)

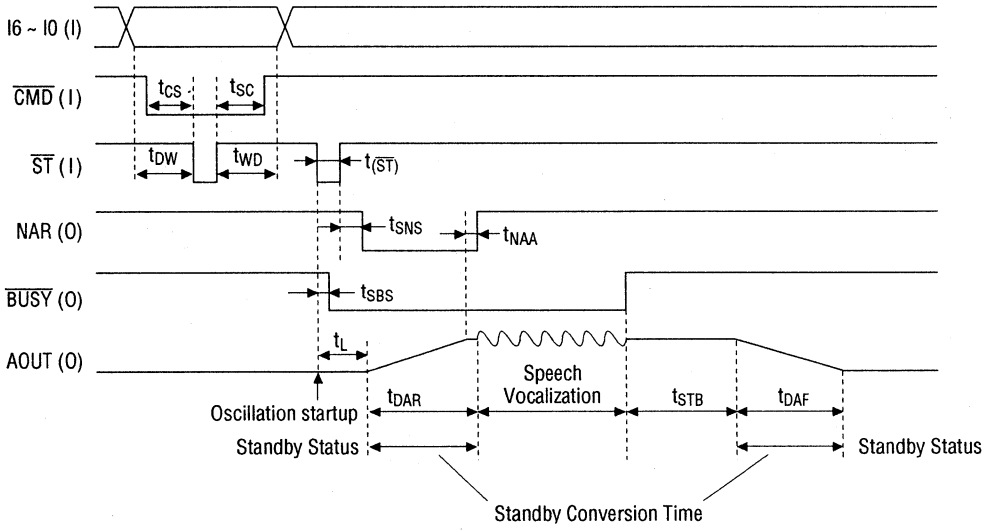
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{RESET}$ Input Pulse Width	$t_{W(\overline{RST})}$	–	10	–	–	µS
$\overline{RESET}$ Input Time after Power on	$t_{D(\overline{RST})}$	–	0	–	–	µS
$\overline{ST}$ Input Pulse Width	$t_{(\overline{ST})}$	–	0.35	–	2000	µS
Data Set Time	t_{DW}	–	1	–	–	µS
Data Hold Time	t_{WD}	–	1	–	–	µS
$\overline{CMD}$ Setup Time (1)	t_{CSF}	When power is turned ON	1	–	–	µS
$\overline{CMD}$ Setup Time (2)	t_{CS}	–	1	–	–	µS
$\overline{CMD}$ Hold Time	t_{SC}	–	1	–	–	µS
$\overline{CH}$ Setup Time	t_{CHS}	–	1	–	–	µS
$\overline{CH}$ Hold Time	t_{SCH}	–	1	–	–	µS
Serial Clock Pulse Width	$t_{W(SCK)}$	When using serial input option	0.35	–	–	µS
Serial Clock Setup Time	t_{SIS}	–	1	–	–	µS
Serial Clock Hold Time	t_{SSI}	–	1	–	–	µS
Serial Data Setup Time	t_{SDS}	When using serial input option	1	–	–	µS
Serial Data Hold Time	t_{SSD}	When using serial input option	1	–	–	µS
$\overline{BYSY}$ Output Time (1)	t_{SBS}	–	–	–	10	µS
$\overline{BUSY}$ Output Time (2)	t_{BN}	When fsam = 8kHz	350	375	400	µS
NAR Output Time (1)	t_{SNS}	–	–	–	10	µS
NAR Output Time (2)	t_{NAA}	When fsam = 8kHz	350	375	400	µS
NAR Output Time (3)	t_{NAB}	When fsam = 8kHz	350	375	400	µS
NAR Output Time (4)	t_{NAC}	When fsam = 8kHz	350	375	500	µS
DA Converter Change Time	t_{DAR}, t_{DAF}	–	60	64	68	mS
LPF Stable Time	t_L	–	6	8	10	mS
Standby Conversion Time (after speech ends)	t_{STB}	–	0.45	0.5	0.55	sec.

TIMING CHART

1.When Power is Turned ON

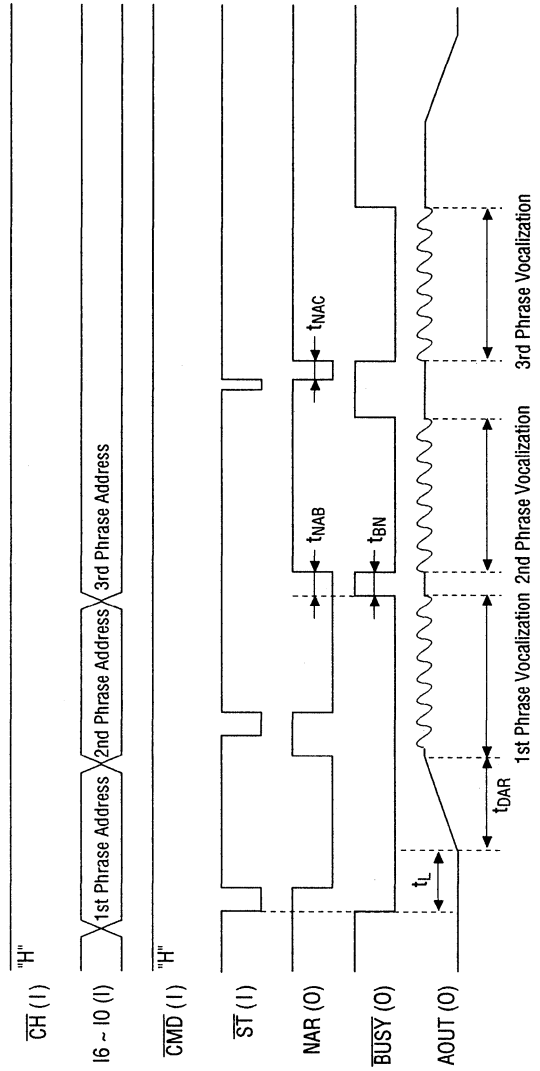


2.When LSI Starts Up and is in Standby Status

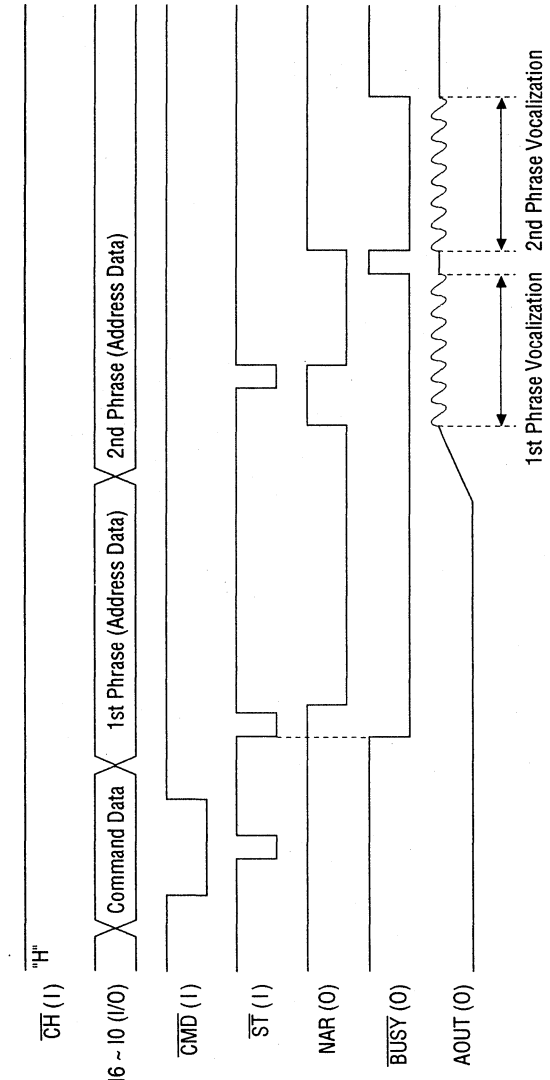


3.Channel 1 Regeneration Timing Chart

when External Command is not used (Parallel Input)

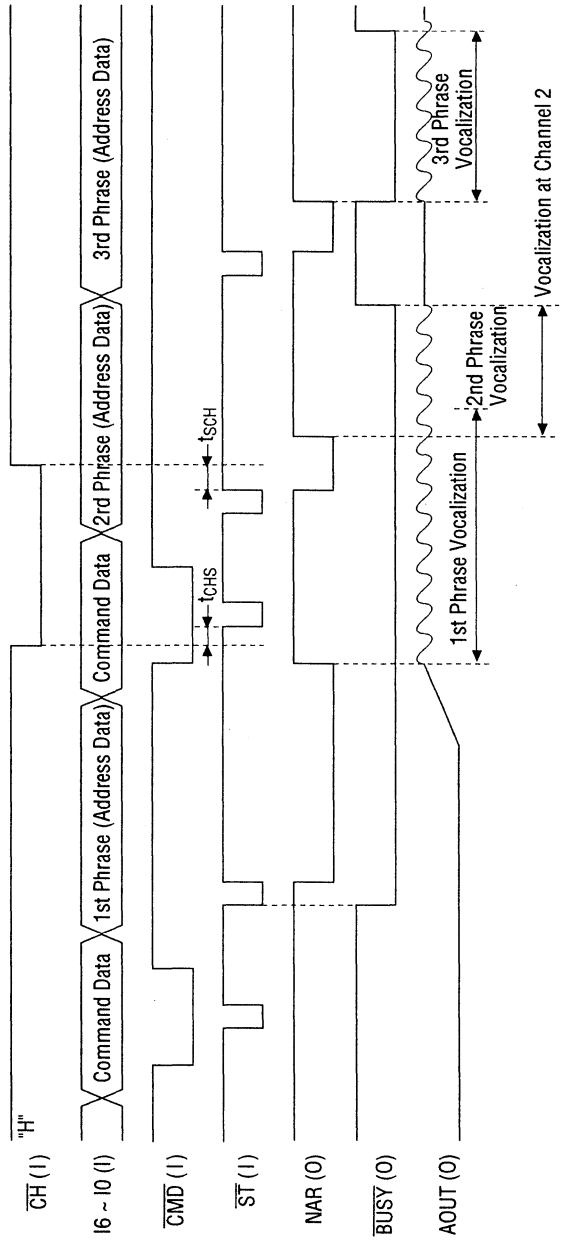


4.Channel 1 Regeneration Timing Chart when External Command is used (Parallel Input)



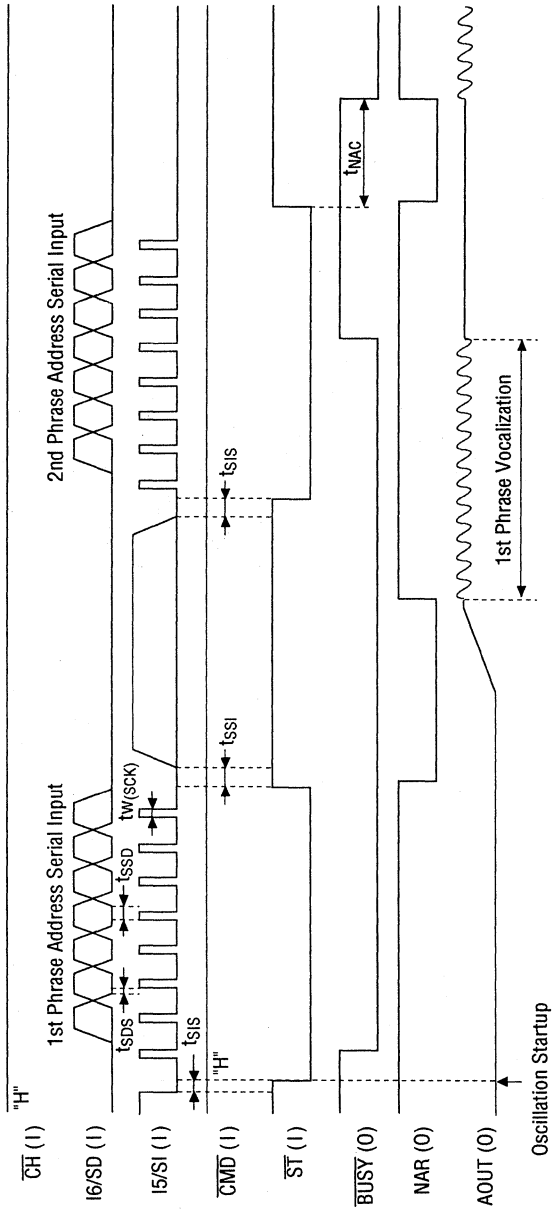
If a command is set externally the status set is maintained until the next command is set. Therefore, if the 1st and 2nd phrases are vocalized at the timing shown above, speech for both phrases is first vocalized in the status set by that command. To vocalize command content that was changed, be certain to input command data before inputting address data. The command input can be continuously set many times until address input. However, the setting of the command inputted last becomes valid (common with 1 and 2 channel regenerations).

5.Channel 1, Channel 2 Regeneration Timing Chart when External Command is used (Parallel Input)



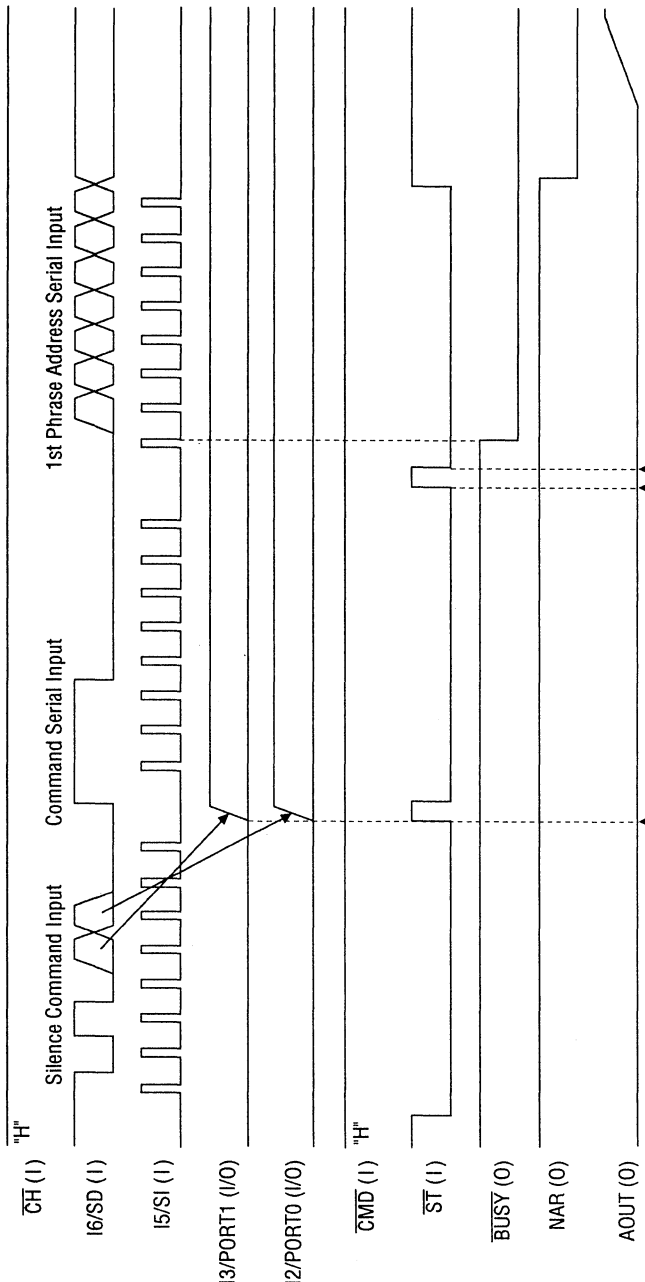
Since command data is maintained independently at channels 1 and 2, If speech is started up at channel 1 without a command setting, speech is vocalized by the same command set at the 1st phrase.

6.Regeneration Timing Chart when External Command is not used (Serial Input)



In serial input, data is transferred to the LSI when the $\overline{ST}$ signal rises after serial data is input.
SD is captured at the former edge of SI.

7.Regeneration Timing Chart when External Command is used (Serial Input)



In serial input, port output can be set by a command setting. Since a port output command and internal command are shared, if a command is set for port output, set the command for speech again to input address data. If address data is input without setting the command, the LSI recognizes it as silence insertion code. The command input can be continuously set many times until address input. However, the setting of the command inputted last becomes valid (common with 1 and 2 channel regenerations).

PIN DETAILS

Pin Name	I/O	Function
$\overline{\text{RESET}}$	I	LSI is in standby status if set to "L" level. At this time oscillation stops and AOUT output becomes GND , and returns to initial status . LSI has internal power on reset . To operate power on reset correctly startup power within 1 ms . If not, apply $\overline{\text{RESET}}$ pulse when power is turned on . This pin has internal pullup resistor .
$\overline{\text{BUSY}}$	O	Outputs "L" level during vocalization. In "H" level when power is turned ON.
NAR	O	$\overline{\text{CMD}}$, $\overline{\text{ST}}$ input becomes effective when NAR is at "H" level. If CH pin is in "H" level, NAR becomes a channel 1 status signal. If in "L" level NAR becomes a channel 2 status signal. NAR signal indicates whether register I6 to I0 address of address/comma nd controller (see block diagram) is in open status. "H" level indicates open status. NAR is in "H" level when power is turned ON.
AOUT	O	Analog speech output pin. DA converter output or LPF output can be selected by a command input.
GND	–	Ground pin
VDD	–	Power pin
XT	I	Ceramic oscillator connection pin. Pin has internal 0.5 to 5MΩ feedback resistor between XT and $\overline{\text{XT}}$. Input from this pin when using external clock.
$\overline{\text{XT}}$	O	Ceramic oscillator connection pin. Set to open to use external clock.
$\overline{\text{CMD}}$	I	Command input and option setting control pin. Command and option input is enabled if $\overline{\text{ST}}$ pin is set to "L" level when $\overline{\text{CMD}}$ pin is in "L" level. Set to "H"level when $\overline{\text{CMD}}$ is not used and when using serial input interface. This pin has internal pullup resistor.

Pin Name	I/O	Function
$\overline{ST}$	I	Speech synthesis starts at fall of $\overline{ST}$, I6 to I0 addresses are captured at rise of $\overline{ST}$. Input $\overline{ST}$ when NAR of channels 1 and 2 status signals are "H". This pin has internal pullup resistor.
$\overline{CH}$	I	Channel control signal. Channel 1 input is in "H" level, channel 2 input is in "L" level. This pin has internal pullup resistor.
I6/SD	I	Command and user specified phrase input pin when parallel input is optionlly selected. A serial data (command and address) input pin when serial input is optionally selected.
I5/SI	I	Command and user specified phrase input pin when parallel input is optionlly selected. A serial clock input pin when serial input is optionally selected.
I4	I	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, leave this pin at "L" level. This pin has pin pulldown resistor.
I3/PORT1	I/O	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, this pin becomes a port output pin. Output from the port varies by command input from the microcontroller.
I2/PORT0	I/O	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, this pin becomes a port output pin. Output from the port varies by command input from the microcontoroller.
I1,I0	I	Command and user specified phrase input pin when parallel input is optionally selected. When serial input is optionally selected, leave this pin at "L" level. This pin has internal pulldown resistor.
Vpp	–	Power supply voltage pin for write in on-chip OTP. Set to "H" or open in repla y.
$\overline{PGM}$	I	Interface pin for speech analysis tool AR76-202. Set to "L" or open in repay. This pin has internal pull-down resistor.

Note: See the pages described about on-chip mask ROM products from the MSM6652 to the MSM6656 for more detailed functions.

OKI Semiconductor

MSM6650

External ROM Drive Speech Synthesis LSI

GENERAL DESCRIPTION

MSM6650, a successor to OKI's MSM6376 speech synthesis LSI, can externally store data by directly connecting a maximum 64 Mbit ROM or EPROM. The PCM method is added to the ADPCM method, a 12-bit DA converter and a -40 dB/oct low pass filter are built-in, insuring high quality speech synthesis sound.

The conventional "BEEP" tone and a 2-channel mixing function are now easier to use, and a melody function, fadeout function and random vocalization function are now included. External control is easier than before due to the addition of an edit ROM that can form sentences by linking phrases.

MSM6650 can support various applications since a standalone or microcomputer interface can be selected option by a pin.

Also for control, serial input minimizes the number of microcomputer ports.

Since MSM6650 has the same internal ROM speech synthesis LSI circuit configuration as MSM6652, MSM6653, MSM6654, MSM6655 and MSM6656, it is an appropriate LSI to evaluate internal ROM speech synthesis LSIs.

The general differences between the MSM6650 family and the MSM6375 family follow.

	MSM6650 Family	MSM6375 Family
Interface	Standalone/microcomputer	SW input/CPU input
Speech Synthesis Method	4bit ADPCM / 8bit PCM / Melody PCM	4bit ADPCM
BEEP Tone Output Frequency Duration	0.5 kHz/1.0 kHz/1.6 kHz/2.0 kHz Arbitrary (16 ms~2100 ms)	1.0 kHz/2.0 kHz Fixed (64 ms/128 ms/250 ms/500 ms)
Sampling Frequency (fsam)	4.0 kHz/5.3 kHz/6.4 kHz/8.0 kHz 10.6 kHz/12.8 kHz/16.0 kHz/32.0 kHz	4.0 kHz/6.4 kHz/8.0 kHz (f_{OSC} = 64 kHz) 16.0kHz/25.6kHz/32.0kHz (f_{OSC} = 256 kHz)
Original Oscillation Frequency (fosc)	256 kHz (RC)/4.096 MHz (X'tal)	40 kHz ~ 256 kHz
LPF Attenuation Factor	-40 dB/oct	-24 dB/oct
LPF Cutoff Frequency f_{CUT} (kHz)	f_{CUT}: 1.8 | 2.6 | 2.6 | 3.2 | 4.2 | 5.1 | 6.4 | 12.8 f_{sam}: 4.0 | 5.3 | 6.4 | 8.0 | 10.6 | 12.8 | 16.0 | 32.0	f_{CUT}: 1.5 | 3.0 | 3.0 f_{sam}: 4.0 | 6.4 | 8.0
Maximum No. of Phases	127	111
Pullup/Pulldown Resistor	Yes	No
Standby Conversion Time	0.2 sec	3.0 sec
Maximum External ROM	64 Mbit	16 Mbit
Additional Functions	Edit ROM Fadeout Random vocalization Melody regeneration PCM regeneration Serial input/Port output	–

See the related Data Book for details on differences.

The MSM6650 is roughly classified into a standalone and microcomputer interface type. Since both types are separately explained in data book, refer to the table of contents below for the appropriate page(s).

Table of Contents

Standalone

Microcomputer Interface

(1) STANDALONE MODE

FEATURES

4bit ADPCM method/8bit PCM method
Melody function
Edit ROM function
2-channel mixing function
Internal random vocalization function
Fadeout function (4-step change of sound volume)

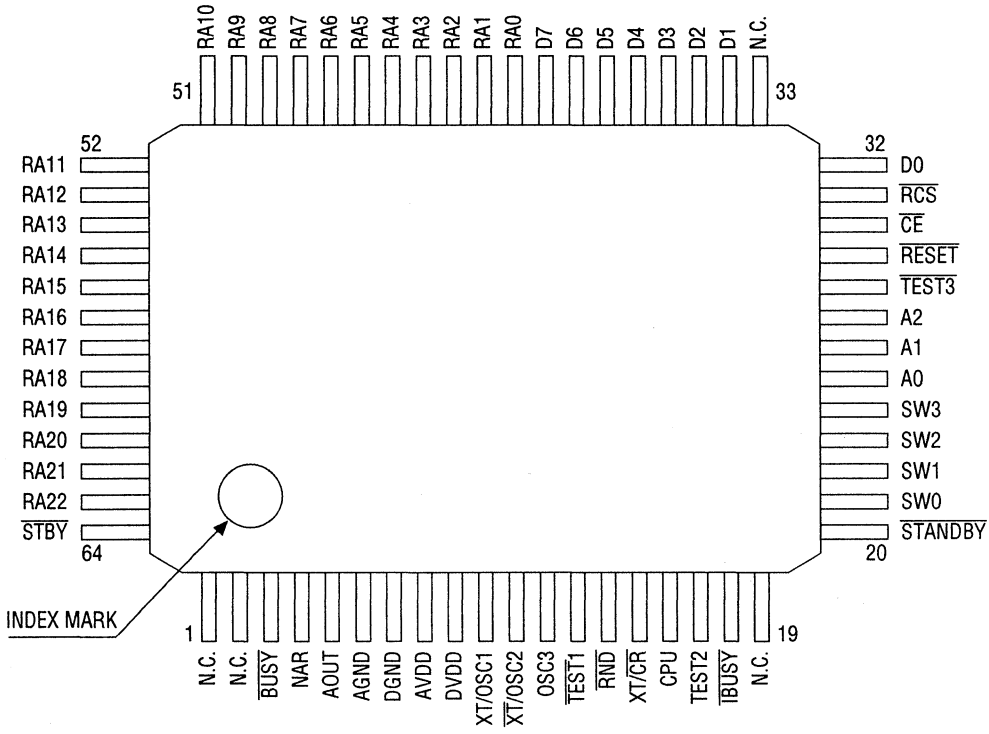
Internal BEEP Tone	BEEP tones of 0.5 kHz, 1.0 kHz, 1.6 kHz and 2.0 kHz can be generated by specification code.
Sampling Frequencies	4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz 1)
	Note 1) 32.0 kHz cannot be selected if RC oscillation is selected.
Maximum phrases	: 120

Internal 12-bit D/A converter
Internal LPF attenuation factor : -40 dB / oct
Internal standby function
RC oscillation or ceramic oscillation can be selected
Package : 64-pin FLAT (QFP64-P-1420-V1K)

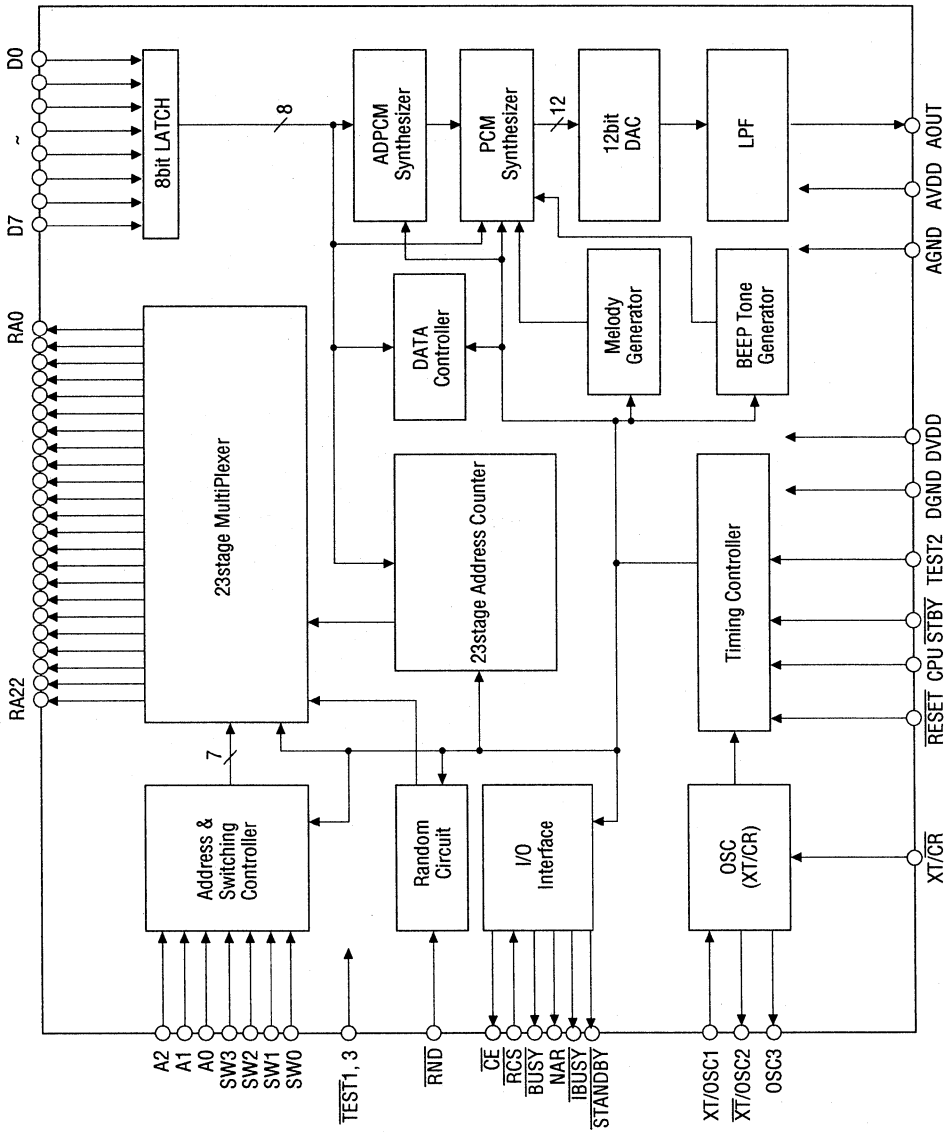
PIN CONFIGURATION

(Top View)

64 Lead Plastic QFP



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operation Range

(GND = 0V)

Parameter	Symbol	Condition	Limits			Unit
Power Supply Voltage	V_{DD}	LPF output	+2.7 ~ +5.5			V
Operating Temperature	T_{op}	–	-40 ~ 85			°C
			Min.	Typ.	Max.	
Original Oscillation Frequency (1)	f_{OSC1}	When XT selected	3.0	4.096	4.5	MHz
Original Oscillation Frequency (2)	f_{OSC2}	When RC selected[1)]	200	256	300	kHz

Note 1: The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the C and R of the external parts.

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-200	-90	-30	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2	I_{IL2}	Internal pullup resistance pin	30	90	200	µA
Operating Current Consumption	I_{DD}	–	–	6	10	mA
Standby Current Consumption	I_{DS}	–	–	–	10	µA
LPF Driving Resistance	R_{AOUT}	–	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	I_F=100µA	–	1	3	kΩ

DC Characteristics

(V_{DD} = 3.1V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	V_{IH}	–	2.7	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	2.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-100	-30	-10	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2	I_{IL2}	Internal pullup resistance pin	10	30	100	µA
Operating Current Consumption	I_{DD}	–	–	4	7	mA
Standby Current Consumption	I_{DS}	–	–	–	1	µA
LPF Driving Resistance	R_{AOUT}	–	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	I_F=100µA	–	1	3	kΩ

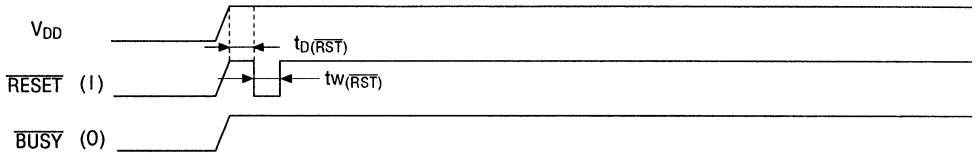
AC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

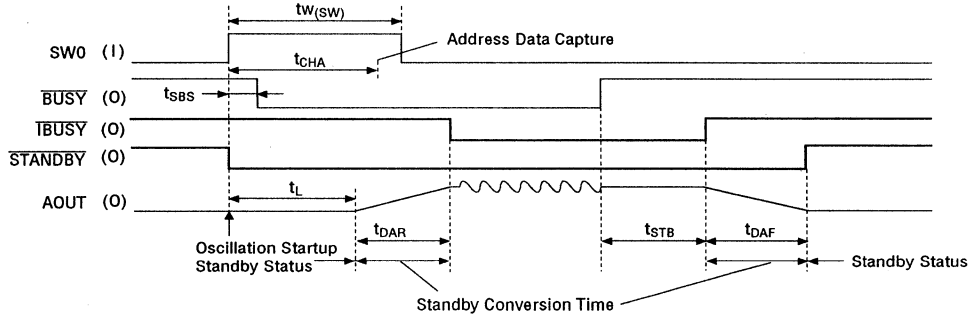
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$tw_{(\overline{RST})}$	–	10	–	–	∝S
RESET Input Time after Starting up Power	$t_{D(\overline{RST})}$	–	0	–	–	∝S
$\overline{\text{RND}}$ Input Pulse Width	$tw_{(\overline{RAN})}$	Function Detailes 4.2	100	–	–	µS
SW3-SW0 Input Pulse Width	$tw_{(SW)}$	–	16	–	–	mS
$\overline{\text{BUSY}}$ Output Time (1)	t_{SBS}	–	–	–	10	∝S
$\overline{\text{BUSY}}$ Output Time (2)	t_{BN}	When fsam = 8kHz	350	375	400	∝S
Chattering Prevention Time	t_{CHA}	–	14	15	16	mS
DA Converter Change Time	t_{DAR},t_{DAF}	–	60	64	68	mS
LPF Stabilization Time	t_L	–	6	8	10	mS
Standby Conversion Time	t_{STB}	–	0.15	0.20	0.25	S
Capture Random Address Time	t_{RA}	Function Detailes 4.2	16	32	48	µS

TIMING CHART

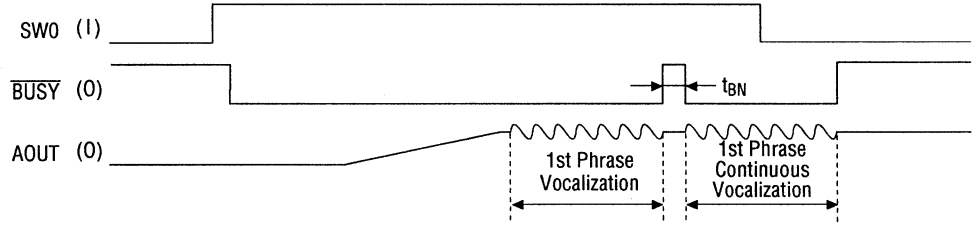
1.When Power Is Turned On



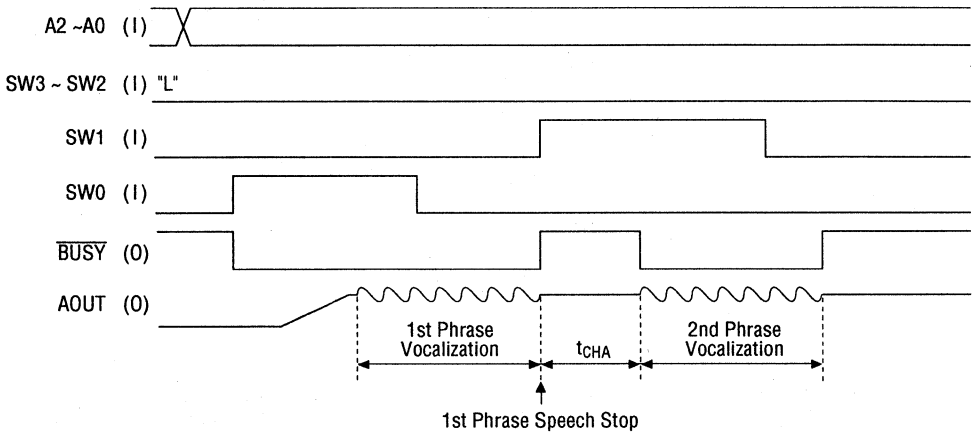
2.When LSI Starts Up And Is In Standby Status



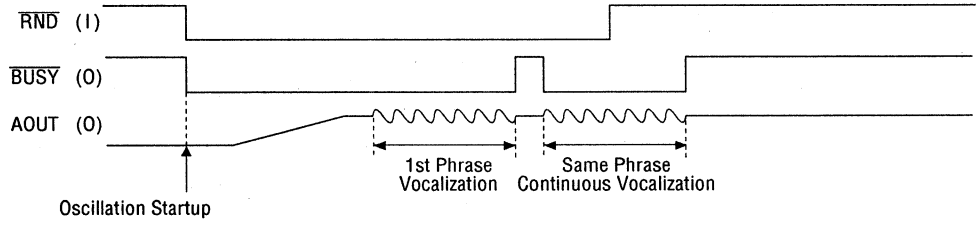
3.Repeat Vocalization Timing Chart



4.Timing Chart When SW3~SW0 Are Changed During Vocalization



5.Repeat Vocalization Timing Chart Of Random Vocalization



PIN DETAILS

Pin Name	I/O	Function
$\overline{BUSY}$	O	Outputs "L" level during vocalization. In "H" level when power is turned ON.
NAR	O	Status signal for microcomputer interface. Set to open for standalone.
AOUT	O	Speech output pin of internal LPF.
AGND	–	Analog ground pin.
DGND	–	Digital ground pin.
AVDD	–	Analog power pin.
DVDD	–	Digital power pin.
XT/OSC1	I	Ceramic oscillator connection pin when ceramic oscillator is selected. RC connection pin when RC pin oscillation is selected. Input from this pin if external clock is used.
$\overline{XT}$/OSC2	O	Ceramic oscillator connection pin when ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Set to open if external clock is used. Outputs "L" level in standby status.
OSC3	O	Set to open if ceramic oscillator is selected. RC connection pin when RC oscillation is selected. Outputs "H" level in standby status when RC oscillation is selected.
$\overline{RND}$	I	Random vocalization starts if $\overline{RND}$ pin is set to "L" level. Captures address from random address generation circuit in LSI at fall of $\overline{RND}$. Set to "H" level if random vocalization function is not used. This pin has internal pullup resistance.
XT/$\overline{CR}$	I	X'tal/RC selectable pin. Set to "H" level if ceramic oscillator is used. Set to "L" level if RC oscillation is used. 32kHz sampling frequency can not be used when RC oscillation is selected.
CPU	I	Set to "L" level if standalone is used.
$\overline{TEST}$ 1~3	I	Test pins. Set to "H" level. $\overline{TEST}$1, 3 terminals have internal pullup resistance.
TEST 2	I	Test pin. Set to "L" level.
SW3~SW0	I	Phrase input pins corresponding to vacalized sound. If input changes, SW3~SW0 pins capture addresses after 16 ms, and starts speech synthesis. This pin includes a pulldown resistor.
A2~A0	I	Phrase input pins corresponding to vacalized sound. A0 input becomes invalid if the random vocalization function is used.
$\overline{IBUSY}$	O	Output "L" level excepting standby conversion time , during voice regeneration or 1/2 VDD level of AOUT pin .
$\overline{STANDBY}$	O	Output "L" level , when the LSI is oscillating .
$\overline{RESET}$	I	LSI is in standby status if set to "L". At this time oscillation stops and AOUT output becomes GND, and returns to initial status. LSI has internal power ON reset. To operate power ON reset correctly startup power within 1 mS If not, apply $\overline{RESET}$ pulse when power is turned ON. This pin has internal pullup resistance.

Pin Name	I/O	Function
$\overline{CE}$	O	Timing output pin to control read of external memory. Outputs when $\overline{RCS}$ is in "L" level.
$\overline{RCS}$	I	Address and $\overline{CE}$ are output from RA22~RA0 if this pin is in "L" level. RA22-RA0 address pins and $\overline{CE}$ become high impedance status if this pin is in "H" level. D7-D0 do not receive external signals and values are internally pulled down.
D7~D0	I	Pins to input data to external memory. Data is input when $\overline{RCS}$ is in "L" level. If $\overline{RCS}$ is in "H" level these pins internally become "L" level without receiving external data.
RA22~RA0	O	Address pins of external memory, output when $\overline{RCS}$ is in "L" level. These pins become high impedance status if $\overline{RCS}$ is in "H" level.
$\overline{STBY}$	I	If set to "L" level status enters standby 0.2 sec after speech ends. If set to "H" level status maintains 1/2 V_{DD} after speech ends.

FUNCTION DETAILS

1. VOCALIZATION CODE SPECIFICATION

The user can specify a maximum of 120 phrases. Table 1.1 shows the settings by A2~A0 and SW3~SW0.

Table 1.1 User Specified Phrase List

A2 ~ A0	SW3 ~ SW0	Code Description
000	0000	Forbidden Code
⟆	0001	User-Specified Phrase
111	⟆	
	1111	(120 phrases)

2. PULLUP and PULLDOWN

The $\overline{\text{RESET}}$, $\overline{\text{RND}}$ and $\overline{\text{TEST1}}$, 3 pins have internal pullup resistors and the pins from SW3 to SW0 have pulldown resistors.

3. OPTION(S)

In standalone the XT/$\overline{\text{CR}}$ pin can be used to select the oscillation circuit. If this pin is set to "H" level the circuit is in ceramic oscillation or X'tal, conversely, if set to "L" level, the circuit is in RC oscillation.

In the case of RC oscillation, however, a 32 kHz sampling frequency cannot be used.

4. STANDALONE MODE

In standalone mode, the complete SW input interface function and the random vocalization function can be used.

4.1 Complete SW Input Interface

With the complete SW input interface, speech synthesis starts when SW3~SW0 pins have changed. However, to prevent chattering, the address at 16 ms (t_{CHA}) is captured after SW3~SW0 pins have changed. Speech synthesis does not start even if A2~A0 pins have changed.
Set the $\overline{\text{RND}}$ pin to "H" level if the random vocalization function is not used.
At the power supply , SW3~SW0 pins are all "L" .

The complete SW input interface is effective when operating MSM6650 using a push switch. Speech synthesis starts when an address is changed by pressing the push switch. If the push switch is released during vocalization, vocalization stops when the current vocalized phrase ends.

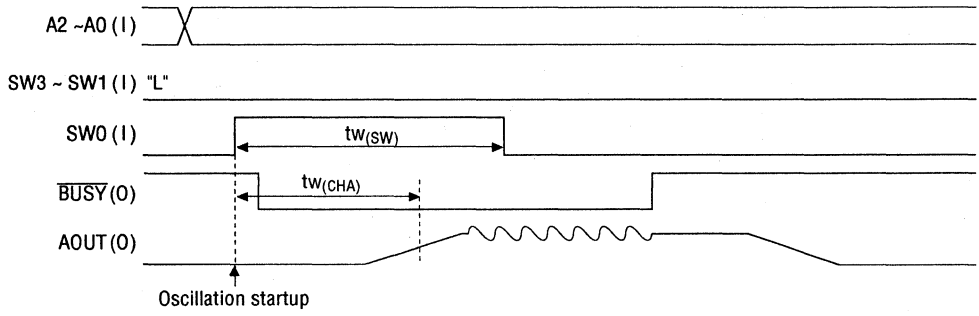


Figure 4.1 Complete SW Input Interface 1 Phrase Vocalization Timing

Figure 4.1 shows one phrase vocalization timing.

If the push switch is continuously pushed, the same phrase vocalization is repeated. Figure 4.2 shows repeat vocalization timing. Figure 4.3 shows vocalization timing when A2~A0 are changed during vocalization .

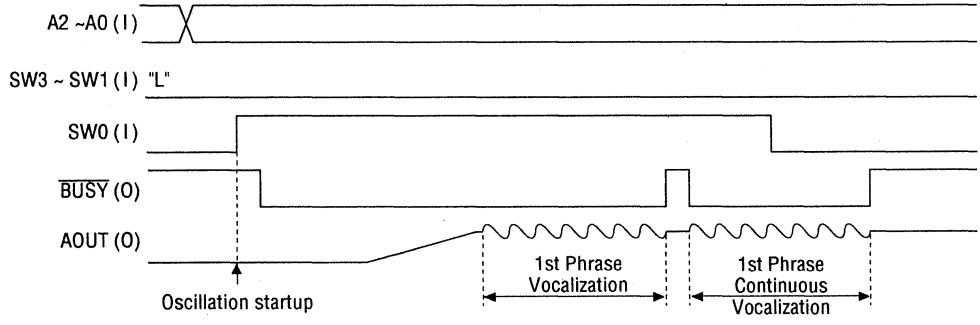


Figure 4.2 Complete SW Input Interface Repeat Vocalization Timing

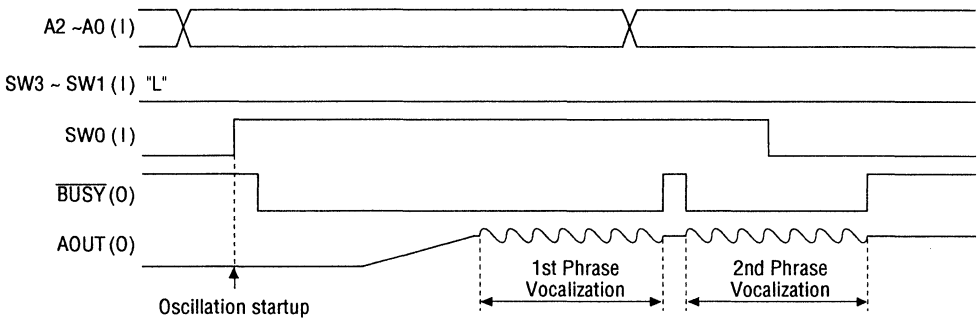


Figure 4.3 Complete SW Input Interface Repeat Vocalization Timing

If SW3~SW0 pins change during vocalization, vocalization stops and the next phrase is vocalized. For the next phrase vocalization, speech is first stopped and is synthesized after 16 ms of chattering prevention.

Figure 4.4 shows vocalization timing when SW3~SW0 are changed during vocalization.

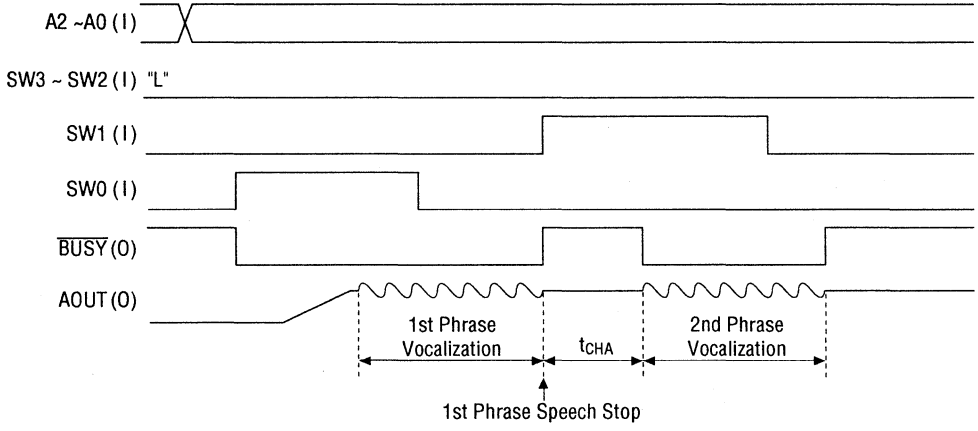


Figure 4.4 Vocalization Timing when SW3~SW0 Are Changed during Vocalization

If speech is started up at an address that is not used in the user specified phrase, AOUT reaches 1/2 VDD, but speech is not vocalized. Figure 4.5 shows the timing.

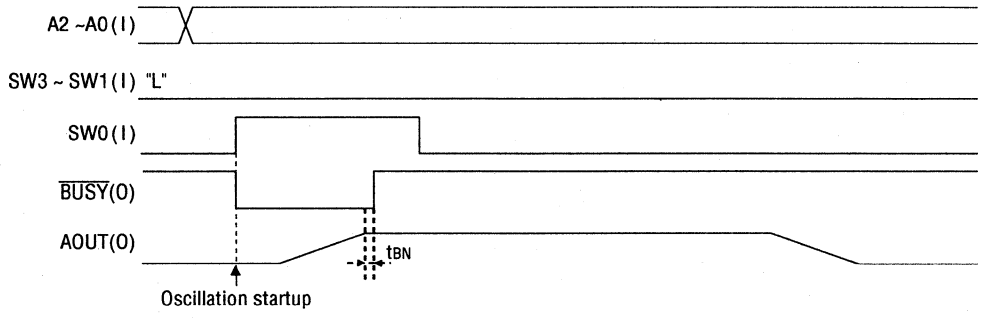


Figure 4.5 Timing when Speech Is Started up at an Address other than the User-Specified Phrase

In the complete SW interface, the addresses (SW8 ~ SW0) that do not start up always exist without fail. In power-on or $\overline{\text{RESET}}$ input, the addresses set to the SW3 ~ SW0 become the addresses that do not start up. Therefore, when the diode matrix is structured by using push switches, the maximum vocalization phrases become 120.

Combinations of A2 ~ A0: 8 kinds

When the addresses of no start-up from SW3 to SW0 are 0000:

$2^7 - 8 = 120$ (phrases)

4.2 Random Vocalization Function

The random vocalization function randomly generates 31 types of addresses corresponding to 5 bits of the addresses of A 0, and SW3~SW0 pins (except ALL "L") on the LSI, and vocalizes speech.

This means there is no external input to A0, SW3~SW0 pins. Since the A0 pin has no internal pullup/pulldown resistance, permanently set to "L" or "H".

Speech may not be vocalized if a phrase is not set to all 31 types of addresses. Caution is advised when creating ROM data.

For example, when 4 types of phrases, "sunny" (English: sunny), "raing", "cloudy", and "snowy" are vocalized, set the phrases shown in Table 4.1 to 31 types of addresses. The 4 types of phrases are then vocalized at random.

Table 4.1 Random Address Setup Example

A2, A1	A0, SW3 ~ SW0	Phrase
00	00001	Sunny
	00010	Rainy
	00011	Cloudy
	00100	Snowy
	00101	Sunny
	⟩	⟩
	11110	Rainy
	11111	Snowy

Random vocalization starts when the timing shown in Figure 4.6 is input to the $\overline{RND}$ terminal. When the LSI is oscillated random address is determined by the "H" level time of the pin. Random address is captured at the fall of the $\overline{RND}$ pin, and speech is vocalized. Therefore when power is turned ON, or when $\overline{RESET}$ is input, the phrase at fixed address "00001" is vocalized at the status that the random counter in the initial state is kept, and a random phrase is vocalized at a second or later time.

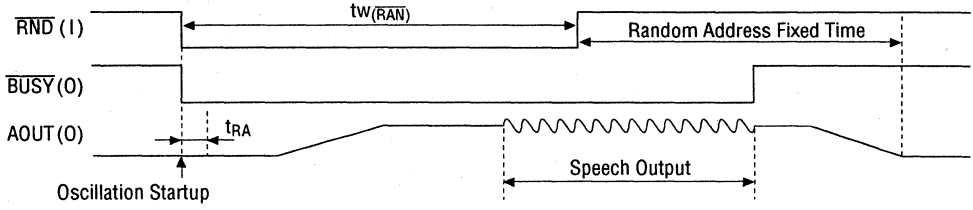


Figure 4.6 Random Address Capture

Table 4.2 Type of Address for Random Vocalization

A2, A1	A0, SW3 ~ SW0 (Note)	Code Description
00	00001 ⟨ 11111	Random Vocalization Address (31 Types)
01	Same as above	Same as above
10		
11		

Note: Address(es) corresponding to A0, SW3~SW0 pins.

For a random address, 31 phrases can be set to each "00", "01", "10" and "11" of A2 and A1 respectively.

In a random vocalization, 4 kinds of "0000000", "0100000", "1000000" and "1100000" in the phrases specified by users can not be used. Therefore, note this point when ROM data is prepared.

By changing the A2 and A1 pins as in Table 4.2, the probability or phrase combination for 4 types of random vocalizations can be changed.

A random address is set by the "H" level time of the $\overline{RND}$ terminal, therefore if the same pulse length is input by microcomputer, the random address determined time becomes constant, and a random phrase may not be vocalized.

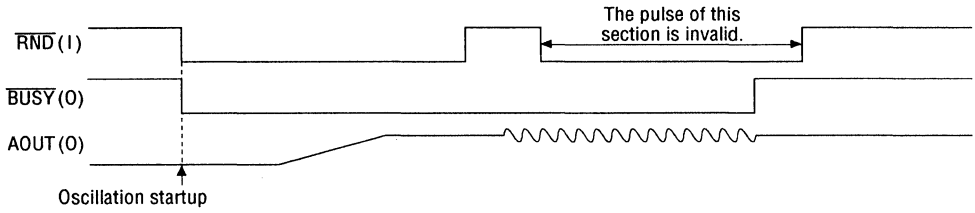


Figure 4.7 Timing when a Pulse Is Input to the $\overline{\text{RND}}$ Pin during Random Vocalization

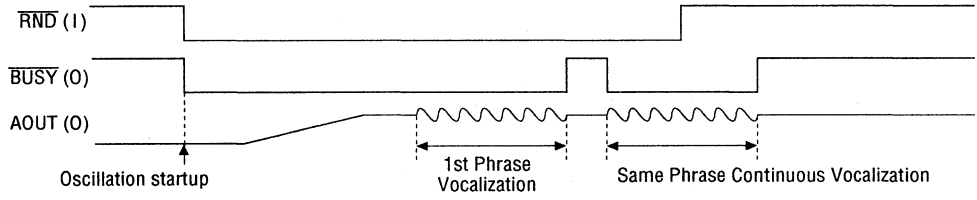


Figure 4.8 Repeat Vocalization Timing of Random Vocalization

As shown in Figure 4.7, if a signal of the $\overline{\text{RND}}$ pin during speech vocalization ("L" section of $\overline{\text{BUSY}}$) is risen, input to the $\overline{\text{RND}}$ pin during vocalization becomes invalid. If the $\overline{\text{RND}}$ pin is in "L" level and the $\overline{\text{RND}}$ pin is still in "L" level after the 1st phrase vocalization is over, as shown in Figure 4.8, the same phrase is vocalized repeatedly.

If SW3~SW0 are changed during random vocalization, speech during random vocalization stops, and speech of phrases that correspond to SW3~SW0 is vocalized.

Figure 4.9 shows the timing when SW3~SW0 are changed during random vocalization.

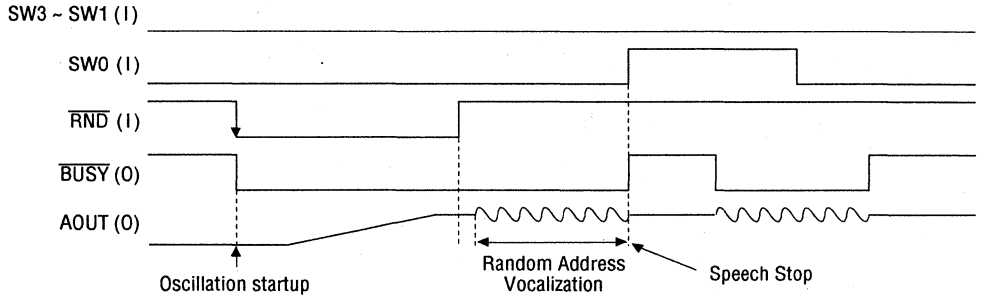


Figure 4.9 Timing when a Pulse Is Input to SW0 Pin during Random vocalization

Table 4.3 and Figure 4.10 show the address settings that quit random vocalization. These settings also stop vocalization when the "infinite repeat" command is in use under edit ROM.

Table 4.3 Type of address for Random Vocalization

A2, A1	A0, SW3 ~ SW0 (Note)	Code Description
00	00001 ↓ 11111	Random Vocalization Address (31 Types)
01	00001	Stop Address

Note: Addresses corresponding to A0, SW3~SW0 pins.

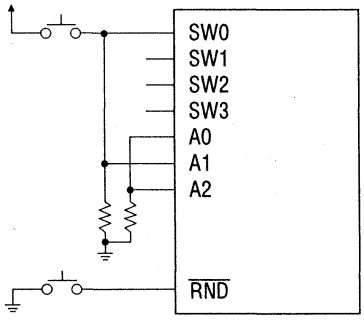


Figure 4.10 Circuit Example to Stop Random Vocalization

For example Table 4.3 shows that addresses other than random vocalization 0100001 are generated to stop vocalization.

A user specified address that is not used is used as a stop address, therefore the status can enter standby without vocalizing speech, also shown in Figure 4.5.

5. SAMPLING FREQUENCY

Sampling frequencies can be specified for each phrase in speech data of internal ROM. For channel synthesis, if channels 1 and 2 are regenerated at the same time, the channel 1 sampling frequency has priority.

For sampling frequency, the following 8 frequencies can be selected when creating speech data.

4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz

In standalone, RC oscillation and ceramic oscillation can be selected. If RC oscillation is selected however, only up to 32.0 kHz can be selected.

6. SPEECH VOCALIZATION TIME

Table 6.1 shows internal ROM configuration. The actual speech data ROM area is different from the indicated ROM capacity.

The speech data management area shown in Table 6.1 is about 6 Kbit, and the edit ROM area includes 16 Kbits.

Table 6.1 ROM Configuration

Speech Data Management Area
Editing ROM Area
Speech Data Area
Disabled Area

Use the following formula as a guide to compute speech vocalization time.

$$\text{Vocalization Time} = (\text{ROM Capacity} - 16 - 6) \times 1024 \times 255/256 \div \text{Bit Rate (kbps)}$$

For example, if data was created at a 4.0 kHz sampling using MSM6652 (288 Kbit internal ROM), the vocalization time is

$$(288 - 16\text{-}6) \times 1024 \times 255/256 \div 16(\text{kbps}) = 16.9 \text{ sec}$$

7. CHANNEL STATUS

The $\overline{\text{BUSY}}$ pin outputs the status signals. It outputs "L" level when either 1 or 2 is synthesizing speech. "H" level is output when power is turned ON.

8. REGENERATION METHOD

The MSM6375 series has only the ADPCM regeneration method, however to support various speech MSM6650 has 3 types of regeneration methods: ADPCM, PCM and melody regeneration. Respective features and how to select are explained below.

8.1 ADPCM Method

With the ADPCM (Adaptive Differential Pulse Code Modulation) method, basic quantization width Δ is adaptively changed for each sampling, and is encoded to 4bit data. This further improves the follow-up properties to speech wave forms.

Conversion to ADPDM data is performed by the AR76-202 analysis tool.

If the ADPCM method is used for human voices, animal cries and natural tones, the speech data capacity becomes smaller.

8.2 PCM Method

The PCM method of MSM6650 uses an 8-bit straight binary format. Of the three methods, PCM is the best for follow-up properties to speech wave forms.

This method is appropriate for sound effects where wave forms sharply change, and for pulse shaped wave forms.

8.3 Melody Regeneration Method

The AR761 analysis tool supports melody playback. The melody data can make an unique sound because musical notes can be composed by the AR761.

8.4 Bit Rate of Each Method

The bit rate shows the degree of data compression and the data amount to synthesize for 1 second. The bit rate is determined by the relationship between the sampling frequency and the data-amount-per-sample. The following formula is used.

Bit Rate (kbps) = Sampling Frequency (kHz) × Data-amount-per-sample (bit)

The bit rate of the three methods are compared below when the sampling frequency is 6.4 kHz.

1) ADPCM Method
   Bit Rate (kbps) = 6.4 kHz × 4 bit = 25.6 kbps

2) PCM Method
   Bit Rate (kbps) = 6.4 kHz × 8 bit = 51.2 kbps

3) Melody Regeneration Method
   With the melody regeneration method, the bit rate changes depending on each sound. The formula does not determine the bit rate changes. The average bit rate is 4 kbps.

8.5 The Regulations of channel synthesis about each regeneration mehtods

Melody regeneration and BEEP tones can not be regenerated in 2 channel side .
The regeneration of channel synthesis about each regeneraion methods as follows Table 8.1.

Table 8.1 The Regulations of channel Synthesis

1 Channel	2 Channel	Setting
ADPCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
ADPCM(0dB～-18dB)	ADPCM(0dB)	○ Note1)
ADPCM(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
ADPCM(0dB～-18dB)	PCM(0dB)	○ Note1)
ADPCM(0dB)	PCM(0dB～-18dB)	○ Note1)
ADPCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
ADPCM(0dB～-18dB)	SILENCE	○
MELODY(0dB)	ADPCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	ADPCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	MELODY(0dB～-18dB)	×
MELODY(0dB)	PCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	PCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	PCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
MELODY(0dB～-18dB)	SILENCE	○
PCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
PCM(0dB)	PCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
PCM(0dB～-18dB)	SILENCE	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	MELODY(0dB～-18dB)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	SILENCE	○
SILENCE	ADPCM(0dB～-18dB)	○
SILENCE	MELODY(0dB～-18dB)	×
SILENCE	PCM(0dB～-18dB)	○
SILENCE	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
SILENCE	SILENCE	○

Note1) In case of channel synthesis , confirm the voice quality with the MSM6650 evaluation board . Because occasionally there is possibility of straining the voice by recording level and synthesis phrases .

9. EDIT ROM

The role of edit ROM is to link phrases and build sentences, which makes an external microcomputer unnecessary. The conventional MSM6375 family could not link phrases and synthesis channels in standalone mode, but the MSM6650 family can using edit ROM.

For example: The phrase "Today's weather is...." is used to compare the MSM6375 family and MSM6650. With the MSM6375 family, individual data must be stored to phrase ROM (see Table 9.1) when individual phrases of "Today's weather is sunny", and "Today's weather is rainy" are vocalized by timing of one time.

On the other hand, the MSM6650 family can vocalize plural phrases for edit ROM function by timing of only one time. If the edit ROM has the phrase ROM of table 9.2, "Today's weather is sunny" will be vocalized by merely one time specifying address [01]. If address [02] is specified, "Today's weather is rainy" will be vocalized.

Conventionally data must be repeatedly stored to phrase ROM to vocalize "Today's weather is....", but the storage of overlapped data is not required as shown in table 9.2 by using edit ROM functions.

Table 9.1 Conventional Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's weather is sunny.
02	Today's weather is rainy.
03	Today's weather is sunny followed by cloudy, some areas are rainy
⟆	⟆
7F	

Table 9.2 Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's
02	weather
03	is
⟆	⟆
10	sunny
11	cloudy
12	rainy
13	snowy
20	occasional
21	followed by
22	some areas are
⟆	⟆
7F	

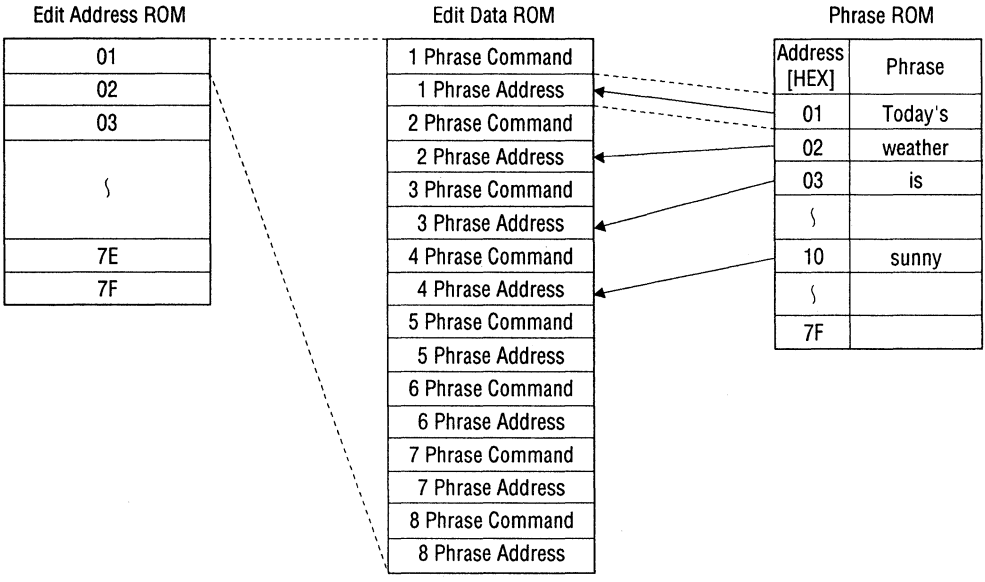
Table 9.3 Edit ROM Configuration

Address [HEX]	Edit Content [Max. 8 Phrases]
01	[01][02][03][10]
02	[01][02][03][12]
03	[01][02][03][10][21][11][22][12]
⟆	⟆
7F	

Edit ROM makes channel synthesis possible, a feature previously not available in standalone mode with the MSM6375 series. With edit ROM commands, phrase linking, channel synthesis, and "BEEP" tone or "silent" can be set.

A maximum of 8 phrases (16 bytes) can be set in 1 edit. Table 9.4 shows the configuration of edit ROM.

Table 9.4 Edit ROM Configuration



Edit address ROM can process a maximum of 127 user specified phrases. Table 9.4 shows the relationship between phrase ROM, edit data ROM, and edit address ROM.

Phrase ROM cannot be directly accessed if edit ROM is used.

Be certain to set commands in edit ROM. Settings cannot be omitted.

Edit ROM can be setup using the previously mentioned AR76-202 analysis tool. For regeneration using edit ROM, regeneration may not be the one requested. Be certain to check the speech using either the analysis tool or MSM6650 of external ROM.

Figure 9.1 shows the flow chart when creating edit ROM.

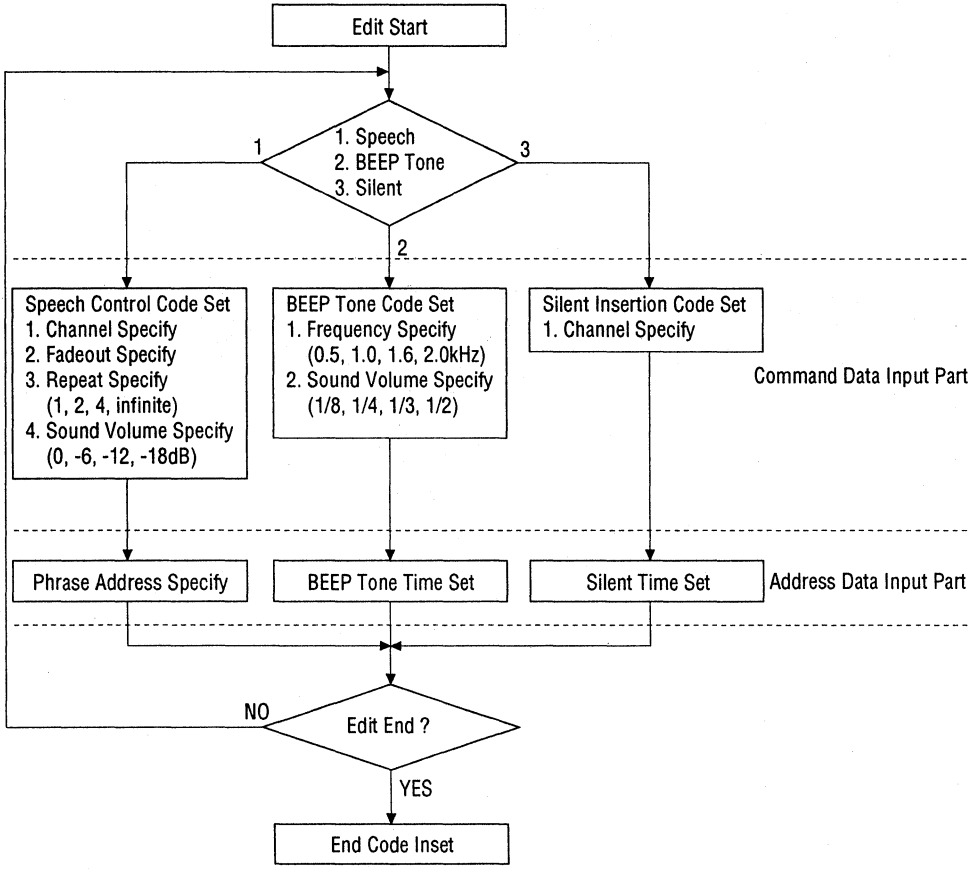


Figure 9.1 Edit Data ROM Creation Flow Chart

9.1 Edit ROM Commands

Table 9.5 shows the commands that can be set in edit ROM.

Table 9.5 List of Commands that can be set in Edit ROM

O7	O6	O5	O4	O3	O2	O1	O0	Command
0	0	0	0	0	0	0	0	End Code
ch	0	1	0	0	0	0	0	Silence Insertion Code
1	1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
ch	1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

The commands of the 4 codes shown in Table 9.5 are explained below.

9.1.1 End Code

End code means that one edit data is completed. Although this is necessary at the end of one edit data, since the LSI can recognize the end of editing, it is unnecessary when the maximum number of phrases are used.

9.1.2 Silence Insertion Code

Silence insertion code inserts silence to each channel, reducing speech data.

O7	O6	O5	O4	O3	O2	O1	O0
ch	0	1	0	0	0	0	0

The channel to insert silence is specified in command data, and silence time is set in address data.

The channel to insert silence is set to "O7" command data. If "O7" is "H" channel 1 is set, if "L" channel 2 is set.

Silence time is set at the address settings of phrases shown in Table 9.4.

Minimum Silence Time ... 16.384 ms
Maximum Silence Time ... 2.1 sec

The formula to set the silence time is shown below.

$t_{MU} = (2^6 \times (O6) + 2^5 \times (O5) + 2^4 \times (O4) + 2^3 \times (O3) + 2^2 \times (O2) + 2^1 \times (O1) + 2^0 \times (O0)) \times 16.384\text{ms}$

Table 9.6 Edit Data Example of Silence Insertion Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	0	1	0	0	0	0	0	Silence Insertion Code
2nd Byte	0	0	0	1	1	0	0	0	Silence Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 9.6, 393 ms of silence is inserted to channel 1.

9.1.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data.

The BEEP tone can be set only at channel 1.

To mix a BEEP tone and channel 2 vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz.

If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

The sound volume is set to O3, O2 and the frequency is set to O1, O0.

O7	O6	O5	O4	O3	O2	O1	O0
1	1	0	0	bl1	bl0	bf1	bf0

Tables 9.7 and 9.8 show the sound volumes and the frequencies that can be set.

Table 9.7 Sound Volume Settings

O3	O2	Sound Volume
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 9.8 Frequency Settings

O1	O0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

The BEEP tone time is set to the address setting of phrases shown in Table 9.4.

Minimum BEEP Tone Time ... 16.384 ms
Maximum BEEP Tone Time ... 2.1 sec

The formula to set a BEEP tone time is shown below.

$t_{BE} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384mS$

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	0	0	1	1	0	1	BEEP Tone Code
2nd Byte	0	0	0	1	1	0	0	0	BEEP Tone Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 9.9, a 1.0 kHz BEEP tone is vocalized at a 1/2 amplitude sound volume at channel 1 for 393 ms.

9.1.4 Speech Control Code

Speech control code can set repeat and sound volume.

O7	O6	O5	O4	O3	O2	O1	O0
ch	1	1	sm	rp1	rp0	vl1	vl0

The channel is set at "O7". If "O7" is "H", channel 1 is set, if "L" channel, 2 is set. The speech control condition of each channel is set between O4 to O0.

1) Setting Number of Repeats

The number of repeats is set at O3 and O2, and can be selected from 4 types: 1, 2, 4 and infinite. If infinite is selected, repeat can be stopped by switching to another phrase.

Table 9.10 shows the relationship between O3, O2 and the number of repeats.

Table 9.10 Number of Repeats Settings

O3	O2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "O4" is set to "H", sound volume during repeat is attenuated from 1 to 1/2, 1/4 and 1/8. This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at O1 and O0. Table 9.11 shows the correspondence.

Table 9.11 Attenuation Volume Setting

O1	O0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound volume is 1/8 of speech data)

9.2 PCM Regeneration in Edit ROM

For PCM regeneration, edit data is set together with speech control code. All settable items in speech control code (channel, sound volume smoothing during repeat, number of repeats, and sound volume) can be set.

9.3 Melody Regeneration in Edit ROM

For melody regeneration, edit data is set together with speech control code. Channels however cannot be set. Channel 1 is fixed. Channel 2 mixing of melody regeneration/melody regeneration combination is not possible.

All settable items in speech control code can be set except channels.

9.4 Random Vocalization in Edit ROM

If the $\overline{\text{RND}}$ pin is used during random vocalization, the 1st edit phrase (consists of edit data ROM up to 16 bytes) is vocalized and the random vocalization of the 2nd edit phrase then starts continuously.

However, this occurs only when the channel setting of the 1st and 2nd edit phrase are the same, and when echo regeneration and channel 2 regeneration are not performed. For example, if the 1st edit phrase is echo regeneration, and the 2nd edit phrase channel 1 regeneration, as shown in Figure 9.2 (1), 2 edit phrases overlap.

To avoid this, insert silence to channel 1, as shown in Figure 9.2 (2), and set edit data ROM so that channels 1 and 2 end regeneration at the same time.

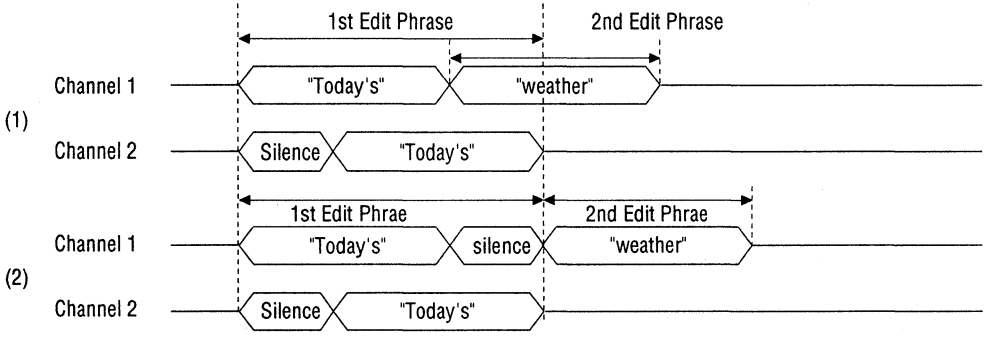


Figure 9.2 Example of Random Vocalization Timing

9.5 Channel 2 Mixing Function in Edit ROM

This function overlaps 2 phrases. By using edit ROM, it is easy to echo a phrase (echo regeneration) and to vocalize a phrase with a musical instrument sound or BGM (channel 2 regeneration).

9.5.1 Echo Regeneration

Echo regeneration delays and overlaps -6 dB attenuation (1/2 amplitude speech wave form of channel 1) to a speech wave form vocalized at channel 1.

ECHO REGENERATION OF 1 PHRASE

Using address [02] of phrase ROM, "weather", an echo regeneration edit data example is explained below.

Tabel 9.12 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
7th Byte	0	0	0	0	0	0	0	0	End code

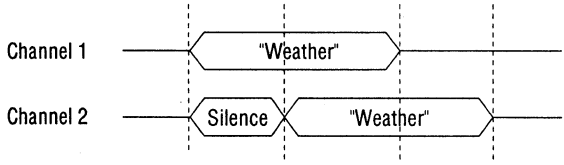
If edit data is set as in Table 9.12 , "weather" is vocalized at channel 1, and is overlapped and vocalized from channel 2 with a -6 dB attenuated sound volume 98.3 ms. later.

When 2 phrases overlap set the attenuation of the speech control command with attention to sound volume.

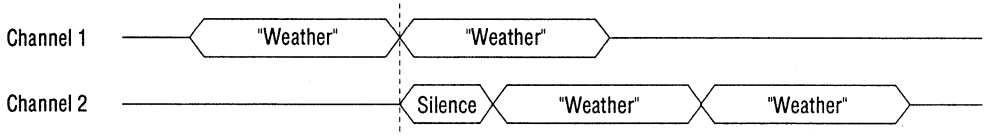
The silence time by silence insertion code is an element that influences the echo quality. Set the silence time so that the desired echo is created.

For channel synthesis in standalone, wave forms may be cramped due to the sound volume of the phrase. Check this with the AR761 analysis tool.

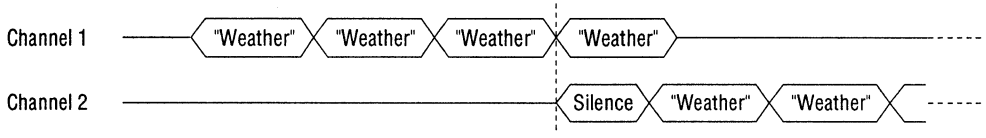
When performing echo regeneration set the number of repeats of the speech control command to 1. If 2, 4 or infinite is set, timing becomes as shown in Figure 9.3. This figure shows that the number of repeats of the 1st and 5th byte of edit data in Table 9.12 have changed.



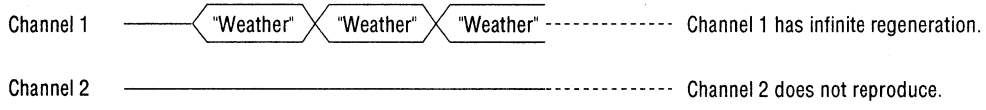
(1) Number of Repeats: 1



(2) Number of Repeats: 2



(3) Number of Repeats: 4



(4) Number of Repeats: infinite

Figure 9.3 Vocalization Timing of Echo Regeneration According to Number of Repeats

The vocalization timing, when the number of repeats of the speech control command is set for an edit data phrase, is explained below.

1 When number of repeats is set to 1

If the same channel is specified for the next phrase, vocalization of the next phrase starts when vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of vocalization.

2 When number of repeats is set to 2

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the second vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the second vocalization after the first vocalization ends.

3 When number of repeats is set to 4

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the fourth vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the fourth vocalization after the 3rd vocalization ends.

4 When number of repeats is set to infinite

The next phrase becomes invalid and is not vocalized regardless the channel specification.

Echo Regeneration of Multiple Phrases

A maximum of 8 phrases (16 bytes) are set to one edit data ROM. Up to 3 phrases are possible for an echo regeneration with 16 bytes. Set the phrase ROM so that the number of phrases do not exceed four. Using "Today's", "weather" and "is" of the phrase ROM in Table 9.2 as an example, Table 9.13 shows a three phrase echo regeneration edit data example, and Figure 9.4 shows vocalization timing.

Table 9.13 Three Phrase Echo Regeneration Edit Data Example

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting repeat once, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	0	0	0	1	0	Phrae Address (02H "weather")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
13th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
14th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
15th Byte	1	1	1	0	0	0	1	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
16th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")

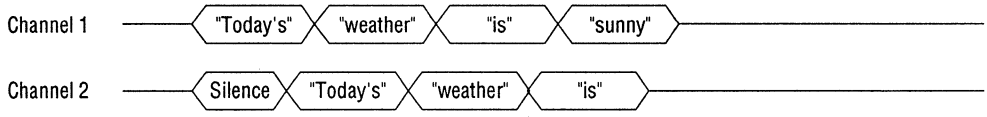


Figure 9.4 Vocalization Timing of a Three Phrase Echo Regeneration

For the echo regeneration of multiple phrases, set so that the sampling frequency of each phrase is the same. If a phrase with a different sampling frequency is mixed, the speech of channel 2 will become fast or slow because the sampling frequency of channel 1 has priority. Figure 9.5 shows the timing.

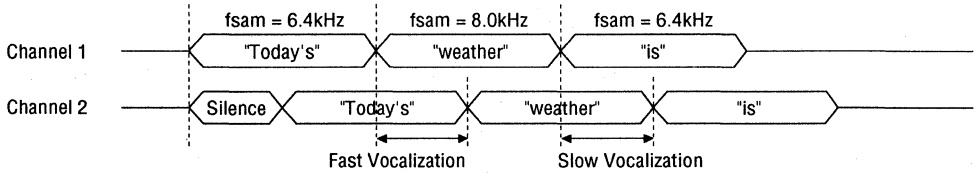


Figure 9.5 Vocalization Timing of Echo Regenerations with Different Sampling Frequencies

Echo Regeneration of an Arbitrary Phrase in Multiple Phrases

Table 9.14 shows an edit data example to apply echo to "is" in the four phrases of "Today's", "weather", "is" and "sunny".

Table 9.14 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	1	1	0	0	0	0	1	Silence Time (1.59 mS)
5th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting repeat once, -6 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (01H "weather")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	1	0	0	0	0	Phrae Address (10H "is")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")
13th Byte	0	0	0	0	0	0	0	0	End Code

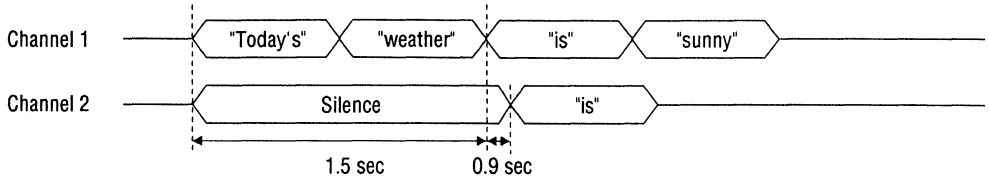


Figure 9.6 Vocalization Timing Using Edit Data of Table 9.14

As shown by the timing in Figure 9.6, "is" is echoed by setting the silence time, which is the addition of the vocalization time for "Today's" and "weather" and the delay time for echo to channel 2. If the silence time exceeds 2.1 sec, it is necessary to add a silence insertion setting to 2 bytes of edit data.

For the echo regeneration of one arbitrary phrase of multiple phrases, a maximum of 6 phrases are possible if the silence insertion setting is 2 bytes.

9.5.2 Two-channel Regeneration

Two-channel regeneration uses PCM, melody and ADPCM methods. Channel synthesis is possible with all combinations except a melody reregeneration/melody reregeneration combination. Melody regeneration is fixed to channel 1. The sampling frequency of phrases to be overlapped must be the same.

Figures 9.7~9.10 show the vocalization timings of two-channel regeneration.

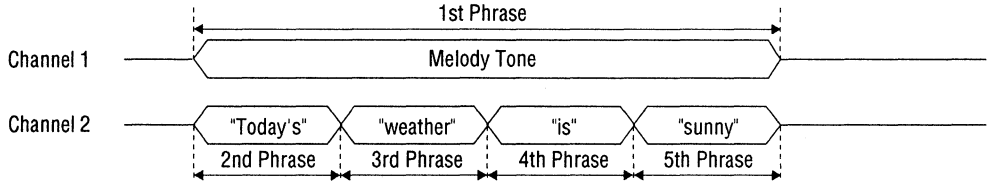


Figure 9.7 Example of Four Phrase Channel Synthesis Timing with Melody Tone as BGM

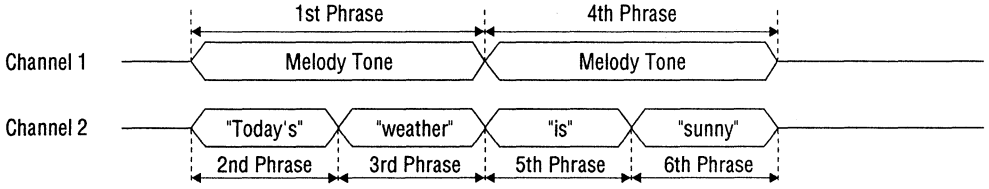


Figure 9.8 Example of Four Phrase Channel Synthesis Timing with Melody Tone and 1st and 4th Phrases as BGM

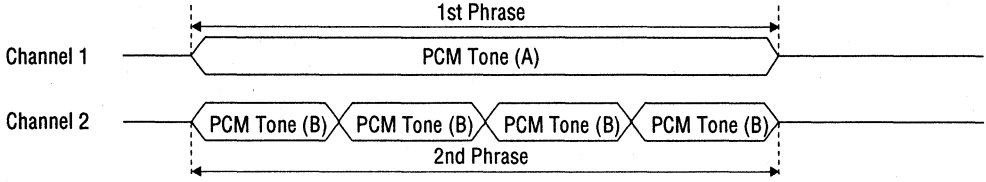


Figure 9.9 Example of Channel Synthesis between PCM Main Melody Tone (A) and PCM Rhythm Tone (B) with 4 Repeats

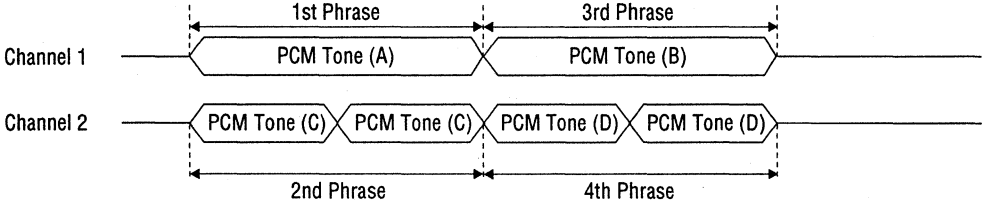


Figure 9.10 Example of Channel Synthesis between PCM Main Melody Tone (A) (B) and PCM Rhythm Tone (C) (D) with 2 Repeats

10. STANDBY CONVERSION

When $\overline{STBY}$ is set to "L" and standby conversion "YES" is selected, if the next phrase is not started up within 0.2 sec after speech ends, the LSI enters standby status and all operation stops. If restarted, it takes about 100 ms from start up to speech start because the "pop noise" countermeasure circuit is in operation.

If $\overline{STBY}$ is set to "H" and standby conversion "NO" is selected, the LSI does not enter standby status even if speech is over. Current is flowing since AOUT output remains at about 1/2 VDD and oscillation is in operation. If started up speech starts in about 350 µs to enter standby status when standby conversion "NO" is selected, the $\overline{RESET}$ pulse must be input.

If the $\overline{RESET}$ pulse is input, the AOUT output level instantaneously changes to GND level, causing pop noises.

11. SPEECH OUTPUT

In standalone mode speech is output via an internal low pass filter. Table 11.1 shows output level of AOOT pin. This filter consists of switched capacitors. Table 11.2 shows the relationship between sampling frequencies and cutoff frequencies.

Table 11.1 Output level of AOUTpin

Regeneration method	Most lowest level	Centre level	Most highest level
ADPCM	About 0.15 x VDD	About 0.5 x VDD	About 0.95 x VDD
PCM	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
Melody	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
BEEP Tone	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD

Table 11.2 Cutoff Frequencies of Low Pass Filter

Sampling Frequency (fsam)	Cutoff Frequency (fcut)
4.0kHz	About 1.8kHz
5.3kHz	About 2.6kHz
6.4kHz	About 2.6kHz
8.0kHz	About 3.2kHz
10.6kHz	About 4.2kHz
12.8kHz	About 5.1kHz
16.0kHz	About 6.4kHz
32.0kHz	About 12.8kHz

12. RC OSCILLATION

Figure 12.1 shows an-external circuit diagram using RC oscillation

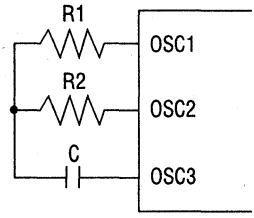


Figure 12.1 RC Oscillation

Figure 12.1 shows an-external circuit diagram using RC oscillation12.1 Determine of RC Constants
The RC oscillation frequency characteristics are shown in Figure 12.2.If fosc is set to 256 kHz,

R1=100kΩ, R2=30kΩ, C=30pF

when choosing RC oscillation, the RC oscillation frequencies are varied according to the Pluctuation of the external C and R2 as wsll as the process variations of the LSI.

13.2 Fluctuation of RC oscillation frequencies
When using a 30kΩR2 , the error due to process variations of the LSI is maximum ±4 % so flat the fluctuation of RC oscillarion frequency when using a capacitance (C) of ± 1% accuracy (R2) of ±2% accuracy is maximum±7% apporocimately.

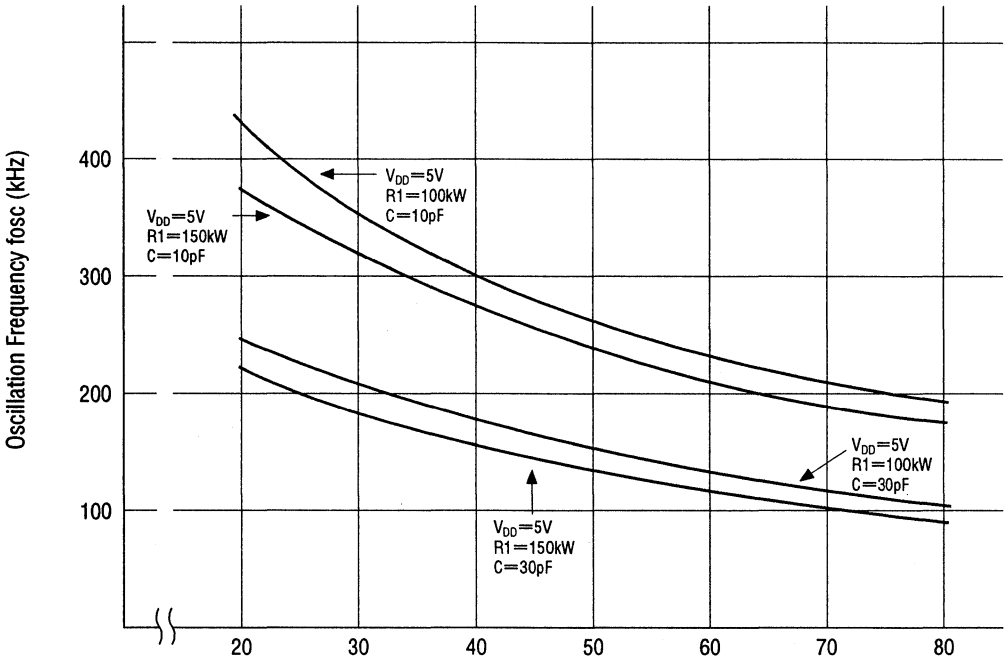


Figure 12.1 RC oscillation Frequency eharacteristics

13. CERAMIC OSCILLATION

Figure13.1 shows an external circuit diagram using a ceramic oscillator.

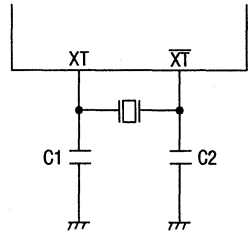


Figure 13.1 External circuit diagram

Figure 13.2 and 13.3 show external circuit diagrams using a cermic oscillator, CSA4.09MGU and CST4.09MGWU made by Murata Seisakusho Co., ltd.

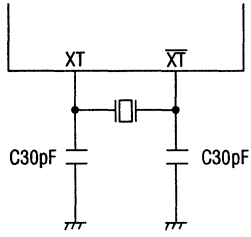


Figure 13.2 CSA4.09MGU

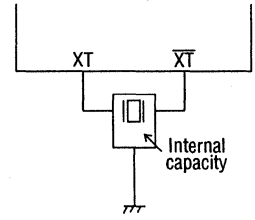


Figure 13.3 CST4.09MGWU

Figure 13.4 shows an external circuit diagram using a cermic oscillator, PBRC4.00MSA/MSK/MWS made by Kyocera Co., ltd.

Note) In case of using a oscillator 4.00MHz, vocalization speed is low about 2% than AR76-202 analysis tool and evaluation board.

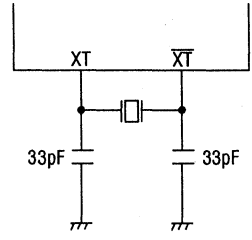
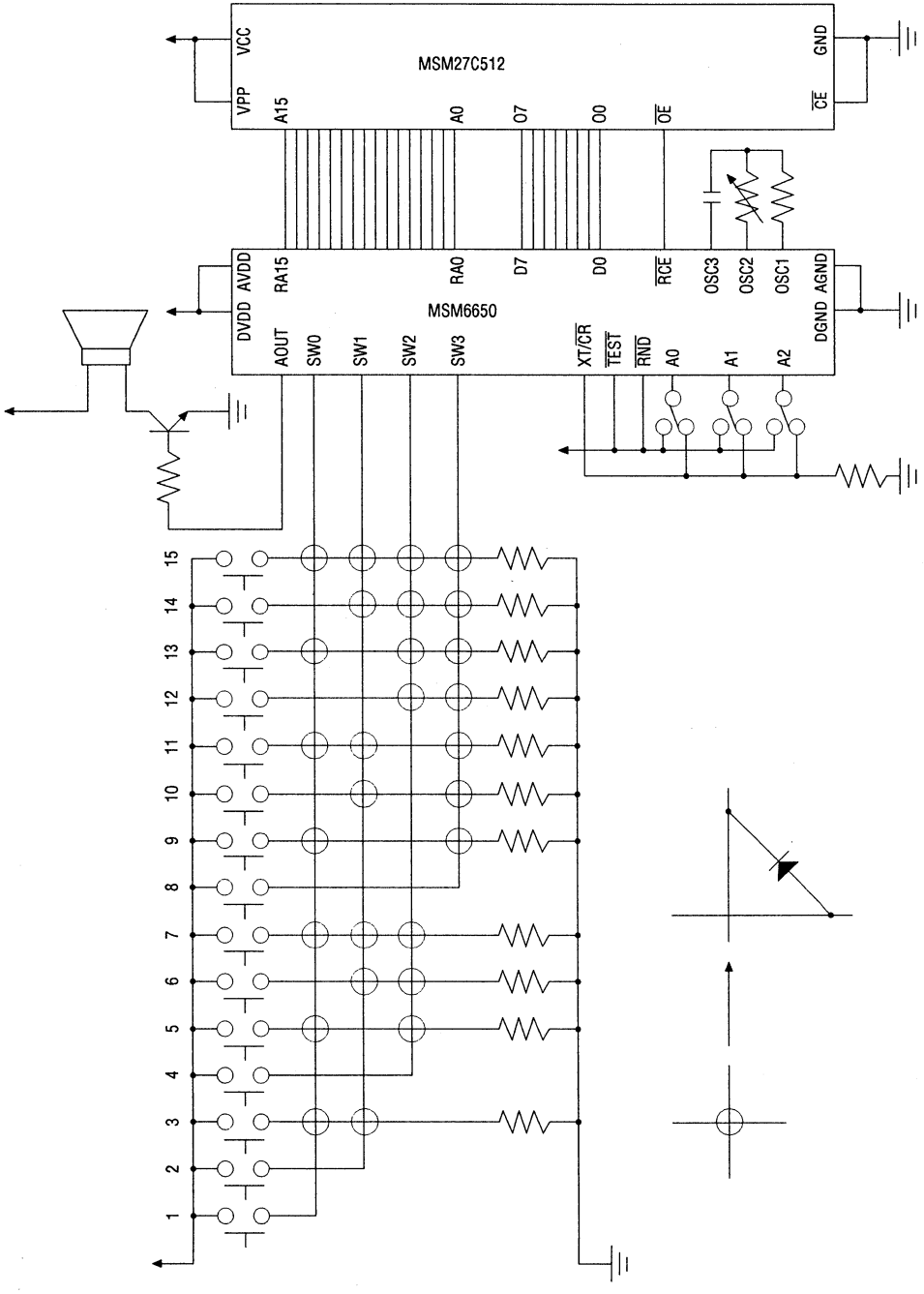
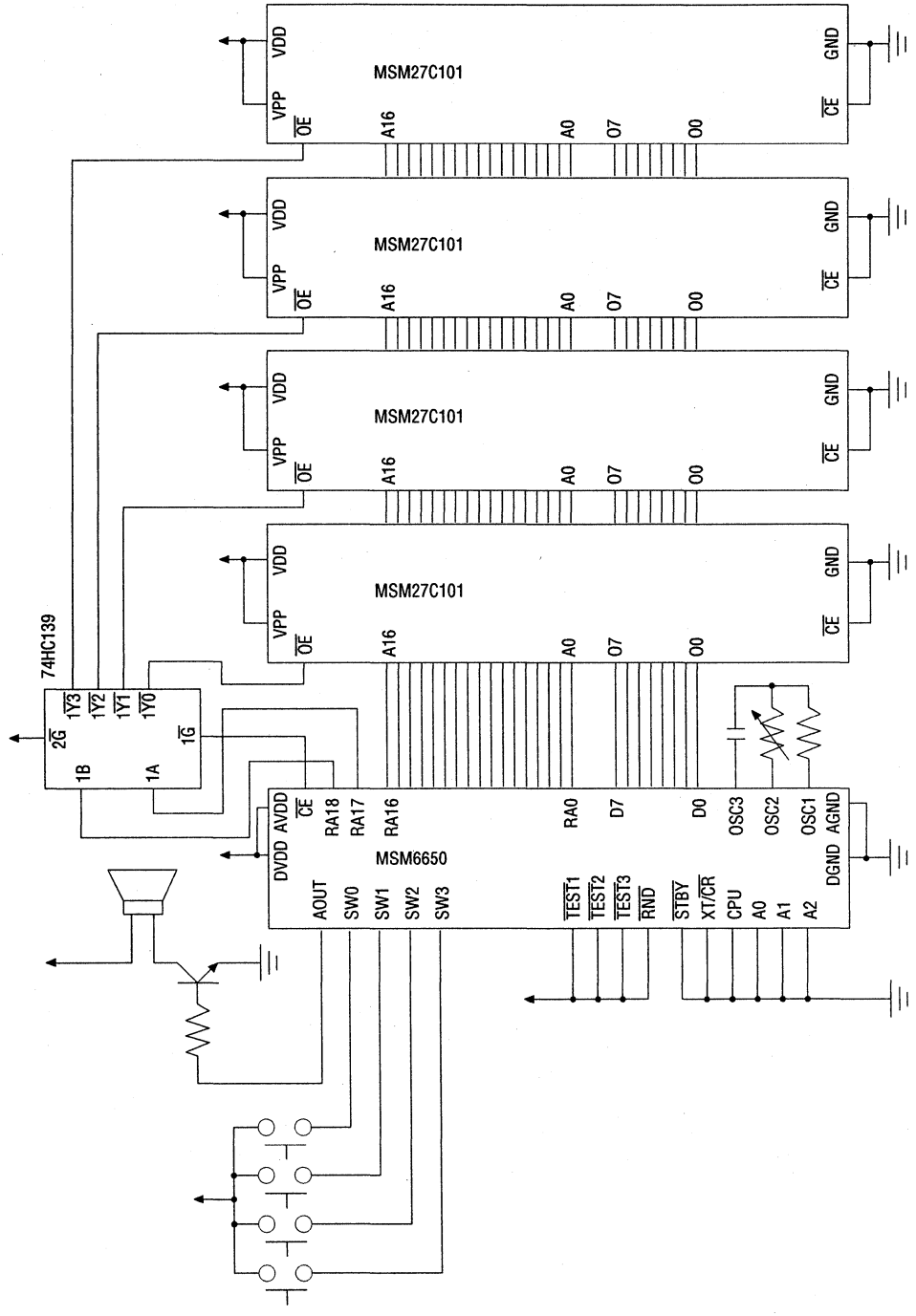


Figure 13.4 PRBC 4.00 MSA/MSK/MWS

APPLICATION CIRCUIT EXAMPLE



Application Circuit Example to Speech-output 15 Phrases by Switching



Application Circuit Example when Using Four 1 Mbit EPROMs

(2) MICROCOMPUTER INTERFACE MODE

FEATURES

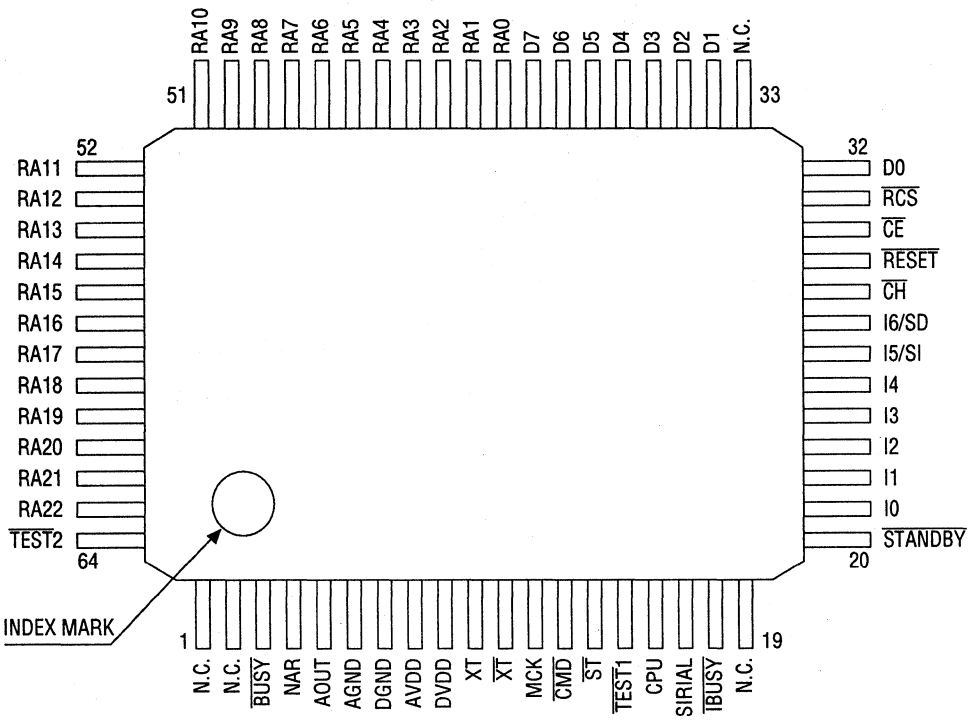
4-bit ADPCM method/8-bit PCM method
Melody function
Edit ROM function
2-channel mixing function
Fadeout function (sound volume 4-step change)
Serial input/parallel input can be selected

Internal BEEP tone	0.5 kHz, 1.0 kHz, 1.6 kHz, 2.0 kHz BEEP tone can be vocalized by specified code
Sampling frequencies	4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz
Maximum number of phrases	: 127
Internal 12-bit D/A converter	
Internal LPF attenuation factor	: -40 dB/oct
Internal standby function	
Package	: 64-pin FLAT (QFP64-P-1420-V1K)

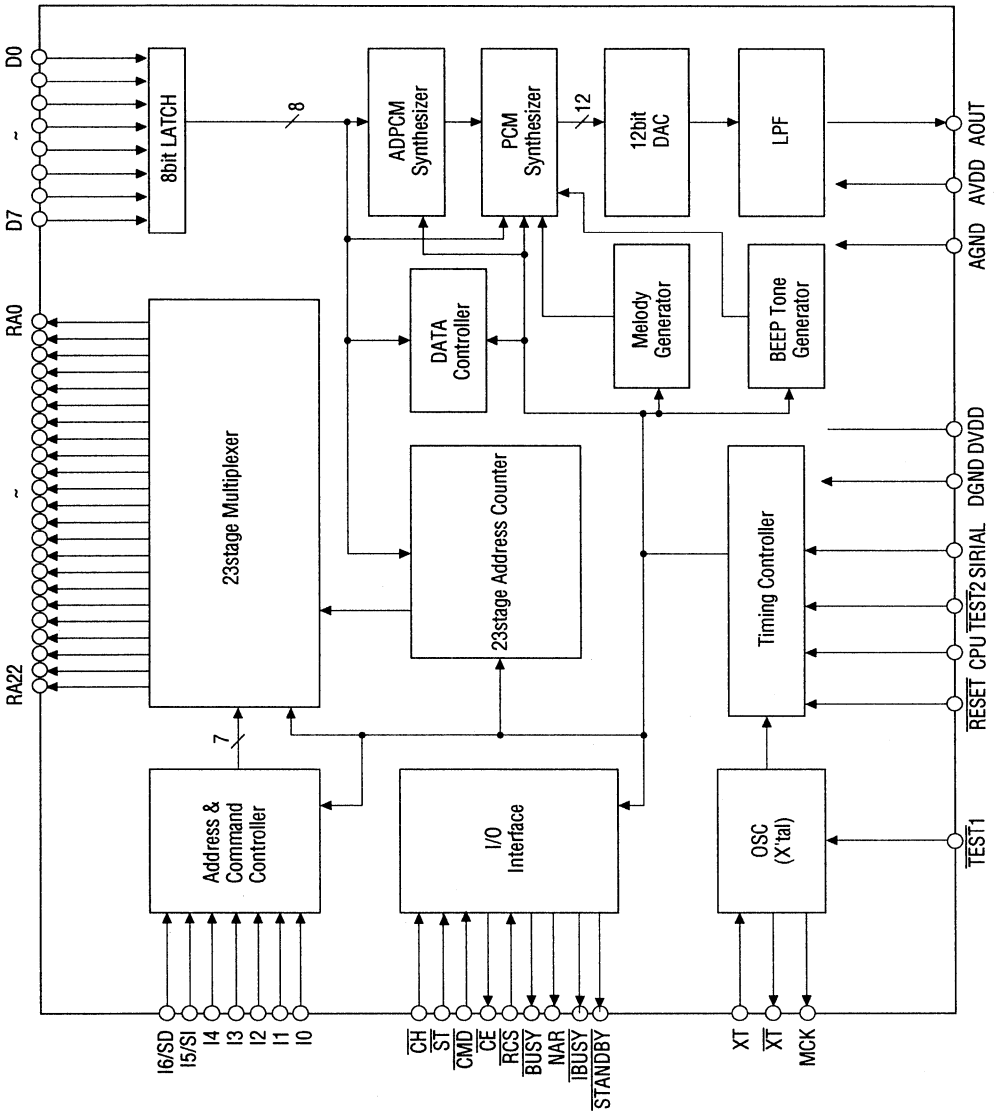
PIN CONFIGURATION

(Top View)

64 Lead Plastic QFP



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Rating

(GND = 0V)

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ 7.0	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	–	-55 ~ 150	°C

Operation Range

(GND = 0V)

Parameter	Symbol	Condition	Limits			Unit
Power Supply Voltage	V_{DD}	DAC output	+2.4 ~ +5.5			V
		LPF output	+2.7 ~ +5.5			V
Operating Temperature	T_{OP}	–	-40 ~ 85			°C
			Min.	Typ.	Max.	
Original Oscillation Frequency	f_{OSC}	–	3.5	4.096	4.5	MHz

DC Characteristics

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	V_{IH}	–	4.2	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	4.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	V_{IH} = V_{DD}	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-200	-90	-30	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2 (Note)	I_{IL2}	Internal pullup resistance pin	30	90	200	µA
Operating Current Consumption	I_{DD}	–	–	6	10	mA
Standby Current Consumption	I_{DS}	–	–	–	10	µA
DA Output Relative Accuracy	$\|V_{DAE}\|$	When DA output selected	–	–	40	mV
DA Output Impedance	R_{DAO}	When DA output selected	15	25	35	kΩ
LPF Drive Resistance	R_{AOUT}	When LPF output selected	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	I_F=100µA	–	1	3	kΩ

DC CHARACTERISTICS

(V_{DD} = 3.1V, GND = 0V, Ta = -40 ~ 85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input Voltage	V_{IH}	–	2.7	–	–	V
"L" Input Voltage	V_{IL}	–	–	–	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = -1mA	2.6	–	–	V
"L" Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	–	–	10	µA
"H" Input Current 2	I_{IH2}	Internal pulldown resistance pin	-100	-30	-10	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	-10	–	–	µA
"L" Input Current 2 (Note)	I_{IL2}	Internal pullup resistance pin	10	30	100	µA
Operating Current Consumption	I_{DD}	–	–	4	7	mA
Standby Current Consumption	I_{DS}	–	–	–	1	µA
DA Output Relative Accuracy	$\|V_{DAE}\|$	When DA output selected	–	–	20	mV
DA Output Impedance	R_{DAO}	When DA output selected	15	25	35	kΩ
LPF Drive Resistance	R_{AOUT}	When LPF output selected	50	–	–	kΩ
LPF Output Impedance	R_{LPF}	I_F=100µA	–	1	3	kΩ

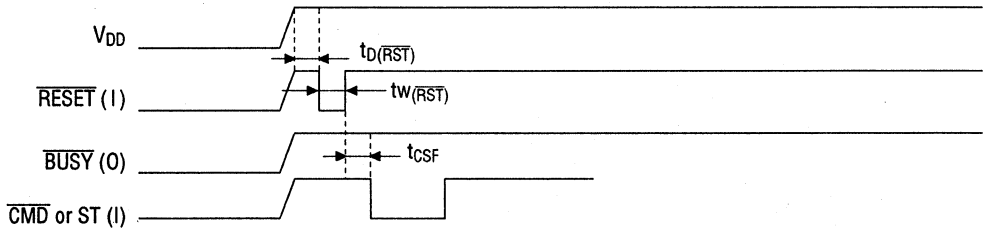
AC CHARACTERISTICS

(V_{DD} = 5.0V, GND = 0V, Ta = -40 ~ 85°C)

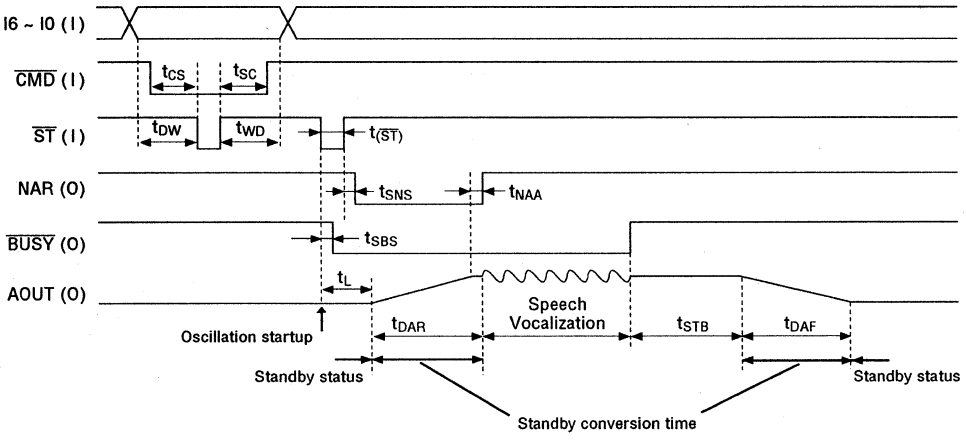
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Original Oscillation Duty Cycle	f_{duty}	–	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{(\overline{RST})}$	–	10	–	–	µS
$\overline{\text{ST}}$ Input Pulse Width	$tw_{(\overline{ST})}$	–	0.35	–	2000	µS
Data Set Time	t_{DW}	–	1	–	–	µS
Data Hold Time	t_{WD}	–	1	–	–	µS
$\overline{\text{CMD}}$ Setup Time	t_{CS}	–	1	–	–	µS
$\overline{\text{CMD}}$ Hold Time	t_{SC}	–	1	–	–	µS
$\overline{\text{CH}}$ Setup Time	t_{CHS}	–	1	–	–	µS
$\overline{\text{CH}}$ Hold Time	t_{SCH}	–	1	–	–	µS
Serial Clock Pulse Width	$tw_{(SCK)}$	When using serial input option	0.35	–	–	µS
Serial Data Setup Time	t_{SDS}	When using serial input option	1	–	–	µS
Serial Data Hold Time	t_{SSD}	When using serial input option	1	–	–	µS
$\overline{\text{BYSY}}$ Output Time (1)	t_{SBS}	–	–	–	10	µS
$\overline{\text{BUSY}}$ Output Time (2)	t_{BN}	When fs = 8kHz	350	375	400	µS
$\overline{\text{BUSY}}$ Output Time (3)	t_{BF}	–	–	–	64	mS
NAR Output Time (1)	t_{SNS}	–	–	–	10	µS
NAR Output Time (2)	t_{NAA}	When fs = 8kHz	350	375	400	µS
NAR Output Time (3)	t_{NAB}	When fs = 8kHz	350	375	400	µS
NAR Output Time (4)	t_{NAC}	When fs = 8kHz	350	375	500	µS
DA Converter Change Time	t_{DAR}	–	60	64	68	mS
LPF Stable Time	t_L	–	6	8	10	mS
Standby Conversion Time (after speech ends)	t_{STB}	–	0.15	0.20	0.25	S

TIMING CHART

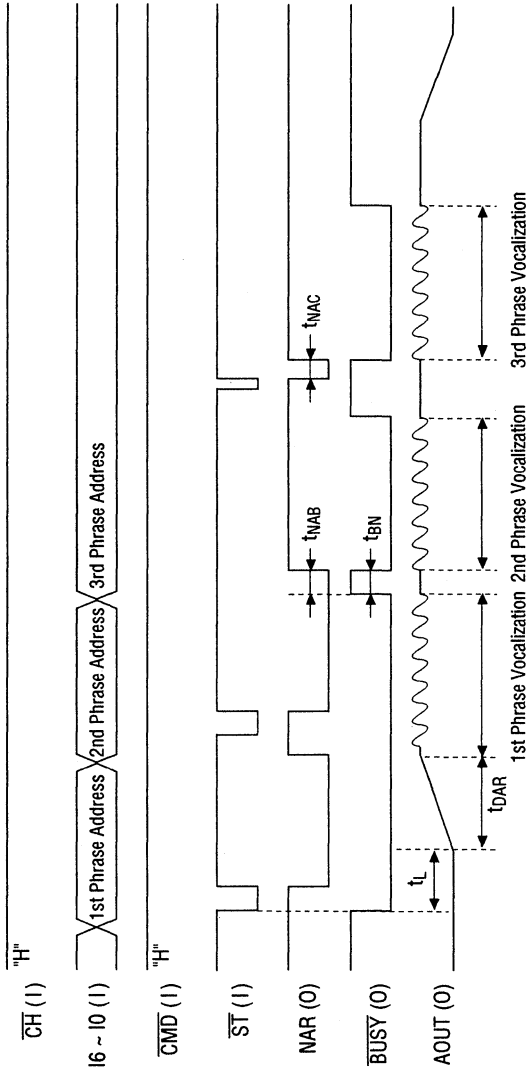
1. When Power Is Turned ON



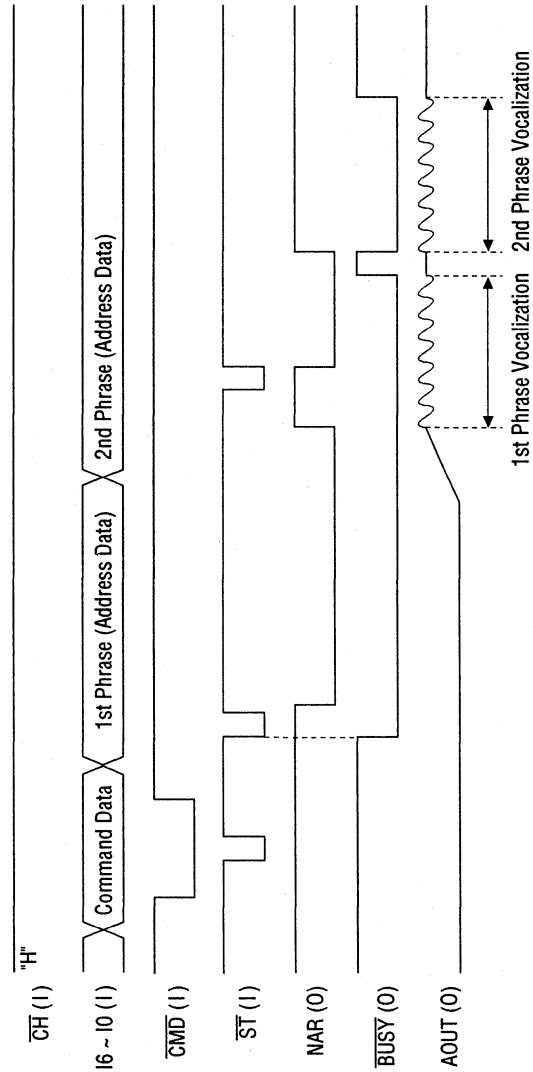
2. When LSI Starts Up and Is in Standby Status



3. Channel 1 Regeneration Timing Chart when External Command Is Not Used (Parallel Input)

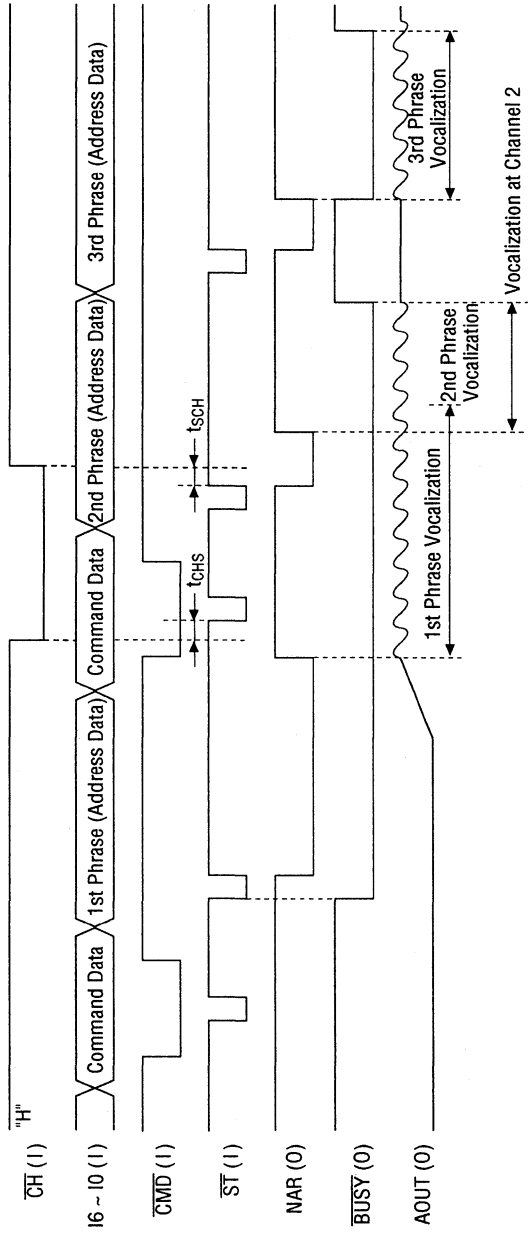


4. Channel 1 Regeneration Timing Chart when External Command Is Used (Parallel Input)



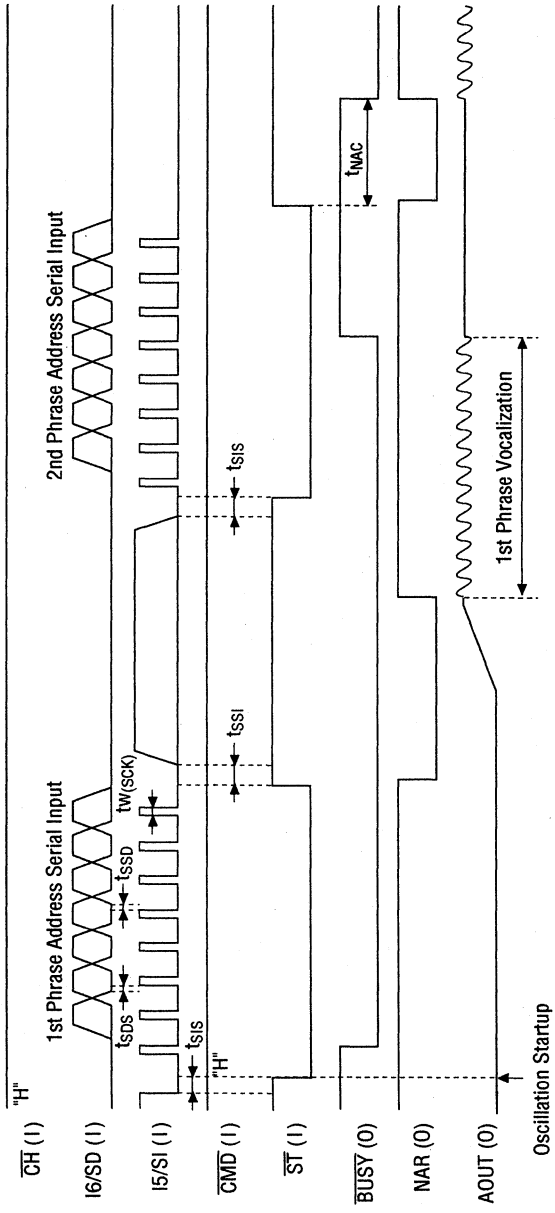
If a command is set externally the status set is maintained until the next command is set. Therefore, if the 1st and 2nd phrases are vocalized at the timing shown above, speech for both phrases is first vocalized in the status set by that command. To vocalize command content that was changed, be certain to input command data before inputting address data. The command input can be continuously set until the address input even in many times. However, the setting of the command inputted last is valid (common with 1 channel and 2 channel).

5. Channel 1, Channel 2 Regeneration Timing Chart when External Command Is Used (Parallel Input)



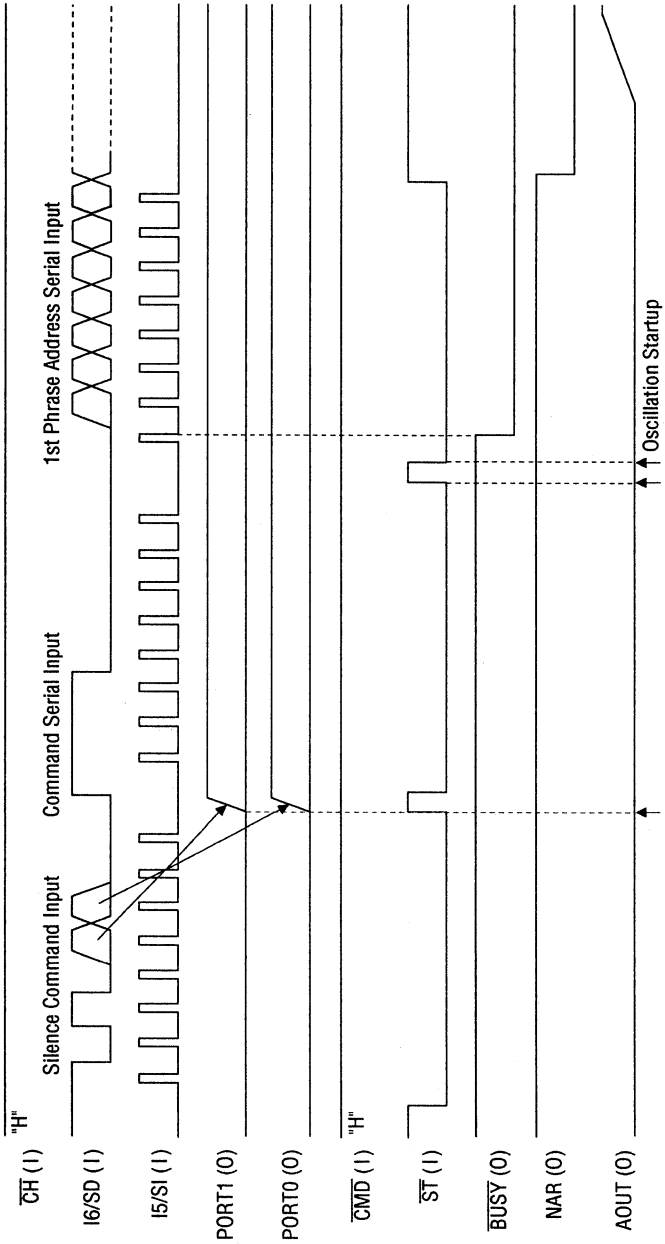
Since command data is maintained independently, if speech is started up at channel 1 without a command setting, speech is vocalized by the same command set at the 1st phrase.

6. Regeneration Timing Chart when External Command Is Not Used (Serial Input)



In serial input, data is transferred to the LSI when the $\overline{ST}$ signal rises after serial data is input.
SD is captured at the end before SI.

7. Regeneration Timing Chart when External Command Is Used (Serial Input)



In serial input, port output can be set by a command setting. Since a port output command and internal command are shared, if a command is set for port output, set the command for speech again to input address data. If address data is input without setting the command, the LSI recognizes it as silence insertion code.

PIN DETAILS

Pin Name	I/O	Function
$\overline{BUSY}$	O	Outputs "L" during vocalization. At "H" level when power is turned ON.
NAR	O	$\overline{CMD}$, $\overline{ST}$ input becomes effective when NAR is at " H" level. If CH pin is in "H" level, NAR becomes a channel 1 status signal. If in "L" level NAR becomes a channel 2 status signal. NAR signal indicates whether registers I6 to I0 address of address/command controller (see block diagram) is in open status. "H" level indicates open status. NAR is in "H" level when power is turned ON.
AOUT	O	Analog speech output pin. DA converter output or LPF output can be selected by a command input.
AGND	–	Analog ground pin.
DGND	–	Digital ground pin
AVDD	–	Analog power pin
DVDD	–	Digital power pin
XT	I	Ceramic oscillator connection pin. Pin has internal 500 kΩ to 4 MΩ feedback resistance between XT and $\overline{XT}$. Input from this pin when using external clock.
$\overline{XT}$	O	Ceramic oscillator connection pin. Outputs "L" in standby status. Set to open to use external clock.
MCK	O	Main clock output pin. Use MCK as a connection pin for MSC 1192, etc. Pin is in "H" level in standby status.
$\overline{CMD}$	I	Command input and option setting control pin. Command and option input is enabled if $\overline{ST}$ pin is set to "L" level when $\overline{CMD}$ pin is in "L" level. Set to "H" level when $\overline{CMD}$ is not used and when using serial input interface. This pin has internal pullup resistance.
$\overline{ST}$	I	Speech synthesis starts at fall of $\overline{ST}$, I6 to I0 addresses are captured at rise of $\overline{ST}$. Input $\overline{ST}$ when NAR of channels 1 and 2 status signals are "H". This pin has internal pullup resistance.
CPU	I	Set to "H" level if MSM6650 is used in a microcomputer interface.
SERIAL	I	Selects either parallel or serial input interface. Serial input interface is selected in "H" level, parallel input interface in "L" level.
I1 ~ I0	I	Command and user specified phrase input pins when using parallel input interface. Since the pins are not used with a serial input interface, set to "L" level. These pins have internal pulldown resistance.
I2/PORT0	I/O	Command and user specified phrase input pins when using parallel input interface. Port out put pin when using serial input interface. Output of port changes by command input from microcomputer when using serial input interface.
I3/PORT0	I/O	Command and user specified phrase input pins when using parallel input interface. Port output pin when using serial input interface. Output of port changes by command input from microcomputer when using serial input interface.
I4	I	Command and user specified phrase input pins when using parallel input interface. Since it is not used with a serial input interface, set to "L" level. This pin have internal pulldown resistance.
I5 / SI	I	Command and user specified phrase input pins when using parallel input interface. A serial clock input pin when using serial input interface.

Pin Name	I/O	Function
I6/SD	I	Command and user specified phrase input pin when using parallel input interface. A serial data (command and address) input pin when using serial input interface.
$\overline{CH}$	I	Channel control signal. Channel 1 input is in "H" level, channel 2 input is in "L" level. This pin has internal pullup resistance.
$\overline{RESET}$	I	LSI enters standby status if "L" is input. Oscillation then stops, AOUT output changes to GND, and status returns to initial status. MSM6650 has internal power ON reset. Startup power within 1 mS to operate power ON reset correctly. If not, apply $\overline{RESET}$ pulse when power is turned ON. This pin has internal pullup resistance.
$\overline{CE}$	O	Timing output pin to control read for external memory. Outputs when $\overline{RCS}$ is in "L".
$\overline{RCS}$	I	Address RA22 to RA0 and $\overline{CE}$ are output when in "L". If in "H" level address pins of RA22 to RA0 and $\overline{CE}$ become high impedance status. D7 to D0 do not receive external signal, and are internally pulled down.
D7 to D0	I	Pins to input data of external memory. Data is input when $\overline{RCS}$ is in "L" level. If $\overline{RCS}$ is in "H", external data is not received and pins become "L" level.
RA22 to RA0	O	Address pins of external memory. Outputs when $\overline{RCS}$ is in "L" level. If $\overline{RCS}$ is in "H" level status becomes high impedance.
$\overline{TEST}$ 1, 2	I	Test pins. Set to "H" level.
$\overline{IBUSY}$	O	Output "L" level excepting standby conversion time. during voice regeneration or 1/2 VDD level of AOUT pin .
$\overline{STANDBY}$	O	Output "L" level , when the LSI is oscillating .

FUNCTION DETAILS

Parallel input or serial input can be selected for the microcomputer interface. Select with the SERIAL terminal. "H" level selects serial input, "L" level selects parallel input.

1. VOCALIZATION CODE SPECIFICATION

The user can specify a maximum of 127 phrases. Table 1.1 shows the settings by I6 to I0.

Table 1.1 User Specified Phrases

I6 ~ I0	Code Details
0000000	Stop Code
0000001 ⌇ 1111111	User Specified Phrase (127 Phrases)

2. PULLUP / PULLDOWN RESISTANCE

$\overline{\text{RESET}}$, $\overline{\text{CMD}}$, $\overline{\text{ST}}$ and $\overline{\text{CH}}$ pins have internal pullup resistance. I4, I1 and I0 pins have pulldown resistance in serial input.

3. MODE SETTING

Three items can be set by command option. Table 3.1 shows the options that can be selected.

Table 3.1 Command Option Item List

No.	Item	Selection		Remarks
1	Standby Conversion	Yes	No	If standby conversion YES is selcted, status enters standby unless the next user specified phrase is input within 0.2 sec after speech ends.
2	AOUT Output	LPF Output	DAC Output	
3	Maximum amplitude of 1 phrase	0 ~ VDD	1/4 VDD ~ 3/4 VDD (1/2 amplitude)	Maximum amplitude at 1 phrase

An option is set as in Table 3.2 when power is turned ON.

Table 3.2 Option when Power Is Turned ON

Standby Conversion	AOUT Output	Amplitude for 1 Phrase
YES	LPF Output	0 ~ V_{DD}

To change an option that is already set use command again. If the $\overline{\text{RESET}}$ terminal is set to "L" level, the option returns to the status when power was turned ON (Table 3.2).

After setting the option, be certain to input the speech, silence and BEEP tone commands, then startup.

Figures 3.1 and 3.2 show the option setting timing, and Tables 3.3 and 3.4 show the option correspondences.

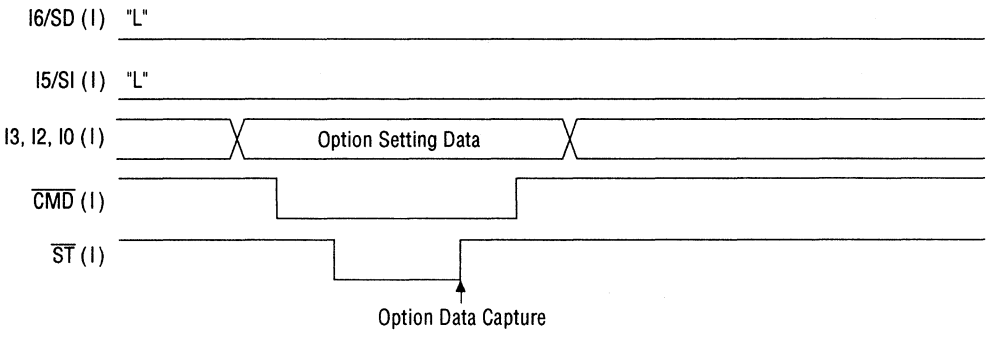


Figure 3.1 Option Setting Timing (during Parallel Input)

Table 3.3 Correspondence between Options and I3, I2, I0

	I3	I2	I0
	AOUT Output	Standby Conversion	Amplitude of 1 Phrase
"0" Data	LPF	YES	0 ~ V_{DD}
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4V_{DD}

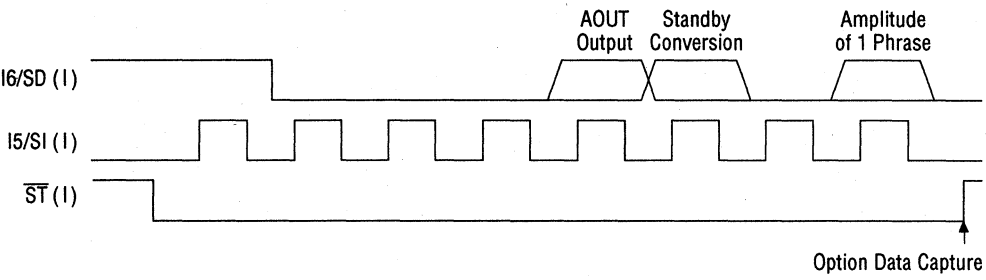


Figure 3.2 Command Option Setting Timing (during Serial Input)

Table 3.4 Command Correspondence between Option and Serial Data

	AOUT Output	Standby Conversion	Amplitude of 1 Phrase
"0" Data	LPF	YES	0 ~ V_{DD}
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4V_{DD}

4. MICROCOMPUTER INTERFACE MODE

External command settings are enabled with the microcomputer interface. However, if edit ROM is used, the command settings of channel 1 are disabled.

Figures 4.1 and 4.2 show the command input and address input method when using the microcomputer interface.

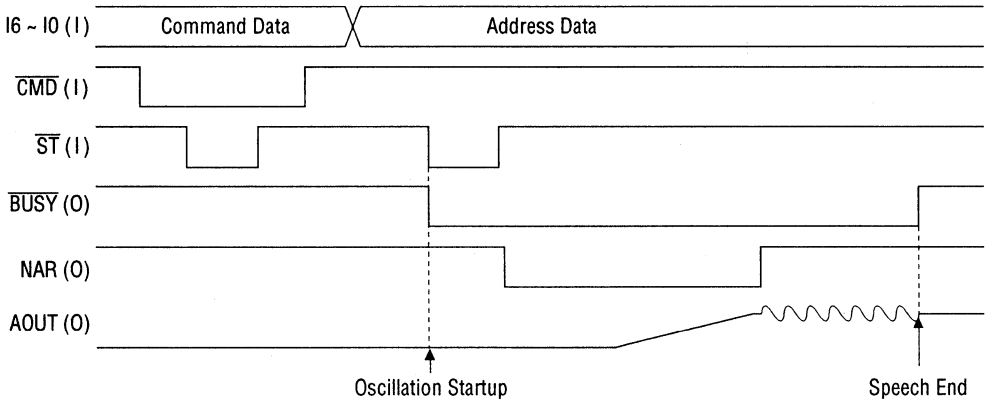


Figure 4.1 Command, Address Input Timing (Parallel Input)

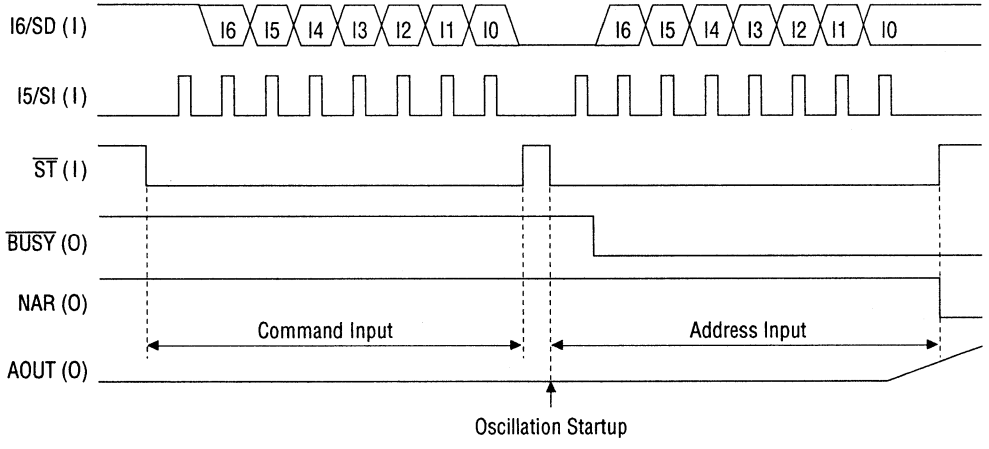


Figure 4.2 Command, Address Input Timing (Serial Input)

In microcomputer interface serial input, command data and address data are distinguished by the initial data input serially. If the initial data is "H", it is judged as command data, if "L", it is judged as address data.

Input command data and address data after inputting the command and address judgment data as initial data. Figures 4.3, 4.4, and 4.5 show the external input flow.

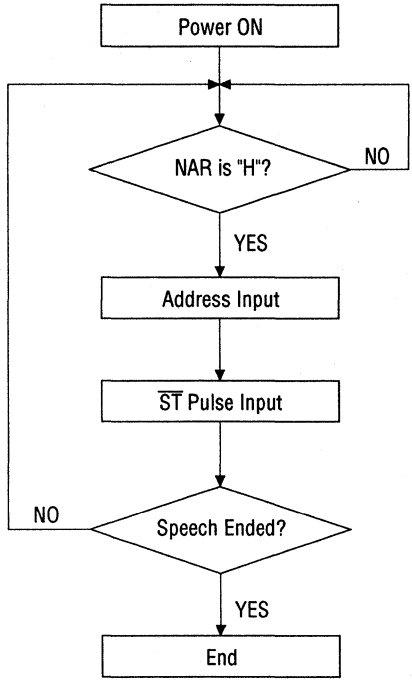


Figure 4.3 Input Flow Chart when Command Is Not Set

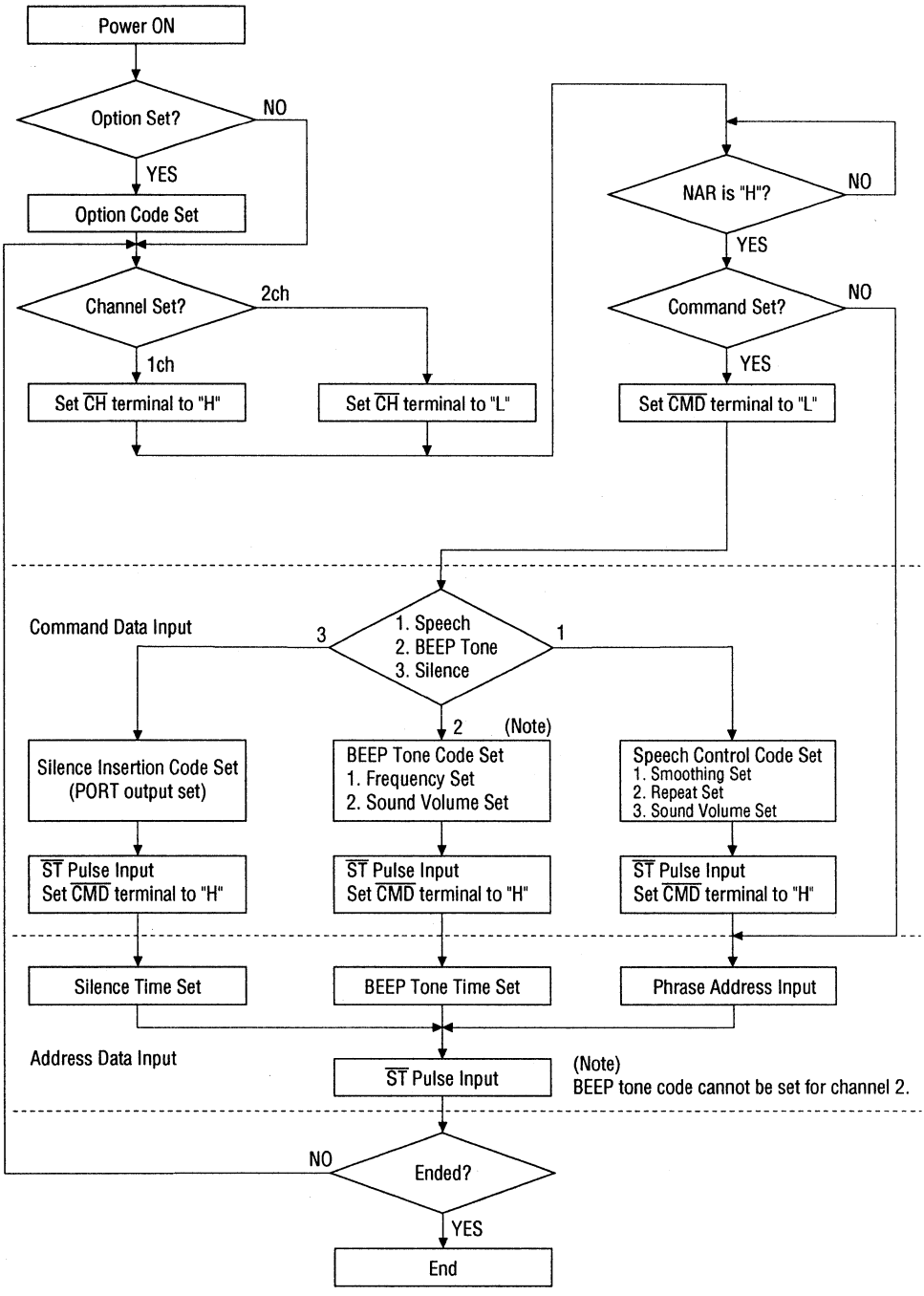


Figure 4.4 Parallel Input Flow Chart when External Command Is Used.

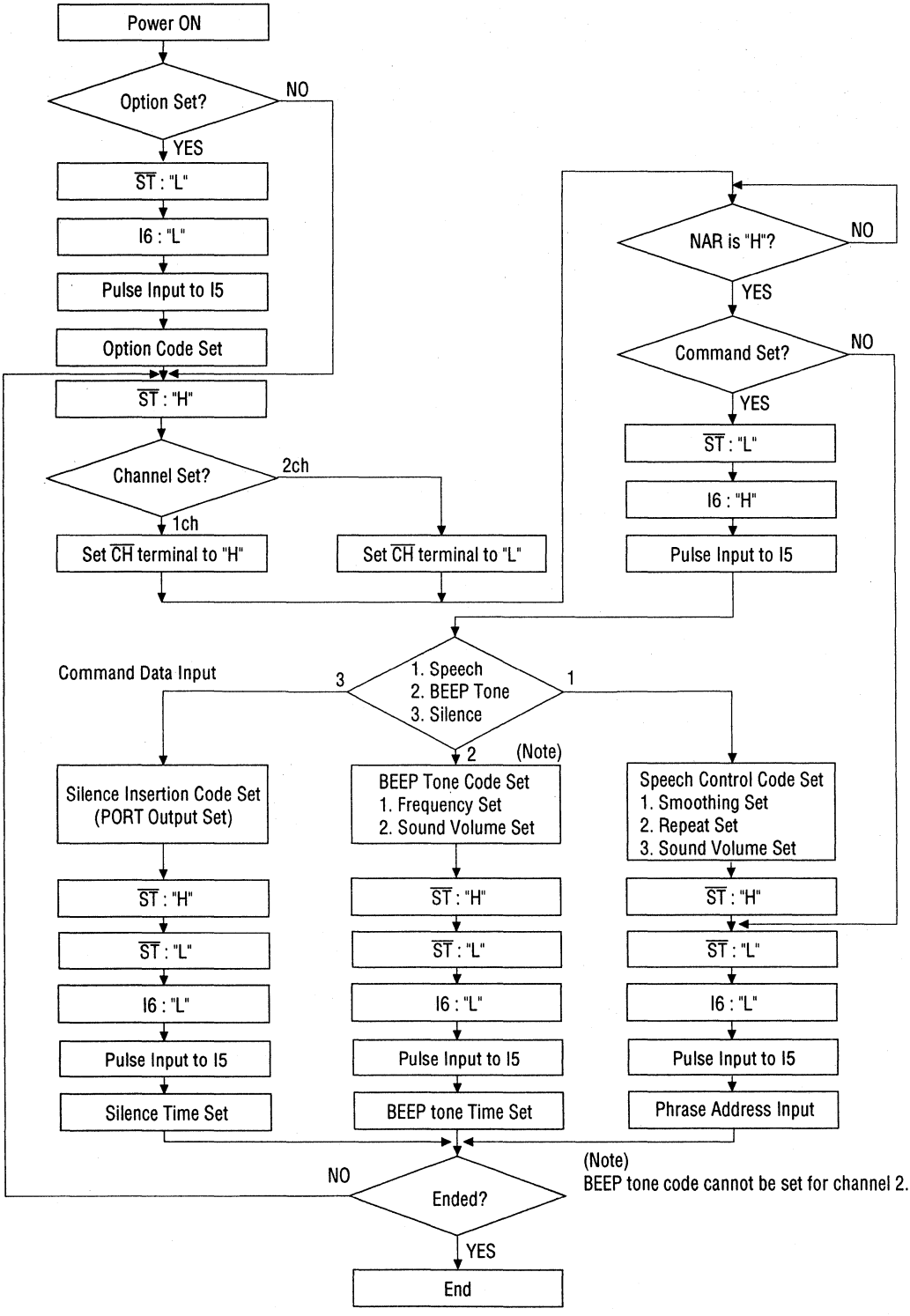


Figure 4.5 Serial Input Flow Chart when External Command is used

5. COMMAND DATA

Table 5.1 shows the conditions that can be set by command data. Command data is set with I6 to I0. In serial input, input data corresponding to I6 to I0 serially as shown in Figure 4.2.

Table 5.1 Command Setting Content List

I6	I5	I4	I3	I2	I1	I0	Command Content
0	0	0	oa	os	0	ov	Option Setting
0	1	0	p1	p0	0	0	Silence Insertion Code
1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

Command data is set to "1100000" when power is turned ON.

5.1 Option Setting Code

An option can be set by command. Since an option is set as in Table 3.2 when power is turned ON, use this command to change an option. Once an option is set, it remains effective either until power is shut OFF or until the $\overline{\text{RESET}}$ signal is input.

When an option is set, input speech, silence and BEEP tone commands again by both command input and the set address (phrase, silence time and BEEP tone time).

Table 5.2 shows the options that can be set.

Table 5.2 Option Correspondence Table

	I3	I2	I0
	AOUT output	**Standby Conversion**	**Amplitude of 1 Phrase**
"0" Data	LPF	YES	0 ~ VDD
"1" Data	DAC	NO	1/4 V_{DD} ~ 3/4 V_{DD}

Options can be set anytime, but if set during vocalization, AOUT output impedance and acoustic pressure may change.

5.2 Silence Insertion Code

Silence code inserts silence to each channel. Speech data can be reduced by inserting silence externally.

I6	I5	I4	I3	I2	I1	I0	
0	1	X	p1	p0	X	X	X: Don't care

Command data specifies to insert silence, address data sets the silence time. The $\overline{CH}$ pin inserts silence to either channel 1 or 2.

Silence time is set by address data (I6 to I0).

Minimum Silence Time: ... 16.384 ms
Maximum Silence Time: ... (128 - 1) × 16.384 ms=2.1 sec

Figure 5.3 shows the channel 1 silence insertion setting timing.

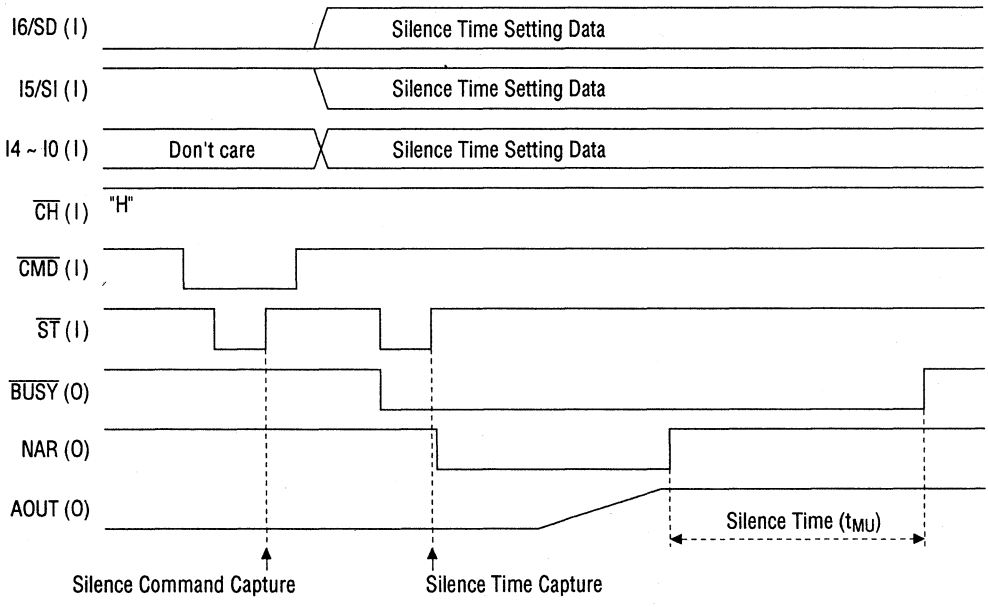


Figure 5.3 Channel 1 Silence Setting Timing (Parallel Input)

For example, if silence time setting data shown in Figure 5.3 is set as (I6 to I0) = ("0011000"), the silence time (t_{MU}) becomes

$$(2^6 \times 0+2^5 \times 0+2^4 \times 1+2^3 \times 1+2^2 \times 0+2^1 \times 0+2^0 \times 0) \times 16.384\text{mS} = 393.216 \text{ ms}$$

The formula to set silence time is shown below.

$$t_{MU} = (2^6 \times (I6)+2^5 \times (I5)+2^4 \times (I4)+2^3 \times (I3)+2^2 \times (I2)+2^1 \times (I1)+2^0 \times (I0)) \times 16.384 \text{ ms}$$

The channel 2 silence insertion setting timing becomes as shown in Figure 5.4.

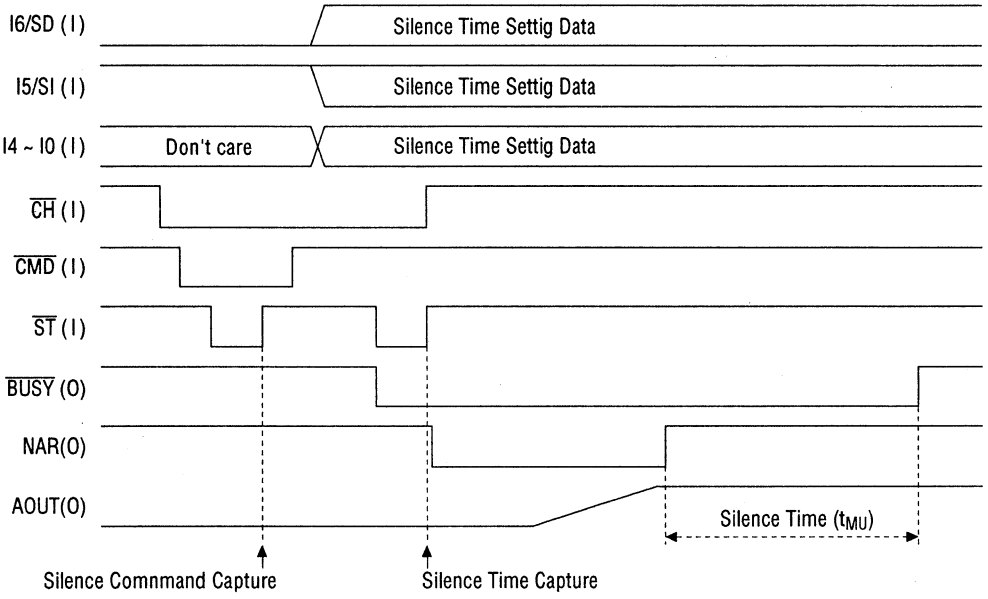


Figure 5.4 Channel 2 Silence Setting Timing (Parallel Input)

In serial input, the port output signals from PORT1 and PORT0 pins is also controlled by silence insertion code. PORT1 and PORT0 pins are in "L" level when power is turned ON, and when the $\overline{\text{RESET}}$ signal is input.

If speech synthesis starts after setting the port output, first set the port output by silence insertion code, then input the speech vocalization code and set the address. Figure 5.5 shows the timing. If it is necessary to set the port again after setting the port, since a port cannot be set continuously, input the BEEP tone code or speech vocalization code after first setting the port, then set the port again.

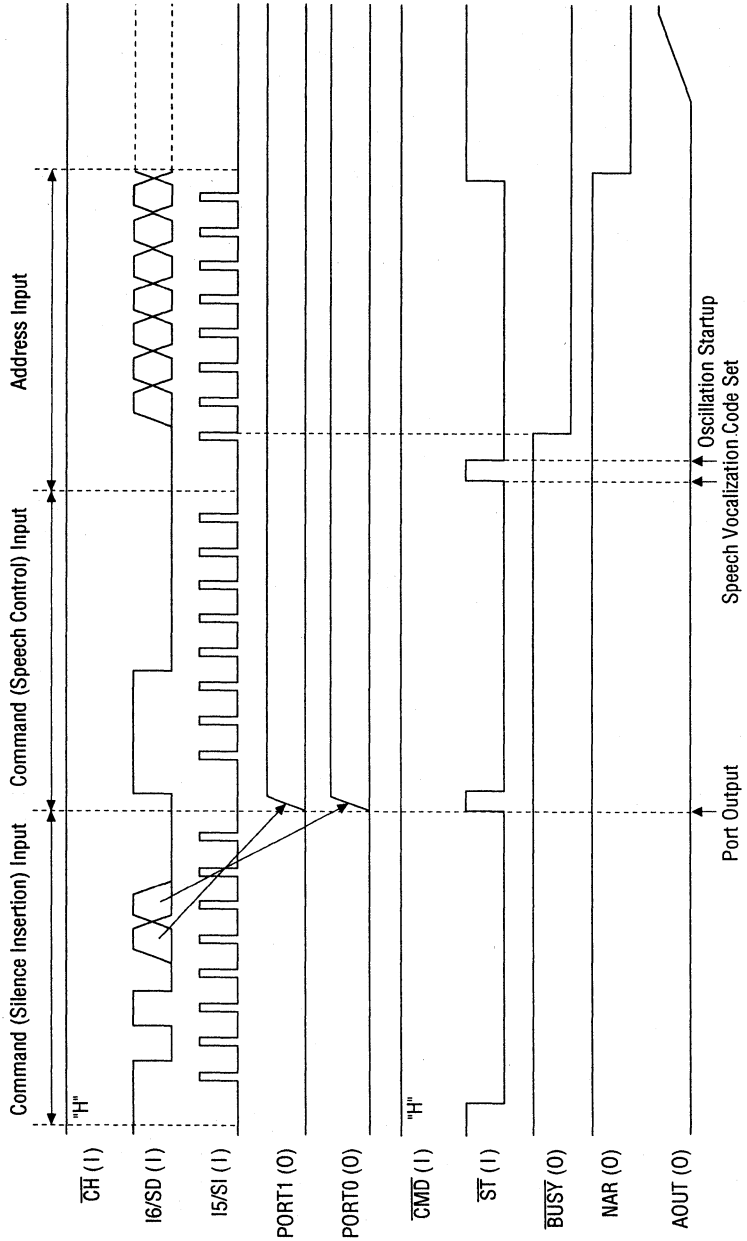


Figure 5.5 Port Output and Command, Address Setting Timing (during Serial Input)

5.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data. The BEEP tone can be set only at channel 1. Do not select the BEEP tone at channel 2.

To mix a BEEP tone and channel 2, vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz. If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

I6	I5	I4	I3	I2	I1	I0
1	0	0	bl1	bl0	bf1	bf0

The sound volume is set to I3 and I2 pins, and the frequency is set to I1 and I0 pins. Tables 5.3 and 5.4 show the sound volumes and the frequencies that can be set.

Table 5.3 Sound Volume Settings

I3	I2	Sound Volume (Note 1)
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 5.4 Frequency Settings

I1	I0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

(NOTE1)

If 1/2 amplitude of channel 1 is set, and if the maximum amplitude is set to 1/2 V_{DD} as an option the sound volume of BEEP tone becomes 1/4 V_{DD}.

The BEEP tone time is set by address data (I6 to I0).

Minimum BEEP Tone Time ..... 16.384 ms
Maximum BEEP Tone Time ..... (128 - 1) × 16.384 ms = 2.1 sec

Figure 5.6 shows BEEP tone setting timing.

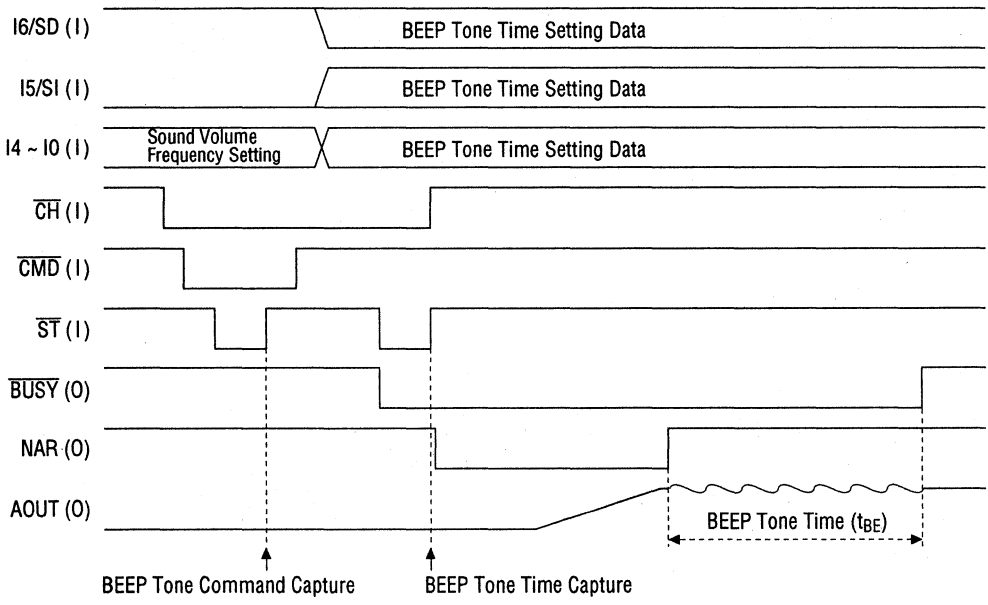


Figure 5.6 BEEP Tone Setting Timing (during Parallel Input)

For example, if the BEEP time setting data shown in Figure 5.6 is set as (I6 to I0) = ("0011000"), the BEEP tone time (t_{BE}) becomes

$$(2^6 \times 0+2^5 \times 0+2^4 \times 1+2^3 \times 1+2^2 \times 0+2^1 \times 0+2^0 \times 0) \times 16.384\text{mS} = 393.216 \text{ ms}$$

The formula to set BEEP tone time is shown below.

$$t_{BE} = (2^6 \times (I6)+2^5 \times (I5)+2^4 \times (I4)+2^3 \times (I3)+2^2 \times (I2)+2^1 \times (I1)+2^0 \times (I0)) \times 16.384 \text{ ms}$$

5.4 Speech Control Code

Command data can set repeat and sound volume.

I6	I5	I4	I3	I2	I1	I0
1	1	sm	rp1	rp0	vl1	vl0

Channel 1 is set if $\overline{CH}$ pin is in "H", channel 2 is set if in "L". Once a command is set, it is maintained as both channels until another command is set. The LSI cannot be maintained commands contens as each channels. Conditions of each channel are set by I4 to I0. Three conditions can be set: 1) to 3).

1) Setting Number of Repeats

The number of repeats is set by I3 and I2 pins. For the number of repeats 4 types can be selected: 1, 2, 4 and infinite. Input stop code to stop speech when infinite repeat is selected. Table 5.5 shows the correspondence between I3 and I2 pins, and the number of repeats.

Table 5.5 Selection of Number of Repeats

I3	I2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "I4" is set to "H", sound volume during repeat is automatically attenuated from 1 to 1/2, 1/4 and 1/8 (fadeout function). This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at I1 and I0 pins.

Table 5.6 shows the correspondence between I1, I0 pins and sound volume settings.

Table 5.6 Attenuation Volume Setting

I1	I0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound vlume is 1/8 of speech data)

6. ADDRESS DATA

If a user specified phrase is input to I6 to I0 terminals by address data, and if an $\overline{ST}$ signal is then input, speech synthesis starts. Time is set if silence and BEEP tone were set by command. Figure 6.1 shows speech start timing. Figures 6.2 and 6.3 show timing when an address, other than a user phrase, is input.

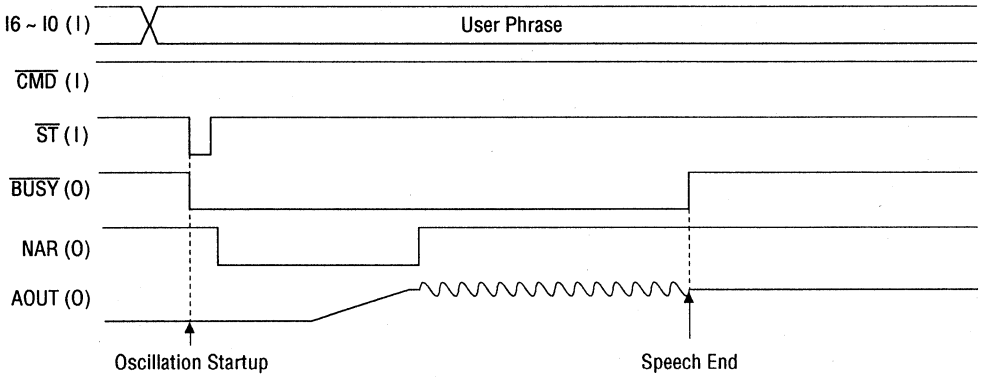


Figure 6.1 Speech Startup Timing

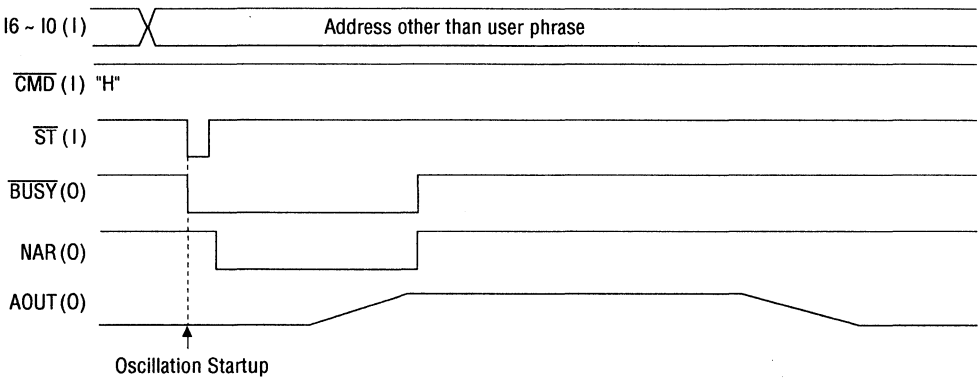


Figure 6.2 Timing when Address, other than User Phrase, Is Input in Standby Status

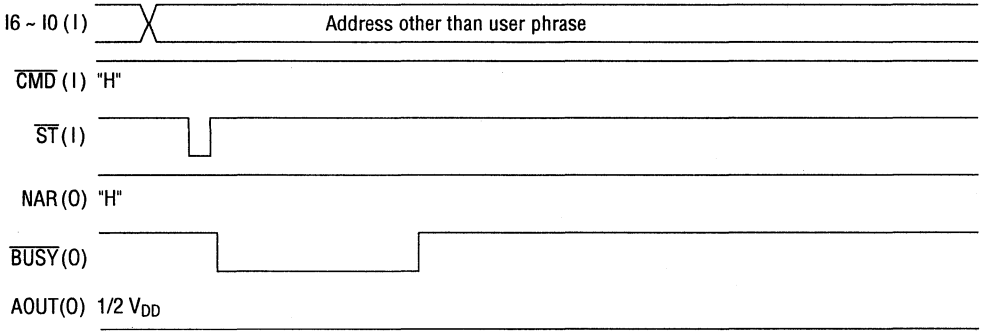


Figure 6.3 Timing when Address, other than User Phrase, Is Input in Status that AOUT is 1/2 V_{DD}

7. STOP CODE

If I6 to I0 are set to "0000000" during speech vocalization, and if an $\overline{ST}$ signal is input, vocalization regardless of "H" or "L" of NAR stops and AOUT becomes 1/2 V_{DD}.
STOP code becomes valid in rising of $\overline{ST}$ (common with serial and parallel).
Use the stop code only at setting "L" $\overline{BUSY}$ pin. The stop code cannot be used in states of standby-mode.

Figure 7.1 shows stop code input timing.

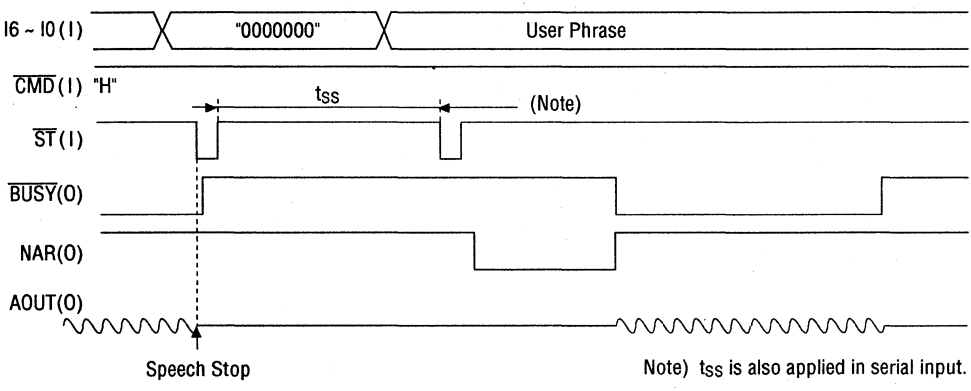


Figure 7.1 Stop Code Input Timing

If an $\overline{ST}$ signal is input by stop code in standby status, NAR stays in "H" level and AOUT becomes 1/2 V_{DD} after standby conversion time, as shown in Figure 7.2. If an $\overline{ST}$ signal is input by stop code in standby status, the status does not follow AC characteristics.

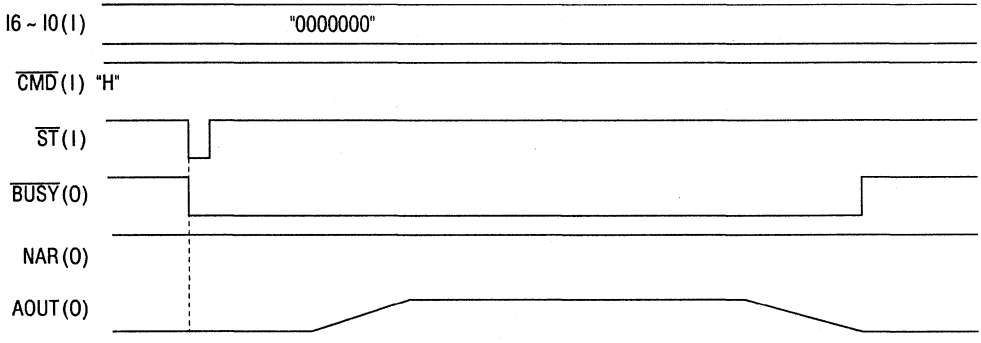


Figure 7.2 Timing when Stop Code Is Input in Standby Status

8. SAMPLING FREQUENCY

Sampling frequencies can be specified for each phrase in speech data of internal ROM. For channel synthesis, if channels 1 and 2 are regenerated at the same time, the channel 1 sampling frequency has priority.

For sampling frequency, the following 8 frequencies can be selected when creating speech data.

4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz

9. SPEECH VOCALIZATION TIME

Table 9.1 shows internal ROM configuration. The actual speech data ROM area is different from the indicated ROM capacity.

The speech data management area as shown in Table 9.1 is about 6 Kbit, and the edit ROM area includes 16 Kbit.

Table 9.1 ROM Configuration

Speech Data Management Area
Editing ROM Area
Speech Data Area
Disabled Area

Use the following formula as a guide to compute speech vocalization time.

$$\text{Vocalization Time} = \text{ROM Capacity} - 16 - 6) \times 1024 \times 255/256 \div \text{Bit Rate (kbps)}$$

For example, if data was created at a 4.0 kHz sampling using MSM6652 (288 kbit internal ROM), the vocalization time is

$$(288 - 16\text{-}6) \times 1024 \times 255/256 \div 16(\text{kbps}) = 16.9 \text{ sec}$$

10. CHANNEL STATUS

The $\overline{BUSY}$ pin and NAR pin output status signals.

$\overline{BUSY}$ pin outputs "L" level when either channel 1 or 2 is synthesizing speech. It is in "H" level when power is turned ON.

The NAR pin is the channel 1 and 2 input status signal (Next Address Request), enabled $\overline{ST}$ signal input when NAR is in "H" level. The channel status is switched by $\overline{CH}$ pin. If $\overline{CH}$ pin is in "H" level, the status signal of channel 1 is output, and if in "L" level, the status signal of channel 2 is output.

11. REGENERATION METHOD

The MSM6375 series has only the ADPCM regeneration method, however to support various speech MSM6650 has 3 types of regeneration methods: ADPCM, PCM and melody regeneration.

Respective features and how to select are explained below.

11.1 ADPCM Method

With the ADPCM (Adaptive Differential Pulse Code Modulation) method, basic quantization width Δ is adaptively changed for each sampling, and is encoded to 4bit data. This further improves the follow-up properties to speech wave forms.

Conversion to ADPDM data is performed by the AR76-202 analysis tool.

If the ADPCM method is used for human voices, animal cries and natural tones, the speech data capacity becomes smaller.

11.2 PCM Method

The PCM method of MSM6650 uses an 8-bit straight binary format. Of the three methods, PCM is the best for follow-up properties to speech wave forms.

This method is appropriate for sound effects where wave forms sharply change, and for pulse shaped wave forms.

11.3 Melody Regeneration Method

The AR76-202 analysis tool supports melody regeneration method. The melody data can make an unique sound because musical notes can be composed by the AR761.

11.4 Bit Rate of Each Method

The bit rate shows the degree of data compression and the data amount to synthesize for 1 second. The bit rate is determined by the relationship between the sampling frequency and the data-amount-per-sample. The following formula is used.

Bit Rate (kbps) = Sampling Frequency (kHz) × Data-amount-per-sample (bit)

The bit rate of the three methods are compared below when the sampling frequency is 6.4 kHz.

1) ADPCM Method

Bit Rate (kbps) = 6.4 kHz × 4 bit = 25.6 kbps

2) PCM Method

Bit Rate (kbps) = 6.4 kHz × 8 bit = 51.2 kbps

3) Melody Regeneration Method

With the melody regeneration method, the bit rate changes depending on each sound. The formula does not determine the bit rate changes. The average bit rate is 4 kbps.

11.5 The Regulations of channel synthesis about each regeneration methods

Melody regeneration and BEEP tone cannot be regenerated in 2 channel side. The regulations of channel synthesis about each regeneration methods as follows table 11.1.

11.5 The regulations of channel synthesis about each regeneration method

1 Channel	2 Channel	Setting
ADPCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
ADPCM(0dB～-18dB)	ADPCM(0dB)	○ Note1)
ADPCM(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
ADPCM(0dB～-18dB)	PCM(0dB)	○ Note1)
ADPCM(0dB)	PCM(0dB～-18dB)	○ Note1)
ADPCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
ADPCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
ADPCM(0dB～-18dB)	SILENCE	○
MELODY(0dB)	ADPCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	ADPCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	ADPCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	MELODY(0dB～-18dB)	×
MELODY(0dB)	PCM(0dB～-18dB)	○ Note1)
MELODY(0dB～-18dB)	PCM(0dB)	○ Note1)
MELODY(-6dB～-18dB)	PCM(-6dB～-18dB)	○
MELODY(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
MELODY(0dB～-18dB)	SILENCE	○
PCM(0dB)	ADPCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	MELODY(0dB～-18dB)	×
PCM(0dB)	PCM(0dB～-18dB)	○ Note1)
PCM(0dB～-18dB)	PCM(0dB)	○ Note1)
PCM(-6dB～-18dB)	PCM(-6dB～-18dB)	○
PCM(0dB～-18dB)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
PCM(0dB～-18dB)	SILENCE	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	ADPCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	MELODY(0dB～-18dB)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(0dB)	○ Note1)
BEEP TONE(1/2, 1/3, 1/4, 1/8)	PCM(-6dB～-18dB)	○
BEEP TONE(1/2, 1/3, 1/4, 1/8)	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
BEEP TONE(1/2, 1/3, 1/4, 1/8)	SILENCE	○
SILENCE	ADPCM(0dB～-18dB)	○
SILENCE	MELODY(0dB～-18dB)	×
SILENCE	PCM(0dB～-18dB)	○
SILENCE	BEEP TONE(1/2, 1/3, 1/4, 1/8)	×
SILENCE	SILENCE	○

Note1) In case of channel synthesis , confirm the voice quality with the MSM6650 evaluation board. Because , occasionally , there is possible of straining the voice by recording level and synthesis phrases .

12. EDIT ROM

The role of edit ROM is to link phrases and build sentences, making an external microcomputer unnecessary. The conventional MSM6375 family could not link phrases and synthesis channels in standalone mode, but the MSM6650 family can using edit ROM.

For example: The phrase "Today's weather is...." is used to compare the MSM6375 family and MSM6650 family. With the MSM6375 family, individual data must be stored to phrase ROM (see Table 12.1) when indivudual phrases of "Today's weather is sunny", and "Today's weather is rainy" are vocalized by timing of one time.

On the other hand, the MSM6650 family can vocalize plural phrases for edit ROM function by timing of only one time. If the edit ROM has the phrase ROM of Table 12.2, "Today's weather is sunny" will be vocalized by merely one time specifying address [01]. If address [02] is specified, "Today's weather is rainy" will be vocalized.

Conventionally data must be repeatedly stored to ROM to vocalize "Today's weather is....", but the storage of overlapped data is not required as shown in Table 12.2 by using edit ROM functions.

Table 12.1 Conventional Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's weather is sunny.
02	Today's weather is rainy.
03	Today's weather is sunny followed by cloudy, some areas are rainy.
⟨	⟨
7F	

Table 12.2 Phrase ROM Configuration

Address [HEX]	Phrase
01	Today's
02	weather
03	is
⟆	⟆
10	sunny
11	cloudy
12	rainy
13	snowy
20	occasional
21	followed by
22	some areas are
⟆	⟆
7F	

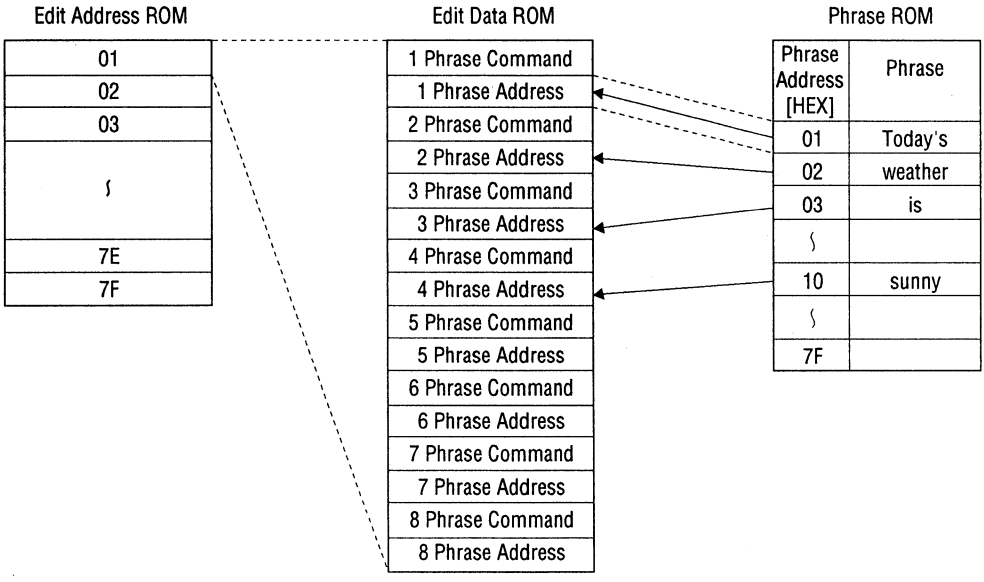
Table 12.3 Edit ROM Configuration

Address [HEX]	Edit Content [Max. 8 Phrases]
01	[01][02][03][10]
02	[01][02][03][12]
03	[01][02][03][10][21][11][22][12]
⟆	⟆
7F	

In edit ROM, not only phrase linking but channel synthesis, BEEP tone and silence can be set by command settings.

A maximum of 8 phrases (16 bytes) can be set in 1 edit. Table 12.4 shows the configuration of edit ROM.

Table 12.4 Edit ROM Configuration



Edit address ROM can process a maximum of 127 user specified phrases. Table 12.4 shows the relationship between phrase ROM, edit data ROM, and edit address ROM.

Phrase ROM cannot be directly accessed if edit ROM is used.

Edit ROM can be setup using the previously mentioned AR76-202analysis tool. For regeneration using edit ROM, regeneration may not be the one requested. Be certain to check the speech using either the analysis tool or MSM6650 of external ROM.

Figure 12.1 shows the flow chart when creating edit ROM.

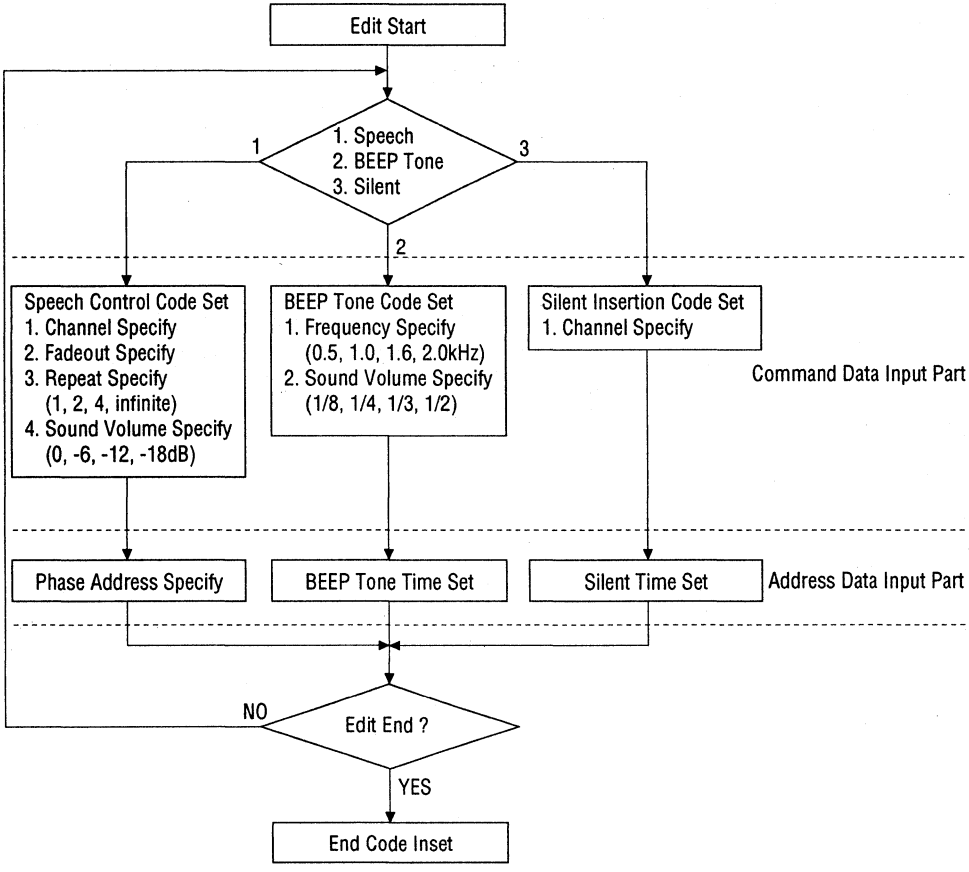


Figure 12.1 Edit Data ROM Creation Flow Chart

12.1 Edit ROM Commands

Table 12.5 shows the commands that can be set in edit ROM.

Table 12.5 List of Commands that Can Be Set in Edit ROM

O7	O6	O5	O4	O3	O2	O1	O0	Command
0	0	0	0	0	0	0	0	End Code
ch	0	1	0	0	0	0	0	Silence Insertion Code
1	1	0	0	bl1	bl0	bf1	bf0	BEEP Tone Code
ch	1	1	sm	rp1	rp0	vl1	vl0	Speech Control Code

The commands of the 4 codes shown in Table 12.5 are explained below.

12.1.1 End Code

End code means that one edit data is completed. Although this is necessary at the end of one edit data, since the LSI can recognize the end of editing, it is unnecessary when the maximum number of phrases are used.

12.1.2 Silence Insertion Code

Silence insertion code inserts silence to each channel, reducing speech data.

O7	O6	O5	O4	O3	O2	O1	O0
ch	0	1	0	0	0	0	0

The channel to insert silence is specified in command data, and silence time is set in address data.

The channel to insert silence is set to "O7" command data. If "O7" is "H" channel 1 is set, if "L" channel 2 is set.

Silence time is set at the address settings of phrases shown in Table 12.4.

Minimum Silence Time ... 16.384 ms
Maximum Silence Time ... 2.1 sec

The formula to set the silence time is shown below.

$t_{MU} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384$ ms

Table 12.6 Edit Data Example of Silence Insertion Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	0	1	0	0	0	0	0	Silence Insertion Code
2nd Byte	0	0	0	1	1	0	0	0	Silence Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data is set as in Table 12.6, 393 mS of silence is inserted to channel 1.

12.1.3 BEEP Tone Code

BEEP tone code vocalizes a BEEP tone without using ADPCM data. The sound volume and frequency of a BEEP tone is set in command data, and the vocalization time of a BEEP tone is set in address data.

The BEEP tone can be set only at channel 1.

To mix a BEEP tone and channel 2 vocalize an 8 kHz sampling frequency of a phrase at channel 2, this is because the sampling frequency of a BEEP tone is set to 8 kHz.
If the sampling frequency of channel 2 differs, speech at channel 2 may be either too slow or too fast.

O7	O6	O5	O4	O3	O2	O1	O0
1	1	0	0	bl1	bl0	bf1	bf0

The sound volume is set to O3, O2 and the frequency is set to O1, O0. Tables 12.7 and 12.8 show the sound volumes and the frequencies that can be set.

Table 12.7 Sound Volume Settings

O3	O2	Sound Volume
0	0	1/8 amplitude sound volume of channel 1
0	1	1/4 amplitude sound volume of channel 1
1	0	1/3 amplitude sound volume of channel 1
1	1	1/2 amplitude sound volume of channel 1

Table 12.8 Frequency Settings

O1	O0	Frequency
0	0	0.5 kHz
0	1	1.0 kHz
1	0	1.6 kHz
1	1	2.0 kHz

The BEEP tone time is set to the address setting of phrases shown in Table 12.4.

Minimum BEEP Tone Time ... 16.384 ms
Maximum BEEP Tone Time ... 2.1 sec

The formula to set a BEEP tone time is shown below.

$t_{MU} = (2^6 \times (O6)+2^5 \times (O5)+2^4 \times (O4)+2^3 \times (O3)+2^2 \times (O2)+2^1 \times (O1)+2^0 \times (O0)) \times 16.384$ ms

Table 12.9 Edit Data Example of BEEP Tone Code

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	0	0	1	1	0	1	BEEP Tone Insertion Code
2nd Byte	0	0	0	1	1	0	0	0	BEEP Tone Time
3rd Byte	0	0	0	0	0	0	0	0	End Code

For example, if edit data are set as in Table 12.9, Beep sound of 1.0kHz is vocalized for 393 ms with 1/2 of amplitude of sound volume of channel 1.

12.1.4 Speech Control Code

Speech control code can set repeat and sound volume.

O7	O6	O5	O4	O3	O2	O1	O0
ch	1	1	sm	rp1	rp0	vl1	vl0

The channel is set at "O7". If "O7" is "H", channel 1 is set, if "L" channel, 2 is set. The speech control condition of each channel is set between O4 to O0.

1) Setting Number of Repeats

The number of repeats is set at O3 and O2, and can be selected from 4 types: 1, 2, 4 and infinite. If infinite is selected, repeat can be stopped by inputting stop code.

Table 12.10 shows the relationship between O3, O2 and the number of repeats.

Table 12.10 Number of Repeats Settings

O3	O2	Number of Repeats
0	0	1
0	1	2
1	0	4
1	1	Infinite

2) Sound Volume Smoothing During Repeat

If "O4" is set to "H", sound volume during repeat is attenuated from 1 to 1/2, 1/4 and 1/8. This smoothing, however, is effective only when 2, 4 or infinite is selected at repeat setting.

If infinite is selected, speech is vocalized remaining at 1/8 after attenuating from 1, 1/2, 1/4 and to 1/8. If the initial sound volume setting is other than 1, the sound volume attenuates from that value in 1/2 units, stopping at 1/8.

3) Setting Sound Volume

Speech to vocalize can be changed in 4 steps if speech is vocalized overlapping in channel synthesis. The sound volume is set at O1 and O0. Table 12.11 shows the correspondence.

Table 12.11 Attenuation Volume Setting

O1	O0	Attenuation Volume
0	0	No attenuation (sound volume is same as speech data)
0	1	-6 dB attenuation (sound volume is 1/2 of speech data)
1	0	-12 dB attenuation (sound volume is 1/4 of speech data)
1	1	-18 dB attenuation (sound volume is 1/8 of speech data)

12.2 PCM Regeneration in Edit ROM

For PCM regeneration, edit data is set together with speech control code. All settable items in speech control code (channel, sound volume smoothing during repeat, number of repeats, and sound volume) can be set.

12.3 Melody Regeneration in Edit ROM

For melody regeneration, edit data is set together with speech control code. Channels however cannot be set. Channel 1 is fixed. Channel 2 mixing of melody regeneration/melody regeneration combination is not possible.

All settable items in speech control code can be set except channels.

12.4 Continuous Regeneration in Edit ROM

If at the 2nd edit phrase is input during speech vocalization of the 1st edit phrase (phrase consists of 16 bytes or less of edit data ROM: referred to as edit phrase), speech vocalization starts continuously after 1st edit phrase vocalization ends.

However, this occurs only when the channel setting of the 1st and 2nd edit phrase are the same, and when echo regeneration and channel 2 regeneration are not performed. For example, if the 1st edit phrase is echo regeneration, and the 2nd edit phrase channel 1 regeneration, as shown in Figure 12.2 edit phrases overlap.

To avoid this, insert silence to channel 1, as shown in Figure 12.2, and set edit data ROM so that channels 1 and 2 end regeneration at the same time.

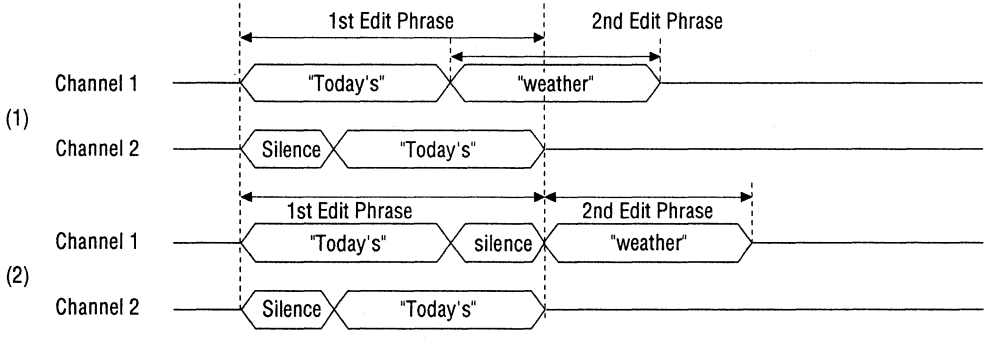


Figure 12.2 Example of Continuous Regeneration Timing

12.5 Channel 2 Mixing Function in Edit ROM

This function overlaps 2 phrases.

By using edit ROM, it is easy to echo a phrase (echo regeneration) and to vocalize a phrase with a musical instrument sound or BGM (channel 2 regeneration).

12.5.1 Echo Regeneration

Echo regeneration delays and overlaps -6 dB attenuation (1/2 amplitude speech wave form of channel 1) to a speech wave form vocalized at channel 1.

ECHO REPRODUCTION OF MULTIPLE PHRASES

Using address [02] of phrase ROM, "weather", an echo regeneration edit data example in Table 12.2, is explained below.

Table 12.2 Edit Data Example of 1 Phrase Echo Regeneration

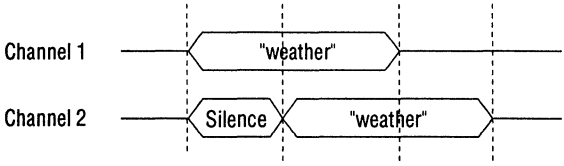
	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat, no attenuation)
2nd Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	0	1	Speech Control Code (2ch setting, repeat, -6 dB attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
7th Byte	0	0	0	0	0	0	0	0	End code

If edit data is set as in Table 12.12 , "weather" is vocalized at channel 1, and is overlapped and vocalized from channel 2 with a -6 dB attenuated sound volume 98.3 ms later.

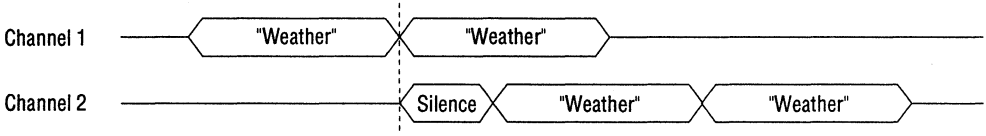
When 2 phrases overlap, set the attenuation of the speech control command with attention to sound volume.

The silence time by silence insertion code is a factor that influences echo quality. Set the silence time so that the desired echo is created.

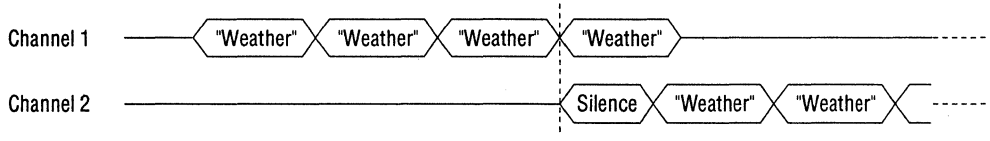
When performing echo regeneration set the number of repeats of the speech control command to 1. If 2, 4 or infinite is set, timing becomes as shown in Figure 12.3. This figure shows that the number of repeats of the 1st and 5th byte of edit data in Table 12.12 have changed.



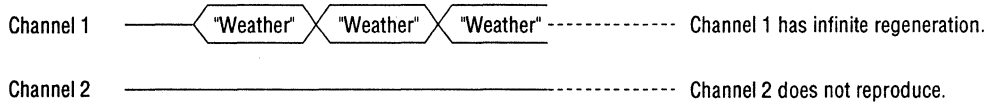
(1) Number of Repeats: 1



(2) Number of Repeats: 2



(3) Number of Repeats: 4



(4) Number of Repeats: infinite

Figure 12.3 Vocalization Timing of Echo Reproduction According to Number of Repeats

The vocalization timing, when the number of repeats of the speech control command is set for an edit data phrase, is explained below.

① When number of repeats is set to 1

If the same channel is specified for the next phrase, vocalization of the next phrase starts when vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of vocalization.

② When number of repeats is set to 2

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the second vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the second vocalization after the first vocalization ends.

③ When number of repeats is set to 4

If the same channel is specified for the next phrase, vocalization of the next phrase starts when the fourth vocalization ends. If the channel of the next phrase is different, channel synthesis starts at the start of the fourth vocalization after the 3rd vocalization ends.

④ When number of repeats is set to infinite

The next phrase becomes invalid and is not vocalized regardless the channel specification.

ECHO REPRODUCTION OF MULTIPLE PHRASES

A maximum of 8 phrases (16 bytes) are set to one edit data ROM. Up to 3 phrases are possible for an echo reproduction with 16 bytes. Set the phrase ROM so that the number of phrases do not exceed four.

Using "Today's", "weather" and "is" of the phrase ROM in Table 12.2 as an example, Table 12.13 shows a three phrase echo regeneration edit data example, and Figure 12.4 shows vocalization timing.

Table 12.13 Three Phrase Echo Regeneration Edit Data Example

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	0	0	0	0	1	1	0	Silence Time (98.3 mS)
5th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting repeat once, -12 dB attenuation)
6th Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
7th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
8th Byte	0	0	0	0	0	0	1	0	Phrae Address (02H "weather")
9th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
10th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
11th Byte	1	1	1	0	0	0	0	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
12th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
13th Byte	0	1	1	0	0	0	1	0	Speech Control Code (2ch setting, repeat once, -12 dB attenuation)
14th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
15th Byte	1	1	1	0	0	0	1	1	Speech Control Code (1ch setting, repeat once, -6 dB attenuation)
16th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")

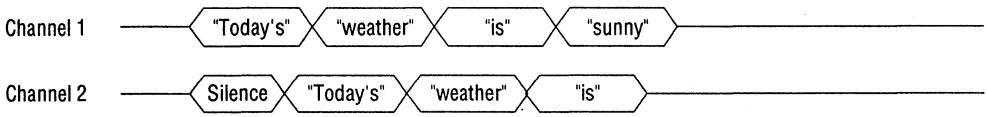


Figure 12.4 Vocalization Timing of a Three Phrase Echo Regeneration

For the echo regeneration of multiple phrases, set so that the sampling frequency of each phrase is the same. If a phrase with a different sampling frequency is mixed, the speech of channel 2 will become fast or slow because the sampling frequency of channel 1 has priority. Figure 12.5 shows the timing.

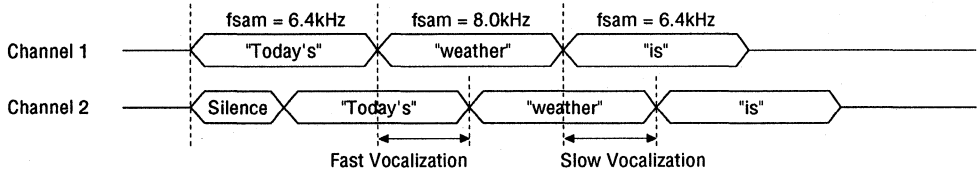


Figure 12.5 Vocalization Timing of Echo Regenerations with Different Sampling Frequencies

ECHO REPRODUCTION OF AN ARBITRARY PHRASE IN MULTIPLE PHRASES

Table 12.14 shows an edit data example to apply echo to "is" in the four phrases of "Today's", "weather", "is" and "sunny".

Table 12.14 Edit Data Example of 1 Phrase Echo Regeneration

	O7	O6	O5	O4	O3	O2	O1	O0	
1st Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
2nd Byte	0	0	0	0	0	0	0	1	Phrase Address (01H "Today's")
3rd Byte	0	0	1	0	0	0	0	0	Silence Insertion Code (2ch setting)
4th Byte	0	1	1	0	0	0	0	1	Silence Time (1.59 mS)
5th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting repeat once, no attenuation)
6th Byte	0	0	0	0	0	0	1	0	Phrase Address (02H "weather")
7th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
8th Byte	0	0	0	1	0	0	0	0	Phrae Address (10H "is")
9th Byte	0	1	1	0	0	0	0	1	Speech Control Code (2ch setting, repeat once, -6 dB attenuation)
10th Byte	0	0	0	1	0	0	0	0	Phrase Address (10H "is")
11th Byte	1	1	1	0	0	0	0	0	Speech Control Code (1ch setting, repeat once, no attenuation)
12th Byte	0	0	0	0	0	0	1	1	Phrase Address (03H "sunny")
13th Byte	0	0	0	0	0	0	0	0	End Code

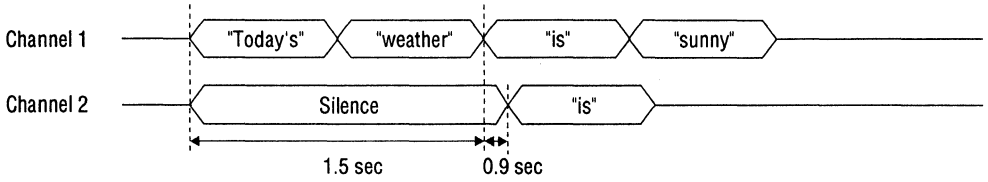


Figure 12.6 Vocalization Timing Using Edit Data of Table 12.14

As shown by the timing in Figure 12.6, "is" is echoed by setting the silence time, which is the addition of the vocalization time for "Today's" and "weather" and the delay time for echo to channel 2. If the silence time exceeds 2.1 sec, it is necessary to add a silence insertion setting to 2 bytes of edit data.

For the echo reproduction of one arbitrary phrase of multiple phrases, a maximum of 6 phrases are possible if the silence insertion setting is 2 bytes.

12.5.2 Two-channel Regeneration

Two-channel regeneration uses PCM, melody and ADPCM methods. Channel synthesis is possible with all combinations except a melody regeneration / melody regeneration combination. Melody regeneration is fixed to channel 1. The sampling frequency of phrases to be overlapped must be the same.

Figures 12.7 to 12.10 show the vocalization timings of two-channel regeneration.

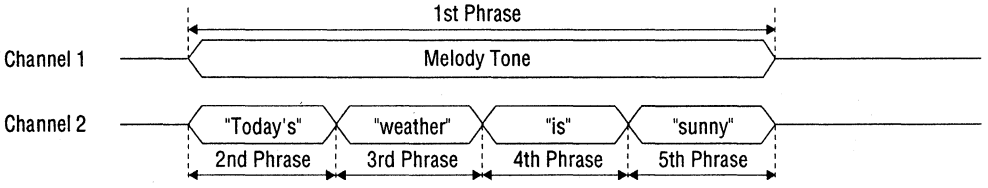


Figure 12.7 Example of Four Phrase Channel Synthesis Timing with Melody Tone as GBM

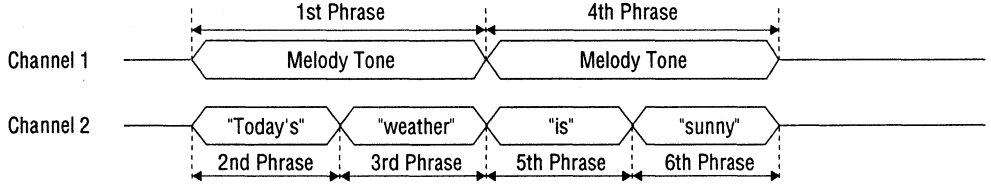


Figure 12.8 Example of Four Phrase Channel Syntehsis Timing with Melody Tone and 1st and 4th Phrases as BGM

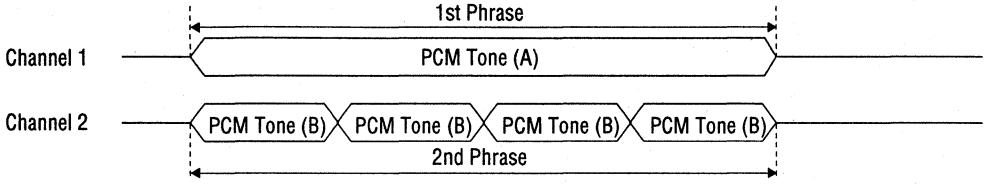


Figure 12.9 Example of Channel Synthesis between PCM Main Melody Tone (A) and PCM Rhythm Tone (B) with 4 Repeats

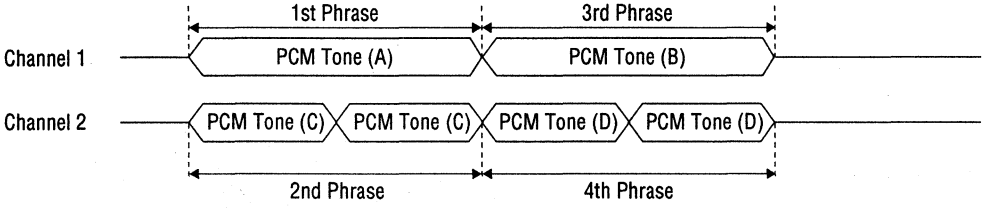


Figure 12.10 Example of Channel Synthesis between PCM Main Melody Tone (A), (B) and PCM Rhythm Tone (C), (D) with 2 Repeats

13. STANDBY CONVERSION

If standby conversion YES is selected by command option, if the next phrase does not startup within 0.2 sec after vocalization ends, the LSI enters standby status and stops all operations. If restarted it takes about 100 ms until speech starts, since a pop noise countermeasure circuit operates .

If standby conversion NO is selected by command option, the LSI does not enter standby status, even if speech ends, and the output of AOUT becomes about 1/2 VDD. Current is flowing since oscillation is operating. If started up speech starts in about 350 µs.

If standby conversion NO is selected, it is necessary to input an $\overline{\text{RESET}}$ pulse to enter standby status.

If an $\overline{\text{RESET}}$ pulse is input, a pop noise is generated since the AOUT output level instantaneously becomes GND level.

14. SPEECH OUTPUT

For the speech output terminal, a command option can select whether the DA converter output is directly output or output through an internal low pass filter.
Table14.1 shows output level of AOUT pin

Table 14.1 Output level of AOUT pin

Regeneration method	Conditions	Most lowest level	Centre level	Most highest level
ADPCM	DA converter output	0	About 0.5 x VDD	About VDD
	LPF output	About 0.15 x VDD	About 0.5 x VDD	About 0.95 x VDD
PCM	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
Melody	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD
BEEP Tone	-	About 0.25 x VDD	About 0.5 x VDD	About 0.75 x VDD

14.1 DA Converter Output Wave Form

The output amplitude from the DA converter becomes a step wave form synchronizing the sampling frequency at a maximum 4095/4096 × VDD.

If DA output is selected, it is recommended to externally attach a low pass filter. Since the output impedance of a DA converter changes between 15 kΩ to 35 kΩ, determine the filter constant so that this resistance change does not affect the cutoff frequency of the low pass filter.

14.2 Low Pass Filter Output

A low pass filter consists of switched capacitors. The attenuation characteristic of the MSM6650 low pass filter is -40 dB/oct. The cutoff frequency changes depending on the sampling frequency.

Table 14.2 shows the relationship between sampling frequency and cutoff frequency.

Table 14.2 Cutoff Frequencies of Low Pass Filter

Sampling Frequency (fsam)	Cut-off Frequency (fcut)
4.0kHz	About 1.8kHz
5.3kHz	About 2.6kHz
6.4kHz	About 2.6kHz
8.0kHz	About 3.2kHz
10.6kHz	About 4.2kHz
12.8kHz	About 5.1kHz
16.0kHz	About 6.4kHz
32.0kHz	About 12.8kHz

15. EXTERNAL ROM DRIVING TIMING

Figure 15.1 shows the external ROM driving timing during speech regeneration at f_{OSC} = 4.096 MHz, f_S = 8.0 kHz.

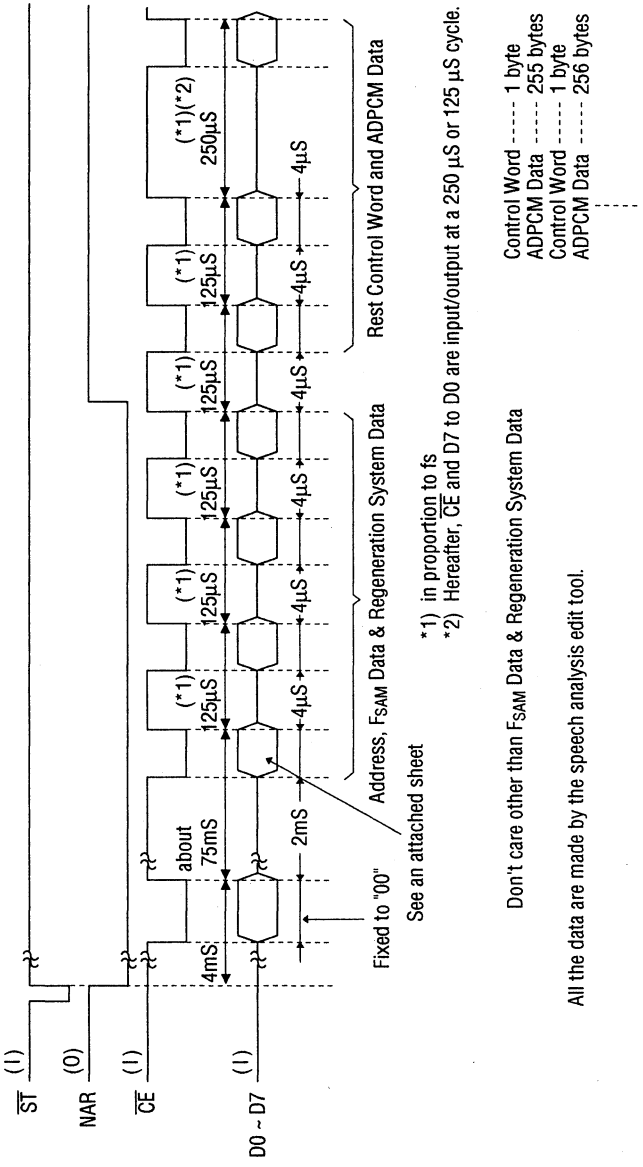


Figure 15.1 External ROM Driving Timing

Attached Sheet

1) f_{sam} Data

O2	O1	O0	Sampling Frequency
0	0	0	8.0kHz
0	0	1	10.6kHz
0	1	0	12.8kHz
0	1	1	32.0kHz
1	0	0	4.0kHz
1	0	1	5.3kHz
1	1	0	6.4kHz
1	1	1	16.0kHz

2) Regeneration System Data

O7	O6	Regeneration System
0	0	Regeneration by ADPCM
0	1	Regeneration by PCM
1	0	Melody regeneration

Melody regeneration can not be controlled externally.

16. CERAMIC OSCILLATION

Figure16.1 shows an external circuit diagram using a ceramic oscillator.

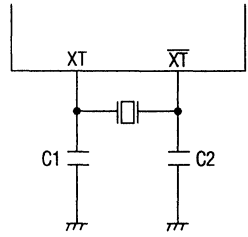


Figure 16.1 External circuit diagram

Figure 16.2 and 16.3 show external circuit diagrams using a cermic oscillator, CSA4.09MGU and CST4.09MGWU made by Murata Seisakusho Co., ltd.

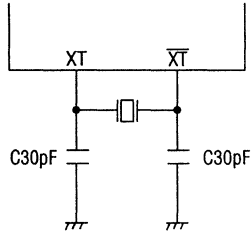


Figure 16.2 CSA4.09MGU

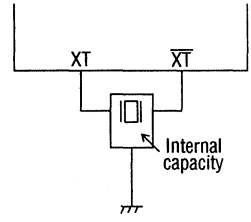


Figure 16.3 CST4.09MGWU

Figure 16.4 shows an external circuit diagram using a cermic oscillator, PBRC4.00MSA/MSK/MWS made by Kyocera Co., ltd.

Note) In case of using a oscillator 4.00MHz, vocalization speed is low about 2% than AR76-202 analysis tool and evaluation board.

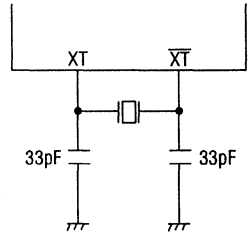
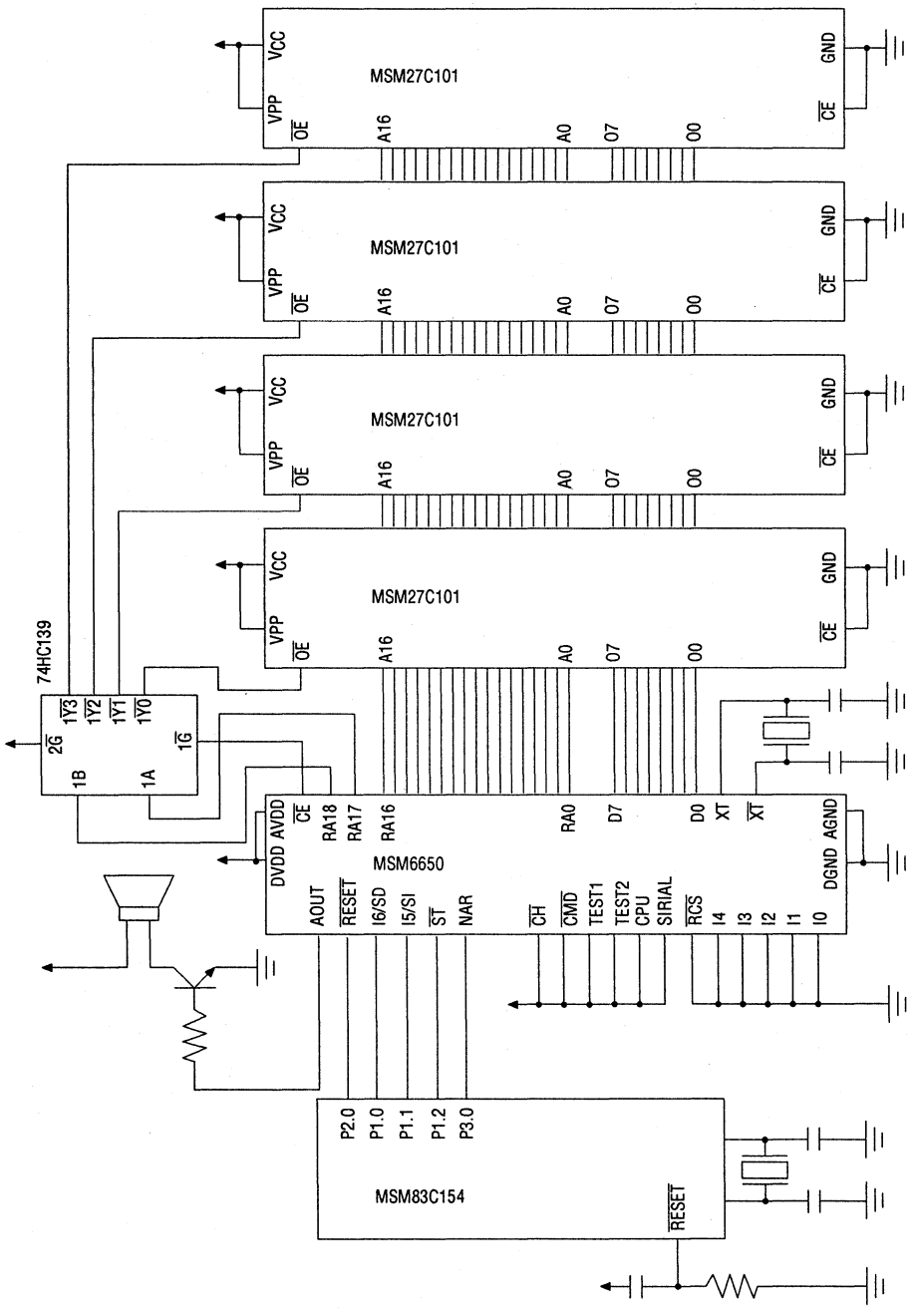
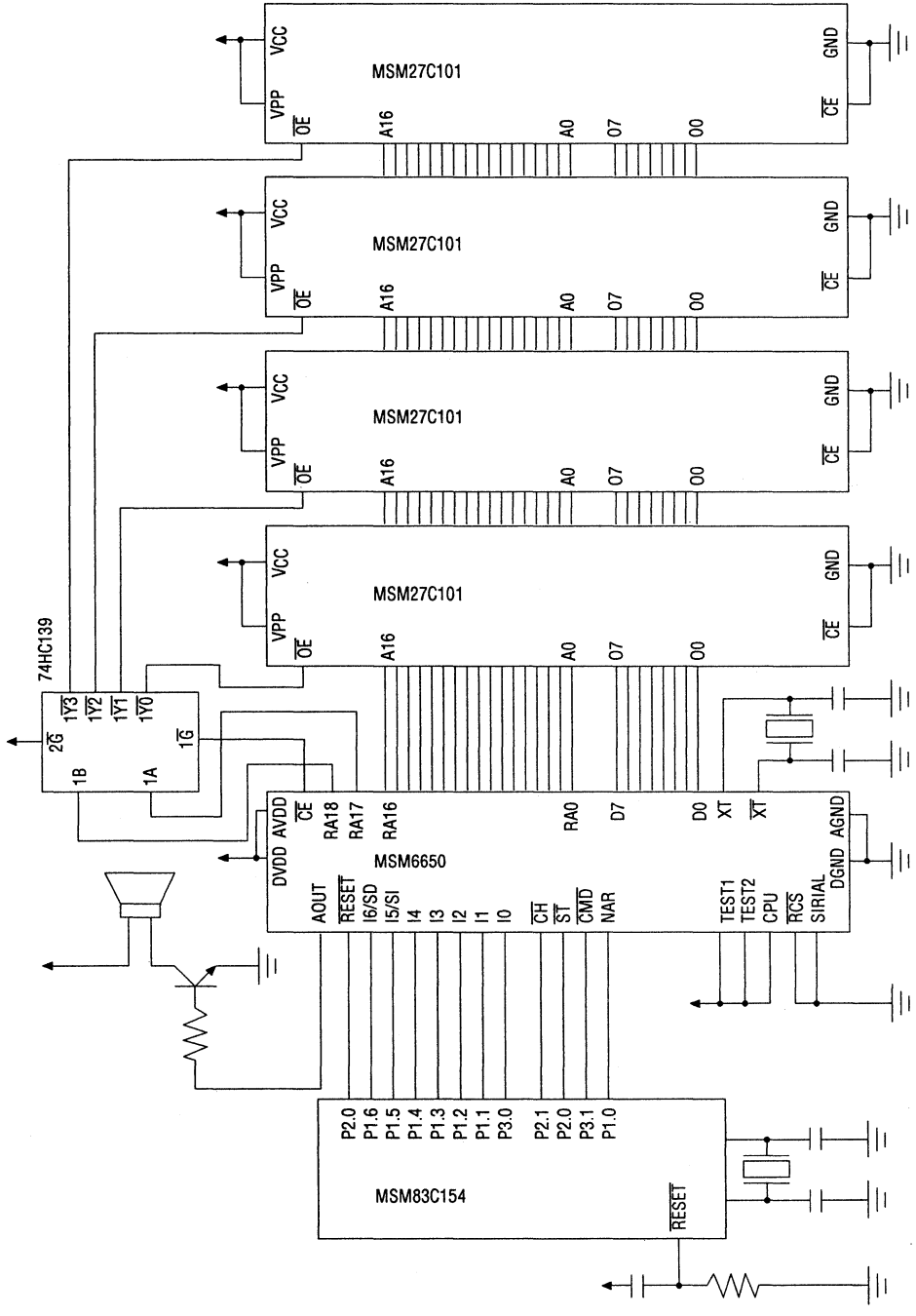


Figure 16.4 PRBC 4.00 MSA/MSK/MWS

APPLICATION CIRCUIT EXAMPLE



Application circuit example when four 1 M-bit EPROMs are used (serial input interface).



Application circuit example when four 1 M-bit EPROMs are used (parallel input interface).

Voice Recorder

OKI Semiconductor

MSM5218

ADPCM SPEECH ANALYSIS/SYNTHESIS IC

GENERAL DESCRIPTION

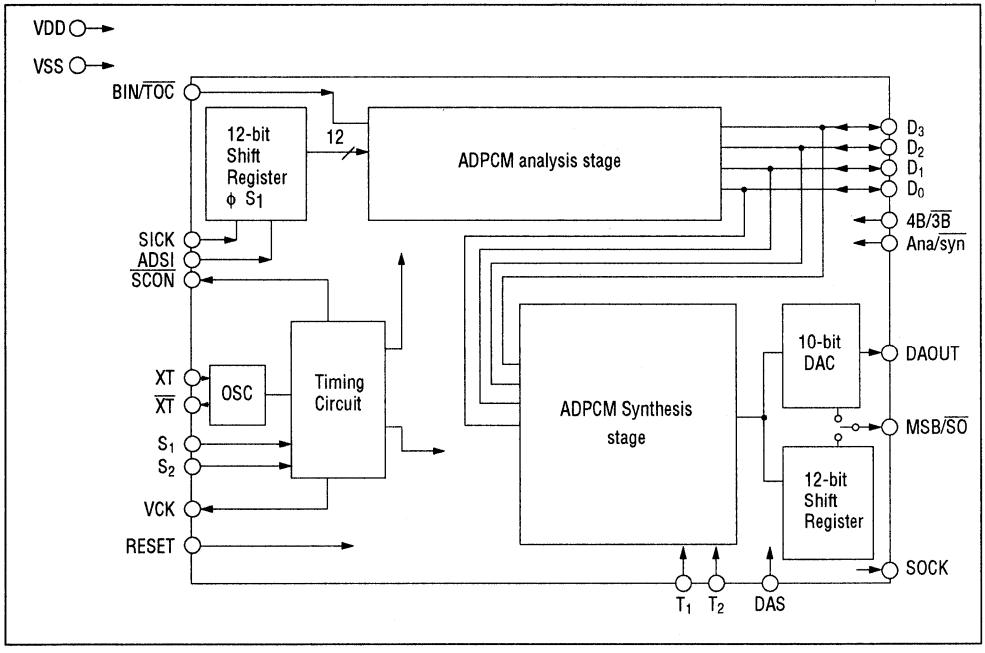
The MSM5218 is a complete speech analysis/synthesis LSI featuring the Adaptive Differential Pulse Code Modulation (ADPCM) method of data compression. The MSM5218 contains an analysis stage where serial PCM data is compressed to 3- or 4-bit parallel ADPCM data. In addition, a synthesis stage synthesizes PCM data from ADPCM data. This PCM data can be output directly or routed to the internal 10-bit DAC for analog signal output.

In addition to simplifying speech analysis and simulation, this circuit enables users to develop their own speech analysis and synthesis systems.

FEATURES

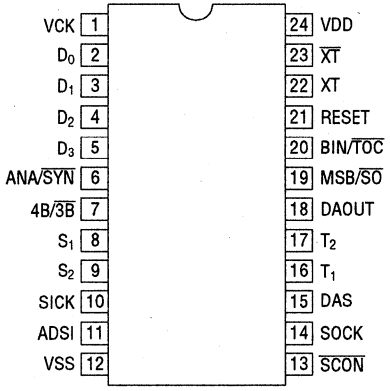
- One-chip speech analyzer/synthesizer
- 3- or 4-bit ADPCM system
- ADPCM data compatible with Oki's synthesis LSI MSM5205RS
- Single power supply
- Variable sampling frequency (4 kHz, 6 kHz, 8 kHz)
- Lower power consumption CMOS process (15 mW typical)
- Built-in 10-bit D/A converted for analog output
- Handshaking signals provided for synchronous operation with an external A/D converter.
- 24-pin plastic DIP, (DIP24-P-600)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

(Top View) 24 Lead Plastic DIP



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	T_a = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD}	V
Power dissipation	P_D	T_a = 25°C	200 max	mW
Storage temperature	T_{stg}	–	−55 ~ + 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD	–	+3 ~ +6	V
Operating temperature	Top	–	−30 ~ +70	°C
Oscillator Frequency	fosc	Specified Oscillator	386 ~ 768	kHz

D.C./A.C. CHARACTERISTICS

(VDD = 5V± 5%, Ta = –30°C to +70°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except XT, T_1, T_2	4.2	–	–	V
Input Low Voltage	V_{IL}	All inputs except XT, T_1, T_2	–	–	0.8	V
Input High Current (1)	I_{IH}	V_{IN} = VDD	–	–	1	µA
Input Low Current	I_{IL}	V_{IN} = 0V	–	–	–1	µA
Output High Current	I_{OH}	$\overline{SCON}$, VCK, SOCK, MSB/$\overline{SO}$, D0~D3 V_0 = 4.2V	–50	–	–	µA
Output Low Current	I_{OL}	$\overline{SCON}$, VCK SOCK, MSB/$\overline{SO}$, D0~D3 V_0 = 0.4V	50	–	–	µA
Operating Current	I_{DD}	f_{VCK} = 8kHZ	–	3	6	mA
Operating Current	I_{DD}	f_{VCK} = 16 kHz	–	6	12	mA
DA. OUT Output Impedance	V_{OR}	–	–	100	–	kΩ
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale VDD = +5V	– –	±4	–	LSB
SICK Clock Frequency	f_{SICK}	–	–	–	500	kHz
Input High Current (2)	I_{IH2}	V_{IN} = VDD Note 1	20	–	400	µA

Note 1: Applicable for Reset.

PIN DESCRIPTION

Pin Name	Terminal Number	I/O
	24 DIP	
VCK	1	O
This pin outputs a signal whose frequency is equal to the sampling frequency selected by S1, S2 inputs.		
D_0	2	I/O
D_1	3	I/O
D_2	4	I/O
D_3	5	I/O
Data I/O port for the ADPCM data. For 3-bit ADPCM data, D_0 input is not used.		
ANA/$\overline{SYN}$	6	I
Analyze/synthesize function selector. Controls data I/O port direction. When high, data I/O are outputs and simultaneous analysis and synthesis occur. When low, data I/O are inputs and no analysis occurs.		
4B/$\overline{3B}$	7	I
Specifies whether 3-bit or 4-bit ADPCM data is to be used. High = 4-bit.		
S_1	8	I
S_2	9	I
These inputs select the sampling frequency according to figure 1.		
SICK	10	I
Clock input for clocking in serial PCM data from an external ADC into the internal 12-bit shift register.		
ADSI	11	I
Serial PCM data.		
VSS	12	—
Ground (0 V)		
$\overline{SCON}$	13	O
Output which signals the start of conversion.		
SOCK	14	O
When serial PCM data output mode is selected (DAS = H), this pin provides a 192 kHz signal which is synchronized with the output of the serial PCM data through the MSB/$\overline{SO}$ pin. Each bit of the 12-bit PCM data will be valid before the positive edge of this 192 kHz signal.		
DAS	15	I
Selected for analog signal output (DAS = L), or serial PCM data output (DAS = H).		
T_1	16	I
T_2	17	I
IC test pins used at the factory for testing purposes only. During normal operation, T_1 is grounded and T_2 is left open.		
DAOUT	18	O
Analog signal output pin.		
MSB/$\overline{SO}$	19	O
MSB/serial data output pin – MSB of the data in the internal 10-bit DAC will appear at this pin if analog signal output mode (DAS = L) is selected. When serial PCM data output mode is selected (DA = H), serial PCM data can be clocked out of this pin.		

Pin Name	Terminal Number	I/O
	24 DIP	
BIN/$\overline{TOC}$	20	I

Specifies whether the input serial PCM data is in binary or 2's complement form.

RESET	21	I

An active high input which initializes the MSM5218RS internal circuitry. To be effective, must be held true for at least one VCK time.

XT	22	I
$\overline{XT}$	23	O

Oscillator inputs for a 384 kHz crystal or ceramic resonator (Figure 2).

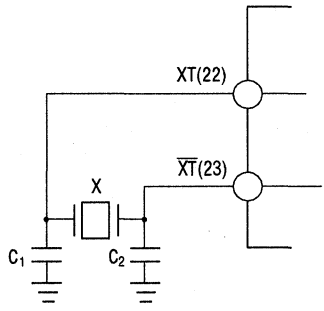
VDD	24	—

Power supply pin. (typical +5V)

S1	S2	Sampling Frequency
L	L	4 kHz (384 kHz/96)
L	H	6 kHz (384 kHz/64)
H	L	8 kHz (384 kHz/48)
H	H	Prohibited

Note: The 384 kHz resonator must be used with 4kHz, 6kHz, 8kHz.
Other oscillator frequencies are possible and will proportionately modify the sampling rate.

Figure 1



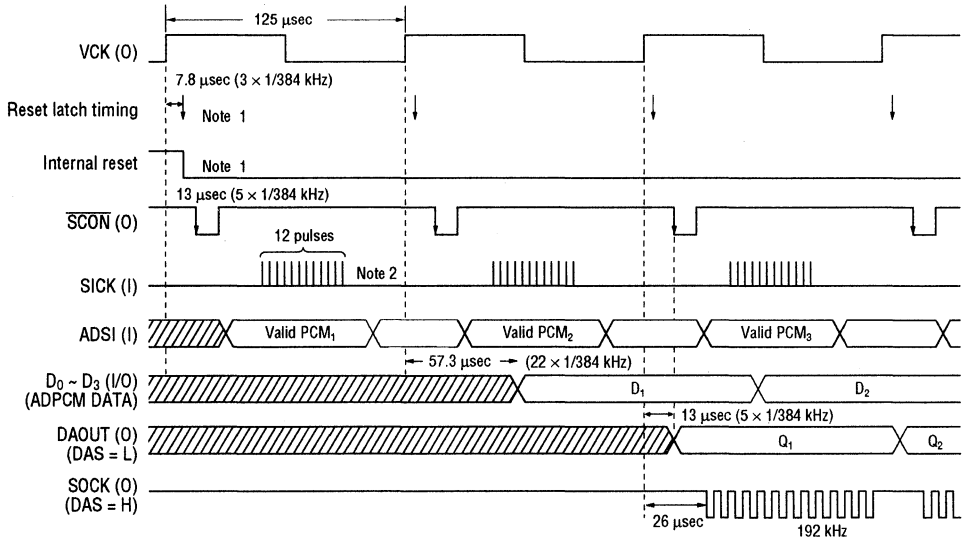
XT and $\overline{XT}$ (Oscillator connector pins)

X-384 kHz
C_1-220pF
C_2-220pF

Murata Corporation
CSB 384P
Or as required to match crystal or ceramic resonator load specifications.

Figure 2

ANALYSIS WITH SIMULTANEOUS SYNTHESIS (f_S = 8 kHz)

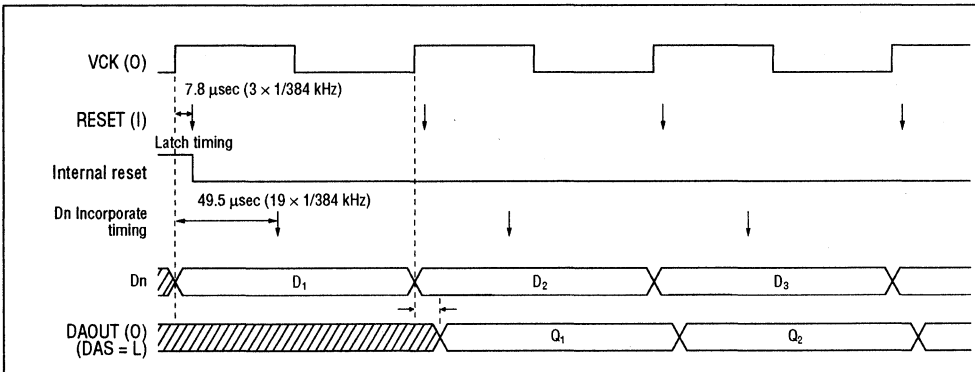


Note 1 The state of the RESET input is strobed into the internal reset latch by the reset latch timing pulse. Analysis begins on the H to L transition of internal reset.

Note 2 Up to 12 bits of PCM data may be strobed into the device by SICK. If more than 12 SICK pulses occur in a given VCK cycle, only the last 12 are regarded as valid. The cycle of SICK pulses must be completed before the next SCON- pulse.

PCMn: nth input PCM data (12-bit)

SYNTHESIS ONLY (f_{SAMPLE} = 8 kHz)



Dn: nth ADPCM data.
Qn: Analog Output corresponding to input nth ADPCM data.

Figure 3

BLOCK DIAGRAM - ANALYZER

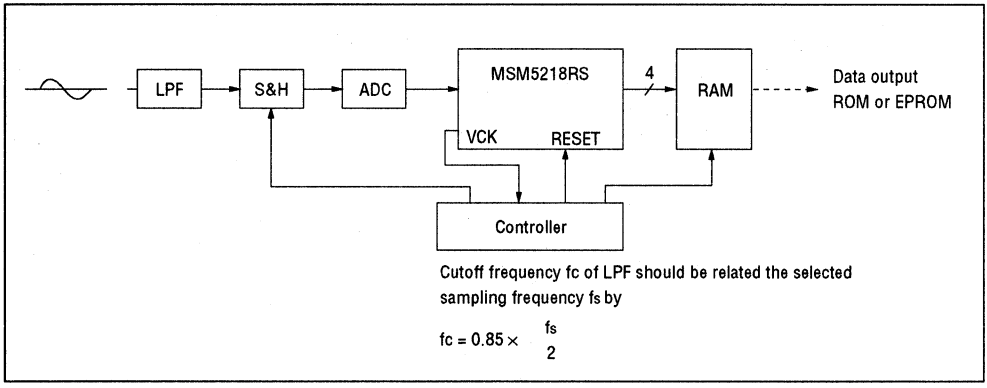


Figure 4

BLOCK DIAGRAM - SYNTHESIZER

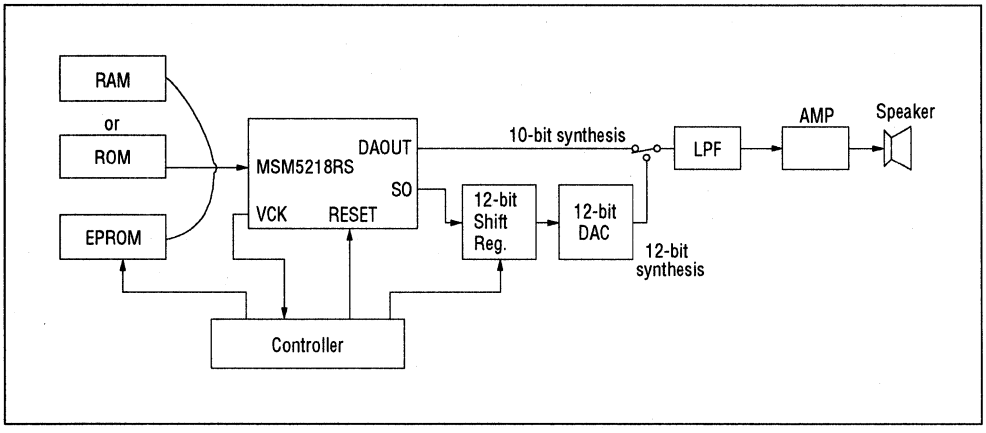


Figure 5

THE FOLLOWING TIMING SHOWS HOW TO APPLY THE RESET

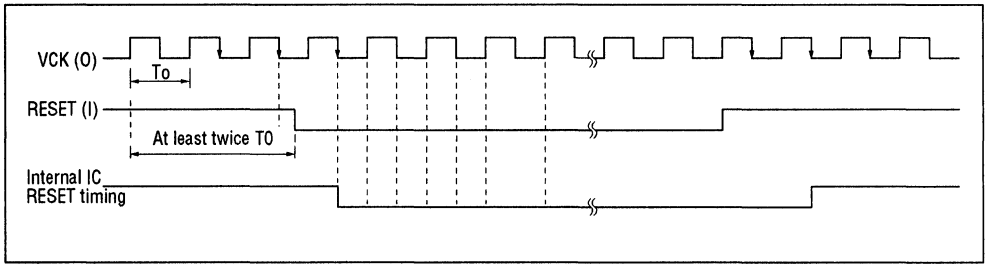


Figure 6 MSM5205 Reset Timing

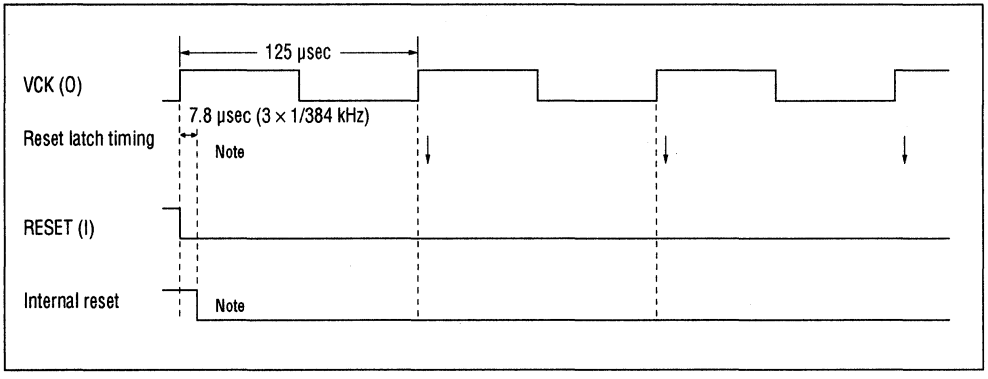


Figure 7 MSM5218 Reset Timing (fsample = 8kHz)

Note: The reset signal is latched within the LSI by the reset latch timing. Analysis is commenced by switching the external reset signal from H to L before this timing. Switching is probably best achieved by the leading edge of the VCK signal.

DA converter SN ratio improvement method

The accuracy near the center of the voice waveform of this LSI may be worse due to the configuration of the DA converter. Therefore, the SN ratio can be improved by shifting the waveform center up or down. This is an extremely effective method for improving the SN ratio of a small signal or improving residual noise during silence (between 2 speech patterns.)

To put it concretely, by adding data before or after the current ADPCM data (voice data), the waveform center can be shifted as shown in Figure 8.

Adding data is as follows:

(A) section	(B) section	
0 0 0 0	1 0 0 0	
0 0 0 0	1 0 0 0	100 data
⋮	⋮	

(The ADPCM bit length is 4-bits.)

Since an offset of about 5 mV can be obtained for respection 2 samples of data, it is recommended that about 100 samples of data be entered to shift the waveform center about 250 mV.

For 3-bit data, an offset of about 5 mV can be obtained for each data. Therefore, about 50 samples of data is required to be entered to shift the waveform center about 250 mV.

In the (A) section, the waveform center should be shifted up. In the (B) section, the waveform center should be shifted down. The number of data in the (A) section should be the same as that in the (B) section.

When (A) is added before voice data and (B) is added after the voice data, the output waveform is as shown in Figure 8.

Since the dynamic range is narrowed by the shifted area, some data may overflow, causing the voice to be distorted.

If this occurs, decrease the sound pressure about 20% and analyze the data once again. (For an overflow, see the precautions for ADPCM data creation on the next page.)

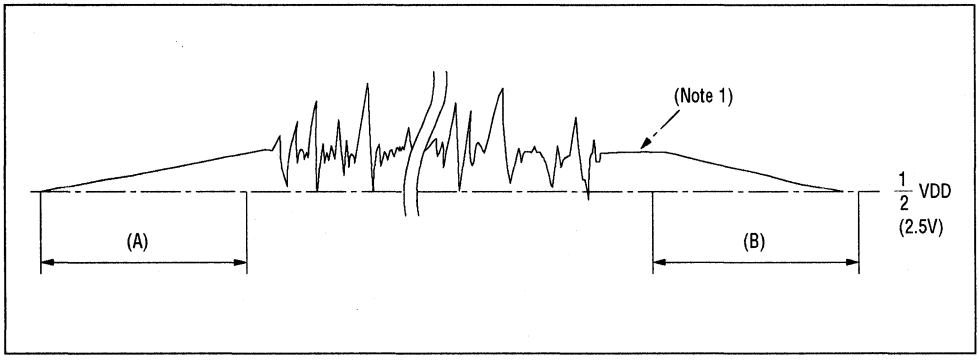


Figure 8 Waveform the DA Converter

Note 1: Voice data should be sufficiently small just prior to (B). For voice editing, insert a silence of about 10msec.

Precaution for ADPCM data creation

When voices are synthesized by the MSM5205 using the ADCPM data analyzed by the MSM5218, noise may be generated in the composite voice.

The MSM5205 is not equipped with an overflow protection unit in the internal operation circuit even though the MSM5218 is. Therefore, although the MSM5218 produces normal voice, the MSM5205 may cause noise in the composite voice due to an overflow in the data. If this occurs, analyze and create the ADPCM data once again.

An example of a waveform when an overflow occurs and the overflow protection method are as follows:

(1) Waveform when an overflow occurs

The observation of the output waveform from the DA converter of the MSM5205 on an oscilloscope shows that an overflowed waveform is looped as shown in Figure 9.

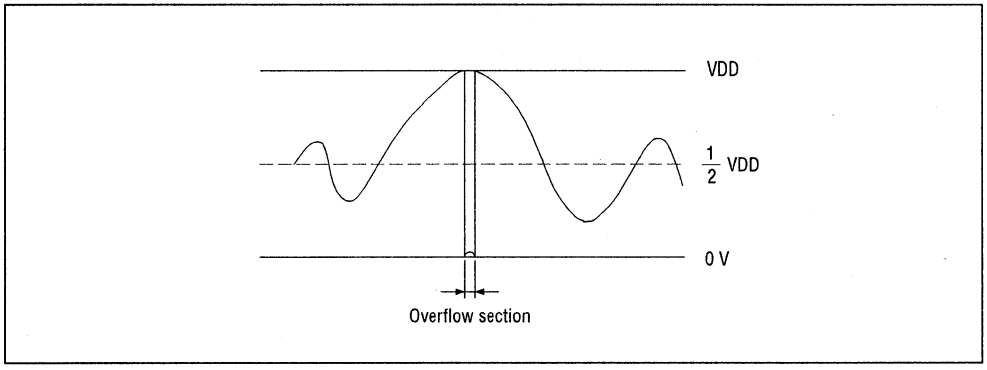


Figure 9 Output Waveform When an Overflow Occurs

(2) Overflow protection method

Even if an input waveform is not beyond the dynamic range when the ADPCM data is analyzed by the MSM5218, the output waveform may overflow due to an internal operation error.

Therefore, if the maximum amplitude level of the input wave form when the ADPCM data is analyzed by the MSM5218, is controlled to about 80% of the dynamic range or less (see Figure 10), the output waveform of the MSM 5205 will not overflow, causing no noise in the composite voice.

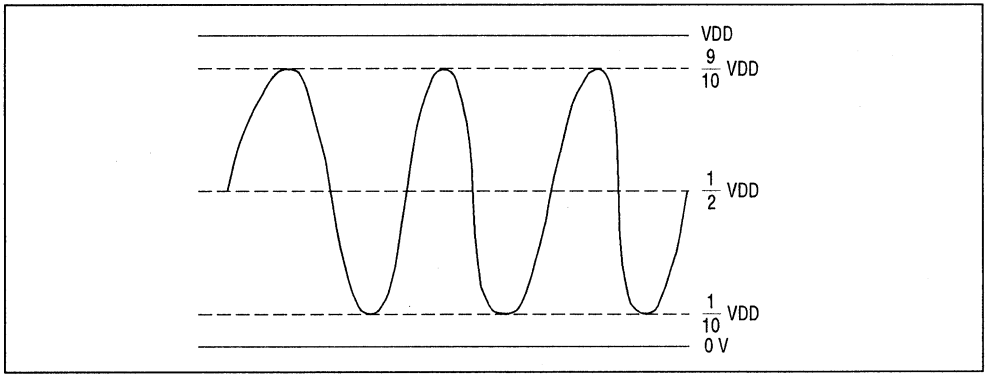


Figure 10 Waveform When the Maximum Amplitude Level of the Input Waveform is about 80% of the Dynamic Range

ANALYZER/SYNTHESIZER

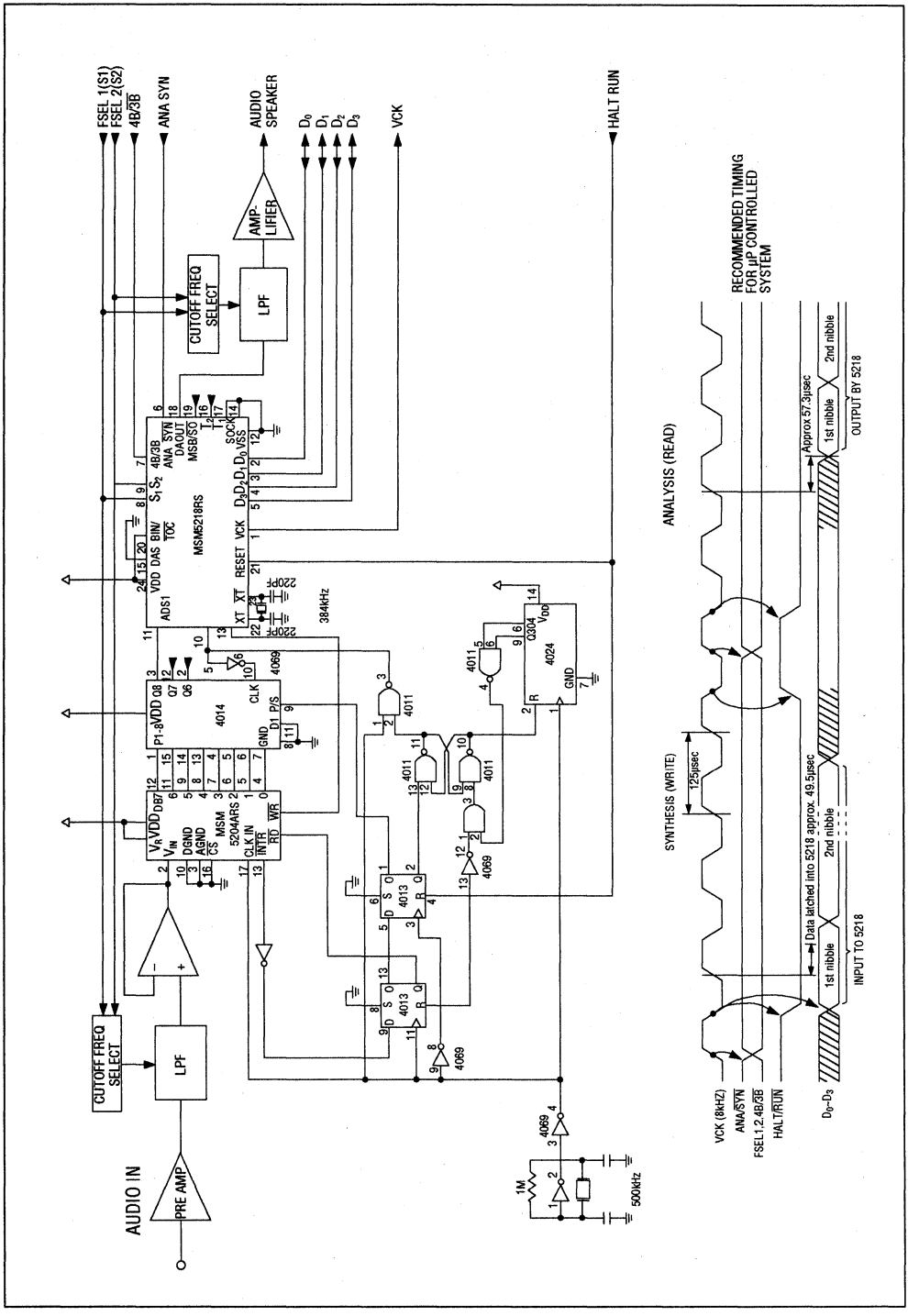


Figure 11 Typical Application Analyzer/Synthesizer

- **MSM5218 Voice Analysis/Synthesis Circuit Example(When MSM5204 is Used)**

An example of an application circuit for voice analysis and synthesis using MSM5218 and MSM5204 is shown in Figure 12. The time charts for these circuits are given in Figures 13 and 14.

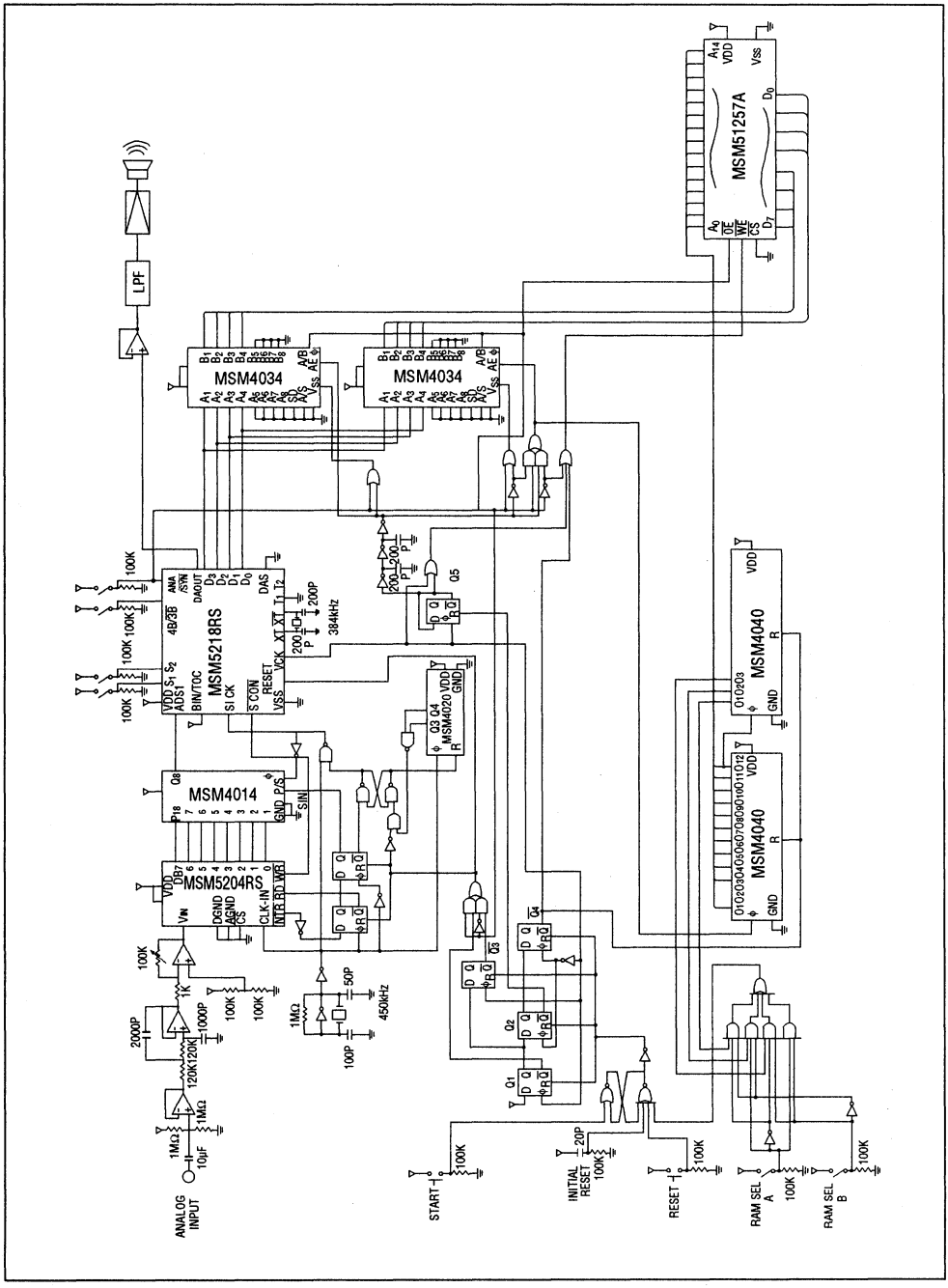


Figure 12 MSM5218

VOICE ANALYSIS TIMING CHART

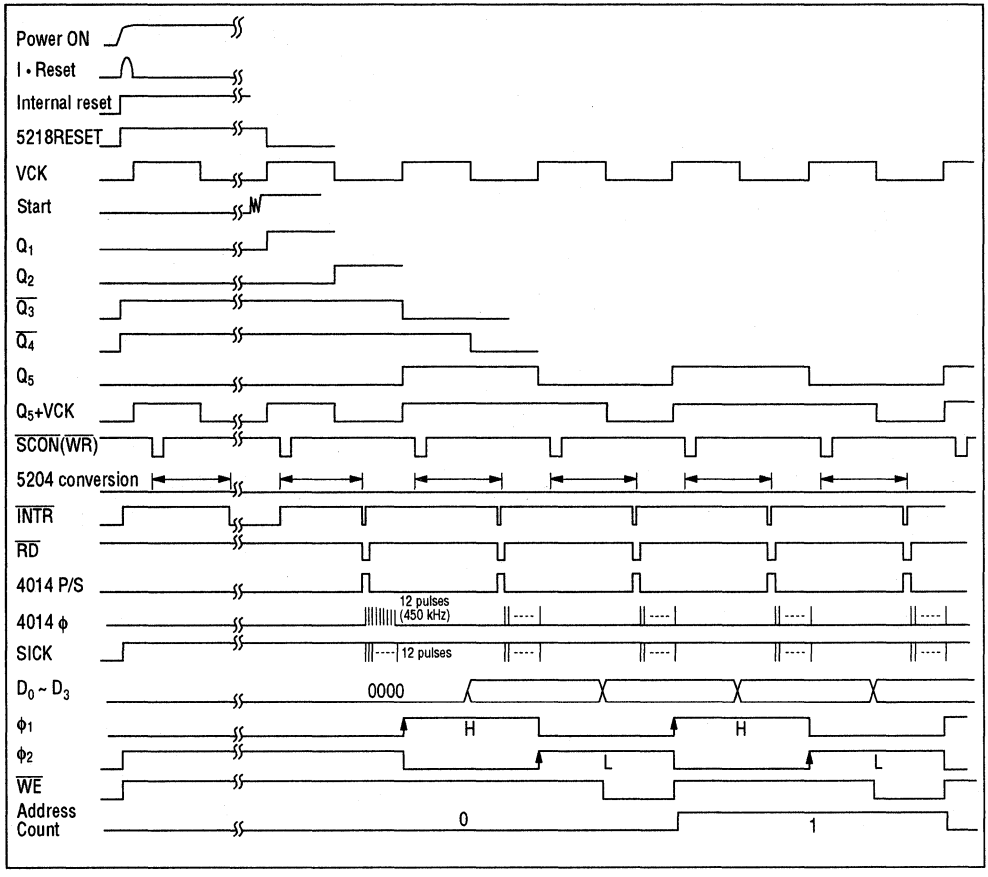


Figure 13

VOICE ANALYSIS TIMING CHART

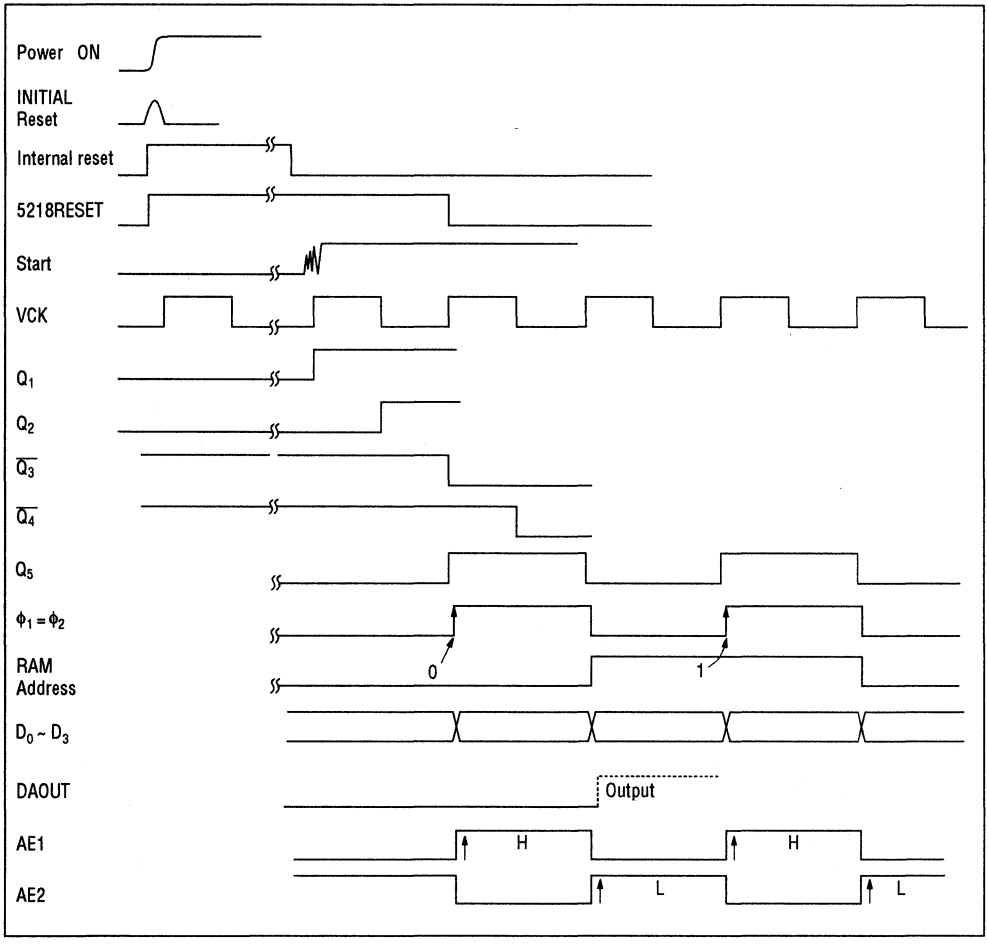


Figure 14

- **MSM5218 Voice Analysis/Synthesis Circuit Example (When 12-bit AD Converter is Used)**

An example of an application circuit for voice analysis and synthesis using MSM5218 and a 12-bit AD converter (ADC-80AG is manufactured by *MN Co.) is shown in Figure 15.

The time charts for these circuits are given in Figures 14 and 16.

*Micro Network Corp.

VOICE SYNTHESIS CIRCUIT EXAMPLE

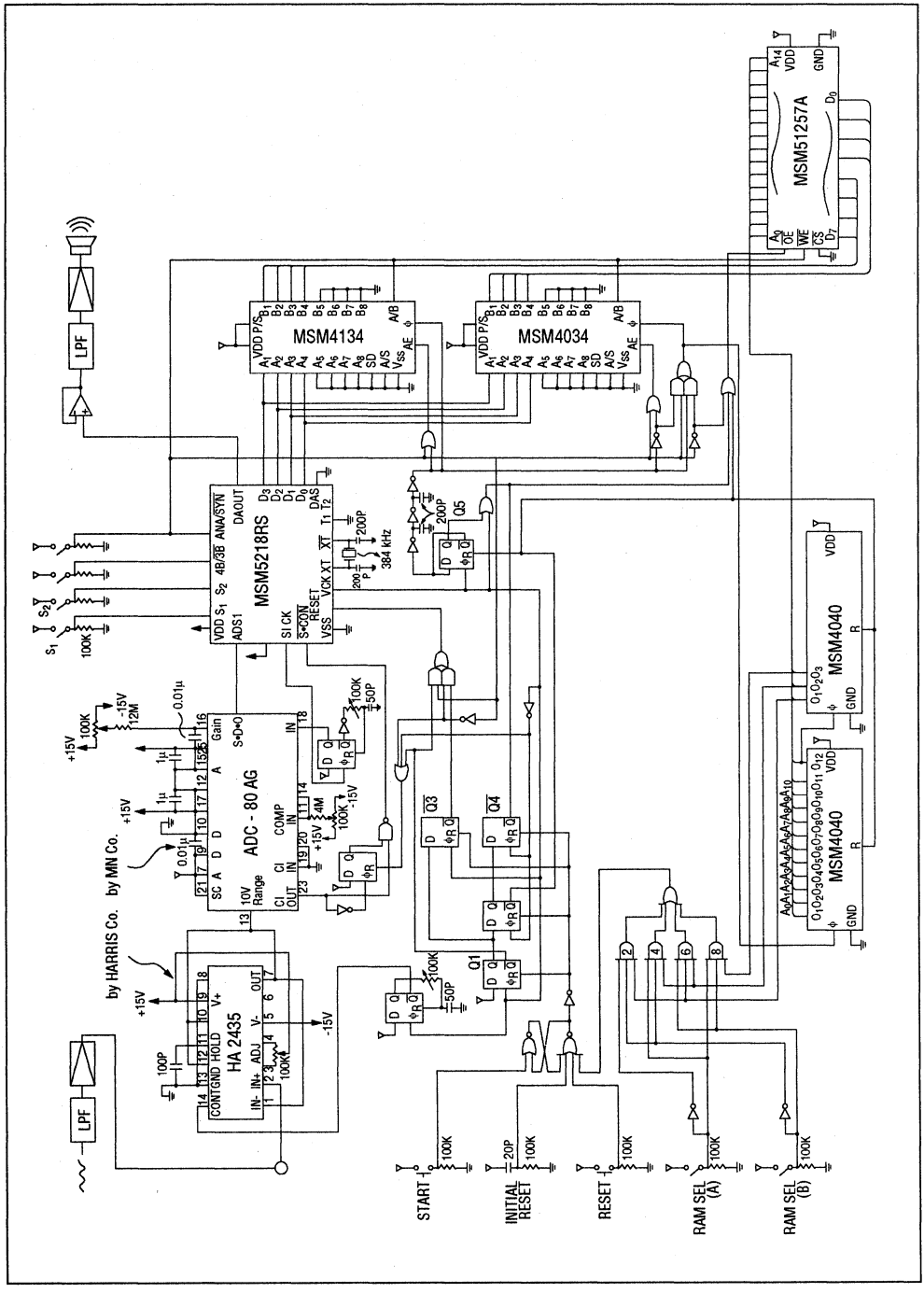


Figure 15

MSM5218 TIMING CHART

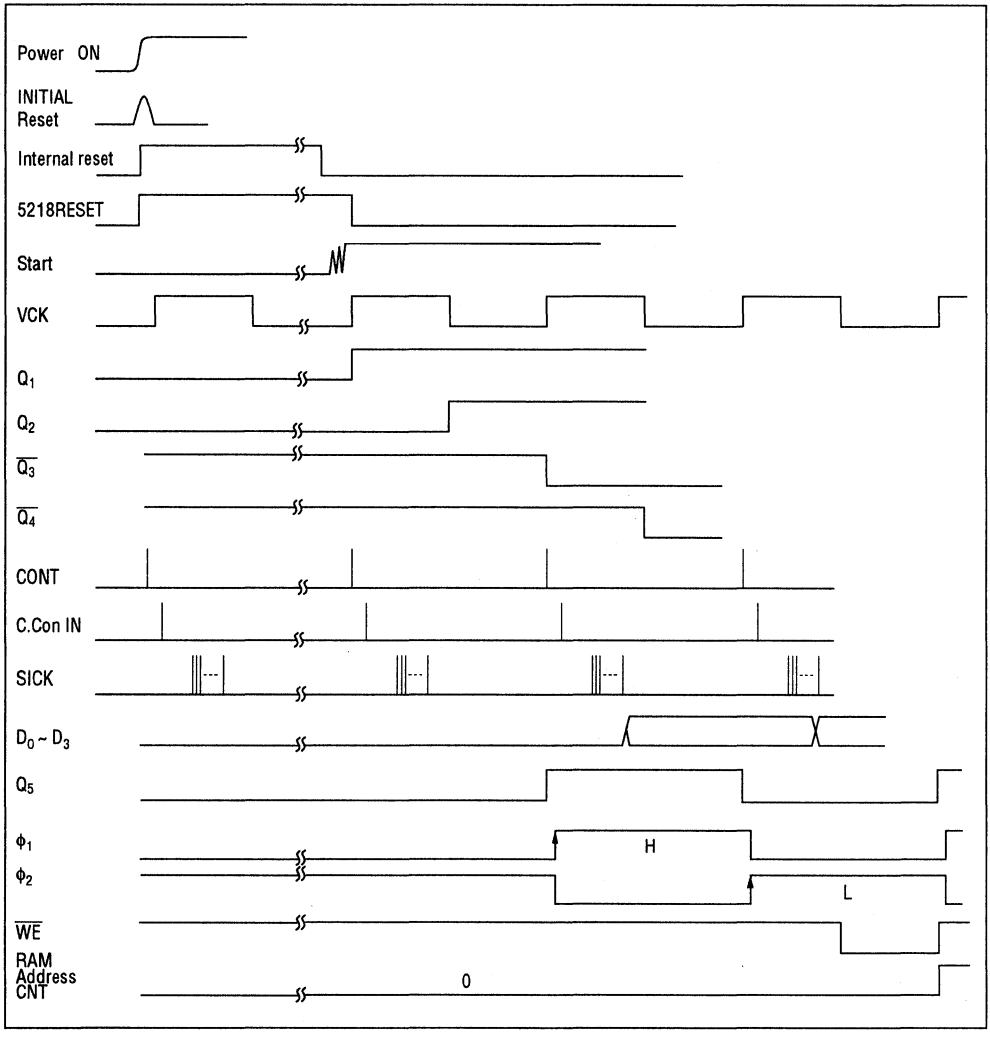
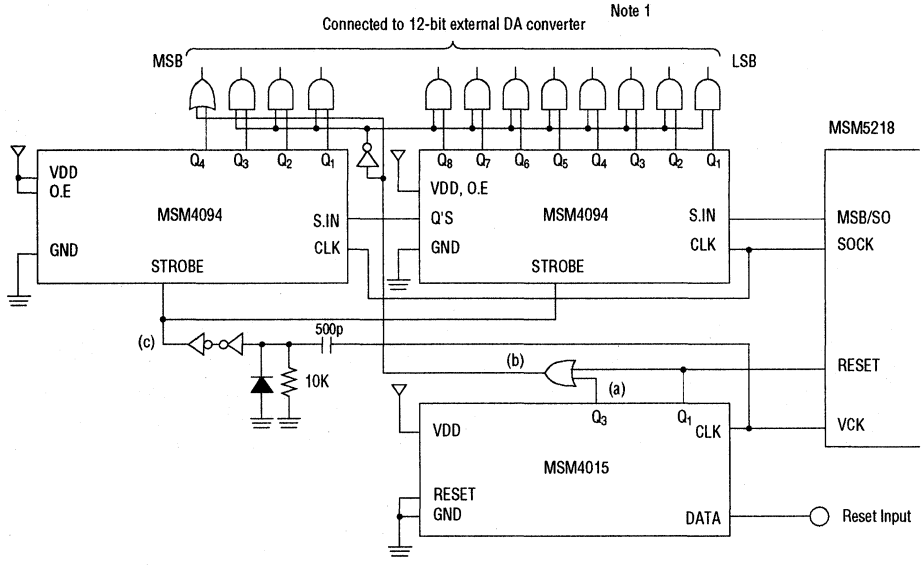


Figure 16

- **Example of Interface between MSM5218 and an External DA Converter**

An example of an interface circuit between MSM5218 and an external DA converter is shown in Figure 17.

The time chart for this circuit is given in Figure 18.



Note 1. The 12-bit output is in regular straight binary code.

Figure 17

MSM5218 TIMING CHART

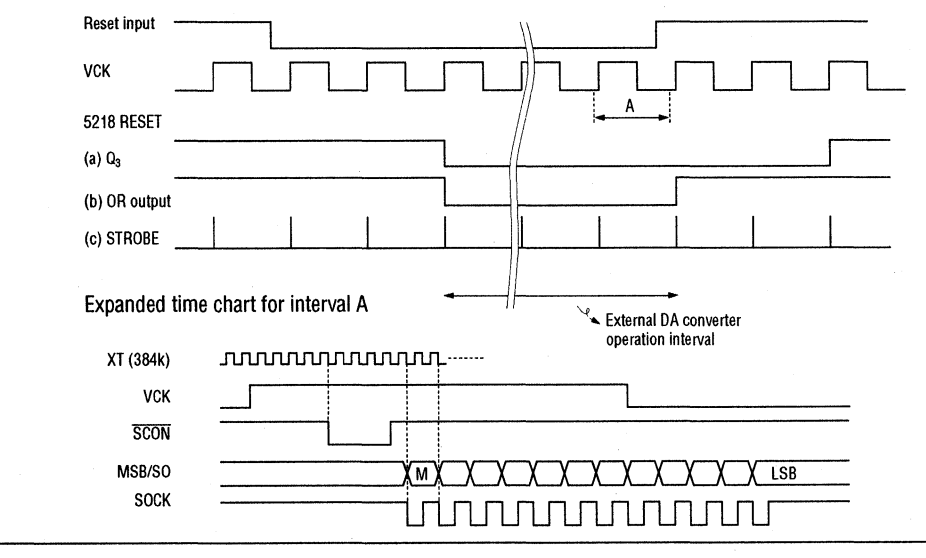


Figure 18

OKI Semiconductor

MSM6258/MSM6258V

ADPCM SPEECH PROCESSOR FOR SOLID STATE RECORDER

TO CUSTOMERS FOR NEW CIRCUIT DESIGN

For a new circuit design, it is recommended to use not the MSM6258, but the MSM6388/MSM6588 as described later.

The MSM6258 has an 8-bit AD converter and does not have a built in low pass filter. On the other hand, the MSM6388/MSM6588 has a 12-bit AD converter and includes a low pass filter. Therefore, the MSM6388/MSM6588 can realize a high quality voice.

In addition, the same control as a CPU interface of the MSM6258 can be performed by using the EPLAY/EREC command of the MSM6388 and the EXT command of the MSM6588.

GENERAL DESCRIPTION

The MSM6258 is a complex and highly integrated ADPCM speech processor, implemented in CMOS technology for low power consumption. The integrated A/D and D/A converters make the chip more self-contained, relieving the need for external conversion circuitry. The device comprises internally. A DRAM controller permitting the use of DRAMs alternatively to SRAMs and ROMs to store speech data. In other words, less periphery, thus less system vulnerability a voice detection circuit and phrase select provision are successfully added features for increased performance.

The ADPCM analysis and synthesis block is identical to the popular OKI MSM5218, that is, the bit overflow protection is included in for improved reproduction quality. The device is offered in two basic versions one of which comes in two package types. One is the version designed to be interfaced with an 8-bit CPU like the OKI MSM80C85 or MSM80C51 microcontroller, and comes in a 40-pin flat package; the other operates as a stand-alone solution that includes 19-pin programmable output lines for memory addressing and chip select in a 60-pin flat package or in a 68-pin PLCC, respectively, to permit full surface mount implementation.

MSM6258 accepts 4 to 8MHz master clocks, out of which two sets of sampling frequencies can be derived. Additionally, the ADPCM bit number is pin-selectable between 3 or 4 bits per sample. When using 256k or 1Mb DRAMs, the maximum I/O time is approximately 17 minutes at a bit-rate of 16kbps, while 256k SRAMs offer a little more than a minute of speech, both in their maximum memory configurations. At the higher bit-rates, 21.2 and 32 kbps, the I/O times are reduced proportionally.

In the case of DRAMs, the OKI MSC2304 (2-Megabit, module) or MSC2305 (4-Megabit module) are recommendable for space and cost saving benefits and in the interest of simplified handling. In the external mode, the built-in 8-bit ADC is looped so that a separate ADC can be connected to MSM6258, the accuracy of which may be between 8 to 12-bit for 'recording' speech. When the playback mode is set, the internal 10-bit DAC will be disabled to permit the connection of an external DAC of 10 to 12-bit of resolution.

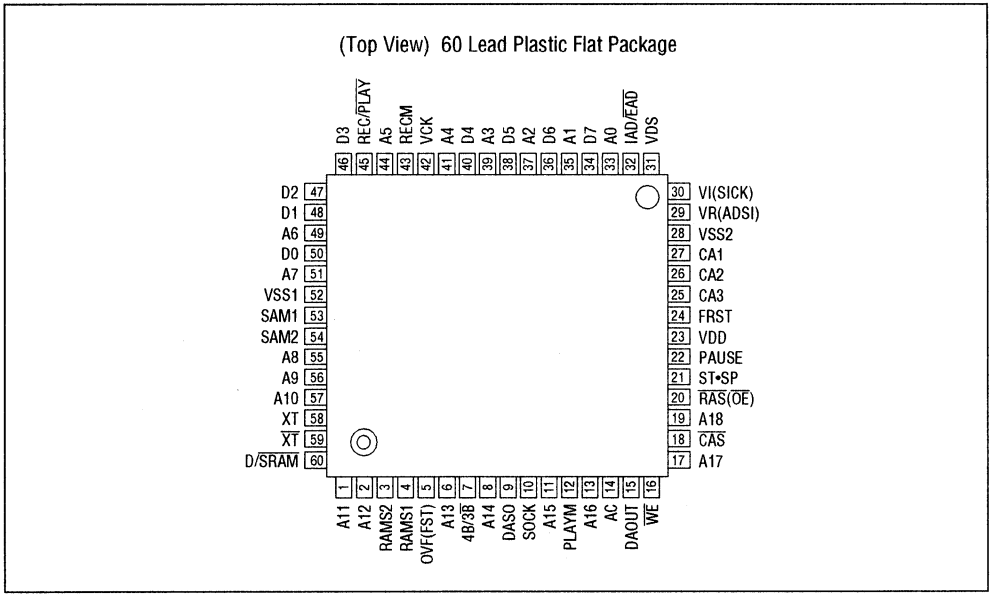
FEATURES

1. STAND-ALONE VERSION
   - Switch or microcomputer interface is possible
   - Straight ADPCM (3-bit/4-bit)
   - Built-in voice detection circuit
   - Built-in DRAM refresh circuit
   - SRAM/DRAM can be directly connected.
     Maximum 16 M-bit (with 256K or 1M DRAM used)
   - Sampling frequency selection
     3.9, 5.2, 7.8kHz (for original oscillation frequency of 4.0 MHz)
     4.0, 5.3, 8.0kHz (for original oscillation frequency of 4.096 MHz)
     7.8, 10.4, 15.6kHz (for original oscillation frequency of 8.0 MHz)
   - Maximum number for words recorded: 7-word
   - Original oscillation frequency: 4~8 MHz
   - Built-in AD converter: 8-bit
   - Built-in DA converter: 10-bit (voltage type of class A)
   - Operable with a single power supply
   - 60-pin plastic QFP (QFP60-P-1519-K)
     - 60-pin V plastic QFP (QFP60-P-1519-VK)
     - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950)

2. CPU INTERFACE VERSION
   - Command/status can be input and output through the data bus.
   - Straight ADPCM (3-bit/4-bit)
   - Sampling frequency selection
     3.9, 5.2, 7.8kHz (for original oscillation frequency of 4.0 MHz)
     4.0, 5.3, 8.0kHz (for original oscillation frequency of 4.096 MHz)
     7.8, 10.4, 15.6kHz (for original oscillation frequency of 8.0 MHz)
   - Maximum number for words recorded: 7-word
   - Original oscillation frequency: 4~8 MHz
   - Built-in AD converter: 8-bit
   - Built-in DA converter: 10-bit (voltage type of class A)
   - Operable with a single power supply
     - 40-pin plastic DIP (DIP40-P-600)
     - 44-pin plastic QFP (QFP44-P-910-K)
     - 44-pin-V plastic QFP (QFP44-P-910-V1K)
     - 44-pin plastic QFJ (PLCC) (QFJ44-P-S650)

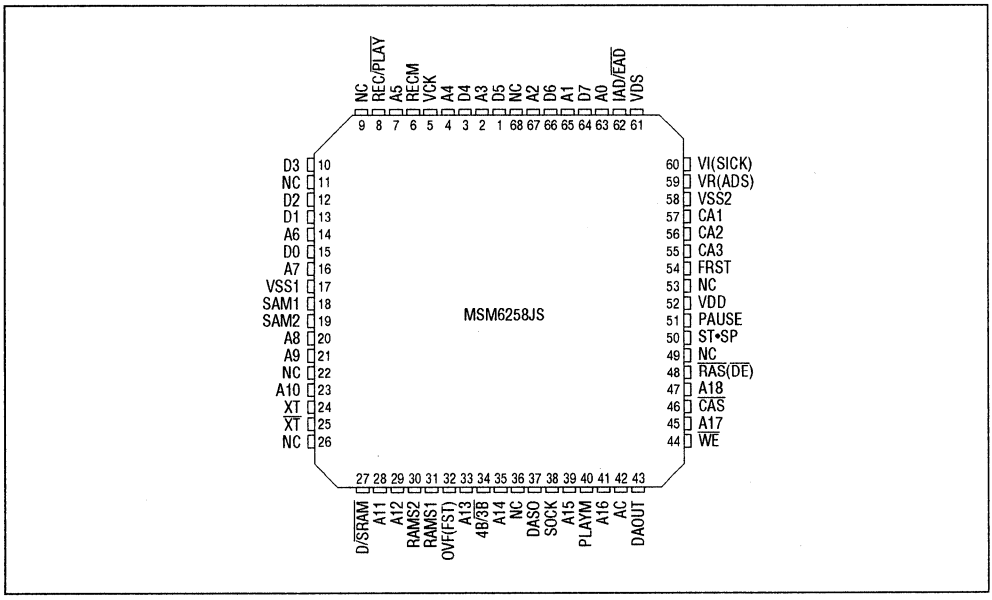
PIN CONFIGURATION

1. Stand-alone version



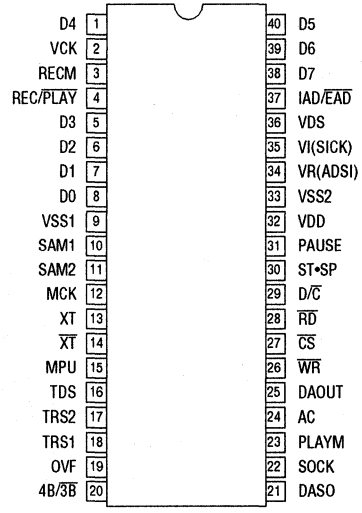
Note 1: Applicable to the MSM6258GS-K, GS-VK.

68-lead plastic leaded chip carrier



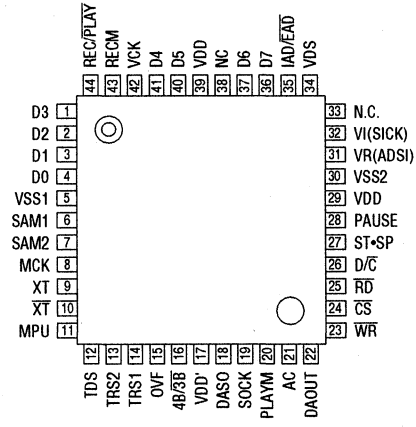
2. CPU interface verison

(Top View) 40 Lead Plastic DIP



Note 1: Applicable to the MSM6258VRS.

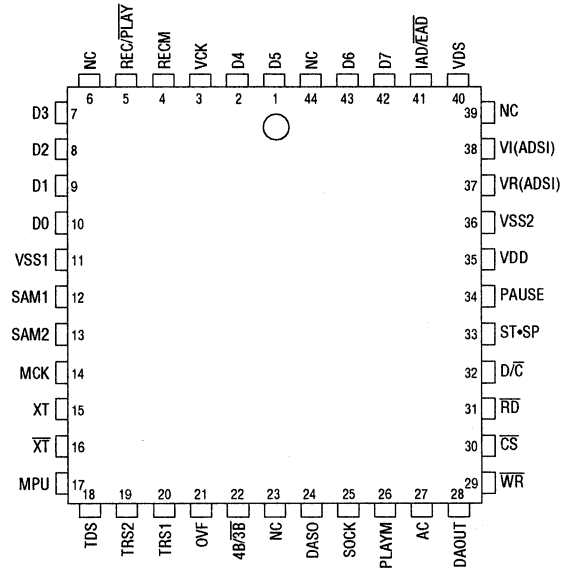
(Top View) 44 Lead Plastic Flat Package



Note 1: Applicable to the MSM6258VGS-K & GS-V1K
Note 2: VDD' connected to VDD Pin

MSM6258VJS

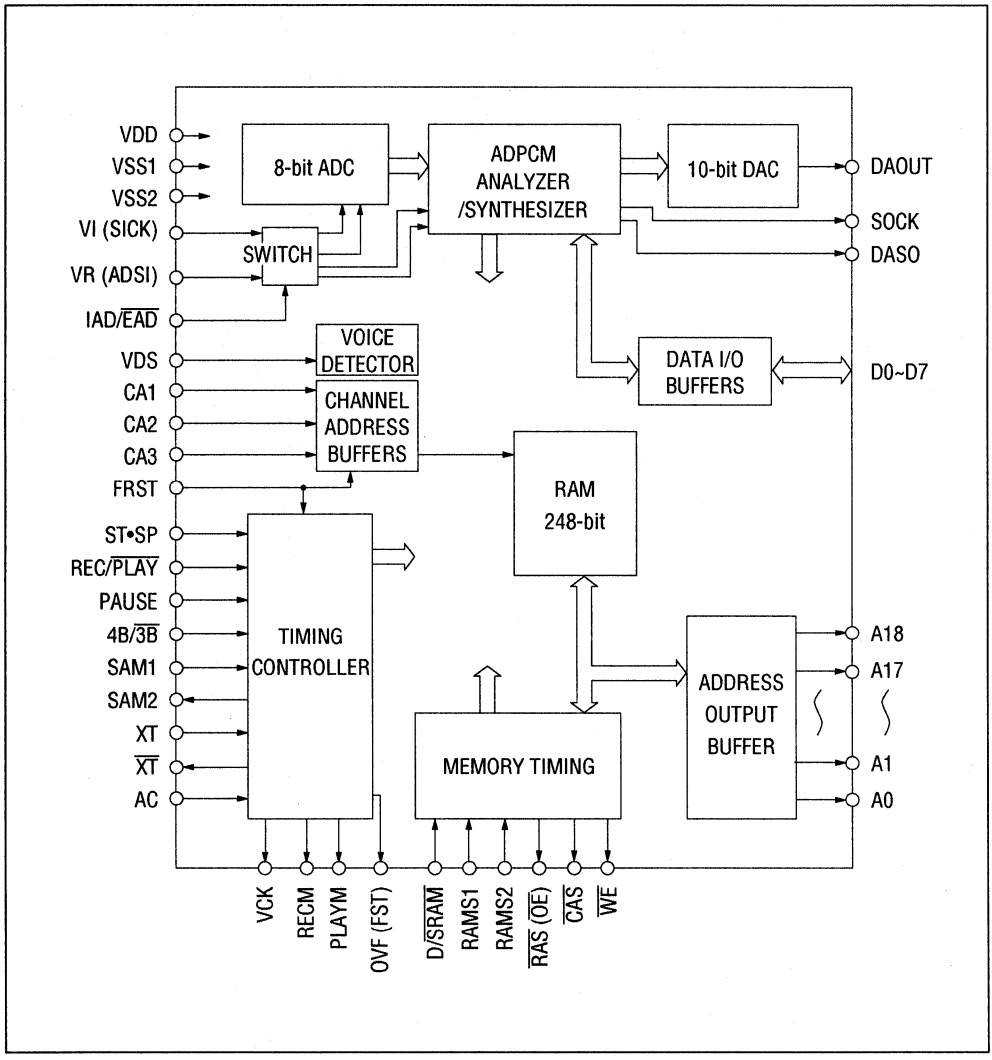
(Top View) 44-Pin Plastic Leaded Chip Carrier



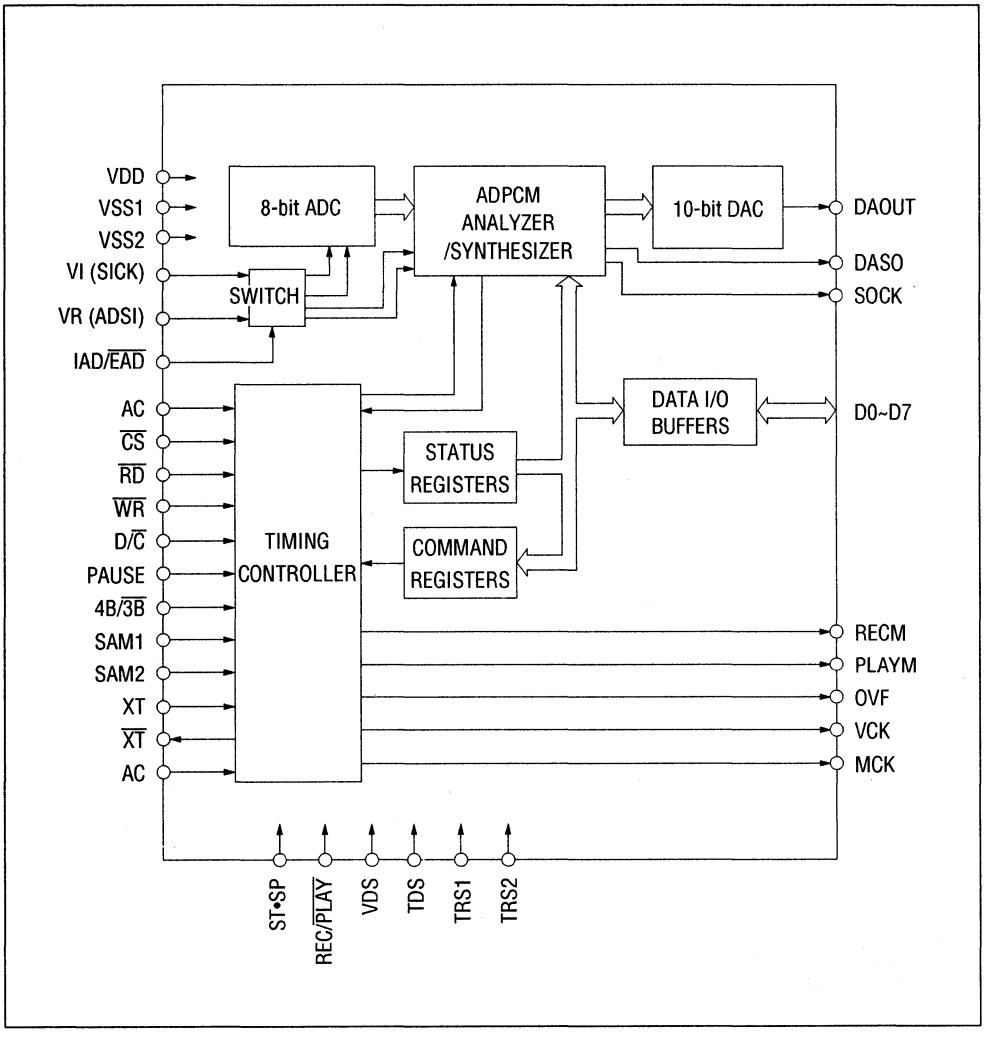
Note 1: Applicable to the MSM6258VJS.

FUNCTIONAL BLOCK DIAGRAM

1. Stand-alone version



2. CPU interface version



ABSOLUTE MAXIMUM RATINGS

STAND-ALONE & MPU interface version

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	T_a = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	–	−55 ~ +150	°C

Note: Permanent device damage may occur it ABSOLUTE MAXIMUM RATINGS are exceeded Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	V_{SS1} = V_{SS2} = 0V	+3 ~ +6.0	V
Ambient range	T_{OP}	–	−40 ~ +85	°C
Oscillation frequency	F_{OSC}	–	4.0 ~ 8.0	MHz

DC CHARACTERISTICS

(VDD = 5V/10%, Ta = –40 to +85°C) STAND–ALONE VERSION
(VDD = 5V/10%, Ta = –40 to +70°C) CPU I/F VERSION

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current	I_{DD}	F_{OSC} = 4.0MHz	–	–	4	mA
Stand by current	I_{DS}	With SRAM, AC=H	–	–	10	µA
H input voltage	V_{IH1}	–	3.6	–	–	V
H input voltage (Note 1)	V_{IH2}	–	0.8 × VDD	–	–	V
L input voltage	V_{IL}	–	–	–	0.8	V
H output voltage	V_{OH}	IOH = –40µA	4.2	–	–	V
L output voltage	V_{OL}	IOL = 2mA	–	–	0.45	V
H input current	I_{IH1}	Without pull down VIH=VDD	–	–	10	µA
H input current (Note 2)	I_{IH2}	With pull down VIL=0V	20	–	400	µA
L input current	I_{IL}	V_{IL}=V_{SS}	–10	–	10	µA
Output leakage current	I_{LO}	0V < VO < VDD	–10	–	10	µA
DA–output relative error	$\|V_{DAE}\|$	No-load	–	–	40	mV
AD conversion precision	$\|V_{ADE}\|$	VSS1=VSS2=0V VR=VDD	–	–	40	mV
DA output impedance	R_{DA}	–	12	17	22	kΩ
VR input impedance	R_{VR}	–	–	35	–	kΩ
VR input voltage	V_{VR}	–	0.9 × VDD	–	VDD	V
VI input voltage	V_{VI}	–	0	–	V_{VR}	V
VI input impedance	R_{VI}	–	10	–	–	kΩ

- S/N = (n-1) × 6
  n = ADC bit number

Note 1: Applies to XT
Note 2: Applies to ST•SP and PAUSE and MPU, FRST, VDS (only CPU I/F version)

AC CHARACTERISTICS

1. Stand-Alone Version

VDD = 4.5 - 5.5V, Ta = –40 - 85°C
fosc = 4.096 MHz, fs= 8.0 kHz

Item		Symbol	Min.	Typ.	Max.	Unit
AC pulse width		t_{ACP}	2.0	–	–	µs
PAUSE pulse width		t_{PAP}	2.0	–	–	µs
FRST pulse width		t_{FRP}	2.0	–	–	µs
ST•SP pulse width (1) (STOP pulse width when D SRAM ="L", and REC/$\overline{PLAY}$="H") (Note 2)		t_{SPP}	66	–	–	ms
ST•SP pulse width(2) (STOP pulse width excepting (1) above)		t_{STP}	2.0	–	–	µs
Time from entry of start pulse to rise of RECM when DRAM is selected (Note 1)		t_{DRR}	–	16.3	–	ms
Time from starting of oscillation to rise of RECM when SRAM is selected		t_{SRR}	56.2	–	70	ms
Time from starting of oscillation to initial change of DAOUT when SRAM is selected (Note 1)		t_{XDS}	–	40	–	ms
Time from entry of STOP pulse to fall of RECM (Note 1)		t_{SRF}	0	–	66	ms
Time for DAOUT to change from GND to 1/2 VDD (Note 1)		t_{DAR}	–	16	–	ms
Time from entry of STOP pulse to change of DAOUT to GND (Note 1)	REC/$\overline{PLAY}$ "H"	t_{DAL}	0	50	100	ms
	REC/$\overline{PLAY}$ "L"	t_{DAF}	0	16	32	ms
Time from setting of PLAYM to "L" to entry of restart pulse (Note 1)		t_{PRS}	52	–	–	ms
Time from entry of START pulse to rise of PLAYM (Note 1)		t_{SPR}	0	–	4	µs
Time from entry of STOP pulse to fall of PLAYM (Note 1)		t_{SPF}	0	–	4	µs
Time from setting of REC/$\overline{PLAY}$, CA1 - CA3 to entry of START pulse		t_{STC}	2	–	–	µs
Time from completion of entry of STOP pulse to change of REC/$\overline{PLAY}$, CA1 - CA3		t_{SPC}	2	–	–	µs

(Note 1) Proportionate to fosc (Raising fosc shortens the time.)

(Note 2) Proportionate to fs (Raising fs shortens the time.)

2. CPU Interface Version

VDD = 4.5 - 5.5V, Ta = –40 - 85°C
fosc = 4.096 MHz, fs = 8.0 kHz

Item		Symbol	Min.	Typ.	Max.	Unit
Time during which the level of VCK remains "H"	(Note 1)	t_{VH}	–	62.5	–	µs
Time during which the level of VCK remains "L"	(Note 1)	t_{VL}	–	62.5	–	µs
Time during which the level of MCK remains "H"	(Note 2)	t_{MH}	–	39.1	–	µs
Time during which the level of MCK remains "L"	(Note 3)	t_{ML}	–	210.9	–	µs
Time from rise of VCK to rise of MCK	(Note 2)	t_{VM}	–	19.5	–	µs
Setup time for fall of MCK during ADPCM data reading	(Note 2)	t_{RMS}	15	–	–	µs
Hold time for fall of MCK during ADPCM data reading	(Note 2)	t_{RMH}	55	–	–	µs
Setup time for fall of MCK during ADPCM data writing	(Note 2)	t_{WMS}	70	–	–	µs
Hold time for fall of MCK during ADPCM data writing	(Note 2)	t_{WMH}	2	–	–	µs
$\overline{RD}$ pulse width		t_{RR}	250	–	–	ns
D/$\overline{C}$ setup time for fall of $\overline{RD}$		t_{DCR}	50	–	–	ns
D/$\overline{C}$ hold time for rise of $\overline{RD}$		t_{RDC}	100	–	–	ns
$\overline{CS}$ setup hold time for $\overline{RD}$		t_{CR}	0	–	–	ns
Data establishment time from fall of $\overline{RD}$		t_{DRE}	–	–	200	ns
Data float time from rise of $\overline{RD}$		t_{DRF}	10	–	200	ns
$\overline{WR}$ pulse width		t_{WW}	250	–	–	ns
D/$\overline{C}$ setup time for fall of $\overline{WR}$		t_{DCW}	50	–	–	ns
D/$\overline{C}$ hold time for rise of $\overline{WR}$		t_{WDC}	100	–	–	ns
$\overline{CS}$ setup hold time for $\overline{WR}$		t_{CW}	0	–	–	ns
Data setup time for rise of $\overline{WR}$		t_{DWS}	100	–	–	ns
Data hold time for rise of $\overline{WR}$		t_{DWH}	30	–	–	ns
Time from fall of AC to entry of start command	(Note 2)	t_{AS}	16.0	–	–	ms
Setup time for entry of start command in rise of VCK	(Note 2)	t_{WVS}	4	–	120	µs
Hold time for entry of stop command in rise of VCK	(Note 2)	t_{WVP}	4	–	120	µs

Item	Symbol	Min.	Typ.	Max.	Unit
Time from fall of VCK to rise of RECK	t_{VRR}	0.0	–	2.0	µs
Time from fall of VCK to fall of RECM	t_{VRF}	0.0	–	2.0	µs
Time from fall of AC to time when DAOUT is set to 1/2 VDD (Note 2)	t_{DAR}	–	15.6	–	ms
Time from entry of start command to rise of PLAYM	t_{WPR}	0.0	–	4.0	µs
Time from entry of stop command to fall of PLAYM (Note 2)	t_{WPF}	0.0	–	2.0	µs
Time from entry of stop command to entry of start command (Note 1)	t_{SPT}	260	–	–	µs
Duty cycle for input of original oscillation clock to XT	f_{DUTY}	40	50	60	%

(Note 1) Proportionate to fs (Raising fs extends the time.)

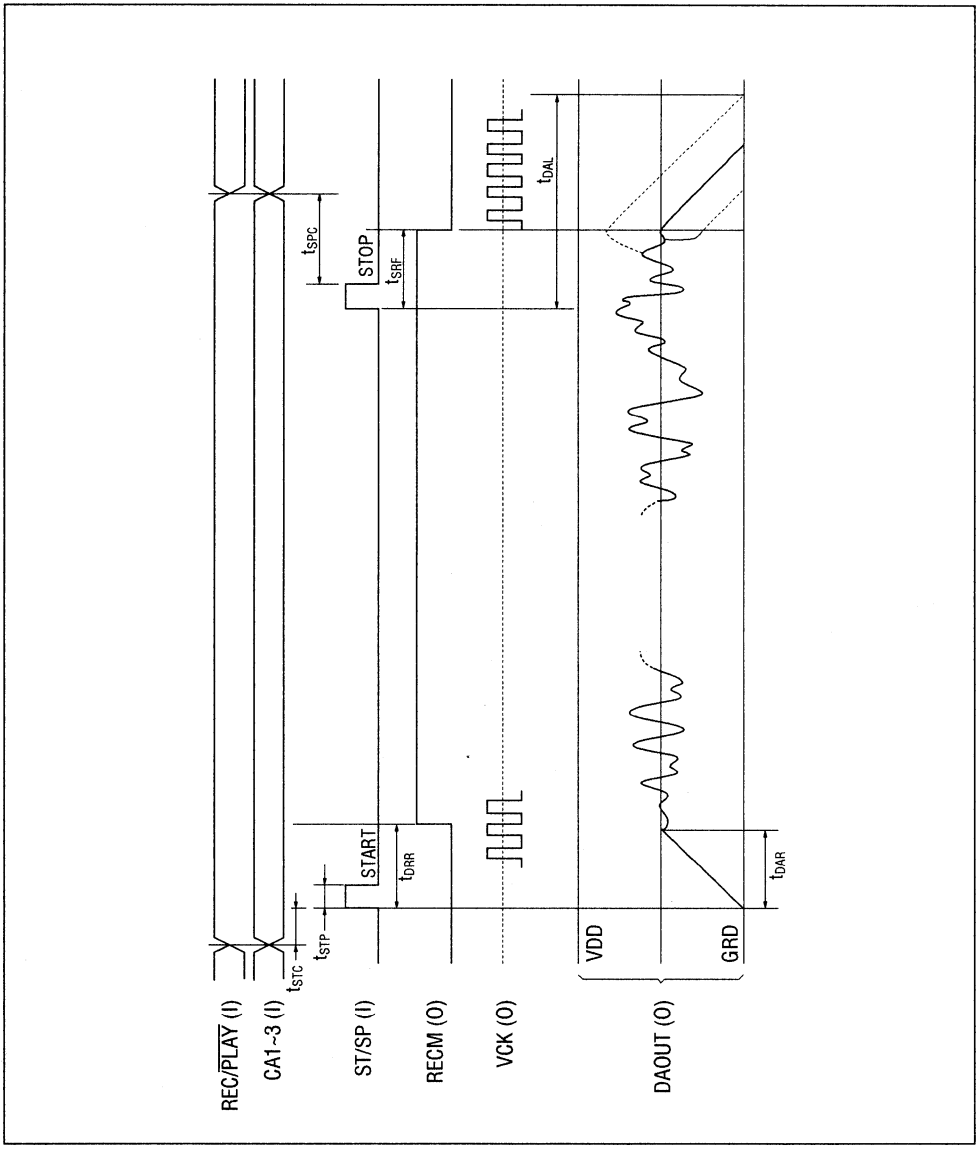
(Note 2) Proportionate to fosc (Raising fosc shortens the time.)

(Note 3) Equivalent to two times the sampling period minus t_{MH}

TIMING CHART

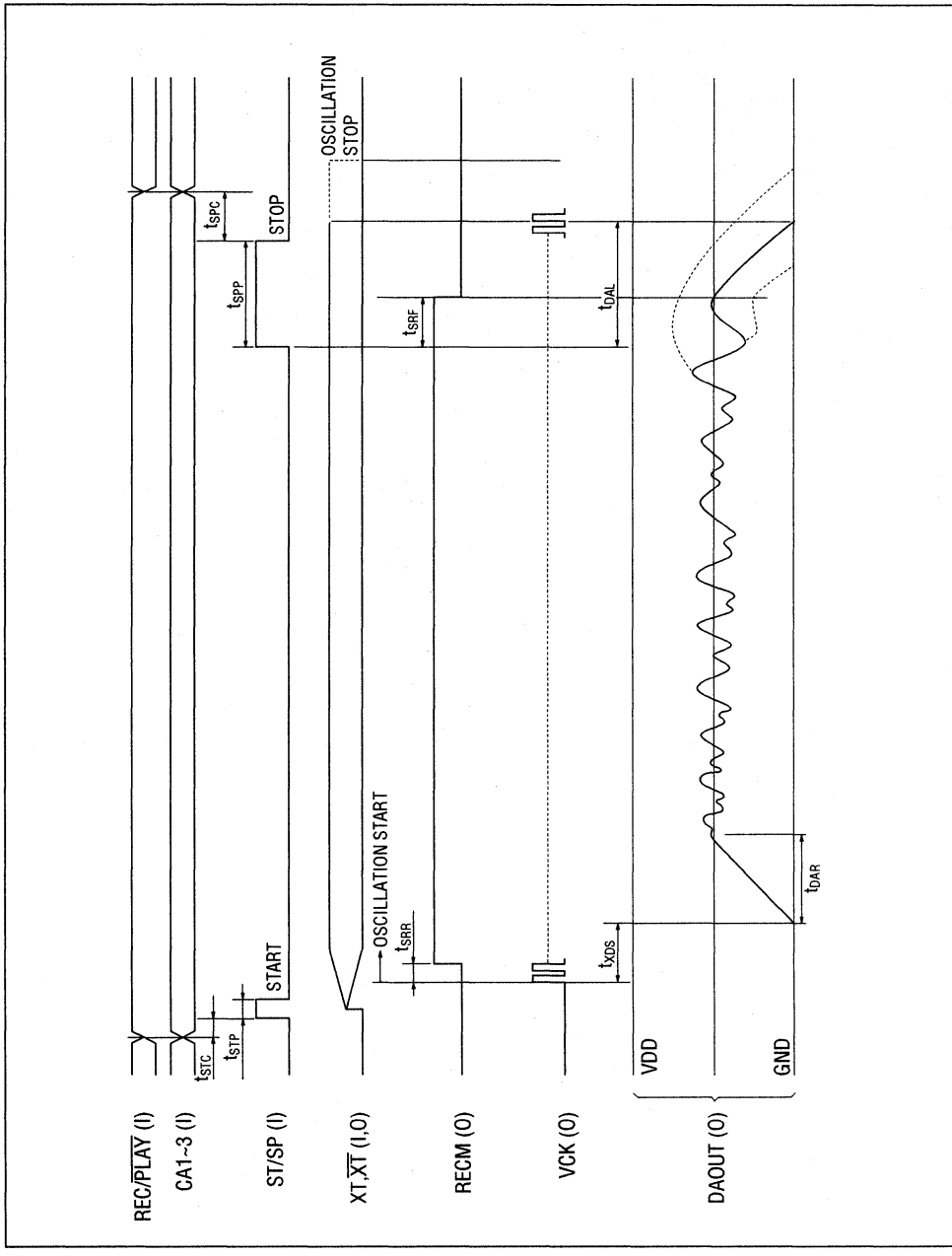
1. Stand-Alone Version

- **RECORD TIMING** (with DRAM selected, VDS = "L")



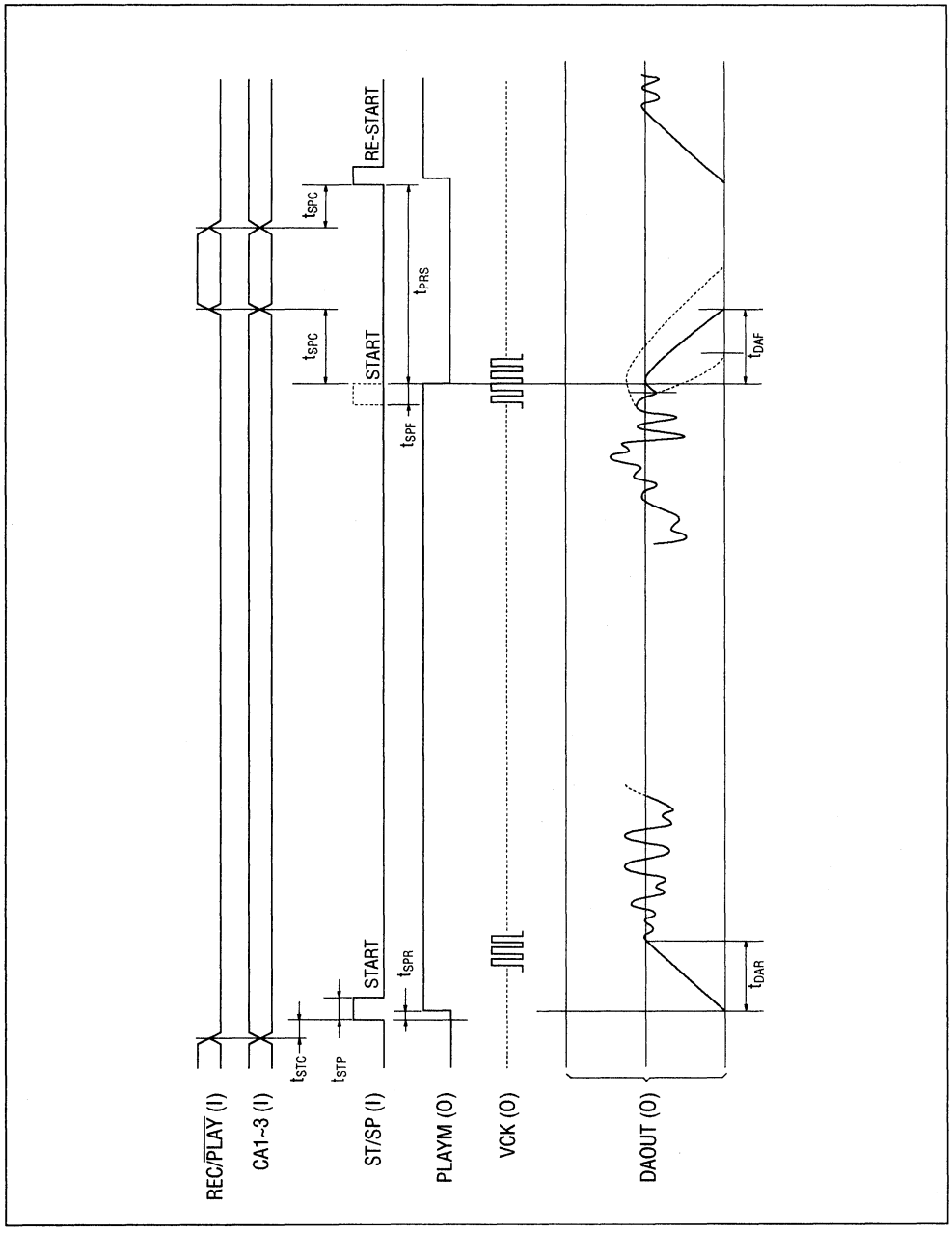
Note If VDS = "H", RECM outputs 2 Hz clock during detection of voice.

- **RECORD TIMING** (with SRAM selected, VDS = "L")



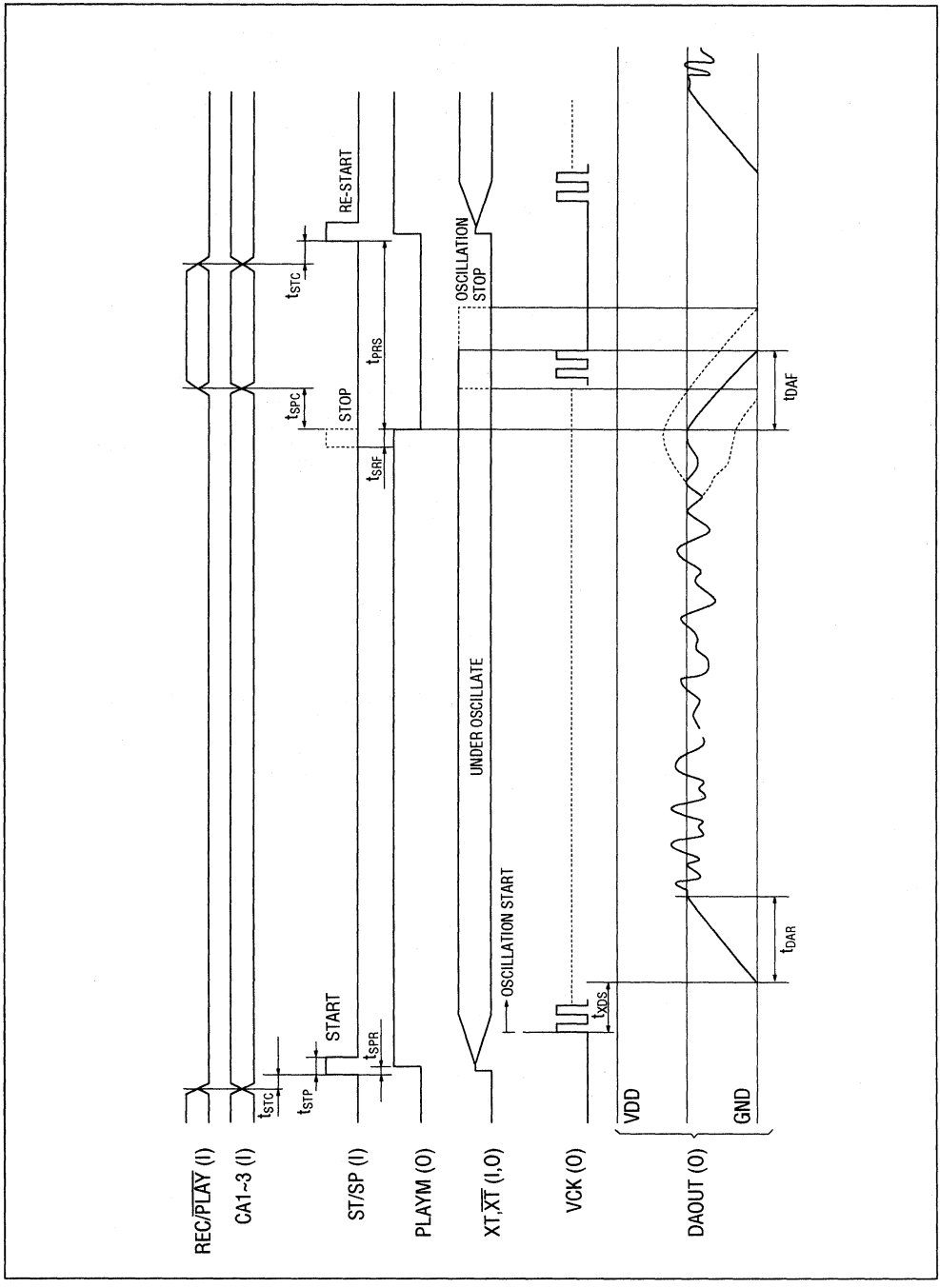
Note If VDS = "H", RECM outputs 2 Hz clock during detection of voice.

- **PLAYBACK TIMING** (with DRAM selected)



Note t_{DAF} = 16 msec when DAOUT signal level is 1/2 VDD,
t_{DAF} = 32 msec when DAOUT signal level is VDD.

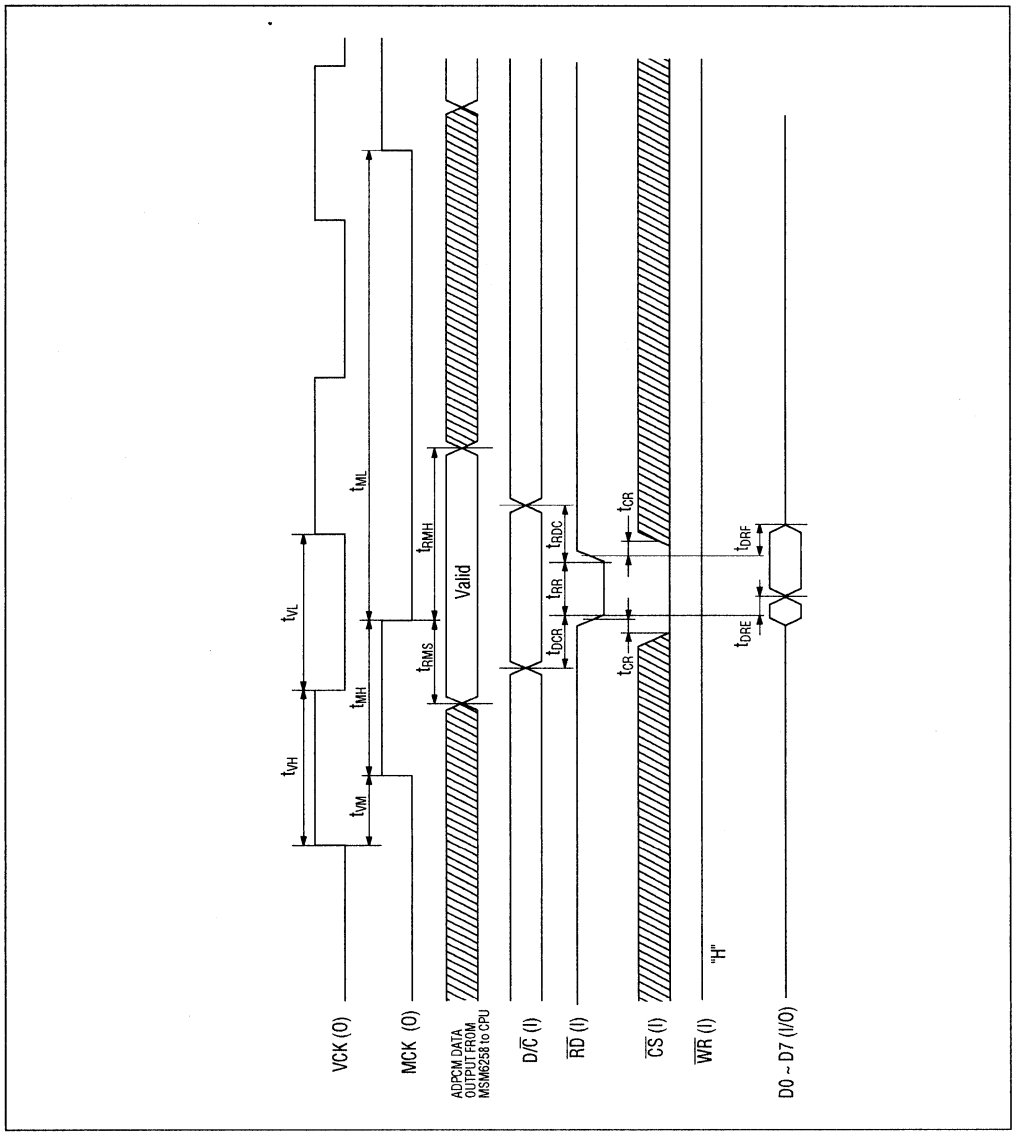
- **PLAYBACK TIMING** (with SRAM selected)



2. CPU INTERFACE VERSION

- **READ TIMING** (with record or status output)

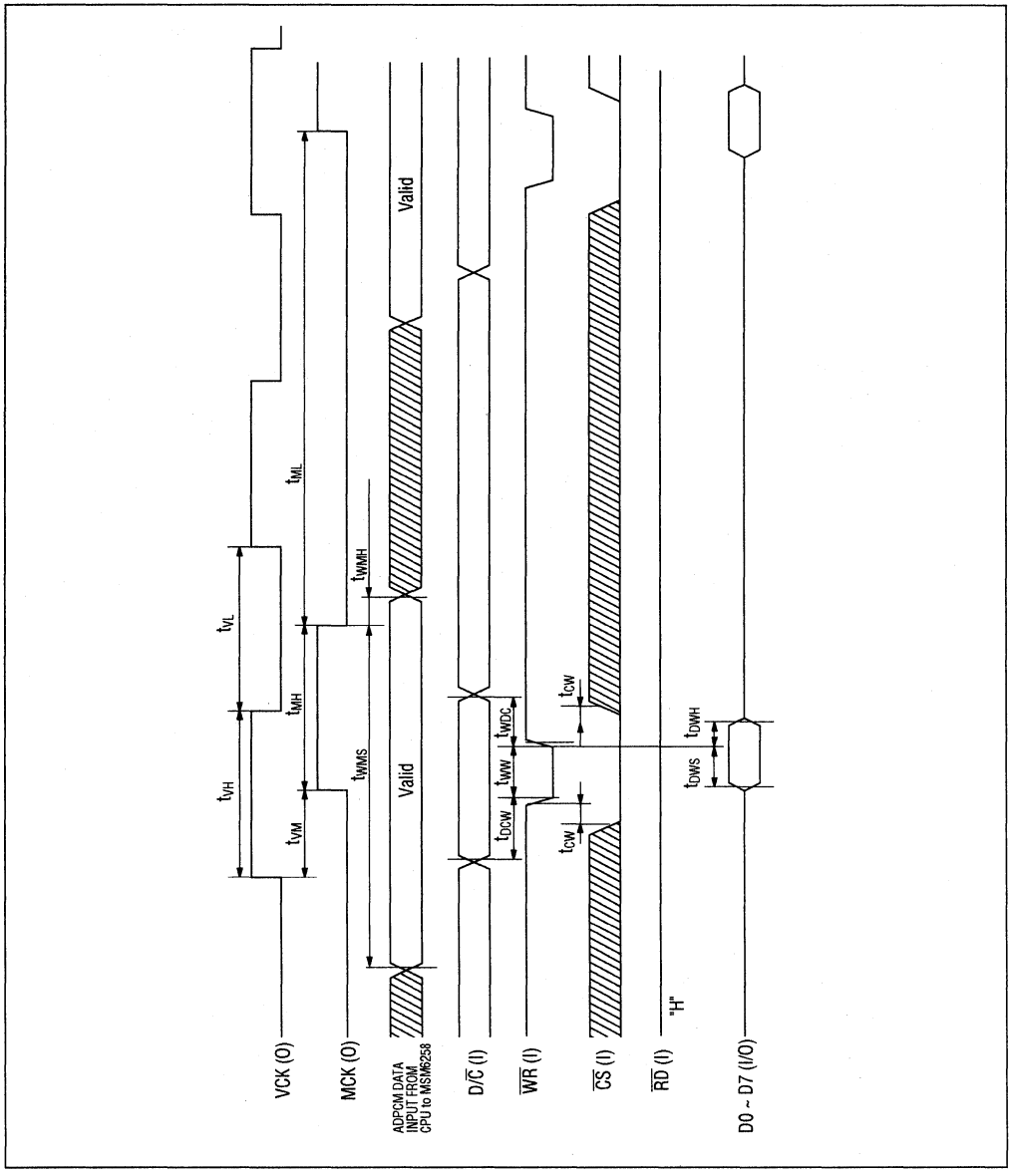
• **READ TIMING** (with record or status output)



Note Use the above valid section to reference ADPCM data output from the MSM6258 to CPU. Status reading may be performed anywhere.

- **WRITE TIMING** (with playback or command input)

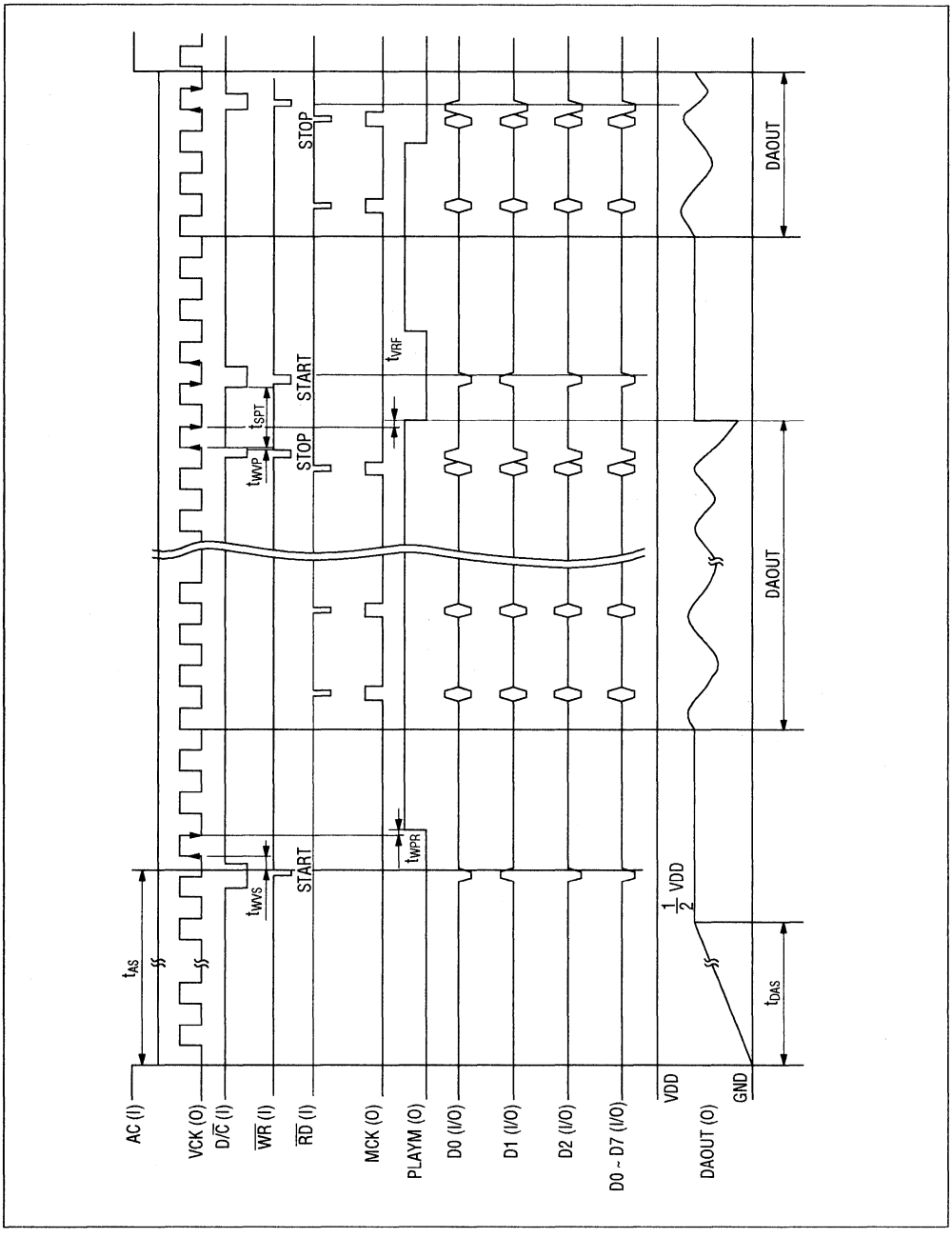
• **WRITE TIMING** (with playback or command input)



Note Use the above valid section to reference ADPCM data input from CPU to the MSM6258. Command write may be performed anywhere.

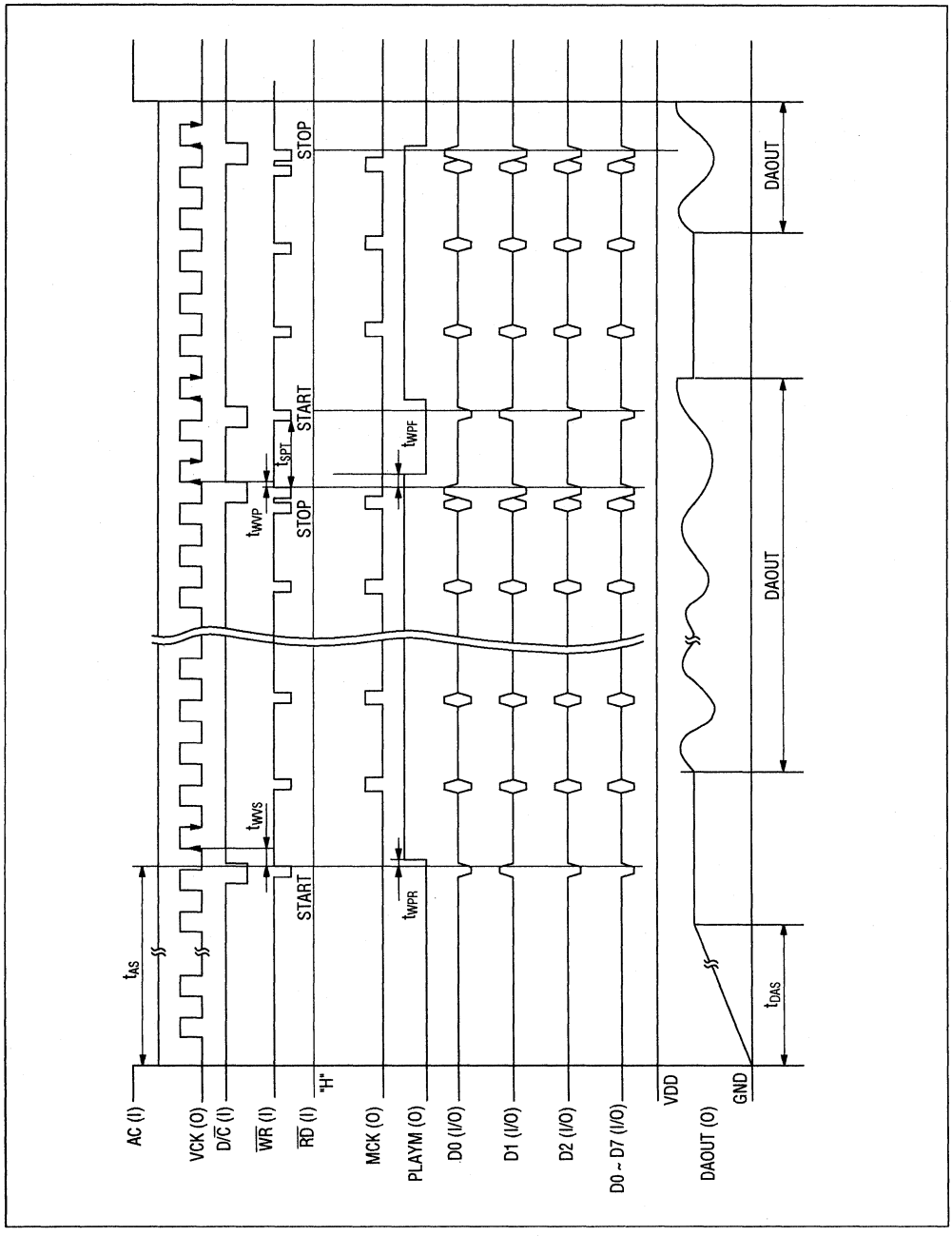
- **RECORD TIMING**

• RECORD TIMING



- **PLAYBACK TIMING**

• PLAYBACK TIMING



DESCRIPTION OF TERMINALS

1. Stand-Alone Version

Pin Name	I/O	Function
VDD	–	Power supply pin
VSS1	–	Digital GND pin
VSS2	–	Analog GND pin
AC (All Clear)	I	If the level of this pin is set to "H", the internal circuitry is set to the initial state. So, the output level of DAOUT is set to GND, the flag for each channel is reset to inhibit reproduction in channel 1 through channel 7 ; and oscillation is stopped if SRAM has been selected. The built-in power-on resetting circuit causes the level of this pin to go "H". For assurance, it is recommended to connect an external power-on resetting circuit.
REC/$\overline{\text{PLAY}}$	I	Selects recording or playing. If the level of this pin is set to "H", record mode is invoked. Do not change the input level of this pin during recording or playing.
ST•SP	I	Enables entry of pulses to start and terminate recording or playing. It is internally pulled down. A chatter prevention circuit is provided.
PAUSE	I	When momentarily connected to VDD, the record or playback operation is temporarily suspended. It is internally pulled down.
PLAYM (PLAY MONITOR)	O	Its output level is set to "H" during vocalization in play mode. Its output level is set to "L" during standby and record mode.
RECM (REC MONITOR)	O	Outputs "L", "H", and "2 Hz clock output" depending on the state of the LSI. In play or standby mode, its output level is set to "L". During recording, the level of this pin is set to "H". It outputs 2 Hz clock during detection of voice, and during pause.
DAOUT	O	Voice output pin. Voice is output during recording and playing. For reference, a muting circuit, which inhibits the output of voice during recording, is given in Figure 34. In standby mode, its level is set to GND level to make the power consumption of the speaker driving transistor null. At this time, pop noise is eliminated internally.
CA1~CA3	I	Specifies channels for recorded phrases or phrases to be reproduced. Up to eight channels can be specified. Do not change the input level of this pin during recording or playing.
OVF(FST) Overflow (Flag Status)	O	Outputs the flag status ("H" level if the selected channel has already been used for recording) for the selected channel in standby mode. Outputs "H" level pulses if the voice signal exceeds approximately 80% of the dynamic range in record or play mode.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>FRST
(FLAG RESET)</td><td>I</td><td>Setting the level of this pin to "H" resets the flag for the selected channel to inhibit reproduction in that channel.
The signal from this pin is valid only in standby mode. Do not set the level to "H" during recording or playing. A pull down resistor is used.</td></tr>
<tr><td>VDS
(Voice Detect Select)</td><td>I</td><td>In record mode, when VDS="H", this input determines whether the silence preceding the voice input is silence or voice and if voice then recording is started. This is called a "Voice Triggered Starting Circuit".</td></tr>
<tr><td>SAM1
SAM2</td><td>I</td><td>Selects a sampling frequency.
If the original oscillation frequency is 4.096 MHz, a sampling frequency is selected as shown below:
<table>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>fs</td><td>4.0kHz</td><td>5.3kHz</td><td>8.0kHz</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>4B/$\overline{3B}$</td><td>I</td><td>Selects bit length for ADPCM. "H" stands for 4-bit, and "L" stands for 3-bit.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>This bi-directional data bus conveys the ADPCM-coded data to and from the memory. One byte consists of two nibbles in the 4-bit ADPCM data format. In the case of 3-bit data format, two nibbles are presented, but the LSB of each is always externally pulled-down. The MSB of every nibble indicates whether the input waveform is ascending (MSB=0) or descending (MSB=1). D0 to D7 output or input a pair of ADPCM nibbles during every sampling period, which is VCK.</td></tr>
<tr><td>D/$\overline{SRAM}$</td><td>I</td><td>Selects either DRAM or SRAM. Set the level to "H" if DRAM is to be used.</td></tr>
<tr><td>RAMS1
RAMS2
(RAM SIZE SELECT)</td><td>I</td><td>According to the type of memory connected, do the following settings:
<table>
<tr><th>D/$\overline{SRAM}$</th><th>RAMS1</th><th>RAMS2</th><th>Connectable memory</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>64K × 1-bit (64K DRAM)
64K × 4-bit (256K DRAM)</td></tr>
<tr><td></td><td>H</td><td>L</td><td>256K × 1-bit (256K DRAM)
256K × 4-bit (1M DRAM)</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1M × 1-bit (1M DRAM)</td></tr>
<tr><td></td><td>H</td><td>H</td><td>Inhibited.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>64K SRAM, 64K ROM</td></tr>
<tr><td></td><td>H</td><td>L</td><td>256K SRAM, 256K ROM</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>*SRAM, EPROM, Madk ROM</td></tr>
<tr><td></td><td>H</td><td>H</td><td>Internal RAM access mode</td></tr>
</table>
* Address pins A0 through A18 output binary data.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>A0 ~ A18</td><td>O</td><td>External memory address pins and chip select pins.
Depending on the type of memory, pins A0 through A18 are used as shown below. In standby mode, the address pins output "L" level signals, and the chip select terminals output "H" level signals.
<table>
<tr><th colspan="2">Type of memory</th><th>Maximum q'ty</th><th>Address pin(*2)</th><th>Chip select pin</th></tr>
<tr><td rowspan="3">DRAM</td><td>64K × 1-bit
64K × 4-bit</td><td>11 sets
(*1)</td><td>A0 ~ A7</td><td>A8 ~ A18</td></tr>
<tr><td>256K × 1-bit
256K × 4-bit</td><td>8 sets
(*1)</td><td>A0 ~ A8</td><td>A9 ~ A16</td></tr>
<tr><td>1M × 1-bit</td><td>2 sets
(*1)</td><td>A0 ~ A9</td><td>A10 ~ A11</td></tr>
<tr><td rowspan="2">SRAM</td><td>8K × 8-bit (64K)</td><td>6</td><td>A0 ~ A12</td><td>A13 ~ A18</td></tr>
<tr><td>32K × 8-bit (256K)</td><td>4</td><td>A0 ~ A14</td><td>A15 ~ A18</td></tr>
</table>
(*1) A set consists of six or eight DRAMs for one-bit data input/output. A set consists of two DRAMs for 4-bit data input/output.
(*2) If RAMS1 and RAMS2 are set to select binary output, A0 through A18 are all used as address pins.</td></tr>
<tr><td>VCK
(Voice Clock)</td><td>O</td><td>This pin outputs the selected sampling frequency.</td></tr>
<tr><td>XT
$\overline{XT}$</td><td>I
O</td><td>Oscillator connecting pin (4 MHz - 8 MHz)
If external clock signal is to be used, enter it through the XT pin with the $\overline{XT}$ pin open.</td></tr>
<tr><td>IAD/$\overline{EAD}$
(Internal AD/
Externla/AD)</td><td>I</td><td>Determines whether the built-in ADC is used or not. Entry of "H" level signal enables the use of the built-in ADC.</td></tr>
<tr><td>VI (SICK)</td><td>I</td><td>If the built-in ADC has been selected, this pin functions as V1 (analog signal input) pin. If the external ADC has been selected, it functions as SICK (serial clock input to read PCM data before AD conversion into LSI) pin.</td></tr>
<tr><td>VR (ADSI)</td><td>I</td><td>This pin functions as VR (AD converter reference voltage input terminal) pin if the built-in ADC has been selected. If the potential of VR is made equal to that of VDD, the input level for V1 and the output level for DAOUT become almost equivalent. If the external ADC has been selected, this pin functions as ADSI (serial input of PCM data after AD conversion) pin.</td></tr>
<tr><td>SOCK</td><td>O</td><td>Serial output clock. Used to output PCM data before DA conversion to the outside of LSI.</td></tr>
<tr><td>DASO</td><td>O</td><td>Output pin used to output serial PCM data before DA conversion to an external D/A.</td></tr>
</table>

Pin Name	I/O	Function
$\overline{RAS}$ ($\overline{OE}$)	O	DRAM and SRAM control timing output pin. It functions as RAS if DRAM is selected, and functions as OE if SRAM is selected. In standby mode, OE outputs "H" level signal.
$\overline{CAS}$	O	pin enabling the monitoring of CAS signal to DRAM. Do not directly connect this terminal to CAS pin on DRAM, but connect it to the chip select pins (A8 through A18).
$\overline{WE}$	O	This pin outputs timing signals used to control reading from and writing to DRAM and SRAM. It outputs "H" level signals in play or standby mode.

2. CPU Interface Version

Pin Name	I/O	Function
VDD	–	Power supply pin
VSS1	–	Digital GND pin
VSS2	–	Analog GND pin
MPU	I	If ther level of this pin is set to "H", LSI is switched to CPU interface. Since this input is internally pulled-down, be sure to apply a "H" level to this pin.
MCK (Main Clock)	O	Outputs signal for synchronization with CPU. During recording and playing, a frequency equivalent to 1/2 of the sampling frequency is output.
VCK (Voice Clock)	O	Outputs the selected sampling frequency. While the level of AC is set to "L", a sampling frequency is always output.
AC (All Cler)	I	Setting the level of this pin to "H" sets LSI to initial state, and sets the output level of DAOUT to GND. The built-in power-on resetting circuit sets AC to the "H" level temporarily when power is turned on. For assurance, however, it is recommended to connect an external power-on resetting circuit.
D0 ~ D7	I/O	These pins input and output ADPCM data, command data, and status data.
$\overline{CS}$ (Chip Select)	I	Setting the level of this pin to "L" enables data transfer with CPU. When setting the level of this pin to "H", data bus (D0 ~ D7) become high impedance, inhibiting reading and writing through the data bus.
$\overline{RD}$ (Read)	I	Setting this pin to the "L" level enables the CPU to read ADPCM data and status data from the MSM6258.
$\overline{WR}$ (Write)	I	Enables writing of ADPCM data and command data from the CPU to the MSM6258 at the rising edge of $\overline{WR}$.

Pin Name	I/O	Function
D/$\overline{C}$ (Data/Command)	I	Setting this pin to the "H" level sends ADPCM data through the data bus (D0 ~ D7). Setting it to the "L" level sends command data or status data through the data bus.
RECM (Record Monitor)	O	during recording, this pin outputs a "H" level signal.
PLAYM (Play Monitor)	O	During playback, this pin outputs a "H" level signal.
IAD/$\overline{EAD}$ (Internal AD/ External AD)	I	Makes a selection to use the build-in AD converter or an external AD converter. Setting the pin to the "H" level enables the use of the built-in AD converter.
VI (SICK) Voice in serial In Clock	I	Setting IAD/$\overline{EAD}$ to the "H" level causes this pin to function as analog signal input pin (VI). Setting IAD/$\overline{EAD}$ to the "L" level causes this pin to function as a serial input clock (SICK), which enables loading of PCM data after AD conversion into the LSI.
VR(ADSI) (Voltage Reference AD DATA Serial IN)	I	Setting IAD/$\overline{EAD}$ to the "H" level makes this pin function as AD converter reference voltage input pin (VR). If VR and VDD are made common, the input level of VI becomes equivalent to the output level of DAOUT. Setting IAD/$\overline{EAD}$ to the "L" level makes this pin function as input pin for serial PCM data subject to AD conversion.
DAOUT	O	Voice output pin. If outputs voice during recording and playing. For reference, an example of a muting circuit which inhibits voice output during recording is given in Figure 34. Setting AC to the "H" level sets the level of this terminal equivalent to the GND level. Changing AC from the "H" to "L" level gradually increases the level until it reaches 1/2 VDD.
SOCK (Serial Out Clock)	O	This pin outputs a clock used to output serial PCM data for external DA conversion.
DASO (DA Data Serial Out)	O	This pin outputs serial PCM data for external DA conversion.
4B/$\overline{3B}$ (4-bit/3-bit)	I	ADPCM bit length selection pin. Setting it to the "H" level makes the data bus (D0 ~ D7) send 4-bit ADPCM data. Setting the terminal to the "L" level makes the data bus send 3-bit ADPCM data.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SAM1
SAM2
(Sampling 1,2)</td><td>I</td><td>Sampling frequency selecting pin.
If the original oscillaiton frequency is 4.096 MHz, any of the following sampling frequencies can be selected:
<table>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>fs</td><td>4.0kHz</td><td>5.3kHz</td><td>8.0kKz</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>OVF (Overflow)</td><td>O</td><td>This pin outputs a "H" level signal if voice signal reaches more than 80% of the dynamic range during reocrding and playing. It outputs a "H" level signal in any mode other than record and play modes.</td></tr>
<tr><td>XT
$\overline{XT}$</td><td>I
O</td><td>Oscillator connecting pin.
If an external clock is to be used, enter it through the XT pin with the $\overline{XT}$ pin open.</td></tr>
<tr><td>VDS
ST•SP
REC/$\overline{PLAY}$
TDS
TRS 1
TRS 2
PAUSE</td><td>I</td><td>Set all these pins to the GND level.</td></tr>
</table>

DESCRIPTION OF FUNCTIONS

• Recording Time and RAM Capacity

Recording time varies with the capacity of external RAM, sampling frequency, and ADPCM bit length. Their relations are given by the following expression:

Recording time (sec.)

$$= \frac{1.024 \times \text{RAM capacity (K-bit)}}{\text{Sampling frequency (kHz)} \times \text{bit length (3 or 4)}}$$

If two 256K DRAMs are used with the sampling frequency set to 4 kHz, and with ADPCM bit length set to 4-bit, recording can be performed for 32.7 seconds as calculated below:

Recording time (sec.)

$$= \frac{1.024 \times 256 \text{ (K-bit)} \times 2}{4 \text{ (kHz)} \times 4 \text{ (bit)}} = 32.7 \text{ seconds}$$

• Analog Input

1. Waveform Input to VI

The analog input (voice waveform) to VI should be so designed to oscillate around 1/2VR. The maximum amplitude can equal VR.

As the input amplitude approaches VR, S/N during AD conversion is improved. Therefore, it is recommended to set the input amplitude in the range between 1/2VR and VR.

2. Conversion Method & Impedance of Analog Input to VI

MSM6258 employs an AD converter of the load comparison type, which uses a capacitor.

The VI terminal is connected to the internal capacitor for 8 μs each time the sampling frequency is given (125 μs for 8 kHz sampling), and disconnected from it for the rest of the time. So, input equivalent impedance varies with the frequency of the input waveform, ambient temperature, etc. by 10 k-ohms to more than several tens of M-ohms. Therefore, design should be performed so as to connect a low impedance output circuit to the VI terminal. The capacity of the internal capacitor is 100 - 200pF.

3. Input Filter Section

The low pass filter located before the VI terminal eliminates the repeated noise during AD conversion. The cutoff frequency should generally be set to 0.8 x 1/2 to 1/2 of the sampling frequency.

For the construction of the filter, refer to "Q&A" of this data book.

• Analog Output

1. Output Waveform from DAOUT

The maximum amplitude of the output from DAOUT is 1023/1024 x VDD The waveform is a stair step waveform synchronous with the sampling frequency.

Input/output waveform for the VI, VR, and DAOUT terminals are illustrated below:

2. Output Filter Section

Because the output from DAOUT is a stair step waveform, add a low pass filter.

The output impedance of DAOUT varies in the range between 12 kΩ and 22 kΩ

Determine a filter constant so that resistance variations caused by the change of the output impedance may not affect the cutoff frequency for the filter.

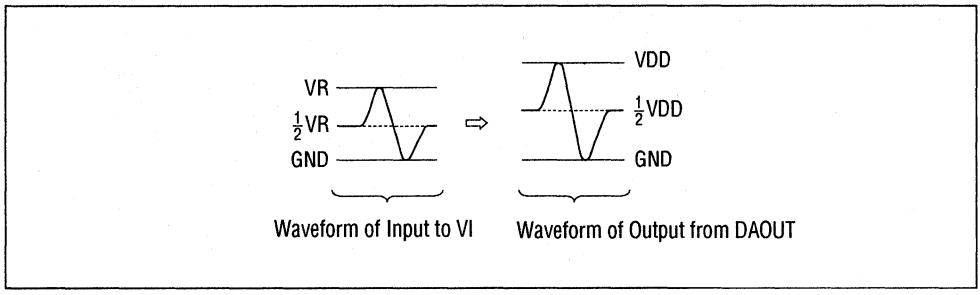


Figure 1

- **Use of External AD and DA Converters**

To establish a high quality recording/playing system, a 12-bit AD and 12-bit DA converters can be externally mounted.

1. Use of External AD Converter

Enter data, which has underwent straight binary conversion with the AD converter, to ADSI, and enter clock signal through SICK.

Read data from ADSI at the rise of SICK. Figure 2-1 shows the timing:

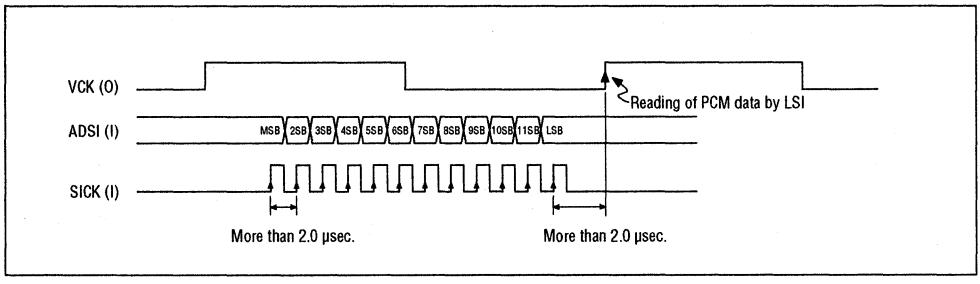


Figure 2-1 Use of External AD Converter and Timing

2. Use of External DA Converter

According to the timing of DASO and SOCK shown in Figure 2-2, straight binary data and clock are output. The data from DASO changes at the rise of SOCK.

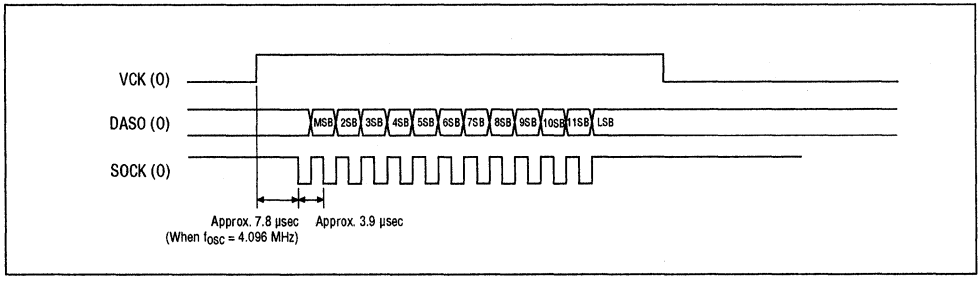


Figure 2-2 Use of External DA Converter and Timing

- **Original Oscillation Frequency and Sampling Frequency**

1. Relationship between the Original Oscillation Frequency and the Sampling Frequency

The LSI can use an original oscillation frequency in the range between 4 and 8MHz. The sampling frequency (fs) can be selected as shown in the table below:

Table 1 Relationship between SAM1, SAM2 and Sampling Frequency

SAM1	L	H	L	H
SAM2	L	L	H	H
fs	$\frac{f_{osc}}{1024}$	$\frac{f_{osc}}{768}$	$\frac{f_{osc}}{512}$	Inhibited

f_{osc} : Original oscillation frequency

2. Connection of Oscillator

Figure 3 illustrates how to connect an oscillator. For reference, the optimum capacity when a Kyocera-produced ceramic oscillator is connected to XT and $\overline{XT}$ is shown in the table below. If a Murata Seisakusho-produced ceramic oscillator is to be used, connect 30pF to C1 and C2.

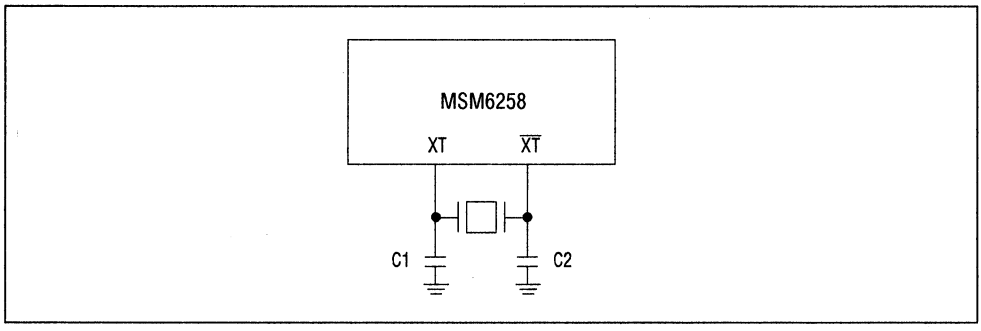


Figure 3 Connection of Oscillator

Ceramic oscillator		Optimum capacity	
Model	**Frequency (kHz)**	**C1 (pF)**	**C2 (pF)**
KBR-4.0MS	4000	33	33
KBR-4.096MS	4096	33	33
KBR-5.0MS	5000	33	33
KBR-6.0 MS	6000	33	33
KBR-8.0 MS	8000	22	22

- **Relationship between D0-D7 and ADPCM Data**

Table 2 Relations between D0-D7 and ADPCM Data

D0	D1	D2	D3	D4	D5	D6	D7	
B0n	B1n	B2n	B3n	B0n+1	B1n+1	B2n+1	B3n+	← 4-bit ADPCM
*	B0n	B1n	B2n	*	B0n+1	B1n+1	B2n+1	← 3-bit ADPCM

4-bit ADPCM
- B3n ..... Polarity bit for n-th sampling
- B2n ..... MSB for n-th sampling
- B1n ..... 2SB for n-th sampling
- B0n ..... LSB for n-th sampling

3-bit ADPCM
- B2n ..... Polarity bit for n-th sample
- B1n ..... MSB for n-th sampling
- B0n ..... LSB for n-th sampling
- * ..... Pull down when the resistance reaches approximately 100 k-ohms.

As shown above, data D0 through D3 precedes data D4 through D7.

To prepare ADPCM data for MSM6295 or to perform reproduction using ADPCM data, connection must be changed to exchange D0-D3 with D4-D7.

- **Operation for Stand-Alone Version**

1. Power Saving Function

When SRAM is selected, the power saving function for the LSI is activated to stop oscillation in standby mode (in any mode other than record or play mode).

It may sometimes take 20 to 30 msec. before oscillation is stabilized.

To shorten the stabilizing time, it is recommended to use a ceramic oscillator.

2. Basic procedure for recording and playing

Basic procedure for recording and playing using channel 1 is described in this section. Recording and playing can be done very easily.

2.1 Recording

Set the REC/$\overline{\text{PLAY}}$ terminal to record mode, and select channel 1 using CA1 through CA3. Enter a pulse to the ST•SP terminal, and recording begins. To terminal recording, enter a pulse to the ST•SP terminal again. Recording is done between these two pulses. If 8kHz sampling is selected, recording time can be extended by up to 64ms (equivalent to 2k-bit). Figure 4 shows the relations between ST•SP and recording time.

In the initial state, recording is not terminated automatically. So, it is necessary to enter a pulse for termination.

2.2 Playing

Playing begins if the REC/$\overline{\text{PLAY}}$ terminal is set to play mode, and a pulse is entered to the ST•SP terminal. When recording time is reached, playing is terminated automatically. To suspend playing half way, enter a pulse to the ST•SP terminal again. Figure 5 shows the relationship between ST•SP and playing time.

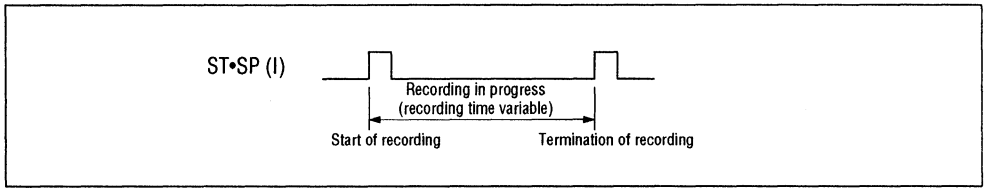


Figure 4 Recording Sequence

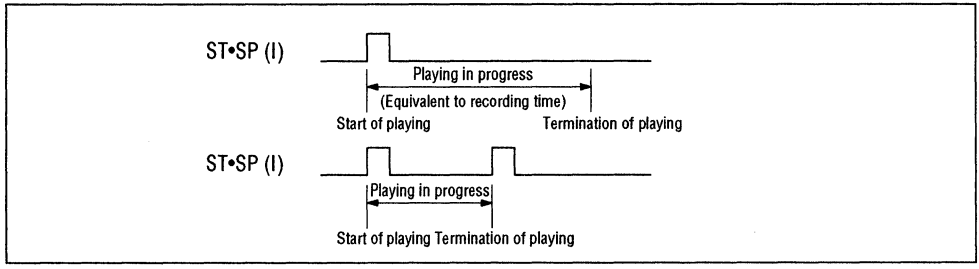


Figure 5 Playing Sequence

3. Use of Channels

MSM6258 allows selection of eight channels: channel 0 through channel 7. Each channel has flag status (FST). Use of the channels is described below.

3.1 Initial Recording conditions of channels 1 through 7 and external RAM

To start recording in the initial state (nothing is recorded in any channel), channel 1 through channel 7 must be used in that order. Table 3 shows the channels and their addresses.

The external RAM after completion of recording in channel 1 through 7 is demarcated in proportion with recording time in 2 K-bit steps. The length of each channel can be freely set so far as the capacity of the external RAM allows. Figure 6 shows an example. FST for the channel that was used for recording is set to the "H" level.

3.2 Use of Channel 0

If channel 0 is selected, FST is always set to the "H" level, and the data saved beginning with the start address of the external RAM. This is helpful if only one word is to be recorded in the external RAM or if voice data written to EPROM or masked ROM is to be reproduced. (See an example of an applied circuit in Figure 27.)

To terminate recording or playing, enter a stop pulse to the ST•SP terminal.

Do not forget to set the VDS terminal to the "L" level.

Table 3 Channels and Addresses

Channel	Channel address		
	CA1	CA2	CA3
0	L	L	L
1	H	L	L
2	L	H	L
3	H	H	L
4	L	L	H
5	H	L	H
6	L	H	H
7	H	H	H

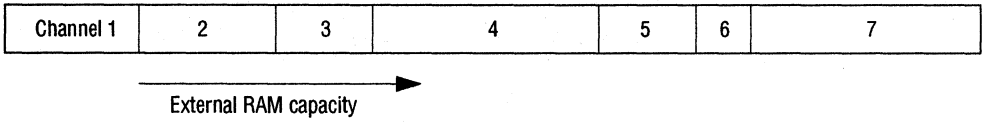


Figure 6 Example of External RAM and Channel Length

4. Recording/Playing and FST

The LSI enables selection of channels using CA1, CA2, and CA3. Each of channels 1 through 7 has flag status (FST). The relationship between recording/playing and FST are shown in Table 4:

Table 4 Relationship between recording/playing and FST

	FST = "L"	FST = "H"
Recording	a	b
Playing	c	d

a: Recording time is variable. Recording can be done according to the procedure described in 2.1. When the power is turned on, this status ensues.

b: Recording can be done for the time equivalent to that of the previous recording. Entry of a pulse to the ST•SP terminal starts recording, and terminates it automatically. A pulse entered during recording is invalid. Without external control of addresses, the data in the other channels is preserved as illustrated in Figure 7. However, if VDS is set to the "H" level, recording time can become 0.12 second shorter.

c: Playing is inhibited. When the power is entered, this status ensues.

d: Recording is possible. For recording, follow the procedure described in 2.2.

Notice that FST for channel 0 is always set to the "H" level.

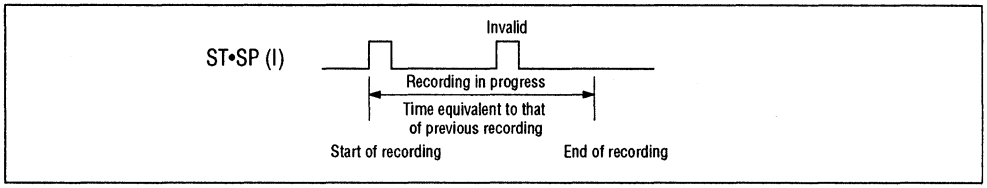


Figure 7 Recording in Status B (Preservation of Data in Channel)

5. Function of Pause Terminal

5.1 Two Pauses after Start

Entering a pulse to the PAUSE terminal temporarily stops a record or play operation.

Entering a pulse again re-starts the paused record or play operation.

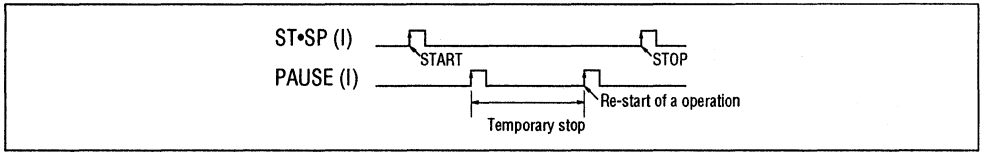


Figure 8

5.2 One Pause after Start

If a pause is invoked once after start, the stop pulse has preference.

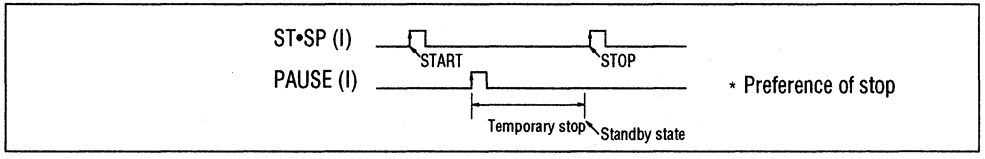


Figure 9

5.3 Pause in Standby Mode

A pause is invalid.

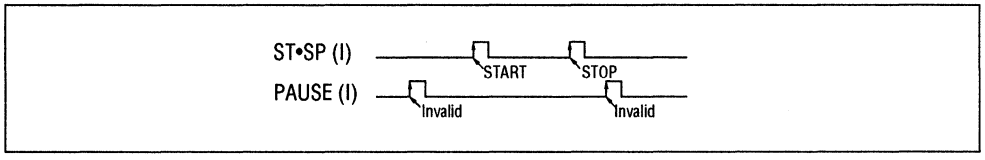


Figure 10

6. Recording

(1) Set the selecting terminals (SAM1, SAM2, ETC.).

(2) Set the REC/PLAY terminal to the "H" level.

(3) Set the channel address terminals CA1 through CA3, and check the OVF (FST) terminal to make sure of the flag status for the channel selected.

If the level of the output from OVF (FST) is "H", it means that data is already recorded in the selected channel. If it is "L", no data is recorded in the selected channel.

(4) Enter a pulse to the ST•SP terminal to start recording.

If the flag of the selected channel is set to "H", recording is automatically terminated when the recording time saved in the selected channel is reached. In this case, entry of a pulse from the ST•SP terminal does not terminate recording half way.

If the flag for the selected channel is "L", a pulse can be entered for the ST•SP terminal to terminate recording.

7. Playing

(1) Set the REC/PLAY terminal to "L".

(2) Set a channel desired to play using the CA1 through CA3 terminals.

(3) Make sure that the OVF (FST) terminal is "H". (If it is "L", playing is not possible.)

(4) Enter a pulse from the ST•SP terminal, and playing begins.

(5) When playing for the selected channel is completed, playing stops automatically.

(6) To terminate playing half way, enter a pulse from the ST•SP terminal.

8. Re-Recording (with Recording length Changed)

MSM6258 has a function to protect the contents in channels other than the one that is selected. To change the recording length for a certain channel, the protection function must be cleared using the flag reset (FRST) terminal.

Suppose recording is done with channels 1 through 4 in the external RAM as shown in Figure 11(a). Let us see how to change the recording lengths for channels 2 thorough 4.

First select channel 2, and reset it using the flag FRST for channel 2. (See Figure 11(b)).

Perform re-recording in channel 2. Because FST is set to "L", pulses have to be entered to the ST•SP terminal to set the start and end of recording. If the recording time for channel 2 is made longer than before, FST for channel 3 is automatically set to "L". At the same time, reproduction for channel 3 is inhibited. (See Figure 11(c).)

In an example shown in figure 11 (d), channel 3 is selected, and re-recording is done so as not to trespass the area of channel 4.

Figure 11 (e) shows an example in which the flag for channel 4 is reset, and re-recording done in channel 4.

In this manner, the external RAM is efficiently used for the channels of the MSM6258.

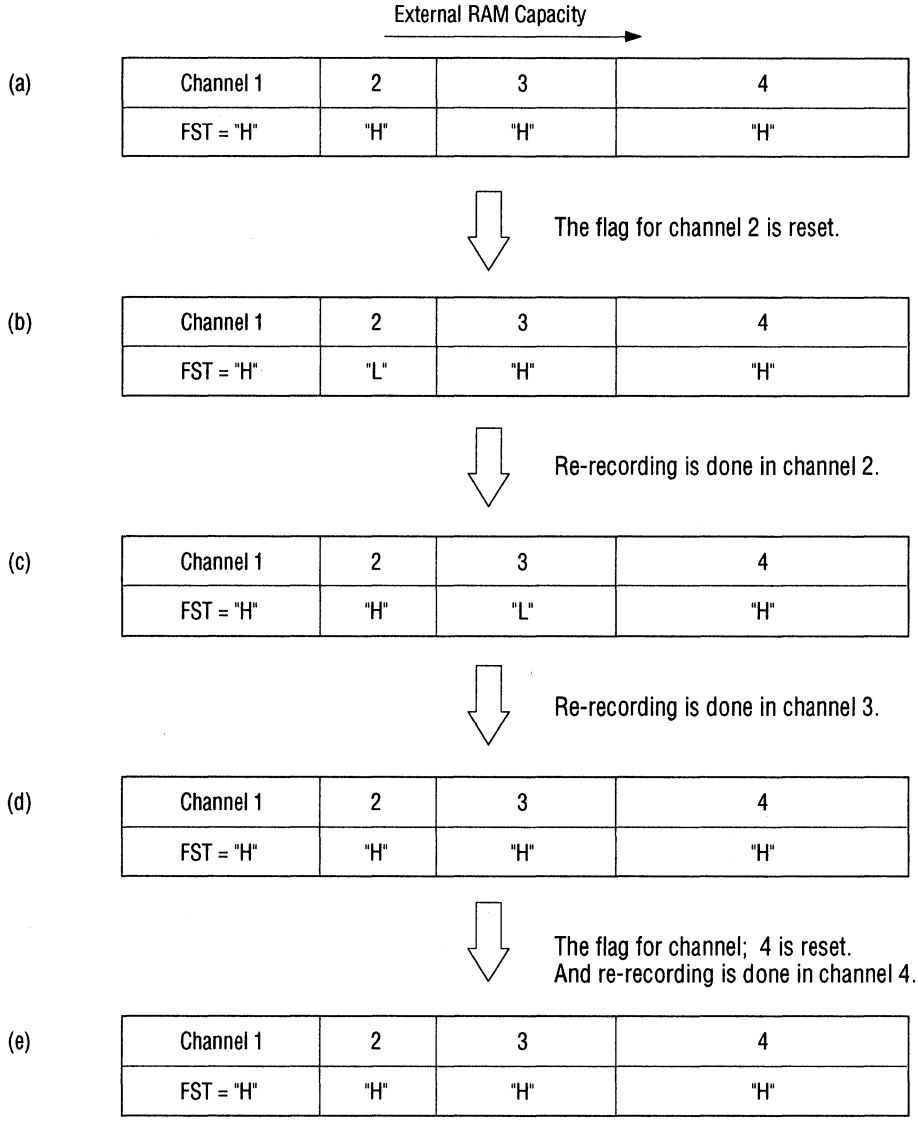


Figure 11 Re-Recording (examples in which recording lengths are changed)

9. Voice Starting

Setting the VDS terminal to "H" activates the voice triggered starting circuit. The circuit decides that there is voice if the difference between the input amplitude for the (n-1)-th sampling and that for the n-th sampling reaches a certain value, and if the number of occurrences reaches a certain value. Saving of ADPCM data in the external RAM begins 64-128 mseconds (fosc=4.096MHz, and fs=8.0kHz) after that time.

10. Access to Internal RAM

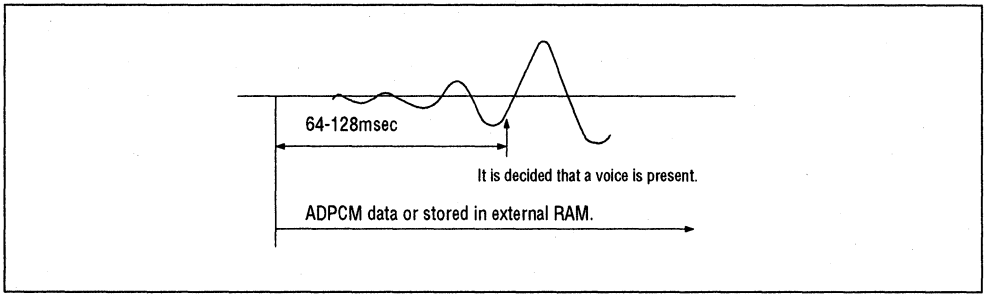


Figure 12 Outline of Voice-Triggered Starting

The start address and stop address for each channel are stored in the internal RAM in MSM6258.

The start/stop addresses for each channel can be changed by writing data to RAM inside the MSM6258.

Using this function, a certain word can be reproduced by externally connecting masked ROM or EPROM. (See an example of circuit shown in Figure 28.)

Procedure for writing the start/stop addresses for channel 1, and time chart are described below:

10.1 Procedure for Writing Start/Stop Addresses

(1) Set RAMS1 to "H", and D/$\overline{\text{SRAM}}$ to "L",

RAMS2 to "H", and REC/$\overline{\text{PLAY}}$ to "L"

Then, the internal RAM can be directly accessed.

(2) Set CA1 to "H", CA2 to "L", and CA3 to "L" to select channel 1.

(3) Set D4 to "L" to invoke start address write mode.

(4) Enter address data to D0, read clock signals (18) to D1, and write signal to D5.

(5) Set D4 to "H" to invoke stop address write mode, and follow the step (4) above again.

Then, the flag status for channel 1 is set to "H".

10.2 Timing Chart

Figure 13 shows a timing chart.

10.3 Control of Addresses in External Memory

RAM inside MSM6258 controls the start/stop addresses of the external memory. Figure 14 shows the outline of the circuit.

In Figure 14, the internal addresses are total 21-bit: the low-order 8-bit and D0 through D12. However, the external addresses are 19-bit: A0 through A18.

If SRAM or ROM is externally connected, D11 and D12 for the internal addresses are not used externally.

Write addresses in all the thirteen bits D0 through D12 to write start/stop addresses in the internal RAM.

At this time, D0 through D12 correspond to A0 through A18 as follows:

D12	→	None
D11	→	None
D10	→	A18
|		|
D0	→	A8

If DRAM is connected, all the 21-bit of the internal addresses are output.

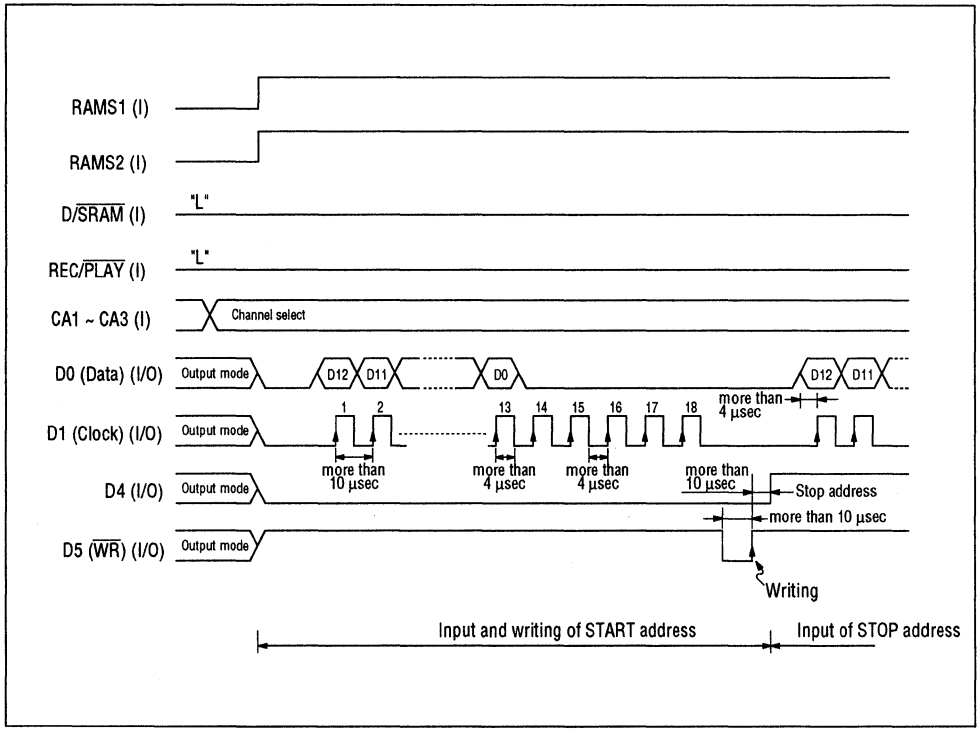


Figure 13

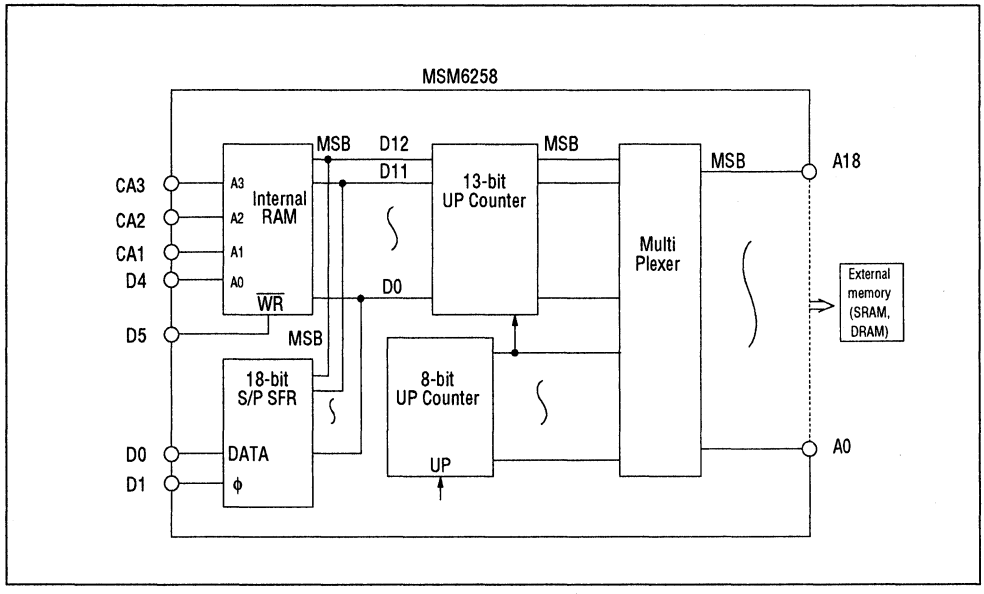


Figure 14

11. Connection and Use of DRAMS

11.1 Connection of DRAMs

64K × 1-bit, 64K × 4-bit, 256 × 1-bit, and 256 × 4-bit, and 1M × 1-bit DRAMs can be connected. MSM6258 allows the connection of up to 16 M-bit. Therefore, DRAMs can be added easily.

Use buffers if sixteen or more DRAMs are to be connected.

Figure 25 shows an example of a circuit in which four DRAMs are connected. As apparent from the figure, MSM6258 has eight data lines: D0 through D7. If the ADPCM bit length is 4-bits, ADPCM data is input and output through 8 data lines. ×4-bit DRAMs installed must be even in number, and the number of ×1 bit DRAMs must be a multiple of 8. If the ADPCM bit length is 3-bit, data is input and output through 6 data lines. So, the number of ×1-bit DRAMs installed must be a multiple of 6.

11.2 Use of DRAMs

DRAM is refreshed by "RAS only refresh" method. So almost any DRAM can be used. MSM6258 has the address terminals A0 through A18. If DRAM is used, the high order address outputs CAS signal, and it also works for chip selection.

Timing charts when 256 × 1-bit or 256 × 4-bit DRAMs are given in Figures 15, 16, and 17. These figures show timing for fosc=4MHz, and fs=7.8kHz.

11.3 Termination of Recording

If recording is started when FST is "L", recording is not terminated until a stop pulse is entered. If recorded data exceeds the capacity of the externally connected RAM, noise is generated when they are reproduced.

So, a stop pulse must be entered according to the RAM size. For this purpose, a timer may be used to control recording time, or chip select signal may be used.

Suppose two 256K × 4-bit DRAMs are connected. If a signal whose polarity is reverse to the signal from the chip select terminal A10 (shown in Figure 15) is entered to the ST • SP terminal as a stop pulse, recording is automatically terminated when recording has been done in two 1M DRAMs.

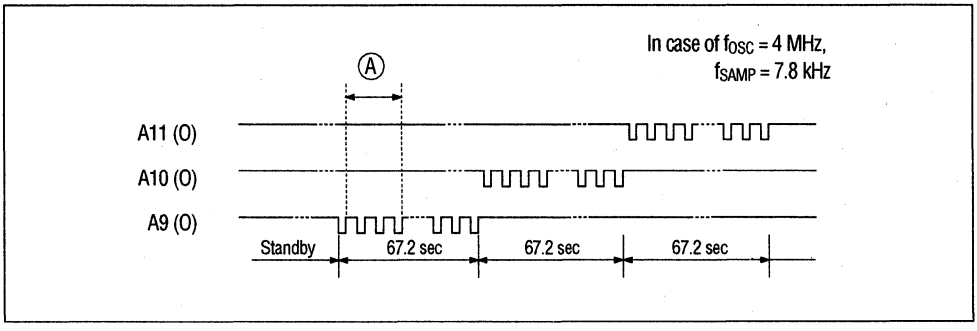


Figure 15 Address Timing for 256 x 4-Bit DRAM

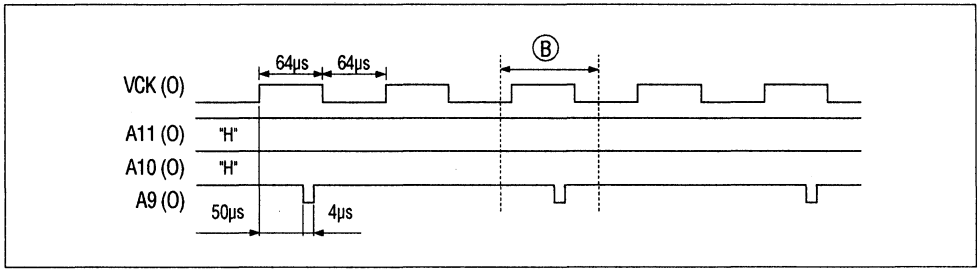


Figure 16 Enlarged View of A

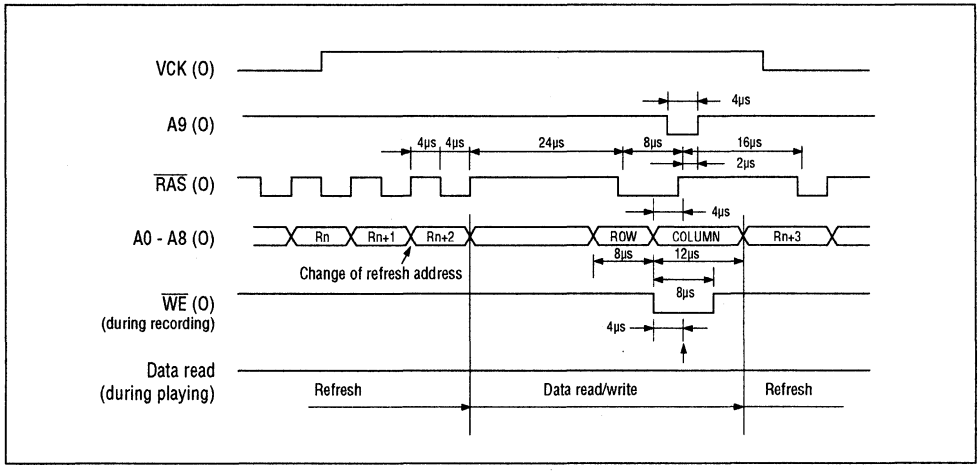


Figure 17 Enlarged View of B

12. Connection and Use of SRAMs

12.1 Connection of SRAMs

MSM6258 allows the direct connection of two types of SRAMs: 64K-bit and 256K-bit SRAMs. The maximum capacity of SRAMS that can be directly connected is 1M-bit (for 256K SRAMs).

The SRAM size can be expanded to up to 4M-bit if A0 through A18 are set for binary output using the RAMS1 and RAMS2 terminals, and a decoder is externally connected.

12.2 Use of SRAMs

Figures 18 and 19 show timing charts when 256K SRAM is selected.

The high-order address terminal automatically functions as a chip select terminal according to the type of SRAM.

These figures show timing when fosc is 4MHz, and fs is 7.8 kHz.

12.3 Recording Termination

If recording is started when FST is "L", recording is not terminated until a stop pulse is entered. If recorded data exceeds the capacity of the externally connected RAM, noise is generated when they are reproduced.

So,a stop pulse must be entered according to the RAM size. For this purpose, a timer may be used to control recording time, or chip select signal may be used.

Suppose two 256K SRAMs are connected. If a signal whose polarity is reverse to the signal from the chip select terminal A17 (shown in Figure 18) is entered to the ST•SP terminal as stop pulse, recording is automatically terminated when recording has been done in two 1M DRAMs.

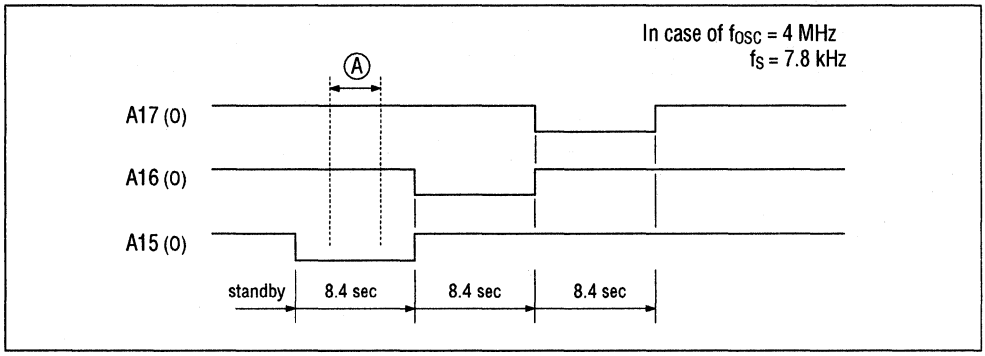


Figure 18 Address Timing for 256K SRAM

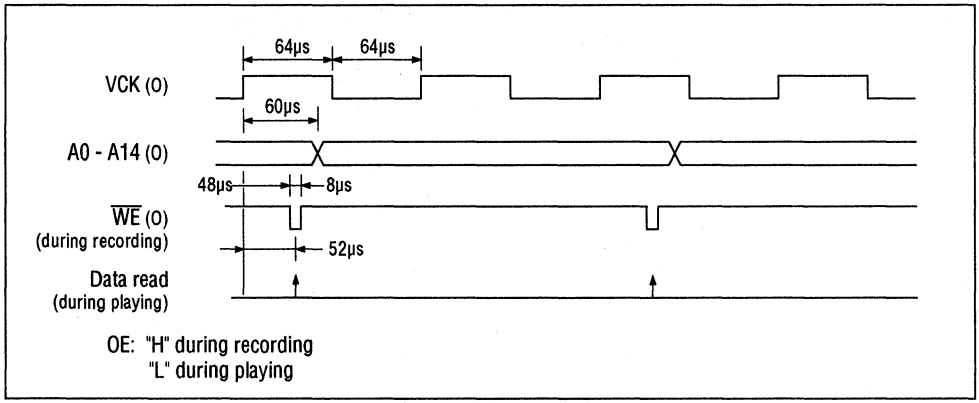


Figure 19 Enlarged View of A

13. Connection and Use of External ROMs

EPROM or masked ROM storing ADPCM data may be connected to reproduce either the entire contents of ROM or part of them.

13.1 Reproduction of Entire Contents of ROM

To reproduce the entire contents of External ROM, set the address to binary output mode using the RAMS1 and RAMS2 terminals, and enter a stop pulse to the ST•SP terminal within 50µs after the level of the A14 terminal is set to "H". Timing is shown in Figure 20.

Similarly, the contents of ROM can be easily reproduced by entering a stop pulse using the A15 terminal for 256K ROM, and the A16 terminal for 512K ROM.

13.2 Reproduction of Part of Contents of External ROM

By connecting ROM, to which many words of ADPCM data is written, to MSM6258, and controlling the internal RAM in MSM6258 using a microcomputer, individual words stored in ROM can be randomly reproduced. Figure 21 shows a flow chart.

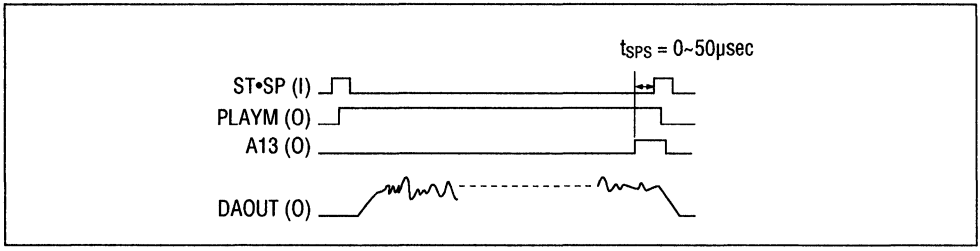


Figure 20 Stop Timing for Reproduction from ROM

Setting of other terminals
(D/$\overline{\text{SRAM}}$ = "L", CA1, 2, 3 = "L",
REC/$\overline{\text{PLAY}}$ = "L", RAMS1 = "L",
RAMS2 = "H")

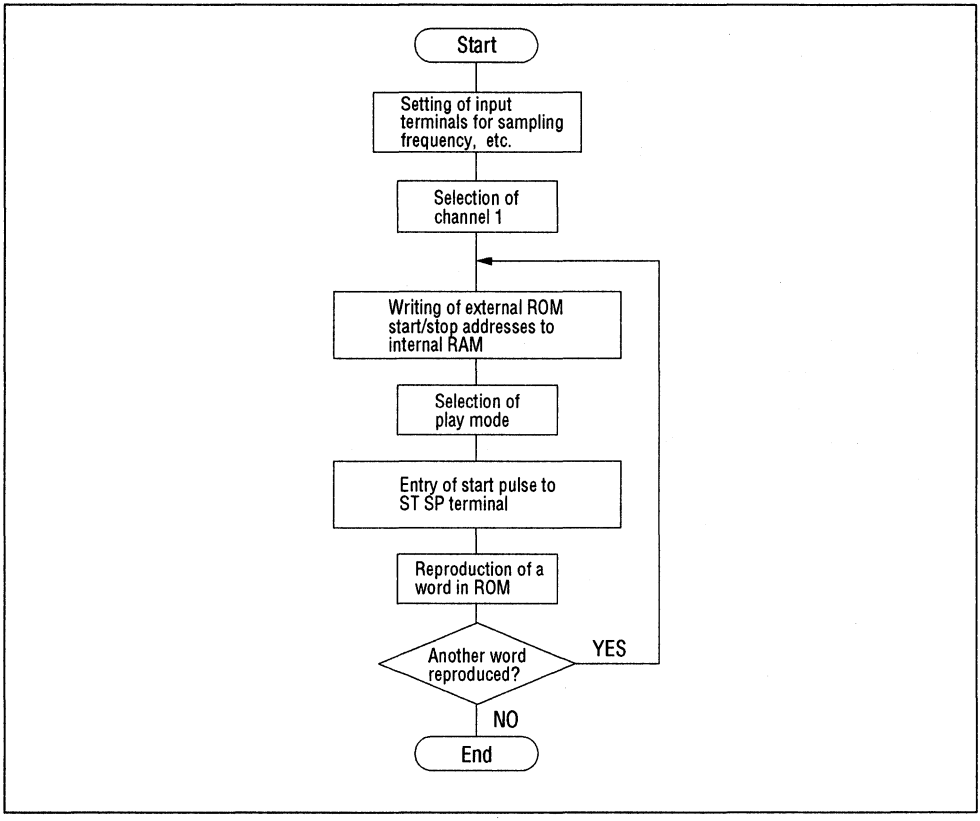


Figure 21 Flow Chart for Reproduction from ROM

14. Use

14.1 Recording of 7 or More Words

As stated earlier, seven words can be recorded in channel 1 through 7. If the internal RAM in MSM6258 is controlled using a microcomputer, more than seven words can be recorded. Operating procedure is similar to that described in 13.2, "Reproduction of Part of Contents of External ROM". Select channel 1, write start/stop addresses to the internal RAM, and record data to that address.

14.2 Use of both RAM and ROM

RAM and ROM may be connected to MSM6258 to record a variable message in RAM and a fixed message in ROM.

Examples of circuits are given in Figures 28 and 29.

15. Backup with Battery

When backing up SRAM storing ADPCM data with a battery, be sure to also back up MSM6258. MSM6258 has RAM to store start/stop addresses for each channel. Even if SRAM is backed up, its contents cannot be reproduced unless MSM6258 itself is backed up.

- **Operation with CPU Interface**

As stated earlier, CPU interface does not control external RAM addresses. Therefore, an external control circuit for RAM must be designed.

1. Connection of Data Bus

Insert a pull-up or pull-down resistor to the data bus bits D0~D7.

Table 5 Use of $\overline{CS}$, D/C, $\overline{RD}$, and $\overline{WR}$

CS	D/C	RD	WR	Operation
L	H	L	H	Output of ADPCM data (during recording)
L	H	H	L	Input of ADPCM data (during playing)
L	L	L	H	Output of status
L	L	H	L	Entry of command
H	x	x	x	Use of data bus is inhibited. (high impedance)

2. Use of Data Bus

The data bus can be controlled using the four pins of the D/C terminal by making a selection as to whether the CS, RD, and WR terminals, and data bus should be used for input/output of ADPCM data or for input/output of command/status.

Table 5 is a list of "H" and "L" combinations of these terminals. As shown in Table 2, ADPCM data for two samples are input and output at a time.

3. Entry of Commands

These are commands for start of recording, start of reproduction, stop of recording/reproduction, and setting of initial pointers.

Entering "H" level makes each of these commands valid.

However, "L" level should be entered for initial pointers P0 through P4. If "H" level is entered, the amplitude of the waveform for reproduction will be changed.

Table 6 shows the relationships between the data bus and command.

Table 6 Data Bus and Command

D0	D1	D2	D3	D4	D5	D6	D7
SP ST	PLAY ST	REC	P4	P3	P2	P1	P0

SP ..... Stop recording and playing
PLAY ST ..... Start playing
REC ST ..... Start recording
P0 ~ P4 ..... Setting of initial pointers (Always enter "L".)

4. Status Output

The status output tells which is currently performed, recording or playing.

The status output in standby mode is as follows:

D0 ~ D6: "L"level
D7: "H"level

Table 7 shows the relationships between the data bus and status.

Table 7 Relationships between Data Bus and Status

D0	D1	D2	D3	D4	D5	D6	D7
X	X	X	X	X	X	X	REC/PLAY

REC/PLAY ..... "H" during recording
"L" during playing

5. Read/Write Timing

Read/write timing of ADPCM DATA is synchronized to MCK.

6. Recording/Playback Method

To start recording, a recording start command is entered using the D/C, WR, and D0 ~ D7 terminals.

During recording, ADPCM data is written to the external RAM in synchronization with the MCK output.

To terminate recording, enter a stop command.

Playing is performed if a play start command is entered, and ADPCM data is read from the external RAM in synchronization with MCK.

Timing for recording and playing is shown in Figure 22. If recording or playing is stopped using a stop command, DAOUT retains the level at which recording or playing has been terminated, and its level is changed to 1/2VDD as soon as a start command is entered.

7. Voice-Triggered Starting

With the CPU interface, voice-triggered starting cannot be performed using the logic circuit in MSM6258. To perform voice-triggered starting, use an external analog circuit. An example of such a circuit is given in Figure 35.

8. Troubleshooting Check List

If normal playing is impossible even when the hardware and software for CPU interface are used, perform check up according to the following procedure:

(1) Check DAOUT output during recording:

The waveform of the output from the DAOUT terminal during recording is just the same as that during playing. Make sure that the waveform of the output from the DAOUT is normal.

(2) Recording and playing of muted voice:

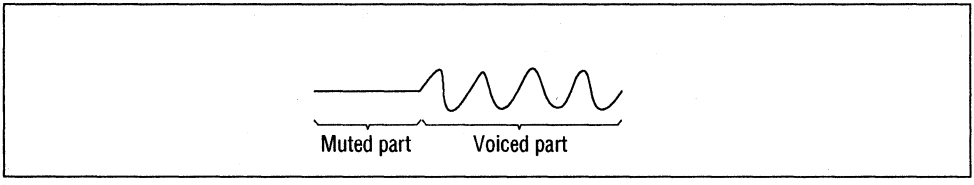
If the waveform of the output during recording is normal, use a muted voice waveform, or DC level waveform.

If the waveform of the output from DAOUT during playing rises or falls, ADPCM data read/write timing is wrong. Check read/write timing.

(3) Recording and playing of muted voice waveform and voice waveform:

To check read/write timing, perform recording and playing using a waveform consisting of muted voice and voice.

If the waveform of the output from DAOUT rises or falls during playing, or if its amplitude changes, check read/write timing again.



(4) Recording and playing of voice waveform:

For final checkup, perform recording and playing using a voice waveform.

If the amplitude of the waveform of the output from DAOUT during playing changes, the trouble may lie in the interface with the external RAM. More concretely, it is likely that ADPCM data for several samples are not stored in the external RAM before start of recording, or ADPCM data for several samples are not transferred from the external RAM to LSI before start of playing. To see whether the timing after start of playing is normal, enter the ADPCM data given below to the LSI, and check that a 1.5Vp-p sine wave is output from DAOUT.

If the waveform is 1.5Vp-p sine wave, the interface for playing is judged to be normal. Check the timing for start of recording again.

How to generate 1.5Vpp sine wave:

Enter the following ADPCM data:

0,3,3,7,F,7,F,4,C,4,C,4,0,9,C,8,1 repetitions of 4,0,9,C,8,1

This data will work with a M5205 but must be nibble swapped for the 6258.

<Example>

D7 ~ D0

(3 0)$_{HEX}$ Please refer to ADPCM data of P.29.

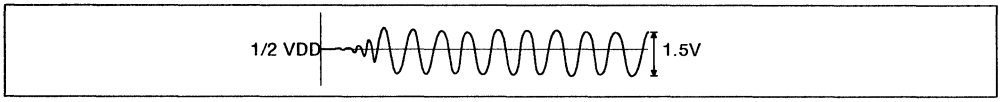
(7 3)$_{HEX}$

(7 F)$_{HEX}$

(4 F)$_{HEX}$

Waveform of output from DAOUT

Waveform of output from DAOUT



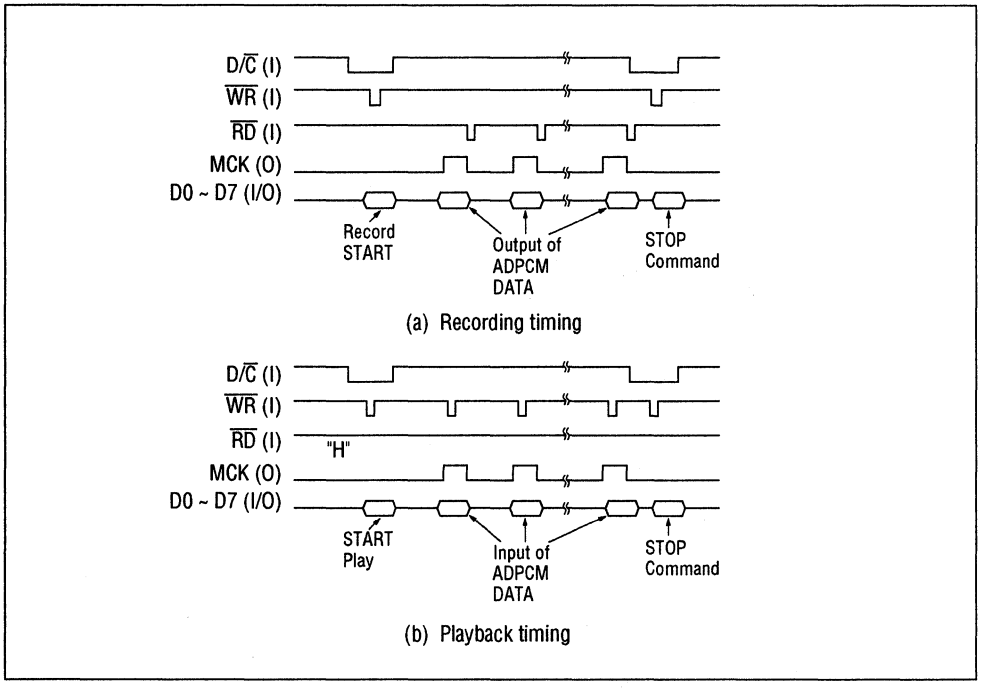


Figure 22

CIRCUIT EXAMPLES

- Figure 23 shows an example of interface with 64K SRAM.
- Figure 24 shows an example of interface with 256K SRAM.
- Figure 25 shows an example of interface with 256K SRAM.
- Figure 26 shows an example of interface with 256K DRAM.
- Figure 27 shows an example of interface with 1M DRAM.
- Figure 28 shows an example of interface with 256K EPROM.
- Figure 29 shows an example of interface with 512K EPROM.
- Figure 30 shows an example of interface with MSM5840A when MSM6258, masked ROM, and SRAM used for fixed and variable messages.
- Figure 31 shows an example of a circuit when MSM6258, masked ROM, and DRAM, and SRAM are used for fixed and variable messages.
- Figure 32 shows an example of interface with MSM80C85 when MSM6258, is used in CPU interface.
- Figure 33 shows an example of a mute circuit used for recording with MSM6258.
- Figure 34 shows an example of a voice-triggered starting circuit for the CPU interface with MSM6258.

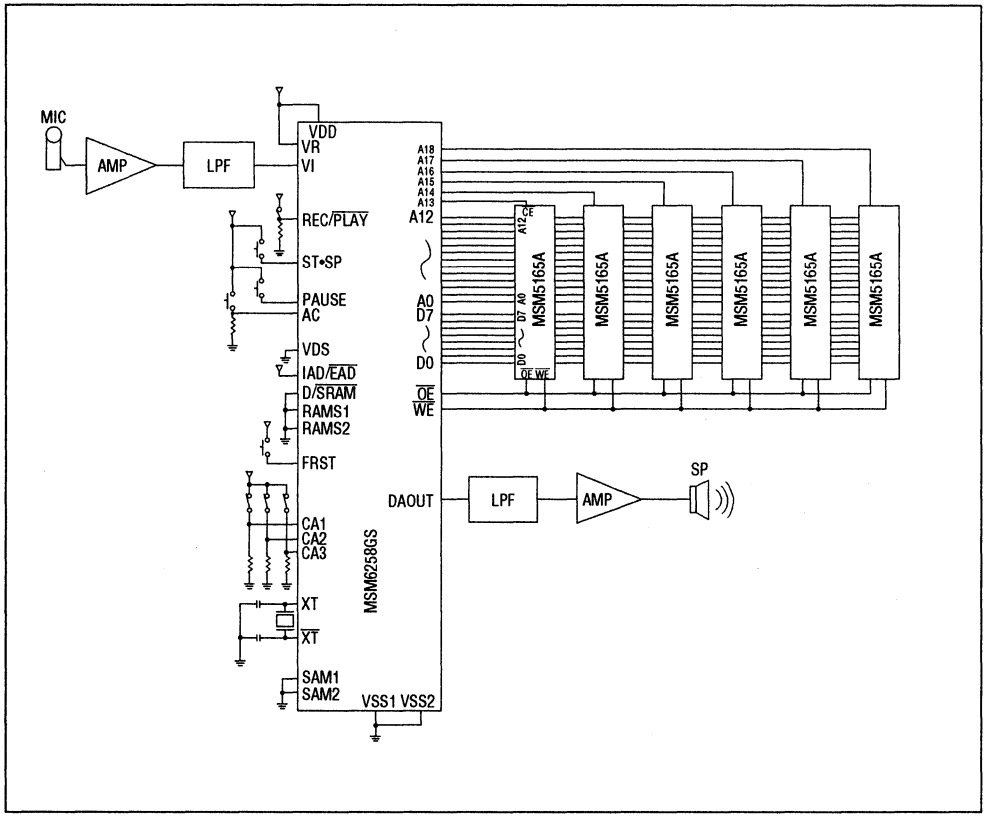


Figure 23 Application Note for 64K SRAM

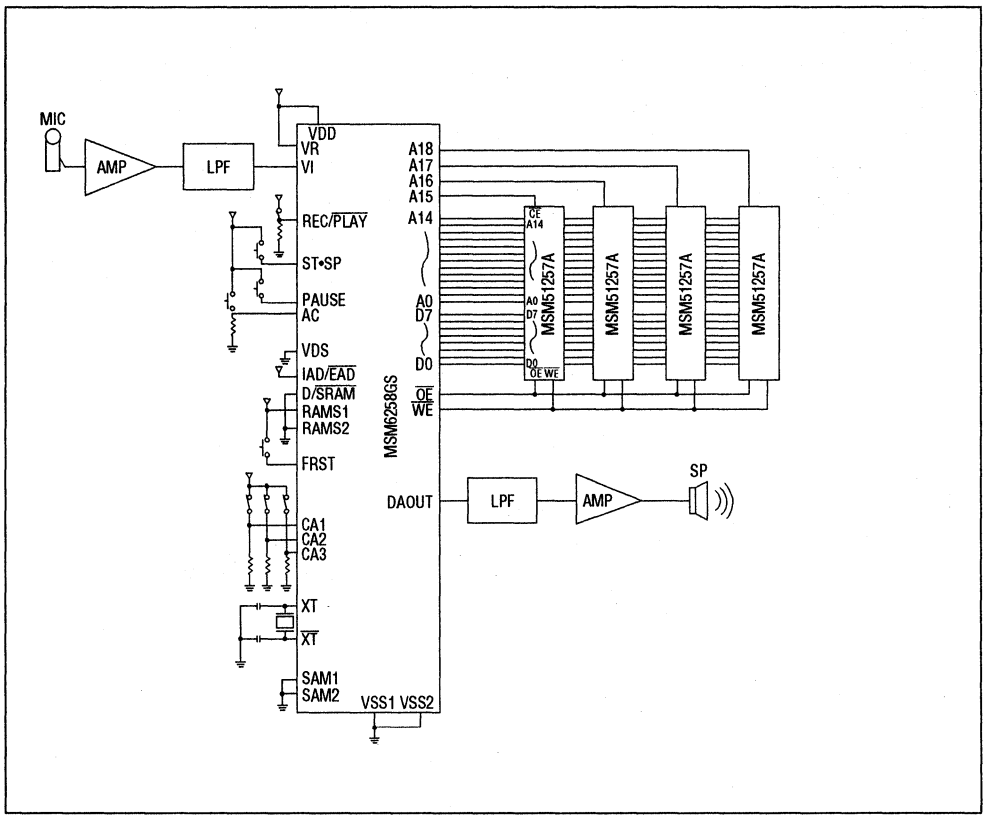


Figure 24 Application Note for 256K SRAM

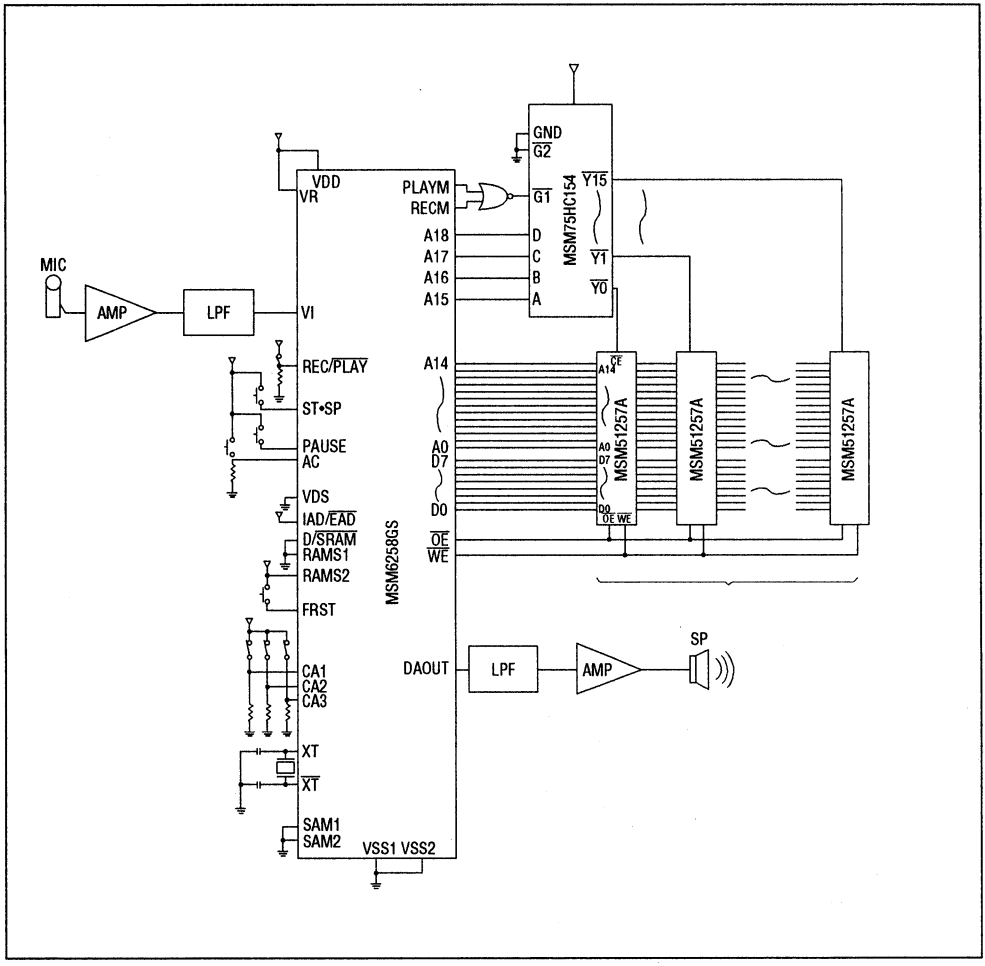


Figure 25 Application Note for 256K SRAM (Use 16 pcs)

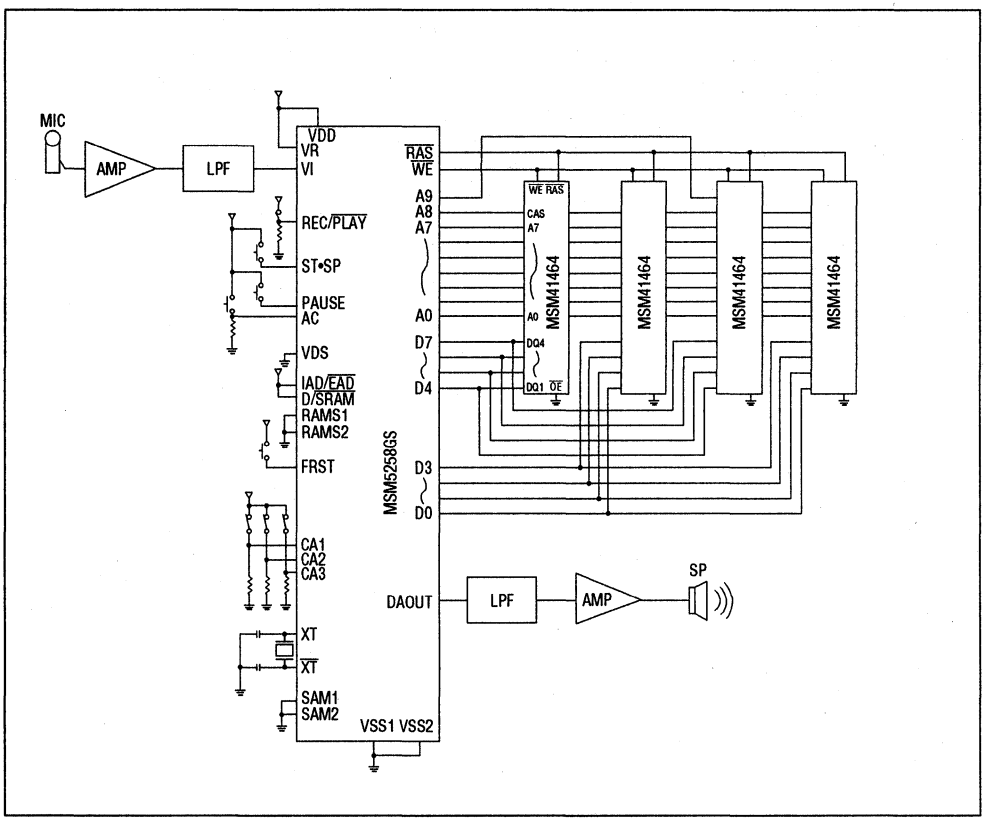


Figure 26 Application Note for 256K DRAM

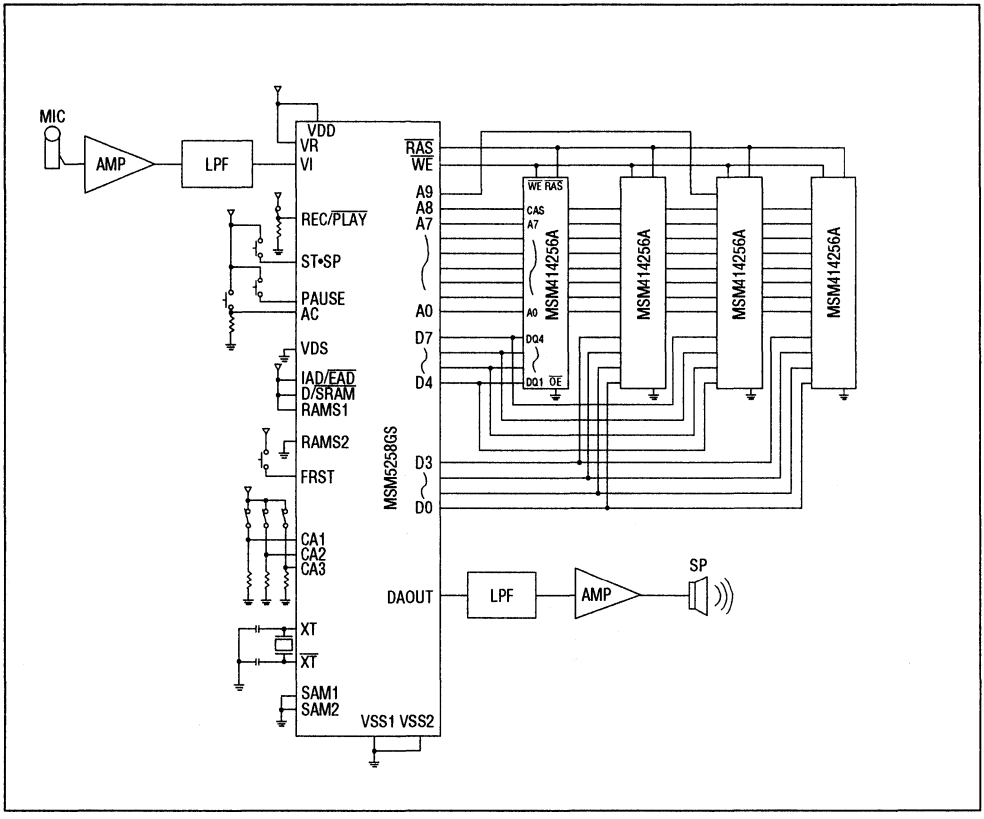


Figure 27 Application Note for 1M-bit DRAM

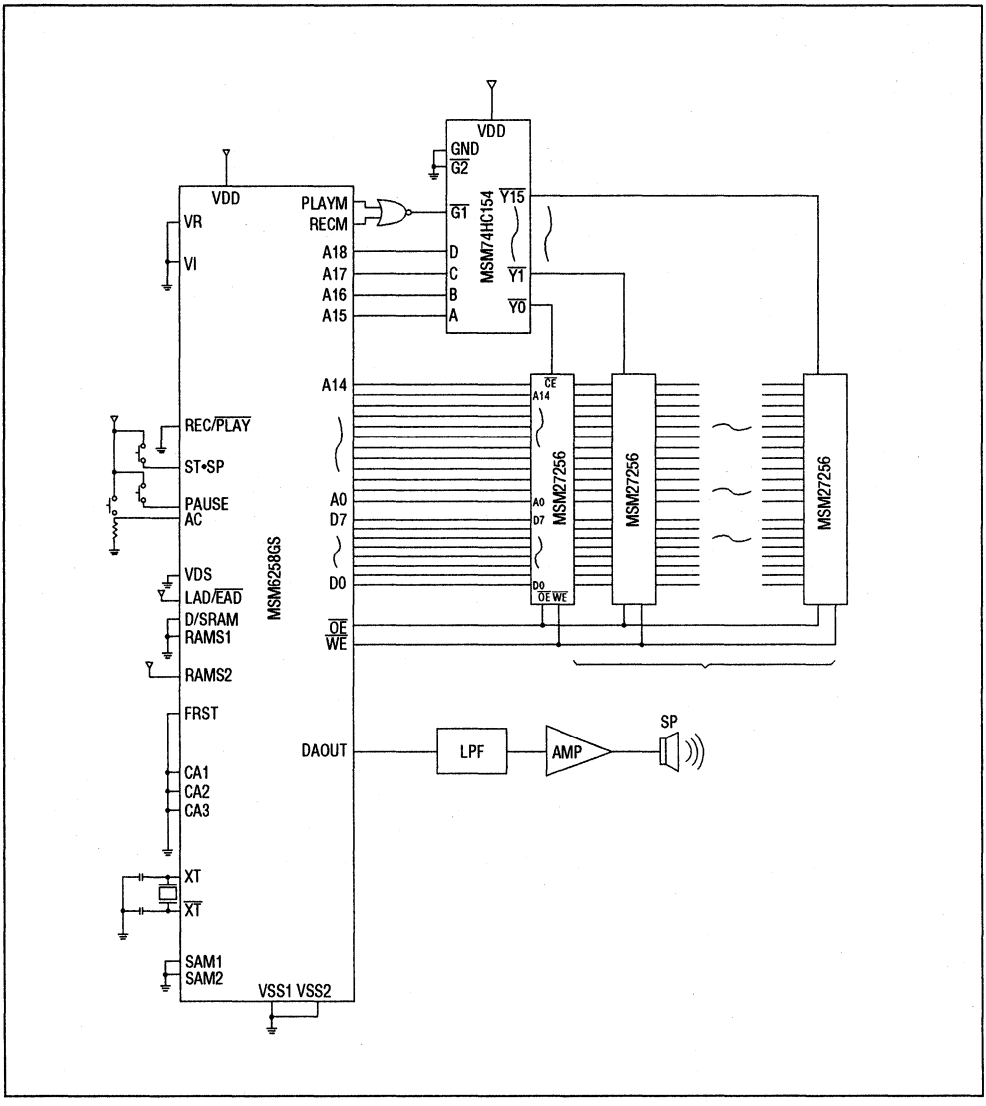


Figure 28 Application Note for 256K EPROM (Use 16 pcs)

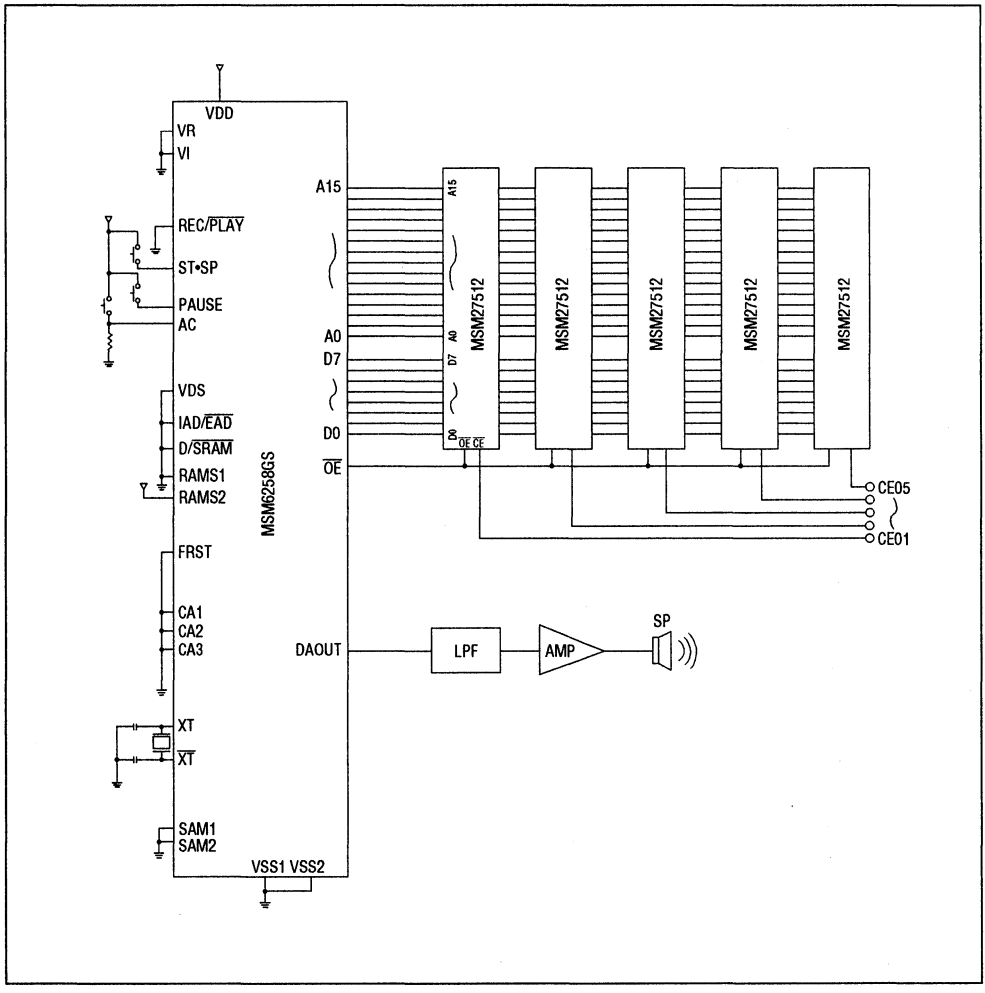


Figure 29 Application Note for 512K EPROM (Address is binary output)

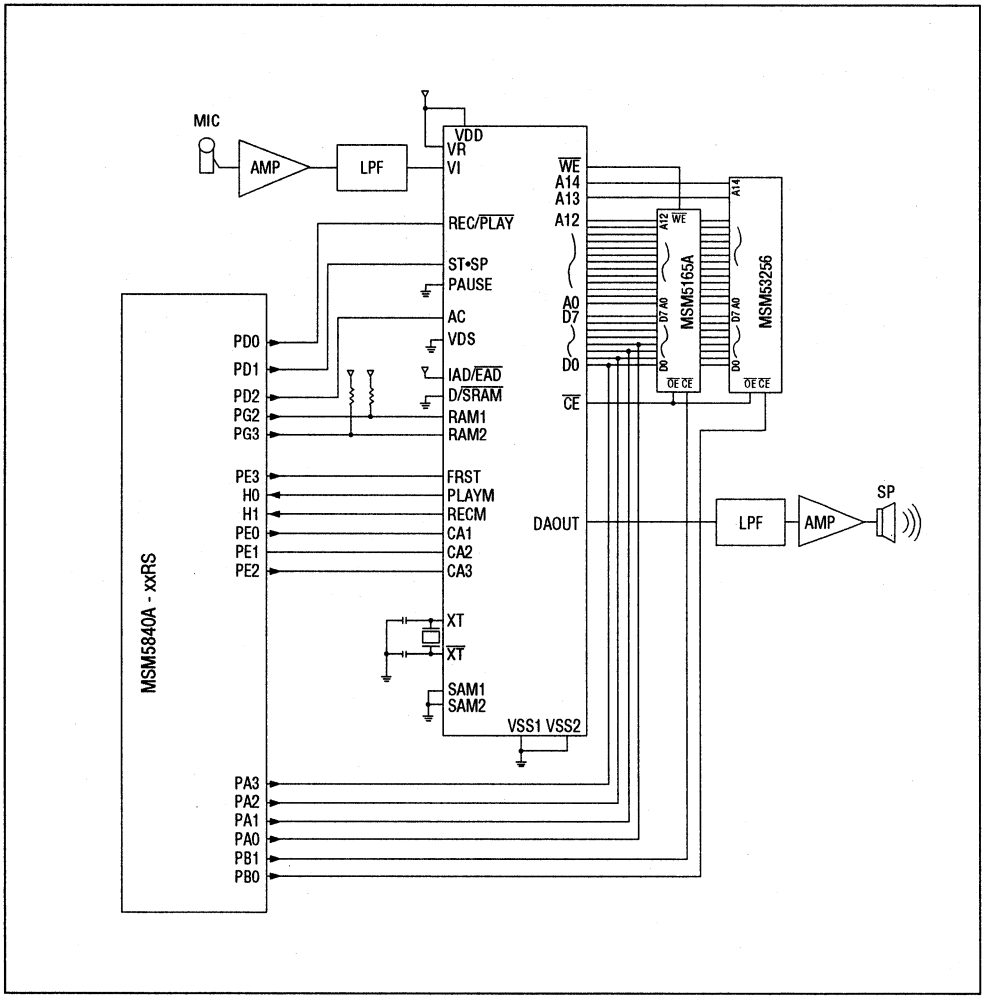
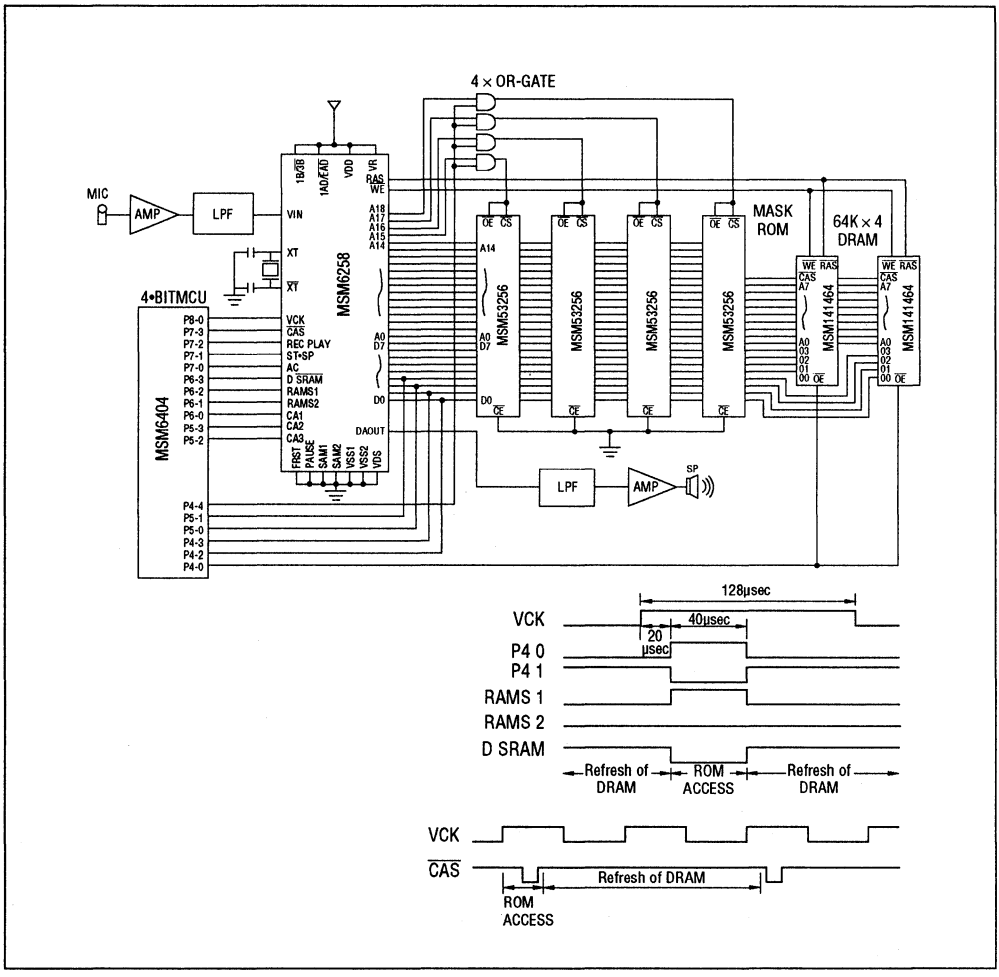


Figure 30 Example of Interface with 64K SRAM & 256K Mask ROM



In case both DRAM and masked ROM are used, it is necessary to refresh DRAM except when data is being read from the masked ROM.
The figure on the right shows the timing when fs is 3.9kHz. Read data from ROM during the ROM access time shown in the figure.

Figure 31 Example of Interface for 256K DRAM and Masked ROM

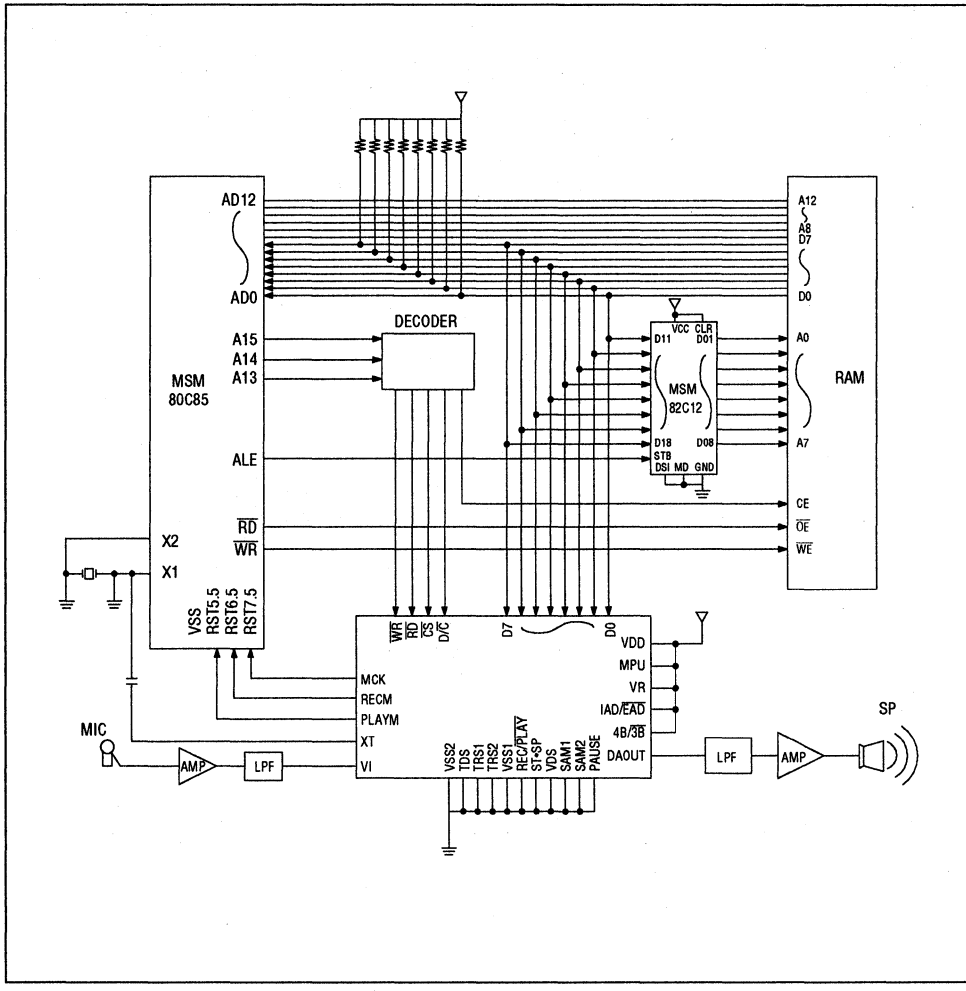


Figure 32 Example of Interface with MSM80C85

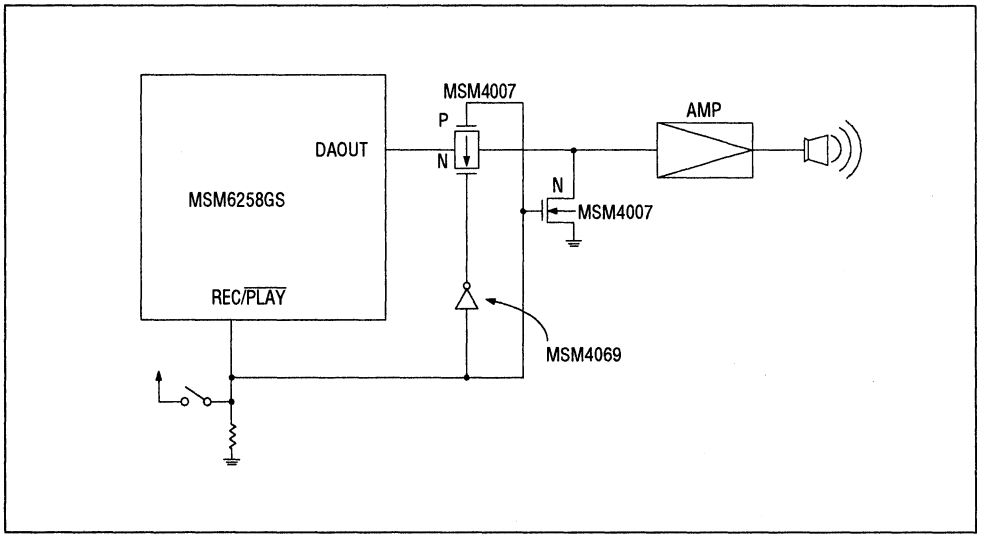


Figure 33 Example of Mute Circuit for Recording

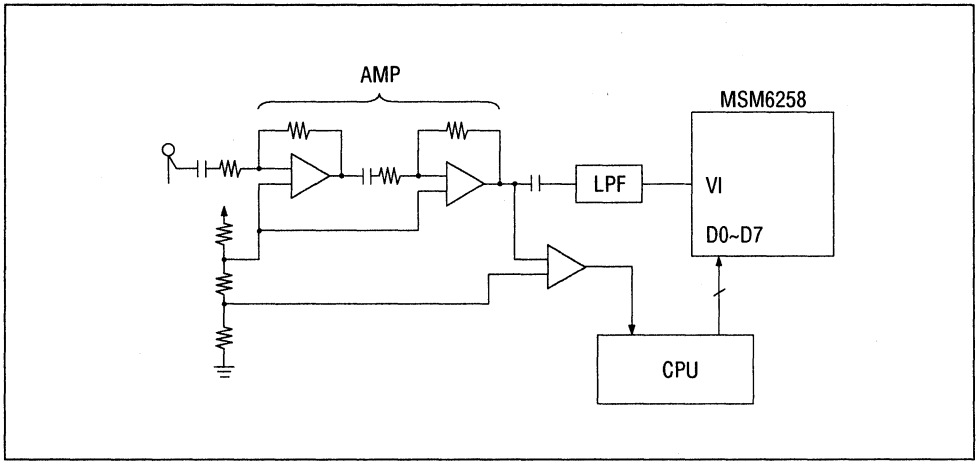


Figure 34 Voice-Triggered Starting Circuit for CPU Interface

OKI Semiconductor

MSM6310

PCM RECORDING & PLAYBACK LSI

GENERAL DESCRIPTION

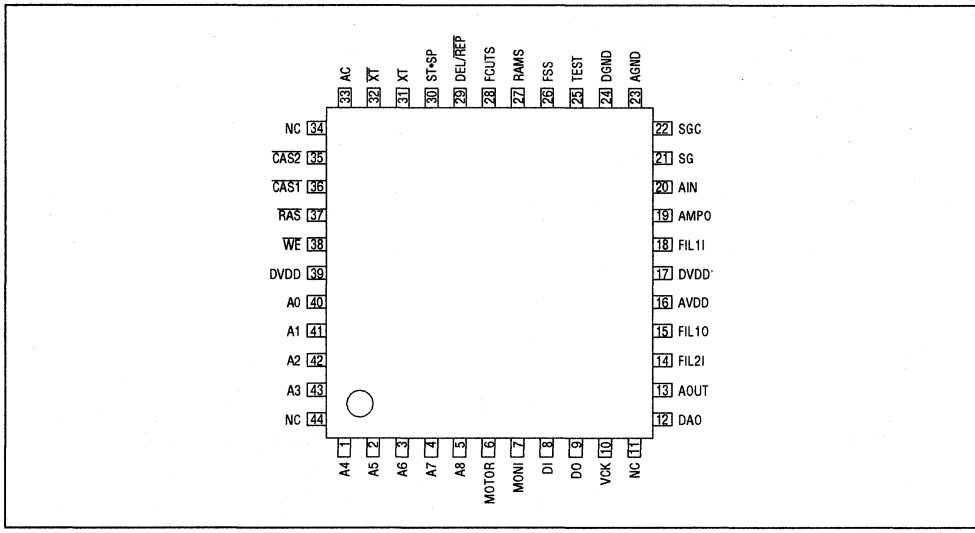
The MSM6310 is a PCM recording & playback LSI which is manufactured using Oki's low power CMOS silicon gate technology. The MSM6310 is designed for the purpose of endless loop recording by 8-bit PCM.

The internal circuit is made up of following three units. The first one is an input unit which consists of line amplifier, low pass filter and 8-bit AD converter. The second one is an output unit which consists of 8-bit DA converter and low pass filter. The third one is a control unit for external DRAMs.

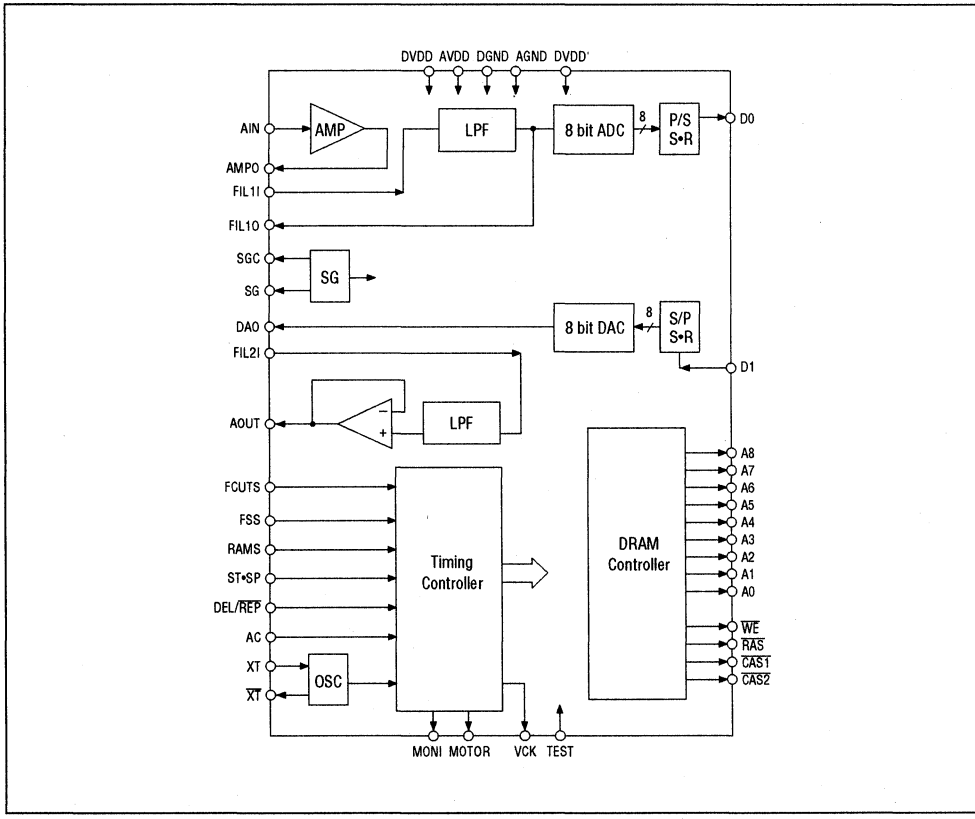
FEATURES

- 8-bit PCM
  (built-in 8-bit AD/DA converter)
- External DRAM driving capability 256K, 2 pcs.
  *256K DRAM type → 256KW x 1 bit
  (MSM41256A) $\overline{CAS}$ before $\overline{RAS}$ refresh
- Sampling frequency:
  4 kHz (f_{OSC}=4.096 MHz)
- Oscillation frequency:
  4 to 8.2 MHz (nominally 4.096 MHz)
- Supply voltage: +5V
- Analog line input
- Motor driving signal output
- Recording/Playback period:
  4 sec (f_S=4kHz, 1 x 256K DRAM)
  8 sec (f_S=4kHz, 1 x 256K DRAM or f_S=8kHz, 2 x 256K DRAM)
  16 sec (f_S=4kHz, 2 x 256 K DRAM)
- 44 pin plastic QFP
  (QFP44-P-910-K)

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 to 7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–	−55 to + 150	°C

Operating Range

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}	DGND = AGND = 0V	+4.5 to +5.5	V
Operating temperature range	T_{OP}	–	−40 to 85	°C
Oscillator frequency	F_{OSC}	–	4.0 to 8.2	MHz

- **DC Electrical Characteristics**

(DVDD=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage (Note 1)	V_{IH1}	—	3.6	—	—	V
High input voltage (Note 2)	V_{IH2}	—	0.8xV_{DD}	—	—	v
Low input voltage	V_{IL}	—	—	—	0.8	v
High output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	v
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	v
High input current (Note 3)	I_{IH1}	V_{IH} = V_{DD}	20	—	400	μA
High input current (Note 4)	I_{IH2}	V_{IH} = V_{DD}	—	—	10	μA
Low input current	I_{IL}	V_{IL} = V_{SS}	−10	—	—	μA
Output leak current	I_{LO}	$V_{SS} \leqq V_{OUT} \leqq V_{DD}$	−10	—	10	μA
Operating consumed current	I_{OD}	f_{OSC} = 4.096MHz	—	—	10	mA
DA output relative precision	$\lvert V_{DAE} \rvert$	No load	—	—	40	mV
AD conversion relative precision	$\lvert V_{ADE} \rvert$	—	—	—	40	mV

Note 1: Applicable to the input terminal excluding the XT terminal.
Note 2: Applicable to the XT terminal.
Note 3: Applicable to the terminals (ST, SP, TEST1) with a pulldown resistance.
Note 4: Applicable to the terminal without a pulldown resistance.

• AC Electrical Characteristics

f_{OSC}=4.096MHz, f_S=8.0kHz, V_{DD}=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
ST-SP pulse amplitude	t_{STP}	35	—	—	ms
When DEL/$\overline{REP}$=L, time from start pulse input to the waveform output from the AOUT terminal	t_{SRA}	16	—	256	ms
When DEL/$\overline{REP}$=L, time from start pulse input to the rising edge of MOTOR terminal	t_{STM}	16	—	35	ms
When DEL/$\overline{REP}$=L, non-sound time from stop pulse input to rising edge of MOTOR terminal	t_{MS}	—	256	—	ms
When DEL/$\overline{REP}$=L, time from stop pulse input to MOTOR terminal	t_{SPM}	16	—	35	ms
Time from strat pulse input to rising edge of MONI terminal	t_{SMN}	16	—	35	ms
Time from strat pulse input to falling edge of MONI terminal	t_{PMN}	16	—	35	ms
Under condition 2.2), time from start pulse input to time from rising edge of MOTOR terminal	t_{SMT}	16	—	35	ms
Time from rising edge of DEL/$\overline{REP}$ to falling edge of MOTOR terminal	t_{DPM}	—	2	—	µs
Time from falling edge of DEL/$\overline{REP}$ to falling edge of MOTOR terminal	t_{RPM}	—	2	—	µs
VCK H level amplitude, VCK L level amplitude	t_{VH}, t_{VL}	—	62.5	—	µs
Time from falling edge of MONI terminal to rising edge of DEL/REP	t_{DRM}	—	2	—	µs
$\overline{RAS}$ pulse amplitude	t_{RAS}	—	4.4	—	µs
$\overline{CAS}$ pulse amplitude	t_{CAS}	—	3.9	—	µs
$\overline{WE}$ pulse amplitude	t_{WE}	—	1.0	—	µs
$\overline{RAS}$ precharge time	t_{RP}	—	0.5	—	µs
Time from rising edge of VCK to falling edge of $\overline{RAS}$	t_{VRP}	—	2.9	—	µs
Time from rising edge of VCK to falling edge of $\overline{CAS}$	t_{VCF}	—	4.9	—	µs
Time from rising edge of VCK to falling edge of $\overline{WE}$	t_{VWE}	—	6.8	—	µs

Note: All items are proportional to f_{OSC}. (If f_{OSC} is higher, the time is shorter.)

FUNCTIONAL DESCRIPTION

This description is based on the following conditions.

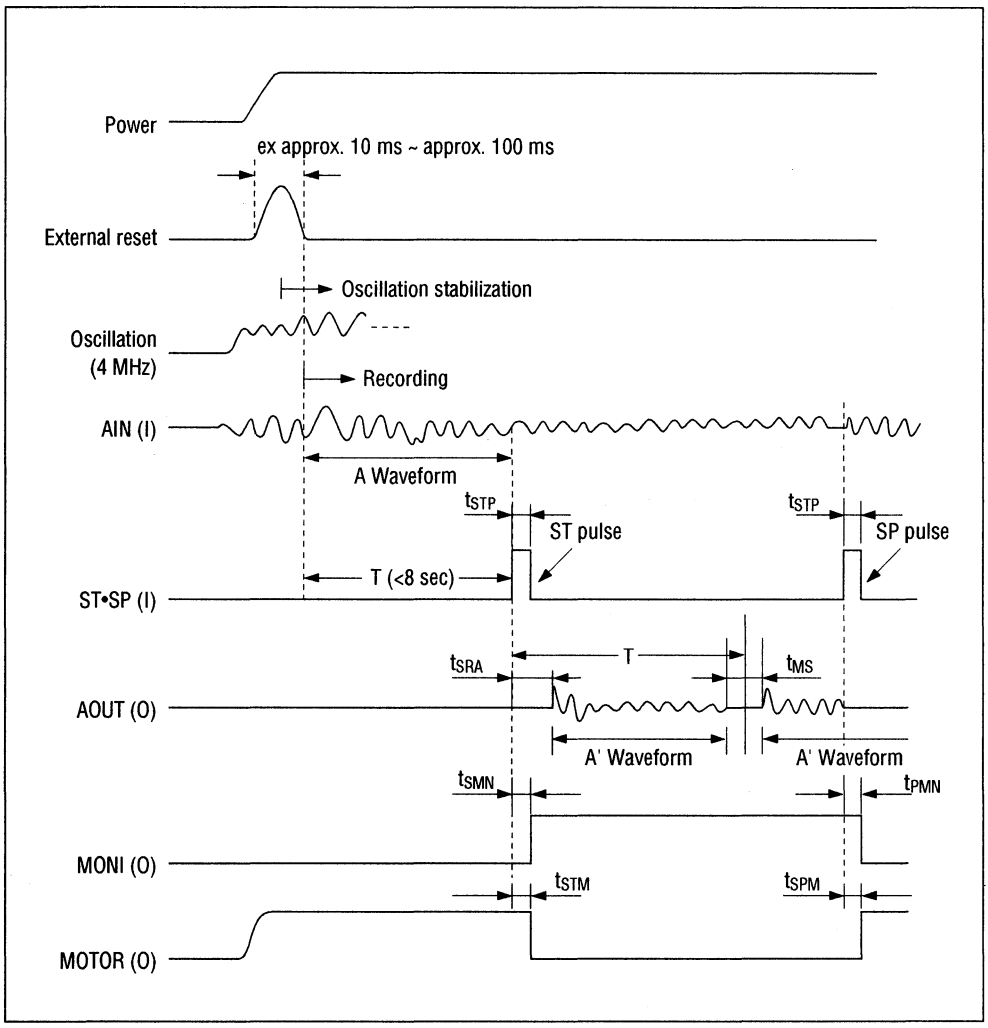
{ Sampling Frequency 8kHz
{ DRAM(256K bit) 2pcs

Basic Operation

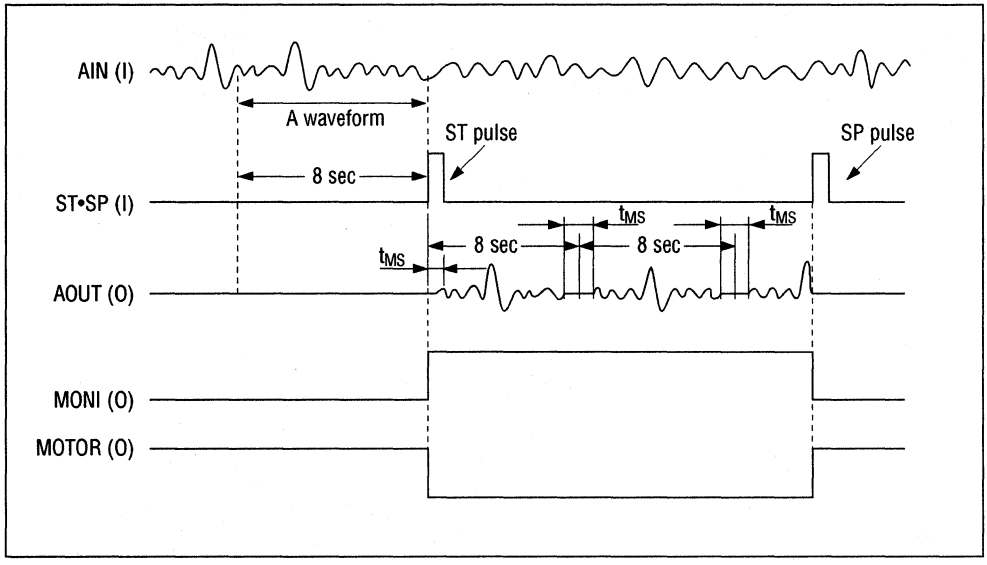
1. DEL/$\overline{\text{REP}}$="L" ..... REPEAT mode

1) After power is turned on, ST pulse is output within 8 sec.

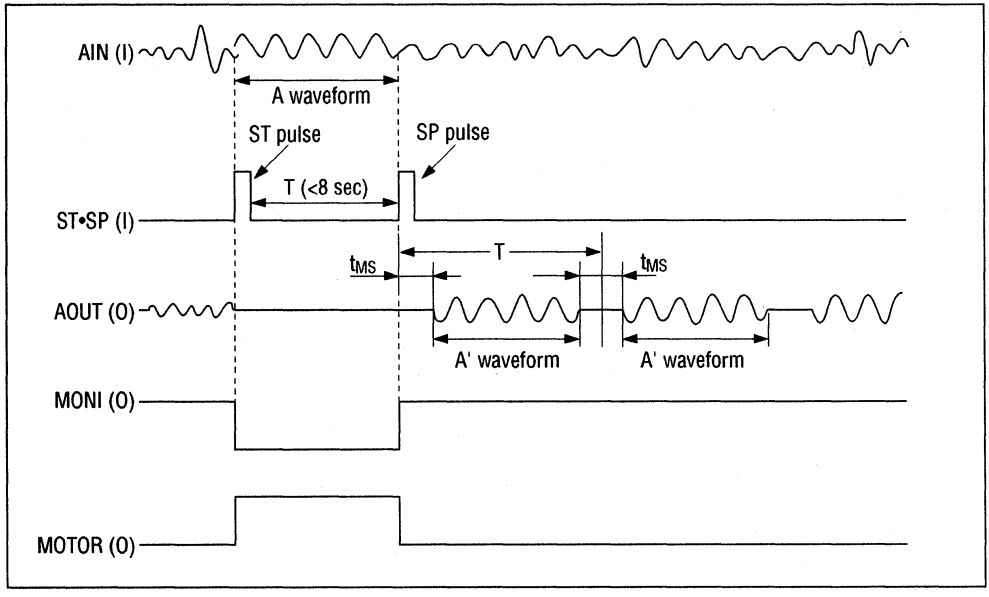
Basic Operation



2) After power is turned on, ST pulse is input 8 sec. later.



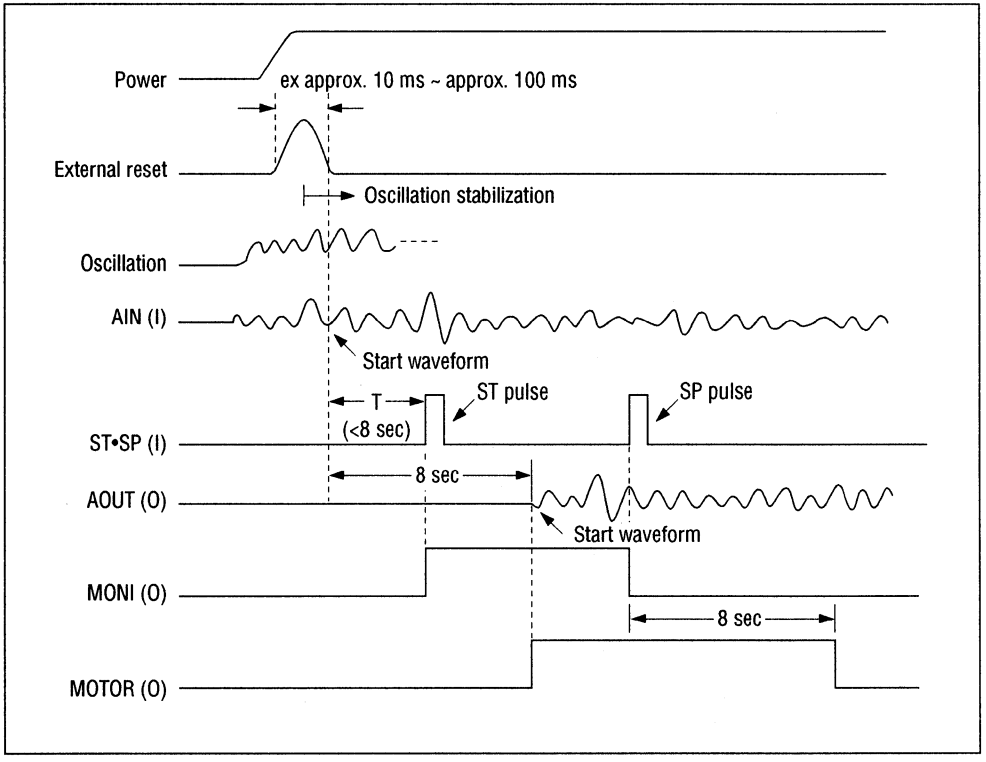
3) After inputting SP pulse, ST pulse is input within 8 sec.



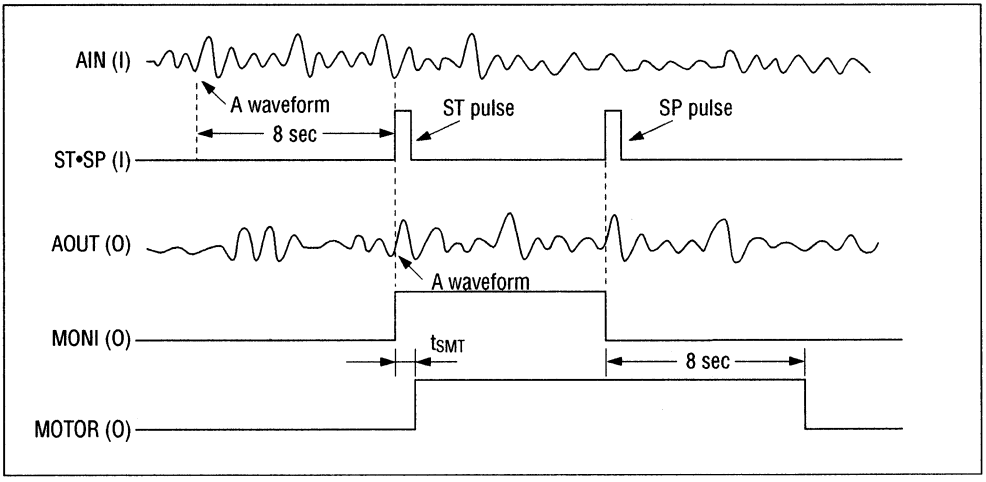
4) After inputting SP pulse, ST pulse is input 8 sec. later. Same as 2).

2. DEL/$\overline{\text{REP}}$="H" ..... DELAY mode

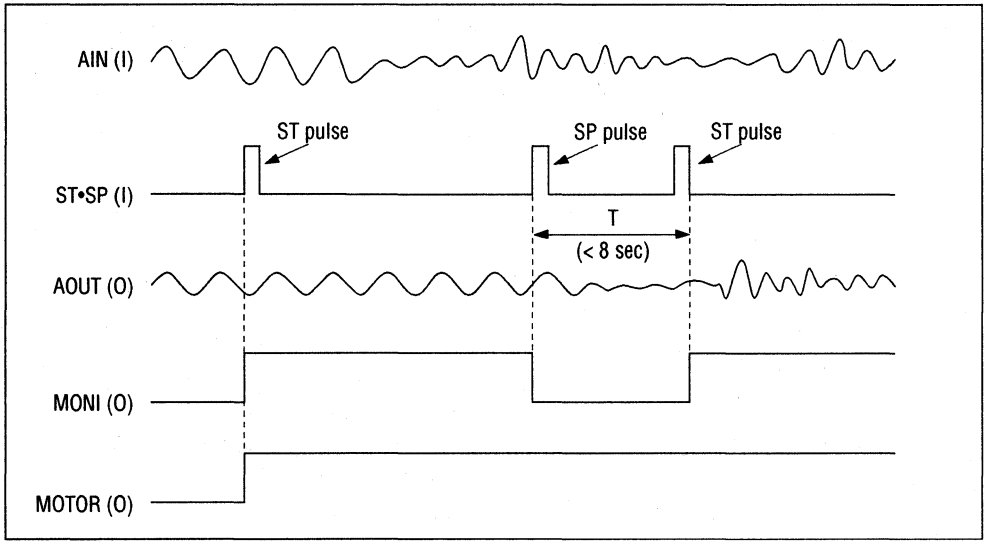
1) After power is turned on, ST pulse is input within 8 sec.



2) After powe is turned on, ST pulse is input 8 sec. later.



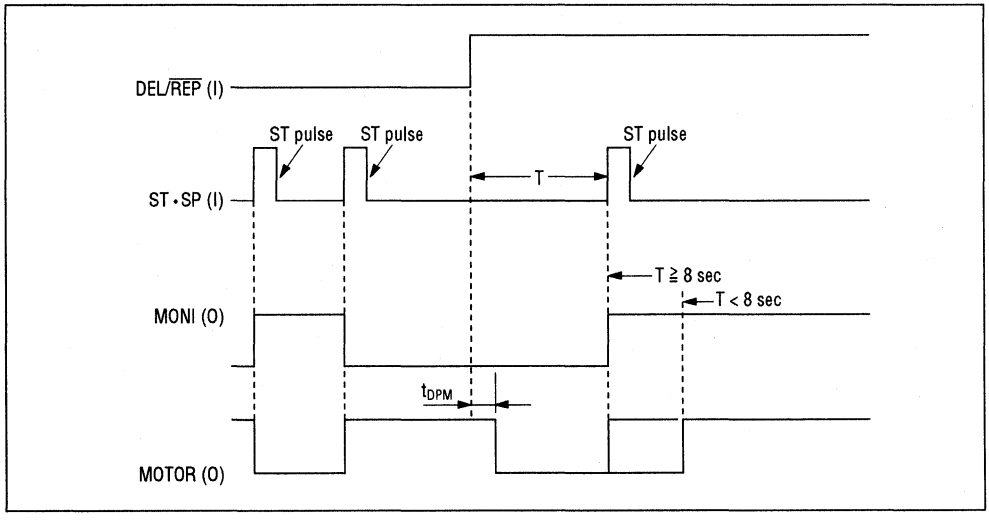
3) After SP pulse is input, ST pulse is input within 8 sec.



Change Operation during DEL/$\overline{\text{REP}}$

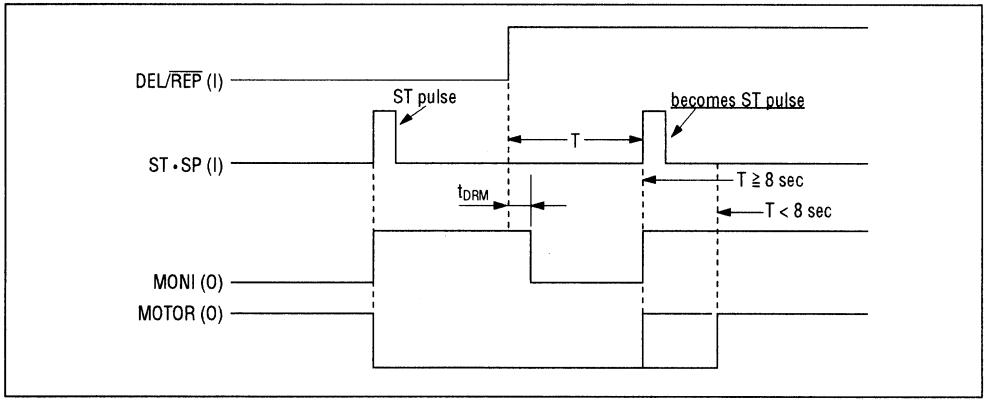
1. DEL/$\overline{\text{REP}}$="L" → "H"
   ..... from REPEAT mode
   to DELAY mode

1) Change operation is activated after SP pulse (before ST pulse)



Note 1: If T is 8 sec. or longer, MOTOR rises at the same time when ST pulse is input.
Note 2: If T is 8 sec. or shorter, MOTOR rises 8 seconds after DEL/$\overline{\text{REP}}$ is selected.

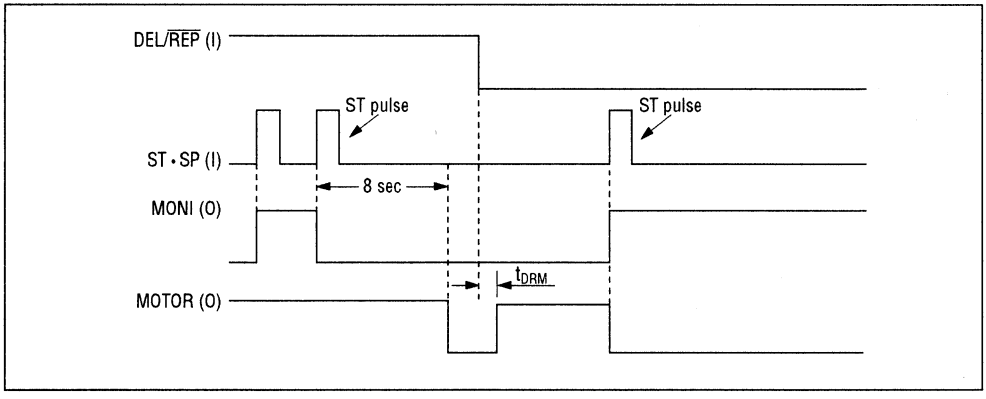
2) Change operation is activated after ST pulse (before SP pulse)



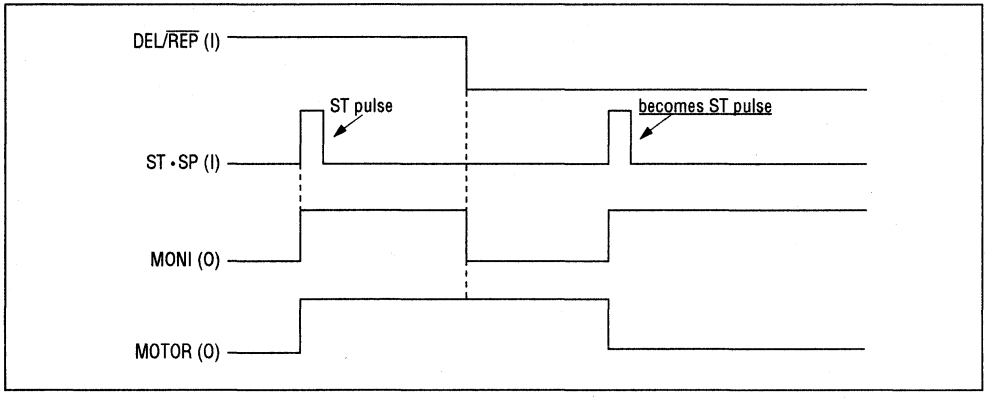
Note 1: If T is 8 sec. or longer, MOTOR rises at the same time when ST pulse is input.
Note 2: If T is 8 sec. or shorter, MOTOR rises 8 seconds after DEL/$\overline{\text{REP}}$ is selected.

2. DEL/$\overline{\text{REP}}$="L" → "H"
..... from REPEAT mode
to DELAY mode

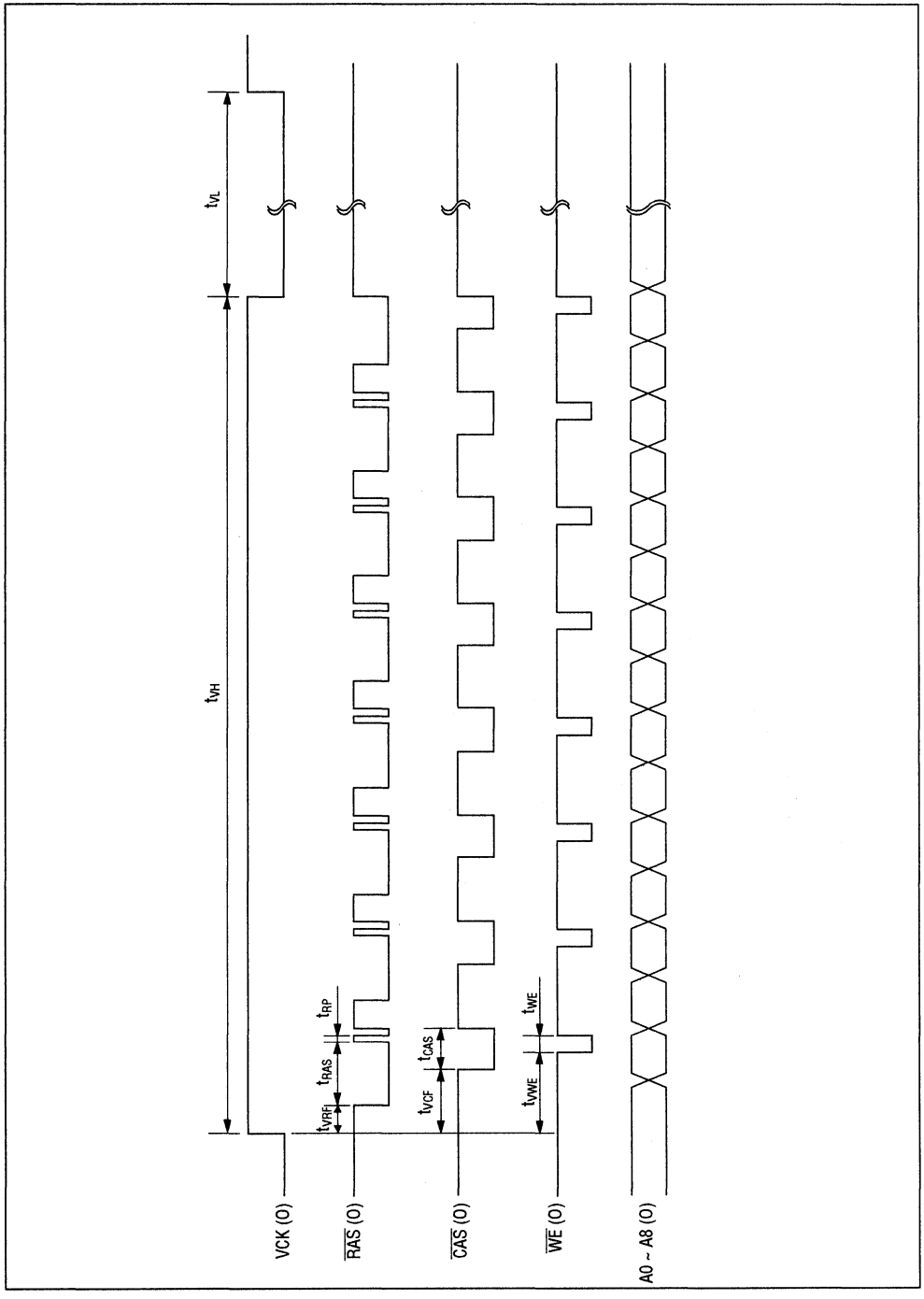
1) Change operation is activated after SP pulse (before ST pulse)



2) Change operation is activated after ST pulse (before SP pulse)



DRAM DRIVING TIMING



MSM6310 performs read/write and CAS before RAS refresh of voice data with the above timing (hidden refresh cycle).

PIN DESCRIPTION

Pin symbol	Pin No.	Function
A_0	40	Address outputs to the DRAM.
A_1	41	
A_2	42	
A_3	43	
A_4	1	
A_5	2	
A_6	3	
A_7	4	
A_8	5	
AIN	20	Analog input terminal. The external line level source, microphone, tape or similar is connected to this pin via adequate signal coupling circuits, that are matched to the pick up.
AMPO	19	The output of the input amplifier, which is usually bonded to FIL 1 I.
FIL1T	18	The direct access input to the internal low-pass filer. In case of external audio amplifier this is the input for the analog source. Usually, FIL 1 I is bonded to AMPO.
FIL1O	15	The output of the internal low-pass filter and at the same time the input of the internal ADC. Usually, this pin is left open.
DO	9	The serial data output to the data input of the external DRAMs.
DI	8	The serial data input from the data output of the external DRAMs.
DAO	12	The output of the internal DAC, which is usually bonded to FIL2I, when the internal filter is used.
FIL2I	14	The input of the internal playback LPF, receiving the signal from DAO.
AOUT	13	This is the terminal that provides the actual output of the regenerated analog waveform. The signal presented has passed the low-pass filter and is buffered.
FSS	26	On this input, the sampling frequency is selectable: H=f_{osc}/512, L=f_{osc}/1024.
RAMS	27	The level to this input informs the chip how many pieces of DRAM devices are externally connected. H=1, L=2.
ST•SP	30	When this chatter-free input receives a H pulse, the LSI starts replaying or stops the reproduction of the recorded analog source. This operation can be cancelled any time with another pulse to ST•SP. The input is internally pulled down. The LSI recognizes which is a START and which is a STOP pulse.
DEL/$\overline{\text{REP}}$	29	On this input the playback modes, delayed or repeated, are determined: H-delayed, L=repeated.
AC	33	The "all clear" input. When receiving H level, the internal circuitry is reset. Auto-reset is activated when power is engaged. See application circuit.
XT	31	The crystal connector input. In case of external supply, the source is input here.
$\overline{\text{XT}}$	32	The crystal connector output. It is to be left open, when the clock is supplied from external.

PIN DESCRIPTION

Pin symbol	Pin No.	Function
$\overline{WE}$	38	This output provides the write enable signal to the DRAMs in the recording mode.
$\overline{RAS}$	37	The row address strobe signal to the DRAMs.
$\overline{CAS1}$	36	The column address strobe signal to DRAM #1.
$\overline{CAS2}$	35	The column address strobe signal to DRAM #2.
MONI	7	Between the interval of two pulses to ST•SP (start and stop instructions), this output goes to H. When connected to a buffer and a LED, the active state of the LSI can be optically displayed.
MOTOR	6	This signal output can be used to control a tape motor or equivalent equipment controls.
VCK	10	The selected sampling frequency is output here eventual peripheral controlling purposes.
FCUTS	28	On this input the cut-off frequency of the LPF is selectable.
TEST1	25	This is an input used exclusively for factory testing and must be grounded to DGND in applications. The input is internally pulled down.
AVDD	16	The analog supply voltage input, nominally + 5 Volts DC.
DVDD	39	The digital supply voltage input, nominally + 5 Volts DC.
DVDD'	17	This pin must not be drained to feed successive circuits. It can be bonded to DVDD (#39)
AGND	23	Analog ground terminal, nominally 0 Volts.
DGND	24	Digital ground terminal, nominally 0 Volts.
SG	21	Signal ground output providing about VDD/2 level. Connect a capacitor of 47μF across SG and AGND.
SGC	22	Signal ground control input. To stabilize the signal ground, connect a capacitor of > 10μF across SGC and AGND.
NC	11,34,44	These pins must be left open. Do not wire to power sources, ground or signal lines.

FUNCTIONAL DESCRIPTION

LSI operation takes place in basically two modes, one is the DELAY mode, the other the REPEAT mode, selectable on terminal DEL/$\overline{REP}$. The modes cannot be referred to as RECORD and PLAYBACK modes as such, since both recording & playback occurs in the two modes.

The repeat mode denotes that recording of analog data (for the time the memory offers at the selected bit-rate), is repeated again and again until stopped intentionally.

The delay mode denotes that after every recording (for the time the memory offers at the selected bit-rate), the recorded contents is replayed until another recording commences. So, the subsequent recording is "delayed".

THE REPEAT MODE

When applying power or switching over from DELAY to REPEAT, the LSI automatically converts the connected analog input to PCM data and stores it in the external DRAM. When the analog input presence exceeds the available memory, the DRAM is rewritten from the beginning while the old contents are erased, and so on. The output MOTOR issues a H level during recording.

When a H active pulse is applied to ST•SP, the LSI automatically interprets it as a START pulse for the replay of the memory contents. Here, we are talking about the last actual recording, or rather re-recording. The replay of that recording is stopped with another pulse to ST•SP. When ST•SP is not served with a pulse after the memory time has elapsed, the replay is repeated until the pulse is applied. During replay the MOTOR output issues L.

Right after that pulse to ST•SP, the LSI changes the mode from replay back to recordings as described above.

THE DELAY MODE

When applying power or switching over from REPEAT to DELAY, the DRAM changes its read/write mode. The LSI then reads out old data and writes new data, thus the address count up is controlled.

Consequently, the analog data on AIN is recorded and played back immediately after the memory time has elapsed. The reproduced data is available on terminal on terminal AOUT. During this continuous change between recording and playback the output MOTOR issues a H level.

The procedure starts with a H active pulse to ST•SP and MOTOR goes H. The operation is stopped with another pulse to the same pin.. Then MOTOR changes from H to L and AOUT goes to VDD/2 level.

THE SAMPLING FREQUENCY

Nominally, the sampling frequencies are 4 and 8 kHz resulting in a bit rate of 32 kbit/s and 64 kbit/s, respectively. Since the sampling frequencies are submultiples of the clock frequency, other than the nominal values can be adjusted. The LSI is specified for a clock ranging from 4.0 to 8.2 MHz. When the input FSS is L, the divisor is f_{OSC}/512, when H, f_{OSC}/1024. Practically, the available sampling range is from 3.9 kHz to 16 kHz.

RECORDING & PLAYBACK TIMES

The available time is determined by the memory capacity and the sampling frequency selected: memory capacity/bit-rate.

RAMS	FSS = H	FSS = L
L	8.2 sec	16.4 sec
H	4.1 sec	8.2 sec

Where f_s is the sampling frequency and the bit number is 8.

EXTERNAL SOLUTIONS

For maximum application convenience, the MSM6310 provides the user with internal analog circuits to prepare the source signal, amplifier and low-pass filter. However, the internal portions can be by-passed to favor external solutions if desired. This applies to the amplifier or the low-pass filter or both. The internal converters cannot be omitted.

SIGNAL GROUND

For the analog signal processing, the LSI contains a signal ground generation circuit providing a signal ground, SG, at approximately VDD/2. This level is stabilized by two capacitors connected to the inputs SG and SGC (Signal ground control).

NOISE IMMUNITY

It is strictly recommended to make use of the individual power supply inputs and grounds.

Carefully separate analog and digital lines and bond them together at a carefully chosen system point. Avoid the proximity of the LSI to high speed digital systems. Also connect a by-pass capacitor across DVDD and DGND in close proximity to the LSI and other integrated active devices, including memories.

Quantization noise is conditioned by the AD-converter. Through the digitalization of the analog signal, every sampling point is expressed by a value. The limited repertoire of the ADC provides a vertical resolution of 8 bits, i.e., 256 numbers. At quantization intervals, equal to the intervals between two adjacent digital values, inaccuracies result through the limitation of available values...the source of quantization noise. An 8-bit ADC is as accurate as 20mV analog intervals.

In order to minimize the noise, the use of low pass filters is inevitable and OKI has designed-in a filter with optimum characteristics that suited to efficient reduction of the conversion-conditioned noise and to smooth the output waveform.

THE LPF CUT-OFF FREQUENCY & ATTENUATION

Like the sampling frequency, also the cut-off frequency of the internal low-pass filter changes as the oscillation frequency changes.

When the nominal value is selected (4.096 MHz), the filter cuts off as the following table shows:

Sampling Frequency	FCUTS = H	FCUTS = L
4.0kHz	2200Hz	1700Hz
8.0 kHz	3600Hz	2700Hz

The attenuation characteristic of the internal LPF is reflected by the table below:

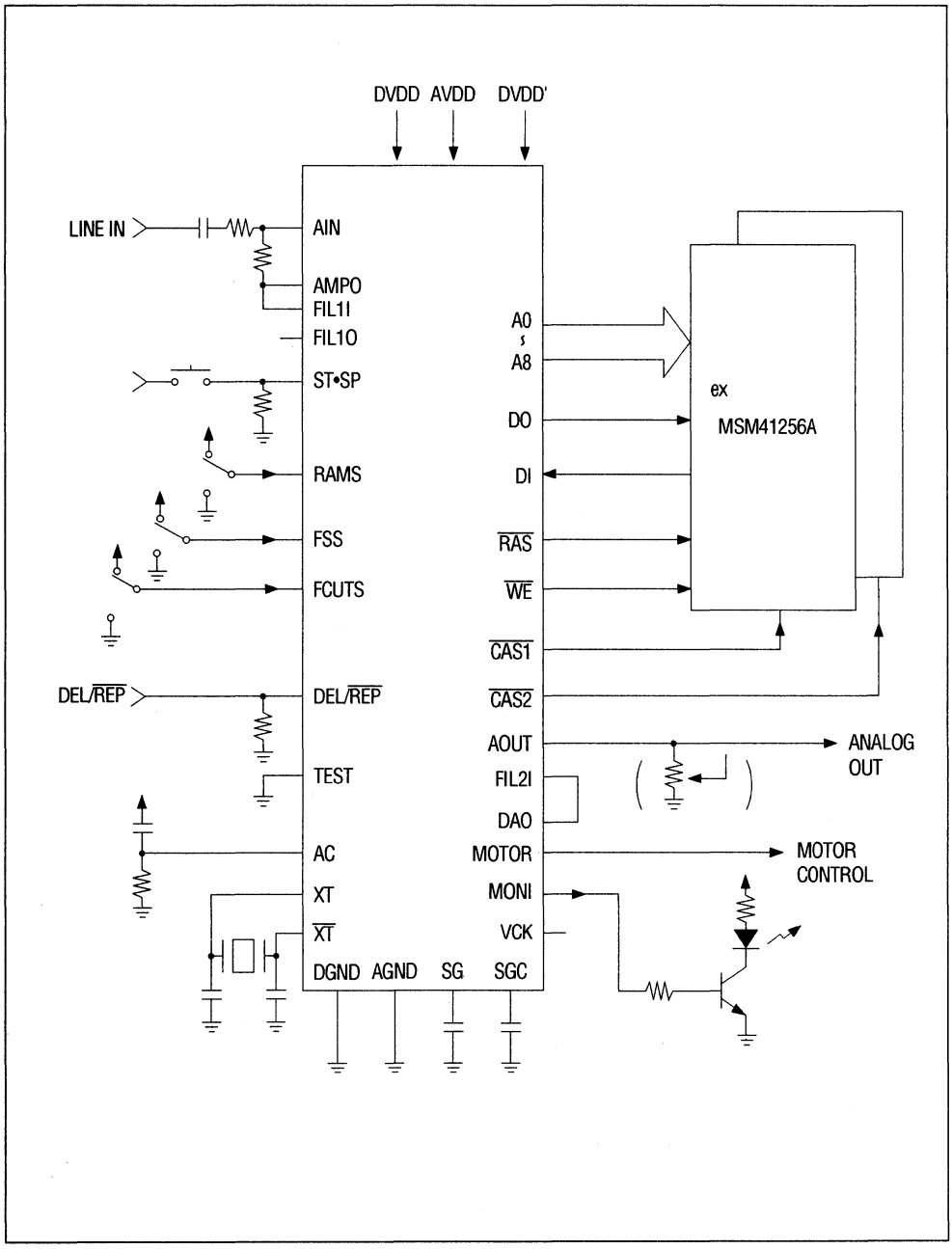
Band Width Frequency	Attenuation			Unit
	Min.	Typ.	Max.	
300~3400 Hz	-3	-	+3	dB
4000Hz	-	-	-3	dB
7500Hz	-	-	-25	dB

Measured at f_s = 8 kHz, VDD = 4.5~5.5V, Ta = 25°C, FCUTS = "L"

AMPLIFIER CHARACTERISTICS

AMPO maximum DC gain
..... 40 dB
AMPO minimum drive impedance
..... 200kΩ
AOUT minimum drive impedance
..... 50kΩ

APPLICATION CIRCUIT



OKI Semiconductor

MSM6388

ADPCM SOLID STATE RECORDER

GENERAL DESCRIPTION

The MSM6388 is a "solid-state recorder" LSI developed using ADPCM (Adaptive Differential Pulse Code Modulation) technology. When an external microphone, speaker driving amplifier, and OKI's original 1M-bit serial voice registers for ADPCM data storage are connected to the MSM6388, it can be used to record and play back voice or other sounds in a manner similar to that of a tape recorder.

FEATURES

- 4bit ADPCM
- Built-in 12bit A/D converter
- Built-in 12bit D/A converter
- Built-in microphone pre-amplifier
- Built-in low pass filter (Attenuation characteristics -40dB/oct)
- Serial voice register
  1Mbit serial voice register (MSM6389):
  Direct drive for 4 serial voice registers
  512Kbit serial voice register (MSM6587):
  Direct drive for 1 serial voice register
  256Kbit serial voice register (MSM6586):
  Direct drive for 1 serial voice register
- Serial Voice ROMs
  1Mbit serial voice ROM (MSM6595-XXX)
  2Mbit serial voice ROM (MSM6596-XXX)
  3Mbit serial voice ROM (MSM6597-XXX)
- Maximum recording time: 262 seconds (when the sampling frequency is 4.0kHz)
- Power supply voltage: 5 V only
- 44 pin V 1 plastic QFP (QFP44-P-910-V1K)

(WHEN USED AS A STANDALONE LSI)

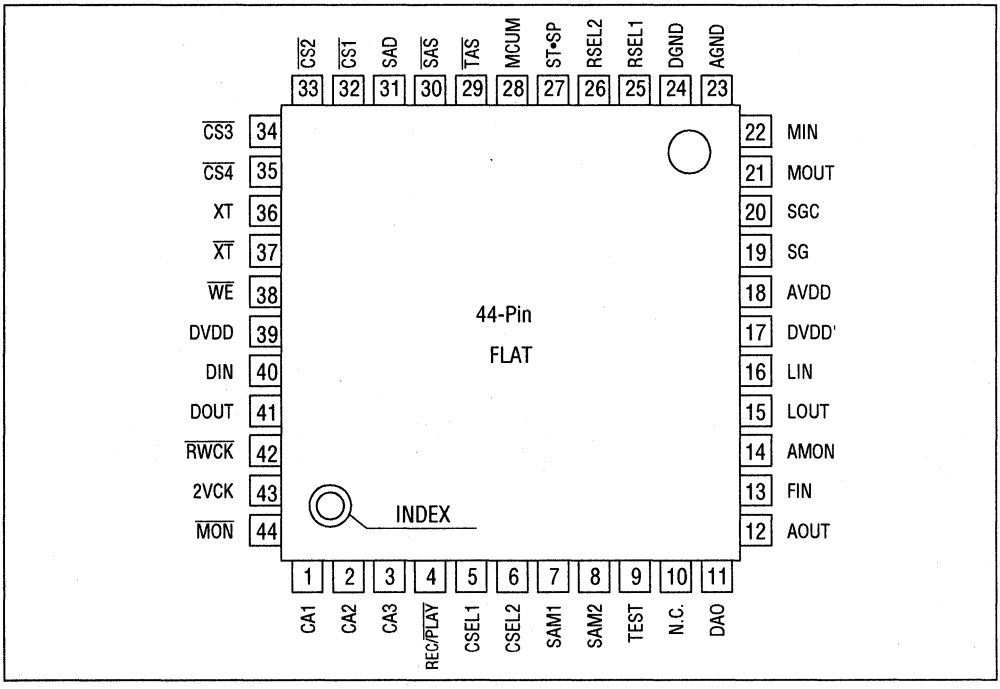
- Oscillator frequency:
  1.5MHz ~ 4MHz
- Sampling frequencies:
  5.2, 5.9, 6.7kHz
  (when the oscillator operates at 1.5MHz)
  3.9, 6.9, 7.8, 8.9 kHz
  (when the oscillator operates at 2.0MHz)
  7.8, 13.9, 15.6kHz
  (when the oscillator operates at 4.0MHz)
- Number of phrases to be recorded
  When one, two, or four serial voice registers are connected, one, two, four or eight phrases can be selected. When three serial voice registers are connected, one, two, three, or six phrases can be selected.
  For the maximum recording time of each channel, the time divided by the number of phrases shall be assigned.

(WHEN INTERFACED WITH A MICRO-CONTROLLER)

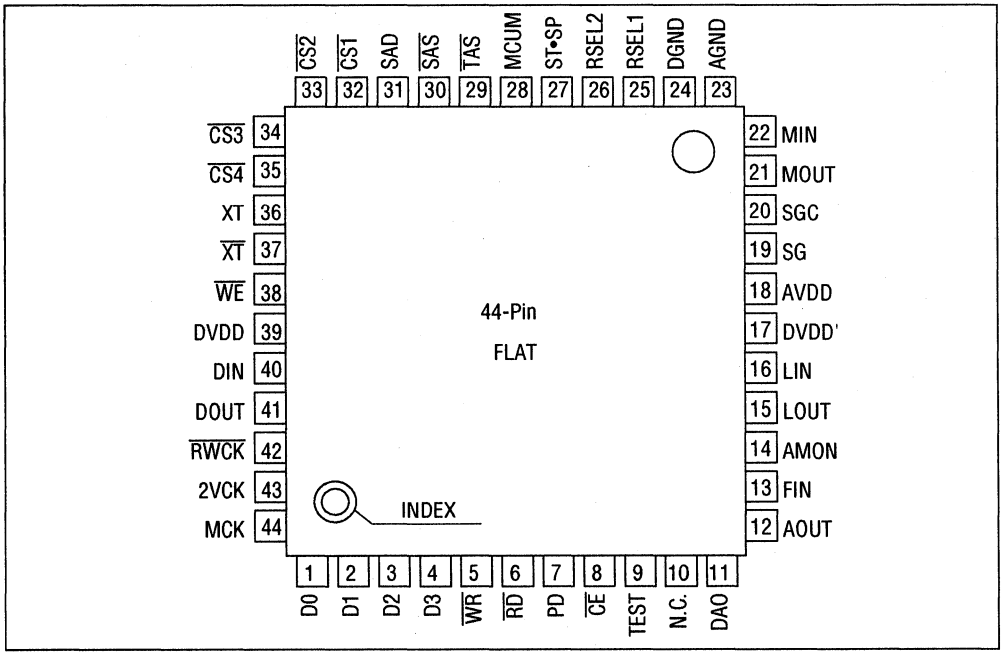
- Oscillator frequency:
  1.5MHz ~ 4MHz
  (when a serial voice register is used)
  1.5MHz~ 8MHz
  (when other memories are used)
- Sampling frequencies:
  3.2kHz ~ 16kHz
  (when a serial voice register is used)
  2.9kHz ~ 32kHz
  (when the other memories are used)
  2.6, 2.9, 3.3, 5.2, 5.9, 6.7kHz
  (when the oscillator operates at 1.5MHz)
  3.5, 3.9, 4.5, 6.9, 7.8, 8.9kHz
  (when the oscillator operates at 2.0MHz)
  6.9, 7.8, 8.9, 13.9, 15.6, 17.8kHz
  (when the oscillator operates at 4.0MHz)
- Number of phrases to be recorded
  To be controlled externally
  The maximum recording time at each channel can be set freely.
- 44 pin V1 plastic QFP (QFP44-P-910-V1K)

PIN LAYOUT

- Stand-alone mode (MCUM pin = "L")

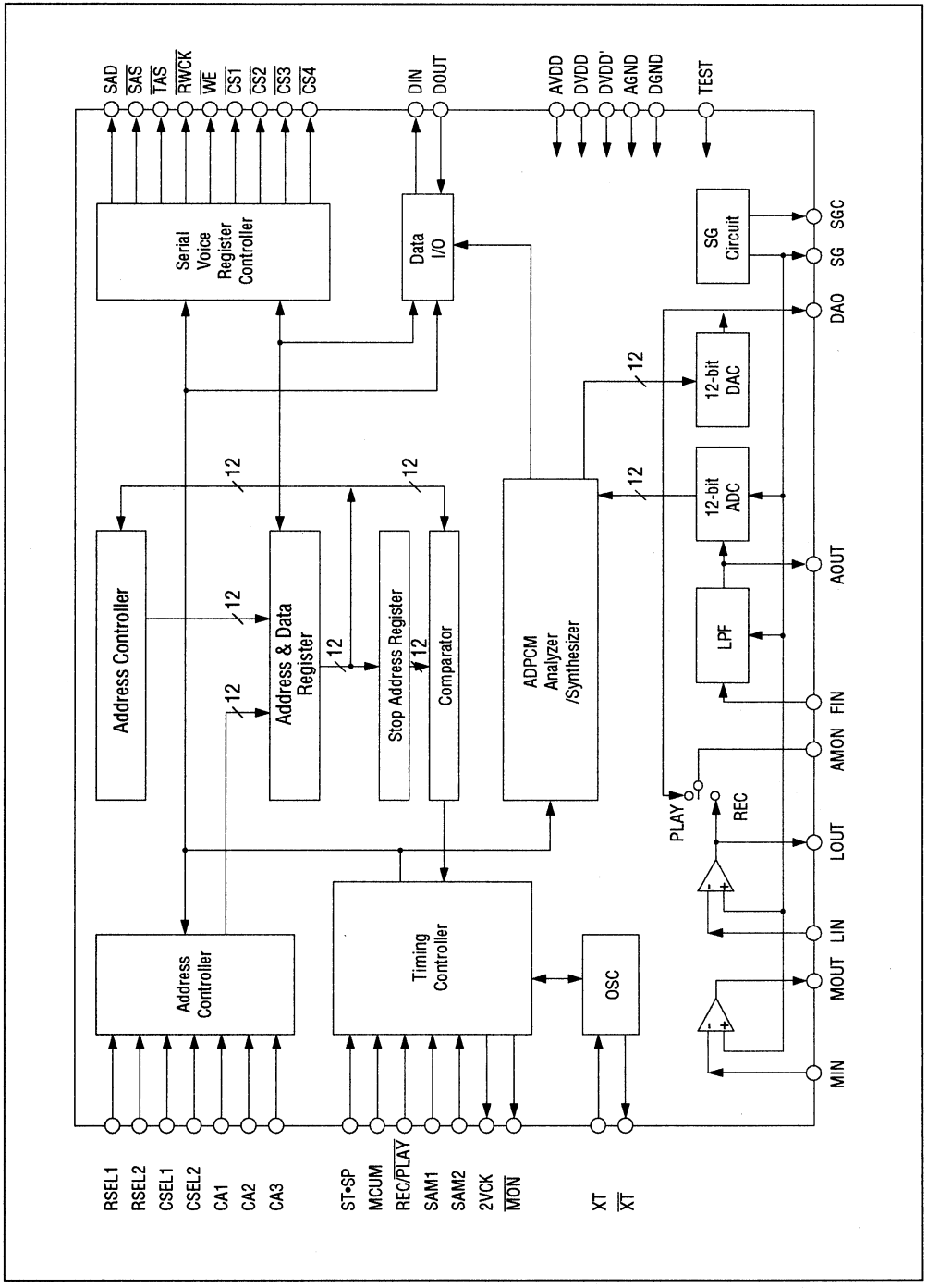


- Microcontroller interface mode (MCUM pin "H")

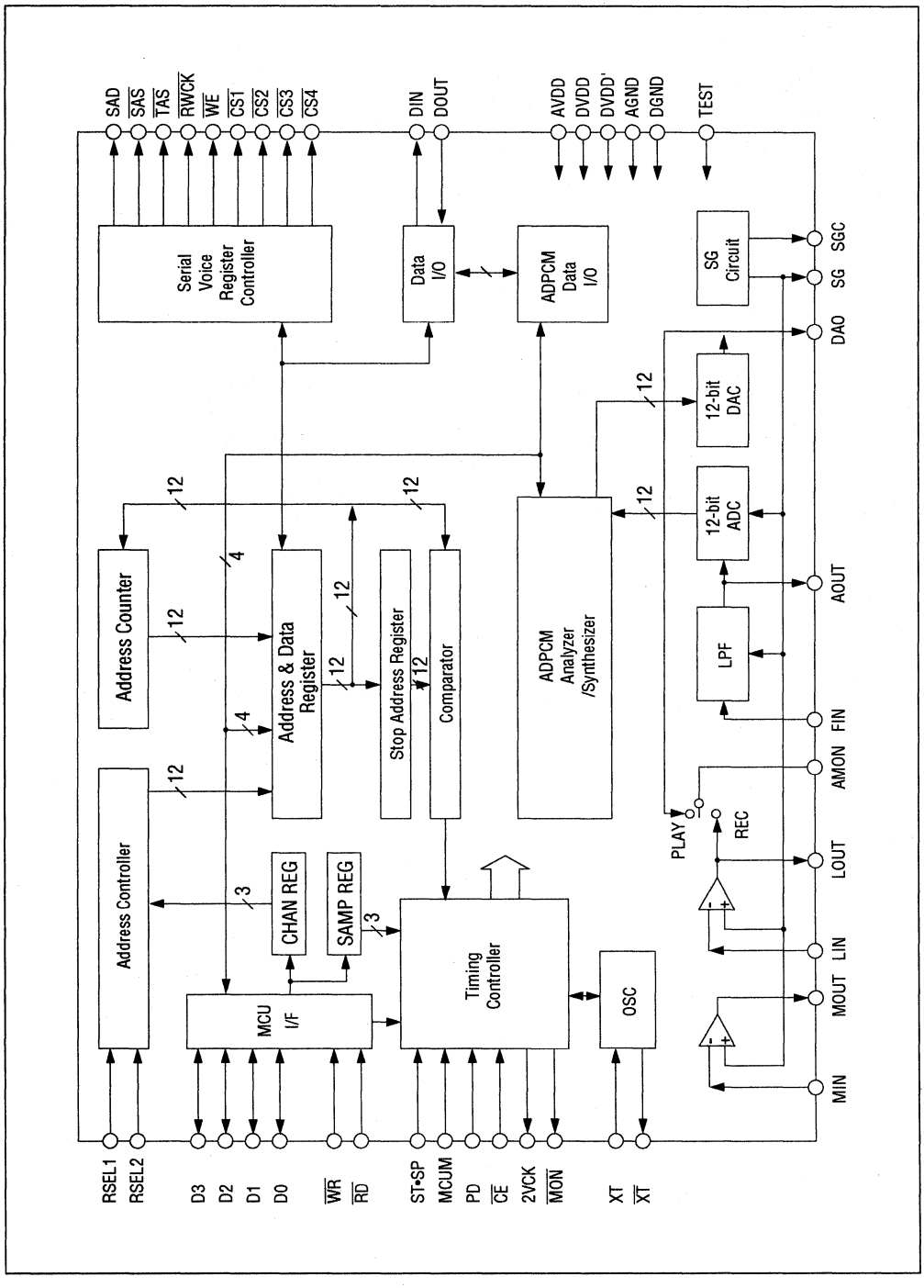


Note: Leave the NC pin open.

CIRCUIT DIAGRAM (Stand-alone application)



CIRCUIT DIAGRAM (microcontroller interface application)



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Range

Item	Symbol	Conditions	Range	Unit
Power supply voltage	VDD	DGND = AGND = 0V	+3.5 ~ +5.5	V
Operating temperature range	T_{op}	—	−40 ~ +85	°C
Oscillator frequency	f_{OSC}	—	1.5 ~ 8	MHz

• DC Current Characteristics

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage (Note 1)	V_{IH1}	—	3.6	—	—	V
High input voltage (Note 2)	V_{IH2}	—	0.8×VDD	—	—	V
Low input voltage (Note 1)	V_{IL1}	—	—	—	0.8	V
Low input voltage (Note 2)	V_{IL2}	—	—	—	0.8	V
High output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	V
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
High input current (Note 3)	I_{IH1}	V_{IH} = VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH} = VDD	—	—	20	μA
High input current (Note 4)	I_{IH3}	V_{IH} = VDD	20	—	400	μA
Low input current (Note 1)	I_{IL1}	V_{IL} = GND	−10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL} = GND	−20	—	—	μA
Operating current (1)	I_{DD}	f_{OSC} = 4.0MHz, without load	—	5	10	mA
Operating current (2)	I_{PD}	At power down, without load	—	—	10	μA

Note 1: Applies to the input pins excluding the XT pins.
Note 2: Applies to the XT pin.
Note 3: Applies to the pins not connected to pull-down resistors and excluding the XT pin.
Note 4: Applies to the pins connected to pull-down resistors and excluding the XT pin.

• Analog Characteristics

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Relative DA output error	$\|V_{DAE}\|$	Under no load	—	—	10	mV
DA output impedance	R_{DAO}	—	12	20	28	kΩ
Fin input voltage	V_{FIN}	—	1	—	VDD-1	V
Fin input impedance	R_{FIN}	—	1	—	—	MΩ
Operational amplifier open loop gain	G_{OP}	f_{IN} = 0 ~ 4kHz	40	—	—	dB
Operational amplifier input impedance	R_{INA}	—	1	—	—	MΩ
Operational amplifier load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ

• A.C. Characteristics

1. Stand-alone Application

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C, f_{OSC}=2.048MHz, and f_{sam}=8.0kHz)

Item		Symbol	Min.	Typ.	Max.	Unit
ST•SP pulse width	*	t_{STP}	70	—	—	ms
$\overline{MON}$ clock output time during recording	*	t_{ALW}	—	4	—	S
$\overline{MON}$ clock cycle during recording	*	t_{ALC}	—	256	—	ms
Time before starting record or playback after start pulse input	*	t_{ANA}	—	260	—	ms
Time required for AOUT/DAOUT output to reach 1/2 VDD from GND level	*	t_{DAR}	—	44	—	ms
Time required from the end of playback to power down state	*	t_{DAF}	—	128	—	ms
Time required for voice to be output again during a repeated playback	*	t_{MS}	—	1	—	ms

Note: * Duration of items with "*" is proportional to the cycle of the sampling frequency f_{sam}.

2. Microcontroller Interface Application

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=–40~+85°C, f_{OSC}=2.048MHz, and f_{sam}=8.0kHz)

Item		Symbol	Min.	Typ.	Max.	Unit
PD pulse width		t_{PP}	2	—	—	µs
Time from PD release to $\overline{WR}$ pulse input (Note 2)		t_{PDW1}	10	—	—	ms
		t_{PDW2}	2	—	—	µs
$\overline{RD}$ pulse width		t_{RR}	200	—	—	ns
$\overline{CE}$ setup and hold times to $\overline{RD}$		t_{CR}	50	—	—	ns
Time from $\overline{RD}$ fall to data valid		t_{DRE}	—	60	150	ns
Time from $\overline{RD}$ rise to data float		t_{DRF}	—	40	90	ns
$\overline{WR}$ pulse width		t_{WW}	200	—	—	ns
$\overline{CE}$ setup and hold times to $\overline{WR}$		t_{CW}	50	—	—	ns
Data setup time to $\overline{WR}$ rise		t_{DWS}	100	—	—	ns
Data hold time to $\overline{WR}$ rise	*	t_{DWH}	30	—	—	ns
$\overline{RD}$ and $\overline{WR}$ disable time	*	t_{DRW}	250	—	—	ns
2VCK "H" level time	*	t_{VH}	—	125	—	µs
2VCK "L" level time	*	t_{VL}	—	125	—	µs
MCK "H" level time	*	t_{MH}	—	62.5	—	µs
MCK "L" level time		t_{ML}	—	62.5	—	µs
Time required from 2VCK rise to MCK rise		t_{VM}	—	23.4	—	µs
Time required from MCK rise to the rise of the first shot of $\overline{RD}$ and $\overline{WR}$ pulse	*	t_{RW1}	250	—	—	ns
Time required from MCK rise to the rise of the second shot of $\overline{RD}$ and $\overline{WR}$ pulse		t_{RW2}	—	—	62.5	µs

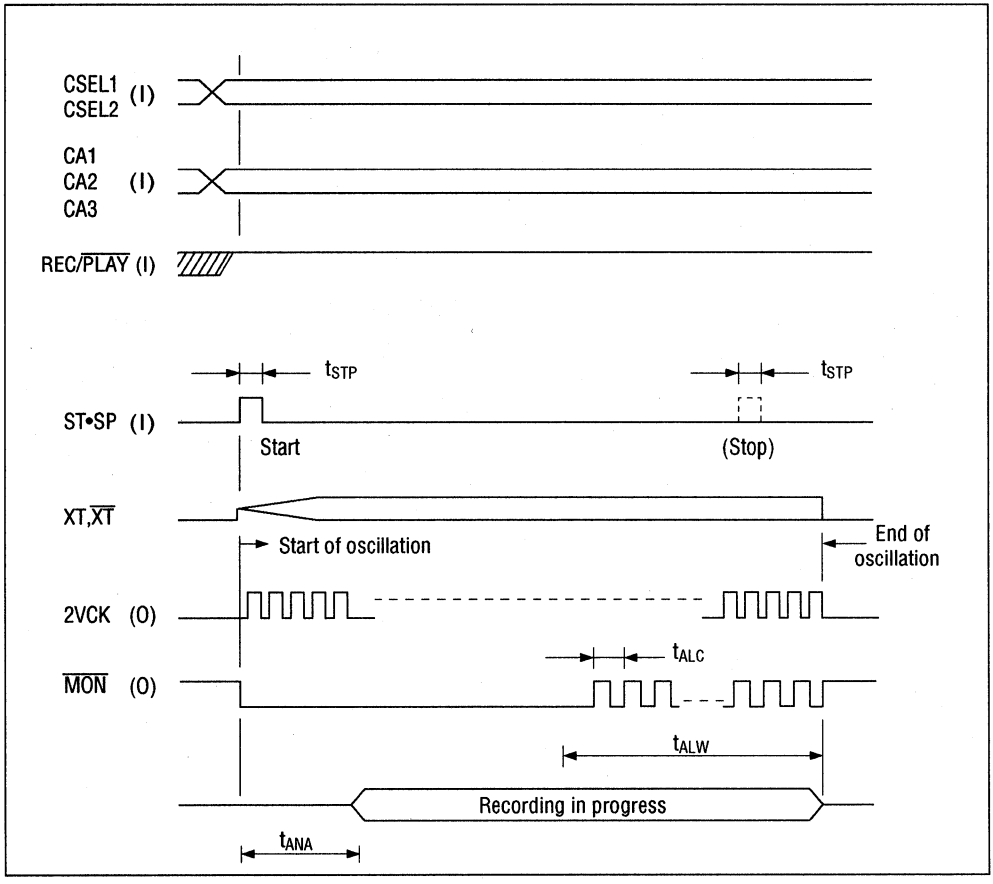
Note 1: * Duration of items marked with "*" is proportionate to the cycle of the sampling frequency f_{sam}.

Note 2: The oscillation stable time is added to t_{PDW1}.
The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a ms for ceramic oscillators.

TIMING CHARTS

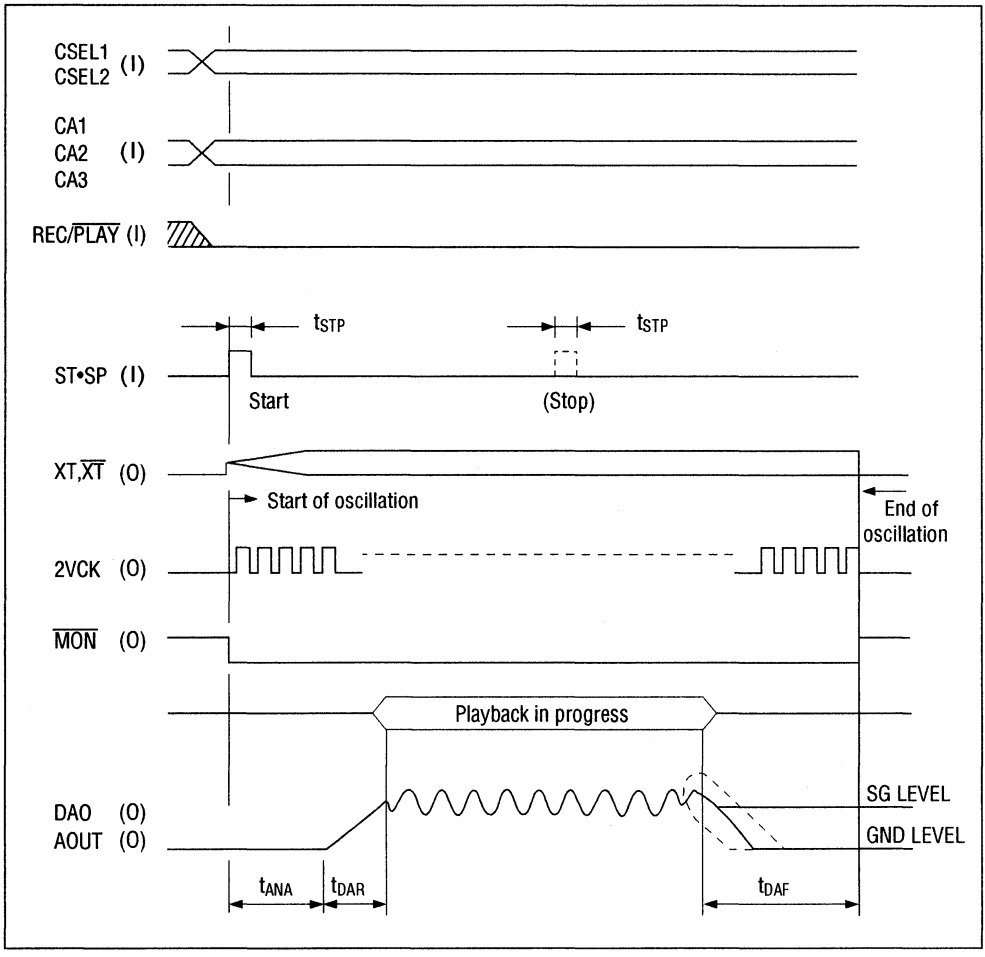
- **Standalone Application**

1. Recording timing

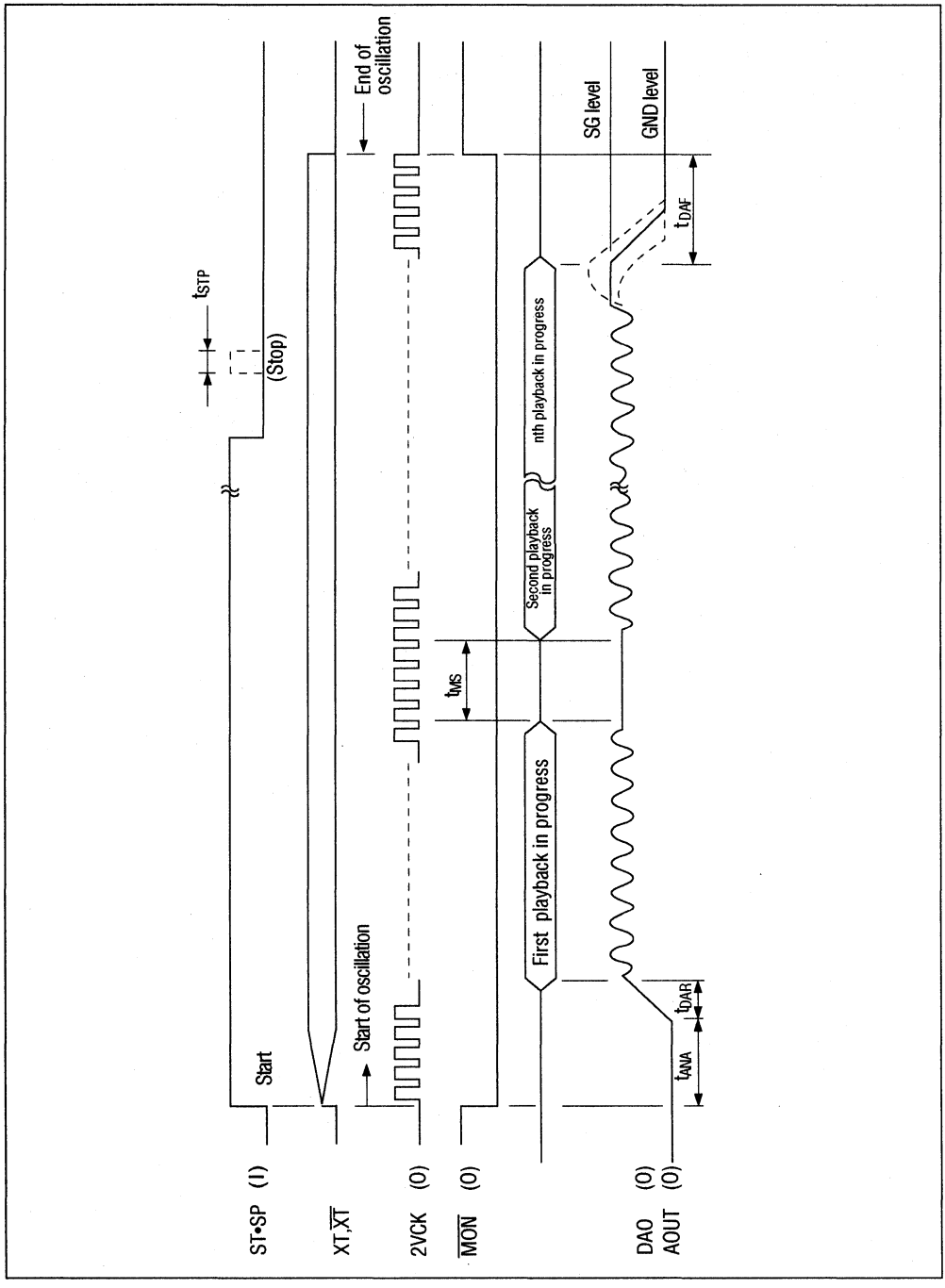


Note: When the remaining capacity of available memory of the selected channels falls to 128K-bit (last four seconds) during recording, a 4Hz clock is output from the $\overline{MON}$ pin. (f_{sam}=8kHz)

2. Playback Timing



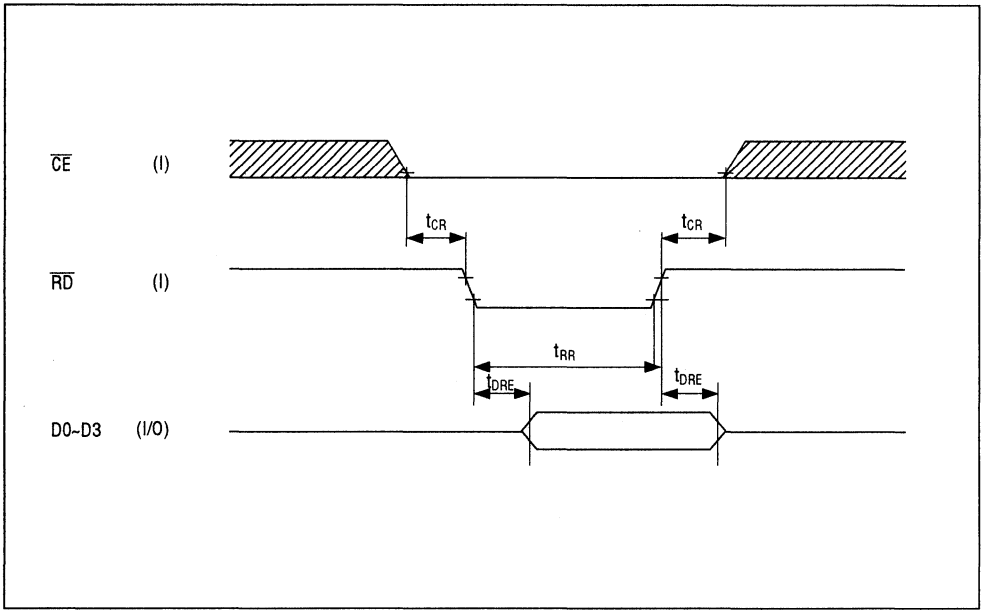
3. Repetitive playback timing



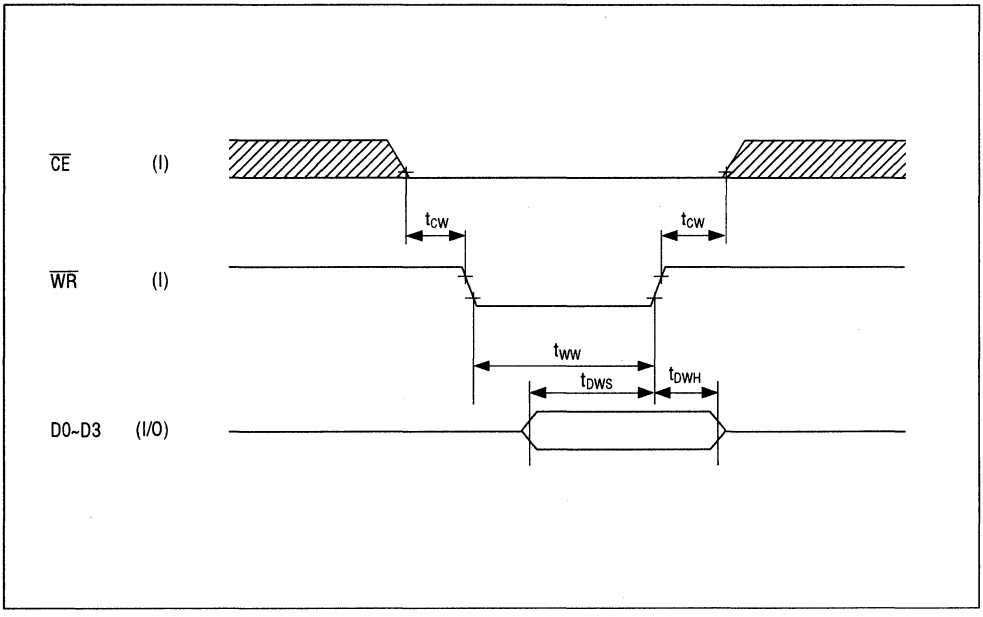
Note: Playback is peformed repeatedly while the ST•SP pin is maintained at the high level. When the pin goes low then a Stop pulse is input or playback proceeds up to the end of the channel memory and is stopped.

• **Microcontroller interface application**

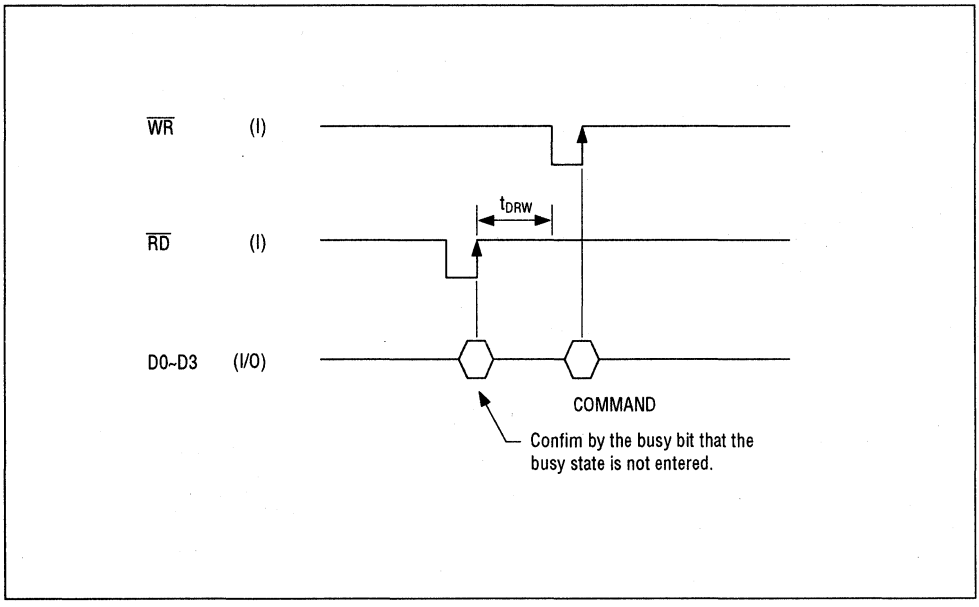
1. Data Read ($\overline{RD}$ pulse)



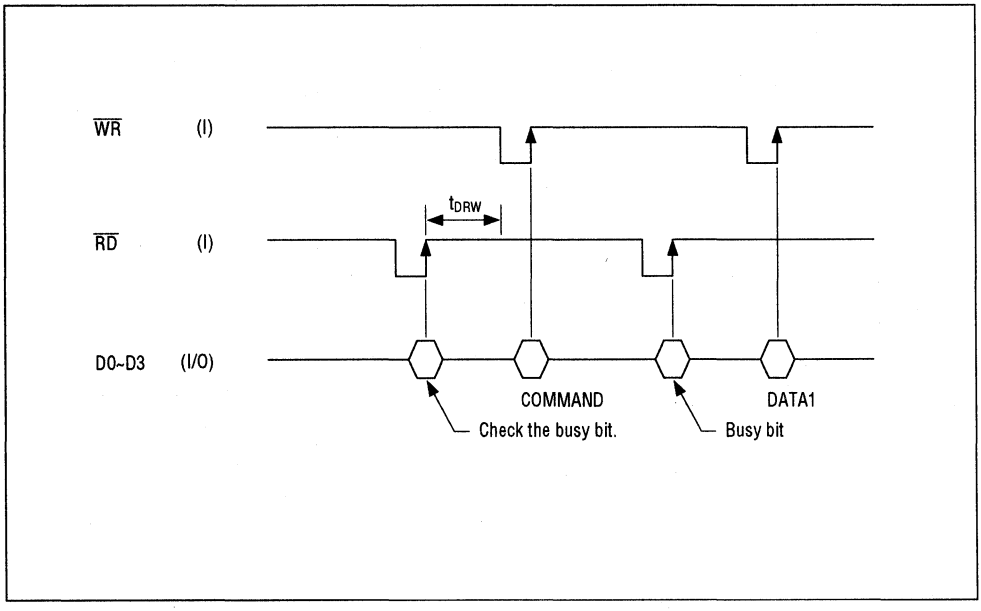
2. Data Write ($\overline{WR}$ pulse)



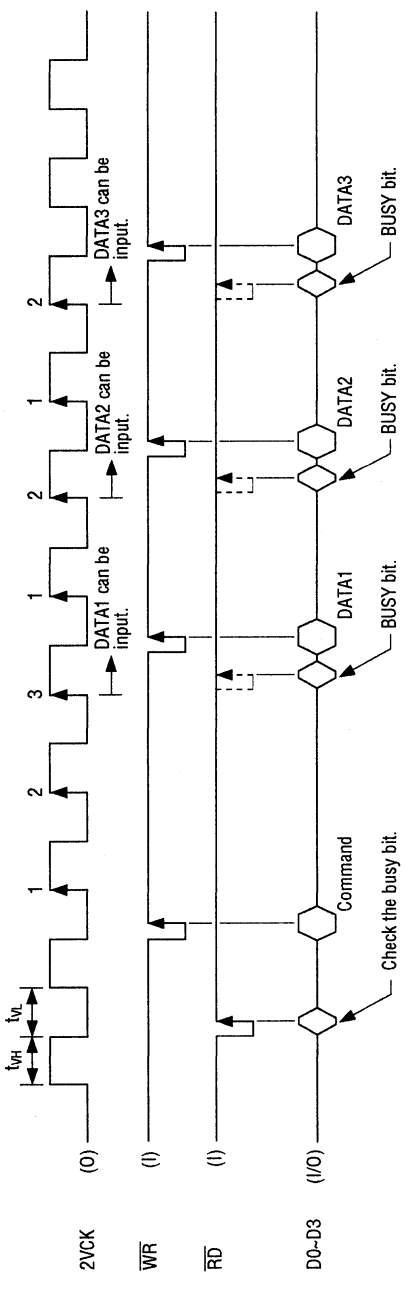
3. How to Input One-nibble Commands, NOP, INIT, PLAY, REC, START and STOP



4. How to Input Two-nibble Commands, SAMP and CHAN



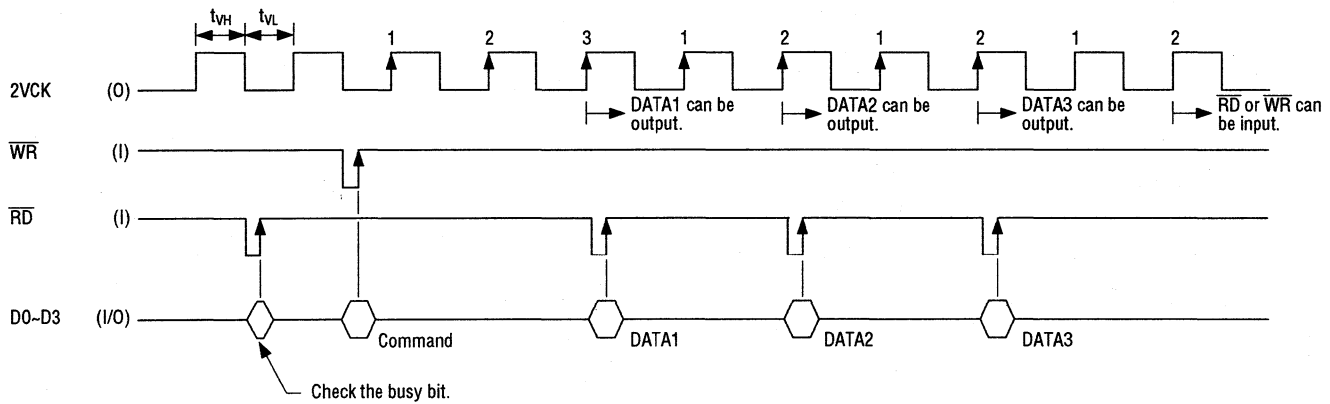
5. How to Enter STWR and SPWR Commands



1. Before entering a command, check the busy bit of the status register to see that the busy state is not entered.
2. Again make sure that the busy state is not entered by performing both A & B then eneter DATA1 to DATA3.

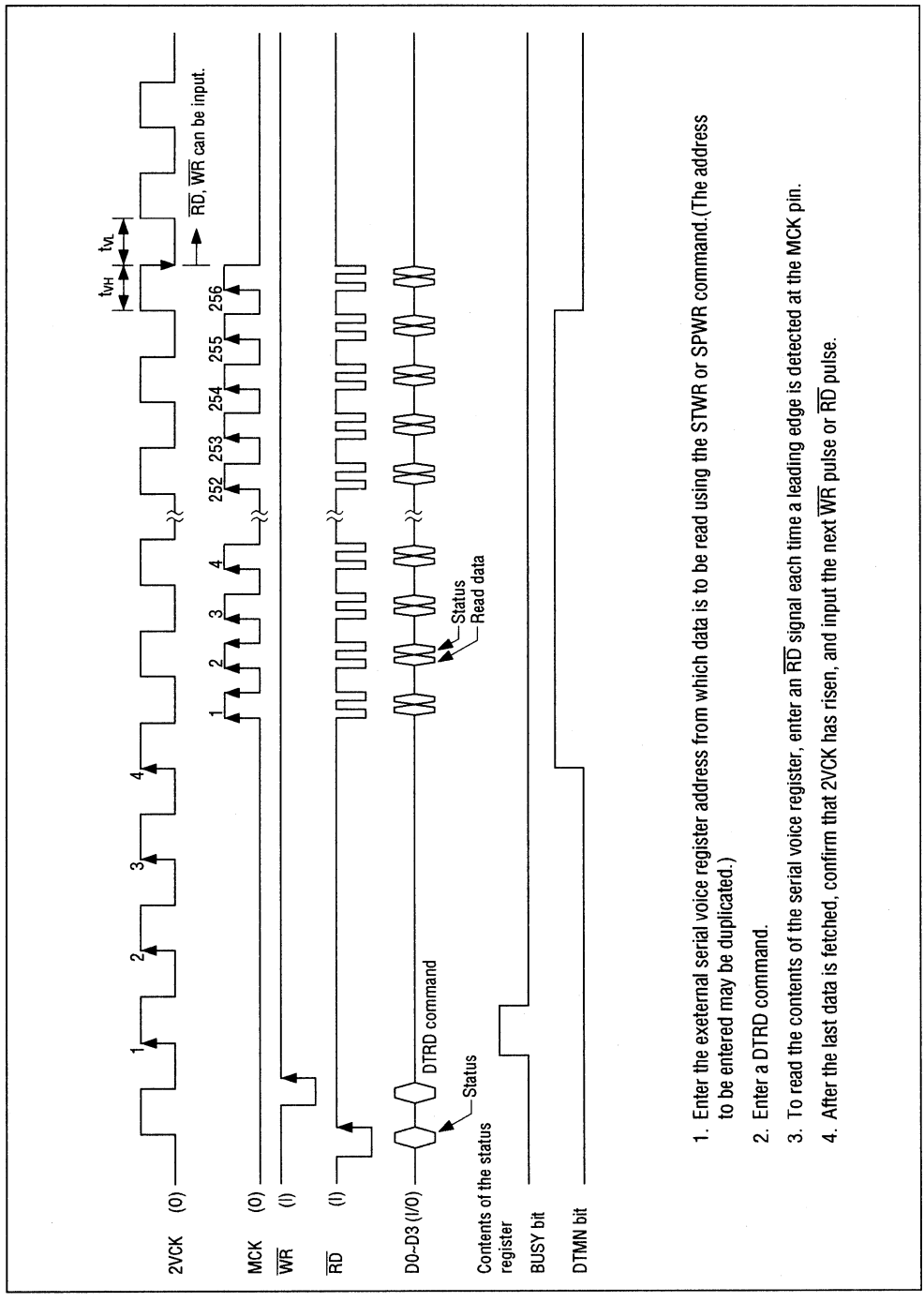
   A) Make sure that the 2VCK pin goes high at least three times(twice when DATA2 and DATA3 are to be entered) after a $\overline{WR}$ pulse is input, then input the next $\overline{WR}$ pulse.

   B) Check the busy bit of the status register to see that the busy state is not entered, then input the next $\overline{WR}$ pulse.



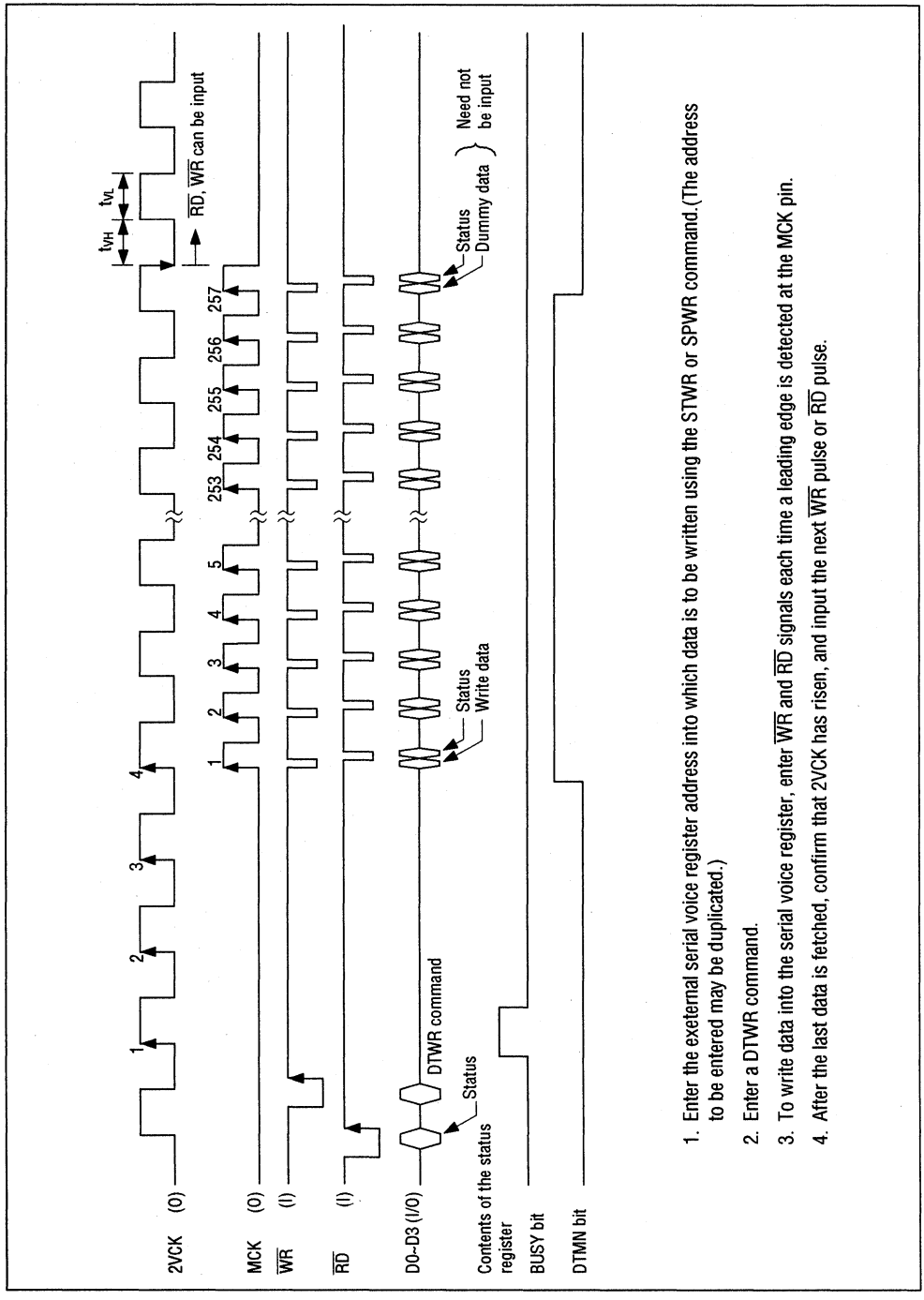
1. Before entering a command, check the busy bit of the status register to see that the busy state is not entered.
2. Then read DATA1 to DATA3 by the following ways :
   - Make sure that the 2VCK pin goes high at least three times then enter a $\overline{WR}$ pulse to read DATA1. To read DATA2 or DATA3, make sure that the 2VCK pin goes high at least twice after the last RD pulse is input then input the next $\overline{RD}$ pulse.
3. After reading DATA3, make sure that the 2VCK pin goes high at least twice then input the next $\overline{WR}$ or $\overline{RD}$ pulse.

7. How to Read Data from a Serial Voice Register Using a DTRD Command



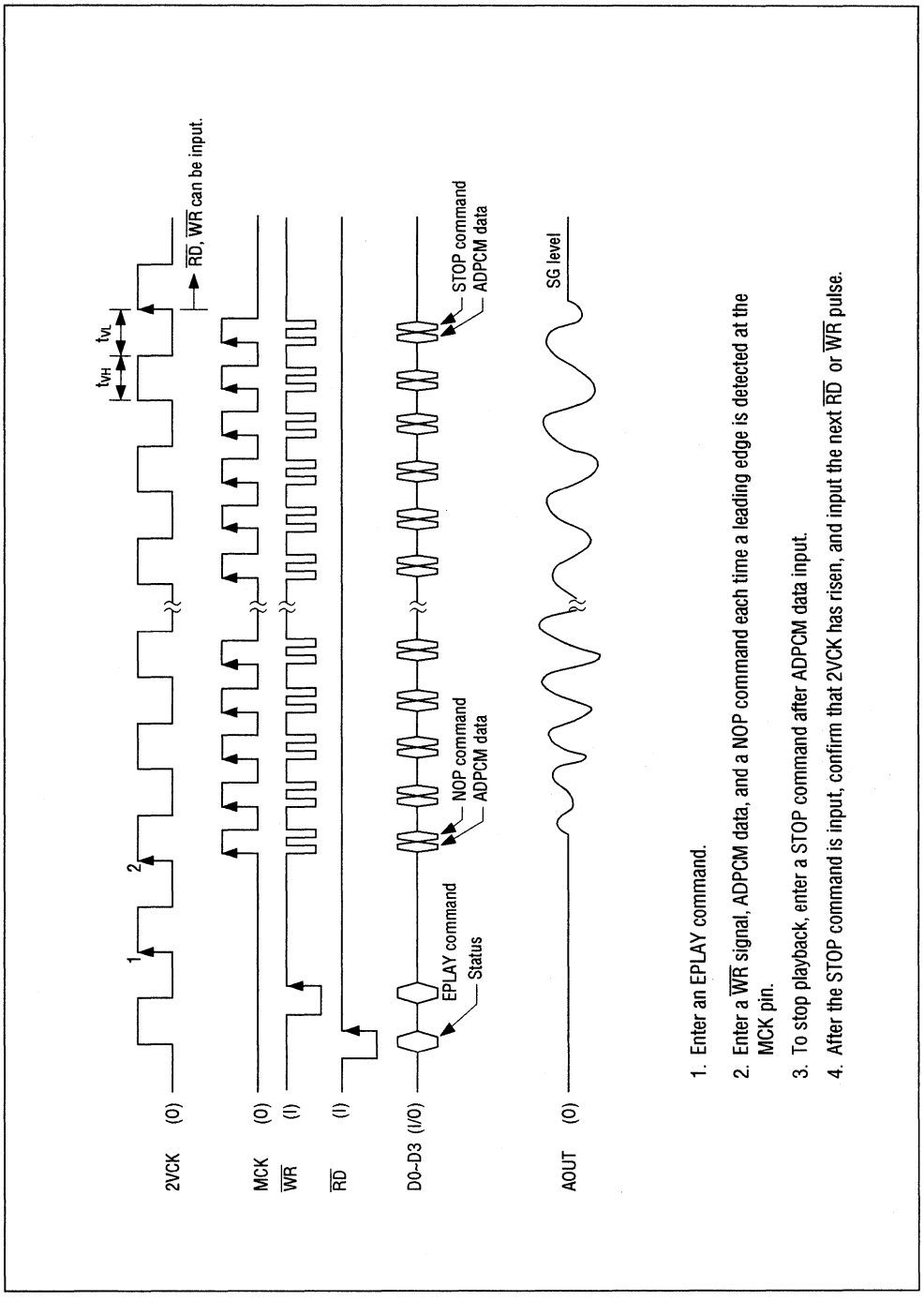
1. Enter the exeternal serial voice register address from which data is to be read using the STWR or SPWR command.(The address to be entered may be duplicated.)
2. Enter a DTRD command.
3. To read the contents of the serial voice register, enter an $\overline{RD}$ signal each time a leading edge is detected at the MCK pin.
4. After the last data is fetched, confirm that 2VCK has risen, and input the next $\overline{WR}$ pulse or $\overline{RD}$ pulse.

8. How to Write Data into a Serial Voice Register Using a DTWR Command



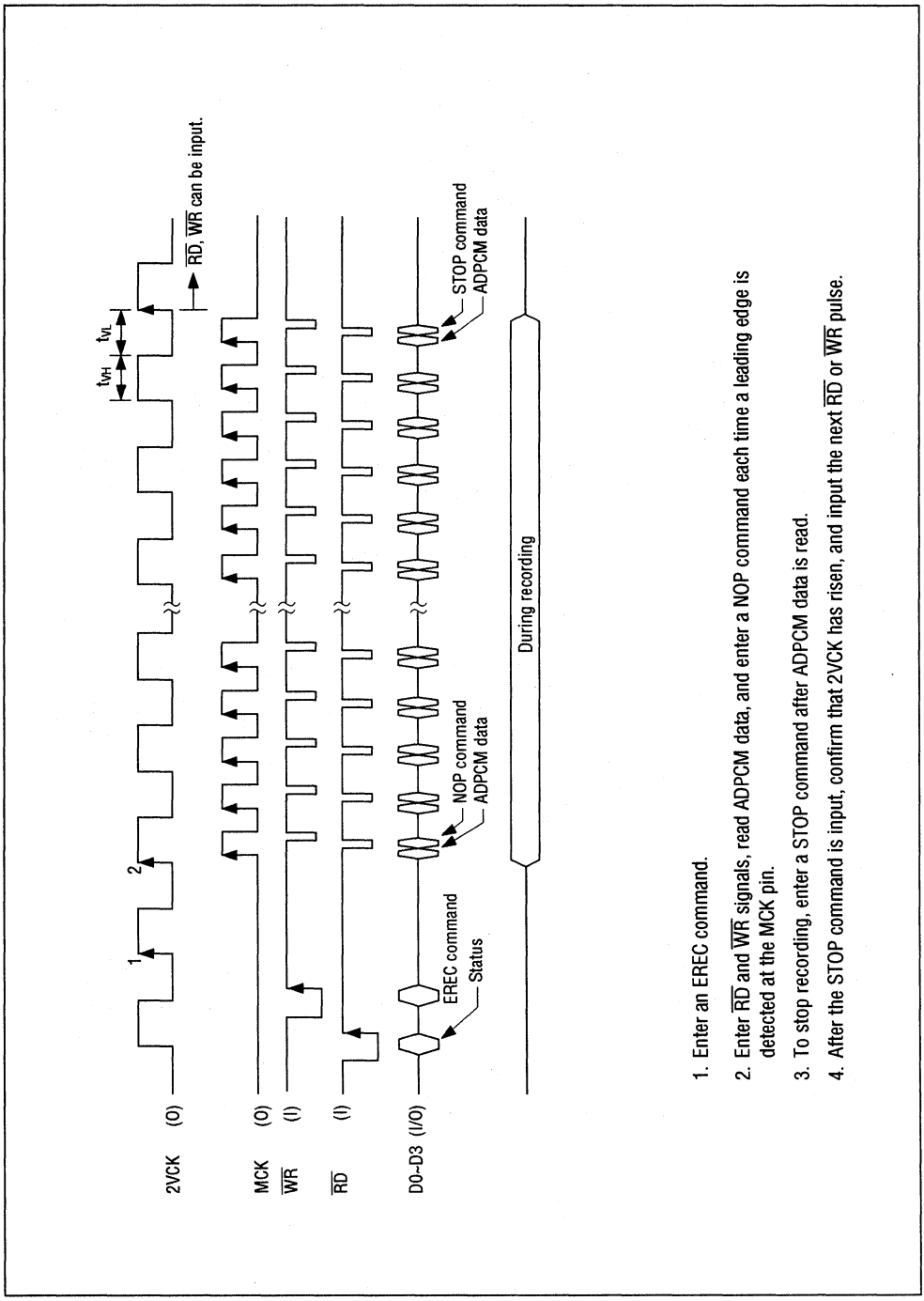
1. Enter the exeternal serial voice register address into which data is to be written using the STWR or SPWR command.(The address to be entered may be duplicated.)
2. Enter a DTWR command.
3. To write data into the serial voice register, enter $\overline{WR}$ and $\overline{RD}$ signals each time a leading edge is detected at the MCK pin.
4. After the last data is fetched, confirm that 2VCK has risen, and input the next $\overline{WR}$ pulse or $\overline{RD}$ pulse.

9. How to Playback Using an EPLAY Command



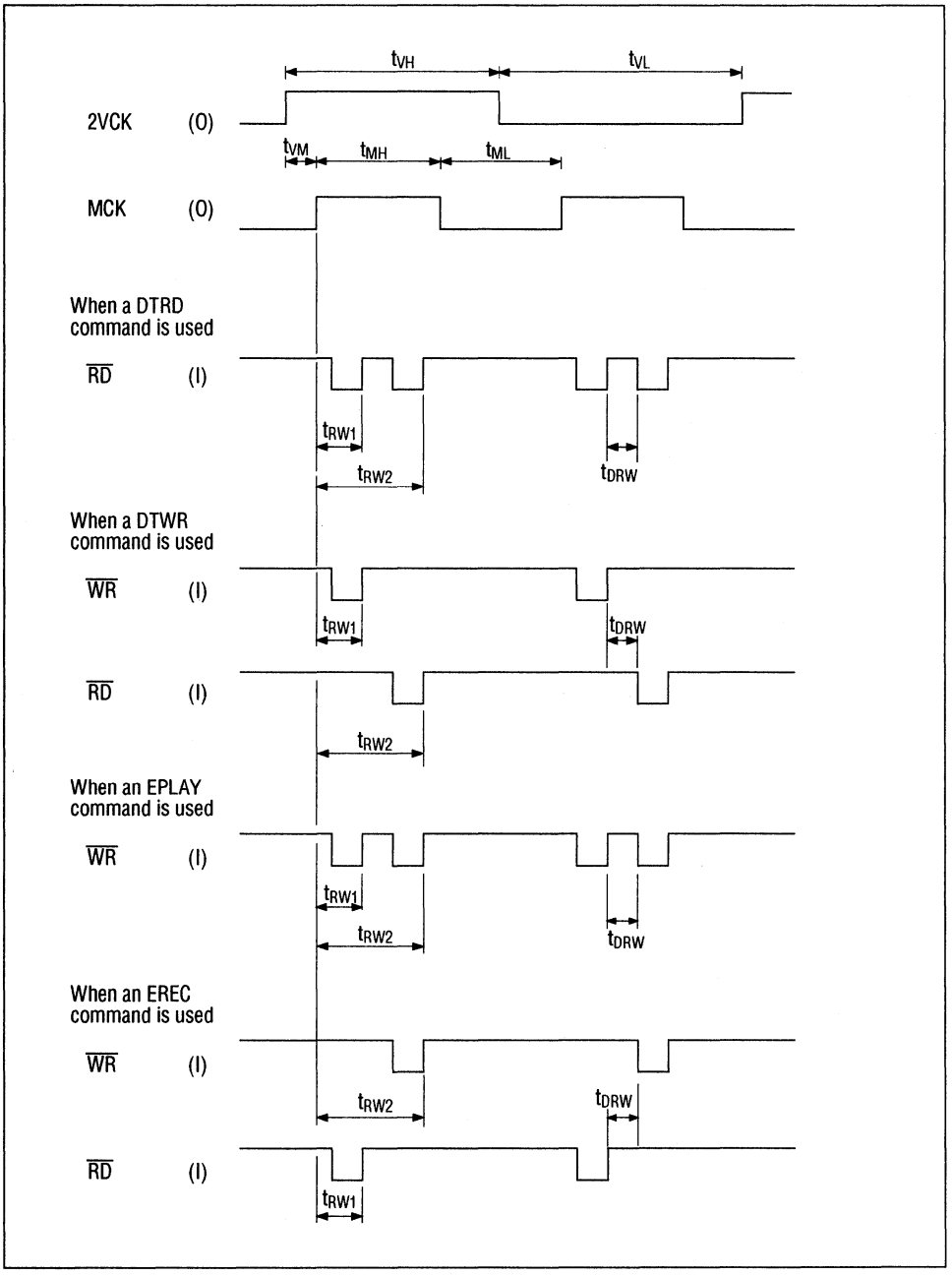
1. Enter an EPLAY command.
2. Enter a WR signal, ADPCM data, and a NOP command each time a leading edge is detected at the MCK pin.
3. To stop playback, enter a STOP command after ADPCM data input.
4. After the STOP command is input, confirm that 2VCK has risen, and input the next RD or WR pulse.

10. How to Record Using an EREC Command

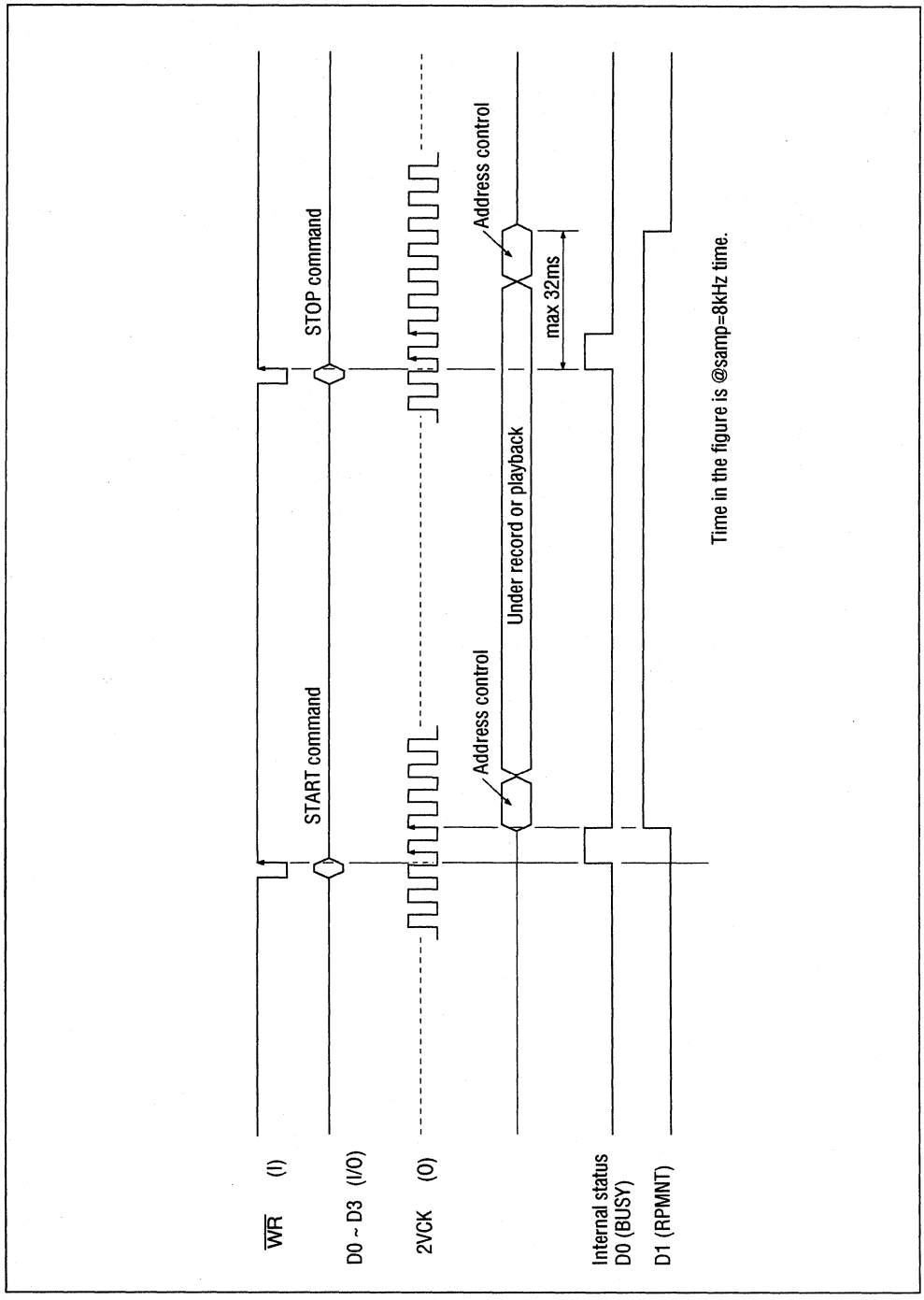


1. Enter an EREC command.
2. Enter $\overline{RD}$ and $\overline{WR}$ signals, read ADPCM data, and enter a NOP command each time a leading edge is detected at the MCK pin.
3. To stop recording, enter a STOP command after ADPCM data is read.
4. After the STOP command is input, confirm that 2VCK has risen, and input the next $\overline{RD}$ or $\overline{WR}$ pulse.

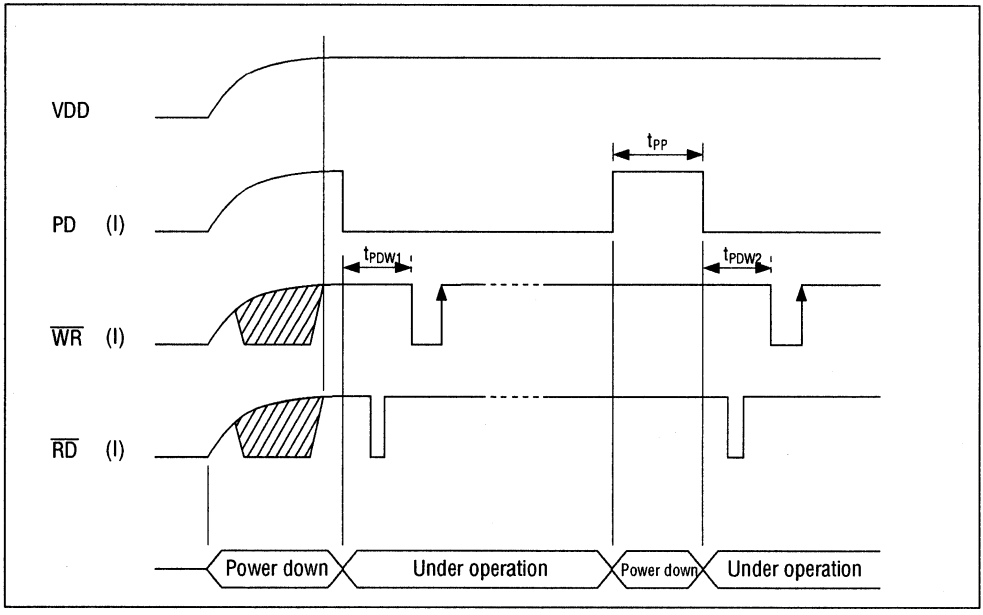
11. How to enter $\overline{WR}$ and $\overline{RD}$ signals in one sampling cycle when a DTRD, DTWR, EPLAY, or EREC command is used



12. Start and Stop of Playback by START Command and STOP Command

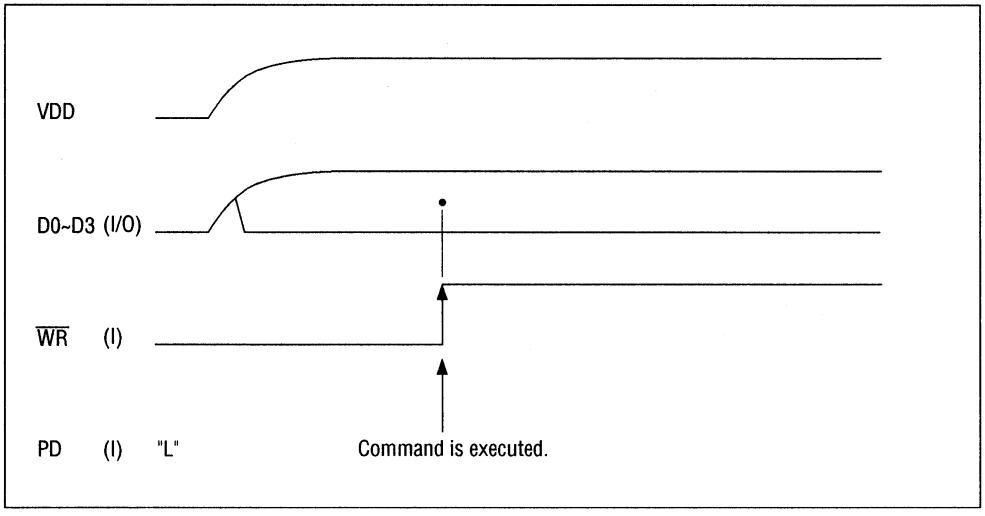


13. Power down, reset timing



Power-down state occurs by inputting "H" level to PD pin and at the same time, the control circuit is reset. However, this is not a forced reset pin, but is invalid during performing DTRD and DTWR commands, and during recording and playback.

After power-on, input "H" level to PD pin until the VDD voltage is stabilized. For instance, after power is put on as illustrated below, the "H" edge is generated at $\overline{WR}$ pin and then the commands of the contents for D_0~D_3 pins are executed. At this time, if a START command or the DTRD and DTWR commands are carried out, the reset by PD pin becomes impossible.



FUNCTION OF PINS

- **Pins for Both Stand-alone and Microcontroller Interface Application**

Pin Name	I/O	Function
DVDD	–	Digital power supply pin
AVDD	–	Analog power supply pin
DVDD'	–	Power supply pin
DGND	–	Digital ground pin
AGND	–	Analog ground pin
SGC SG	O	Outputs the reference voltage (signal ground (SG)) of the analog circuit. A capacitor is connected between this pin and the GND pin to stabilize the voltage.
MIN LIN	I	Input pin that inverts the input to the built-in operational amplifier. Non-inverted pins are connected to the SG internally.
MOUT LOUT	O	MOUT is an output pin of the built-in operational amplifier corresponding to the MIN input pin. The LOUT output pin corresponds to the LIN input pin.
AMON	O	Connected to the LOUT pin during recording and to the DA converter output pin during playback. Connect to the FIN input pin of the built-in amplifier.
FIN	I	Input pin ot the built-in low-pass filter
AOUT	O	Analog voice output pin
DAO	O	Output pin of the built-in 12-bit DA conveter
SAD	O	(Serial Address Data) Connected to the SAD pin of the serial voice register to output the first address for read/write operation.
$\overline{SAS}$	O	(Serial Address Strobe) Clock pin connected to the $\overline{SAS}$ pin of the serial voice register to write serial addresses
$\overline{TAS}$	O	(Transfer Address Strobe) Connected to the $\overline{TAS}$ pin of the serial voice register. The $\overline{TAS}$ pin sets serial addresses to the internal address counter of the serial voice register.
$\overline{RWCK}$	O	(Read/Write Clock) Clock terminal connected to the $\overline{RWCK}$ pin of the serial voice register to read data from and write it into the serial voice register
$\overline{WE}$	O	(Write Enable) Output pin connected to the $\overline{WE}$ pin of the serial voice register to select the write or read mode
DIN	O	(Data Input) Connected to the DIN pin of the serial voice register to outputwrite data

Pin Name	I/O	Function
DOUT	I	(Data Output) Connected to the DOUT pin of the serial voice register to fetch read data. **When used at stand-alone mode, insert a pull-down register of about 100kΩ between DOUT pin and GND.**
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	(Chip Select) Connected to the $\overline{CS}$ pin of the serial voice register
MCUM	I	Determines whether the LSI is used in stand-alone mode or connected to a microcontroller interface. High level: Connected to a microcontroller interface Low level: Used as a stand-alone LSI
RSEL1 RSEL2	I	(Register Select) Selects the number of serial voice registers. For details, see Explanation of Functions described later.
2VCK	O	Outputs a clock at a frequency half the sampling frequency. Used as a synchronizing clock when the LSI is connected to a microcontroller interface.
XT	I	Connected to the resonator. When an external clock is used, clock pulses are supplied through this pin. When the power goes down, it is set to the ground level.
$\overline{XT}$	O	Connected to the resonator. When an external clock is used, it must be left open.
TEST	I	LSI test pin. Connected to a pull-down resistor in the LSI. This pin must be set at the low level.

• Stand-alone Application

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>CSEL1
CSEL2</td><td>I</td><td>Selects the number of phrases to be recorded. For details, see Explanaiton of Functions described later.</td></tr>
<tr><td>CA1
CA2
CA3</td><td>I</td><td>Specifies a channel. For details, see Explanation of Functions described later.</td></tr>
<tr><td>SAM1
SAM2</td><td>I</td><td>Sample frequency selection. The relationships between the oscillator frequency (f_{OSC}) and the sampling frequency (f_{sam}) are as follows (the frequencies in parentheses are measured at f_{OSC}=2.048MHz):
<table>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>f_{sam}</td><td>$\frac{f_{OSC}}{512}$
(4.0kHz)</td><td>$\frac{f_{OSC}}{288}$
(7.1kHz)</td><td>$\frac{f_{OSC}}{256}$
(8.0kHz)</td><td>$\frac{f_{OSC}}{224}$
(9.1kHz)</td></tr>
</table></td></tr>
<tr><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Selects the recording mode when the input is at the high level or the playback mode when it is at the low level.</td></tr>
<tr><td>ST•SP</td><td>I</td><td>Allows the starting or ending of recording or playback to be commanded by inputting a high pulse. It also allows repetitive playback when the high level is maintained during playback.</td></tr>
<tr><td>$\overline{\text{MON}}$</td><td>O</td><td>Set at the low level during recording or playback. When the remaining memory capacity of the channel is almost full, this pin outputs a clock.</td></tr>
</table>

- **Microcontroller Interface Application**

Pin Name	I/O	Function
D3 D2 D1 D0	I/O	Connects to a bidirectional data bus to transfer data and commands to and from an external microcontroller.
$\overline{WR}$	I	Write pulse input pin to write commands or data
$\overline{RD}$	I	Read pulse input pin to read status or data
PD	I	When a high Power Down is input, the LSI enters the power down state.
$\overline{CE}$	I	When a high Chip Enable is input, the write pulse $\overline{WR}$ and read pulse $\overline{RD}$ cannot be accepted and pins D0 to D3 go high impedance.
MCK	O	Outputs a synchronizing clock when ADPCM data is tranferred directly to and from a microcontroller by an EREC or EPLAY command or when data is transferred directly between a microcontroller and serial registers by a DTWR or DTRD command.
ST•SP	I	Not used. Since it is connected to a pull-down resistor in the LSI, it must be set at the low level.

EXPLANATION OF FUNCITONS

• Recording time and memory capacity

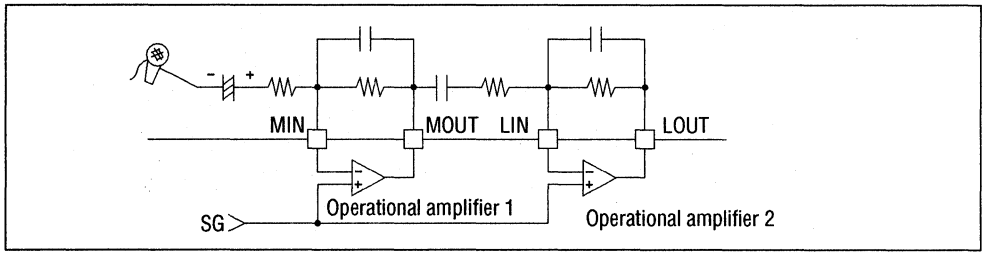
The recording time depends on the capacity of the external serial voice register, sampling frequency, and ADPCM bit length. The relationship between these factors is represented by the following expression:

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K-bit)}}{4(\text{kHz}) \times 4(\text{bit})}(\text{S})$$

• Analog input amplifier circuit

The LSI described in this manual has two operational amplifiers configured as a microphone preamplifier. The LSI is provided with pins for inverted input and output of each amplifier.

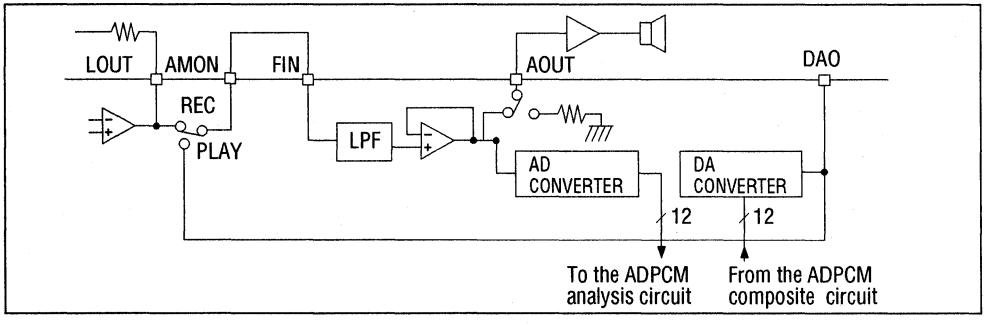
The noninverted input pins are connected to the signal ground (SG) used as the analog circuit reference voltage in the LSI. For amplification, an inverted amplifier circuit is formed. The gain of the amplifier can be adjusted by an external resistor.



• Connection of the low-pass filter circuit periphery

In the LSI, the amplifier circuit from the LOUT pin is connected to the AMON pin. During playback, the D/A converter output from DAO pin is connected to the AMON pin.

The LSI incorporates a fourth-order low-pass filter employing switched capacitor filter technology. Input is provided to the low-pass filter through the FIN pin. Therefore, the AMON pin is connected to the FIN pin directly.

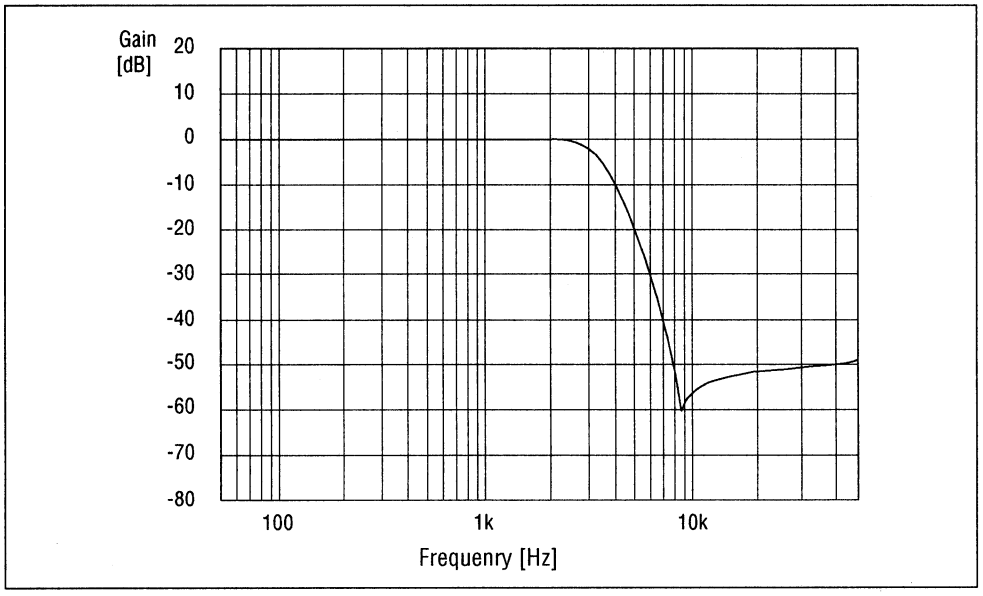


- **LPF characteristics**

The LPF attentuation characteristics of this LSI are about -40dB/oct, and the cutoff frequency and frequency characteristics vary in proportion to the sampling frequency (fsam).

The cutoff frequency is about 3.2kHz when the sampling frequency is 8kHz.

The LPF frequency characteristics are shown below.



LPF Frequency Characteristics (f_{sam}=8.0kHz)

- **Analog (voice) output**

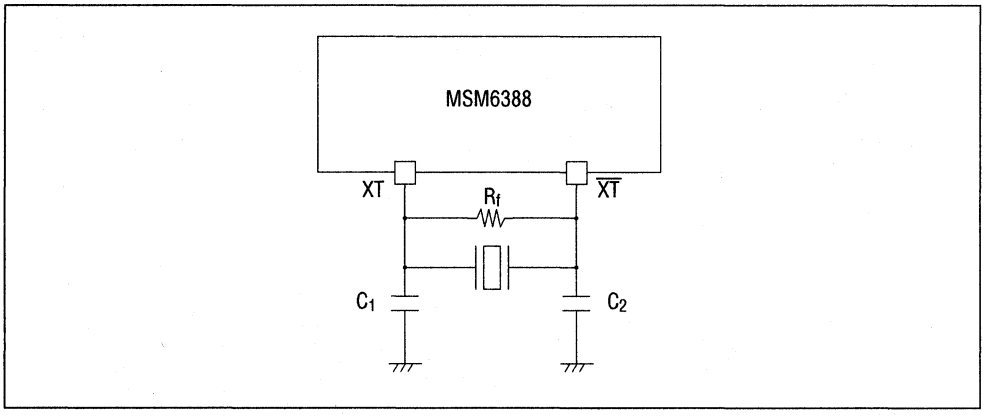
During playback this signal is output from the AOUT pin. Connect the output to a speaker through a power amplifier suitable for driving speakers of from 4 to 16Ω impedance.

The amplitude of the built-in 12bit D/A converter output, provided from the DAO pin, is a maximum of 4095/4096 × VDD. When not using the built-in low-pass filter, connect it to the DAO pin.

- **How to connect the oscillator**

The ceramic oscillator or crystal oscillator are connected to the XT and $\overline{XT}$ terminals as shown below.

For reference, when the ceramic oscillator manufactured by KYOCERA or Murata Seisakusho is connected, the optimum load capacity value is as shown below.



Ceramic oscillator			Optimum load capacity value		Feedback resistance
Model Name		Frequency (Hz)	C_1(PF)	C_2(PF)	R_f(Ω)
Murata Seisakusho	CSA 1.500MK	1.5M	30	30	(1M)
	CSA 2.00MG	2.0M			
	CSA 4.00MG	4.0M			
	CSA 8.00MT	8.0M			
KYOCERA	KBR 2.0MS	2.0M	33	33	—
	KBR 4.0MS	4.0M			
	KBR 8.0MS	8.0M			

- **Battery back up of the 1M serial voice registers**

When backing up the 1M serial voice register, back up MSM6388 at the same time. When backing up only a 1M serial voice register, the bootstrap function works and cannot be played back when the power supply is turned on.

An example of the circuit that obtains VDD supply power is shown below. In this case, VDD and VDD at back up is about respectively 0.7V lower than the system power supply voltage and battery voltage due to the drop of the diode forward voltage.

The non-volatile battery backup circuit has the following conditions:

(1) When the VDD supply voltage is dropped, the H level of the input signal must not exceed VDD +0.3V.

(2) VDD at the time of backup must be in the range of 3.5 to 5.5V.

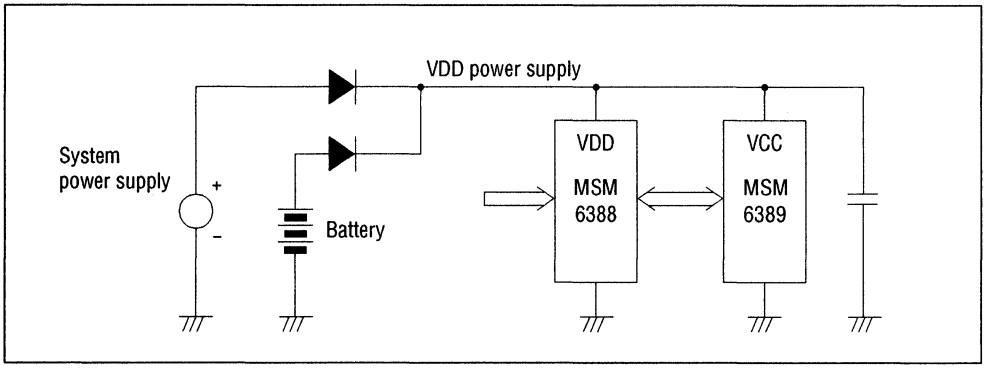


Figure: Example of Battery Backup Circuits of MSM6388 and MSM6389

- **Battery driving**

An example of the estimated battery life when a +4.5V power supply is operated by serially connecting four MSM6389's, MSM6388, speaker driver, and speaker (example of application circuit and circuit diagram 1) with three dry cell batteries is shown below.

For the current capacity, assume a 3 SUM Mn dry cell battery (R6P), and the capacity up to the drop of the voltage to 1.2V of about 600 mAhrs. When the section consuming current in Circuit Diagram 1 is divided into the MSM6388, four MSM6389's, amplifier, and speaker, the current consumed in each section is as shown in the table below, corresponding to each operation mode.

Circuit	Operation mode		
	At recording	At playback	At data retention
MSM6388	5mA	5mA	—
MSM6389 (four)	1mA	1mA	30μA × 4 = 120μA
Amplifier, speaker	—	20mA	—
Total	6mA	26mA	0.12mA

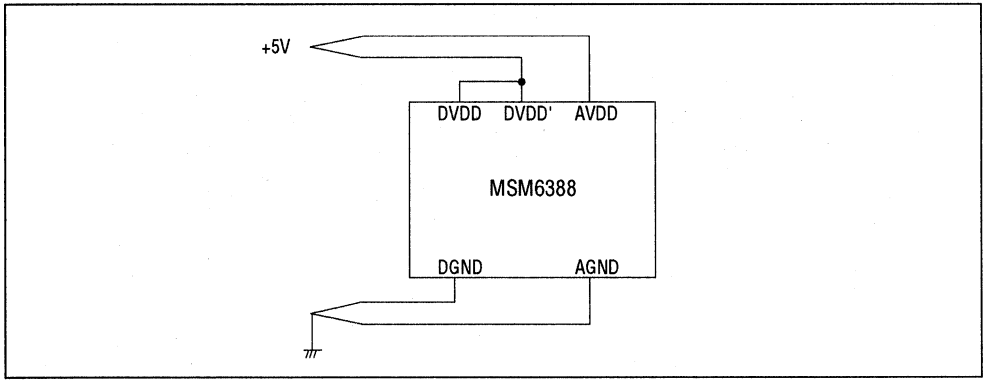
When the recording time per day is 4 minutes, playback time 4 minutes, and the data retention time is 10 hours as the standard time, the current consumption per day is:

At recording:
$$6mA \times \frac{4}{60} = 0.4mAhrs$$
At playback:
$$26mA \times \frac{4}{60} = 1.73mAhrs$$
At data retention:
$$0.12mA \times 10 = 1.2mAhrs$$

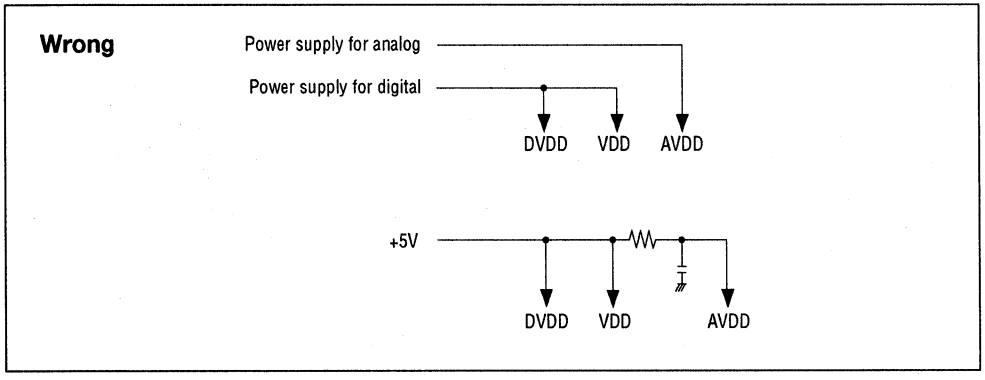
The total consumption per day is 3.3 mAhrs. In other words, if a battery of 600 mAhrs is used for the capacity,a service life of 600 mAhrs/3.3 mAhrs = 180 days is provided. The battery can be used for six months without replacement.

- **Power supply wiring**

Supply the power supply of this LSI from the same power source as illustrated below, while separating the analog portion and logic portion in wiring.



If the analog portion and logic portion are suppied from a separate power source, make sure the voltage difference between both power sources does not exceed ±3 volts or latch-up may occur.



- **Increasing Power supply**

The internal power-on reset circuit of MSM6388 requires that the common supply voltage to AVDD, DVDD, and DVDD' is increased from 0 to +3.5V exponentially and smoothly within 20ms. If the voltages of less than 20ms is provided or if by accident the voltage drops once during the increasing period the MSM6388 may behave unpredictable.

- **Power OFF/ON**

During an interval between a power OFF and a subsequent power ON, the level on VDD input must be less than 0.05V at the instant of a new power ON. Also, this measure accounts for the nature of the internal power-on reset circuit.

- **Operations in the standalone application**

1. Power down function

When the LSI is not recording or playing back data, the power down function is enabled and oscillation is stopped. At power down when an external clock is used, be sure to set the XT pin to the ground level to lower current consumption.

2. Oscillator frequency and sampling frequency

The oscillator frequency fosc can be used between 1.5MHZ and 4MHZ. The sampling frequency (fsam) is related to the oscillator frequency as follows, according to the settings of the SAM1 and SAM2 pins:

SAM2	L	L	H	H
SAM1	L	H	L	H
f_{sam}	$\frac{fosc}{512}$ (4.0kHz)	$\frac{fosc}{288}$ (7.1kHz)	$\frac{fosc}{256}$ (8.0kHz)	$\frac{fosc}{224}$ (9.1kHz)

Note: Sampling frequencies in parentheses are measured at an oscillator frequency of 2.048 MHz.

If the sampling frequency during playback is varied from fsam during recording, fast and slow playback are possible. In this case, the sound level is also varied.

Example:
Sampling frequency during recording:
8.0kHz
Sampling frequency during playback:
7.1kHz: Slow playback
9.1kHz: Fast playback

3. Use of channels

Set the RSEL1 and RSEL2 input pins according to the number of 1Mbit serial voice registers connected to the LSI (see the table below).

RSEL2	L	L	H	H
RSEL1	L	H	L	H
Number of serial voice registers	1	2	3	4

The number of the phrases to be recorded can be set to 1, 2, 4, or 8 according to the setting of the CSEL1 and CSEL2 input pins. (When three external serial voice registers are used, the phrase count can be set to 1, 2, 3, or 6.)

The memory capacity of the external serial voice registers available to each channel equals the total available memory divided by the number of phrases being recorded. IE: When the phrase count is set to 8, for example, one-eighth of the entire memory capacity is assigned as the memory capacity of each channel, and when the phrase count is 4, one-fourth of the entire memory capacity is assigned. (The memory capacity divided and assigned to each channel is called the channel memory capacity.)

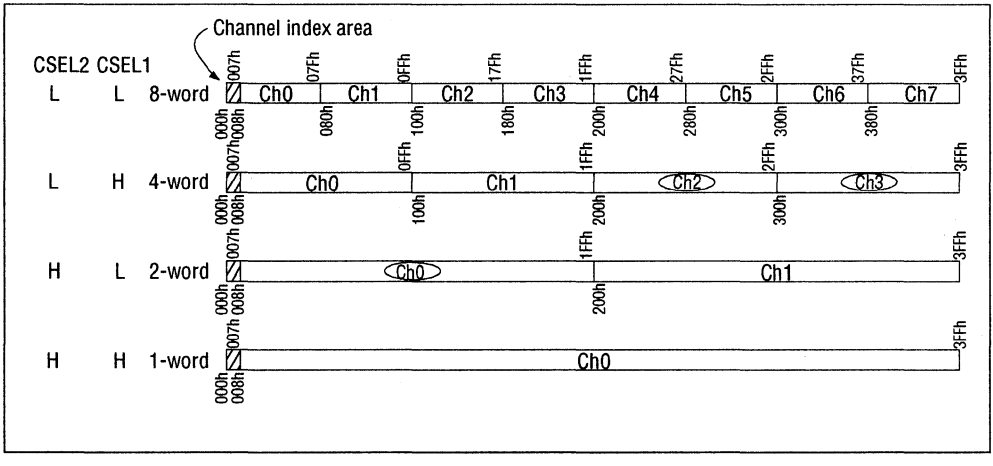
Each channel memory capacity can be assigned to a particular channel by the CA1, CA2, and CA3 input pins.

The relationships between the number of external serial voice registers used, the number of phrases to be recorded, channels, and channel memory capacities are shown in the following table.

CSEL 2	CSEL 1	Number of phrases 1,2, or 4 (Note1)	Number of phrases 3 (Note1)	CA3	CA2	CA1	Channel 1,2, or 4 (Note1)	Channel 3 (Note1)	Channel memory capacity (bit) 1 (Note1)	2 (Note1)	3 (Note1)	4 (Note1)
L	L	8	6	L	L	L	**ch0	ch0	128K (4 s)	256K (8 s)	512K (16 s)	
				L	L	H	**ch1	ch1				
				L	H	L	*ch2	ch2				
				L	H	H	*ch3	ch3				
				H	L	L	ch4	ch4				
				H	L	H	ch5	ch5				
				H	H	L	ch6	ch4				
				H	H	H	ch7	ch5				
L	H	4	3	L	L	–	**ch0	ch0	256K (8 s)	512K (16 s)	1M (32 s)	
				L	H		*ch1	ch1				
				H	L		ch2	ch2				
				H	H		ch3	ch2				
H	L	2		L	–	–	*ch0		512K (16 s)	1M (32 s)	1536K (50 s)	2M (65 s)
				H			ch1					
H	H	1		–	–	–	ch0		1M (32 s)	2M (65 s)	3M (98 s)	4M (131 s)

Note: The number of seconds in parentheses is a recording time measured at f_{sam}=8.0kHz.
The first 8Kbit of the serial voice registers are allocated as a channel index area.
Therefore, the channel memory capacity of channel "0" is 8Kbit less than the value listed in the table above.
1) Number of external serial voice registers
2) When 512Kbit serial voice registers use, only can use (*) (**) mark channel
3) When 256Kbit serial voice regisrers use, only can use (**) mark channel

Allocation for Channel and Channel Memory Capacity in Using 1 Piece of 1M-Bit Serial Voice Register.



Note: By the combination of CSEL1, CSEL2, CA1, CA2 and CA3, the circled channel memory capacities can be allocated as Ch0=16sec., Ch2=8 sec. and Ch3=8 sec. (@f_{sam}=8kHz).

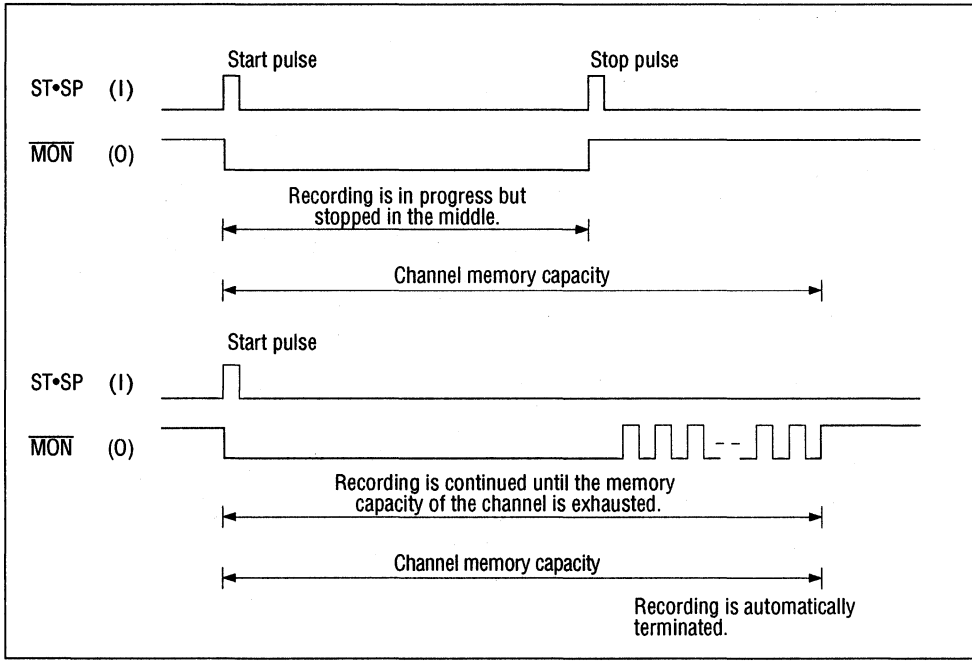
4. Recording

Pull the REC/$\overline{\text{PLAY}}$ pin high. Then, select the number of the phrase to be recorded with the CSEL1 and CSEL2 input pins and select a channel with the CA1 to CA2 input pins.

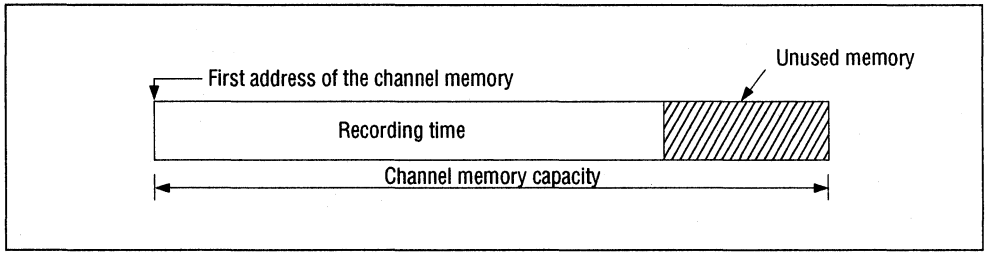
To stop recording in the middle of a phrase, input a pulse to the ST.SP pin again. The recording duration is the time between these two pulses.

When recording is initiated by inputting a pulse to the ST.SP pin, and continued until the memory capacity of the specified channel is exhausted, recording is automatically terminated.

During recording, the $\overline{\text{MON}}$ pin is low.

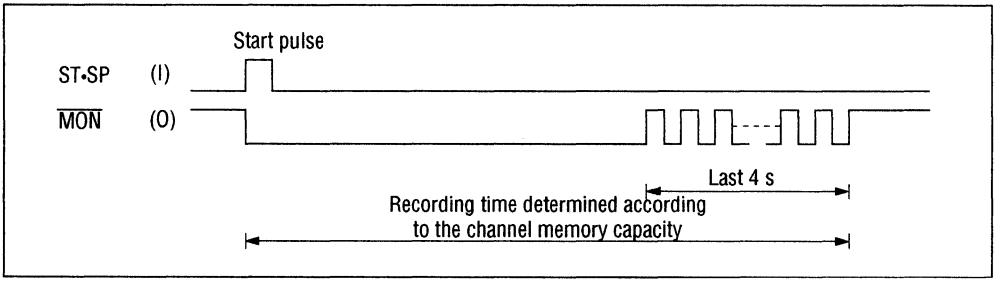


Note: As mentioned above, the memory capacity of the external serial registers is divided by the number of phrases and is assigned as the channel memory capacity. During recording, ADPCM data is written, starting from the first address of the memory of the specified channel. When recording is terminated in the middle of the channel memory capacity by a stop pulse, the subsequent memory area remains unused.



5. Alarm for remaining recording time

When recording is initiated by inputting a pulse to the ST•SP pin and the available recording time reaches the last four seconds, the $\overline{\text{MON}}$ pin outputs a 4Hz clock for the last seconds as an "out of available memory" alarm.



Note : During the last four seconds a clock frequency of 4 Hz described above is output, when the sampling frequency (f_{sam}) of 8.0 kHz is selected. The duration of the alarm clock is proportional to the length of the cycle of the sampling frequency and the clock frequency is proportional to the sampling frequency used.

6. Playback

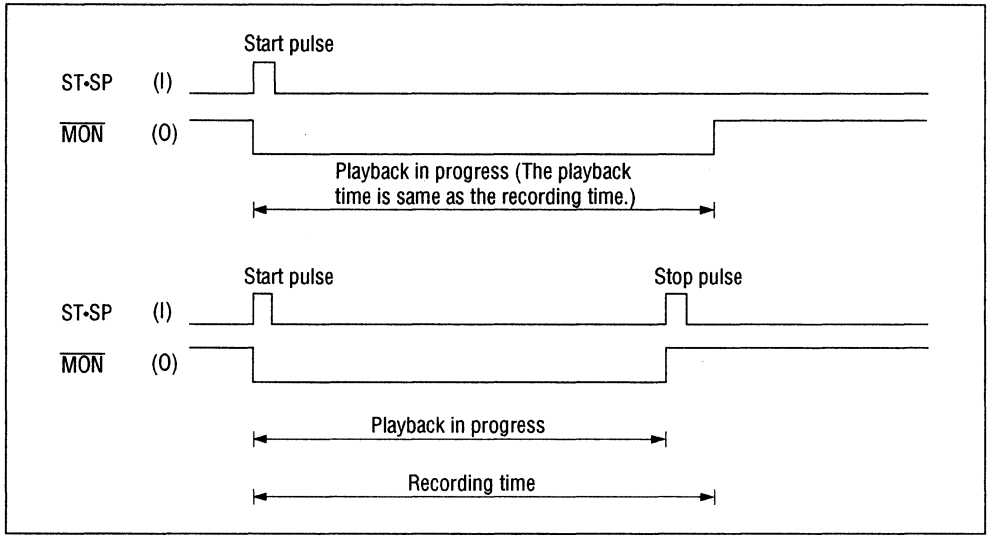
Set the REC/$\overline{\text{PLAY}}$ pin low. Then, select the number of the phrase recorded with the CSEL1 and CSEL2 input pins and select a channel with the CA1 to CA3 input pins. To initiate playback, input a pulse to the ST•SP pin. Playback is automatically stopped when the recording time is expired.

To stop playback in the middle of a phrase, input a pulse to the ST•SP pin again.

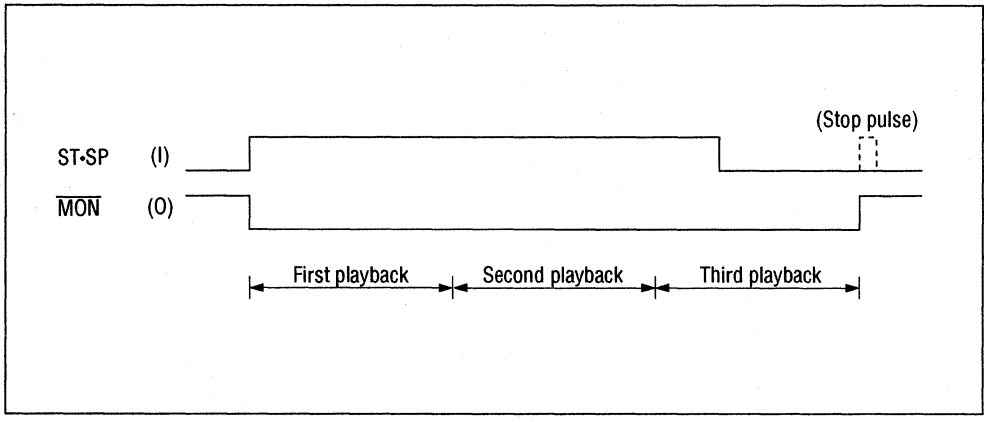
During playback, the $\overline{\text{MON}}$ pin is kept low.

Do not start playback in channels not recorded because the playback data and time are undefined.

However, playback under these conditions can be halted by a stop pulse.

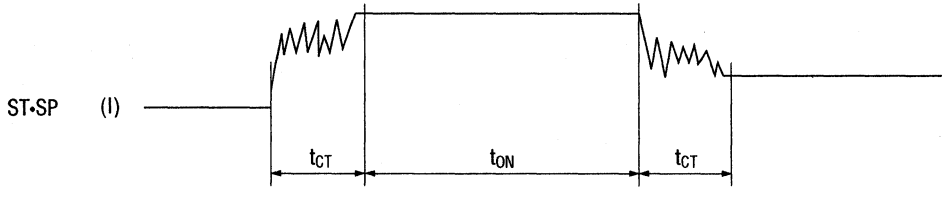


Playback can be repeated by maintaining the ST•SP pin high.



7. Debounce circuit for the ST.SP pin

A debounce circuit functions to prevent the ST.SP pin from malfunctioning due to switch contact bounce. The debounce time is 32 ms. Be sure to set the time during which the ST.SP pin is kept high for at least 70 ms.



Chattering time $t_{CT} \leqq 32ms$
High-level time $t_{ON} \geqq 70ms$

The above chattering time t_{CT} and high-level time t_{ON} are true when the sampling frequency f_{sam} is 8 kHz. These times are proportional to the length of the sampling frequency f_{sam}.

- **Operations in the microcontroller interface application**

The MSM6388 LSI operations are controlled by pins 2VCK, MCK, PD and 16 commands using pins D0 to D3, $\overline{WR}$ and $\overline{RD}$.

1. Explanation of Commands

Command	Code D3	D2	D1	D0	Function
NOP	0	0	0	0	(NON OPERATION) Has no particular function but is used during execution of a EPLAY or EREC command.
INIT	0	0	0	1	(INITIALIZE) • Writes the last address of the external serial voice regisrers as the start and stop addresses of each of channels 0 to 7 to set the channel memory in the unrecorded state. • Sets channel 0 in the channel register.
PLAY	0	0	1	0	(PLAY BACK) Set the playback mode.
REC	0	0	1	1	(RECORD) Set the recording mode.
START	0	1	0	0	(START) Starts recording or playback. At the same time, it writes the start and stop addresses stored in the channel index area into the LSI.
STOP	0	1	0	1	(STOP) Stops recording or playback. When this command is executed during recording, it stores the contents of the address counter at the stop time in the channel index area as the stop address.
SAMP	0	1	1	0	(SAMPLING FREQUENCY) Specifies a sampling frequency together with the next nibble.
CHAN	0	1	1	1	(CHANNEL) Specifies a channel together with the next nibble.
STWR	1	0	0	0	(START ADDRESS WRITE) Stores the start address in the channel index area together with the next three nibbles.
SPWR	1	0	0	1	(STOP ADDRESS WRITE) Stores the stop address in the channel index area together with the next three nibbles.
STRD	1	0	1	0	(START ADDRESS READ) Reads the start address stored in the channel index area through the next three read accesses. During this operation, the contents of the status register cannot be read.
SPRD	1	0	1	1	(STOP ADDRESS READ) Reads the stop address stored in the channel index area through the next three read accesses. During this operation, the contents of the status register cannot be read.

Command	Code D3 D2 D1 D0	Function
DTRD	1 1 0 0	(DATA READ) Reads the contents of external serial voice registers 1K bit sequentially through the data bus on the specified timing. When this command is issued, the LSI enters the playback mode.
DTWR	1 1 0 1	(DATA WRITE) Writes data into external serial voice registers 1Kbit sequentially through the data bus on the specified timing. When this command is issued, the LSI enters the recording mode.
EPLAY	1 1 1 0	(EXTERNAL PLAYBACK) Plays back ADPCM data while reading it from the data bus on the specified timing. When this command is issued, the LSI enters the playback mode.
EREC	1 1 1 1	(EXTERNAL RECORDS) Starts recording and outputs ADPCM data to the data bus on the specified timing. When this command is issued, the LSI enters the recording mode.

- MSM6388 Commands

Command	First nibble command D3 D2 D1 D0	Second nibble command D3 D2 D1 D0	Third nibble command D3 D2 D1 D0	Fourth nibble command D3 D2 D1 D0
NOP	0 0 0 0	———	———	———
INIT	0 0 0 1	———	———	———
PLAY	0 0 1 0	———	———	———
REC	0 0 1 1	———	———	———
START	0 1 0 0	———	———	———
STOP	0 1 0 1	———	———	———
SAMP	0 1 1 0	– S2 S1 S0	———	———
CHAN	0 1 1 1	– C2 C1 C0	———	———
STWR	1 0 0 0	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8
SPWR	1 0 0 1	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8
STRD	1 0 1 0	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8
SPRD	1 0 1 1	A3 A2 A1 A0	A7 A6 A5 A4	A11 A10 A9 A8
DTRD	1 1 0 0	Operates on the specified timing.		
DTWR	1 1 0 1			
EPLAY	1 1 1 0			
EREC	1 1 1 1			

- Sampling frequency specification (SAMP command)

S2	S1	S0	Sampling frequency		
0	0	0	SA0	$f_{OSC}/576$	(3.6kHz)
0	0	1	SA1	$f_{OSC}/512$	(4.0kHz)
0	1	0	SA2	$f_{OSC}/448$	(4.6kHz)
0	1	1			
1	0	0	SA3	$f_{OSC}/288$	(7.1kHz)
1	0	1	SA4	$f_{OSC}/256$	(8.0kHz)
1	1	0	SA5	$f_{OSC}/224$	(9.1kHz)
1	1	1			

Note: Frequencies in parentheses are used when the oscillator frequency f_{OSC} is 2.048MHz.

- Channel specification

C2	C1	C0	Channel
0	0	0	Ch0
0	0	1	Ch1
0	1	0	Ch2
0	1	1	Ch3
1	0	0	Ch4
1	0	1	Ch5
1	1	0	Ch6
1	1	1	Ch7

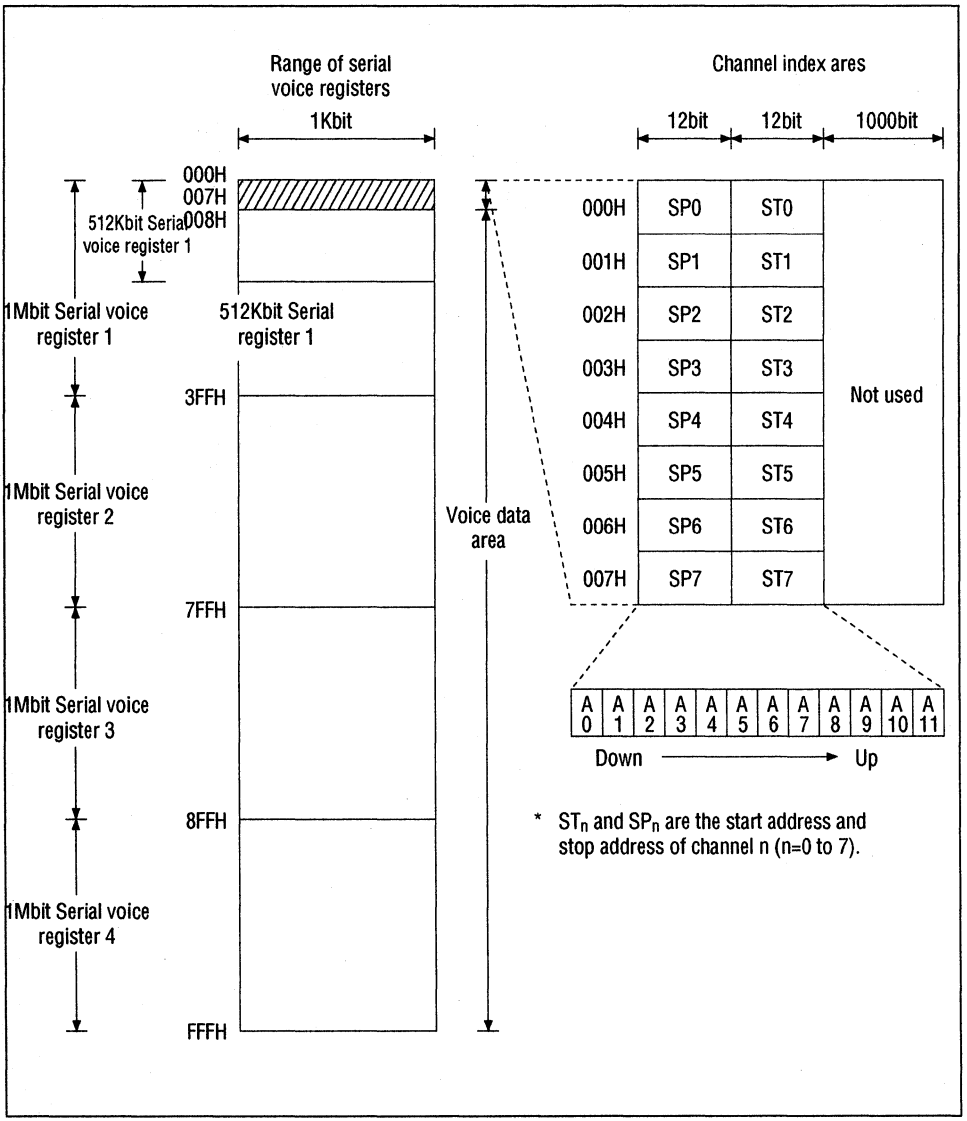
- Start and stop addresses (STWR, SPWR, STRD, and SPRD commands)

The start and stop addresses used to control recording time is managed by 12bit. The available memory capacity varies depending on the number of serial voice registers to be connected externally.

Regardless of the number of serial voice registers, the area between addresses 000H and 007H is allocated as the channel index area to store the start and stop addresses for each channel. The area starting from address 008H can be used to store voice data (ADPCM data).

When on use 512Kbit serial voice register, can use 008H ~ 1FF address.

When on use 256K serical voice register, can use 008H~0FF address.



2. Explanation of the status register

The status register consists of three bits. When a negative-going pulse is supplied to the/RD pin, the status of these bits is output to D0 ~ D2. Note that the status is not output during the execution of an STRD or SPRD command. During execution of a DTRD, DTWR, EPLAY, or EREC command, Status must be read only when the timing is correct.

D3	D2	D1	D0
"L"	DTMNT	RPMNT	BUSY

(1) Busy

The busy bit is high when the LSI is being initialized or when it is executing a command.

When the busy bit is high, do not issue a command from the microcomputer.

BUSY Timing

BUSY conditions		BUSY time max.
NOP, PLAY, REC, START, STOP command		$4/f_{sam}$ (500μs)
INIT command		$34/f_{sam}$ (4.75ms)
SAMP, CHAN command	First nibble	$4/f_{sam}$ (500μs)
	Second nibble	$4/f_{sam}$ (500μs)
STWR, SPWR command	First nibble	$6/f_{sam}$ (750μs)
	After second nibble	$4/f_{sam}$ (500μs)
STRD, SPRD command	First nibble	$6/f_{sam}$ (750μs)
	After second nibble	$4/f_{sam}$ (500μs)

Note: The inside of parentheses shows the time of f_{sam}=8kHz.
BUSY time is porportional to f_{sam} frequency.

(2) RPMNT (Record Playback MoNiTor)

The RPMNT bit is high when the LSI is recording or playing back data. When the RPMNT bit is high, do not input a command except the STOP command.

(3) DTMNT (Data Read Write MoNiTor)

The DTMNT bit is high when data is being transferred to or from serial voice registers by the DTRD or DTWR command.

3. Recording

(1) Sampling frequency select:

To select a sampling frequency fsam, enter a SAMP command.

(2) Channel select:

To select a channel, enter a CHAN command. Usually, specify channel 0.

(3) Start and stop addresses select:

To allocate an area for recording voice data, enter STWR and SPWR commands to store a start address and a stop address in the specified channel field in the channel index area.

(4) To enter the recording mode, enter an REC command.

(5) To start recording, enter a START command. The LSI fetches the start and stop addresses of the specified channel from the channel index area and stores the start address in the address counter and the stop address in the stop address register, then starts recording.

(6) Stopping recording:

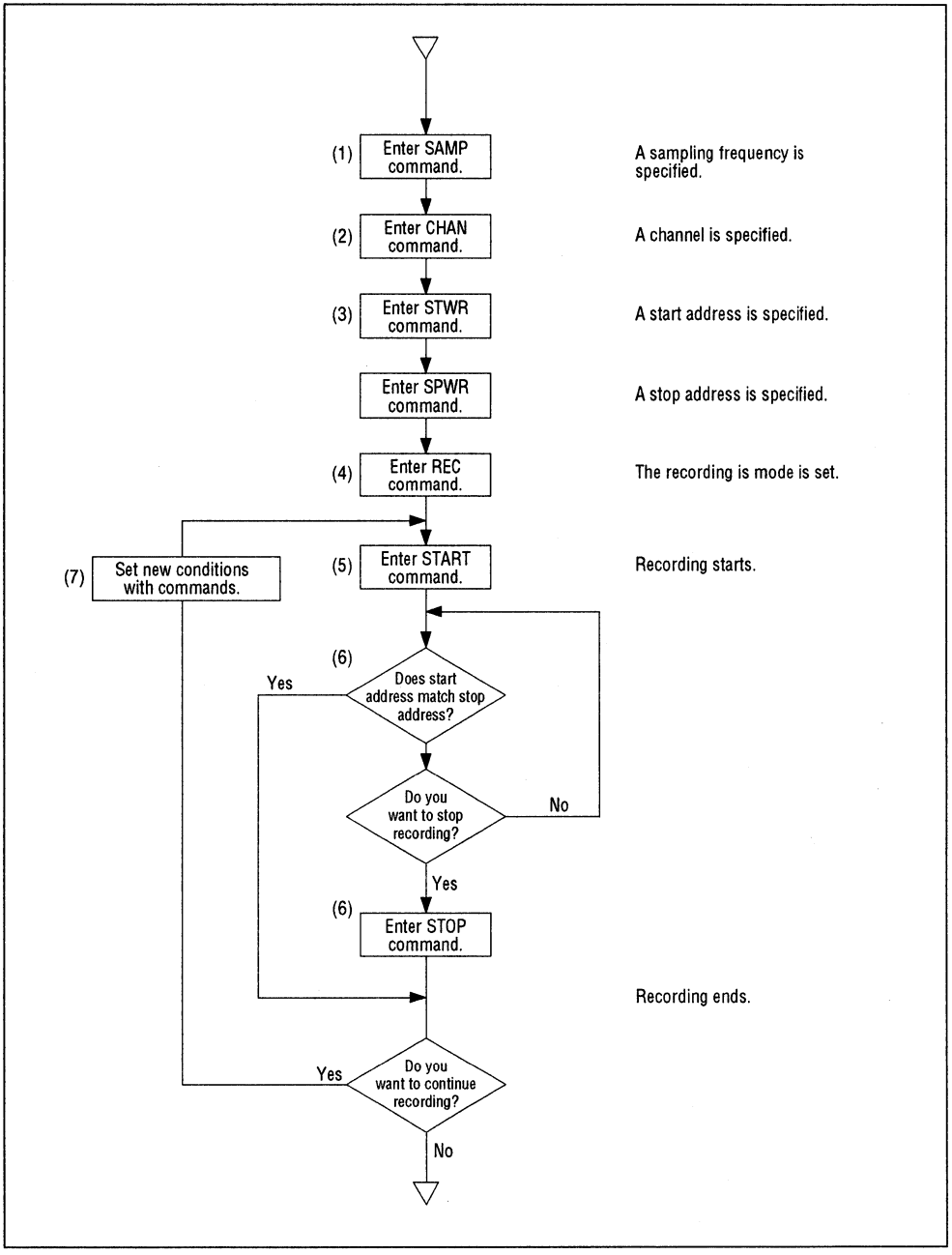
When the contents of the address counter match those of the stop address register, recording is stopped automatically. To stop recording in the middle, enter a STOP command. In this case, the contents of the address counter at recording stop are stored in the channel index area as the stop address.

(7) To resume recording, specify new conditions with commands as described in items (1) to (3) above and follow the procedure described above.

The start and stop address of each channel can be read by STRD and SPRD commands.

When these addresses are controlled by a microcomputer, the memory capacity of external serial voice registers can be used efficiently.

Recording Flowchart when the LSI is Interfaced with a Microcontroller



4. Playback

(1) Sampling frequency select:

To select a sampling frequency, enter a SAMP command.

(2) Channel select:

To select a channel, enter a CHAN command. Usually, specify channel 0.

(3) To enter the playback mode, enter a PLAY command.

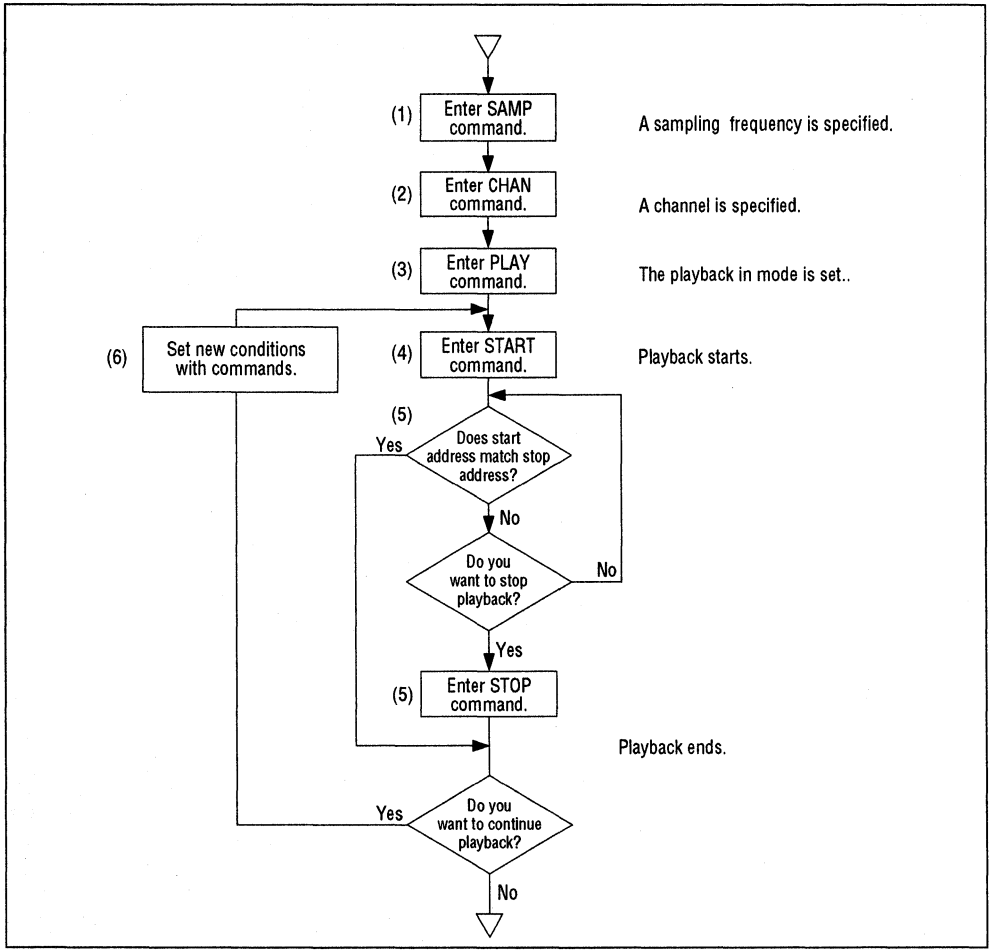
(4) To start playback, enter a START command. The LSI fetches the start and stop addresses of the specified channel index area and then starts playback.

(5) Stopping playback:

When the contents of the address counter match those of the stop address register, playback is stopped automatically. To stop playback in the middle, enter a STOP command.

(6) To resume playback, specify new conditions with commands as described in items (1) and (2) above and follow the procedure described above.

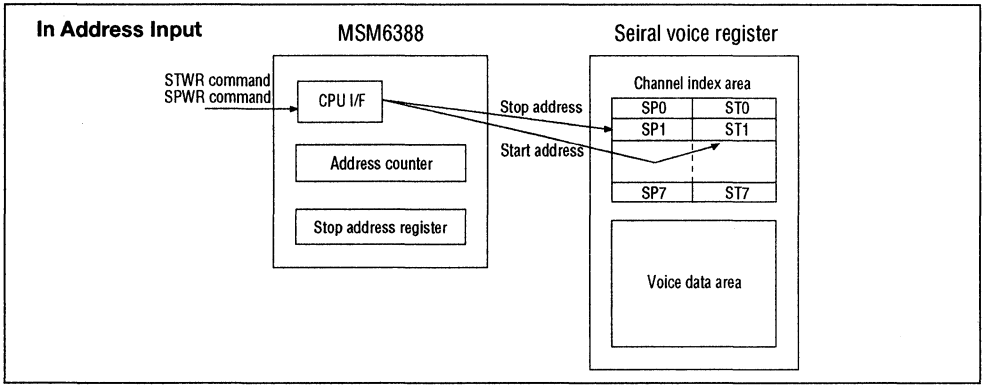
Playback flowchart when the LSI is connected to a microcontroller interface



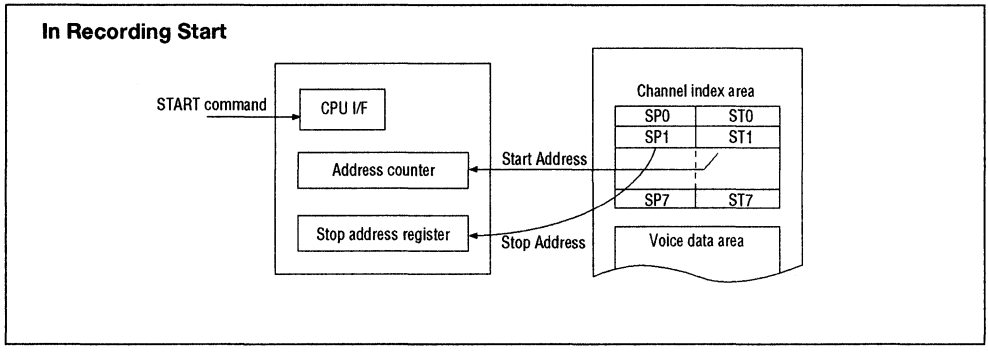
5. Channel Index Area

Operation for channel index area in recording is shown below.

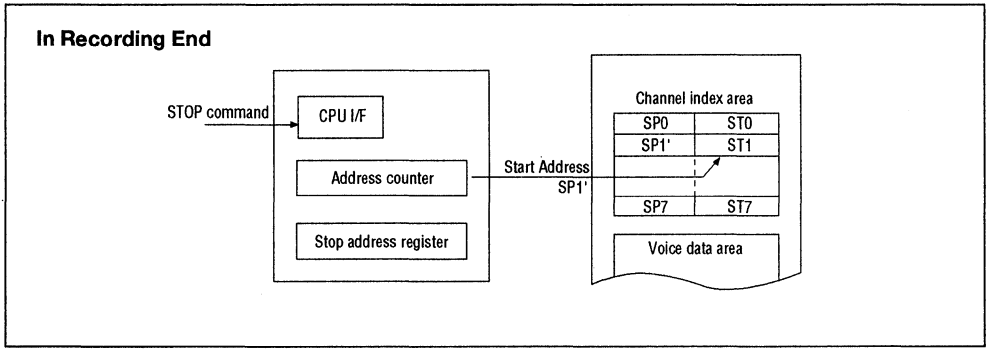
START address and STOP address area written to the channel that designated the channel index area by STWR and SPWR commands.



When START command is inputted, the recording is started after the start addresses of channel index area are automatically set to respective address counter and STOP address register.

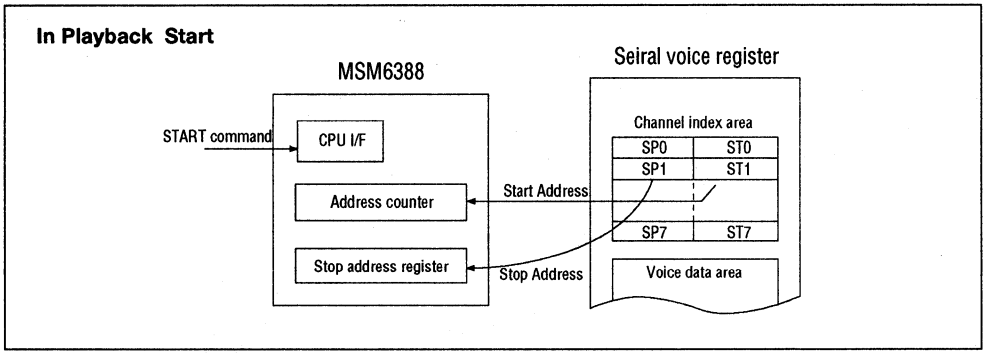


When STOP command is inputted, the contents for the address counter of that time is automatically set to the channel index area as a new STOP address.

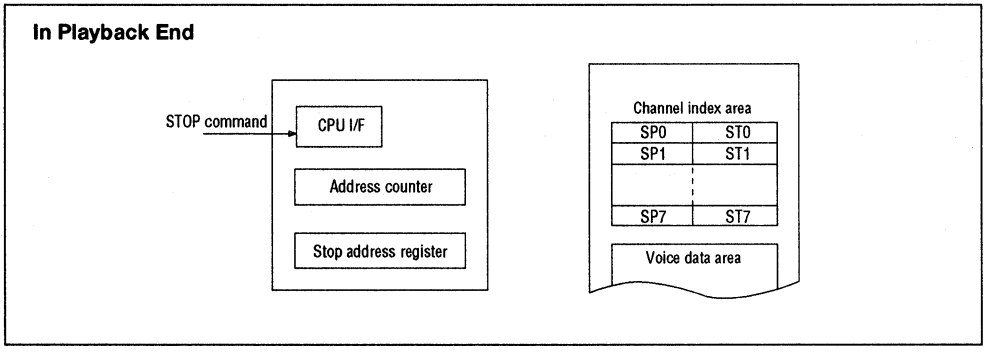


Operation for channel index area in playback is shown below.

When START command is inputted, the playback is started after the START address and STOP address of the channel that designated the channel index area are automatically set to respective address counter and STOP address register.



When STOP command is inputted, the playback finishes. The MSM6388 does not exchange the data with the channel index area.



6. Recording and playback for nine or more channels

When the start and stop addresses of each channel are stored in memory in a microcontroller or external circuitry, recording and playback for nine or more channels is possible. Voice data can be recorded on the same way as for recording described in item 3 above. However, channel 0 must be set.

To play back voice data, enter a STWR command specifying the start address of the voice data area from which to start playback and a SPWR command specifying the stop address of the area to write these addresses in channel 0 field of the channel index area. When a START command is entered, the LSI fetches the start and stop addresses from the channel 0 field in the same way as for playback described in item 4 above, then starts playback.

7. Reading and writing data in external serial voice registers with DTRD and DTWR commands

DTRD and DTWR commands can be used to read from and write to the external serial voice registers.

To read the contents of the serial voice registers, enter an STWR command specifying a start address of the area to be read and an SPWR command specifying a stop address of the area to write these addresses in the channel index area. When a DTRD command is entered, data is read 4bit at a time during each cycle of the sampling frequency.

To write data to the serial voice registers, first write start and stop addresses then enter a DTWR command. Data is written 4bit at a time on the correct RD and WR timings.

Data transfer using DTRD and DTWR commands is performed in 1Kbit units. These two commands can be used to move voice data stored in serial voice registers to different addresses, providing a useful way to use the memory capacity of the serial voice registers.

8. Recording and playing back voice data through the data bus with EREC and EPLAY commands

Specify the sampling frequency with a SAMP command, and input an EREC command.

When an EREC command is entered, the LSI enters the recording mode and recording starts.

Voice data (ADPCM data) is output to the data bus on the correct $\overline{RD}$ and $\overline{WR}$ timings. To stop recording, enter a STOP command on the correct timing.

To perform playback, enter an EPLAY command. The LSI enters the playback mode and starts to play back voice data–the data is input from the data bus on the correct WR timing. To stop playback, enter a STOP command.

During execution of an EREC or EPLAY command, address management and external serial voice register driving are not performed.

9. Initialization by the INIT command

When an INIT command is entered, the channel memory is set in the unrecorded state.

- The INIT command writes the last address of the external serial voice registers as the start and stop addresses in individual fields of channels 0 to 7 in the channel index area. This sets the channel memory in the unrecorded state.
- The command then sets channel 0 in the channel register.

10. Power down function (pin PD)

When pin PD is set at the high level, the LSI enters the power down state. Note that this function is invalid during recording or playback.

- Oscillation is stopped and all operation of the internal circuitry is stopped.
- Data bus pins D0 to D3 are set in the high impedance state.
- Output pins $\overline{CS1}$ to $\overline{CS4}$ are set at the high level, minimizing the current required by the external serial voice registers.

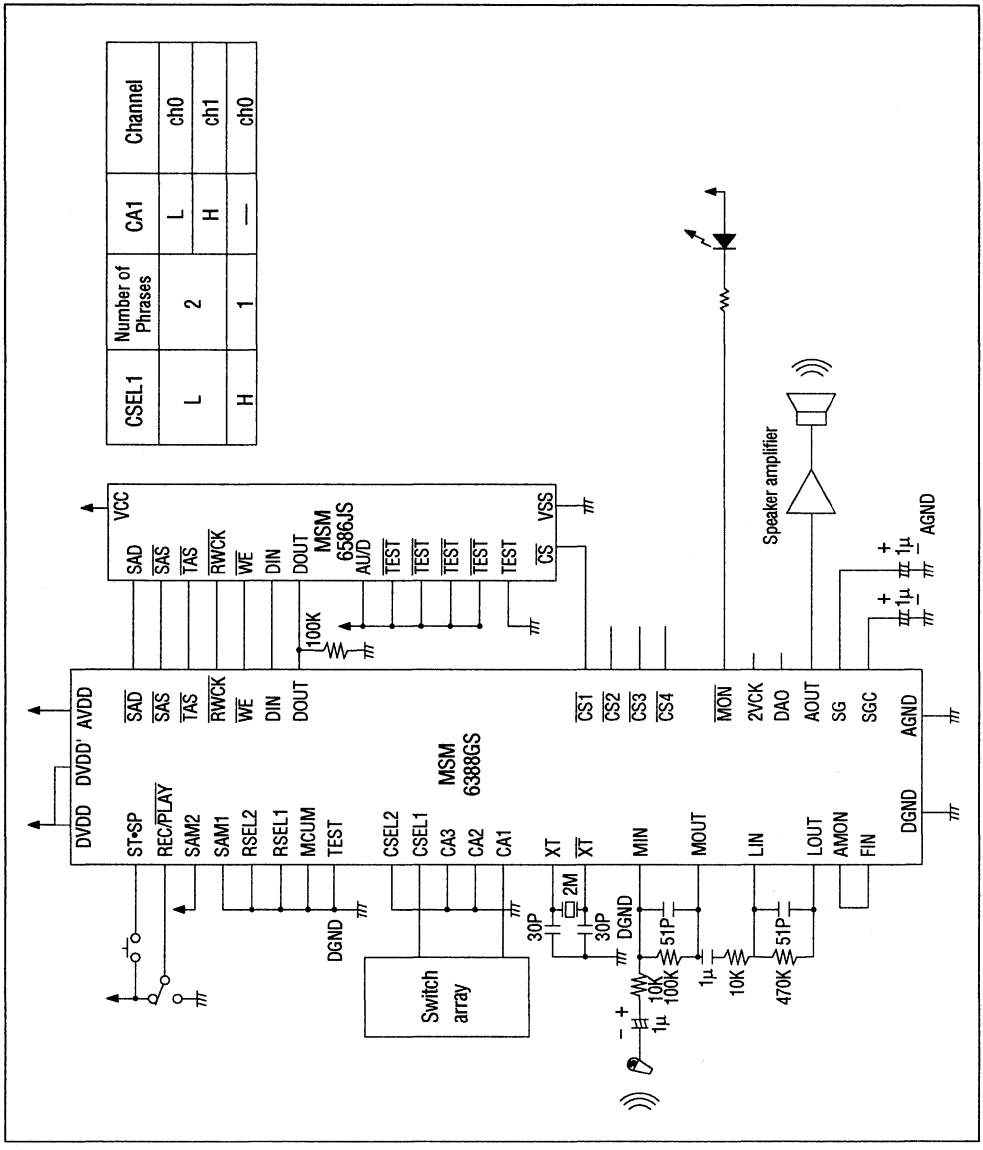
  D0~D3 ..... H~Z
  SAD, $\overline{SAS}$, $\overline{TAS}$, $\overline{WE}$, DIN,
  $\overline{RWCK}$, $\overline{CS1}$~$\overline{CS4}$ ..... "H"
  2VCK, MCK ..... "L"
  AOUT, DAO, SGC ..... GND level

11. Command enable function (pin $\overline{CE}$)

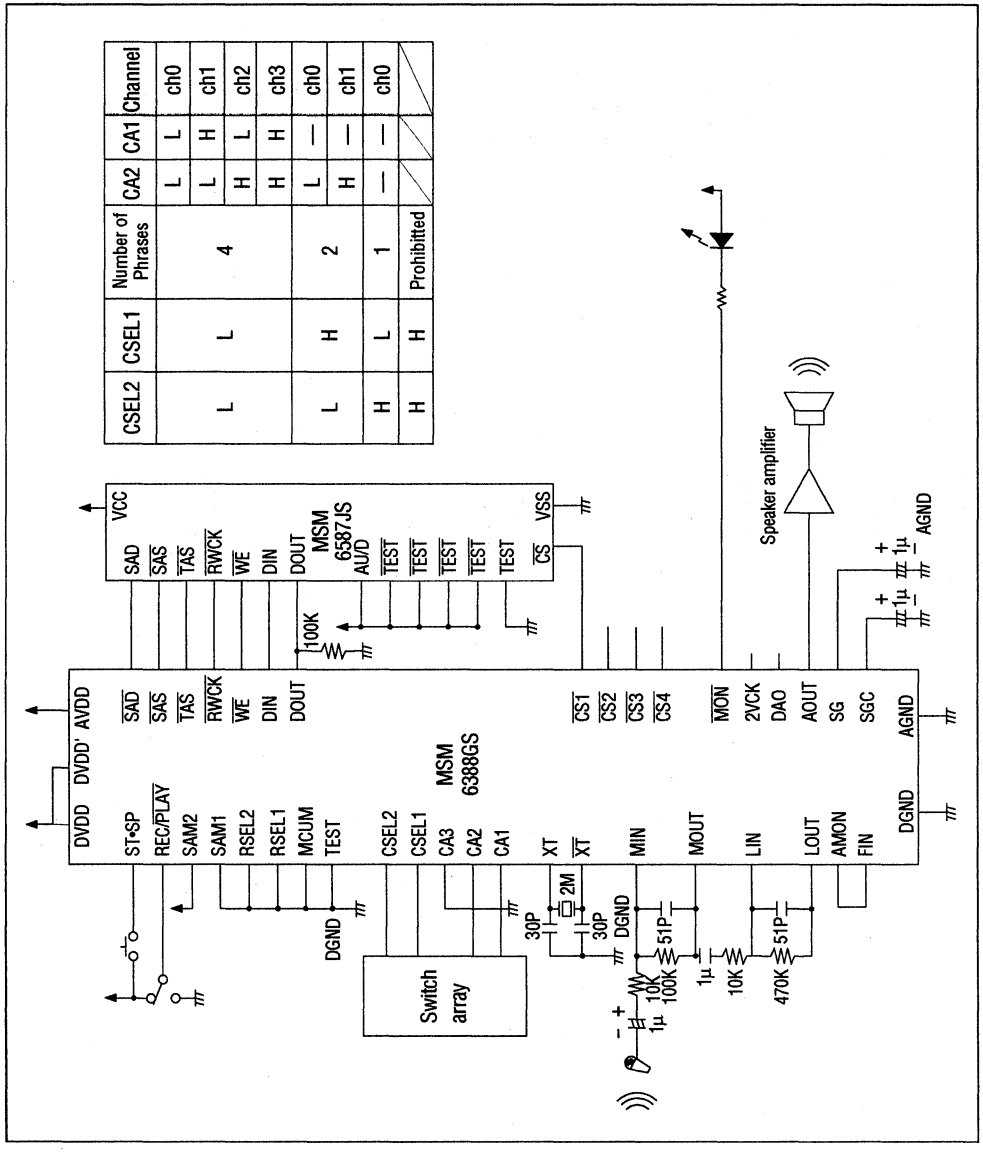
When the pin $\overline{CE}$ is set at the high level, the LSI enters the command enable state, rejecting $\overline{RD}$ and $\overline{WR}$ pulses. In this state, data bus pins D0 to D3 are set in the high impedance state.

SAMPLE APPLICATION CIRCUITS

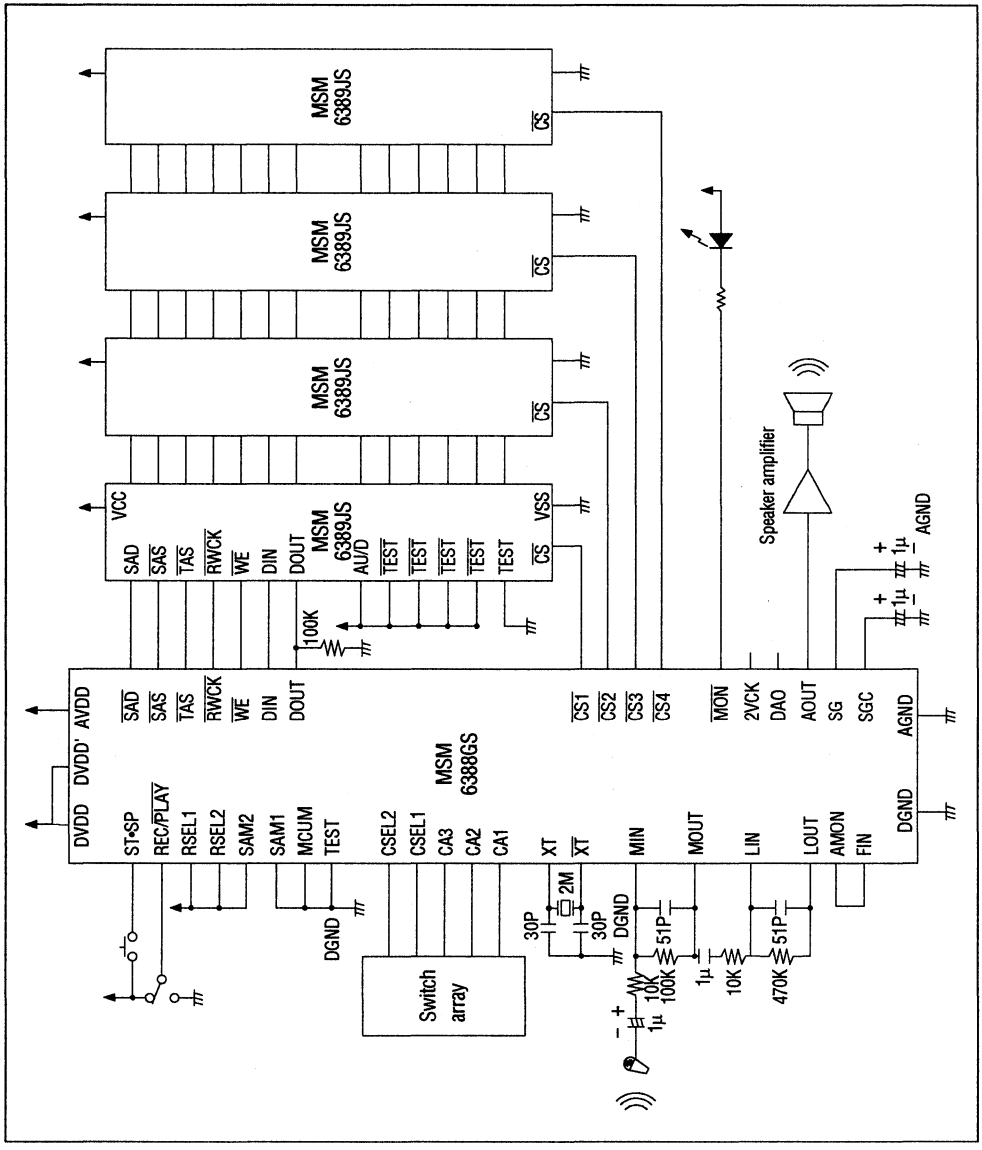
- The circuit diagram 1 shows an example of an application's circuit with the MSM6388 and one 256Kbit serial voice register
- The circuit diagram 2 shows an example of an applications's circuit with the MSM6388 and one 512Kbit serial voice register.
- The circuit diagram 3 shows an example of an application's circuit with the MSM6388 and four 1Mbit serial voice registers.
- Circuit diagram 4 shows an example of the interface with the MSM80C51 when the MSM6388 is used with a microcomputer interface.
- Circuit diagram 5 shows an example of an application using greater than 4-1Mbit serial voice register's with the MSM6388.
- Circuit diagram 6 shows an example of an application's circuit for recording and playback by the EREC and EPLAY commands of the MSM6388.



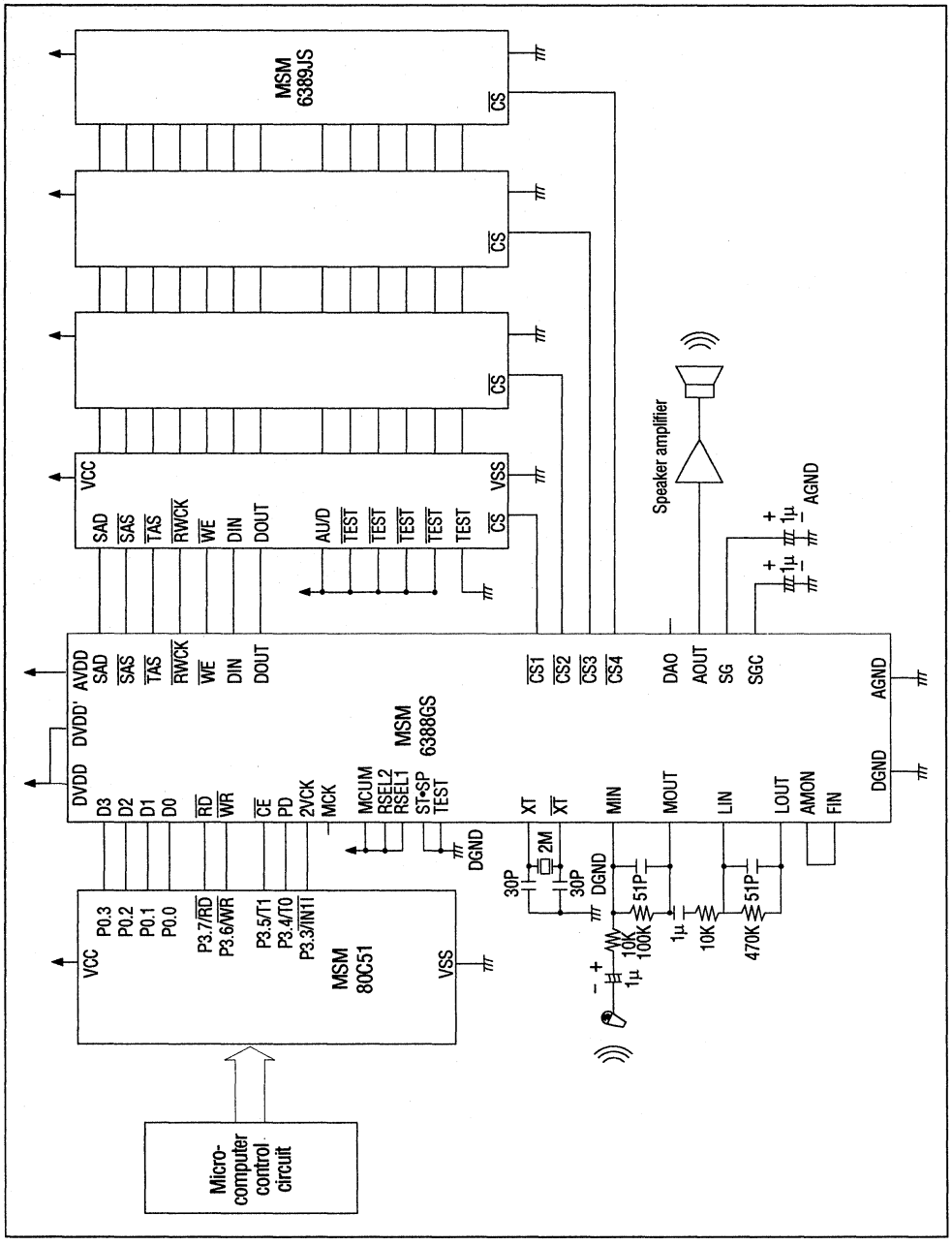
Circuit Diagram 1



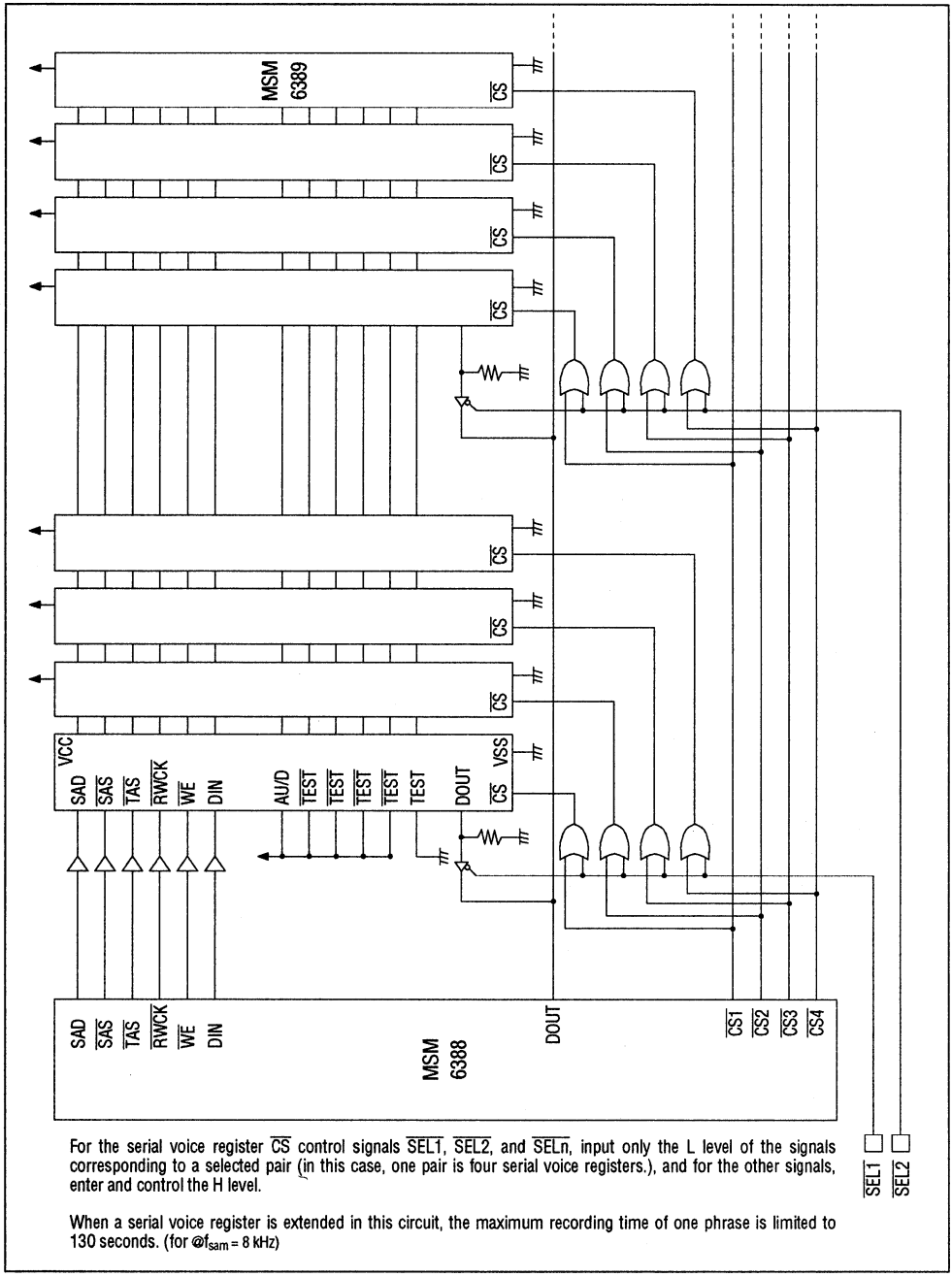
Circuit Diagram 2



Circuit Diagram 3



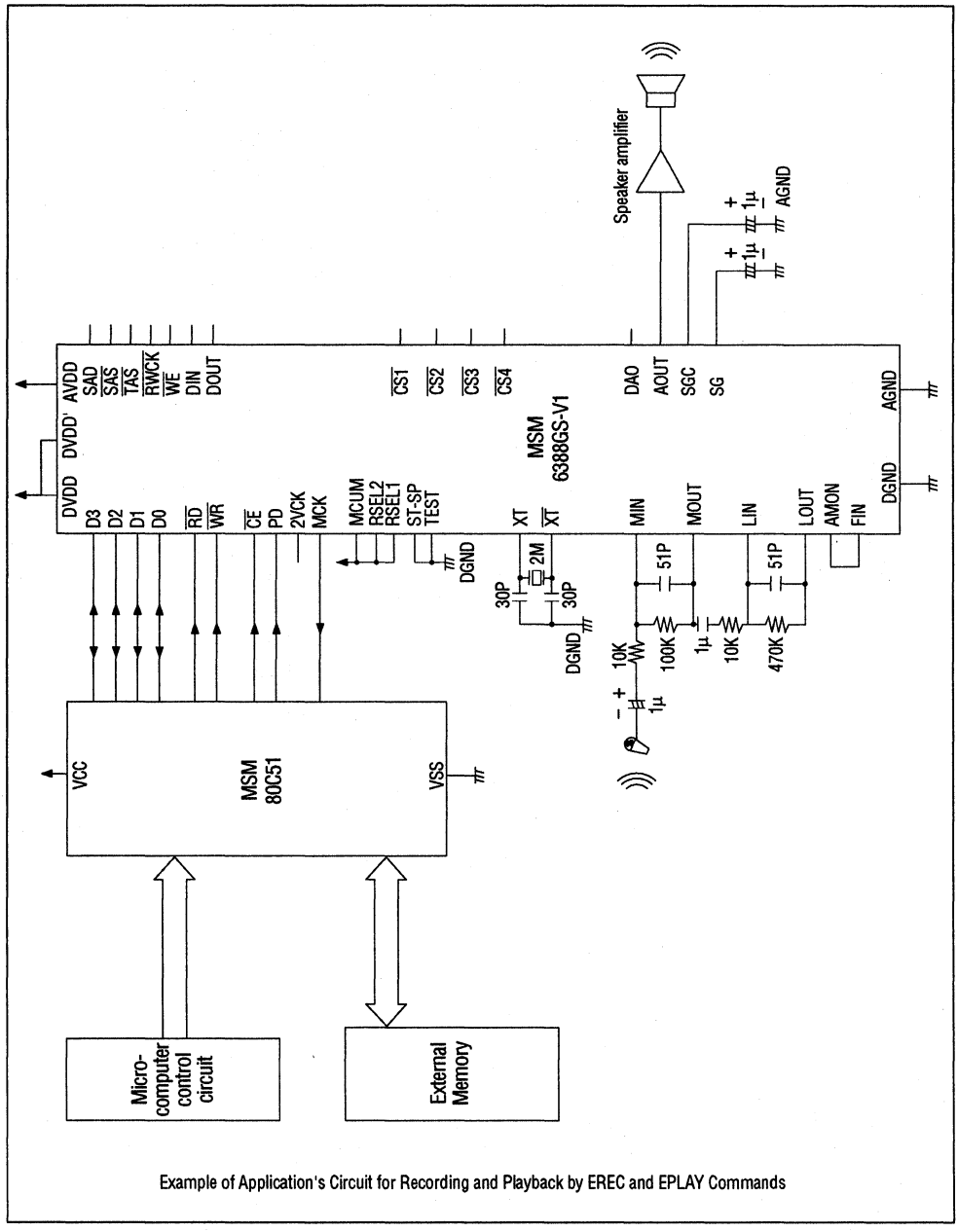
Circuit Diagram 4



For the serial voice register $\overline{CS}$ control signals $\overline{SEL1}$, $\overline{SEL2}$, and $\overline{SELn}$, input only the L level of the signals corresponding to a selected pair (in this case, one pair is four serial voice registers.), and for the other signals, enter and control the H level.

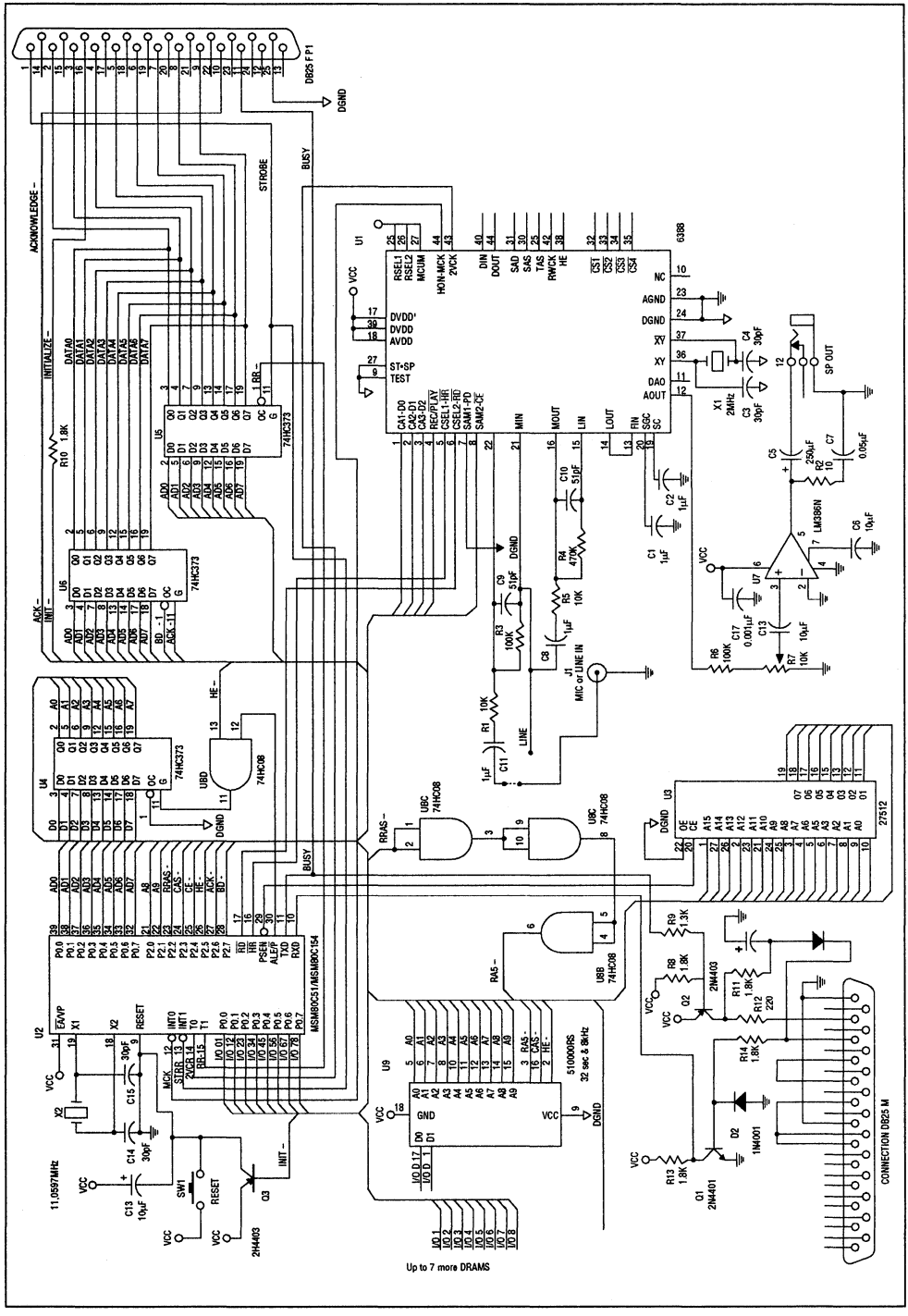
When a serial voice register is extended in this circuit, the maximum recording time of one phrase is limited to 130 seconds. (for @f_{sam} = 8 kHz)

Circuit Diagram 5

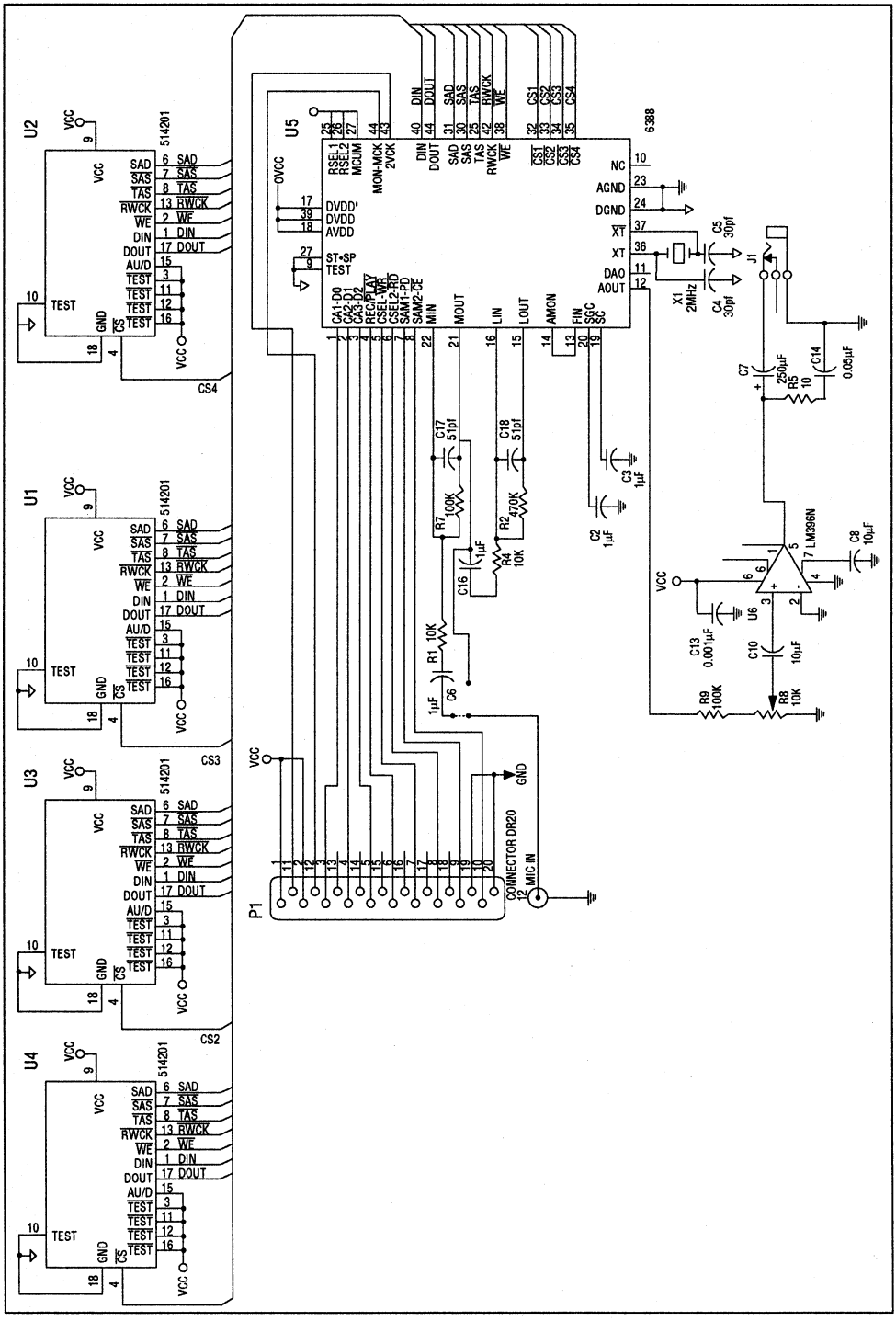


Example of Application's Circuit for Recording and Playback by EREC and EPLAY Commands

Circuit Diagram 6



MSM6388 with 80C154 and DRAMS



MSM6388 Development System

MSM6588

CONTENTS

OKI Semiconductor

MSM6588

ADPCM SOLID-STATE RECORDER

GENERAL DESCRIPTION

The MSM6588 is a "solid-state recorder" LSI developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker amplifier and a serial voice register or other Memory device to store ADPCM data, it can record and playback voice data similar to a tape recorder.

The MSM6588 has a stand-alone mode and a microcontroller interface mode. In stand-alone mode, record/playback can be selected from a pin and it is possible to control the MSM6588 by a simple drive timing. In microcontroller interface mode, record/playback can be controlled by commands from the microcontroller in microcontroller mode, the MSM6588 is much more flexible than in stand-alone operation.

In addition, Recording and Playback with fixed message are easily implemented by connecting a serial voice ROM.

FEATURES

- 12bit AD converter
- 12bit DA converter
- Microphone amplifier
- Low pass filter (LPF)
  Filter characteristics –40dB/oct
- Serial voice registers
  1Mbit serial voice register
  (MSM6389): (4) directly addressable
  512Kbit serial voice register
  (MSM6587): (1) directly addressable
  256Kbit serial voice register
  (MSM6586): (1) directly addressable
- Serial Voice ROMs
  1Mbit serial voice ROM
  (MSM6595-XXX)
  2Mbits serial voice ROM
  (MSM6596-XXX)
  3Mbits serial voice ROM
  (MSM6597-XXX)
- Maximum recording time
  262 seconds (when using 3bit ADPCM, 5.3kHz sampling)
- Voice triggered starting
- Pause function
- Master clock frequency: 4.096MHz ~ 8.192MHz
- Power Supply voltage: 5 V
- Package: 44 pin plastic QFP
  (QFP44-P-910-V1K)

1. Characteristics in stand-alone mode
   - 3bit ADPCM
   - Sampling frequency:
     5.3kHz or 8.0kHz
     (when the oscillator operates at 4.096MHz)
     10.6kHz or 16.0kHz
     (when the oscillator operates at 8.192MHz)
   - Number of Phrases: 1,2,4 or 8
2. Characteristics in microcontroller interface mode
   - 3bit/4bit ADPCM selectable
   - Sampling frequency:
     4.0kHz, 5.3kHz, 6.4kHz or 8.0kHz
     (when the oscillator operates at 4.096MHz)
     8.0kHz, 10.6kHz, 12.8kHz or 16.0kHz
     (when the oscillator operates at 8.192MHz)
   - Condition setting, start, and stop of record/playback controllable by 13 commands.

Functional Comparisons of MSM6388 and MSM6588

		MSM6388	MSM6588
ADPCM bit length	S/A	4 bit	3 bit
	MCU	4 bit	3 bit/4 bit selectable
Recording system	S/A	Fixed mode	Fixed mode Flex mode
	MCU	Direct mode	Direct mode Fixed mode Flex mode
Original oscillating frequency		1.5MHz ~ 4.0MHz (S/A) (1.5 ~ 8.192MHz) (MCU)	4.0MHz ~ 8.192MHz (TYP 4.096MHz)
Sampling frequency	S/A	4 selections	2 selections
	MCU	6 selections	4 selections
Others		Maximum sampling frequency: 32kHz	Voice triggered recording, pause function Forced $\overline{\text{RESET}}$ terminal Built-in LPF independent driving available Maximum sampling frequency: 16kHz Reduction of command processing time

Note: S/A ····· Stand-alone mode
MCU ····· Microcomputer interface mode
— Switchover is available by setting the input and output terminals.

1. ADPCM-bit length

MSM6588 can select 3 bit/4 bit

Example: In the case of bit rate 16 kbps

4 bit ADPCM: 4 bit × 4 kHz = 16 kbps

3 bit ADPCM: 3 bit × 5.3 kHz = 16 kbps

2. Record and playback can be temporarily suspended by the pause function.

3. Voice triggered recording

4. Addition of forced $\overline{\text{RESET}}$ terminal

5. LPF external driving available

Built-in LPF can be used in as single unit.

When LPF is used for another circuit, the LPF of a MSM6588 is available for common use.

6. Reduction of command processing time

Command processing time in microcontroller-interface mode is reduced.

Example:
1 nibble command: 256 µsec → 16 µsec
Address input: 2300 µsec → 640 µsec

7. Addition of flex mode to recording system

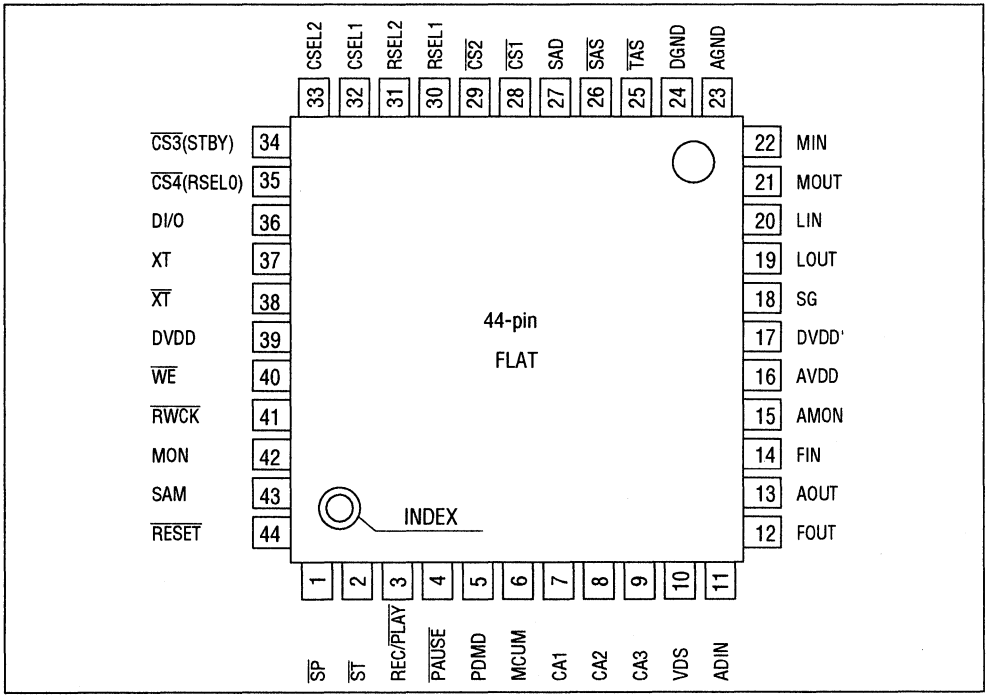
Fixed mode: The memory capacities of serial voice registers are divided by equally for the number of channels assigned.

Flex mode: The memory capacities assigned to each channel become arbitrary. ch0, ch1 and so on are recorded one by one within the range of the memory capacities for the serial voice register.

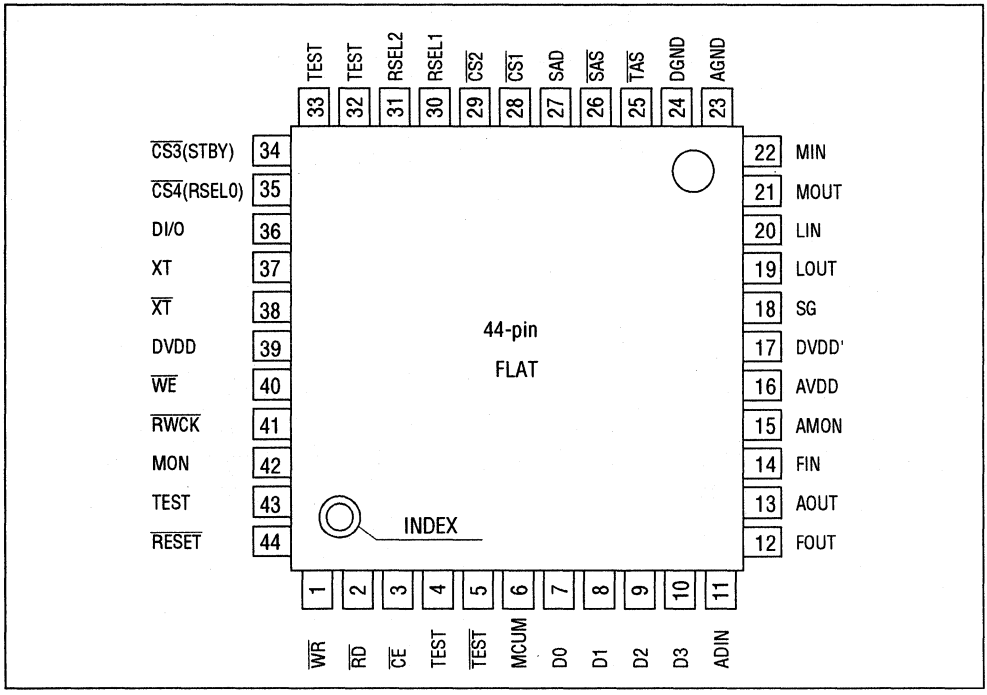
Direct mode: The memory capacities of each channel is directly assigned. The allocation of the memory capacities are free and the address is controlled by a microcontroller.

PIN LAYOUT (Top View) 44 Lead Plastic QFP

1. Stand-alone mode (MCUM pin = "L")



2. Microcontroller interface mode (MCUM pin = "H")



Selection of stand-alone mode or microcontroller interface mode is controlled by the level of the MCUM pin.

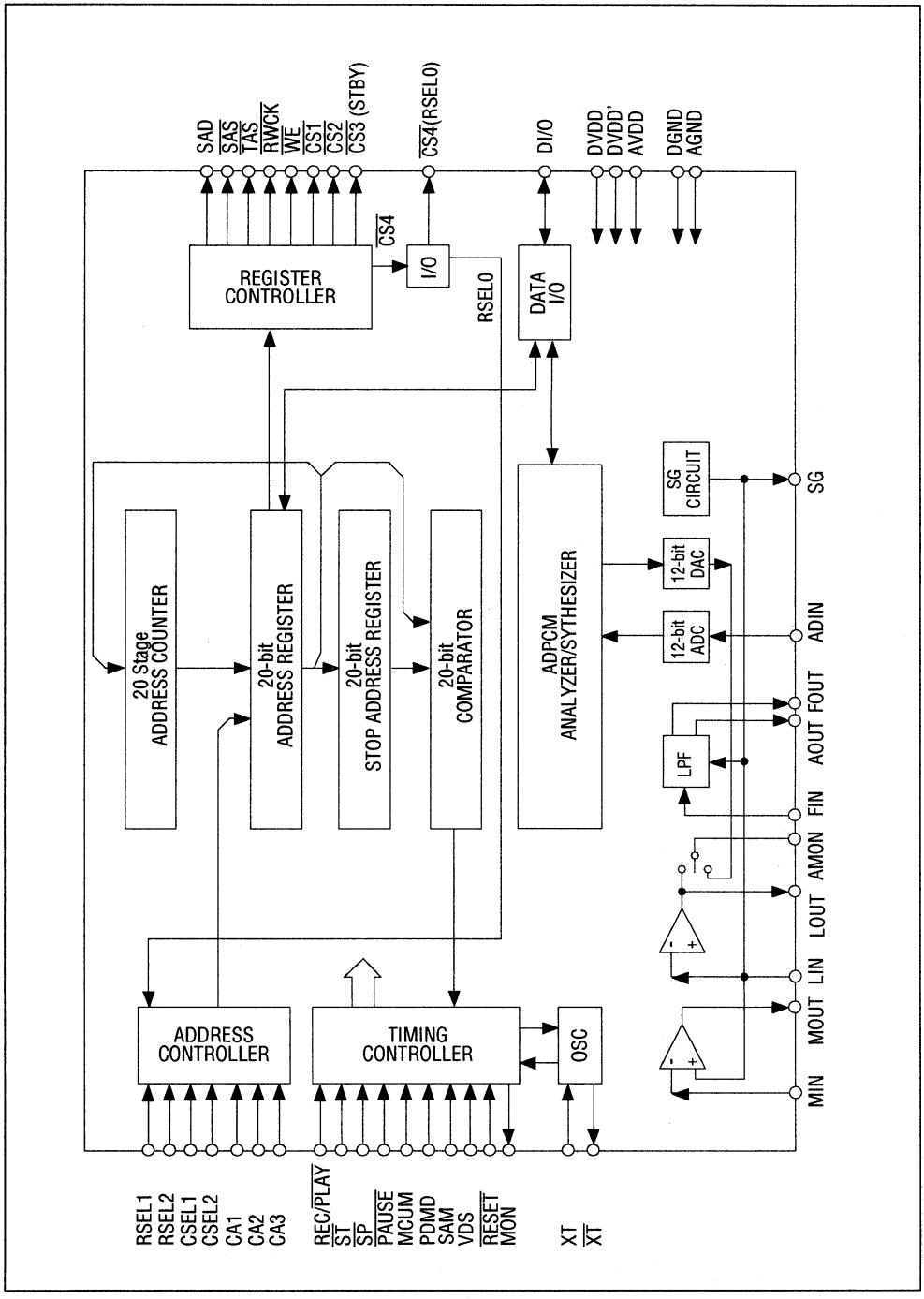
MCUM="L": stand-alone mode

MCUM="H": microcontroller interface mode

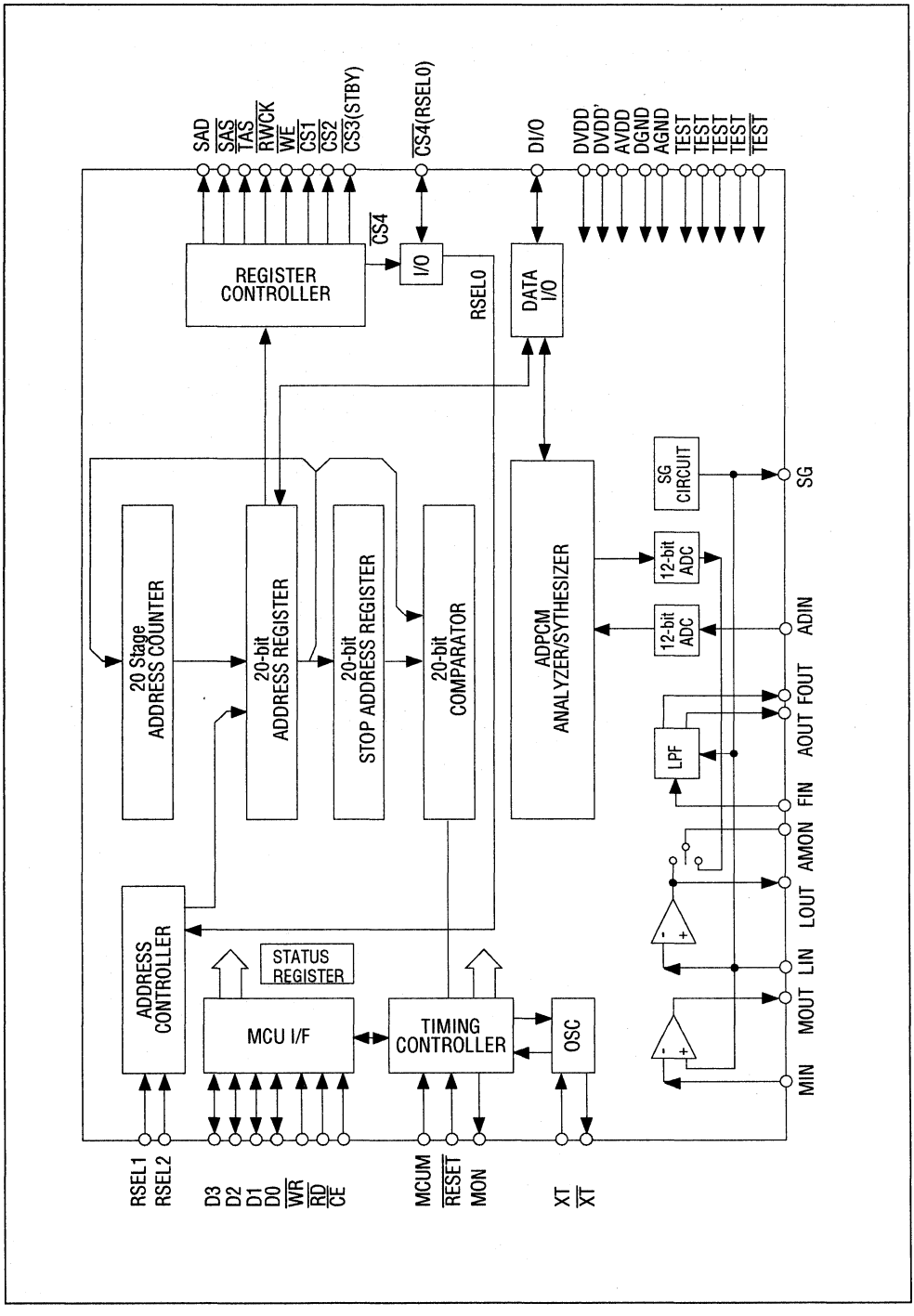
ELECTRICAL CHARACTERISTICS

BLOCK DIAGRAM

Stand-Alone Mode



Microcontroller Interface Mode



EXPLANATION OF FUNCTIONS

• Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

• Operating Range

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	+0.3 ~ +5.5	V
Operating temperature	T_{stg}	—	−40 ~ +85	°C
Master clock frequency	f_{OSC}	—	4.0 ~ 8.192	MHz

• DC Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=–40~+85°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.8 × VDD	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.2 × VDD	V
"H" output voltage	V_{OH}	I_{OH} = –40μA	4.2	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" input current (Note 1)	I_{IH1}	V_{IN} = VDD	—	—	10	μA
"H" input current (Note 2)	I_{IH2}	V_{IN} = VDD	—	—	20	μA
"L" input current (Note 3)	I_{IL1}	V_{IL} = GND	–10	—	—	μA
"L" input current (Note 2)	I_{IL2}	V_{IL} = GND	–20	—	—	μA
"L" input current (Note 4)	I_{IL3}	V_{IL} = GND	–400	—	–20	μA
Operating power consumption (1)	I_{DD}	f_{OSC} = 8MHz, no load	—	7	15	mA
Operating power consumption (2)	I_{PD}	When power down, no load Ta = –40 ~ +70°C	—	—	10	μA
		When power down, no load Ta = +70 ~ +85°C	—	—	50	μA

Note 1: Applicable to all input pins, excluding the XT pin.
Note 2: Applicable to the XT pin.
Note 3: Applicable to all input pins without pull-up resistors, excluding the XT pin.
Note 4: Applicable to input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$) with pull-up resistors, excluding the XT pin.

• Analog Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V, DGND=AGND=0V Ta=–40~+85°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{PIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0 ~ 4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

• AC Characteristics

1. Common characteristics in stand-alone and microcontroller interface mode

DVDD=DVDD'=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C
When f_{sam}=8kHz

Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ pulse width	t_{RST}	1	—	—	μs
$\overline{\text{RESET}}$ execution time (Note 1)*	t_{REX}	—	125	—	μs

Note: * is proportional to the period of sampling frequency (f_{sam}).
1) The oscillation stable time is added to t_{REX}.
The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a μs for ceramic oscillators.

2. Stand-alone mode

The AC characteristic values of stand-alone mode are proportional to the period of the sampling frequency (f_{sam}).

DVDD=DVDD'=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C
When fsam=8kHz

Item		Symbol	Min.	Typ.	Max.	Unit
$\overline{ST}$ pulse width (Note 1)		t_{ST}	40	—	—	µs
$\overline{SP}$ pulse width		t_{SP}	40	—	—	µs
$\overline{PAUSE}$ pulse width		t_{PSE}	40	—	—	µs
Hold time of CA1, CA2, CA3, REC/$\overline{PLAY}$ for MON rise		t_{CAH}	1	—	—	ms
Address control time at the start of record/playback		t_{AD1}	—	1	—	ms
Address control time at the end of recording		t_{AD2}	—	1	—	ms
Time until the release of voice activation function after input of $\overline{SP}$ pulse during voice standby		t_{SPV}	—	—	500	µs
Silence during repeated playback		t_{MID}	—	1.5	—	ms
Time from input of $\overline{PAUSE}$ pulse until pause		t_{PP}	—	—	250	µs
Time from input of $\overline{ST}$ pulse to the continuation of record/playback during pause		t_{PSP}	—	—	500	µs
PDMD =L	Oscillator stable time after input of $\overline{ST}$ pulse	t_{ANA}	—	32	—	ms
	$\overline{SP}$ pulse (during recording) to the fall of MON	t_{SPM1}	—	—	1	ms
	$\overline{SP}$ pulse (during playback) to the fall of MON	t_{SPM2}	—	—	260	ms
	Standby transient time at start of playback	t_{AOR}	—	64	—	ms
	Standby transient time at end of playback	t_{AOF}	—	256	—	ms
	Time from fall of MON to power down state at the end of playback	t_{MS}	—	70	—	µs
	$\overline{SP}$ pulse during pause to record end	t_{PSP1}	—	—	1	ms
	$\overline{SP}$ pulse during pause to playback end	t_{PSP2}	—	—	260	ms
PDMD =H	$\overline{ST}$ pulse to MON rise	t_{STM}	—	—	1	ms
	$\overline{SP}$ pulse to MON fall	t_{SPM1}	—	—	1	ms
	Voice activation standby state	t_{STV}	—	—	1	ms
	SP pulse during pause to record/playback end	t_{PSP1}	—	—	1	ms

Note: 1) When the PDMD pin is "L", the oscillation stable time is added to t_{ST}. The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a micro Sec for ceramic oscillators.

3. Microcontroller interface mode

DVDD=DVDD'=AVDD=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C
When f_{sam}=8kHz

Item		Symbol	Min.	Typ.	Max.	Unit
$\overline{RD}$ pulse width		t_{RR}	200	—	—	ns
Setup and hold time of $\overline{CE}$ for $\overline{RD}$		t_{CR}	30	—	—	ns
Data valid from fall of $\overline{RD}$		t_{DRE}	—	—	200	ns
Data Hi-Z from rise of $\overline{RD}$		t_{DRF}	—	10	50	ns
$\overline{WR}$ pulse width		t_{WW}	200	—	—	ns
Setup and hold time of $\overline{CE}$ from $\overline{WR}$		t_{CW}	30	—	—	ns
Data set up time to rise of $\overline{WR}$		t_{DWS}	100	—	—	ns
Data Hold time from rise of $\overline{WR}$		t_{DWH}	30	—	—	ns
Disable time for $\overline{RD}$ and WR		t_{DRW}	250	—	—	ns
BUSY time after release of $\overline{RESET}$ (Note 1)	*	t_{BR}	—	—	125	µs
BUSY time after input of 1 nibble command	*	t_{B1}	—	—	16	µs
BUSY time after input of 2 nibble command	*	t_{B2}	—	—	16	µs
BUSY time after input of 2 nibble command data	*	t_{BD}	—	—	16	µs
BUSY time after input of ADRWR command	*	t_{BAW}	—	—	270	µs
BUSY time after input address data of ADRWR command	*	t_{BAD}	—	—	50	µs
Data input time after input of ADRRD command	*	t_{WAR}	270	—	—	µs
Time between output of address data nibbles during ADRRD command	*	t_{WDR}	50	—	—	µs

Note : Items with * are proportional to the period of sampling frequency f_{sam}.

: 1) The oscillation stable time is added to t_{BR}.
The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a micro Sec for ceramic oscillators.

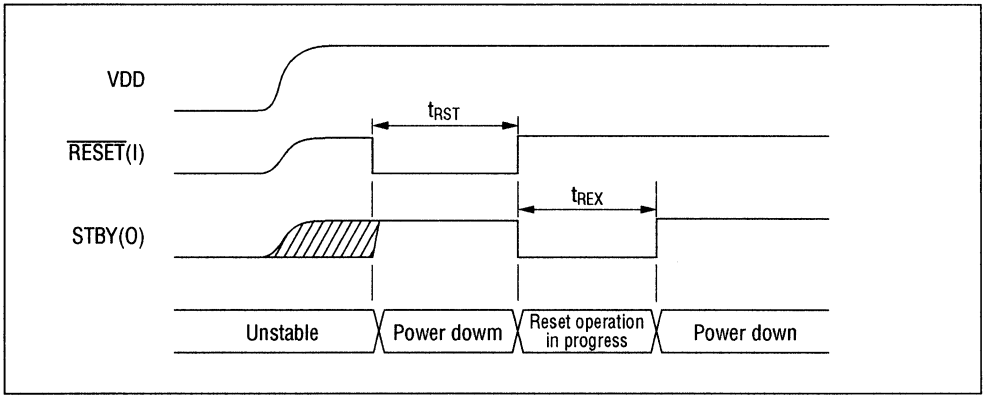
Item		Symbol	Min.	Typ.	Max.	Unit
Address control time at start of record/playback *		t_{AD1}	—	1	—	ms
Address control time at end of recording *		t_{AD2}	—	1	—	ms
START command to rise of MON *		t_{STCM}	—	—	1	ms
STOP command to fall of MON *		t_{SPCM}	—	—	1	ms
START command to RPM bit set ("H" level)		t_{STCR}	—	—	16	µs
START command (during voice triggered starting function) to VPM bit set ("H" level) *		t_{STCV}	—	—	16	µs
STOP command to release of standby (during voice triggered starting function) *		t_{SPCV}	—	—	500	µs
PAUSE command to VPM bit set ("H" level) *		t_{PSCP}	—	—	16	µs
START command (during pause) to VPM bit reset ("L" level) *		t_{STCP}	—	—	500	µs
STOP command (during pause) to VPM bit reset ("L" level) *		t_{SPCP}	—	—	500	µs
When DTRW command is being executed	Delay time after input of DTRW command *	t_{WRW}	16	—	—	µs
	Delay time after input of lower 4-bit of × address *	t_{WXA1}	16	—	—	µs
	Delay time after input of middle 4-bit of × address *	t_{WXA2}	16	—	—	µs
	Delay time after input of upper 4-bit of × address *	t_{WXA3}	270	—	—	µs
	Delay time after input of REC command *	t_{WRC}	16	—	—	µs
	Delay time after input of write data *	t_{WWD}	50	—	—	µs
	Delay time after input of PLAY command *	t_{WPL}	50	—	—	µs
	Delay time after input of STOP command *	t_{WSP}	16	—	—	µs
When executimg EXT command	EXT command to rise of MON *	t_{EM}	125	—	330	µs
	"H" level time of MON *	t_{MH}	—	31	—	µs
	"L" level time of MON *	t_{ML}	—	94	—	µs
	MON rise to $\overline{RD}$ pulse rise (during recording) *	t_{ERD}	—	—	120	µs
	MON rise to $\overline{WR}$ pulse rise (during recording) *	t_{EWR}	—	—	120	µs
	STOP command until rise of MON *	t_{ESP}	—	—	100	µs
	STOP command to record/playback end *	t_{WEX}	—	—	250	µs

Note : Items with *are proportional to the period of sampling frequency (f_{sam}).

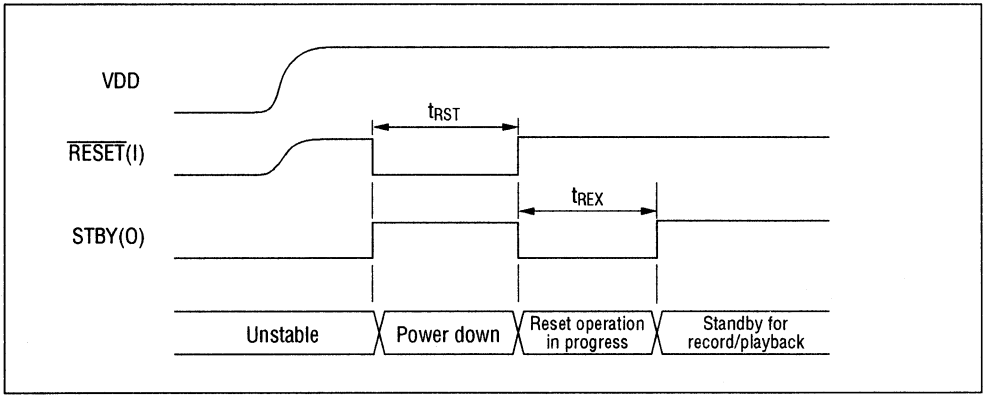
TIMING DIAGRAM

Reset Function and Power Down Function

1. Stand-alone mode when the PDMD pin is "L"

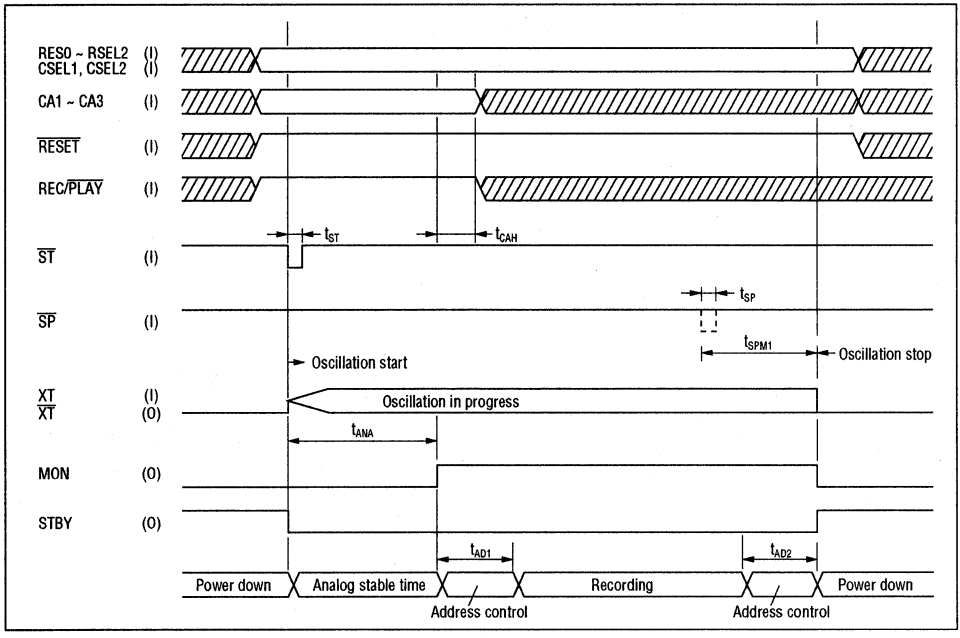


2. Stand-alone mode when the PDMD pin is "H" and in microcontroller interface mode.

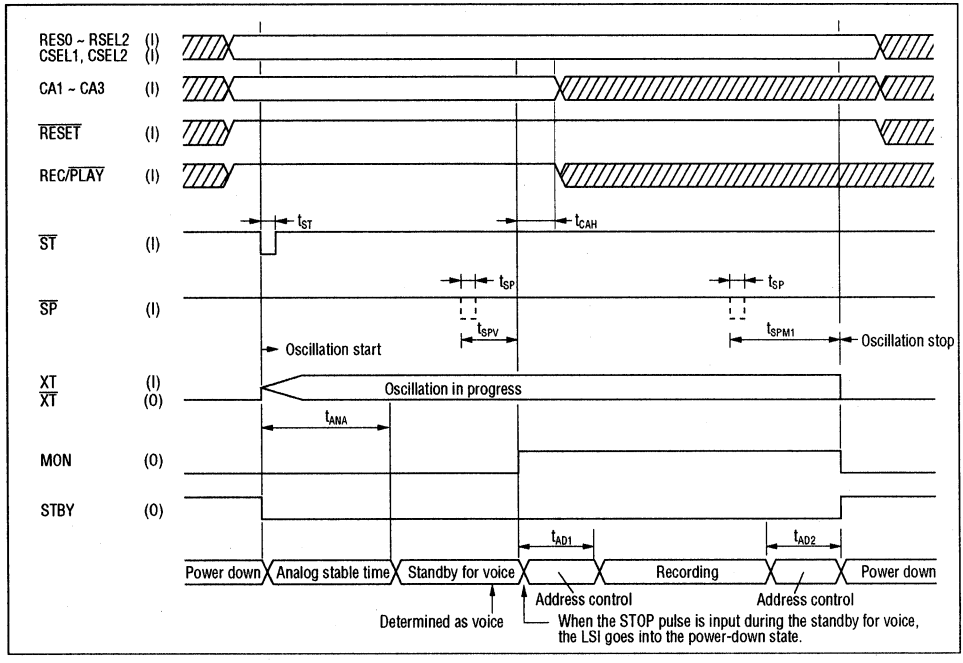


Stand-alone Mode

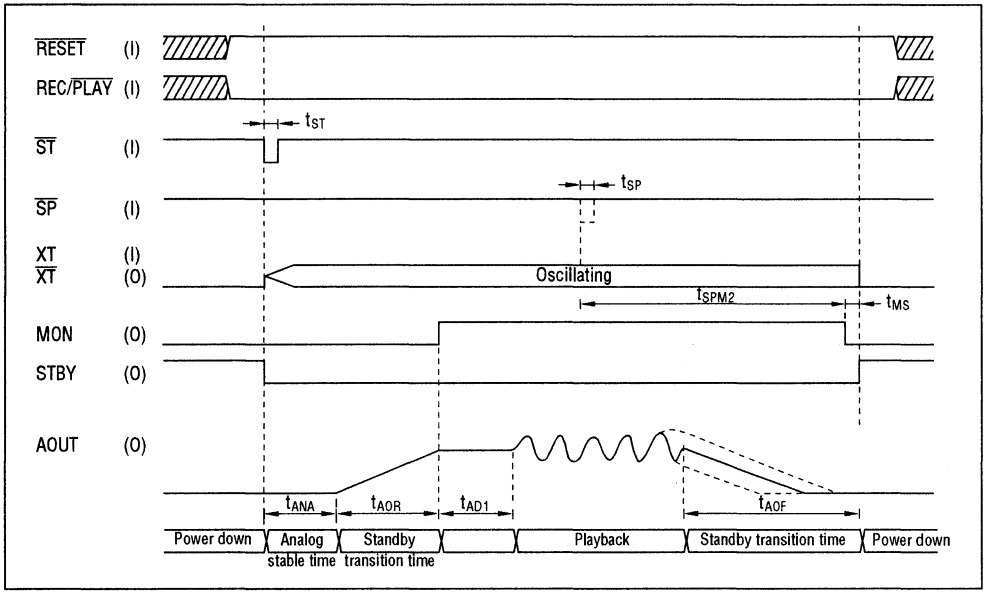
1. Timing during recording (PDMD pin="L", VDS pin="L")



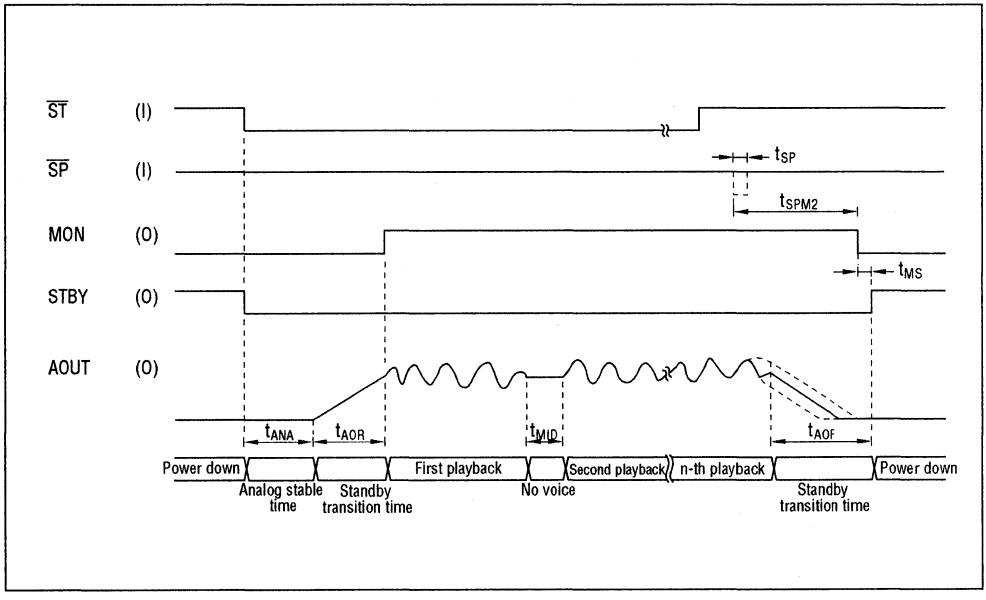
2. Timing during voice triggered starting function on record (PDMD pin="L", VDS pin="H")



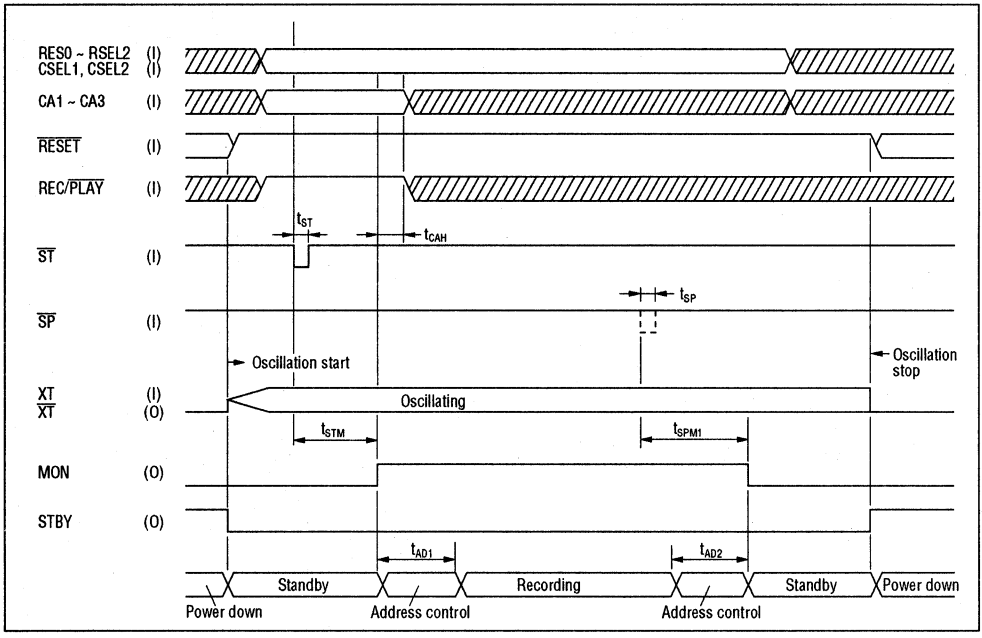
3. Timing during playback (PDMD pin = "L")



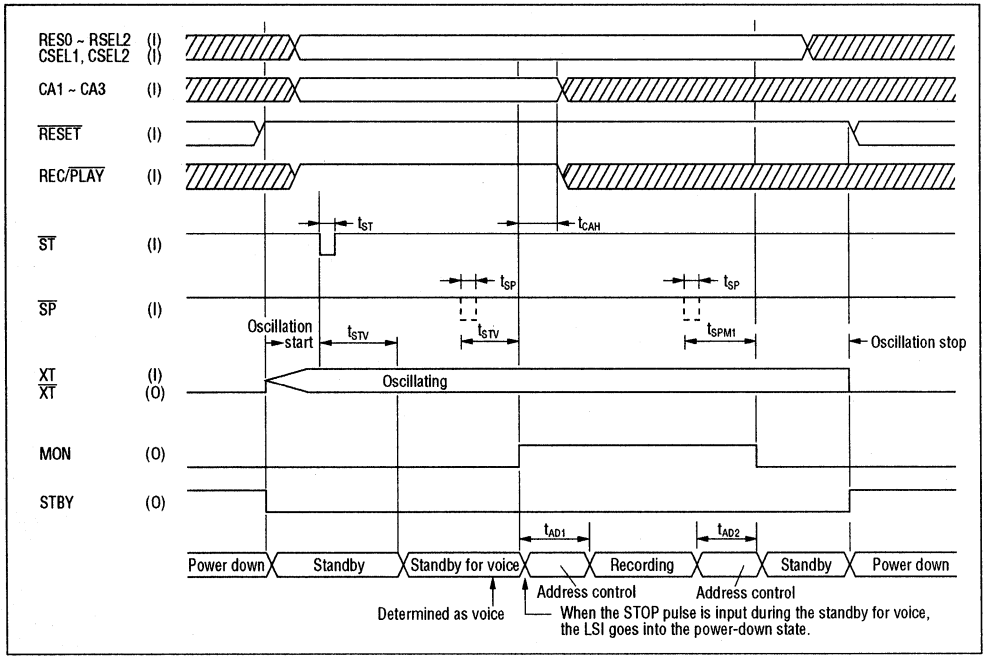
4. Timing during repeated playback (PDMD pin = "L")



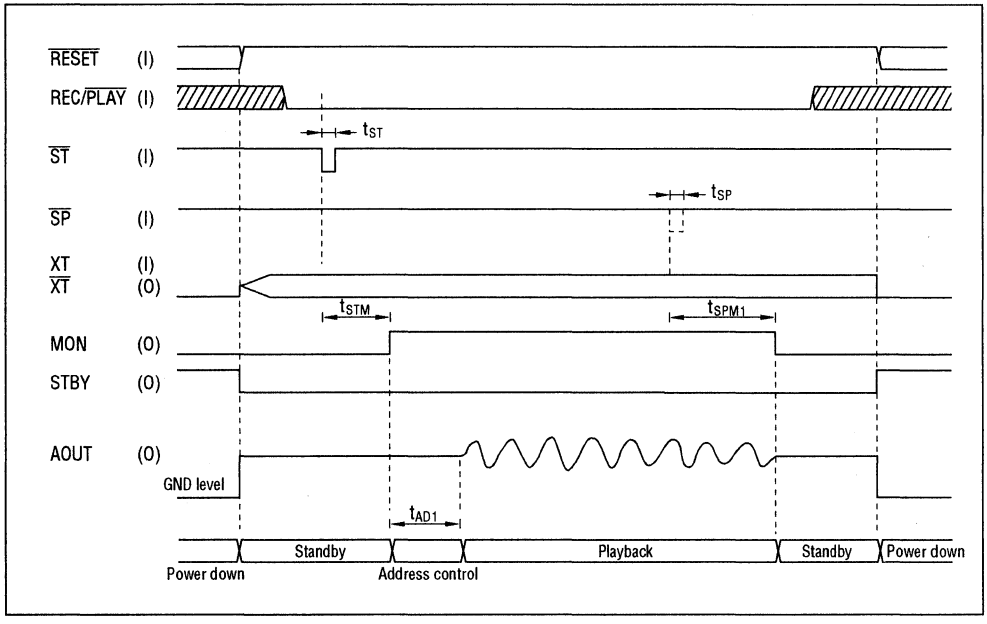
5. Timing during recording (PDMD pin="H", VDS pin="L")



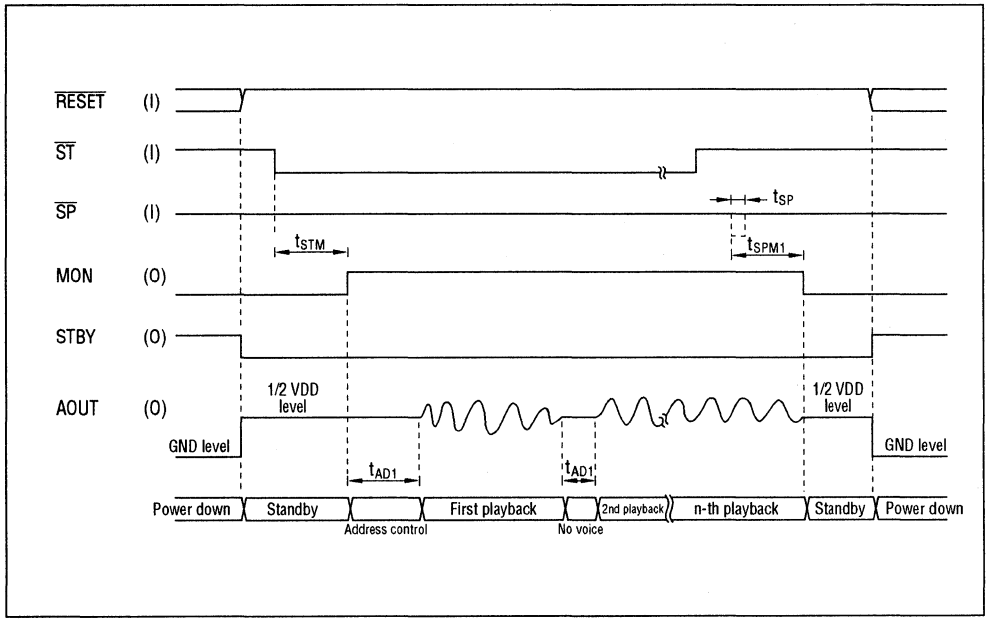
6. Timing during voice triggered starting function on record (PDMD pin="H", VDS pin="H")



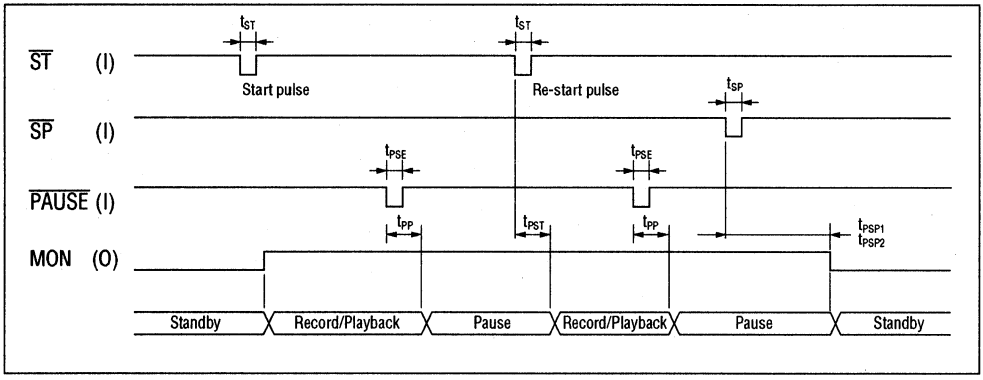
7. Timing during playback (PDMD pin = "H")



8. Timing during repeated playback (PDMD pin = "H")



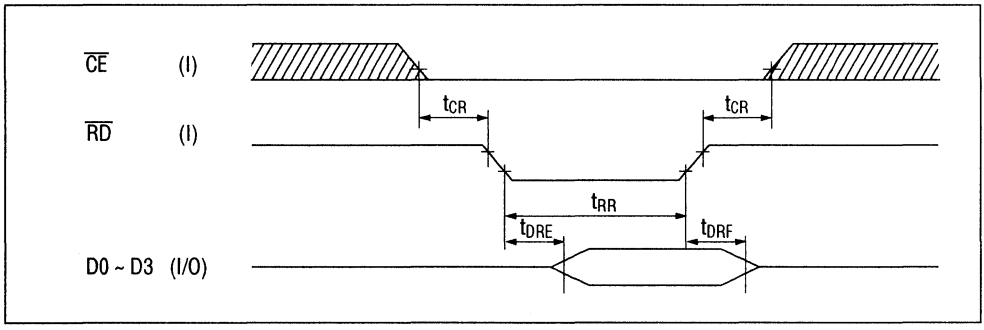
9. Timing of pause in record/playback



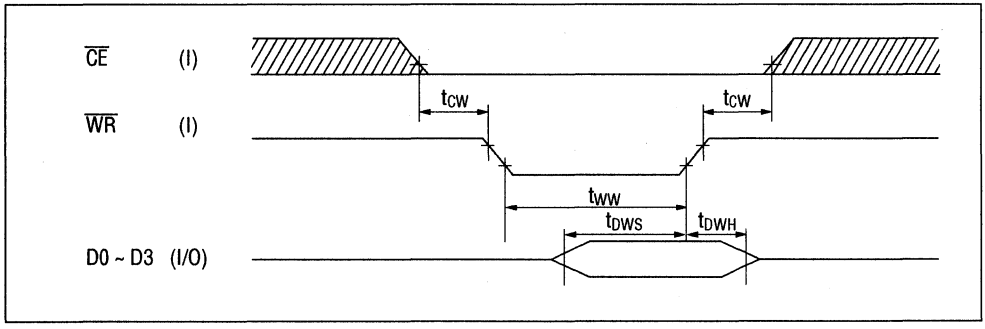
Note: t_{PSP1}------ for recording or playback with the PDMD pin = "H"
t_{PSP2}------ for recording or playback with the PDMD pin = "L"

Microcontroller Interface

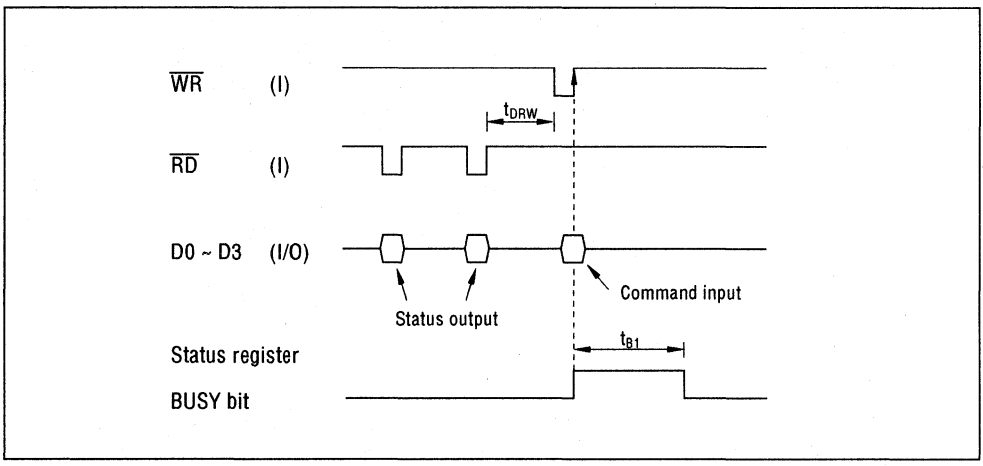
1. Data read ($\overline{RD}$ pulse)



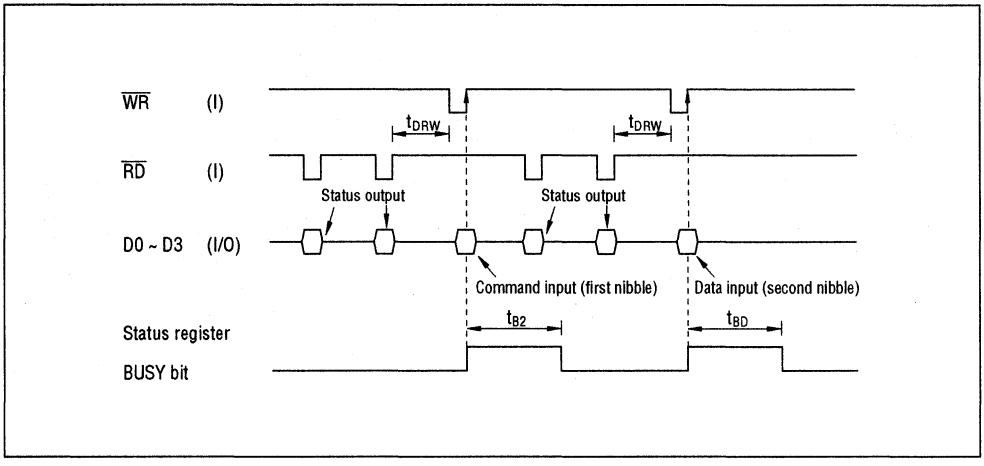
2. Data write ($\overline{WR}$ pulse)



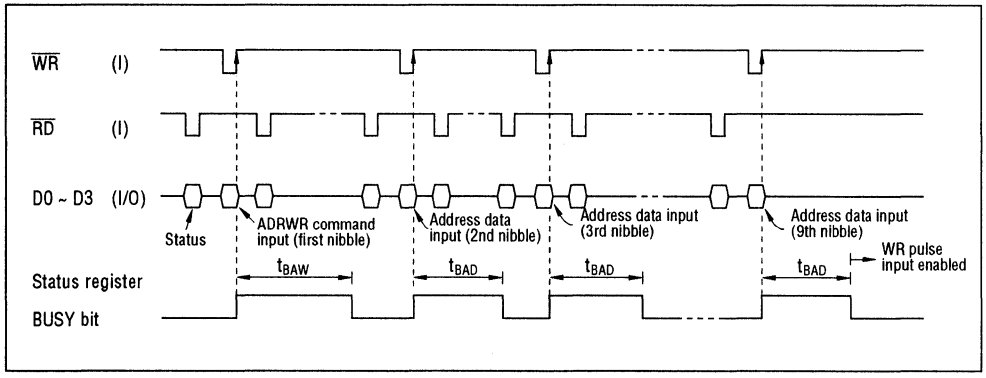
3. Input method of 1 nibble command
(NOP, PAUSE, PLAY, REC, START and STOP commands)



4. Input method of 2 nibble command (SAMP, CHAN and VDS commands)

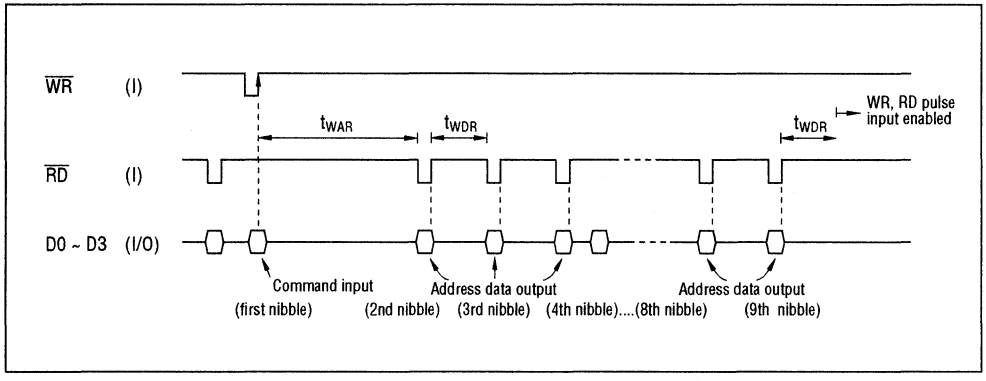


5. Input method of ADRWR command



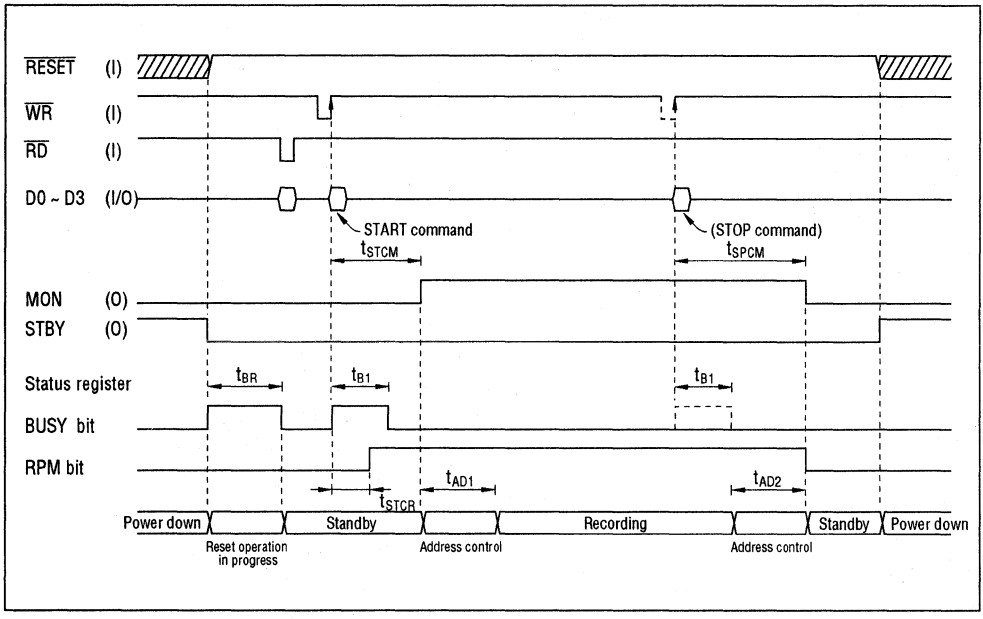
Note 1: In the BUSY bit of the status register, input the command after checking that it is not in the BUSY state.
Note 2: Next, input the address data into 2nd through 9th nibble command, but after checking that the status is not BUSY by either method as follows.
- Check on the BUSY bit of the status register
- Input the next $\overline{WR}$ pulse after the waiting time of t_{BAW} or t_{BAD}

6. Input method of ADRRD command

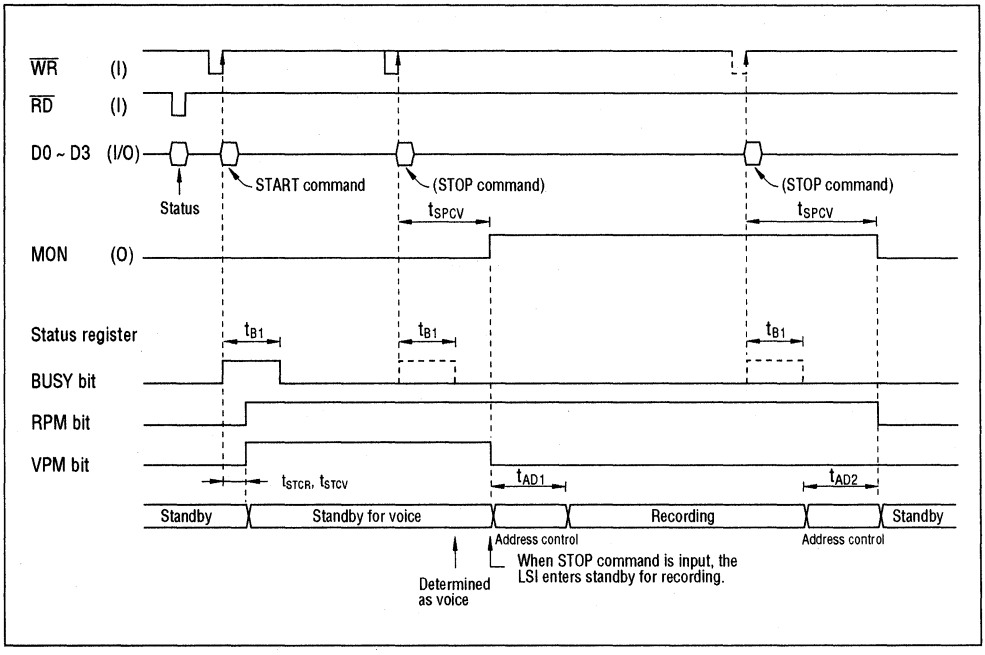


Note 1: In the BUSY bit of the status register, input the command after checking that it is not in the BUSY state.
Note 2: Next, read out the address data into 2nd through 9th nibble command, but this can not check the BUSY bit by the $\overline{RD}$ pulse input. Input the next $\overline{RD}$ pulse after the waiting time of t_{WAR} or t_{WDR}.

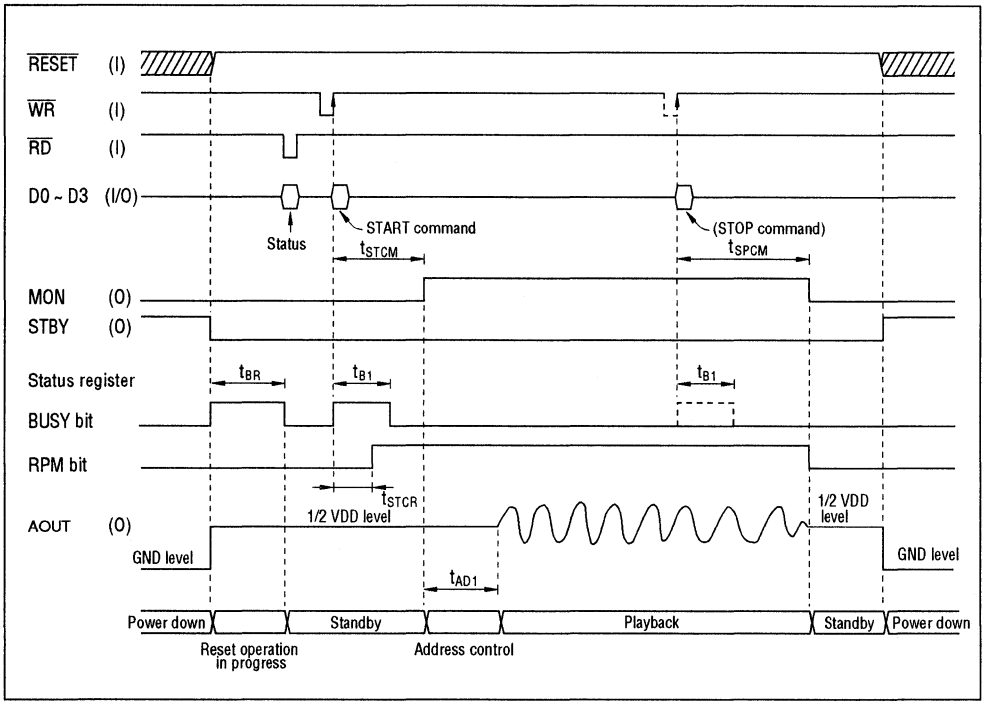
7. Recording method by START command



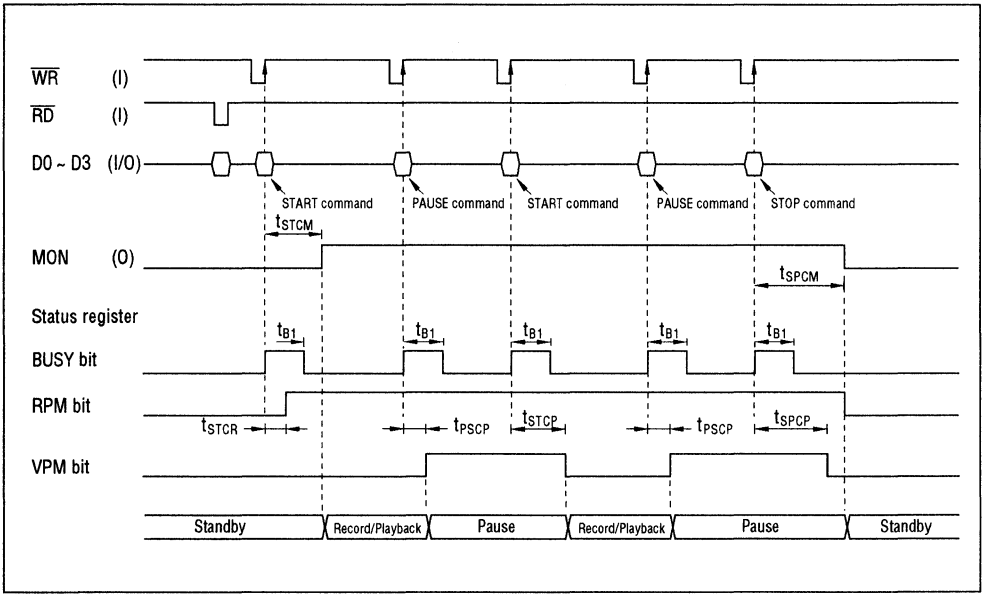
8. Timing of voice triggered starting function



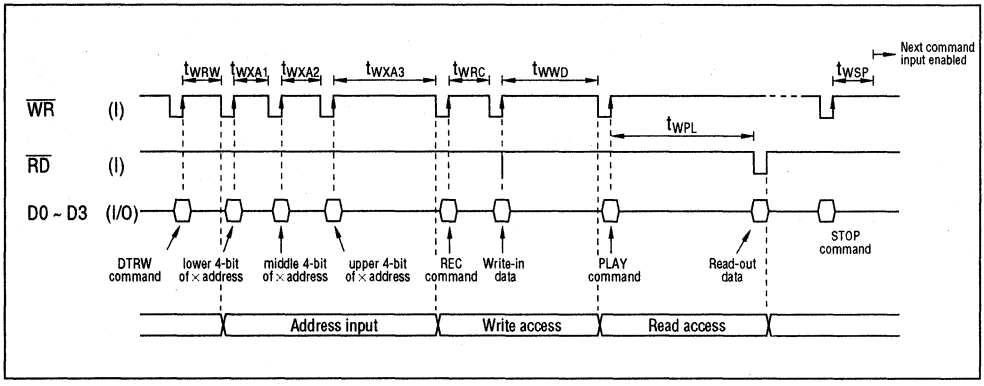
9. Playback method using START command



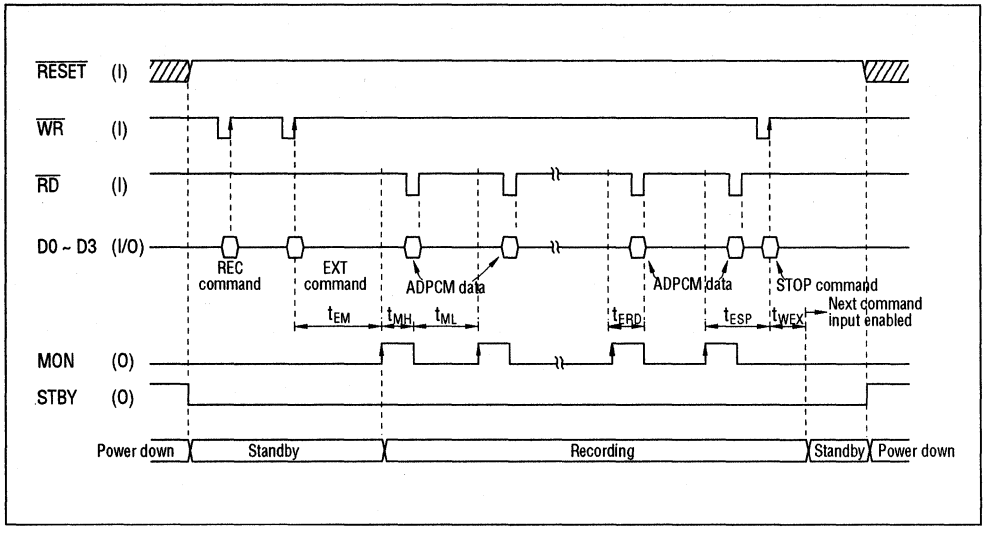
10. Timing of pause in record/playback using PAUSE command



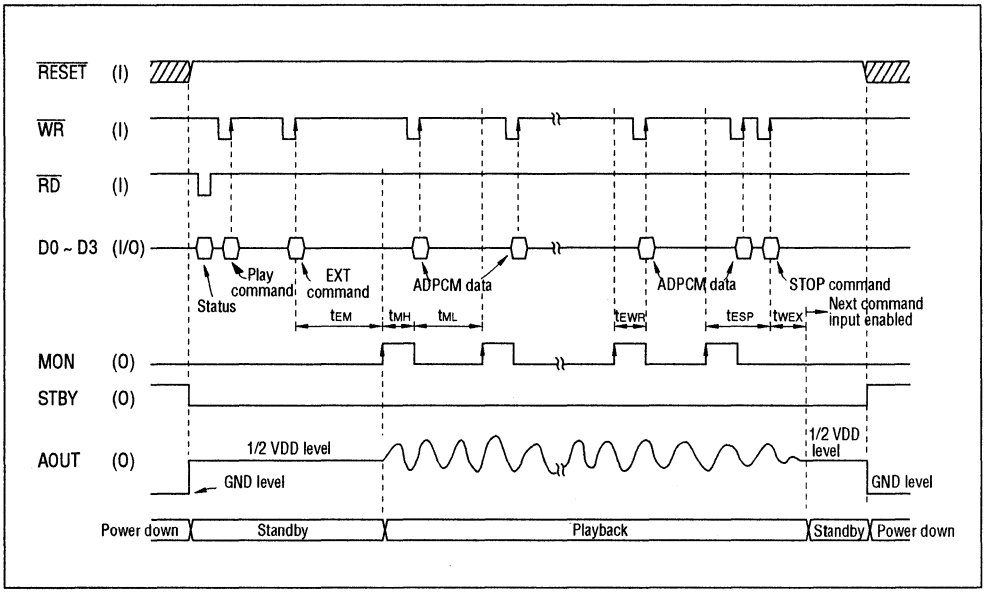
11. Timing of data transfer by DTRW command



12. Timing of recording by EXT command



13. Timing of playback by EXT command



EXPLANATION OF PIN FUNCTIONS

Common Functions in Stand-Alone Mode and Microcontroller Modes

Pin Name	I/O	Function
DVDD	—	Digital power supply pin
DVDD'	—	Digital power supply pin
AVDD	—	Analog power supply pin
DGND	—	Digital GND pin
AGND	—	Analog GND pin
SG	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin for the built-in OP amplifier. Non-inverting input pin is connected to SG internally.
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in recording mode and to the DA converter output in playing mode. Connected to the built-in LPF input (FIN pin).
FIN	I	Input pin for the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Connected to the AD converter (ADIN pin) input.
ADIN	I	Input pin for the built-in 12-bit AD converter.
AOUT	O	Output pin for the built-in LPF. Output pin for playback waveform. Connected to the speaker drive amplifier.
SAD	O	(Senal Address Data) Connected to the SAD pin of serial voice register. This pin outputs the Read/Write header address.
$\overline{SAS}$	O	(Serial Address Strobe) Connected to the $\overline{SAS}$ pin of serial voice register. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe) Connecd to the $\overline{TAS}$ pin of serial voice register. Clock pin which tranfers the serial address data to the address counter inside the serial voice register.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>$\overline{RWCK}$</td><td>O</td><td>(Read/Write Clock) Connected to the $\overline{RWCK}$ pin of the serial voice register. Clock pin for reading and writing data to the serial voice registers.</td></tr>
<tr><td>$\overline{WE}$</td><td>O</td><td>(Write Enable) Connected to the $\overline{WE}$ pin of serial voice register. The pin to select read or write mode.</td></tr>
<tr><td>DI/O</td><td>I/O</td><td>(Data I/O) Connected to the DIN and DOUT pins of serial voice register. Data input and output mode.</td></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$ (STBY)
$\overline{CS4}$ (RSEL0)</td><td>O
O
O
I/O</td><td>(Chip Select) Connected to the $\overline{CS}$ pin of the serial voice register.
$\overline{CS3}$ pin and $\overline{CS4}$ pin have different functions depending on the number of serial voice registers to be connected. The number of serial voice registers is selected by the RSEL1 and RSEL2 pins.
$\overline{CS3}$ (STBY) pin becomes $\overline{CS3}$ when four serial voice registers are used\, otherwise it is the STBY pin which outputs a "H" level at power down.
$\overline{CS4}$ (RSEL0) pin becomes $\overline{CS4}$ when four serial voice registers are used, otherwise it is the RSEL0-pin used to select the number of serial voice registers used.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>$\overline{CS3}$ (STBY)</td><td>STBY</td><td>STBY</td><td>STBY</td><td>$\overline{CS3}$</td></tr>
<tr><td>$\overline{CS4}$ (RSEL0)</td><td>RSEL0
(I)</td><td>RSEL0
(I)</td><td>RSEL0
(I)</td><td>$\overline{CS4}$
(O)</td></tr>
</table>
</td></tr>
<tr><td>$\overline{CS4}$ (RSEL0)
RSEL1
RSEL2</td><td>I/O
I
I</td><td>(Register Select) Those pins are to select the number of serial voice registers to be connected.
<table>
<tr><td>RSEL2</td><td colspan="2">L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td colspan="2">L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>RSEL0 (CS4)</td><td>L
(I)</td><td>H
(I)</td><td>—
(I)</td><td>—
(I)</td><td>$\overline{CS4}$
(O)</td></tr>
<tr><td>Number of serial voice registers</td><td>One 256Kbit</td><td>One 256Kbit</td><td>One 1Mbit</td><td>Two 1Mbit</td><td>Four 1Mbit</td></tr>
</table>
</td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is to select stand-alone mode or microcontroller interface mode.
"L" level···· stand-alone mode
"H" level···· microcontroller interface mode</td></tr>
<tr><td>$\overline{RESET}$</td><td>I</td><td>The LSI is initialized and goes into the power-down state by input of a "L" level.</td></tr>
<tr><td>XT</td><td>I</td><td>Connect to an oscillator. Use this input when providing an external clock. When at power down input the GND level instead.</td></tr>
<tr><td>$\overline{XT}$</td><td>O</td><td>Connect to an oscillator. Leave open when using an external clock.</td></tr>
</table>

Stand-Alone Mode

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>REC/$\overline{PLAY}$</td><td>I</td><td>This pin is to select recording or playback. When an "H" level is input, the LSI is in record mode.</td></tr>
<tr><td>$\overline{ST}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is started. Internal pull up connected.</td></tr>
<tr><td>$\overline{SP}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is ended. Internal pull up connected.</td></tr>
<tr><td>$\overline{PAUSE}$</td><td>I</td><td>When an "L" level pulse is input, record/playback is suspended. Internal pull up connected.</td></tr>
<tr><td>CSEL1
CSEL2</td><td>I</td><td>These pins are to select the number of recorded words and control mode. When the number of the recorded words is wished to be selected in one word, select Flex mode.
<table>
<tr><td>CSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>CSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Number of recorded words</td><td>8</td><td>4</td><td>2</td><td>8</td></tr>
<tr><td>Control mode</td><td colspan="3">fixed</td><td>flex</td></tr>
</table></td></tr>
<tr><td>CA1
CA2
CA3</td><td>I</td><td>These pins are to specify the channel.
(Refer to Explanation of Functions.)</td></tr>
<tr><td>SAM</td><td>I</td><td>This pin is to select the sampling frequency.
The following is the relation between the master clock frequency (f_{osc}) and sampling frequency (f_{sam}).

Numbers inside the parenthenses ( ) are for f_{osc}=4.096MHz
<table>
<tr><td>SAM</td><td>L</td><td>H</td></tr>
<tr><td>f_{sam}</td><td>$\frac{f_{samp}}{768}$
(5.3kHz)</td><td>$\frac{f_{osc}}{512}$
(8.0kHz)</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This pin selects transition to the power down state.
"L" level···· The LSI enters power down state automatically except during record/playback.
"H" level···· The LSI enters standby state except during record/playback.
The power down state can be entered by the $\overline{RESET}$ pin. This mode must be active when using the built-in LPF in an external circuit.</td></tr>
</table>

Pin Name	I/O	Function
VDS	I	This pin is to select voice activated recording when the voice input exceeds the preset amplitude. Input an "H" level and the voice activation circuit is enabled. Input an "L" level to disabel the voice activation circuit.
MON	O	Outputs a "H" level during record/playback.

Microcontroller Interface Mode

Pin Name	I/O	Function
D0 D1 D2 D3	I/O	Bi-directional data bus. Performs input/output of commands and data with an external microcontroller.
$\overline{WR}$	I	This pin is to input WRITE pulses. Input is a "L" pulse when commands or data to the D0~D3 pins are to be input.
$\overline{RD}$	I	This pin is to input READ pulses. Input is a "L" pulse when output status or data from the D0~D3 pins is to read.
$\overline{CE}$	I	Chip enable. A "H" level on this pin disables WRITE (WR)/READ ($\overline{RD}$) input pulses. Input/output of data through the D0~D3 pins is disabled.
MON	O	Outputs a "H" level during record/playback. When record/playback is in operation using the EXT command, clocks for synchronization are output.
TEST $\overline{TEST}$	I	These pins are for LSI testing at the factory. Input a "L" level to the TEST pin and an "H" level to the $\overline{TEST}$ pin.

EXPLANATION OF FUNCTIONS

Recording Time and Memory Capacity

Recording time depends on the memory capacity of the external serial voice registers, sampling frequency, and the ADPCM bit length, and is expressed as

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity(kbit)}}{\text{sampling frequency (kHz)} \times \text{bit length}} \text{(sec)}$$

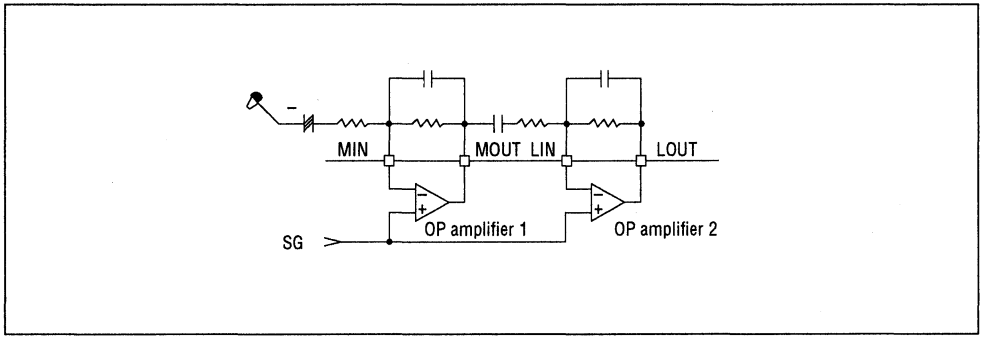
For example, if the sampling frequency is 5.3kHz with a 3bit ADPCM and 4 serial voice registers, it is possible to record up to 262 seconds because

$$\text{Recording time} = \frac{1.024 \times 1024 \text{ (kbit)} \times 4}{5.3 \text{ (kHz)} \times 3\text{(bit)}} = 262 \text{ (seconds)}$$

Analog Input Amplifier Circuit

This LSI has two built-in OP amps for amplifying microphone and line outputs. Both have pins for inverted input and output from the OP amps. Analog circuit reference voltage SG (signal ground) is input to the LSI as the non-inverted input.

When amplifying, prepare an inverse amplifying circuit and adjust the amplifying ratio by external resistors.



Connection of LPF Circuit Peripherals

Inside the LSI, the AMON pin is connected to the output of the amplifying circuit in recording mode (LOUT pin) and output of the DA converter in playback mode. This means that the AMON pin is directly connected to the input pin (FIN pin) of the built-in LPF.

Both the FOUT pin and AOUT pin are output pins of the built-in LPF. The FOUT pin is connected to the input pin (ADIN pin) of the AD converter and the AOUT pin is connected to a speaker through the speaker amplifier.

The connection of the FOUT pin and the AOUT pin changes according to the output of LPF, SG level or GND level inside the LSI depending on the operation state which is summarized by the following:

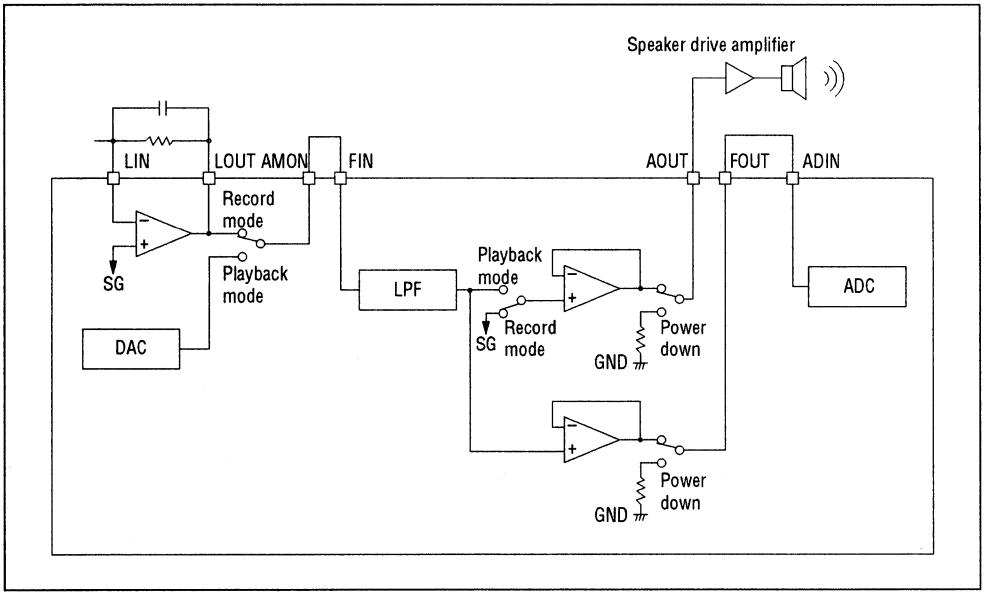
- Microcontroller interface mode and stand-alone mode when the PDMD pin="H"

Analog pin	At power down ($\overline{\text{RESET}}$ pin="L")	During operation ($\overline{\text{RESET}}$ pin="H")	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (record wave form)	LPF output
AOUT pin	GND level	SG level	LPF output (playback wave form)

- Stand-alone mode when the PDMD pin="L"

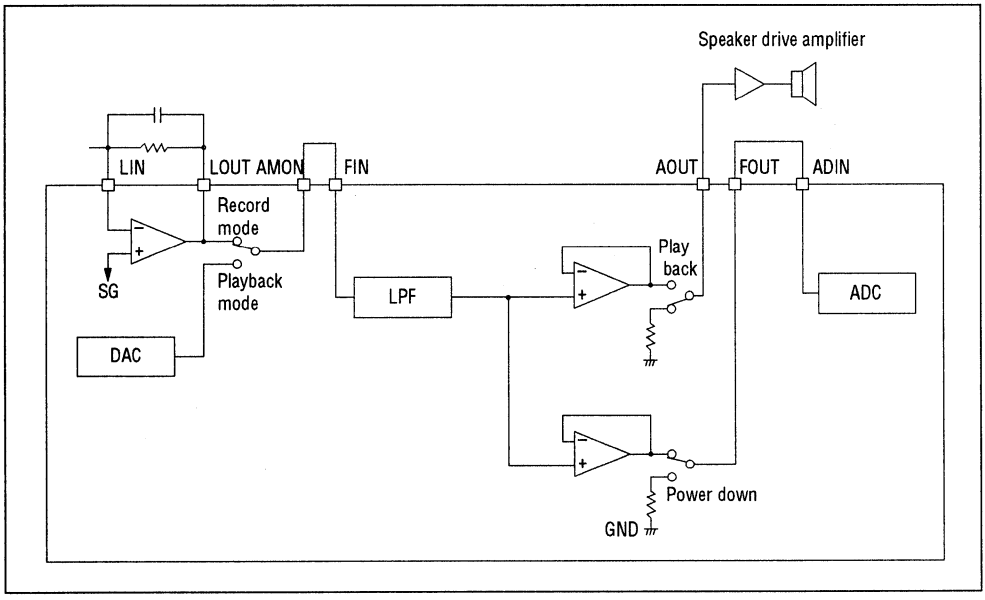
Analog pin	At power down	During operation	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (record wave form)	LPF output
AOUT pin	GND level	GND level	LPF output (playback wave form)

• Microcontroller interface mode and stand-alone mode when the PDMD pin="H"



Note: Switches in the figure denote the state during record operation.

• Stand-alone mode when the PDMD pin="L"



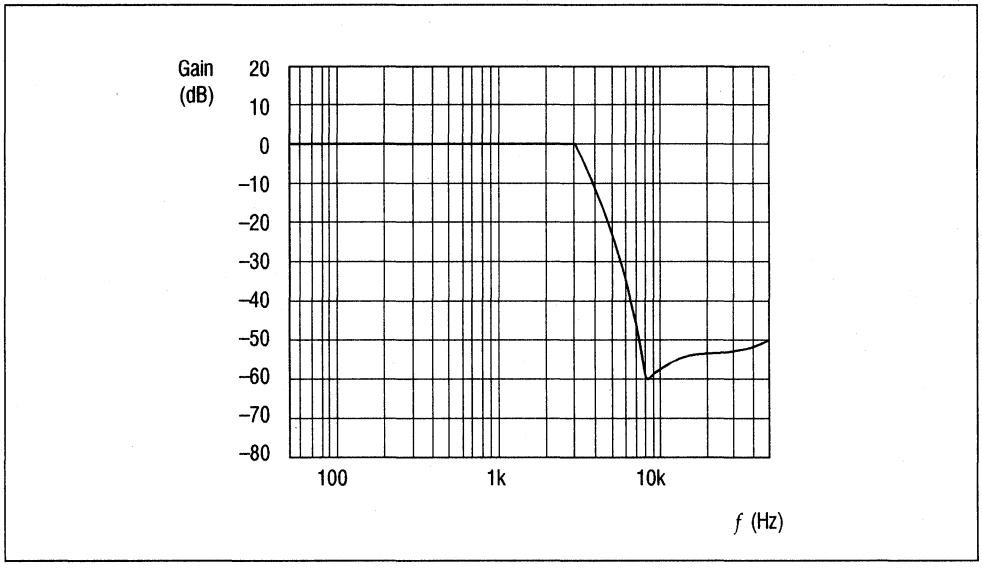
Note: Switches in the figure denote the state during record operation.

LPF Characteristics

This LSI has a built-in fourth order LPF using switched capacitor filter technology.

The filter characteristics are –40dB/oct. Both the cut-off frequency and frequency characteristics change in proportion to the sampling frequency (f_{sam}).

The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of LPF when f_{sam} = 8kHz.



LPF Frequency Characteristics (f_{sam} = 8.0 kHz)

Voice Triggered Starting Function

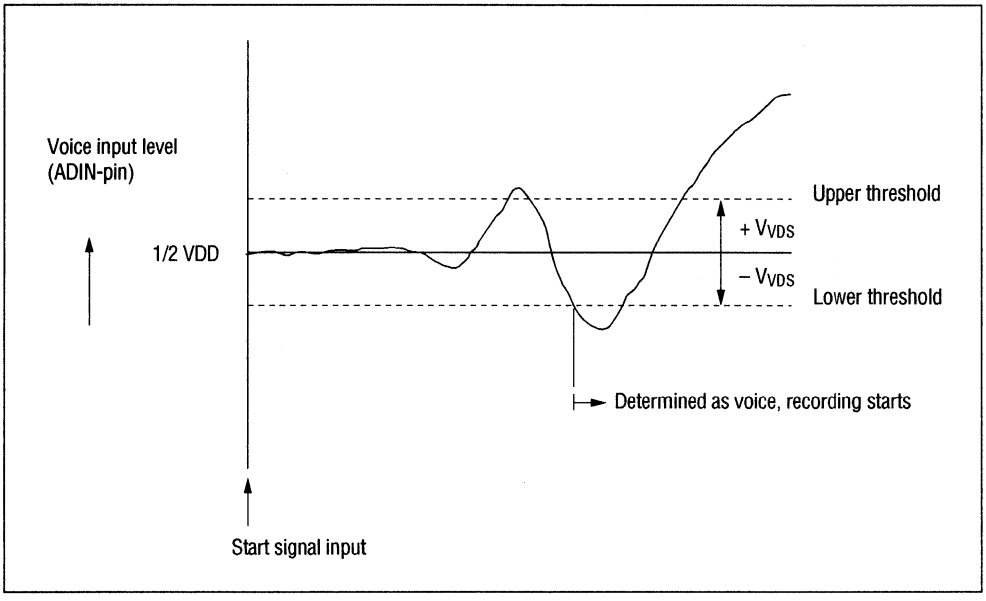
This LSI has a voice triggered starting function that starts recording when the amplitude of voice input exceeds a preset threshold.

The voice triggered starting function is controlled by the VDS pin in stand-alone mode and by the VDS command in microcontroller interface mode. The voice standby state can be released by a STOP pulse or the STOP command.

During recording/playback using the EXT command in microcontroller interface mode, voice triggered starting cannot be used.

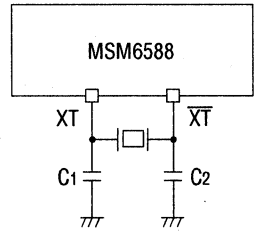
Stand-alone mode	VDS-pin	L	—	H	—
Microcontroller interface	VD1	L	L	H	H
mode	VD0	L	H	L	H
Vocie detection level Vvds		No voice triggered starting function	±VDD/64 (±80mV)	±VDD/32 (±160mV)	±VDD/16 (±320mV)

Note: Values inside ( ) are for VDD = 5.12V.



How to Connect an Oscillator

Connect a ceramic oscillator or a crystal oscillator to XT and $\overline{XT}$ pins as shown below.

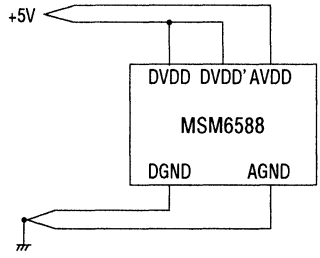


The optimal load capacities when connecting ceramic oscillators from MURATA MFG. and KYOCERA CORPORATION are shown below for reference.

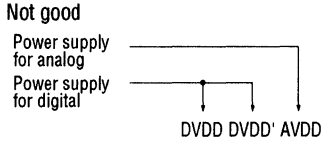
Ceramic oscillator			Freq(MHz)	Optimal load capacity	
Type				C1(pF)	C2(pF)
MURATA MFG.	CSA4.00MG CST4.00MGW		4.0	30	30
	CSA6.00MG CST6.00MGW		6.0		
	CSA8.00MTZ CST8.00MTW		8.0		
KYOCERA CORPORATION	KBR-4.0MSA		4.0	33	33
	KBR-4.0MWS KBR-4.0MKS	(with capacitor)			
	PBRC4.00A				
	KBR-6.0MSA		6.0		
	KBR-6.0MWS KBR-6.0MKS	(with capacitor)			
	PBRC6.00A				
	KBR-8.0M		8.0		
	KBR-8.0MWS	(with capacitor)			
	PBRC8.00A				

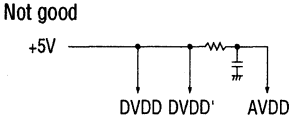
How to Connect Power Supply

This LSI uses a single power supply which is divided into two routes on the wiring, one is to the analog section, and the other is to the logic section.



It is not permitted to have two power supplies for the analog section and the logic section separately because it may cause a latch-up.





Data Configuration of External Serial Voice Registers

The external serial voice registers are composed of (X address in the word direction) × (depth of 1K-bit) and are divided into the channel index area and the voice (ADPCM) data area.

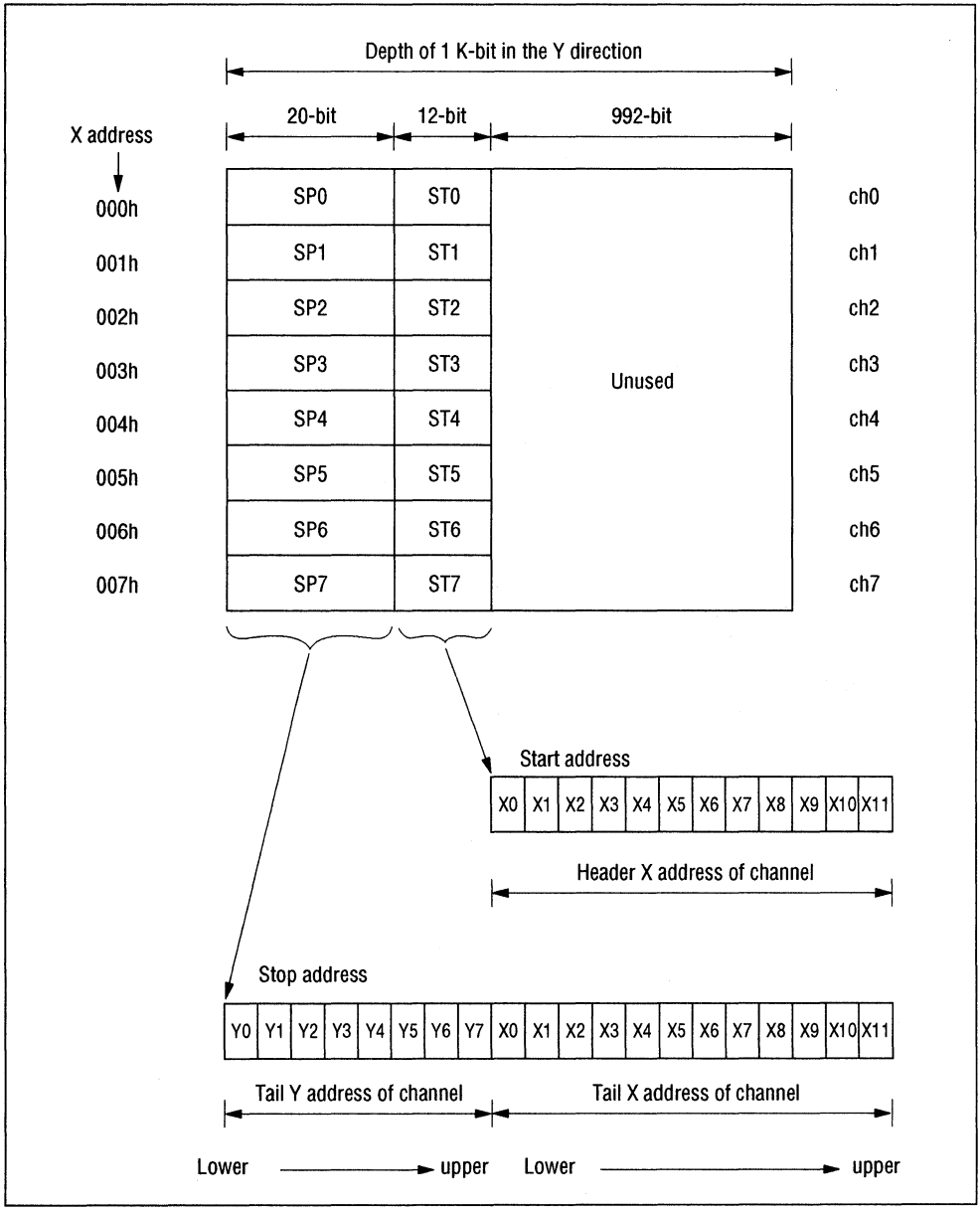
The maximum address of X address in the word direction can be summarized in the following table depending on the memory capacity of the connected serial voice registers:

Connected serial voice registers Memory capacity (bit)	Maximun X address
256K	0FFh
512K	1FFh
1M	3FFh
2M	7FFh
3M	BFFh
4M	FFFh

1. Channel index area

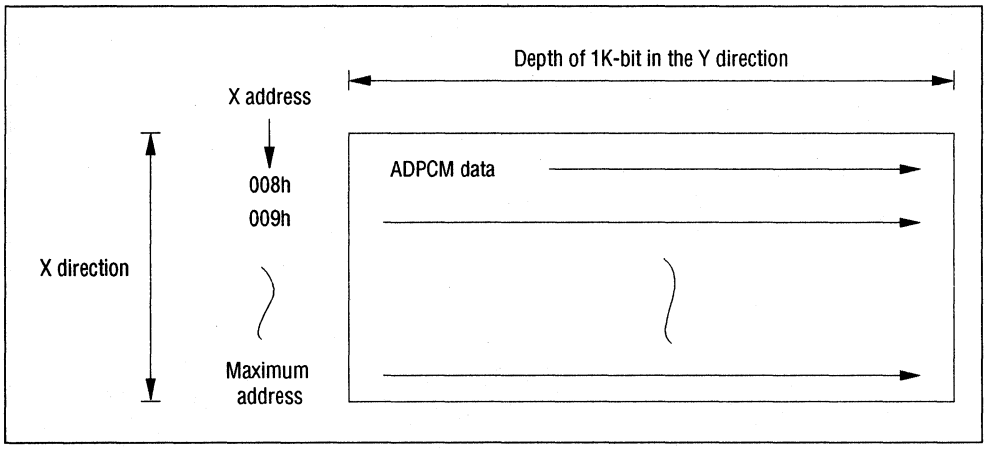
Addresses 000h-007h, are header addresses for the serial voice registers and are known as the channel index area which store the start and stop address of each channel.

The start address and stop address are expressed by 12-bit and by 20-bit, respectively.They store the header and tail addresses of the voice data for each channel.



2. Voice (ADPCM) data area

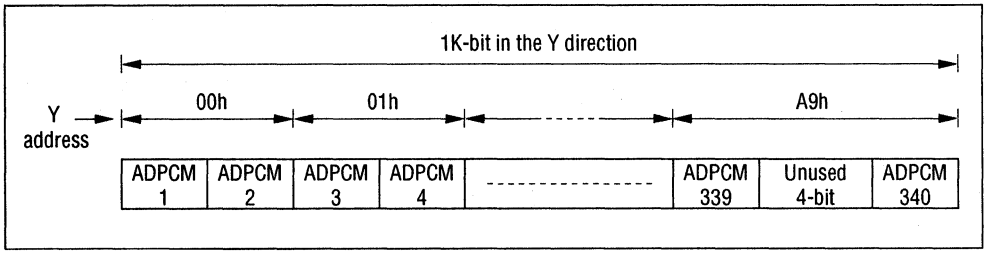
Addresses after 008h of the X address are the voice data area and store ADPCM data.



The storage method of ADPCM data per 1 address in the X-direction (1K-bit) is different for 3-bit and 4-bit ADPCM. It is summarized as follows:

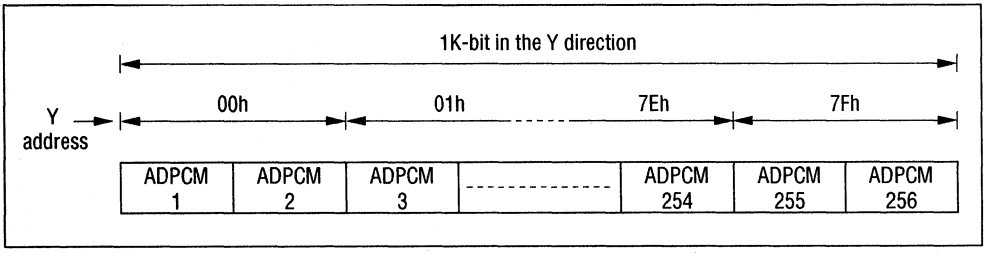
3-bit ADPCM

3-bit data × 340 samples = 1020-bit stored in the 1K-bit memory area. The Y address is assigned one address per two samples and is controlled by 00h-A9h.



4-bit ADPCM

4-bit data × 256 samples = 1024-bit are stored in the 1K-bit memory area. The Y address is assigned one address per two samples and is controlled by 00h-7Fh.



Selection of Serial Voice Registers

RSEL1 and RSEL2 are used select the type and the number of serial voice registers connected externally.

The $\overline{CS4}$ (RSEL0) pin functions as a $\overline{CS4}$ output pin when RSEL1=RSEL2="H" and as an RSEL0 input pin otherwise to select either 512Kbit or 256Kbit.

RSEL2	L		L	H	H
RSEL1	L		H	L	H
RSEL ($\overline{CS4}$)	L (1)	H (1)	— (1)	— (1)	$\overline{CS4}$ (1)
Number of serial voice registers	One 256Kbit	One 512Kbit	One 1Mbit	Two 1Mbit	Four 1Mbit

Recording Control Modes

The recording control modes include fixed and flex mode during stand-alone operation and fixed, flex and direct mode during microcontroller interface operation. The recording control mode is specified by the CSEL1 and CSEL2 pin in stand-alone operation and by data input via commands (RCON, CSEL1 AND CSEL2) during microcontroller interface operation.

RCON	CSEL2	CSEL1	Number of recording words	Control mode
L	—	—	8-word	Direct mode (only in microcontroller interface mode)
H	L	L	8-word	Fixed mode (When the number of the recorded words is wished to be selected in one word, select Flex mode.)
	L	H	4-word	
	H	L	2-word	
	H	H	8-word	Flex mode

1. Direct mode

This mode can be used in microcontroller interface mode only.

The start and stop address of each channel are input to the channel index area directly from the microcontroller. This means that the assignment of memory capacity of each channel is controlled by the microcontroller.

2. Fixed mode

This mode can be used in both stand-alone mode and in microcontroller interface mode.

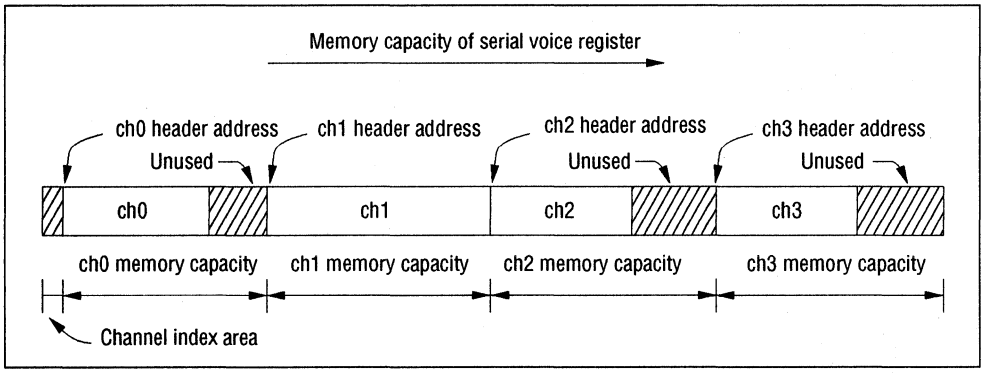
The start and stop address of each channel can be set indirectly by the channel selection (CA1-CA3) and they are input to the channel index area.

The memory capacity of the external serial voice register equally divided by the number of recording words is assigned to each channel by CSEL1 and CSEL2.

(Hereafter, this will be called the channel memory capacity).

When recording, ADPCM data is written-in from the header address of the selected channel memory capacity. When stopping recording by the STOP signal, the memory capacity after that is unused.

An example of selecting 4-word as the number of recording words.



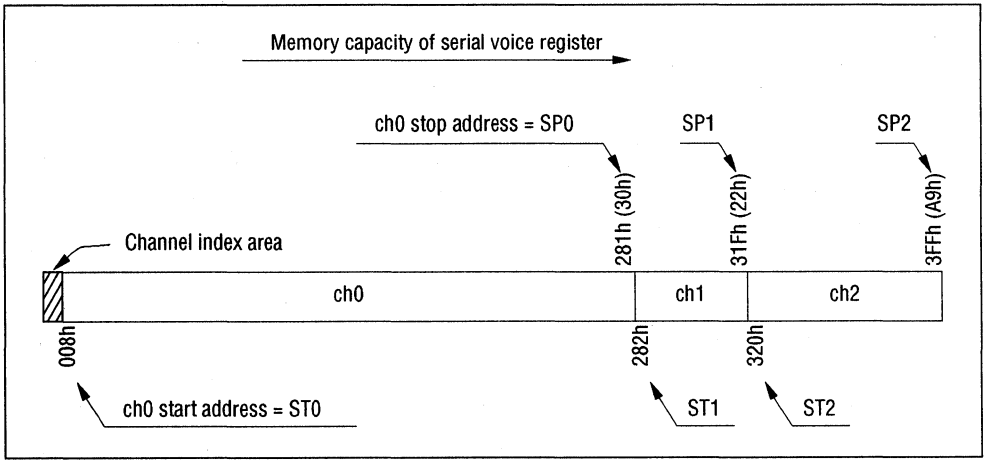
3. Flex mode

This mode can be used in both stand-alone mode and in microcontroller interface mode.

The start and stop address of each channel are indirectly set by channel selection (CA1 – CA3) and are input to the channel index area.

When recording at the initial state (no recording has been performed in any channels), it is necessary to record in the order of ch0 to ch7. When starting recording of ch0, ADPCM data is stored from the header of the voice data area and the recording is stopped when the STOP signal is input. When the STOP signal is not input, recording is stopped when the maximum address of the serial voice register reached.

When ch1 is selected subsequently, the recordable memory area starts from the address incremented by +1 from the stop address of ch0 through the maximum address. Similarly, the recording continues to ch2, ch3.... The start address of chn is the one incremented by +1 from the stop address of



Channel Usage

A channel can be specified by CA1, CA2 and CA3. In stand-alone mode, CA1–CA3 pins are used while in microcontroller interface mode, command data is input with (CA1–CA3).

1. Selection of a channel in direct mode and flex mode

The number of recording words is 8 and is specified by CA1–CA3 as follows:

CA3	CA2	CA1	Channel
L	L	L	ch0
L	L	H	ch1
L	H	L	ch2
L	H	H	ch3
H	L	L	ch4
H	L	H	ch5
H	H	L	ch6
H	H	H	ch7

2. Channel selection in fixed mode

The relationship between the number of recorded words (CSEL1, CSEL2) and channels (CA1–CA3) is shown in the following table.

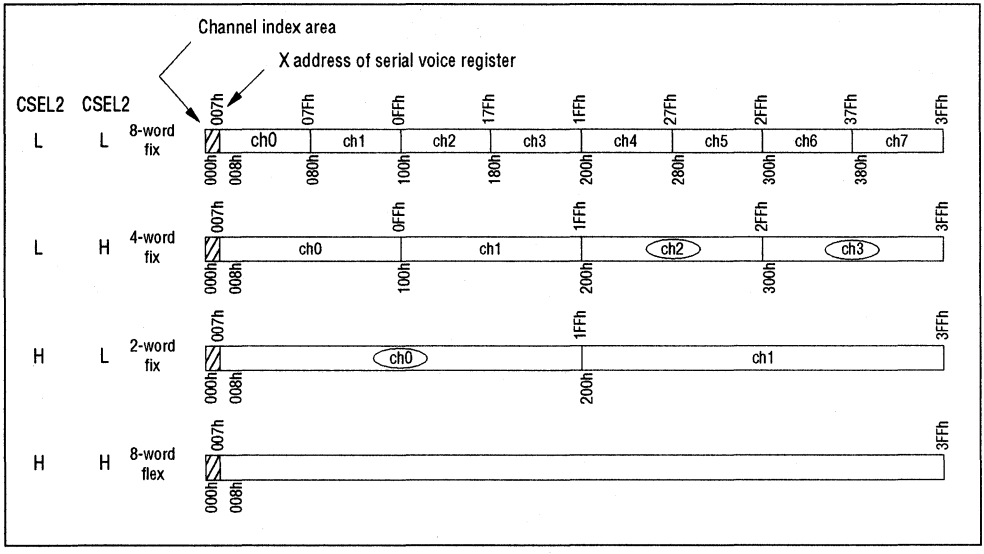
CSEL2	CSEL1	Number of recorded words	CA3	CA2	CA1	Channel
L	L	8-word	L	L	L	ch0
			L	L	H	ch1
			L	H	L	ch2
			L	H	H	ch3
			H	L	L	ch4
			H	L	H	ch5
			H	H	L	ch6
			H	H	H	ch7
L	H	4-word	L	L	—	ch0
			L	H	—	ch1
			H	L	—	ch2
			H	H	—	ch3
H	L	2-word	L	—	—	ch0
			H	—	—	ch1

The relationship between the external serial voice registers, the number of recorded words and the channel memory capacity is shown in the following table.

CSEL 2	CSEL 1	Number of recorded words	Channel memory capacity				
			256Kbit serial voice register	512Kbit serial voice register	1Mbit serial voice register	2Mbit serial voice register	4Mbit serial voice register
L	L	8-word	32Kbit (1 second)	64Kbit (2 second)	128Kbit (4 second)	256Kbit (8 second)	512Kbit (16 second)
L	H	4-word	64Kbit (2 second)	128Kbit (4 second)	256Kbit (8 second)	512Kbit (16 second)	1Mbit (32 second)
H	L	2-word	128Kbit (4 second)	256Kbit (8 second)	512Kbit (16 second)	1Mbit (32 second)	2Mbit (64 second)

Note: Numbers in ( ) are recording time of each channel when the bit rate is 32kbps.

Assignment to channel and channel memory capacity when connecting a 1Mbit serial voice register



By combining CSEL1, CSEL2, CA1, CA2 and CA3, it is possible to assign (the encircled channels) ch0=16 seconds, ch2=8 seconds and ch3=8 seconds (f_{sam}=8kHz, 4 bit ADPCM).

Operation in Stand-alone Mode

1. Power down function

Transition to power down mode is selected by the PDMD pin and is summarized as follows:

PDMD pin	Power down operation
L	The LSI automatically enters the power down state except during recording/playback.
H	The LSI powers down by input of a "L" level to the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin="H" level, the LSI is in stand-by mode and the analog circuit is active. When using the built-in LPF with and external circuit, select this mode.

During power down, the LSI stops oscillating to minimize power consumption and the circuit enters the initialized state.

When using an external clock, input the GND level to the XT pin to reduce power consumption.

2. Master clock frequency and sampling frequency

The relationship between the master clock frequency (f_{OSC}) and the sampling frequency (f_{sam}) is summarized in the following table by the SAM pin.

SAM	L	H
f_{sam}	$\frac{f_{OSC}}{768}$ (5.3kHz)	$\frac{f_{OSC}}{512}$ (8.0kHz)

Note: Numbers inside ( ) are for master clock oscillation f_{OSC} = 4.096 MHz.

3. Method of recording

(1) Select the sampling frequency by the SAM pin.

(2) Select voice activation by the VDS pin.

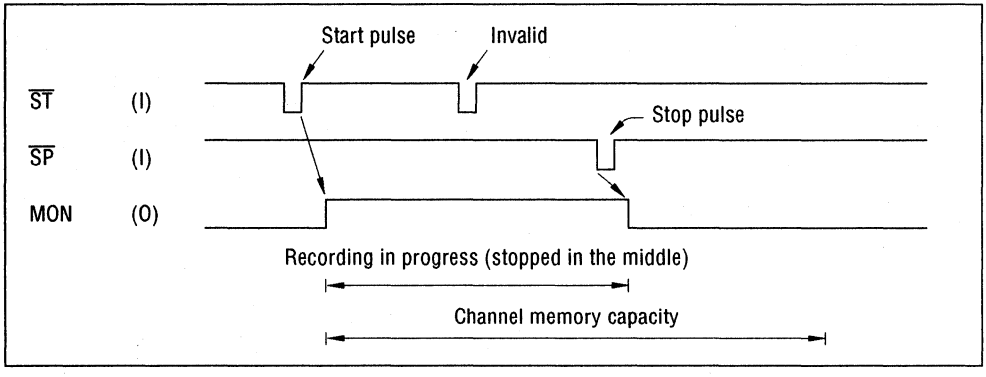
(3) Select the number of words by the CSEL1 and CSEL2 pins and the channel by the CA1, CA2, and CA3 pins.

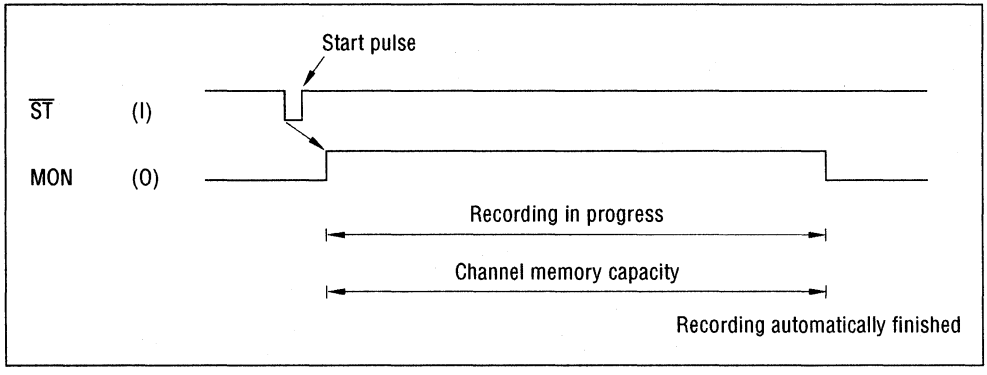
(4) Input the "H" level to the REC/$\overline{\text{PLAY}}$ pin to set recording mode.

(5) Input a "L" pulse to the $\overline{\text{ST}}$ pin to start recording. To finish recording in the middle, input a $\overline{\text{SP}}$ pulse. The time between these two pulses is recording time.

When recording is started by input of a "L" pulse to the $\overline{\text{ST}}$ pin and continues to the end of the channel memory capacity, the recording is automatically finished at that point.

The MON pin outputs a "H" level during recording.





4. Method of playback

(1) Select the sampling frequency by the SAM pin.

(2) Select the number of words by the CSEL1 and CSEL2 pins and the channel by the CA1, CA2 and CA3 pins.

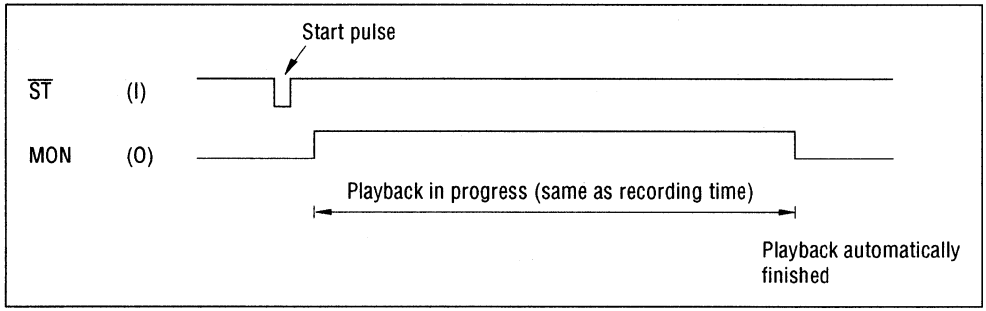
(3) Input a "L" level to the REC/$\overline{\text{PLAY}}$ pin to set playback mode.

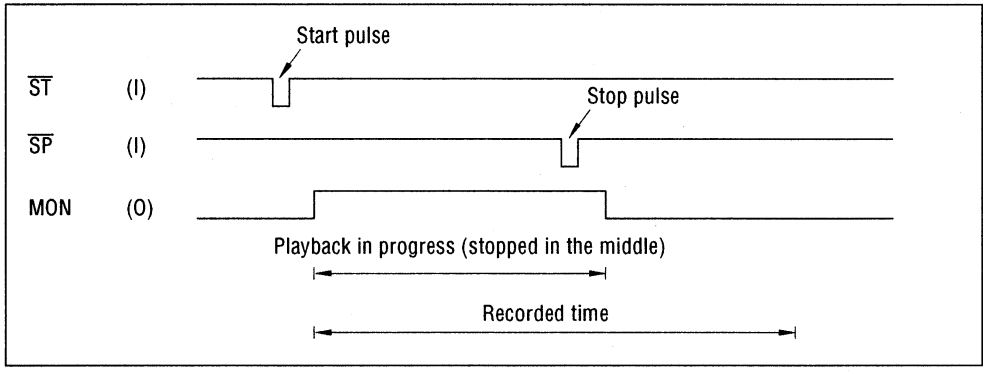
(4) Input a "L" level pulse to the $\overline{\text{ST}}$ pin to start playback. When played back for the duration of recorded time, the playback ends automatically.

To stop the playback in the middle, input a "L" level pulse to the $\overline{\text{SP}}$ pin.

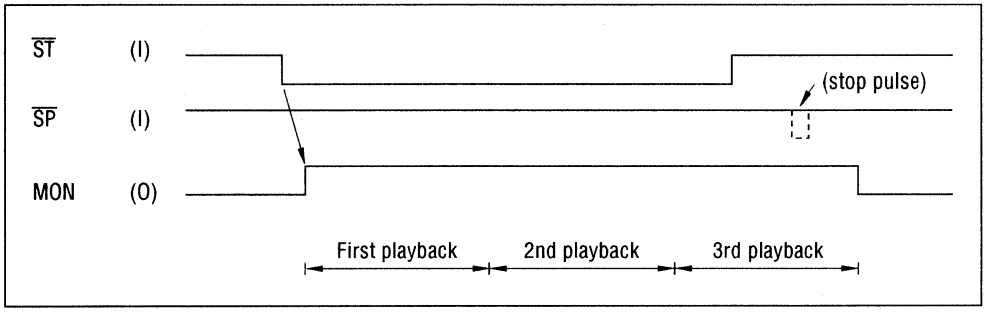
The MON pin outputs a "H" level during playback.

Do not start playback in channels not recorded because the playback data and time are undefined. However, playback under these conditions can be halted by a $\overline{\text{SP}}$ pulse.



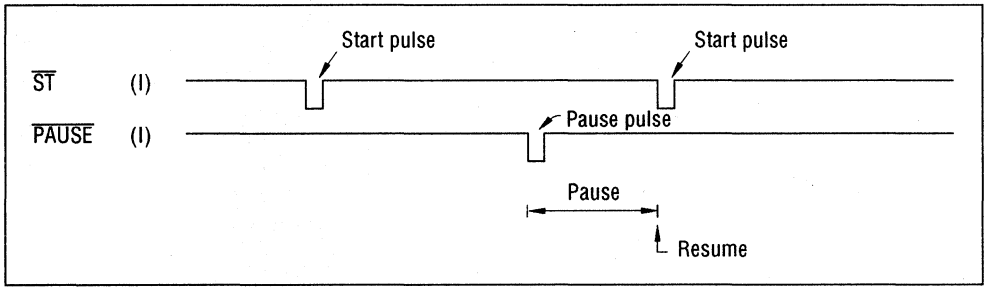


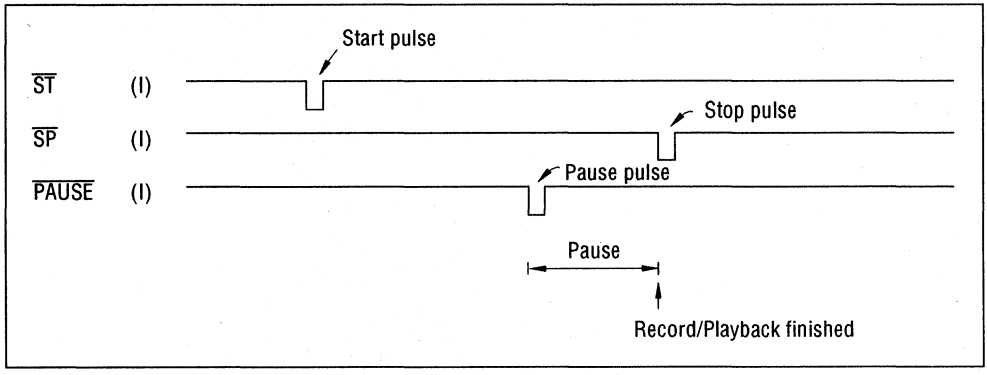
By maintaining the $\overline{\text{ST}}$ pin at "L" level, repeated playback is possible.



5. Method of pause in record/playback

By input of a "L" level pulse to the $\overline{\text{PAUSE}}$ pin during record/playback, input a "L" level pulse to the $\overline{\text{ST}}$ pin. The recording/playback is finished when a "L" level pulse is input to the $\overline{\text{SP}}$ pin.



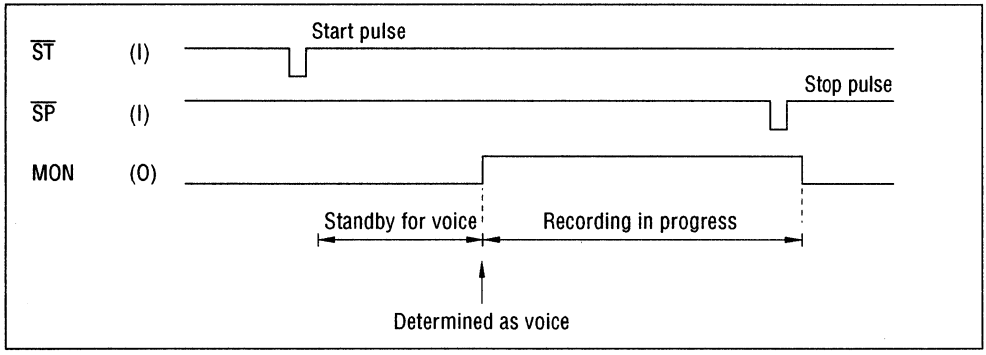


After resuming record/playback, the voice triggered starting function circuit does not operate and the recording is resumed when a START pulse is input.

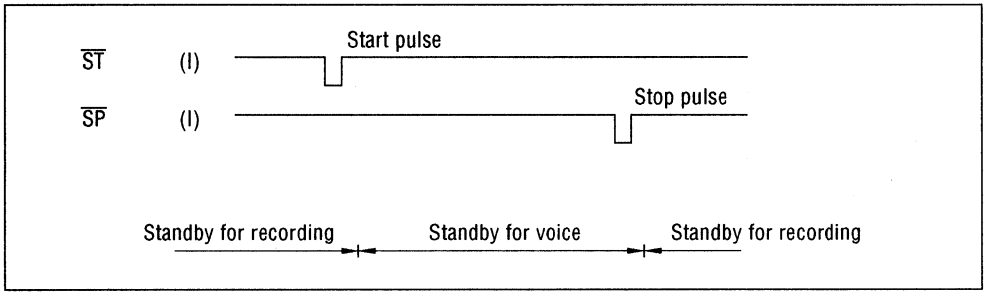
6. Operation in voice triggered recording

By input of a "H" level to the VDS pin, voice triggered recording can be performed. Using the voice activation function, the memory capacity can be utilized effectively by eliminating any data prior to voice detection. However, it does not remove silence data during the recording.

Input of a $\overline{ST}$ pulse initiates standby for voice and recording begins when voice is detected. The MON pin outputs a "H" level.



When a STOP pulse is input during standby for voice, the standby for voice is finished and the LSI enters standby for recording.



7. Method of re-recording

7.1 Fixed mode

In this mode, because the memory area that each channel can use is already assigned, re-recording can by performed without interfering with the contents of other channels. Re-recording can be performed from the beginning similar to a new recording, regardless of the previous recording time.

7.2 Flex mode

In this mode, recording for each channel is started from the address incremented by +1 from the address of preceding channel, chn-1 (if ch0, the header address of the voice data area) and the recording continues until the input of a $\overline{SP}$ pulse. If a $\overline{SP}$ pulse is not input, the recording is continued until the maximum address of the external serial voice register. This indicates that if the duration of recording is longer than the previously recorded time, it interferes with the contents of proceeding channels.

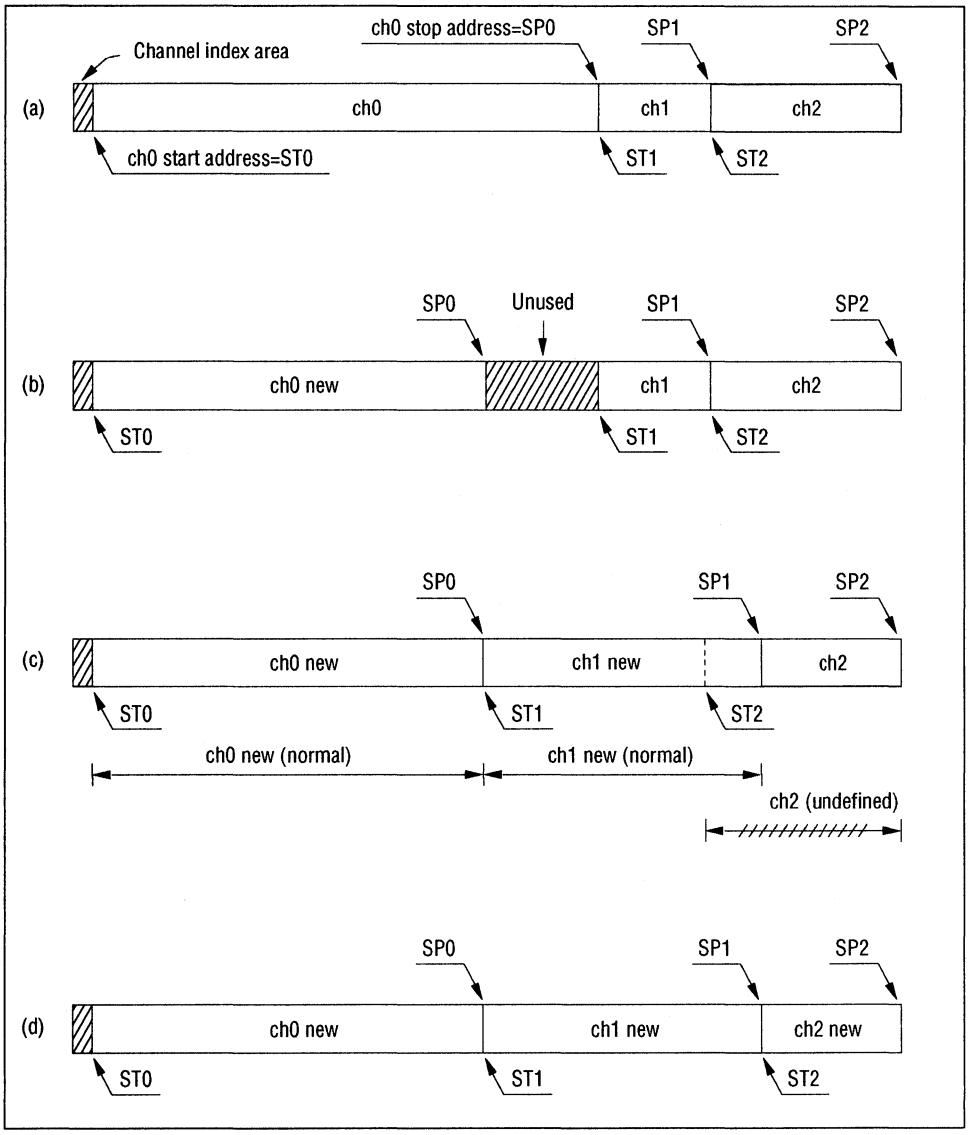
The following shows an example in which the first recording is performed as in Figure (a) and after that each channel is re-recorded.

If the duration of re-recording of ch0 is shorter than the initially recorded time, all the channels function properly as shown in Figure (b).

If the duration of re-recording of ch1 is longer than the initially recorded time and reaches the range of ch2, ch0, and ch1 function properly but the playback data of ch2 becomes undefined as ch2 is played back from the middle of ch1 data.

By re-recording ch2 as shown if Figure (d), ch0-ch2 function properly.

Memory capacity of external serial voice register



8. Pull up resistor

In stand-alone mode, a pull-up resistor is connected internally to the $\overline{ST}$, $\overline{SP}$ and $\overline{PAUSE}$ pins. However, the resistor is disconnected during a "L" level input to the $\overline{RESET}$ pin.

Operation in Microcontroller Interface Mode

There are 13 data bus commands, D0~D3 and $\overline{WR}$, $\overline{RD}$ and $\overline{CE}$ which control the MSM6588 in this mode. It has an internal status register so that the state of the LSI can be monitored.

1. Command input method

Input of commands and data can be performed by input of a "L" level ($\overline{WR}$ pulse) during command data input on the D0~D3-pin.

Input of a "L" level ($\overline{RD}$ pulse), outputs status or data to the D0~D3-pin.

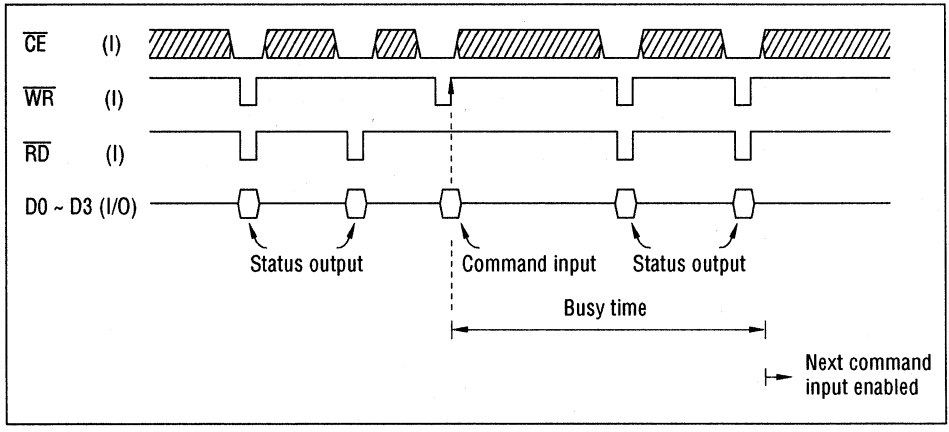
The $\overline{CE}$ pin controls enable/disable of the $\overline{WR}$ and $\overline{RD}$ pulses. Input of a "L" level enables $\overline{WR}$ and $\overline{RD}$ pulses, while a "H" level disables $\overline{WR}$ and $\overline{RD}$ pulses and D0~D3 become high-impedance. When using the D0~D3-pin with the MSM6588 alone, the $\overline{CE}$ pin can be fixed at the "L" level.

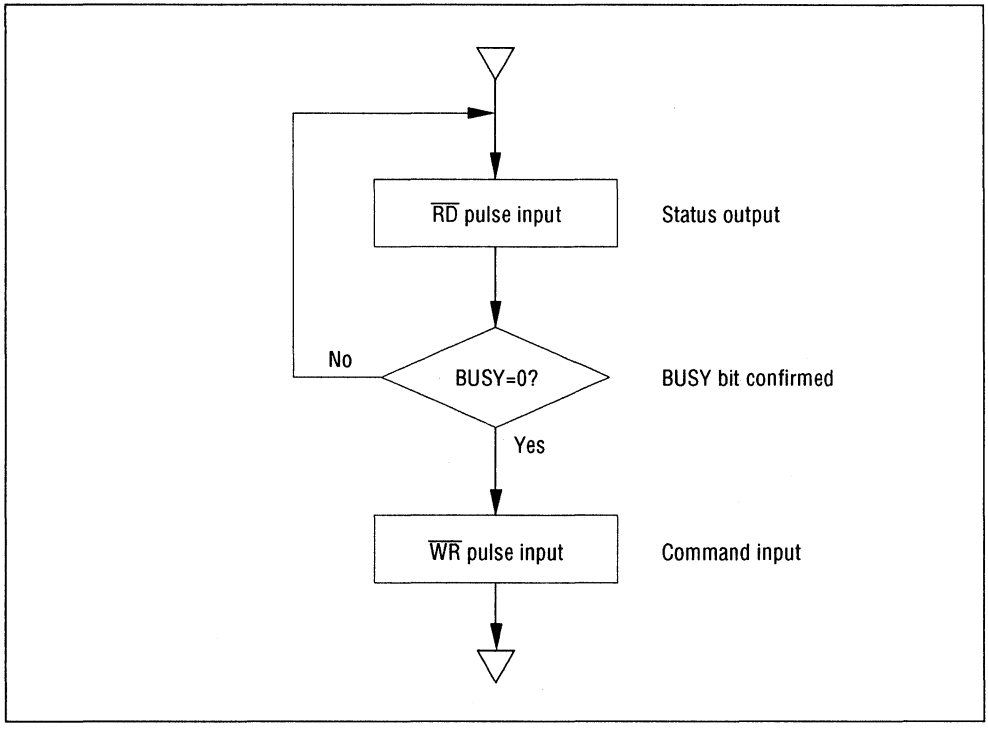
1.1 Input method of 1 nibble command

(1) Input a $\overline{RD}$ pulse to fetch the contents of the status register and make sure that the BUSY bit is 0. When it is 1, repeat input of $\overline{RD}$ pulses until it becomes 0.

(2) Send a command to the D0~D3-pin to input a $\overline{WR}$ pulse.

(3) Confirm that it is not BUSY state as in (1) during input of the next command. Alternatively, wait for the duration of the BUSY time.





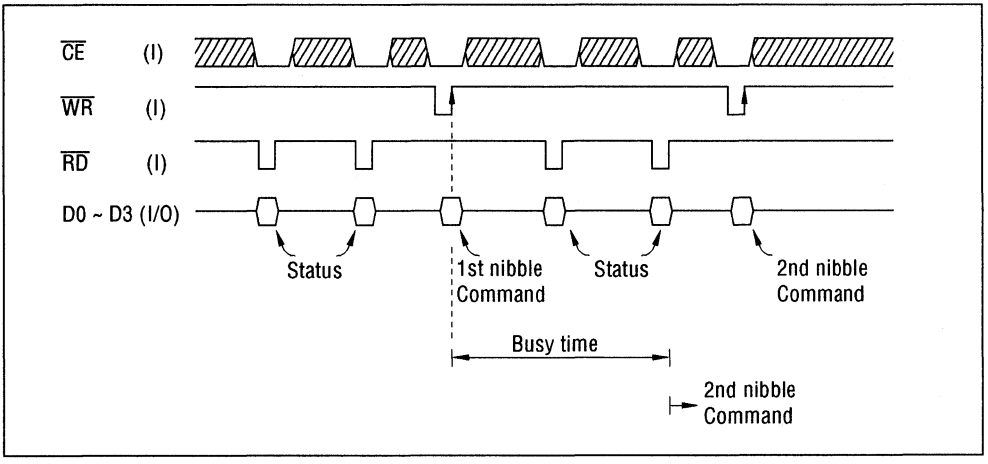
1.2 Input method of 2 nibble command

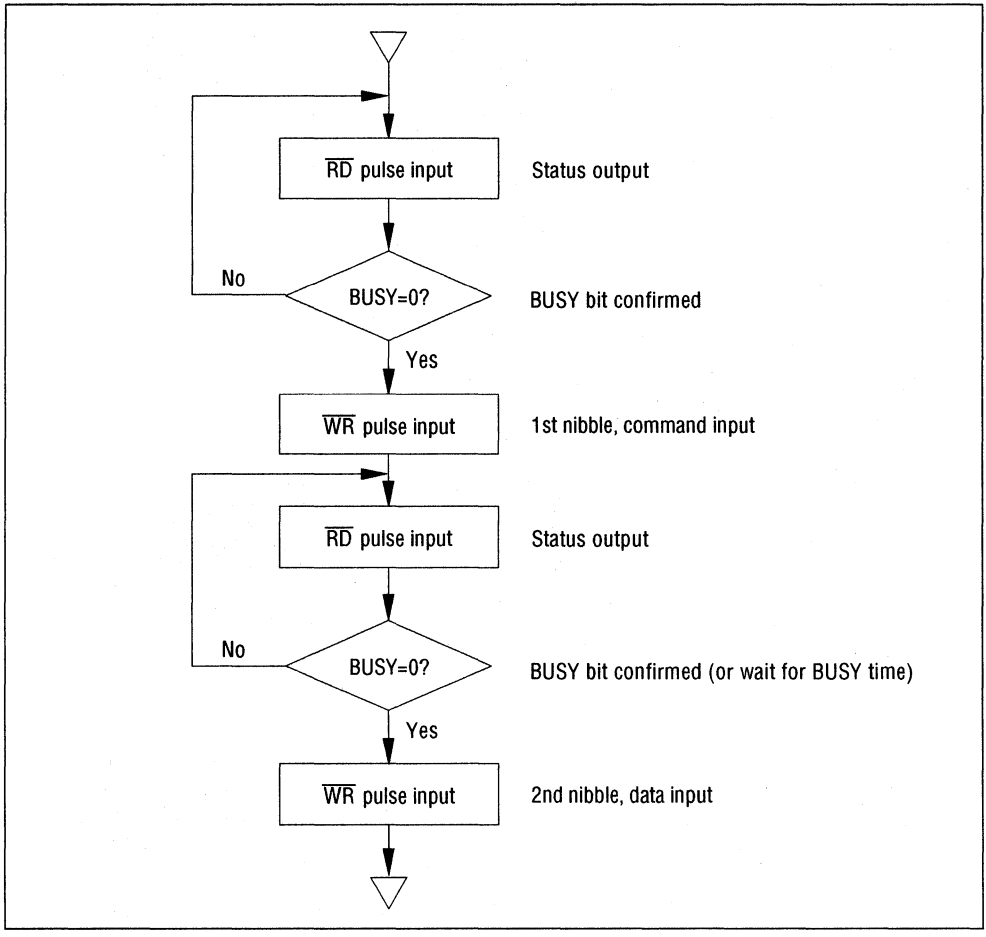
(1) Input a $\overline{RD}$ pulse to confirm the BUSY bit.

(2) Send a command to the D0~D3-pin to input an $\overline{WR}$ pulse.

(3) Input a $\overline{RD}$ pulse and wait until the BUSY bit becomes 0. Alternatively, wait for the duration of the BUSY time.

(4) Set data to the D0~D3-pin to input a $\overline{WR}$ pulse.




RD pulse input
Status output
No
BUSY=0?
BUSY bit confirmed
Yes
WR pulse input
1st nibble, command input
RD pulse input
Status output
No
BUSY=0?
BUSY bit confirmed (or wait for BUSY time)
Yes
WR pulse input
2nd nibble, data input

2. Explanation of commands

Command	Code D3	D2	D1	D0	Function of commands
NOP	0	0	0	0	(NON OPERATION) no function
PAUSE	0	0	0	1	(PAUSE) Suspends record/playback temporarily.
PLAY	0	0	1	0	(PLAYBACK) Set playback mode.
REC	0	0	1	1	(RECORD) Sets recording mode.
START	0	1	0	0	(START) Starts record/playback.
STOP	0	1	0	1	(STOP) Stops record/playback. In record mode, the contents of the address counter are stored in the channel index area as the stop address.
SAMP	0	1	1	0	(SAMPLING FREQUENCY) Specifies the sampling frequency and control mode with the following (1) nibble.
CHAN	0	1	1	1	(CHANNEL) Specifies the channel and control mode with the following (1) nibble.
ADRWR	1	0	0	0	(ADDRESS WRITE) In direct mode, stores the start address and the stop address to the channel index area with the following (8) nibbles.
ADRRD	1	0	0	1	(ADDRESS READ) Reads out the start address and the stop address stored in the channel index area by reading of the following (8) nibbles. During this operation, the contents of the status register cannot be read.
DTRW	1	0	1	0	(DATA READ WRITE) Transfers data to the external serial voice registers through the data bus with preset timing.
EXT	1	0	1	1	(EXTERNAL) Performs record/playback by input and output of ADPCM data through the data bus by preset timing. Use this command when using SRAM or a harddisk as storage media of voice data. Does not control the external serial voice registers nor addresses.
VDS	1	1	0	0	(VOICE DETECT SELECT) Selects the voice triggered starting function condition and the bit length of ADPCM with the following (1) nibble.

Command List

Command	1st nibble command	2nd nibble command D3	D2	D1	D0	Note
NOP	0 0 0 0	———				1 nibble command
PAUSE	0 0 0 1	———				1 nibble command
PLAY	0 0 1 0	———				1 nibble command
REC	0 0 1 1	———				1 nibble command
START	0 1 0 0	———				1 nibble command
STOP	0 1 0 1	———				1 nibble command
SAMP	0 1 1 0	CSEL2	CSEL1	SA1	SA0	2 nibble command CSELn ··· control mode SAn ····· sampling freq
CHAN	0 1 1 1	RCON	CA3	CA2	CA1	2 nibble command RCON ··· control mode CAn ····· channel
ADRWR	1 0 0 0	Inputs address data (2nd-9th nibble)				9 nibble command
ADRRD	1 0 0 1	Outputs address data (2nd-9th nibble)				9 nibble command
DTRW	1 0 1 0	———				Transfers data by preset timing
EXT	1 0 1 1	———				Records/plays back by preset timing
VDS	1 1 0 0	—	BIT	VD1	VD0	2 nibble command BIT ··· ADPCM bit length VDn ·· Voice detection level

3. Explanation of status register

The status register is a 4-bit register and outputs the current state to the D0~D3-pin by input of a "L" level to the $\overline{RD}$ pin.

However, the contents of the status register cannot be read during the execution of ADRRD or during record/playback by the EXT command.

D3	D2	D1	D0
FULL	VPM	RPM	BUSY

Status register

(1) BUSY

"H" level of this bit indicates that the $\overline{RESET}$ operation is in progress or a command is being processed. Do not issue commands at this time.

(2) RPM

This bit becomes "H" level during recording or playback. Do not issue commands except the STOP command, PAUSE command and START command after release of pause.

(3) VPM

This bit becomes "H" level when 1) waiting for voice after voice triggered recording is started and 2) suspending recording/playback by the PAUSE command.

(4) FULL

This status is used for recording in a flex mode. This bit is set to a "H" level when recording is through to the end of the channel capacity which is maximum address of the serial voice register connected to MSM6588. It is reset when either a REC command, PLAY command or START command is input. After recording in flex mode, start recording of the next channel after confirming the FULL bit.

BUSY Condition		BUSY Stauts Bit	Duration of BUSY
After releasing $\overline{\text{RESET}}$		Enable	125μs (Note 3)
After input of 1 nibble command		Enable	16μs
After input of 2 nibble command		Enable	16μs
After input of data of 2 nibble command		Enable	16μs
After input of the ADRWR command		Enable	270μs
After input of address data of the ADRWR command		Enable	50μs
After input of the ADRRD command		Disable	270μs
After output address data of the ADRRD command		Disable	50μs
During execution of the DTRW command	After input of the DTRW command	Enable	16μs
	After input of lower 4-bit of × address	Enable	16μs
	After input of middle 4-bit of × address	Enable	16μs
	After input of upper 4-bit of × address	Enable	270μs
	After input of the REC command	Enable (Note 2)	16μs
	After input of write-in data	Enable (Note 2)	50μs
	After input of the PLAY command	Disable	50μs
	After input of the STOP command	Enable (Note 2)	50μs

Note 1: The duration of BUSY is proportional to the period of the sampling frequency (f_{sam}).

Note 2: When enabling only the data write access after input of the DTRW command, the BUSY state can be confirmed by the BUSY bit.

Note 3: The oscillation stable time is added to the duration of BUSY after releasing $\overline{\text{RESET}}$.
The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a μs for ceramic oscillators.

4. Selection of sampling frequency (SAMP command)

Data that follows the SAMP command will select the sampling frequency.

The relationship between the master clock oscillation frequency (fOSC) and the sampling frequency (f_{sam}) is shown in the following table using data bits SA1 and SA0.

SA1	SA0	Sampling frequency (fsam)	
0	0	f_{osc} / 1024	(4.0kHz)
0	1	f_{osc} / 768	(5.3kHz)
1	0	f_{osc} / 640	(6.4kHz)
1	1	f_{osc} / 512	(8.0kHz)

Note: Numbers in ( ) are for master clock oscillation f_{osc}=4.096MHz.

5. Recording control modes (SAMP and CHAN commands)

In microcontroller interface mode, there are three record control modes. They are direct Fixed, and flex mode. Control mode selection is performed by data bit RCON of the CHAN command and data bits CSEL1 and CSEL2 of the SAMP command.

RCON	CSEL2	CSEL1	Number of record words	Control mode
0	—	—	8-word	Direct mode
1	0	0	8-word	Fixed mode
	0	1	4-word	
	1	0	2-word	
	1	1	8-word	Flex mode

(1) Direct mode

The start and stop address of each channel are input directly to the channel index area using the ADRWR command from a microcontroller. This means that the assignment of memory capacity for each channel is controlled by the microcontroller.

(2) Fixed mode

The start and stop address of each channel is input indirectly to the channel index area by channel selection from a microcontroller. Memory capacity of each channel is assigned by equally dividing the memory capacity of the external serial voice register by the number of recording words.

(3) Flex mode

The start and stop addresses of each channel are input indirectly to the channel index area by channel selection from a micro-controller. There is no assignment of memory capacity of each channel so that the recording time for each channel can be set arbitrarily.

Refer to the Recording Control Modes on each mode description. In the meantime, since the method of re-recording for the fixed and flex modes is the same as that of the stand-alone mode, refer to Item 7, Method of re-recording for the stand-alone mode.

6. Selection of channel (CHAN command)

6.1 Channel selection in direct mode and in flex mode

CA3	CA2	CA1	Channel
0	0	0	ch0
0	0	1	ch1
0	1	0	ch2
0	1	1	ch3
1	0	0	ch4
1	0	1	ch5
1	1	0	ch6
1	1	1	ch7

6.2 Channel selection in fixed mode

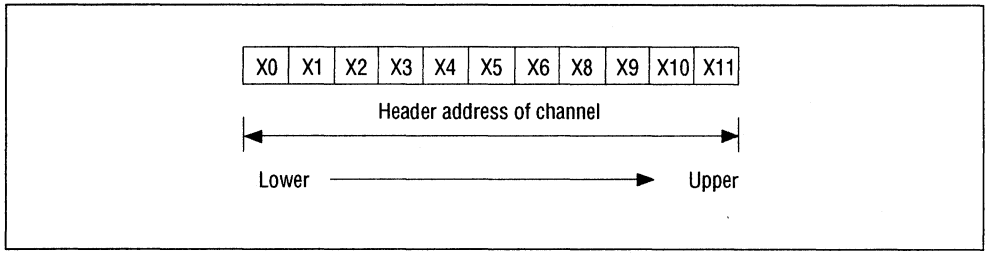
CSEL2	CSEL1	Number of recorded words	CA3	CA2	CA1	Channel
0	0	8-word	0	0	0	ch0
			0	0	1	ch1
			0	1	0	ch2
			0	1	1	ch3
			1	0	0	ch4
			1	0	1	ch5
			1	1	0	ch6
			1	1	1	ch7
0	1	4-word	0	0	—	ch0
			0	1	—	ch1
			1	0	—	ch2
			1	1	—	ch3
1	0	2-word	0	—	—	ch0
			1	—	—	ch1

7. Input/output of start and stop address (ADRWR and ADRRD commands)

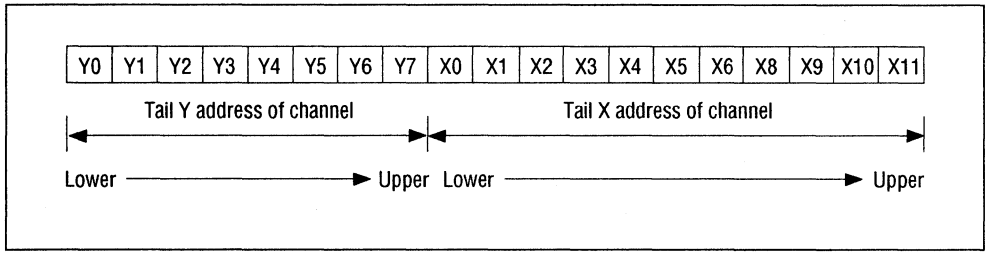
When recording in direct mode, the start and stop address of each channel is directly input to the channel index area by the ADRWR command.

The start address consists of 12bit and the stop address consists of 20bit. They denote the header and tail addresses of the channel, respectively.

Start address STn



Stop address SPn



The X addresses of the voice data area are 008h-FFFh (when connecting the serial voice register for 4Mbit).

The tail Y address changes depending on the ADPCM bit length, the range that can be specified is 00h-A9h (for 3bit ADPCM) and 00h-7Fh (for 4bit ADPCM). For ordinary recording, A9h or 7Fh (tail address) should be input as the tail Y address.

The ADPCM and ADRRD commands input the start and stop address after issuing the commands with the following 8 nibble data.

	D3	D2	D1	D0	Contents
1st nibble	1	0	0	0	ADRWR command
2nd nibble	Y3	Y2	Y1	Y0	Stop address (Y address)
3rd nibble	Y7	Y6	Y5	Y4	
4th nibble	X3	X2	X1	X0	Stop address (X address)
5th nibble	X7	X6	X5	X4	
6th nibble	X11	X10	X9	X8	
7th nibble	X3	X2	X1	X0	Start address (X address)
8th nibble	X7	X6	X5	X4	
9th nibble	X11	X10	X9	X8	

7.1 Input method of address data by the ADRWR command

(1) After confirming the BUSY bit, input the ADRWR command.

(2) After confirming the BUSY bit or waiting for the BUSY time period, input the low 4bit (Y3, Y2,.Y1, Y0) of the Y stop address. This operation is to be repeated for 8 times to input the stop and start address.

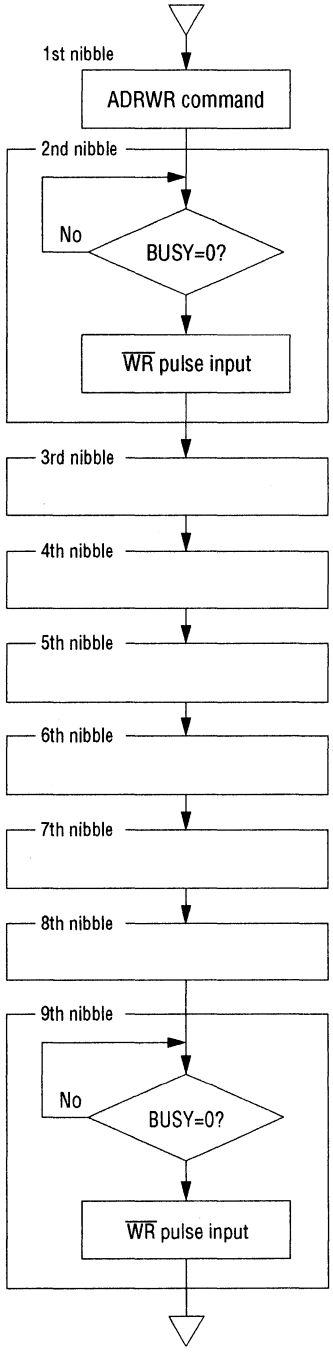
7.2 Output method of address data by the ADRRD command

(1) After confirming the BUSY bit, input the ADRRD command.

(2) Wait for the BUSY time period and input a $\overline{RD}$ pulse to output the address data from the data bus. This operation is to be repeated for 8 times to get the stop and start address to the microcontroller.

(3) After input of the ninth nibble $\overline{RD}$ pulse, the next command is enabled after waiting for the BUSY time period. During the execution of the ADRRD command, the contents of the status register cannot be confirmed. It is necessary to wait for the BUSY time period between each $\overline{RD}$ pulse.

ADRWR Command Flow Chart



BUSY bit confirmed
(or wait for BUSY time)

Input of lower 4 address bits of
Y stop address

Input of upper 4 address bits of
Y stop address

Input of lower 4 address bits of
X stop address

Input of middle 4 address bits of
X stop address

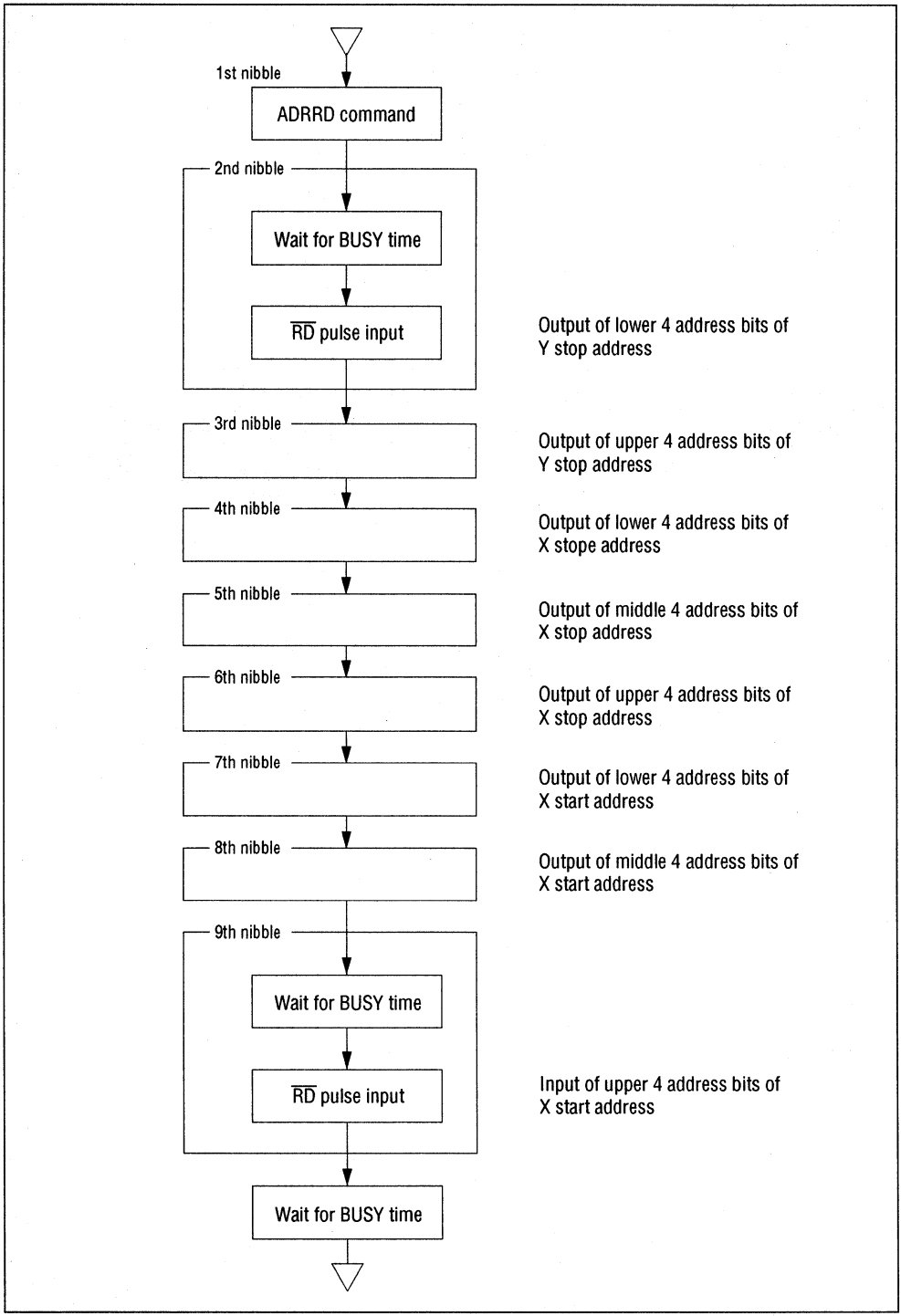
Input of upper 4 address bits of
X stop address

Input of lower 4 address bits of
X start address

Input of middle 4 address bits of
X start address

Input of upper 4 address bits of
X start address

ADRRD Command Flow Chart



8. ADPCM bit length (VDS command)

The ADPCM bit length is specified by the VDS command data (bit).

BIT	ADPCM bit length
0	3-bit
1	4-bit

9. Detection of voice triggered starting function (VDS command)

The detection of voice data and the threshold at which it is detected can be set by the VDS command data bits (VD0 and VD1).

VD1	VD0	Voice detection level Vvds	
0	0	voice detection disabled	
0	1	±VDD/64	(±80mV)
1	0	±VDD/32	(±160mV)
1	1	±VDD/16	(±320mV)

Note: ( ) refers to VDD=5.12 V.

10. Recording method

10.1 Recording in direct mode

(1) Input the VDS command. Specify detection and voice threshold level using VD1 and VD0, set the ADPCM bit length by use of the BIT data.

(2) Input the SAMP command. Specify the sampling frequency by SA0 and SA1 data. In direct mode, CSEL2 data is not looked up.

(3) Input the CHAN command. Specify the channel by CA1, CA2 and CA3 data. By setting RCON data to 0, the control mode is set to the direct mode.

(4) Input the start address and stop address with the ADRWR command to specify the memory area to record into. The address data is stored in the channel index area.

(5) Input the REC command to set recording mode.

(6) Input the START command to begin recording. At this time, the LSI fetches the start address and the stop address of the specified channel from the channel index area and starts recording after storing them to the address counter and the stop address register.

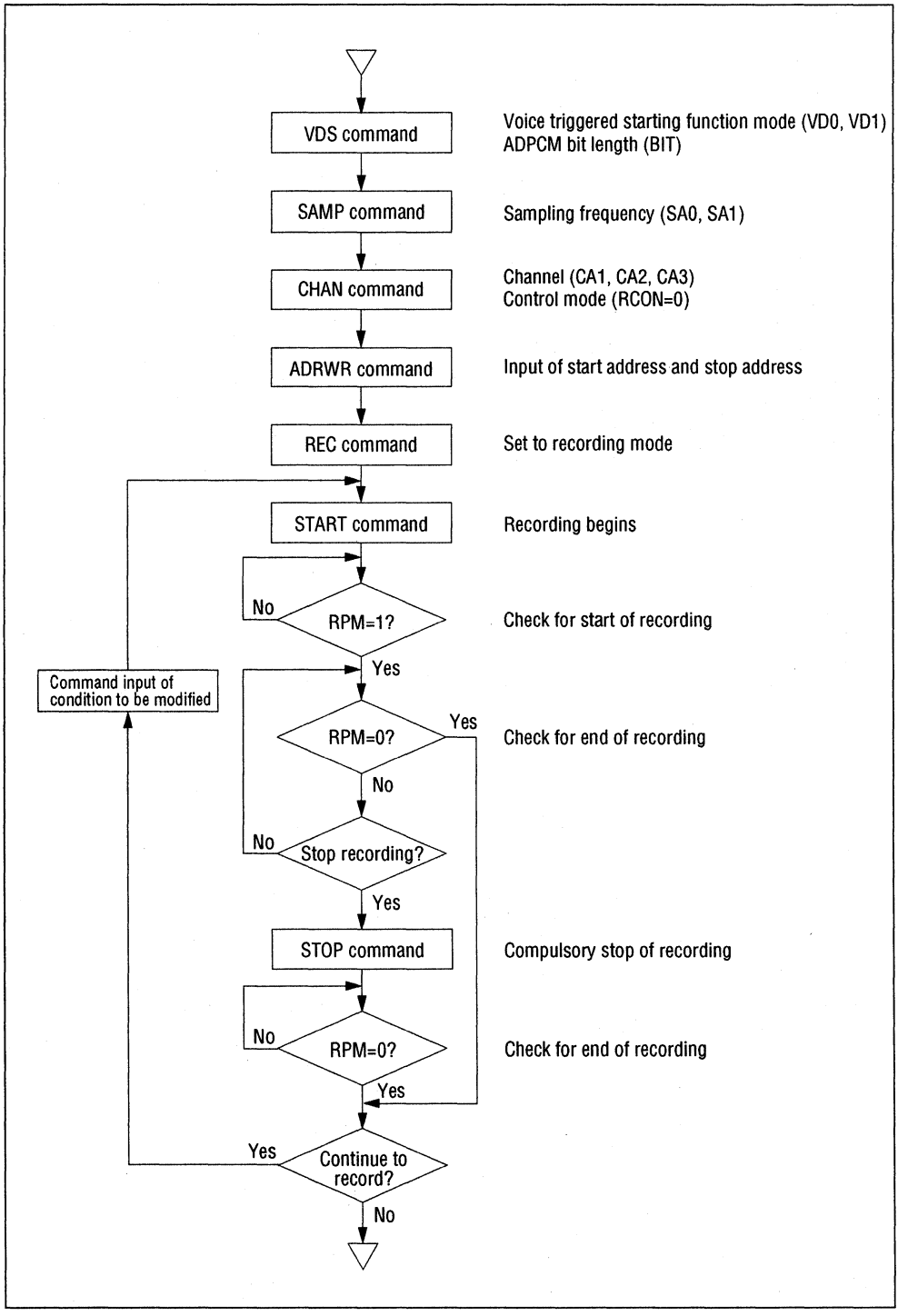
(7) When the contents of the address counter and the stop address register corresponds, the recording is finished. The end of recording is confirmed by the RPM bit of the status register.

(8) If the recording needs to be suspended temporarily, input the STOP command. The contents of the address counter become the new stop address and are automatically stored in the channel index area.

When finishing recording by the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.

(9) If recording is to be continued, specify the condition to be modified by (1)-(4).

Flowchart of Recording in Direct Mode



10.2 Recording method in the fixed and flex modes

(1) Input the VDS command. Specify whether voice detection is needed and set voice detection mode with data bits VD0 and VD1. Specify the ADPCM bit length with the VDS command data (BIT).

(2) Input the SAMP command. Specify the sampling frequency with SA0 and SA1 data and control mode with CSEL1 and CSEL2 data.

(3) Input the CHAN command. Specify the channel with CA1, CA2 and CA3 data. The control mode selection data (RCON) is set to 1.

(4) Input the REC command to set the recording mode.

(5) Start recording by input of the START command.

In fixed mode, recording is begun after storing the start and stop address generated inside the LSI to the address counter and the stop address register respectively, and to the channel index area.

In flex mode, the start address is incremented by +1 from the address of preceding channel (chn-1) fetched from the channel index area.

The stop address is the last address of external serial voice register. Recording is begun after storing each address to the address counter, the stop address register and the channel index area.

(6) When the contents of the address counter and the stop address register corresponds, recording is finished. The end of recording is confirmed by the RPM bit of the status register.

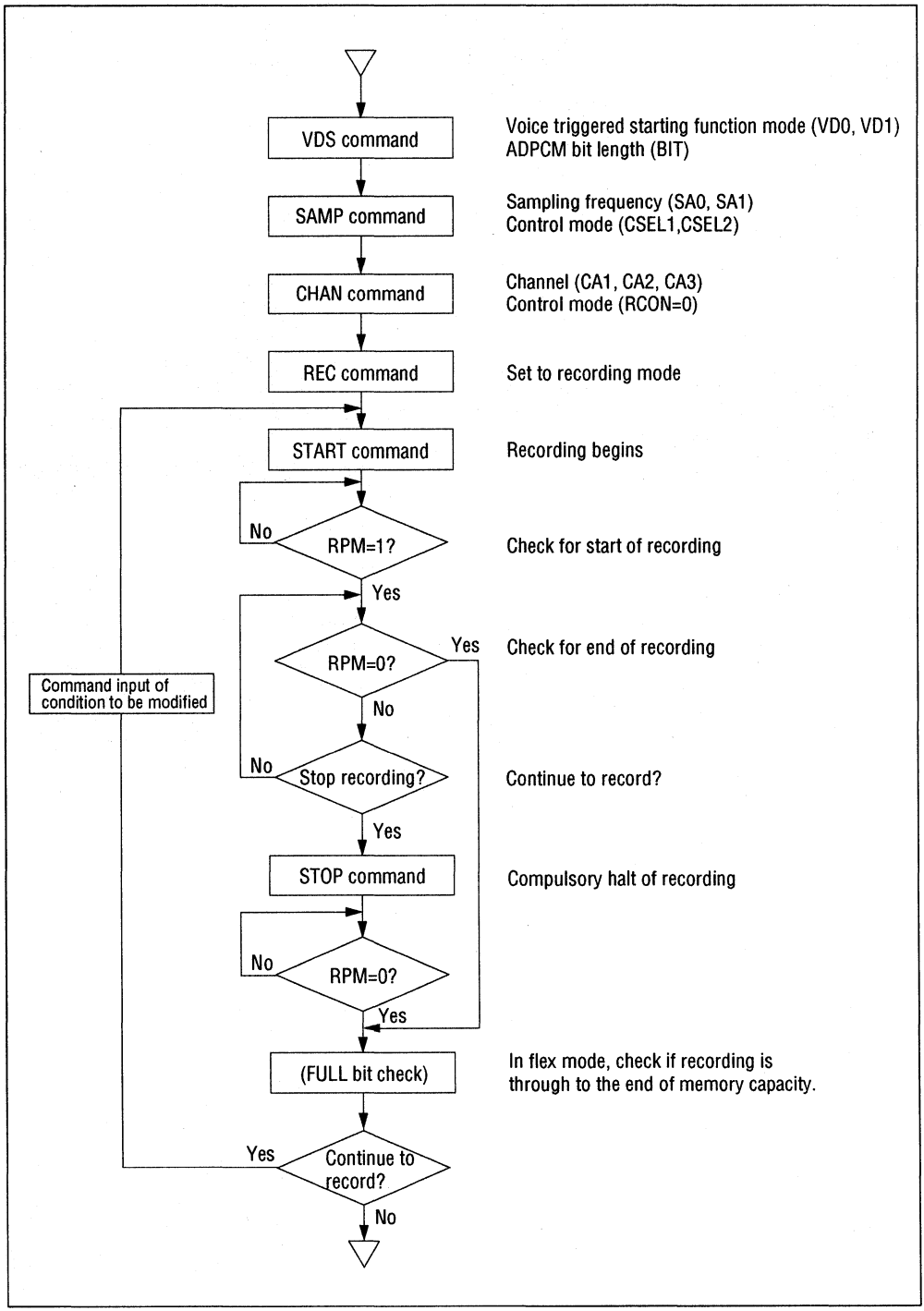
(7) If recording is to be suspended temporarily, input the STOP command. The contents of the address counter become the new stop address and are automatically stored in the channel index area.

After finishing recording using the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.

(8) In flex mode, make sure that the recording is finished to the end of the memory capacity by checking the FULL bit of the status register. If recording is completed to the end of memory, it is not possible to the next channel (chn+1).

(9) If recording is to be continued, specify the condition to be modified by (1)-(3).

Flowchart of Recording in Fixed and Flex Modes



11. Playback method

(1) Input the VDS command. Specify the ADPCM bit length using the VDS command data (BIT). VD0 and VD1 data for voice detection are invalid in playback mode.

(2) Input the SAMP command. Specify the sampling frequency using SA0 and SA1 data and the control mode using CSEL1 and CSEL2 data.

(3) Input the CHAN command. Specify the channel using CA1, CA2 and CA3 and specify the control mode during recording using the RCON data bit. Channel selection during playback can be specified randomly in either control mode.

(4) Input the PLAY command to set playback mode.

(5) Start playback by input of the START command.

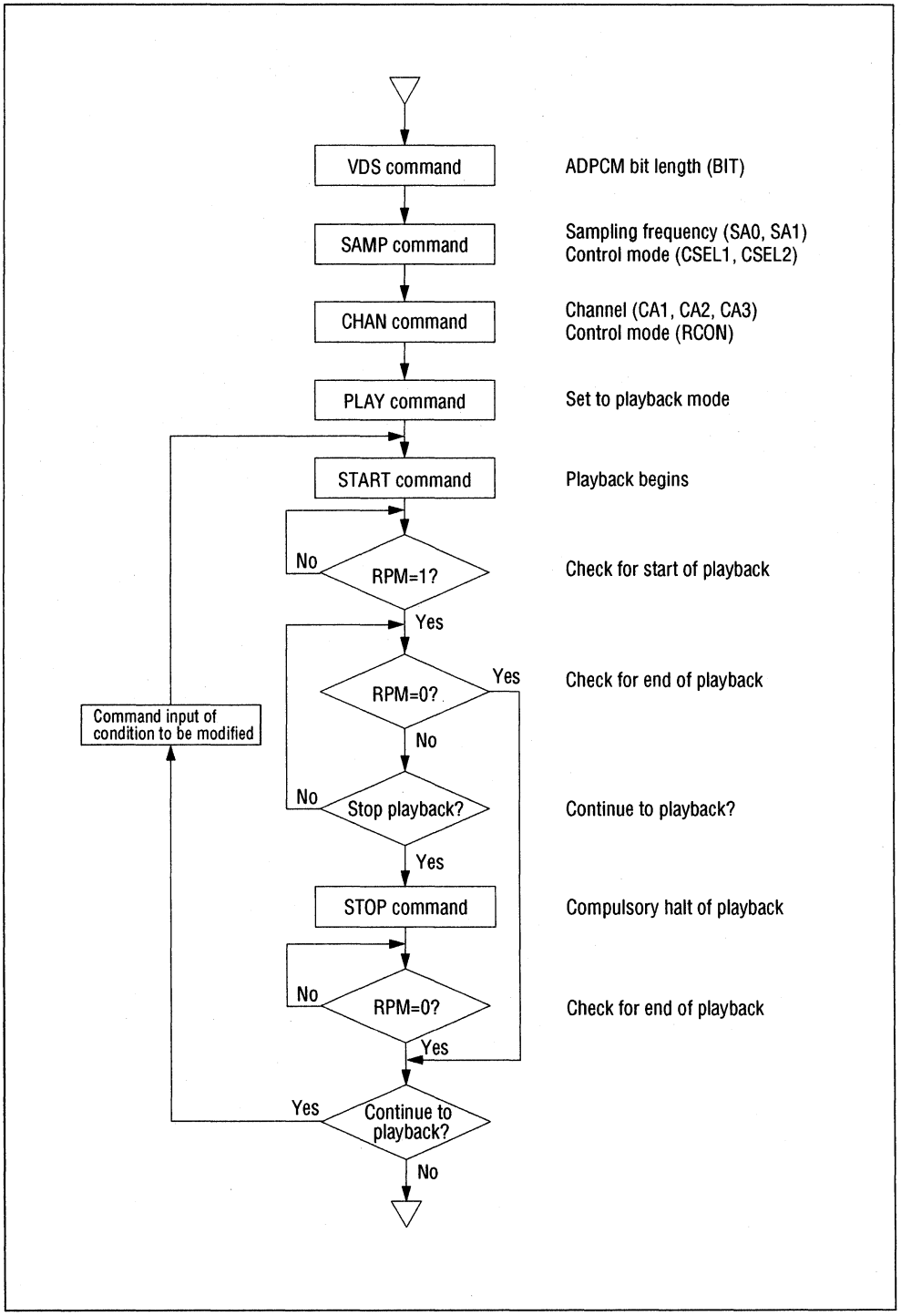
The LSI fetches the start and stop addresses of the specified channel from the channel index area and stores each to the address counter and the stop address register to begin playback.

(6) When the contents of the address counter and the stop address register corresponds, playback is finished. The end of playback is confirmed by the RPM bit of the status register.

(7) If playback is to be suspended temporarily, input the STOP command. After finishing playback using the STOP command, input the next command after confirming that the recording operation is finished using the RPM bit.

(8) If recording is to be continued, specify the condition to be modified by (1)-(3).

Flowchart of Playback

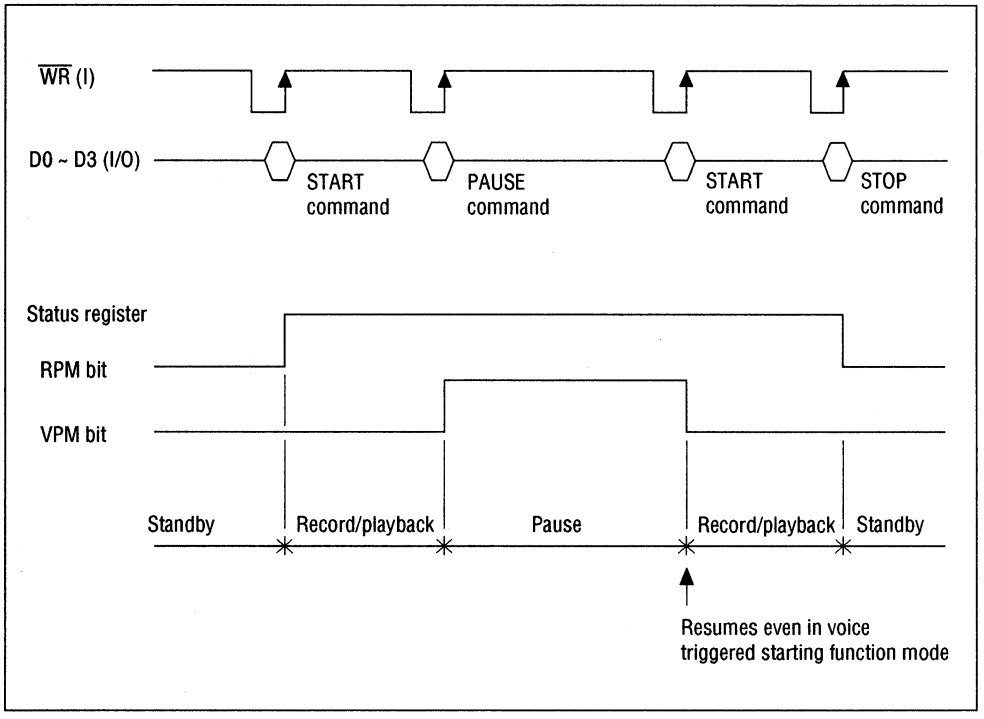


12. Pause method (temporary suspension) with the (PAUSE command)

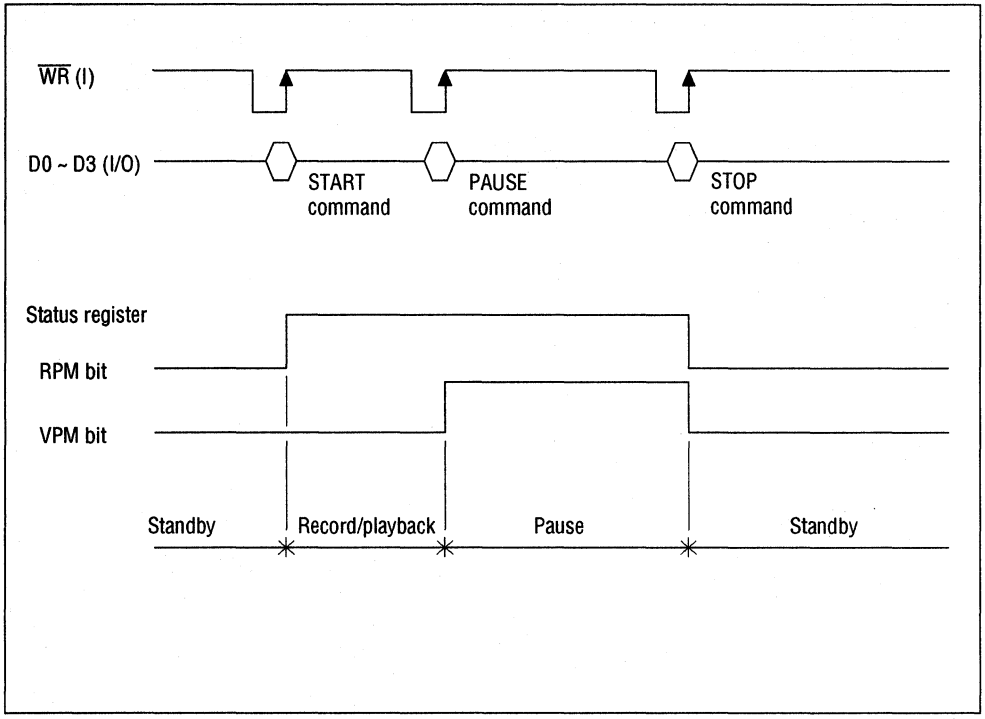
Record/playback is suspended temporarily by input of the PAUSE command and is resumed by input of the START command. During pause, the VPM bit of the status register is 1 and the RPM bit is 1.

When recording is started with voice detection activated, input of the START command during pause resumes recording even in no-voice detected state.

During record/playback, pause and standby for voice, the PAUSE command is invalid.

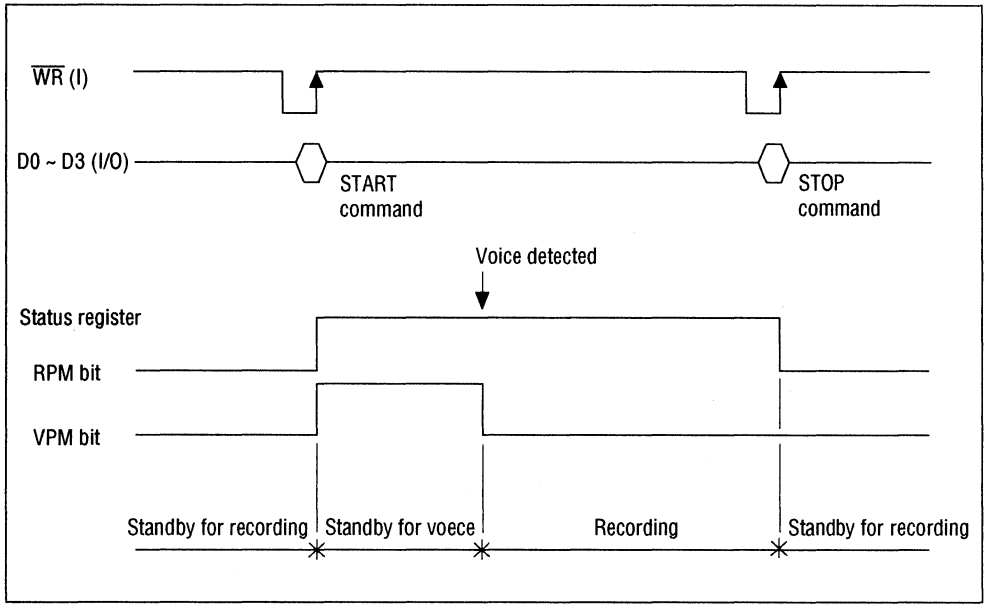


Input of the STOP command during pause, record/playback is finished and the LSI enters standby mode.

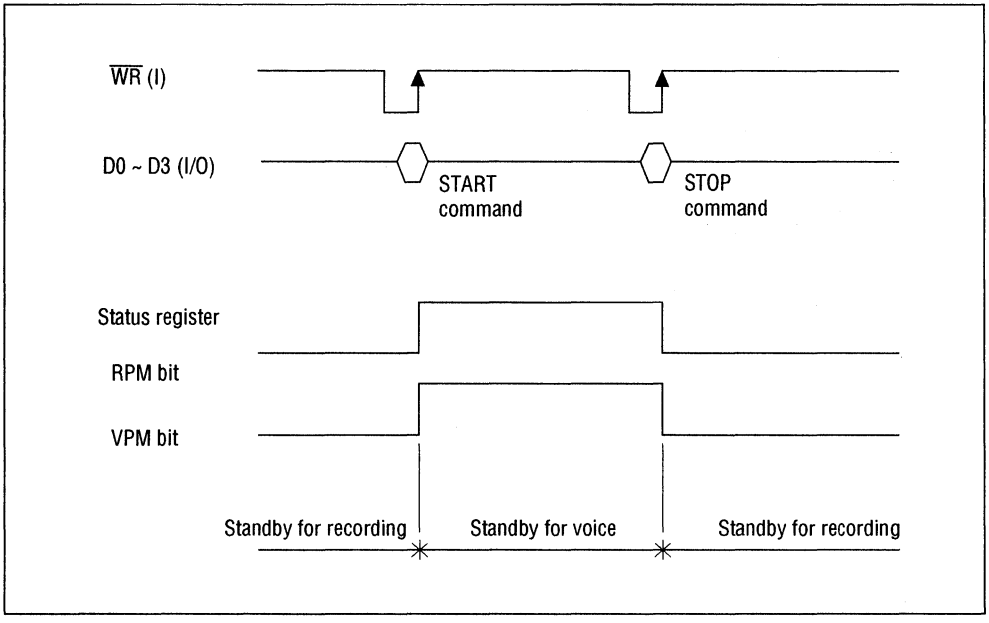


13. Voice detection operation (VDS command)

By setting the VD0 and VD1 data bits of the VDS command, recording thru voice detection starts. Using voice detection, it is possible to eliminate the silence data prior to the detection of voice data thus utilizing the memory capacity efficiently. However, elimination of silence data, once voice triggered recording has begun, does not occur. During standby for voice, the VPM bit of the status register is held at a 1 and is reset back to 0 when recording starts after voice is detected. The RPM bit becomes 1 after recording starts.



Input of a STOP command during standby for voice causes the LSI to first finish standby for voice and then enter standby for recording.



14. Address control operation

Address control operation during record/playback is performed via the channel index area.

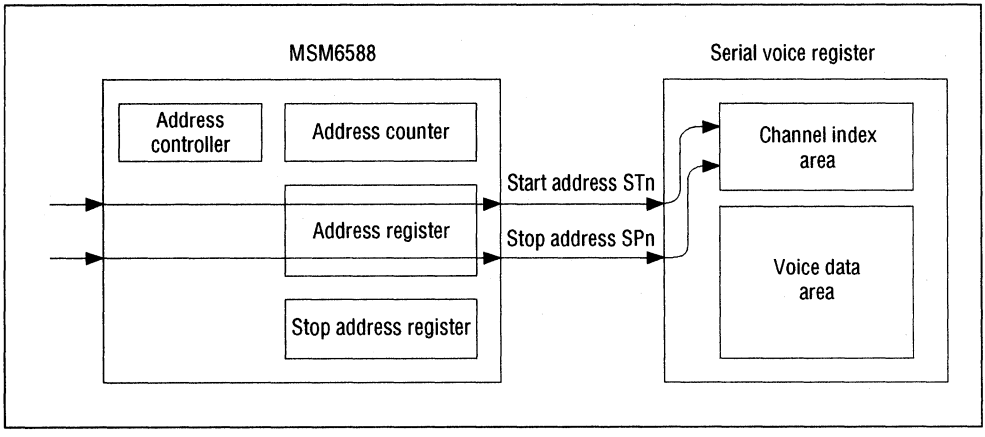
Transfer of data with the channel index area differs depending on the control mode during recording.

14.1 Address control operation during recording

14.1.1 Direct mode recording

(1) Address data is directly written to the channel index area by the ADRWR command.

1) ADRWR Command Input

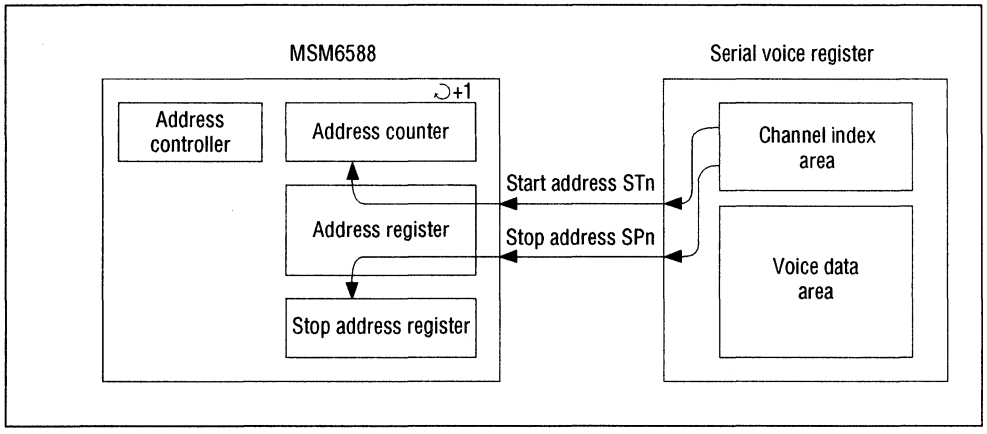


(2) With the input of a START command, the start and stop addresses are read from the channel index area. They are then set to the address counter and the stop address register via the address register.

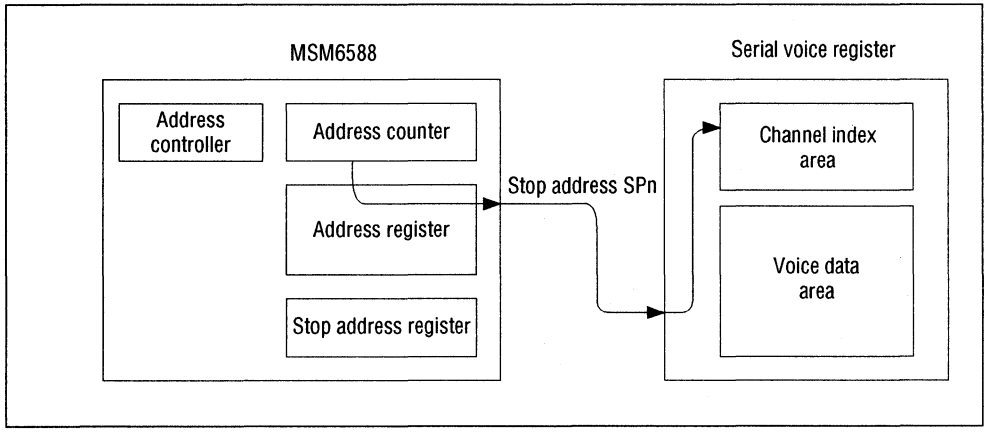
After this address control operation, recording is begun and the address counter counts up.

(3) When recording is stopped by the STOP command, the contents of the address counter at that time are stored in the channel index area as the new stop address.

2) START Command Input (recording begins)



3) STOP Command (recording stops)

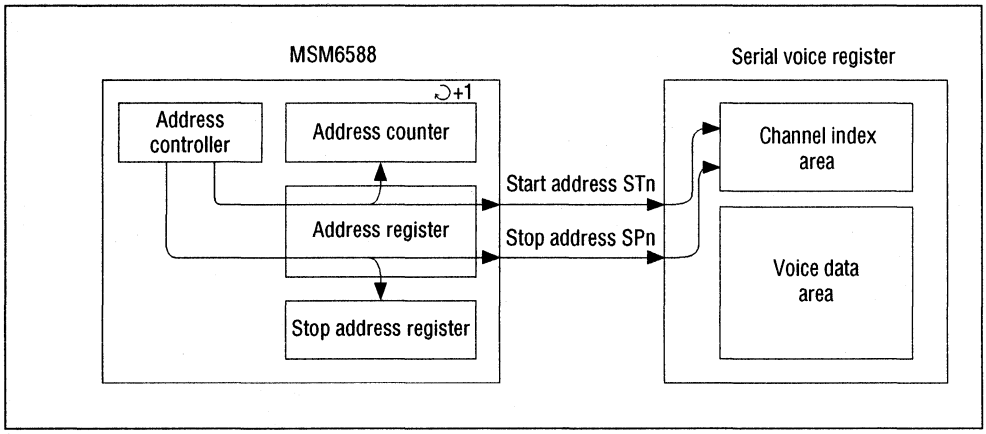


14.1.2 Fixed mode recording

(1) With the input of a START command, the start and stop address generated in the address controller is set to the address counter and the stop address register via the address register, respectively. The address data is stored in the channel index area. After this address control operation, recording is begun and the address counter counts up.

(2) When the recording is stopped by the STOP command, the contents of the start address counter at that time are stored in the channel index area as the new stop address.

1) START Command Input (recording begins)



14.1.3 Flex mode recording

(1) With the input of a START command, the stop address of the preceding channel (SPn-1) is read out from the channel index area.

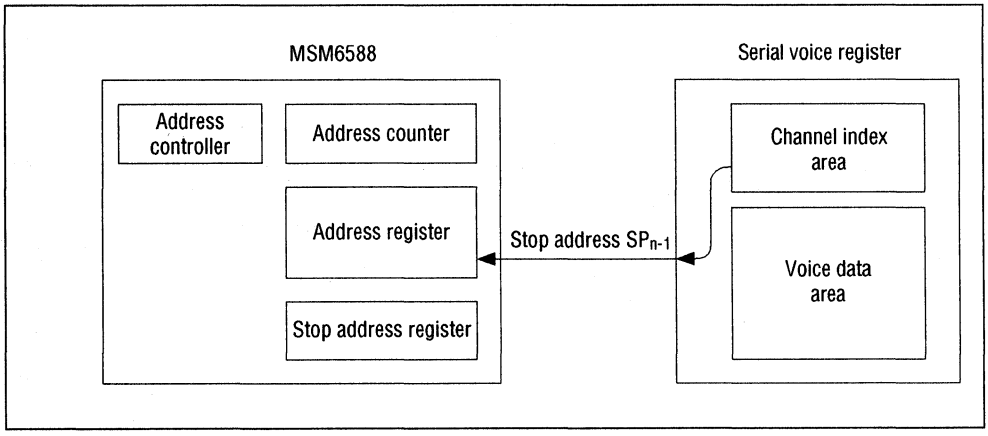
(2) Next, address data incremented by +1 from the contents of the stop address are stored in the address counter and the channel index area as the start address (STn=SPn-1+1).

The stop address generated in the address controller (the maximum address of the serial voice register) is set in the stop address register and is stored in the channel index area.

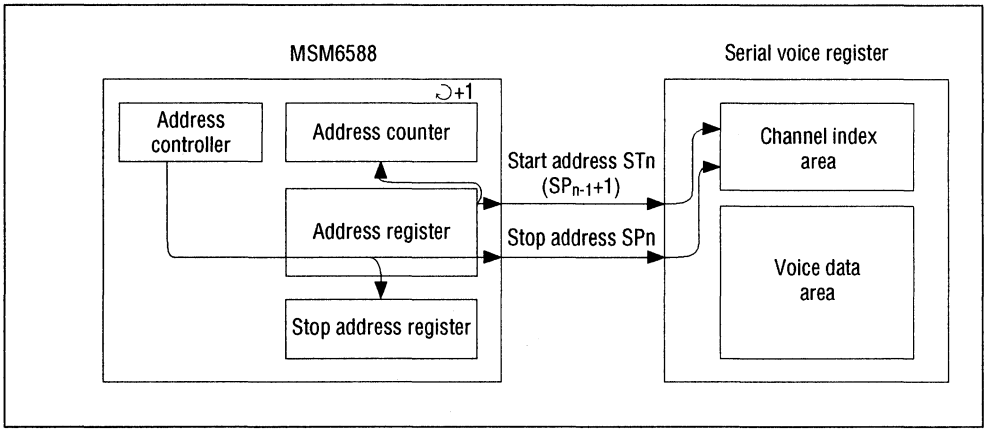
After this operation, recording is begun and the address counter counts up.

(3) When recording is finished by the STOP command, the contents of the address counter at that time are stored in the channel index area as the new stop address.

1) START Command Input



2) Start of Recording



14.2 Address control operation during playback

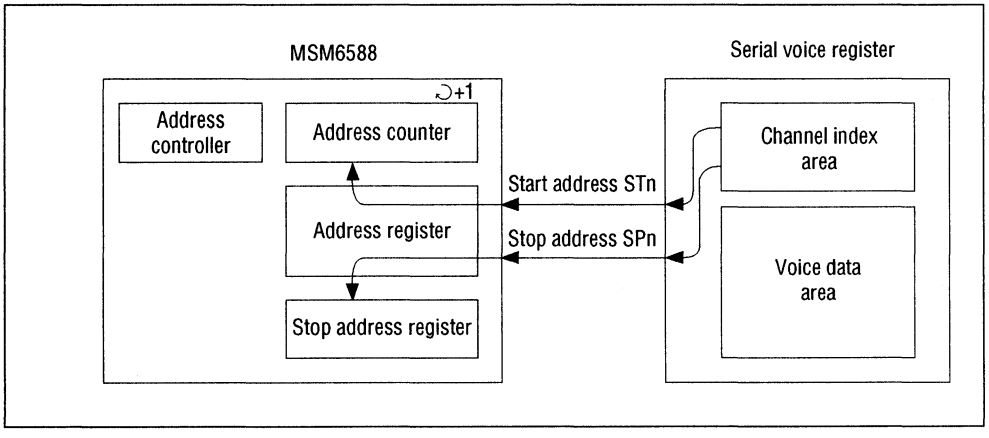
During play back, the LSI performs playback using the address and stop addresses stored in the channel index area regardless of the control mode.

(1) With the input of a START command, the LSI first reads the start and stop address from the channel index area. They are then set to the address counter and the stop address register, respectively, through the address register.

After this address control operation, playback is begin and the address counter counts up.

(2) When a STOP command is input, playback is stopped. No address control operation is performed at this time.

1) START Command Input (playback starts)



15. Multi-channel record/playback method

It is possible to record/playback on multiple channels by preparing memory corresponding to the channel index area that stores the start and stop addresses of each channel inside a microcontroller or equivalent external circuit.

Recording/playback of multiple channels is performed in the direct mode and the channel index area can be used as temporary address data storage. In the case of playback for the fixed message stored into the serial voice ROM, the address data of each word can be similarly stored into a ROM in a microcontroller. The following shows the procedure.

15.1 Multi-channel recording method

(1) Recording conditions are specified by a command input similar to the recording method in direct method. Channels can be specific (e.g. ch0).

(2) The stop and start addresses can be written into the channel index area by the ADRWR command.

(3) Recording is started.

(4) After recording is performed, the stop address which is stored in the channel index area by the ADRRD command is read out.

(5) The stop address is stored in microcontroller memory.

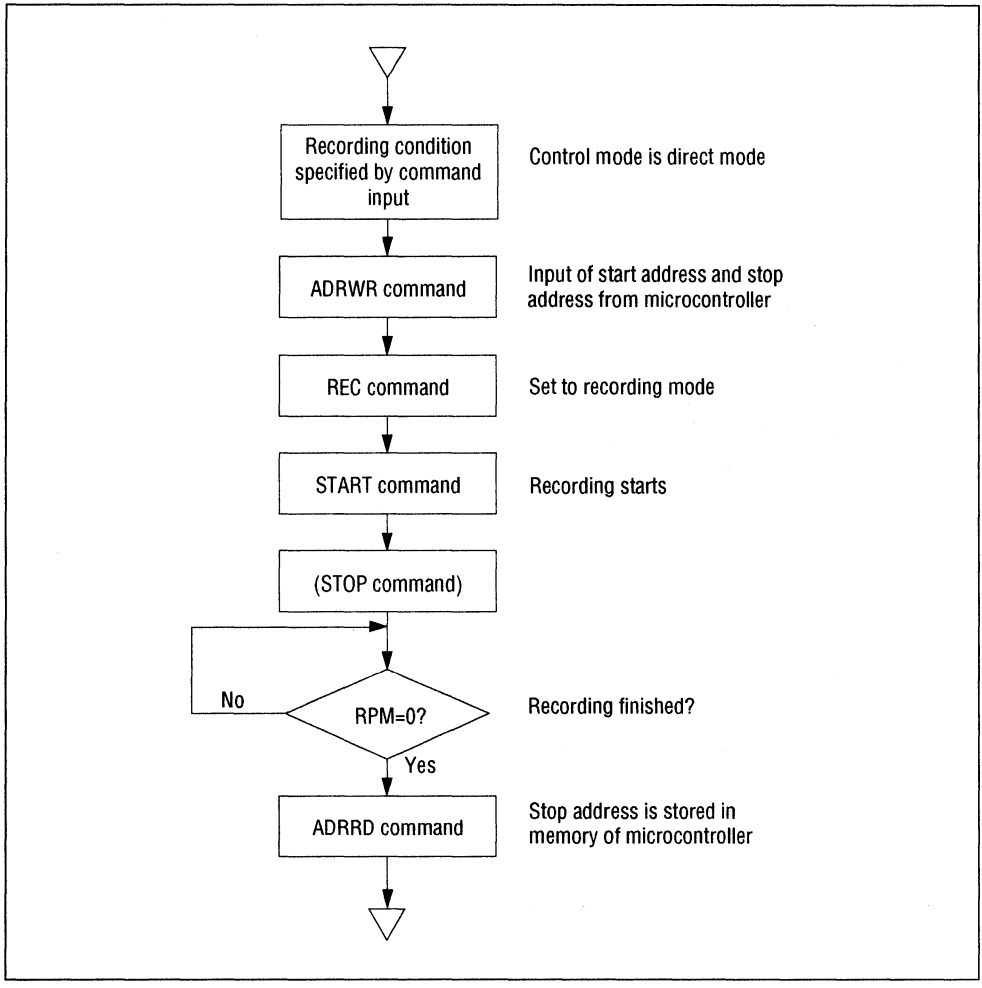
15.2 Multi-channel playback method

(1) Playback conditions are specified by a command input.

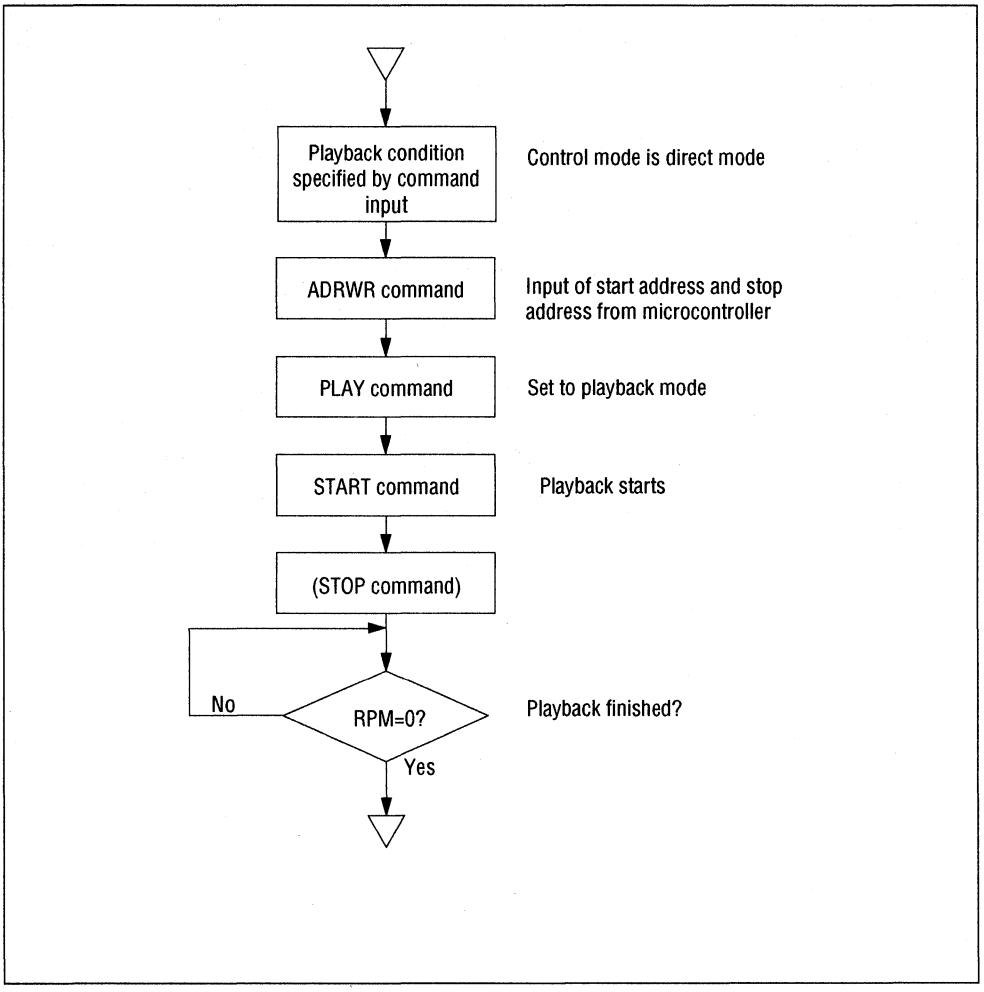
(2) The stop and start addresses that are stored in microcontroller memory are written in the channel index area by the ADRWR command.

(3) Playback is started.

Flowchart to Multi-channel Recording



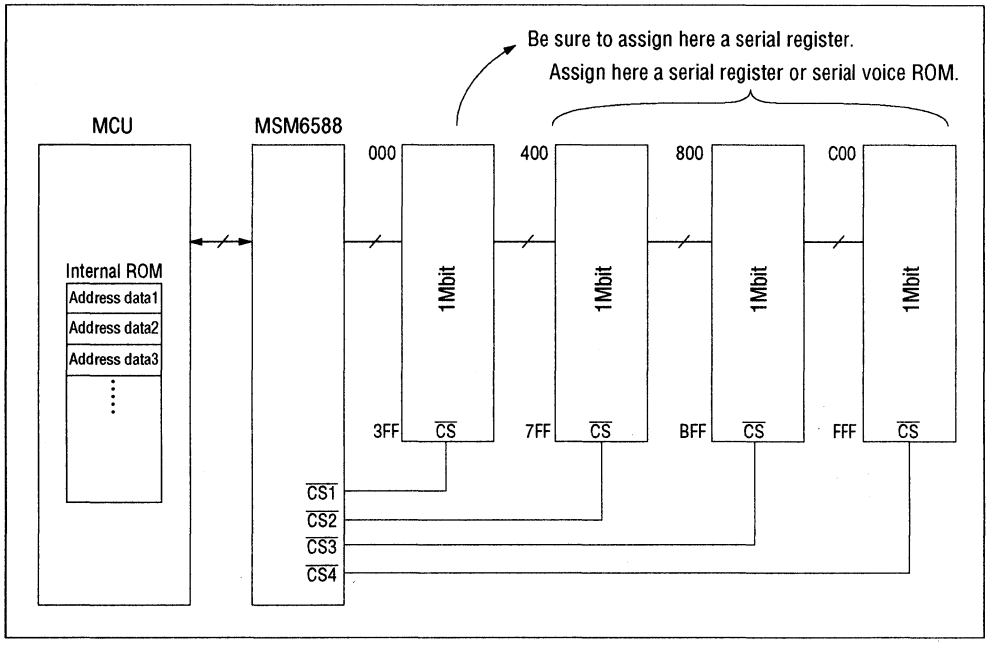
Flowchart to Multi-channel Playback



16. Playback method by means of a serial voice ROM

The following describes how to play a fixed message by connecting a serial voice ROM to the MSM6588.

16. 1 Circuit and memory configrurations



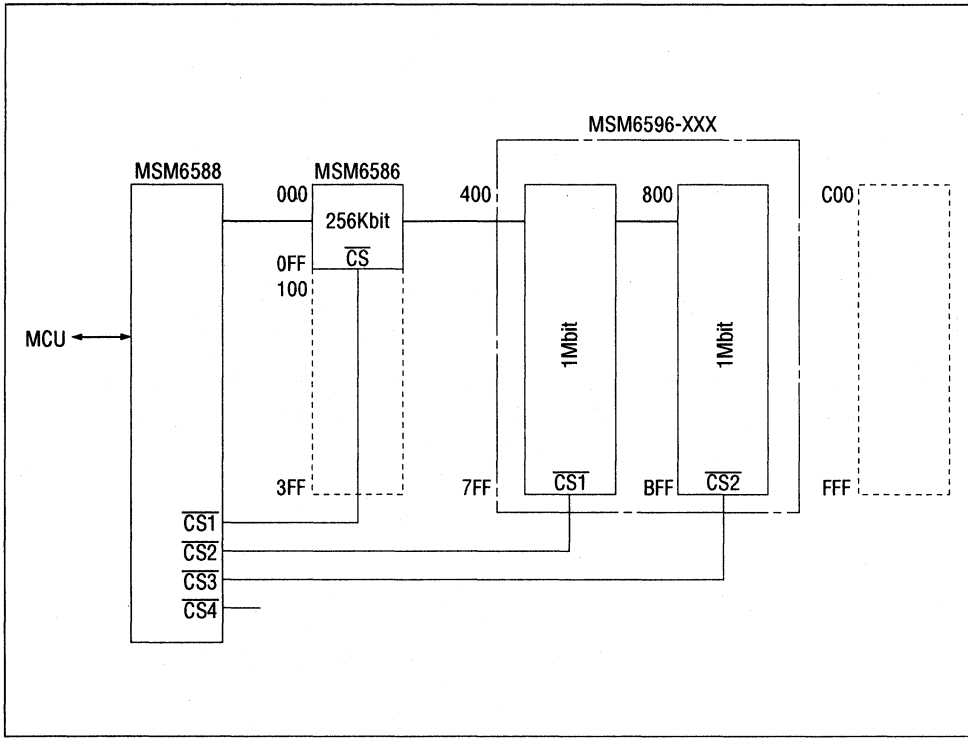
	Address space (X address)	Serial register	Serial voice ROM
$\overline{CS1}$	000h~3FFh	Assignable	**Unassignable**
$\overline{CS2}$	400h~7FFh	Assignable	Assignable
$\overline{CS3}$	800h~BFFh	Assignable	Assignable
$\overline{CS4}$	C00h~FFFh	Assignable	Assignable

A serial register or serial voice ROM is assigned in the unit of 1Mbit ($\overline{CSn}$).

Note: Be sure to connect a serial register to $\overline{CS1}$.
It is impossible to connect only a serial voice ROM and use it for playback only.

The following circuit configuration shows the case where 256Kbit and 2Mbit are used for playback and for a fixed playback, respectively.

For playback (variable message):
256Kbit serial register MSM6586
For fixed message:
2Mbit serial voice ROM MSM6596-XXX



$\overline{CS1}$	000h~0FFh	Serial register for variable message
	100h~3FFh	Unused (no addressing)
$\overline{CS2}$	400h~7FFh	Serial voice ROM for fixed message
$\overline{CS3}$	800h~BFFh	
$\overline{CS4}$	C00h~FFFh	Unused (no addressing)

Serial register
256Kbit MSM6586
512Kbit MSM6587
1Mbit MSM6389

Serial voice ROM
1Mbit MSM6595-XXX
2Mbit MSM6596-XXX
3Mbit MSM6597-XXX

16. 2 How to contorol playback when a serial voice ROM is used.

(1) ROM for saving address data

A start address and stop address for each word must be previously saved in the microcontroller's ROM when a serial voice ROM is used for playback.

The address data is 32bit per word.

	Upper X-address	Lower Y-address	
Start address	12bit	—	32bit per word
Stop address	12bit	8bit	

MCU's ROM size =

32bit × number of voice words

(2) Address data

Address data described in the address correspondence table are saved in the MCU's ROM. The following offset addresses are added to $\overline{CS2}$ thru $\overline{CS4}$, to which a serial voice ROM is assigned.

Assigned to	Offset address
$\overline{CS2}$	+400h
$\overline{CS3}$	+800h
$\overline{CS4}$	+C00h

For example, in the previous circuit, when MSM6596-600 is assigned to $\overline{CS2}$ and $\overline{CS3}$, and "GOZEN" GOZEN that means "morning" is voiced, the address is shown below.

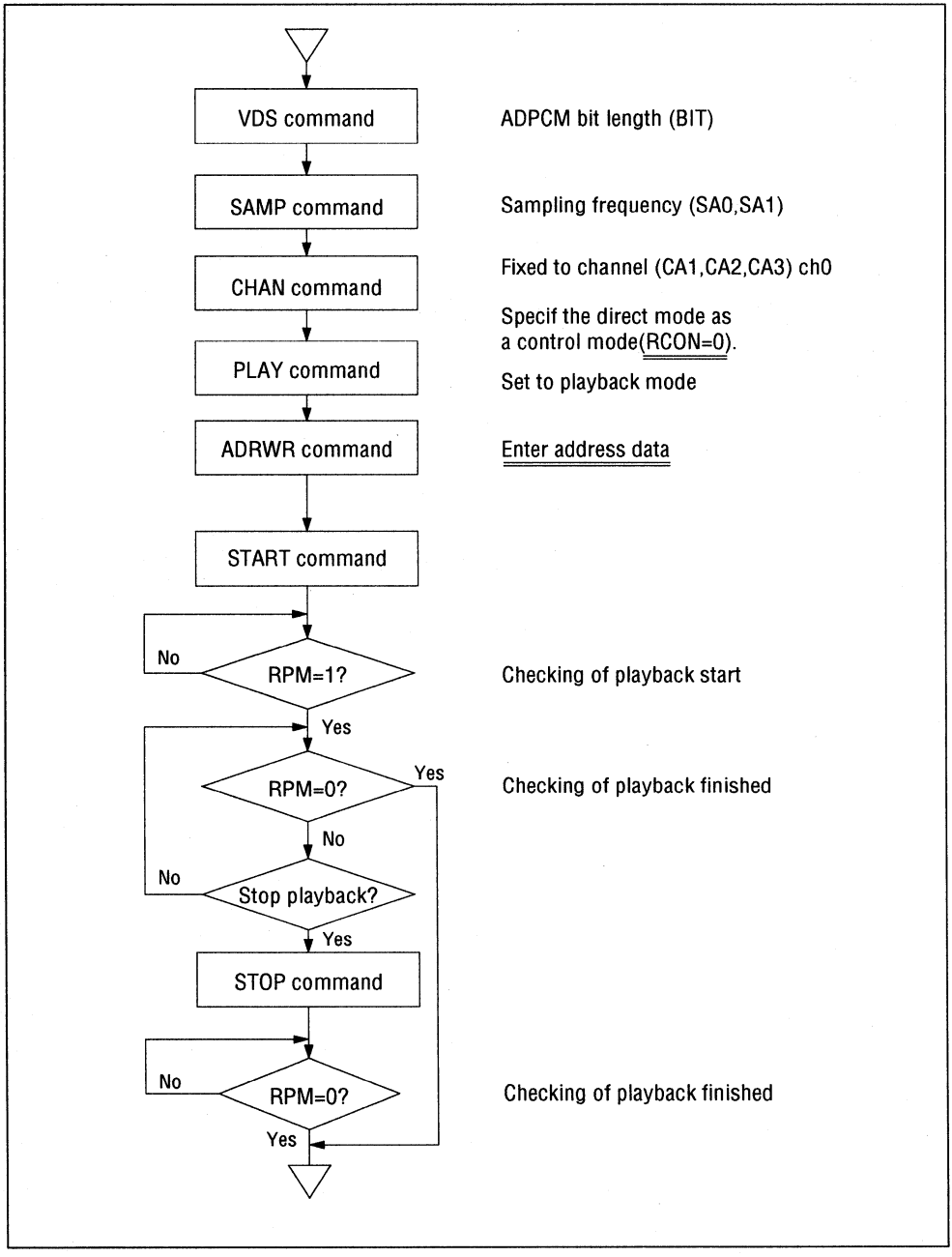
	Start X	Stop X	Stop Y	
No.1. 00	GOZEN	0	10	5D
		↓ +400h	↓ +400H	↓ no addition
	Address to be specified⇒	400h	410h	5Dh

(3) Flowchart to Serial Voice ROM

The serial voice ROM playback differs in its playback method from the serial register playback because after specifying the channel the serial voice ROM playback requires to enter the address data that are saved in the MCU's ROM, using the ADRWR command.

The channel index area is used temporarily.

Therfore, for example, ch0 is used only for serial voice ROM playback.



17. Data transfer method with external serial voice registers (DTRW command)

Data transfer can be performed with external serial voice registers using the DTRW command.

After input of the DTRW command, the X address of the serial voice register for read/write is specified. Data in 4-bit nibbles are transferred from the header of the X address specified. Although the serial voice registers are composed of the X address times 1K-bit (Y direction), the address can be specified only in the X direction and no random address specification can be made that selects the middle of the Y direction.

A single DTRW command input can do read/write operations continuously if they are in the range of the same serial voice register. When the operation extends to other serial voice registers, it is necessary to suspend the operation temporarily and re-specify the address by input of the DTRW command.

The following is the DTRW command input procedure.

(1) The sampling frequency is specified by input of the SAMP command. Because the access time of data transfer by the DTRW command is proportional to the period of the sampling frequency, the highest frequency is usually selected.

(2) Input the DTRW command.

(3) Specify the header X address of the serial voice register with 3 $\overline{WR}$ pulses.

(4) Wait for BUSY time. Alternatively, the BUSY bit of the status register can be used to confirm this.

(5) For writing data, input the data to be written with a $\overline{WR}$ pulse after input of the REC command. It is necessary to wait for BUSY time between each $\overline{WR}$ pulse.

When performing data/write by a single DTRW command, the BUSY state can be checked by the BUSY bit of the status register but if data read is also performed, confirmation by the BUSY bit cannot be performed.

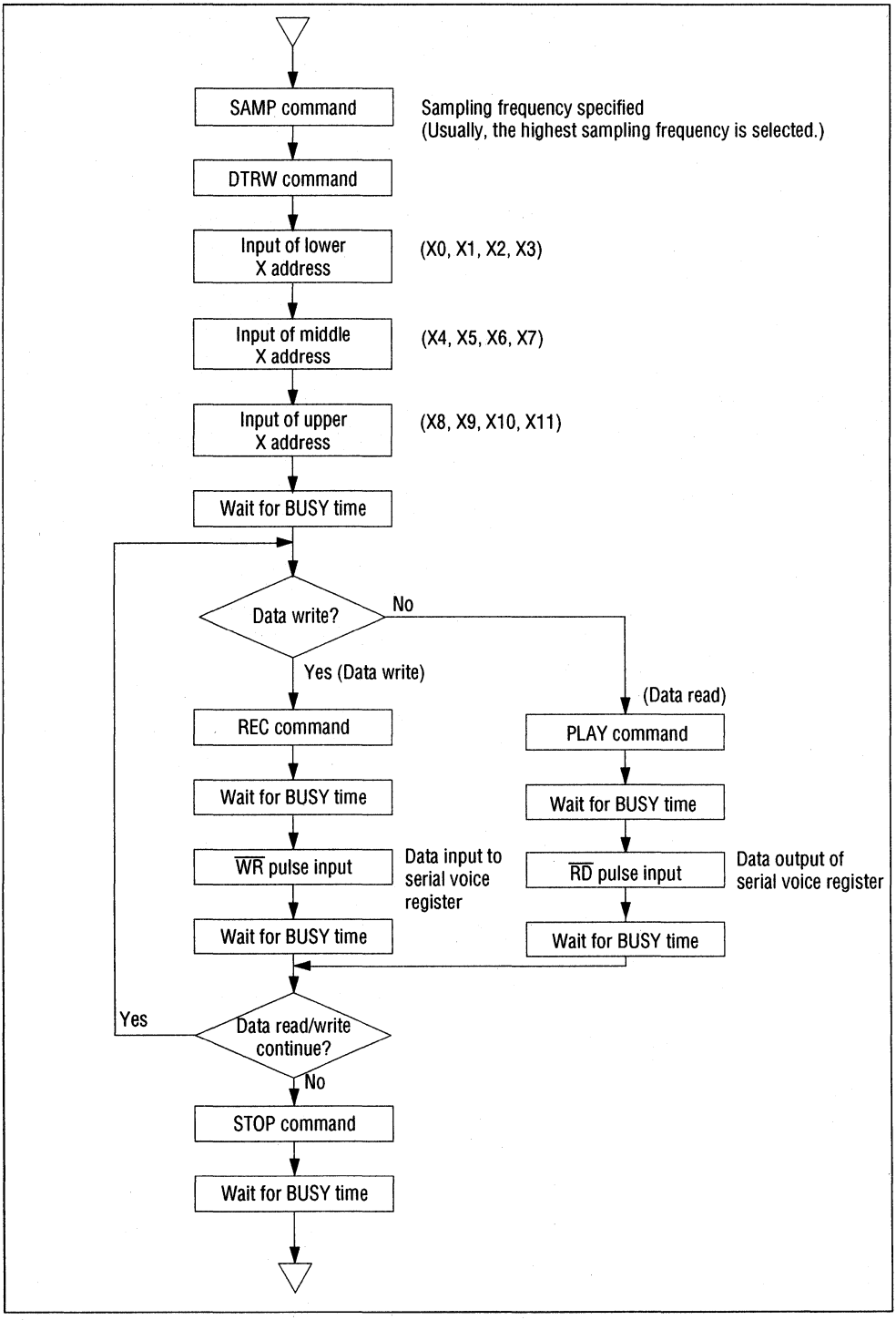
(6) For data read, 4-bit of data are output from the data bus by input of a $\overline{RD}$ pulse, after waiting for the BUSY time, after the input of the PLAY command.

For data read, confirmation of BUSY state by the BUSY bit is invalid.

(7) If data read/write is to be continued, specify data transfer by read/write mode using the PLAY/REC commands.

(8) If data read/write is to be terminated, input the STOP command. Wait for BUSY time and start input of the next command. If data read is performed, confirmation by the BUSY bit is invalid.

Flowchart of data transfer by the DTRW command



18. Method of record/playback by input /output of voice data from the data bus (EXT command)

When SRAM or a harddisk is used to store voice data instead of the serial voice registers, use the EXT command to do record/playback.

During record/playback using the EXT command, voice data (ADPCM data) is directly input/output from the data bus at the sampling frequency. There is no address control nor external serial voice register control at this time, therefore, it is necessary to use the microcontroller to control recording time and addresses.

Pause, voice triggered starting function and selection of channels cannot be made during record/playback. Valid commands are PLAY, REC, STOP, SAMP, VDS and EXT only.

18.1 EXT command recording method

(1) The sampling frequency is specified by SA0 and SA1 data of the SAMP command.

(2) The ADPCM bit length is specified by BIT data of the VDS command.

(3) Input the REC command to set the recording mode.

(4) Input the EXT command to start recording. The sampling frequency clock is output from the MON pin.

(5) When the MON output pin becomes "H" level, input a $\overline{RD}$ pulse to fetch ADPCM data from the data bus. The upper 3bit (D3~D1 pin) are valid for 3bit ADPCM.

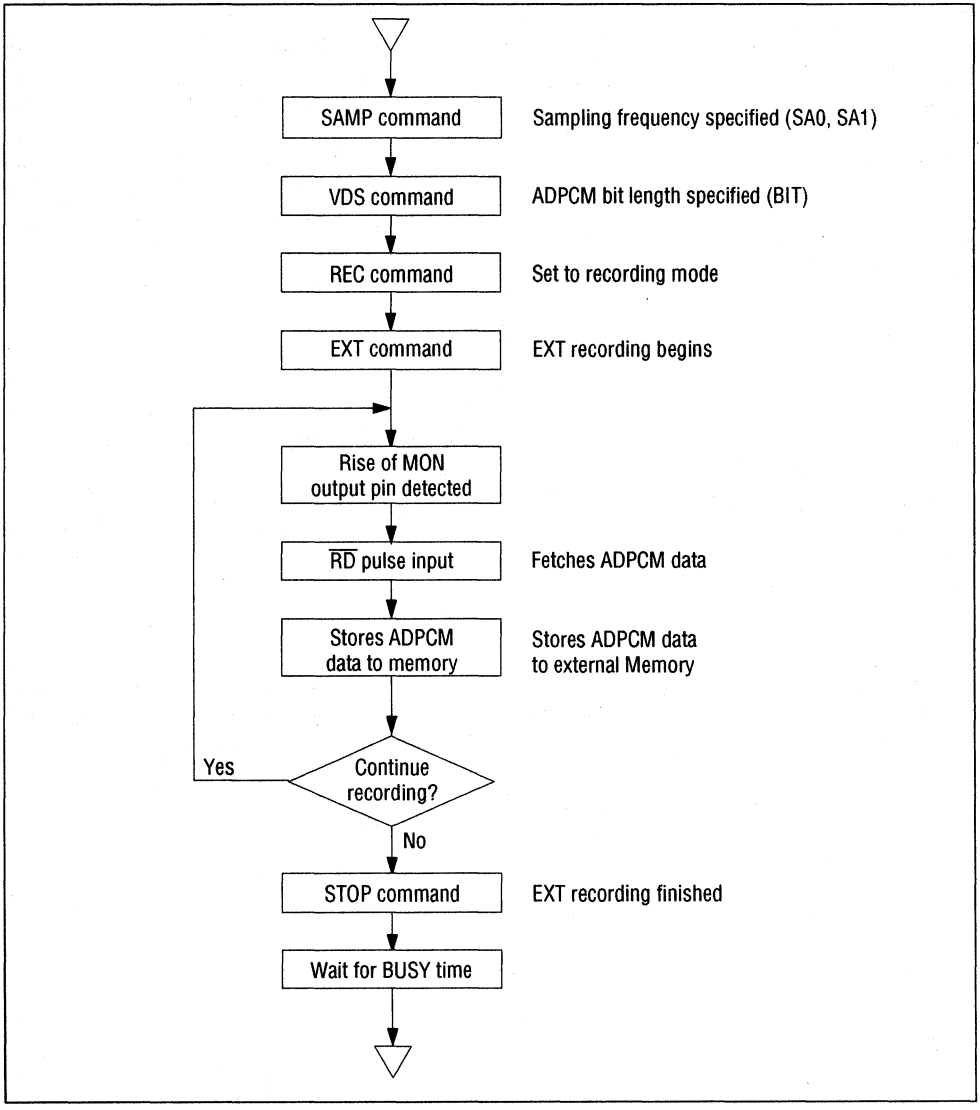
(6) Store ADPCM data to external memory.

(7) Repeat steps (5) and (6) to continue recording.

(8) To stop recording input a STOP command. Recording can be continued for an indefinate period of time until the STOP command is input.

(9) As the status register cannot be checked during recording with the EXT command, it is necessary to wait for BUSY time after input of the STOP command to start input of the next command.

Flowchart of recording with the EXT command



18.2 EXT command playback method

(1) Specify the sampling frequency by SA0 and SA1 data of the SAMP command.

(2) Specify the ADPCM bit length of recording by BIT data of the VDS command.

(3) Input the PLAY command to set playback mode.

(4) Input the EXT command to start playback. The sampling frequency clock is output from the MON pin.

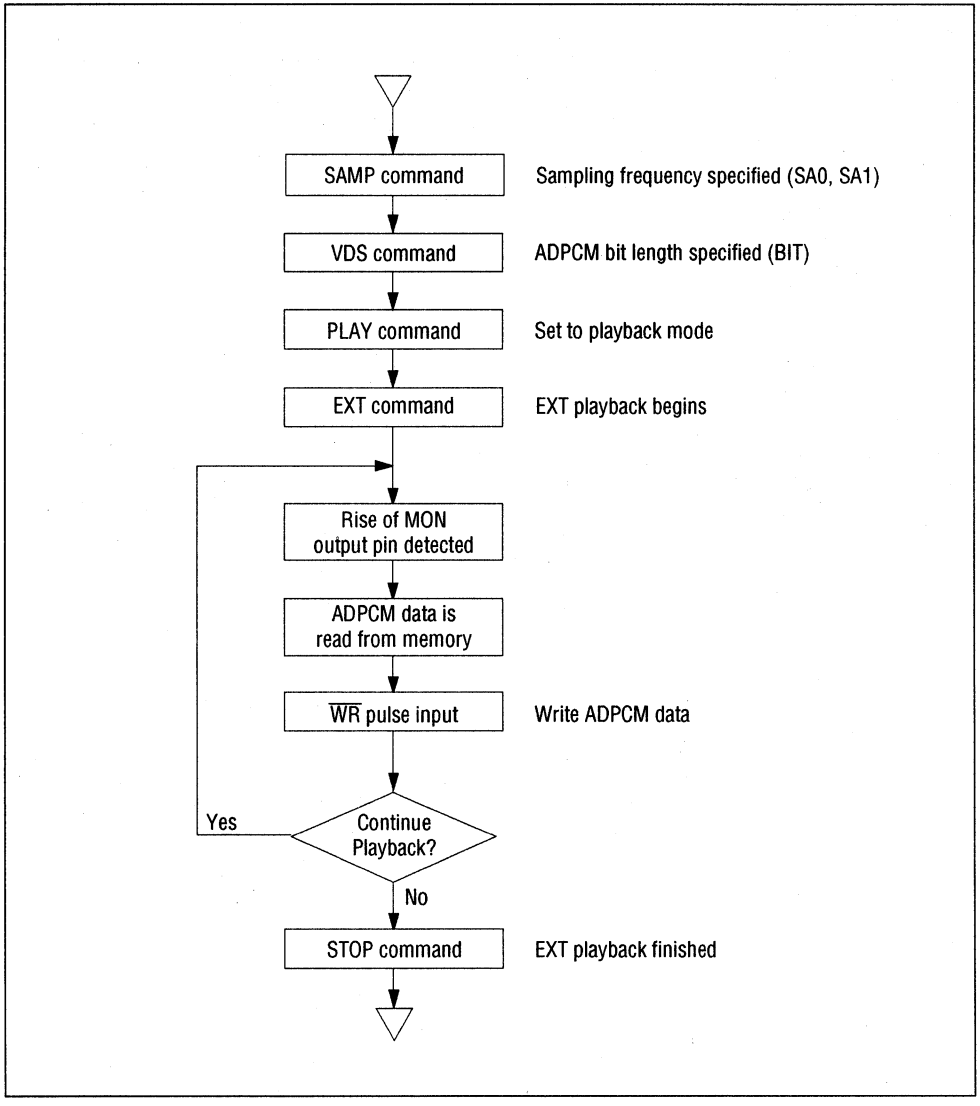
(5) When the MON pin becomes "H", fetch ADPCM data from external memory.

(6) Input a $\overline{WR}$ pulse to get ADPCM data from the data bus. In 3bit ADPCM, the upper 3bit (D3~D1 pin) are valid and data in the lower 1 bit (D0 pin) is invalid.

(7) Repeat steps (5) and (6) to continue playback.

(8) Input the STOP command to end playback.

Flowchart of playback by the EXT command



19. Reset and power down function

By input of a "L" level to the $\overline{\text{RESET}}$ pin, the LSI stops oscillation to minimize power consumption and is set to the power down state. The control circuit is simultaneously initialized. Data specified by 2 nibble commands such as the sampling frequency, ADPCM bit length, and data in the serial voice registers is not affected.

However, when a $\overline{\text{RESET}}$ pulse is input in the middle of record/playback, internal data and voice data become undefined and operation stops.

The following shows the state of the LSI at power down.

(1) Oscillation is stopped and all the operations in the internal circuit are halted, the control circuit is initialized.

(2) Power consumption is minimized. When using an external clock, input the GND level to the XT pin at power down so that no current is flowing to the oscillation circuit.

(3) The D0~D3-pin on the data bus are in the high-impedance state regardless of the $\overline{\text{RD}}$ and $\overline{\text{CE}}$ pins.

(4) Power consumption of the external serial voice registers is minimized by setting the $\overline{\text{CS1}}$~$\overline{\text{CS4}}$ pin to a "H" level output.

(5) The state of the output pins are as follows:

$\overline{\text{SAD}}$, $\overline{\text{SAS}}$, $\overline{\text{TAS}}$, $\overline{\text{CS1}}$~$\overline{\text{CS4}}$, $\overline{\text{WE}}$, $\overline{\text{RWCK}}$, STBY pins ..... "H" level output

MON pin ..... "L" level output

DI/O pin ..... High-impedance

AOUT, FOUT pins. ..... GND level output

EXAMPLE OF APPLICATION CIRCUIT

Figure 1 shows an application circuit when the MSM6588 is used in stand-alone mode and four 1Mbit serial voice registers are used.

Figure 2 shows an application circuit when the MSM6588 is used in microcontroller interface mode with two 1Mbit serial voice registers and one 2Mbit serial voice ROM.

Figure 3 shows an example of application circuit when playback is made using the EXT command for MSM6588.

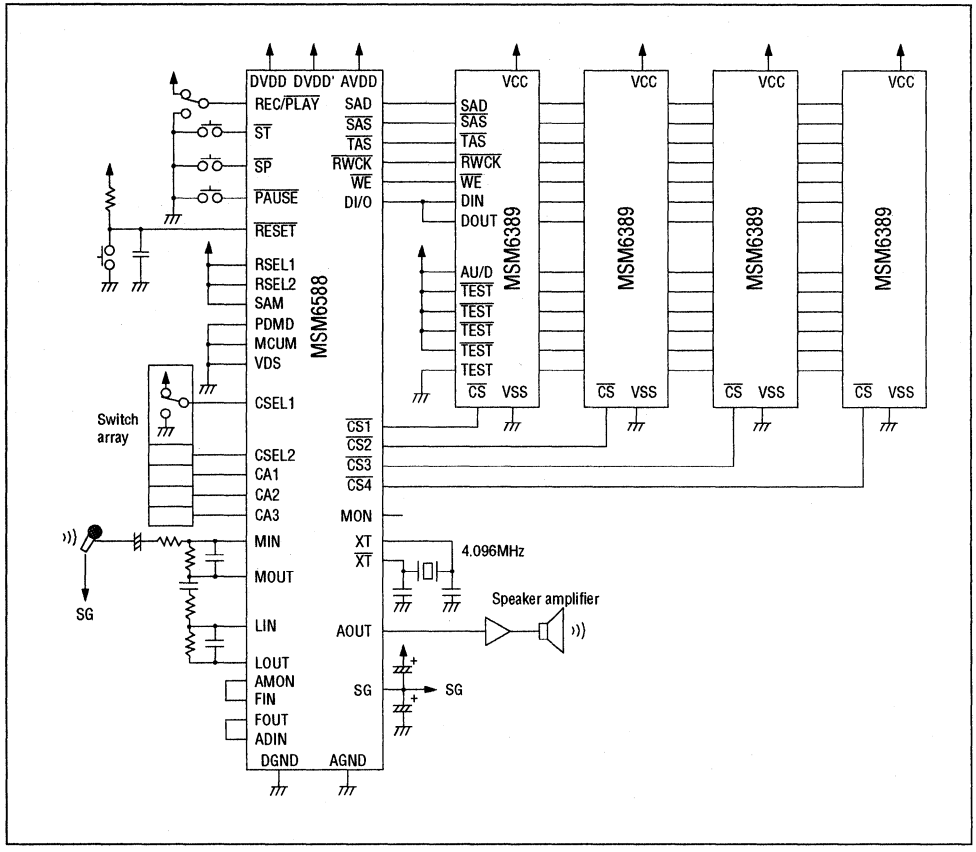
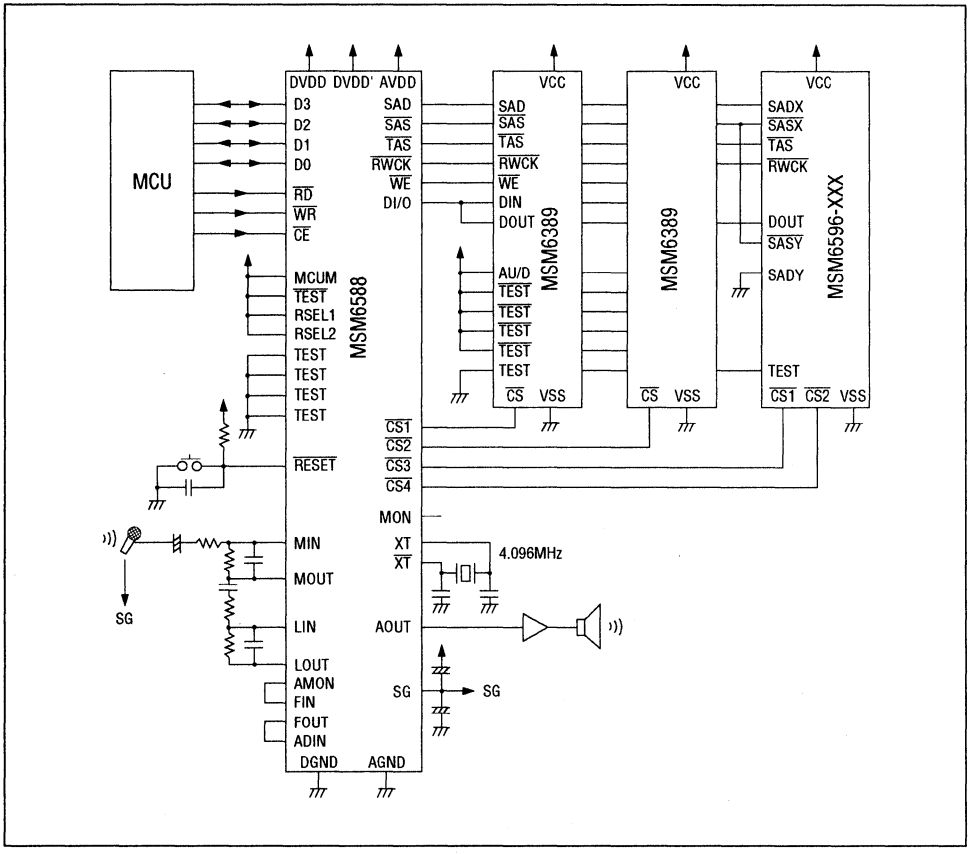


Figure 1 Example of Application Circuit in Stand-alone Mode and with 1Mbit Serial Voice Registers



Note: MSM6588 can not control the Serial voice ROM without use of Serial voice registers.

Figure 2 Example of Application Circuit in Microcontroller Interface Mode with 2Mbit Serial Voice ROM

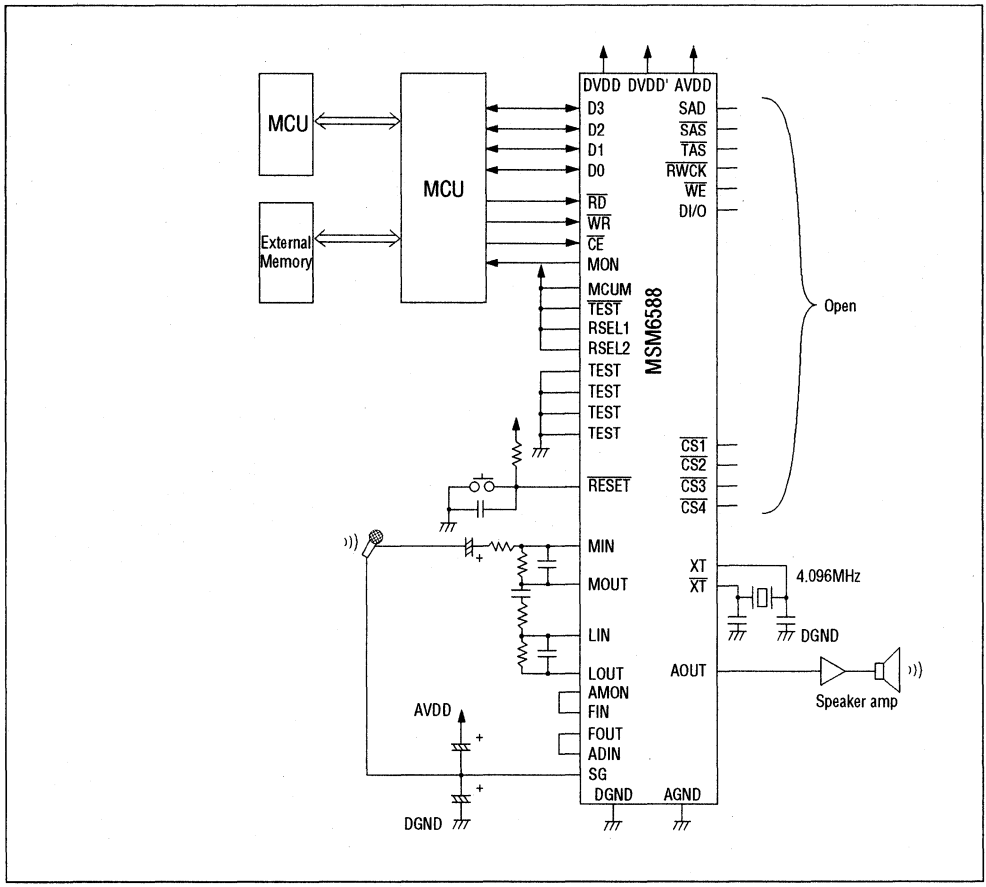


Figure 3 Application Circuit When Playback is Made Using EXT Command

OKI Semiconductor

MSM6688

ADPCM SOLID-STATE RECORDER LSI

■ GENERAL DESCRIPTION

The MSM6688 is a "solid-state-recorder" LSI developed using the ADPCM method. By externally connecting a microphone, a speaker, a speaker drive amplifier, and dedicated DRAM through the MSM6791 to store ADPCM data, it can record and play back voice data in a manner similar to a tape recorder.

The MSM6688 has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6688 can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller. In the microcontroller interface mode, the MSM6688 is much more flexible than in the stand-alone mode.

In addition, the MSM6688 can form easily a recording and playback circuit with fixed messages by connecting DRAMs (include the MSM6791) and serial voice ROMs as external memories.

CONTENTS

(1) STAND-ALONE MODE

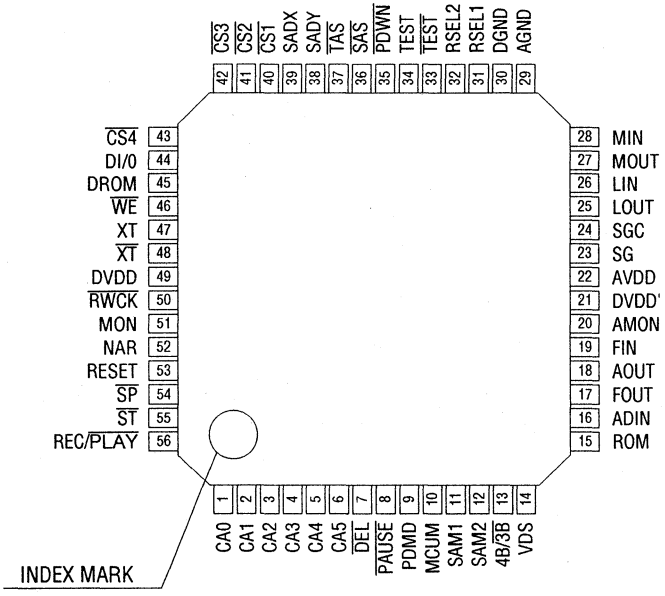
(2) MICROCONTROLLER INTERFACE MODE

(1) STAND-ALONE MODE

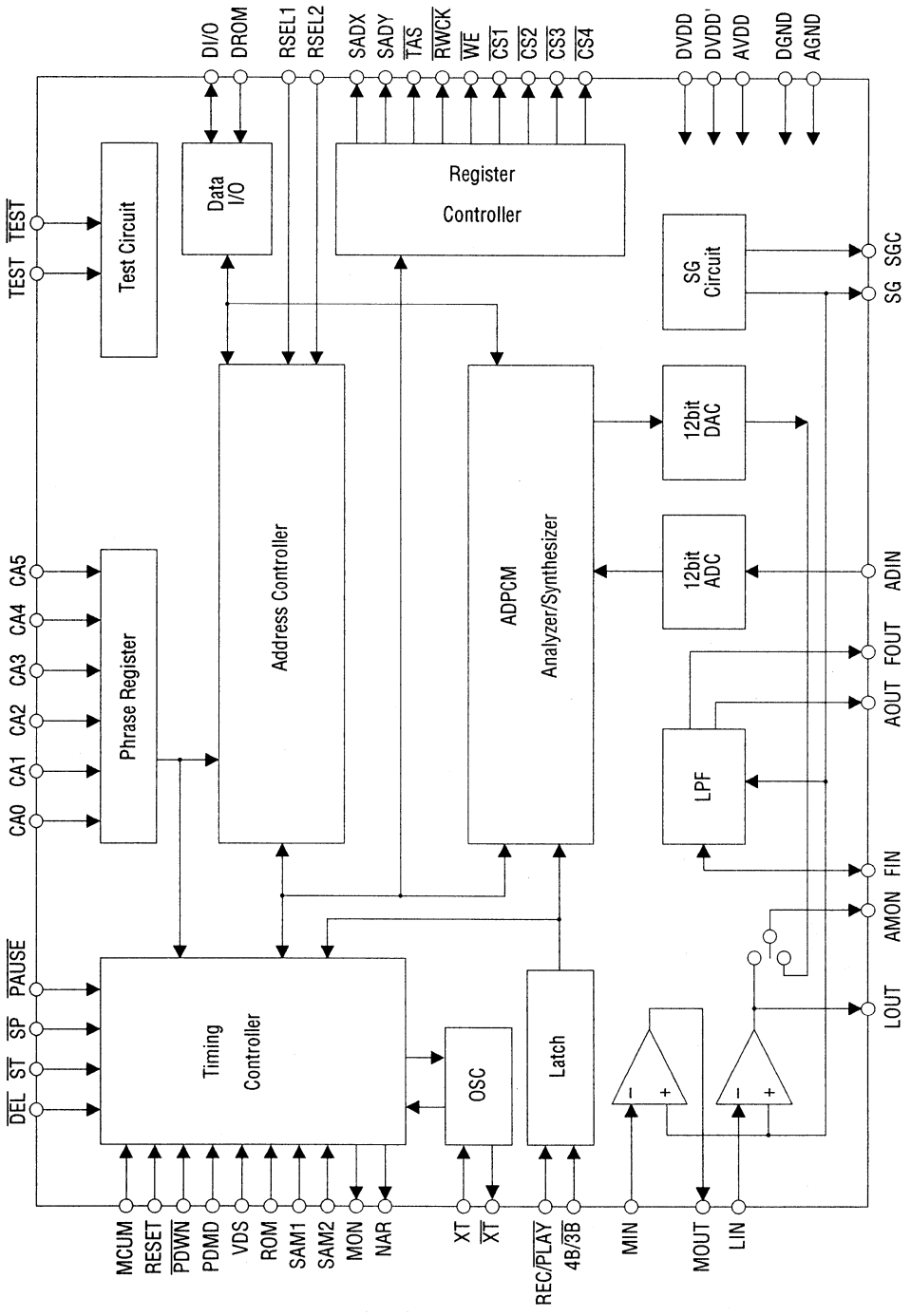
■ FEATURES

- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  DRAM, maximum 32M bits (for variable messages)
  1/4/16Mbit DRAMs (x1bit configuration) are controlled by DRAM interface LSI (MSM6791).
  Serial voice ROMs, maximum 4M bits (for fixed messages)//
  1M bit serial voice ROM (MSM6595), directly addressable
  2M bit serial voice ROM (MSM6596), directly addressable
  3M bit serial voice ROM (MSM6597), directly addressable
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32Mbit RAM is connected)
  34 minutes (for 16kbps ADPCM)
  23 minutes (for 24kbps ADPCM)
  17 minutes (for 32kbps ADPCM)
- Voice activation function
- Pause function
- Master clock frequency: 4.096 MHz
- Power supply voltage: 5 V single power supply
- Package: 56-pin plastic QFP (QFP56-P-910-V1K)

■ PIN LAYOUT (TOP VIEW)



■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3~7.0	V
Input Voltage	V_{IN}	Ta=25°C	−0.3~VDD+0.3	V
Storage temperature	T_{stg}	—	−55~+150	°C

● Operating Range

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5~5.5	V
Operating temperature	T_{op}	—	0~+70	°C
Master clock frequency	fosc	—	4.0~8.192	MHz

● DC Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
High input voltage	V_{IH}	—	0.8×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×VDD	V
High output voltage	V_{OH}	I_{OH} = −40uA	VDD−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	V_{IH} = VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH} = VDD	—	—	20	μA
Low input current (Note 3)	I_{IL1}	V_{IL} = GND	−10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL} = GND	−20	—	—	μA
Low input current (Note 4)	I_{IL3}	V_{IL} = GND	−400	—	−20	μA
Operating current consumption (1)	I_{DD}	fosc = 8 MHz, no load	—	15	30	mA
Operating current consumption (2)	I_{PD}	At power down. no load	—	—	10	μA

Note 1: Applies to all input pins excluding the XT pin.
Note 2: Applies to the XT pin.
Note 3: Applies to the all input pins without pull-up resistors, excluding the XT pin.
Note 4: Applies to the input pins ($\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, $\overline{DEL}$) with pull-up resistors, excluding the XT pin.

● Analog Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0~4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

● AC Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=4.096MHz f_{SAMP}=8.0kHz

Item			Symbol	MIN	TYP	MAX	Unit
RESET pulse width			t_{RST}	1	—	—	μs
RESET execution time	(Note 1)*		t_{REX}	—	1	—	ms
$\overline{PDWN}$ low level time	*		t_{PDL}	500	—	—	μs
$\overline{PDWN}$ high level time	*		t_{PDH}	500	—	—	μs
Oscillating time after input of $\overline{PDWN}$	*		t_{PX}	125	—	500	μs
BUSY time after release of $\overline{PDWN}$	(Note 1)*		t_{BPD}	0.25	—	—	ms
$\overline{ST}$ pulse width	**		t_{ST}	40	—	—	μs
$\overline{SP}$ pulse width	**		t_{SP}	40	—	—	μs
$\overline{PAUSE}$ pulse width	**		t_{PSE}	40	—	—	μs
$\overline{DEL}$ pulse width	*		t_{DEL}	40	—	—	μs
Time required to delete all phrases	*		t_{WBLA}	550	—	—	ms
Time required to delete a specified phrase	*		t_{WBL1}	70	—	—	ms
Time from input of $\overline{DEL}$ pulse to $\overline{CSI}$ fall	*		t_{DCS}	—	—	270	μs
Hold time of CA0~CA5, REC/$\overline{PLAY}$ after MON rise			t_{CAH}	1	—	—	ms
Address control time at the start of record/playback	*		t_{AD1}	—	1	—	ms
Time from input of $\overline{ST}$ pulse to NAR fall	*		t_{STN}	—	—	40	μs
Unvoiced time between phrases during repeated playback	*		t_{MID}	0.75	—	1	ms
POMD=H	Time from input of $\overline{ST}$ pulse to MON rise	Record *	t_{TMH1}	—	—	50	ms
		Playback *	t_{TMH2}	—	—	20	ms
		ROM playback*	t_{TMH3}	—	—	1	ms
	Time from input of $\overline{SP}$ pulse to MON fall	Record *	t_{PMH1}	—	—	80	ms
		Playback *	t_{PMH2}	—	—	2	ms
		ROM playback*	t_{PMH3}	—	—	2	ms
	Time from input of $\overline{ST}$ pulse to voice activation standby state	*	t_{STVH}	—	—	50	ms
	Time from input of $\overline{SP}$ pulse during voice activation standby state to release of voice activation standby state	*	t_{SPVH}	—	—	80	ms

Items with * are proportional to the period of master oscillator frequency fosc.
Items with ** are proportional to the period of the master oscillator frequency fosc, and are also proportional to the samplig frequency f_{SAMP} during record/playback.

Note 1: The oscillation startup stabilization time is added to t_{REX} and t_{BPD}.
The oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

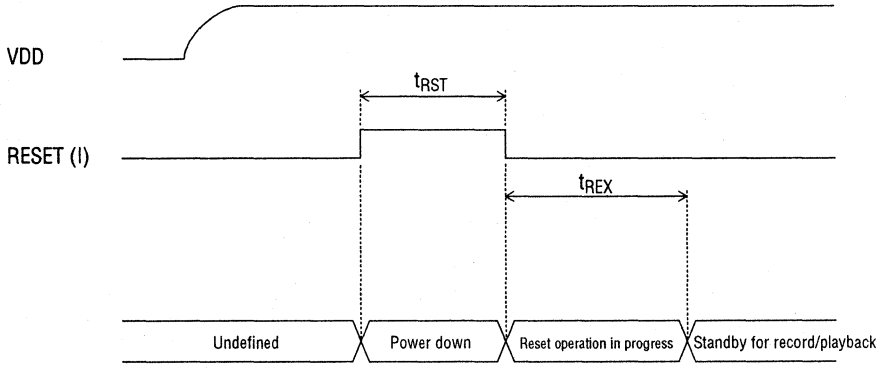
DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70℃
fosc=4.096MHz f_{SAMP}=8.0kHz

Item				Symbol	MIN	TYP	MAX	Unit
PDMD=L	Time from input of $\overline{ST}$ pulse to MON rise	Record	*	t_{TML1}	—	—	120	ms
		Playback	*	t_{TML2}	—	—	150	ms
		ROM playback	*	t_{TML3}	—	—	150	ms
	Time from input of $\overline{SP}$ pulse to MON fall	Record	*	t_{PML1}	—	—	80	ms
		Playback	*	t_{PML2}	—	—	260	ms
		ROM playback	*	t_{PML3}	—	—	260	ms
	Time from input of $\overline{ST}$ pulse to voice activation standby state		*	t_{STVL}	—	—	120	ms
	Time from input of $\overline{SP}$ pulse during voice activation standby state to release of voice activation standby state		*	t_{SPVL}	—	—	80	ms
	Standby transition time at start of playback		*	t_{AOR}	—	64	—	ms
	Standby transition time at end of playback		*	t_{AOF}	—	256	—	ms
Time from input of $\overline{PAUSE}$ pulse to pause			**	t_{PP}	—	—	1	ms
Time from input of $\overline{ST}$ pulse during pause to restart of record/playback			**	t_{PST}	—	—	1	ms

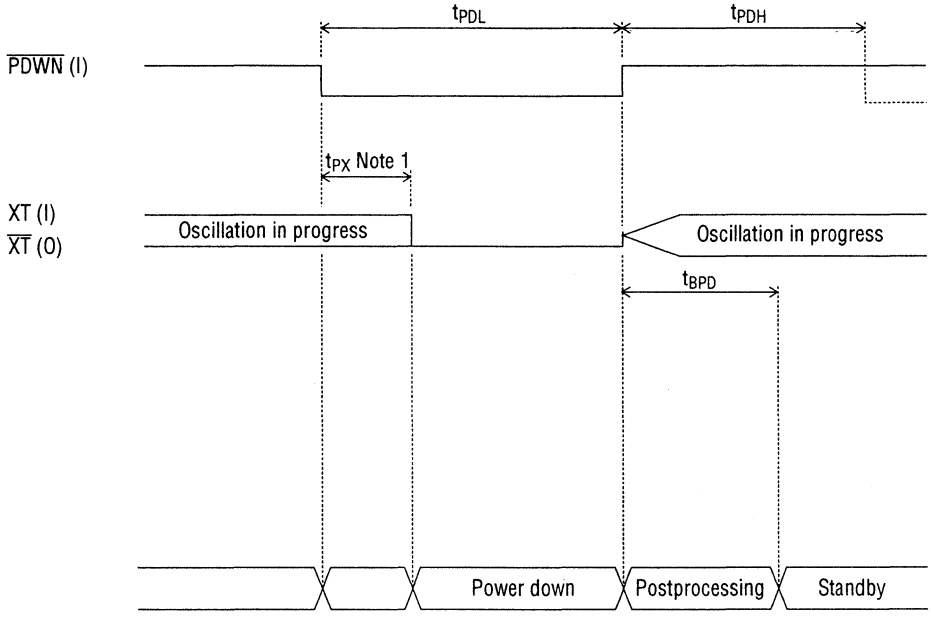
Items with * are proportional to the period of master oscillator frequency fosc.
Items with ** are proportional to the period of the master oscillator frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

■ TIMING DIAGRAMS

● RESET FUNCTION

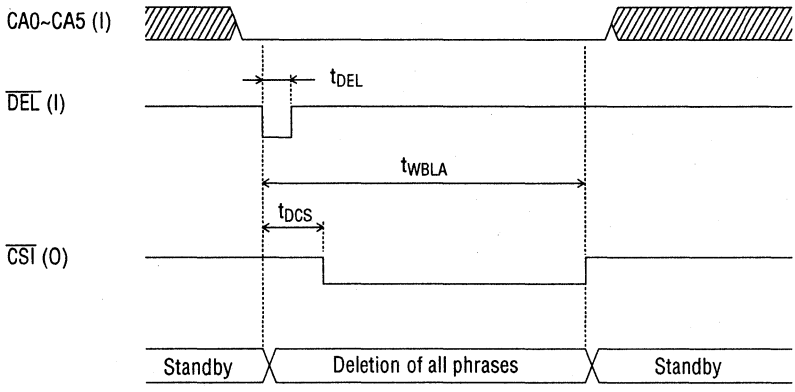


● Power Down by $\overline{\text{PDWN}}$ Pin

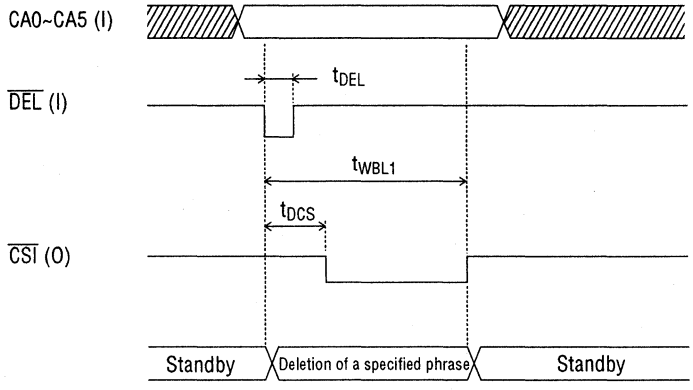


Note 1: When an external clock is used, continue to apply the clock input to the XT terminal during t_{PX} after the $\overline{\text{PDWN}}$ pin is set to a low level.

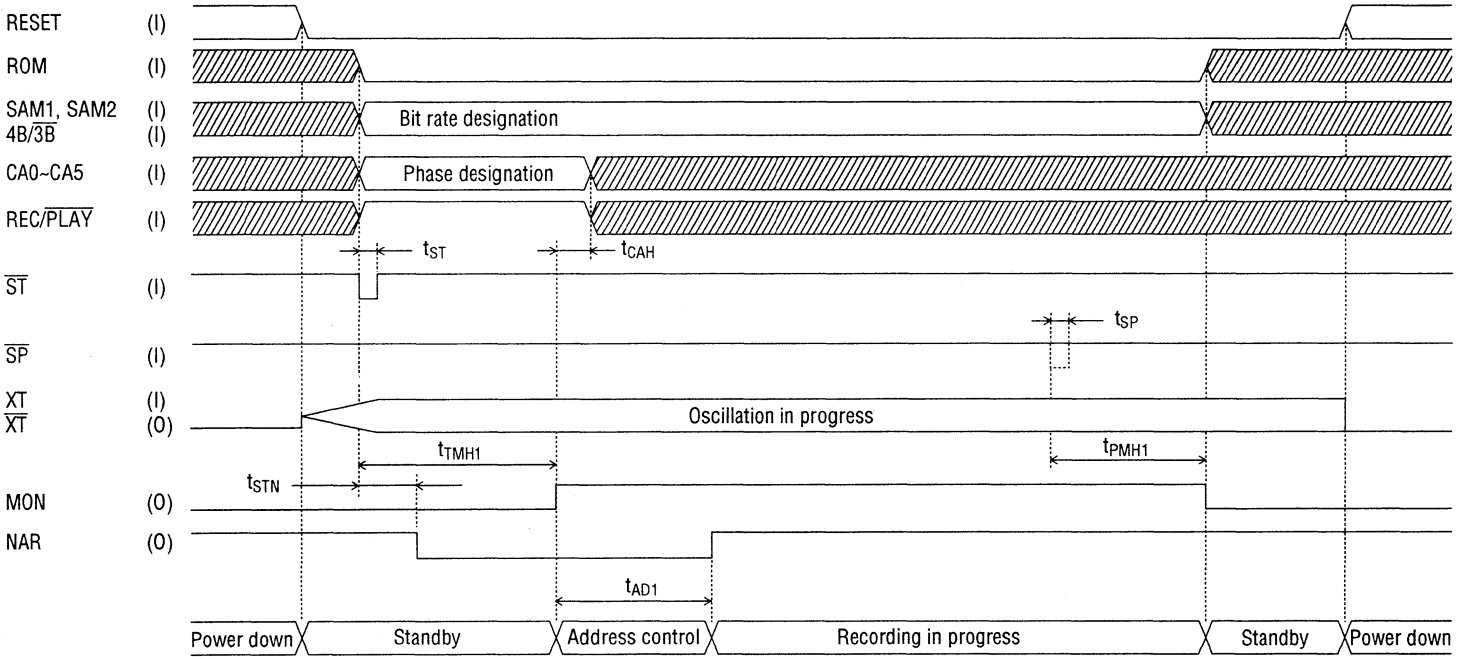
● Timing for Deletion of All Phrases



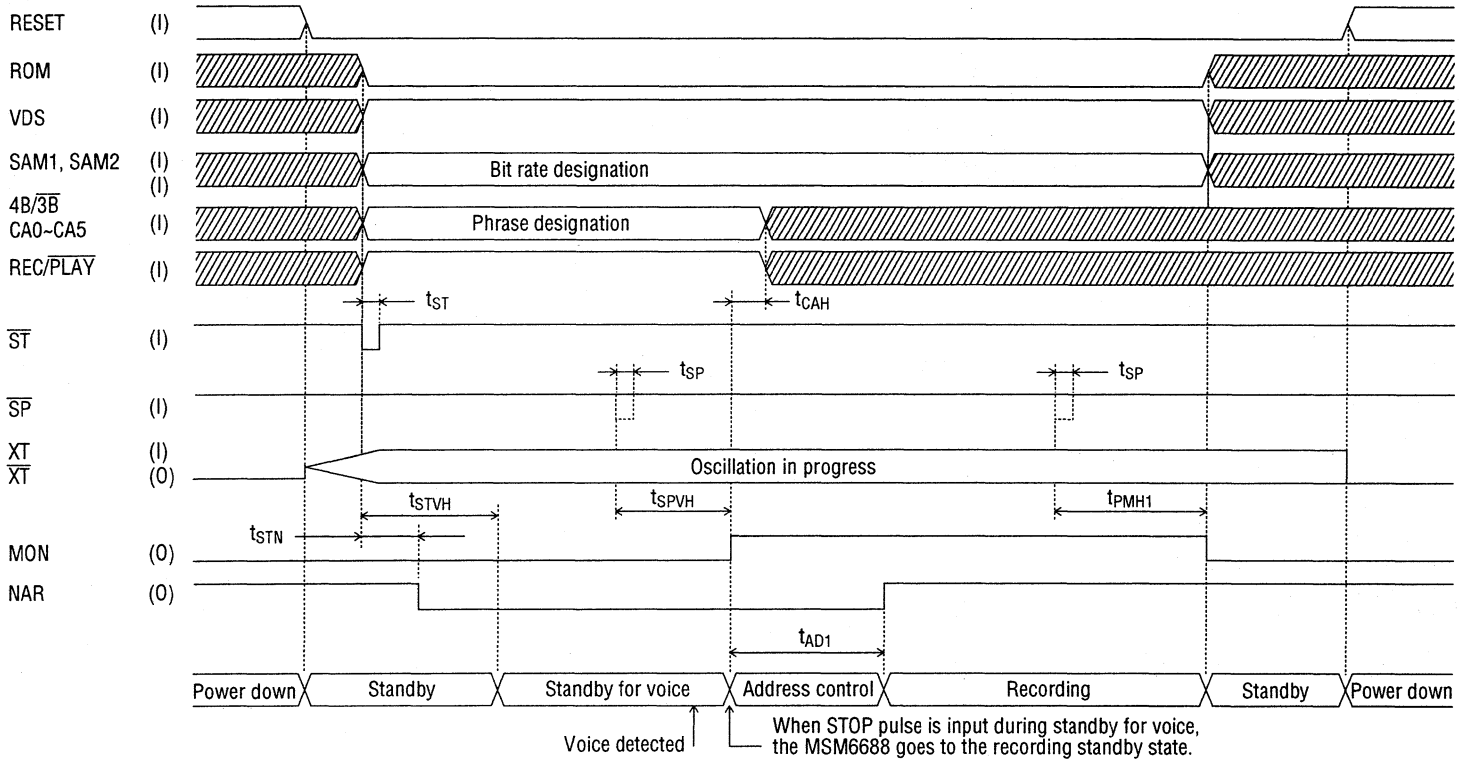
● Timing for Deletion of a Specified Phrase



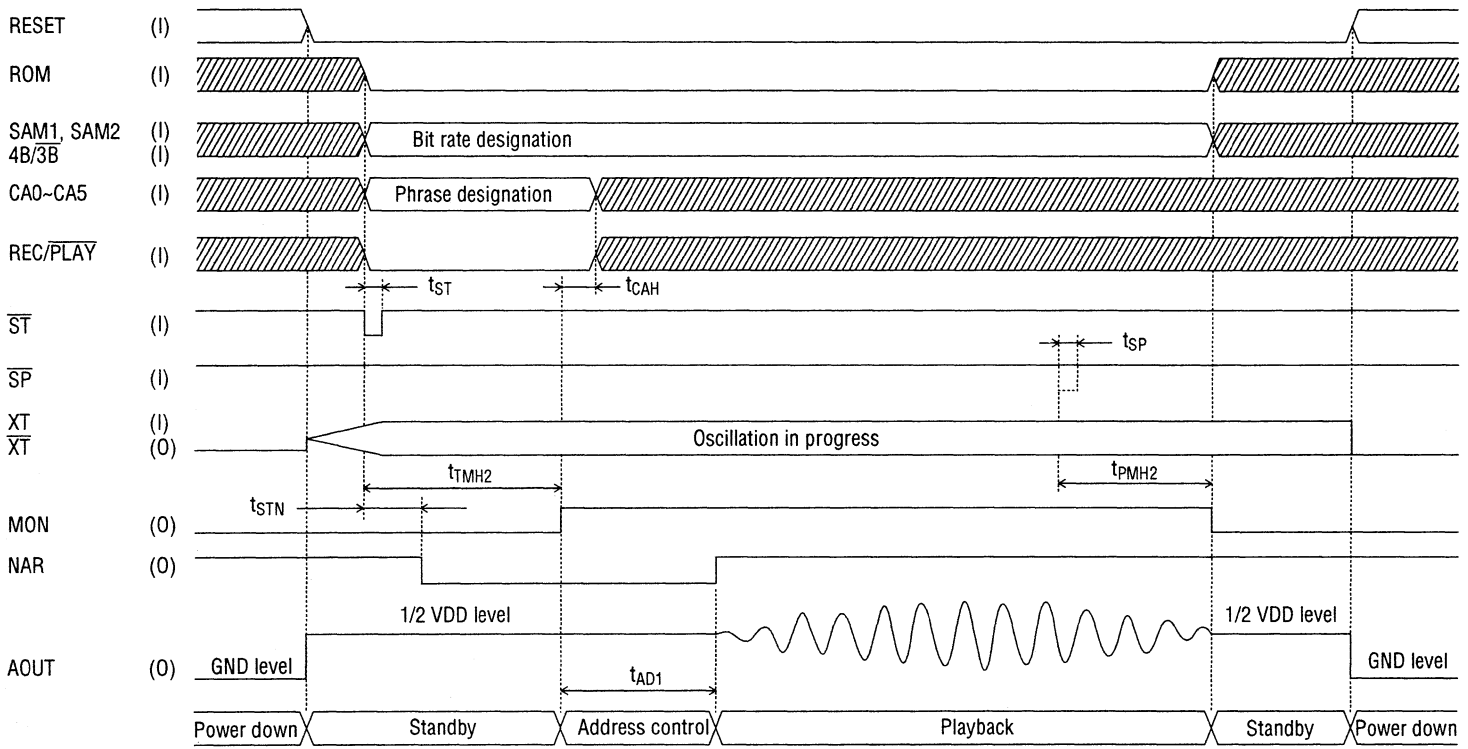
● Recording Timing (PDMD Pin = High)



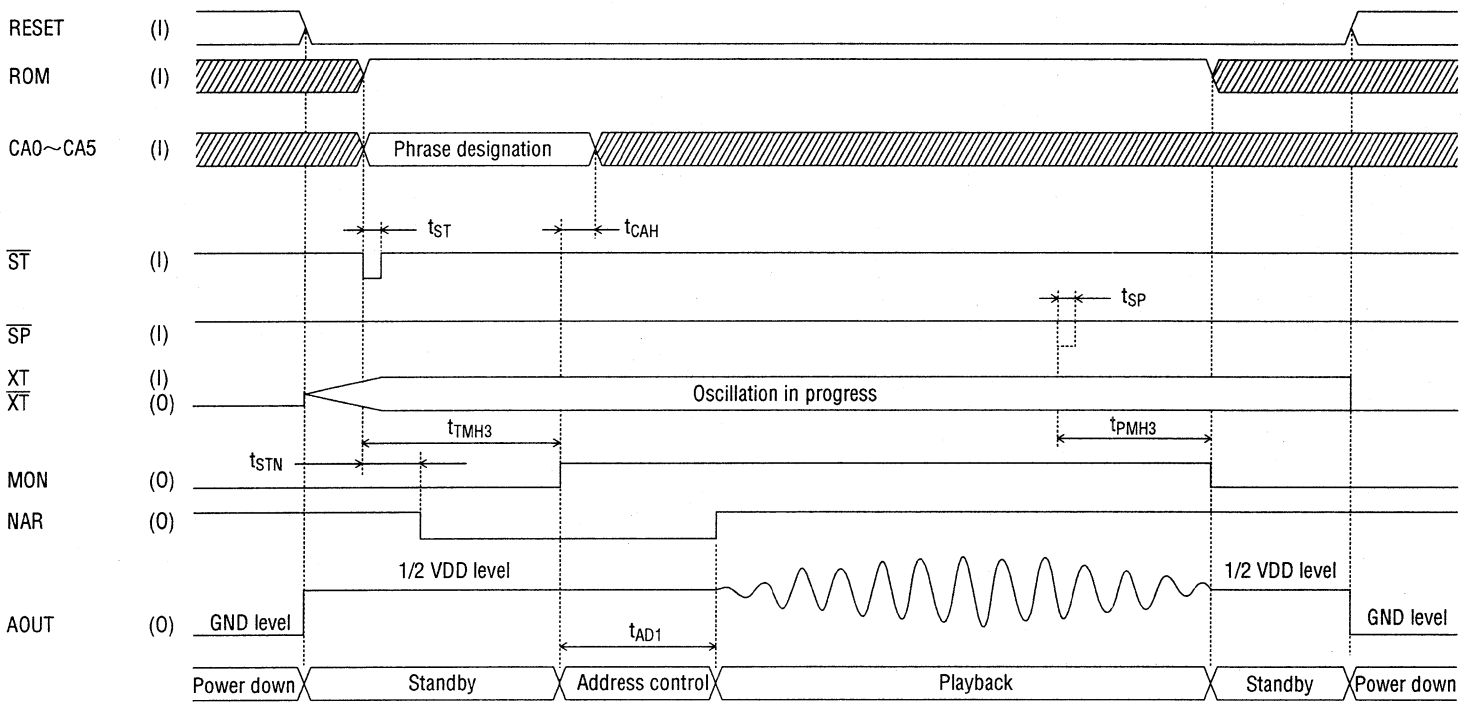
● Timing for Voice Activated Recording (PDMD Pin = High)



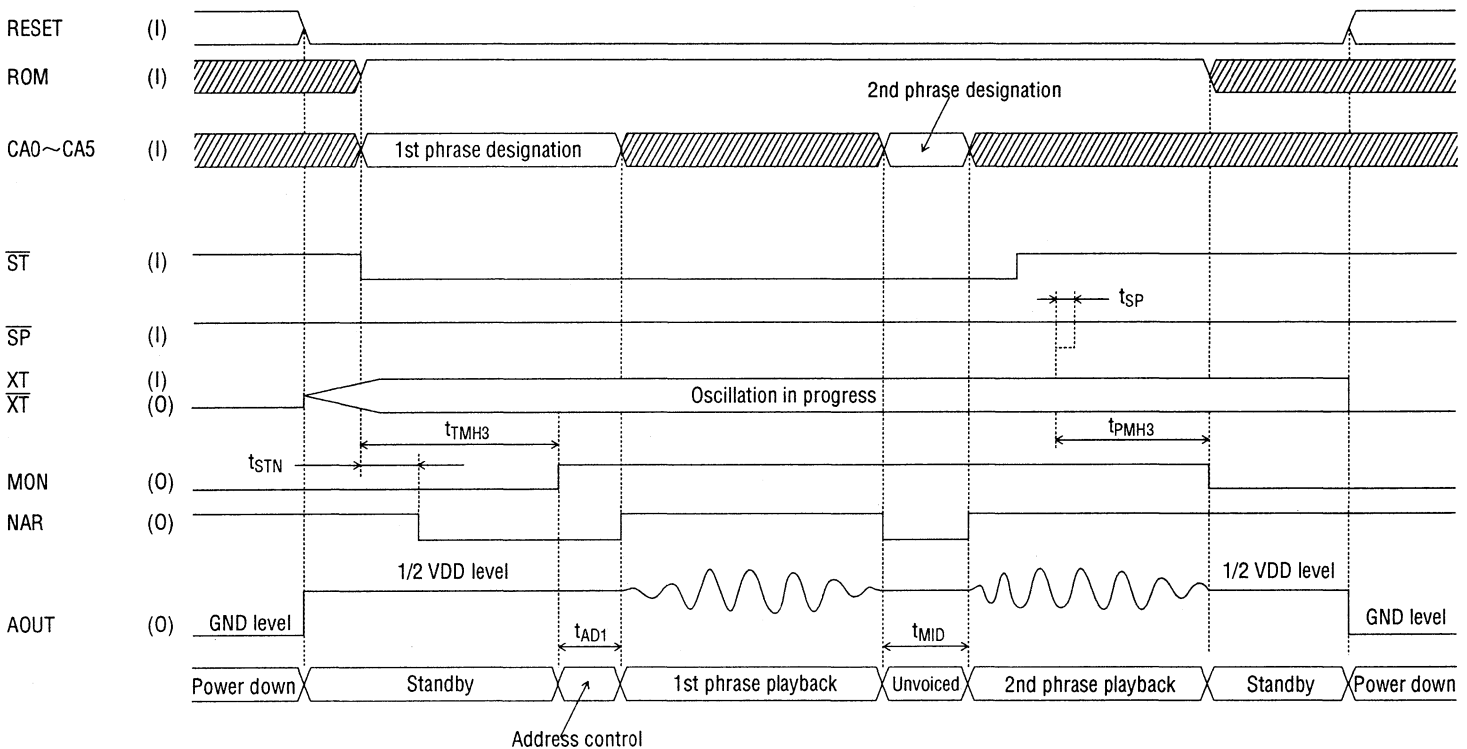
● Playback Timing (PDMD Pin = High)



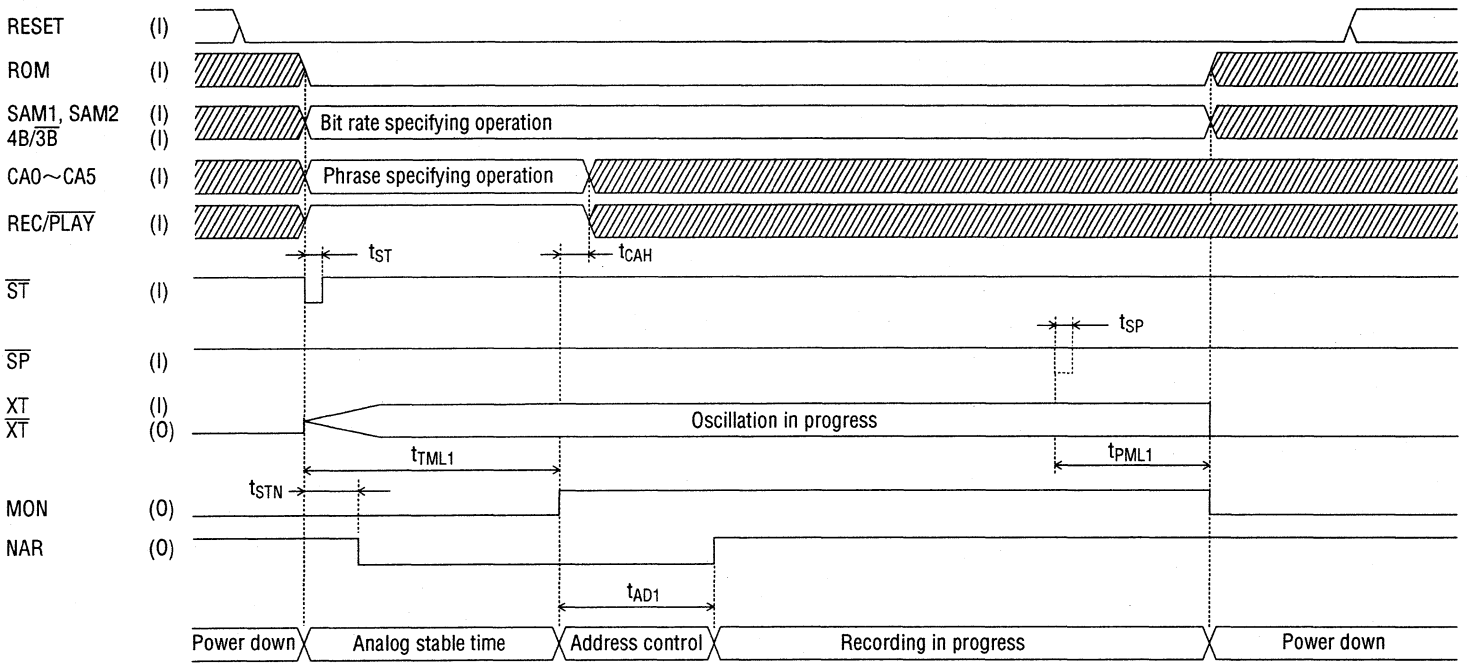
● ROM Playback Timing (PDMD Pin = High)



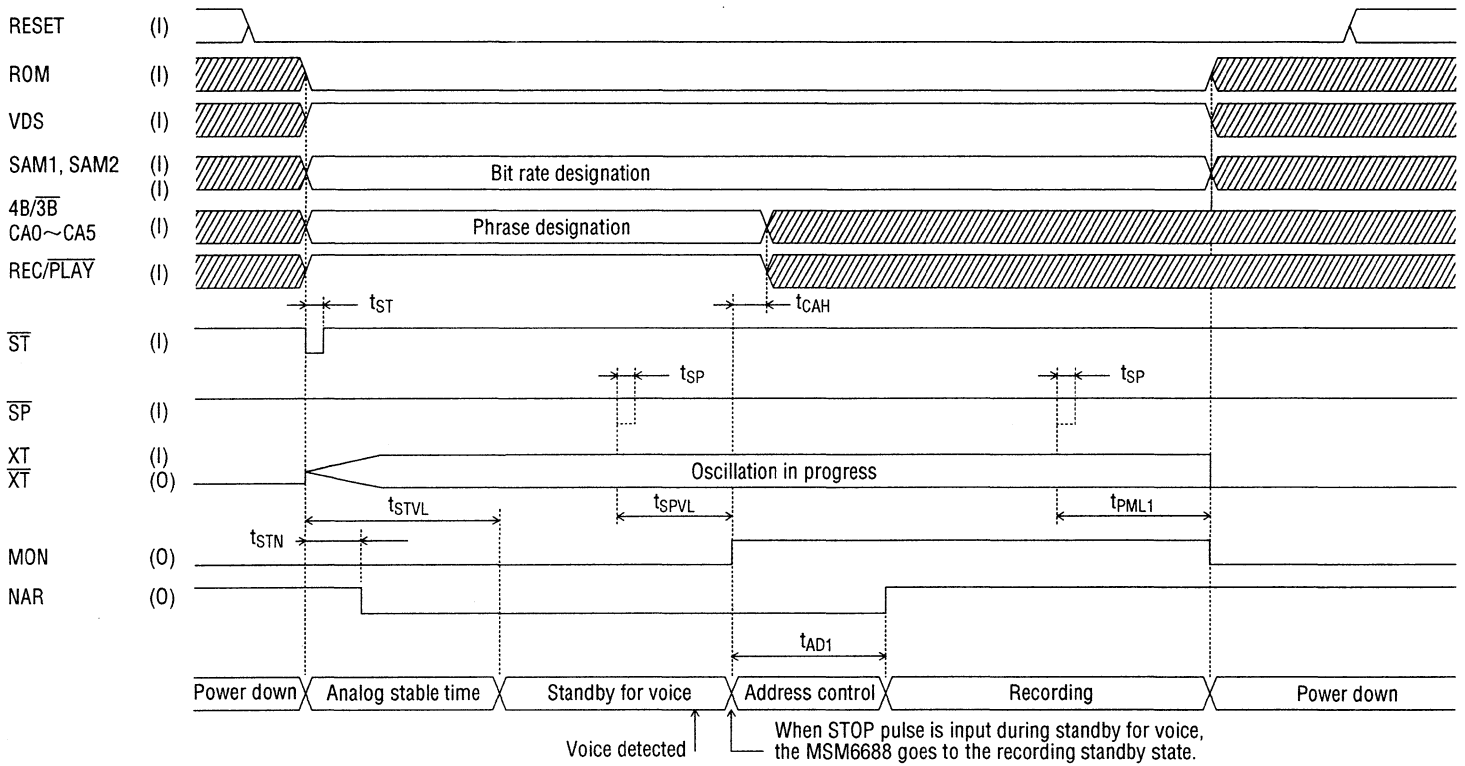
● Continuous ROM Playback Timing (PDMD Pin = High)



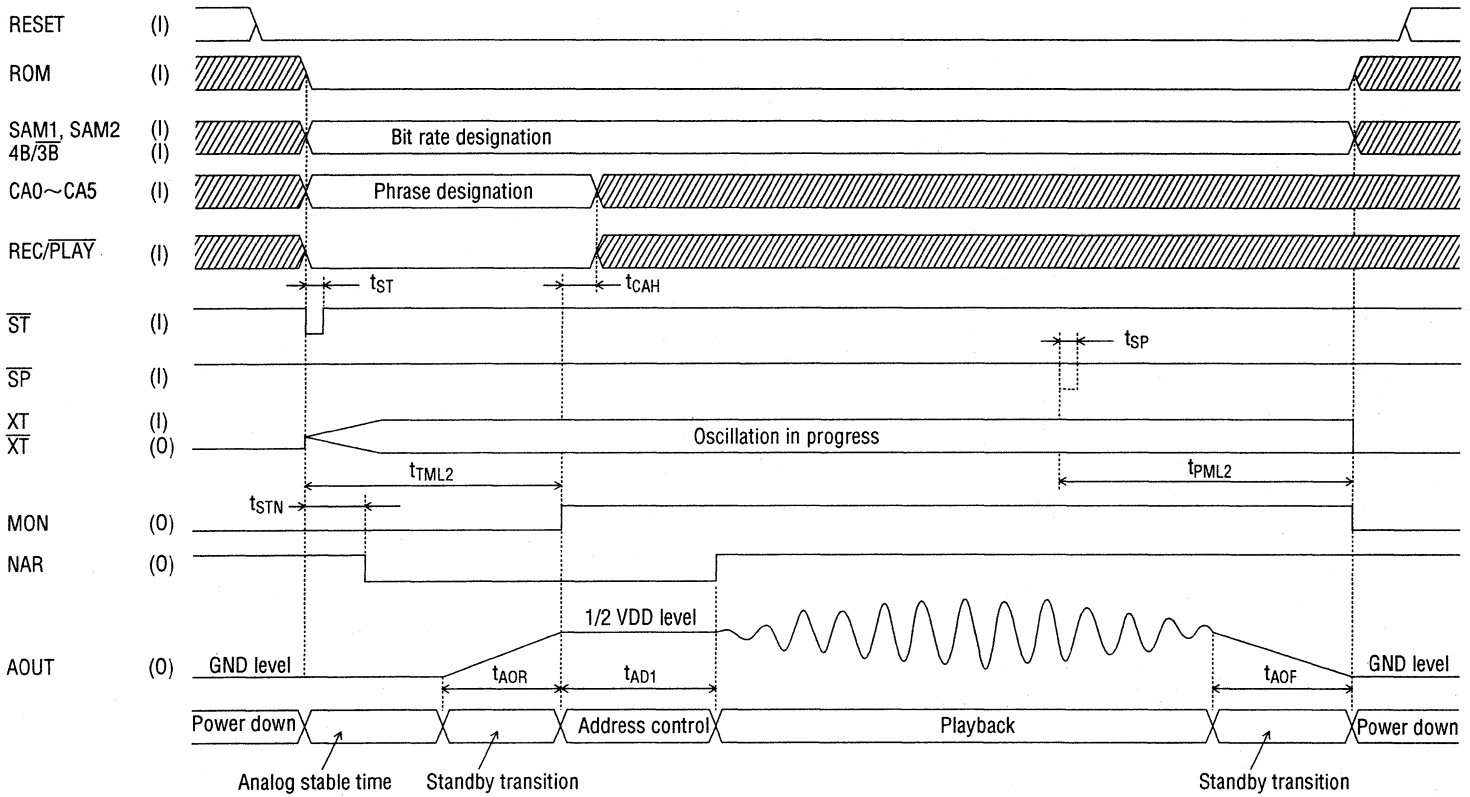
● Recording Timing (PDMD Pin = Low)



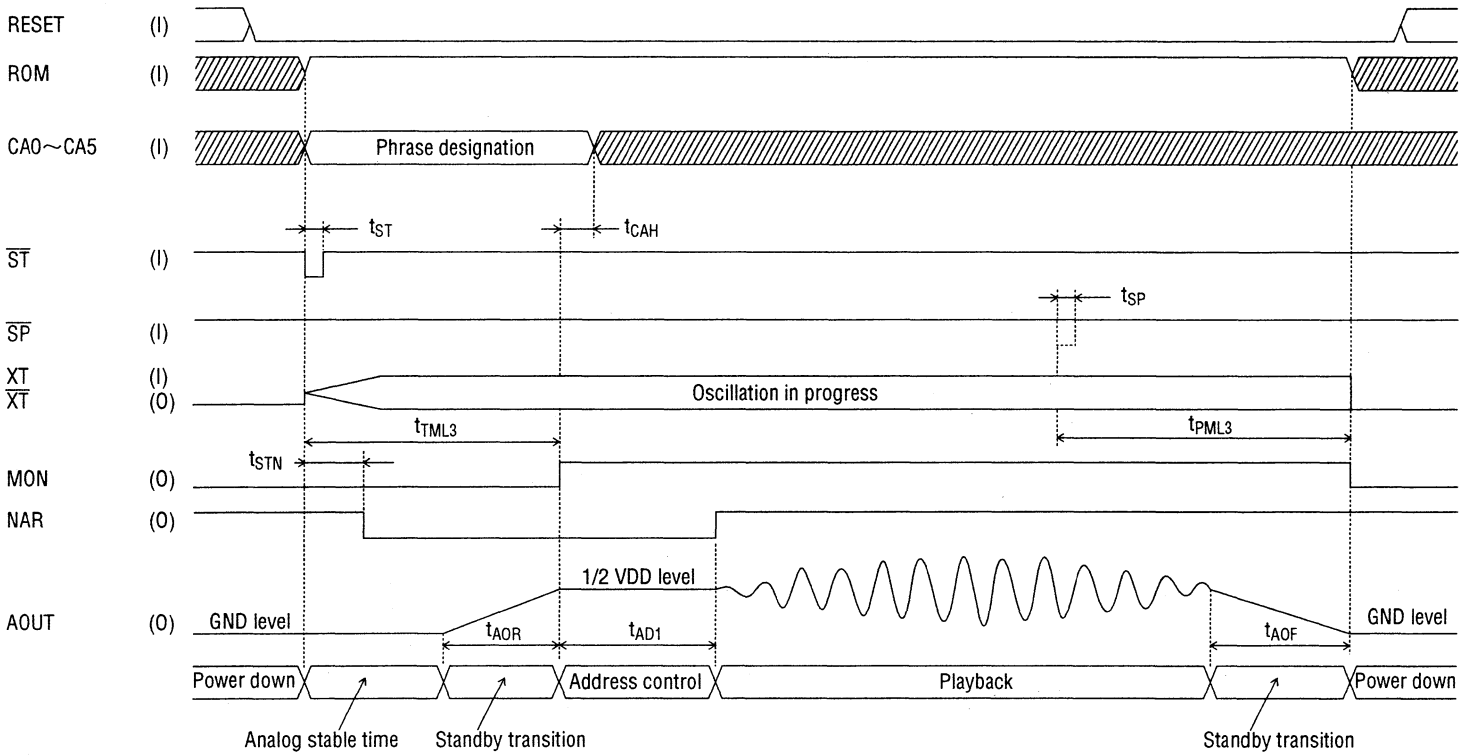
● Timing for Voice Activated Recording (PDMD Pin = Low)



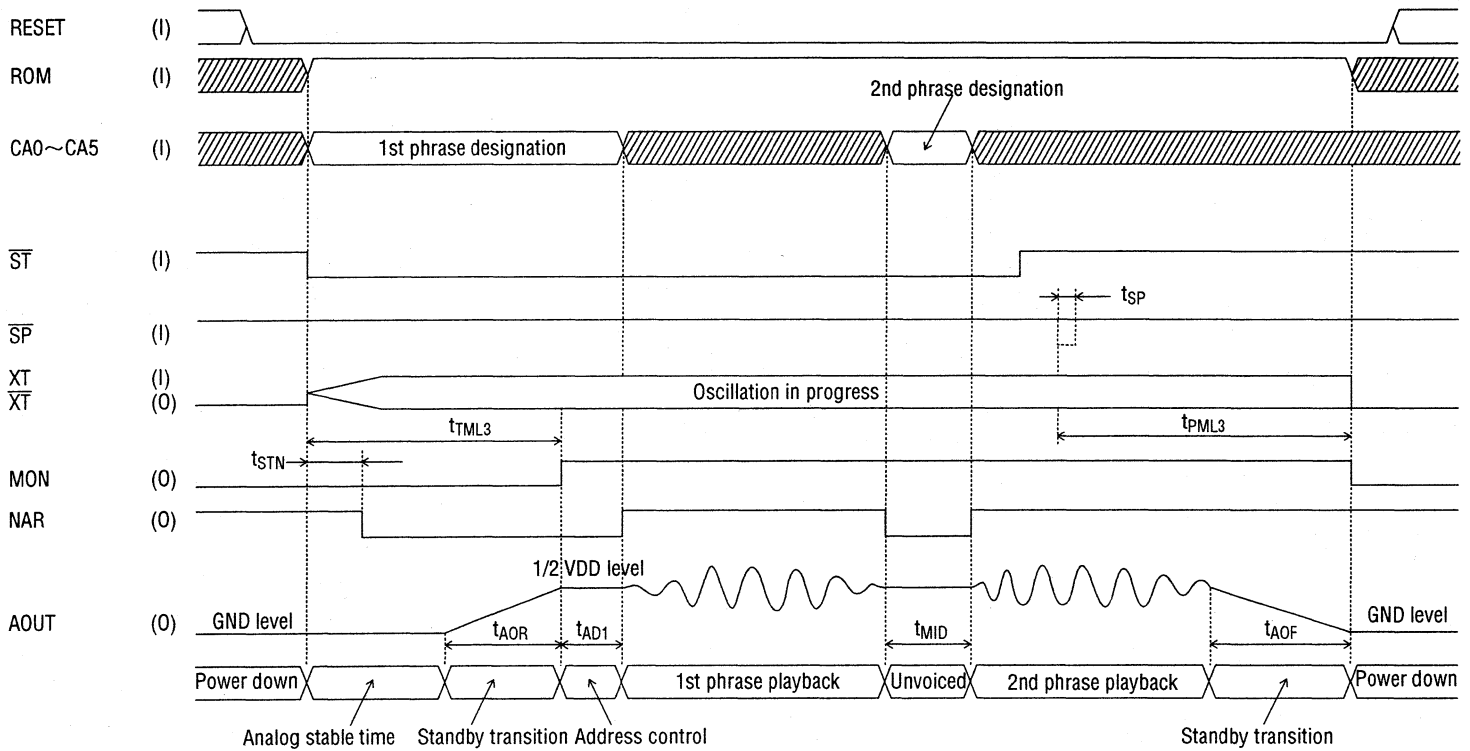
● Playback Timing (PDMD Pin = Low)



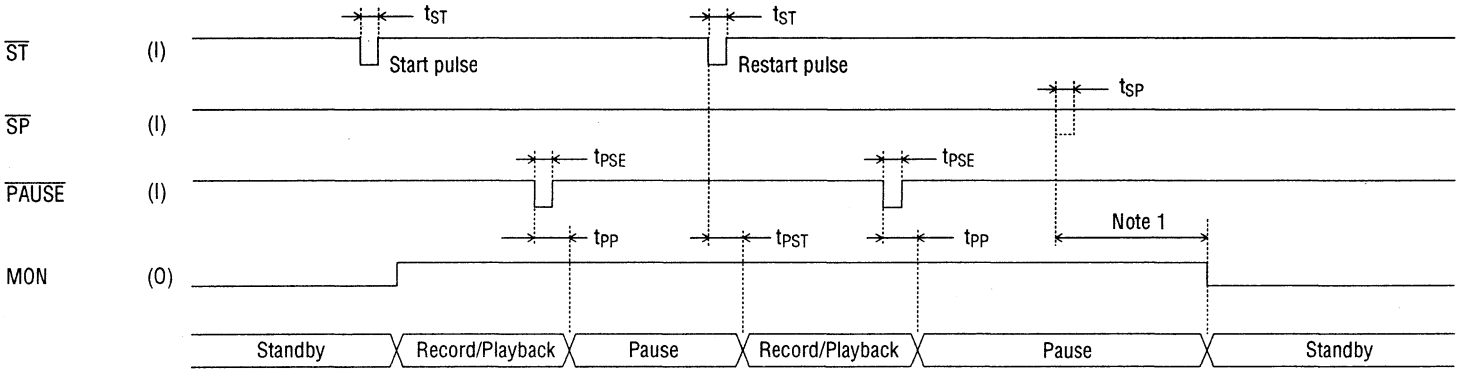
● ROM Playback Timing (PDMD Pin = Low)



● Continuous ROM Playback Timing (PDMD Pin = Low)



● Record/Playback Pause Timing



Note 1: This time interval varies depending on the state of PDMD pin and the record/playback mode and is one of t_{PMH1}, t_{PMH2}, t_{PMH3}, t_{PML1}, t_{PML2} and t_{PML3}.

■ PIN DESCRIPTION

Pin name	I/O	Pin function
DVDD	I	Digital power supply pin
DVDD'	I	Digital power supply pin
AVDD	I	Analog power supply pin
DGND	I	Digital ground pin
AGND	I	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin).
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). Used to connect the SAD pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. Outputs of starting address of read/write.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external MSM6791 (DRAM interface LSI) and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each MSM6791 (DRAM interface LSI) and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external MSM6791 (DRAM interface LSI) and the $\overline{RDCK}$ pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external MSM6791 (DRAM interface LSI).
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external MSM6791 (DRAM interface LSI). This pin outputs $\overline{WE}$ signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN pin of DRAM and MSM6791 (DRAM interface LSI). This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voic ROM.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O O O O	(Chip Select). Used to connect the $\overline{CS1}$~$\overline{CS4}$ pins of MSM6791 (DRAM interface LSI).

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>RSEL1
RSEL2</td><td>I
I</td><td>(Register Select). These are used to select the maximum controllable size of external RAM.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Total memory size</td><td>8Mbit</td><td>16Mbit</td><td>24Mbit</td><td>32Mbit</td></tr>
</table></td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode.</td></tr>
<tr><td>RESET</td><td>I</td><td>A high input level to this pin causes the MSM6688 to be initialized and to go into the power down state.</td></tr>
<tr><td>$\overline{\text{PDWN}}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688. When an Low level is applied to this $\overline{\text{PDWN}}$ pin during recording operation, the MSM6688 is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>XT</td><td>I</td><td>Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>$\overline{\text{XT}}$</td><td>O</td><td>Used to connect an oscillator, when an external clock is used, this pin must be left open.</td></tr>
<tr><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>Used to test the MSM6688. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>ROM</td><td>I</td><td>When low, selects the record/playback operation. When high, selects the ROM playback operation.</td></tr>
<tr><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Used to select the recording mode or the playback mode. This pin is invalid during the ROM playback operation. When low, selects the playback mode. When high, selects the recording mode.</td></tr>
<tr><td>$\overline{\text{ST}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>$\overline{\text{SP}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>$\overline{\text{DEL}}$</td><td>I</td><td>When a low level pulse is applied to this pin, all phase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phase deletion
ch01~ch3F: Specified phrase deletion
After powering up, be sure to input RESET signal and then to delete all phrases. After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>CA0~CA5</td><td>I</td><td>Input pins used to specify desired phases.
A total of 63 phrases can be specified independently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phrase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="5">A total of 63 phrases can be used both for record/playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
<tr><td>4B/$\overline{\text{3B}}$</td><td>I</td><td>Input pin used to select one of two types of ADPCM bit length.
When low, selects the 3-bit ADPCM.
When high, selects the 4-bit ADPCM.</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>SAM1
SAM2</td><td>I</td><td>Used to select one of the following four types of sampling frequency. The relationship between the master oscillator frequency (fosc) and thesampling frequency (fsamp) is shown below. Values in parentheses denote the sampling frequencies for fosc = 4.096 MHz.
<table>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>fsam</td><td>$\frac{fosc}{1024}$ (4.0kHz)</td><td>$\frac{fosc}{768}$ (5.3kHz)</td><td>$\frac{fosc}{640}$ (6.4kHz)</td><td>$\frac{fosc}{512}$ (8.0kHz)</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This input pin is used to select the condition for transition to the power-down state.
Low level: The MSM6688 automatically goes to the power-down state, excepting the time the record/playback operation is being performed.
High level: The MSM6688 automatically goes to the standby state, instead of the power-down state, excepting the time the record/playback operation is being performed. In this case, the MSM6688 can be placed in the power-down state by setting the RESET pin to a high level. If it is desired to use the built-in LPF for an external circuit, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>VDS</td><td>I</td><td>Used to select the voice activated recording that starts recording when the voice input exceeds the preset amplitude. A high input level on this pin enables the voice activated recording circuit.</td></tr>
<tr><td>MON</td><td>O</td><td>Outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>NAR</td><td>O</td><td>Output pin to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after verifying that the NAR pin becomes high.</td></tr>
</table>

■ FUNCTIONAL DESCRIPTION

● Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external serial registers, sampling frequency, and ADPCM bit length, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K bits)}}{\text{sampling frequency (kHz)} \times \text{bit length (bits)}} \quad \text{(seconds)}$$

For example, if the sampling frequency is $\frac{4096}{768}$ kHz (= 5.333 kHz), ADPCM bit length is 3 bits, and four 8M bit serial registers are used, the recording time can be obtained as follows.

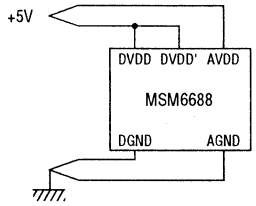
$$\text{Recording time} = \frac{1.024 \times (8192 \times 4 - 64)}{5.333 \times 3} = 2093 \text{ seconds}$$

$$= 34 \text{ minutes } 53 \text{ seconds}$$

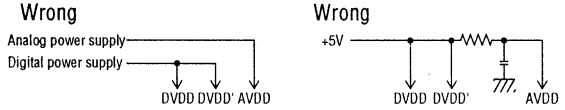
In the above equation, the memory capacity is obtained by subtracting the memory capacity (64 kbits) for the channel index area from the total memory capacity.

● Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6688 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.



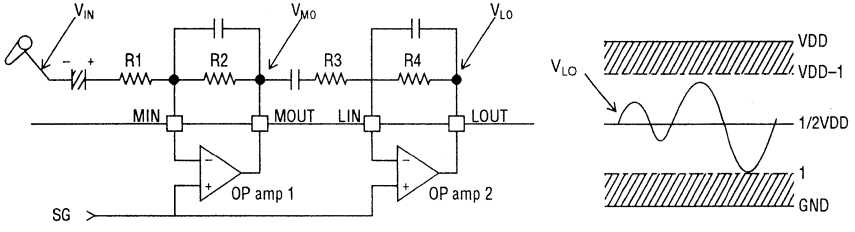
Do not supply the power to the logic portion and the analog portion from the separate power sources. Otherwise, a problem such as latch-up may occur.



● Analog Input Amplifier Circuit

This MSM6688 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \cdot R4}{R1 \cdot R3} \quad V_{IN}(V)$$

During the time the recording operation is performed, the output V_{LO} of OP amp 2 is connected to the input FIN of the built-in LPF. The FIN allowable input voltage (V_{FIN}) ranges from 1V to (V_{DD} – 1)V. Therefore, the amplification ratio must be adjusted so that the V_{LO} amplitude can be within the FIN allowable input voltage range.

For example, if V_{DD} = 5V, V_{LO} becomes 3 V_{p-p} max. If V_{LO} exceeds the FIN allowable input voltage range, the output of the LPF will be a clipped waveform.

The load resistance R_{OUTA} of the OP amp is 200 kΩ minimum, so that the feedback resisters R2 and R4 of the inverting amplifier circuit must be 200 kΩ or more.

● Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6688, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

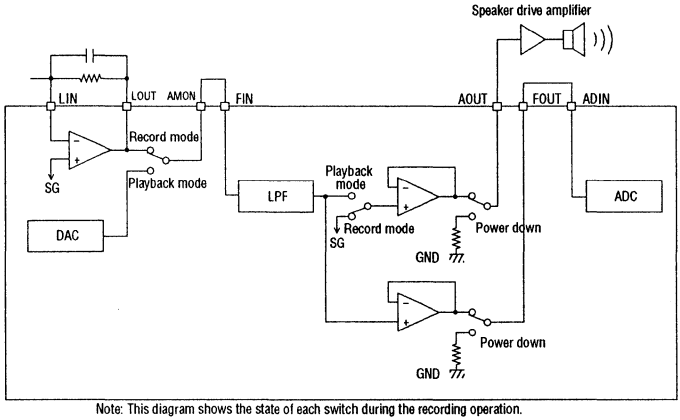
When PDMD pin = high level:

Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)

When PDMD pin = L:

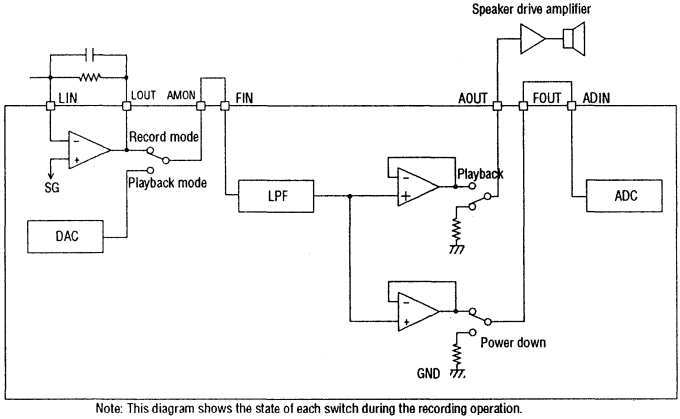
Analog pin	At power down	During operation	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	GND level	LPF output (playback waveform)

When PDMD pin = H:



Note: This diagram shows the state of each switch during the recording operation.

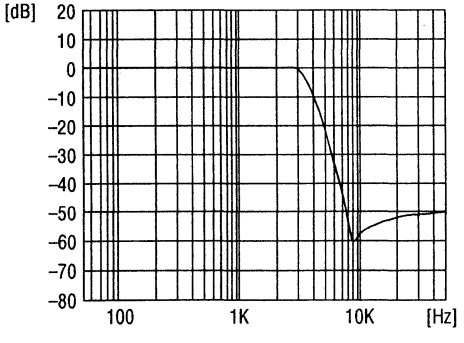
When PDMD = L:



Note: This diagram shows the state of each switch during the recording operation.

● LPF Characteristics

This LSI contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.



LPF Frequency Characteristics (fsamp = 8.0 kHz)

● Reset Function

By applying a high level to the RESET pin, the MSM6688 stops frequency oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

If a high level is applied to the RESET pin during record/playback operation , the MSM6688 is set to the power-down state and initialized state, so that voice data becomes undefined.

The following shows the power-down state of the MSM6688.

(1). Frequency oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) $\overline{CS1}$ – $\overline{CS4}$ pins are set to a high level to minimize the current consumption of external serial registers and serial voice ROMs.

(4) Pull-up resistors are removed from the input control $\overline{ST}$, $\overline{SP}$, $\overline{PAUSE}$, and $\overline{DEL}$ pins.

(5) The state of the output pins are as follows.

$\overline{SADX}$, $\overline{SAS}$, $\overline{TAS}$, $\overline{CS1}$ – $\overline{CS4}$,
$\overline{WE}$, $\overline{RWCK}$, and NAR pins: .....High level
SADY, MON pin: .....Low level
AOUT and FOUT pins: .....Ground level

After powering up the MSM6688, be sure to initialize it by applying a high level to the RESET pin.

● Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6688 may be set to the power-down state, in which the oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external serial registers. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6688 is powered-down ($\overline{\text{PDWN}}$ = L) during the record/plaback operation: The record/plaback operation is stopped. After the release of the power-down state, the postprocessing will be performed.

(2) When the MSM6688 is prowered-down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporalily stopped and will be restarted after the release of the power-down state.

(3) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level is in progress: This transition operation is temporalily stopped and will be continued after the release of the power-down state.

● Record/Playback Control Mode

Either record/playback mode or ROM playback mode can be selected through the ROM pin as described below.

ROM pin	Record/playback control mode
L	Record/plaback
H	ROM playback

1. Record/playback

The recorded voice data is stored in serial registers. The recording area is indirectly allocated to each phrase by setting the phase specifying pins CA0 to CA5 (63 phrases). The recording area for each phrase is managed by the MSM6688 as described below.

The total memory capacity of the connected external serial registers is equally divided into 256 memory blocks. When recording is performed, voice data is written into the memory blocks unused by other phrases. When a specified phase is deleted, the blocks used by this phrase become unused blocks.

When re-recording is performed, voice data is written in the memory area consisting of the memory blocks used by this phrase and the unused memory blocks.

The memory capacity of one memory block and the number of initially available memory blocks (recording time) vary according to the total memory capacity of the connected serial registers.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity		8M bits	16M bits	24M bits	32M bits
Memory capacity of one block		32K bits	64K bits	128K bits	128K bits
Recording time of one block	16kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	24kbps	1.4 seconds	2.7 seconds	5.5 seconds	5.5 seconds
	32kbps	1.0 second	2.0 seconds	4.1 seconds	4.1 seconds
Number of initially available blocks		254	255	191	255

2. ROM playback

For playback of the voice data stored in the connected serial voice ROM, the playback area is allocated indirectly to each fixed message phrase by setting phrase specifying pins CA0 to CA5 (63 phases).

The start address, stop address, sampling frequency, and ADPCM bit length which specify the playback area for each phase are written in the index area of the serial voice ROM. When the playback operation is started, the MSM6688 fetches these data from the index area.

● Deleting phrases

1. Deleting all phrases

All 63 phresses ch01 through ch3F can be deleted by specifying ch00 and applying a low pulse to the $\overline{DEL}$ pin. When all phrases are deleted, all phrases ch01– ch3F (63 phrases) go to the unrecorded status and, at the same time, the initial data for address control is written in the serial registers. Therefore, whenever the MSM6688 is powered up, delete all phrases after applying a high level to the RESET pin.

2. Deleting a specified phrase

By specifying one of ch01 - ch3F phrase and applying a low level to the $\overline{DEL}$ pin, the specified phrase can be deleted and put to the unrecorded state. The blocks for the deleted phrases are added to available unused blocks (available recording time).

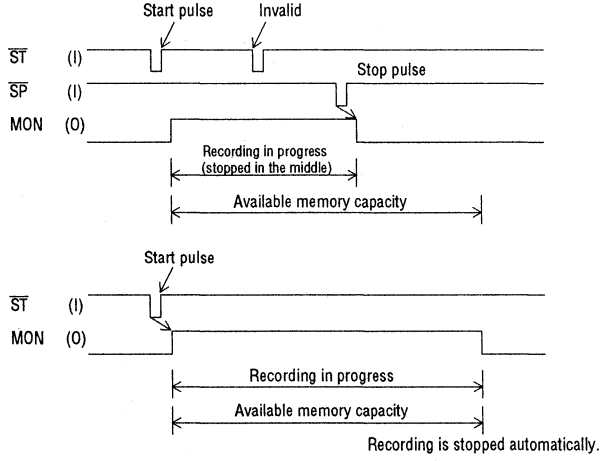
● Recording Method

Whenever the MSM6688 is powered up, be sure to delete all phrases after applying a high level to the RESET pin. Then, start the recording operation.

(1) Set recording conditions at the relevant pins.

ROM pin:	Low level
REC/$\overline{\text{PLAY}}$ pin:	High level
VOS pin:	Selection of voice activation recording (high level enables voice activation and low level disables voice activation.)
SAM1 and SAM2 pins:	Select the smpling frequency.
4B /$\overline{\text{3B}}$ pin:	Select the ADPCM bit length.
CA0 – CA5 pins:	Specify one of 63 phrases ch01 – ch3F.

(2) To start recording, apply a low pulse to the $\overline{\text{ST}}$ pin.
To stop recording in progress, apply a low pulse to the $\overline{\text{SP}}$ pin. When recording continues to the end of the memory capacity, recording is automatically stopped. In case of re-recording, voice data will be written in the memory block used by the specified phrase and unused memory blocks. Therefore, the voice data is overwritten on the previously recorded contents. The MON pin outputs a high level during recording.



● Playback Method

(1) Set playback conditions at the relevant pins.

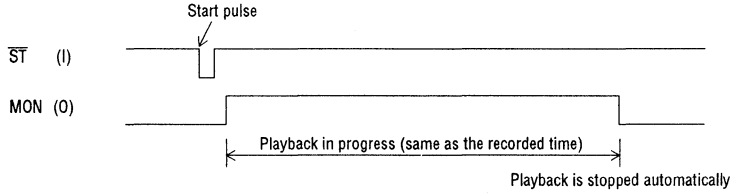
ROM pin:	Low level
REC/$\overline{\text{PLAY}}$ pin:	Low level
SAM1 and SAM2 pins:	Select the sampling frequency.
4B/$\overline{\text{3B}}$ pin:	Specify the ADPCM bit length selected for recording.
CA0–CA5 pins:	Specify one of 63 phases ch01–ch3F.

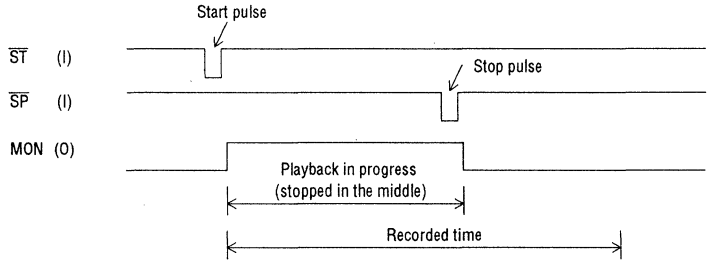
(2) To start playback, apply a low pulse to the $\overline{\text{ST}}$ pin.

When playback for the duration of the recorded data is finished, the playback is stopped automatically.

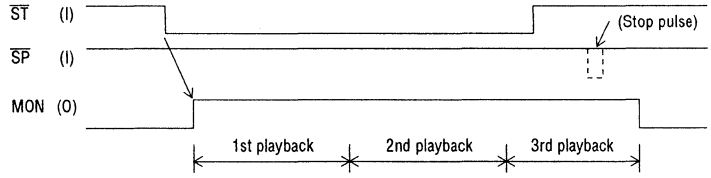
To stop playback in progress, apply a low pulse to the $\overline{\text{SP}}$ pin.

The MON pin outputs a high level during playback.





By maintaining the $\overline{\text{ST}}$ pin at a low level, repeated playback is possible.



● ROM Playback Method

(1) Apply a high level to the ROM pin.

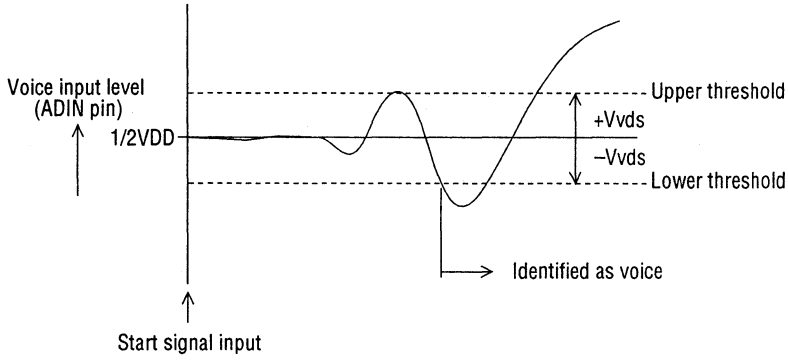
(2) Specify one of 63 phrases ch01 – ch3F by setting the CA0 – CA5 pins.

(3) To start playback, apply a low pulse to the $\overline{ST}$ pin. To stop playback in progress, apply a low pulse to the $\overline{SP}$ pin.

● Voice Activated Recording

This MSM6688 has the voice activated recording function to start recording when the level of voice input exceeds a preset amplitude. Using the voice activated function, the unvoiced part prior to voice detection will not be recorded, so that the memory capacity can be utilized efficiently.

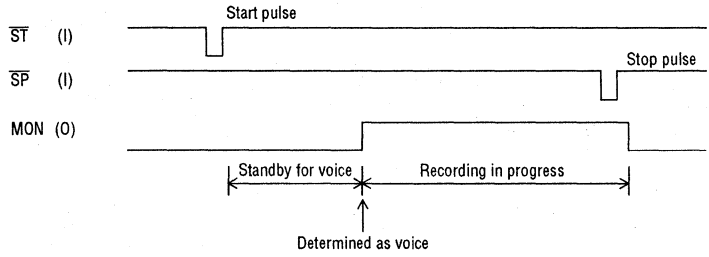
The unvoiced parts in the middle of recording are not eliminated. In the voice activated recording mode, recording is started when a voice input exceeds the preset thresholds. Therefore, a consonant part with a low level may not be recorded.



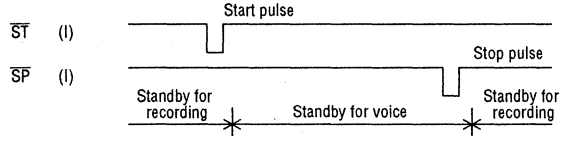
VDS pin	Voice activation conditions
L	Voice activation disabled
H	Voice activation enabled Voice detection threshold Vvds = VDD/32 (±160 mV)

The value in parentheses is for VDD = 5.12V.

When a low level is applied to the $\overline{ST}$ pin in the voice activated mode, the MSM6688 goes to the standby state for voice. When detecting a voiced input, it starts recording and the MON pin outputs a high level.

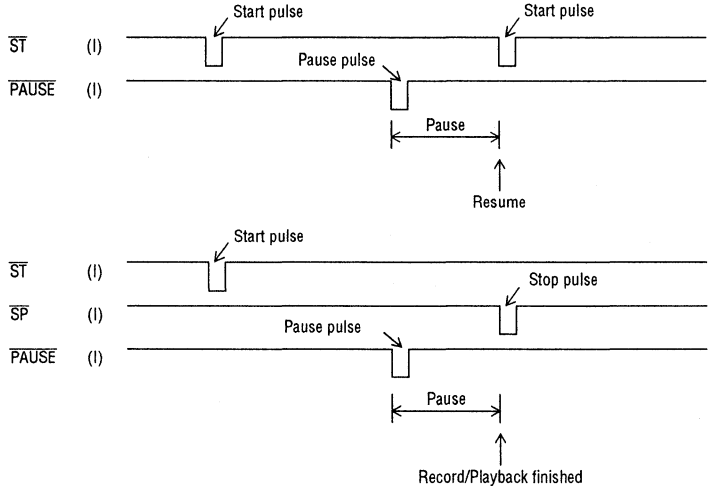


When a low level is applied to the $\overline{SP}$ pin during standby state for voice, the MSM6688 finishes the standby state for voice and goes to the standby state for recording.



● Method of Stopping Temporarily Record/Playback by Pause Function

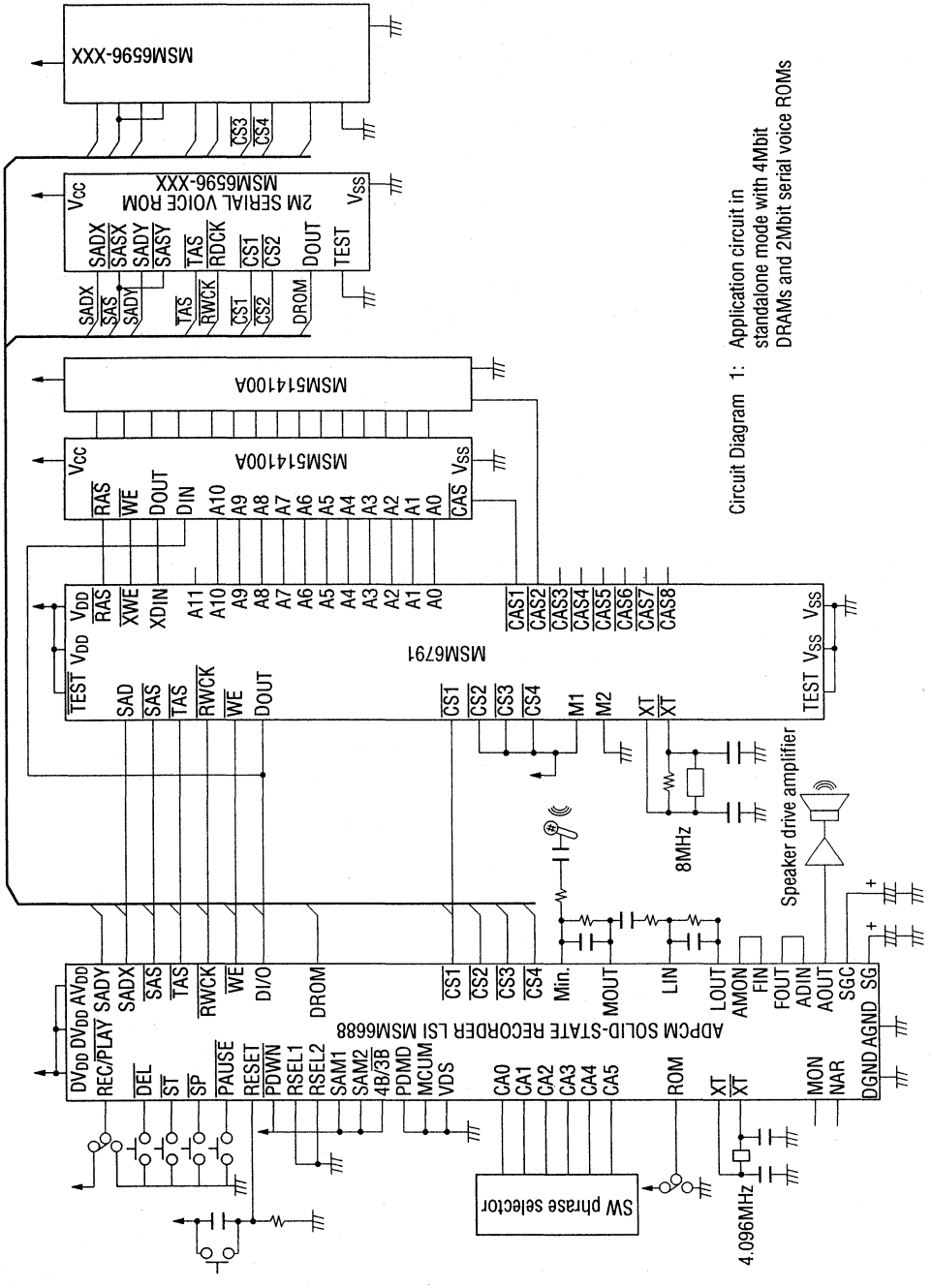
By applying a low pulse to the $\overline{\text{PAUSE}}$ pin during record/playback, record/playback operation can be stopped temporarily. To resume record/playback, apply a low pulse to the $\overline{\text{ST}}$ pin. To stop record/playback, apply a low pulse to the $\overline{\text{SP}}$ pin.



When record/playback is resumed after temporary stop, the voice activating circuit is not operated and recording is started when a start low pulse is applied to $\overline{\text{SP}}$ pin.

■ EXAMPLE OF APPLICATION CIRCUIT

● The circuit diagram 1 shows an application circuit example where the MSM6688 is used in the standalone mode and two 4Mbit DRAMs are used as record/playback memories by connecting a DRAM interface LSI, and two 2Mbit serial voice ROMs also are connected.



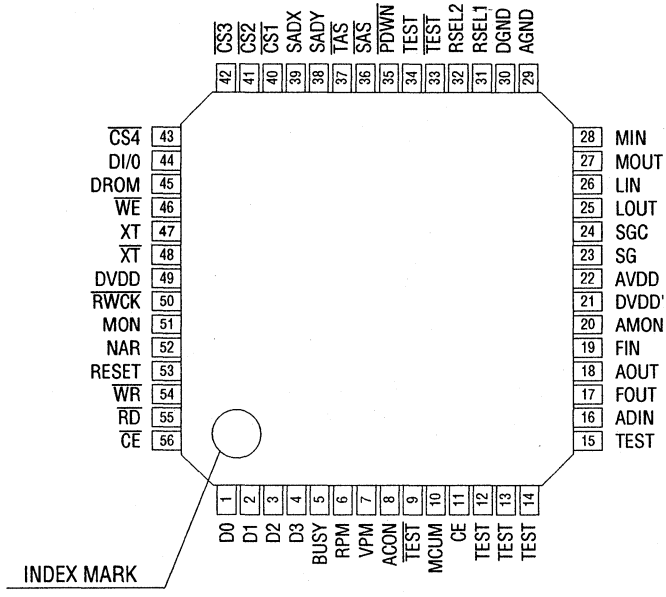
Circuit Diagram 1: Application circuit in standalone mode with 4Mbit DRAMs and 2Mbit serial voice ROMs

(2) MICROCONTROLLER INTERFACE MODE

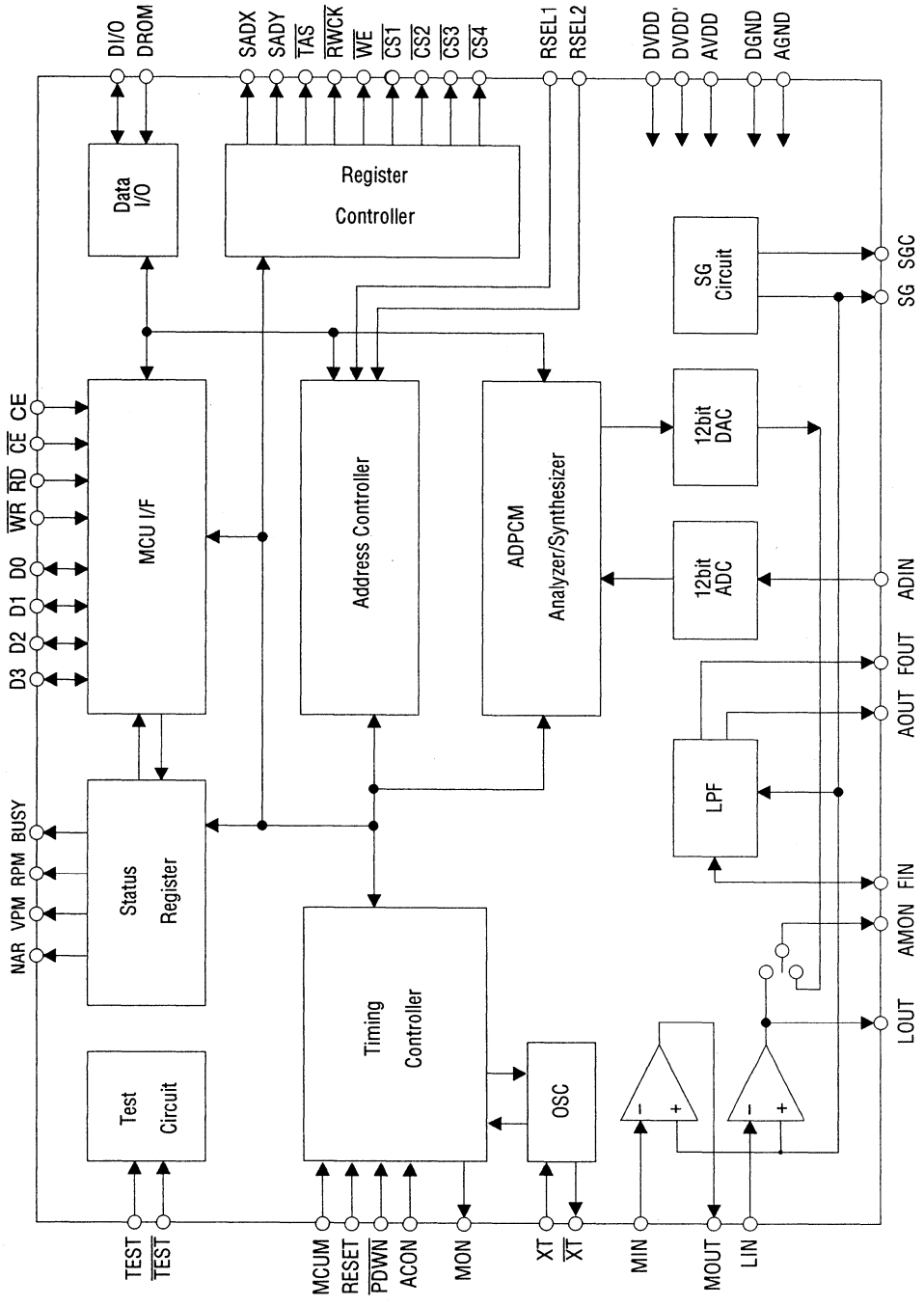
■ FEATURES

- 3-bit or 4-bit ADPCM
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  DRAM, maximum 32M bits (for variable messages)
  1/4/16Mbit DRAM (x1bit configuration) are controlled by DRAM interface LSI (MSM6791).
  Serial voice ROMs, maximum 4M bits (for fixed messages)
  1M bit serial voice ROM (MSM6595), directly addressable
  2M bit serial voice ROM (MSM6596), directly addressable
  3M bit serial voice ROM (MSM6597), directly addressable
- Sampling frequency
  4.0 kHz, 5.3 kHz, 6.4 kHz or 8.0 kHz
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when external 32Mbit RAM is connected)
  34 minutes (for 16kbps ADPCM)
  23 minutes (for 24kbps ADPCM)
  17 minutes (for 32kbps ADPCM)
- Voice activation function
- Pause function
- Master clock frequency: 4.096 MHz
- Power supply voltage: 5 V single power supply
- Package: 6-pin plastic QFP (QFP56-P-910-V1K)

■ PIN LAYOUT (TOP VIEW)



■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3~7.0	V
Input voltage	VIN	Ta=25°C	−0.3~VDD+0.3	V
Storage temperature	T_{stg}	–	−55~+150	°C

● Operating Range

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5~+5.5	V
Operating temperature	Top	–	0~+70	°C
Master clock frequency	fosc	–	4.0~8.192	MHz

● DC characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage	VIH	—	0.8×VDD	—	—	V
Low input voltage	VIL	—	—	—	0.2×VDD	V
High output voltage	VOH	IOH=−40μA	VDD−0.3	—	—	V
Low output voltage	VOL	IOL=2mA	—	—	0.45	V
High input current (Note 1)	IIH1	VIH=VDD	—	—	10	μA
High input current (Note 2)	IIH2	VIH=VDD	—	—	20	μA
Low input current (Note 1)	IIL1	VIL=GND	−10	—	—	μA
Low input current (Note 2)	IIL2	VIL=GND	−20	—	—	μA
Operating current consumption (1)	IDD	fosc = 8 MHz, no load	—	15	30	mA
Operating current consumption (2)	IPD	At power down, no load	—	—	10	μA

Note 1: Applies to all input pins excluding the XT pin.
Note 2: Applies to the XT pin.

● Analog Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0~4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

● AC Characteristics

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=4.096MHz f_{SAMP}=8.0kHz

Item		Symbol	Min.	Typ.	Max.	Unit
RESET pulse width		t_{RST}	1	–	–	µs
RESET execution time	(Note 1)*	t_{REX}	–	1	–	ms
$\overline{PDWN}$ low level time	*	t_{PDL}	500	–	–	µs
$\overline{PDWN}$ high level time	*	t_{PDH}	500	–	–	µs
Oscillating time after input of $\overline{PDWN}$	*	t_{PX}	125	–	500	µs
BUSY time after release of $\overline{PDWN}$	(Note 1)*	t_{BPD}	0.25	–	80	ms
$\overline{RD}$ pulse width		t_{RR}	200	–	–	ns
Setup and hold time of $\overline{CE}$ and CE for $\overline{RD}$		t_{CR}	30	–	–	ns
Time from $\overline{RD}$ fall to data valid		t_{DRE}	–	–	200	ns
Time from $\overline{RD}$ rise to data float		t_{DRF}	–	10	50	ns
$\overline{WR}$ pulse width		t_{WW}	200	–	–	ns
Setup and hold time of $\overline{CE}$ and CE for $\overline{WR}$		t_{CW}	30	–	–	ns
Data setup time to $\overline{WR}$ rise		t_{DWS}	100	–	–	ns
Data hold time from $\overline{WR}$ rise		t_{DWH}	30	–	–	ns
$\overline{RD}$ and $\overline{WR}$ disable time		t_{DRW}	250	–	–	ns
BUSY time after release of RESET	(Note 1)*	t_{BR}	–	–	1	ms
BUSY time after input of 1-nibble command	**	t_{B1}	–	–	16	µs
BUSY time after input of 2-nibble command	**	t_{B2}	–	–	16	µs
BUSY time after input of 3-nibble command	**	t_{B3}	–	–	16	µs
BUSY time after input of 2-nibble or 3-nibble command data	**	t_{BD}	–	–	16	µs
WAIT time after input of BLKRD command	*	t_{WBR}	270	–	–	µs
WAIT time after output of BLKRD command block data	*	t_{WDR}	50	–	–	µs
BUSY time after input of ADRWR command	*	t_{BAW}	–	–	270	µs
BUSY time after input of ADRWR command address data	*	t_{BAD}	–	–	50	µs
WAIT time after input of ADRRD command	*	t_{WAR}	270	–	–	µs
WAIT time after output of ADRRD command address data	*	t_{WDR}	50	–	–	µs
Address control time at start of record/playback	*	t_{AD1}	–	1	–	ms

Items with * are proportional to the period of master oscillator frequency fosc.
Items with ** are proportional to the period of the master oscillator frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

Note 1: The oscillation startup stabilization time is added to t_{REX}, t_{BPD} and t_{BR}.
The oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

DVDD=DVDD'=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=4.096MHz f_{SAMP}=8.0kHz

Item			Symbol	Min.	Typ.	Max.	Unit
Time from input of START command to MON rise	Flex record	*	tSTCM	–	–	50	ms
	Flex playback	*	tSTCM	–	–	20	ms
	Direct record/playback	*	tSTCM	–	–	1	ms
	ROM playback	*	tSTCM	–	–	1	ms
Time from input of STOP command to MON fall	Flex record	*	tSPCM	–	–	80	ms
	Flex playback	*	tSPCM	–	–	2	ms
	Direct record/playback	*	tSPCM	–	–	2	ms
	ROM playback	*	tSPCM	–	–	2	ms
Time from input of START command to setting of RPM bit		*	tSTCR	–	–	16	µs
Time from input of STOP command to end of record/playback		*	tSPCR	–	–	2	ms
Time from input of STOP command to release of standby for voice	Flex record	*	tSPCV	–	–	80	ms
	Direct record	*	tSPCV	–	–	2	ms
Time from input of START command to NAR bit fall during continuos playback		*	tSTCN	–	–	16	µs
Unvoiced time between phrases during continuous playback		*	tMID	–	1.25	–	ms
Time from input of PAUSE command to setting of VPM bit		**	tPSCP	–	–	16	µs
Time from input of START command during pause to resetting of VPM bit		**	tSTCP	–	–	500	µs
Time from input of STOP command during pause to resetting of VPM bit		**	tSPCP	–	–	500	µs
CHRW command	WAIT time after input of command	*	tWCRW	770	–	–	µs
	WAIT time after input of REC command	*	tWRC	16	–	–	µs
	WAIT time after input of write data	*	tWWD	50	–	–	µs
	WAIT time after input of PLAY command	*	tWPL	50	–	–	µs
	WAIT time after input of STOP command	*	tWSP	50	–	–	µs
DTRW and DTRD commands	WAIT time after input of command	*	tWRW	16	–	–	µs
	WAIT time after input of address (2nd–5th nibbles)	*	tWA1	16	–	–	µs
	WAIT time after input of address (6th nibble)	*	tWA2	270	–	–	µs
	WAIT time after input of REC command	*	tWRC	16	–	–	µs
	WAIT time after input of write data	*	tWWD	50	–	–	µs
	WAIT time after input of PLAY command	*	tWPL	50	–	–	µs
	WAIT time after input of STOP command	*	tWSP	16	–	–	µs

Items with * are proportional to the period of master oscillator frequency fosc.
Items with ** are proportional to the period of the master oscillator frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

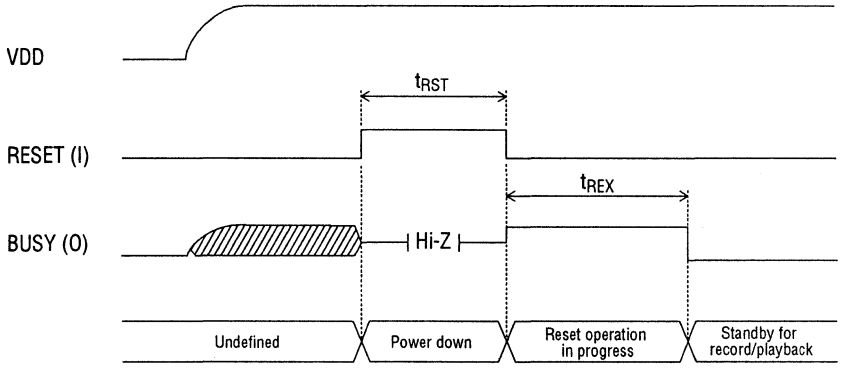
DVDD=DVDD'=AVDD=4.5V~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=4.096MHz f_{SAMP}=8.0kHz

Item			Symbol	Min.	Typ.	Max.	Unit
WAIT time for deletion of all phrases after input of DEL command		*	tWBLA	550	–	–	ms
WAIT time for deletion of a specified phase after input of DEL command		*	tWBLI	70	–	–	ms
Time to start of DC level transition after input of LEV command		*	tLV	–	–	16	µs
DC level transition time (GND to 1/2 VDD)		*	tAOR	–	64	–	ms
DC level transition time (1/2 VDD to GND)		*	tAOF	–	256	–	ms
EXT command	Time from input of EXT command to MON rise	**	tEM	–	–	330	µs
	MON high level time	**	tMH	–	31	–	µs
	MON low level time	**	tML	–	94	–	µs
	Time from MON rise to RD pulse rise during recording	**	tERD	–	–	120	µs
	Time from MON rise to WR pulse rise during playback	**	tEWR	–	–	120	µs
	Time from MON rise to input of STOP command	**	tESP	–	–	100	µs
	Time from input of STOP command to end of record/playback	**	tWEX	–	–	250	µs

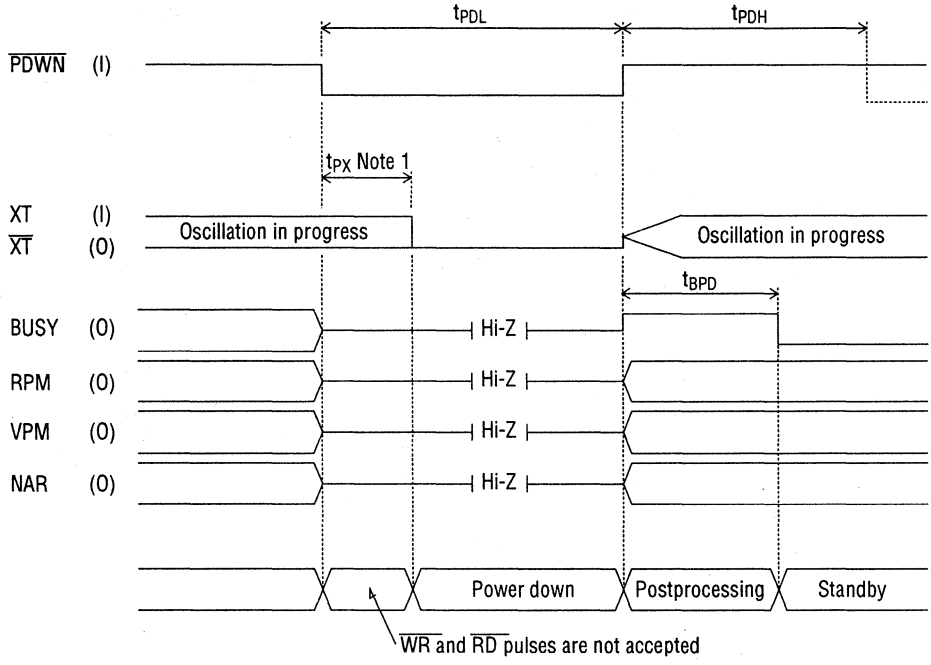
Items with * are proportional to the period of master oscillator frequency fosc.
Items with ** are proportional to the period of the master oscillator frequency fosc, and are also proportional to the sampling frequency f_{SAMP} during record/playback.

■ TIMING DIAGRAMS

● Reset Function

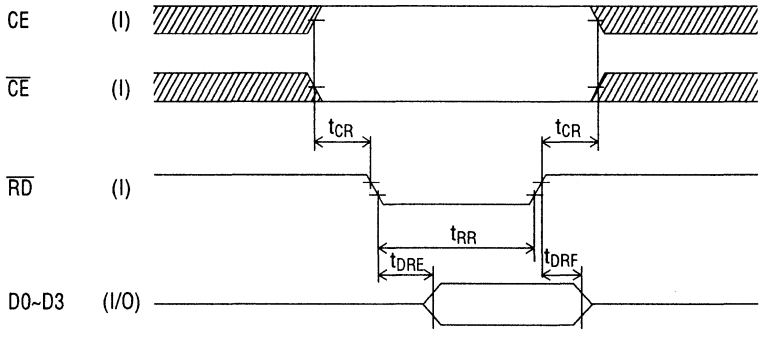


● Power Down by the $\overline{\text{PDWN}}$ pin

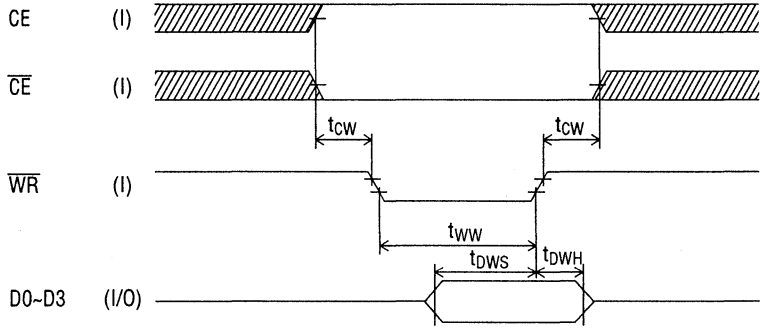


Note 1: When an external clock is used, apply a low level to the $\overline{\text{PDWN}}$ pin and then continue to apply the external clock to the XT pin for t_{PX}.

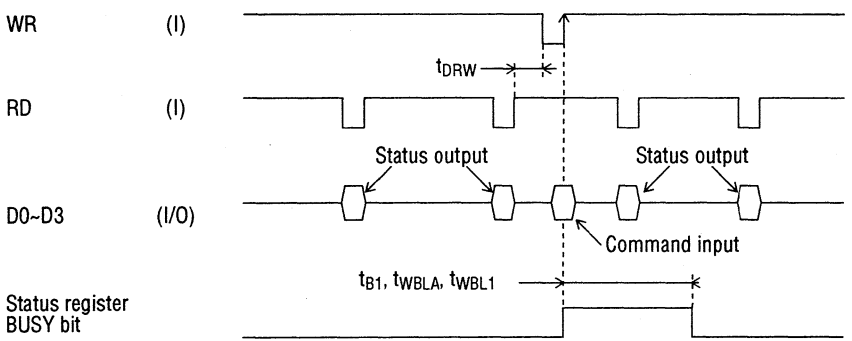
● Data Read Timing ($\overline{RD}$ Pulse)



● Data Write Timing ($\overline{WR}$ Pules)

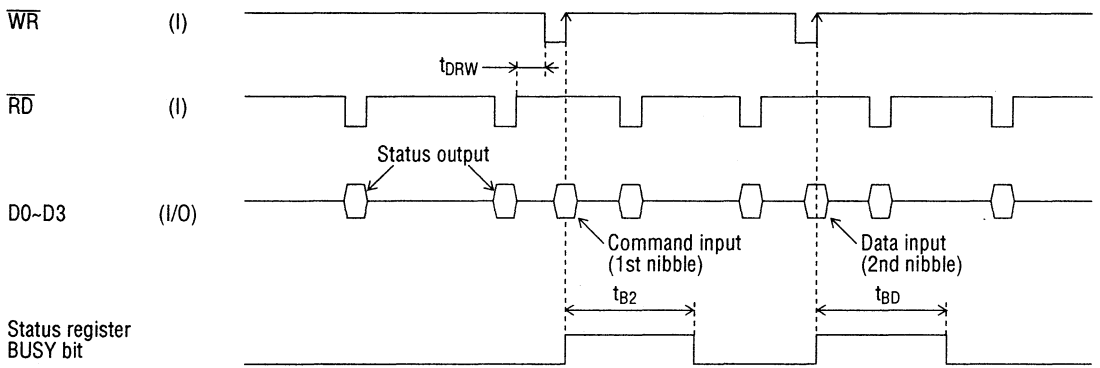


● Inputting 1-Nibble Commands (NOP, PAUSE, PLAY, REC, START, STOP and DEL Commands)



t_{B1}: NOP, PAUSE, PLAY, REC, START, and STOP commands
t_{WBLA}: DEL command (deletion of all phrases)
t_{WBL1}: DEL command (deletion of a specified phrase)

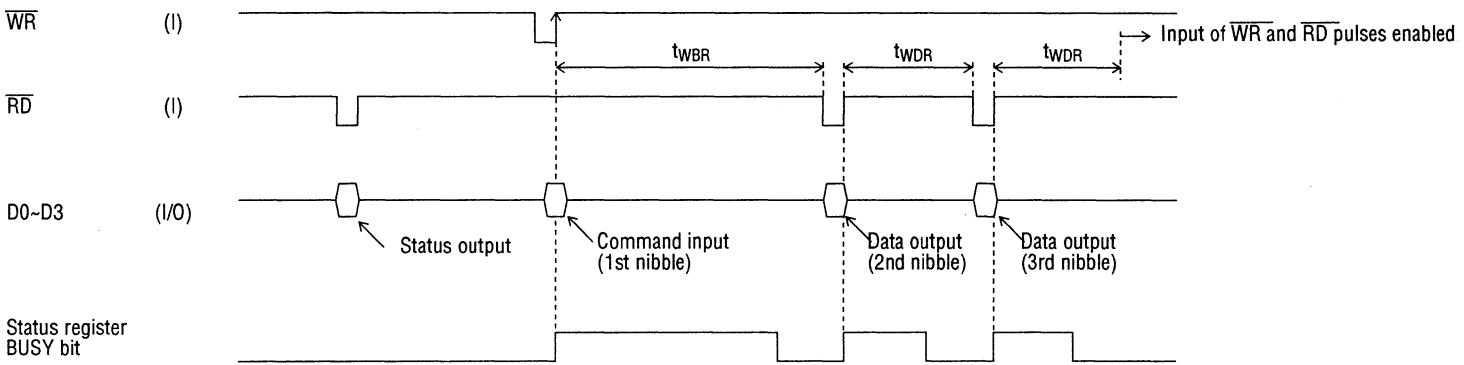
● Inputting 2-Nibble Commands (SAMP, VDS, and LEV Commands)



The LEV command is used to specify the playback level.
See the timing diagram for
DC level transition by the LEV command.

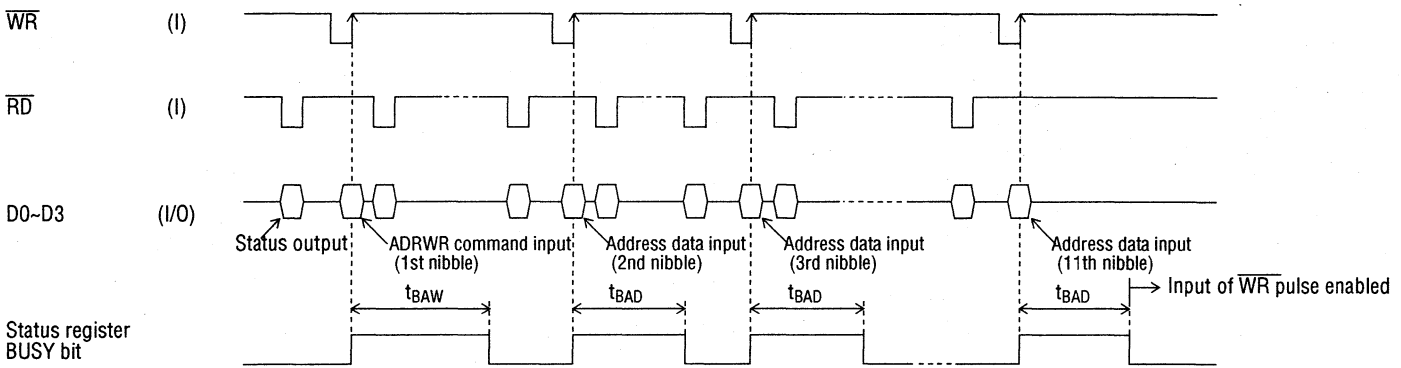
● Inputting 3-Nibble Commands (CHAN and BLKWR Commands)

● Inputting the BLKRD Command



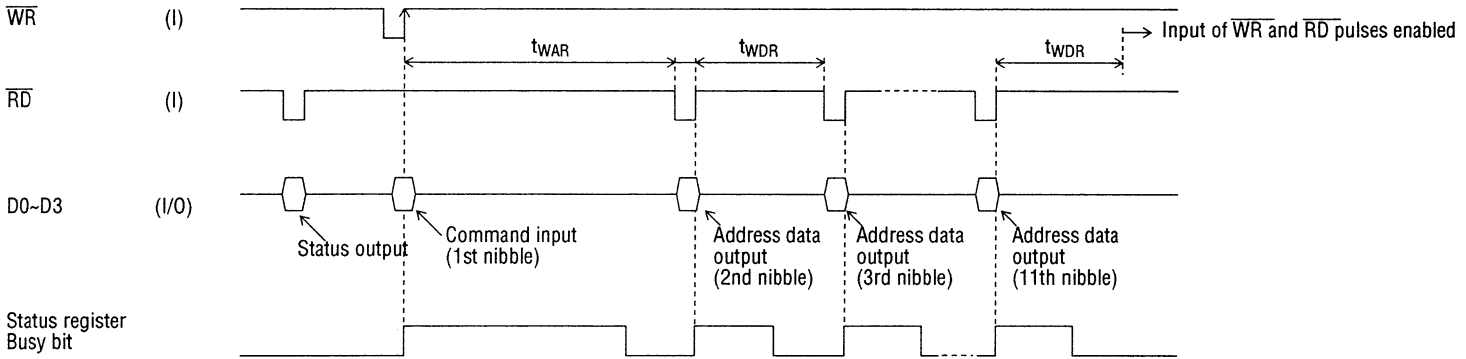
1. After making sure that the MSM6688 is not in the busy state by checking the BUSY bit of the status register, input the BLKRD command.
2. Then, the data is read according to the 2nd and 3rd nibble command.
   However, the status of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse. Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WBR} or t_{WDR} or after verifying the BUSY state at BUSY output pin.

● Inputting the ADRWR Command



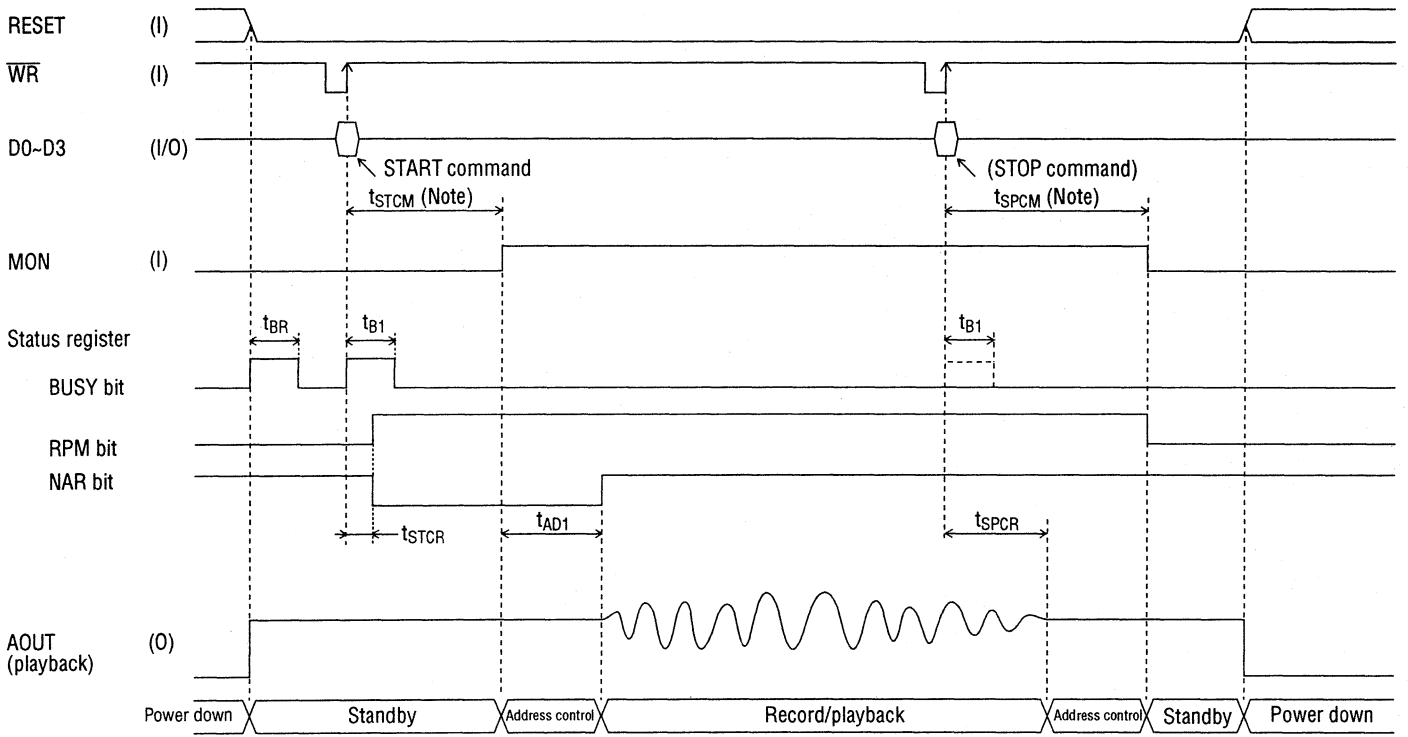
1. After making sure that the MSM6688 is not in the busy state by checking the BUSY bit of the status register, input the ADRWR command.
2. Then, input 2nd-11th nibble address data after making sure that the MSM6688 is not in the BUSY state by one of the following two methods.
   - Check of the BUSY bit in the status register
   - Input the next $\overline{WR}$ pulse after the waiting time t_{BAW} or t_{BAD}.

● Inputting the ADRRD Command



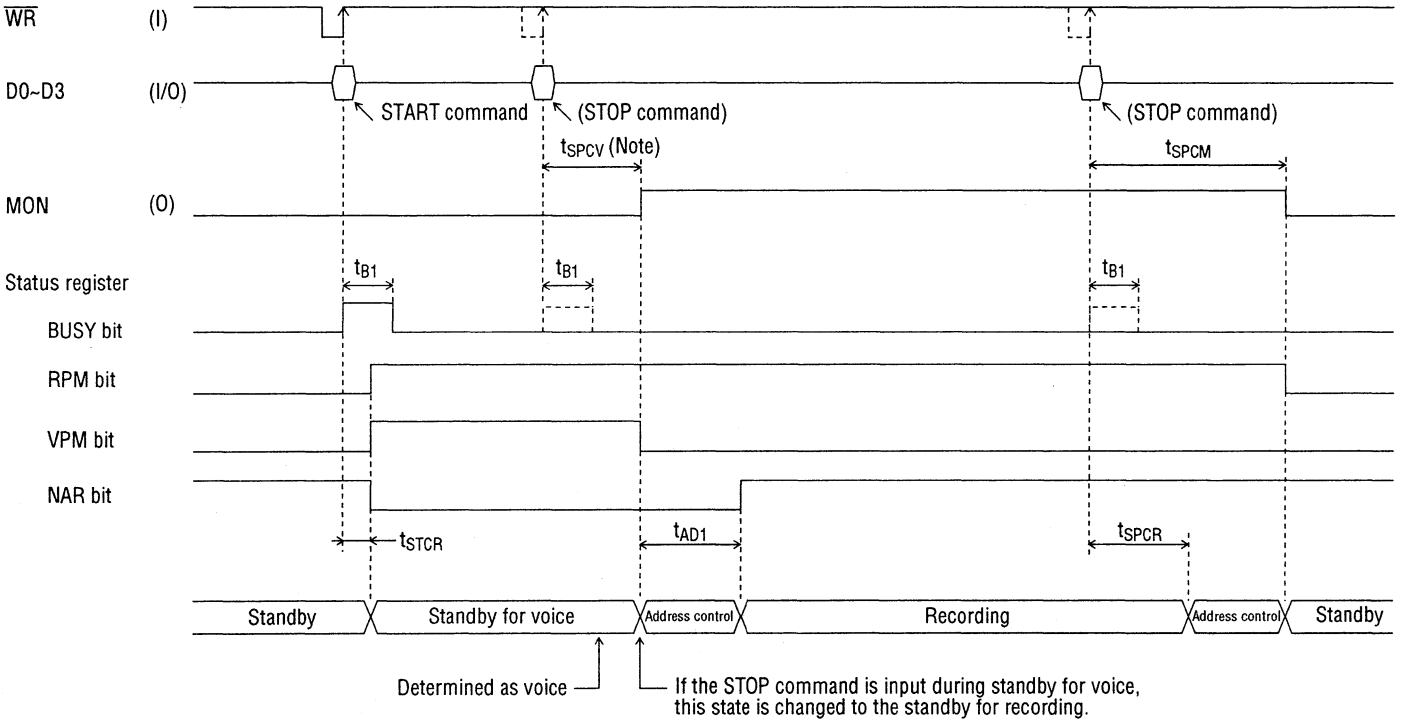
1. After making sure that the MSM6688 is not in the busy state by checking the BUSY bit of the status register, input the ADRRD command.
2. Then, the address data is read according to 2nd through 11th nibble command.
   The state of the BUSY bit cannot be checked by the $\overline{RD}$ pulse.
   Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WAR} or t_{WDR} or after verifying the BUSY state at the BUSY output pin.

● Timing for Record/Playback by START Command



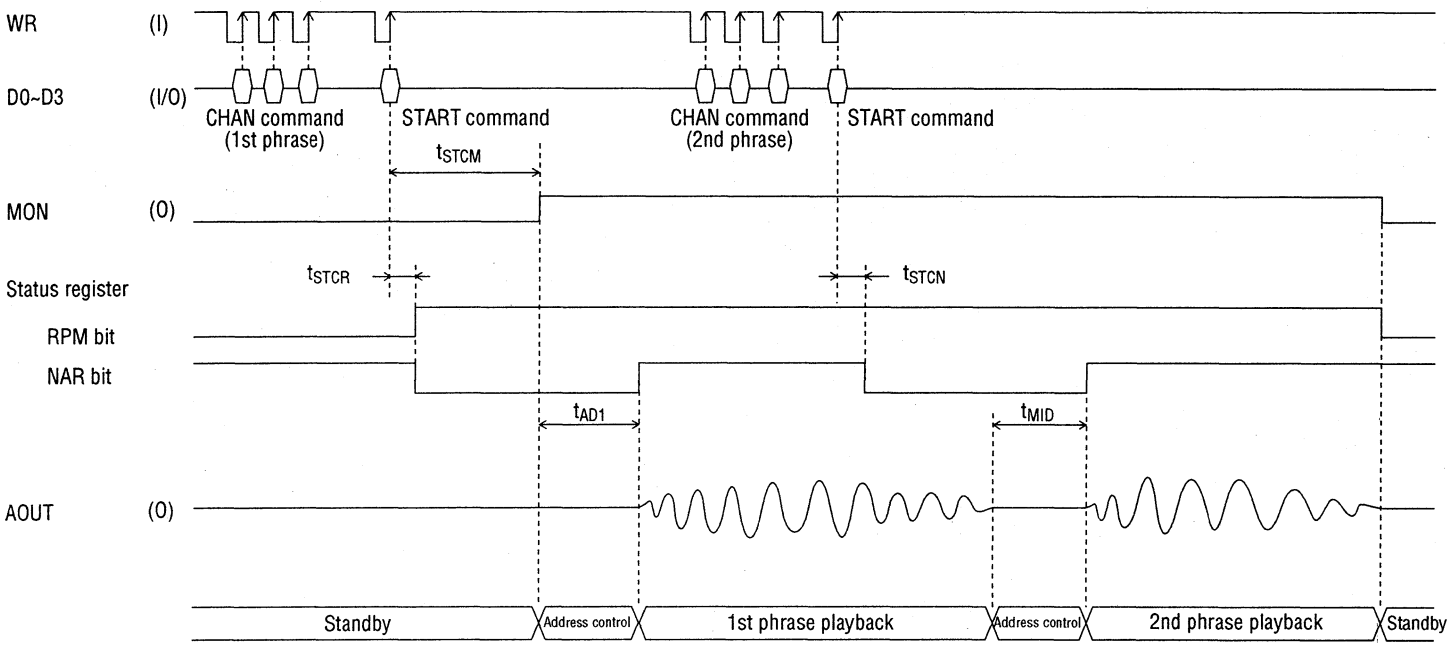
Note: t_{STCM} and t_{SPCM} vary depending on the control mode for record/playback and on record or playback mode.

● Voice Activation Timing

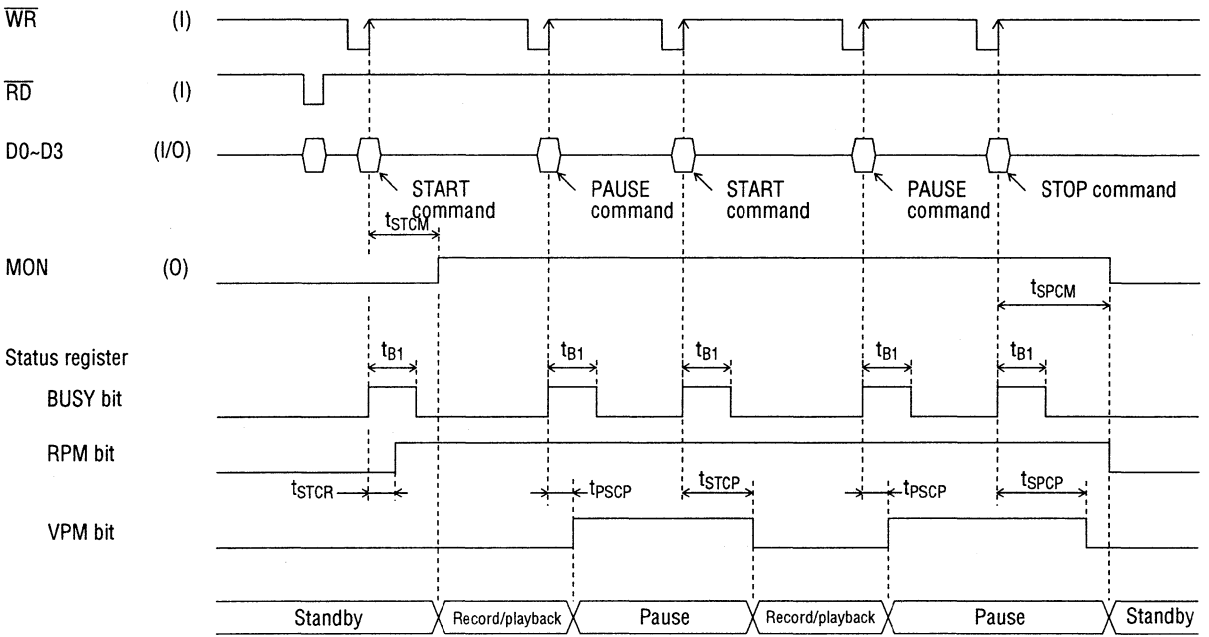


Note: t_{spcv} varies depending on the recording mode (flex recording or direct recording).

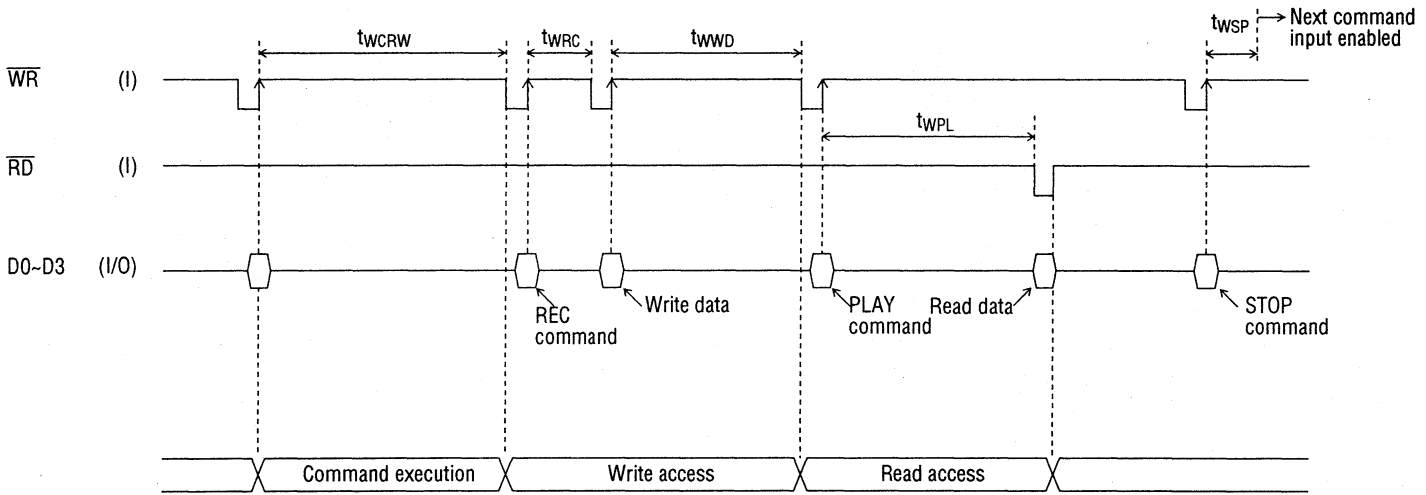
● Timing for Continuous ROM Playback by Input of Address Code



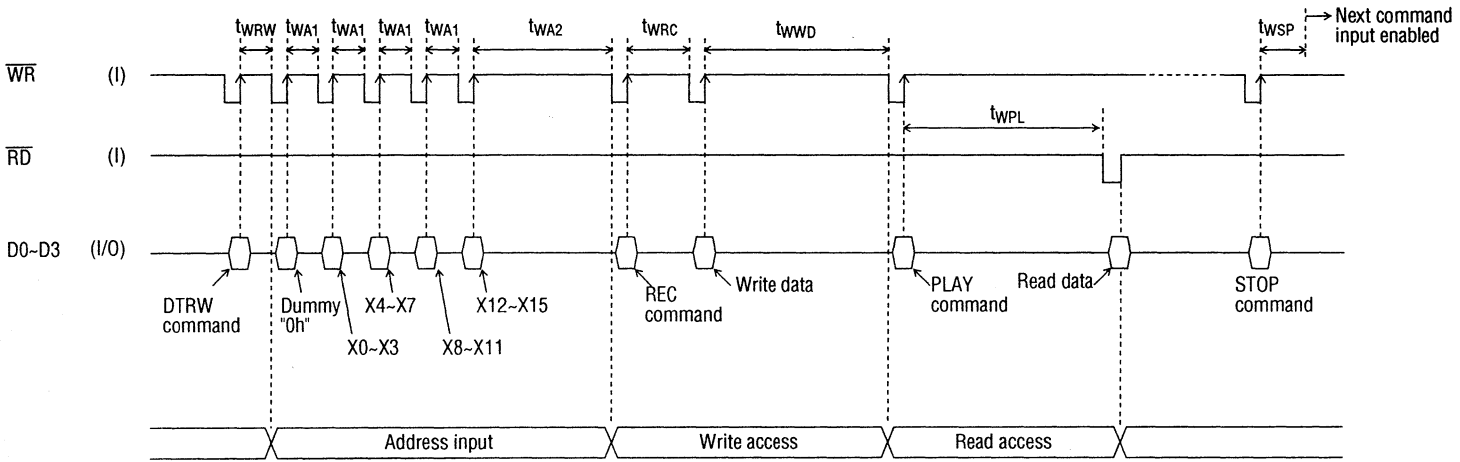
● Timing for Record/Playback Pause Operation by PAUSE Command



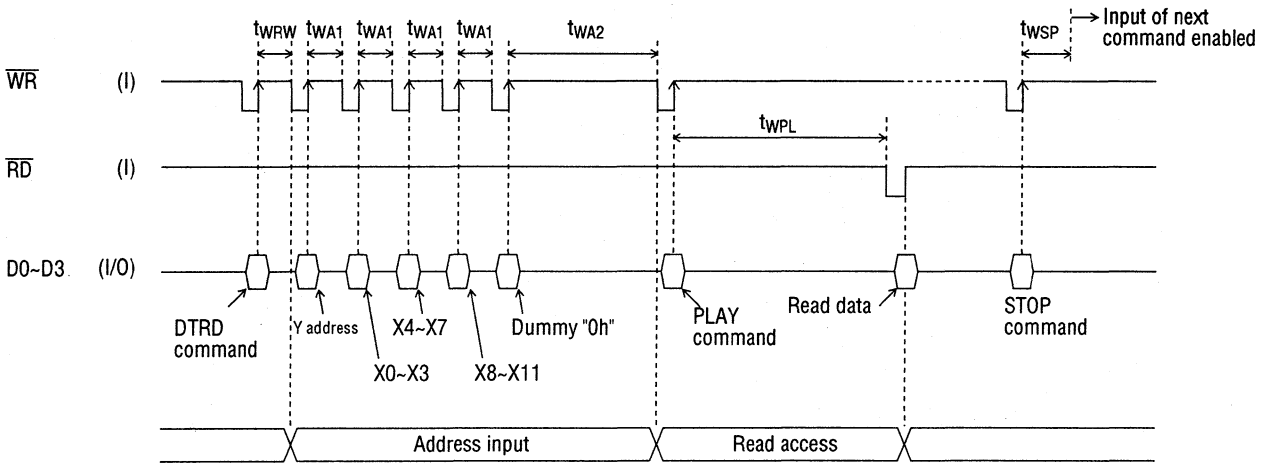
● Timing for Data Transfer by CHRW Command



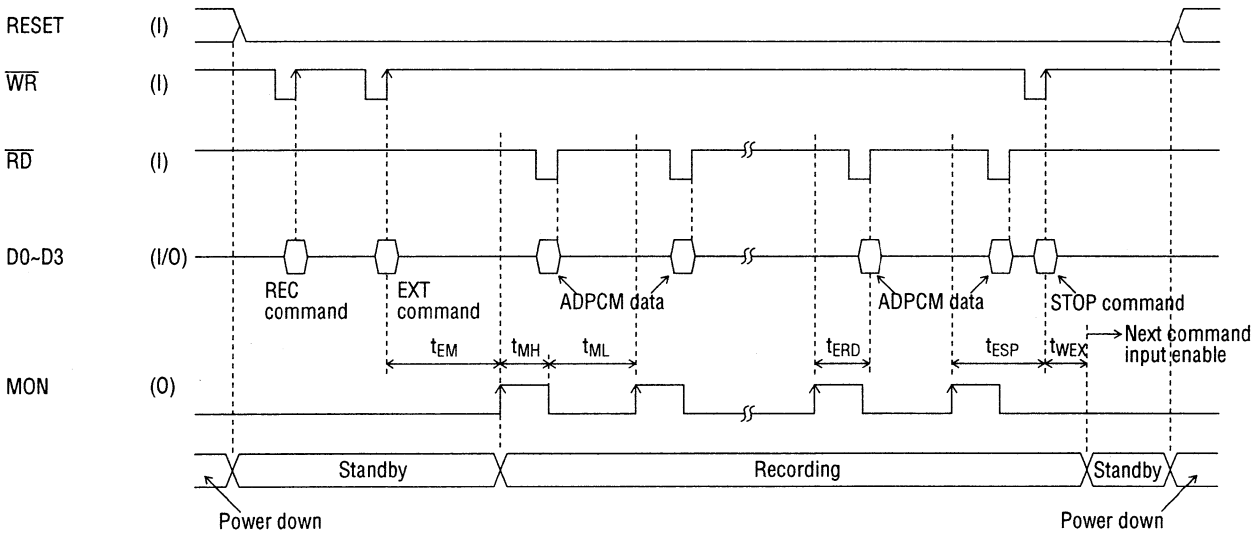
● Timing for Data Transfer by DTRW Command



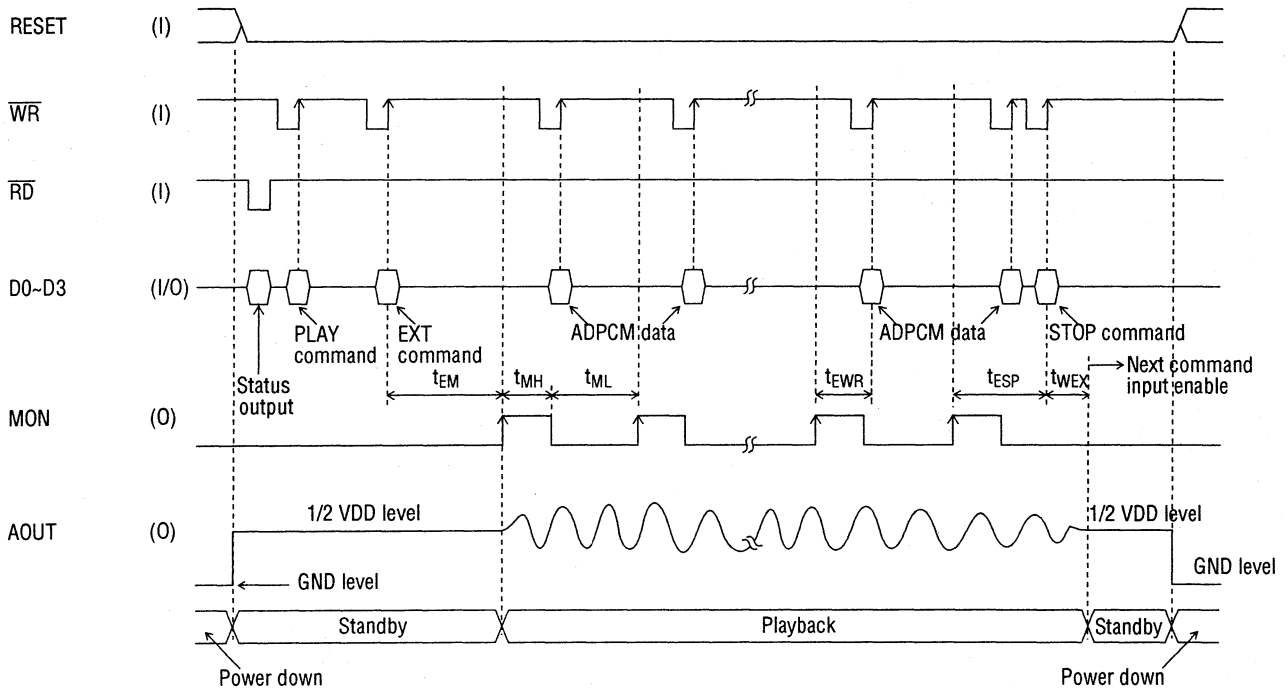
● Timing for Data Read by DTRD command



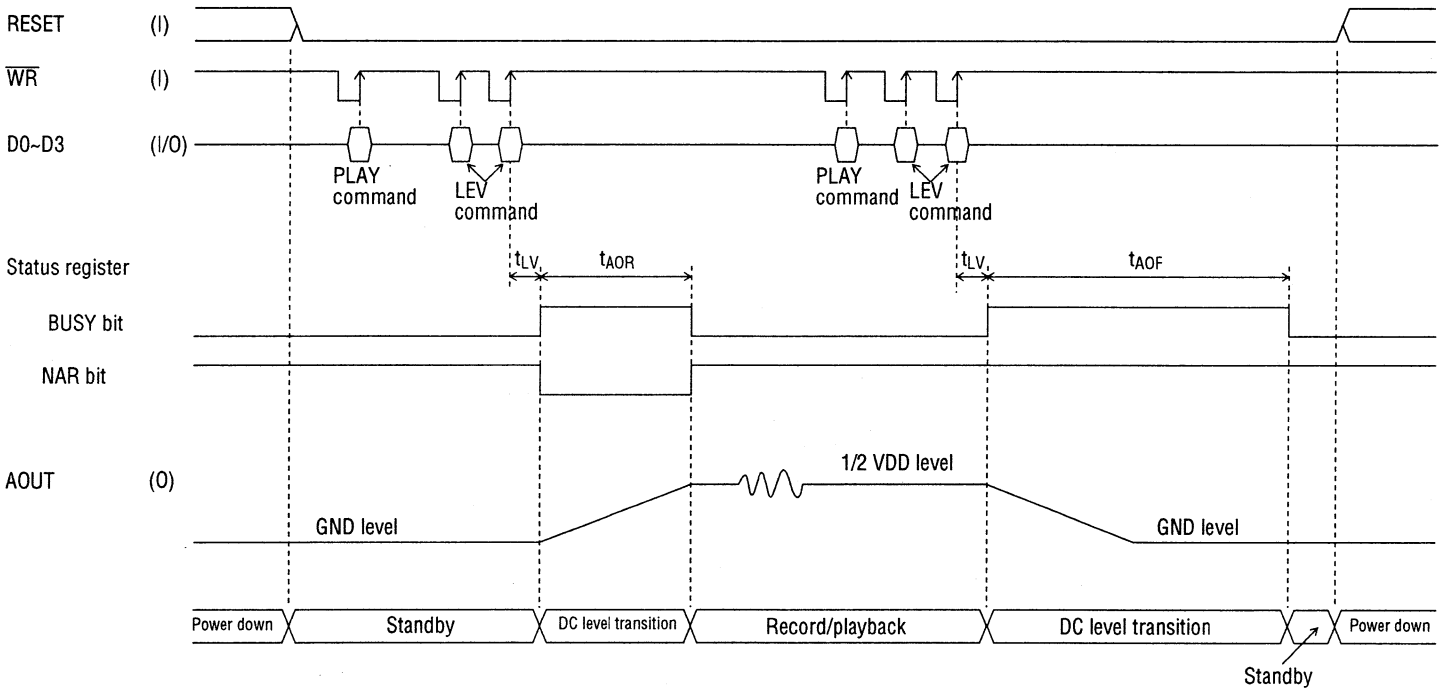
● Recording by EXT Command



● Playback by EXT Command



● Timing for DC Level Transition by LEV Command



■ PIN DESCRIPTION

Pin name	I/O	Pin function
DVDD	I	Digital power supply pin
DVDD'	I	Digital power supply pin
AVDD	I	Analog power supply pin
DGND	I	Digital ground pin
AGND	I	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	O	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin)
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). Used to connect the SAD pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external MSM6791 (DRAM interface LSI) and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each MSM6791 (DRAM interface LSI) and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external MSM6791 (DRAM interface LSI) and the $\overline{RDCK}$ pin of each external serial voiceROM. This pin outputs a clock to read data from or write it into each external serial register
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external MSM6791 (DRAM interface LSI). This pin outputs $\overline{WE}$ signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN pin of DRAM and MSM6791 (DRAM interface LSI). This pin outputs the data to be written into the serial register or inputs the data read from the serial registers.
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voiceROM.

Pin name	I/O	Pin function
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O O O O	(Chip Select). Used to connect the $\overline{CS1}$~$\overline{CS4}$ pins of MSM6791 (DRAM interface LSI). and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of each serial voice ROM
RSEL1 RSEL2	I I	(Register Select). These are used to select the maximum controlled size of external RAM. RSEL2: L L H H RSEL1: L H L H Total memory size: 8Mbit 16Mbit 24Mbit 32Mbit
MCUM	I	This pin is used to select either the stand-alone mode or the microcontroller interface mode. Low level: Stand-alone mode High level: Microcontroller interface mode
RESET	I	A high input level at this pin causes the MSM6688 to be initialized and to go into the power down state.
$\overline{PDWN}$	I	(Power Down). When a low level is input to this pin, the MSM6688 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6688. When an low level is applied to this $\overline{PDWN}$ pin during recording operation, the MSM6688 is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.
D0 D1 D2 D3	I/O	Bi-directional data bus to transfer commands and data to and from an external microcontroller.
$\overline{WR}$	I	Write pulse input pin. Inputting a low pulse to this $\overline{WR}$ pin causes a command or data to be input via D0~D3 pins.
$\overline{RD}$	I	Read pulse input pin. Inputting a low pulse to this $\overline{RD}$ pin causes status bits or data to be output via D0~D3 pins.
$\overline{CE}$ CE	I I	Chip enable input pins. When the $\overline{CE}$ pin is set to a low level or the CE pin is set to a high level, the write pulse ($\overline{WR}$), read pulse ($\overline{RD}$) can be accepted. When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be transferred to and from via D0~D3 pins.
BUSY	O	Outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0~D3 pins. The state of this BUSY pin is the same as the contents of the BUSY bit of the status register
RPM	O	Outputs a high level during recording or playback operation. The state of this RPM is the same as the contents of the RPM bit of the status register.
VPM	O	Outputs a high level during the standby for voice after the start of voice activated recording and the record/playback is stopped temporarily by inputting the PAUSE command. The state of this VPM pin is the same as the contents of the VPM bit of the status register.
NAR	O	This NAR bit indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM playback operation, specify the next phrase after making sure that the NAR output is high, and input the START command.

Pin name	I/O	Pin function
ACON	I	Used to select the use or nonuse of the pop noise suppression circuit at the analog output (AOUT) pin. When low level, the pop noise suppression circuit is used. When high level, the pop noise suppression circuit is not used.
XT	I	Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.
$\overline{XT}$	O	Used to connect an oscillator, when an external clock is used, this pin must be left open.
MON	O	Outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
TEST $\overline{TEST}$	I	Used to test the MSM6688. Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.

■ FUNCTIONAL DESCRIPTION

● Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external serial registers, sampling frequency, and ADPCM bit length, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K bits)}}{\text{sampling frequency (kHz)} \times \text{bit length (bits)}} \quad \text{(seconds)}$$

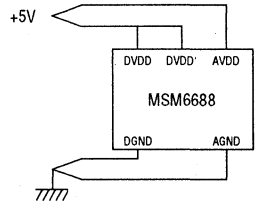
For example, if the sampling frequency is $\frac{4096}{768}$ kHz (= 5.333 kHz), ADPCM bit length is 3 bits, and four 8M bit serial registers are used, the recording time can be obtained as follows.

$$\text{Recording time} = \frac{1.024 \times (8192 \times 4 - 64)}{5.333 \times 3} = 2093 \text{ seconds}$$
$$= 34 \text{ minutes } 53 \text{ seconds}$$

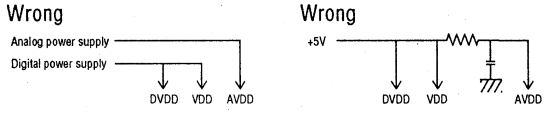
In the above equation, the memory capacity is obtained by subtracting the memory capacity (64 Kbits) for the channel index area from the total memory capacity.

● Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6688 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.



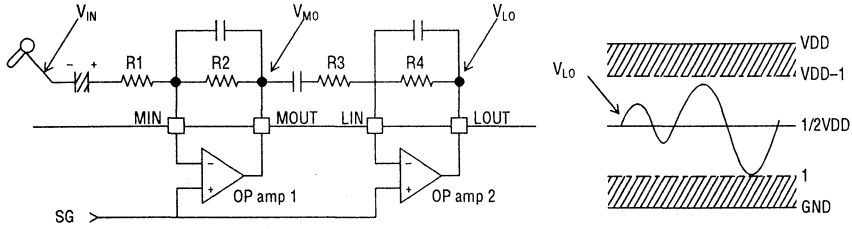
Do not supply the power to the logic portion and the analog portion from the separate power sources. Otherwise, a problem such as latch-up may occur.



● Analog Input Amplifier Circuit

This MSM6688 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \cdot R4}{R1 \cdot R3} V_{IN} \ (V)$$

During the time the recording operation is performed, the output V_{LO} of OP amp 2 is connected to the input FIN of the built-in LPF. The FIN allowable input voltage (V_{FIN}) ranges from 1V to (V_{DD} – 1)V. Therefore, the amplification ratio must be adjusted so that the V_{LO} amplitude can be within the FIN allowable input voltage range.

For example, if V_{DD} = 5V, V_{LO} becomes 3 V_{p-p} max. If V_{LO} exceeds the FIN allowable input voltage range, the output of the LPF will be a clipped waveform.

The load resistance R_{OUTA} of the OP amp is 200 kΩ minimum, so that the feedback resisters R2 and R4 of the inverting amplifier circuit must be 200 kΩ or more.

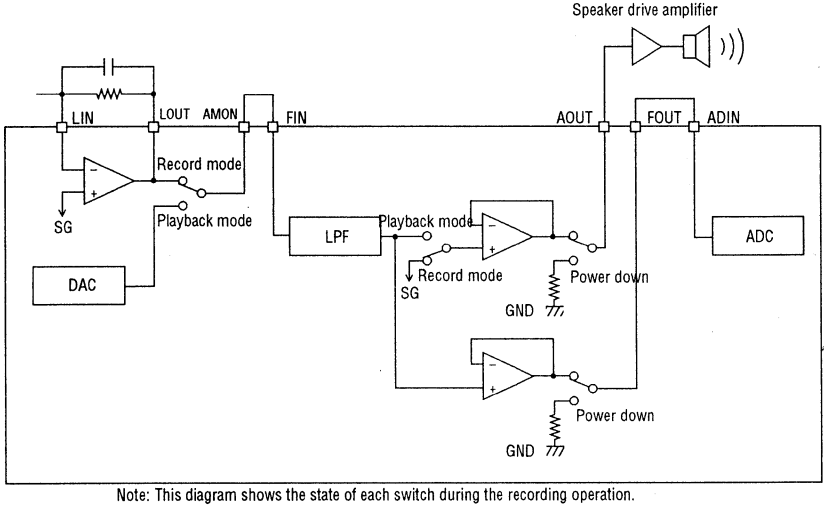
● Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6688, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

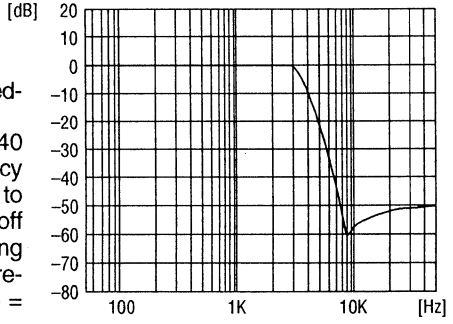
Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)



Note: This diagram shows the state of each switch during the recording operation.

● LPF Characteristics

This MSM6688 contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.



LPF Frequency Characteristics (fsamp = 8.0 kHz)

● Reset Function

By applying a high level to the RESET pin, the MSM6688 stops oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

When this reset operation is performed, the record/playback condition, such as sampling frequency and ADPCM bit length, and the data stored in the serial registers are set to the data stored just before the reset takes place. In this case, the playback level is set to 0 dB amplitude.

If a high level is applied to the RESET pin during command execution or record/playback operation, the MSM6688 is set to the power-down state and initialized state. Internal data voice data becomes undefined.

The following shows the power-down state of the MSM6688.

(1) Oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) D0–D3 pins constituting the data bus go to the high-impedance state, independ the state of the $\overline{RD}$, $\overline{CE}$, and CE pins.

(4) $\overline{CS1}$ – $\overline{CS4}$ pins are set to a high level to minimize the current consumption of external serial registers and serial voice ROMs.

(5) The state of the output pins and input/output pins are as follows.

SADX, $\overline{SAS}$, $\overline{TAS}$, $\overline{CS1}$ – $\overline{CS4}$,
$\overline{WE}$, $\overline{RWCK}$, and NAR pins: ..... High level
SADY, MON pin: ..... Low level
D0–D3, DI/0, BUSY, RPM, and VPM pins: ..... High impedance
AOUT and FOUT pins: ..... Ground level

After powering up the MSM6688, be sure to initialize it by applying a high level to the RESET pin.

● Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6688 is set to the power-down state, in which the frequency oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external serial registers. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ goes to a low level during command execution, this execution of command is halted at the time that power-down operation is performed. When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the record/playback operation: The record/playback operation is stopped. After the release of the power-down state, the postprocessing will be performed. The end of the postprocessing can be verified by checking the BUSY bit and RPM bit of the status register.

(2) When the MSM6688 is prowered down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporarily stopped and will be restarted after the release of the power-down state. The end of the phrase deleting operation can be verified by checking the BUSY bit.

(3) When the MSM6688 is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level by LEV command is in progress: This transition operation is temporarily stopped and will be continued after the release of the power-down state. The end of the transition to a DC level can be verified by checking the BUSY bit.

● Record/Playback Control Modes

There are four types of record/playback mode: flex record/playback, ROM playback by inputting address codes, direct record/playback, and direct ROM playback modes. A desired record/playback control mode can be selected by the command mode set in the SAMP command.

Record/ playback control mode	Flex record/playback	ROM playback by input of address code	Direct record/playback	Direct ROM playback
Command mode	Mode 0	Mode 1	Mode 2	Mode 3
Number of phrases	63	255	64 (expandable)	As required
Addressing	Indirect addressing by phrase designation	Indirect addressing by phrase designation	Direct addressing by ADRWR command	Direct addressing by ADRWR command
Setting of recording time	Setting by BLKWR command	—	Setting by ADRWR command	—

1. Flex record/playback

The recording area for each phrase is indirectly specified by phrase designation (CA0–CA5, 63 phrases). The recording area for each phrase is controlled by the MSM6688, so that the address control load of the microcontroller can be reduced.

The recording time is specified by the BLKWR command. During recording operation, the MSM6688 searches the memory areas that are not used by other phrases and writes the voice data on them. Therefore, the phrase control by the microcontroller can be performed easily even in applications in which it is required to perform phrase deletion and re-recording frequently.

2. ROM playback by input of address codes

The playback area of each phrase of the fixed message is indirectly specified by phrase designation (CA0–CA7, 255 phrases).
The table containing the start address and stop address that indicate the playback area, sampling frequency and ADPCM bit length, is written in the index area of the serial voice ROM.

3. Direct record/playback

The recording area for each phrases is specified directly by inputting the address set in the ADRWR command from the microcontroller after a desired phrase has been specified by phrase designation (CA0–CA5, 64 phrases). This means that the address control such as the allocation of memory capacity (recording time) for each phrases is performed by the microcontroller.

This direct record/playback mode is suitable for the case where the number of phrases and the recording time allocated to each phase are fixed. If the table containing the start address and stop address of each phrase is stored in the microcontroller or an external circuit, it becomes possible to perform record/playback of 65 or more phrases.

4. Direct ROM playback

The playback area of each phrase for a fixed message is specified directly by inputting the address set in the ADRWR command from the microcontroller. In this case, it is required to store the table containing the start and stop addresses of each phrase, sampling frequency and ADPCM bit length in the microcontroller and the external ROM.
If a serial voice ROM products for the MSM6388/MSM6588 ADPCM solid state recorders are used for the MSM6688, this direct ROM playback mode is applied.

● Data Configuration of External Serial Registers

The external RAM constitutes a virtual memory with a address space of (X addresses in the word direction) × (depth of 1kbits) through the DRAM interface (MSM6791).
This virtual memory is addressable only for X addresses in the word direction.
The external RAM is divided into the channel index area that stores the data for address control of each phrase and the voice (ADPCM) data area.
The address space and channel index area in the flex record/playback mode are different from those in the direct record/playback mode.

1. Address space allocation of external serial registers

1.1 Address space for the flex record/playback mode

In the flex record/playback mode, the total memory capacity of external serial registers is equally divided into 256 blocks that are addressable by 00h–FFh.

Each block is composed of multiple words each having the depth of 1K bits. X addresses in the word direction are offset addresses in the blocks. The memory capacity of one block and the maximum address of X addresses vary depending on the total memory capacity of serial registers externally

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity (Number. of serial registers)		8M bits (1)	16M bits (2)	24M bits (3)	32M bits (4)
Memory capacity of one block		32K bits	64K bits	128K bits	128K bits
Recording time of one block	16kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	24kbps	1.4 seconds	2.7 seconds	5.5 seconds	5.5 seconds
	32kbps	1.0 second	2.0 seconds	4.1 seconds	4.1 seconds
Number of words of one block [Offset address]		32 words [00h~1Fh]	64 words [00h~3Fh]	128 words [00h~7Fh]	128 words [00h~7Fh]
Number of initially available blocks		254 (FEh)	255 (FFh)	191 (BFh)	255 (FFh)

connected.

The storing method of 1K-bit ADPCM data in the Y direction varies depending on the ADPCM bit length (3-bit ADPCM or 4-bit ADPCM).

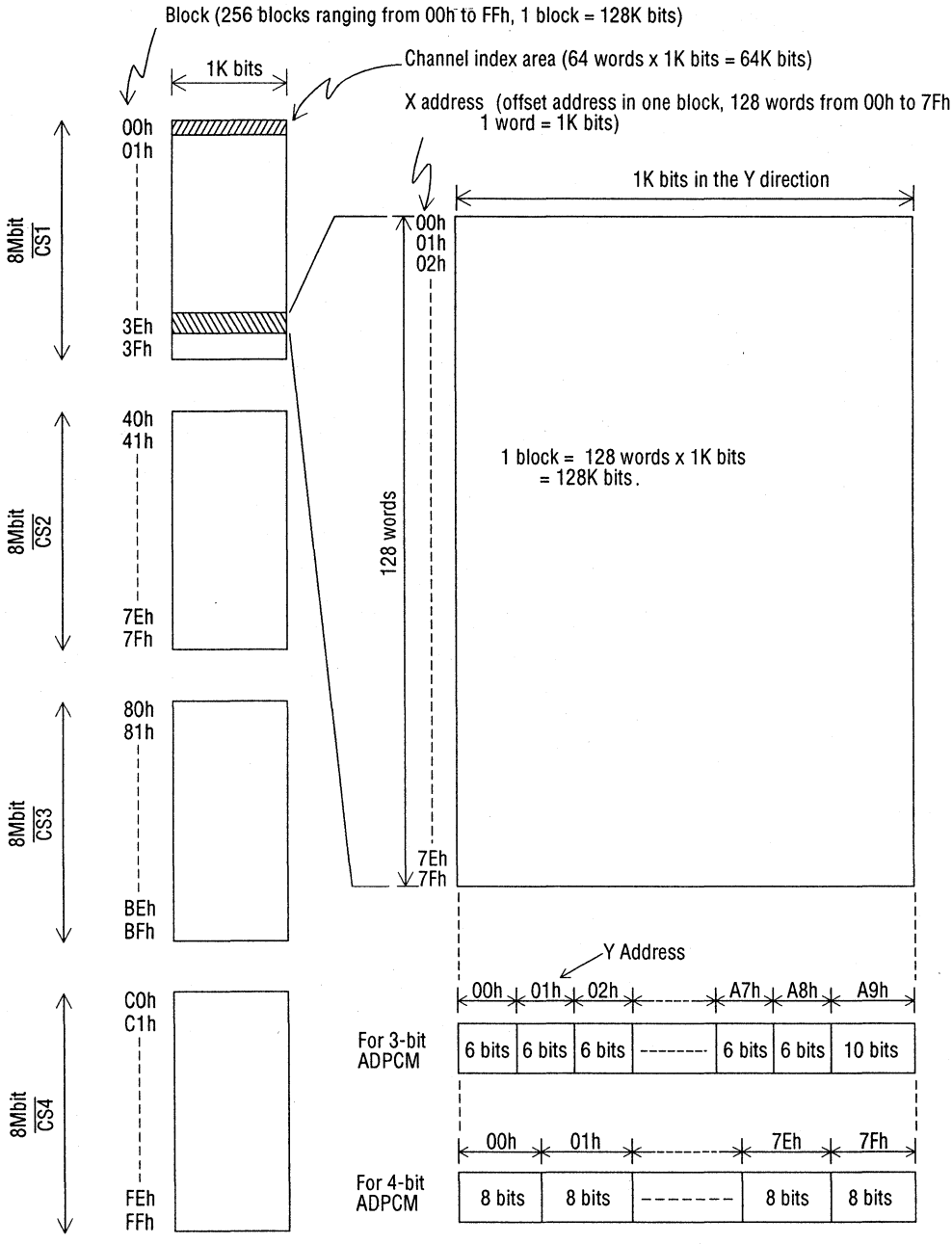
(1) For 3-bit ADPCM, (3 bits × 340 samples + unused 4 bits = 1024 bits) are stored in the 1k-bit memory area.

One Y address is allocated to two ADPCM data samples, so that Y addresses are addressable by 00–A9h

(2) For 4-bit ADPCM, (4 bits × 256 samples = 1024 bits) are stored in the 1K-bit memory area.

One Y address is allocated to two ADPCM data samples, so that Y addresses are addressable by 00–7Fh

Address Space Allocation of RAM
(Flex record/playback, 32M-bit)



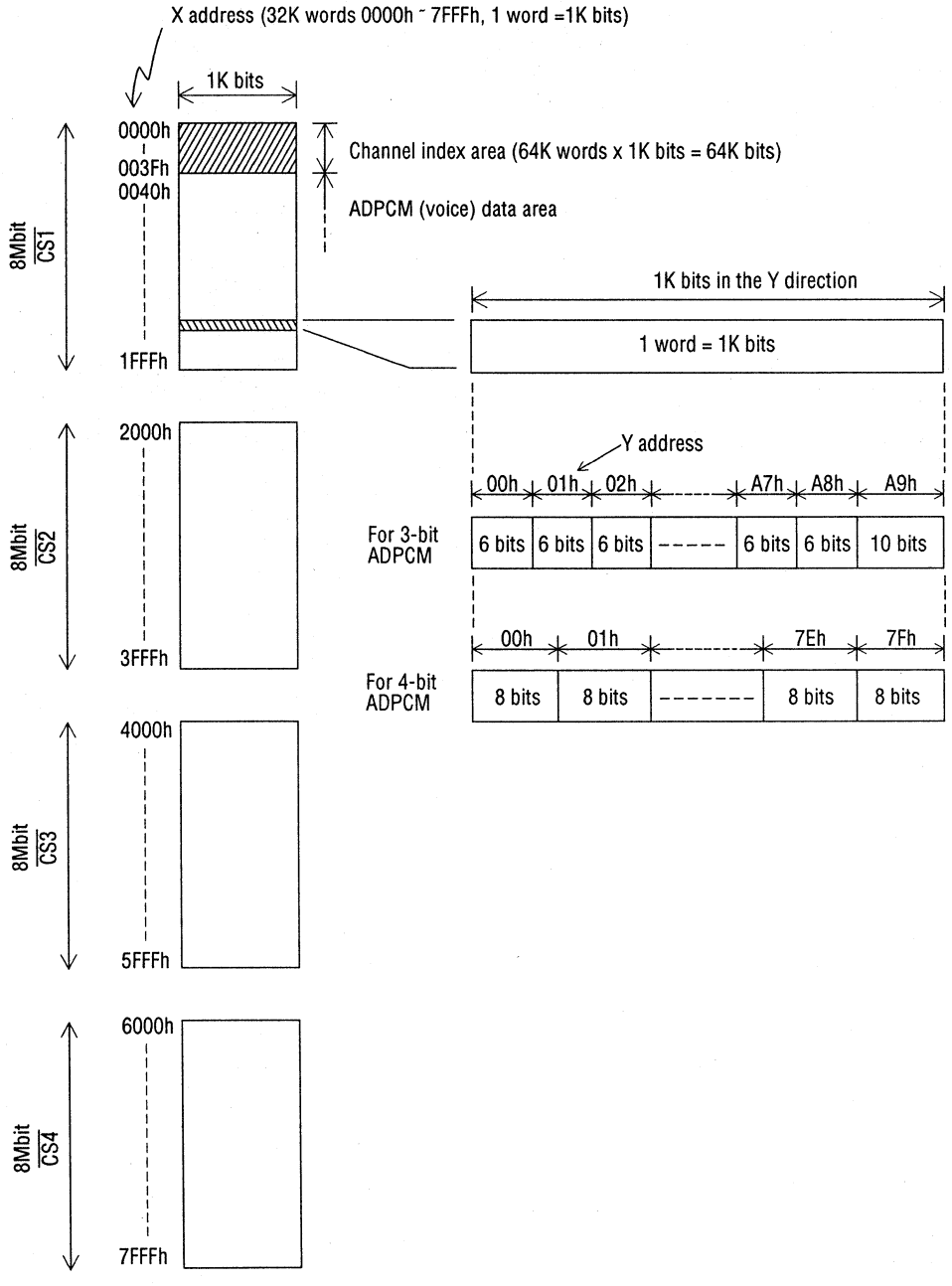
1.2 Address space allocation in the direct record/playback mode

In the direct record/playback mode, address control is performed by (X addresses in the word direction) x (1K bit depth in the Y direction). The maximum address of X addresses in the word direction varies depending on the total memory capacity of RAM externally connected. The header 64 words (64K bits) of the RAM are used as the channel index area. Therefore, addresses after X address 0040h can be used as the voice data area.

RSEL2	L	L	H	H
RSEL1	L	H	L	H
Total memory capacity	8M bits	16M bits	24M bits	32M bits
No. of words	8K words	16K words	24K words	32K words
X address	0000h ~ 1FFFh	0000h ~ 3FFFh	0000h ~ 5FFFh	0000h ~ 7FFFh

The storage method of 1K-bit ADPCM data in the Y direction is identical to that for the flex record/ playback mode. For 3-bit ADPCM data, the storage locations are addressable by 00h–A9h, For 4-bit ADPCM data, the storage locations are addressable by 00h–7Fh.

Address Space Allocation of RAM
(Direct record/playback)



2. Channel index area of serial registers

2.1 Channel index area in the flex record/playback mode

In the flex record/playback mode, the channel index area for one phrase (1K bits) consists of 64K-bit address data, 704-bit user data, and 256-bit address control block table. The address data consists of the number of blocks, stop Y address, stop X address, start block, stop block, and PRED block. In the following, these areas are summarized.

(1) Number of blocks: This area stores the number of blocks (recorded time) used for recording of one phrase. Address ch00 stores the number of unused blocks (available blocks). This number of blocks can be read by the BLKRD command. The recorded time for one phase and the unused capacity (available recording time) of memory can be obtained.

(2) Stop Y address: This area stores the stop Y address of the phrase. A Y address location is addressable by one of 00h–A9h for 3-bit ADPCM, and by one of 00h–7Fh for 4-bit ADPCM.

(3) Stop X address: This area stores the stop X address of a phrase. This X address is offset address of the block. One X address has a 1K-bit memory area. The memory capacity of one block varies depending on the number of serial registers connected externally, and addressing also varies accordingly.

(4) Start block and stop block: The total memory capacity of serial registers is equally divided into 256 blocks. Addresses 00h–FFh are assigned to these blocks. The start block and stop block are stored in the start block area and stop block area, respectively.

(5) PRED block: This area stores the address of a block immediately before the stop block. In the flex record/playback mode, each recording area is controlled on a per-block basis. Therefore, a phrase is not always stored continuously in serial registers. For example, if a phrase is recorded in three blocks 03h, 04h and 07h. The PRED block stores 04h. This PRED block is used to change the stop block and stop X address for deleting a tail part of the recorded phrase.

(6) User data: This user data area can be used by the user. The data can be written to and read from this area by the CHRW command.
This user data area is provided independently for each phrase, so that it is useful to store the sampling frequency, ADPCM bit length and recorded time.

(7) Block table: The block table is an area used for the block control.

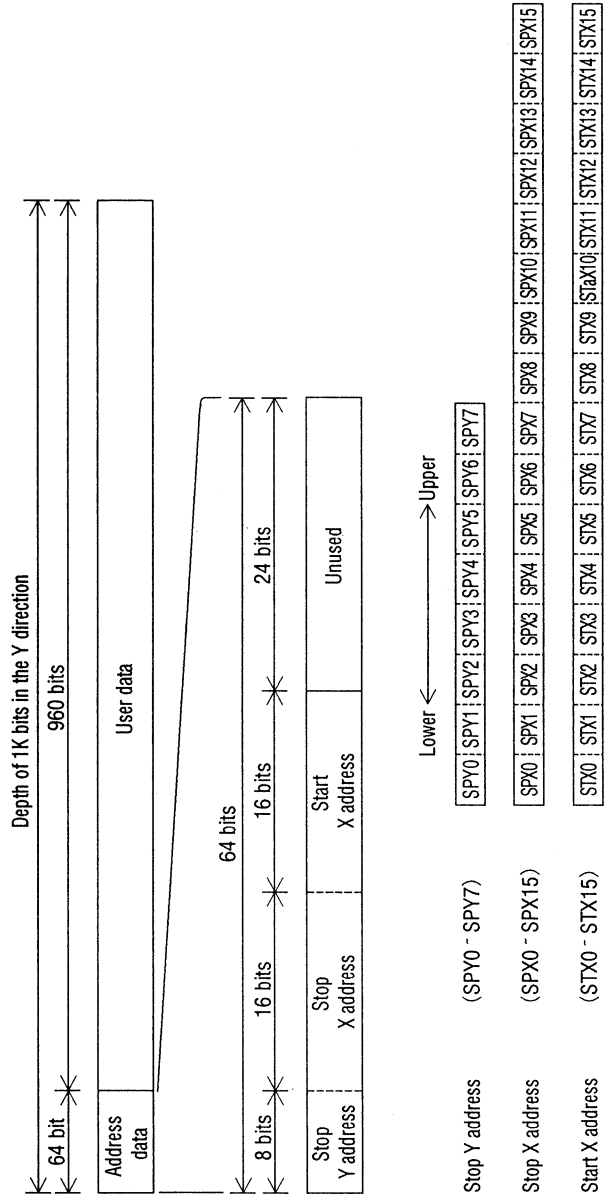
		Lower ← → Upper							
Number of blocks	(BL0 ~ BL7)	BL0	BL1	BL2	BL3	BL4	BL5	BL6	BL7
Stop Y address	(SPY0 ~ SPY7)	SPY0	SPY1	SPY2	SPY3	SPY4	SPY5	SPY6	SPY7
Stop X address	(SPX0 ~ SPX7)	SPX0	SPX1	SPX2	SPX3	SPX4	SPX5	SPX6	SPX7
Stop block	(SP0 ~ SP7)	SP0	SP1	SP2	SP3	SP4	SP5	SP6	SP7
PRED block	(PR0 ~ PR7)	PR0	PR1	PR2	PR3	PR4	PR5	PR6	PR7
Start block	(ST0 ~ ST7)	ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7

2.2 Channel index area in the direct record/playback mode

In the direct record/playback mode, the channel index area for one phrase (1K bits) consists of 64-bit address data and 960-bit user data. The address data consists of the stop Y address, stop X address, start X address, and unused area.

(1) Stop Y address: In the same manner as in the direct record/playback mode, the stop address can be specified by one of 00h–A9h for 3-bit ADPCM and 00h–7Fh for 4-bit ADPCM.
(2) Start X address and stop X address: An X address is specified by 16 bits (15 effective bits). The 32K-word X address space can be addressed by 000h–7FFFh.

(3) User data: In the same manner as in the direct record/playback mode, this user data area can be used by the user. The data can be written to and read from this area by the CHRW command.


Depth of 1K bits in the Y direction
960 bits
64 bit
Address data
User data
64 bits
8 bits
16 bits
16 bits
24 bits
Stop Y address
Stop X address
Start X address
Unused
Lower
Upper
Stop Y address (SPY0 - SPY7)
SPY0 SPY1 SPY2 SPY3 SPY4 SPY5 SPY6 SPY7
Stop X address (SPX0 - SPX15)
SPX0 SPX1 SPX2 SPX3 SPX4 SPX5 SPX6 SPX7 SPX8 SPX9 SPX10 SPX11 SPX12 SPX13 SPX14 SPX15
Start X address (STX0 - STX15)
STX0 STX1 STX2 STX3 STX4 STX5 STX6 STX7 STX8 STX9 STX10 STX11 STX12 STX13 STX14 STX15

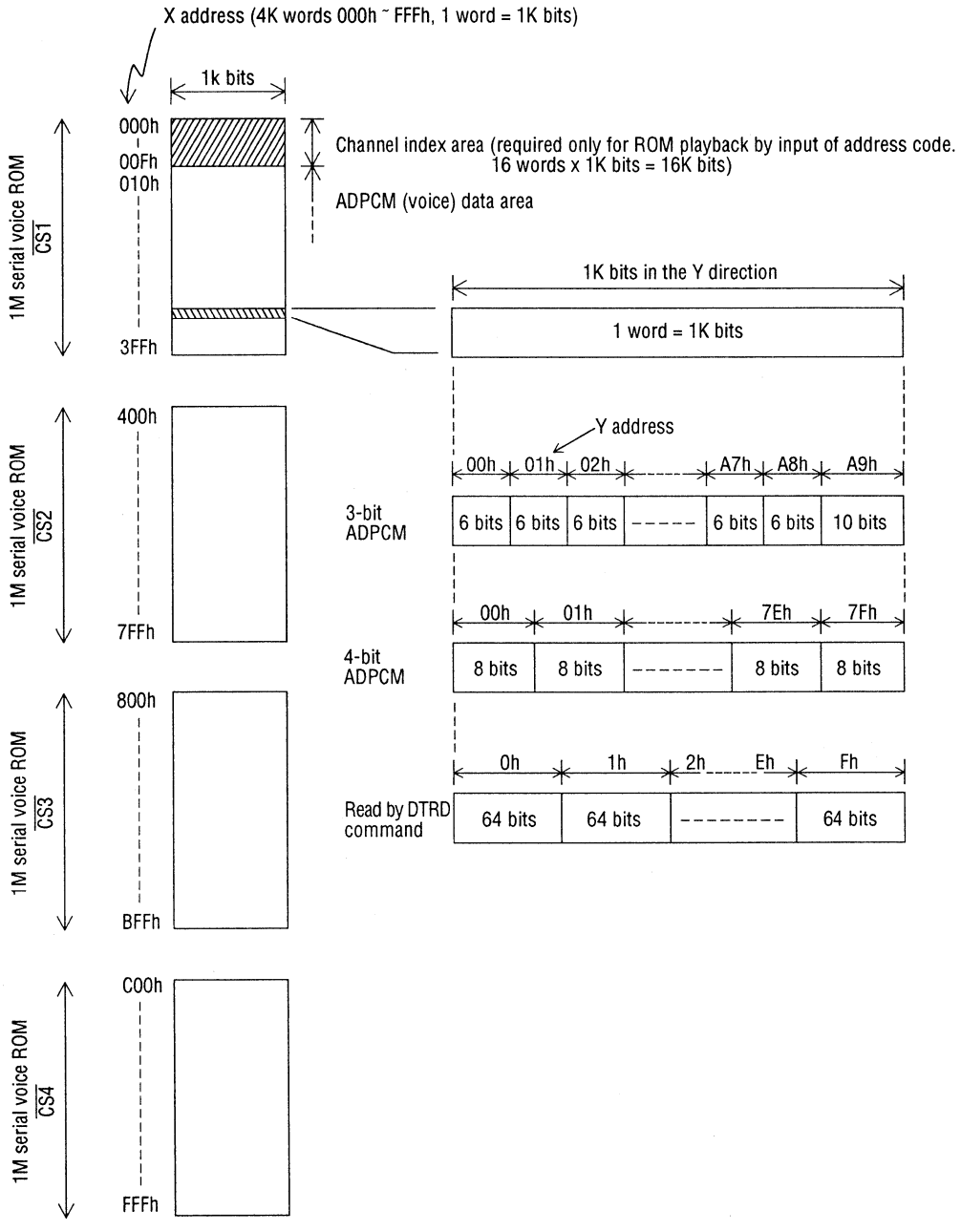
● Data Configuration of External Serial Voice ROMs

The external serial voice ROMs are composed of (X addresses in the word direction) × (depth of 1K bits). The addressing is possible only for X addresses in the word direction. The maximum address of the X addresses in the word direction varies depending on the total memory capacity of the serial voice ROMs externally connected. In the ROM playback by input of address code, the header 16 words (16K bits) are used as the channel index area, so that the addreses after address 010h can be used as the voice data area.

Total memory capacity (Number of ROMs)		1M bits (1)	2M bits (2)	3M bits (3)	4M bits (4)
ROM playback by input of address code	Number of words	1008 words	2032 words	3056 words	4080 words
	X address	010h ~ 3FFh	010h ~ 7FFh	010h ~ BFFh	010h ~ FFFh
Direct ROM playback DTRD command	Number of words	1024 words	2048 words	3072 words	4096 words
	X address	000h ~ 3FFh	000h ~ 7FFh	000h ~ BFFh	000h ~ FFFh

The method for storing the ADPCM data of 1K bits in the Y direction is identical to that for the record/playback mode.
Addressing can be made by 00h–A9h for 3-bit ADPCM and 00h–7Fh for 4-bit ADPCM.
When reading data in the serial voice ROMs by the DTRD command, specify the X address and Y address and then perform the read access operation. The address locations can be specified by 000h–FFFh in the same manner as in the ROM playback. The area of 1K bits in the Y direction is equally divided into 16 of 64K bits each, so that addressing can be performed by 0h–Fh.

Address space allocation of serial voice ROMs.



● Command Description

The MSM6688 is controlled by 19 types of commands via D0-D3 pins constituting the data bus and $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, and CE control pins. The state of the MSM6688 can be know by obtaining the contents of the internal status register via the data bus or the output pins.

There are four command modes available: mode 0, mode 1, mode 2, and mode 3.. Some commands need to set the command mode before inputting them. The command mode can be selected by setting MOD0 bit and MOD1 bit of the SAMP command.

1. Command list

Command	Code D3	D2	D1	D0	Command function	
NOP	0	0	0	0	(NON OPERATION).	Has no function.
PAUSE	0	0	0	1	(PAUSE).	Suspends record/playback temporarily.
PLAY	0	0	1	0	(PLAYBACK).	Sets playback mode.
REC	0	0	1	1	(RECORD).	Sets recording mode.
START	0	1	0	0	(START).	Starts record/playback.
STOP	0	1	0	1	(STOP).	Stops record/playback. Stops execution of CHRW, DTRW, DTRD, and EXT commands.
SAMP	0	1	1	0	(SAMPLING FREQUENCY).	Specifies the command mode and sampling frequency, in conjunction with 1 nibble following this command.
CHAN	0	1	1	1	(CHANNEL).	Specifies a phrase, in conjunction with 2 nibbles following this command.
BLKWR	1	0	0	0	(BLOCK WRITE).	Sets the number of recording blocks (recording time) for the phrase, in conjunction with 2 nibble following this command.
BLKRD	1	0	0	1	(BLOCK READ).	Reads the number of blocks (recording time) for the phrase stored in the channel index area, in conjunction with 2 nibbles following this command. During execution of this command, the contents of the status register cannot be read.
ADRWR	1	0	0	0	(ADDRESS WRITE).	Stores the start address and the stop address to the channel index area, in conjunction with 10 nibbles following this command.
ADRRD	1	0	0	1	(ADDRESS READ).	Reads out the start address and the stop address stored in the channel index area, in conjunction with 10 nibbles following this command. During execution of this command, the contents of the status register cannot be read.

Command	Code				Command function
	D3	D2	D1	D0	
CHRW	1	0	1	0	(CHANNEL READ WRITE). Reads out the user data stored in the channel index area or writes the user data to the channel index area by the read/write access operation following this command.
DTRW	1	0	1	0	(DATA READ WRITE). Transfers data to or from the external serial registers through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
DTRD	1	0	1	0	(DATA READ). Reads the data in the external serial voice ROMs through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
EXT	1	0	1	1	(EXTERNAL). Performs record/playback by inputting/outputting ADPCM data through the data bus, in conjunction with the read/write access operation. This command will be used when an SRAM or a hard disk is used for storing voice data. Does not control external serial registers and addresses.
VDS	1	1	0	0	(VOICE DETECT SELECT). Selects the ADPCM bit length and voice activated start function, in conjunction with 1 nibble following this command.
DEL	1	1	0	1	(DELETE). Deletes the phrase specified by the CHAN command. When ch00 is specified by the CHAN command, all phrases are deleted by this command.
LEV	1	1	1	0	(LEVEL) Specifies the playback output level and the transition of analog output (AOUT pin) to the DC level, in conjunction of 1 nibble following this command. This level is initialized by the RESET input.
NOP	1	1	1	1	(NON OPERATION). Has no function.

2. Command format

MOD1					0	0	1	1
MOD0					0	1	0	1
Code				HEX	Mode 0	Mode 1	Mode 2	Mode 3
D3	D2	D1	D0					
0	0	0	0	0h	NOP	NOP	NOP	NOP
0	0	0	1	1h	PAUSE	PAUSE	PAUSE	PAUSE
0	0	1	0	2h	PLAY	PLAY	PLAY	PLAY
0	0	1	1	3h	REC	REC	REC	REC
0	1	0	0	4h	START (Flex record/ playback)	START (ROM playback by input of address code)	START (Direct record/ playback)	START (Direct ROM playback)
0	1	0	1	5h	STOP	STOP	STOP	STOP
0	1	1	0	6h	SAMP	SAMP	SAMP	SAMP
0	1	1	1	7h	CHAN	CHAN	CHAN	CHAN
1	0	0	0	8h	BLKWR	BLKWR	ADRWR	ADRWR
1	0	0	1	9h	BLKRD	BLKRD	ADRRD	ADRRD
1	0	1	0	Ah	CHRW	CHRW	DTRW	DTRD
1	0	1	1	Bh	EXT	EXT	EXT	EXT
1	1	0	0	Ch	VDS	VDS	VDS	VDS
1	1	0	1	Dh	DEL	DEL	DEL	DEL
1	1	1	0	Eh	LEV	LEV	LEV	LEV
1	1	1	1	Fh	NOP	NOP	NOP	NOP

3. Command data format

Command	Code HEX		D3	D2	D1	D0	Note
NOP	0h		0	0	0	0	1-nibble command
PAUSE	1h		0	0	0	1	1-nibble command
PLAY	2h		0	0	1	0	1-nibble command
REC	3h		0	0	1	1	1-nibble command
START	4h		0	1	0	0	1-nibble command
STOP	5h		0	1	0	1	1-nibble command
SAMP	6h	1st nibble	0	1	1	0	2-nibble command
		2nd nibble	MOD1	MOD0	SA1	SA0	Command mode, sampling frequency

MOD1	MOD0	Command mode
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

SA1	SA0	Sampling frequency
0	0	f_{osc}/1024 (4.0kHz)
0	1	f_{osc}/768 (5.3kHz)
1	0	f_{osc}/640 (6.4kHz)
1	1	f_{osc}/512 (8.0kHz)

Values in parentheses are for fosc = 4.096 MHz.

CHAN	7h	1st nibble	0	1	1	1	3-nibble command
		2nd nibble	CA3	CA2	CA1	CA0	Phrase No.
		3rd nibble	CA7	CA6	CA5	CA4	

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.
0	0	0	0	0	0	0	0	ch00
0	0	0	0	0	0	0	1	ch01
0	0	0	0	0	0	1	0	ch02
0	0	0	0	0	0	1	1	ch03
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	chFE
1	1	1	1	1	1	1	1	chFF

Command	Code HEX		D3	D2	D1	D0	Note
BLKWR	8h	1st nibble	1	0	0	0	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
BLKRD	9h	1st nibble	1	0	0	1	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
ADRWR	8h	1st nibble	1	0	0	0	11-nibble command
		2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address
		3rd nibble	SPY7	SPY6	SPY5	SPY4	
		4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address
		5th nibble	SPX7	SPX6	SPX5	SPX4	
		6th nibble	SPX11	SPX10	SPX9	SPX8	
		7th nibble	SPX15	SPX14	SPX13	SPX12	
		8th nibble	STX3	STX2	STX1	STX0	Start X address
		9th nibble	STX7	STX6	STX5	STX4	
		10th nibble	STX11	STX10	STX9	STX8	
		11th nibble	STX15	STX14	STX13	STX12	
ADRRD	9h	1st nibble	1	0	0	1	11-nibble command
		2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address
		3rd nibble	SPY7	SPY6	SPY5	SPY4	
		4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address
		5th nibble	SPX7	SPX6	SPX5	SPX4	
		6th nibble	SPX11	SPX10	SPX9	SPX8	
		7th nibble	SPX15	SPX14	SPX13	SPX12	
		8th nibble	STX3	STX2	STX1	STX0	Start X address
		9th nibble	STX7	STX6	STX5	STX4	
		10th nibble	STX11	STX10	STX9	STX8	
		11th nibble	STX15	STX14	STX13	STX12	

Command	Code HEX		D3	D2	D1	D0	Note
CHRW	Ah		1	0	1	0	1-nibble command + read/write access + STOP command
DTRW	Ah	1st nibble	1	0	1	0	6-nibble command + read/write access + STOP command
		2nd nibble	0	0	0	0	Dummy nibble
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	X15	X14	X13	X12	
DTRD	Ah	1st nibble	1	0	1	0	6-nibble command + read access + STOP command
		2nd nibble	Y3	Y2	Y1	Y0	Y address
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	0	0	0	0	Dummy nibble
EXT	Bh		1	0	1	1	1-nibble command + read/write access + STOP command
VDS	ch	1st nibble	1	1	0	0	2-nibble command
		2nd nibble	0	BIT	VD1	VD0	ADPCM bit length, voice activation condition

BIT	ADPCM bit length
0	3 bits
1	4 bits

VD1	VD0	Voice detection level V_{VDS}
0	0	Voice activation disabled
0	1	±VDD/64 (±80mV)
1	0	±VDD/32 (±160mV)
1	1	±VDD/16 (±320mV)

Values in parentheses are for VDD = 5.12 V.

<table>
<tr><th>Command</th><th>Code HEX</th><th></th><th>D3 D2 D1 D0</th><th>Note</th></tr>
<tr><td>DEL</td><td>Dh</td><td></td><td>1 1 0 1</td><td>1-nibble command</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">ch00: Deletion of all phrases
ch01 ~ chFF: Deletion of a specified phrase</td></tr>
<tr><td>LEV</td><td>Eh</td><td>1st nibble</td><td>1 1 1 0</td><td>2-nibble command</td></tr>
<tr><td></td><td></td><td>2nd nibble</td><td>LV1 LV0 PN1 PN0</td><td>Playback level, transition to DC level</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">
<table>
<tr><th>LV1</th><th>LV0</th><th>Playback level</th></tr>
<tr><td>0</td><td>0</td><td>0dB</td></tr>
<tr><td>0</td><td>1</td><td>0dB</td></tr>
<tr><td>1</td><td>0</td><td>–6dB</td></tr>
<tr><td>1</td><td>1</td><td>–12dB</td></tr>
</table>
<table>
<tr><th>PN1</th><th>PN0</th><th>Transition to DC level</th></tr>
<tr><td>0</td><td>0</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>Disabled</td></tr>
<tr><td>1</td><td>0</td><td>Transition from GND to 1/2 VDD.</td></tr>
<tr><td>1</td><td>1</td><td>Transition from 1/2 VDD to GND.</td></tr>
</table>
</td></tr>
<tr><td>NOP</td><td>Fh</td><td></td><td>1 1 1 1</td><td>1-nibble command</td></tr>
</table>

4. Relationship between record/playback control modes and commands

Command \ Record/playback mode	Flex record/playback	ROM playback by input of address code	Direct record/playback	Direct ROM playback
NOP	—	—	—	—
PAUSE	○	○	○	○
PLAY	◎	—	◎	—
REC	◎	—	◎	—
START	◎	◎	◎	◎
STOP	○	○	○	○
SAMP	◎	◎	◎	◎
Command mode	◎	◎	◎	◎
Sampling frequency	◎	—	◎	◎
CHAN	◎	◎	◎	◎
BLKWR	◎	—	—	—
BLKRD	○	—	—	—
ADRWR	○	—	◎	◎
ADRRD	○	—	○	—
CHRW	Data transfer command			
DTRW	Data transfer command			
DTRD	Data transfer command			
EXT	Record/playback without use of serial registers			
VDS	◎	—	◎	◎
ADPCM bit length	◎	—	◎	◎
Voice activation condition	◎	—	◎	—
DEL	◎	—	○	—
Deletion of all phrases	◎	—	○	—
Deletion of a specified phrase	○	—	○	—
LEV	○	○	○	○

Note: ◎ : Required command ○ : Useful command — : Unnecessary command

● Status Register

The status register used in the MSM6688 is a 4-bit status register. When a low level is applied to the $\overline{RD}$ pin, the contents of the status register are output to D0–D3 pins to indicate the internal state of the MSM6688. The contents of the status register are also output to the BUSY, RPM, VPM, and NAR pins.

D3	D2	D1	D0
NAR	VPM	RPM	BUSY

(1) BUSY bit

The BUSY bit set to a high level indicates that the MSM6688 is executing RESET operation or command processing operation. When BUSY bit is high, do not input any command from the microcontroller. While any of data read commands is being executed, the state of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse. In this case, input a read command either after waiting a time longer than the duration of BUSY state or after verifying the end of the busy state by the BUSY pin.

While the RESET operation is being executed, the BUSY bit is set to a high level, and it returns to a low level after the end of the RESET operation. After a high level pulse is applied to the RESET pin to perform the RESET operation, the BUSY bit is set to a high level during execution of the RESET operation. It goes to a low level after the end of the RESET operation.

(2) RPM bit

The RPM bit goes to a high level during record/playback operation. While the RPM bit is high, do not input any command except those indicated below. Otherwise, the state of the MSM6688 becomes undefined.

NOP, PAUSE, STOP commands, START command for release of temporary stop and playback of next phrase, CHAN command for specifying the next phrase during playback and LEV command for designation of playback output level

After a high level pulses is applied to the RESET pin to perform the RESET operation, the RPM bit goes to a low level that is the initial state.

(3) VPM bit

The VPM bit goes to a high level during standby for voice after start of the voice activated recording and during the time that record/playback is temporarily stopped by the PAUSE command.

When the VPM bit is high, do not apply any command except the STOP command and the START command for release of temporary stop. Otherwise, the state of the MSM6688 becomes undefined.

After a high level pulse is applied to the RESET pin to perform the reset operation, the VPM bit goes to a low level that is the initial state.

(4) NAR bit

The NAR bit indicate the enabled or disabled state for phrase designation. When this bit is high, the phrase designation by the CHAN command is enabled.

If it is desired to play back different phrases continuously during ROM playback, specify the next phrase and input the START command after verifying that the NAR bit becomes high.

After a high level pulse is applied to the RESET pin to perform the reset operation, the NAR bit goes to a high level that is the initial state.

BUSY causing conditions	Symbol	BUSY state duration	BUSY bit verification	Note
Release of reset operation	t_{REX}	(Note 2) 1 ms	Possible	Input of RESET pulse
Input of 1-nibble command	t_{B1}	16 µs	Possible	NOP, PAUSE, PLAY, REC, START, STOP
Input of 2-nibble command	t_{B2}	16 µs	Possible	SAMP, VDS, LEV
Input of 3-nibble command	t_{B3}	16 µs	Possible	CHAN, BLKWR
Input of 2-nibble or 3-nibble command data	t_{BD}	16 µs	Possible	SAMP, VDS, LEV, CHAN, BLKWR
BLKRD command				
Input of command	t_{WBR}	270 ms	Impossible	
Output of block data	t_{WDR}	50 µs	Impossible	
ADRWR command				
Input of command	t_{BAW}	270 ms	Possible	
Input of address data	t_{BAD}	50 µs	Possible	
ADRRD command				
Input of command	t_{WAR}	270 ms	Impossible	
Output of address data	t_{WDR}	50 µs	Impossible	
CHRW command				
Input of command	t_{WCRW}	770 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
DTRW and DTRD commands				
Input of command	t_{WRW}	16 µs	Possible	
Input of address (2nd ~ 5th nibbles)	t_{WA1}	16 µs	Possible	
Input of address (6th nibble)	t_{WA2}	270 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
Input of DEL command (all phrases)	t_{WBLA}	550 ms	Possible	
Input of DEL command (a specified phrase)	t_{WBL1}	70 ms	Possible	

Note 1: The BUSY state can be verified by the BUSY bit when only the datawrite access operation is executed after the CHRW or DTRW command is input.

Note 2: The BUSY state duration after release of RESET operation includes the oscillation startup stabilization time. This oscillation startup stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

● Inputting the Commands

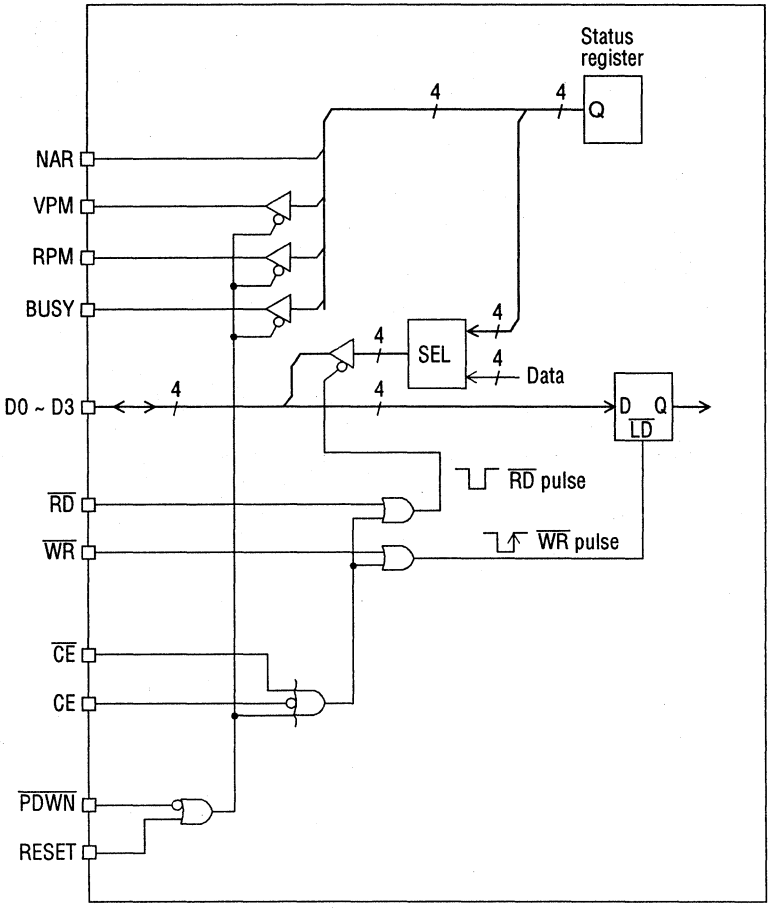
To input a command or data, apply the command or data to D0–D3 pins and then apply a low level pulse ($\overline{WR}$ pulse) to the $\overline{WR}$ pin.

By inputting a low level pulse ($\overline{RD}$ pulse) to the $\overline{RD}$ pin, the contents of the status register or data will be output via D0–D3 pins.

The $\overline{CE}$ pin is used to enable or disable the $\overline{WR}$ pulse and $\overline{RD}$ pulse. When a low-level is applied to this $\overline{CE}$ pin, the enable state is present, so that $\overline{WR}$ and $\overline{RD}$ pulses can be accepted. When a high level is applied to this $\overline{CE}$ pin, the disable state is present, so that $\overline{WR}$ and RD pulses cannot be accepted and, at the same time, D0–D3 pins are placed in the high-impedance state.

The CE pin also has the same function as the $\overline{CE}$ pin. However, when high, this CE pin gives the enable state for the $\overline{WR}$ and $\overline{RD}$ pulses, and when low, it gives the disable state. When D0–D3 pins are used exclusively for the MSM6688, $\overline{CE}$ and CE pins can be fixed to a low level and a high level, respectively.

An equivalent circuit of the microcontroller interface section of the MSM6688 is shown below.

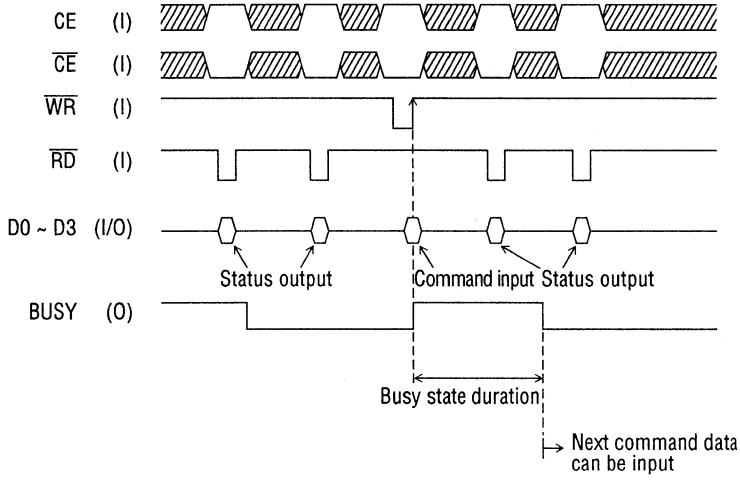

Status
register
4
4
Q
NAR
VPM
RPM
BUSY
4
4
SEL
4
Data
D0 ~ D3
4
4
D Q
LD
RD pulse
RD
WR pulse
WR
CE
CE
PDWN
RESET

The steps for inputting the commands are described below.

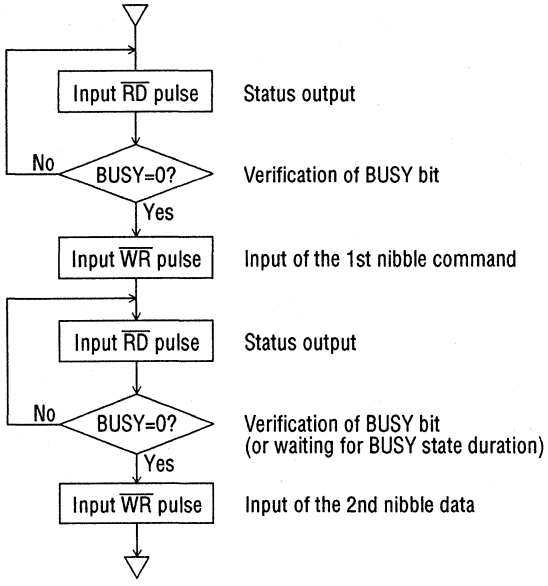
(1) Output the contents of the status register by applying the $\overline{RD}$ pulse (namely, by applying a low level pulse to the $\overline{RD}$ pin). Verify that the BUSY bit is 0. If the BUSY bit is 1, input the $\overline{RD}$ pulse repeatedly until the BUSY bit goes to 0. The BUSY state can also be verified through the BUSY pin.

(2) Set a command to D0–D3 pin and input the $\overline{WR}$ pulse.

(3) In case of a 2-nibble or 3-nibble command, verify that the BUSY bit of the status register is 0 in the same way as in (1). Then, set the command data to D0–D3 pins and input the $\overline{WR}$ pulse. In this case, the $\overline{WR}$ pulse can also be input after the waiting time that is longer than the BUSY state duration, instead of verifying the BUSY bit of the status register.



1. Inputting a 2-nibble command



● Changes of Record/Playback Conditions

Record/playback condition	POWER ON	RESET input	$\overline{\text{PDWN}}$ input	Command input
Record/playback mode	Undefined	Unchanged (Note 1)	Unchanged	REC command → Record mode PLAY command → Playback mode
Command mode	Undefined	Unchanged (Note 1)	Unchanged	Set by SAMP command
Sampling frequency	Undefined	Unchanged (Note 1)	Unchanged	Set by SAMP command
Phrase No.	Undefined	Unchanged (Note 1)	Unchanged	Set by CHAN command
Number of phrase recording blocks	Undefined	Unchanged (Note 1)	Unchanged	Set by BLKWR command
ADPCM bit length	Undefined	Unchanged (Note 1)	Unchanged	Set by VDS command
Voice activation	Undefined	Unchanged (Note 1)	Unchanged	Set by VDS command
Playback level	Undefined	0dB	Unchanged	Set by LEV command
Data in serial registers	Undefined	Unchanged (Note 1)	Unchanged	—

Note 1: RESET is performed without synchronization with the clock. When the RESET pulse is input during standby for commands, record/playback condition will not be changed. When the RESET pulse is input during execution of a command, all record/playback conditions may be changed and the data may become undefined.

● Setting and Confirming the Record/Playback Conditions

1. Specifying the control mode for record/playback (by the SAMP command)

Specify the control mode for record/playback by setting the command mode (using MOD1 and MOD0 bits) as shown in the following table.

MOD1	MOD0	Command mode	Control mode for record/playback
0	0	Mode 0	Flex record/playback
0	1	Mode 1	ROM playback by input of address code
1	0	Mode 2	Direct record/playback
1	1	Mode 3	Direct ROM playback

2. Specifying the sampling frequency (by the SAMP command)

Specify the sampling frequency by setting SA0 and SA1 bit data of the SAMP command. The relationship between the master oscillator frequency (f_{osc}), and sampling frequency (f_{SAMP}) depends on the SA0 and SA1 bit data of the SAMP command as shown in the following table.

SA1	SA0	Sampling frequency fsamp
0	0	f_{osc}/1024 (4.0kHz)
0	1	f_{osc}/768 (5.3kHz)
1	0	f_{osc}/640 (6.4kHz)
1	1	f_{osc}/512 (8.0kHz)

( ) Values in parentheses are for f_{osc}=4.096MHz.

3. Specifying the ADPCM bit length (by the VDS command)

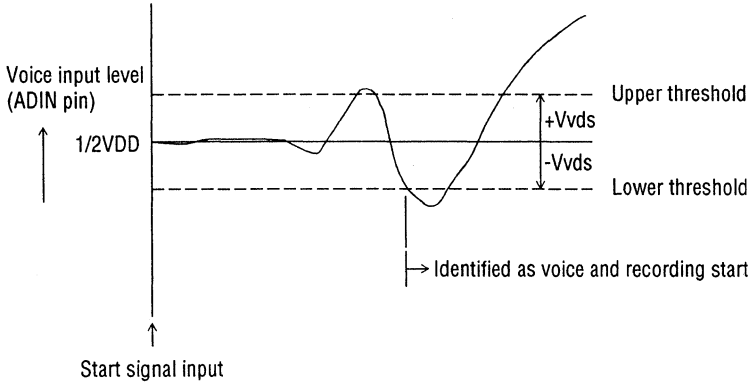
Specify the ADPCM bit length by setting the BIT bit data of the VDS command as shown in the following table.

BIT	ADPCM bit length
0	3 bit
1	4 bit

4. Specifying the voice activated recording condition (by the VDS command)

This MSM6688 has the voice activated recording function to start recording when the level of voice input exceeds a preset amplitude. Using the voice activated function, the unvoiced part prior to voice detection will not be recorded, so that the memory capacity can be utilized efficiently.

The unvoiced parts in the middle of recording are not eliminated. In the voice activated recording mode, recording is started when a voice input exceeds the preset thresholds. Therefore, a consonant part with a low level may not be recorded.

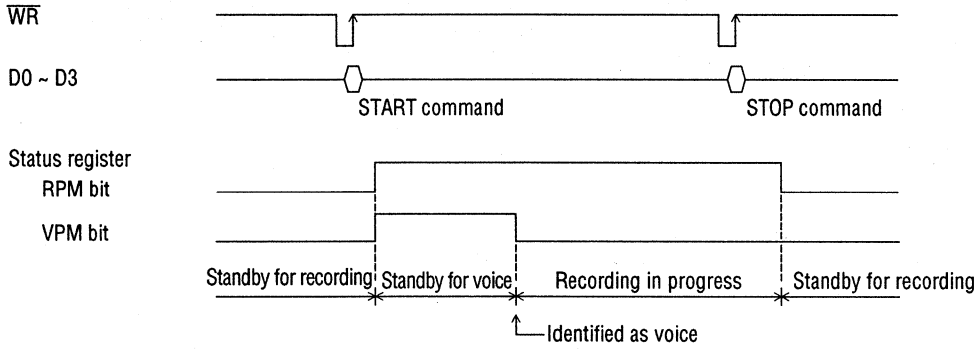


Specify the enable/disable of the voice activated recording function and the voice detection level by VD0 and VD1 bit data of the VDS command as shown in the following table.

VD1	VD0	Voice detection level, V_{vds}
0	0	Voice activation disabled
0	1	±VDD/64 (±80mV)
1	0	±VDD/32 (±160mV)
1	1	±VDD/16 (±320mV)

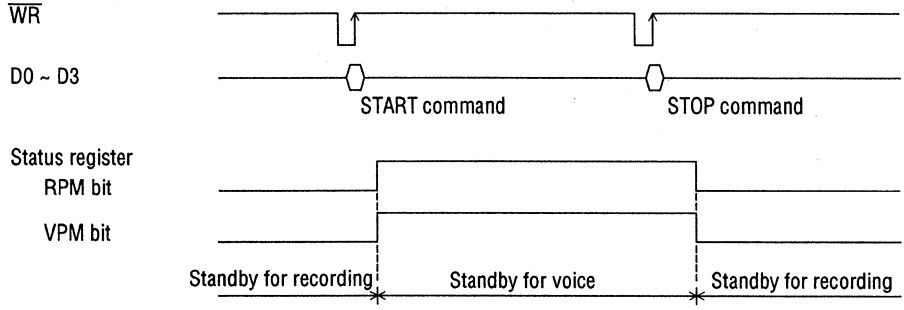
Values in parentheses are for VDD = 5.12 V

During standby for voice, the VPM bit of the status register is 1. This bit returns to 0 at the start of voice activated recording after detection of voiced signal. The RPM bit is 1 during standby for voice and during recording.



When the STOP command is input during standby for voice, standby for voice will be finished and changed to standby for recording,

If in the flex record/playback mode, the STOP command is input during standby for voice, the contents of the specified phrase will be deleted.



5. Specifying a phrase (by the CHAN command)

Specify a phrase by CA0–CA7 bit data of the CHAN command as shown in the following table.

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.	Flex record/ playback	ROM playback by input of address code	Direct record/ playback	Direct ROM playback
0	0	0	0	0	0	0	0	ch00	(Note 1)	Disabled	Enable (64 phrases)	Enable (Note 2)
0	0	0	0	0	0	0	1	ch01	Enable (63 phrases)	Enable (255 phrases)		
0	0	0	0	0	0	1	0	ch02				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
0	0	1	1	1	1	1	0	ch3E				
0	0	1	1	1	1	1	1	ch3F				
0	1	0	0	0	0	0	0	ch40	Inhibit		Inhibit	Inhibit
0	1	0	0	0	0	0	1	ch41				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮				
1	1	1	1	1	1	1	0	chFE				
1	1	1	1	1	1	1	1	chFF				

Note 1: In the flex record/playback mode, ch00 cannot be used for recording/playback. This is a special phrase only used for deletion of all phrases and control of unused blocks.

Note 2: In the direct ROM playback mode, playback will be started after transferring the address data to the channel index area of the serial registers. Therefore, it is required for direct ROM playback to use a phase unused for record/playback operation. Normally, phrase ch3FH is used as the phrase dedicated for direct ROM playback.

6. Specifying the number of phrase recording blocks (by the BLKWR command)

In the flex record/playback mode, set the number of blocks before starting the recording to specify the recording time for a phrase. In this mode, the total memory capacity of serial registers connected externally is divided equally into 256 blocks. Therefore, the memory capacity of one block varies depending on the number of serial registers connected externally.

For example, when one 8M bit serial register is connected and recording is performed by 4-bit ADPCM and 8-kHz sampling, the memory capacity of one block and the recording time of one block are obtained as follows.

$$\text{Memory capacity of one block} = \frac{8\text{M bits}}{256} = 32\text{K bits}$$

$$\text{Recording time/block} = \frac{\text{Memory capacity of one block}}{\text{Sampling frequency} \times \text{ADPCM bit length}}$$

$$= \frac{32 \times 1024 \times \text{bits}}{8000\ \text{Hz} \times 4\ \text{bits}} = \text{Approximately 1 second}$$

If it is desired to make recording for 10 seconds on a phrase in this example, 10 (0Ah) phrase recording blocks are required.

The number of phrase recording blocks can be specified by the BLKWR command and is stored in the (corresponding) register in the MSM6688. The BLKWR command is enabled for command mode 0 or 1. Therefore, before inputting this BLKWR command, it is required to set the corresponding command mode using the SAMP command.

BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	Number of phrase recording blocks (HEX)
0	0	0	0	0	0	0	0	Input inhibit
0	0	0	0	0	0	0	1	1 (01h)
0	0	0	0	0	0	1	0	2 (02h)
0	0	0	0	0	0	1	1	3 (03h)
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	254 (FEh)
1	1	1	1	1	1	1	1	255 (FFh)

7. Reading the number of phrase recording blocks (by the BLKRD command)

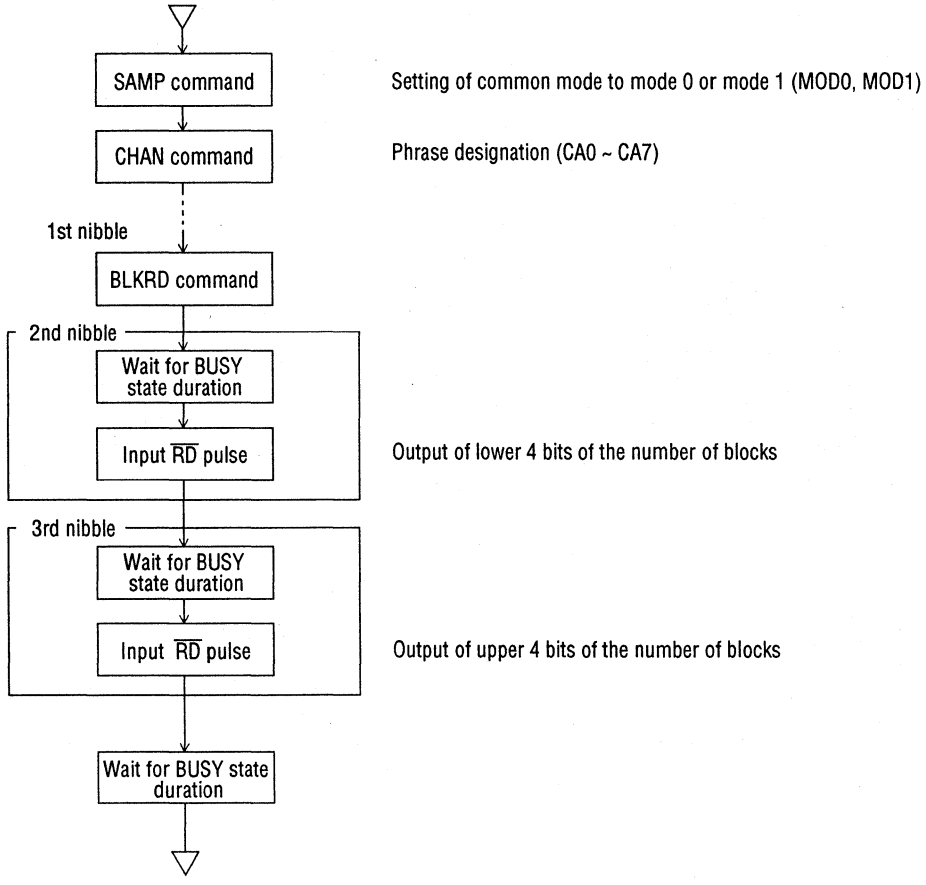
The number of blocks for each phrase stored in the channel index area can be read by the read access operation using the BLKRD command and two nibbles following this BLKRD command. In the flex record/playback mode, the number of blocks (namely, the recording time) of the specified phrase can be obtained. In the BLKRD command, the number of blocks is specified by a binary number consisting of BL0–BL7 in the same way as in the BLKWR command.

Before inputting the BLKRD command, the command mode must be set to either mode 0 or mode 1 by using the SAMP command.

(1) When ch00 phrase is specified: The number of unused blocks (or available blocks) is stored in address ch00 of the channel index area. Therefore, the unused and available memory capacity (or available recording time) can be obtained.

(2) When one of ch01–ch3F is specified as a phrase: The number of blocks (or recording time) used by the specified phrase can be obtained.

BLKRD command flow chart



During execution of the BLKRD command, verification of the status register cannot be performed by input of the $\overline{RD}$ pulse. When inputting the $\overline{RD}$ pulse for the 2nd nibble or 3rd nibble or inputting the next command after the BLKRD command, input the $\overline{RD}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

8. Inputting/outputting the address data (by the ADRWR/ADRRD command)

In the direct record/playback mode or direct ROM playback, input the start address and stop address of a phrase directly into the channel index area in the RAM by the ADRWR command.

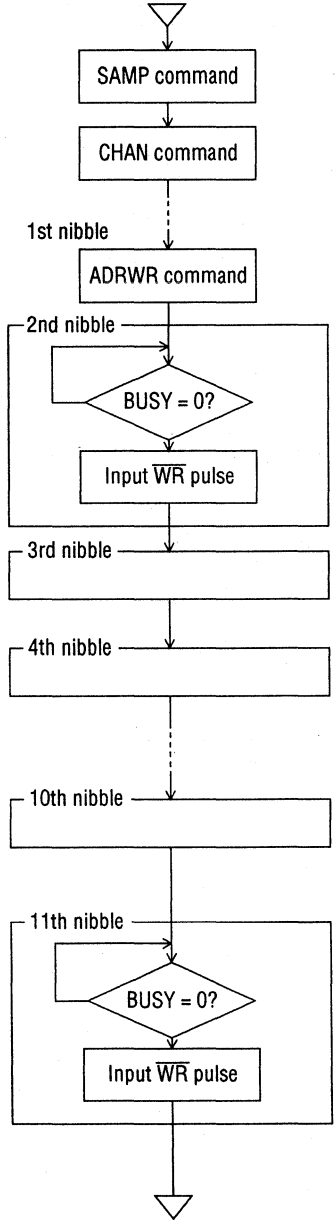
The ADRRD command is used to read the address data stored in the channel index area.

The header 40 bits of each phrase of the channel index area can be accessed by the ADRWR or ADRRD command. In the flex record/playback mode, these commands can be used to change the address data for deleting the tail part of a recorded phrase.

	Direct record/playback and direct ROM playback					Flex record/playback				
	D3	D2	D1	D0	Contents	D3	D2	D1	D0	Contents
1st nibble	1	0	0	*	Command	1	0	0	*	Command
2nd nibble	SPY3	SPY2	SPY1	SPY0	Stop Y address	BL3	BL2	BL1	BL0	Number of blocks
3rd nibble	SPY7	SPY6	SPY5	SPY4		BL7	BL6	BL5	BL4	
4th nibble	SPX3	SPX2	SPX1	SPX0	Stop X address	SPY3	SPY2	SPY1	SPY0	Stop Y address
5th nibble	SPX7	SPX6	SPX5	SPX4		SPY7	SPY6	SPY5	SPY4	
6th nibble	SPX11	SPX10	SPX9	SPX8		SPX3	SPX2	SPX1	SPX0	Stop X address
7th nibble	SPX15	SPX14	SPX13	SPX12		SPX7	SPX6	SPX5	SPX4	
8th nibble	STX3	STX2	STX1	STX0	Start X address	SP3	SP2	SP1	SP0	Stop block
9th nibble	STX7	STX6	STX5	STX4		SP7	SP6	SP5	SP4	
10th nibble	STX11	STX10	STX9	STX8		PR3	PR2	PR1	PR0	PRED block
11th nibble	STX15	STX14	STX13	STX12		PR7	PR6	PR5	PR4	

Note: When the address data is input by the ADRWR command in the direct ROM playback mode, the 7th nibble and the 11th nibble are dummy nibbles. Therefore, input 0h data into SPX12–SPX15 (7th nibble) and STX12–STX15 (11th nibble).

ADRWR command flow chart



Setting of command mode to mode 2 or mode 3 (MOD = 1)

Phrase designation(CA0 ~ CA7)

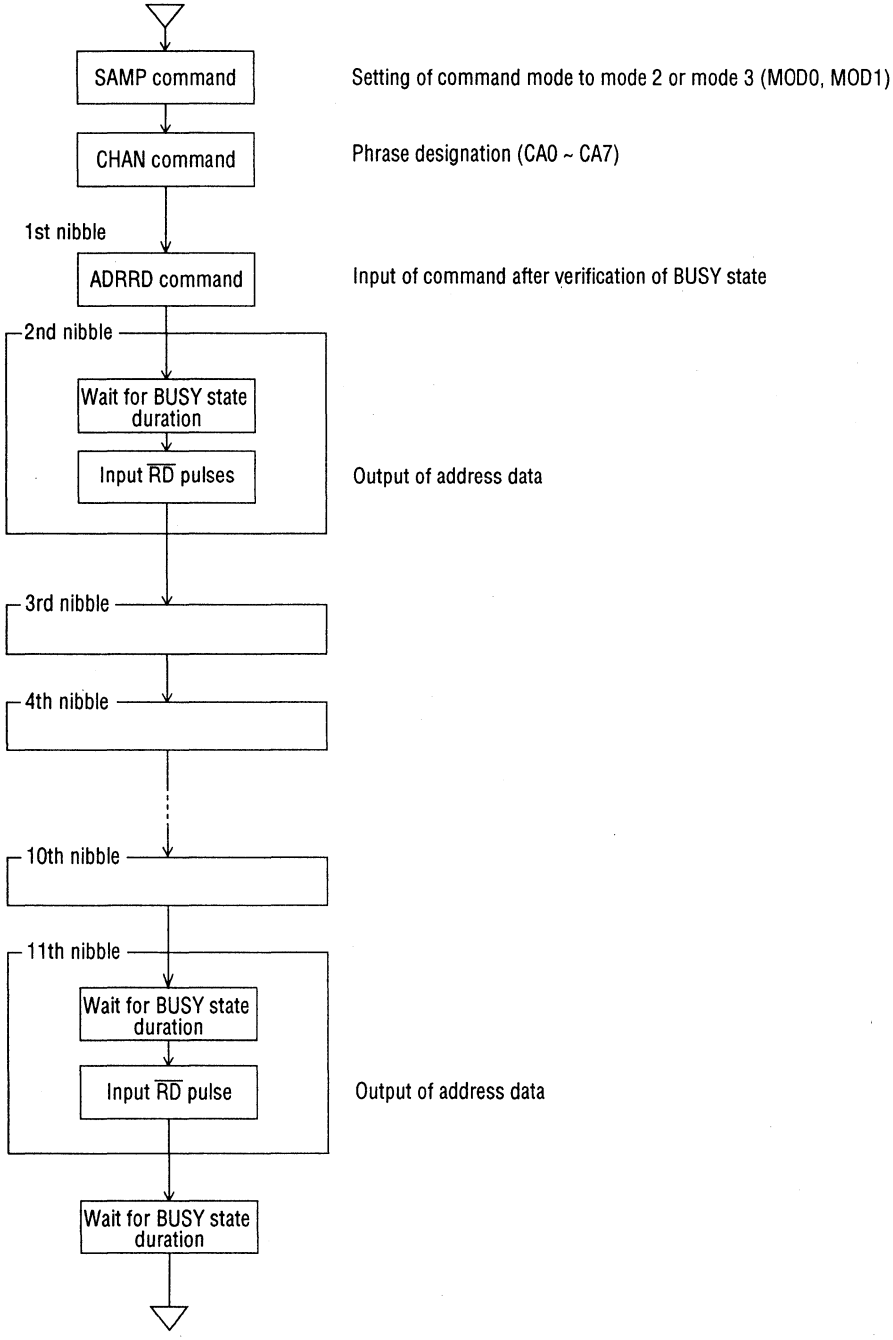
Input of command after verification of BUSY state

BUSY bit verification
(or waiting for BUSY state duration or longer)

Input of address data

Verification of address data

ADDRD command flow chart



During execution of the ADRRD command, verification of the status register cannot be performed by input of the $\overline{RD}$ pulse. When inputting the $\overline{RD}$ pulse for the 2nd nibble to 11th nibbles or inputting the next command after the ADRRD command, input the $\overline{RD}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

9. Specifying the playback level (by the LEV command)

For playback, one of three output levels 0 dB, –6 dB and –12 dB can be selected. The playback level can be specified by LV0 and LV1 bit data of the LEV command. If the LEV command is input during playback operation, the playback level will be changed at the moment when the command is input. When the RESET pulse is input, the playback output level is set 0 dB that is the initial state.

LV1	LV0	Playback level
0	0	0dB (equal to the voice data amplitude)
0	1	0dB (equal to the voice data amplitude)
1	0	−6dB (one-half of the voice data amplitude)
1	1	−12dB (one-fourth of the voice data amplitude)

● Flex Record/Playback Method

1. Deleting phrases

1.1 Deleting all phrases

To delete all phrases, specify ch00 by the CHAN command and input the DEL command. When all phrases are deleted in this manner, "0" data is written into ch01–ch3F addresses of the channel index area of the serial registers to place these addresses in the unrecorded state. The initial data for address control is written in ch00 address. Therefore, whenever the power is turned on, always perform the deletion of all phrases after inputting the RESET pulse.

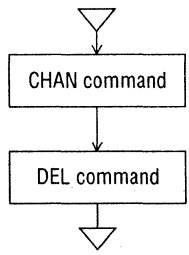
The deletion of all phrases causes the user data area ch00–ch3F to be cleared to all 0s. Note that when the data was transferred to the channel index area by the CHRW command, this data is deleted by the deletion of all phrases.

Phrases No.	State of the channel index area		
	Address data	User data	Block table
ch00:	Initial data	Cleared to all 0s	Initial data
ch01~ch3F	Cleared to all 0s		

1.2 Deleting a specified phrase

To delete a specified phrase, specify one of ch0–ch3F by the CHAN command and input the DEL command. The deleted phrase is placed in the unrecorded state. The channel index area for the specified phrase, including the user data, is cleared to all 0s. The data stored in ch00 address for control of unused blocks is updated.

Phrase deletion flow chart



ch00 Deletion of all phrases
ch01 ~ ch3F: Deletion of a specified phrase

2. Method of recording in the flex record/playback mode

(1) Before starting the recording operation in the flex record/playback mode, always perform the deletion of all phrases after turning power on and resetting the MSM6688 by input of the RESET pulse. Otherwise, the address control cannot be performed correctly.

(2) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT) and voice activation condition (VD0, VD1).

SAMP command: Set the command mode to mode 0 (MOD0 = 0, MOD1=0) and specify the sampling frequency (SA0, SA1).

CHAN command: Select phrases (CA0 ~ CA5) from one of 63 phrases ch01–ch3F.

BLKWR command: Specify the number of phrase recording blocks (BL0–BL7)

REC command: Set to the recording mode.

(3) Input the START command to start recording

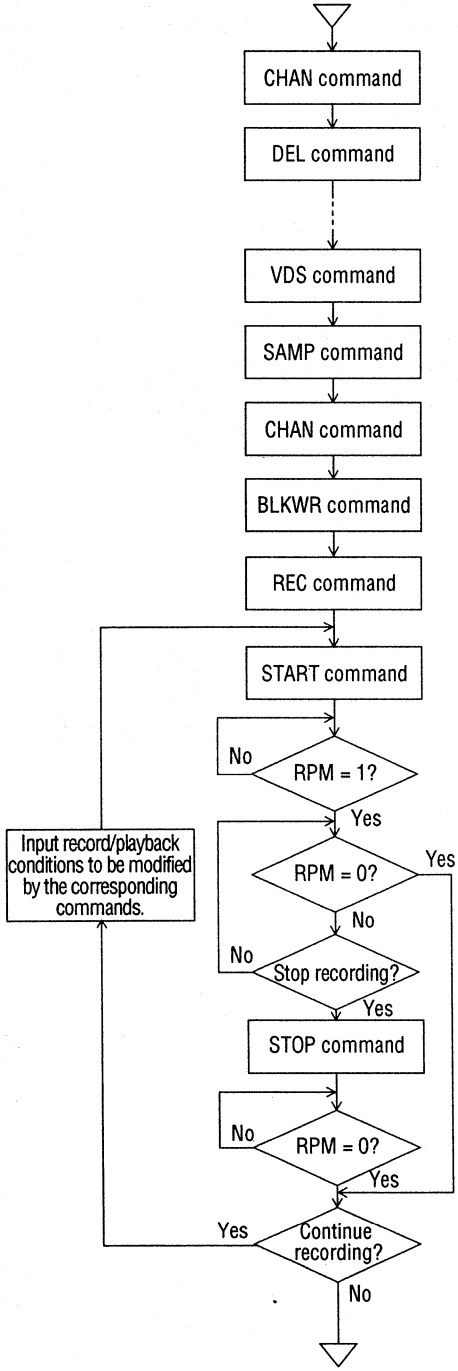
(4) When the number of blocks specified by the BLKWR command is reached or when all available blocks are used for recording, recording is finished. The end of recording can be verified by the RPM bit of the status register.

(5) To stop recording in the middle, input the STOP command. The contents of the block counter and the contents of the address counter at this moment are automatically stored in the channel index area as the stop block and the stop address, respectively.

In this case, make sure that recording is finished by examining the RPM bit before inputting the next command.

(6) To continue recording, specify the record/playback conditions to be modified by the corresponding commands and perform the steps (3)–(5).

Flow chart of flex recording in the record/playback mode



Specify ch00.

Delete all phrases.

ADPCM bit length (BIT)
Voice activation condition (VD0, VD1)

Set the command mode to mode 0 (MOD0 =0, MOD1 = 0).
Specify the sampling frequency (SA0, SA1).

Select one of 63 phrases (CA0 ~ CA5).

Set the phrase recording time (BL0 ~ BL7).

Set the recording mode.

Start of recording

Verify the start of recording.

Verify the end of recording.

Stop of recording

Verify the end of recording.

3. Playback method in the flex record/playback mode

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT)
The voice activation condition (VD0, VD1) is invalid for the playback operation.

SAMP command: Set the command mode to mode 0 (MOD0 = 0, MOD1= 0) and specify the sampling frequency (SA0, SA1).

CHAN command: Select one of 63 phrases ch01–ch3F (CA0–CA5).

LEV command: Specify the playback output level (LV0, LV1).

PLAY command: Set to the playback mode.

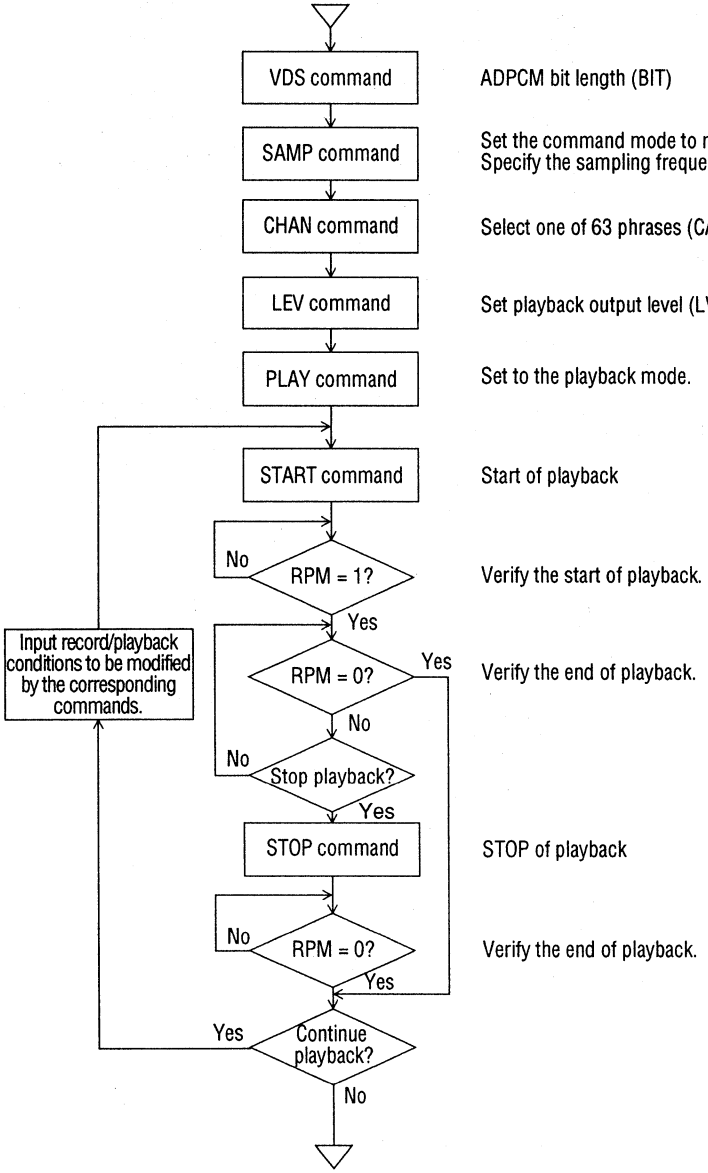
(2) Input the START command to start the playback. The MSM6688 fetches the contents of the block table and the stop address of the specified phrase from the channel index area and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of playback in the flex record/playback mode



This flow chart can apply to the playback operation in the direct record/playback mode, excluding that the command mode is set to mode 2 by the SAMP command and one of 64 phrases (ch00–ch3F) can be selected by the CHAN command in the direct record/playback mode.

● Direct Record/Playback Method

1. Recording method in the direct record/playback mode

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT) and voice activation condition (VD0, VD1).

SAMP command: Set the command mode to mode 2 (MOD = 0, MOD = 1) and specify the sampling frequency (SA0, SA1).

CHAN command: Select one of 64 phases ch00–ch3F (CA0–CA5).

ADRWR command: Input the start address and the stop address.

REC command: Set to the recording mode.

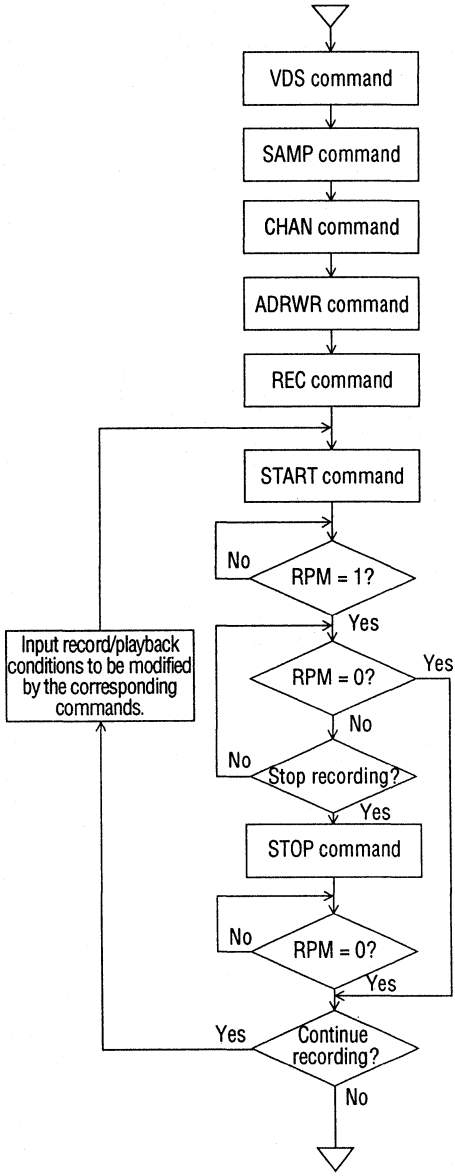
(2) Input the START command to start the recording. The MSM6688 fetches the start address and the stop address of the specified phrase input by the ADRWR from the channel index area and stores them in the address counter and the stop address register, respectively. Then it starts recording.

(3) When the contents of the address counter coincide with the contents of the stop address register, recording is finished. Verity the end of recording by the RPM bit of the status register.

(4) To stop recording in the middle, input the STOP command. In this case, the contents of the address counter is automatically stored in the channel index area as a new stop address. Make sure that recording is finished by examining the RPM bit before inputting the next command.

(5) To continue recording, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of recording in the direct record/playback mode



ADPCM bit length (BIT)
Voice activation condition (VD0, VD1)

Set the command mode to mode 2 (MOD0 = 0, MOD1 = 1).
Specify the sampling frequency (SA0, SA1).

Select one of 64 phrases (CA0 ~ CA5).

Input the start address and stop address.

Set the recording mode.

Start of recording

Verify the start of recording.

Verify the end of recording.

Stop of recording.

Verify the end of recording.

2. Playback method in the direct record/playback mode

The playback method in the direct record/playback mode is similar to that in the flex record/playback mode, excepting that in the direct playback mode, the command mode is specified to mode 2 by the SAMP command and a phrase can be selected from a total of 64 phrases (ch00~ch3F)by the CHAN command.

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT)
The voice activation condition (VD0, VD1) is invalid for the playback operation.

SAMP command: Set the command mode to mode 2 (MOD = 0, MOD = 1) and specify the sampling frequency (SA0, SA1).

CHAN command: Select one of 64 phrases ch00–ch3F (CA0–CA5).

LEV command: Specify the playback output level (LV0, LV1).

PLAY command: Set the playback mode.

(2) Input the START command to start the playback. The MSM6688 fetches the start address and the stop address of the specified phrase from the channel index area and stores them in the address counter and the stop address register, respectively. Then it starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

For the flow chart, refer to the flow chart of record/playback in the flex record/playback mode.

● ROM Playback by Inputting of Address Code

1. Method inputting commands

(1) Input the record/playback conditions by the corresponding commands as follows.

SAMP command: Set the command mode to mode 1 (MOD0 = 1, MOD1= 0). The sampling frequency (SA0, SA1) is invalid.

CHAN command: Select one of 255 phrases ch01–chFF (CA0–CA7).

LEV command: Specify the playback output level (LV0, LV1)

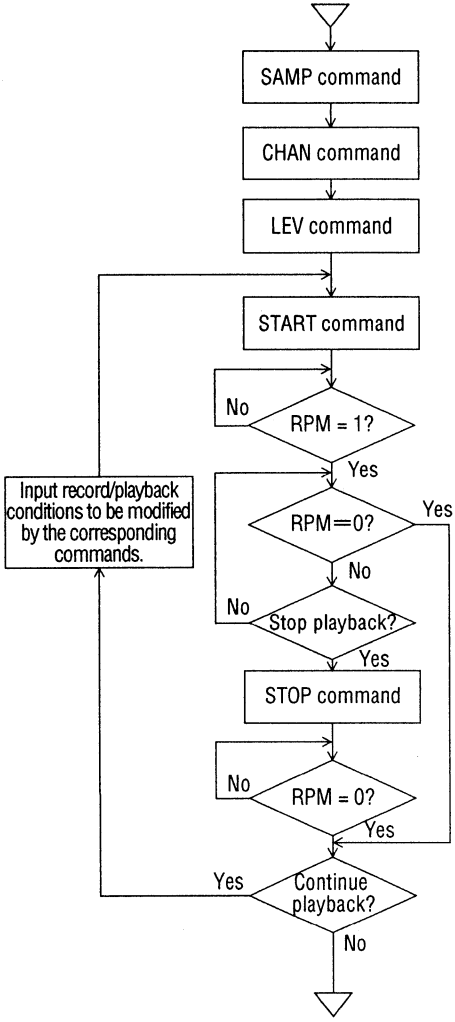
(2) Input the START command to start the playback. The MSM6688 fetches the data of the start address, stop address, sampling frequency, and ADPCM bit length of the specified phrase from the channel index area of the serial voice ROMs and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)–(4).

Flow chart of ROM playback by Input of Address Code



Set the command mode to mode 1 (MOD0 = 1, MOD1 = 0).

Select one of 255 phrases (CA0 ~ CA7)

Set playback output level (LV0, LV1).

Start of playback

Verify the start of playback.

Verify the end of playback.

STOP of playback

Verify the end of playback.

2. Continuous ROM playback

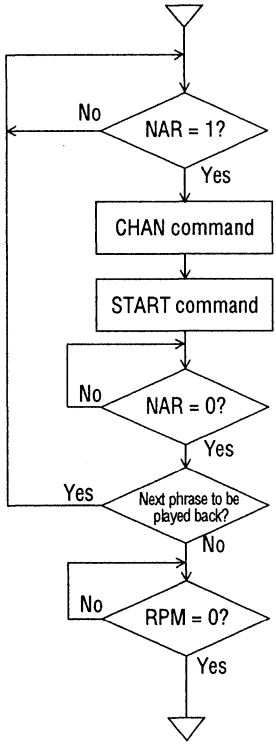
The procedure for playback of different phrases such as the time signal continuously is described below. The command inputting procedure for continuous ROM playback is basically equal to that for a single phrase. In this case, during playback of a phrase, the next phrase to be played back can be specified by the NAR bit of the status register. Continuous playback can also be performed by verifying the end of playback of each phrase using the RPM, instead of use of the NAR bit. To make continuous playback using NAR bit perform the following procedure.

(1) Specify a phrase by the CHAN command and input the START command to start playback. When the START command is accepted, the NAR bit of the status register goes to 0.

(2) When the NAR bit is changed from 0 to 1 to indicate that the next phrase can be specified and inputted, specify the next phrase to be played back by the CHAN command and input the START command. After the START command is accepted, the NAR bit goes to 0 again.

(3) In the same way as mentioned above, repeat the designation of a phrase and input of the START command verifying the state of the NAR bit.

Flow chart of continuous ROM playback



Verify whether a phrase can be specified or not.

Specify one of 255 phrases (CA0 ~ CA7).

The specified phrase is accepted.

Verify whether playback of the specified phrase is accepted or not.

Verify the end playback.

● Direct ROM Playback Method

MSM6688 playbacks serial voice ROM code products for the MSM6388/MSM6588ADPCM solid-state recorders, use the direct ROM playback mode.

The channel index area is not provided at the header area of these serial voice ROMs. Therefore, it is required to prepare an ROM in the microcontroller or an external ROM to store the start and stop addresses, sampling frequency, and ADPCM bit length of each phrase.

The start address and stop address of each phrase consists of 32 bits. These addresses are indicated in the voice address corresponding list of the serial voice ROM.

For example, the addresses to provide the "Message + Cattle Voice (English)" are as shown in the following table.

	Voice words	Start X address STX11 ~ STX0	Stop X address SPX11 ~ SPX0	Stop Y address SPY7 ~ SPY0	Sampling frequency fs	ADPCM bit length
No. 1	Message + Cattle Voice (English)	000h	010h	5Dh	6.4kHz	4bit

Before starting playback, the address data must be transferred to the channel index area of the status register using the ADRWR command. In this case, a phrase that is not used for record/playback must be specified for this direct ROM playback using the CHAN command. When recording a phrase in the flex record/playback mode, ch00 is inhibited to specify. Normally, ch3F address is used as the phrase dedicated for direct ROM playback.

(1) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Specify the ADPCM bit length (BIT).
The voice activation condition (VD0, VD1) is invalid for the playback operation.

SAMP command: Set the command mode to mode 3 (MOD1 = 1, MOD0 = 1) and specify the sampling frequency (SA0, SA1).

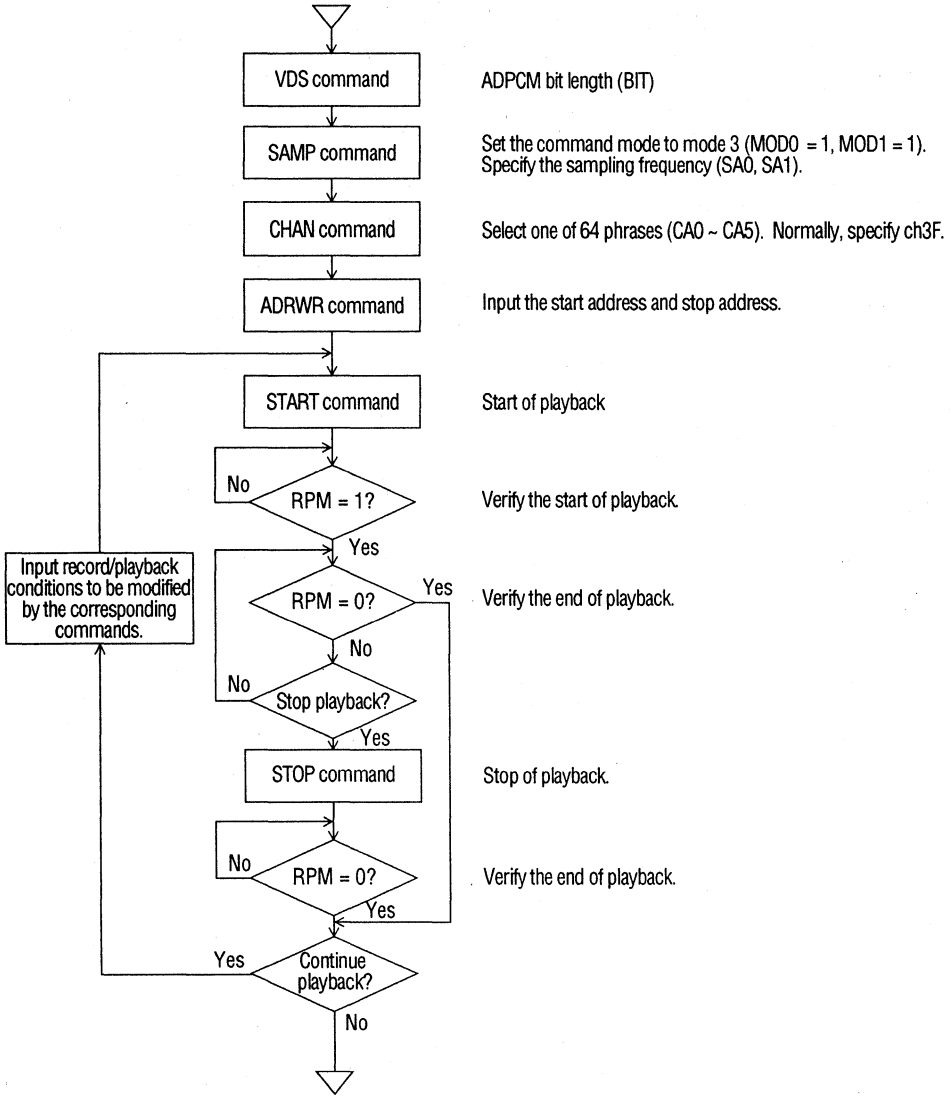
CHAN command: Select one of 64 phrases ch00–ch3F (CA0–CA5). Normally ch3F is used for direct ROM playback

ADRWR command: Specify the start and stop addresses.

(2) Input the START command to start the ROM playback. The MSM6688 fetches the start address and the stop address of the specified phrase from the channel index area of the serial registers. Then it starts the playback operation.

(3) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit.

Flow chart of direct ROM playback

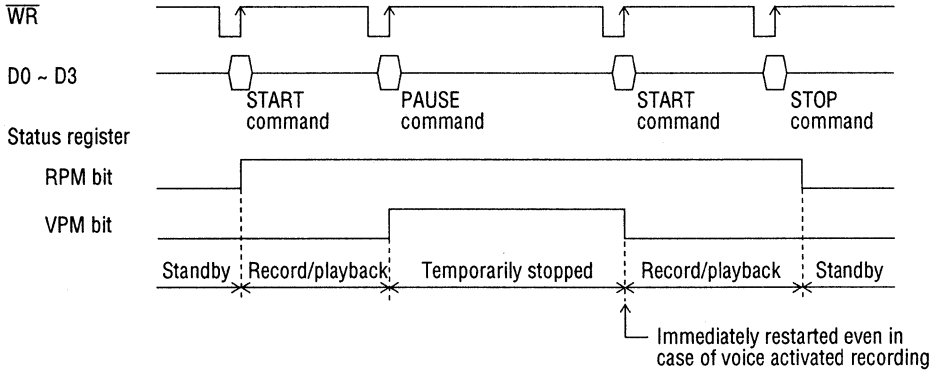


● Stopping Temporarily Record/Playback (by the PAUSE Command)

The record/playback operation in progress can be stopped temporarily by inputting the PAUSE command. The record/playback operation stopped using the PAUSE command can be restarted by inputting the START command. During temporary stop state, the VPM bit of the status register is 1 and the RPM bit keeps 1.

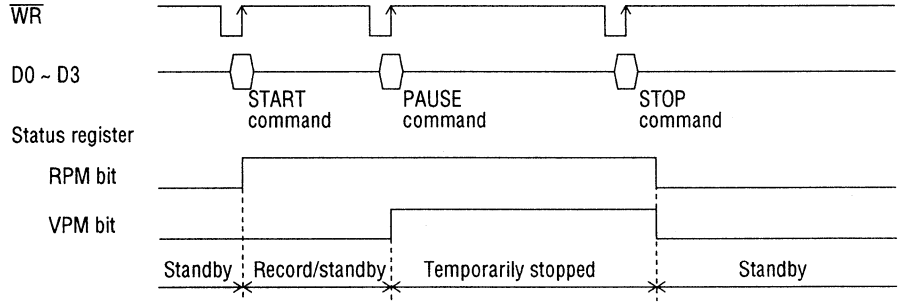
If the START command is input to restart the recording operation that is temporarily suspended by the PAUSE command in the voice activated recording mode, the recording will be started immediately even in the state of silence. The PAUSE command is invalid during record/playback state, temporarily stopped state, and standby state for voice.

When the STOP command is input during temporarily stopped state, the record/playback operation



is finished and the MSM6688 is placed in the standby state.

● Transferring Data to/from External Memories



● Transferring Data to/from External Memories

1. Method of transferring data to/from external serial registers (by the CHRW command)

The MSM6688 can transfer data to/from the user area in the channel index area of external RAM using the CHRW command. Before starting this data transfer operation, a desired phrase must be specified using the CHAN command. The memory capacity for each phrase is 704 bits (176 nibbles) in the flex record/playback mode and 960 bits (240 nibbles) in the direct record/playback mode. The read/write operation must be performed for the data that does not exceed this memory capacity per phrase.

The contents of the user area for a specified phrase or for all phrases will be cleared to all 0s (0h data) using the CHAN and DEL commands.

The following shows the procedure for inputting the CHRW command.

(1) Set the command mode to mode 0 or mode 1 (MOD1=0) using the SAMP command.

(2) Specify a phrase using the CHAN command.

(3) After inputting the CHAN command, wait for BUSY state duration. The end of the BUSY state duration can also be verified by the BUSY bit of the status register.

(4) To write data, input the REC command and then input the data to be written by applying the $\overline{WR}$ pulse. It is required to wait for the busy state duration between the contiguous $\overline{WR}$ pulses.

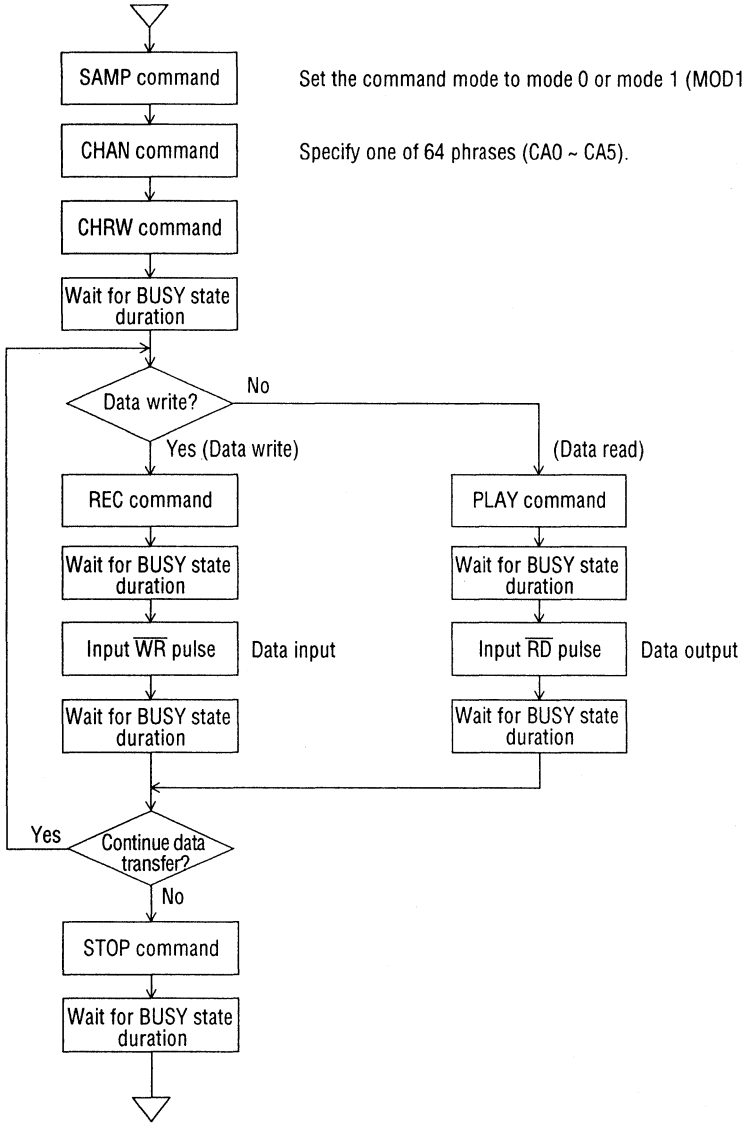
When the data writing operation is performed by inputting a single input of the CHRW command, the state of the BUSY bit of the status register can be verified by inputting the $\overline{RD}$ pulse. When the data read operation is performed with the data write operation, the state of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse.

(5) When reading data, wait for the BUSY state duration after inputting the PLAY command and then input the $\overline{RD}$ pulse. With this operation, 4-bit data will be output via the data bus.

(6) To continue the data read or write operation, specify the read or write mode using the PLAY or REC commands.

(7) To stop the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer by the CHRW command



2. Method of transferring data to and from external RAM (by the DTRW command)

The data transfer to/from external RAM is performed using the DTRW command. After inputting the DTRW command, specify an address to be accessed for data read/write. The transfer of each 4-bit data is performed from the starting nibble of the specified address. For the address space, refer to Section 1.2 "Address space allocation in the direct record/playback mode" in "Data Configuration of External RAM." The address designation can be made only in the X direction and random address designation cannot be made in the Y direction to select an arbitrary address in the Y direction.

With the input of a single DTRW command, continuous read/write operation can be made in the range of addresses 8Mbit ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$,). When the read/write operation is extended to two or more 8Mbits ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$,), it is necessary to stop temporarily the read/write operation each time the operation is finished for one serial register, and set the address for another serial register using the DTRW command.

(1) Set the common mode to mode 2 (MOD0 = 0, MOD1 = 1)

(2) Input the DTRW command

(3) Specify the X address in a serial register by inputting the $\overline{WR}$ pulse five times. Wait for the BUSY state duration. The BUSY state can be verified by examining the state of the BUSY bit of the status register. The 2nd nibble of the DTRW command is a dummy nibble. Always input 0h data into the 2nd nibble.

(4) For data writing, input the REC command and input the data to be written by inputting the $\overline{WR}$ pulse. Wait for the BUSY state duration between the contiguous $\overline{WR}$ pulses.

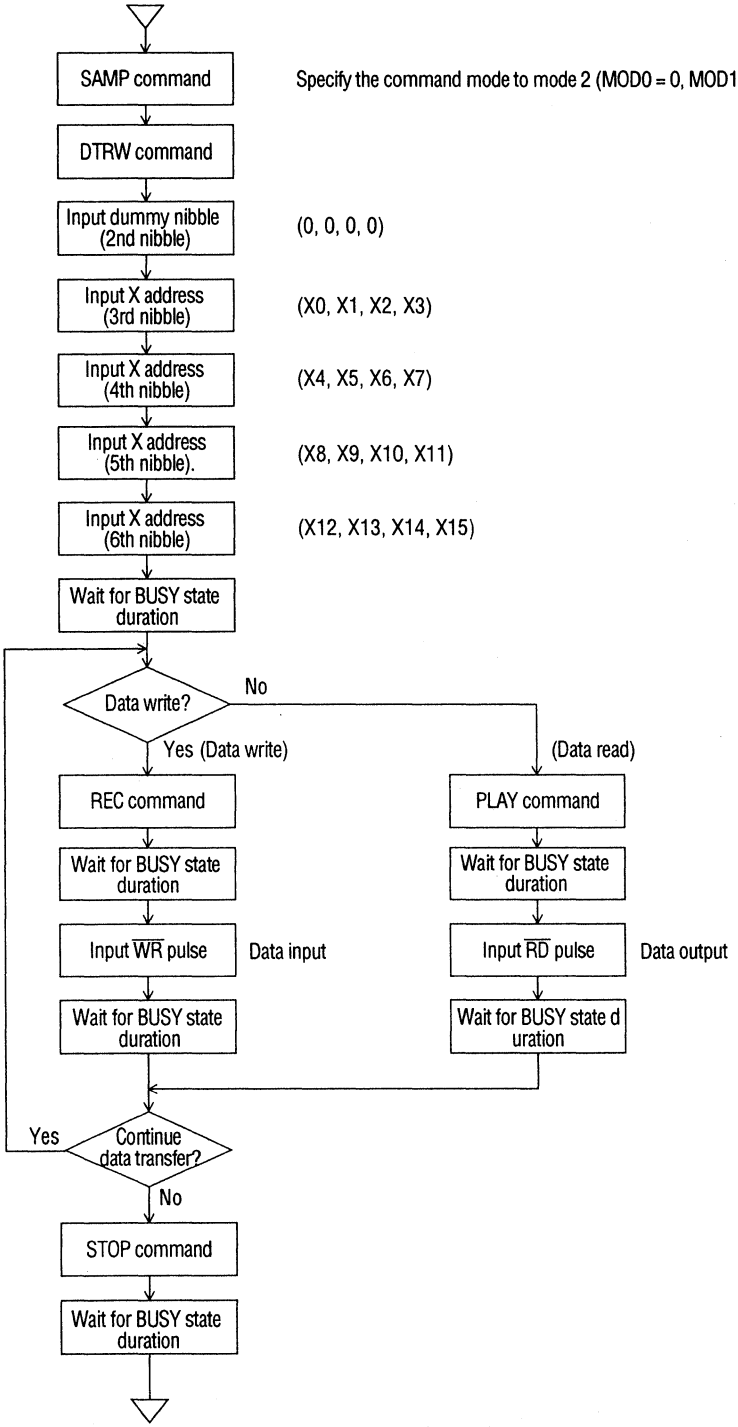
To make the data write operation by a single input of the DTRW command, the state of the BUSY bit can be verified by inputting the $\overline{RD}$ pulse. When data write and data read operations are performed jointly, the state at the BUSY bit cannot be verified using the $\overline{RD}$ pulse.

(5) To read data, input the PLAY command and then input the $\overline{RD}$ pulse after waiting for the BUSY state duration. With this operation, 4-bit data will be output via the data bus.

(6) To continue data read/write operation, specify the read or write mode using the PLAY or REC command and make data transfer operation.

(7) To finish the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer using the DTRW command



3. Method of reading data from external serial voice ROMs (by the DTRD command)

The data from external serial voice ROMs can be read using the DTRD command. After inputting the DTRD command, specify the address to be read. The data is read in groups of 4 bits from the specified address. For the address space, refer to "Data Configuration of External Serial Voice ROMs." The data can be addressed on a 64-bit basis.

With the input of a single DTRD command, continuous read/write operation can be made in the range of addresses assigned to the same serial voice ROM. When the read/write operation is extended to two or more serial voice ROMs, it is necessary to stop temporarily the read/write operation each time the operation is finished for the serial voice ROM, and set the address for another serial voice ROM using the DTRD command.

The following shows the procedure for inputting the DTRD command.

(1) Set the command mode to mode 3 (MOD0 = 1, MOD1 = 1).

(2) Input the DTRD command.

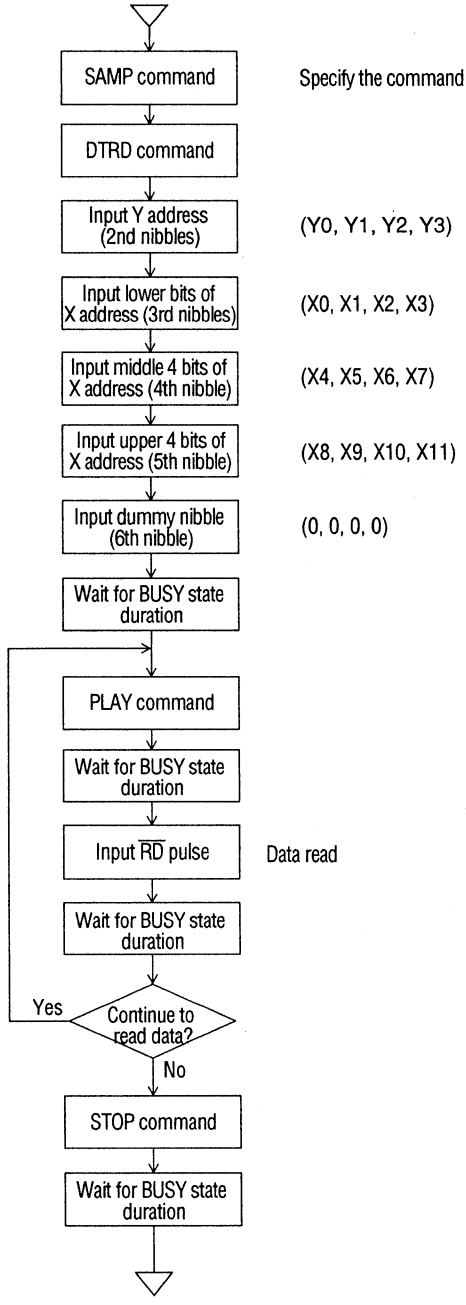
(3) Specify the X address and Y address of the serial voice ROM by inputting the $\overline{WR}$ pulse five times. Then, wait for the BUSY state duration. The 6th nibble is a dummy nibble. Always input 0h data into this 6th nibble.

(4) Input the PLAY command and wait for the BUSY state duration. Then, input the $\overline{RD}$ pulse, so that 4-bit data will be output via the data bus.

(5) To continue data read operation, perform the data read operation inputting the PLAY command and $\overline{RD}$ pulse in the same way as mentioned above.

(6) To finish the data read operation input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data read using the DTRD command



● Record/Playback by Inputting/Outputting Voice Data via Data Bus

When SRAMs (static RAMs) or other hardware memory products are used to store voice data, the record/playback operation will be performed by using the EXT command. In the case of the record/playback using the EXT command, voice data is directly input or output via the data bus in synchronization with the sampling frequency. In this record/playback mode, the address control and the control of external RAM and serial voice ROMs are not performed. Therefore, the microcontroller performs the recording time control and address control. In this mode, temporary stop of record/playback operation by the PAUSE command and the voice activated recording cannot be performed.

1. Method of recording using the EXT command

(1) Input the record/playback conditions using the corresponding commands as shown below.

VDS command: Set the ADPCM bit length (BIT).
Specify the disabled state of voice activation (VD0 = 0, VD1 = 0)

SAMP command: Specify the sampling frequency (SA0, SA1)
The command mode (MOD0, MOD1) is invalid.

REC command: Set to the recording mode

(2) Input the EXT command to start the recording. The sampling frequency clock is output via the MON pin.

(3) When the MON pin goes high, input the $\overline{RD}$ pulse to fetch the ADPCM data from the external memory via the data bus. In the case of 3-bit ADPCM, the upper 3 bits (D3–D1 pins) are valid and the lower 1 bit (D0 pins) is invalid.

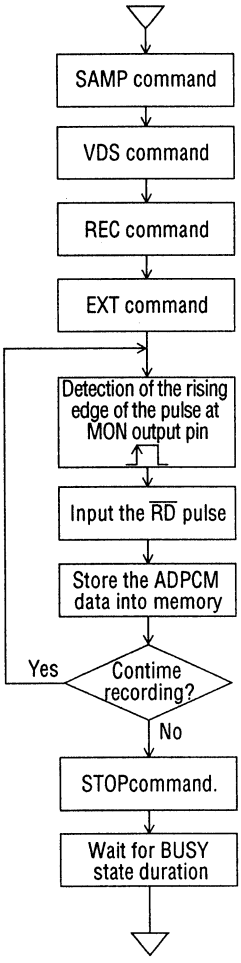
(4) Store the ADPCM data into the external memory such as SRAMs.

(5) Repeat steps (3) and (4) to continue the recording operation.

(6) Input the STOP command to stop the recording operation. Until the STOP command is input, the recording operation will be continued without the limit for the recording time.

(7) During recording by the EXT command, the contents of the status register cannot be verified by the $\overline{RD}$ pulse. Therefore, after inputting the STOP command, wait for the BUSY state duration and then input the next command.

Flow chart of recording using the EXT command



Specify the sampling frequency (SA0, SA1).

Specify the ADPCM bit length (BIT)

Set to the recording mode

Start the recording by EXT command.

Fetch ADPCM data from memory.

Store the ADPCM data into an external memory such as SRAM.

End of recording by EXT command

2. Method of playback using the EXT command

(1) Input the record/playback conditions using the corresponding commands as shown below.

VDS command: Set to the ADPCM bit length (BIT) specified for recording.
Voice activation conditions go invalid.

SAMP command: Specify the sampling frequency (SA0, SA1)
The command mode (MOD0, MOD1) is invalid.

PLAY command: Set to the playback mode

(2) Input the EXT command to start the playback. The sampling frequency clock is output via the MON pin.

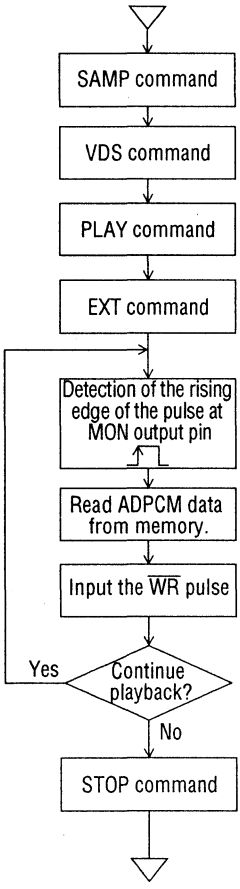
(3) When the MON pin goes high, the ADPCM data is ready to be fetched from an external memory such as an SRAM.

(4) Input the $\overline{WR}$ pulse to fetch the ADPCM data from the external memory via the data bus. In the case of 3-bit ADPCM, the upper 3 bits (D3–D1 pins) are valid and the lower 1 bit (D0 pins) is invalid.

(5) Repeat steps (3) and (4) to continue the playback operation.

(6) Input the STOP command to stop the playback operation.

Flow chart of playback using the EXT command



Specify the sampling frequency (SA0, SA1).

Specify the ADPCM bit length (BIT)

Set to the playback mode

Start the playback by EXT command.

Write the ADPCM data.

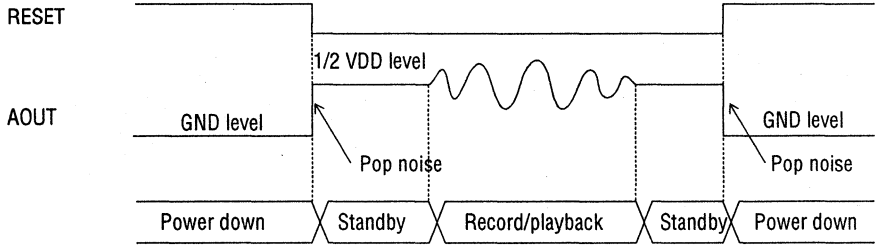
Stop the playback by EXT command.

● Suppression of Pop Noise at AOUT Output (by the LEV Command)

The MSM6688 has a on-chip pop noise suppression circuit to prevent pop nose from being generated due to sharp changes of the DC level of the analog output (at the AOUT pin). The enabled or disabled state of this pop noise suppression circuit can be selected using the ACON pin. When the ACON pin is low, this circuit is disabled and when high, this circuit is enabled.

1. When the POP noise suppression circuit is disabled (ACON = low)

When the RESET pin is high, the DC level at the AOUT pin is the ground level, and when the RESET pin is low, the DC level at the AOUT pin is the 1/2 VDD level. Each time the state of the RESET pin is changed, the DC level is changed sharply and pop noise is generated.

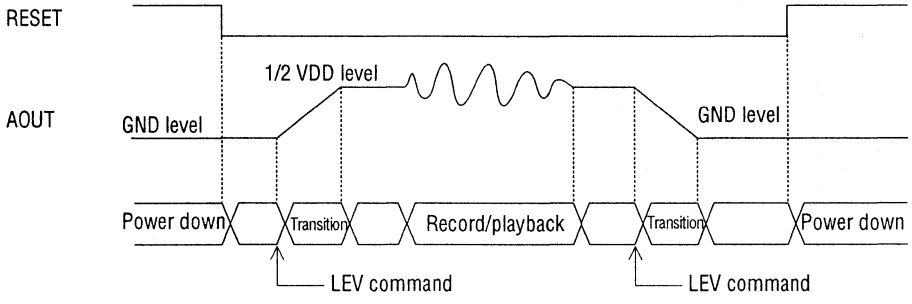


2. When the POP noise suppression circuit is enabled (ACON = high)

The transition of the DC level at the AOUT (analog output) pin is controlled using the LEV command. When the RESET pulse (low) is applied to the RESET pin, the DC level at the AOUT output pin goes to the ground level. If the pop noise suppression circuit is activated using the PN0 and PN1 bits of the 2nd nibble of the LEV command, the DC level at the AOUT output pin will be changed from the ground level to the 1/2 VDD level or from the 1/2 VDD level to the ground level slowly to prevent pop noise from being generated.

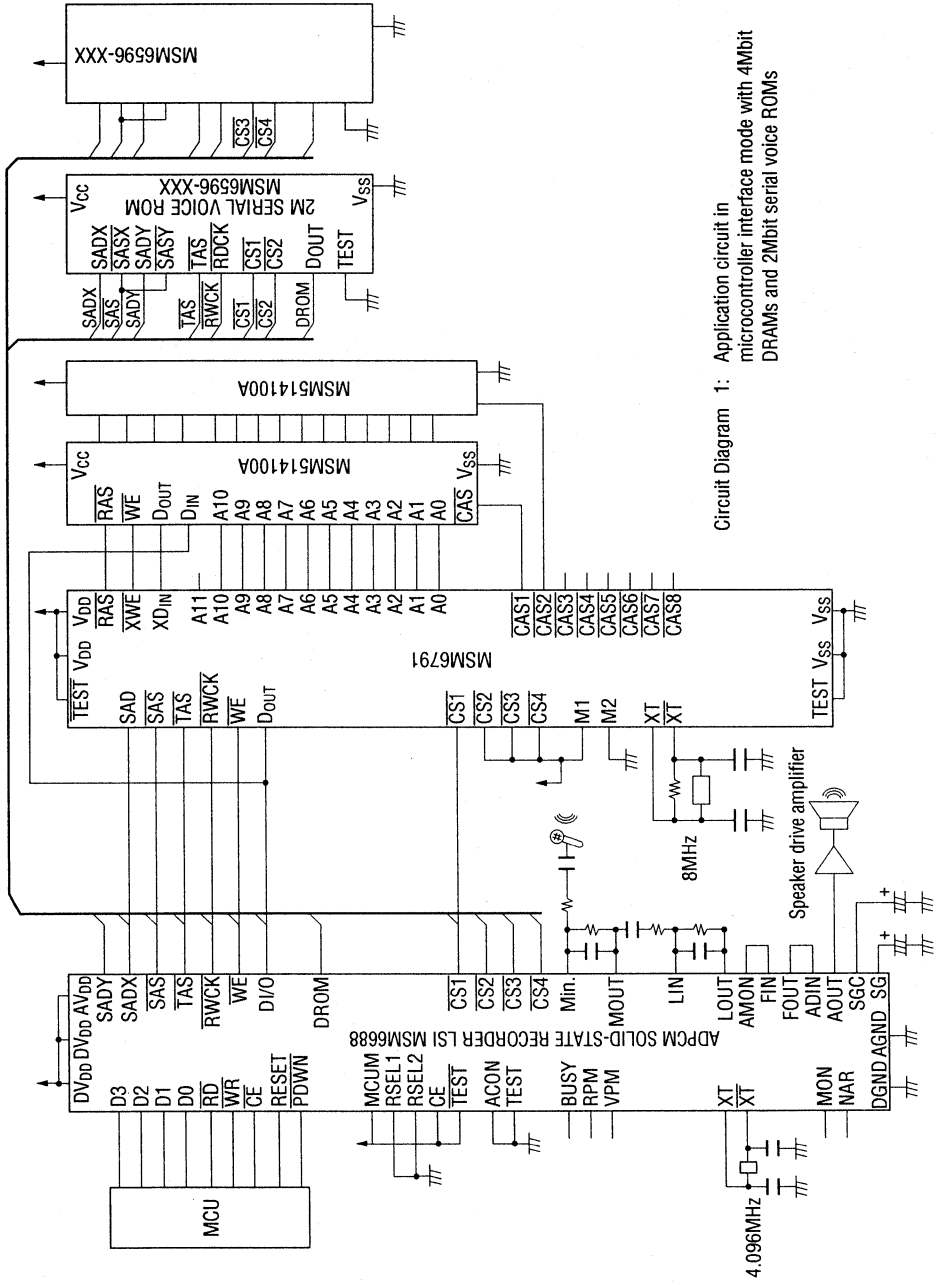
Before starting the record/playback operation, always set the DC level at the AOUT pin to the 1/2 VDD level using the LEV command. When enabling the DC level transition function by the LEV command, first specify the playback mode by the PLAY command and then input the LEV command.

PN1	PN0	DC level transition
0	0	Disabled
0	1	Disabled
1	0	Transition from ground to 1/2 VDD
1	1	Transition from 1/2 VDD to ground



■ EXAMPLE OF APPLICATION CIRCUIT

● The circuit diagram 1 shows an application circuit example where the MSM6688 is used in the microcontroller interface mode and two 4Mbit DRAMs are used as record/playback memories by connecting a DRAM interface LSI, and two 2Mbit serial voice ROMs also are connected.



Circuit Diagram 1: Application circuit in microcontroller interface mode with 4Mbit DRAMs and 2Mbit serial voice ROMs

MSM6788

SBC SOLID-STATE RECORDER LSI

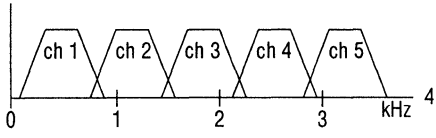
GENERAL DESCRIPTION

The MSM6788 is a solid-state-recorder developed using the Sub Band Coding (SBC) method. By externally connecting a microphone, a speaker, a speaker drive amplifier, and dedicated DRAM through the MSM6791 to store SBC data, it can record and play back voice data in a manner similar to a tape recorder.

The MSM6788 has a stand-alone mode and a microcontroller interface mode. In the stand-alone mode, record/playback conditions can be selected from pins and the MSM6788 can be controlled by a simple drive timing. In the microcontroller interface mode, record/playback can be controlled by commands from the microcontroller, and more functions are available than in the stand-alone mode.

In addition, the MSM6688 can form easily a recording and playback circuit with fixed messages by connecting DRAMs (include the MSM6791) and serial voice ROMs as external memories.

- SBC method:
  The Sub Band Coding (SBC) method divides voice frequency into five bands and codes them respectively.



CONTENTS

(1) STAND-ALONE MODE

(2) MICROCONTROLLER INTERFACE MODE

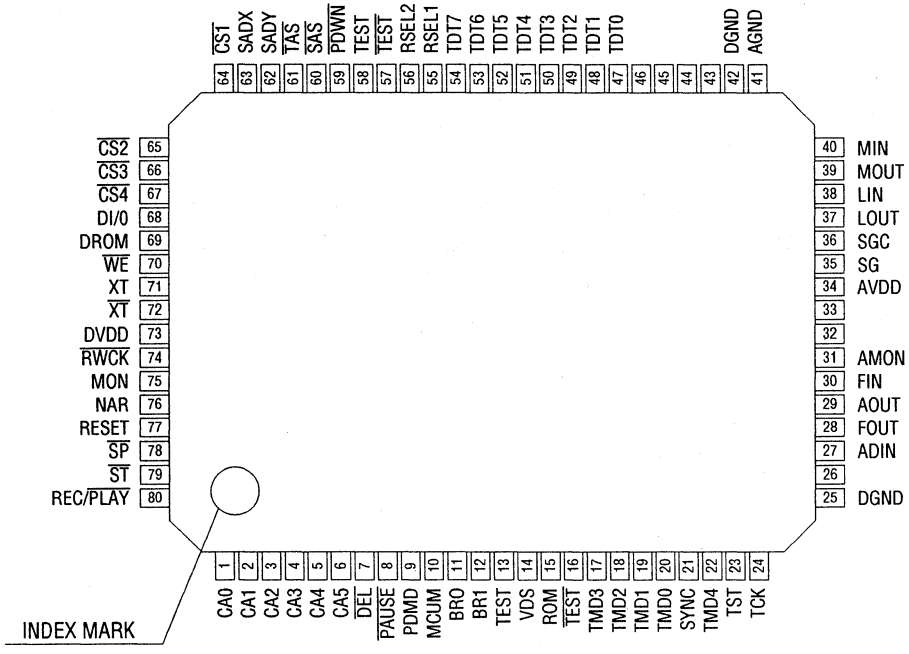
(1) STAND-ALONE MODE

■ FEATURES

- SBC method
- Built-in 12-bit AD converter
- Built-in12-bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  DRAM, maximum 32M bits (for variable messages)
  1/4/16M bit DRAMs (× 1 bit configuration) are controlled by DRAM interface LSI (MSM6791)
  Serial voice ROMs, maximum 4M bits (for fixed messages)
  1M bit serial voice ROM (MSM6595), directly addressable
  2M bit serial voice ROM (MSM6596), directly addressable
  3M bit serial voice ROM (MSM6597), directly addressable
- Bit rate
  10.0k, 12.6k, 16.0kbps (at 8 kHz sampling freq.)
  7.5k, 9.5k, 12.0kbps (at 6 kHz sampling freq.)
- Number of phrases
  63 phrases for variable messages
  63 phrases for fixed messages
- Maximum recording time (when one 8M bit serial register is connected)
  13.8 minutes (for 10.0 kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6 kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.6 minutes (for 16.0 kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Voice activation function
- Pause function
- Master clock frequency: 6.0MHz ~ 8.192 MHz
- Power supply voltage: 5 V single power supply
- Package:80-pin plastic QFP (QFP80-P-1420-V1K)

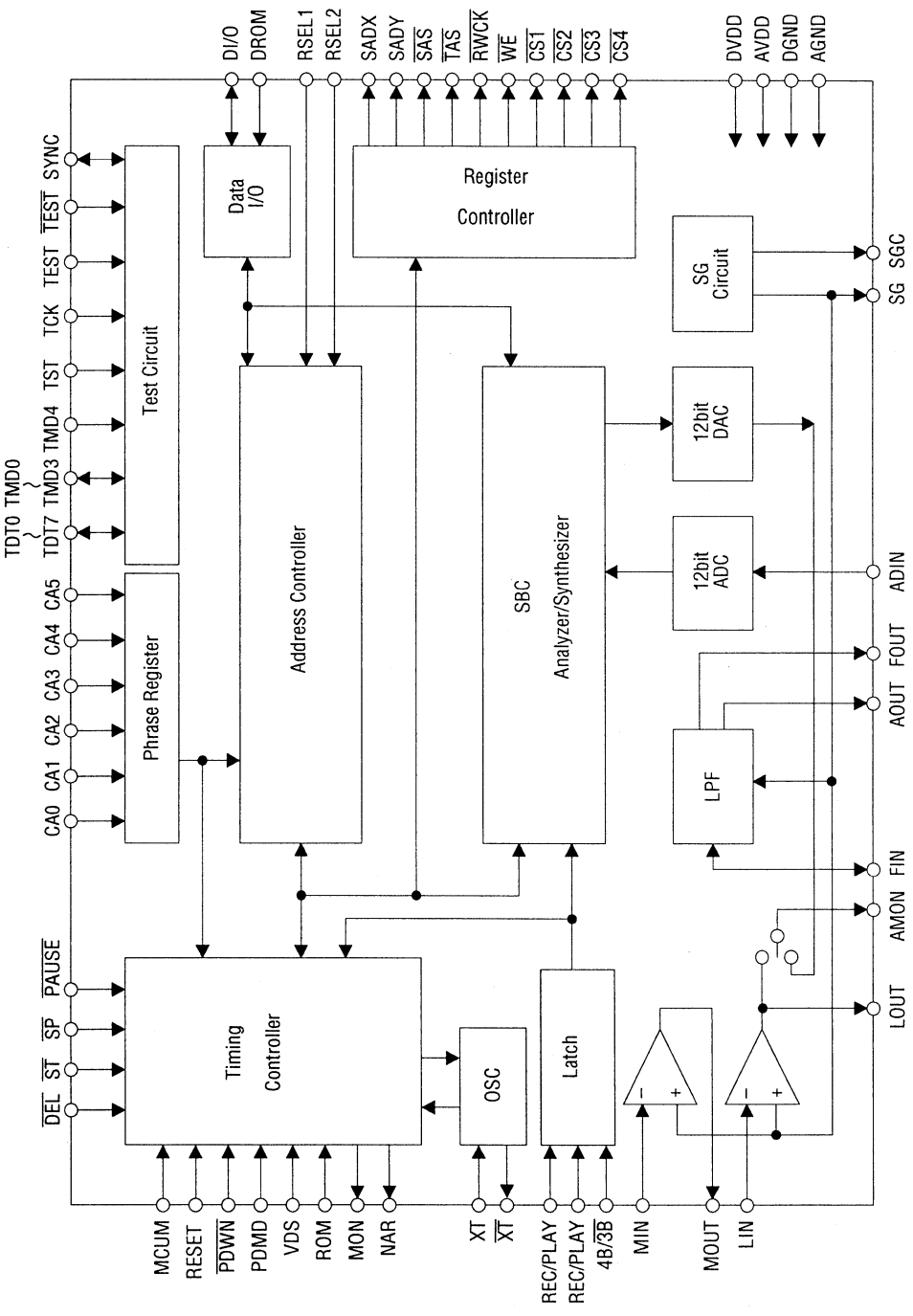
■ PIN LAYOUT (TOP VIEW)

80 LEAD PLASTIC FLAT PACKAGE



NC: No connection (Open)

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3~7.0	V
Input Voltage	VIN	Ta=25°C	−0.3~VDD+0.3	V
Storage temperature	T_{stg}	—	−55~+150	°C

● Operating Range

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5~5.5	V
Operating temperature	Top	—	0~+70	°C
Master clock frequency	fosc	—	6.0~8.192	MHz

● DC characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
High input voltage	V_{IH}	—	0.8×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×VDD	V
High output voltage	VOH	IOH = −40uA	VDD−0.3	—	—	V
Low output voltage	VOL	IOL = 2mA	—	—	0.45	V
High input current (Note 1)	IIH1	VIH = VDD	—	—	10	μA
High input current (Note 2)	IIH2	VIH = VDD	—	—	20	μA
Low input current (Note 1)	IIL1	VIL = GND	−10	—	—	μA
Low input current (Note 2)	IIL2	VIL = GND	−20	—	—	μA
Operating current consumption (1)	IDD	fosc = 8 MHz, no load	—	15	30	mA
Operating current consumption (2)	IPD	At power down. no load	—	—	10	μA

Note 1: Applies to all input pins excluding the XT pin.
Note 2: Applies to the XT pin.

● Analog Characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN}=0~4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

● AC Characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=8.192MHz

Item			Symbol	MIN	TYP	MAX	Unit
RESET pulse width			t_{RST}	1	—	—	μs
RESET execution time		(Note 1)*	t_{REX}	—	1	—	ms
$\overline{PDWN}$ low level time		*	t_{PDL}	250	—	—	μs
$\overline{PDWN}$ high level time		*	t_{PDH}	250	—	—	μs
Oscillating time after input of $\overline{PDWN}$		*	t_{PX}	125	—	250	μs
BUSY time after release of $\overline{PDWN}$		(Note 1)*	t_{BPD}	0.25	—	—	ms
$\overline{ST}$ pulse width		*	t_{ST}	40	—	—	μs
$\overline{SP}$ pulse width		*	t_{SP}	40	—	—	μs
$\overline{PAUSE}$ pulse width		*	t_{PSE}	40	—	—	μs
$\overline{DEL}$ pulse width		*	t_{DEL}	40	—	—	μs
Time required to delete all phrases		*	t_{WBLA}	550	—	—	ms
Time required to delete a specified phrase		*	t_{WBL1}	70	—	—	ms
Time from input of $\overline{DEL}$ pulse to $\overline{CSI}$ fall		*	t_{DCS}	—	—	270	μs
Hold time of CA0~CA5, REC/$\overline{PLAY}$ after MON rise			t_{CAH}	1	—	—	ms
Address control time at the start of record/playback		*	t_{AD1}	—	1	—	ms
Time from input of $\overline{ST}$ pulse to NAR fall		*	t_{STN}	—	—	40	μs
Unvoiced time between phrases during repeated playback		*	t_{MID}	0.75	—	1	ms
PDMD=H	Time from input of $\overline{ST}$ pulse to MON rise	Record *	t_{TMH1}	—	—	50	ms
		Playback *	t_{TMH2}	—	—	20	ms
		ROM playback*	t_{TMH3}	—	—	1	ms
	Time from input of $\overline{SP}$ pulse to MON fall	Record *	t_{PMH1}	60	—	80	ms
		Playback *	t_{PMH2}	1	—	15	ms
		ROM playback*	t_{PMH3}	1	—	15	ms
	Time from input of $\overline{ST}$ pulse to voice activation standby state	*	t_{STVH}	—	—	50	ms
	Time from input of $\overline{SP}$ pulse during voice activation standby state to release of voice activation standby state	*	t_{SPVH}	60	—	80	ms

Items with * are proportional to the period of master oscillator frequency fosc.

Note 1: The oscillation startup stabilization time is added to t_{REX} and t_{BPD}.
The oscillation startup stabilization time is several tens of milliseconds for crystaloscillators and is several hundreds of microseconds for ceramic oscillators.

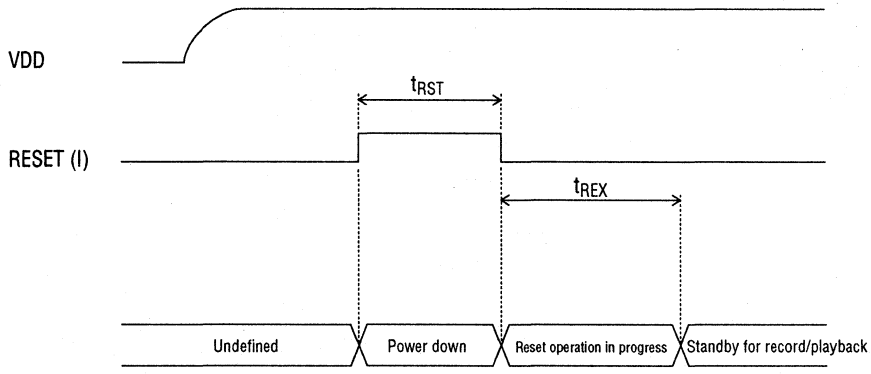
DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70℃
fosc=8.192MHz

Item			Symbol	MIN	TYP	MAX	Unit
PDMD=L	Time from input of $\overline{ST}$ pulse to MON rise	Record *	t_{TML1}	—	—	120	ms
		Playback *	t_{TML2}	—	—	150	ms
		ROM playback *	t_{TML3}	—	—	150	ms
	Time from input of $\overline{SP}$ pulse to MON fall	Record *	t_{PML1}	60	—	80	ms
		Playback *	t_{PML2}	64	—	80	ms
		ROM playback *	t_{PML3}	64	—	80	ms
	Time from input of $\overline{ST}$ pulse to voice activation standby state *		t_{STVL}	—	—	120	ms
	Time from input of $\overline{SP}$ pulse during voice activation standby state to release of voice activation standby state *		t_{SPVL}	60	—	80	ms
	Standby transition time at start of playback *		t_{AOR}	—	64	—	ms
	Standby transition time at end of playback *		t_{AOF}	—	64	—	ms
Time from input of $\overline{PAUSE}$ pulse to pause *			t_{PP}	—	—	15	ms
Time from input of $\overline{ST}$ pulse during pause to restart of record/playback *			t_{PST}	—	—	15	ms

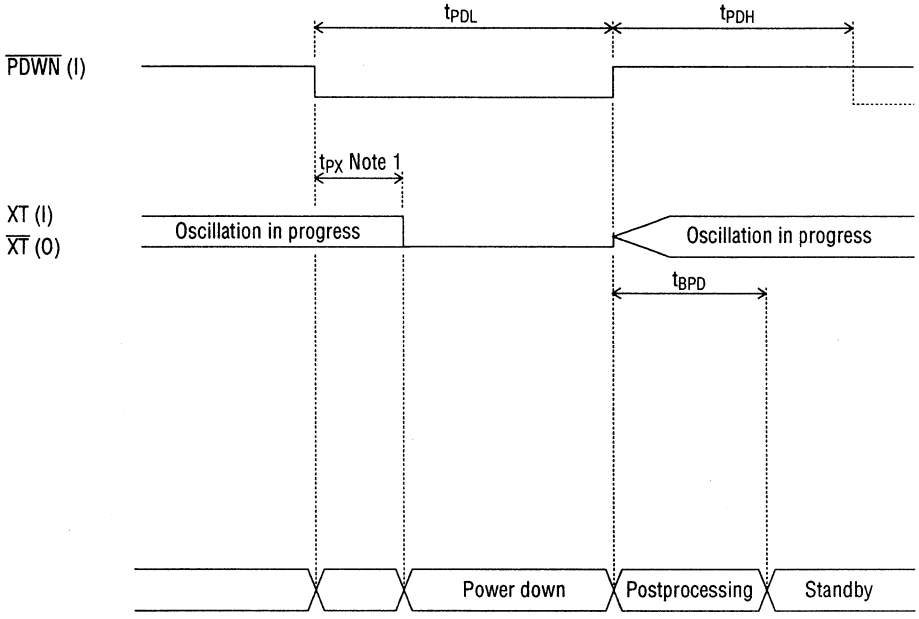
Items with * are proportional to the period of master oscillator frequency fosc.

■ TIMING DIAGRAMS

● RESET FUNCTION

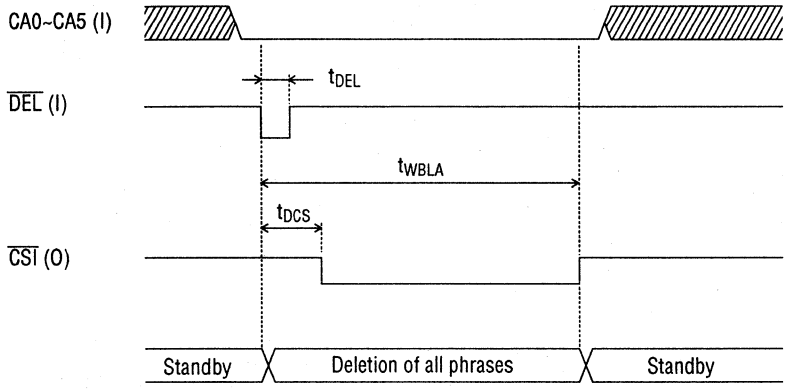


● Power Down by $\overline{\text{PDWN}}$ Pin

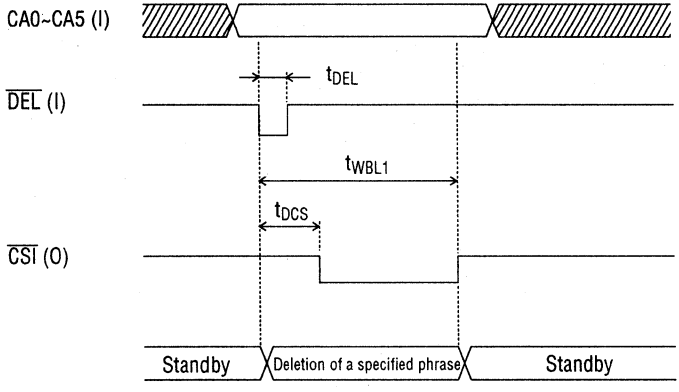


Note 1: When an external clock is used, continue to apply the clock input to the XT terminal during t_{PX} after the $\overline{\text{PDWN}}$ pin is set to a low level.

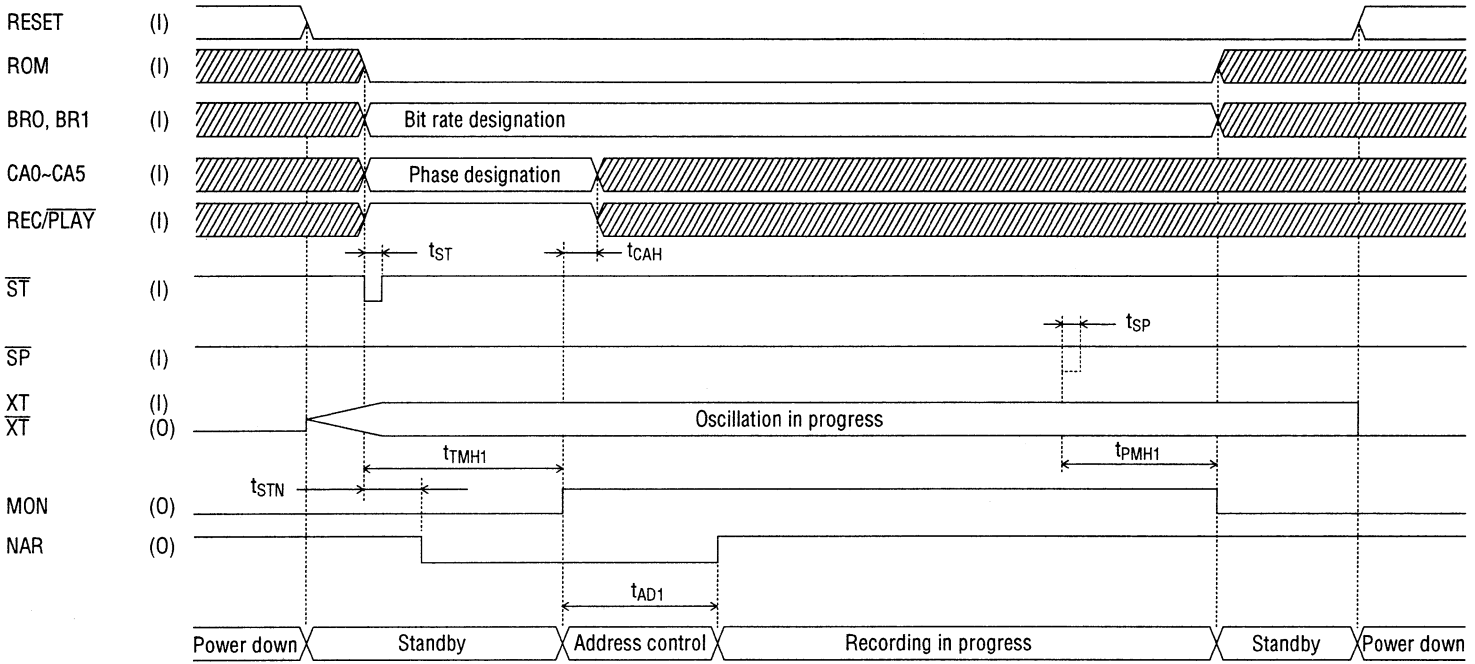
● Timing for Deletion of All Phrases



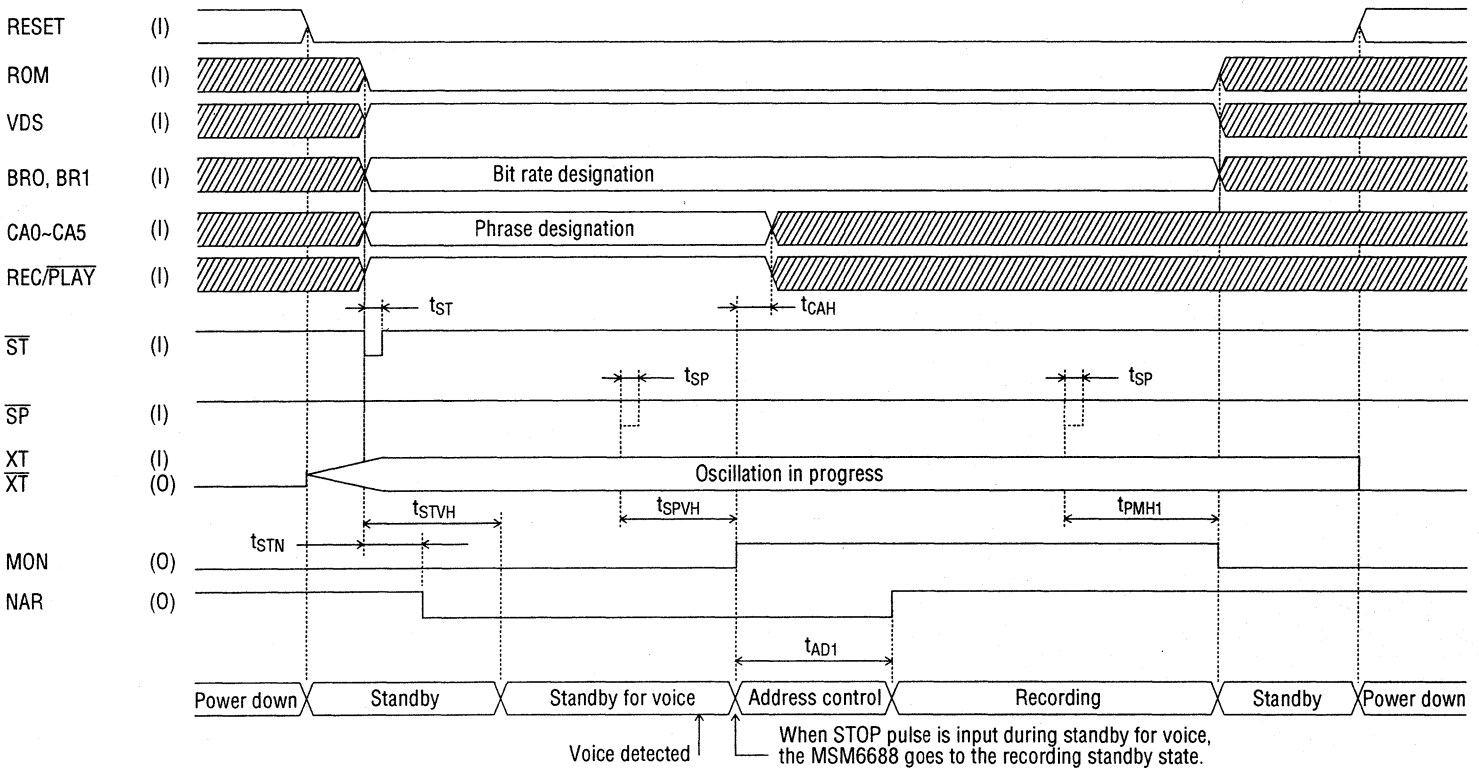
● Timing for Deletion of a Specified Phrase



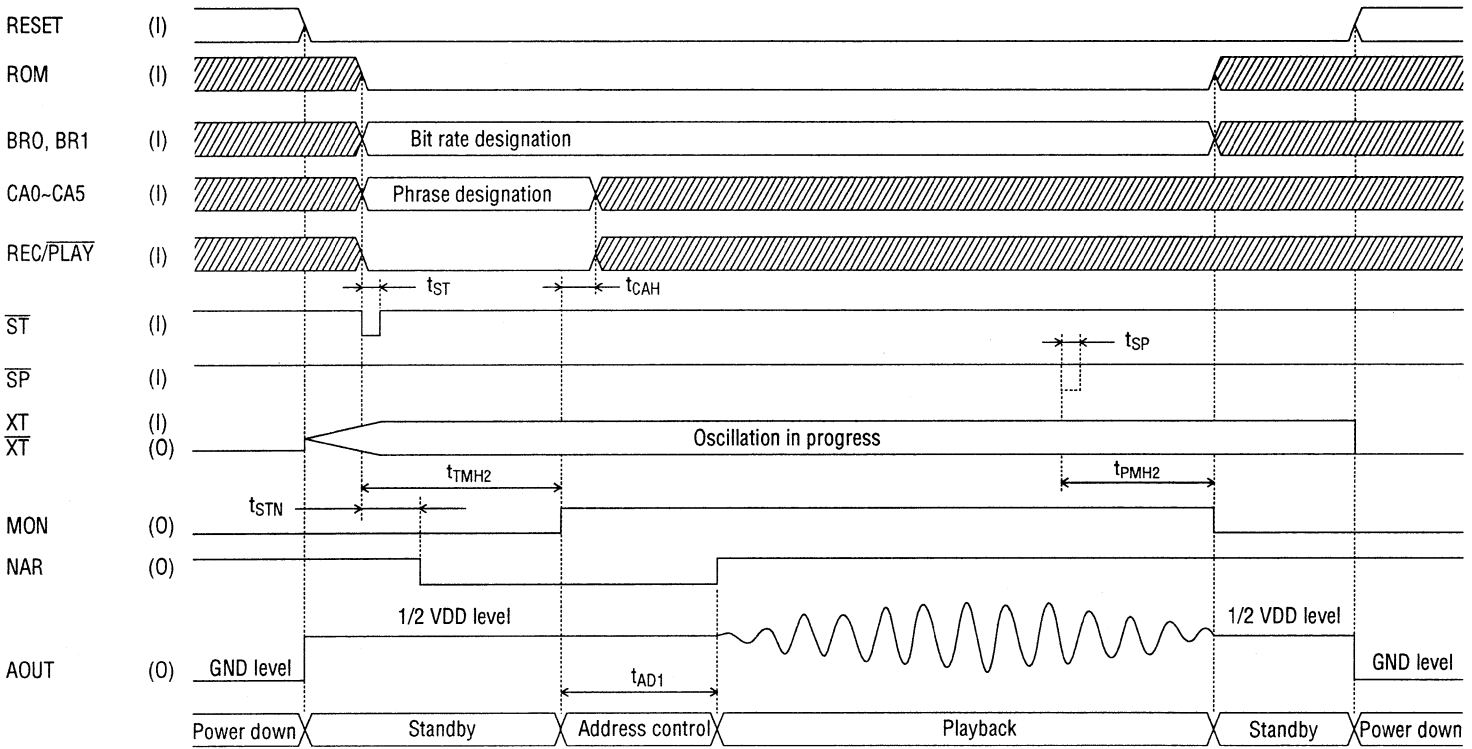
● Recording Timing (PDMD Pin = High)



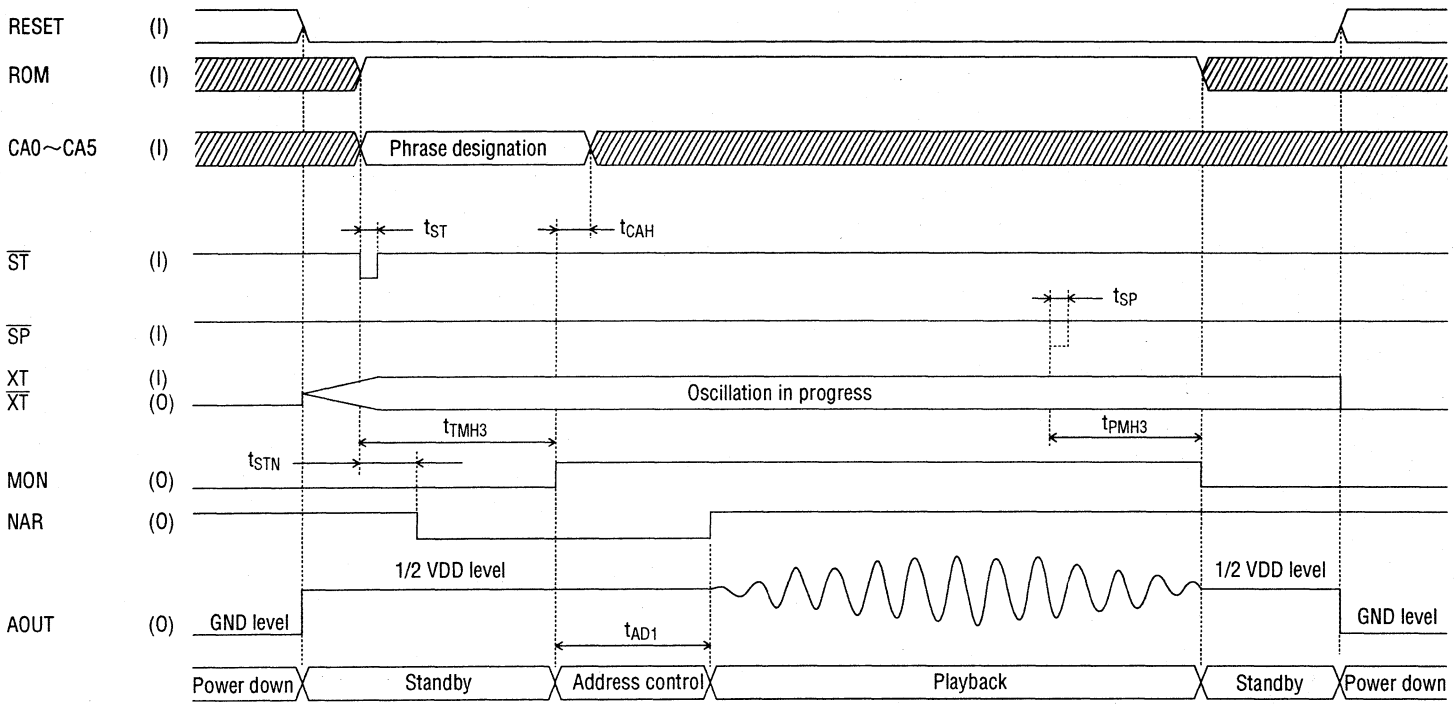
● Timing for Voice Activated Recording (PDMD Pin = High)



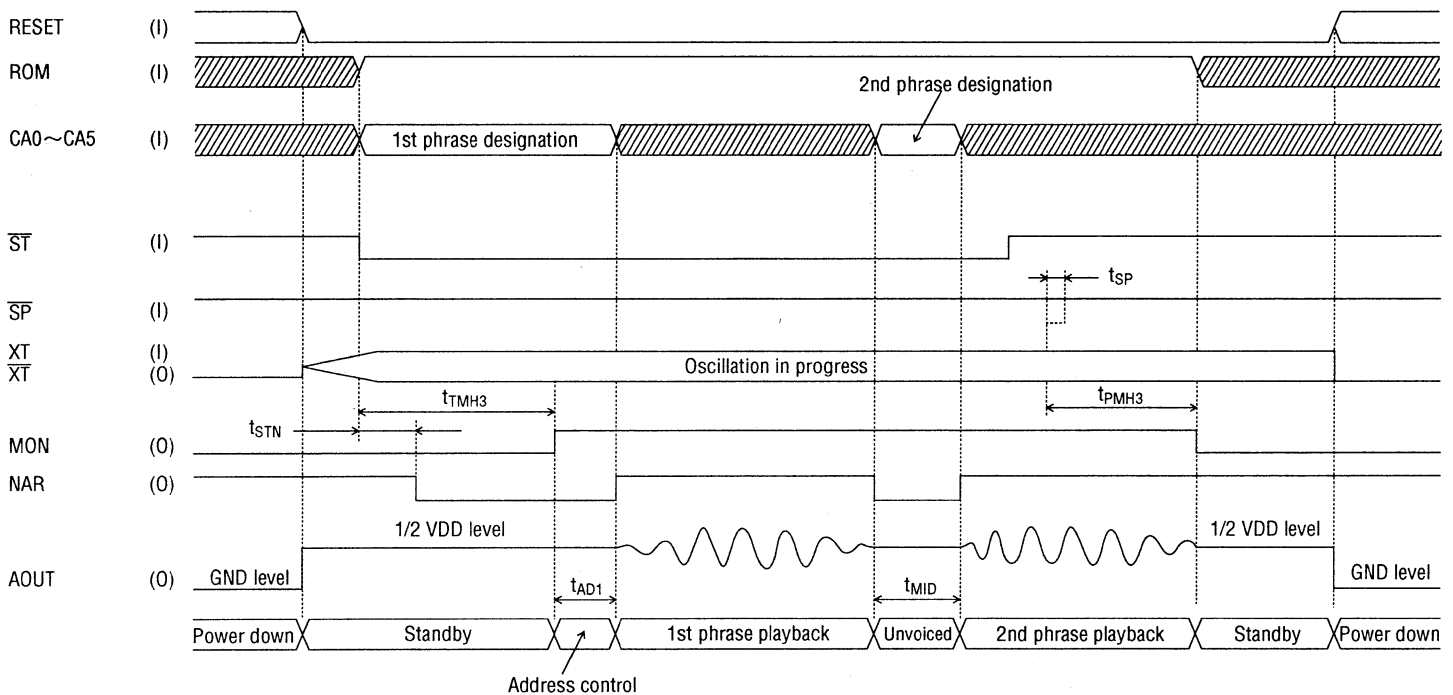
● Playback Timing (PDMD Pin = High)



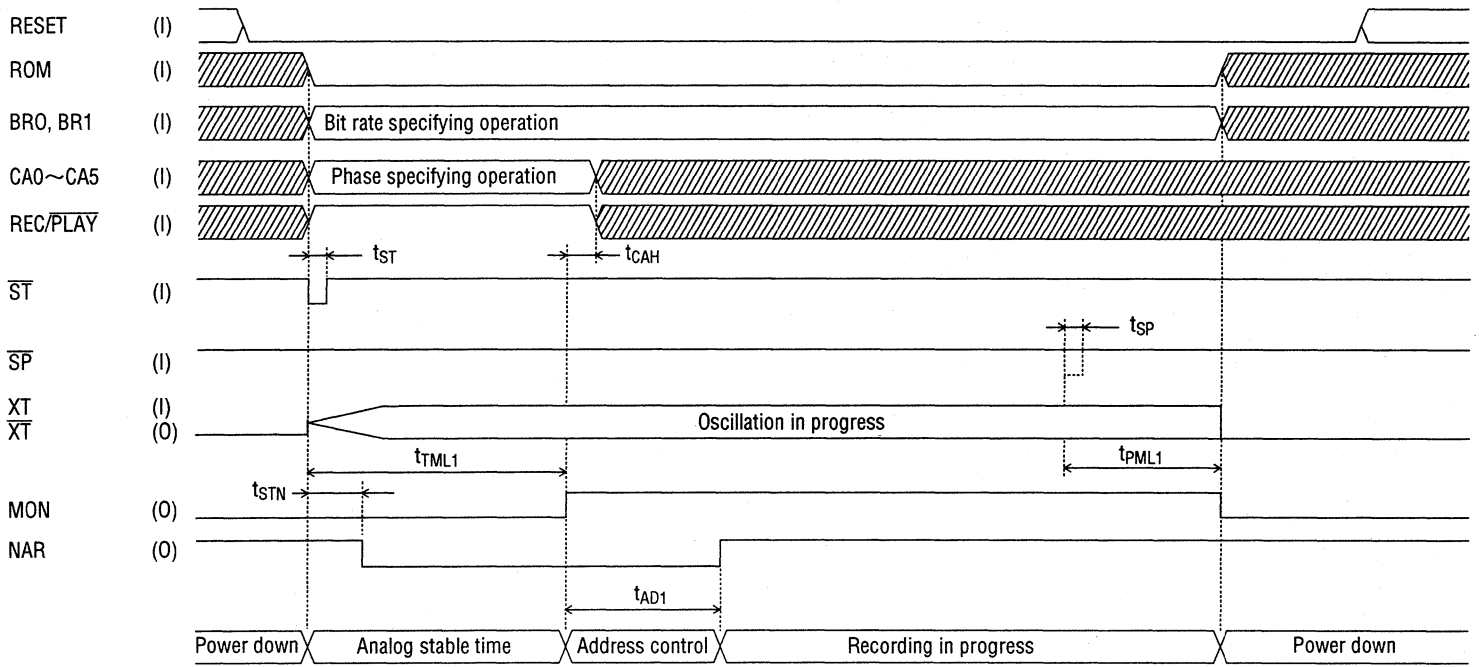
● ROM Playback Timing (PDMD Pin = High)



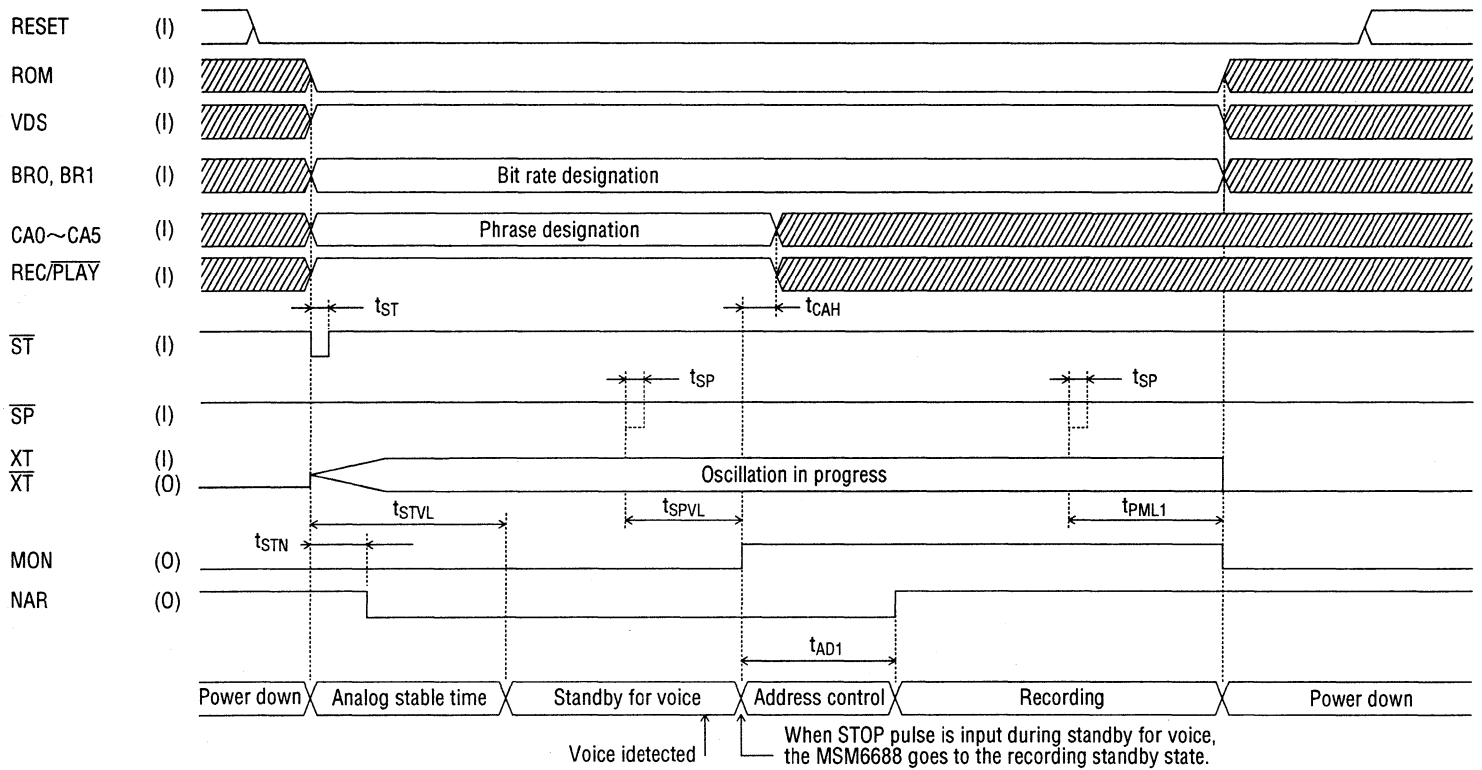
● Continuous ROM Playback Timing (PDMD Pin = High)



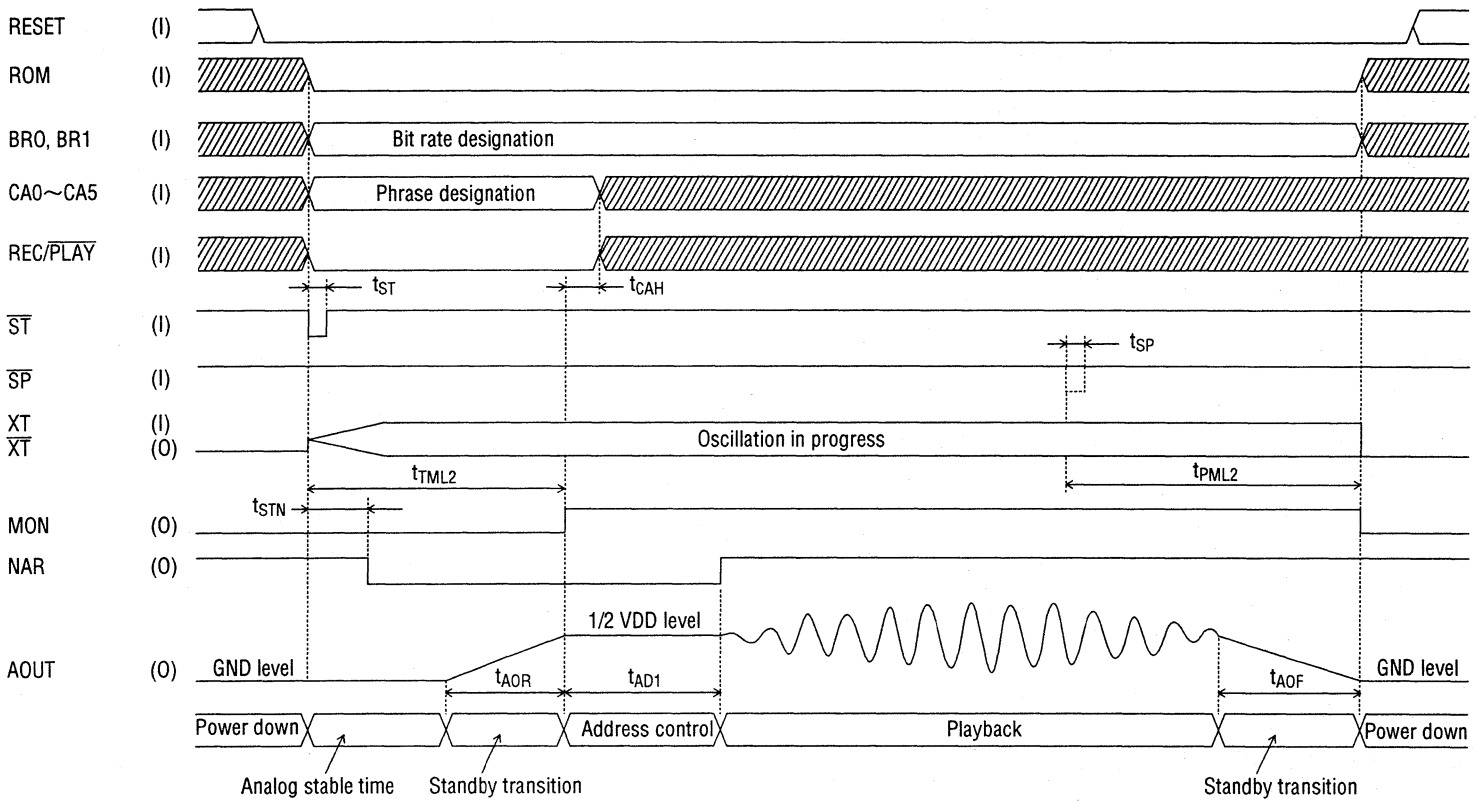
● Recording Timing (PDMD Pin = Low)



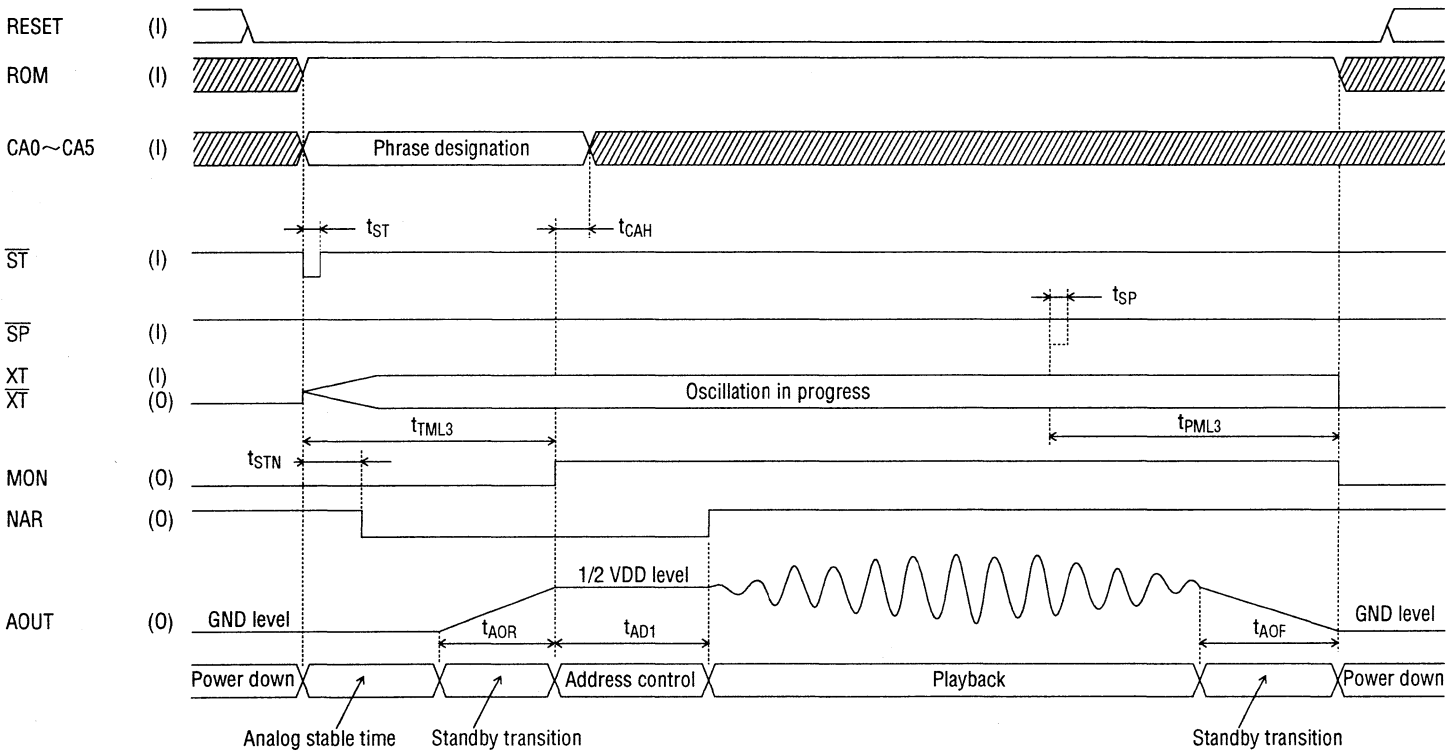
● Timing for Voice Activated Recording (PDMD Pin = Low)



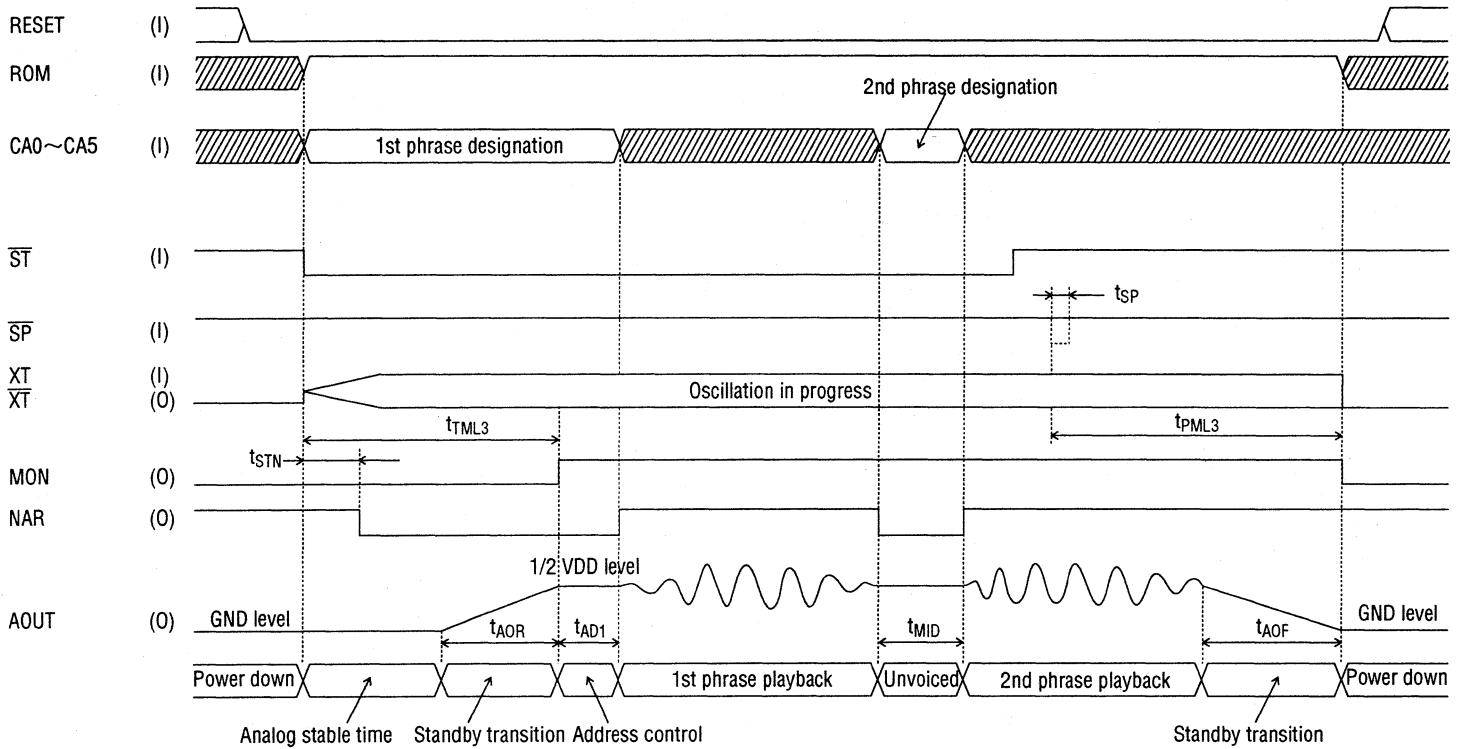
● Playback Timing (PDMD Pin = Low)



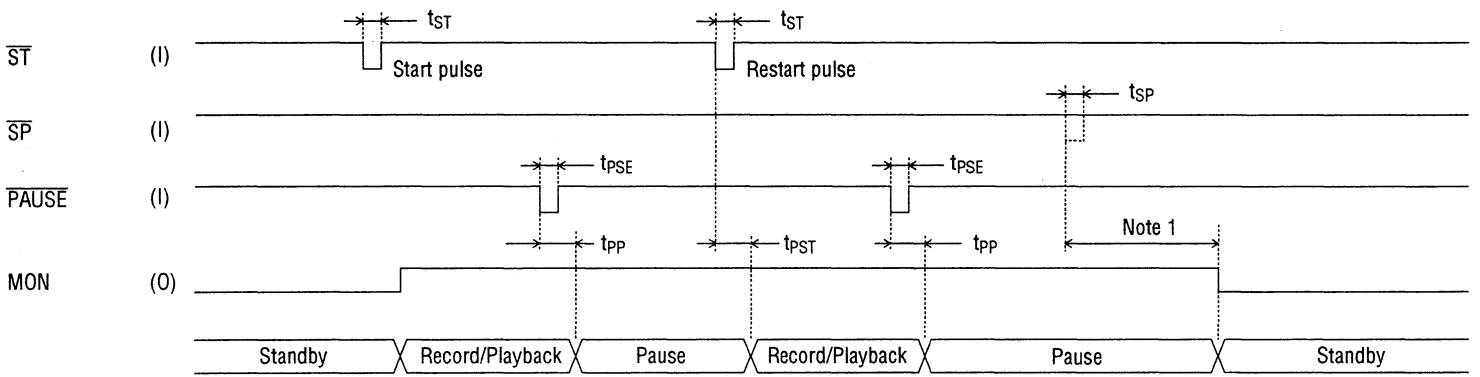
● ROM Playback Timing (PDMD Pin = Low)



● Continuous ROM Playback Timing (PDMD Pin = Low)



● Record/Playback Pause Timing



Note 1: This time interval varies depending on the state of PDMD pin and the record/playback mode and is one of t_{PMH1}, t_{PMH2}, t_{PMH3}, t_{PML2} and t_{PML3}.

■ PIN DESCRIPTION

Pin Name	I/O	Pin function
DVDD	–	Digital power supply pin
AVDD	–	Analog power supply pin
DGND	–	Digital ground pin
AGND	–	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin).
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). Used to connect the SAD pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs of starting address of read/write.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external MSM6791 (DRAM interface LSI) and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each external MSM6791 (DRAM interface LSI) and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external MSM6791 (DRAM interface LSI) and the $\overline{RDCK}$ pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external MSM6791 (DRAM interface LSI).
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external MSM6791 (DRAM interface LSI). This pin outputs WE signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN and DOUT pins of external MSM6791 (DRAM interface LSI). This pin outputs the data to be written into the external MSM6791 (DRAM interface LSI) or inputs the data read from the external MSM6791 (DRAM interface LSI).
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voic ROM.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	(Chip Select). Used to connect $\overline{CS}$ pin of each external MSM6791 (DRAM interface LSI) and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of each serial voice ROM.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>RSEL1
RSEL2</td><td>I</td><td>(Register Select). These input pins are used to select the number of external RAM to be connected.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Total memory size</td><td>8Mbit</td><td>16Mbit</td><td>24Mbit</td><td>32Mbit</td></tr>
</table></td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode.</td></tr>
<tr><td>RESET</td><td>I</td><td>A high input level at this pin causes the MSM6788 to be initialized and to go into the power down state.</td></tr>
<tr><td>$\overline{\text{PDWN}}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6788 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6788. When an Low level is applied to this $\overline{\text{PDWN}}$ pin during recording operation, the MSM6788 is halted, and will be maintained in the power down state while $\overline{\text{PDWN}}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>XT</td><td>I</td><td>Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.</td></tr>
<tr><td>$\overline{\text{XT}}$</td><td>O</td><td>Used to connect an oscillator. When an external clock is used, this pin must be left open.</td></tr>
<tr><td>TEST
$\overline{\text{TEST}}$</td><td>I</td><td>Used to test the LSI. Input a low level to the TEST pin and a high level to the $\overline{\text{TEST}}$ pin.</td></tr>
<tr><td>TMDO ~TMD3
TDTO ~TDT7
SYNC</td><td>I/O</td><td>Used to test the MSM6788. This pin must be left open.</td></tr>
<tr><td>TST
TCK
TMD4</td><td>I</td><td>Used to test the MSM6788. Input a low level.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>ROM</td><td>I</td><td>When low, selects the record/playback operation. When high, selects the ROM playback operation.</td></tr>
<tr><td>REC/$\overline{\text{PLAY}}$</td><td>I</td><td>Used to select the recording mode or the playback mode. This pin is invalid during the ROM playback operation. When low, selects the playback mode. When high, selects the recording mode.</td></tr>
<tr><td>$\overline{\text{ST}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is started.</td></tr>
<tr><td>$\overline{\text{SP}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM playback is stopped.</td></tr>
<tr><td>$\overline{\text{PAUSE}}$</td><td>I</td><td>When a low-level pulse is applied to this pin, the record/playback or ROM operation is stopped temporarily.</td></tr>
<tr><td>$\overline{\text{DEL}}$</td><td>I</td><td>When a low level pulse is applied to this pin, all phase deletion or specified phrase deletion can be performed according to the setting of pins CA0 through CA5,
ch00: All phase deletion
ch01~ch3F: Specified phrase deletion
After powering up, be sure to input RESET signal and then to delete all phrases. After completing this procedure, start the record/playback operation.</td></tr>
<tr><td>CA0~CA5</td><td>I</td><td>Input pins used to specify desired phases.
A total of 63 phrases can be specified independently for the record/playback operation and the ROM playback operation.
<table>
<tr><th>CA5</th><th>CA4</th><th>CA3</th><th>CA2</th><th>CA1</th><th>CA0</th><th>Phrase No.</th><th>Remarks</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>ch00</td><td>All phase deletion</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>ch01</td><td rowspan="6">A total of 63 phrases can be used both for record/playback and ROM playback operation.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td><td>ch02</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>ch3E</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>ch3F</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>BR0
BR1</td><td>I</td><td>Used to select one of the following four types of bit rate. This pin is invalid during the ROM playback operation.
<table>
<tr><th>BR1</th><th>BR0</th><th>Bit rate</th></tr>
<tr><td>L</td><td>L</td><td>16.0 kbps</td></tr>
<tr><td>L</td><td>H</td><td>12.6kbps</td></tr>
<tr><td>H</td><td>L</td><td>10.0 kbps</td></tr>
<tr><td>H</td><td>H</td><td>No use</td></tr>
</table></td></tr>
<tr><td>PDMD</td><td>I</td><td>This input pin is used to select the condition for transition to the power-down state.
Low level: The MSM6788 automatically goes to the power-down state, excepting the time the record/playback operation is being performed.
High level: The MSM6788 automatically goes to the standby state, instead of the power-down state, excepting the time the record/playback operation is being performed. In this case, the MSM6788 can be placed in the power-down state by setting the RESET pin to a high level. If it is desired to use the built-in LPF for an external circuit, this standby mode must be selected by applying a high level to the PDMD pin.</td></tr>
<tr><td>VDS</td><td>I</td><td>Used to select the voice activated recording that starts recording when the voice input exceeds the preset amplitude. A high input level on this pin enables the voice activated recording circuit.</td></tr>
<tr><td>MON</td><td>O</td><td>Outputs a high level while the record/playback operation is being performed.</td></tr>
<tr><td>NAR</td><td>O</td><td>Output pin to indicate the enable or disable state of the operation for specifying a phrase. When continuous ROM playback is performed, the next phrase can be specified after verifying that the NAR pin becomes high.</td></tr>
</table>

■ FUNCTIONAL DESCRIPTION

● Bit Rate

The master clock frequency (fosc) and sampling frequency (fsam) are shown in the following equation. When the master clock frequency is 8.192 MHz, the sampling frequency is 8.0 kHz.

$$\text{Sampling frequency} = \frac{\text{Master clock frequency}}{1024} = \frac{8.192\text{MHz}}{1024}$$
$$= 8.0\ (\text{kHz})$$

In the SBC method, 96 sampled frequencies are grouped into one frame, and coded on the frame basis. Data quantity per frame can be selected out of the following three types of bit rate.

Bit rate	Data quantity per one frame
16.0 kbps	24 byte (192 bit)
12.6 kbps	19 byte (152 bit)
10.0 kbps	15 byte (120 bit)

@fosc=8.192MHz

For example, when the data quantity is 24 bytes, the bit rate is calculated as follows:

$$\text{Bit rate} = \frac{\text{Data quantity per one frame}}{\text{Time per one frame}} = \frac{\text{Data quantity per one frame}}{\text{Sampling cycle} \times 96}$$
$$= \frac{24\ \text{byte}}{1/8.0\ \text{kHz} \times 96} = \frac{192\ \text{bit}}{12.0\ \text{msec}}$$
$$= 16.0\ (\text{kbps})$$

● Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external DRAM and bit rate, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K bits)}}{\text{Bit rate (kbps)}}\ (\text{seconds})$$

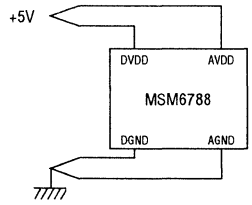
For example, if the bit rate is 10 kbps and successive 8Mbit DRAM is used, the recording time can be obtained as follows.

$$\text{Recording time} = \frac{1.024 \times (8192 - 64)}{10} = 832\ \text{seconds}$$
$$= 13\ \text{minutes}\ 52\ \text{seconds}$$

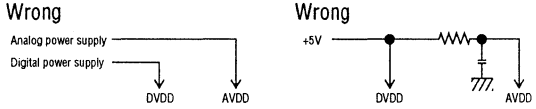
In the above equation, the memory capacity is obtained by subtracting the memory capacity (64Kbits) for the channel index area from the total memory capacity.

● Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6788 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.



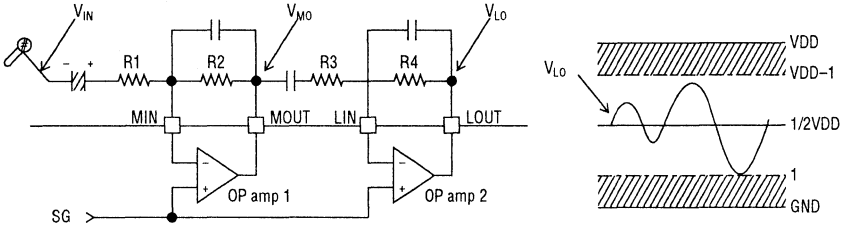
Do not supply the power to the logic portion and the analog portion from the separate power sources. Otherwise, a problem such as latch-up may occur.



● Analog Input Amplifier Circuit

This MSM6788 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \cdot R4}{R1 \cdot R3} V_{IN} \ (V)$$

During the time the recording operation is performed, the output V_{LO} of OP amp 2 is connected to the input FIN of the built-in LPF. The FIN allowable input voltage (V_{FIN}) ranges from 1V to (V_{DD} – 1)V. Therefore, the amplification ratio must be adjusted so that the V_{LO} amplitude can be within the FIN allowable input voltage range.

For example, if V_{DD} = 5V, V_{LO} becomes 3 V_{p-p} max. If V_{LO} exceeds the FIN allowable input voltage range, the output of the LPF will be a clipped waveform.

The load resistance R_{OUTA} of the OP amp is 200 kΩ minimum, so that the feedback resisters R2 and R4 of the inverting amplifier circuit must be 200 kΩ or more.

● Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6788, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

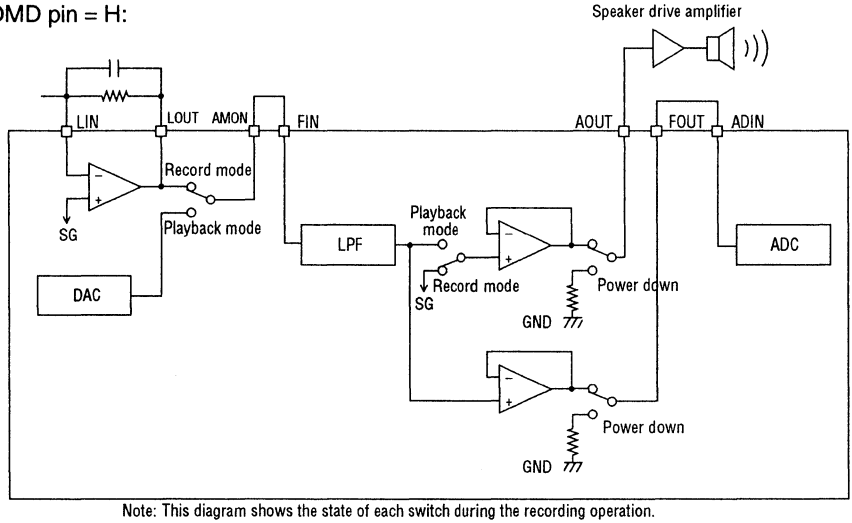
When PDMD pin = H:

Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)

When PDMD pin = L:

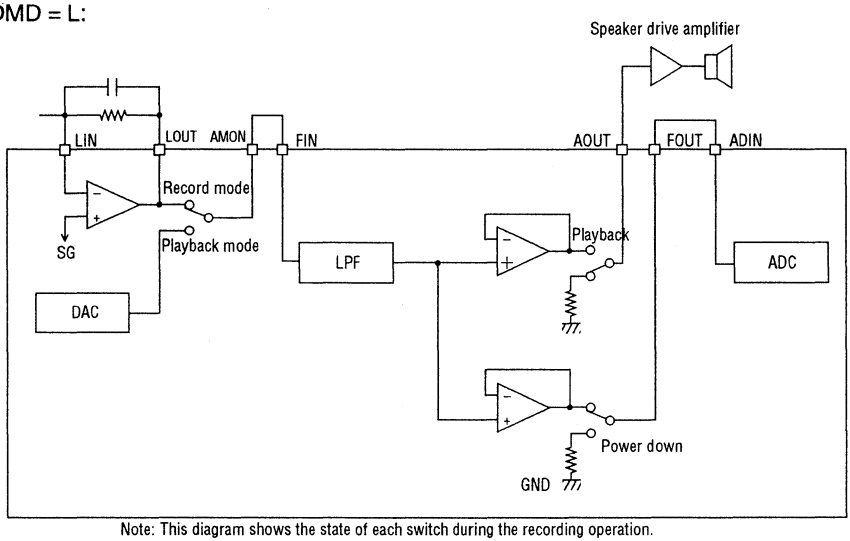
Analog pin	At power down	During operation	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	GND level	LPF output (playback waveform)

When PDMD pin = H:



Note: This diagram shows the state of each switch during the recording operation.

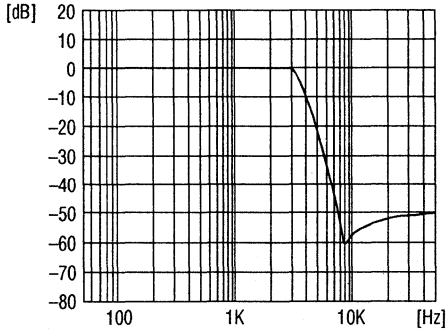
When PDMD = L:



Note: This diagram shows the state of each switch during the recording operation.

● LPF Characteristics

This LSI contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.



LPF Frequency Characteristics (fsamp = 8.0 kHz)

● Reset Function

By applying a high level to the RESET pin, the MSM6788 stops frequency oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

If a high level is applied to the RESET pin during record/playback operation , the MSM6788 is set to the power-down state and initialized state, so that voice data becomes undefined.

The following shows the power-down state of the MSM6788.

(1). Frequency oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) $\overline{CS1}$ ~ $\overline{CS4}$ pins are set to a high level to minimize the current consumption of external DRAMs and serial voice ROMs.

(4) The state of the output pins are as follows.

SADX, $\overline{SAS}$, $\overline{TAS}$, $\overline{CS1}$~ $\overline{CS4}$, $\overline{WE}$, $\overline{RWCK}$, and NAR pins: .....High level
SADY, MON pin: .....Low level
AOUT and FOUT pins: .....Ground level

After powering up the MSM6788, be sure to initialize it by applying a high level to the RESET pin.

● Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6788 may be set to the power-down state, in which the frequency oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external DRAMs. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6788 is powered down ($\overline{\text{PDWN}}$ = L) during the record/plaback operation: The record/plaback operation is stopped. After the release of the power-down state, the postprocessing will be performed.

(2) When the MSM6788 is prowered-down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporalily stopped and will be restarted after the release of the power-down state.

(3) When the MSM6788 is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level is in progress: This transition operation is temporalily stopped and will be continued after the release of the power-down state.

● Record/Playback Control Mode

Either record/plaback mode or ROM playback mode can be selected through the ROM pin as described below.

ROM pin	Record/plaback control mod
L	Record/plaback
H	ROM playback

1. Record/playback

The recorded voice data is stored in DRAMs. The recording area is indirectly allocated to each phrase by setting the phase specifying pins CA0 to CA5 (63 phrases). The recording area for each phrase is managed by the MSM6788 as described below.

The total memory capacity of the connected external DRAMs is equally devided into 256 memory blocks. When recording is performed, voice data is written into the memory blocks unused by other phrases. When a specified phase is deleted, the blocks used by this phrase become unused blocks.

When recording is performed, voice data is written in the memory area consisting of the memory blocks used by this phase and the unused memory blocks.

The memory capacity of one memory block and the number of initially available memory blocks (recording time) vary according to the total memory capacity of the connected DRAMs.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity		8M bits	16M bits	24M bits	32M bits
Memory capacity of one block		32K bits	64K bits	128K bits	128K bits
Recording time of one block	16kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	12.6kbps	2.6 seconds	5.2 seconds	10.3 seconds	10.3 seconds
	10.0kbps	3.3 second	6.6 seconds	13.1 seconds	13.1 seconds
Number of initially available blocks		254	255	191	255

2. ROM playback

For playback of the voice data stored in the connected serial voice ROM, the playback area is allocated indirectly to each fixed message phase by setting phrase specifying pins CA0 to CA5 (63 phases).

The start address, stop address, sampling frequency, and bit rate which specify the playback area for each phase are written in the index area of the serial voice ROM. When the plaback operation is started, these data fetched into the MSM6788.

● Deleting phrases

1. Deleting all phrases

All 63 phrases ch01 through ch3F can be deleted by specifying ch00 and applying a low pulse to the $\overline{DEL}$ pin. When all phrases are deleted, all phreases ch01~ch3F (63 phrases) go to the unrecorded status and, at the same time, the initial data for address control is written in the DRAMs. Therefore, whenever the MSM6788 is powered up, delete all phrases after applying a high level to the RESET pin.

2. Deleting a specified phrase

By specifying one of ch01~ch3F phrases and applying a low level to the $\overline{DEL}$ pin, the specified phrases can be deleted and put to the unrecorded state. The blocks for the deleted blocks are added to available unused blocks (available recording time).

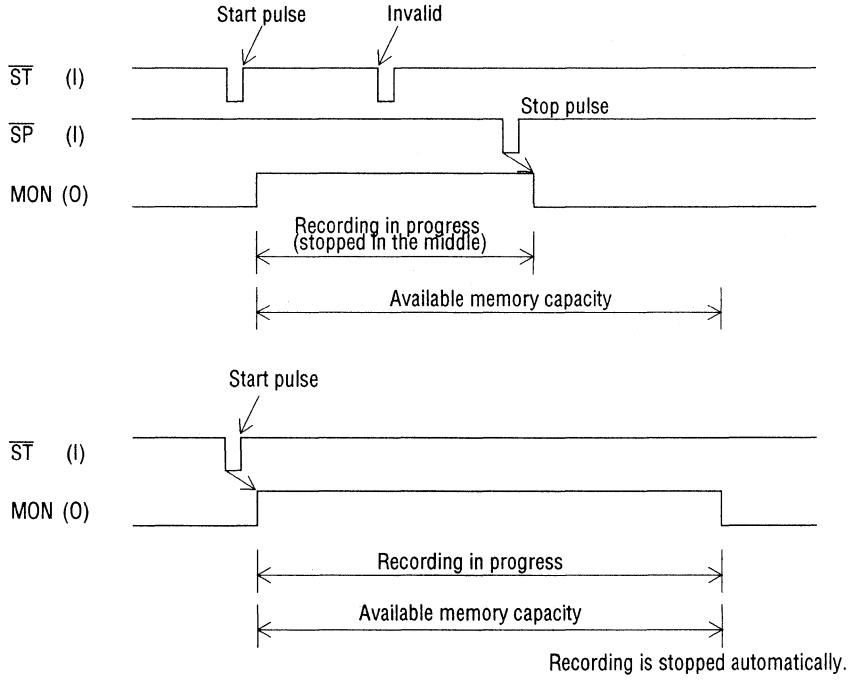
● Recording Method

Whenever the MSM6788 is powered up, be sure to delete all phrases after applying a high level to the RESET pin. Then, start the recording operation.

(1) Set recording conditions at the relevant pins.

ROM pin:	Low level
REC/$\overline{\text{PLAY}}$ pin:	High level
VDS pin:	Selection of voice activation recording (high level enables voice activation and low level disables voice activation.)
BR0, BR1 pins:	Select the SBC bit rate.
CA0 ~ CA5 pins:	Specify one of 63 phrases ch01 ~ ch3F.

(2) To start recording, apply a low pulse to the $\overline{\text{ST}}$ pin.
To stop recording in progress, apply a low pulse to the $\overline{\text{SP}}$ pin. When recording continues to the end of the memory capacity, recording is automatically stopped. In case of re-recording, voice data will be written in the memory block used by the specified phrase and unused memory blocks. Therefore, the voice data is overwritten on the previously recorded contents. The MON pin outputs a high level during recording.



● Playback Method

(1) Set playback conditions at the relevant pins.

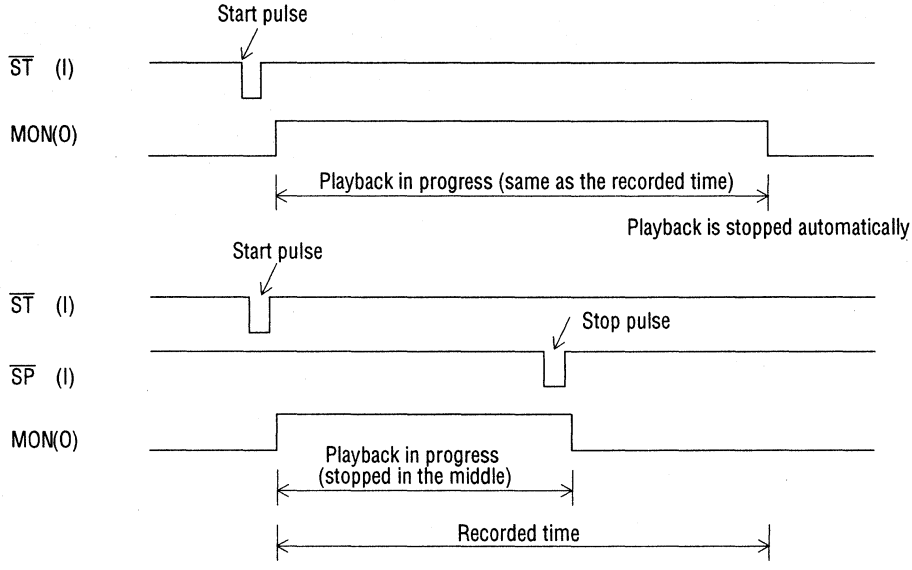
ROM pin:	Low level
REC/PLAY pin:	Low level
BR0, BR1 pins:	Select the SBC bit rate.
CA0~CA5 pins:	Specify one of 63 phrases ch01~ch3F.

(2) To start playback, apply a low pulse to the $\overline{ST}$ pin.

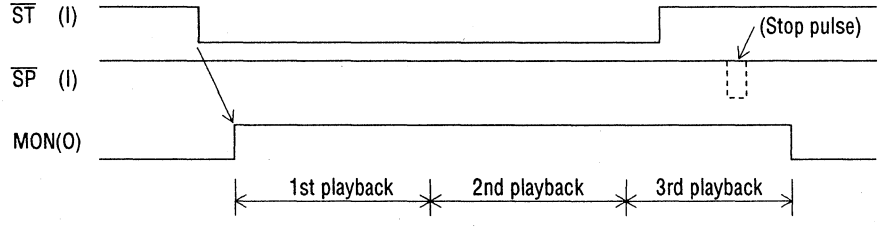
When playback for the duration of the recorded data is finished, the playback is stopped automatically.

To stop playback in progress, apply a low pulse to the $\overline{SP}$ pin.

The MON pin outputs a high level during playback.



By maintaining the $\overline{ST}$ pin at a low level, repeated playback is possible.



● ROM Playback Method

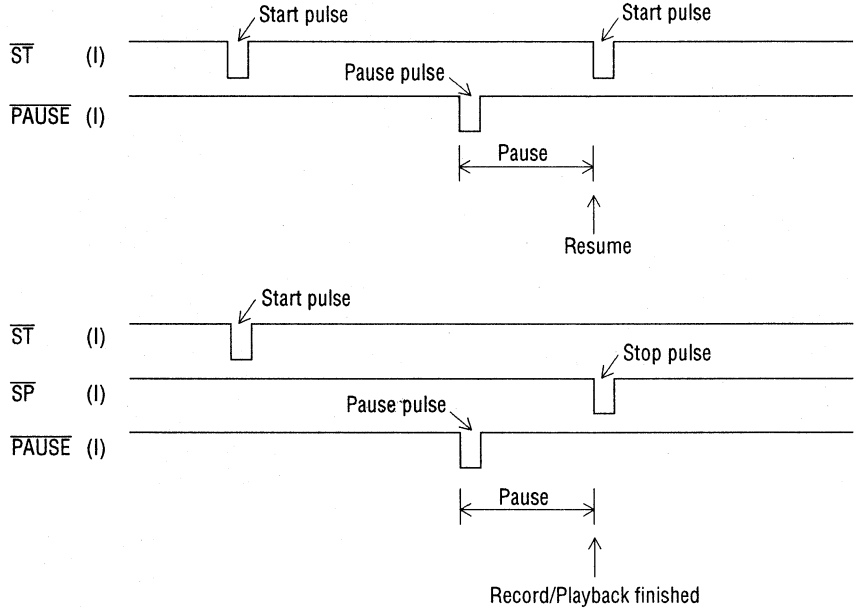
(1) Apply a high level to the ROM pin.

(2) Specify one of 63 phrases ch01 ~ ch3F by setting the CA0 ~ CA5 pins.

(3) To start playback, apply a low pulse to the $\overline{ST}$ pin. To stop playback in progress, apply a low pulse to the $\overline{SP}$ pin.

● Method of Stopping Temporarily Record/Playback by Pause Function

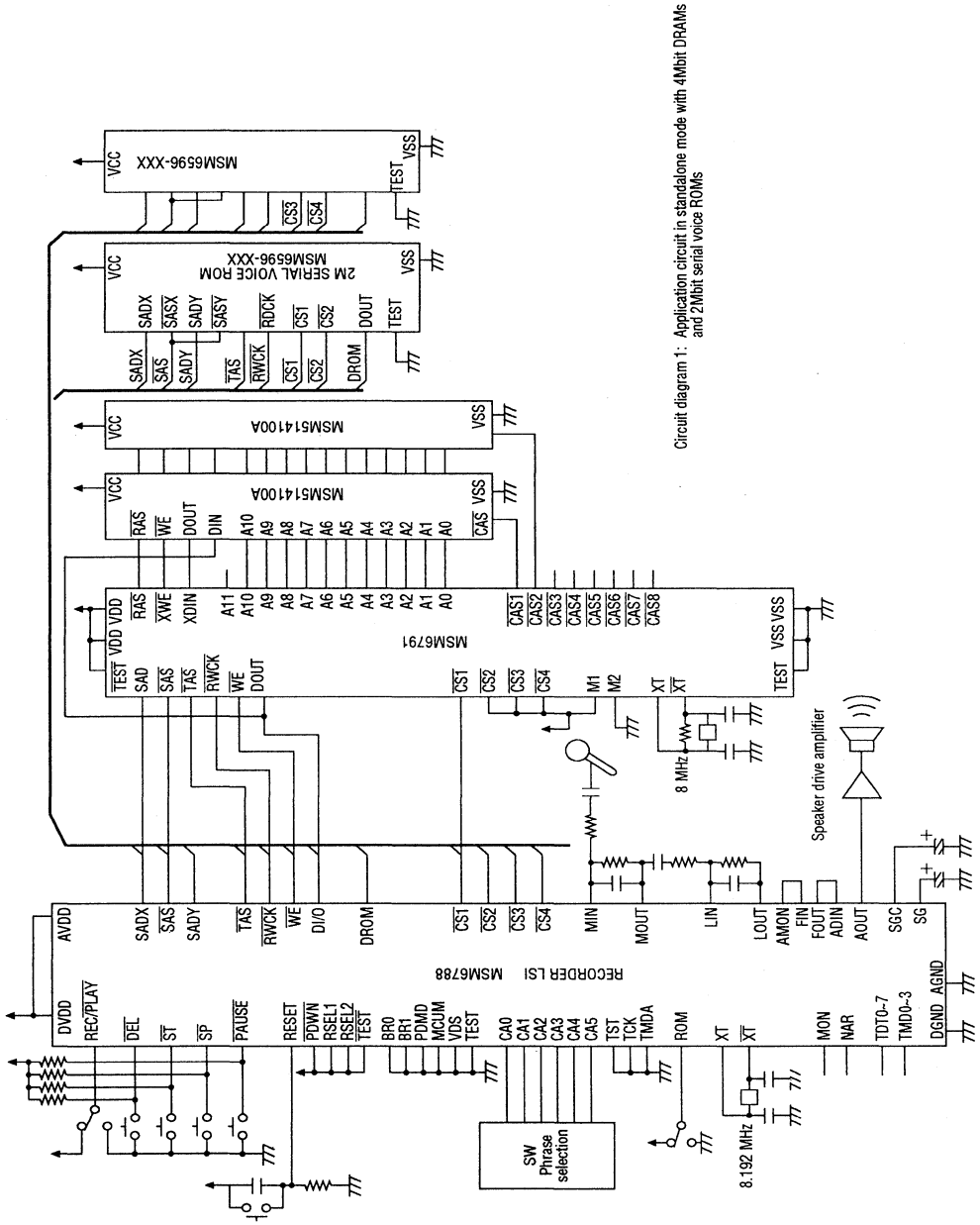
By applying a low pulse to the $\overline{\text{PAUSE}}$ pin during record/playback, record/playback operation can be stopped temporarily. To resume record/playback, apply a low level to the $\overline{\text{ST}}$ pin. To stop record/playback, apply a low pulse to the $\overline{\text{SP}}$ pin.



When record/playback is resumed after temporary stop, the voice activating circuit is not operated and recording is started when a start low pulse is applied to $\overline{\text{SP}}$ pin.

■ EXAMPLE OF APPLICATION CIRCUIT

● The circuit diagram 1 shows an application circuit example, which the MSM6788 is used in the standalone mode , and two 4Mbit DRAMs are used as record/playback memories by connecting a DRAM interface LSI,MSM6791, and two 2Mbit serial voice ROMs also are connected .



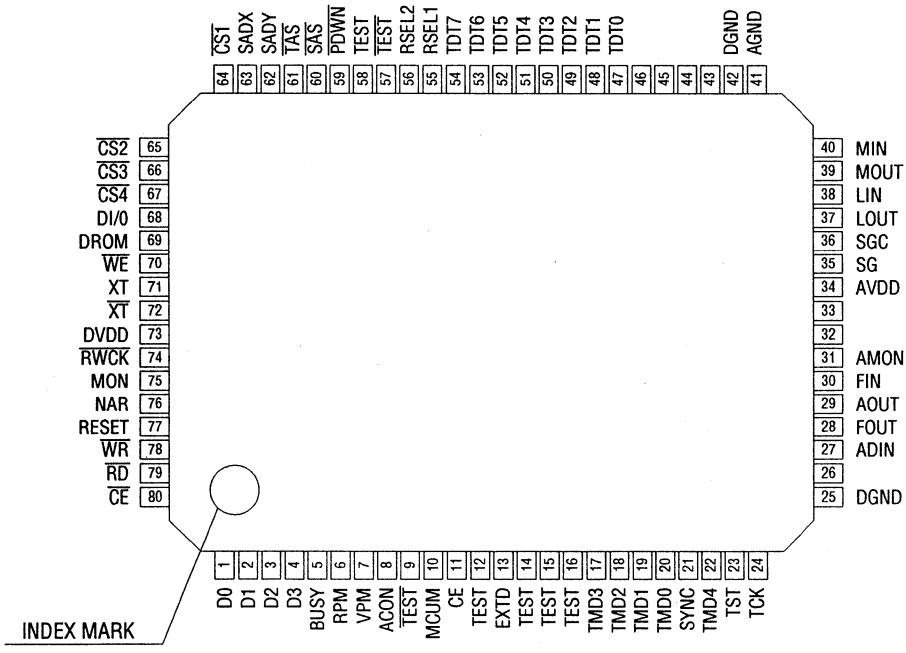
(2) MICROCONTROLLER INTERFACE MODE

■ FEATURES

- SBC method
- Built-in 12bit AD converter
- Built-in 12bit DA converter
- Built-in microphone amplifier
- Built-in low-pass filter
  Attenuation characteristics –40 dB/oct
- External memories
  DRAM maximum 32M bits (for variable messages)
  1/4/16M bit DRAMs (× 1 bit configuration) are controlled by DRAM interface LSI (MSM6791)
  Serial voice ROMs, maximum 4M bits (for fixed messages)
  1M bit serial voice ROM (MSM6595), directly addressable
  2M bit serial voice ROM (MSM6596), directly addressable
  3M bit serial voice ROM (MSM6597), directly addressable
- Bit rate
  10.0k, 12.6k, 16.0kbps (at 8kHz sampling freq.)
  7.5k, 9.5k, 12.0kbps(at 6kHz sampling freq.)
- Number of phrases
  63 phrases for variable messages
  255 phrases for fixed messages
- Maximum recording time (when external 32M bit RAM is connected)
  13.8 minutes (for 10.0kbps SBC) 18.4 minutes (for 7.5 kbps SBC)
  11.0 minutes (for 12.6kbps SBC) 14.6 minutes (for 9.5 kbps SBC)
  8.5 minutes (for 16.0kbps SBC) 11.5 minutes (for 12.0 kbps SBC)
- Voice activation function
- Pause function
- Master clock frequency: 6.0MHz ~ 8.192 MHz
- Power supply voltage: 5 V single power supply
- Package: 80-pin plastic QFP (QFP80-P-1420-V1K)

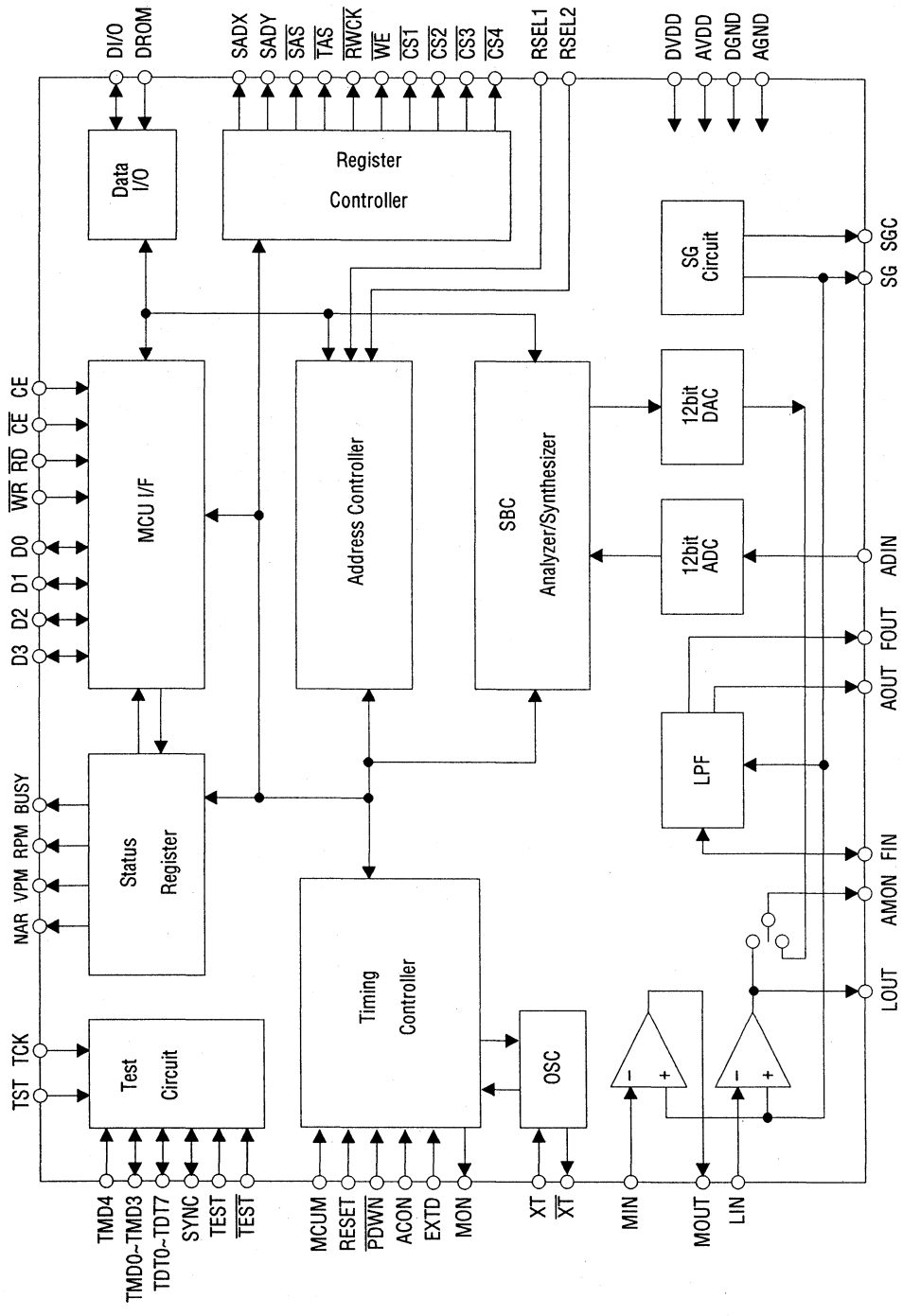
■ PIN LAYOUT (TOP VIEW)

80 LEAD PLASTIC FLAT PACKAGE



NC: No connection (Open)

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta=25°C	−0.3~7.0	V
Input voltage	V_{IN}	Ta=25°C	−0.3~VDD+0.3	V
Storage temperature	T_{stg}	–	−55~+150	°C

● Operating Range

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	DGND=AGND=0V	+3.5~+5.5	V
Operating temperature	T_{op}	–	0~+70	°C
Master clock frequency	fosc	–	6.0~8.192	MHz

● DC characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	—	0.8×VDD	—	—	V
Low input voltage	V_{IL}	—	—	—	0.2×VDD	V
High output voltage	V_{OH}	I_{OH} = −40μA	VDD−0.3	—	—	V
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
High input current (Note 1)	I_{IH1}	V_{IH} = VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH} = VDD	—	—	20	μA
Low input current (Note 1)	I_{IL1}	V_{IL} = GND	-10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL} = GND	-20	—	—	μA
Operating current consumption (1)	I_{DD}	fosc = 8 MHz, no load	—	15	30	mA
Operating current consumption (2)	I_{PD}	At power down. no load	—	—	10	μA

Note 1: Applies to all input pins excluding the XT pin.
Note 2: Applies to the XT pin.

● Analog Characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DA output relative error	$\|V_{DAE}\|$	no load	—	—	10	mV
FIN admissible input voltage range	V_{FIN}	—	1	—	VDD-1	V
FIN input impedance	R_{FIN}	—	1	—	—	MΩ
Op-amp open loop gain	G_{OP}	f_{IN} = 0~4kHz	40	—	—	dB
Op-amp input impedance	R_{INA}	—	1	—	—	MΩ
Op-amp load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT load resistance	R_{FOUT}	—	50	—	—	kΩ

● AC Characteristics

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=8.192MHz f_{sam}=8.0kHz

Item		Symbol	Min.	Typ.	Max.	Unit
RESET pulse width		t_{RST}	1	–	–	µs
RESET execution time	(Note 1)*	t_{REX}	–	1	–	ms
$\overline{PDWN}$ low level time	*	t_{PDL}	250	–	–	µs
$\overline{PDWN}$ high level time	*	t_{PDH}	250	–	–	µs
Oscillating time after input of $\overline{PDWN}$	*	t_{PX}	125	–	250	µs
BUSY time after release of $\overline{PDWN}$	(Note 1)*	t_{BPD}	0.25	–	80	ms
$\overline{RD}$ pulse width		t_{RR}	200	–	–	ns
Setup and hold time of $\overline{CE}$ and CE for $\overline{RD}$		t_{CR}	30	–	–	ns
Time from $\overline{RD}$ fall to data valid		t_{DRE}	–	–	200	ns
Time from $\overline{RD}$ rise to data float		t_{DRF}	–	10	50	ns
$\overline{WR}$ pulse width		t_{WW}	200	–	–	ns
Setup and hold time of data for $\overline{WR}$		t_{CW}	30	–	–	ns
Data setup time to $\overline{WR}$ rise		t_{DWS}	100	–	–	ns
Data hold time from $\overline{WR}$ rise		t_{DWH}	30	–	–	ns
$\overline{RD}$ and $\overline{WR}$ disable time		t_{DRW}	250	–	–	ns
BUSY time after release of RESET	(Note 1)*	t_{BR}	–	–	1	ms
BUSY time after input of 1-nibble command	*	t_{B1}	–	–	16	µs
BUSY time after input of 2-nibble command	*	t_{B2}	–	–	16	µs
BUSY time after input of 3-nibble command	*	t_{B3}	–	–	16	µs
BUSY time after input of 2-nibble or 3-nibble command data	**	t_{BD}	–	–	16	µs
WAIT time after input of BLKRD command	*	t_{WBR}	270	–	–	µs
WAIT time after output of BLKRD command block data	*	t_{WDR}	50	–	–	µs
BUSY time after input of ADRWR command	*	t_{BAW}	–	–	270	µs
BUSY time after input of ADRWR command address data	*	t_{BAD}	–	–	50	µs
WAIT time after input of ADRRD command	*	t_{WAR}	270	–	–	µs
WAIT time after output of ADRRD command address data	*	t_{WDR}	50	–	–	µs
Address control time at start of record/playback	*	t_{AD1}	–	1	–	ms

Items with * are proportional to the period of master oscillator frequency fosc.

Note 1: The oscillation start-up stabilization time is added to t_{REX}, t_{BPD} and t_{BR}.
The oscillation start-up stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

DVDD=AVDD=4.5~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=8.192MHz f_{sam}=8.0kHz

Item			Symbol	Min.	Typ.	Max.	Unit
Time from input of START command to MON rise	Flex record	*	t_{STCM}	–	–	50	ms
	Flex playback	*	t_{STCM}	–	–	20	ms
	ROM playback	*	t_{STCM}	–	–	1	ms
Time from input of STOP command to MON fall	Flex record	*	t_{SPCM}	60	–	80	ms
	Flex playback	*	t_{SPCM}	1	–	15	ms
	ROM playback	*	t_{SPCM}	1	–	15	ms
Time from input of START command to setting of RPM bit		*	t_{STCR}	–	–	16	µs
Time from input of STOP command to end of record/playback		*	t_{SPCR}	–	–	15	ms
Time from input of STOP command to release of standby for voice		*	t_{SPCV}	–	–	80	ms
Time from input of START command to NAR bit fall during continuos playback		*	t_{STCN}	–	–	16	µs
Unvoiced time between phrases during continuous playback		*	t_{MID}	–	13.25	–	ms
Time from input of PAUSE command to setting of VPM bit		*	t_{PSCP}	–	–	16	µs
Time from input of START command during pause to resetting of VPM bit		*	t_{STCP}	–	–	500	µs
Time from input of STOP command during pause to resetting of VPM bit		*	t_{SPCP}	–	–	500	µs
CHRW command	WAIT time after input of command	*	t_{WCRW}	770	–	–	µs
	WAIT time after input of REC command	*	t_{WRC}	16	–	–	µs
	WAIT time after input of write data	*	t_{WWD}	50	–	–	µs
	WAIT time after input of PLAY command	*	t_{WPL}	50	–	–	µs
	WAIT time after input of STOP command	*	t_{WSP}	50	–	–	µs
DTRW and DTRD commands	WAIT time after input of command	*	t_{WRW}	16	–	–	µs
	WAIT time after input of address (2nd–5th nibbles)	*	t_{WA1}	16	–	–	µs
	WAIT time after input of address (6th nibble)	*	t_{WA2}	270	–	–	µs
	WAIT time after input of REC command	*	t_{WRC}	16	–	–	µs
	WAIT time after input of write data	*	t_{WWD}	50	–	–	µs
	WAIT time after input of PLAY command	*	t_{WPL}	50	–	–	µs
	WAIT time after input of STOP command	*	t_{WSP}	16	–	–	µs

Items with * are proportional to the period of master oscillator frequency fosc.

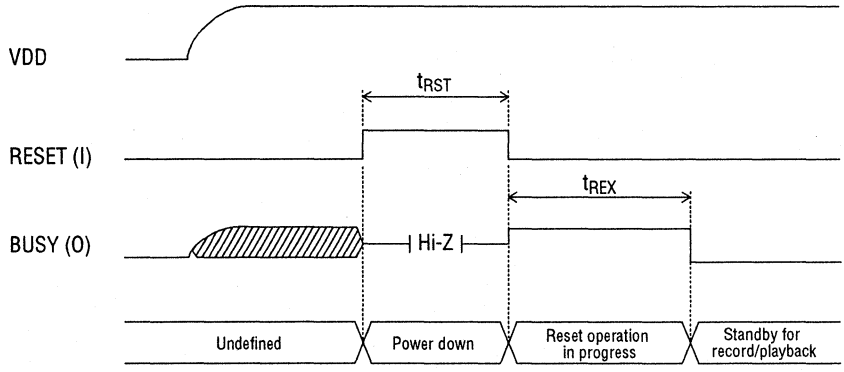
DVDD=AVDD=4.5V~5.5V
DGND=AGND=0V Ta=0~70°C
fosc=8.192MHz f_{sam}=8.0kHz

Item		Symbol	Min.	Typ.	Max.	Unit
WAIT time for deletion of all phrases after input of DEL1 command *		t_{WBLA}	550	–	–	ms
WAIT time for deletion of a specified phase after input of DEL1 command *		t_{WBLI}	70	–	–	ms
WAIT time for deletion of a specified phase after input of DEL2 command *		t_{WBLI}	70	–	–	ms
Time to start of DC level transition after input of LEV command *		t_{LV}	–	–	16	µs
DC level transition time (GND to 1/2 VDD) *		t_{AOR}	–	64	–	ms
DC level transition time (1/2 VDD to GND) *		t_{AOF}	–	64	–	ms
EXT command	Set-up/hold time of EXTD to $\overline{WR}$/$\overline{RD}$ pulse	t_{ERW}	30	–	–	ns
	MON clock cycle *	t_{ME}	–	12	–	ms
	MON high level time *	t_{MH}	–	6	–	ms
	Time from input of EXT command to RPM bit set *	t_{ER}	–	–	16	µs
	Time from input of EXT command to RPM bit reset *	t_{ESP}	–	–	250	µs
	Time from EXT command input to MON rise during recording *	t_{EMR}	15	–	16	ms
	Disable time of $\overline{RD}$ pulse of SBC data during recording *	t_{EDR}	–	–	4	µs
	Time from input of EX command to MON rise during playback *	t_{EMP}	3	–	4	ms
	Disable time of $\overline{WR}$ pulse of SBC data during playback *	t_{EDW}	–	–	4	µs
	BUSY occurence time after SBC data read/write within one frame *	t_{BER}	–	–	4	µs
	Time from SBC data read/write end to NAR reset within one frame *	t_{ENR}	–	–	4	µs

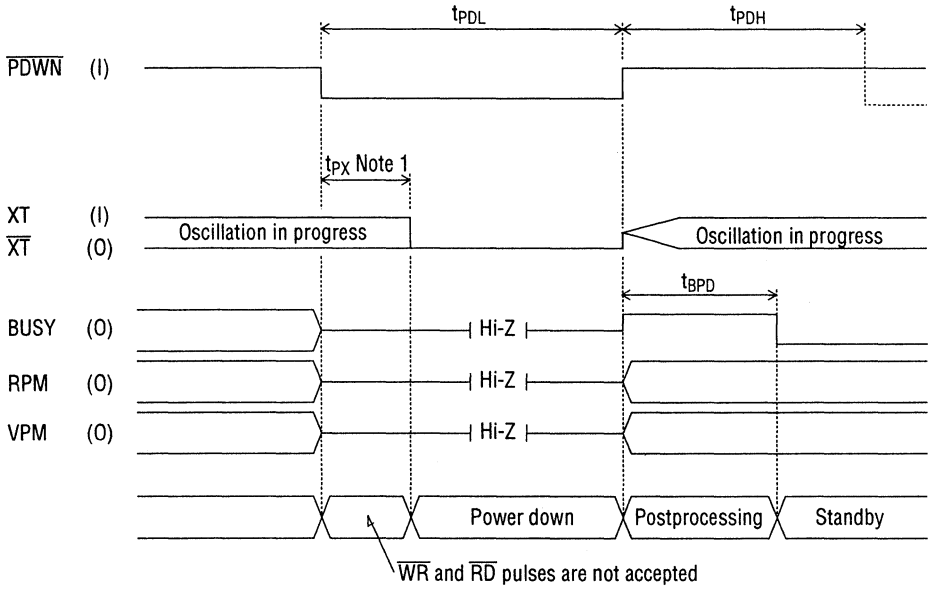
Items with * are proportional to the period of master oscillator frequency fosc.

■ TIMING DIAGRAMS

● Reset Function

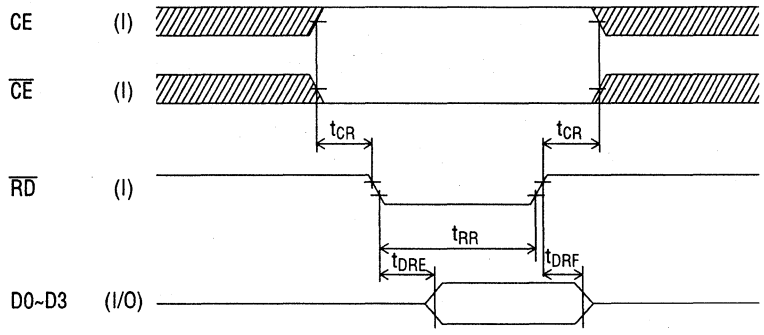


● Power Down by the $\overline{\text{PDWN}}$ pin

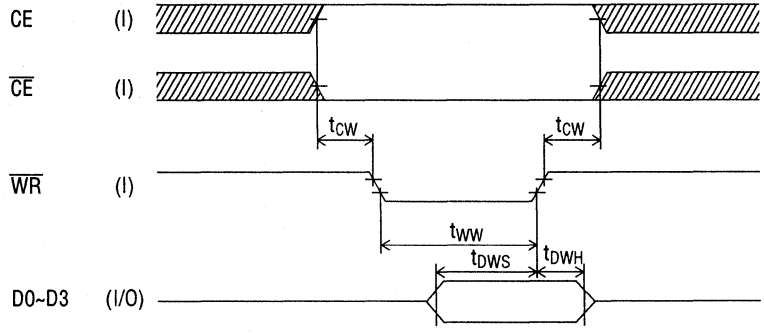


Note 1: When an external clock is used, apply a low level to the $\overline{\text{PDWN}}$ pin and then continue to apply the external clock to the XT pin for t_{PX}.

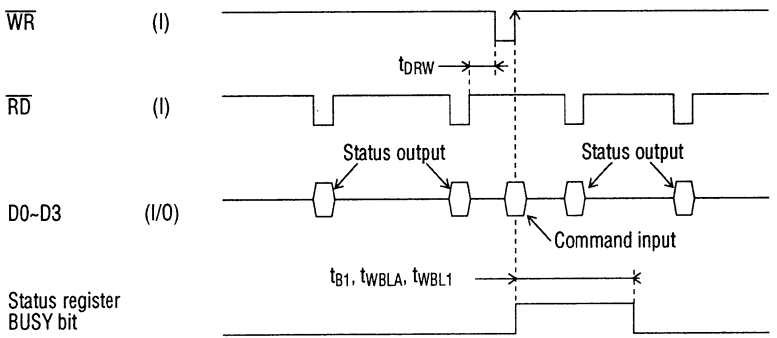
● Data Read Timing ($\overline{RD}$ Pulse)



● Data Write Timing ($\overline{WR}$ Pulse)

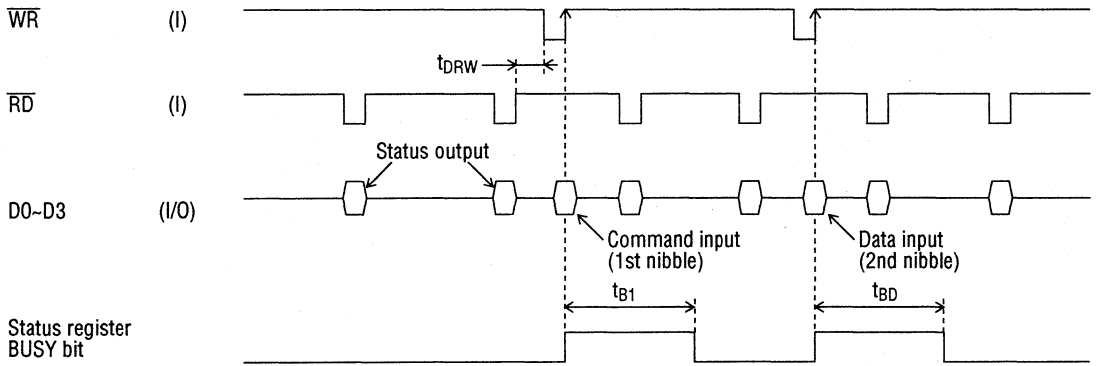


● Inputting 1-Nibble Commands (NOP, PAUSE, PLAY, REC, START, STOP, DEL1 and DEL2 Commands)



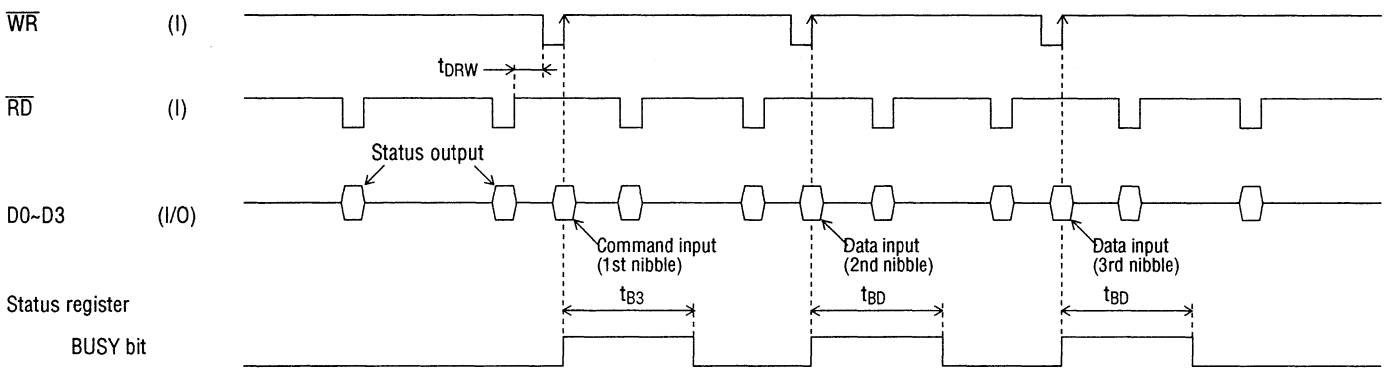
t_{B1}: NOP, PAUSE, PLAY, REC, START, and STOP commands
t_{WBLA}: DEL1 command (deletion of all phrases)
t_{WBL1}: DEL1 command (deletion of a specified phrase)and DEL2 command (deletion of tail)

● Inputting 2-Nibble Commands (BRATE, FLGWR, VDS, and LEV Commands)

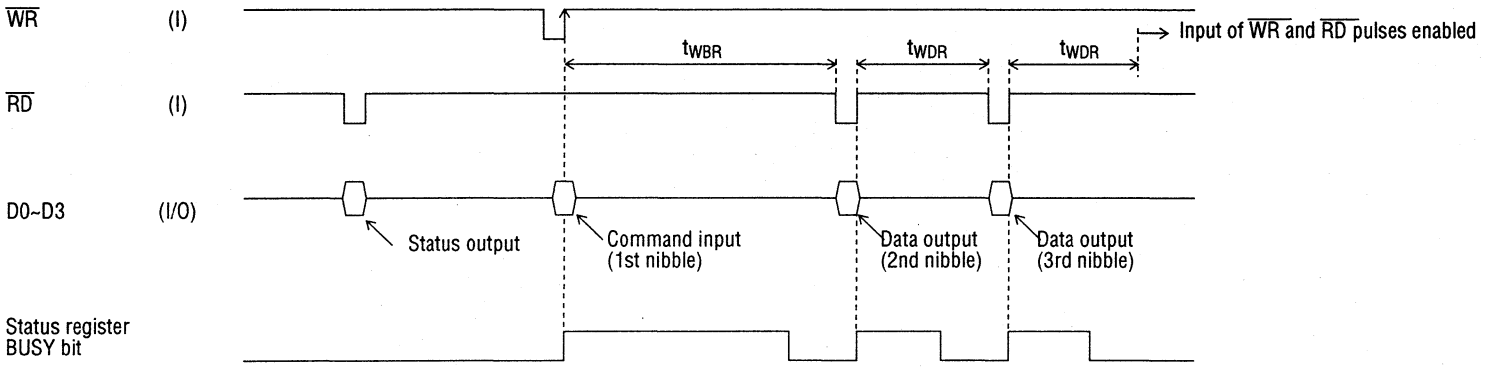


The LEV command is used to specify the playback level.
For DC level transition by the LEV command, see the timing diagram for DC level transition by the LEV command.

● Inputting 3-Nibble Commands (CHAN and BLKWR Commands)

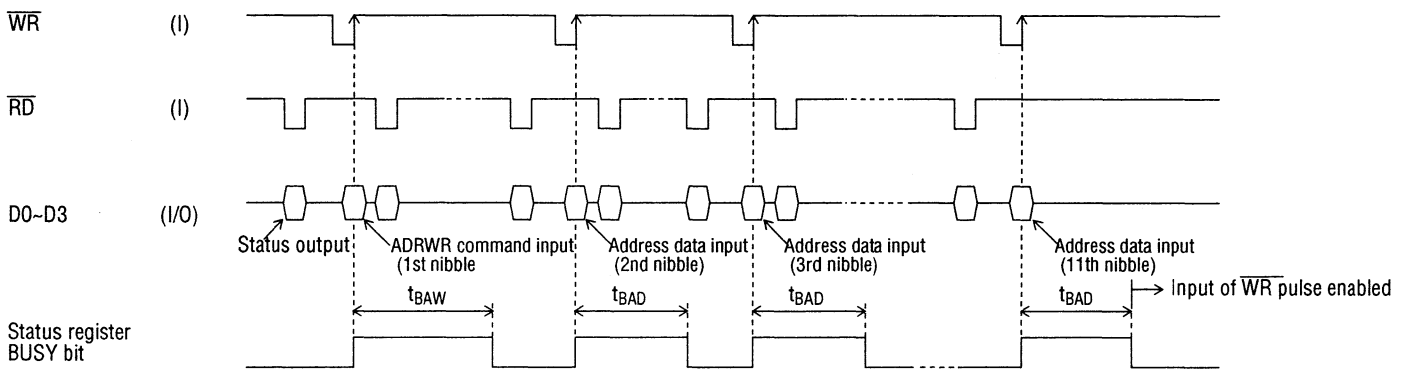


● Inputting the BLKRD1, BLKRD2 Command



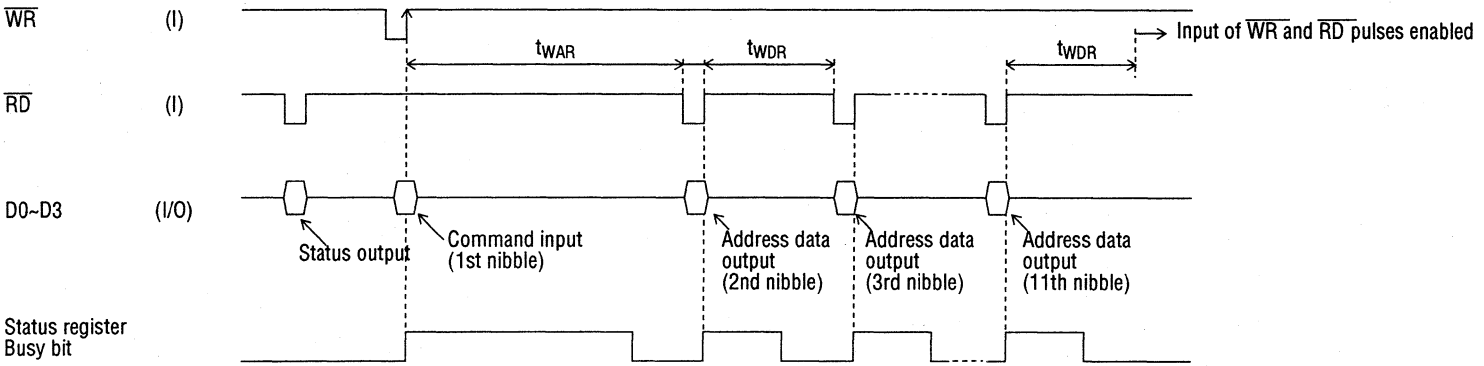
1. After making sure that the MSM6788 is not in the busy state by checking the BUSY bit of the status register, input the BLKRD command.
2. Then, the data is read according to the 2nd and 3rd nibble command data.
   However, the status of the BUSY bit connot be verified by inputting the $\overline{RD}$ pulse. Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WBR} or t_{WDR} or after verifying the BUSY state at BUSY output pin.

● Inputting the ADRWR Command



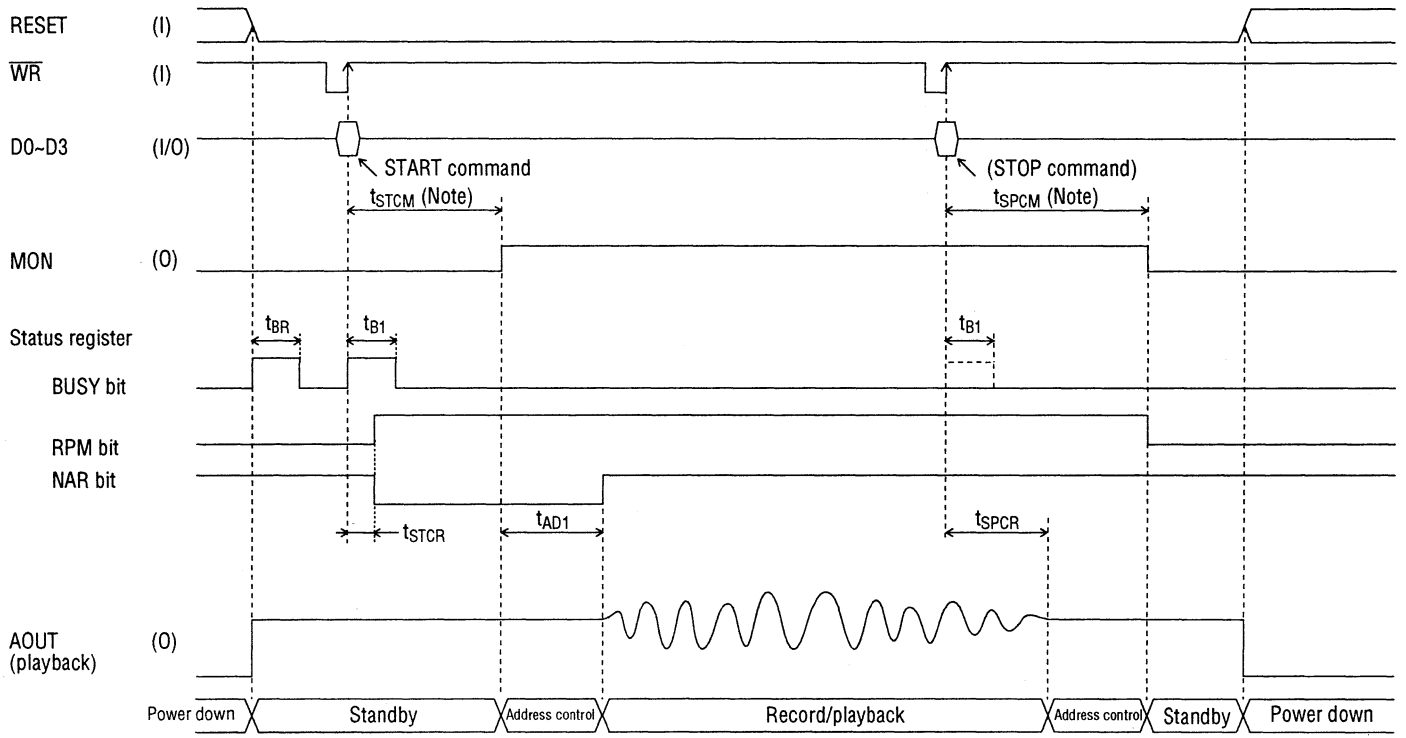
1. After making sure that the MSM6788 is not in the busy state by checking the BUSY bit of the status register, input the ADRWR command.
2. Then, input 2nd-11th nibble address data after making sure that the MSM6788 is not in the BUSY state by one on the following two methods.
   - ● Check of the BUSY bit in the status register
   - ● Input the next $\overline{WR}$ pulse after the waiting time t_{BAW} or t_{BAD}.

● Inputting the ADRRD Command



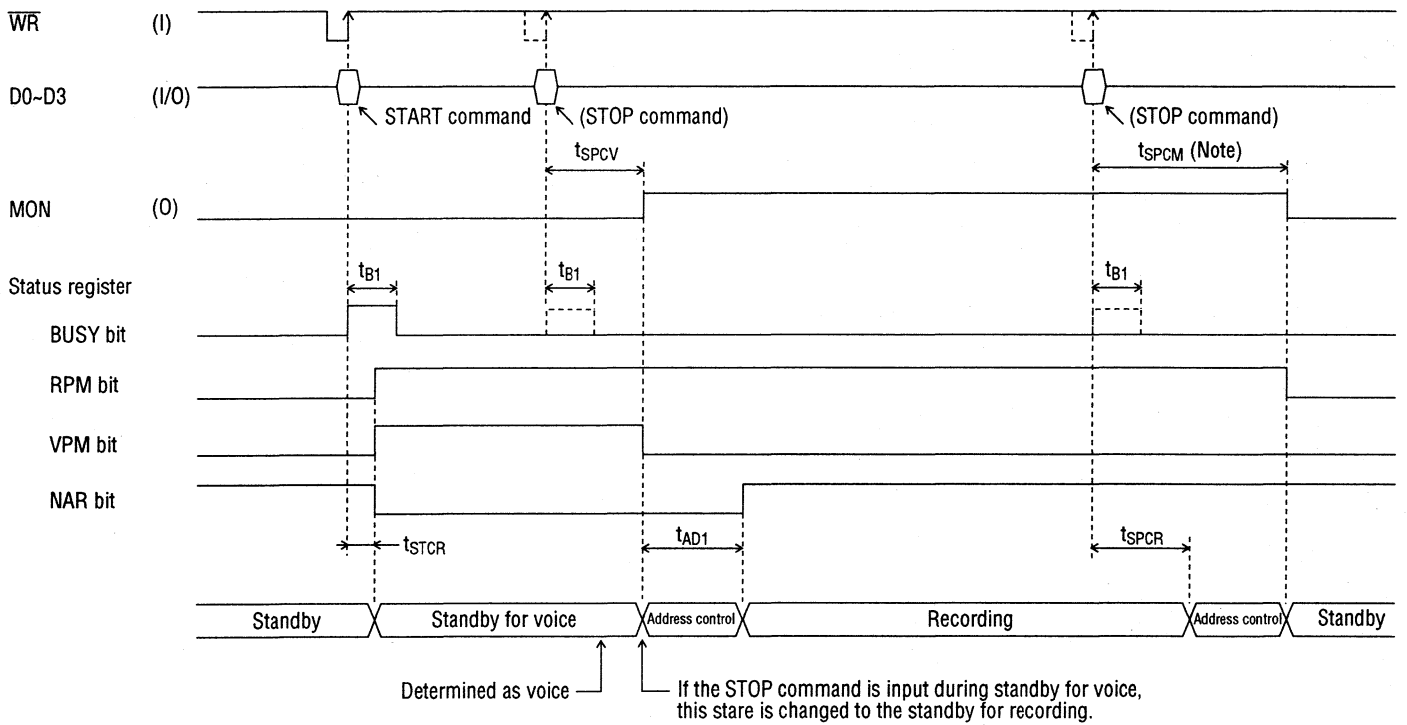
1. After making sure that the MSM6788 is not in the busy state by checking the BUSY bit of the status register, input the ADRRD command.
2. Then, the address data is read according to 2nd through11th nibble command data.
   The state of the BUSY bit cannot be checked by the $\overline{RD}$ pulse.
   Therefore, input the $\overline{RD}$ pulse either after the waiting time t_{WAR} or t_{WDR} pr after verifying the BUSY state at the BUSY output pin.

● Timing for Record/Playback by START Command

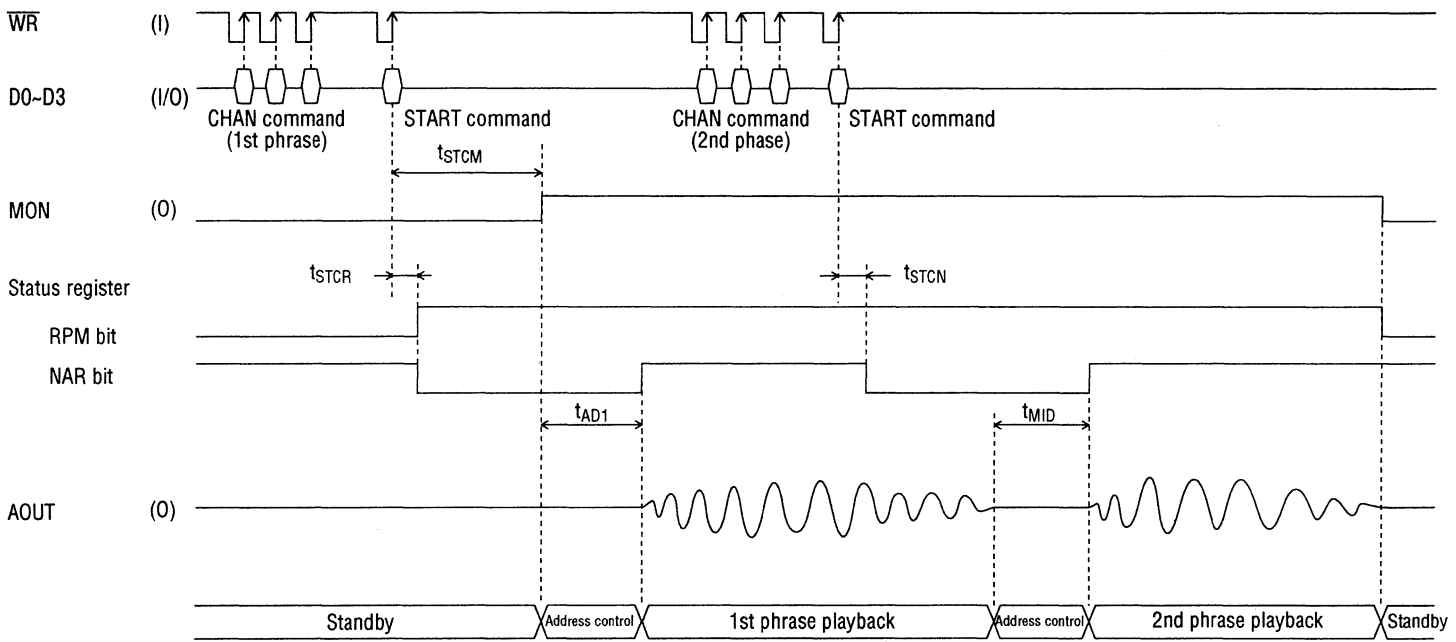


Note: t_{STCM} and t_{SPCM} vary depending on the control mode for record/playback and on record or playback mode.

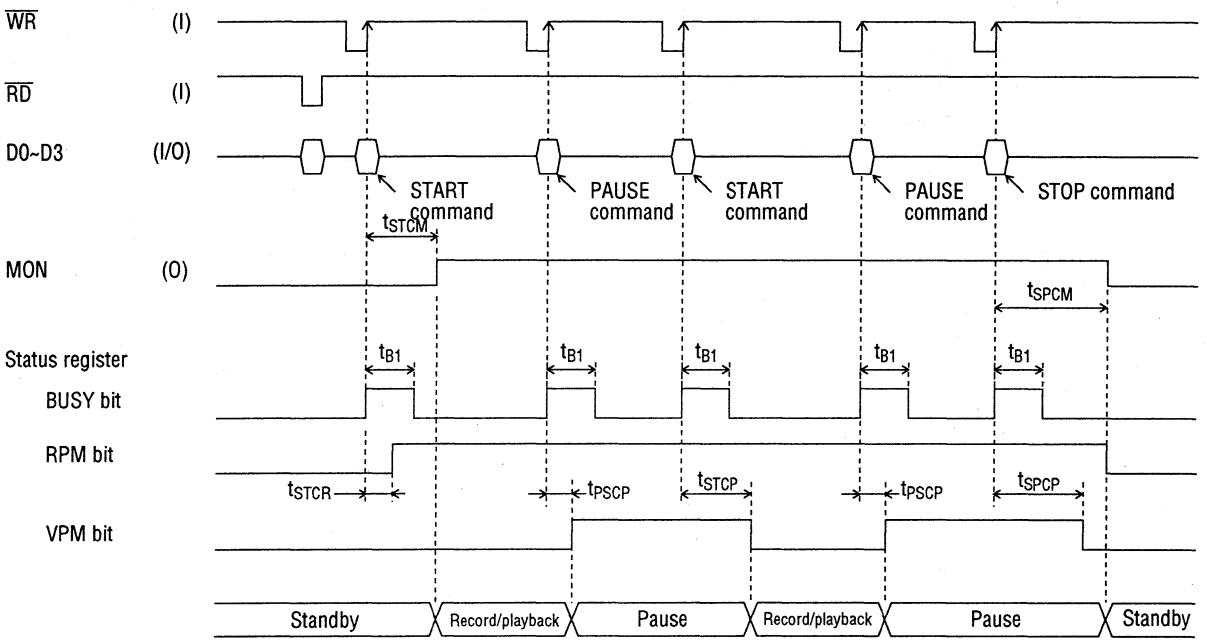
● Voice Activation Timing



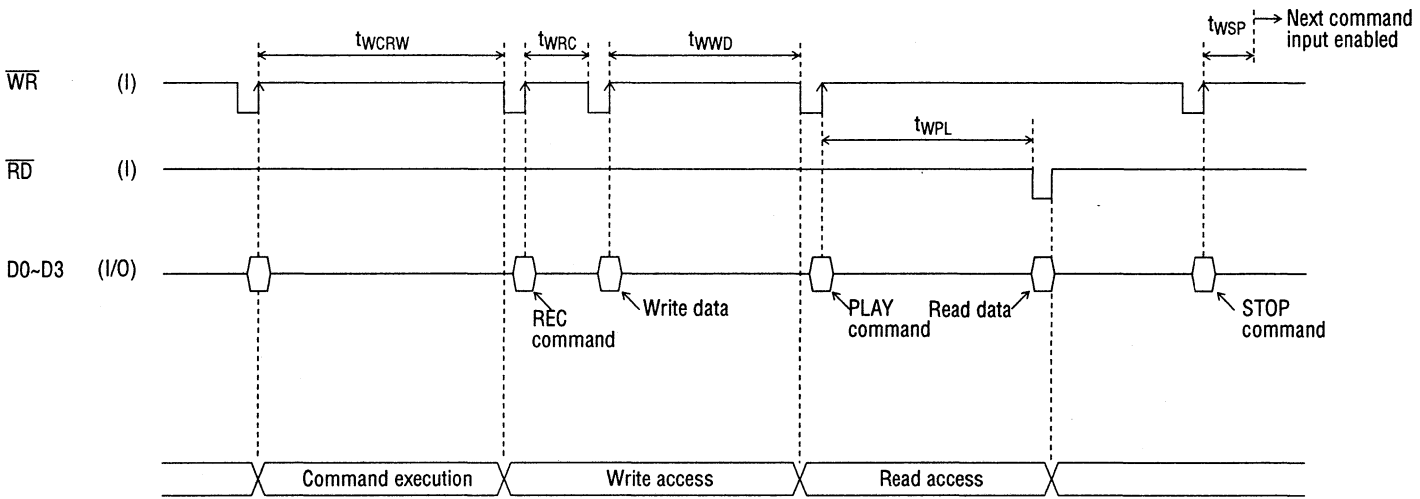
● Timing for Continuous ROM Playback



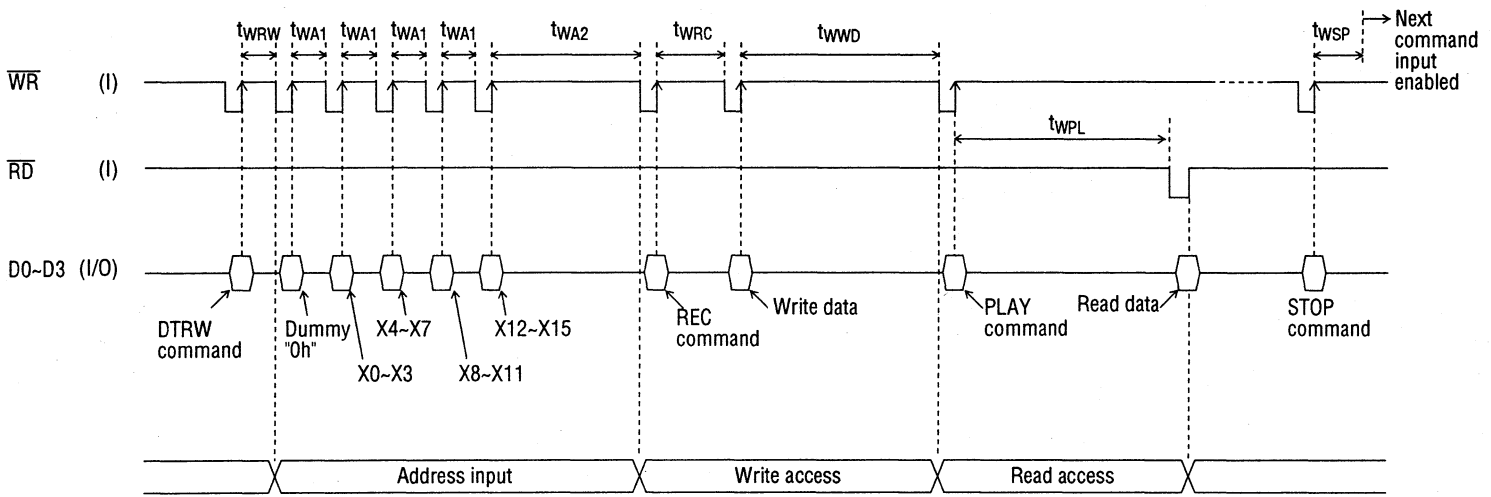
● Timing for Record/Playback Pause Operation by PAUSE Command



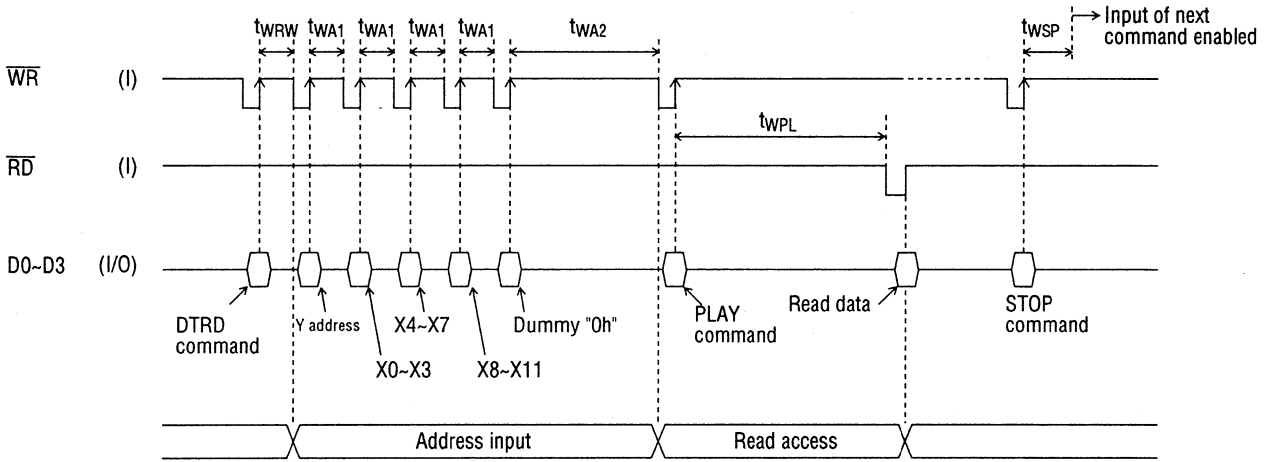
● Timing for Data Transfer by CHRW Command



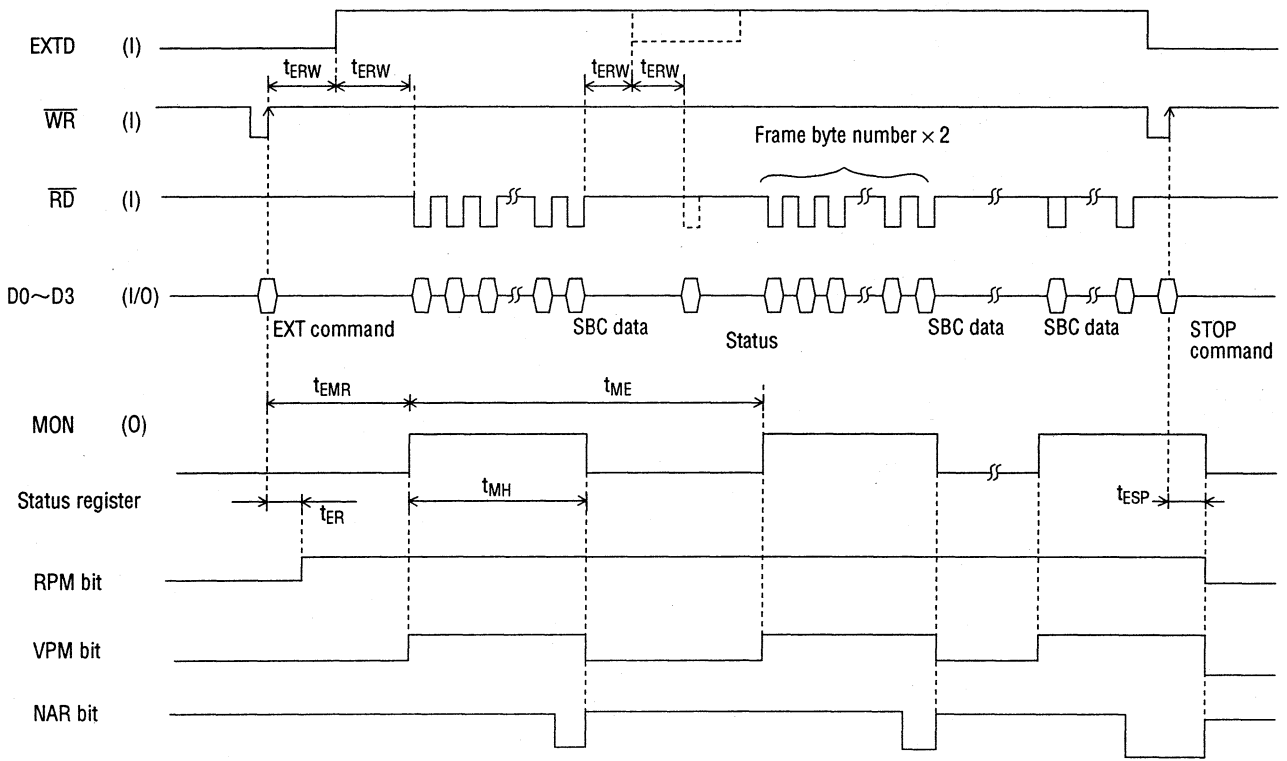
● Timing for Data Transfer by DTRW



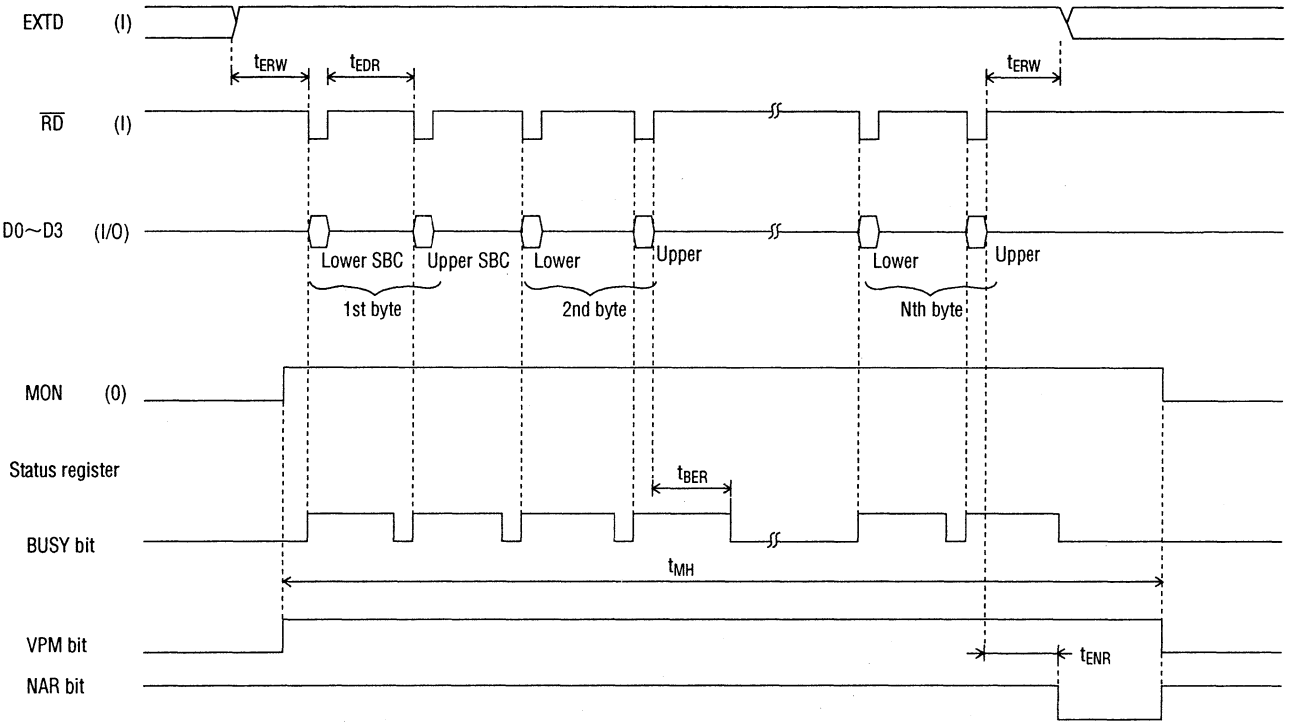
● Timing for Data Read by DTRD command



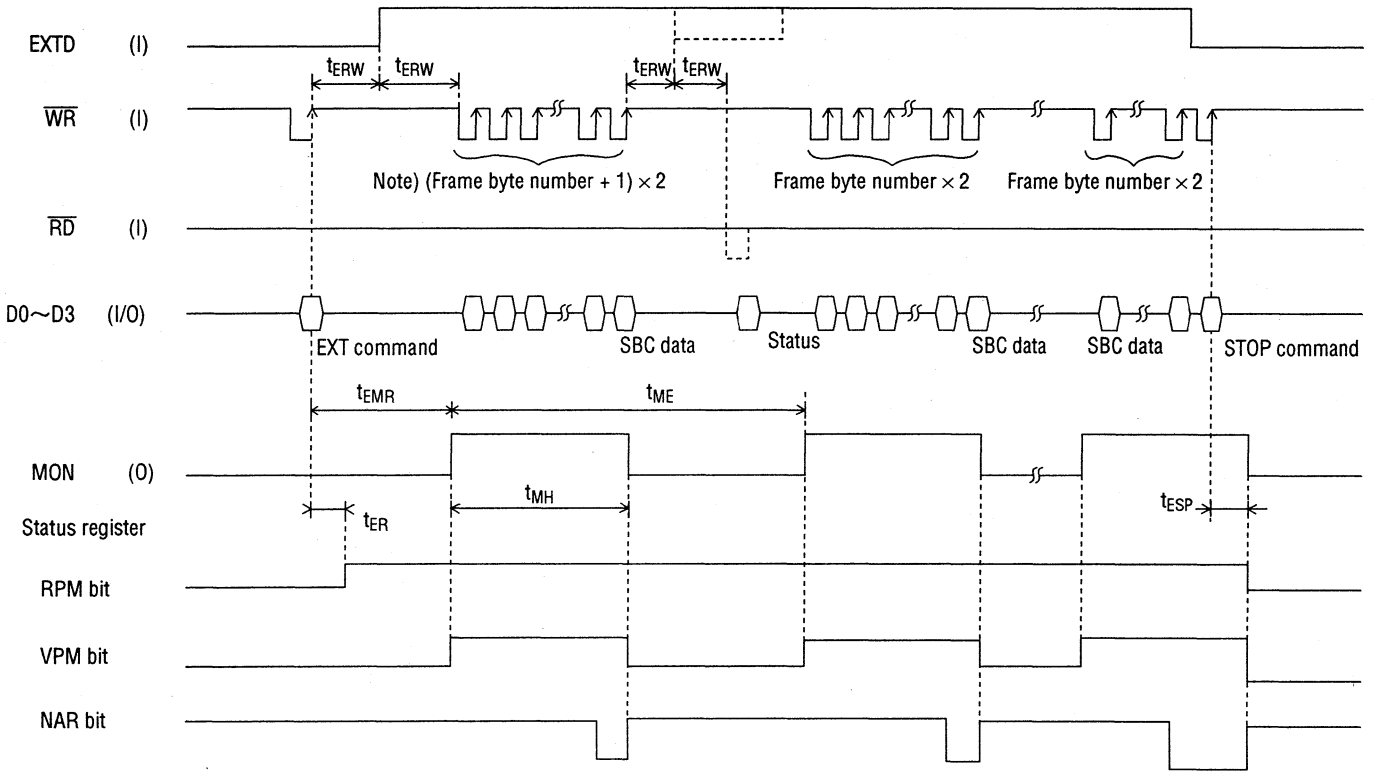
● Recording by EXT Command



● Read Access in a Frame during EXT Recording

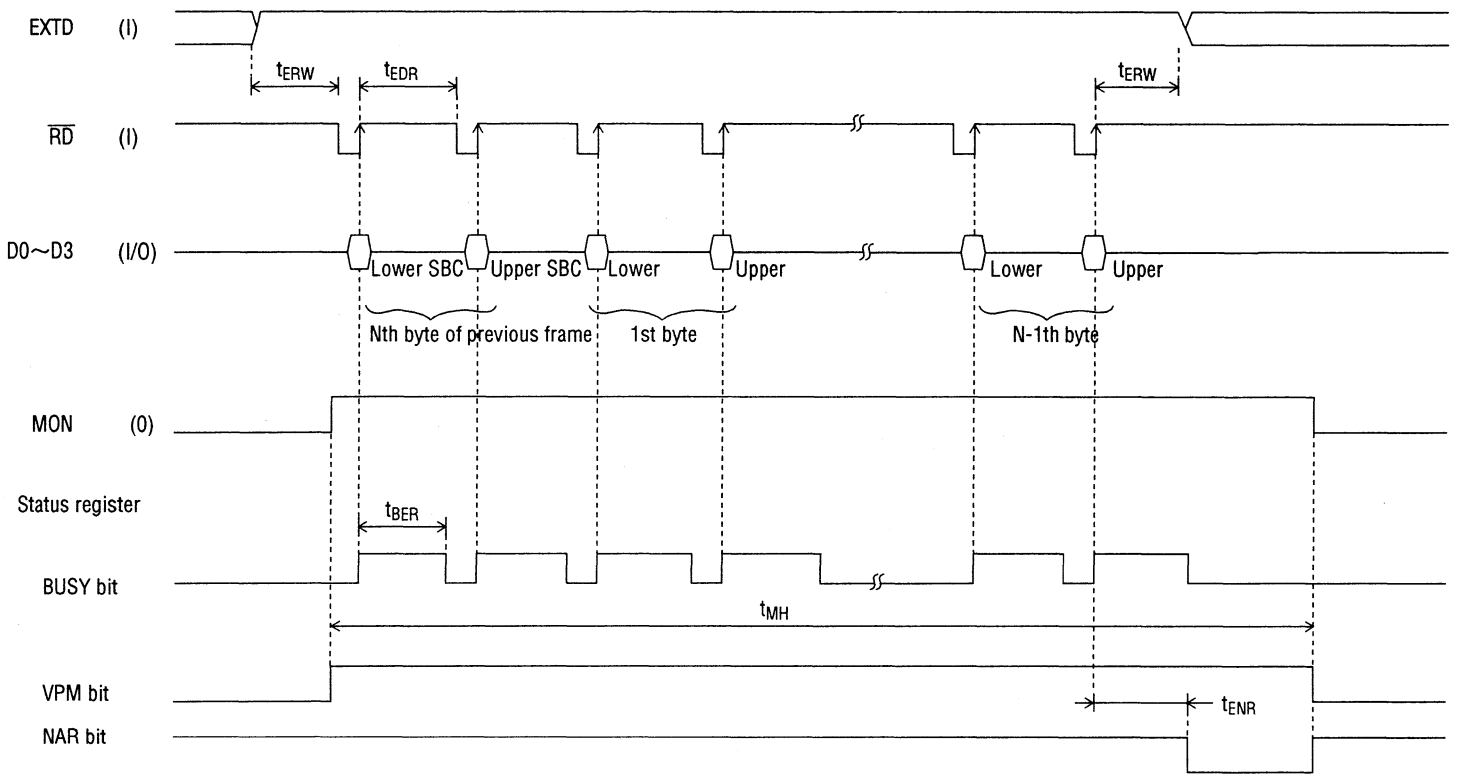


● Playback by EXT Command

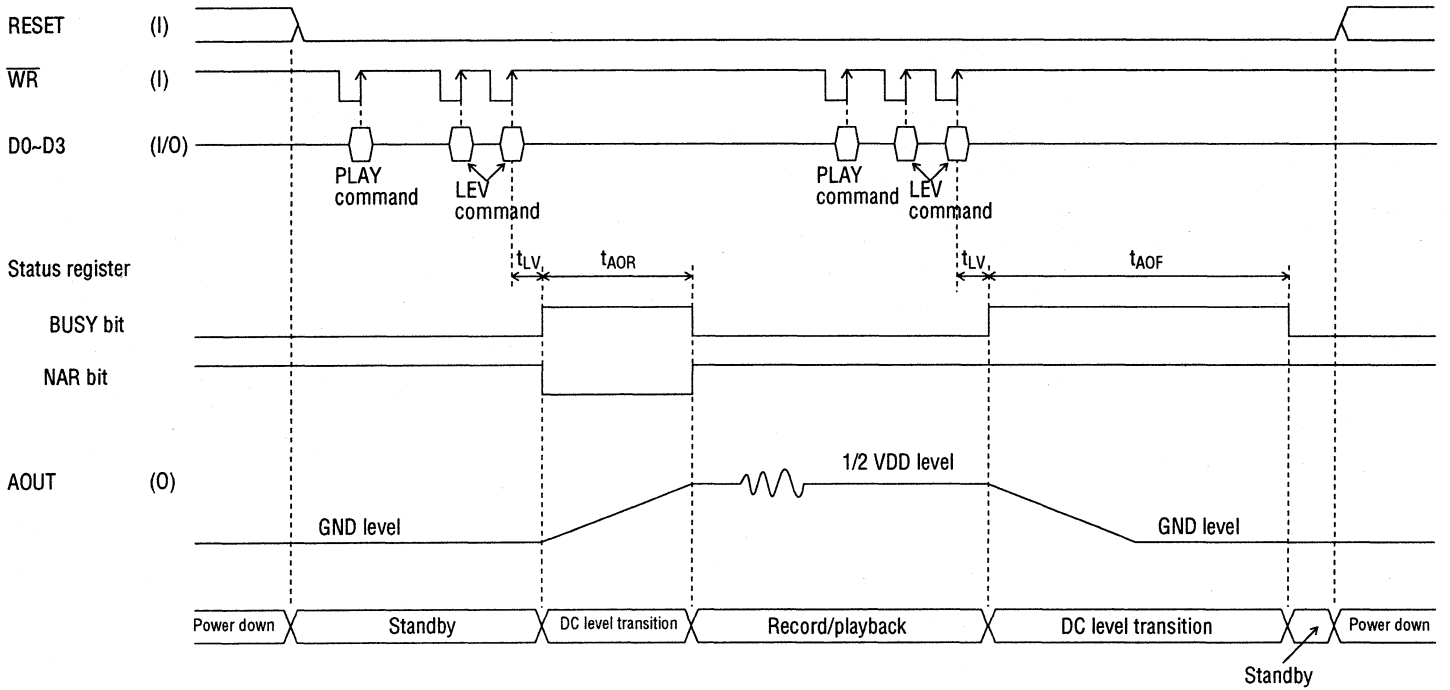


Note) During playback, the 1st frame writes (byte number in a frame + 1 byte), and the following frames writes the byte number of each frame.

● Write Access in a Frame during EXT Recording



● Timing for DC Level Transition by LEV Commnad



■ PIN DESCRIPTION

Pin Name	I/O	Pin function
DVDD	–	Digital power supply pin
AVDD	–	Analog power supply pin
DGND	–	Digital ground pin
AGND	–	Analog ground pin
SG, SGC	O	Output pin for analog circuit reference voltage (signal ground)
MIN LIN	I	Inverting input pin of the built-in OP amplifier. Non-inverting input pin is internally connected to SG (signal ground).
MOUT LOUT	O	MOUT and LOUT are output pins of the built-in OP amplifier for MIN and LIN, respectively.
AMON	O	This pin is connected to the LOUT pin in the recording mode and to the DA converter output in the playback mode. Used to connect the built-in LPF input (FIN pin).
FIN	I	Input pin of the built-in LPF.
FOUT	O	Output pin of the built-in LPF. Used to connect the AD converter input (ADIN pin).
ADIN	I	Input pin of the built-in 12-bit AD converter.
AOUT	O	Output pin of the built-in LPF. This pin outputs playback waveforms and used to connect an external speaker drive amplifier.
SADX SADY	O	(Serial Address Data). Used to connect the SAD pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs of starting address of read/write.
$\overline{SAS}$	O	(Serial Address Strobe). Used to connect the $\overline{SAS}$ pin of external MSM6791 (DRAM interface LSI) and the $\overline{SASX}$ and $\overline{SASY}$ pins of external serial voice ROM. Clock pin to write the serial address.
$\overline{TAS}$	O	(Transfer Address Strobe). Used to connect the $\overline{TAS}$ pin of each external MSM6791 (DRAM interface LSI) and serial voice ROM. This pin outputs address strobe outputs to set the serial address data from the SADX and SADY pins into the internal address counter of each external MSM6791 (DRAM interface LSI) and serial voice ROM.
$\overline{RWCK}$	O	(Read/Write Clock). Used to connect the $\overline{RWCK}$ pin of each external MSM6791 (DRAM interface LSI) and the $\overline{RDCK}$ pin of each external serial voice ROM. This pin outputs a clock to read data from or write it into each external MSM6791 (DRAM interface LSI).
$\overline{WE}$	O	(Write Enable) Used to connect the $\overline{WE}$ pin of each external MSM6791 (DRAM interface LSI). This pin outputs WE signal to select either read or write mode.
DI/O	I/O	(Data I/O). Used to connect the DIN and DOUT pins of external MSM6791 (DRAM interface LSI). This pin outputs the data to be written into the external MSM6791 (DRAM interface LSI) or inputs the data read from the external MSM6791 (DRAM interface LSI).
DROM	I	(Data ROM). Used to connect the DOUT pin of each external serial voic ROM.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin function</th></tr>
<tr><td>$\overline{CS1}$
$\overline{CS2}$
$\overline{CS3}$
$\overline{CS4}$</td><td>O</td><td>(Chip Select). Used to connect $\overline{CS}$ pin of MSM6791 (DRAM interface LSI) and the $\overline{CS}$ ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$) pins of each serial voice ROM.</td></tr>
<tr><td>RSEL1
RSEL2</td><td>I</td><td>(Register Select). These input pins are used to select the maximum controlled size of external RAM.
<table>
<tr><td>RSEL2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>RSEL1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>Total memory size</td><td>8Mbit</td><td>16Mbit</td><td>24Mbit</td><td>32Mbit</td></tr>
</table></td></tr>
<tr><td>MCUM</td><td>I</td><td>This pin is used to select either the stand-alone mode or the microcontroller interface mode.
Low level: Stand-alone mode
High level: Microcontroller interface mode</td></tr>
<tr><td>RESET</td><td>I</td><td>A high input level at this pin causes the MSM6788 to be initialized and to go into the power down state.</td></tr>
<tr><td>$\overline{PDWN}$</td><td>I</td><td>(Power Down). When a low level is input to this pin, the MSM6788 goes to the power down state. Unlike the RESET pin, this pin does not force to reset the MSM6788. When an Low level is applied to this $\overline{PDWN}$ pin during recording operation, the MSM6788 is halted, and will be maintained in the power down state while $\overline{PDWN}$ is low. After this pin is restored to a high level, postprocessing for recording will be performed.</td></tr>
<tr><td>D0
D1
D2
D3</td><td>I/O</td><td>Bi-directional data bus to transfer commands and data to and from an external microcontroller.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>Write pulse input pin. Inputting a low pulse to this $\overline{WR}$ pin causes a command or data to be input via D0~D3 pins.</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td>Read pulse input pin. Inputting a low pulse to this $\overline{RD}$ pin causes status bits or data to be output via D0~D3 pins.</td></tr>
<tr><td>$\overline{CE}$
CE</td><td>I</td><td>Chip enable input pins. When the $\overline{CE}$ pin is set to a low level and the CE pin is set to a high level, the write pulse ($\overline{WR}$), read pulse ($\overline{RD}$) can be accepted.
When the $\overline{CE}$ pin is set to a high level or CE pin is set to a low level, the write pulse ($\overline{WR}$) and read pulse ($\overline{RD}$) cannot be accepted so that data cannot be transferred to and from via D0~D3 pins.</td></tr>
<tr><td>BUSY</td><td>O</td><td>Outputs a high level while a command is being executed. When this pin is held high, do not apply any data to D0~D3 pins. The state of this BUSY pin is the same as the contents of the BUSY bit of the status register</td></tr>
<tr><td>RPM</td><td>O</td><td>Outputs a high level during recording or playback operation. The state of this RPM is the same as the contents of the RPM bit of the status register.</td></tr>
<tr><td>VPM</td><td>O</td><td>Outputs the state of standby for voice after the start of voice activated recording and outputs a high level when the record/display is stopped temporality by inputting the PAUSE command. The state of this VPM pin is the same as the contents of the VPM bit of the status register.</td></tr>
</table>

Pin Name	I/O	Pin function
NAR	O	This NAR bit indicates whether the phrase designation by the CHAN command is enabled or disabled. In the ROM play back operation, specify the next phrase after making sure that the NAR output is high, and input the START command.
ACON	I	Used to select the use or of the pop noise suppression circuit at the analog output (AOUT) pin. When low level, the pop noise suppression circuit is used. When high level, the pop noise suppression circuit is nor used.
EXTD	I	In the record/playback operation by the EXT command, input a high level for read/write of SBC data. Input a low level for usual command input and status output.
XT	I	Used to connect an oscillator. When an external clock is used, input the clock through this pin. At the power down state, this pin must be set to the ground level.
$\overline{XT}$	O	Used to connect an oscillator, when an external clock is used, this pin must be left open.
MON	O	Outputs a high level while the record/playback operation is being performed. Outputs a synchronizing clock while record/playback activated by the EXT command is being performed.
TEST $\overline{TEST}$	O	Used to test the MSM6788. Input a low level to the TEST pin and a high level to the $\overline{TEST}$ pin.
TMD0~TMD3 TDT0 ~TDT7 SYNC	I/O	Used to test the MSM6788. These pins must be left open.
TST TCK TMD4	I	Used to test the MSM6788. Input a low level.

■ FUNCTIONAL DESCRIPTION

● Bit Rate

The master clock frequency (fosc) and sampling frequency (fsam) are shown in the following equation. When the master clock frequency is 8.192 MHz, the sampling frequency is 8.0 kHz.

$$\text{Sampling frequency} = \frac{\text{Master clock frequency}}{1024} = \frac{8.192\ \text{MHz}}{1024}$$

$$= 8.0\ (\text{kHz})$$

In the SBC method, 96 sampled frequencies are grouped into one frame, and coded on the frame basis. Data quantity per frame can be selected out of the following three types of bit rate.

Bit rate	Data quantity per one frame
16.0 kbps	24 byte (192 bit)
12.6 kbps	19 byte (152 bit)
10.0 kbps	15 byte (120 bit)

@fosc=8.192MHz

For example, when the data quantity is 24 bytes, the bit rate is calculated as follows:

$$\text{Bit rate} = \frac{\text{Data quantity per one frame}}{\text{Time per one frame}} = \frac{\text{Data quantity per one frame}}{\text{Sampling cycle} \times 96}$$

$$= \frac{24\ \text{byte}}{1 / 8.0\ \text{kHz} \times 96} = \frac{192\ \text{bit}}{12.0\ \text{msec}}$$

$$= 16.0\ (\text{kbps})$$

● Recording Time and Memory Capacity

The recording time depends on the memory capacity of the external DRAM and bit rate, and is given by

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (Kbits)}}{\text{bit rate (kbps)}}\ \text{(seconds)}$$

For example, if the bit rate is 10 kbps, and successive 8Mbit DRAM is used, the recording time can be obtained as follows.

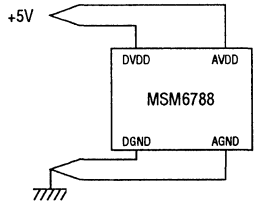
$$\text{Recording time} = \frac{1.024 \times (8192 - 64)}{10} = 832\ \text{seconds}$$

$$= 13\ \text{minutes}\ 52\ \text{seconds}$$

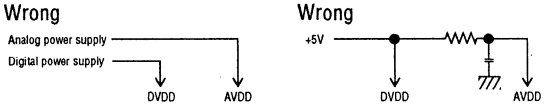
In the above equation, the memory capacity is obtained by subtracting the memory capacity (64Kbits) for the channel index area from the total memory capacity.

● Power Supply Wiring

As shown in the following diagram, supply the power to this MSM6788 from the same power source, but separate the power supply wiring to the analog portion from that to the logic position.



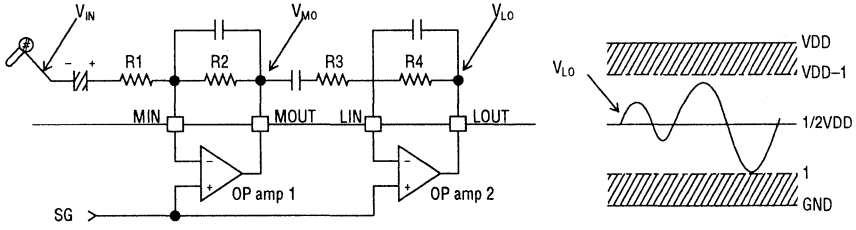
Do not supply the power to the logic portion and the analog portion from the separate power sources. Otherwise, a problem such as latch-up may occur.



● Analog Input Amplifier Circuit

This MSM6788 has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



$$V_{LO} = \frac{R4}{R3} \quad V_{MO} = \frac{R2 \cdot R4}{R1 \cdot R3} V_{IN} \ (V)$$

During the time the recording operation is performed, the output V_{LO} of OP amp 2 is connected to the input FIN of the built-in LPF. The FIN allowable input voltage (V_{FIN}) ranges from 1V to (V_{DD} – 1)V. Therefore, the amplification ratio must be adjusted so that the V_{LO} amplitude can be within the FIN allowable input voltage range.

For example, if V_{DD} = 5V, V_{LO} becomes 3 V_{p-p} max. If V_{LO} exceeds the FIN allowable input voltage range, the output of the LPF will be a clipped waveform.

The load resistance R_{OUTA} of the OP amp is 200 kΩ minimum, so that the feedback resisters R2 and R4 of the inverting amplifier circuit must be 200 kΩ or more.

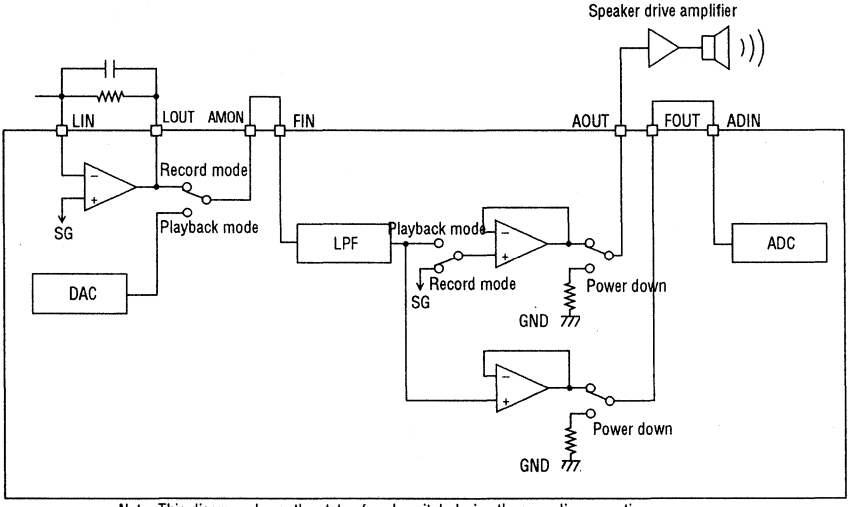
● Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM6788, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND (ground) level, and SG (signal ground) level, depending on the operation status as shown below.

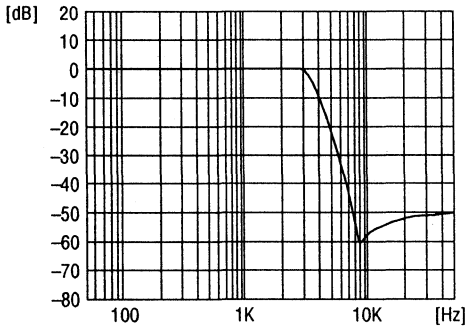
Analog pin	At power down (RESET pin = H)	During operation (RESET pin = L)	
		Recording mode	Playback mode
FOUT pin	GND level	LPF output (recording waveform)	LPF output
AOUT pin	GND level	SG level	LPF output (playback waveform)



Note: This diagram shows the state of each switch during the recording operation.

● LPF Characteristics

This MSM6788 contains a fourth-order switched-capacitor LPF.
The attenuation characteristic of this LPF is –40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsam). The cut-off frequency is preset to 0.4 times the sampling frequency. The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsam = 8 kHz.



LPF Frequency Characteristics (fsam = 8.0kHz)

● Reset Function

By applying a high level to the RESET pin, the MSM6788 stops frequency oscillation to minimize current consumption and goes to the power-down state. At the same time, the control circuit is reset and initialized.

When this reset operation is performed, the record/playback condition such as bit rate and the data stored in the DRAMs are set to the data stored just before the reset takes place. In this case, the playback level is set to 0 dB amplitude and the voice start condition is set to the voice start and normal recording. The PLFLG/RDFLG set by the FLGWR command is reset to 0.

If a high level is applied to the RESET pin during command execution or record/playback operation, the MSM6788 is set to the power-down state and initialized state. Internal data voice data becomes undefined.

The following shows the power-down state of the MSM6788.

(1) Frequency oscillation is stopped and all operations of the internal circuit are halted.

(2) The current consumption is minimized. When an external clock is used, apply a ground (GND) level to the XT pin at power down so that no current can flow into the oscillation circuit.

(3) D0~D3 pins constituting the data bus go to the high-impedance state, independ the state of the $\overline{RD}$, $\overline{CE}$, and CE pins.

(4) $\overline{CS1}$~$\overline{CS4}$ pins are set to a high level to minimize the current consumption of external DRAMs and serial voice ROMs.

(5) The state of the output pins and input/output pins are as follows.

SADX, $\overline{SAS}$, $\overline{TAS}$, $\overline{CS1}$ ~ $\overline{CS4}$, $\overline{WE}$, $\overline{RWCK}$, and NAR pins: .....High level
SADY, MON pin: .....Low level
D0~D3, DI/0, BUSY, RPM, and VPM pines: .....High impedance
AOUT and FOUT pins: .....Ground level

After powering up the MSM6788, be sure to initialize it by applying a high level to the RESET pin.

● Power Down by the $\overline{\text{PDWN}}$ pin

By applying a low level to the $\overline{\text{PDWN}}$ pin, the MSM6788 may be set to the power-down state, in which the frequency oscillation and all operations of internal circuits are halted. Unlike the reset operation by the RESET input, the control circuit will not be initialized by this power-down operation.

The power-down operation will not affect the data in the internal control circuit and external DRAMs. Therefore, this power-down operation is useful when the battery backup takes place in case of power failure.

When $\overline{\text{PDWN}}$ goes to a low level during command execution, this execution of command is halted at the time that power-down operation is performed. When $\overline{\text{PDWN}}$ becomes low during one of the following operations, their respective operations will be performed after the power-down state is released ($\overline{\text{PDWN}}$ = H).

(1) When the MSM6788 is powered down ($\overline{\text{PDWN}}$ = L) during the record/playback operation: The record/playback operation is stopped. After the release of the power-down state, the postprocessing will be performed. The end of the postprocessing can be verified by checking the BUSY bit and RPM bit of the status register.

(2) When the MSM6788 is powered down ($\overline{\text{PDWN}}$ = L) during the phrase deleting operation: The phrase deleting operation is temporarily stopped and will be restarted after the release of the power-down state. The end of the phrase deleting operation can be verified by checking the BUSY bit.

(3) When the MSM6788 is powered down ($\overline{\text{PDWN}}$ = L) during the time the transition of the AOUT output to a DC level by LEV command is in progress: This transition operation is temporarily stopped and will be continued after the release of the power-down state. The end of the transition to a DC level can be verified by checking the BUSY bit.

● Record/Playback Control Modes

Selection of record/playback or ROM playback is made by the command mode set in the BRATE command.

Record/ playback control mode	Record/playback	ROM playback
Command mode	Mode 0	Mode 1
Number of phrases	63	255

1. Record/playback

The recording area for each phase is indirectly specified by phrase designation (CA0~CA5, 63 phrases). The recording area for each phrase is controlled by the LSI.

The recording time is specified by the BLKWR command. During recording operation, this LSI searches the memory areas that are not used by other phrases and writes the voice data on them. Therefore, the phrase control by the microcontroller can be performed easily even in applications in which it is required to perform phrase deletion and re-recording frequently.

2. ROM playback

The playback area of each phrase of the fixed message is indirectly specified by phrase designation (CA0~CA7, 255 phrases).
The table containing the start address and stop address that indicate the playback area and bit rate, is written in the index area of the serial voice ROM.

● Data Configuration of External RAM

The external RAM constitutes a virtual memory with a address space of (X addresses in the word direction) × (depth of 1Kbits) through the DRAM interface (MSM6791).
This virtual memory is addressable only for X addresses in the word direction.
The external RAM is divided into the channel index area that stores the data for address control of each phrase and the voice (SBC) data area.

1. Address space allocation of external RAM

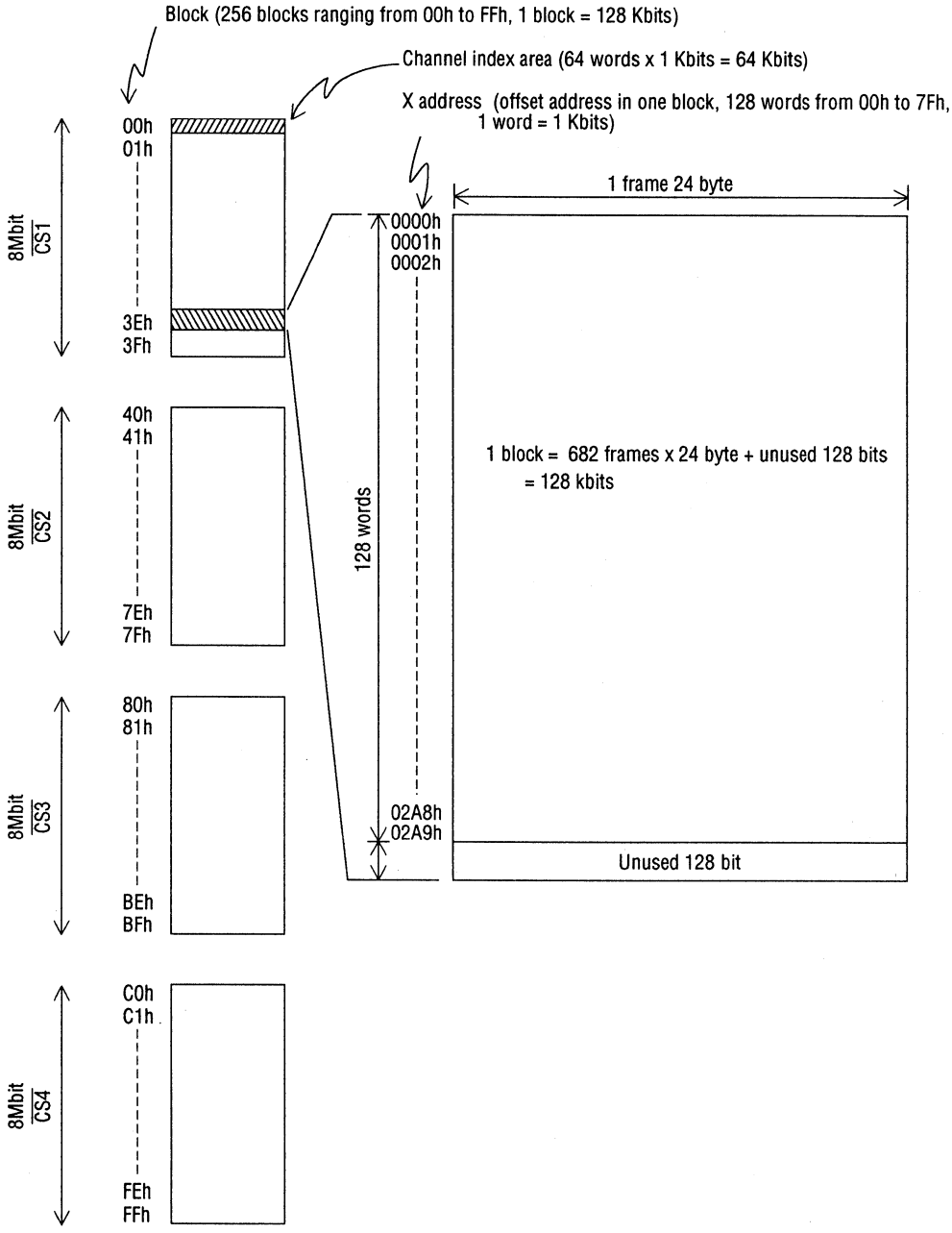
1.1 Address space for the record/playback mode

In the recording/playback mode, the total memory capacity of external RAM is equally divided into 256 blocks that are addressable by 00h~FFh.

Each block is composed of several frames depending on the bit rate. The memory capacity of one block and the number of frames vary depending on the total memory capacity of RAM externally connected.

RSEL2		L	L	H	H
RSEL1		L	H	L	H
Total memory capacity		8M bits	16M bits	24M bits	32M bits
Memory capacity of one block		32 kbits	64 kbits	128 kbits	128 kbits
Recording time of one block	16.0 kbps	2.0 seconds	4.1 seconds	8.2 seconds	8.2 seconds
	12.6 kbps	2.6 seconds	5.2 seconds	10.3 seconds	10.3 seconds
	10.0 kbps	3.3 seconds	6.6 seconds	13.1 seconds	13.1 seconds
Number of frames of one block [Frame address]	16.0 kbps	170 [0000h~00A9h]	341 [0000h~0154h]	682 [0000h~02A9h]	682 [0000h~02A9h]
	12.6 kbps	215 [0000h~00D6h]	431 [0000h~01AEh]	862 [0000h~035Dh]	862 [0000h~035Dh]
	10.0 kbps	273 [0000h~0110h]	546 [0000h~0221h]	1092 [0000h~0443h]	1092 [0000h~0443h]
Unused memory of one block	16.0 kbps	128 bit	64 bit	128 bit	128 bit
	12.6 kbps	88 bit	24 bit	48 bit	48 bit
	10.0 kbps	8 bit	16 bit	32 bit	32 bit

Address Space Allocation of RAM
(record/playback, 32Mbit 16.0 kbps)



2. Channel index area of RAM

The 64Kbit address data at the head of the RAM is used for the channel index area. The channel index area for one phrase (1Kbits) consists of 64Kbit address data, 704bit user data, 256bit address control block table.

(1) Number of blocks: This area stores the number of blocks (recorded time) used for recording of one phrase. Address ch00 stores the number of unused blocks (available blocks). This number of blocks can be read by the BLKRD command. The recorded time for one phrase and the unused capacity (available recording time) of memory can be obtained.

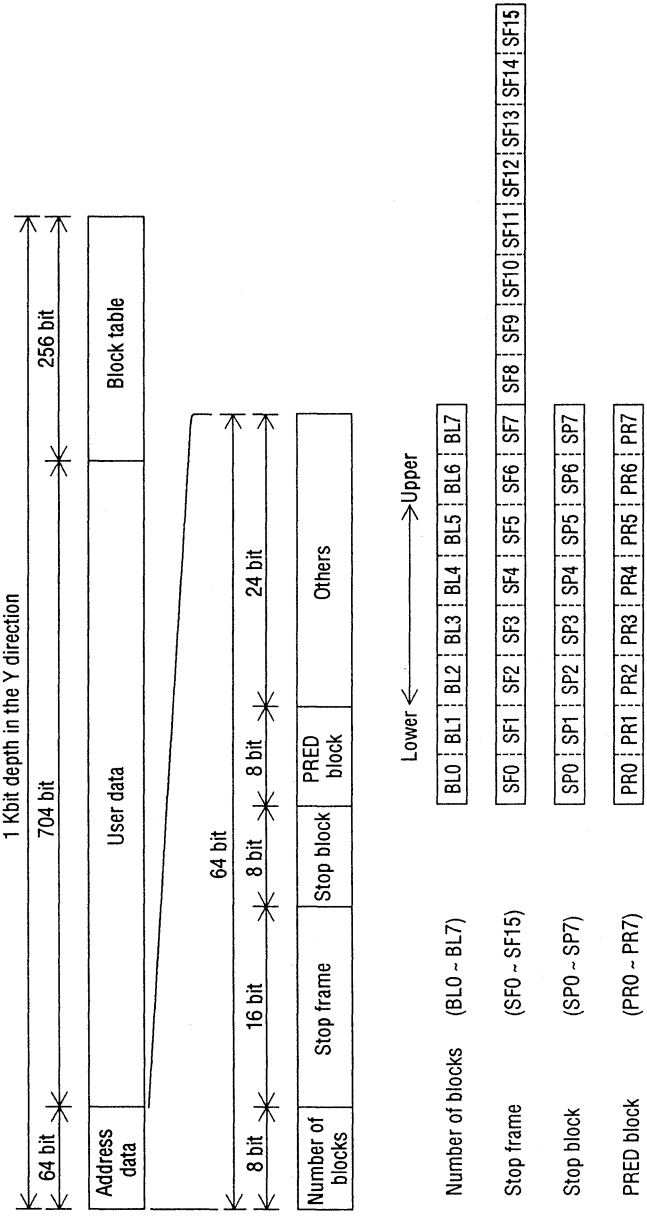
(2) Stop frame: This area stores the final phrase address of one block. Addressing varies depending on the memory capacity and bit rate. For example, addresses 0000h - 00A9h are assigned in case of successive 8Mbit DRAM and 16Kbps.

(3) Stop block: The final block is stored. Addresses 00h~FFh are assigned to this block.

(4) PRED block: This area stores the address of a block immediately before the stop block.

(5) User data: This user data area can be used by the user. The data can be written to and read from this area by the CHRW command.
This user data area is provided independently for each phrase, so that it is useful to store the phrase bit rate and recorded time.

(6) Block table: The block table is an area used for the block control.


1 Kbit depth in the Y direction
64 bit
704 bit
256 bit
Address data
User data
Block table
64 bit
8 bit
16 bit
8 bit
8 bit
24 bit
Number of blocks
Stop frame
Stop block
PRED block
Others
Lower
Upper
Number of blocks (BL0 ~ BL7)
BL0 BL1 BL2 BL3 BL4 BL5 BL6 BL7
Stop frame (SF0 ~ SF15)
SF0 SF1 SF2 SF3 SF4 SF5 SF6 SF7 SF8 SF9 SF10 SF11 SF12 SF13 SF14 SF15
Stop block (SP0 ~ SP7)
SP0 SP1 SP2 SP3 SP4 SP5 SP6 SP7
PRED block (PR0 ~ PR7)
PR0 PR1 PR2 PR3 PR4 PR5 PR6 PR7

● Command Description

The MSM6788 is controlled by 22 types of commands via D0-D3 pins constituting the data bus and $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, and CE control pins. The state of the MSM6788 can be know by obtaining the contents of the internal status register via the data bus or the output pins.

There are four command modes available: mode 0, mode 1, mode 2, and mode 3.. Some commands need to set the command mode before inputting them. The command mode can be selected by setting MOD0 bit and MOD1 bit of the BRATE command.

Command	Code D3	D2	D1	D0	Command function	
NOP	0	0	0	0	(NON OPERATION).	Has no function.
PAUSE	0	0	0	1	(PAUSE).	Suspends record/playback temporarily.
PLAY	0	0	1	0	(PLAYBACK).	Sets playback mode.
REC	0	0	1	1	(RECORD).	Sets recording mode.
START	0	1	0	0	(START).	Starts record/playback.
STOP	0	1	0	1	(STOP).	Stops record/playback. Stops execution of CHRW, DTRW, DTRD, and EXT commands.
BRATE	0	1	1	0	(BIT RATE).	Specify the command mode and bit rate in conjunction with 1 nibble following this command.
CHAN	0	1	1	1	(CHANNEL).	Specifies a phrade, in conjunction with 2 nibbles following this command.
BLKWR	1	0	0	0	(BLOCK WRITE).	Input the following block data into the internal block register, in conjunction with the nibble following this command: Before record: Specify the number of phrase recording blocks (recording time). Before a specified block playback: Specify the block at the head of playback start block as 00h. Before DEL2 command input: Specify the location to erase the phrase tail.
BLKRD1	1	0	0	1	(BLOCK READ1).	Reads the number of blocks (recording time) for the phrase stored in the channel index area, in conjunction with 2 nibbles following this command. During execution of this command, the contents of the status register cannot be read.
BLKRD2	1	0	0	1	(BLOCK READ2).	Reads the number of blocks accessed before during record/playback in conjunction with the lead access of 2 nibbles following this command, in order to know the record/playpack time progress. During record/playback standby, reads the number of blocks accessed in the last record/playback. During this period, the contents of status register cannot be read.
ADRWR	1	0	0	0	(ADDRESS WRITE).	Stores the start address and the stop address to the channel index area, in conjunction with 10 nibbles following this command.
ADRRD	1	0	0	1	(ADDRESS READ).	Reads out the start address and the stop address stored in the channel index area, in conjunction with 10 nibbles following this command. During execution of this command, the contents of the status register cannot be read.

Command	Code D3	D2	D1	D0	Command function
CHRW	1	0	1	0	(CHANNEL READ WRITE). Reads out the user data stored in the channel index area or writes the user data to the channel index area by the read/write access operation following this command.
DTRW	1	0	1	0	(DATA READ WRITE). Transfers data to or from the external RAM through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
DTRD	1	0	1	0	(DATA READ). Reads the data in the external serial voice ROMs through the data bus, by the address designation in 5 nibbles following this command and the read/write access operation.
EXT	1	0	1	1	(EXTERNAL). Performs record/playback by inputting/outputting SBC data through the data bus, in conjunction with the read/write access operation. This command will be used when an SRAM or a hard disk is used for storing voice data. Does not control external RAM and addresses.
FLGWR	1	1	0	0	(FLAG WRITE). Sets and resets the RDFLG and PLFLG. By RESET input, this commnad is reset to 0. RDFLG: 0: BLKRD 1 commnad 1: BLKRD 2 command PLFLG: 0: Usually playback. Playback from the first record. 1: Specified block playback
VDS	1	1	0	0	(VOICE DETECT SELECT). Select voice activated start function, in conjunction with 1 nibble following this command.
DEL1	1	1	0	1	(DELETE1). Deletes the phrase specified by the CHAN command. When ch00 is specified by the CHAN command, all phrases are deleted by this command.
DEL2	1	1	0	1	(DELETE2). Deletes the tail of the command specified by the CHAN command. Deletes the contents recorded after specified by the BLKWR command.
LEV	1	1	1	0	(LEVEL). Specifies the playback output level and the transition of analog output (AOUT pin) to the DC level, in conjunction of 1 nibble following this command. This level is initialized by the RESET input.
NOP	1	1	1	1	(NON OPERATION). Has no function.

1. Command List

MOD1		0	0	1	1	Note
MOD0		0	1	0	1	
Code		Mode 0	Mode 1	Mode 2	Mode 3	
D3 D2 D1 D0	HEX					
0 0 0 0	0h	NOP	NOP	NOP	NOP	
0 0 0 1	1h	PAUSE	PAUSE	Disabled	Disabled	
0 0 1 0	2h	PLAY	PLAY	PLAY	PLAY	
0 0 1 1	3h	REC	REC	REC	REC	
0 1 0 0	4h	START (Record/playback)	START (ROM playback)	Disabled	Disabled	
0 1 0 1	5h	STOP	STOP	STOP	STOP	
0 1 1 0	6h	BRATE	BRATE	BRATE	BRATE	
0 1 1 1	7h	CHAN	CHAN	CHAN	CHAN	
1 0 0 0	8h	BLKWR	BLKWR	ADRWR	ADRWR	
1 0 0 1	9h	BLKRD1	BLKRD1	ADRRD	ADRRD	RDFLG=0
		BLKRD2	BLKRD2	ADRRD	ADRRD	RDFLG=1
1 0 1 0	Ah	CHRW	CHRW	DTRW	DTRD	
1 0 1 1	Bh	EXT	EXT	EXT	EXT	
1 1 0 0	Ch	FLGWR	FLGWR	VDS	VDS	
1 1 0 1	Dh	DEL1	DEL1	DEL2	DEL2	
1 1 1 0	Eh	LEV	LEV	LEV	LEV	
1 1 1 1	Fh	NOP	NOP	NOP	NOP	

2. Command data format

Command	Code HEX		D3	D2	D1	D0	Note
NOP	0h		0	0	0	0	1-nibble command
PAUSE	1h		0	0	0	1	1-nibble command
PLAY	2h		0	0	1	0	1-nibble command
REC	3h		0	0	1	1	1-nibble command
START	4h		0	1	0	0	1-nibble command
STOP	5h		0	1	0	1	1-nibble command
SAMP	6h	1st nibble	0	1	1	0	2-nibble command
		2nd nibble	MOD1	MOD0	BR1	BR0	Command mode, bit rate

MOD1	MOD0	Command mode
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

BR1	BR0	Bit rate
0	0	16.0 kbps
0	1	12.6 kbps
1	0	10.0 kbps
1	1	Disabled

Values in parentheses are for fosc = 8.192 MHz.

CHAN	7h	1st nibble	0	1	1	1	3-nibble command
		2nd nibble	CA3	CA2	CA1	CA0	Phrase No.
		3rd nibble	CA7	CA6	CA5	CA4	

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.
0	0	0	0	0	0	0	0	ch00
0	0	0	0	0	0	0	1	ch01
0	0	0	0	0	0	1	0	ch02
0	0	0	0	0	0	1	1	ch03
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	chFE
1	1	1	1	1	1	1	1	chFF

Command	Code HEX		D3	D2	D1	D0	Note
BLKWR	8h	1st nibble	1	0	0	0	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Block data
		3rd nibble	BL7	BL6	BL5	BL4	
BLKRD	9h	1st nibble	1	0	0	1	3-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Block data
		3rd nibble	BL7	BL6	BL5	BL4	
ADRWR	8h	1st nibble	1	0	0	0	11-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
		4th nibble	SF3	SF2	SF1	SF0	Stop frame
		5th nibble	SF7	SF6	SF5	SF4	
		6th nibble	SF11	SF10	SF9	SF8	
		7th nibble	SF15	SF14	SF13	SF12	
		8th nibble	SP3	SP2	SP1	SP0	Stop block
		9th nibble	SP7	SP6	SP5	SP4	
		10th nibble	PR3	PR2	PR1	PR0	PRED block
		11th nibble	PR7	PR6	PR5	PR4	
ADRRD	9h	1st nibble	1	0	0	1	11-nibble command
		2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
		3rd nibble	BL7	BL6	BL5	BL4	
		4th nibble	SF3	SF2	SF1	SF0	Stop frame
		5th nibble	SF7	SF6	SF5	SF4	
		6th nibble	SF11	SF10	SF9	SF8	
		7th nibble	SF15	SF14	SF13	SF12	
		8th nibble	SP3	SP2	SP1	SP0	Stop block
		9th nibble	SP7	SP6	SP5	SP4	
		10th nibble	PR3	PR2	PR1	PR0	
		11th nibble	PR7	PR6	PR5	PR4	

Command	Code HEX		D3	D2	D1	D0	Note
CHRW	Ah		1	0	1	0	1-nibble command + read/write access + STOP command
DTRW	Ah	1st nibble	1	0	1	0	6-nibble command + read/write access + STOP command
		2nd nibble	0	0	0	0	Dummy nibble
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	X15	X14	X13	X12	
DTRD	Ah	1st nibble	1	0	1	0	6-nibble command + read access + STOP command
		2nd nibble	Y3	Y2	Y1	Y0	Y address
		3rd nibble	X3	X2	X1	X0	X address
		4th nibble	X7	X6	X5	X4	
		5th nibble	X11	X10	X9	X8	
		6th nibble	0	0	0	0	Dummy nibble
EXT	Bh		1	0	1	1	1-nibble command + read/write access + STOP command
FLGWR	Ch	1st nibble	1	1	0	0	2-nibble command
		2nd nibble	0	0	PLFLG	RDFLG	Flag data

PLFLG	Playback mode
0	Usual playback
1	Playback with block specified

RDFLG	Command selection
0	BLKRD1
1	BLKRD2

Command	Code HEX		D3	D2	D1	D0	Note
VDS	Ch	1st nibble	1	1	0	0	2-nibble command
		2nd nibble	VD3	VD2	VD1	VD0	Voice activation condition

VD3	VD2	VD1	VD0	Voice activation condition
0	0	0	0	Voice activation disabled
0	0	0	1	Voice detection level 1
0	0	1	0	Voice detection level 2
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Voice detection level 15

DEL1	Dh		1	1	0	1	1-nibble command
			ch00: Deletion of all phrases ch01 ~ ch3F: Deletion of a specified phrase				
DEL2	Dh		1	1	0	1	1-nibble command
LEV	Eh	1st nibble	1	1	1	0	2-nibble command
		2nd nibble	LV1	LV0	PN1	PN0	Playback level, transition to DC level

LV1	LV0	Playback level
0	0	0dB
0	1	0dB
1	0	–6dB
1	1	–12dB

PN1	PN0	Transition to DC level
0	0	Disabled
0	1	Disabled
1	0	Transition from GND to 1/2 VDD.
1	1	Transition from 1/2 VDD to GND.

NOP	Fh		1	1	1	1	1-nibble command

3. Relationship between record/playback control modes and commands

Command \ Record/playback mode	Record/display	ROM playback	EX command record/playback
NOP	—	—	—
PAUSE	○	○	—
PLAY	◎	—	◎
REC	◎	—	◎
START	◎	◎	—
STOP	○	○	◎
BRATE	◎	◎	◎
Command mode	◎	◎	—
Bit rate	◎	—	◎
CHAN	◎	◎	—
BLKWR	◎	—	—
BLKRD1	○	—	—
BLKRD2	○	—	—
ADRWR	○	—	—
ADRRD	○	—	—
CHRW	Data transfer command		
DTRW	Data transfer command		
DTRD	Data transfer command		
EXT	—	—	◎
FLGWR	○	—	—
VDS	○	—	—
DEL1	◎	—	—
Deletion of all phrases	◎	—	—
Deletion of a specified phase	○	—	—
DEL2	○	—	—
LEV	○	○	○

Note: ◎ : Required command ○ : Useful command — : Unnecessary command

● Status Register

The status register used in the MSM6788 is a 4-bit status register. When a low level is applied to the $\overline{RD}$ pin, the contents of the status register are output to D0~D3 pins to indicate the internal state of the MSM6788. The contents of the status register are also output to the BUSY, RPM, VPM, and NAR pins.

D3	D2	D1	D0
NAR	VPM	RPM	BUSY

(1) BUSY bit

The BUSY bit set to a high level indicates that the MSM6788 is executing RESET operation or command processing operation. When BUSY bit is high, do not input any command from the microcontroller. While any of data read commands is being executed, the state of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse. In this case, input a read command either after waiting a time longer than the duration of BUSY state or after verifying the end of the busy state by the BUSY pin.

While the RESET operation is being executed, the BUSY bit is set to a high level, and it returns to a low level after the end of the RESET operation. After a high level pulse is applied to the RESET pin to perform the RESET operation, the BUSY bit is set to a high level during execution of the RESET operation. It goes to a low level after the end of the RESET operation.

(2) RPM bit

The RPM bit goes to a high level during record/playback operation. While the RPM bit is high, do not input any command except those indicated below. Otherwise, the state of the MSM6788 becomes undefined.

NOP, PAUSE, STOP, BLKRD2 commands, START command for release of temporary stop and playback of next phrase, CHAN command for specifying the next phrase during playback, and LEV command for designation of playback output level

After a high level pulses is applied to the RESET pin to perform the RESET operation, the RPM bit goes to a low level that is the initial state.

(3) VPM bit

The VPM bit goes to a high level during standby for voice after start of the voice activated recording and during the time that record/playback is temporarily stopped by the PAUSE command.

When the VPM bit is high, do not apply any command except the START command for release of temporary stop. Otherwise, the state of the MSM6788 becomes undefined.

After a high level pulse is applied to the RESET pin to perform the reset operation, the VPM bit goes to a low level that is the initial state.

(4) NAR bit

The NAR bit indicate the enabled or disabled state for phrase designation. When this bit is high, the phrase designation by the CHAN command is enabled.

If it is desired to play back different phrases continuously during ROM playback, specify the next phrase and input the START command after verifying that the NAR bit becomes high.

After a high level pulse is applied to the RESET pin to perform the reset operation, the NAR bit goes to a high level that is the initial state.

BUSY causing conditions	Symbol	BUSY state duration	BUSY bit verification	Note
Release of reset operation	t_{REX}	(Note 2) 1 ms	Possible	Input of RESET pulse
Input of 1-nibble command	t_{B1}	16 µs	Possible	NOP, PAUSE, PLAY, REC, START, STOP
Input of 2-nibble command	t_{B2}	16 µs	Possible	BRATE, FLGWR, VDS, LEV
Input of 3-nibble command	t_{B3}	16 µs	Possible	CHAN, BLKWR
Input of 2-nibble or 3-nibble command data	t_{BD}	16 µs	Possible	BRATE, FLGWR, VDS, LEV, CHAN, BLKWR
BLKRD command				
Input of command	t_{WBR}	270 µs	Impossible	
Output of block data	t_{WDR}	50 µs	Impossible	
ADRWR command				
Input of command	t_{BAW}	270 µs	Possible	
Input of address data	t_{BAD}	50 µs	Possible	
ADRRD command				
Input of command	t_{WAR}	270 µs	Impossible	
Output of address data	t_{WDR}	50 µs	Impossible	
CHRW command				
Input of command	t_{WCRW}	770 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
DTRW and DTRD commands				
Input of command	t_{WRW}	16 µs	Possible	
Input of address (2nd ~ 5th nibbles)	t_{WA1}	16 µs	Possible	
Input of address (6th nibble)	t_{WA2}	270 µs	Possible	
Input of REC command	t_{WRC}	16 µs	Possible (Note 1)	
Input of write data	t_{WWD}	50 µs	Possible (Note 1)	
Input of PLAY command	t_{WPL}	50 µs	Impossible	
Input of STOP command	t_{WSP}	50 µs	Possible (Note 1)	
Input of DEL1 command (all phrases)	t_{WBLA}	550 ms	Possible	
Input of DEL1 command (a specified phrase)	t_{WBL1}	70 ms	Possible	
Input of DEL2 command (tail erased)	t_{WBL1}	70 ms	Possible	

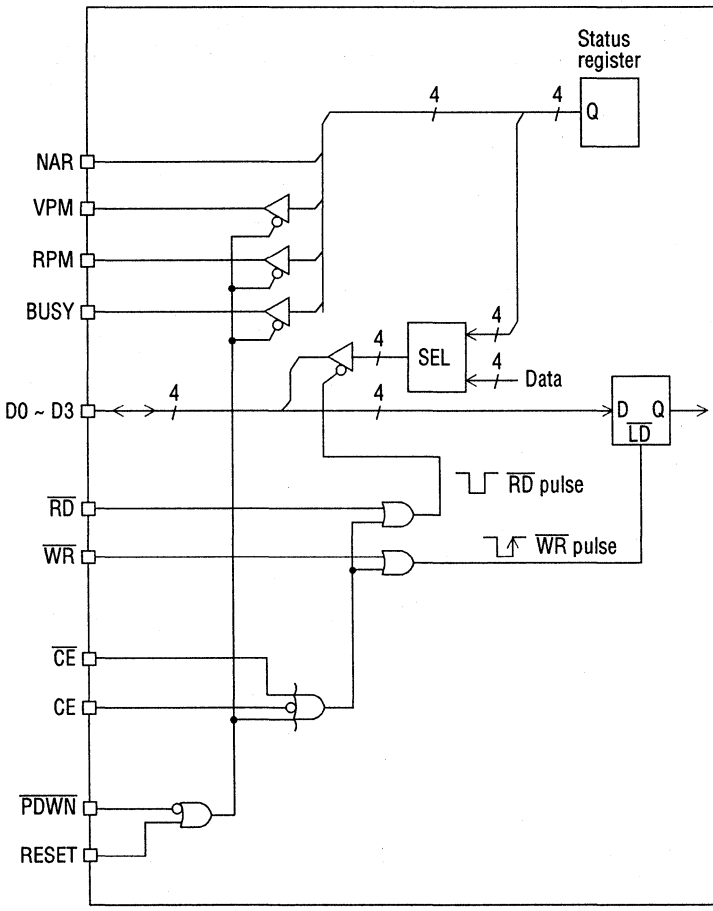
Note 1: The BUSY state can be verified by the BUSY bit when only the data write access operation is executed after the CHRW or DTRW command is input.

Note 2: The BUSY state duration after release of RESET operation includes the oscillation start-up stabilization time. This oscillation start-up stabilization time is several tens of milliseconds for crystal oscillators and is several hundreds of microseconds for ceramic oscillators.

● Inputting the Command

To input a command or data, apply the command or data to D0~D3 pins and then apply a low level pulse ($\overline{WR}$ pulse) to the $\overline{WR}$ pin.
By inputting a low level pulse ($\overline{RD}$ pulse) to the $\overline{RD}$ pin, the contents of the status register or data will be output via D0~D3 pins.
The $\overline{CE}$ pin is used to enable or disable the $\overline{WR}$ pulse and $\overline{RD}$ pulse. When a low-level is applied to this $\overline{CE}$ pin, the enable state is present, so that $\overline{WR}$ and $\overline{RD}$ pulses can be accepted. When a high level is applied to this $\overline{CE}$ pin, the disable state is present, so that $\overline{WR}$ and RD pulses cannot be accepted and, at the same time, D0~D3 pins are placed in the high-impedance state.
The CE pin also has the same function as the $\overline{CE}$ pin. However, when high, this CE pin gives the enable state for the $\overline{WR}$ and $\overline{RD}$ pulses, and when low, it gives the disable state. When D0~D3 pins are used exclusively for the MSM6788, $\overline{CE}$ and CE pins can be fixed to a low level and a high level, respectively.

An equivalent circuit of the microcontroller interface section of the MSM6788 is shown below.

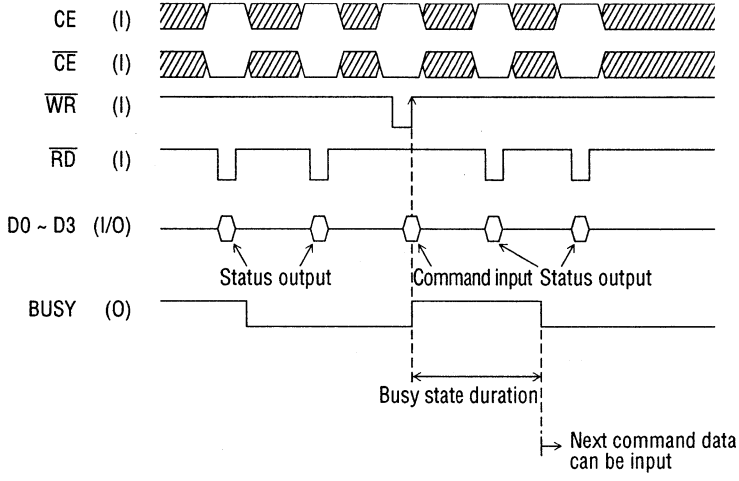


The steps for inputting the commands are described below.

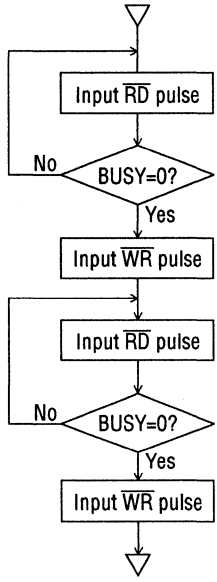
(1) Output the contents of the status register by applying the $\overline{RD}$ pulse (namely, by applying a low level pulse to the $\overline{RD}$ pin). Verify that the BUSY bit is 0. If the BUSY bit is 1, input the $\overline{RD}$ pulse repeatedly until the BUSY bit goes to 0. The BUSY state can also be verified through the BUSY pin.

(2) Set a command to D0~D3 pin and input the $\overline{WR}$ pulse.

(3) In case of a 2-nibble or 3-nibble command, verify that the BUSY bit of the status register is 0 in the same way as in (1). Then, set the command data to D0~D3 pins and input the $\overline{WR}$ pulse. In this case, the $\overline{WR}$ pulse can also be input after the waiting time that is longer than the BUSY state duration, instead of verifying the BUSY bit of the status register.



1. Inputting a 2-nibble command



● Changes of Record/Playback Conditions

Record/playback condition	POWER ON	RESET input	$\overline{\text{PDWN}}$ input	Command input
Record/playback mode	Undefined	Unchanged (Note 1)	Unchanged	REC command → Record mode PLAY command → Playback mode
Command mode	Undefined	Unchanged (Note 1)	Unchanged	Set by BRATE command
Bit rate	Undefined	Unchanged (Note 1)	Unchanged	Set by BRATE command
Phrase No.	Undefined	Unchanged (Note 1)	Unchanged	Set by CHAN command
Block data	Undefined	Unchanged (Note 1)	Unchanged	Set by BLKWR command
PLFLG, RDFLG	Undefined	Reset to 0	Unchanged	Set by FLGWR command
Voice activation	Undefined	Voice activation disabled	Unchanged	Set by VDS command
Playback level	Undefined	0dB	Unchanged	Set by LEV command
Data in RAM	Undefined	Unchanged (Note 1)	Unchanged	—

Note 1: RESET is performed without synchronization with the clock. When the RESET pulse is input during standby for command, record/playback condition will not be changed. When the RESET pulse is input during execution of a command, all record/playback conditions may be changed and the data may become undefined.

● Setting and Confirming the Record/Playback Conditions

1. Specifying the control mode for record/playback (by BRATE command)

Specify the control mode for record/playback by setting the BRATE command data and the command mode (using MOD1 and MOD0 bits).

MOD1	MOD0	Command mode	Control mode for record/playback
0	0	Mode 0	Record/playback
0	1	Mode 1	ROM playback by input of address code

2. Specifying the bit rate (by the BRATE command)

Specify the bit rate by setting BR0 and BR1 bit data of the BRATE command. The bit rate varies depending on the master clock frequency (f_{osc}).

BR1	BR0	Bit rate
0	0	16.0 kbps
0	1	12.6 kbps
1	0	10.0 kbps
1	1	Disabled

f_{osc}=8.192MHz

3. Specifying the voice activated recording(by the VDS command)

This MSM6788 has the voice activated recording function to start recording when the level of voice input exceeds a preset amplitude. Using the voice activated function, the unvoiced part prior to voice detection will not be recorded, so that the memory capacity can be utilized efficiently.

The unvoiced parts in the middle of recording are not eliminated. In the voice activated recording mode, recording is started when a voice input exceeds the preset thresholds. Therefore, a consonant part with a low level may not be recorded.

4. Specifying a phrase (by the CHAN command)

Specify a phrase by CA0~CA7 bit data of the CHAN command according to the following table.

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Phrase No.	Record/playback	ROM playback
0	0	0	0	0	0	0	0	ch00	(Note 1)	Disabled
0	0	0	0	0	0	0	1	ch01	Enabled (63 phrases)	Enabled (255 phrases)
0	0	0	0	0	0	1	0	ch02		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
0	0	1	1	1	1	1	0	ch3E		
0	0	1	1	1	1	1	1	ch3F		
0	1	0	0	0	0	0	0	ch40	Disabled	
0	1	0	0	0	0	0	1	ch41		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
1	1	1	1	1	1	1	0	chFE		
1	1	1	1	1	1	1	1	chFF		

Note 1: In the record/playback mode, ch00 cannot be used for recording/playback. This is a special phrase only used for deletion of all phrases and control of unused blocks.

5. Specifying the number of phrase recording blocks (by the BLKWR command)

The block data is set for the following operations:

Before recording: Specify the number of phrase recording blocks (recording time).
Before specified block playback: Specify the block at the head of playback start block as 00h.
Before DEL 2 command input: Specify the location to delete the tail of phrase.

In the record/playback mode, the total memory capacity of RAM connected externally is divided equally into 256 blocks. Therefore, the memory capacity of one block varies depending on the number of RAM connected externally.

For example, when 8Mbit RAM is connected and recording is performed by 16kbps, the memory capacity of one block and the recording time of one block are obtained as follows.

$$\text{Memory capacity of one block} = \frac{8\text{Mbits}}{256} = 32\text{Kbits}$$

$$\text{Recording time/block} = \frac{\text{Memory capacity of one block}}{\text{bit rate}}$$

$$= \frac{32 \times 1024 \text{ bits}}{1600} = 2 \text{ second}$$

If it is desired to make recording for 40 seconds on a phrase in this example, 20 (14h) phrase recording blocks are required.

The number of phrase recording blocks can be specified by the BLKWR command and is stored in the corresponding register in the MSM6788. The BLKWR command is enabled for command mode 0 or 1. Therefore, before inputting this BLKWR command, it is required to set the corresponding command mode using the BRATE command.

BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	Number of phase recording blocks (HEX)
0	0	0	0	0	0	0	0	0 (00h)
0	0	0	0	0	0	0	1	1 (01h)
0	0	0	0	0	0	1	0	2 (02h)
0	0	0	0	0	0	1	1	3 (03h)
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	254 (FEh)
1	1	1	1	1	1	1	1	255 (FFh)

6. Reading the number of phrase recording blocks (by the BLKRD1 command)

The number of blocks for each phrase stored in the channel index area can be read by the read access operation using the BLKRD1 command and two nibbles following this BLKRD1 command. In the record/playback mode, the number of blocks (namely, the recording time) of the specified phrase can be obtained. In the BLKRD command, the number of blocks is specified by a binary number consisting of BL0~BL7 in the same way as in the BLKWR command.

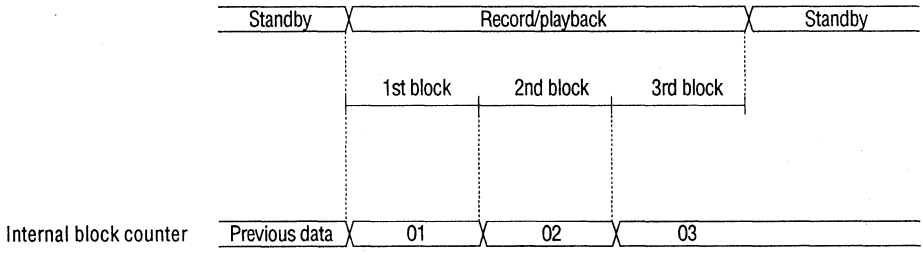
Before inputting the BLKRD1 command, the command mode must be set to either mode 0 or mode 1 by using the BRATE command. And RDFLG is cleared to zero by using the FLGWR command.

(1) When ch00 phrase is specified: The number of unused blocks (or available blocks) is stored in address ch00 of the channel index area. Therefore, the unused and available memory capacity (or available recording time) can be obtained.

(2) When one of ch01~ch3F is specified as a phrase: The number of blocks (or recording time) used by the specified phrase can be obtained.

7. Reading the number of blocks during record/playback (by the BLKRD2 command)

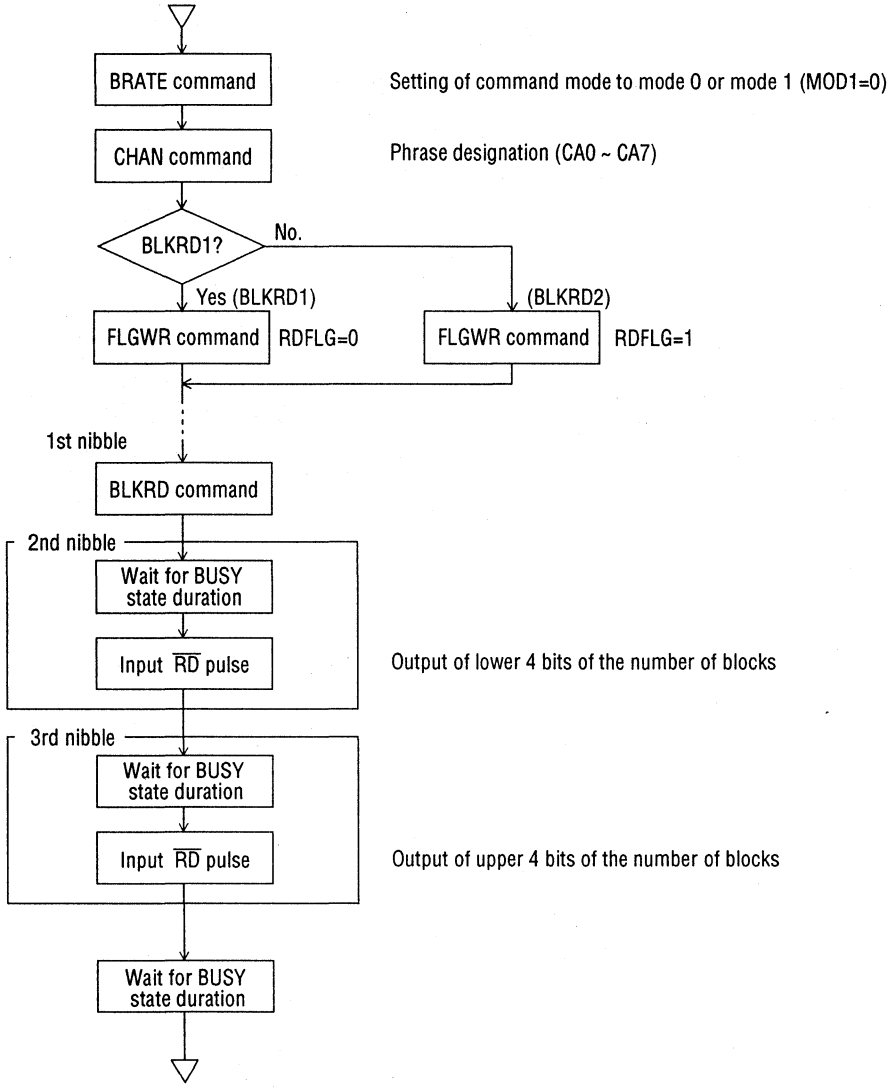
The number of blocks given access before during the record/playback operation can be read by the read access operation using the BLKRD2 command and two nibbles following this BLKRD2 command, and the record/playback duration can be obtained. While waiting for the record/playback operation, the number of blocks given access when the last record/playback operation is carried out. The number of blocks can also be counted from 01 when the recorded phrase is played back halfway by the specified block playback command. Data set by the BLKRD2 command is invalid during the ROM playback operation.



When the internal block counter starts to record/playback, as shown in the above figure, it counts up from 01, so that the number of blocks can be read by the BLKRD2 command at any time. The number of blocks is shown binary (BL0~BL7) as same as in the case of BLKWR, BLKRD1.

When the BLKRD2 command is input, set in advance the command mode to mode 0 or mode 1 using the BRATE command, and the RDFLG to 1.

BLKRD1, BLKRD2 command flow chart



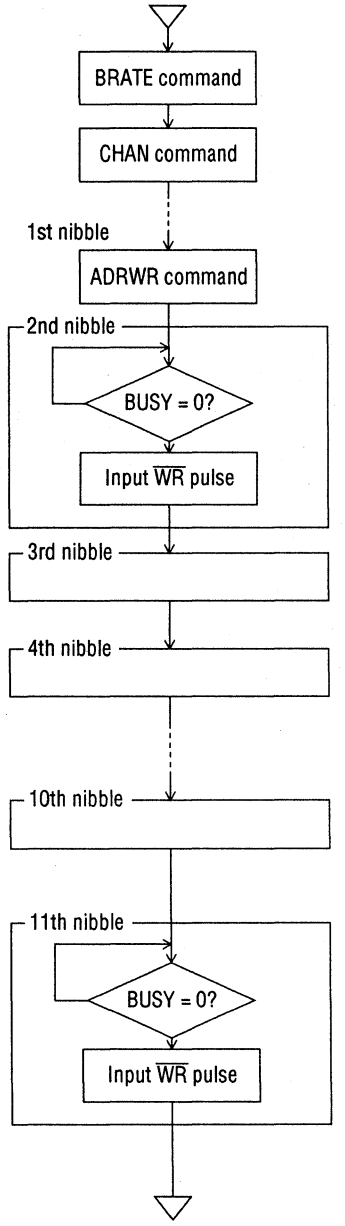
During execution of the BLKRD1, BLKRD2 command, verification of the status register cannot be performed by input of the $\overline{RD}$ pulse. When inputting the $\overline{RD}$ pulse for the 2nd nibble or 3rd nibble or inputting the next command after the BLKRD command, input the $\overline{RD}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

8. Inputting/outputting the address data (by the ADRWR/ADRRD command)

The ADRWR command is used to write the address data at the header 40 bits for each phrase of the channel index area, and the ADRRD to read the address data. These commands can also be used to change the address data for deleting the tail part of the recorded phrase. When the ADRWR and ADRRD commands are input, specify in advance the command mode to mode 2 or mode 3 by the BRATE command.

	D3	D2	D1	D0	Contents
1st nibble	1	0	0	*	Command
2nd nibble	BL3	BL2	BL1	BL0	Number of blocks
3rd nibble	BL7	BL6	BL5	BL4	
4th nibble	SF3	SF2	SF1	SF0	Stop frame
5th nibble	SF7	SF6	SF5	SF4	
6th nibble	SF11	SF10	SF9	SF8	
7th nibble	SF15	SF14	SF13	SF12	
8th nibble	SP3	SP2	SP1	SP0	Stop block
9th nibble	SP7	SP6	SP5	SP4	
10th nibble	PR3	PR2	PR1	PR0	PRED block
11th nibble	PR7	PR6	PR5	PR4	

ADRWR command flow chart



Setting of command mode to mode 2 or mode 3 (MOD1=1)

Phrase designation(CA0 ~ CA7)

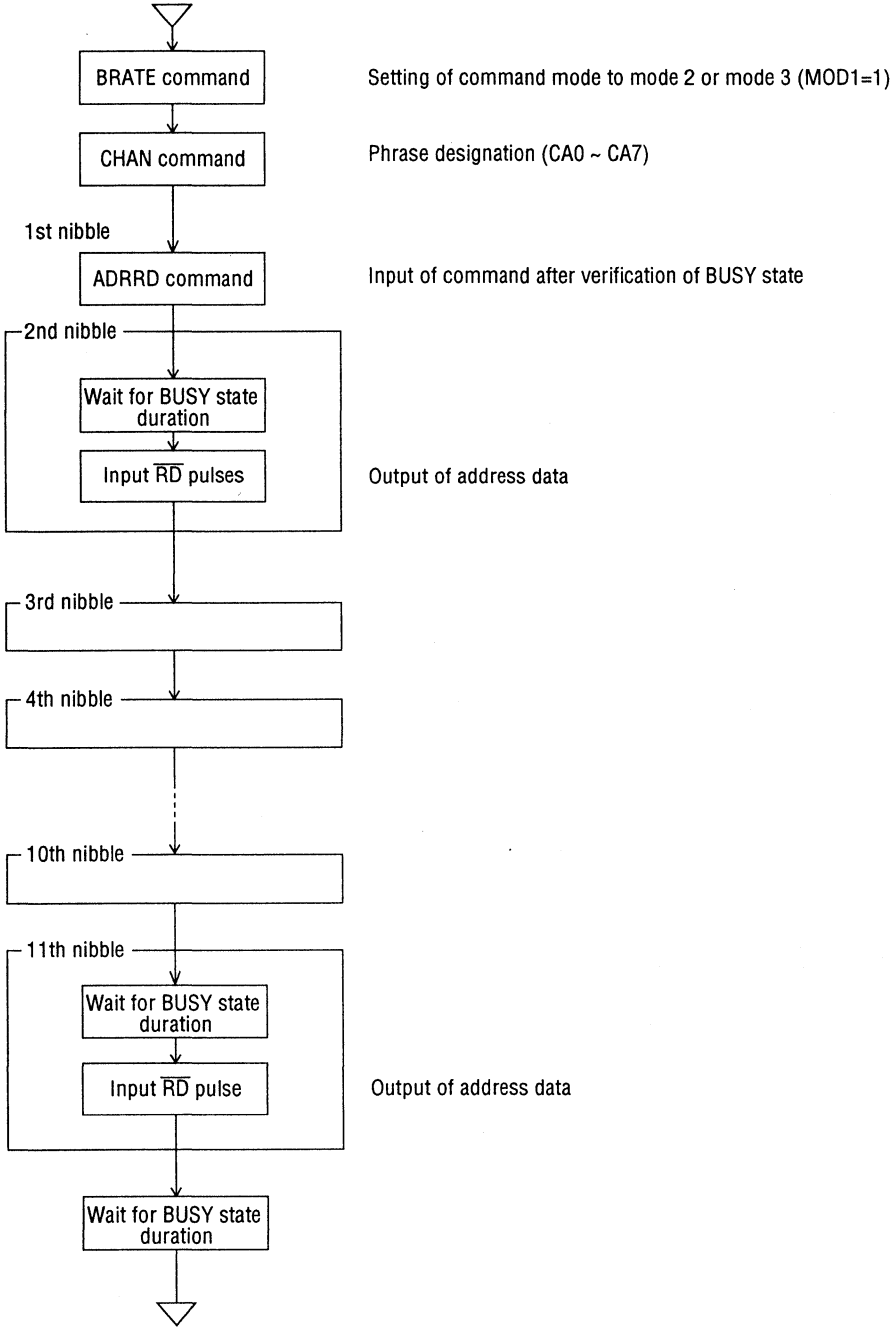
Input of command after verification of BUSY state

BUSY bit verification
(or waiting for BUSY state duration or longer)

Input of address data

Verification of address data

ADDRD command flow chart



During execution of the ADRRD command, verification of the status register cannot be performed by input of the $\overline{RD}$ pulse. When inputting the $\overline{RD}$ pulse for the 2nd nibble to 11th nibbles or inputting the next command after the ADRRD command, input the $\overline{RD}$ pulse either after the waiting time longer than the BUSY state duration or after verifying that the BUSY status is not present via the BUSY pin.

9. Specifying the playback level (by the LEV command)

For playback, one of three output levels 0 dB, –6 dB and –12 dB can be selected. The playback level can be specified by LV0 and LV1 bit data of the LEV command. If the LEV command is input during playback operation, the playback level will be changed at the moment when the command is input. When the RESET pulse is input, the playback output level is set 0 dB that is the initial state.

LV1	LV0	Playback level
0	0	0dB (equal to the voice data amplitude)
0	1	0dB (equal to the voice data amplitude)
1	0	–6dB (one-half of the voice data amplitude)
1	1	–12dB (one-fourth of the voice data amplitude)

● Record/Playback Method

1. Deleting phrases

1.1 Deleting all phrases (DEL1 command)

To delete all phrases, specify ch00 by the CHAN command and input the DEL1 command. When all phases are deleted in this manner, "0" data is written into ch01~ch3F addresses of the channel index area of the external RAM to place these addresses in the unrecorded state. The initial data for address control is written in ch00 address. Therefore, whenever the power is turned on, always perform the deletion of all phrases after inputting the RESET pulse.

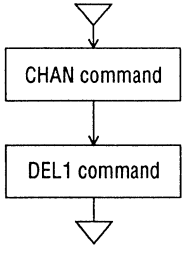
The deletion of all phrases causes the user area ch00~ch3F to be cleared to all 0s. Note that when the data was transferred to the channel index area by the CHRW command, this data is deleted by the deletion of all phrases.

Phases No.	State of the channel index area		
	Adress data	User data	Block table
ch00:	Initial data	Cleared to all 0s	Initial data
ch01~ch3F	Cleared to all 0s		

1.2 Deleting a specified phrase (DEL1 command)

To delete a phrase, specify one of ch01~ch3F by the CHAN command and input the DEL1 command. The deleted phrase is placed in the unrecorded state. The channel index area for the deleted phrase, including the user data, is cleared to all 0s. The data stored in ch00 address for control of unused blocks is updated.

Phrase deletion flow chart



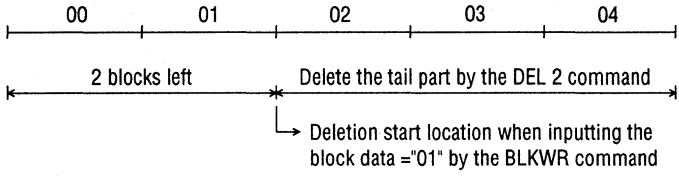
ch00 : Deletion of all phrases
ch01 ~ ch3F : Deletion of a specified phrase

1.3 Deletion of tail part (by the DEL2 command)

To delete the tail part of phrase, specify the phrase by the CHAN command and the location of deletion by the BLKWR command, and then delete the tail part of phrase by inputting the DEL 2 command.

Leaving the number of blocks with one added to the block data input by the BLKWR command, the succeeding blocks can be deleted. For example, assume that five blocks in a phrase are recorded. To delete three blocks succeeding to the header two blocks, input "01" by the BLKWR command.

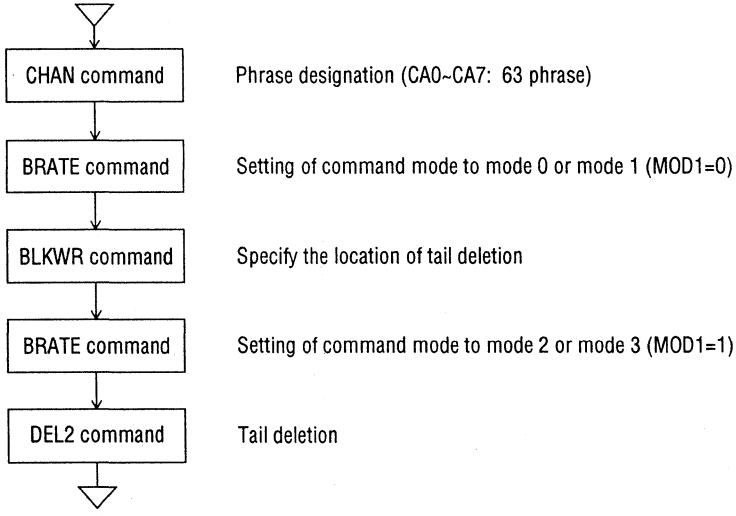
5 blocks → Deletion of tail part → 2 blocks



After the tail part of phrase is deleted by the DEL 2 command, the number of blocks in the channel index area, stop block and address ch00 are renewed. In this case, the contents of stop frame are not changed. To change these contents, input the block data by the ADRWR command.

The block data input by the BLKWR command must be less than the (number of blocks - 2). In the above example, input block data less than "03".

Tail deletion flow chart



2. Method of recording in the record/playback mode

(1) Before starting the recording operation in the record/playback mode, always perform the deletion of all phrases after turning power on and resetting the MSM6788 by input of the RESET pulse. Otherwise, the address control cannot be performed correctly.

(2) Input the record/playback conditions by the corresponding commands as follows.

VDS command: Voice activation condition (VD0, VD1, VD2, VD3).

BRATE command: Set the command mode to mode 0 (MOD0 = 0, MOD1=0) and specify the bit rate (BR0, BR1).

CHAN command: Select one of 63 phrases ch01~ch3F (CA0~CA5).

BLKWR command: Specify the number of phrase recording blocks (BL0~BL7)

REC command: Set to the recording mode.

(3) Input the START command to start recording

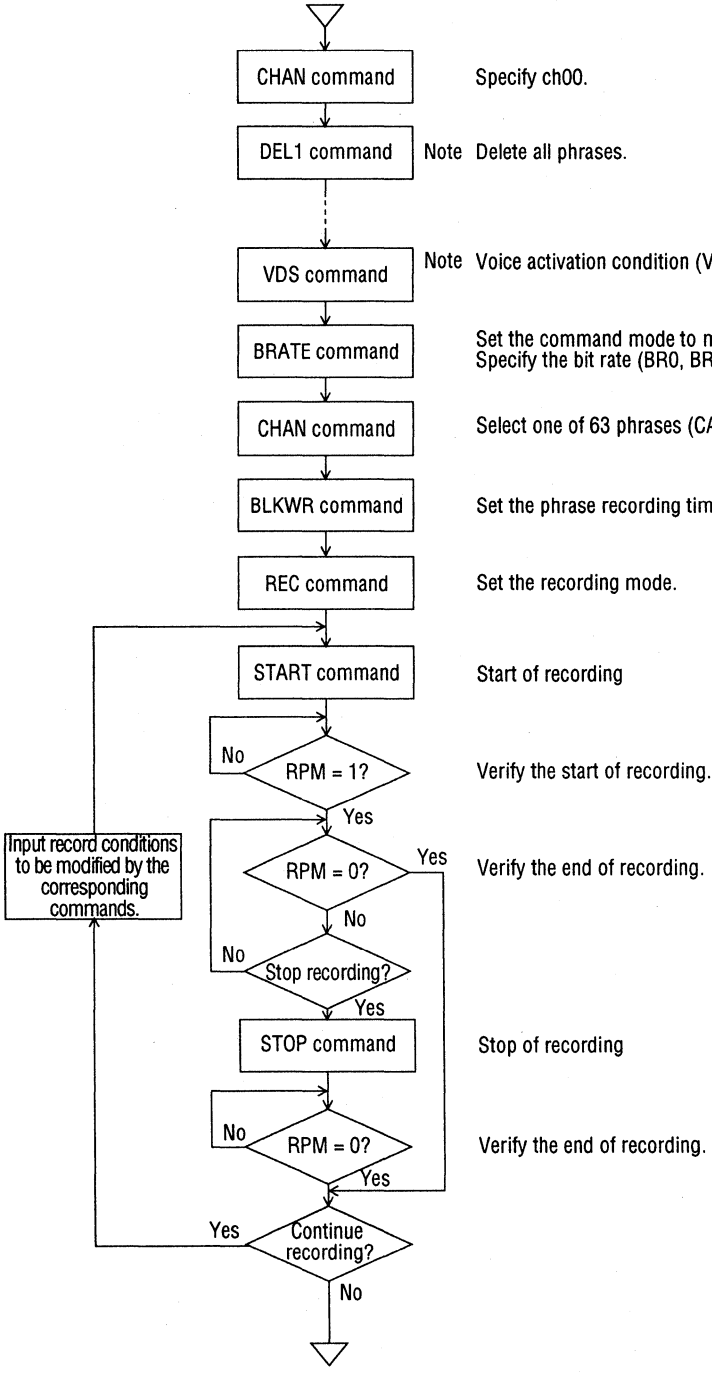
(4) When the number of blocks specified by the BLKWR is reached or when all available blocks are used for recording, recording is finished. The end of recording can be verified by the RPM bit of the status register.

(5) To stop recording in the middle, input the STOP command. The contents of the block counter and the contents of the address counter at this moment are automatically stored in the channel index area as the stop block and the stop address, respectively.

In this case, make sure that recording is finished by examining the RPM bit before inputting the next command.

(6) To continue recording, specify the record/playback conditions to be modified by the corresponding commands and perform the steps (3)~(5).

Flow chart of recording in the record/playback mode



Note: Setting of the command mode by BRATE command is deleted in this flow chart.

3. Playback method in the record/playback mode

3.1 Usual playback

(1) Input the record playback conditions by the corresponding commands as follows.

BRATE command: Set the command mode to mode 0 (MOD0 = 0, MOD1= 0) and specify the bit rate (BR0, BR1).

CHAN command: Select one of 63 phrases ch01~ch3F (CA0~CA5).

LEV command: Specify the playback output level (LV0, LV1).

PLAY command: Set to the playback mode.

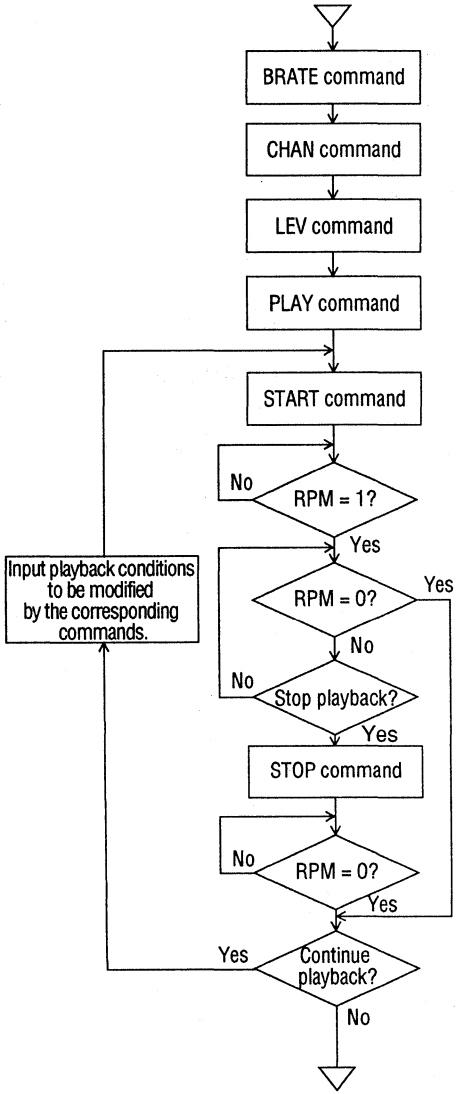
(2) Input the START command to start the playback. The MSM6788 fetches the contents of the block table and the stop address of the specified phrase from the channel index area and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record/playback conditions to be modified by the corresponding commands and perform steps (2)~(4).

Flow chart of playback in the record/playback mode



Set the command mode to mode 0 (MOD0 = 0, MOD1 = 0). Specify the bit rate (BR0, BR1).

Select one of 63 phrases (CA0 ~ CA5)

Set playback output level (LV0, LV1).

Set to the playback mode.

Start of playback

Verify the start of playback.

Verify the end of playback.

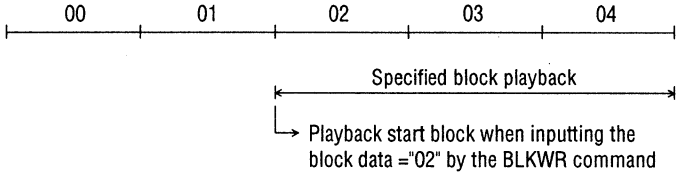
STOP of playback

Verify the end of playback.

3.2 Specified block playback

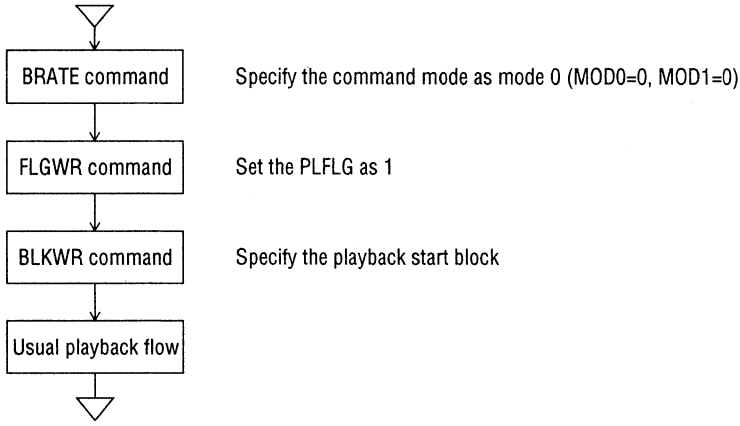
To playback in the middle of recorded phrase, specify the playback start block by the BLKWR command. For example, since each block takes about 2 seconds when using successive 8Mbit RAM at 16kbps bit rate, the playback start block can be specified on the 2-second basis. The playback start block is specified by the block data, with 00 as the header block.

In order to playback from 3rd phrase in the recorded 5 blocks of phrase



The block data input by the BLKWR command must be less than (the number of recorded blocks - 1). In above example, input the block data not higher than "04".

Specfied block playback flow chart



● ROM Playback

1. Method inputting commands

(1) Input the record playback conditions by the corresponding commands as follows.

BRATE command: Set the command mode to mode 1 (MOD0 = 1, MOD1= 0) and specify the bit rate (BR0, BR1).

CHAN command: Select one of 255 phrases ch01~chFF (CA0~CA5).

LEV command: Specify the playback output level (LV0, LV1)

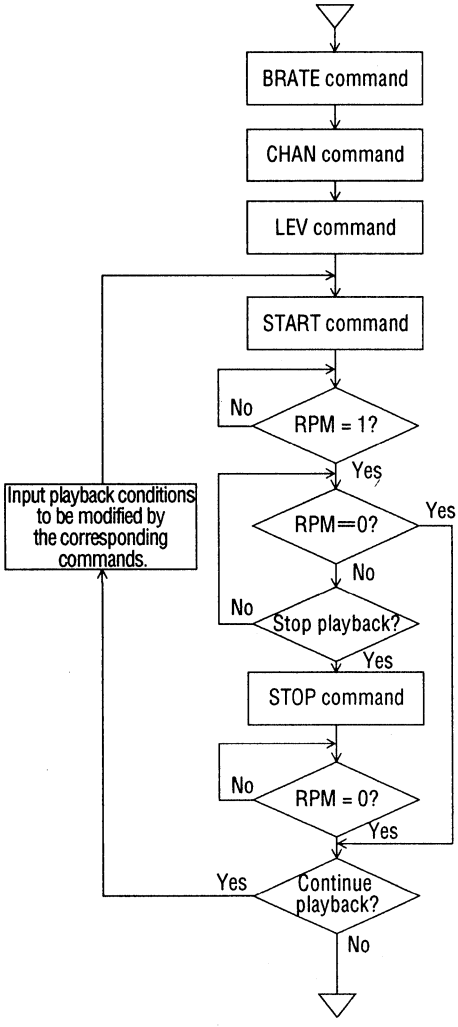
(2) Input the START command to start the playback. The MSM6788 fetches the data of the start address, stop address, and bit rate of the specified phrase from the channel index area of the serial voice ROMs and starts the playback operation.

(3) When the contents of the address counter coincide with the contents of the stop address register, playback is finished. The end of playback is verified by the RPM bit of the status register.

(4) To stop playback in the middle, input the STOP command. In this case, make sure that playback is finished by examining the RPM bit before inputting the next command.

(5) To continue playback, specify the record playback conditions to be modified by the corresponding commands and perform steps (2)~(4).

Flow chart of ROM playback by Input of Address Code



Set the common mode to mode 1 (MOD0 = 1, MOD1 = 0).

Select one of 255 phrases (CA0 ~ CA7)

Set playback output level (LV0, LV1).

Start of playback

Verify the start of playback.

Verify the end of playback.

STOP of playback

Verify the end of playback.

2. Continuous ROM playback

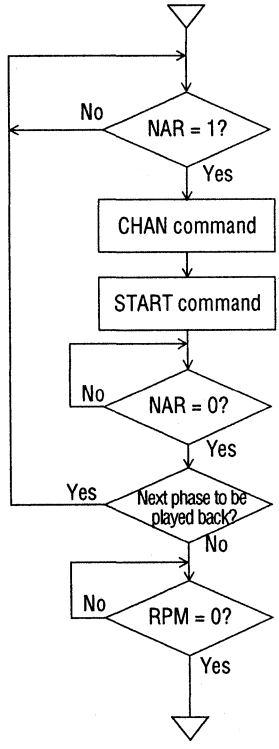
The procedure for playback of different phrases such as the time signal continuously is described below. The command inputting procedure for continuous ROM playback is basically equal to that for a single phrase. In this case, during playback of a phrase, the next phrase to be played back can be specified by the NAR bit of the status register. Continuous playback can also be performed by verifying the end of playback of the phrase using the RPM, instead of use of the NAR bit. To make continuous playback, perform the following procedure.

(1) Specify a phrase by the CHAN command and input the START command to start playback. When the START command is accepted, the NAR bit of the status register goes to 0.

(2) When the NAR bit is changed from 0 to 1 to indicate that the next phrase can be specified and inputted, specify the next phrase to be played back by the CHAN command and input the START command. After the START command is accepted, the NAR bit goes to 0.

(3) In the same way as mentioned above, repeat the designation of a phrase and input of the START command verifying the state of the NAR bit.

Flow chart of continuous ROM playback



Verify whether a phase can be specified or not.

Specify one of 255 phrases (CA0 ~ CA7).

The specified phase is accepted.

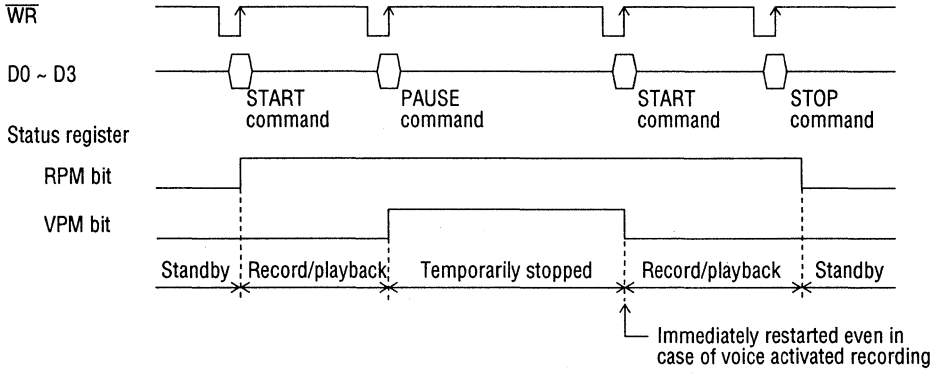
Verify whether playback of the specified phase is accepted or not.

Verify the end playback.

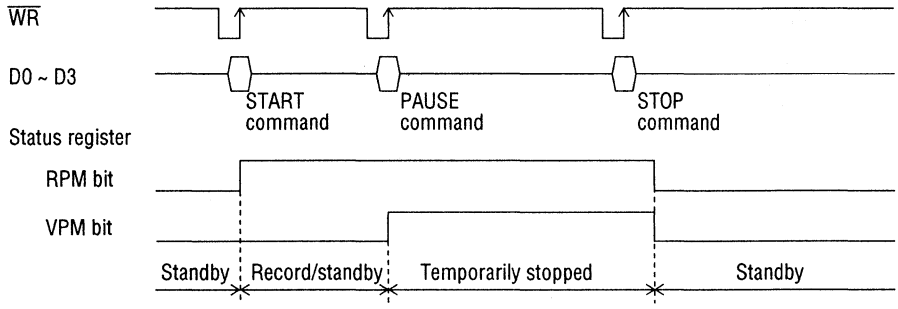
● Method of Stopping Temporarily Record/Playback (by the PAUSE Command)

The record/playback operation in progress can be stopped temporarily by inputting the PAUSE command. The record/playback operation stopped using the PAUSE command can be restarted by inputting the START command. During temporary stop state, the VPM bit of the status register is 1 and the RPM bit is 1.

If the START command is input to restart the recording operation that is temporarily suspended by the PAUSE command in the voice activated recording mode, the recording will be started immediately even in the state of silence. The PAUSE command is invalid during standby state for temporarily stopped state, and standby state for voice.



When the STOP command is input during temporarily stopped state, the record/playback operation is finished and the MSM6788 is placed in the standby state.



● Transferring Data to/from External Memories

1. Method of transferring data to/from user data area (by the CHRW command)

The MSM6788 can transfer data to/from the user area in the channel index area of external RAM using the CHRW command. Before starting this data transfer operation, a desired phrase must be specified using the CHAN command. The memory capacity for each phrase is 704 bits (176 nibbles). The read/write operation must be performed for the data that does not exceed this memory capacity per phrase.

The contents of the user area for a specified phrase or for all phrases will be cleared to all 0s (0h data) using the CHAN and DEL commands.

The following shows the procedure for inputting the CHRW command.

(1) Set the command mode to mode 0 or mode 1 using the BRATE command (MOD0, MOD1).

(2) Specify a phrase using the CHAN command.

(3) After inputting the CHAN command, wait for BUSY state duration. The end of the BUSY state duration can also be verified by the BUSY bit of the status register.

(4) To write data, input the REC command and then input the data to be written by applying the $\overline{WR}$ pulse. It is required to wait for the busy state duration between the contiguous $\overline{WR}$ pulses.

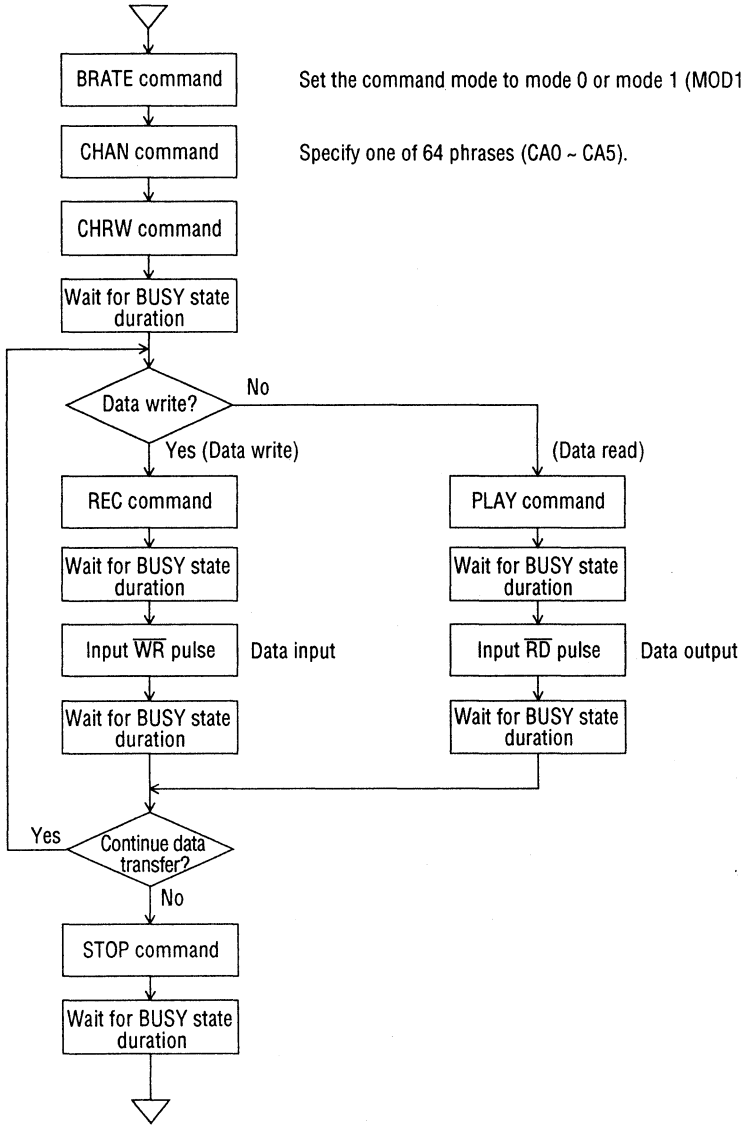
When the data writing operation is performed by inputting a single input of the CHRW command, the state of the BUSY bit of the status register can be verified by inputting the $\overline{RD}$ pulse. When the data read operation is performed with the data write operation, the state of the BUSY bit cannot be verified by inputting the $\overline{RD}$ pulse.

(5) When reading data, wait for the BUSY state duration after inputting the PLAY command and then input the $\overline{RD}$ pulse. With this operation, 4-bit data will be output via the data bus.

(6) To continue the data read or write operation, specify the read or write mode using the PLAY or REC commands.

(7) To stop the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer by the CHRW command



2. Method of transferring data to and from external RAM (by the DTRW command)

The data transfer to/from external RAM is performed using the DTRW command. After inputting the DTRW command, specify an address to be accessed for data read/write. The transfer of each 4-bit data is performed from the starting nibble of the specified address. The address designation can be made only in the X direction and random address designation cannot be made in the Y direction to select an arbitrary address in the Y direction.

The read/write operation can be made within the same 8Mbit ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$) range by entering the DTRW command once. But when the read/write operation is extended to another 8Mbit range, cancel the DTRW command before addressing by re-entering the DTRW command.

(1) Set the common mode to mode 2 (MOD0 = 0, MOD1 = 1)

(2) Input the DTRW command

(3) Specify the X address in a RAM by inputting the $\overline{WR}$ pulse five times. Wait for the BUSY state duration. The BUSY state can be verified by examining the state of the BUSY bit of the status register. The 2nd nibble of the DTRW command is a dummy nibble. Always input 0h data into the 2nd nibble.

(4) For data writing, input the REC command and input the data to be written by inputting the $\overline{WR}$ pulse. Wait for the BUSY state duration between the contiguous $\overline{WR}$ pulses.

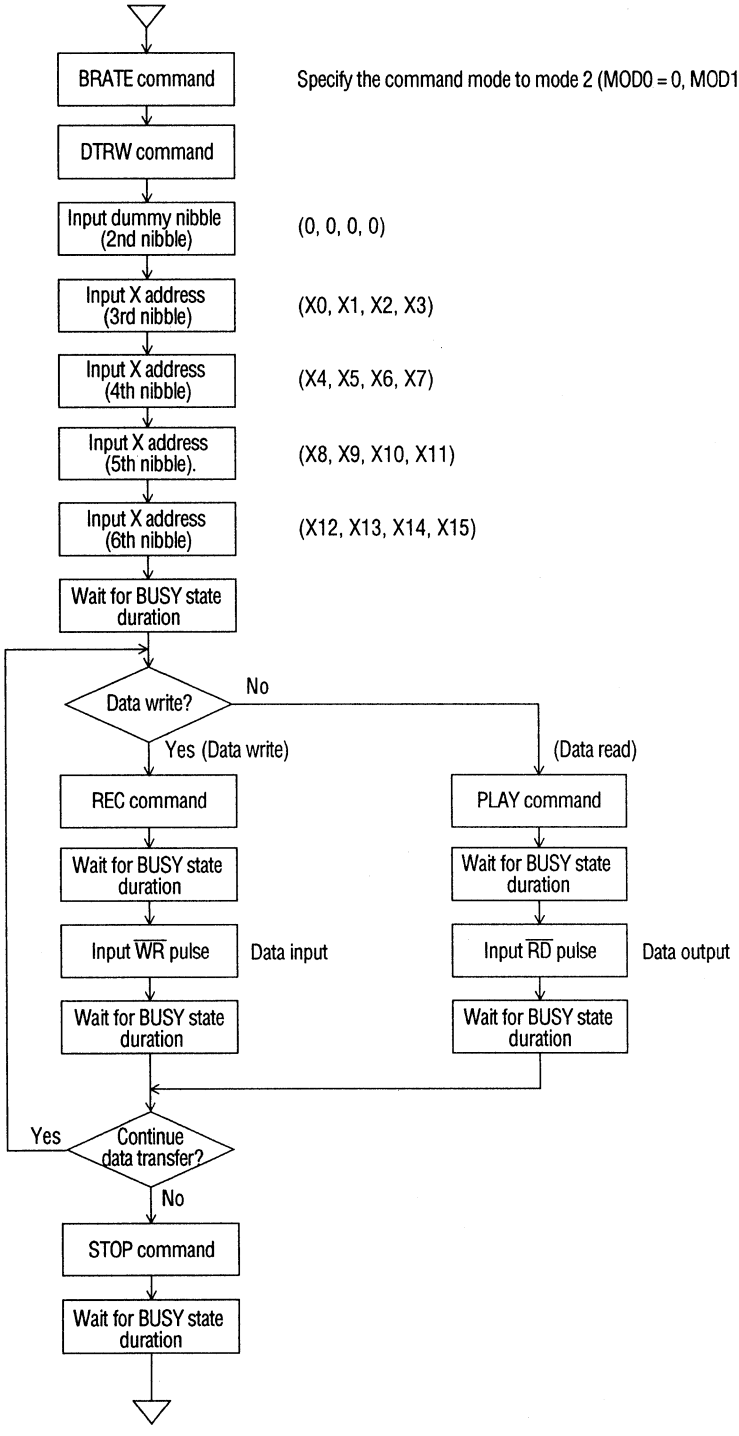
To make the data write operation by a single input of the DTRW command, the state of the BUSY bit can be verified by inputting the $\overline{RD}$ pulse. When data write and data read operations are performed jointly, the state at the BUSY bit cannot be verified using the $\overline{RD}$ pulse.

(5) To read data, input the PLAY command and then input the $\overline{RD}$ pulse after waiting for the BUSY state duration. With this operation, 4-bit data will be output via the data bus.

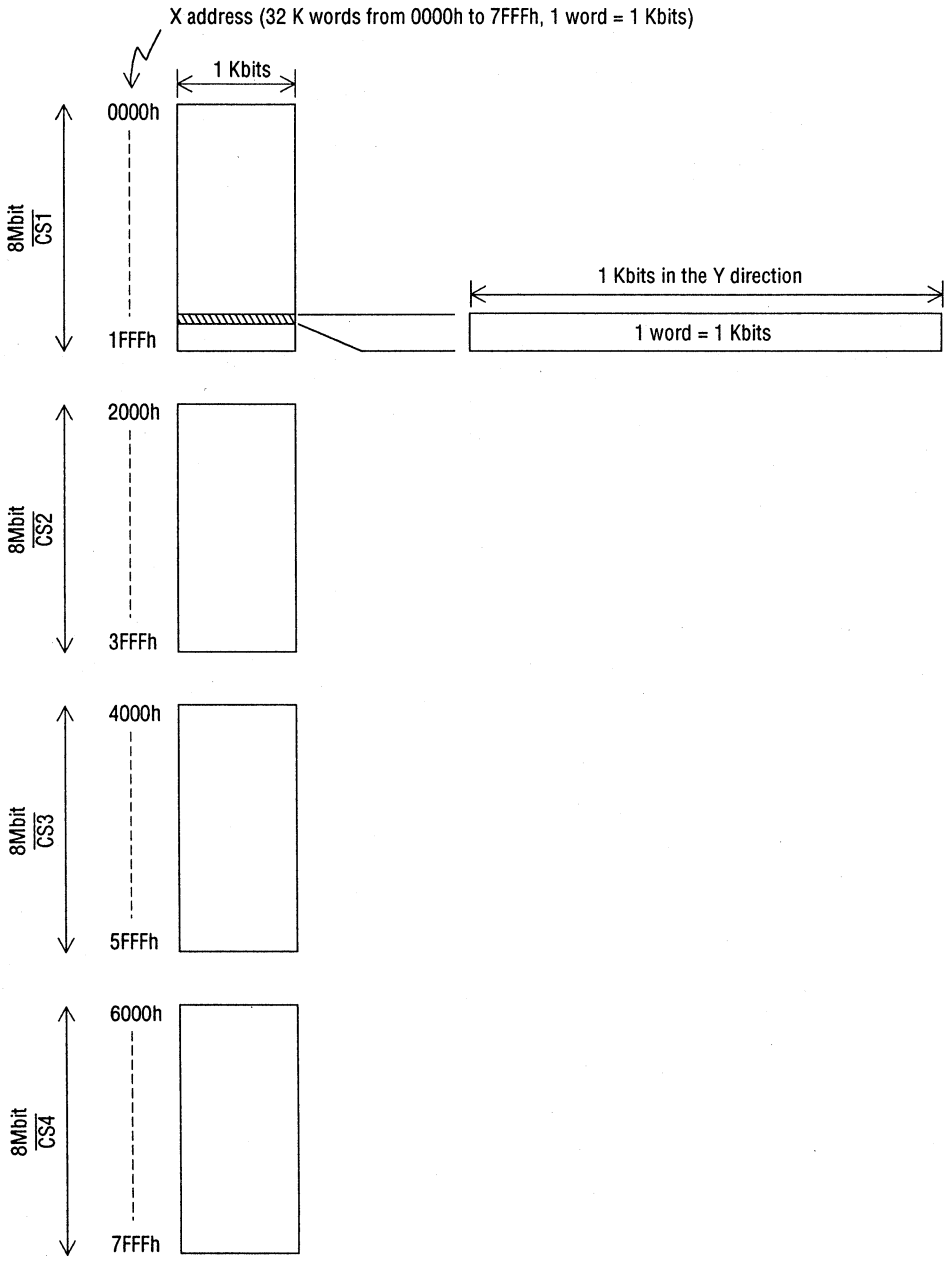
(6) To continue data read/write operation, specify the read or write mode using the PLAY or REC command and make data transfer operation.

(7) To finish the data read/write operation, input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data transfer using the DTRW command



Address Space of RAM
(by the DTRW command)



3. Method of reading data from external serial voice ROMs (by the DTRD command)

Data from external serial voice ROMs can be read using the DTRD command. After inputting the DTRD command, specify the address to be read. Data is read in groups of 4 bits from the specified.

With the input of a single DTRD command, continuous read/write operation can be made in the range of addresses assigned to the same serial voice ROM. When the read/write operation is extended to two or more serial voice ROMs, it is necessary to stop temporarily the read/write operation each time the operation is finished for the serial voice ROM, and set the address for another serial voice ROM using the DTRD command.

The following shows the procedure for inputting the DTRD command.

(1) Set the command mode to mode 3 (MOD0 = 1, MOD1 = 1).

(2) Input the DTRD command.

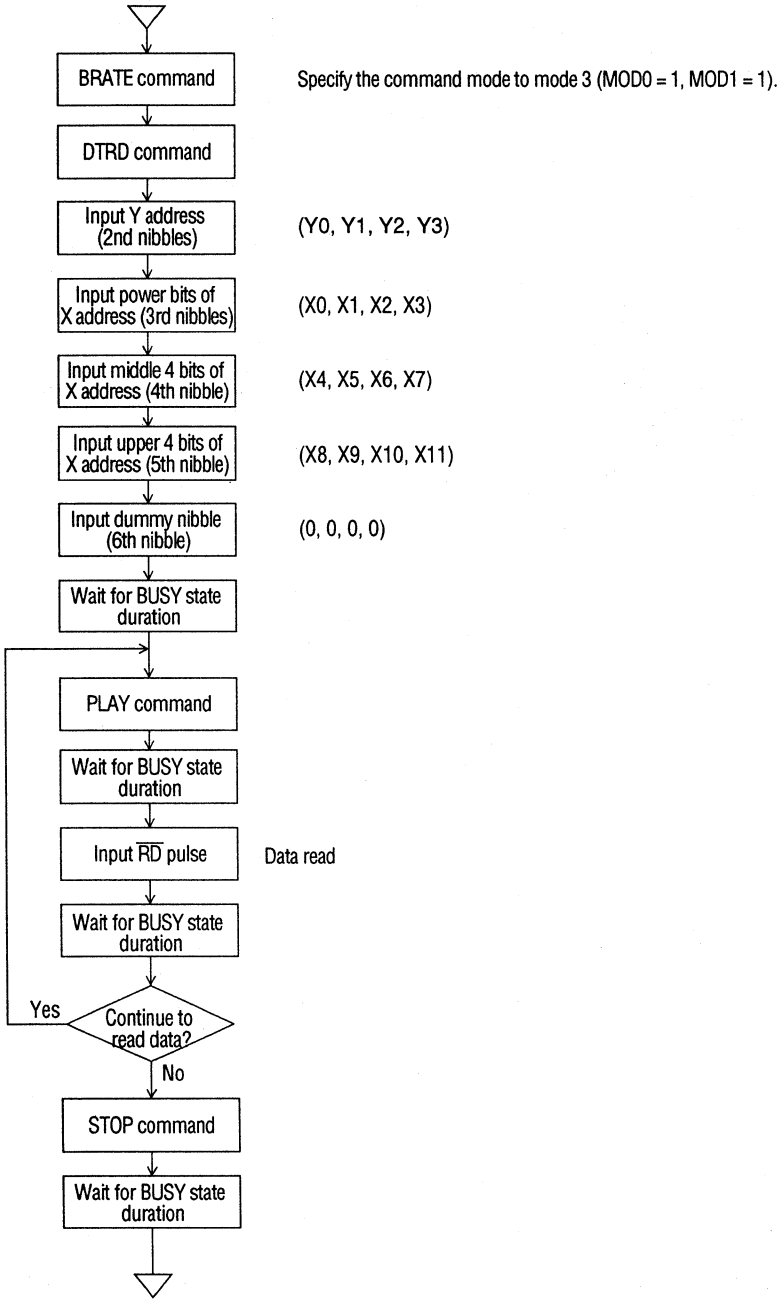
(3) Specify the X address and Y address of the serial voice ROM by inputting the $\overline{WR}$ pulse five times. Then, wait for the BUSY state duration. The 6th nibble is a dummy nibble. Always input 0h data into this 6th nibble.

(4) Input the PLAY command and wait for the BUSY state duration. Then, input the $\overline{RD}$ pulse, so that 4-bit data will be output via the data bus.

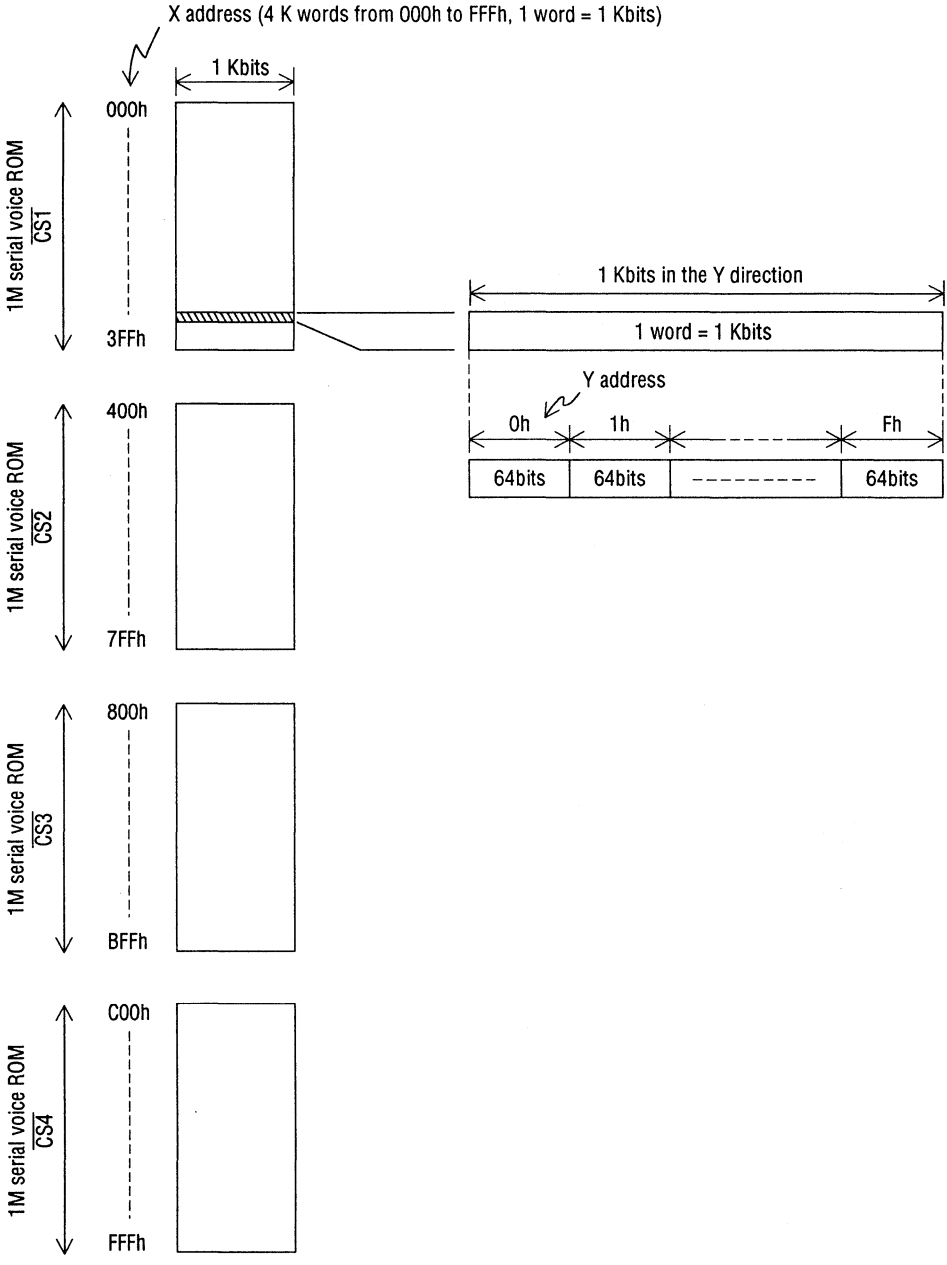
(5) To continue data read operation, perform the data read operation inputting the PLAY command and $\overline{RD}$ pulse in the same way as mentioned above.

(6) To finish the data read operation input the STOP command. After waiting for the BUSY state duration, the next command can be input.

Flow chart of data read using the DTRD command



Address Space of Serial Voice ROMs (by the DTRD command)



● Methods of Record/Playback Using the EXT Command

When using not the RAM but an SRAM or hard desk to store the voice data, record/playback operation is made by the EXT command.

In the record/playback operation by the EXT command, the voice data (SBC data) is input/output through the direct bus on the frame basis. In this case, since address control and external RAM control are not made, the microcontroller controls the recording time and address. Stopping temporarily record/playback, voice start, and specifying the phrase can not be established. The enable commands are PLAY, REC, STOP, BRATE (BR0, BR1 data), LEV, and EXT.

1. Status register at the EXT command and pin functions

The contents of status registers at the EXT command are as follows.

(1) BUSY bit: Goes high during transferring SBC. Input the following $\overline{WR}$ or $\overline{RD}$ pulses when changed to low level. Without confirming the BUSY bit, following $\overline{WR}$ and $\overline{RD}$ pulses can be input after the BUSY state duration.

(2) RPM bit: Goes high during record/playback operation by the EXT command.

(3) VPM bit: After the EXT command is input, the clock at the same frame cycle as the one at the MON pin. This bit transfers one frame of SBC data between high levels.

(4) NAR bit: When the SBC within one frame is transferred, set to low level, and when VPM bit and MON pin go low, set to high level.

The functions of MON and EXTD pins are as follows.

(5) MON pin: After the EXT command is input, the clock is output at the frame cycle. While the MON pin is set high, one frame of SBC data is transferred. The VPM bit of status register also outputs the same clock.

(6) EXTD pin: When the SBC data is input, set the EXTD pin high . In case of the command input and status output, set it low.

2. Methods of EXT recording

(1) Specify the bit rate using BRATE command data bit BR0 and BR1.

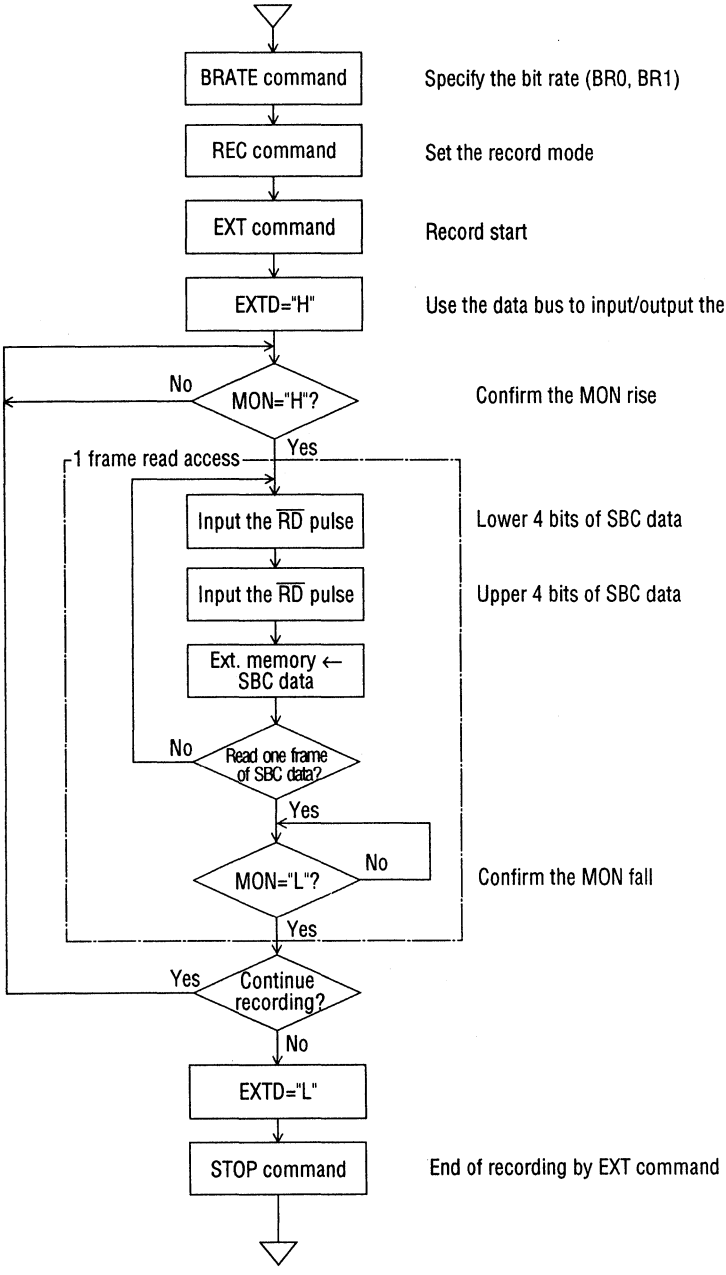
(2) Set to the record mode by inputting the REC command.

(3) Start the record, inputting the EXT command. Then the clock pulse at the frame cycle is output at the MON pin.

(4) Input the $\overline{RD}$ pulse while the MON pin goes high, store one frame of SBC data output from the data bus. Set the EXTD pin to high level when inputting the SBC data. As for the method of reading the one frame of SBC data, refer to "4. Method of reading/writing the SBC data."

(5) When inputting the STOP command, the recording operation is finished. Since recording continues until the STOP command is input, recording at any duration can be established.

Flow chart of recording by the EXT command



3. Method of playback using the EXT command

(1) Specify the bit rate when recorded, using the BRATE command data bit BR0 and BR1.

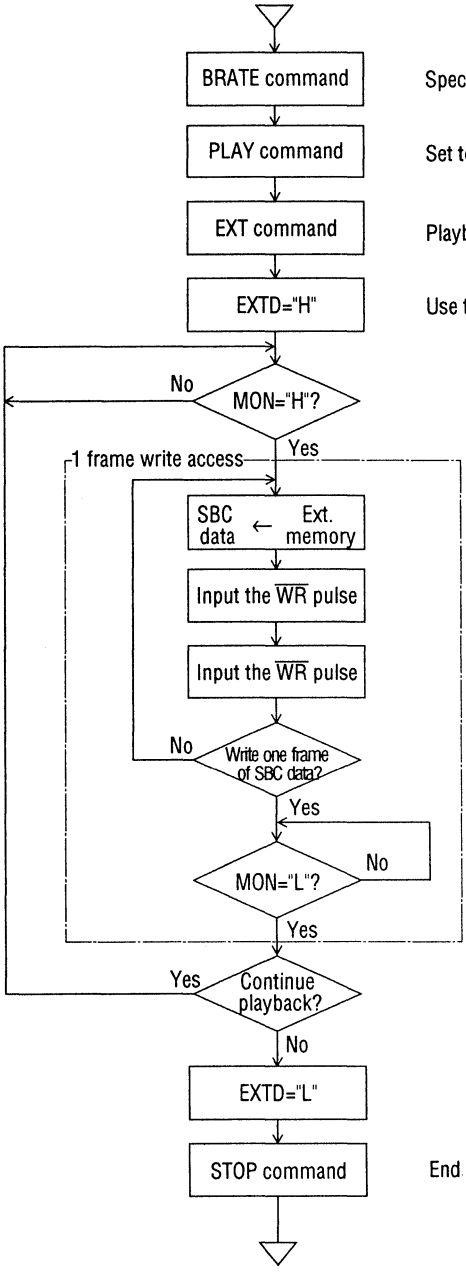
(2) Set to the playback mode by inputting the PLAY command.

(3) Start the playback operation by inputting the EXT command. The clock pulse at the frame cycle is output at the MON pin.

(4) Input the $\overline{WR}$ pulse while the MON pin goes high, and input one frame of SBC data from the data bus. When inputting the SBC data, set the EXTD pin high. As for the method of writing data within one frame, refer to "4. Methods of reading/writing the SBC data."

(5) When inputting STOP command, the playback operation is finished.

Flow chart of playback by the EXT command



Specify the bit rate (BR0, BR1)

Set to the playback mode

Playback start

Use the data bus to input/output the SBC data

Confirm the MON rise

Lower 4 bits of SBC data

Upper 4 bits of SBC data

The number of bits varies by the 1st frame and the 2nd and succeeding frame.

Confirm the MON fall

End of playback by EXT command

4. Method of reading and writing the SBC data

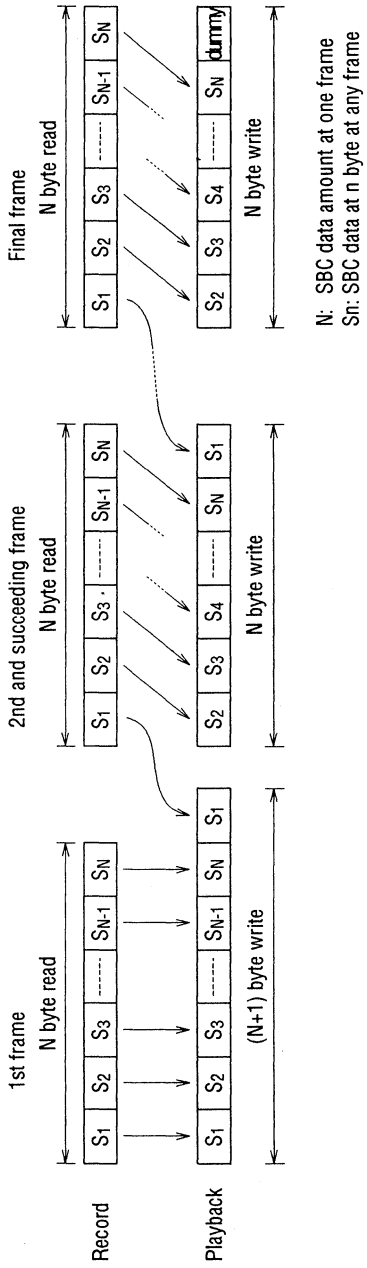
Input/output one frame of SBC data while the MON pin and VPM bit goes high. 1 byte of SBC data is divided into two portion, and input the lower 4 bits and then upper 4 bits. Set the EXTD pin low when the inputting and outputting the SBC data.

In the recording operation, number of bytes at one frame over all frames are read. In the playback operation, at the 1st frame, number of bytes at one frame + 1 byte are written and at the 2nd and succeeding frames, number of bytes at one frame is written.

	Bit rate	1st frame		2nd frame	
		bytes	$\overline{RD}$, $\overline{WR}$ pulses	bytes	$\overline{RD}$, $\overline{WR}$ pulses
Recording	16.0 kbps	24	48	24	48
	12.6 kbps	19	38	19	38
	10.0 kbps	15	30	15	30
Playback	16.0 kbps	25 (Note)	50 (Note)	24	48
	12.6 kbps	20 (Note)	40 (Note)	19	30
	10.0 kbps	16 (Note)	32 (Note)	15	30

In the playback operation, at the 1st frame, the data at 1st frame and the data at the 1 byte of 2nd frame are written. At the 2nd and succeeding frame, the data at the 2nd byte of its own frame and the dummy data at the following frame are written. At the final frame, the data at the final frame and 1 byte of dummy data are written.

The method of reading and writing the SBC data is illustrated as follows.

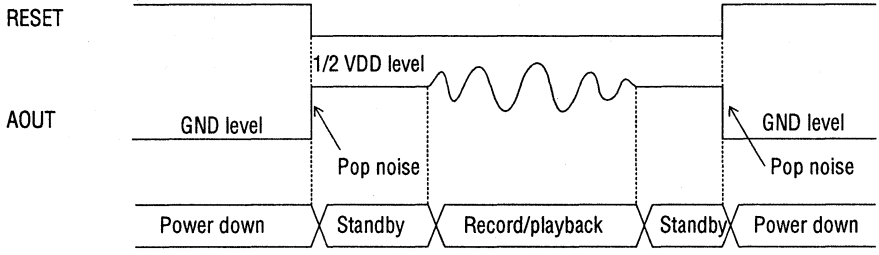


● Suppression of Pop Noise at AOUT Output (LEV Command)

The MSM6788 has a on-chip pop noise suppression circuit to prevent pop nose from being generated due to sharp changes of the DC level of the analog output (at the AOUT pin). The enabled or disabled state of this pop noise suppression circuit can be selected using the ACON pin. When the ACON pin is low, this circuit is disabled and when high, this circuit is enabled.

1. When the POP noise suppression circuit is disabled (ACON = low)

When the RESET pin is low, the DC level at the AOUT pin is the ground level, and when the RESET pin is high, the DC level at the AOUT pin is the 1/2 V_{DD} level. Each time the state of the RESET pin is changed, the DC level is changed sharply and pop noise is generated.

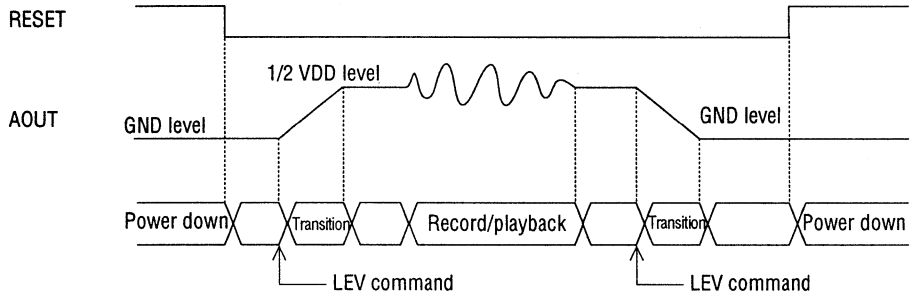


2. When the POP noise suppression circuit is enabled (ACON = high)

The transition of the DC level at the AOUT (analog output) pin is controlled using the LEV command. When the RESET pulse (low) is applied to the RESET pin, the DC level at the AOUT output pin goes to the ground level. If the pop noise suppression circuit is activated using the PN0 and PN1 bits of the 2nd nibble of the LEV command, the DC level at the AOUT output pin will be changed from the ground level to the 1/2 V_{DD} level or from the 1/2 V_{DD} level to the ground level slowly to prevent pop noise from being generated.

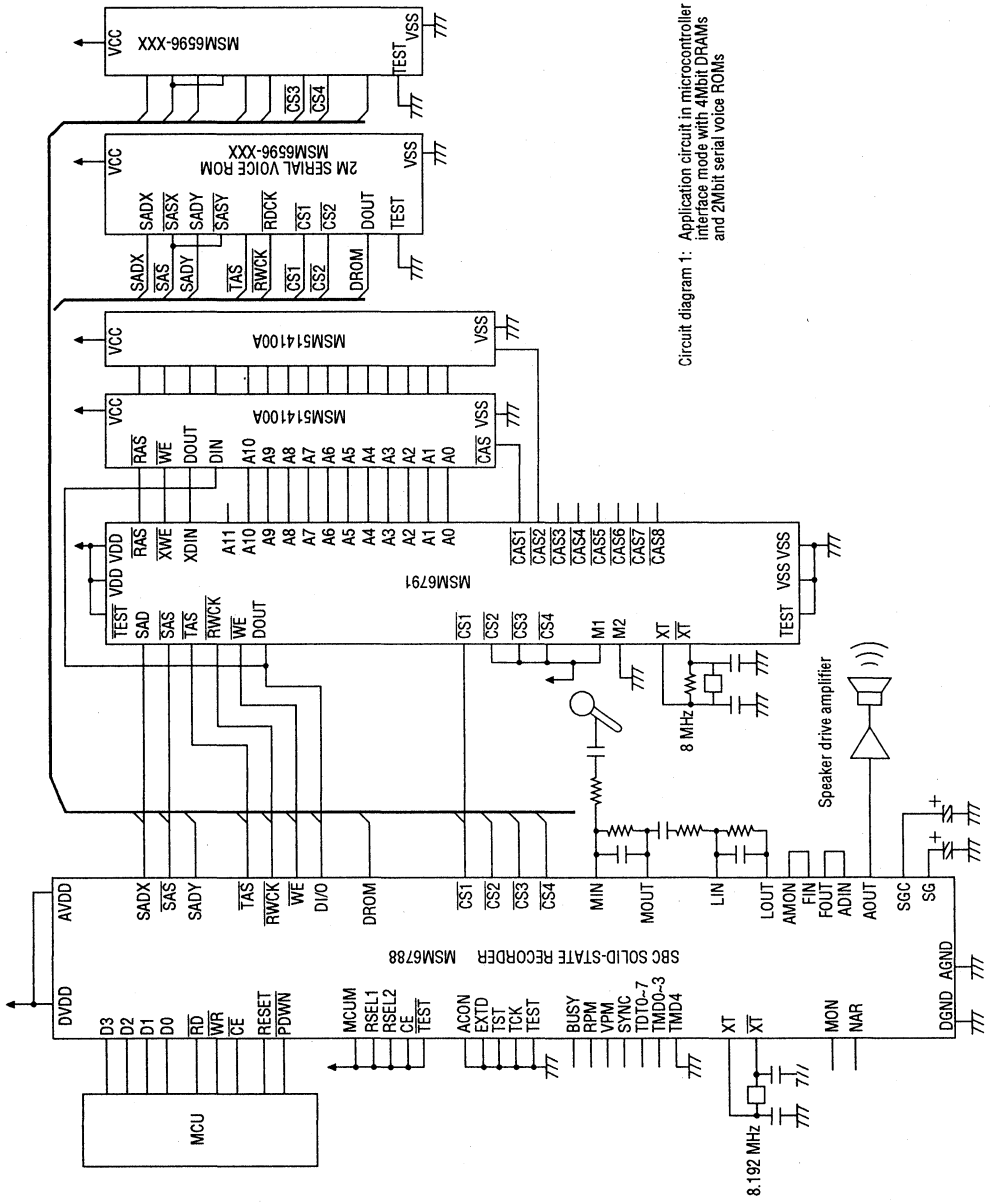
Before starting the record/playback operation, always set the DC level at the AOUT pin to the 1/2 V_{DD} level using the LEV command. When enabling the DC level transition function by the LEV command, first specify the playback mode and then input the LEV command.

PN1	PN0	DC level transition
0	0	Disabled
0	1	Disabled
1	0	Transition from ground to 1/2 VDD
1	1	Transition from 1/2 VDD to ground



■ EXAMPLE OF APPLICATION CIRCUIT

● The circuit diagram 1 shows an application circuit example, which the MSM6788 is used in the microcontroller interface mode, and two 4Mbit DRAMs are used as record/playback memories by connecting a DRAM interface LSI,MSM6791, and two serial voice ROMs also are connected .

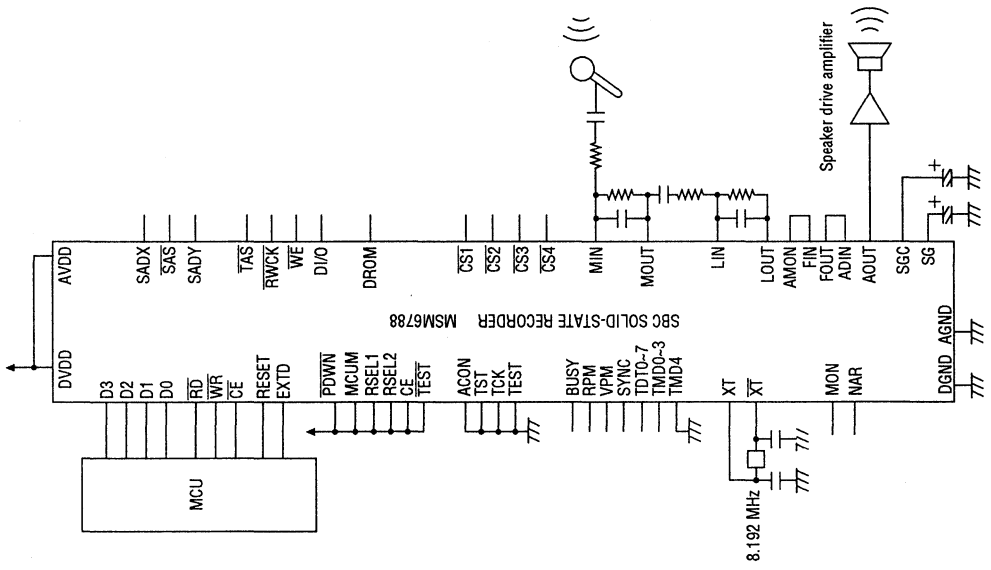


Circuit diagram 1: Application circuit in microcontroller interface mode with 4Mbit DRAMs and 2Mbit serial voice ROMs

■ EXAMPLE OF APPLICATION CIRCUIT

● The circuit diagram 2 shows and application circuit example, which the MSM6788 is used with EXT command .

Circuit diagram 2.



Voice Register /ROM

OKI Semiconductor

MSM6389

1,048,576-WORD x 1-BIT SOLID STATE RECORDER DATA REGISTER

GENERAL DESCRIPTION

MSM6389 is a solid state recorder data register in 1,048,576 words x 1 bit configuration.

MSM6389 has a built-in internal address generator circuit allowing continuous serial read/write operation by single external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

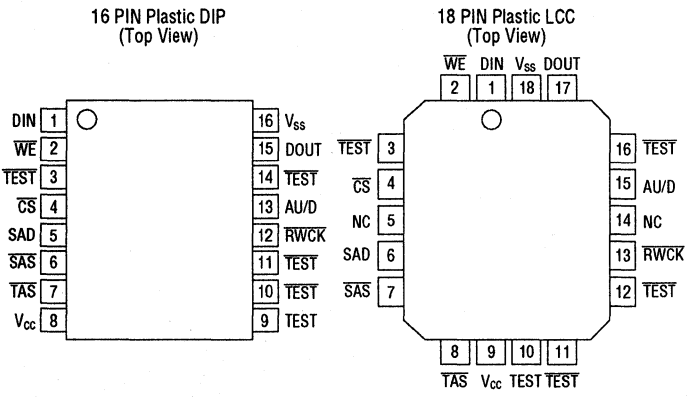
18-pin plastic QFJ (PLCC) is used as the pack are and the operating temperature range is between 0°C and 70°C.

MSM6389 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be built-in combination with OKI's voice synthesizer LSIs, MSM6388 and MSM6588.

FEATURES

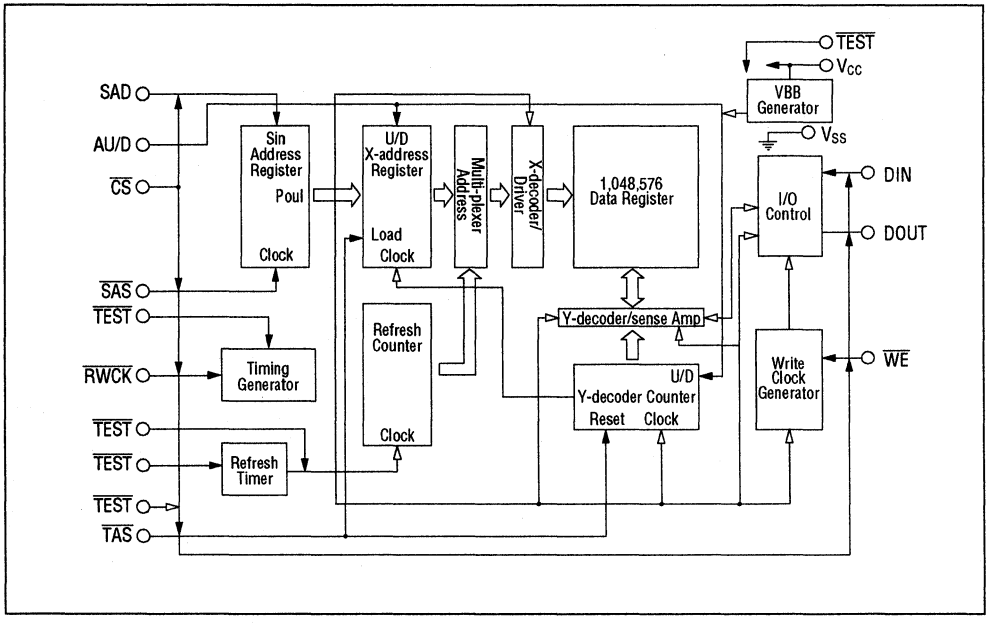
- Configuration: 1,048,576 x 1 bit
- Serial access operation:
  - Serial access time 3.0μs
  - Serial read/write cycle time 4.0μs
- Low current consumption:
  100 μA max. (for data holding, V_{CC}=4.0V)
- Wide operating supply voltage range:
  Single 3.5 to 5.5V
- Refresh operation:
  Self-refresh (refresh-free)
- 18-pin Plastic QFJ (PLCC)
  (QFJ18-P-R290)
- 16-pin Plastic DIP
  (DIP16-P-300-W1)

PIN CONFIGURATION



1 : Data input
2 : Write enable
3 : Test input
4 : Chip select
5 : No connection
6 : Serial address data
7 : Serial address strobe
8 : Transfer address strobe
9 : Power supply (+5V)
10 : Test input
11 : Test input
12 : Test input
13 : Read/write clock
14 : No connection
15 : Address up/down select
16 : Test input
17 : Data output
18 : Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTIC

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Terminal voltage	V_T	T_a = 25°C, relative to V_{SS}	−1.0 ~ +7.0	V
Output short-circuit current	I_{OS}	T_a = 25°C	50	mA
Power dissipation	P_D	T_a = 25°C	1	W
Operating temperature	T_{Op}	—	0 ~ +70	°C
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Recommended Operating Conditions

(Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Terminal voltage	V_{CC}	3.5	5.0	5.5	V
Terminal voltage	V_{SS}	0	0	0	V
"H" input voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" input voltage	V_{IL}	−0.5	0	0.5	V

DC Characteristics

(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

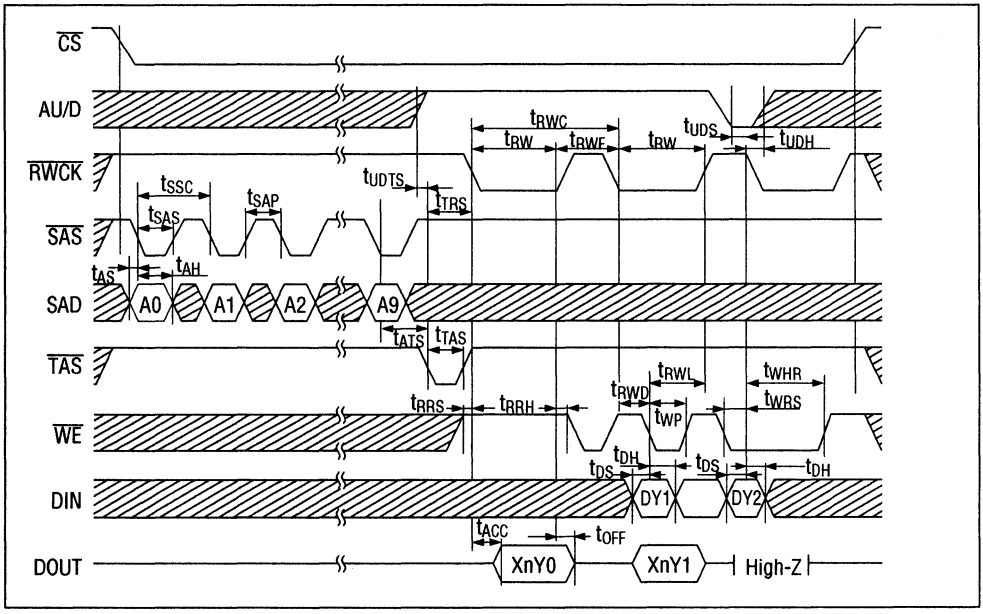
Parameter	Symbol	Conditions	Min.	Max.	Unit
"H" output voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input leakage current	I_{LI}	V_I = 0V ~ V_{CC}	−1	1	µA
Output leakage current	I_{LO}	V_O = 0V ~ V_{CC}	−10	10	µA
Supply current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4µs	—	5	mA
Supply currnet (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA

• AC Characteristics

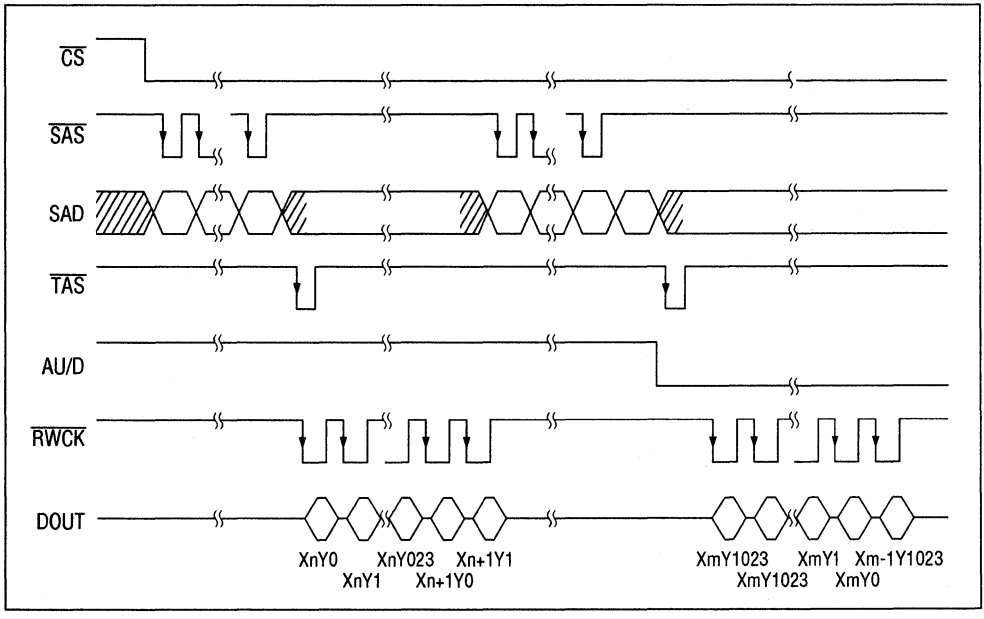
(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Refresh cycle	t_{REF}	—	—	ms
Read/write cycle time	t_{RWC}	4,000	—	ns
Access time	t_{ACC}	—	3,000	ns
Output turn off delay time	t_{OFF}	0	50	ns
Input signal rise/fall time	t_T	3	50	ns
$\overline{RWCK}$ precharge time	t_{RWP}	1,000	—	ns
$\overline{RWCK}$ pulse width	t_{RW}	3,000	10,000	ns
$\overline{SAS}$ cycle time	t_{SSC}	100	—	ns
$\overline{SAS}$ pulse width	t_{SAS}	50	—	ns
$\overline{SAS}$ precharge time	t_{SAP}	50	—	ns
Address setup time	t_{AS}	0	—	ns
Address hold time	t_{AH}	50	—	ns
$\overline{TAS}$ setup time	t_{ATS}	50	—	ns
$\overline{TAS}$ to $\overline{RWCK}$ setup time	t_{TRS}	50	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	50	—	ns
Read command setup time	t_{RRS}	0	—	ns
Read command hold time	t_{RRH}	250	—	ns
Write command setup time	t_{WRS}	0	—	ns
Write command hold time	t_{WRH}	50	—	ns
Write command pulse width	t_{WP}	50	—	ns
Write command to $\overline{RWCK}$ lead time	t_{RWL}	50	—	ns
Data setup time	t_{DS}	0	—	ns
Data hold time	t_{DH}	50	—	ns
$\overline{RWCK}$ to $\overline{WE}$ delay time	t_{RWD}	100	—	ns
AU/D setup time	t_{UDS}	0	—	ns
AU/D hold time	t_{UDH}	50	—	ns
AU/D to $\overline{TAS}$ setup time	t_{UDTS}	0	—	ns

Read/Write/Read Modify Write Cycle



Address Up/Down Select Mode



PIN FUNCTIONS AND OPERATION MODES

Pin	Function
SAD	(Serial Address Input) Pin for inputting the read/write starting address-Designation in units of 1024 words is possible. The 1,024 address data can be input as 10-bit (A0-A9) serial from the SAD pin.
$\overline{SAS}$	(Serial address strode) Pin for the clock used to store the serial address data into the internal register.
$\overline{TAS}$	(Address transfer strode) Input pin for setting the serial address data stored in the address register to the internal address counter. When the $\overline{TAS}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.
$\overline{RWCK}$	(Read/write clock) Input pin for the data register information read/write clock. Internal operation starts at the following edges of $\overline{RWCK}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{RWCK}$ falls.
$\overline{WE}$	(Write enable) Input pin for selecting the read mode, write mode or read modify write mode. The read mode is set when $\overline{WE}$ is "H", and the write mode is set when $\overline{WE}$ is "L". When $\overline{WE}$ falls from "H" to "L" while $\overline{RWCK}$ is active, the read modify write mode is set.
DIN	(Data input) Input pin for write data. The information at the data input pin is stored at the falling edge of $\overline{RWCK}$ in the write mode, and at the falling edge of $\overline{WE}$ in the read modify write mode.
DOUT	(Data output) The data output pin is always in kept in the high impedance state when $\overline{RWCK}$ or $\overline{CS}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{RWCK}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.
AU/D	(Address up/down select) Input pin for selecting the direction of automatic address updating. When the $\overline{TAS}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{RWCK}$ is input. When the $\overline{TAS}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y. Then the address is decremented by 1 every time $\overline{RWCK}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS}, t_{UDH} are satisfied.
$\overline{CS}$	(Chip select) Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM6389s by connecting the data input and output pins.

OKI Semiconductor

MSM6587

524,288-WORD x 1-BIT SERIAL REGISTER

GENERAL DESCRIPTION

MSM6587 is a serial register in 524,288 words x 1 bit configuration featuring medium speed operation with low-power consumption.

MSM6587 has a built-in internal address generator circuit allowing continuous serial read/write operation by external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words impossible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power consumption.

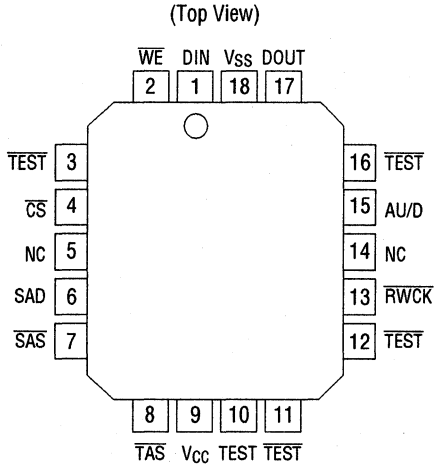
18-pin plastic QFJ (PLCC) is used as the package and the operating temperature range is between 0°C and 70°C.

MSM6587 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be built-in combination with OKI's voice synthesizer LSIs, MSM6388 and MSM6588.

FEATURES

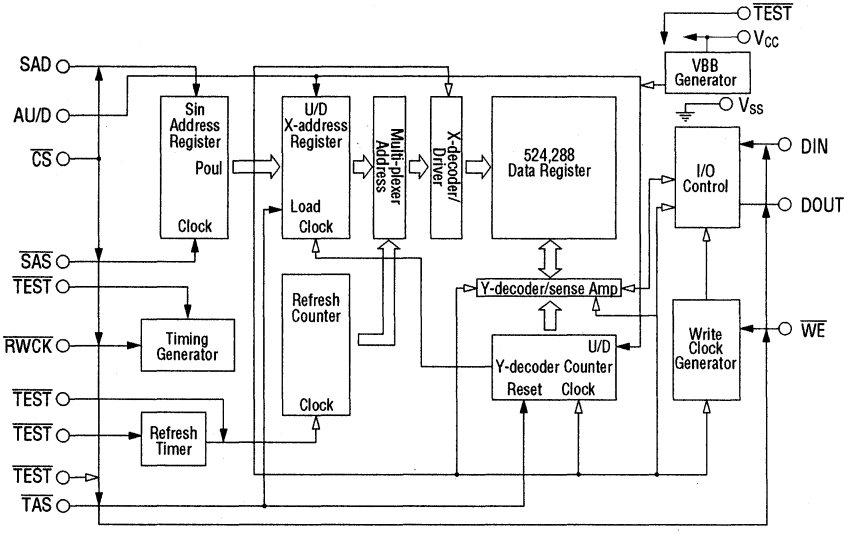
- Configuration: 524,288 x 1 bit
- Serial access operation:
  - Serial access time 3.0 μs
  - Serial read/write cycle tiem 4.0 μs
- Low current consumption:
  - 100 μA max. (for data holding, Vcc=4.0V)
- Wide operating supply voltage range:
  - Single 3.5 to 5.5V
- Refresh operation:
  - Self-refresh (refresh-free)
- 18-pin Plastic QFJ (PLCC)
  - (QFJ18-P-R290)

PIN CONFIGURATION



1 : Data input
2 : Write enable
3 : Test input
4 : Chip select
5 : No connection
6 : Serial address data
7 : Serial address strobe
8 : Transfer address strobe
9 : Power supply (+5V)
10 : Test input
11 : Test input
12 : Test input
13 : Read/write clock
14 : No connection
15 : Address up/down select
16 : Test input
17 : Data output
18 : Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Terminal voltage	V_T	T_a = 25°C, relative to V_{SS}	−1.0 ~ +7.0	V
Output short-circuit current	I_{OS}	T_a = 25°C	50	mA
Power dissipation	P_D	T_a = 25°C	1	W
Operating temperature	T_{Op}	—	0 ~ +70	°C
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Recommended Operating Conditions

(Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Terminal voltage	V_{CC}	3.5	5.0	5.5	V
Terminal voltage	V_{SS}	0	0	0	V
"H" input voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" input voltage	V_{IL}	−0.5	0	0.5	V

DC Characteristics

(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

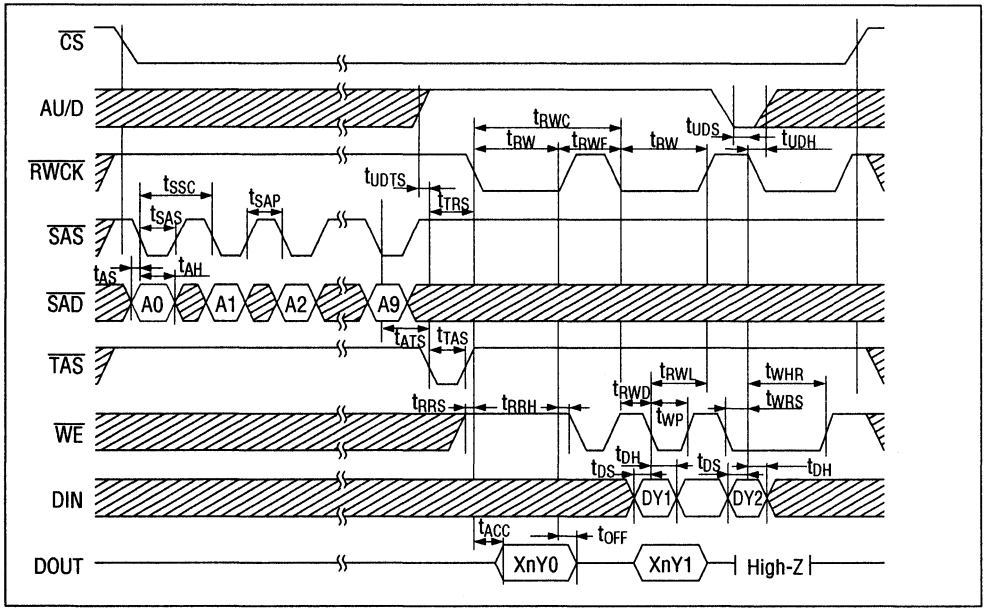
Parameter	Symbol	Conditions	Min.	Max.	Unit
"H" output voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input leakage current	I_{LI}	V_I = 0V ~ V_{CC}	−1	1	µA
Output leakage current	I_{LO}	V_O = 0V ~ V_{CC}	−1	1	µA
Supply current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4µs	—	5	mA
Supply currnet (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA

• AC Characteristics

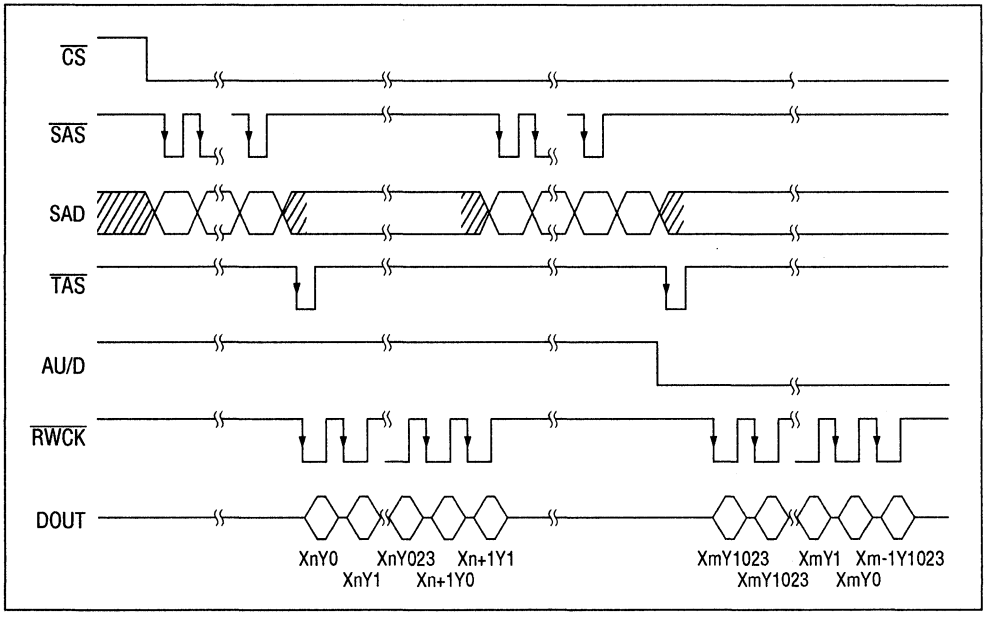
(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Refresh cycle	t_{REF}	—	—	ms
Read/write cycle time	t_{RWC}	4,000	—	ns
Access time	t_{ACC}	—	3,000	ns
Output turn off delay time	t_{OFF}	0	50	ns
Input signal rise/fall time	t_T	3	50	ns
$\overline{RWCK}$ precharge time	t_{RWP}	1,000	—	ns
$\overline{RWCK}$ pulse width	t_{RW}	3,000	10,000	ns
$\overline{SAS}$ cycle time	t_{SSC}	100	—	ns
$\overline{SAS}$ pulse width	t_{SAS}	50	—	ns
$\overline{SAS}$ precharge time	t_{SAP}	50	—	ns
Address setup time	t_{AS}	0	—	ns
Address hold time	t_{AH}	50	—	ns
$\overline{TAS}$ setup time	t_{ATS}	50	—	ns
$\overline{TAS}$ to $\overline{RWCK}$ setup time	t_{TRS}	50	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	50	—	ns
Read command setup time	t_{RRS}	0	—	ns
Read command hold time	t_{RRH}	50	—	ns
Write command setup time	t_{WRS}	0	—	ns
Write command hold time	t_{WRH}	50	—	ns
Write command pulse width	t_{WP}	50	—	ns
Write command to $\overline{RWCK}$ lead time	t_{RWL}	50	—	ns
Data setup time	t_{DS}	0	—	ns
Data hold time	t_{DH}	50	—	ns
$\overline{RWCK}$ to $\overline{WE}$ delay time	t_{RWD}	50	—	ns
AU/D setup time	t_{UDS}	0	—	ns
AU/D hold time	t_{UDH}	50	—	ns
AU/D to $\overline{TAS}$ setup time	t_{UDTS}	0	—	ns

Read/Write/Read Modify Write Cycle



Address Up/Down Select Mode



Note: A0 to A8 are enable and A9 is stable in the 10 bit (A0 ~ A9).

PIN FUNCTIONS AND OPERATION MODES

Pin	Function
SAD	(Serial Address Input) Pin for inputting the read/write starting address-Designation in units of 1024 words is possible. The 1,024 address data can be input as 10-bit (A0-A9) serial from the SAD pin.(A0-A8 has enable address, A9 keep "L".)
$\overline{SAS}$	(Serial address strode) Pin for the clock used to store the serial address data into the internal register.
$\overline{TAS}$	(Address transfer strode) Input pin for setting the serial address data stored in the address register to the internal address counter. When the $\overline{TAS}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.
$\overline{RWCK}$	(Read/write clock) Input pin for the data register information read/write clock. Internal operation starts at the following edges of $\overline{RWCK}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{RWCK}$ falls.
$\overline{WE}$	(Write enable) Input pin for selecting the read mode, write mode or read modify write mode. The read mode is set when $\overline{WE}$ is "H", and the write mode is set when $\overline{WE}$ is "L". When $\overline{WE}$ falls from "H" to "L" while $\overline{RWCK}$ is active, the read modify write mode is set.
DIN	(Data input) Input pin for write data. The information at the data input pin is stored at the falling edge of $\overline{RWCK}$ in the write mode, and at the falling edge of $\overline{WE}$ in the read modify write mode.
DOUT	(Data output) The data output pin is always in kept in the high impedance state when $\overline{RWCK}$ or $\overline{CS}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{RWCK}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.
AU/D	(Address up/down select) Input pin for selecting the direction of automatic address updating. When the $\overline{TAS}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{RWCK}$ is input. When the $\overline{TAS}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y. Then the address is decremented by 1 every time $\overline{RWCK}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS}, t_{UDH} are satisfied.
$\overline{CS}$	(Chip select) Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM6587s by connecting the data input and output pins.

OKI Semiconductor

MSM6586

262,144-WORD x 1-BIT SERIAL REGISTER

GENERAL DESCRIPTION

MSM6586 is a serial register in 262.144 words x 1 bit configuration featuring medium speed operation with low power consumption.

MSM6586 has a built-in intermal address generator circuit allowing continuous serial read/write operation by externalclock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power consumption.

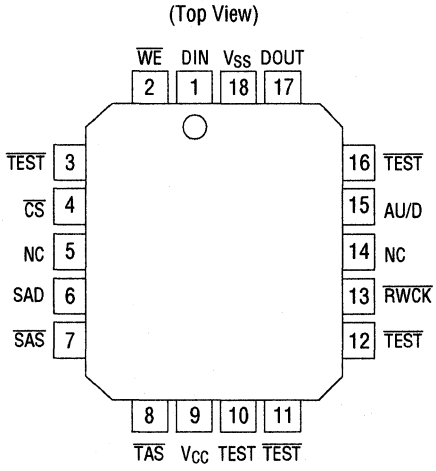
18-pin plastic QFJ (PLCC) is used as the package and the operating temperature range is between 0°C and 70°C.

MSM6586 is suitable fot storing large capacity data with battery backup. A solid state recording and playback system can easily be built-in combination woth OKI's voice synthesizer LSIs, MSM6388 and MSM6588.

FEATURES

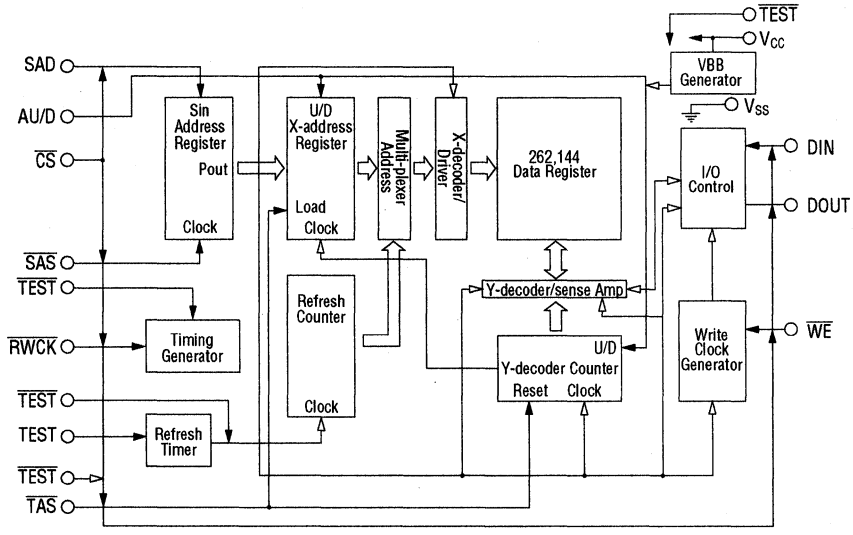
- Configuration: 262,144 x 1 bit
- Serial access operation:
  - Serial access time 3.0μs
  - Serial read/write cycle time 4.0μs
- Low current consumption:
  - 100μA max. (for data holding, V_{CC} = 4.0V)
- Wide operating supply voltage range:
  - Single 3.5 to 5.5V
- Refresh operation:
  - Self-refresh (refresh-free)
- 18-pin Plastic QFJ (PLCC)
  - (QFJ18-P-R290)

PIN CONFIGURATION



1 : Data input
2 : Write enable
3 : Test input
4 : Chip select
5 : No connection
6 : Serial address data
7 : Serial address strobe
8 : Transfer address strobe
9 : Power supply (+5V)
10 : Test input
11 : Test input
12 : Test input
13 : Read/write clock
14 : No connection
15 : Address up/down select
16 : Test input
17 : Data output
18 : Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTIC

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Terminal voltage	V_T	T_a = 25°C, relative to V_{SS}	−1.0 ~ +7.0	V
Output short-circuit current	I_{OS}	T_a = 25°C	50	mA
Power dissipation	P_D	T_a = 25°C	1	W
Operating temperature	T_{Op}	—	0 ~ +70	°C
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Recommended Operating Conditions

(Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Terminal voltage	V_{CC}	3.5	5.0	5.5	V
Terminal voltage	V_{SS}	0	0	0	V
"H" input voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" input voltage	V_{IL}	−0.5	0	0.5	V

DC Characteristics

(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

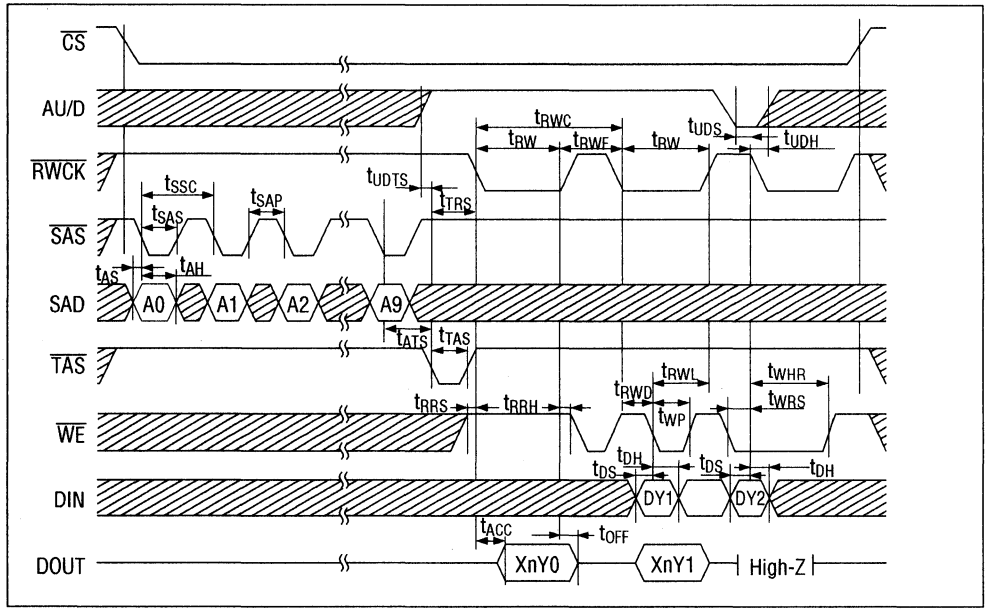
Parameter	Symbol	Conditions	Min.	Max.	Unit
"H" output voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input leakage current	I_{LI}	V_I = 0V ~ V_{CC}	−1	1	µA
Output leakage current	I_{LO}	V_O = 0V ~ V_{CC}	−1	1	µA
Supply current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4µs	—	5	mA
Supply currnet (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA

• AC Characteristics

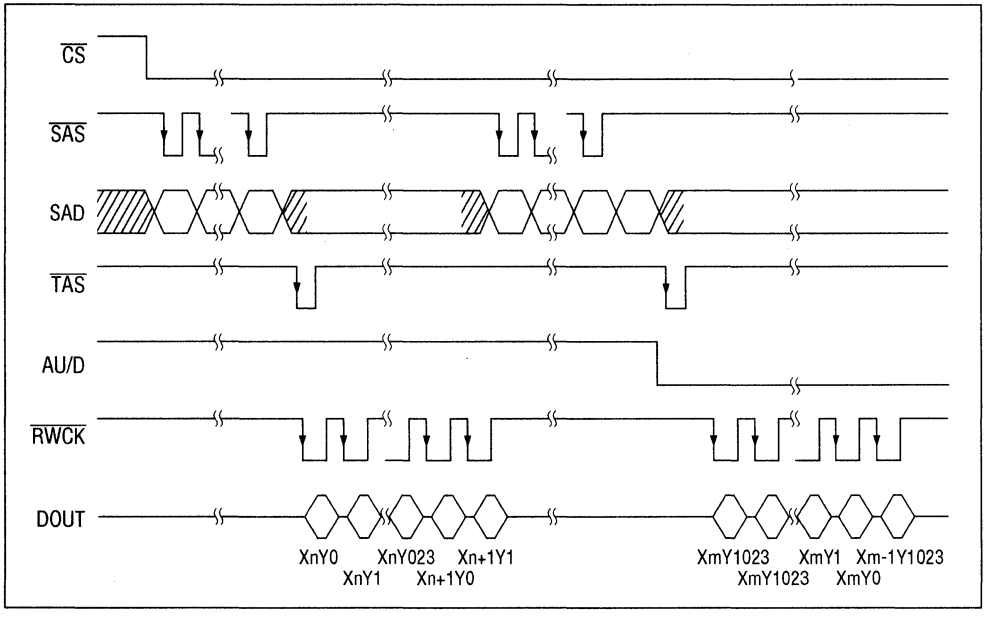
(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Refresh cycle	t_{REF}	—	—	ms
Read/write cycle time	t_{RWC}	4,000	—	ns
Access time	t_{ACC}	—	3,000	ns
Output turn off delay time	t_{OFF}	0	50	ns
Input signal rise/fall time	t_T	3	50	ns
$\overline{RWCK}$ precharge time	t_{RWP}	1,000	—	ns
$\overline{RWCK}$ pulse width	t_{RW}	3,000	10,000	ns
$\overline{SAS}$ cycle time	t_{SSC}	100	—	ns
$\overline{SAS}$ pulse width	t_{SAS}	50	—	ns
$\overline{SAS}$ precharge time	t_{SAP}	50	—	ns
Address setup time	t_{AS}	0	—	ns
Address hold time	t_{AH}	50	—	ns
$\overline{TAS}$ setup time	t_{ATS}	50	—	ns
$\overline{TAS}$ to $\overline{RWCK}$ setup time	t_{TRS}	50	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	50	—	ns
Read command setup time	t_{RRS}	0	—	ns
Read command hold time	t_{RRH}	50	—	ns
Write command setup time	t_{WRS}	0	—	ns
Write command hold time	t_{WRH}	50	—	ns
Write command pulse width	t_{WP}	50	—	ns
Write command to $\overline{RWCK}$ lead time	t_{RWL}	50	—	ns
Data setup time	t_{DS}	0	—	ns
Data hold time	t_{DH}	50	—	ns
$\overline{RWCK}$ to $\overline{WE}$ delay time	t_{RWD}	50	—	ns
AU/D setup time	t_{UDS}	0	—	ns
AU/D hold time	t_{UDH}	50	—	ns
AU/D to $\overline{TAS}$ setup time	t_{UDTS}	0	—	ns

Read/Write/Read Modify Write Cycle



Address Up/Down Select Mode



Note: A0 to A7 are enable and A8, A9 is stable in the 10 bit (A0 ~ A9).

PIN FUNCTIONS AND OPERATION MODES

Pin	Function
SAD	(Serial Address Input) Pin for inputting the read/write starting address-Designation in units of 1024 words is possible. The 1,024 address data can be input as 10-bit (A0-A9) serial from the SAD pin.(A0-A7 has enable address, A8 and A9 keep "L".)
$\overline{SAS}$	(Serial address strode) Pin for the clock used to store the serial address data into the internal register.
$\overline{TAS}$	(Address transfer strode) Input pin for setting the serial address data stored in the address register to the internal address counter. When the $\overline{TAS}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.
$\overline{RWCK}$	(Read/write clock) Input pin for the data register information read/write clock. Internal operation starts at the following edges of $\overline{RWCK}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{RWCK}$ falls.
$\overline{WE}$	(Write enable) Input pin for selecting the read mode, write mode or read modify write mode. The read mode is set when $\overline{WE}$ is "H", and the write mode is set when $\overline{WE}$ is "L". When $\overline{WE}$ falls from "H" to "L" while $\overline{RWCK}$ is active, the read modify write mode is set.
DIN	(Data input) Input pin for write data. The information at the data input pin is stored at the falling edge of $\overline{RWCK}$ in the write mode, and at the falling edge of $\overline{WE}$ in the read modify write mode.
DOUT	(Data output) The data output pin is always in kept in the high impedance state when $\overline{RWCK}$ or $\overline{CS}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{RWCK}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.
AU/D	(Address up/down select) Input pin for selecting the direction of automatic address updating. When the $\overline{TAS}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{RWCK}$ is input. When the $\overline{TAS}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y. Then the address is decremented by 1 every time $\overline{RWCK}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS}, t_{UDH} are satisfied.
$\overline{CS}$	(Chip select) Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM6586s by connecting the data input and output pins.

OKI Semiconductor

MSM6595-XXX

1M-bit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6595 is a Serial Voice ROM of a 1,048,576-word × 1-bit for the voice system. The MSM6595 enables to continue the serial read operation due to the input of one external clock for the built-in internal address generating circuit.

The internal address is automatically made to +1 with the read operation and the address can designate 1024-word to X direction and 1024-word to Y direction by inputting the external serial address.

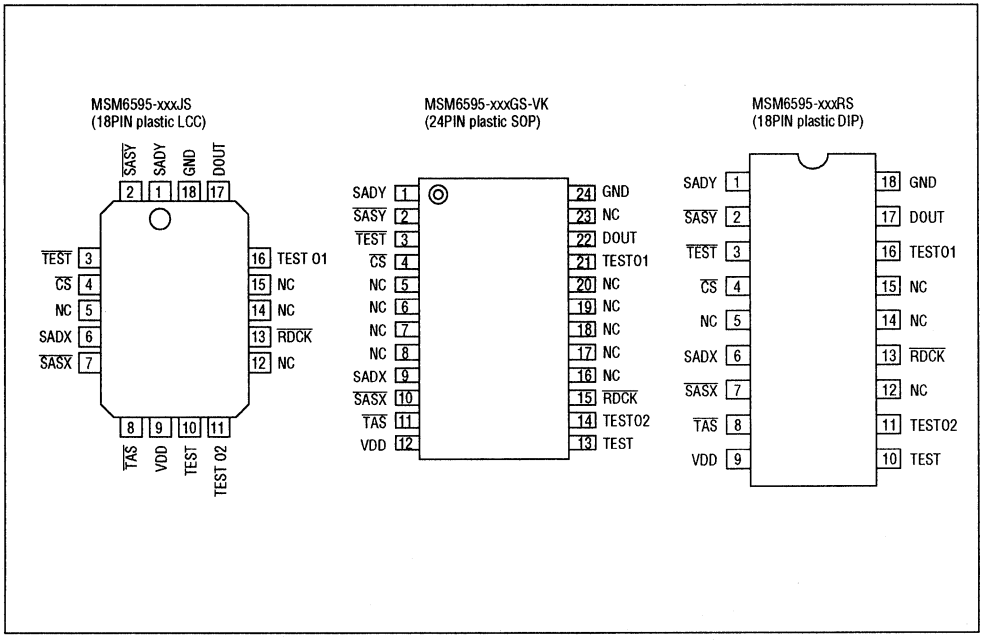
The combination of the Serial Voice ROM (MSM6595), the Solid State recorder (MSM6388, MSM6588) and Serial Voice Register (MSM6389, MSM6587, MSM6586) can easily make up the record and playback system with the fixed message which is stored in the Serial Voice ROM.

Note: MSM6388 or MSM6588 can not control only MSM6595-XXX without the Serial Voice Register.

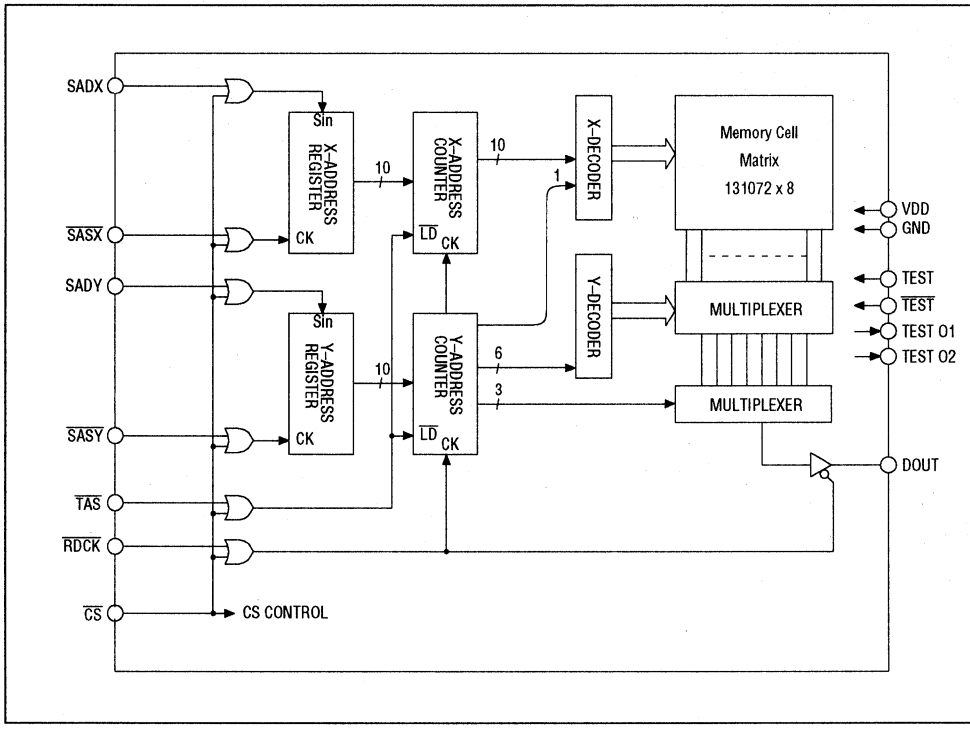
FEATURES

- Configuration:
  1,048,576-word × 1-bit
- Serial access:
  Serial read cycle time: 2.5μs
- Power supply: 5V single voltage
- Package: 18-pin plastic LCC
  (QFJ 18-P-R290)
  24-pin plastic SOP
  (SOP 24-P-430-VK)
  18-pin plastic DIP
  (DIP 18-P-300-W1)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICLAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD+0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Conditions

Parameter	Symbol	Conditions	Range	Unit
Power supply voltage	VDD	GND = 0V	+3.5 ~ +5.5	V
Operating temperature	T_{op}	—	−40 ~ +85	°C

• DC Characteristics

(VDD = 3.5~5.5V, Ta= −40 ~ +85°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
"H" level input voltage	V_{IH}	—	0.8×VDD	—	—	V
"L" level input voltage	V_{IL}	—	—	—	0.8	V
"H" level output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" level input current	I_{IH}	V_{IH} = VDD	—	—	10	μA
"L" level input current	I_{IL}	V_{IL} = GND	−10	—	—	μA
Operating consumption current (1)	I_{DD}	t_{RDC} =2.5μs	—	—	15	mA
Operating consumption current (2)	I_{DS}	$\overline{CS}$ = VDD- 0.2V	—	—	10	μA

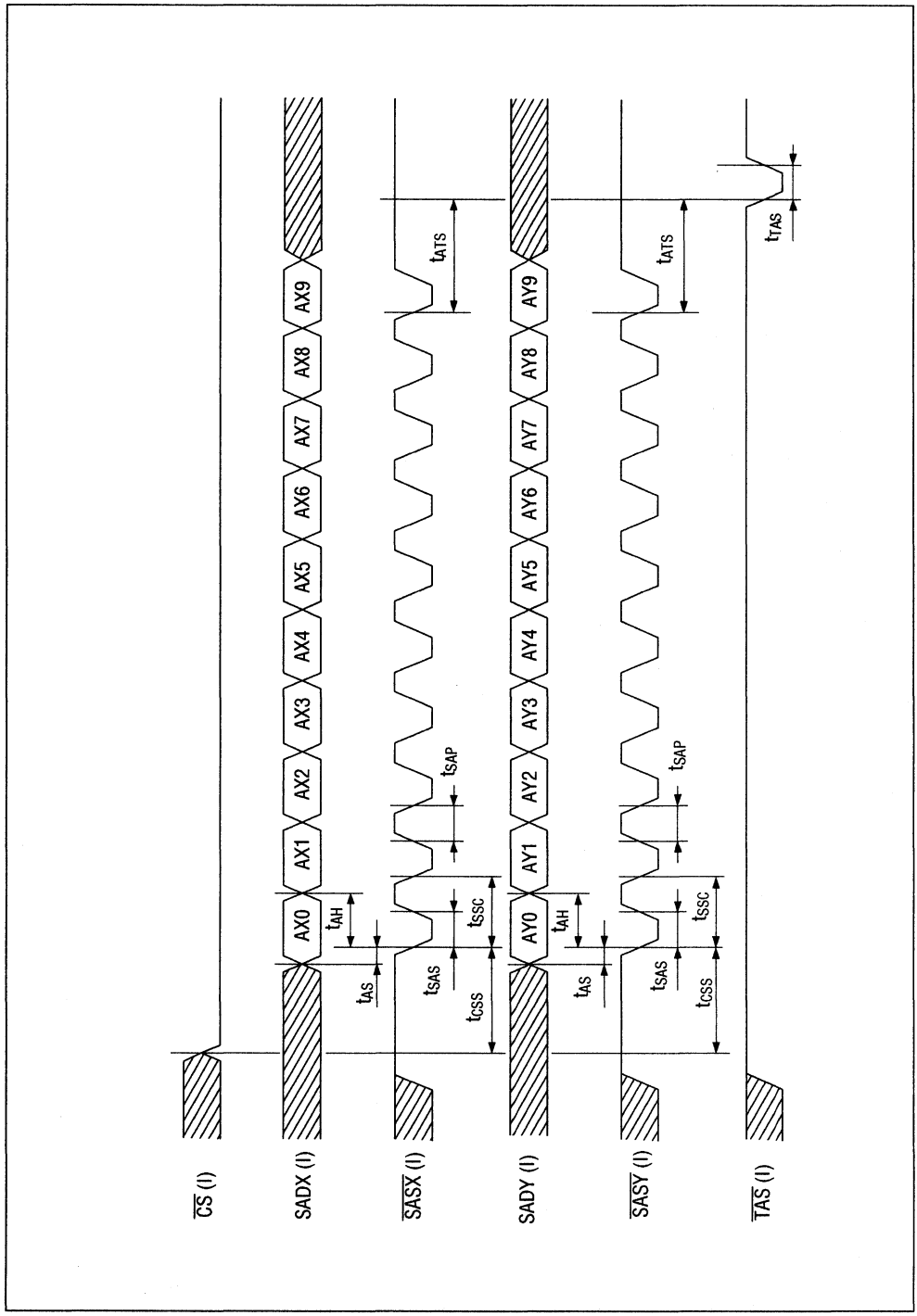
• AC Characteristics

(VDD= 3.5 ~ 5.5V, Ta= −40 ~ +85°C)

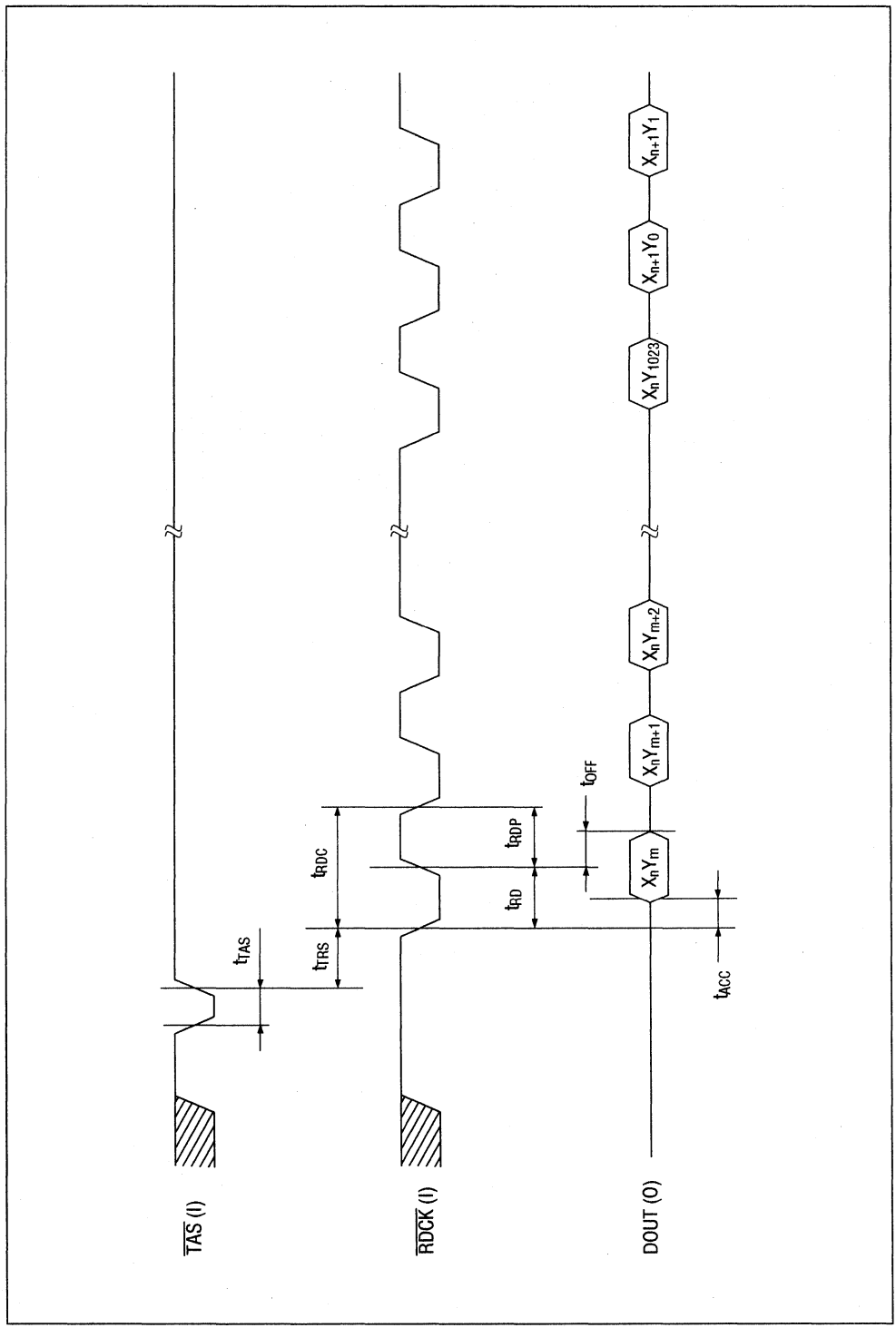
Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
$\overline{CS}$ • $\overline{SAS}$ set-up time	t_{CSS}	—	1000	—	ns
$\overline{SASX}$, $\overline{SASY}$ cycle time	t_{SSC}	—	500	—	ns
$\overline{SASX}$, $\overline{SASY}$ precharge time	t_{SAP}	—	250	—	ns
$\overline{SASX}$, $\overline{SASY}$ pulse width	t_{SAS}	—	250	—	ns
Address set-up time	t_{AS}	—	100	—	ns
Address hold time	t_{AH}	—	100	—	ns
$\overline{TAS}$ set-up time	t_{ATS}	—	500	—	ns
$\overline{TAS}$ • $\overline{RDCK}$ set-up time	t_{TRS}	—	500	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	—	250	—	ns
Read cycle time	t_{RDC}	—	2500	—	ns
Access time	t_{ACC}	—	—	1500	ns
Output turn off delay time	t_{OFF}	—	0	200	ns
$\overline{RDCK}$ precharge time	t_{RDP}	—	1000	—	ns
$\overline{RDCK}$ pulse width	t_{RD}	—	1500	—	ns

TIME CHART

- **Timing for Serial Address Input**



- **Read Access Timing**

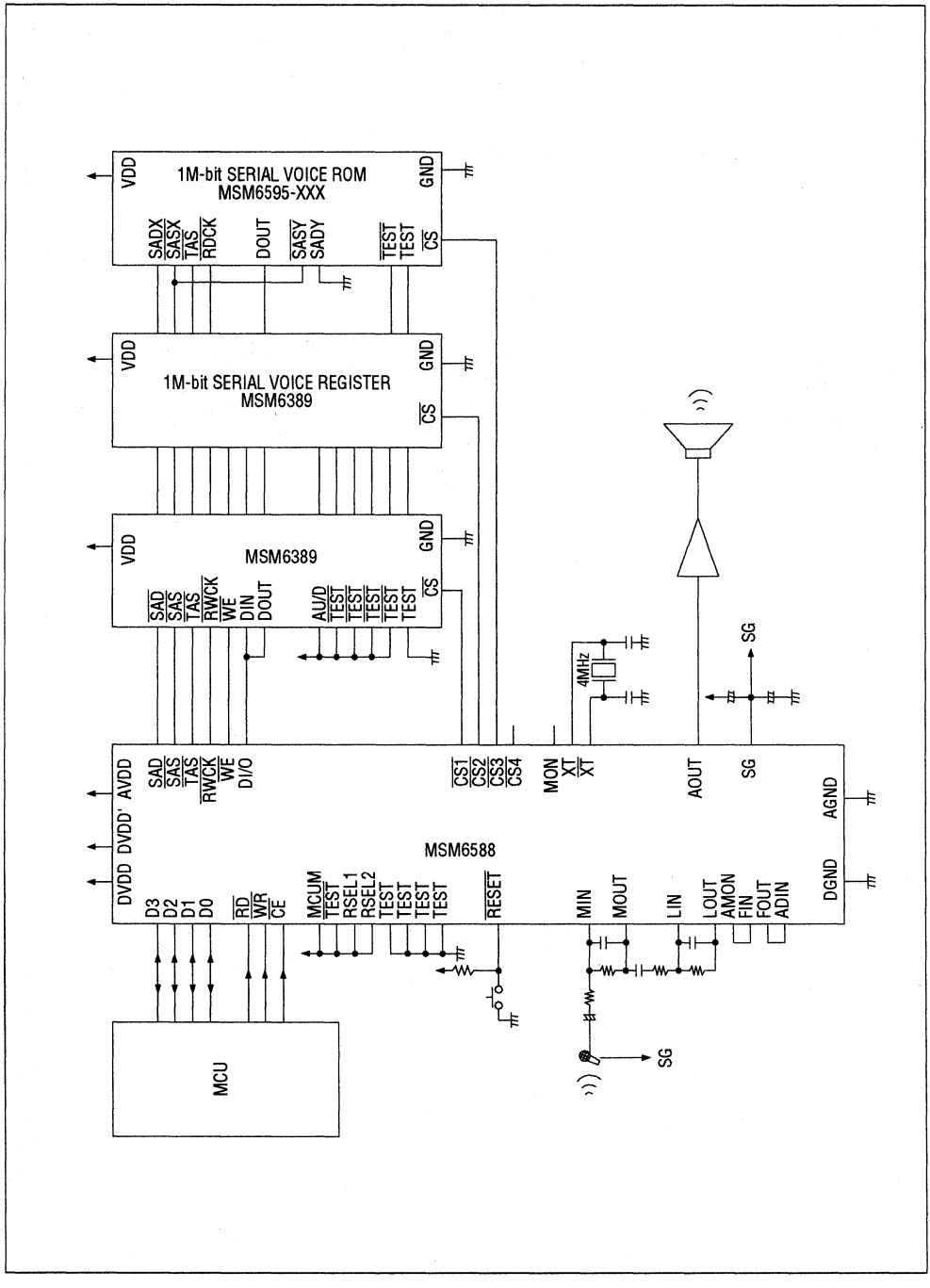


TERMINAL FUNCTION EXPLANATION

Terminal	I/O	Function
VDD	—	Power supply terminal.
GND	—	Ground terminal.
SADX	I	(SERIAL ADDRESS) This is a terminal for inputting the head X address of read. This terminal can designate 1024-word and can input 1024 address data as serial data of 10-bit (AX0~AX9).
SADY	I	(SERIAL ADDRESS) This is a terminal for inputting the head Y address of read. This terminal can designate 1024-word and can input 1024 address data as serial data of 10-bit (AY0~AY9).
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is a clock input terminal to take in serial address data of X address to the internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is a clock input terminal to take in serial address data of Y address to the internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) This is an input terminal to set serial address data to be taken in the address register to the internal address counter. X address and Y address are taken in by fall of $\overline{TAS}$ terminal.
$\overline{RDCK}$	I	(READ CLOCK) This clock terminal to read out information of the data register. Internal operation starts by fall edge of $\overline{RDCK}$ and information of the data register is outputted from DOUT terminal. In addition, the terminal address counter is automatically increased by fall of $\overline{RDCK}$.
DOUT	O	(DATA OUT) As far as $\overline{CS}$ or $\overline{RDCK}$ of data terminals are held to "H", terminal always keeps high impedance state. If information of "H" or "L" is read out during read, the output terminal is set to "H" or "L" and information read out is kept until $\overline{RDCK}$ is restored to "H".
$\overline{CS}$	I	(CHIP SELECT) All input terminals enable to make disable by making "H" with $\overline{CS}$. This terminal can be used in parallel by connecting data output terminals of plural serial Mask ROM's.
TEST $\overline{TEST}$	I	This is a terminal for LSI test. Input "L" level to TEST terminal and "H" level to $\overline{TEST}$ terminal.
TESTO1 TESTO2	O	This is a terminal for LSI test. Open this terminal.

APPLICATION CIRCUIT

- **Application Circuit for MSM6588**



Note: MSM6588 cannot control only MSM6595-XXX without Serial Voice Register.

OKI Semiconductor

MSM6596-XXX

2M-bit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6596 is a Serial Voice ROM of a 1,048,576-word × 1-bit × 2-bank for voice systems. The MSM6596 enables the continuing of the serial read operation with the input of a single external clock for the built-in internal address generating circuit.

The internal address is automatically incremented to +1 with the read operation and the address can designate 1024-word to X direction and 1024-word to Y direction by inputting the external serial address. The bank is switched by $\overline{CS1}$, $\overline{CS2}$.

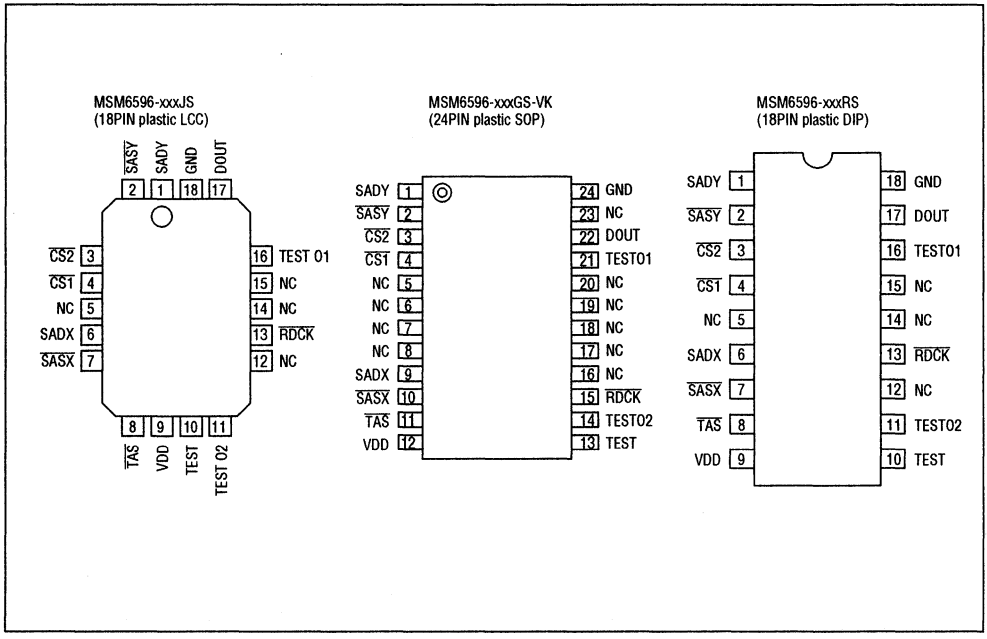
The combination of the Serial Voice ROM (MSM6596), the Solid State recorder (MSM6388, MSM6588) and Serial Voice Register (MSM6389, MSM6587, MSM6586) can easily provide a record and playback system with a fixed message which is stored in the Serial Voice ROM.

Note: MSM6388 or MSM6588 can not control only MSM6596-XXX without the addition of a Serial Voice Register.

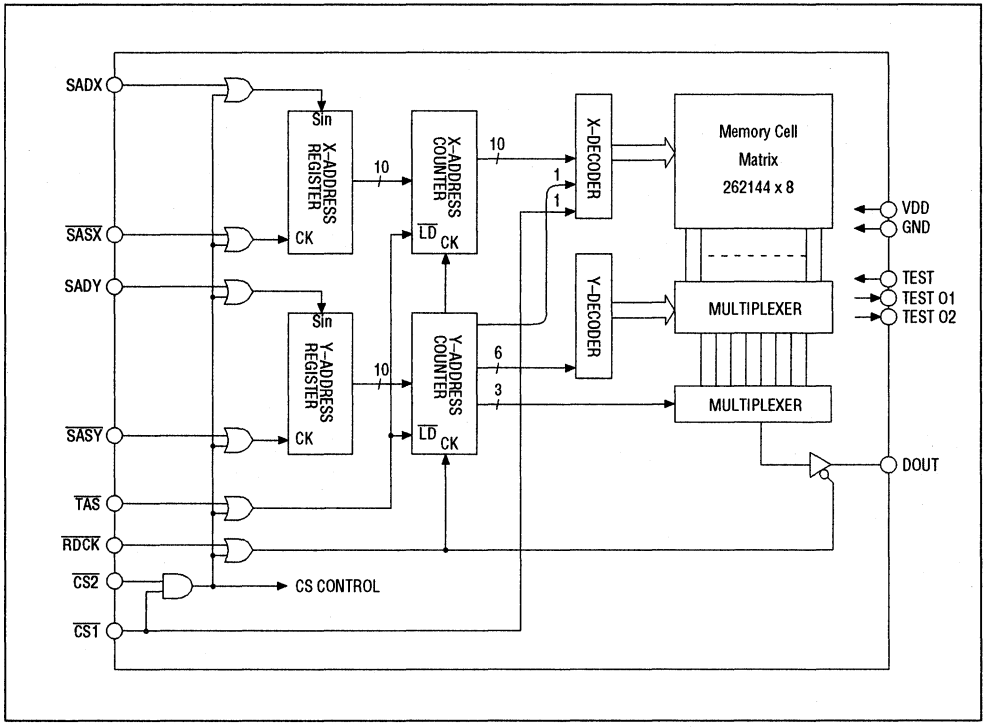
FEATURES

- Configuration:
  1,048,576-word × 1-bit × 2-bank
- Serial access:
  Serial read cycle time: 2.5μs
- Power supply: 5V single voltage
- Package: 18-pin plastic LCC
  (QFJ 18-P-R290)
  24-pin plastic SOP
  (SOP 24-P-430-VK)
  18-pin plastic DIP
  (DIP 18-P-300-W1)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Conditions

Parameter	Symbol	Conditions	Range	Unit
Power supply voltage	VDD	GND = 0V	+3.5 ~ +5.5	V
Operating temperature	T_{op}	—	−40 ~ +85	°C

• DC Characteristics

(VDD = 3.5~5.5V, Ta= −40 ~ +85°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
"H" level input voltage	V_{IH}	—	0.8×VDD	—	—	V
"L" level input voltage	V_{IL}	—	—	—	0.8	V
"H" level output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
"H" level input current	I_{IH}	V_{IH} = VDD	—	—	10	μA
"L" level input current	I_{IL}	V_{IL} = GND	−10	—	—	μA
Operating consumption current (1)	I_{DD}	t_{RDC} =2.5μs	—	—	15	mA
Operating consumption current (2)	I_{DS}	$\overline{CS1}$ = $\overline{CS2}$ = VDD - 0.2V	—	—	10	μA

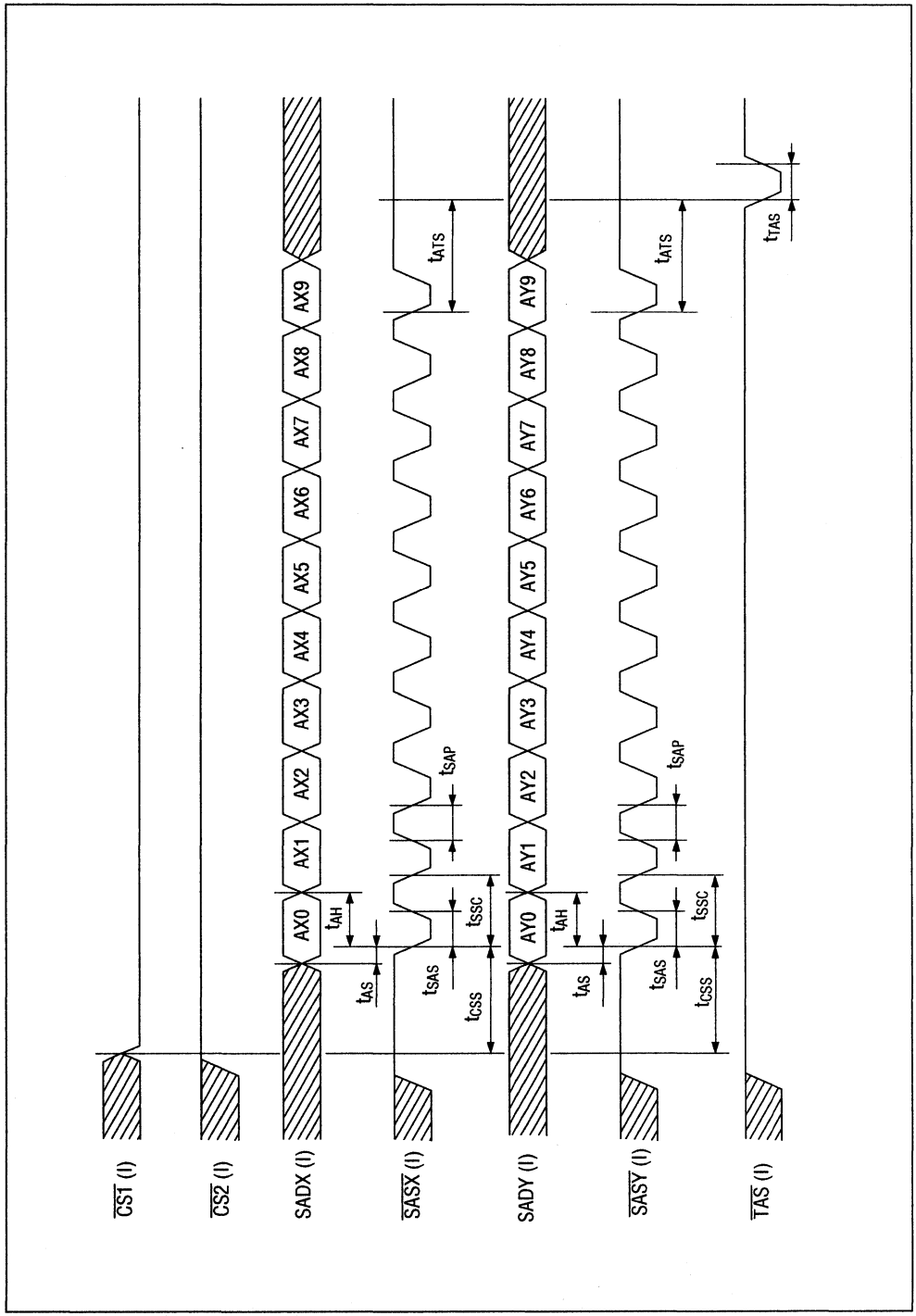
• AC Characteristics

(VDD = 3.5 ~ 5.5V, Ta= −40 ~ +85°C)

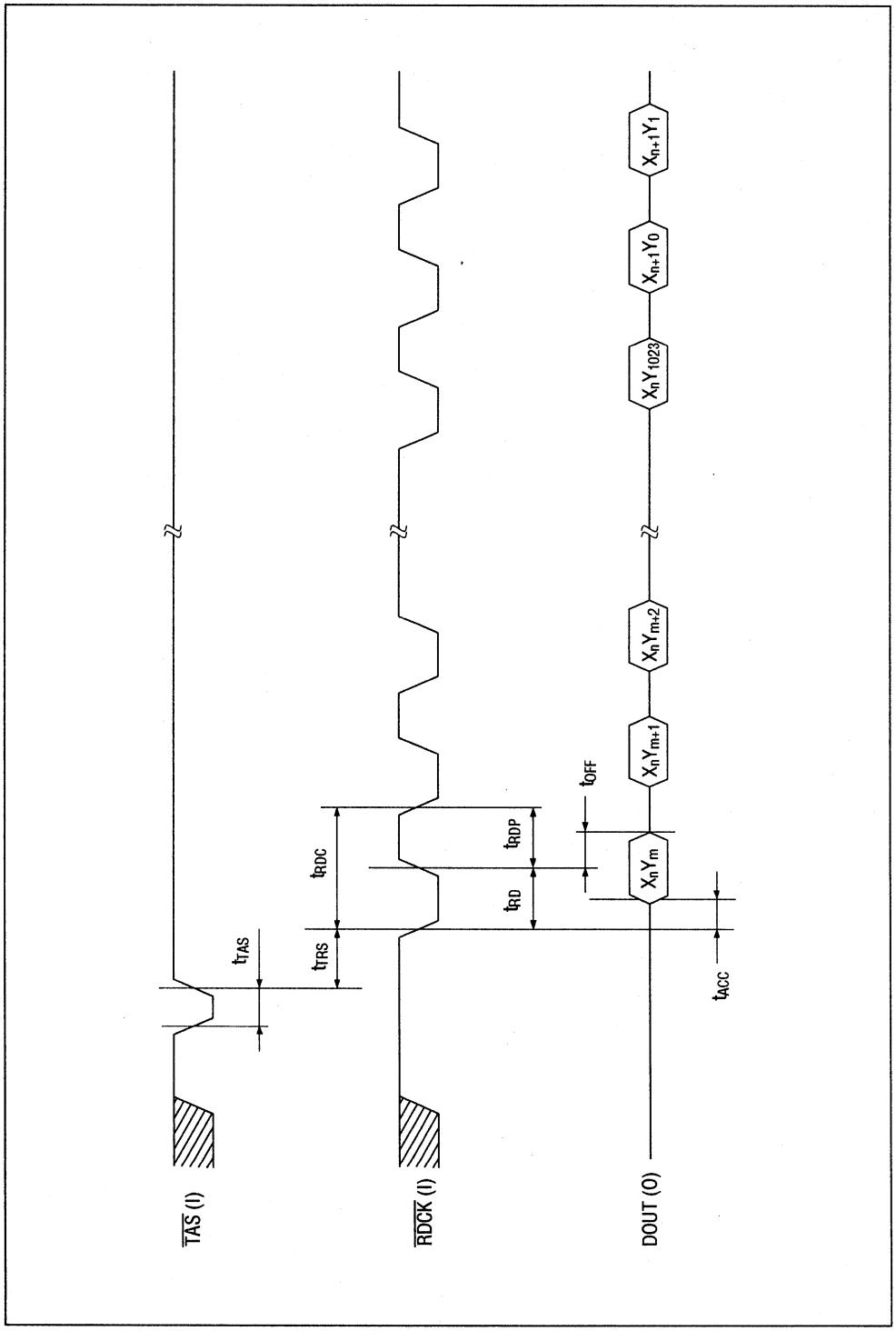
Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
$\overline{CS}$ • $\overline{SAS}$ set-up time	t_{CSS}	—	1000	—	ns
$\overline{SASX}$, $\overline{SASY}$ cycle time	t_{SSC}	—	500	—	ns
$\overline{SASX}$, $\overline{SASY}$ precharge time	t_{SAP}	—	250	—	ns
$\overline{SASX}$, $\overline{SASY}$ pulse width	t_{SAS}	—	250	—	ns
Address set-up time	t_{AS}	—	100	—	ns
Address hold time	t_{AH}	—	100	—	ns
$\overline{TAS}$ set-up time	t_{ATS}	—	500	—	ns
$\overline{TAS}$ • $\overline{RDCK}$ set-up time	t_{TRS}	—	500	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	—	250	—	ns
Read cycle time	t_{RDC}	—	2500	—	ns
Access time	t_{ACC}	—	—	1500	ns
Output turn off delay time	t_{OFF}	—	0	200	ns
$\overline{RDCK}$ precharge time	t_{RDP}	—	1000	—	ns
$\overline{RDCK}$ pulse width	t_{RD}	—	1500	—	ns

TIME CHART

- **Timing for Serial Address Input**



- **Read Access Timing**

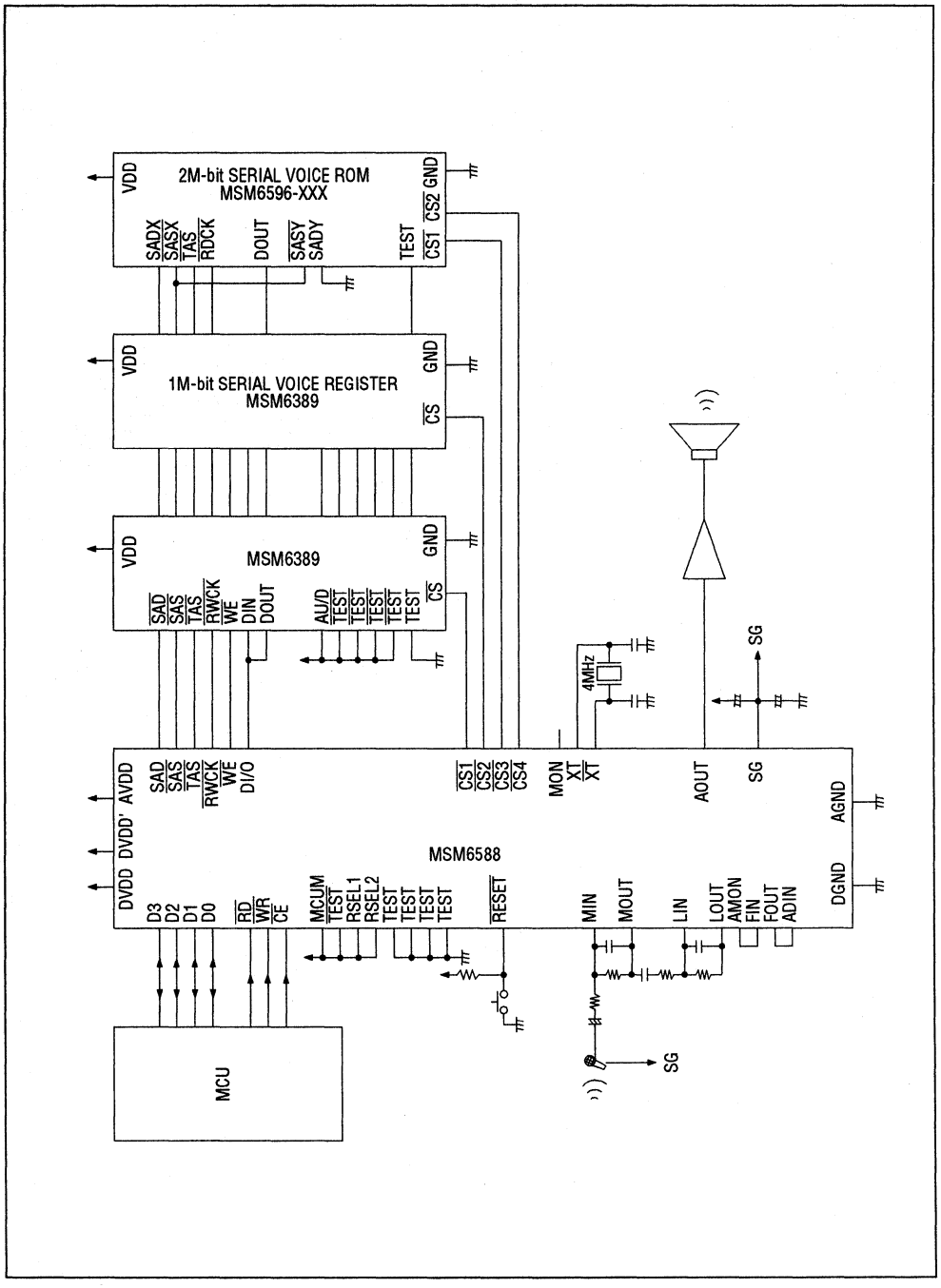


PIN FUNCTION EXPLANATION

Terminal	I/O	Function
VDD	–	Power supply pin.
GND	–	Ground pin.
SADX	I	(SERIAL ADDRESS) This is pin for input of X address header of read. This pin can designate 1024 words and can input 1024 address data as serial data of 10-bit (AX0~AX9).
SADY	I	(SERIAL ADDRESS) This is pin for input of Y address header of read. This pin can designate 1024 words and can input 1024 address data as serial data of 10 bits (AY0~AY9).
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is clock input pin for input of serial address data of X address to internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is clock input pin for input of serial address data of Y address to internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) This is input pin to set serial address data to be taken in address register to internal address counter. X address and Y address are taken in by fall of $\overline{TAS}$ pin .
$\overline{RDCK}$	I	(READ CLOCK) This clock pin to read out information of data register. Internal operation starts with the falling edge of $\overline{RDCK}$ and the information of the data register is output from DOUT pin. In addition, pin address counter is automatically incremented by the fall of $\overline{RDCK}$.
DOUT	O	(DATA OUT) If both $\overline{CS1}$ and $\overline{CS2}$ or $\overline{RDCK}$ are held to "H", DOUT remains in the high impedance state. If information of "H" or "L" is read out during read, DOUT pin is set to "H" or "L" and information read out is held until $\overline{RDCK}$ is restored to "H".
$\overline{CS1}$ $\overline{CS2}$	I	(CHIP SELECT) When $\overline{CS1}$ goes "L", bank 1 is selected and when $\overline{CS2}$ goes "L", bank 2 is selected. In addition, all input pins are disabled when both $\overline{CS1}$ and $\overline{CS2}$ go "H". This pin can be used in parallel by connecting data output pins of multiple serial Mask ROM's.
TEST	I	This is pin for LSI test. Input "L" level.
TEST01 TEST02	O	This is pin for LSI test. Open this pin .

APPLICATION CIRCUIT

- **Application Circuit for MSM6588**



Note: MSM6588 cannot control the MSM6596-XXX without a Serial Voice Register.

GENERAL-PURPOSE CODE FOR MSM6596

The Serial Voice ROM is available for a custom order depending on the user's request. Standard LSIs for general purpose are also available.

The specifications for the standard LSIs are as follows:

Product Name	Application	Contents
MSM6596-600	Japanese time stamp for answering machine, English and Japanese demonstration.	Japanese/English, female
MSM6596-629	Japanese time stamp and English time stamp for answering machine, greetings of 8 languages, and the another demonstration.	Japanese/English, female

MSM6596-600 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words		M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	fs (kHz)	Playback Time
No. 1	01	午前		0	10	5D	6.4	0.67 sec
No. 2	02	午後		11	1F	31	6.4	0.58 sec
No. 3	03	メモ		20	2B	27	6.4	0.45 sec
No. 4	04	れい	(時)	2C	37	27	6.4	0.45 sec
No. 5	05	いち	(時)	38	42	74	6.4	0.44 sec
No. 6	06	に	(時)	43	4A	33	6.4	0.30 sec
No. 7	07	さん	(時)	4B	55	0F	6.4	0.40 sec
No. 8	08	よ	(時)	56	5D	01	6.4	0.28 sec
No. 9	09	ご	(時)	5E	64	4F	6.4	0.26 sec
No.10	0A	ろく	(時)	65	6F	43	6.4	0.42 sec
No.11	0B	なな	(時)	70	7A	39	6.4	0.42 sec
No.12	0C	はち	(時)	7B	86	27	6.4	0.45 sec
No.13	0D	く	(時)	87	8D	1D	6.4	0.25 sec
No.14	0E	じゅう	(時)	8E	98	57	6.4	0.43 sec
No.15	0F	じゅういち	(時)	99	AD	25	6.4	0.81 sec
No.16	10	じゅうに	(時)	AE	BD	15	6.4	0.61 sec
No.17	11	時		BE	C2	5F	6.4	0.19 sec
No.18	12	じゅう		C3	CE	21	6.4	0.45 sec
No.19	13	にじゅう		CF	DD	0D	6.4	0.56 sec
No.20	14	さんじゅう		DE	EE	27	6.4	0.65 sec
No.21	15	よんじゅう		EF	FF	7B	6.4	0.68 sec
No.22	16	ごじゅう		100	10D	1F	6.4	0.53 sec
No.23	17	いっ	(分)	10E	117	5F	6.4	0.39 sec
No.24	18	さん	(分)	118	121	69	6.4	0.39 sec
No.25	19	よん	(分)	122	12B	23	6.4	0.37 sec
No.26	1A	ご	(分)	12C	133	79	6.4	0.32 sec
No.27	1B	ろっ	(分)	134	13D	13	6.4	0.37 sec
No.28	1C	なな	(分)	13E	148	3B	6.4	0.42 sec
No.29	1D	はっ	(分)	149	152	2D	6.4	0.37 sec
No.30	1E	きゅう	(分)	153	15B	07	6.4	0.32 sec
No.31	1F	じゅっ	(分)	15C	166	6F	6.4	0.44 sec
No.32	20	にじゅっ	(分)	167	175	19	6.4	0.57 sec
No.33	21	さんじゅっ	(分)	176	186	77	6.4	0.68 sec
No.34	22	よんじゅっ	(分)	187	198	37	6.4	0.70 sec
No.35	23	ごじゅっ	(分)	199	1A6	53	6.4	0.55 sec

MSM6596-600 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words	M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	fs (kHz)	Playback Time
No. 36	24	ぜろ	1A7	1B1	11	6.4	0.41 sec
No. 37	25	ふん	1B2	1BA	33	6.4	0.34 sec
No. 38	26	ぷん	1BB	1C3	4D	6.4	0.34 sec
No. 39	27	件	1C4	1CD	31	6.4	0.38 sec
No. 40	28	です	1CE	1D2	37	6.4	0.18 sec
No. 41	29	メッセージ+音楽(日本語)	1D3	216	5F	4.0	4.34 sec
No. 42	2A	メッセージ+音楽(日本語)	217	277	35	5.3	4.66 sec
No. 43	2B	メッセージ+音楽(日本語)	278	2EE	47	6.4	4.74 sec
No. 44	2C	メッセージ+音楽(日本語)	2EF	377	47	8.0	4.37 sec
No. 45	2D	メッセージ+牛の声(日本語)	378	3B0	13	4.0	3.59 sec
No. 46	2E	メッセージ+牛の声(日本語)	3B1	405	19	5.3	4.07 sec
No. 47	2F	メッセージ+牛の声(日本語)	406	464	6D	6.4	3.79 sec
No. 48	30	メッセージ+牛の声(日本語)	465	4D0	6F	8.0	3.45 sec
No. 49	31	Message+Music (English)	4D1	510	49	4.0	4.07 sec
No. 50	32	Message+Music (English)	511	571	5D	5.3	4.67 sec
No. 51	33	Message+Music (English)	572	5E8	15	6.4	4.73 sec
No. 52	34	Message+Music (English)	5E9	663	5B	8.0	3.93 sec
No. 53	35	Message+Cattle Voice (English)	664	6A5	11	4.0	4.17 sec
No. 54	36	Message+Cattle Voice (English)	6A6	707	7D	5.3	4.73 sec
No. 55	37	Message+Cattle Voice (English)	708	77A	45	6.4	4.58 sec
No. 56	38	Message+Cattle Voice (English)	77B	7F3	25	8.0	3.85 sec

(Total playback time: 85.56 sec)

MSM6596-629 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words	M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	length	fs (kHz)	Playback Time
No. 1	01	ALRAM	0	B	71	4bit	6.4	0.48 sec
No. 2	02	SETTING	C	16	4B	4bit	6.4	0.42 sec
No. 3	03	ON	17	1E	55	4bit	6.4	0.31 sec
No. 4	04	OFF	1F	25	67	4bit	6.4	0.27 sec
No. 5	05	HOUR	26	2E	67	4bit	6.4	0.35 sec
No. 6	06	MINUTE	2F	37	35	4bit	6.4	0.34 sec
No. 7	07	SECOND	38	41	0B	4bit	6.4	0.36 sec
No. 8	08	NINE	42	4D	0D	4bit	6.4	0.44 sec
No. 9	09	TEN	4E	56	31	4bit	6.4	0.34 sec
No. 10	0A	ELEVEN	57	65	37	4bit	6.4	0.58 sec
No. 11	0B	TWELVE	66	70	47	4bit	6.4	0.42 sec
No. 12	0C	ZERO	71	7F	09	4bit	6.4	0.56 sec
No. 13	0D	TWEN –	80	85	33	4bit	6.4	0.22 sec
No. 14	0E	THIR –	86	8A	57	4bit	6.4	0.19 sec
No. 15	0F	FIF –	8B	90	47	4bit	6.4	0.22 sec
No. 16	10	TY – FOUR	91	A2	0D	4bit	6.4	0.68 sec
No. 17	11	TY – FIVE	A3	B6	47	4bit	6.4	0.78 sec
No. 18	12	TY – SIX	B7	C6	5B	4bit	6.4	0.63 sec
No. 19	13	TY – SEVEN	C7	D6	01	4bit	6.4	0.60 sec
No. 20	14	TY – EIGHT	D7	E6	4B	4bit	6.4	0.62 sec
No. 21	15	TY – NINE	E7	F6	6B	4bit	6.4	0.63 sec
No. 22	16	– TY	F7	FD	2B	4bit	6.4	0.25 sec
No. 23	17	– TEEN	FE	106	3D	4bit	6.4	0.34 sec
No. 24	18	ONE	107	110	39	4bit	6.4	0.38 sec
No. 25	19	TWO	111	118	1B	4bit	6.4	0.29 sec
No. 26	1A	THREE	119	121	01	4bit	6.4	0.32 sec
No. 27	1B	FOUR	122	12B	0D	4bit	6.4	0.36 sec
No. 28	1C	FIVE	12C	135	4B	4bit	6.4	0.38 sec
No. 29	1D	SIX	136	140	2D	4bit	6.4	0.41 sec
No. 30	1E	SEVEN	141	14A	51	4bit	6.4	0.39 sec
No. 31	1F	EIGHT	14B	152	2B	4bit	6.4	0.29 sec
No. 32	20	O'CLOCK	153	163	35	4bit	6.4	0.66 sec
No. 33	21	SIX –	164	16B	73	4bit	6.4	0.32 sec
No. 34	22	SEVEN –	16C	176	05	4bit	6.4	0.40 sec
No. 35	23	EIGHT –	177	17D	2B	4bit	6.4	0.25 sec

MSM6596-629 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words	M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	length	fs (kHz)	Playback Time
No. 36	24	NINE –	17E	186	11	4bit	6.4	0.33 sec
No. 37	25	TY – ONE	187	196	0F	4bit	6.4	0.60 sec
No. 38	26	TY – TWO	197	1A6	45	4bit	6.4	0.62 sec
No. 39	27	TY – THREE	1A7	1B7	3B	4bit	6.4	0.66 sec
No. 40	28	OH	1B8	1BF	65	4bit	6.4	0.31 sec
No. 41	29	FOR –	1C0	1C6	31	4bit	6.4	0.26 sec
No. 42	2A	TO GO	1C7	1D4	29	4bit	6.4	0.53 sec
No. 43	2B	IT'S	1D5	1DC	11	4bit	6.4	0.29 sec
No. 44	2C	Silence 50mS	1DD	1DE	1D	4bit	6.4	0.05 sec
No. 45	2D	Silence 200mS	1DF	1E3	7D	4bit	6.4	0.20 sec
No. 46	2E	AM	1E4	1F2	55	4bit	6.4	0.59 sec
No. 47	2F	PM	1F3	201	73	4bit	6.4	0.60 sec
No. 48	30	午前	202	212	5D	4bit	6.4	0.67 sec
No. 49	31	午後	213	221	31	4bit	6.4	0.58 sec
No. 50	32	メモ	222	22D	27	4bit	6.4	0.45 sec
No. 51	33	れい (時)	22E	239	27	4bit	6.4	0.45 sec
No. 52	34	いち (時)	23A	244	74	4bit	6.4	0.44 sec
No. 53	35	に (時、分)	245	24C	33	4bit	6.4	0.30 sec
No. 54	36	さん (時)	24D	257	0F	4bit	6.4	0.40 sec
No. 55	37	よ (時)	258	25F	01	4bit	6.4	0.28 sec
No. 56	38	ご (時)	260	266	4F	4bit	6.4	0.26 sec
No. 57	39	ろく (時)	267	271	43	4bit	6.4	0.42 sec
No. 58	3A	なな (時)	272	27C	39	4bit	6.4	0.42 sec
No. 59	3B	はち (時)	27D	288	27	4bit	6.4	0.45 sec
No. 60	3C	く (時)	289	28F	1D	4bit	6.4	0.25 sec
No. 61	3D	じゅう (時)	290	29A	57	4bit	6.4	0.43 sec
No. 62	3E	じゅういち (時)	29B	2AF	25	4bit	6.4	0.81 sec
No. 63	3F	じゅうに (時)	2B0	2BF	15	4bit	6.4	0.61 sec
No. 64	40	時	2C0	2C4	5F	4bit	6.4	0.19 sec
No. 65	41	じゅう	2C5	2D0	21	4bit	6.4	0.45 sec
No. 66	42	にじゅう	2D1	2DF	0D	4bit	6.4	0.56 sec
No. 67	43	さんじゅう	2E0	2F0	27	4bit	6.4	0.65 sec
No. 68	44	よんじゅう	2F1	301	7B	4bit	6.4	0.68 sec
No. 69	45	ごじゅう	302	30F	1F	4bit	6.4	0.53 sec
No. 70	46	いっ	310	319	5F	4bit	6.4	0.39 sec

MSM6596-629 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words	M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	length	fs (kHz)	Playback Time
No. 71	47	さん (分)	31A	323	69	4bit	6.4	0.39 sec
No. 72	48	よん (分)	324	32D	23	4bit	6.4	0.37 sec
No. 73	49	ご (分)	32E	335	79	4bit	6.4	0.32 sec
No. 74	4A	ろっ (分)	336	33F	13	4bit	6.4	0.37 sec
No. 75	4B	なな (分)	340	34A	3B	4bit	6.4	0.42 sec
No. 76	4C	はっ (分)	34B	354	2D	4bit	6.4	0.37 sec
No. 77	4D	きゅう (分)	355	35D	07	4bit	6.4	0.32 sec
No. 78	4E	じゅっ (分)	35E	368	6F	4bit	6.4	0.44 sec
No. 79	4F	にじゅっ (分)	369	377	19	4bit	6.4	0.57 sec
No. 80	50	さんじゅっ (分)	378	388	77	4bit	6.4	0.68 sec
No. 81	51	よんじゅっ (分)	389	39A	37	4bit	6.4	0.70 sec
No. 82	52	ごじゅっ (分)	39B	3A8	53	4bit	6.4	0.55 sec
No. 83	53	ぜろ	3A9	3B3	11	4bit	6.4	0.41 sec
No. 84	54	ふん	3B4	3BC	33	4bit	6.4	0.34 sec
No. 85	55	ぷん	3BD	3C5	4D	4bit	6.4	0.34 sec
No. 86	56	件	3C6	3CF	31	4bit	6.4	0.38 sec
No. 87	57	です	3D0	3D4	37	4bit	6.4	0.18 sec
No. 88	58	月	3D5	3DF	35	4bit	6.4	0.42 sec
No. 89	59	火	3E0	3E5	3D	4bit	6.4	0.22 sec
No. 90	5A	水	3E6	3EE	25	4bit	6.4	0.33 sec
No. 91	5B	木	3EF	3F8	7D	4bit	6.4	0.40 sec
No. 92	5C	金	3F9	402	1B	4bit	6.4	0.37 sec
No. 93	5D	土	403	409	17	4bit	6.4	0.25 sec
No. 94	5E	日	40A	414	73	4bit	6.4	0.44 sec
No. 95	5F	曜日	415	421	4D	4bit	6.4	0.50 sec
No. 96	60	(Chinese)	422	434	71	4bit	6.4	0.60 sec
No. 97	61	再見 (Chinese)	435	448	41	4bit	6.4	0.62 sec
No. 98	62	Hello (English)	449	45A	59	4bit	6.4	0.57 sec
No. 99	63	Good-bye (English)	45B	46E	05	4bit	6.4	0.61 sec
No.100	64	Guten tag (Germane)	46F	487	05	4bit	6.4	0.77 sec
No.101	65	Aufwiedershen (Germane)	488	4A1	59	4bit	6.4	0.82 sec
No.102	66	Bonjour Monsieur (French)	4A2	4BC	73	4bit	6.4	0.86 sec
No.103	67	Au revoir Monsieur(French)	4BD	4D5	3F	4bit	6.4	0.78 sec
No.104	68	Buenos dias (Spanish)	4D6	4ED	5D	4bit	6.4	0.76 sec
No.105	69	Adios (Spanish)	4EE	5FB	77	4bit	6.4	0.45 sec

MSM6596-629 Voice Word Address Corresponding List (for time stamp and demonstration)

	Address	Voice Words	M6388, M6588 Start Address	M6388 Stop Address M6588 Upper Stop Address	M6588 Lower Stop Address	length	fs (kHz)	Playback Time
No.106	6A	(Korean)	4FC	522	58	4bit	8.0	1.24 sec
No.107	6B	(Korean)	523	549	17	4bit	8.0	1.22 sec
No.108	6C	こんにちは (Japanese)	54A	55E	4F	4bit	8.0	0.66 sec
No.109	6D	さようなら (Japanese)	55F	576	3F	4bit	8.0	0.75 sec
No.110	6E	Buongirno Signore (Italian)	577	5A1	27	4bit	8.0	1.35 sec
No.111	6F	Arrivederla Signore (Italian)	5A2	5D8	4B	4bit	8.0	1.75 sec
No.112	70	Salutation of Japanese 3 bits	5D9	5EF	49	3bit	8.0	0.95 sec
No.113	71	Salutation of Japanese 4 bits	5F0	60D	65	4bit	8.0	0.95 sec
No.114	72	Salutation of English 3bits	60E	61F	15	3bit	8.0	0.73 sec
No.115	73	Salutation of English 4bits	620	636	5F	4bit	8.0	0.73 sec
No.116	74	Effective sound-1	637	660	29	4bit	8.0	1.32 sec
No.117	75	Effective sound-2	661	68A	7F	4bit	8.0	1.34 sec
No.118	76	Effective sound-3	68B	6EB	29	4bit	8.0	3.08 sec
No.119	77	Barking of dog	6EC	709	7D	4bit	8.0	0.96 sec
No.120	78	Roar of lion	70A	789	27	4bit	8.0	4.07 sec
No.121	79	Lowing of cattle	78A	7E1	43	4bit	8.0	2.80 sec

OKI Semiconductor

MSM6597-XXX

3M-bit Serial Voice ROM

GENERAL DESCRIPTION

The MSM6597 is a Serial Voice ROM of a 1,048,576-word × 1-bit × 3-bank for voice system. The MSM6597 enables to continuing of the serial read operation with the input of a single external clock for the built-in internal address generating circuit.

The internal address is automatically incremented to +1 with the read operation and the address can designate 1024-word to X direction and 1024-word to Y direction by inputting the external serial address. The bank is switched by $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$.

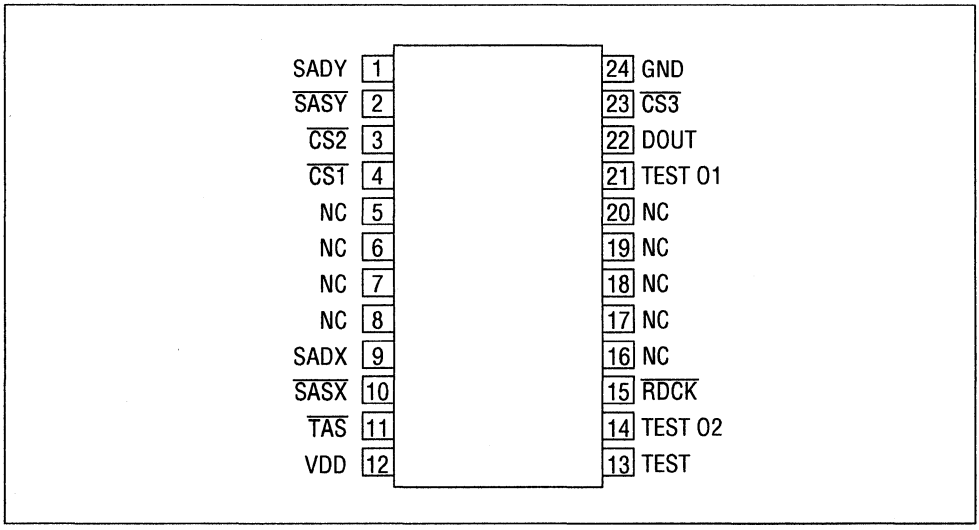
The combination of the Serial Voice ROM (MSM6597) to which the voice data is added, the Solid State recorder (MSM6388, MSM6588) and Serial Voice Register (MSM6389, MSM6587, MSM6586) can easily provide a record and playback system with a fixed message which is stored in the Serial Voice ROM.

Note: MSM6388 or MSM6588 can not control only MSM6597-XXX without the addition of a Serial Voice Register.

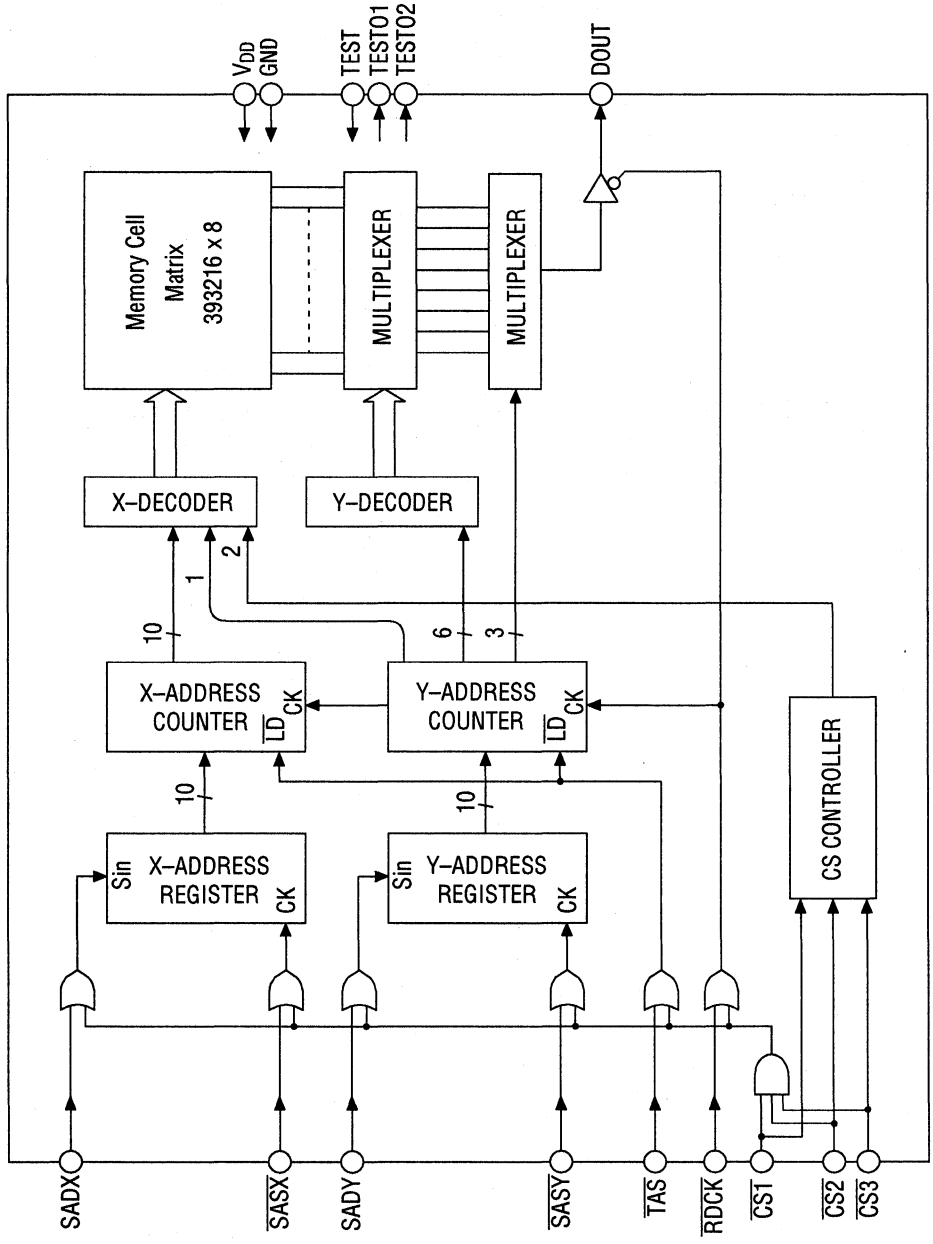
FEATURES

- Configuration:
  1,048,576-word × 1-bit × 3-bank
- Serial access:
  Serial read cycle time: 2.5μs
- Power supply: 5V single voltage
- Package: 24-pin plastic SOP
  (SOP 24-P-430-VK)

PIN CONFIGURAATION



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ V_{CC}+0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Operating Conditions

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	GND = 0V	+3.5 ~ +5.5	V
Operating temperature	T_{op}	—	−40 ~ +85	°C

DC Characteristics

(V_{DD} = 3.5~5.5V, Ta= −40 ~ +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
"H" level input voltage	V_{IH}	—	0.8×V_{DD}	—	V_{DD}−0.3	V
"L" level input voltage	V_{IL}	—	−0.3	—	0.8	V
"H" level output voltage	V_{OH}	I_{OH} = −40μA	V_{DD}−0.3	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = 2mA	0	—	0.45	V
"H" level input current	I_{IH}	V_{IH} = V_{DD}	—	—	10	μA
"L" level input current	I_{IL}	V_{IL} = GND	−10	—	—	μA
Operating consumption current (1)	I_{DD}	t_{RDC} =2.5μS	—	—	15	mA
Operating consumption current (2)	I_{PD}	$\overline{CS1}$=$\overline{CS2}$=$\overline{CS3}$=V_{DD}-0.2V	—	—	10	μA

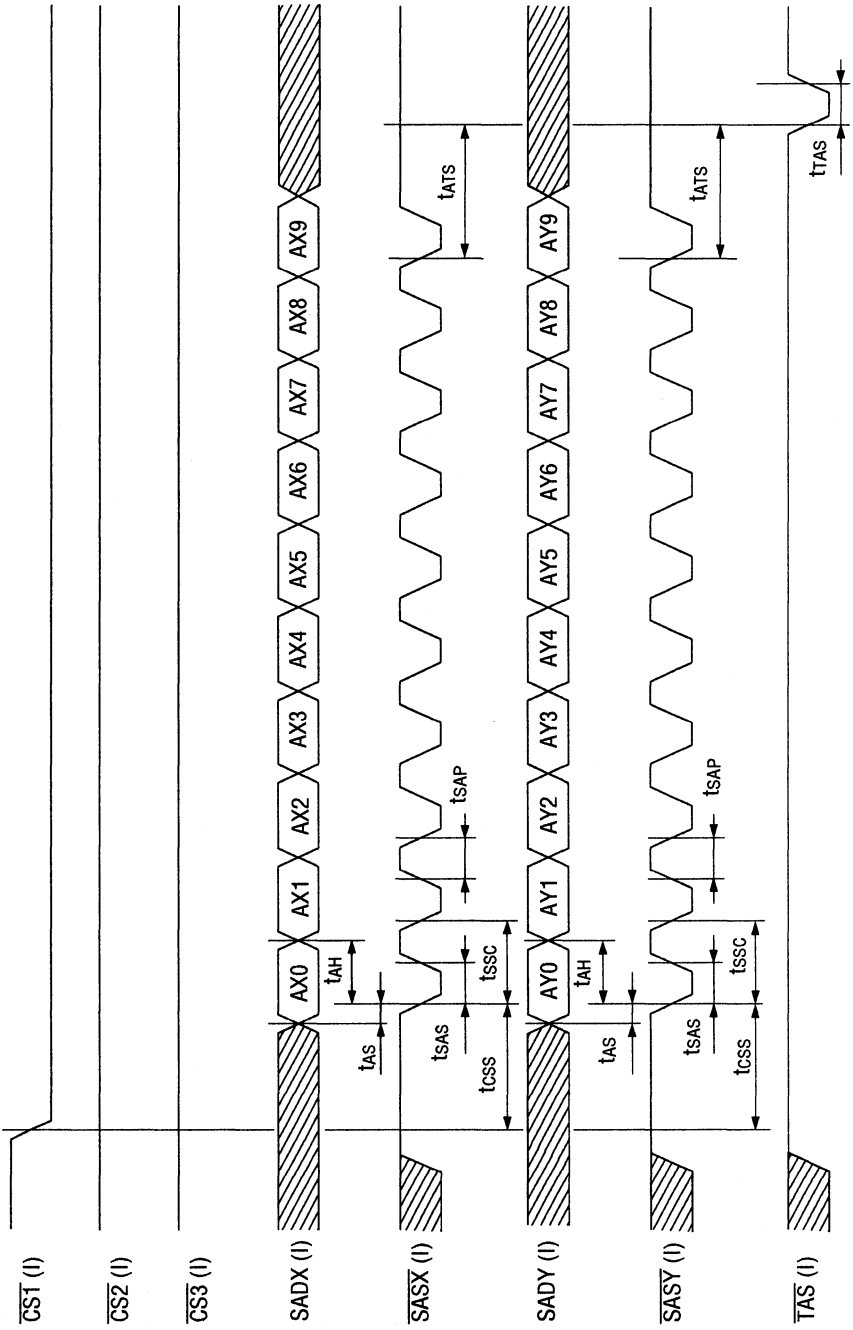
AC Characteristics

(V_{DD}= 3.5 ~ 5.5V, Ta= –40 ~ +85°C)

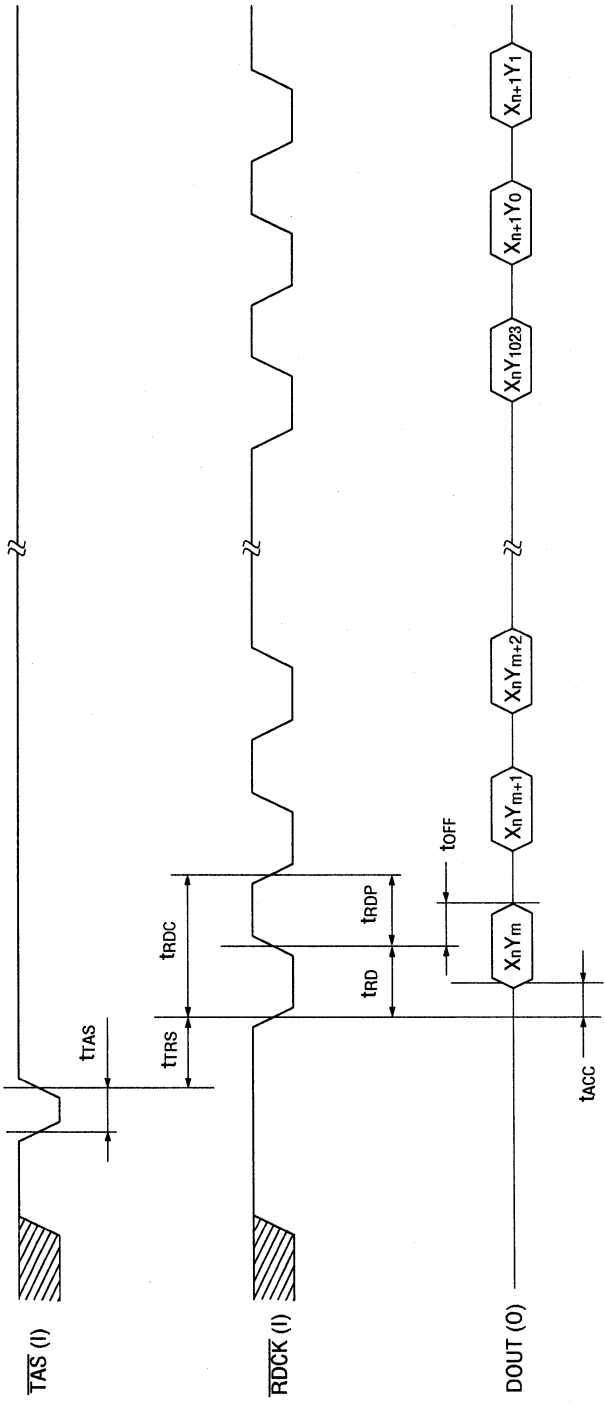
Parameter	Symbol	Value		Unit
		Min.	Max.	
$\overline{CS}$ • $\overline{SAS}$ set-up time	t_{CSS}	1000	—	ns
$\overline{SASX}$, $\overline{SASY}$ cycle time	t_{SSC}	500	—	ns
$\overline{SASX}$, $\overline{SASY}$ precharge time	t_{SAP}	250	—	ns
$\overline{SASX}$, $\overline{SASY}$ pulse width	t_{SAS}	250	—	ns
Address set-up time	t_{AS}	100	—	ns
Address hold time	t_{AH}	100	—	ns
$\overline{TAS}$ set-up time	t_{ATS}	500	—	ns
$\overline{TAS}$ • $\overline{RDCK}$ set-up time	t_{TRS}	500	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	250	—	ns
Read cycle time	t_{RDC}	2500	—	ns
Access time	t_{ACC}	—	1500	ns
Output turn off delay time	t_{OFF}	0	200	ns
$\overline{RDCK}$ precharge time	t_{RDP}	1000	—	ns
$\overline{RDCK}$ pulse width	t_{RD}	1500	—	ns

TIME CHART

Timing for Serial Address Input



Read Access Timing

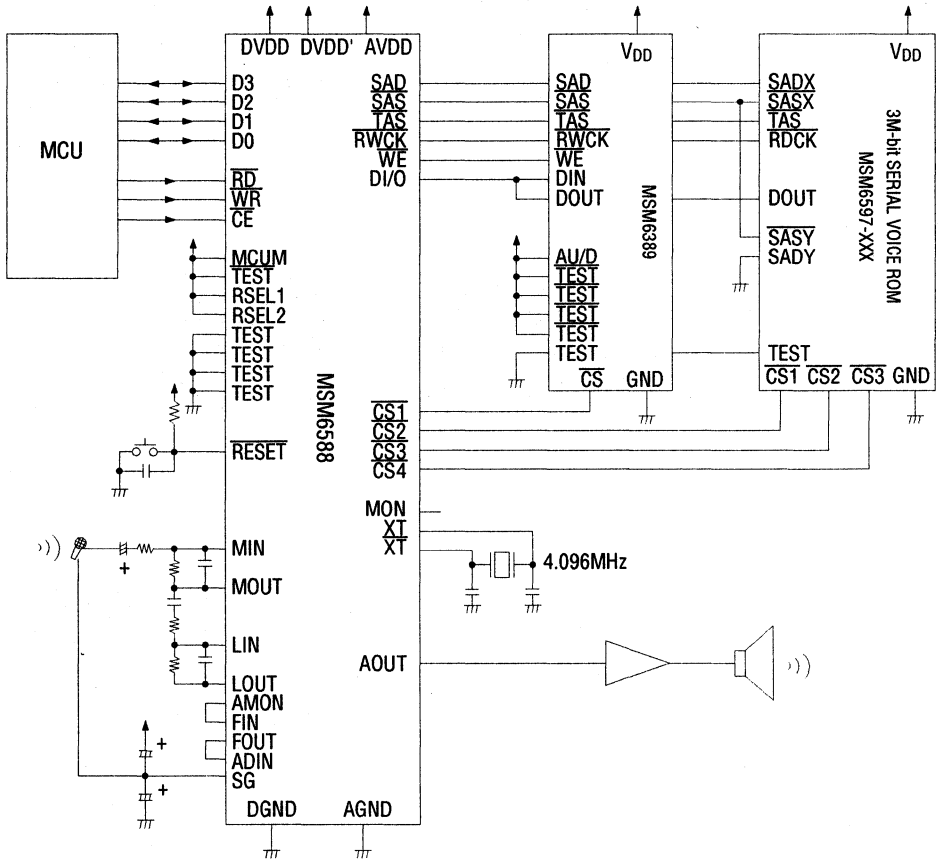


TERMINAL FUNCTION EXPLANATION

Pin Name	I/O	Function
VDD	-	Power supply pin.
GND	-	Ground pin .
SADX	I	(SERIAL ADDRESS) This is pin for input of X address header of read. This pin can designate 1024-word and can input 1024 address data as serial data of 10-bit (AX0~AX9).
SADY	I	(SERIAL ADDRESS) This is pin for input of Y address header of read. This pin can designate 1024-word and can input 1024 address data as serial data of 10-bit (AY0~AY9).
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) This is clock input pin for input of serial address data of X address to internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROBE) This is clock input pin for input of serial address data of Y address to the internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) This is input pin to set serial address data to be taken in address register to internal address counter. X address and Y address are taken in by fall of $\overline{TAS}$ pin.
$\overline{RDCK}$	I	(READ CLOCK) This is clock pin to read out information of data register. Internal operation starts with the falling edge of $\overline{RDCK}$ and the information of the data register is output from DOUT pin. In addition, internal address counter is automatically increased by the fall of $\overline{RDCK}$.
DOUT	O	(DATA OUT) If $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ or $\overline{RDCK}$ are held to "H", DOUT remains in the high impedance state. If information of "H" or "L" is read out during read, DOUT pin is set to "H" or "L" and information read out is held until $\overline{RDCK}$ is restored to "H".
$\overline{CS}$ $\overline{CS2}$ $\overline{CS3}$	I	(CHIP SELECT) When $\overline{CS1}$ goes "L", bank 1 is selected, when $\overline{CS2}$ goes "L", bank 2 is selected, and when $\overline{CS3}$ goes "L", bank 3 is selected. In addition, all input pins are disabled when $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ go "H". This pin can be used in parallel by connecting data output pins of multiple serial Voice ROM's.
TEST	I	This is pin for LSI test. Input "L" level.
TESTO1 TESTO2	O	This is pin for LSI test. Open this pin.

APPLICATION CIRCUIT

Application Circuit for MSM6588



Note: When MSM6597 is driven by MSM6388 or MSM6588, a serial register is required. (MSM6597 can not operate without it.)

Interface LSI

OKI Semiconductor

MSM6690

ROM Interface LSI

DESCRIPTION

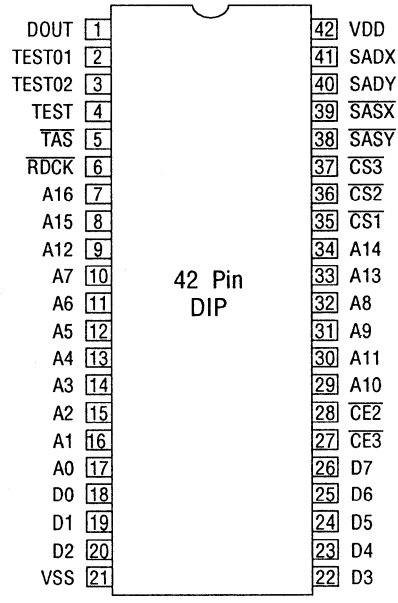
The MSM6690 is a LSI capable of driving 3 devices of 131,072 x 8 bit EPROM or MASKROM.

The MSM6690 is provided with a built-in internal address generator circuit and one external clock input enables continued serial read operations. The internal address counter is automatically incremented by 1 each time of read operation. The external serial address input allows 1,024 words to be addressed toward the X-direction, and 1,024 words toward the Y-direction.

The ROM is selected through $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$.

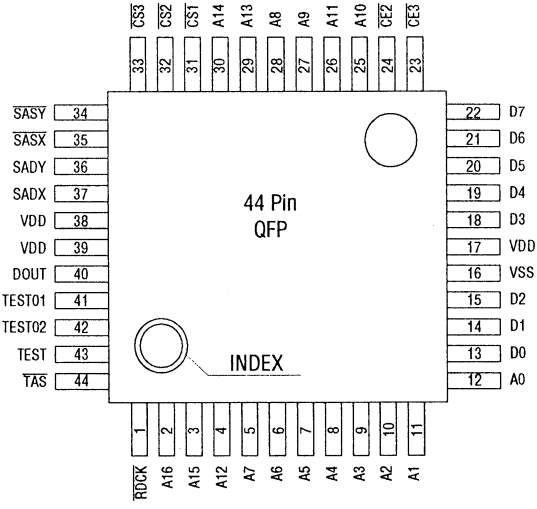
By combining a MSM6690, a voice data-stored ROM, an OKI solid recording LSI (MSM6388 or MSM6588), and an OKI serial register (MSM6389, MSM6587 or MSM6586), a record player with a fixed message can be easily structured. And the MSM6690 can be used for evaluating voice data to be stored in a serial voice ROM (M6595, M6596, or M6597).

* When driving the MSM6690 with the MSM6388 or the MSM6588, a serial register is required.

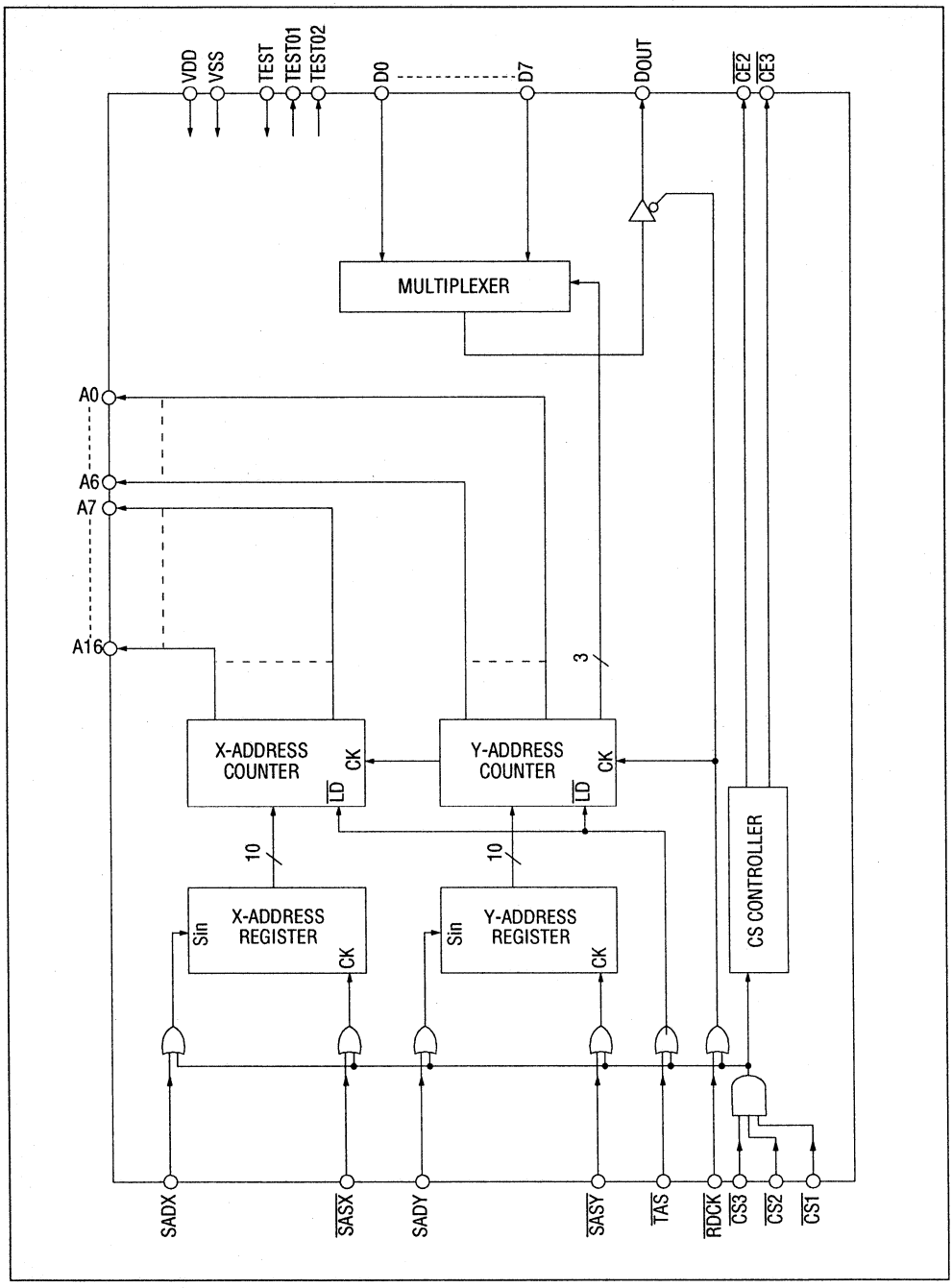


FEATURES

- Capable of driving 3 devices of 1 Mbit EPROM
- Capable of driving 3 devices of 1 Mbit MASKROM
- Supply voltage: Single 5V
- Package: 42 pin plastic DIP (DIP42-P-600)
  44 pin plastic QFP (QFP44-P-910-VK)



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Typical: VSS ≡ 0V	-0.3 ~ +7.0	V
Input Voltage	V_I		-0.3 ~ V_{DD}+0.3	V
Output Voltage	V_O		-0.3 ~ V_{DD}+0.3	V
Input Current	I_I		-10 ~ +10	mA
Output Current	I_O		-20 ~ +20	mA
Storage Temperature	T_{stg}	–	-55 ~ +150	°C

Operating Range

(VSS = 0V)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	+3.0 ~ +6.0	V
Operating Temperature	T_{op}	-40 ~ +85	°C

DC Characteristics

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, Ta = -40 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ.*	Max.	Unit
"H" level Input Voltage	V_{IH}	CMOS level input	3.5	–	V_{DD}+3	V
"L" level Input Voltage	V_{IL}	CMOS level input	-0.3	–	1.5	V
"H" level Input Current	I_{IH}	$V_{IH} = V_{DD}$	–	0.01	10	µA
"L" level Input Current	I_{IL}	$V_{IL} = V_{SS}$	-10	-0.01	–	µA
3-state output leak current	I_{OZH}	$V_{OH} = V_{DD}$	–	0.01	10	µA
(with open drain output)	I_{OZL}	$V_{OL} = V_{SS}$	-10	-0.01	–	
"H" level Output Voltage	V_{OH}	I_{OH} = -5.0µA	2.4	4.2	V_{DD}	V
"L" level Output Voltage	V_{OL}	I_{OL} = 5.0µA	V_{SS}	0.24	0.5	V
Supply Current at standby	I_{DS}	Output open $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	–	0.1	100	µA
supply Current at operating	I_{DD}	–	–	–	2	mA

(Note) The typical is in the case of VDD = 5.0V , Ta = 25°C

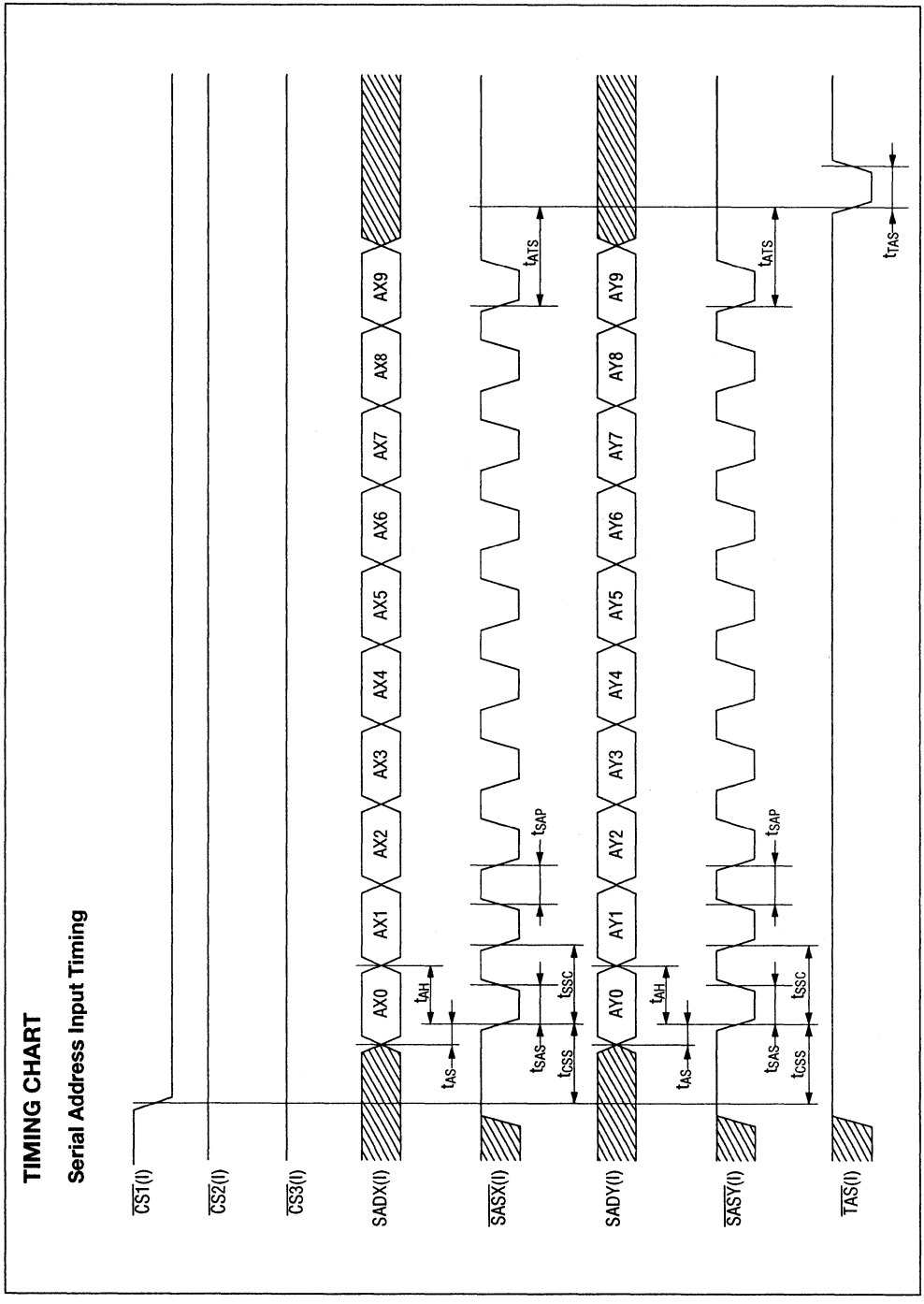
AC Characteristics

VDD= 4.5 to 5.5V Ta = 0 to 70°C

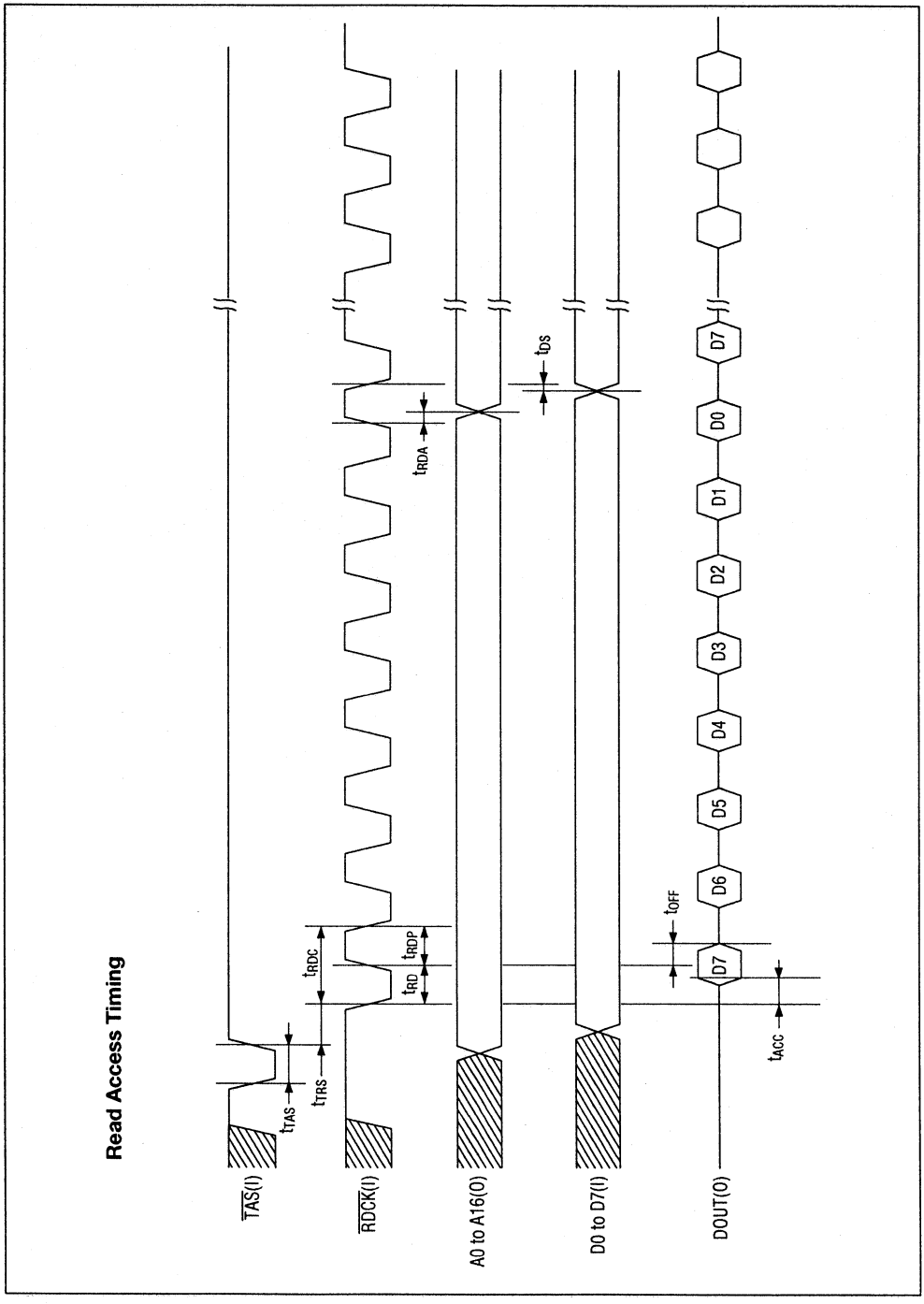
Parameter	Symbol	MIN	TYP	MAX	Unit
$\overline{CS}$•$\overline{SAS}$ setup time	t_{CSS}	1000	—	—	ns
$\overline{SASX}$, $\overline{SASY}$ cycle time	t_{SSC}	500	—	—	ns
$\overline{SASX}$, $\overline{SASY}$ precharge time	t_{SAP}	250	—	—	ns
$\overline{SASX}$, $\overline{SASY}$ pulse time	t_{SAS}	250	—	—	ns
Address setup time	t_{AS}	100	—	—	ns
Address hold time	t_{AH}	100	—	—	ns
$\overline{TAS}$ setup time	t_{ATS}	500	—	—	ns
$\overline{TAS}$.$\overline{RDCK}$ setup time	t_{TRS}	500	—	—	ns
$\overline{TAS}$ pulse time	t_{TAS}	250	—	—	ns
Read cycle time	t_{RDC}	4000	—	—	ns
Access time	t_{ACC}	—	—	3000	ns
Output turnoff delay time	t_{OFF}	0	—	200	ns
$\overline{RDCK}$ precharge time	t_{RDP}	1000	—	—	ns
$\overline{RDCK}$ pulse time	t_{RD}	3000	—	—	ns
$\overline{RDCK}$ • address delay time	t_{RDA}	200	—	—	ns
Data setup time	t_{DS}	200	—	—	ns

TIMING CHART

Serial Address Input Timing



Read Access Timing



PIN FUNCTIONS

Pin name	I/O	Pin function
VDD	-	Supply pin
VSS	-	GND pin
SADX	I	(SERIAL ADDRESS) Pin to input starting X address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AX0 to AX9) via SADX pin.
SADY	I	(SERIAL ADDRESS) Pin to input starting Y address. 1024 words are addressed, and 1024 address data can be input as serial data of 10 bit (AY0 to AY9) via SADY Pin.
$\overline{SASX}$	I	(SERIAL ADDRESS STROBE) Clock input pin to load X address's serial address data to internal register.
$\overline{SASY}$	I	(SERIAL ADDRESS STROGE) Clock input pin to load Y address's serial address data to internal register.
$\overline{TAS}$	I	(TRANSFER ADDRESS STROBE) Input pin to set serial address data loaded in address register, to internal address counter. X address and Y address data are loaded at fall of $\overline{TAS}$ pin.
$\overline{RDCK}$	I	(READ CLOCK) Clock input pin to read data in data register. Internal operation starts on falling edge of $\overline{RDCK}$, and data in data register is output via DOUT Pin. And internal address counter is automatically incremented by 1 due to falling of $\overline{RDCK}$.
DOUT	O	(DATA OUT) In case $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are all at "H" level, or $\overline{RDCK}$ is at "H" level data output pin is always at high impedance state. When "H" level data or "L" level data is read out, output pin is set to "H" level or "L" level and its read data is kept until $\overline{RDCK}$ turns to "H" level.
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$	I	(CHIP SELECT) Pin to select 3 ROMS $\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CE2}$ $\overline{CE3}$ L — — H H H L — L H H H L H L H H H H H When $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are all set to "H" level, all input/output pins become disable. By use of these pins, 3 ROM data output pins can be connected in paralle.

PIN FUNCTIONS (cont'd)

Pin name	I/O	Pin function
$\overline{CE2}$ $\overline{CE3}$	O	(CHIP ENABLE) Pin to make ROM enable. Connect it to ROM's $\overline{CE}$.
A0 ~ A16	O	(ADDRESS OUT) Pin to output ROM address
D0 ~ D7	I	(DATA IN) Pin to input ROM data
TEST	I	Pin to test LSI Input "L" level data
TEST01 TEST02	O	Pin to test LSI Set to open

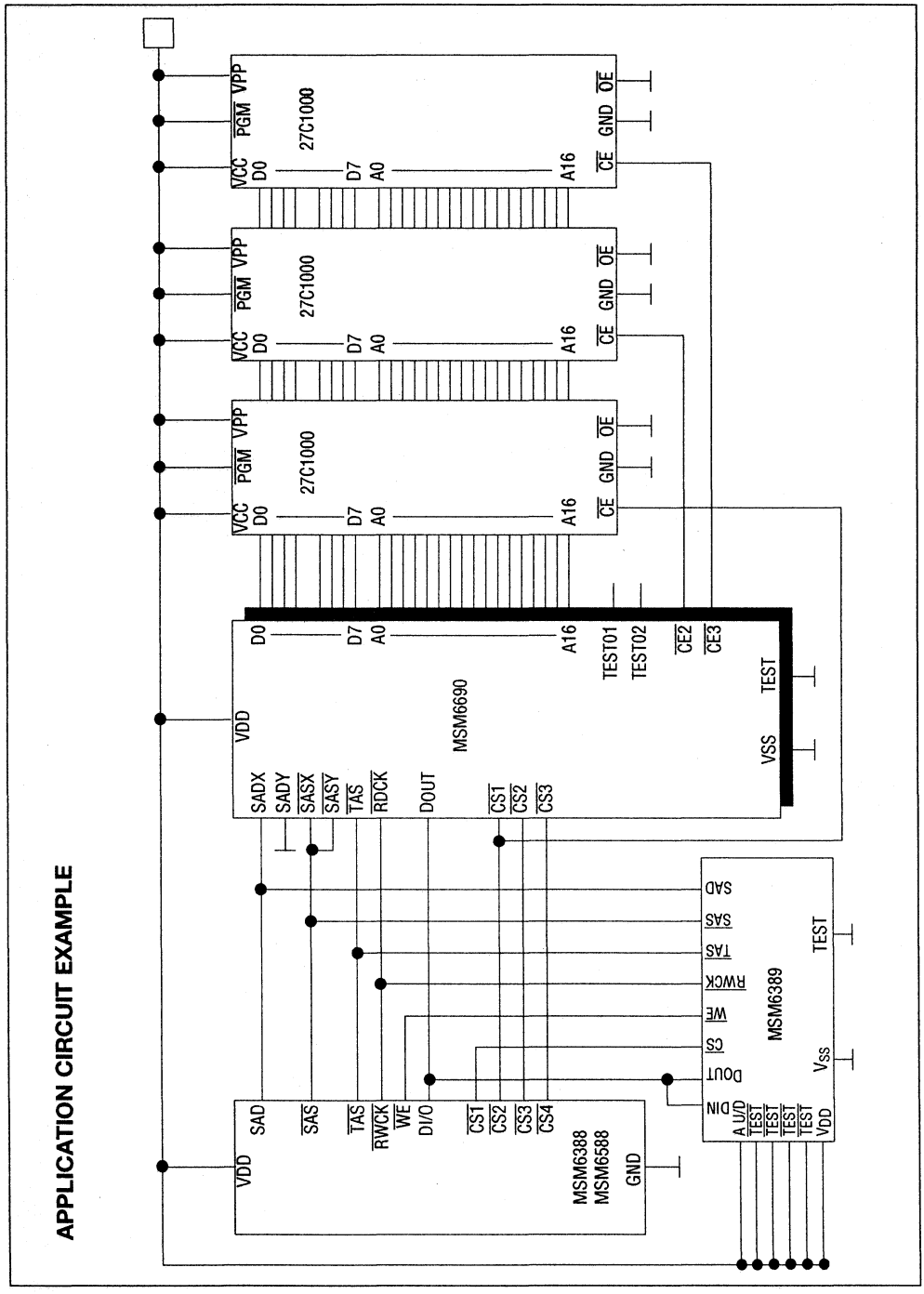
1 Mbit EPROM AND 1 Mbit MASKROM ADDRESS CONFIGURATON

128K = 131072 words

128 words

	D7	D6	D5	D4	D3	D2	D1	D0
00000h	X_0 Y_0	X_0 Y_1	X_0 Y_2	X_0 Y_3	X_0 Y_4	X_0 Y_5	X_0 Y_6	X_0 Y_7
00001h	X_0 Y_8	X_0 Y_9	X_0 Y_{10}	X_0 Y_{11}	X_0 Y_{12}	X_0 Y_{13}	X_0 Y_{14}	X_0 Y_{15}
00002h	X_0 Y_{16}	X_0 Y_{17}	X_0 Y_{18}	X_0 Y_{19}	X_0 Y_{20}	X_0 Y_{21}	X_0 Y_{22}	X_0 Y_{23}
0007Eh	X_0 Y_{1008}	X_0 Y_{1009}	X_0 Y_{1010}	X_0 Y_{1011}	X_0 Y_{1012}	X_0 Y_{1013}	X_0 Y_{1014}	X_0 Y_{1015}
0007Fh	X_0 Y_{1016}	X_0 Y_{1017}	X_0 Y_{1018}	X_0 Y_{1019}	X_0 Y_{1020}	X_0 Y_{1021}	X_0 Y_{1022}	X_0 Y_{1023}
00080h	X_1 Y_0	X_1 Y_1	X_1 Y_2	X_1 Y_3	X_1 Y_4	X_1 Y_5	X_1 Y_6	X_1 Y_7
00081h	X_1 Y_8	X_1 Y_9	X_1 Y_{10}	X_1 Y_{11}	X_1 Y_{12}	X_1 Y_{13}	X_1 Y_{14}	X_1 Y_{15}
1FFFDh	$X_{1023}Y_{1000}$	$X_{1023}Y_{1001}$	$X_{1023}Y_{1002}$	$X_{1023}Y_{1003}$	$X_{1023}Y_{1004}$	$X_{1023}Y_{1005}$	$X_{1023}Y_{1006}$	$X_{1023}Y_{1007}$
1FFFEh	$X_{1023}Y_{1008}$	$X_{1023}Y_{1009}$	$X_{1023}Y_{1010}$	$X_{1023}Y_{1011}$	$X_{1023}Y_{1012}$	$X_{1023}Y_{1013}$	$X_{1023}Y_{1014}$	$X_{1023}Y_{1015}$
1FFFFh	$X_{1023}Y_{1016}$	$X_{1023}Y_{1017}$	$X_{1023}Y_{1018}$	$X_{1023}Y_{1019}$	$X_{1023}Y_{1020}$	$X_{1023}Y_{1021}$	$X_{1023}Y_{1022}$	$X_{1023}Y_{1023}$

APPLICATION CIRCUIT EXAMPLE



OKI Semiconductor IC

MSM6691

DRAM INTERFACE LSI

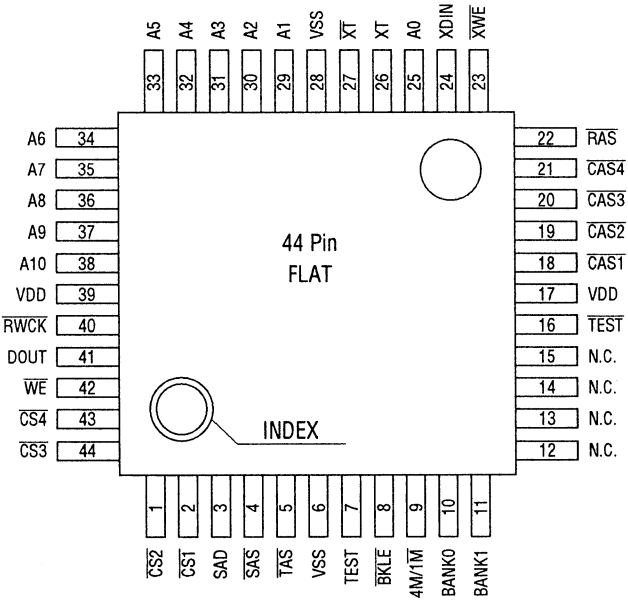
Description

DRAMs can be used for voice storage by connecting the MSM6691 with Oki's integrate R/W (Read/Write) LSIs, the MSM6388, and the MSM6588. The MSM6691 translates the signals associated with the dedicated serial register interface of the MSM6388 and MSM6588 driver interface when used in stand-alone mode.

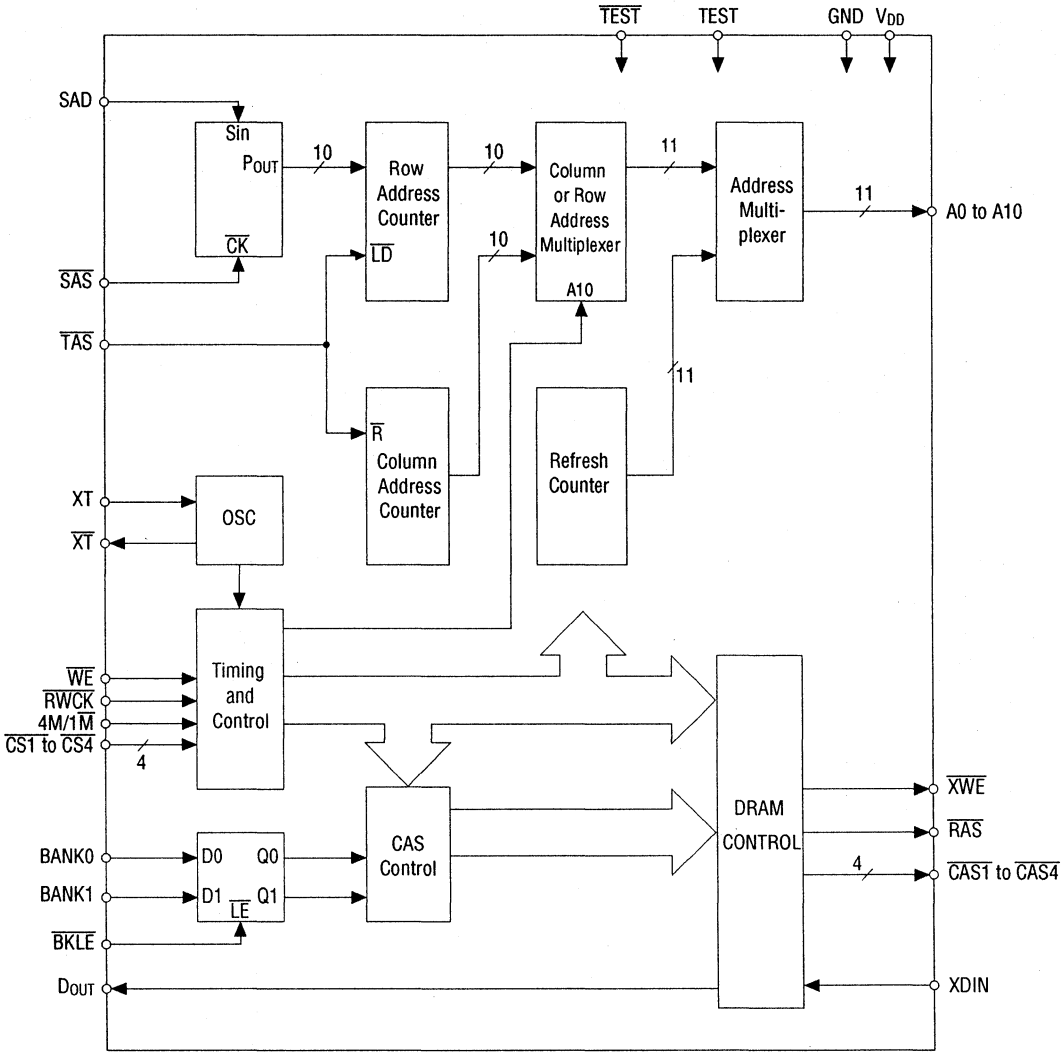
Features

- DRAM (x 16-bit configuration)
- 1-Mbit DRAM (M 51100A, M511001A): 4 units can be used
- 4-Mbit DRAM (M 514100A, M514101A): 4 units can be used
- Power voltage: 5 V single
- Built-in refresh circuit (RAS only refresh)
- Oscillation frequency: 8 MHz (during refresh)
- Sampling frequency
- 4 kHz to 32 kHz when MSM6388 is connected.
- 4 kHz to 16 kHz when MSM6588 is connecred.
- Package
- 44-pin plastic QFP (QFP44-P-910-VK)

Terminal Connection Diagram



Circuit Configuration



Electric Characteristics

Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Unit
Power Voltage	V_{DD}	Ta = 25°C Standard is Vss = 0V	0.5 to +7	V
Input Voltag	V_I		0.5 to V_{DD}+0.5	V
Output Voltag	V_O		0.5 to V_{DD}+0.5	V
Input Current	I_I		10 to +10	mA
Output Current	I_O		20 to +20	mA
Storage Temperature	T_{stg}	——	65 to +150	°C

Operation Range

VSS = 0V

Item	Symbol	Rated Value	Unit
Power Voltage	V_{DD}	4.5 to +5.5	V
Operation Temperature	V_{OPR}	0 to +70	°C
Oscillation Frequency	fosc	8	MHz

DC Characteristics

(Ta = 0 to 70 °C, V_{DD} = 5V±10%, V_{SS} = 0V)

Item	Symbol	Conditions	Rated value			Unit
			Minimum	Standard *1	Maximum	
H Level Input Voltage	V_{IH}	—	3.5	—	V_{DD}+0.3	V
L Level Input Voltage	V_{IL}	—	0.3	—	1.5	V
H Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	µA
L Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	10	-0.01	—	µA
3-state Output Leak Current (Including open drain output)	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	µA
	I_{OZL}	$V_{OL} = V_{SS}$	-10	-0.01	—	
H Level Output Voltage	V_{OH}	I_{OH} = -5.0mA	2.4	4.20	V_{DD}	V
L Level Output Voltage	V_{OL}	I_{OL} = +5.0mA	V_{SS}	0.24	0.5	V
Operating Current Consumption	I_{DD}	Output Open V_{IH}=V_D f_{OSC}=8MHz V_{IL}=V_{SS}	—	—	3	mA

(Note)*1 Standard when V_{DD} = 5.0V, Ta = 25°C

AC Characteristics

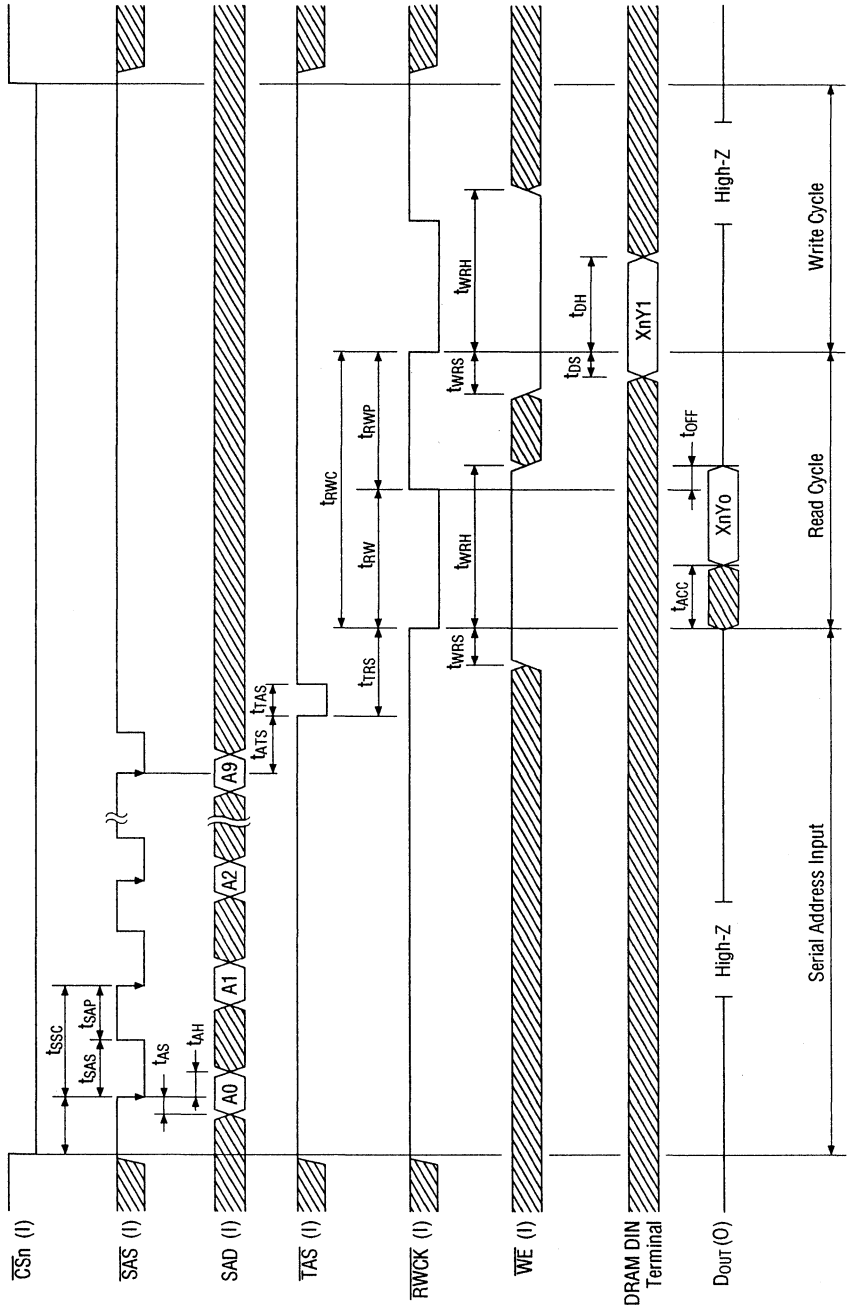
(Ta = 0 to 70 °C, VDD = 5V±10%, Vss = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
$\overline{CS}$,• $\overline{SAS}$ Setup Time	tCSS	1000	—	—	ns
$\overline{SAS}$ Cycle Time	tSSC	100	—	—	ns
$\overline{SAS}$ Precharge Time	tSAP	500	—	—	ns
$\overline{SAS}$ Pulse Width	tSAS	500	—	—	ns
$\overline{SAD}$ Address Setup Time	tAS	200	—	—	ns
$\overline{SAD}$ Address Hold Time	tAH	200	—	—	ns
$\overline{TAS}$, Setup Time	tATS	800	—	—	ns
$\overline{TAS}$,• $\overline{RWCK}$ Setup Time	tTRS	800	—	—	ns
$\overline{TAS}$ Pulse Width	tTAS	400	—	—	ns
Read/Write Cycle Time	tRWC	1800	—	—	ns
Access Time	tACC	—	—	875	ns
Output Turnoff Time	tOFF	—	—	—	ns
$\overline{RWCK}$ Precharge Time	tRWP	90	—	—	ns
$\overline{RWCK}$ Pulse Width	tRW	900	—	—	ns
Read/Write Instruction Setup Time	tWRS	20	—	—	ns
Read/Write Instruction Hold Time	tWRH	200	—	—	ns
DRAM • DIN Data Setup Time	tDS	0	—	—	ns
DRAM • DIN Data Set Hold Time	tDH	1000	—	—	ns
$\overline{RWCK}$ • $\overline{RAS}$, Delay Time	tRRS	125	—	375	ns
$\overline{RAS}$, Pulse Width	tRAS	—	750	—	ns
$\overline{CAS}$, Pulse Width	tCAS	—	500	—	ns
Low Address Setup Time	tASR	—	125	—	ns
Low Address Hold TimetRAH	tRAH	—	125	—	ns
Column Address Setup Time	tASC	—	125		ns
Column Address Hold Time	tCAH	—	500	—	ns
Write Instruction Setup Time	tWCS	—	375	—	ns
Write Instruction Hold Time	tWCH	—	625	—	ns
XDIN Data Input Setup Time	tDCS	250	—	—	ns
XDIN Data Input Hold Time	tDCH	0	—	—	ns

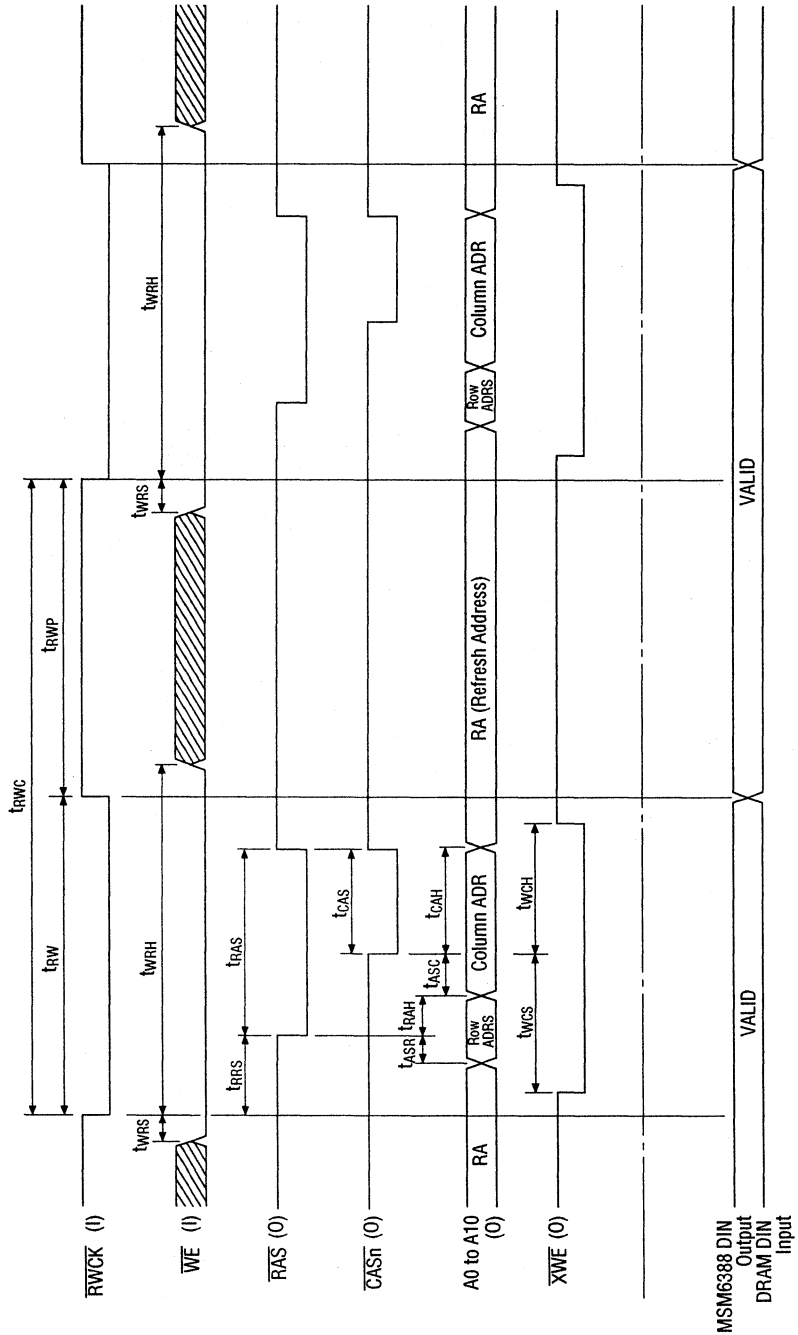
AC Characteristics (Continued)

Item	Symbol	MIN	TYP	MAX	Unit
Refresh Cycle Time	tRRC	—	8000	—	ns
Refresh $\overline{RAS}$ Pulse Width	tRRAS	—	1000	—	ns
	tRRAS2	125	—	875	ns
Refresh Precharge Time	tRRP2	—	125	—	ns
Bank Select Setup Time	tBKS	1000	—	—	ns
Bank Select Hold Tim	tBKH	1000	—	—	ns
$\overline{BKLE}$ Pulse Width	BKLE	1000	—	—	ns
Bank Data Setup Time	tBDS	200	—	—	ns
Bank Fata Hold Time	tBDH	200	—	—	ns

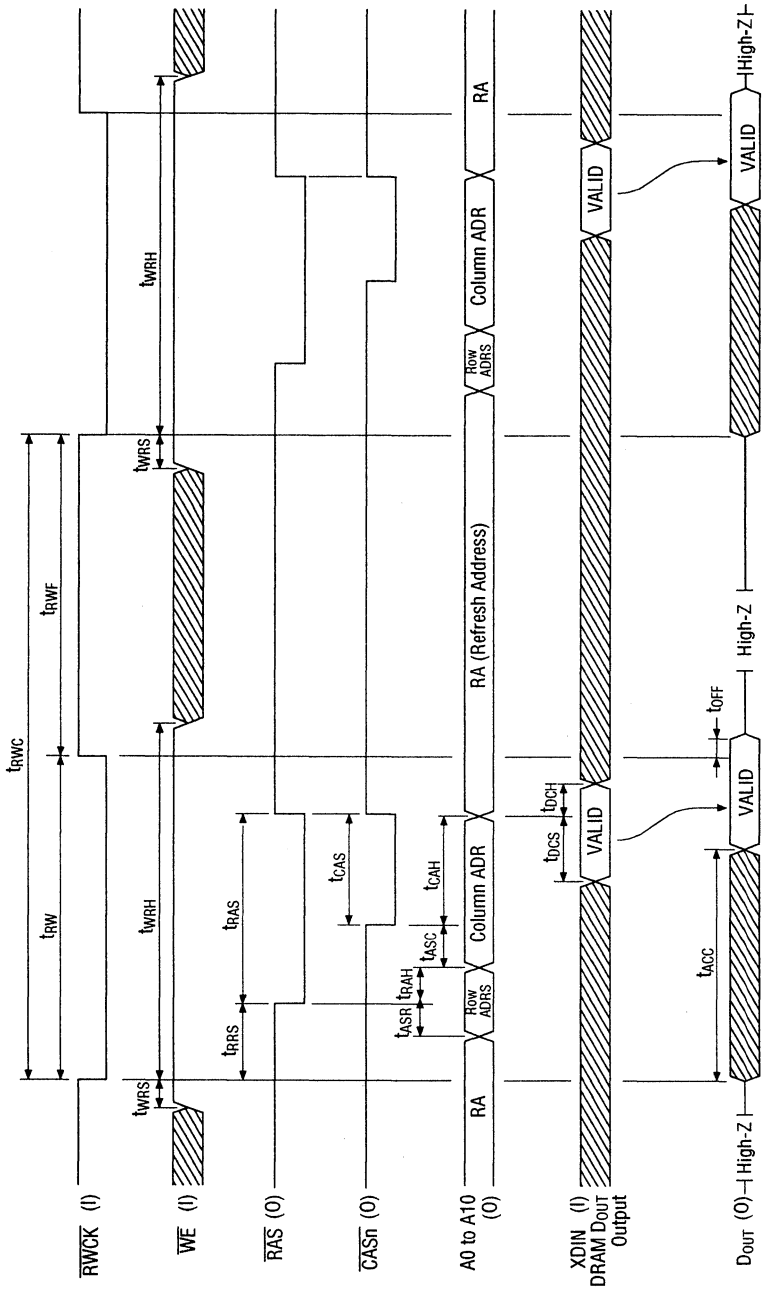
Serial Address Input Timing, R/W Cycle



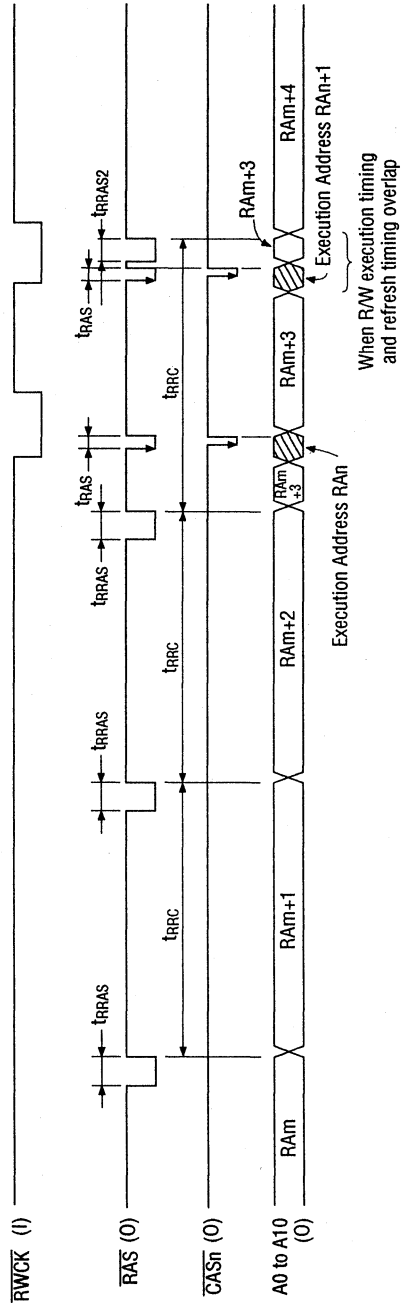
DRAM Drive Timing (Write Cycle, Write Time)



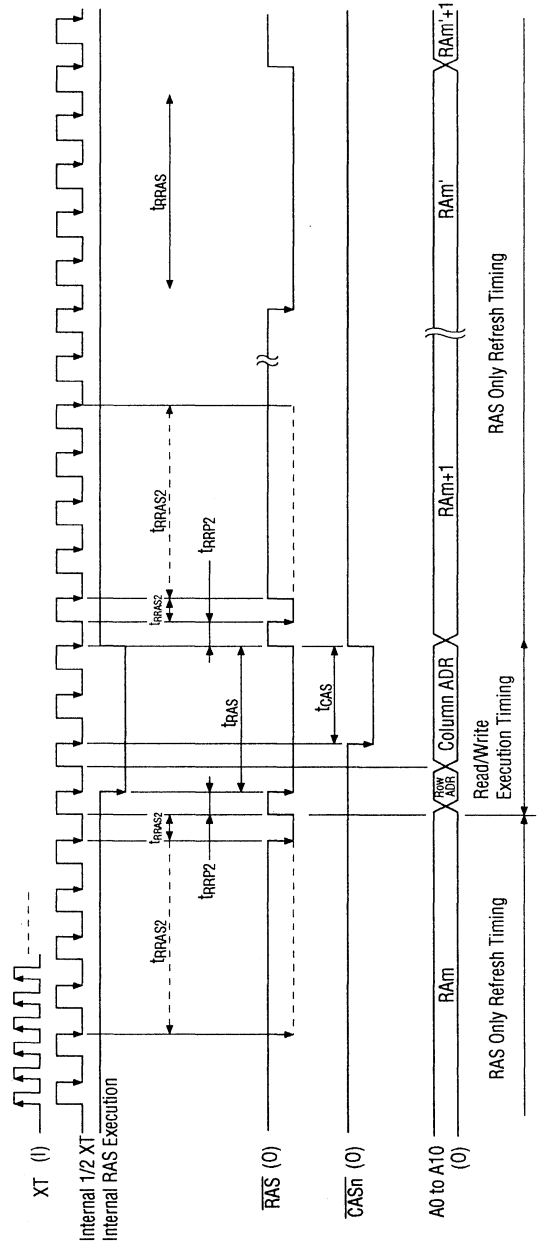
DRAM Drive Timing (Read Cycle, Read Time)



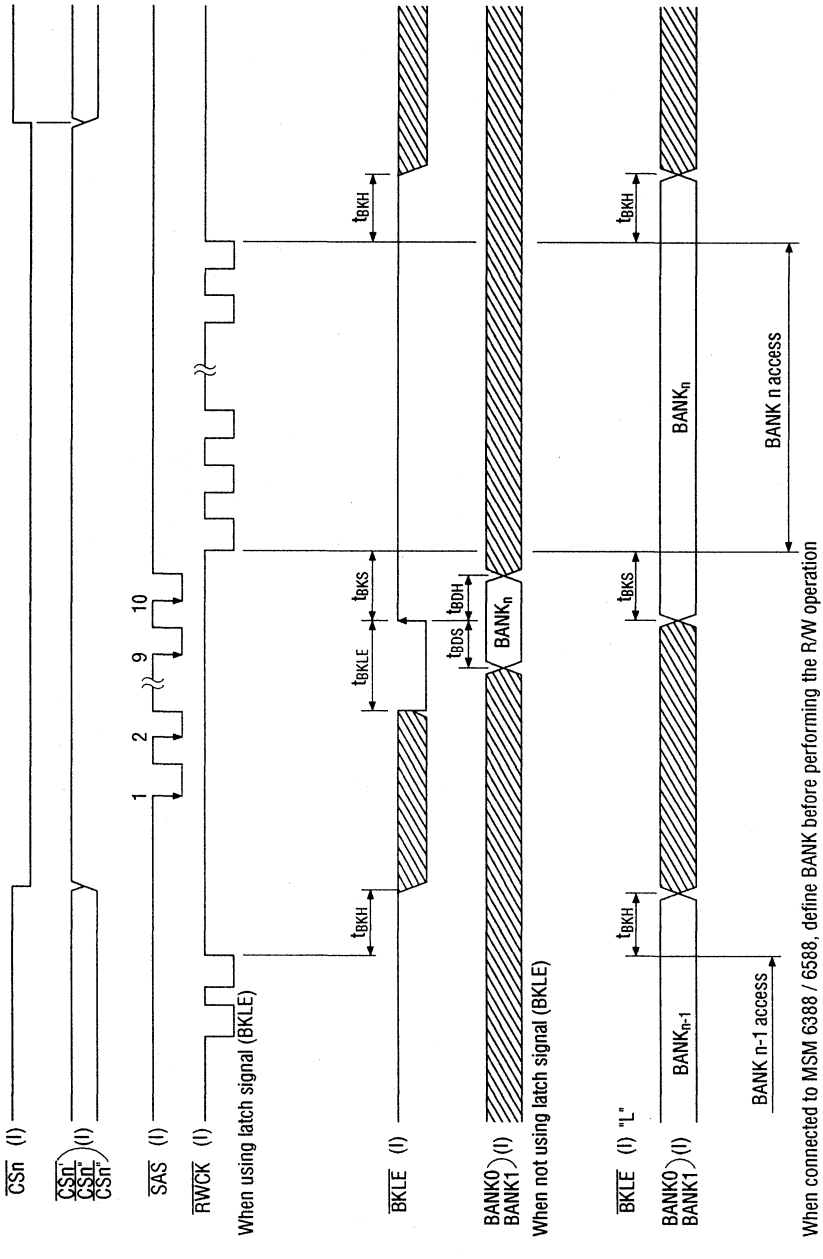
DRAM Drive Timing (RAS Only Refresh Cycle)



DRAM Drive Timing (When R/W timing and refresh timing overlap)



Chip Select, Bank Select (When using 4-M DRAM)



Terminal Functions

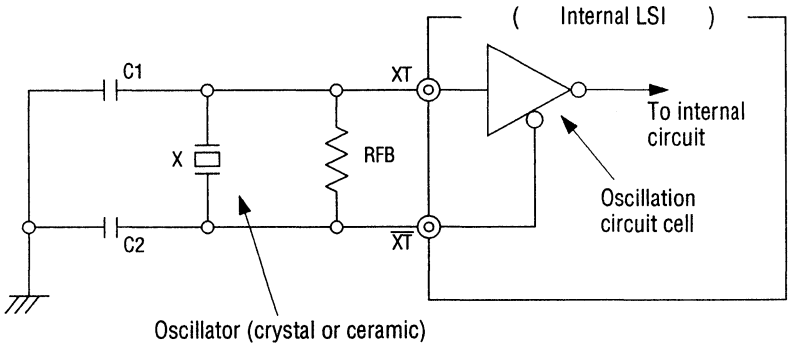
Terminal Symbol	I/O	Function
V_{DD}	I	Power terminal
GND	I	GND terminal
XT	I	Oscillator connecting terminal
$\overline{XT}$	O	Oscillator connecting terminal
TEST	I	LSI test terminal. Set to "L"
$\overline{TEST}$	I	LSI test terminal. Set to "H"
SAD	I	Terminal to input initial address of R/W
$\overline{SAS}$	I	Clock terminal to input serial address data to internal register
$\overline{TAS}$	I	Input terminal to load serial data, input to address register, and reset to internal address countert
$\overline{RWCK}$	I	Clock input terminal to read and write data register information. At $\overline{RWCK}$ fall, internal operation starts. In read mode data input to XDIN is latched and output to DOUT terminal. In write mode, DIN (D I/O) output data MSM6388 (MSM6588) is input to DIN of DRAM. At $\overline{RWCK}$ fall internal address counter automatically increments, and address data is output from A_0 to A_{10}.

Terminal Functions (Continued)

Terminal Symbol	I/O	Function
$\overline{WE}$	I	Input terminal to select R/W modes
$\overline{XWE}$	O	Terminal to control DRAM
A0 to A10	O	Address output terminals to control DRAM
$\overline{RAS}$	O	Terminal to control DRAM
$\overline{CAS1}$ $\overline{CAS2}$ $\overline{CAS3}$ $\overline{CAS4}$	O	Terminals to control DRAM
XDIN	I	Terminal to input write data
DOUT	O	Terminal to output data
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Terminals to input chip select when 1-M DRAM is connected . Because input terminal to select most significant address when 4-M DRAM is connected.
4M/$\overline{1M}$	I	Input terminal to select 4-M DRAM ro 1-M DRAM for connection. "L" 1M DRAM oonnected; 4-M DRAM connected
BANK0 BANK1	I	Terminal to input chip select data when 4-M DRAM is connected. Terminal is used to select desired DRAM from DRAMs connected to select terminals. $\overline{CAS1}$ to $\overline{CAS4}$. Set to "L" when 1-M DRAM is connected.
$\overline{BKLE}$	I	Input terminal to latch data, input to BANK0, BANK1, when 4-M DRAM is used. "L" indicates a "through" setting. "H" indicates a "latch" setting . Set to "L" when 1-M DRAM is used.

Select Terminal	Bank1	Bank0
$\overline{CAS1}$	L	L
$\overline{CAS2}$	L	H
$\overline{CAS3}$	H	L
$\overline{CAS4}$	H	H

Schematic of the MSM 6691 Oscillator



Figue 1 Crystal/Ceramic Oscillation Circuit

Manufacture	Origini Oscillation	Oscillator	Model Name	C1 = C2	RFB
	8 MHz				1MΩ

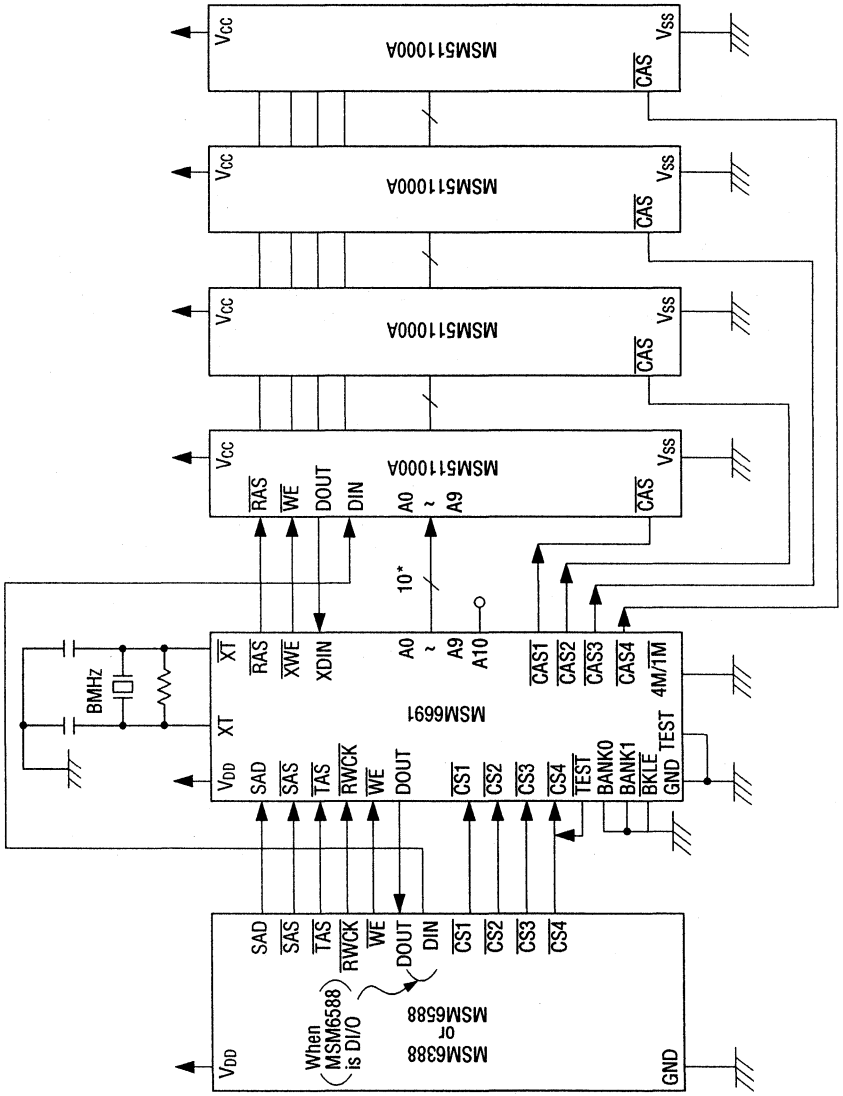
The configuration and resistance values of the oscillation circuit and the value of the capacitor diffeers depending on the oscillation frequency and the oscillator used.

When using an oscillation circuit, evaluate the characteristics according to the actual conditions of use. Determine the circuit configuration and the circuit constants.

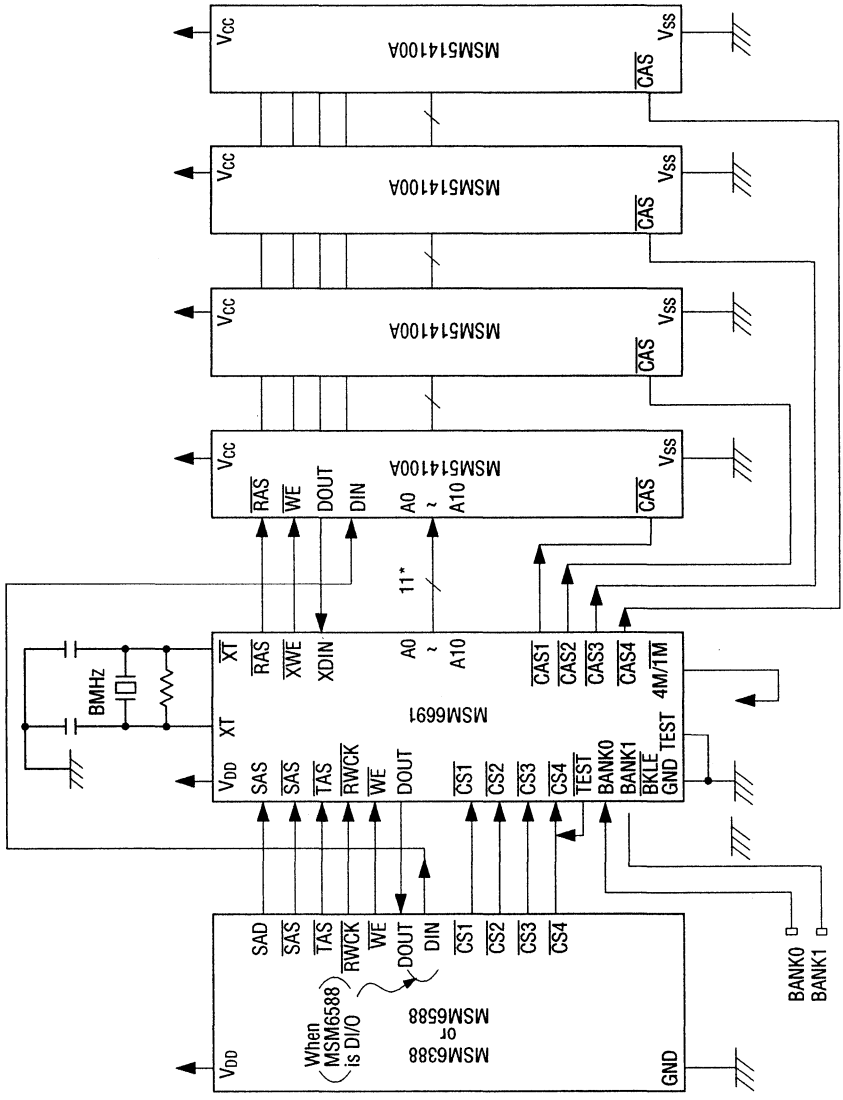
Circuit Example

* Figure 2 indicates an edxample of the circuits usedd when MSM 6388 (M 6588) is used with foru 1 - Mbit DRAMs.

* Figure 3 indicates an example of the circuits used when MSM 6388 (M 6588) is used with foru 4 - Mbit DRAMs.



* One of four DRAMs can be selected by BANK0 and BANK1,



OKI Semiconductor

MSM6791

DRAM INTERFACE LSI

GENERAL DESCRIPTION

MSM6791 can be used as a memory for which DRAM stores a voice data by connecting OKI solid-state recording and playback LSIs (MSM6788 and MSM6688).

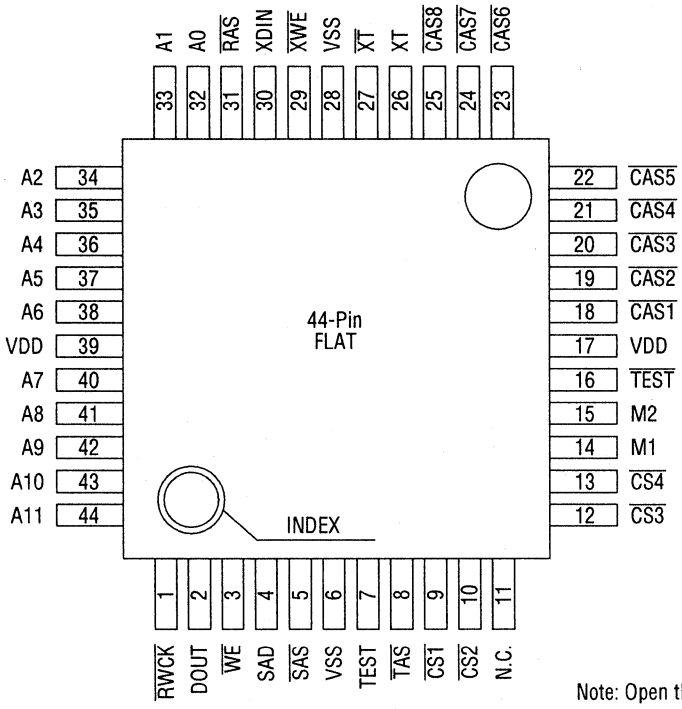
FEATURES

- DRAM (× 1-bit configuration)
  1M-bit DRAM (MSM511000A, MSM511001A) : 8 pcs. can be connected.
  4M-bit DRAM (MSM514100A, MSM514101A) : 8 pcs. can be connected.
  16M-bit DRAM (MSM5116100) : 2 pcs. can be connected.

  Note: MSM511002A/MSM514102A that corresponds to a static column mode can not be used.

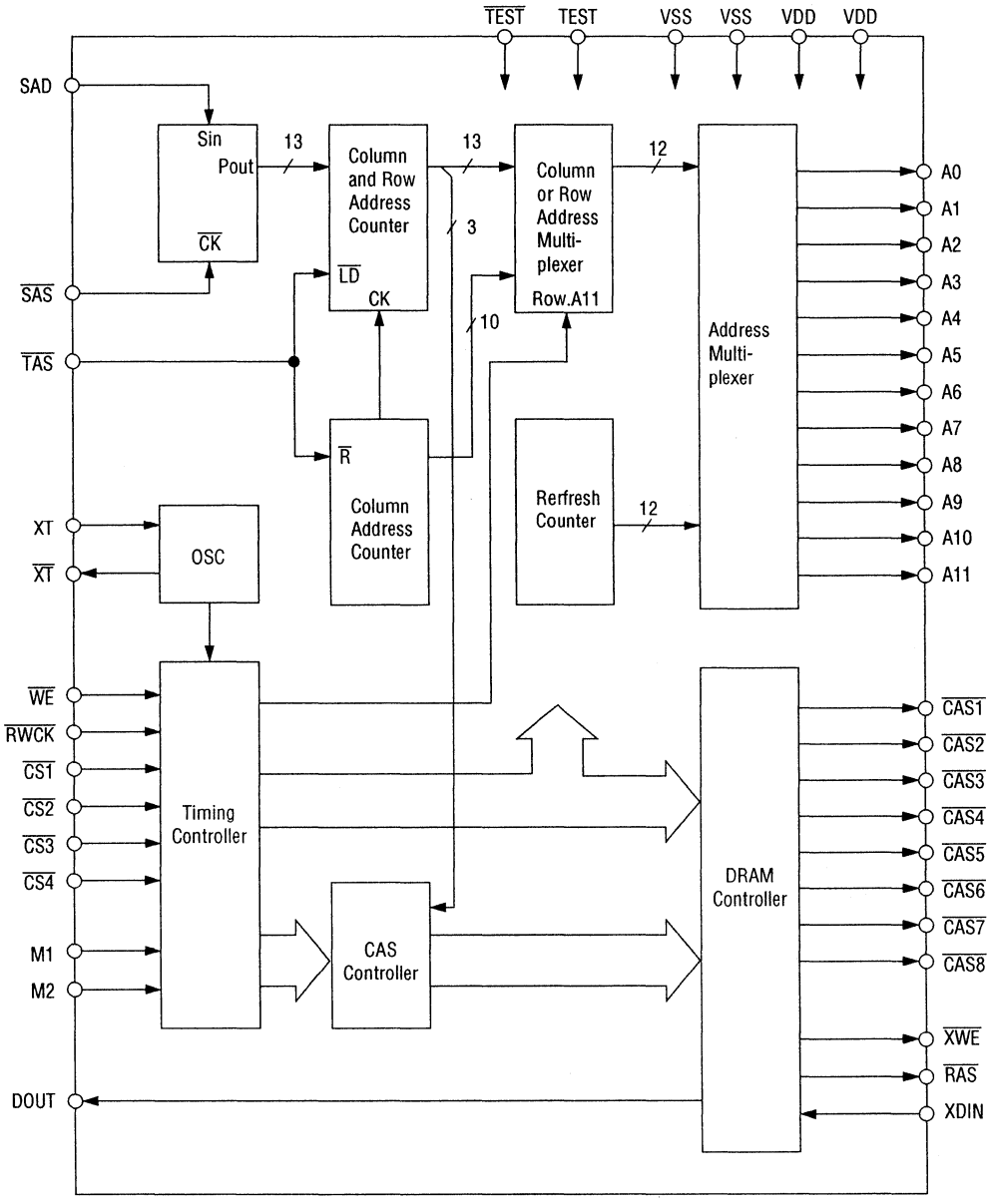
- Power supply voltage: 5V single rail
- Built-in refresh circuit (RAS only refresh)
- Original oscillation frequency: 8MHz
- Bit rates: 10kbps, 12.5kbps, 16kbps in MSM6788 connection (8kHz sampling fixation)
  7.5kbps, 9.4kbps, 12kbps in MSM6788 connection (6kHz sampling fixation)
  16kbps~32kbps in MSM6688 connection (4kHz~8kHz sampling)
- Package: 44-pin plastic QFP (QFP44-P-910-VK)

PIN CONFIGURATION



Note: Open the N.C. pin.

BLOCK DIAGRAM



ELECTORICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	VDD	Ta = 25°C VSS = 0V	−0.5 ~ +7	V
Input voltage	V_I		−0.5 ~ VDD+0.5	V
Output voltage	V_O		−0.5 ~ VDD+0.5	V
Input current	I_I		−10 ~ +10	mA
Output current	I_O		−20 ~ +20	mA
Storage temperature	T_{stg}	—	−65 ~ +150	°C

Operating Conditions

VSS = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	4.5 ~ 5.5	V
Operating temperature	T_{OP}	−40 ~ +85	°C
Oscillation frequency	f_{osc}	8	MHz

DC Characteristics

(Ta = -40~+85°C, VDD = 5V±10% VSS = 0V)

Parameter	Symbol	Conditions	Rating			Unit
			MIN.	TYP.*1	MAX.	
"H" level input voltage	V_{IH}	—	3.5	—	VDD+0.3	V
"L" level input voltage	V_{IL}	—	−0.3	—	1.5	V
"H" level input current	I_{IH}	V_{IH} = VDD	—	0.01	10	μA
"L" level input current	I_{IL}	V_{IL} = VSS	−10	−0.01	—	μA
3-state output leak current (includes open-drain output)	I_{OZH}	V_{OH} = VDD	—	0.01	10	μA
	I_{OZL}	V_{OL} = VSS	−10	−0.01	—	μA
H" level output voltage	V_{OH}	I_{OH} = -5.0 mA	2.4	4.20	VDD	V
"L" level output voltage	V_{OL}	I_{OL} = 5.0 mA	VSS	0.24	0.5	V
Operational current consumption	I_{DD}	Output open f_{osc} = 8MHZ V_{IH} = VDD V_{IL} = VSS	—	—	3	mA

(Note) *1 TYP means VDD = 5.0 V, Ta = 25°C

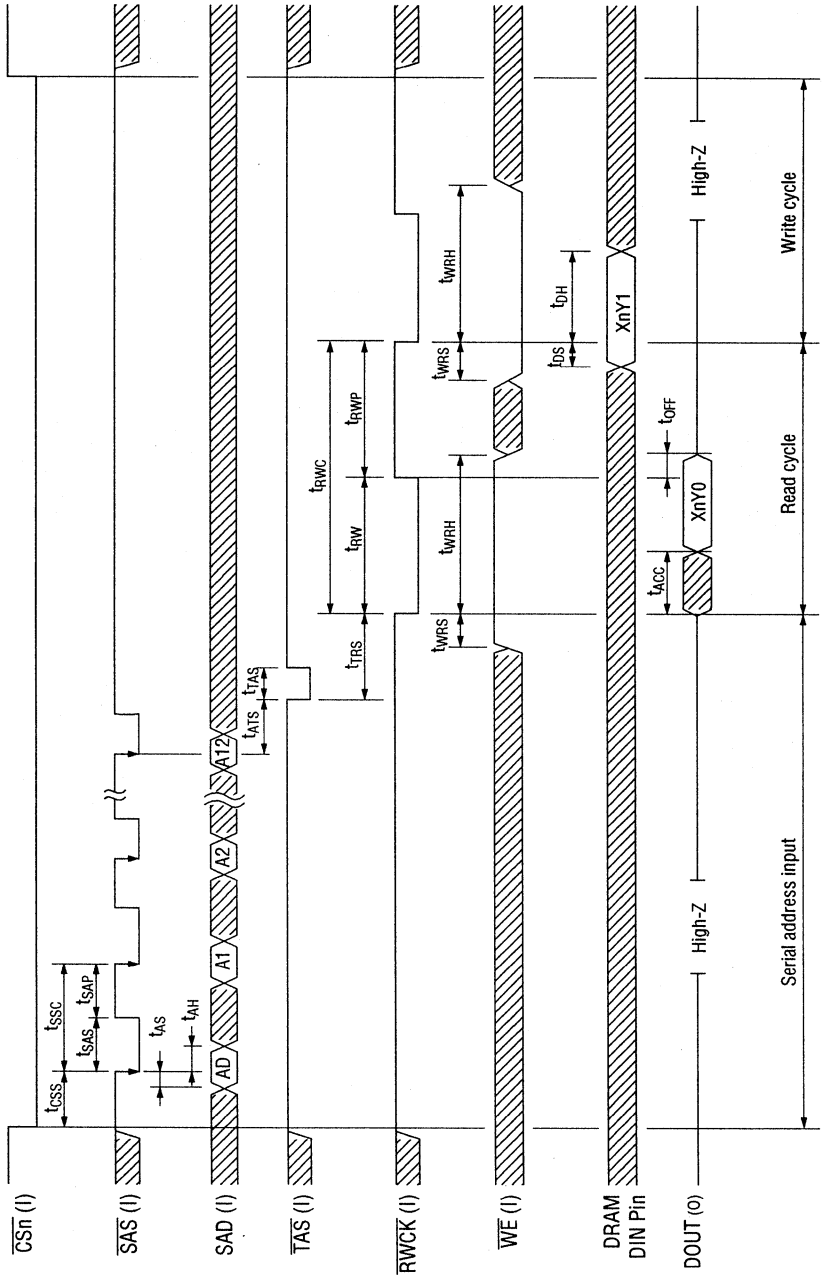
AC Characteristics

(Ta = -40 ~ +85°C, VDD = 5V ± 10%, VSS = 0V)

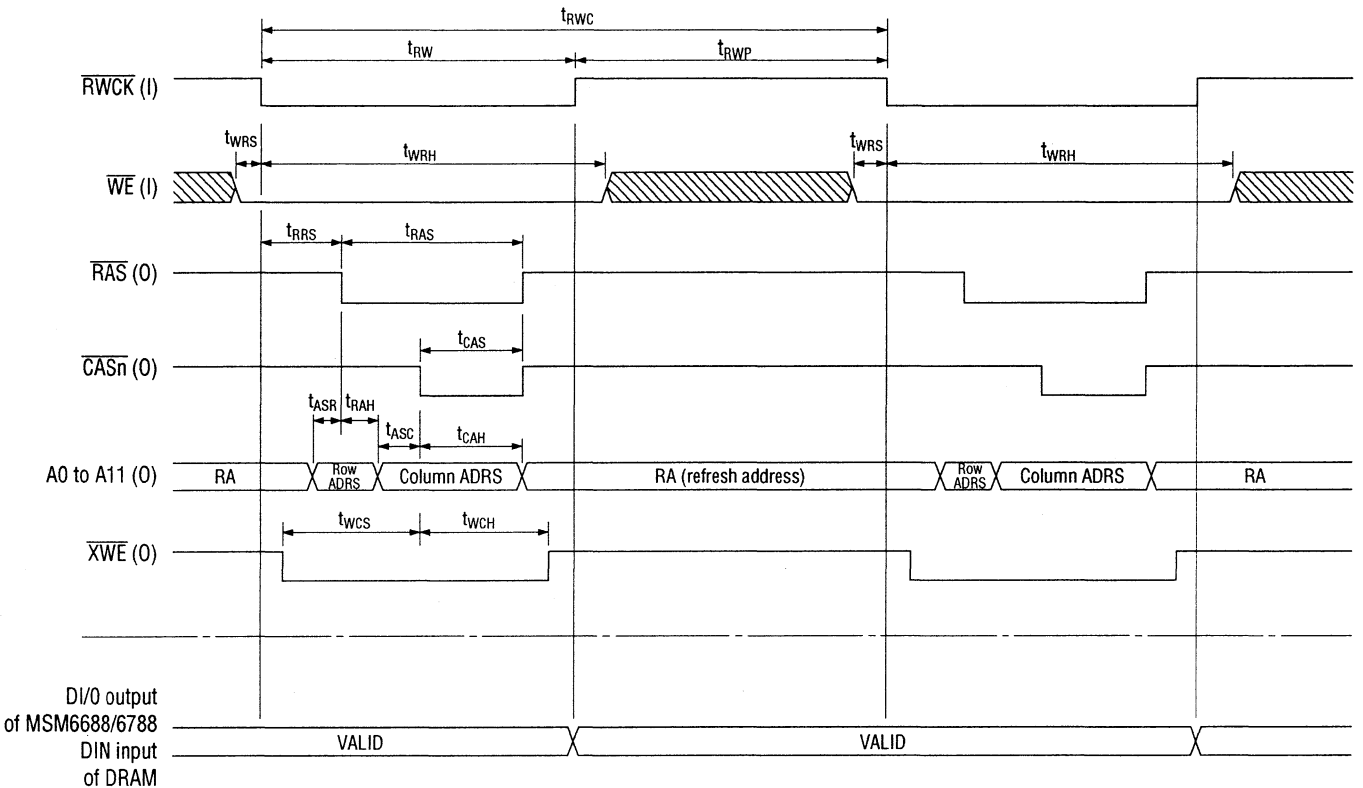
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
$\overline{CS}$•$\overline{SAS}$ setup time	t_{CSS}	1000	–	–	ns
$\overline{SAS}$ cycle time	t_{SSC}	1000	–	–	ns
$\overline{SAS}$ precharge time	t_{SAP}	500	–	–	ns
$\overline{SAS}$ pulse width	t_{SAS}	500	–	–	ns
SAD address setup time	t_{AS}	200	–	–	ns
SAD address hold time	t_{AH}	200	–	–	ns
$\overline{TAS}$ setup time	t_{ATS}	800	–	–	ns
$\overline{TAS}$•$\overline{RWCK}$ setup time	t_{TRS}	800	–	–	ns
$\overline{TAS}$ pulse width	t_{TAS}	400	–	–	ns
Read/ write cycle time	t_{RWC}	1800	–	–	ns
Access time	t_{ACC}	–	–	875	ns
Output turn off time	t_{OFF}	–	–	–	ns
$\overline{RWCK}$ precharge time	t_{RWP}	900	–	–	ns
$\overline{RWCK}$ pulse width	t_{RW}	900	–	–	ns
Read/ write instruction setup time	t_{WRS}	200	–	–	ns
Read/write instruction hold time	t_{WRH}	200	–	–	ns
DRAM•DIN data setup time	t_{DS}	0	–	–	ns
DRAM•DIN data sethold time	t_{DH}	1000	–	–	ns
$\overline{RWCK}$•$\overline{RAS}$ delay time	t_{RRS}	125	–	375	ns
$\overline{RAS}$ pulse width	t_{RAS}	–	750	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	–	500	–	ns
Row address setup time	t_{ASR}	–	125	–	ns
Row address hold time	t_{RAH}	–	125	–	ns
Column address setup time	t_{ASC}	–	125	–	ns
Column address hold time	t_{CAH}	–	500	–	ns
Write instruction setup time	t_{WCS}	–	375	–	ns
Write instruction hold time	t_{WCH}	–	625	–	ns
XDIN data input setup time	t_{DCS}	250	–	–	ns
XDIN data input hold time	t_{DCH}	0	–	–	ns
Refresh cycle time	t_{RRC}	–	8000	–	ns
Refresh $\overline{RAS}$ pulse width	t_{RRAS}	–	1000	–	ns
	t_{RRAS2}	125	–	875	ns
Refresh precharge time	t_{RRP}	–	125	–	ns

TIME CHART

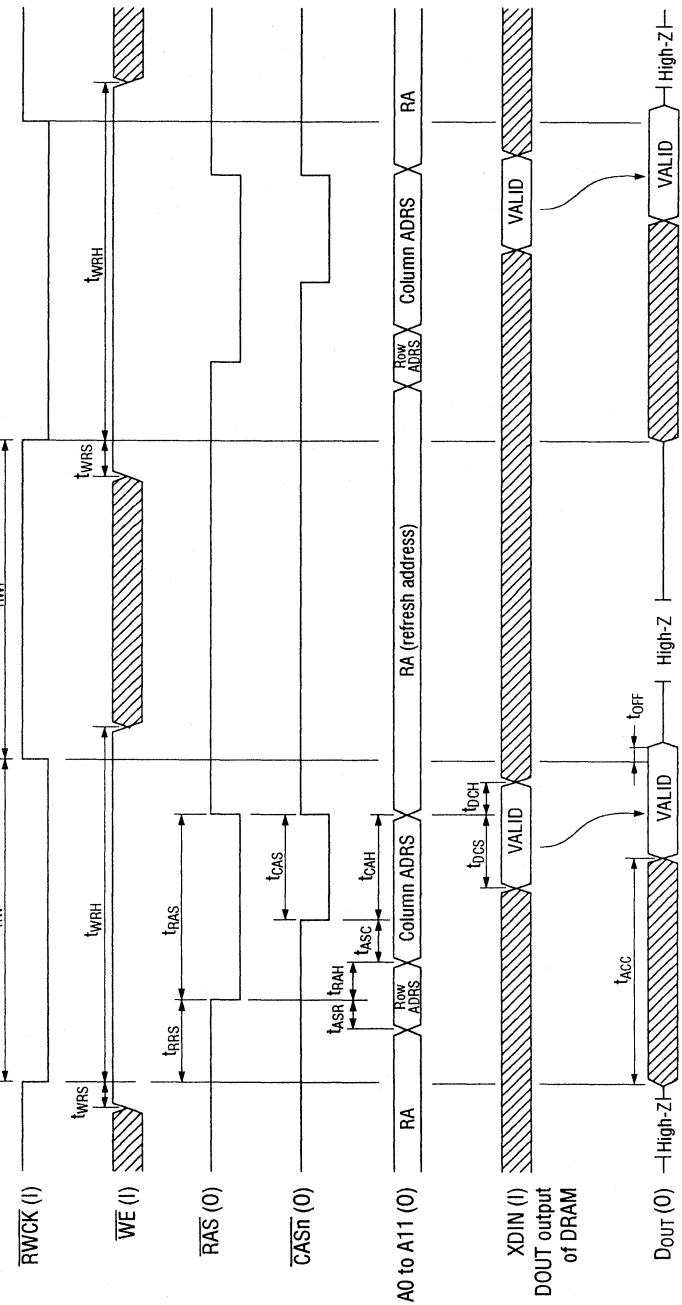
Serial Address Input Timing & Read/Write Cycle



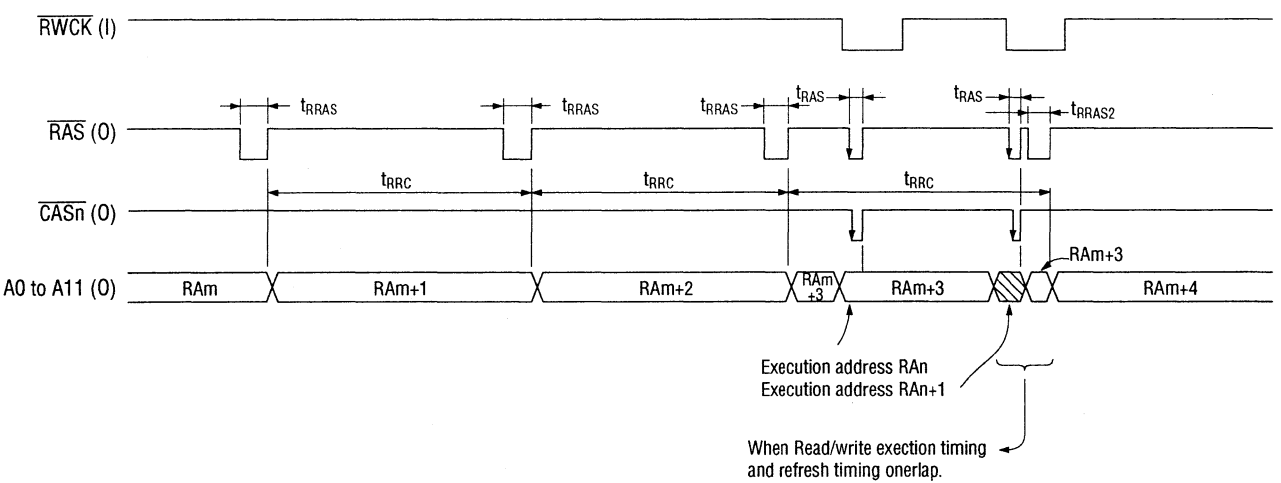
DRAM Drive Timing (Write cycle at recording)



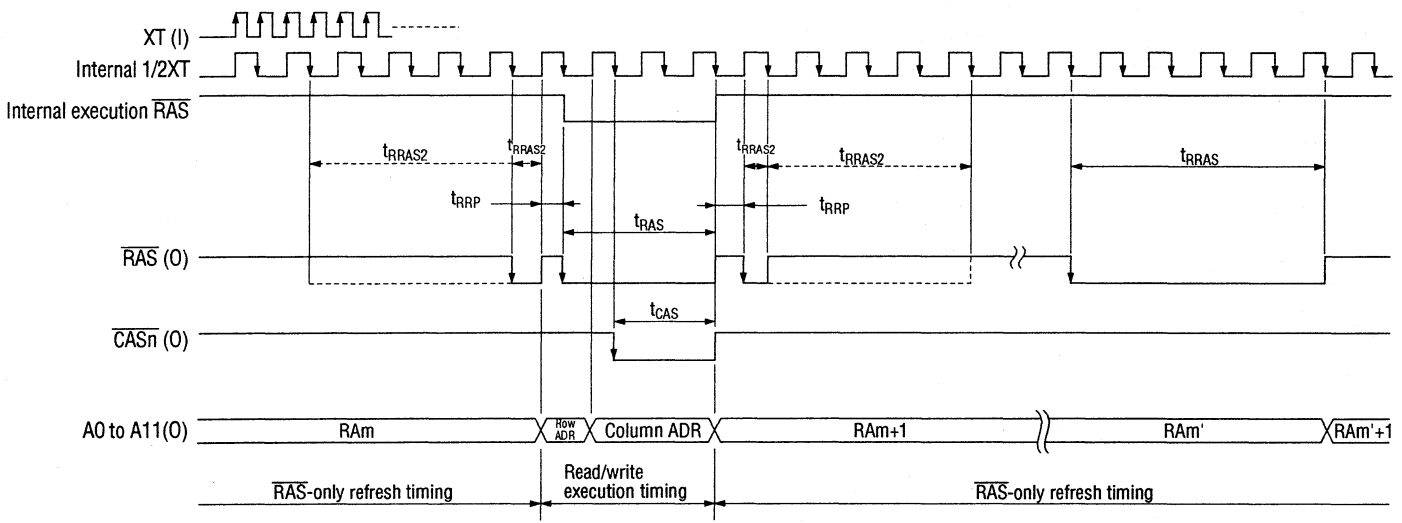
DRAM Drive Timing (Read cycle at playback)



DRAM Drive Timing ($\overline{RAS}$-only refresh cycle)



DRAM Drive Timing (When execution timing and refresh timing overlap)



PIN DESCRIPTION

Pin name	I/O	Pin explanation
VDD	–	Power supply pin
VSS	–	GND pin
XT	I	Oscillator connecting pin
$\overline{XT}$	O	Oscillator connecting pin
TEST	I	Test pin for LSI. Use this pin by setting to 'L' level.
$\overline{TEST}$	I	Test pin for LSI. Use this pin by setting to 'H' level.
SAD	I	Pin to input the read/write head address
$\overline{SAS}$	I	Clock pin to take the serial address data in the internal register.
$\overline{TAS}$	I	Input pin to set the serial address data taken in the address register to the internal address counter
$\overline{RWCK}$	I	Clock input pin to read out and write the information of the data register. The internal operation starts by the fall edge of $\overline{RWCK}$. In a read mode, the data taken in XDIN is latched and it is output to DOUT pin. In a write mode, the DI/O output data of MSM6788 (MSM6688) is taken in the DIN of DRAM. In addition, the internal address counter automatically increments by the fall edge of $\overline{RWCK}$ and the address data output from A0 to A11.
$\overline{WE}$	I	Pin to select a read mode and write mode
$\overline{XWE}$	O	DRAM control pin
A0~A11	O	DRAM address output pin
$\overline{RAS}$	O	DRAM control pin
$\overline{CAS1}$ ~ $\overline{CAS8}$	O	DRAM control pin
XDIN	I	Pin to input the data
DOUT	O	Pin to output the data
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Pin to input the chip select data in connecting DRAM By inputting a "L" level signal to each pin, up to 32M-bit of memory (8M-bit of memory for each pin) can be controlled for 4 pins. These pins become the input pins to select the highest address in 16M-bit DRAM connection.
M1 M2	I	Input pin to set the connecting pattern of DRAM.

Connecting mode	M2	M1	DRAM connecting pattern
Mode 0	L	L	1M-bit DRAM × 1~8pcs. connectable
Mode 1	L	H	4M-bit DRAM × 1~8pcs. connectable
Mode 2	H	L	(4M-bit DRAM × 1pcs.) + (1M-bit DRAM × 0~3pcs.) connectable
Mode 3	H	H	16M-bit DRAM × 1~2pcs. connectable

FUNCTIONAL DESCRIPTION

The relations between $\overline{CSn}$ and $\overline{CASn}$ in MSM6791 by connection mode are listed below.

Connection mode 0

M1 = M2 = "L", $\overline{CS2}$ ~ $\overline{CS4}$ = "H"

Chip Select pin of MSM6791. Connection to MSM6788/6688 is made via this pin.	Connection to $\overline{CAS}$ pin of 1M-bit DRAM is made via this pin.
$\overline{CS1}$	$\overline{CAS1}$ ~ $\overline{CAS8}$

Connection mode 1

M1 = "H", M2 = "L"

Chip Select pin of MSM6791. Connection to $\overline{CSn}$ MSM6788/ 6688 is made via this pin.	Connection to $\overline{CAS}$ pin of 4M-bit DRAM is made via this pin.	
$\overline{CS1}$	$\overline{CAS1}$	$\overline{CAS2}$
$\overline{CS2}$ *1	$\overline{CAS3}$	$\overline{CAS4}$
$\overline{CS3}$ *1	$\overline{CAS5}$	$\overline{CAS6}$
$\overline{CS4}$ *1	$\overline{CAS7}$	$\overline{CAS8}$

Connection mode 2

M1 = "L", M2 = "H", $\overline{CS2}$ ~ $\overline{CS4}$ = "H"

Chip Select pin of MSM6791. Connection to MSM6788/6688 is made via this pin.	Connection to $\overline{CAS}$ of 4M/ 1M-bit DRAM is made via this pin
$\overline{CS1}$	To CAS of 4M-bit DRAM $\overline{CAS1}$
	To CAS of 1M-bit DARM $\overline{CAS2}$
	To CAS of 1M-bit DARM $\overline{CAS3}$
	To CAS of 1M-bit DARM $\overline{CAS4}$

Connection mode 4

M1 = M2 = "H"

Chip Select pin of MSM6791. Connection to MSM6788/6688 is made via this pin.	Connection to $\overline{CAS}$ of 16M-bit DRAM is made via this pin.
$\overline{CS1}$	$\overline{CAS1}$
$\overline{CS2}$	
$\overline{CS3}$ *1	$\overline{CAS2}$
$\overline{CS4}$ *1	

*1) In the connection mode 1 and connection mode 3, some input pin may be needless depending on the number of DRAMs conneced. At this time, the unused pin should at "H" level.

Example) In the connection mode 1, when 1 to 2 4Mbit DRAMs are connected, unused input pins should be treated as shown below.

$\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$: "H" level

OSCILLATOR OF MSM6791

Refer to the following circuit on the oscillator of MSM6791.

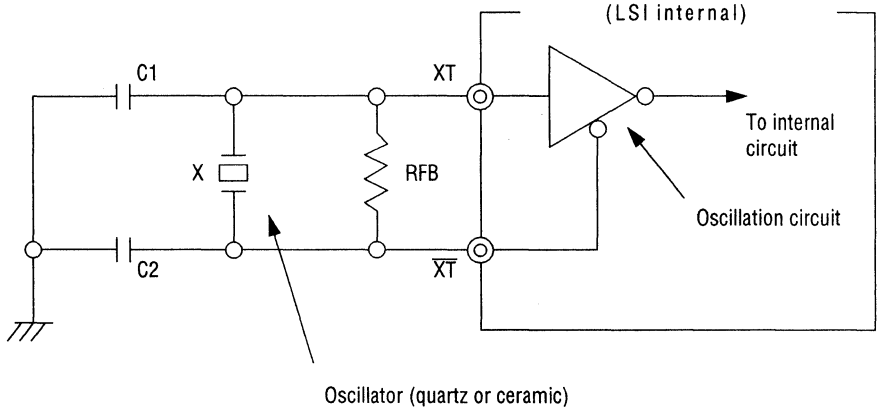


Figure 1. Quarty/Ceramic Oscillation Circuit

Maker	Oscillation frequency	Oscillator (X)	Type	C1=C2	RFB
Kyocera	8MHz	Ceramic	KBR-8.0M	33pF	1MΩ
Kyocera		Ceramic (chip type)	KBR-8.0MWS	— *2	
Murata		Ceramic	CSA8.00MTZ	30pF	
Murata		Ceramic (chip type)	CSA8.00MTW	— *2	

*2) KBR-8.0MWS and CSA8.00MTW include C1 and C2.

The configuration and resistance value of the oscillation circuit and the value of the capacitor differs depending on the oscillation frequency and the oscillator used.
When using an oscillator circuit, evaluate the characteristics according to the actual conditions of use. Determine the circuit configuration and the circuit constants.

APPLICATION CIRCUIT EXAMPLES

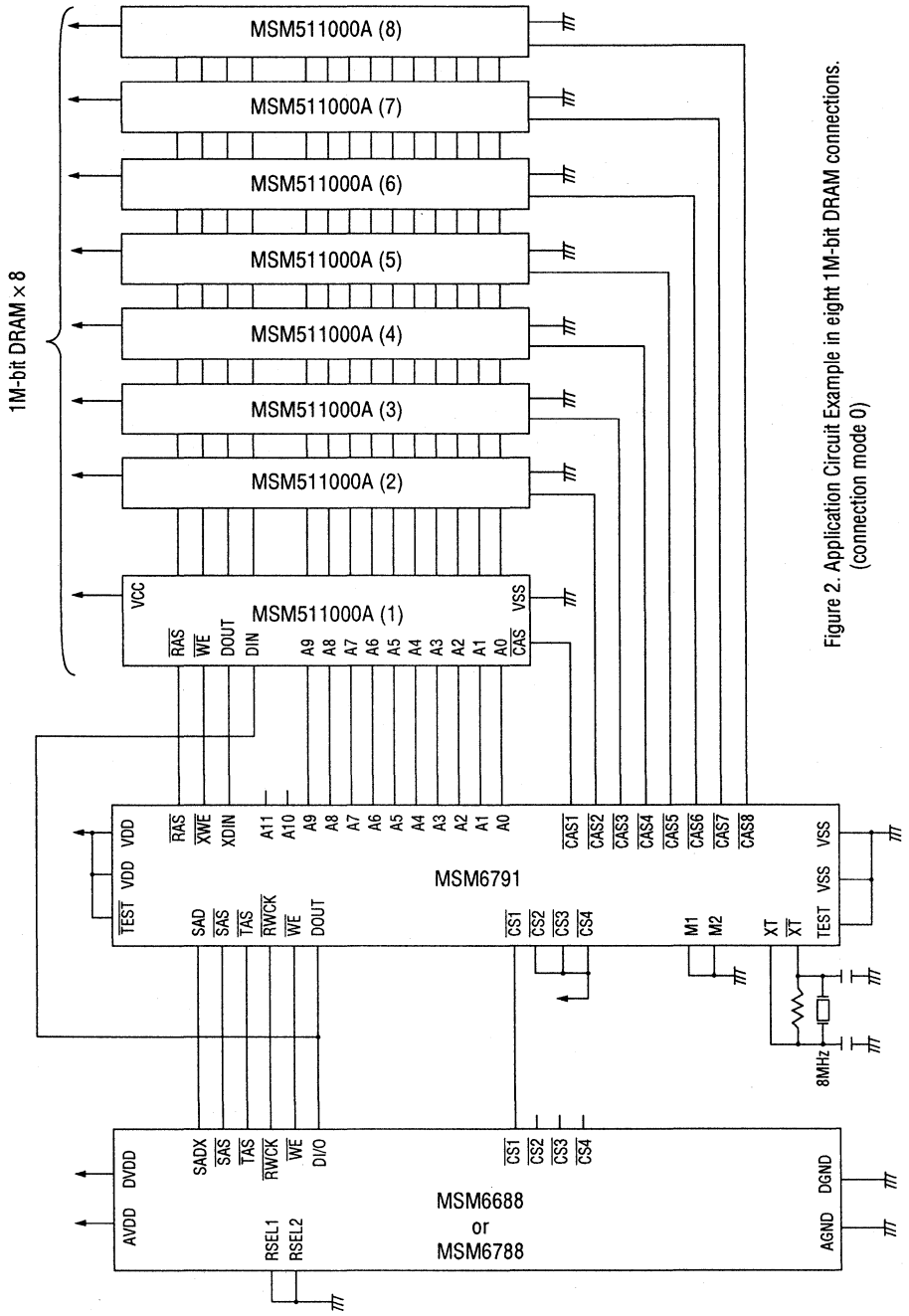


Figure 2. Application Circuit Example in eight 1M-bit DRAM connections. (connection mode 0)

APPLICATION CIRCUIT EXAMPLES

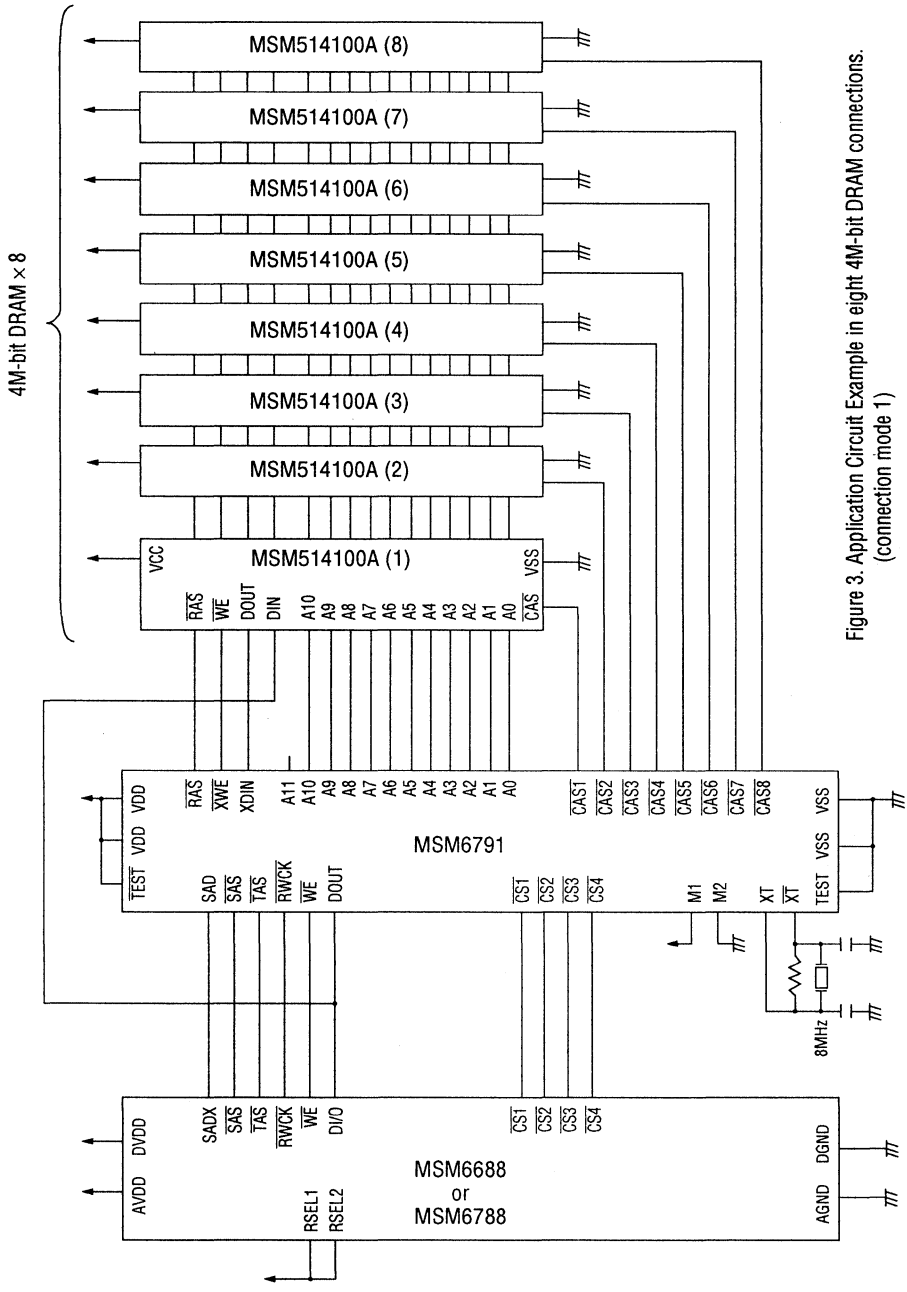


Figure 3. Application Circuit Example in eight 4M-bit DRAM connections. (connection mode 1)

APPLICATION CIRCUIT EXAMPLES

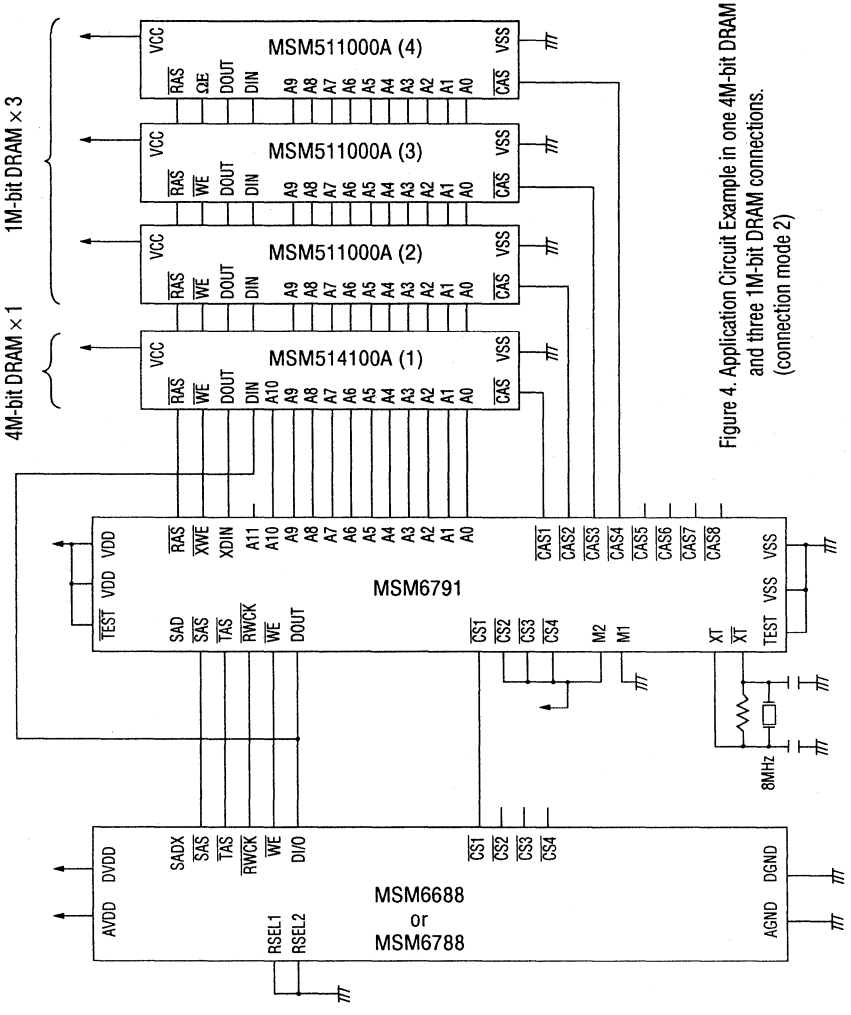


Figure 4. Application Circuit Example in one 4M-bit DRAM and three 1M-bit DRAM connections. (connection mode 2)

APPLICATION CIRCUIT EXAMPLES

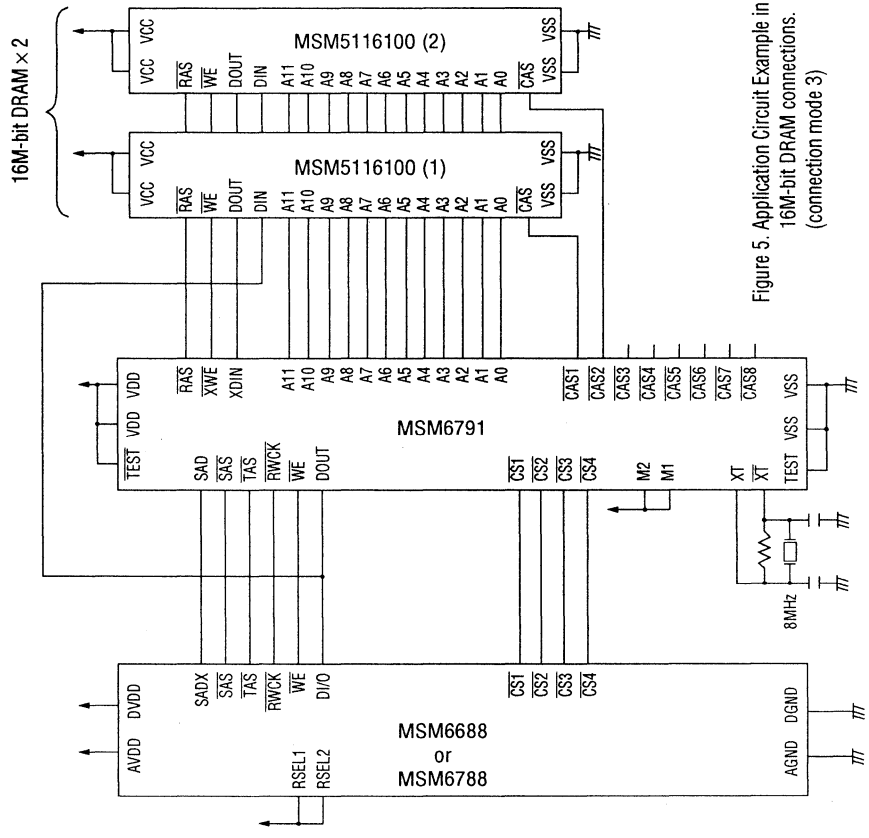


Figure 5. Application Circuit Example in two 16M-bit DRAM connections. (connection mode 3)

APPLICATION CIRCUIT EXAMPLES

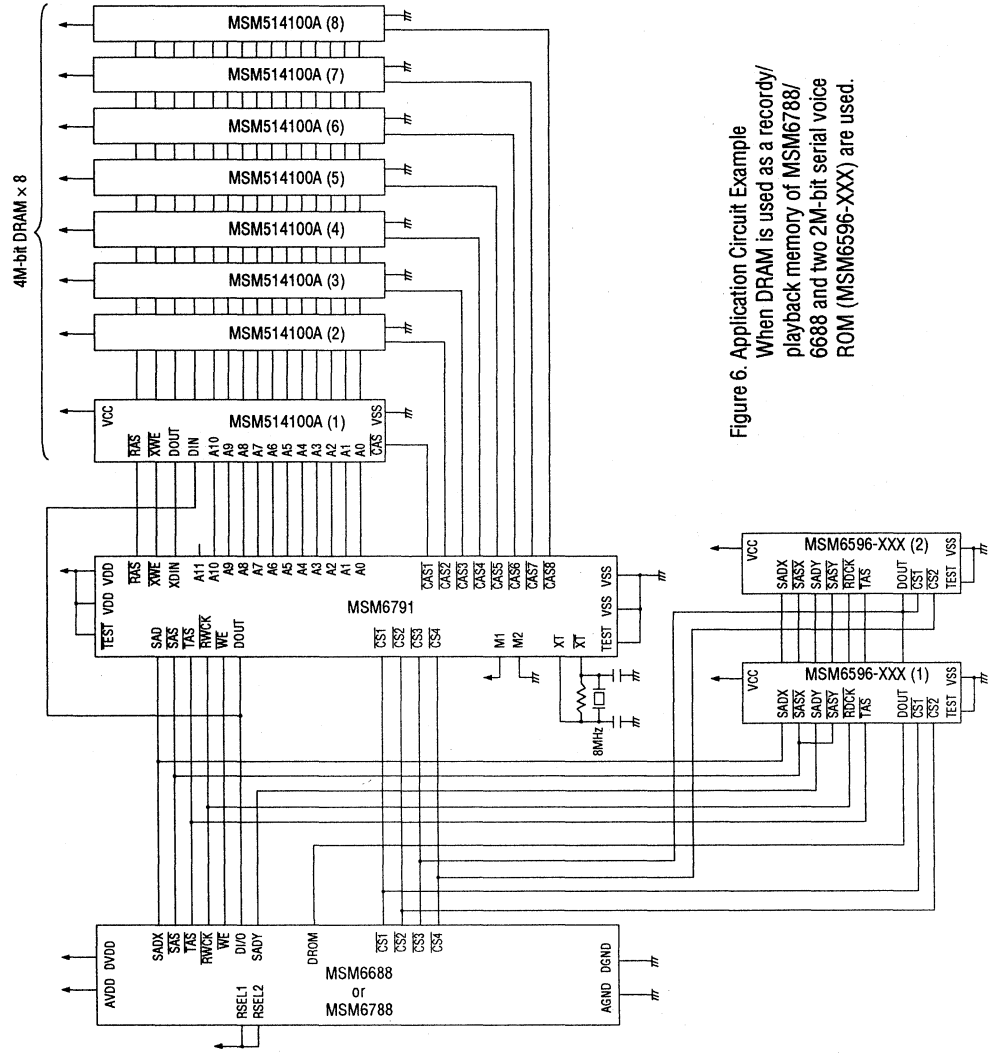


Figure 6. Application Circuit Example
When DRAM is used as a recordy/playback memory of MSM6788/6688 and two 2M-bit serial voice ROM (MSM6596-XXX) are used.

Pitch Control

OKI Semiconductor

MSM6322

PITCH CONTROL LSI FOR THE SPEECH SIGNAL

GENERAL DESCRIPTION

The MSM6322 converts in realtime the pitch of the speech signal in a range of one octave upward or downward.

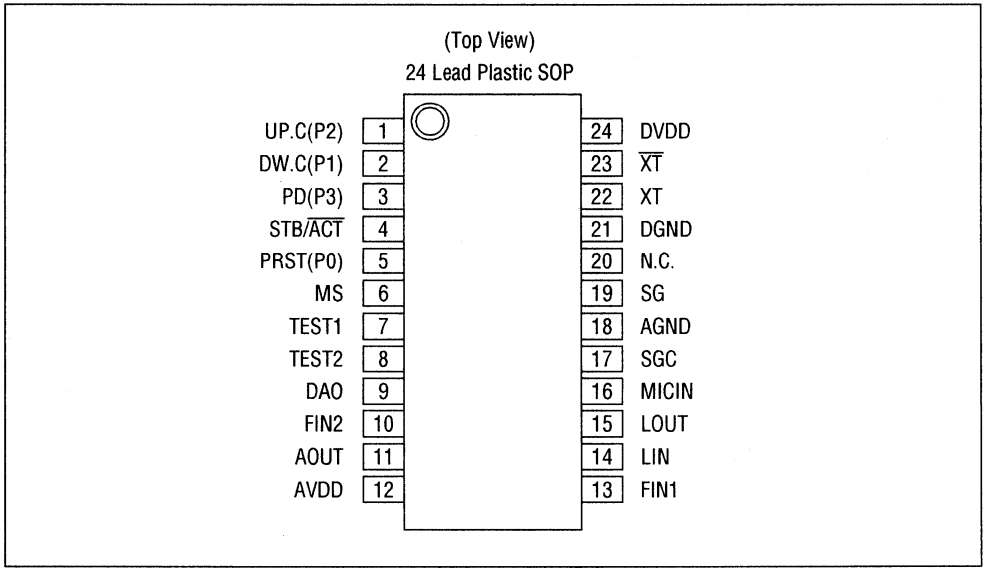
Two pitch control methods can be selected. One is to change the pitch in 17 steps by two switch inputs, and the other is to select one of 16 steps by four binary input lines.

Since a microphone preamplifier and a low pass filter are built in, the pitch conversion set can easily be configured by connecting a microphone, amplifier and speaker in the peripheral circuit.

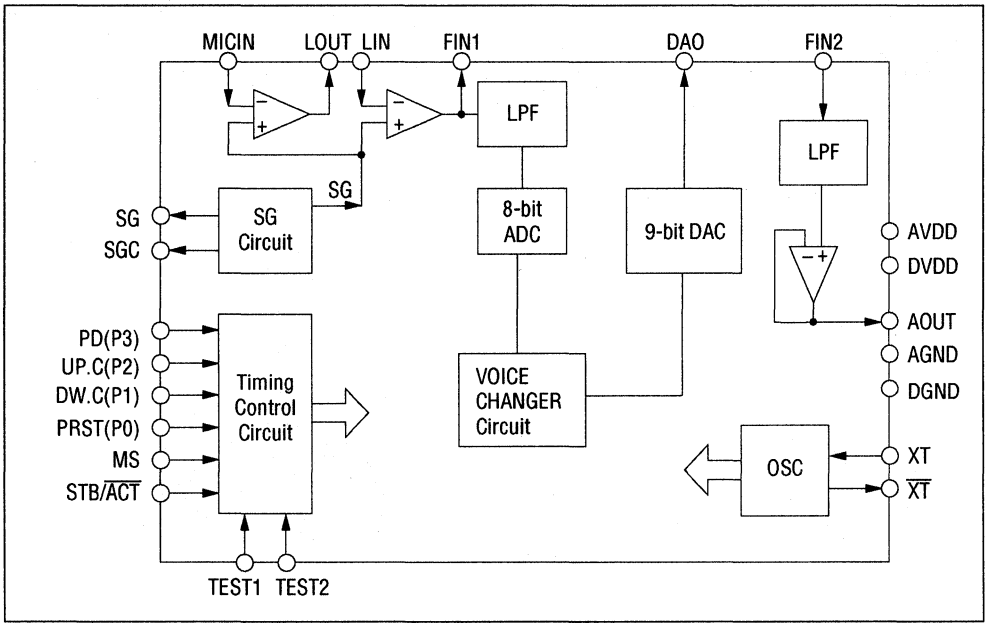
FEATURES

- Built-in microphone preamplifier
- Built-in low pass filters (4th order LPF on input and 3rd order LPF on output)
- Built-in 8-bit AD converter
- Built-in 9-bit DA converter
- Speech pitch alterable in 17 steps
- Oscillation frequency at 4 MHz
- 5V single power supply
- Silicon construction (Si gate CMOS IC)
  Note) Designed for application to home electronic equipment (toys).
- 24-pin plastic SOP
  (SOP24-P-430-K)

PIN ASSIGNMENT



CIRCUIT CONFIGURATION



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage (1)	DVDD	For DGND and AGND Ta = 25°C	−0.3 ~ +7.0	V
Supply voltage (2)	AVDD		−0.3 ~ +7.0	V
Analog input voltage	V_{IN} (ANALOG)		AGND −0.3 ~ AVDD +0.3	V
Digital input voitage	V_{IN} (DIGITAL)		DGND −0.3 ~ AVDD +0.3	V
Storage temperature range	T_{stg}	—	−55 ~ +150	°C

• Operating Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage (1)	DVDD	For DGND	4.0 ~ 6.0	V
Supply voltage (2)	AVDD	For AGND	4.0 ~ 6.0	V
Rated operating temperature range	Top	–	−40 ~ 85	°C

• DC Characteristics

(Ta = -40~+85°C, F_{OSC} = 4MHz, DVDD = AVDD = 4.5V~5.5V, DGND = AGND = 0V)

Parameter		Symbol	Conditions	Limits			Unit
				Min.	Typ.	Max.	
"H" input voltage (excluding XT and RST)		$V_{IH}(1)$	–	3.6	–	–	V
"H" input voltage (applicable to XT and RST)		$V_{IH}(2)$	–	0.8 × VDD	–	–	V
"L" input voltage		V_{IL}	–	–	–	0.8	V
"H" input current for match 3, 4, 6, 22, 23 pin		I_{IH1}	V_{IH} = DVDD	–	–	10	μA
"H" input current for match 1, 2, 5, 7, 8 pin		I_{IH2}	V_{IH} = DVDD	–	–	400	μA
"L" output current		I_{IL}	V_{IL} = DGND	−10	–	–	μA
Output impedance	LOUT	RO_{LOUT}	–	–	15	–	kΩ
Output impedance	DAO	RO_{DAO}	–	–	10	–	kΩ
	AOUT	RO_{AOUT}	–	–	15	–	kΩ
	FIN1	RO_{FIN1}	–	–	15	–	kΩ
Input impedance	MICIN	RI_{MICIN}	–	–	100	–	MΩ
	LIN	RI_{LIN}	–	–	100	–	MΩ
	FIN2	RI_{FIN2}	–	–	30	–	MΩ
AD conversion precision		$\|V_{ADE}\|$	AVDD = DVDD = 5V	–	–	40	mV
DA conversion precision		$\|V_{DAE}\|$	AVDD = DVDD = 5V No load	–	–	40	mV
Operating current consumption		I_{DD}	In case of 4 MHz oscillator	–	–	10	mA
Standby current		I_{DS}	In case of 4 MHz oscillator with STB/$\overline{ACT}$ = "H"	–	–	7	mA
Power down current		I_{DP}	In case of PD = "H"	–	–	10	μA

• AC Characteristics

(Ta = −40~85°C, F_{OSC} = 4MHz, DVDD = AVDD = 4.5V~5.5V, DGND = AGND = 0V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
DAO output delay from falling edge of STB/$\overline{ACT}$	t_{CSD}	–	–	15.36	ms
DAO output delay from falling edge of PD	t_{PDD}	–	–	15.36	ms
Pulse width of PRST, UP.C, DW.C pulses	t_{UDPW}	–	61.44	–	ms
Time between UP.C, and DW.C pulses	t_{RUD}	–	30.72	–	ms
Scale change delay from positive edge of PRST	t_{CHG1}	–	61.44	–	ms
Scale change delay from falling edge of UP.C and DW.C	t_{CHG2}	–	–	15.36	ms
Maximum operating frequency	t_{CMAX}	–	–	4.5	MHz

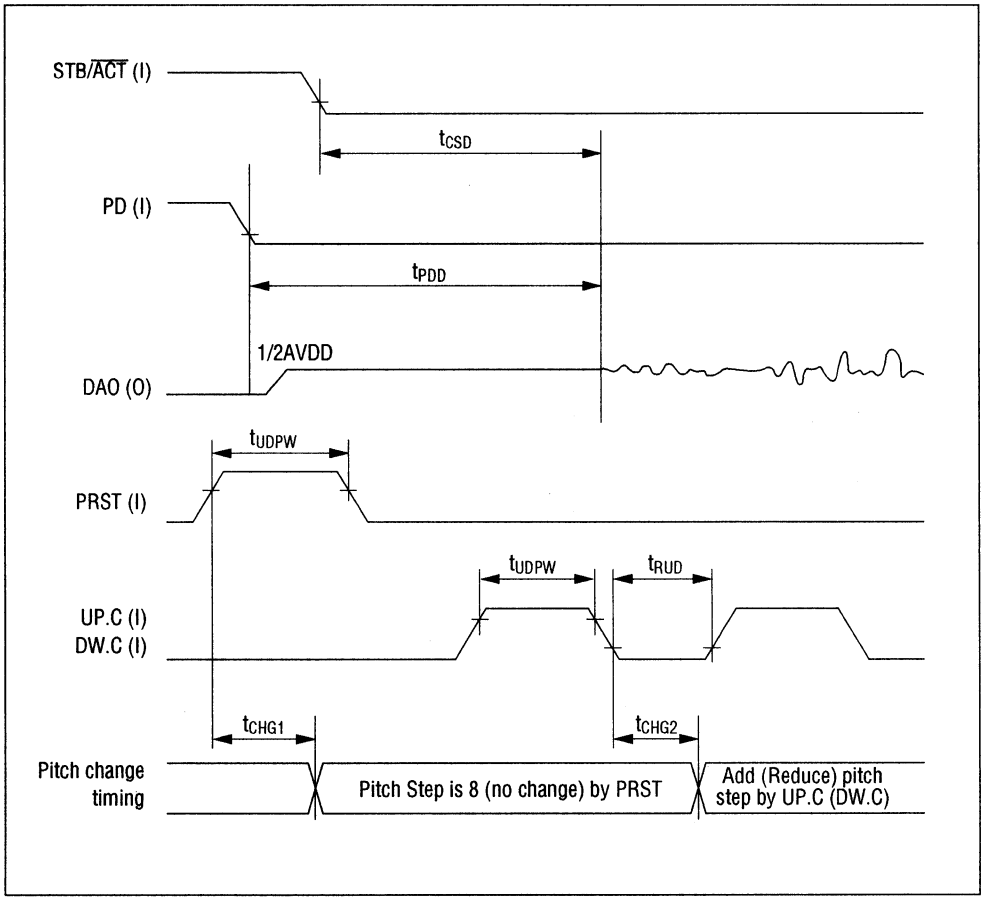
• LPF Characteristics

(Ta = 25°C, AVDD = DVDD = 4.5V~5.5V,,
DGND = AGND = 0V)

Frequency (Hz)	Gain characteristic (dB)		
	Min.	Typ.	Max.
300 ~ fc	−3.0	–	3.0
fc	–	−3.0	–
2 × fc	–	–	−20.0

See the pitch conversion Table

TIMING DIAGRAM



• **PIN FUNCTION** (Setting method = "UP/DOWN") [MS pin fixed to "L"]

Pin Name	I/O	Function
MS	I	Mode select pin always connected to the "L" level.
MICIN	I	Connects the microphone input via a coupling capacitor.
LOUT	O	Output obtained by amplifying the audio signal input from the microphone.
LIN	I	Input pin for connecting the LOUT output or line out signal from other audio equipment.
FIN1	O	Sets the input audio signal amplitude in combination with the LIN pin. The gain of the built-in amplifier can be set by two pins each of MICIN and LOUT, and LIN and FIN1.
UP.C	I	Pulse switch input to raise the pitch by one stage at a time.
DW.C	I	Pulse switch input to lower the pitch by one stage at a time. The pitch varies by one stage upward (or downward) each time a pulse is input to the UP.C (or DW.C) pin along the 17 stages shown in the pitch conversion table. Cyclic up or down operation is also possible.
STB/$\overline{\text{ACT}}$	I	Standby/$\overline{\text{active}}$ pin. When the standby/$\overline{\text{active}}$ is at the "H" level, the processing is interrrupted by stopping only the clocks other than the oscillator clock. The DAO pin outputs 1/2 VDD for about 15ms (in case of 4MHz oscillator) after the standby/$\overline{\text{active}}$ goes to the "L" level.
PD	I	Power down pin. All clocks including the oscillator are stopped when the power down pin is set to the "H" level. The DAO pin outputs the "L" level in this state. It requires ten milliseconds after the power down pin is set to the "L" level until clock stabilization.
PRST	I	Reset pin to connect the pulse switch input to set the scale to stage 8 upon resetting.
TEST1 TEST2	I	Test pins to be fixed to the "L" level.
XT, $\overline{\text{XT}}$	I, O	Crystal oscillator connecting pins
SG,SGC	I	Reference voltage pins.
DAO	O	DA converter output.
FIN2	I	Input pin for built-in filter (for output).
AOUT	O	Output pin for built-in filter (for output).
DGND DVDD	—	Power supply pins.
AGND AVDD	—	Analog power supply pins.

• **PIN FUNCTION** (Setting method = "BIN") [MS pin fixed to "H"]

Pin Name	I/O	Function
MS	I	Mode select pin always connected to the "H" level.
MICIN	I	Pin for connecting the microphone input via a coupling capacitor.
LOUT	O	Output obtained by amplifying the audio signal input from the microphone.
LIN	I	Input pin for connecting the LOUT output or line out signal from other audio equipment.
FIN1	O	Sets the input audio signal amplitude in combination with the LIN pin. The gain of the built-in amplifier can be set by two pins each of MICIN and LOUT, and LIN and FIN1.
P3 P2 P1 P0	I	16 stages are set by 4-bit of P3 (MSB) to P0 (LSB). Stages 0 (p3=p2=p1=p0=0) to 16 (P3=P2=P1=P0=1) shown on the pitch conversion table can be set.
STB/$\overline{ACT}$	I	Chip select pin. The processing is interrupted by stopping clocks other then the oscillator when the chip select pin level "H". The DAO outputs 1/2 VDD for about 15ms (in case of 4 MHz oscillator) after the chip select pin is set to the "L" level.
TEST1 TEST2	I	Test pins to be fixed to the "L" level.
XT, $\overline{XT}$	I, O	Crystal oscillator connecting pins.
SG,SGC	I	Reference voltage input pins.
DAO	O	DA converter output pin.
FIN2	I	Input pin for built-in filter (for output).
AOUT	O	Output pin for built-in filter (for output).
DGND DVDD	—	Power supply pins.
AGND AVDD	—	Analog power supply pins.

FUNCTIONAL EXPLANATION

- **Analog Input/output (MICIN, LOUT, LIN and FIN1)**

These pins are to connect microphone or other audio equipment line inputs and to set the input gain. Fig.1 shows the basic circuit. Amplifier 1, and the LIN and FIN1 pins are connected to the input and output of amplifier 2.

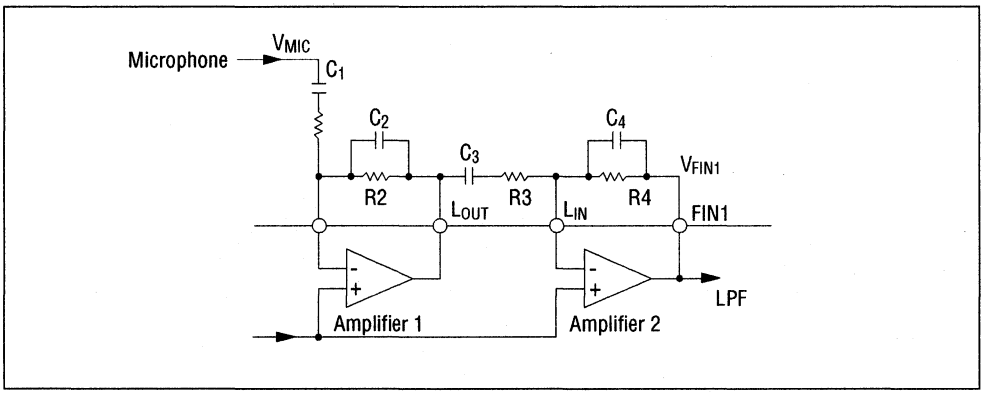


Figure 1 Analog Input Block

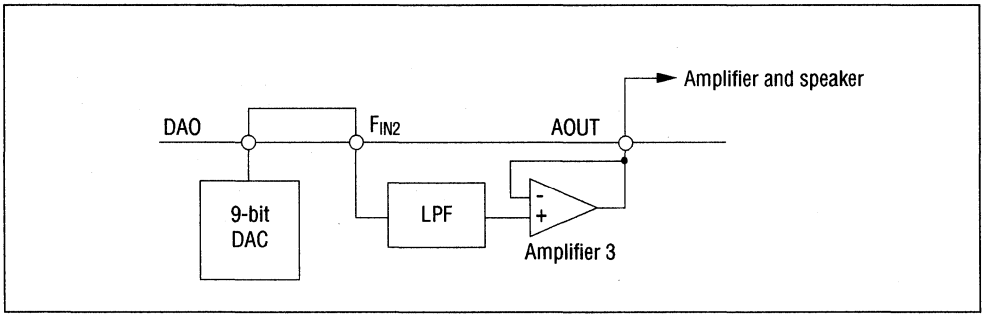


Figure 2 Analog Output Block

The output of amplifier 2 is also connected to the LPF (low pass filter) configured by the SCF (switched capacitance filter).

For input from the microphone, DC cutoff of the microphone input is carried out by capacitor C1 (approx. 1μF), (1/2 AVDD becomes the center internally.)

The amplitude (generally ten millivolts) of the microphone input is amplified by R1 and R2 (to $V_{LOUT} = (R2/R1)*V_{MIN}$). Similarly, the DC component of the LOUT output is cut off by capacitor C3 (approx. 1μF), and the resultant signal is amplified by R3 and R4 (to $V_{FIN1} = (R4/R3)*V_{LOUT}$).

Capacitors C2 and C4 are to prevent oscillation of the internal amplifier. 20 to 50pF is used.

When considering connection of other audio equipment, it is recommended to suppress the maximum amplitude at the LOUT pin to within 500mV. The maximum amplitude shall be suppressed to within 5V (AVDD - AGND voltage width) by the FIN1 pin.

- **Analog Output (DAO, FIN2 and AOUT)**

The output signal after scale conversion is output through the 9-bit DAC (digital-analog converter) to the DAO pin. The maximum amplitude of this signal is ±2.5V with 1/2 AVDD as the reference voltage. The DAO signal again goes through the internal LPF using SCF to amplifier 3 for impedance conversion, and the resultant signal is output from the AOUT pin.

It is possible to insert an external filter or equalizer between the DAO and FIN2 pins.

- **Analog Reference Voltage (SG and SGC)**

The SG and SGC pins are to connect external capacitors for stabilizing the internal analog reference voltage of 1/2 AVDD.

Connect respective these pins to the ground through capacitor C5 or C6 as shown in Fig. 3.

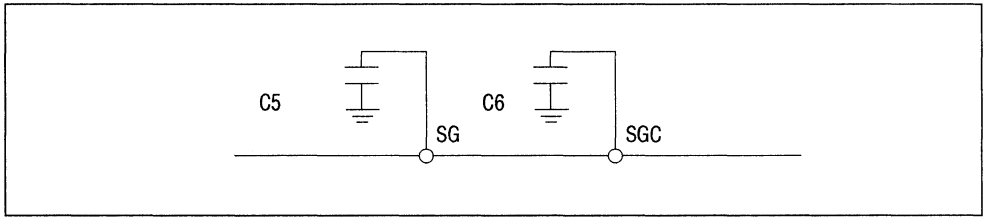


Figure 3 Analog Reference Voltage Block

- **Pitch-control Circuit**

[BIN mode] (P3, P2, P1 and P0)

As shown in Fig. 4, this LSI has an internal 46ms chattering prevention circuit. P2 to P0 are internally terminated by over 10kΩ resistors.

16 pitch stages are provided however the 16th stage cannot be set.

[UP/DOWN mode] (UP.C, DW.C and PRST)

As shown in Fig. 4, this LSI has internal 46ms chattering prevention circuit.

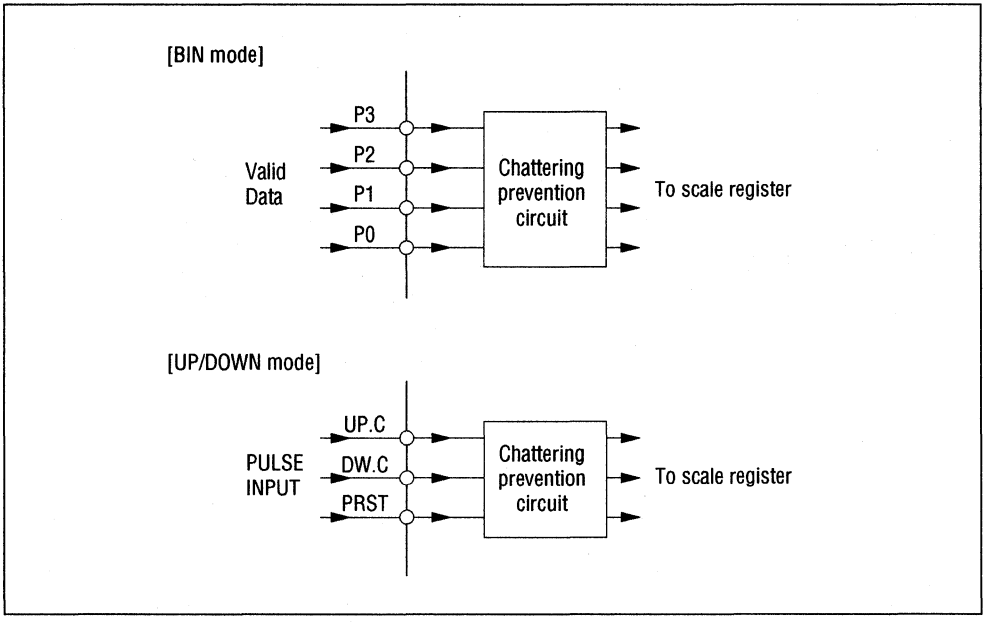


Figure 4 Scale Control Circuit

A high input to the UP.C pin raises the scale by one stage, and inputting one pulse to the DW.C pin lowers the scale by one stage. One pulse input to the PRST pin sets the no scale conversion state (scale stage 8).

Since the scale stage change functions cyclically, change from scale stage 0 to 16 or 16 to 0 occurs. The UP.C, DW.C and PRST pins are terminated by over 10kΩ resistors. The tone scale stage is undefined after power on. First of all, use the circuit at the state of changeless tone scale by using the PRST.

- **System Control Circuit**

[BIN mode] (STB/$\overline{ACT}$)

The STB/$\overline{ACT}$ signal is the power control signal not affecting the scale.

When the STB/$\overline{ACT}$ goes to the "H" level, any scale stage control signal input is ignored.

The DAO pin, however, outputs 1/2 AVDD if the STB/$\overline{ACT}$ is "H", or outputs the AGND irrelevant to the STB/$\overline{ACT}$ state if the PD is "H".

Since the oscillation circuit is instable for ten milliseconds after power on or the falling edge of the PD, it is recommended to set the STB/$\overline{ACT}$ to "H" in this period and make the STB/$\overline{ACT}$ fall after the stabilization of the oscillator to minimize abnormal output after power on or the fall of the PD.

Such an abnormal output, however, can hardly be distinguished from pop noise.

- **Oscillation circuit (XT and $\overline{XT}$)**

Since the feedback resistor and amplifier are provided internally, the oscillation circuit can be realized by connecting only a crystal or ceramic oscillator and oscillation stabilizing capacitors (C7 and C8) externally. It is recommended to use C7 = C8 = 30pF for Murata's ceramic oscillator CSA4.00MG, CST4.00MGW, 4.19 MHz OR 4.5MHz, or use C7 = C8 = 33pF for Kyocera's ceramic oscillator KBR-4.0MS.

Fig. 5 shows the circuit example. To use the external clock, input it to the XT pin and leave the $\overline{XT}$ pin open.

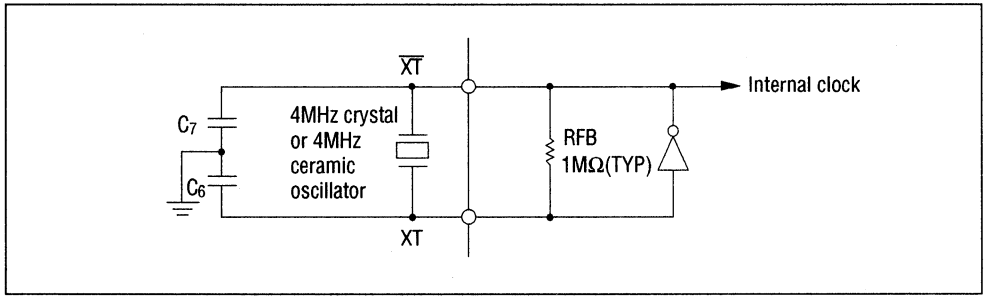
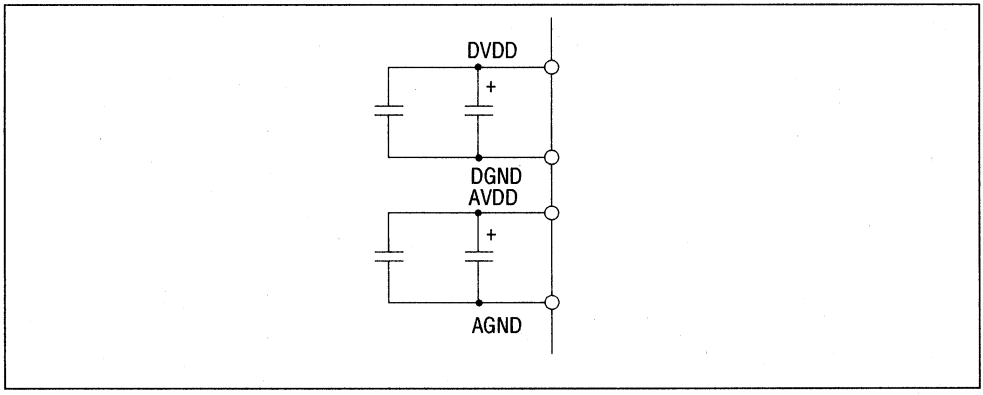


Figure 5 Oscillation Circuit

- **Power Supply Circuit (DVDD/DGND, AVDD and AGND)**

To prevent the power noise from entering the analog circuit, insert a capacitor of about 10μF each between AVDD and AGND and between DVDD and DGND to obtain a stable level without power noise.

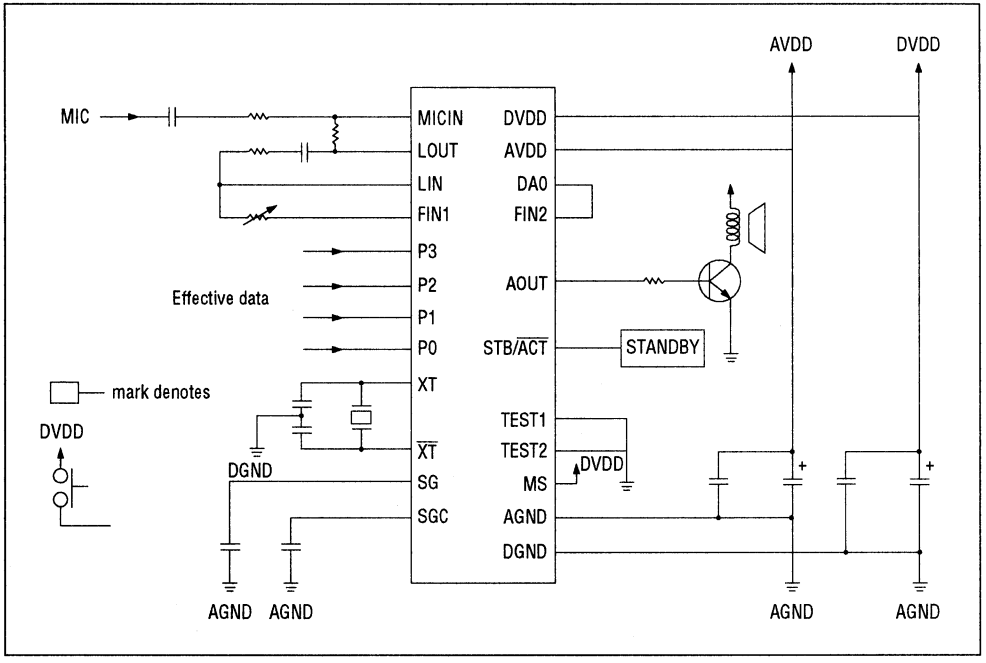
Be sure that the capacity between AVDD and AGND equals the capacity between DVDD and DGND.



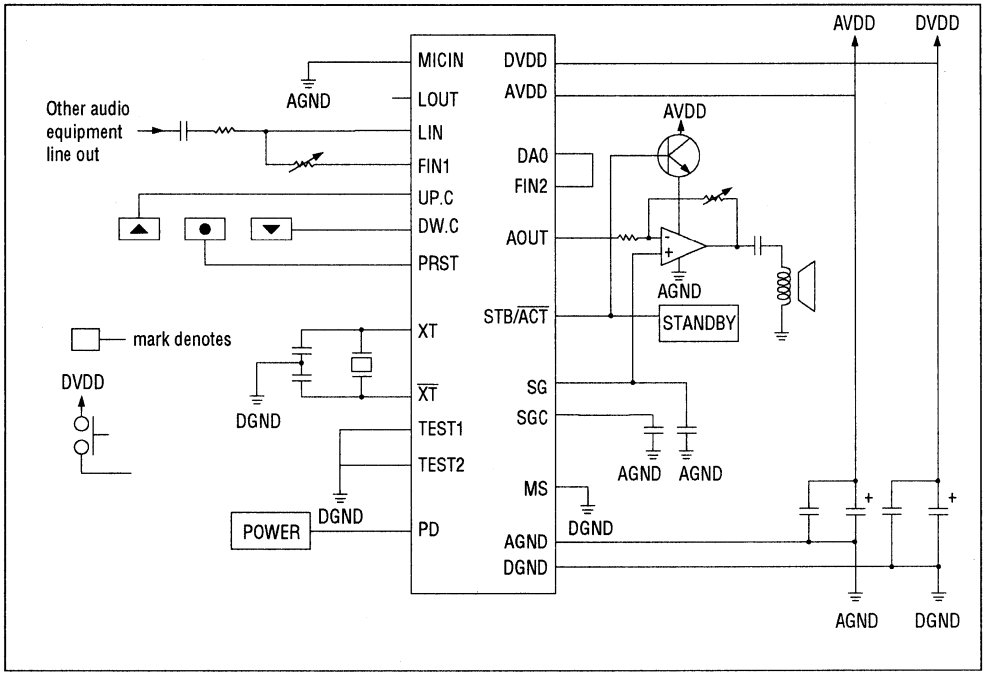
Note: The voltages of AVDD and DVDD should rise from 0V to 4V within 2ms when the power is risen.

Figure 6 Power Supply Circuit

APPLICATION CIRCUIT EXAMPLE 1 [BIN mode]



APPLICATION CIRCUIT EXAMPLE 2 [UP/DOWN mode]



Pitch Conversion Table

Scale and cutoff frequency

Scale stage / Remarks		DA sampling cycle (μS)/ frequency (kHz)	LPF cutoff frequency (kHz)	Interval of discontinuous point (ms)
16	One octave up	60/16.6	7.60	Approx 7.0
15	Major sixth up	71/14.0	7.60	Approx 10.0
14	Minor sixth up	76/13.1	5.70	Approx 12.0
13	Fifth up	80/12.5	5.70	Approx 15.0
12	Fourth up	90/11.1	5.70	Approx 22.0
11	Major third up	95/10.5	5.70	Approx 28.0
10	Minor third up	101/9.90	4.56	Approx 40.0
9	Minor second up	113/8.84	4.56	Approx 120.0
8	No change	120/8.33	3.80	—
7	Minor second down	127/7.87	3.80	Approx 110.0
6	Minor third down	143/6.99	3.26	Approx 45.0
5	Major third down	151/6.62	3.26	Approx 40.0
4	Fourth down	160/6.25	3.26	Approx 38.0
3	Fifth down	180/5.55	2.85	Approx 30.0
2	Minor sixth down	190/5.26	2.53	Approx 20.0
1	Major sixth down	202/4.95	2.53	Approx 20.0
0	Above one octave down	227/4.40	2.07	Approx 18.0

OKI Semiconductor

MSM6722

VOICE INTERVAL CONVERSION LSI **PRELIMINARY**

GENERAL DESCRIPTION

MSM6722 converts a voice signal into an actual time. In other words, it can convert a voice interval in the range of an active higher or lower.

As for the conversion of the voice interval, the voice control methods of two kinds are selected. That is the way to change 17 steps by two input switches and the way to select one of 16 steps by four binary inputs.

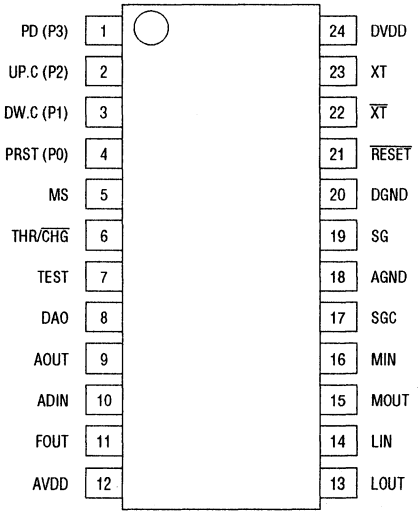
MSM6722 can be composed simply of a voice interval conversion set in only the connection of a mike, speaker amplifier and speaker peripherally to include a mike amplifier and low-pass filter.

FEATURES

- Built-in mike amplifier
- Built-in low-pass filter (input side fourthly, output side thirdly)
- Built-in 8-bit AD converter
- Built-in 9-bit DA converter
- Voice interval: Maximum 17 kinds
- Oscillation frequency: 4MHz
- 5V single power supply
- Package: 24-pin plastic SOP (SOP24-P-430-VK)
  24-pin plastic TSSOP (Under development)
- Structure: Silicon (Si Gate CMOS IC)

PIN CONFIGURATION

24 Lead Plastic Flat Package (Top View)



Speaker Amplifier

OKI Semiconductor

MSC1191/1192

DIRECT DRIVE SPEAKER AMPLIFIER

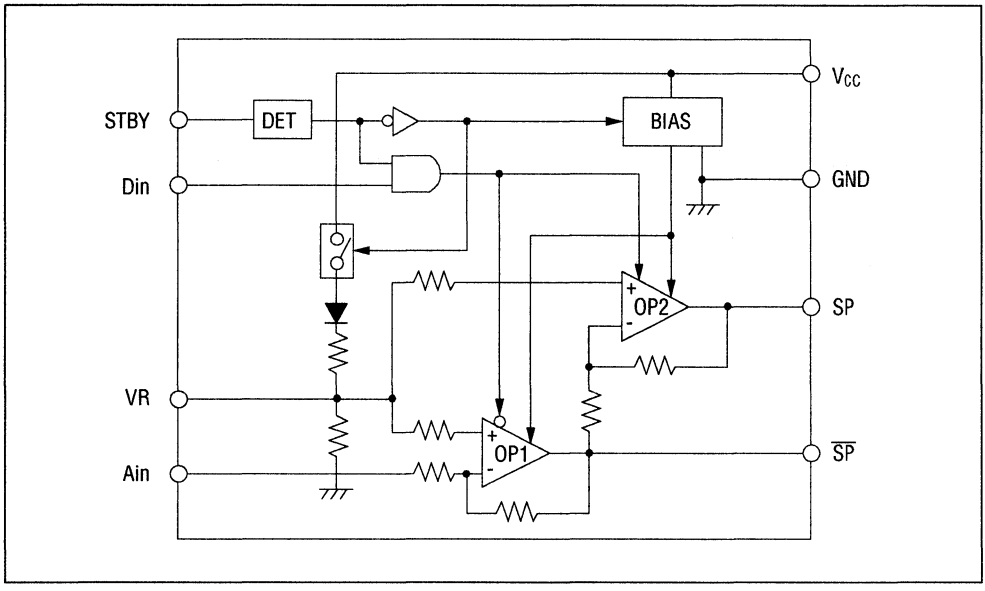
GENERAL DESCRIPTION

MSC1191/1192 is a low voltage, low current consumption type power amplifier IC developed for driving the speaker in a speech synthesizer application. It directly drives a speaker without any output coupling capacitance. The MSC1191 is set to the standby state at the "H" level, and MSC1192 at the "L" level.

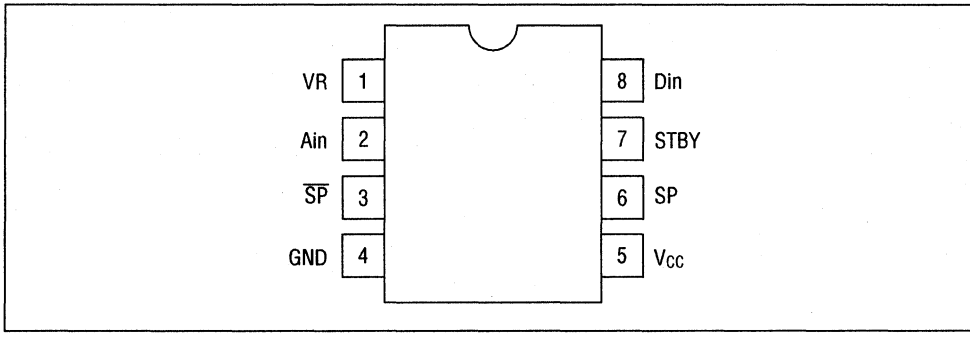
FEATURES

- Low voltage operation :
  2.0 to 6.0V single power supply
- Low current consumption:
  No-load operation current of 1.5 mA (typ)
- Standby function:
  Current consumption of 1 μA or less in standby state
- Two input pins:
  Analog signal input pin for speech signal, etc. and digital signal input pin for alarm signal, etc.
- High output current: 250 mA, peak
- Differential outputs:
  A speaker can be connected directly between differential output pins.
- 8 pin plastic DIP (DIP8-P-300)
- 8 pin plastic SOP (SOP8-P-250-K)
- Die

BLOCK DIAGRAM



PIN CONFIGURATION



• Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Rating	Unit	Pins
Power supply voltage	V_{CC}	Ta = 25°C	−0.3 ~ +6.5	V	V_{CC}
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ V_{DD} +0.3	V	STBY Din, Ain
Maximum output current	I_OMAX	Ta = 25°C	±300 (Note 1)	mA	SP, $\overline{SP}$
Power dissipation	P_d	Ta = 25°C	660	mW	
Storage temperature	T_{stg}	—	−45 ~ +125	°C	

Note 1: Shorting the output pins (SP and $\overline{SP}$) to V_{CC} or GND will damage the IC.

• Recommended Operating Ranges

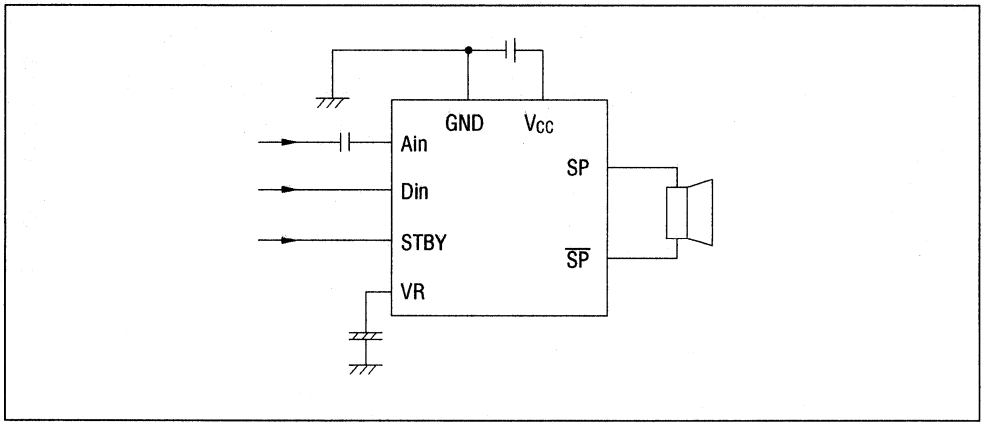
Characteristic	Symbol	Recommended values		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.0	6.0	V	
Load impedance	RL	8.0	—	Ω	
Peak load current	I_{O-P}	—	250	mA	
"H" input voltage	V_{IH}	0.7 V_{CC}	—	V	
"L" input voltage	V_{IL}	—	0.3 V_{CC}	V	
STBY operating frequency	f_{STBY}	8k	4M	Hz	At clock input
Operating temperature	T_{OP}	−10	60	°C	

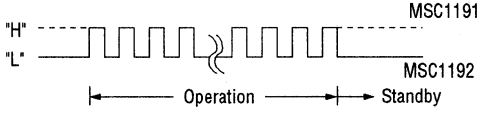
• Electrical Characteristics

(Ta=25°C)

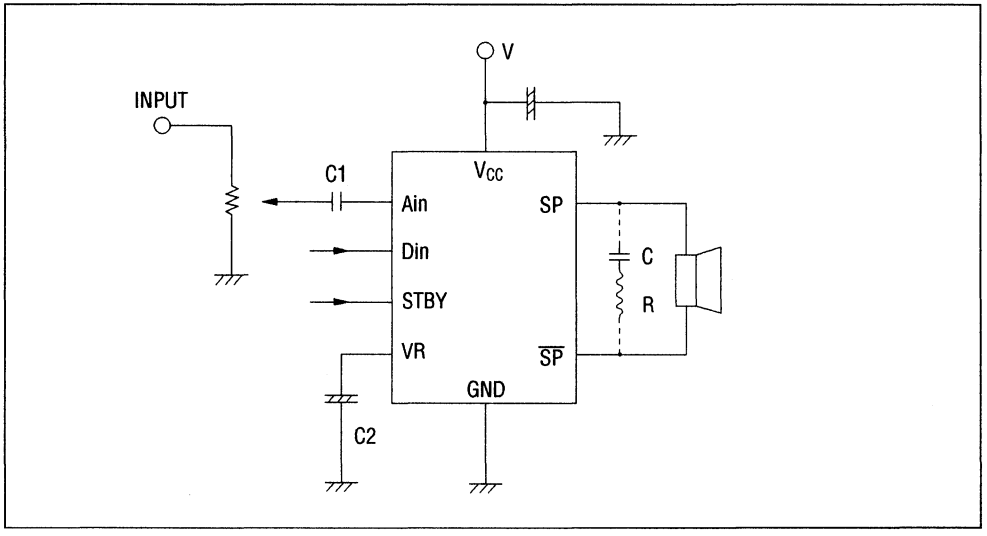
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input/resistance	R_{in}		70	100	130	kΩ
Voltage gain	AV1	Ain → $\overline{SP}$	−0.35	0	0.35	dB
	AV2	$\overline{SP}$ → SP	−0.35	0	0.35	dB
	AV3	Ain → (between SP− $\overline{SP}$)	5.3	6.0	6.7	dB
Output power	P_{out1}	V_{CC} = 3V RL = 8Ω, THD ≧ 10%	100		—	mW
	P_{out2}	V_{CC} = 6V RL = 32Ω, THD ≧ 10%	300		—	mW
Total harmonic distortion rate	THD1	V_{CC} = 3V, RL = 8Ω f = 1kHz, P_{OUT} = 45mW	—	0.35	1.0	%
	THD2	V_{CC} = 6V, f = 1kHz, P_{OUT} = 125mW	—	0.17	1.0	%
Ripple elimination ratio	RR	f = 1kHz, C2 = 1μF	30	37	—	dB
STBY operating frequency	f_{STBY}	At clock input	8K		4M	Hz
Output voltage	V_O	At no signal	Standard value −0.12	$\frac{V_{CC}-0.67V}{2}$	Standard value +0.12	V
Output offset voltage	$\triangle V_O$		—		±30	mV
Output "H" voltage	VOH1	Ain = V_{CC} or GND Iout = −100mA	V_{CC} −1.15	V_{CC} −1.04	—	V
	VOH2	Din = "H" Iout = −100mA	V_{CC} −1.15	V_{CC} −1.02	—	V
Output "L" voltage	VOL1	Ain = V_{CC} or GND Iout = 100mA	—	0.17	0.3	V
	VOL2	Din = "H" Iout = 100mA	—	0.33	0.45	V
"H" input voltage	VIH		0.7V_{CC}		—	V
"L" input voltage	VIL		—		0.3V_{CC}	V
Input current	I_I	VI = GND ~ V_{CC}	—		±0.1	μA
VR equivalent resistance	RVR		18	25	32	kΩ
Circuit current in operation	I_{CC1}	V_{CC} = 6V, RL = ∞	1.1	1.5	2.2	mA
	I_{CC2}	V_{CC} = 6V, RL = ∞ DIN = "H"	2.5	4.5	7.0	mA
Circuit current in standby state	I_{CCS}	V_{CC} = 6V	—		1.0	μA

PIN DESCRIPTION



Pin name	Function
V_{CC}	Power supply pin
GND	Ground pin
Ain	Analog signal input pin for speech signal, etc.
Din	Digital signal input pin for alarm signal, etc. valid in the standby state. SP = H and $\overline{SP}$ = L for Din =H, and SP = $\overline{SP}$ = HiZ for Din =L.
STBY	Input pin for bias block on/off to set the whole IC to on and off. **Model** / **Status** MSC1191: "H" Standby; "L" Operation MSC1192: "H" Operation; "L" Standby The signal shown at right may be used, or the LSI oscillation output may also be used. 
VR	Operating level bias output pin. Connecting a capacitor between this pin and the GND pin reduces the pop noise at power on and improves the ripple elimination ratio.
SP, $\overline{SP}$	Speaker connecting pins. DC level is $\frac{V_{CC} - 0.67}{2}$V

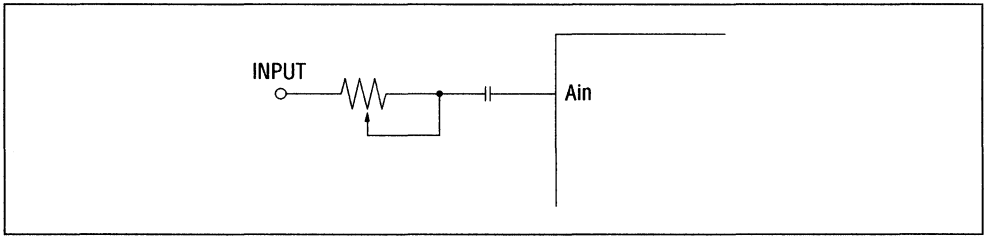
APPLICATION CIRCUIT EXAMPLE



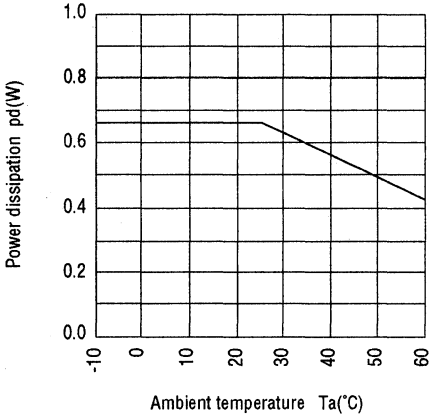
- C1 is the AC coupling capacitance. Low cut off frequency fc can be obtained by the following equation:

$$fc \fallingdotseq \frac{1}{2 * \pi * C1 * 100k} \quad (Hz)$$

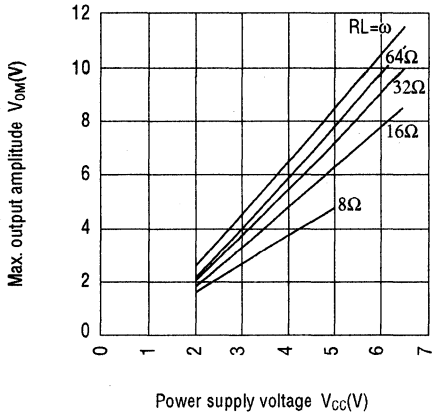
- C2 shall be 50 to 100 times the value of C1.
- C and R are for prevention of parasitic oscillation. Select proper values according to the speaker used. Generally recommended values are C = 0.02 μF and R = 6 to 10 Ω.
- When the Din and STBY functions are not to be used, fix Din = L and STBY = L for MSC1191, and Din = L and STBY =H for MSC1192.
- Sound volume control is also possible as shown below. This method is effective when the signal source impedance is high.



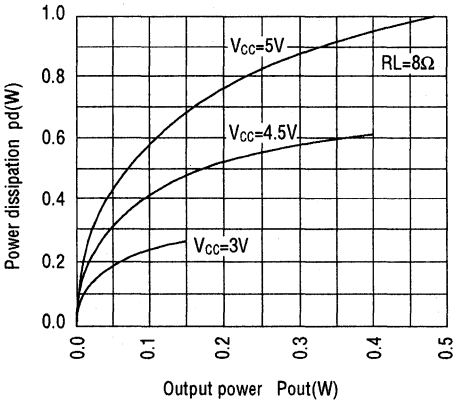
Power dissipation vs ambient temperature



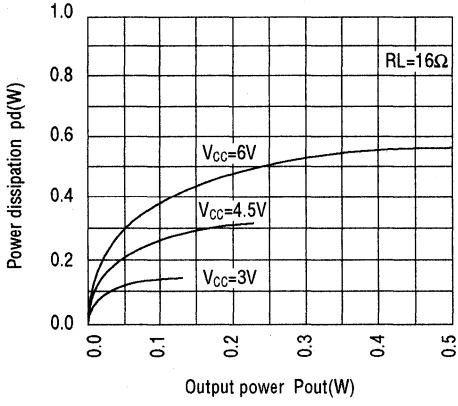
Max. output amplitude vs power supply voltage (example)



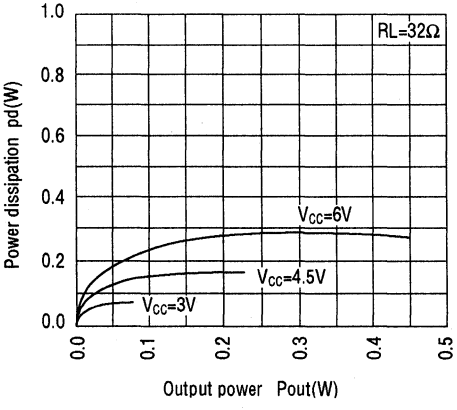
Power dissipation vs output power (example)



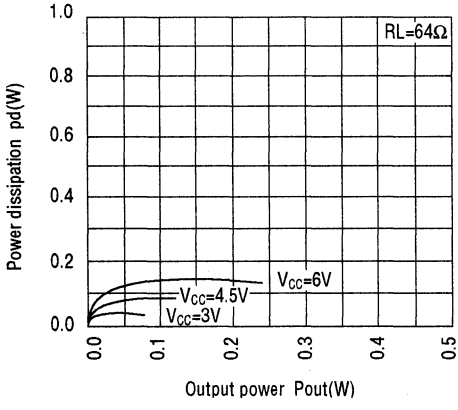
Power dissipation vs output power (example)



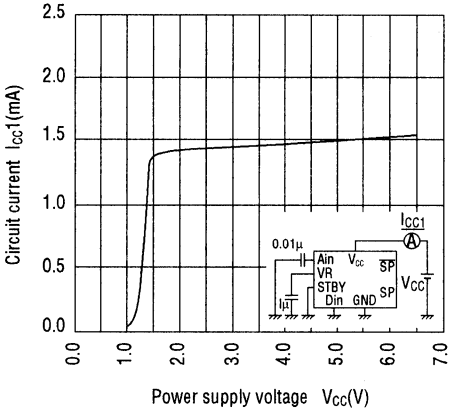
Power dissipation vs output power (example)



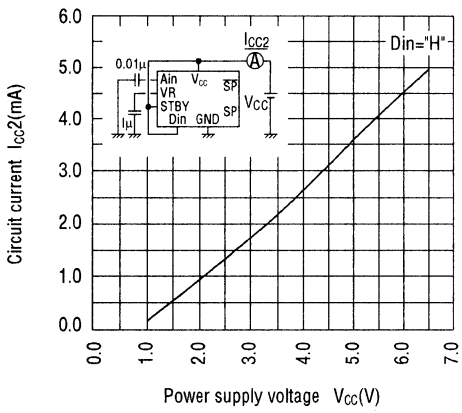
Power dissipation vs output power (example)



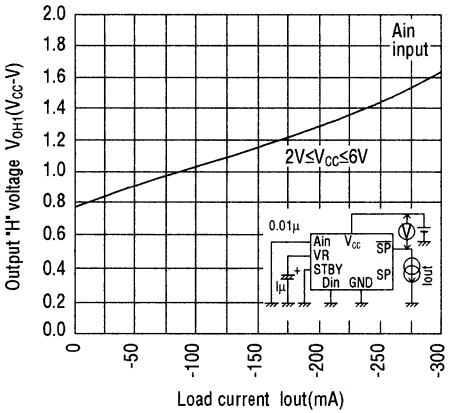
Circuit current vs power supply voltage (example)



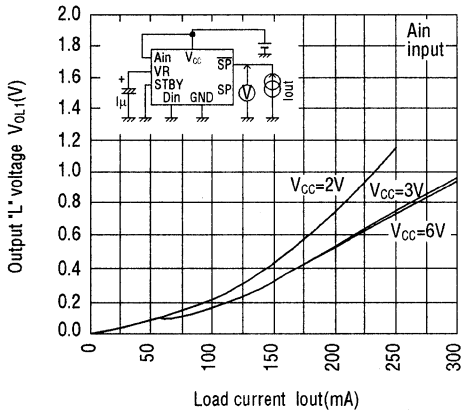
Circuit current vs power supply voltage (example)



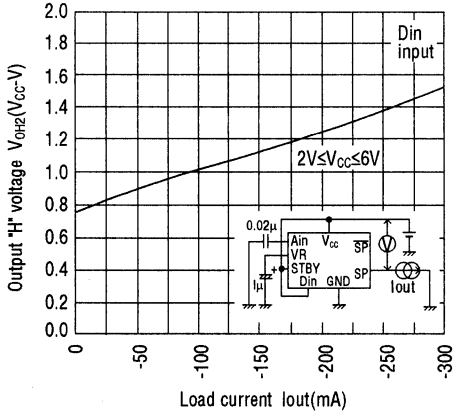
Output voltage vs load current (example)



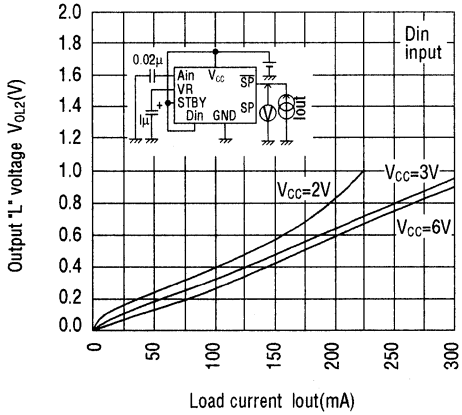
Output voltage vs load current (example)



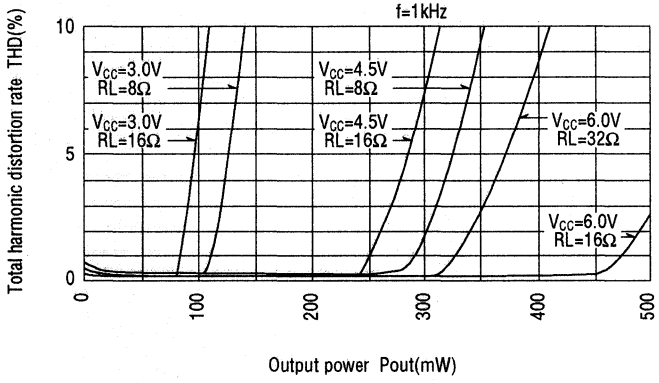
Output voltage vs load current (example)



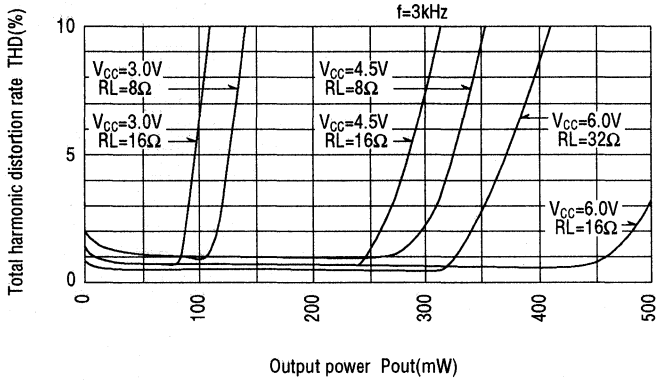
Output voltage vs load current (example)



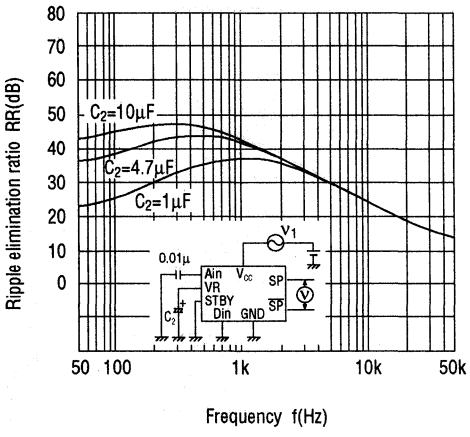
Total harmonic distortion rate vs output power (example)



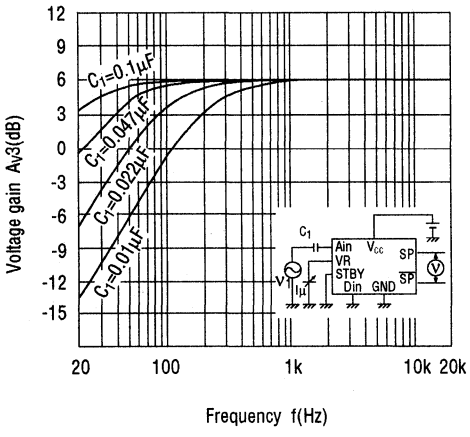
Total harmonic distortion rate vs output power (example)



Ripple elimination ratio vs frequency (example)



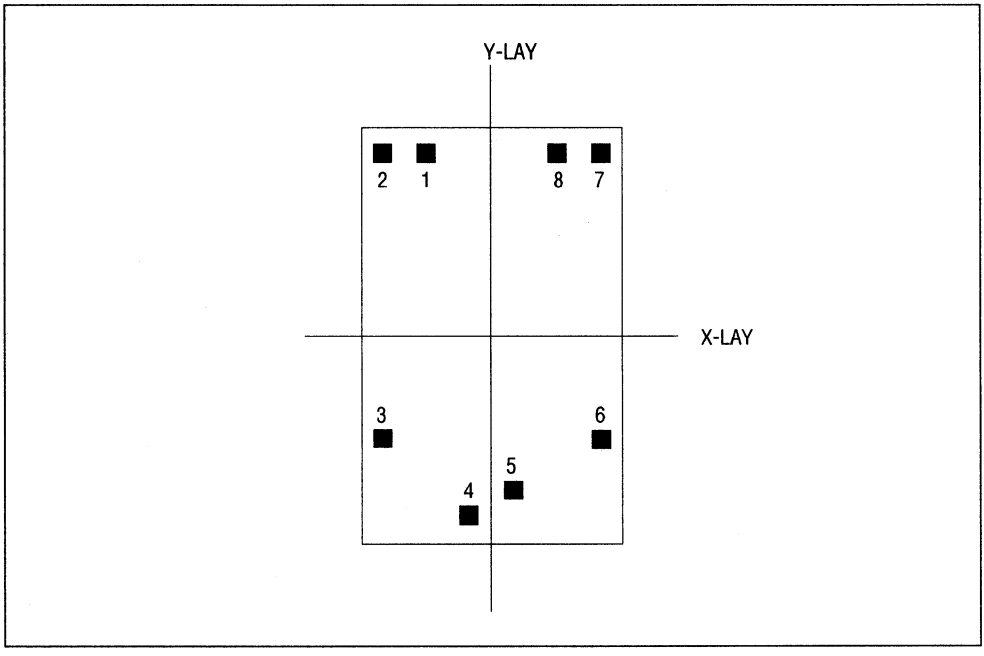
Voltage gain vs frequency (example)



MSC1191/1192 PAD LAYOUT

Die size : X = 1.84 mm Y = 2.6 mm
Die thickness : 350 ± 30 µm
Pad size : 112 x 112 µm
Substorate Voltage: GND

Pad location diagram



Pad Positions (the die center is located at X=0, Y=0)

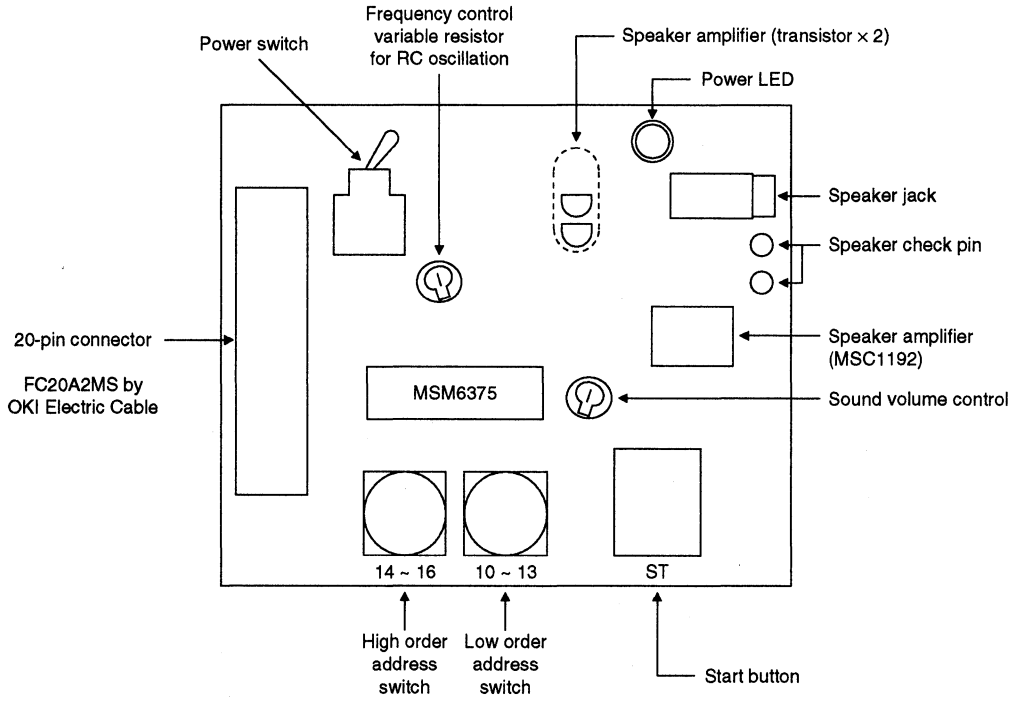
(Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS
1	VR	–442	1134
2	Ain	–754	1134
3	$\overline{SP}$	–754	–754
4	GND	–126	–1134
5	V_{CC}	126	–998
6	SP	754	–754
7	STBY	754	1134
8	Din	442	1134

Demonstration Board

MSM6375 Demonstration Board

1. Board Outline



2. Voice Reproduction Procedure

2.1 Turn the power switch to the ON side.
→ The power LED lights.

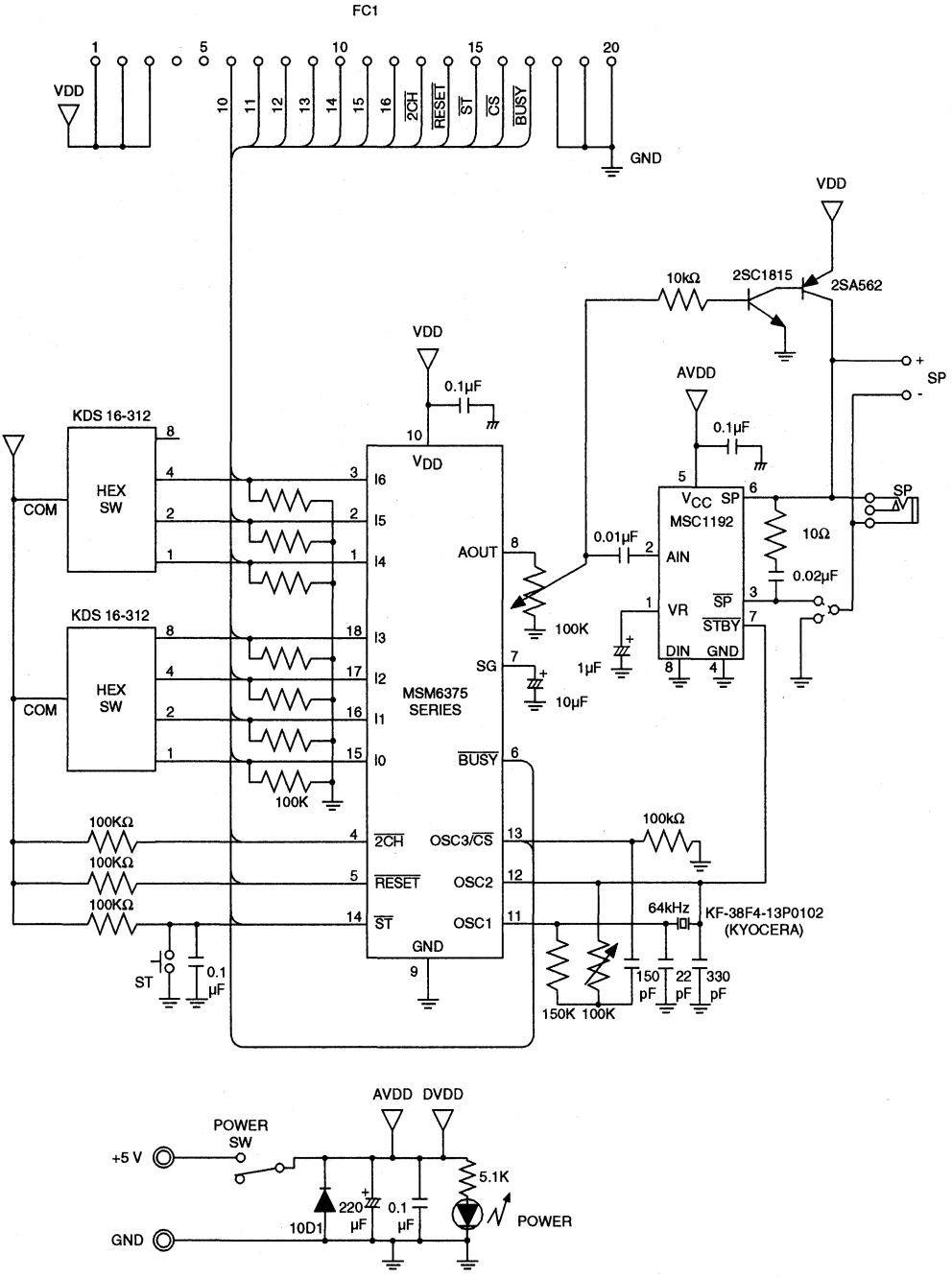
2.2 Set the high order and low order switches to the predetermined addresses. (The white numbers on the operator's side are addresses.)

2.3 Press the start button.
→ The Voice is reproduced.

(When the ROM option is set to "CPU Interface", the voice is reproduced two times when the start switch is pressed.)

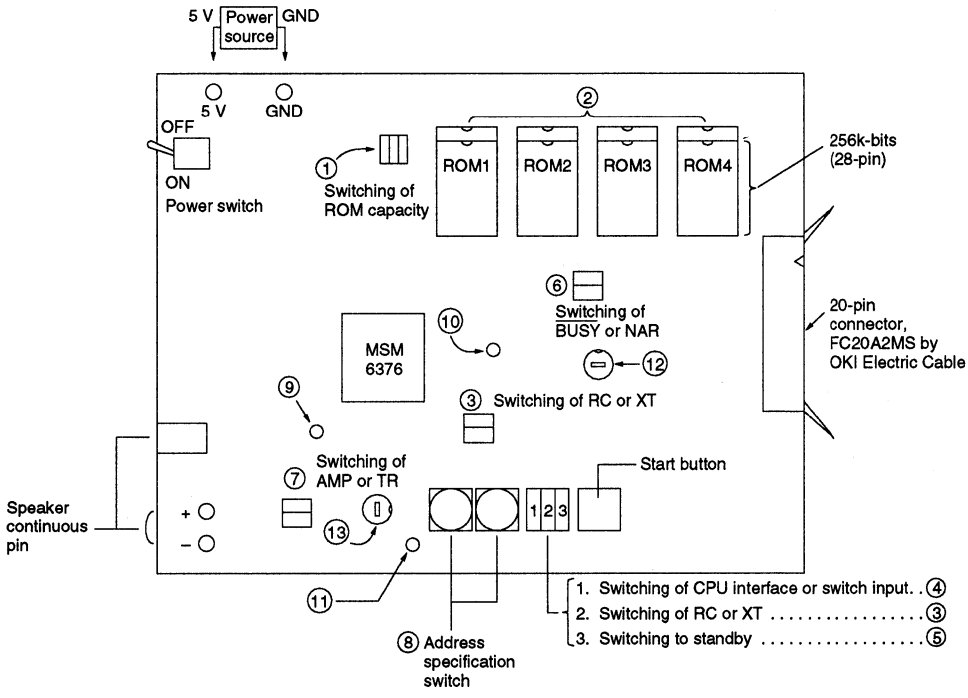
2.4 Turn the power switch to the OFF side.
→ The power LED goes off.

3. Circuit Design



MSM6376 Demonstration Board

1. Board Outline



2. How to Use Board

① ROM capacity switching jumper

256K-bit and 1M-bit (× 8-bit) CMOS type EPROMs can be used. For a 256K-bit EPROM, bridge the lower pins. For a 1M-bit EPROM, bridge the upper pins.

Note: Use an INTEL equivalent type 1 Megabit EPROM (27C010)

② EPROM socket

Insert EPROMs with the smaller address sequentially from the left. The EPROM socket has 32-pin. For 256K-bit EPROMs (28-pin), align them to the lower end.

③ RC/XT selector switch and jumper

This switch selects RC oscillation or crystal oscillation. To operate the IC with RC oscillation, turn the DIP switch to OFF and set the jumper to the left. To operate the IC with crystal oscillation, turn the DIP switch to ON and set the jumper to the right.

④ CPU interface/switch input interface selector switch

This switch selects the operation by CPU or by the momentary button labeled ST.

When using only this demonstration board, select "Switch Input" (at the DIP switch to OFF). When connecting the demonstration board to the CPU, turn the DIP switch to ON. When the CPU is connected, all necessary signals are connected to the 20-pin connector. The connector pins are arranged as shown below.

Connector pin No.	Signal	Connector pin No.	Signal
1	VDD	11	I5
2	VDD	12	I6
3	VDD	13	$\overline{2CH}$
4	N.C.	14	$\overline{RESET}$
5	N.C.	15	$\overline{ST}$
6	I0	16	$\overline{RCS}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

Note: Leave NC lines open connect. The $\overline{RCS}$ signal at Pin 16 to Low level.

⑤ Standby selector switch

When the standby selector switch is turned to ON and the board is not activated within 3 seconds after the voice is terminated, the board enters the standby state. (In the standby state, all the functions of the LSI are stopped.)

⑥ BUSY/NAR switching jumper

When the jumper is turned to the left side, the BUSY signal is output from the 20-pin connector. When the jumper is turned to the right side, the NAR signal is output from the 20-pin connector. Please refer to the data sheet for the timing of the BUSY or NAR signal.

⑦ AMP/TR switching jumper

To amplify an analog signal provided by the output pin AOUT with the transistor, turn the jumper to the right side. To amplify an analog signal provided by the output pin AOUT with the amplifier, turn the jumper to the left side.

⑧ Address specification switch

When using only this demonstration board, select a word to be reproduced by this HEX switch. The left is the MSB side and the right is the LSB side. When 0F is set, for example, 0001111 is set in I6 to I0. When connecting the board to the CPU, set the address to 00 and remove the capacitor 0.1 µF (C18) nearby the start switch.

⑨ DA converter output pin (without LPF)

⑩ Input frequency check pin

⑪ GND pin

⑫ Variable resistor (VR2) for adjusting the frequency of RC oscillation

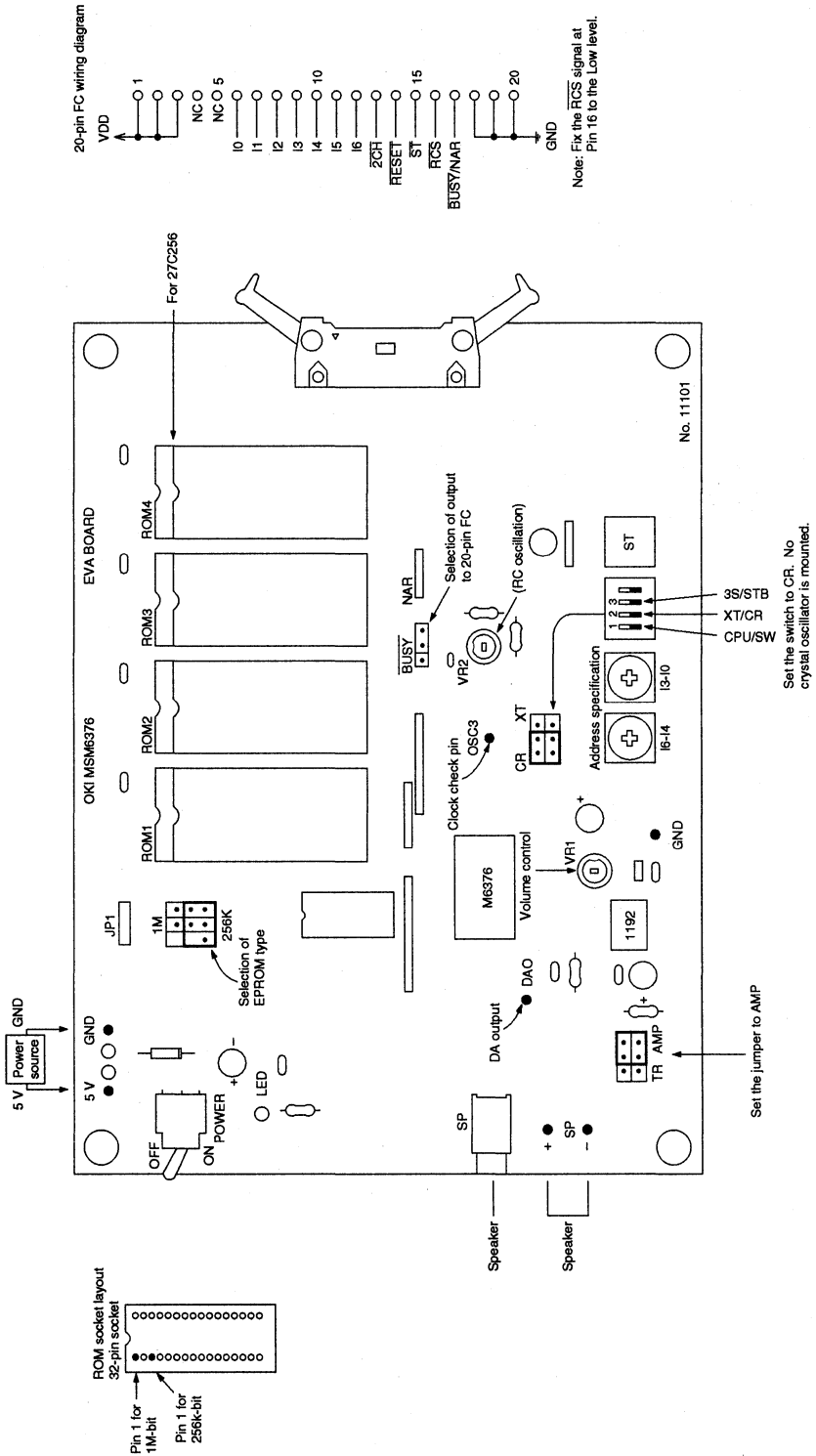
⑬ Variable resistor for volume control (shared by the amplifier and transistor)

Note: Use a CMOS type 27C256 or 27C010 EPROM. When a NMOS type 27256 or 27010 EPROM is used, the supply current of the EPROM fluctuates, causing noise.

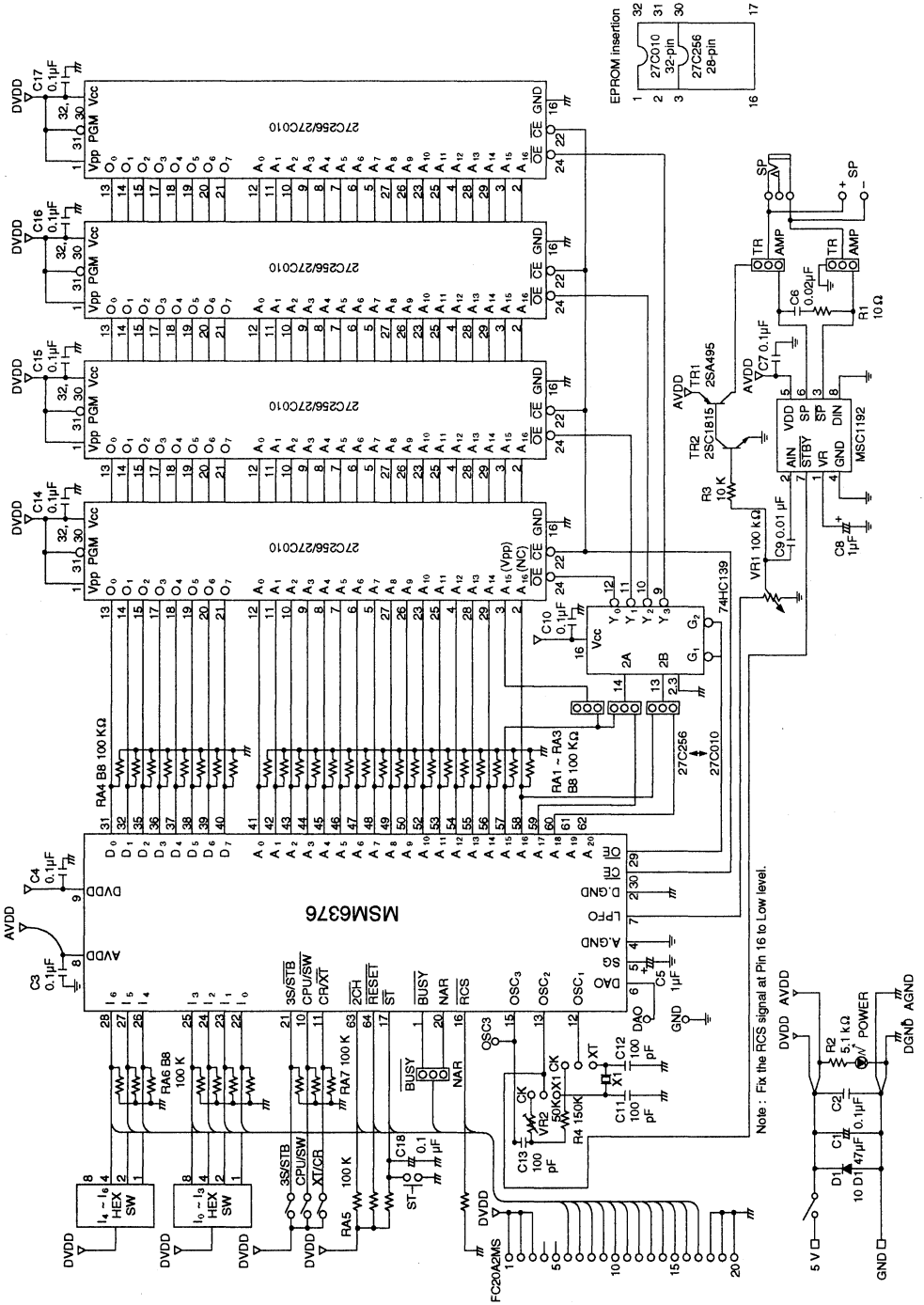
3. Voice Reproduction Procedure

3.1 Set the address specification switch.

3.2 Press the start button.

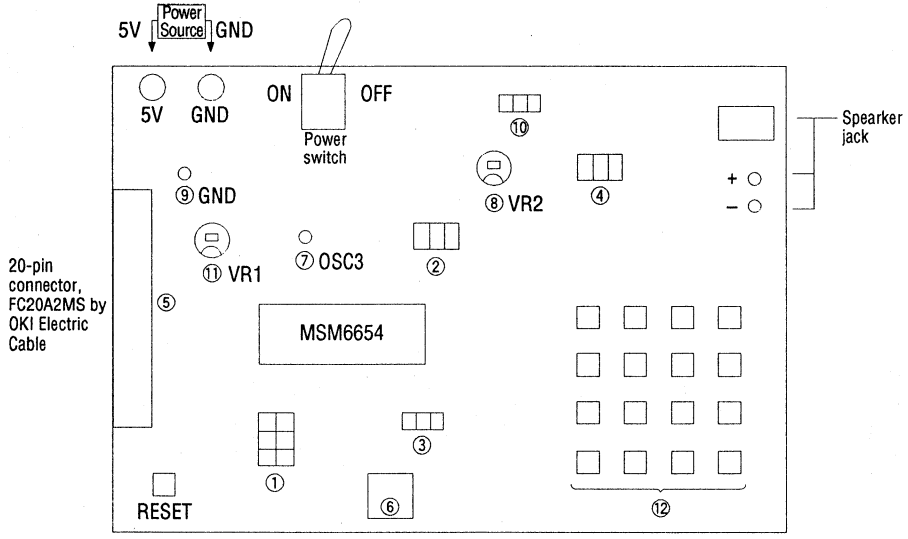

20-pin FC wiring diagram
VDD
1
NC
NC
5
I0
I1
I2
I3
I4
I5
I6
2CH
RESET
ST
RCS
BUSY/NAR
10
15
20
GND
Note: Fix the RCS signal at Pin 16 to the Low level.
For 27C256
EVA BOARD
OKI MSM6376
No. 11101
ROM1
ROM2
ROM3
ROM4
NAR
Selection of output to 20-pin FC
BUSY
VR2
(RC oscillation)
ST
3S/STB
XT/CR
CPU/SW
Address specification
I3-I0
I6-I4
Set the switch to CR. No crystal oscillator is mounted.
CR
XT
Clock check pin
OSC3
M6376
Volume control
VR1
GND
JP1
1M
256K
Selection of EPROM type
1192
DAO
DA output
TR
AMP
Set the jumper to AMP
5 V
GND
Power source
5 V
GND
LED
POWER
OFF
ON
SP
SP
Speaker
Speaker
ROM socket layout
32-pin socket
Pin 1 for 1M-bit
Pin 1 for 256k-bit

4. Circuit Diagram



MSM6654 Demonstration Board

1. Board outline



2. How to Use Board

①, ② Standalone/microcontroller interface switching jumpers and XT/CR switching jumpers

The jumpers in ① are used to select the operation by a standalone-mode or by a microcontroller interface-mode. The jumpers in ② are used to select RC oscillation or crystal oscillation. When a standalone-mode is used, for RC oscillation, set the jumpers in ① to the lower right side and set the three jumpers in ② to the lower side. For crystal oscillation, set the jumpers in ① to the upper right side and set the three jumpers in ② to the upper side. When a microcontroller is used, only CR oscillation is settable. Set the jumpers in ① to the upper left side and set the three jumpers in ② to the upper side.

③ $\overline{\text{BUSY}}$/NAR switching jumper

When the jumper is turned to the right side, the $\overline{\text{BUSY}}$ signal is output from pin 17 of the 20-pin connector. When the jumper is turned to the left side, the NAR signal is output from the same pin. When a standalone computer is used, turn the jumper to the right side.

④ AMP/TR switching jumpers

To amplify an analog signal which is output from AOUT, with transistors, set the two jumpers to the right side. To amplify it with an amplifier, turn the two jumpers to the left.

⑤ 20-pin connector

All necessary signals are connected to the 20-pin connector when a microcontroller is used. The connector pins are arranged as shown below.

Connector pin No.	Signal	Connector pin No.	Signal
1	VCC	11	I5
2	VCC	12	I6
3	VCC	13	$\overline{CH}$
4	N.C.	14	$\overline{RESET}$
5	N.C.	15	$\overline{ST}$
6	I0	16	$\overline{CMD}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

⑥ Address specification switch

When a standalone-mode is used, select a word to be reproduced by this HEX switch. 0~7 in this HEX switch correspond to A0~A2 in binary data. When a microcontroller is used, set the HEX switch to 0.

⑦ Frequency check pin (OSC3)

This pin monitors and checks the oscillation frequency.

⑧ Speaker amplifier volume (VR1 shared by AMP/TR)

Turn the volume switch to the right to increase the sound volume. Turn the volume switch to the left to reduce the sound volume.

⑨ GND pin

⑩ OSC/VDD switching jumper

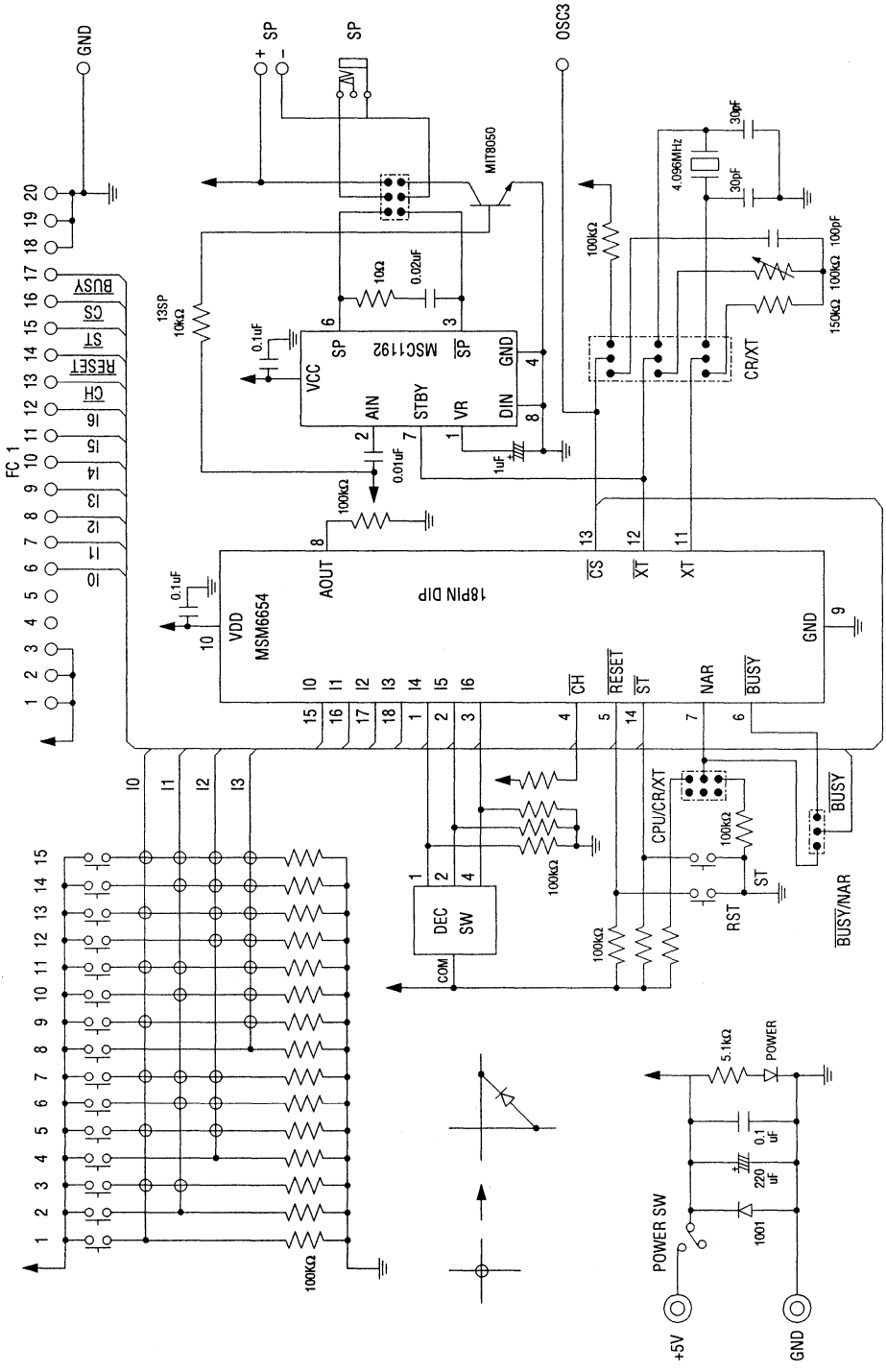
Set the jumper to the left side.

⑪ Variable resistor (VR2) for adjusting the frequency of RC oscillation

This variable resistor can change the frequency of RC oscillation, When the resistor is turend to the right, the frequency goes low. When the resistor is turned to the left, the frequency goes high. In this case, the frequency can be monitored by pin 7.

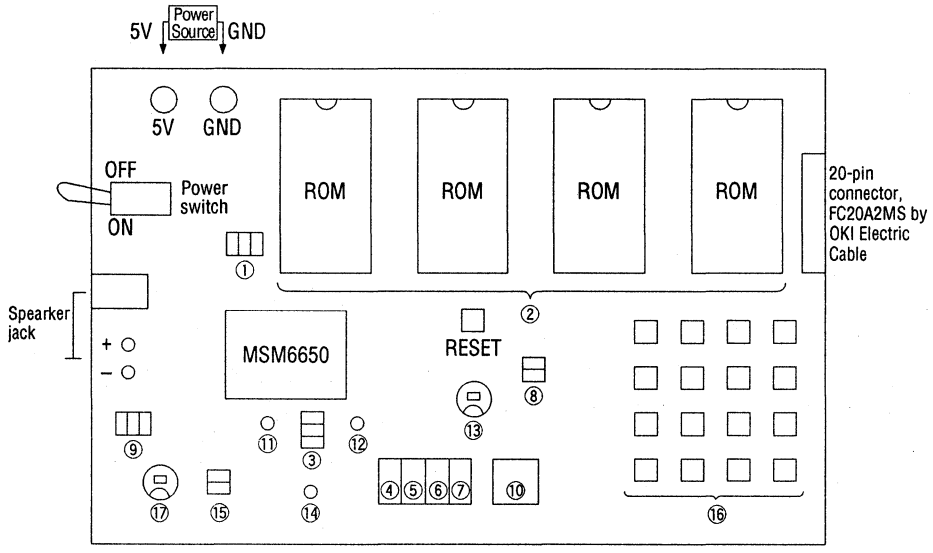
⑫ Complete SW input interface

When a standalone computer is used, press the 1~F buttons to reproduce voices corresponding to 1~F of SW3~SW0. Press the lower left ST button (random voice reproduction button) to reproduce voices that are randomly selected from 31 types of phrases corresponding to A0 and SW3~SW0. But, when the ST switch is pressed while turning the power ON or during the input of $\overline{\text{RESET}}$, firstly voice reproduction is made starting from the the 1st phrase and beyond secondly it is made randomly.


GND
SP
SP
OSC3
MIT8050
4.096MHz
30pF
30pF
100kΩ
100kΩ
100pF
150kΩ
CR/XT
13SP
10kΩ
10Ω
0.02uF
0.1uF
MSC1192
VCC
SP
SP
GND
AIN
STBY
VR
DIN
0.01uF
1uF
100kΩ
FC 1
BUSY
CS
ST
RESET
CH
I6
I5
I4
I3
I2
I1
I0
0.1uF
VDD
MSM6654
AOUT
18PIN DIP
CS
XT
XT
GND
I0
I1
I2
I3
CH
RESET
ST
NAR
BUSY
CPU/CR/XT
100kΩ
BUSY
BUSY/NAR
DEC
SW
COM
100kΩ
100kΩ
RST
ST
100kΩ
5.1kΩ
POWER
0.1 uF
220 uF
1001
POWER SW
+5V
GND

MSM6650 Demonstration Board

1. Board outline



2. How to Use Board

① ROM capacity switching jumpers

1M-bit and 4M-bit CMOS type EPROMs can be used. For a 1M-bit EPROM, set the 3 jumpers to the lower pins. For a 4M-bit EPROM, set them to the upper pins.

② EPROM socket

Insert EPROMs fabricated by voice analysis, sequentially from the left.

③, ④ XT/$\overline{CR}$ selector switch and jumpers

This switch selects RC oscillation or crystal oscillation. To operate the IC with RC oscillation, turn the DIP switch to the lower side and set the two jumpers in ③ to the upper side. To operate the IC with crystal oscillation, turn the DIP switch to the upper side and set the two jumpers in ③ to the lower side.

⑤ Standalone/microcontroller selector switch

This switch selects the operation by a standalone-mode or by a microcontroller interface-mode. For a standalone-mode, turn the DIP switch to the lower side. For a microcontroller, turn the DIP switch to the upper side. When the microcontroller is connected, all necessary signals are connected to the 20-pin connector. The connector pins are arranged as shown below. If the standalone computer is used, turn the SIRI switch ⑥ to the lower side.

Connector pin No.	Signal	Connector pin No.	Signal
1	VDD	11	I5
2	VDD	12	I6
3	VDD	13	$\overline{CH}$
4	N.C.	14	$\overline{RESET}$
5	N.C.	15	$\overline{ST}$
6	I0	16	$\overline{CMD}$
7	I1	17	$\overline{BUSY}$/NAR
8	I2	18	GND
9	I3	19	GND
10	I4	20	GND

⑥ Serial input interface/parallel input interface selector switch

When a microcontroller is used, this switch selects the serial inputs of addresses and command data or the parallel inputs of them. For the serial inputs, turn the switch to the upper side. For the parallel inputs, turn the switch to the lower side.

⑦ Standby selector switch

When the switch is turned to the lower side and the board is not activated toward the next phrase within 0.2 second after the voice is terminated, the board enters the standby state. (In the standby state, all the functions of the LSI are stopped.)

⑧ $\overline{BUSY}$/NAR switching jumper

When the jumper is turned to the upper side, the $\overline{BUSY}$ signal is output from the 20-pin connector. When the jumper is turned to the lower side, the NAR signal is output from the 20-pin connector. When a standalone computer is used, set the jumper to the upper side.

⑨ AMP/TR switching jumpers

To amplify an analog signal which is output from AOUT, with transistors, set the two jumpers to the left side. To amplify it with an amplifier, turn the two jumpers to the right.

⑩ Address specification switch

When a standalone computer is used, select a word to be reproduced by this HEX switch. 0~7 in this HEX switch correspond to A0~A2 in binary data. When a microcontroller is used, set the HEX switch to 0.

⑪ LPF output pin

This pin outputs a voice signal passed through the low path filter. When the DA converter is selected by option, this pin works as the DA converter pin.

⑫ Frequency check pin (OSC3)

This pin monitors and checks the oscillation frequency.

⑬ Variable resistor (VR2) for adjusting the frequency of RC oscillation.

This variable resistor can change the frequency of RC oscillation. When the resistor is turned to the right, the frequency goes low. When the resistor is turned to the left, the frequency goes high. In this case, the frequency can be monitored by the OSC3.

⑭ GND pin

⑮ OSC/GND switching jumper

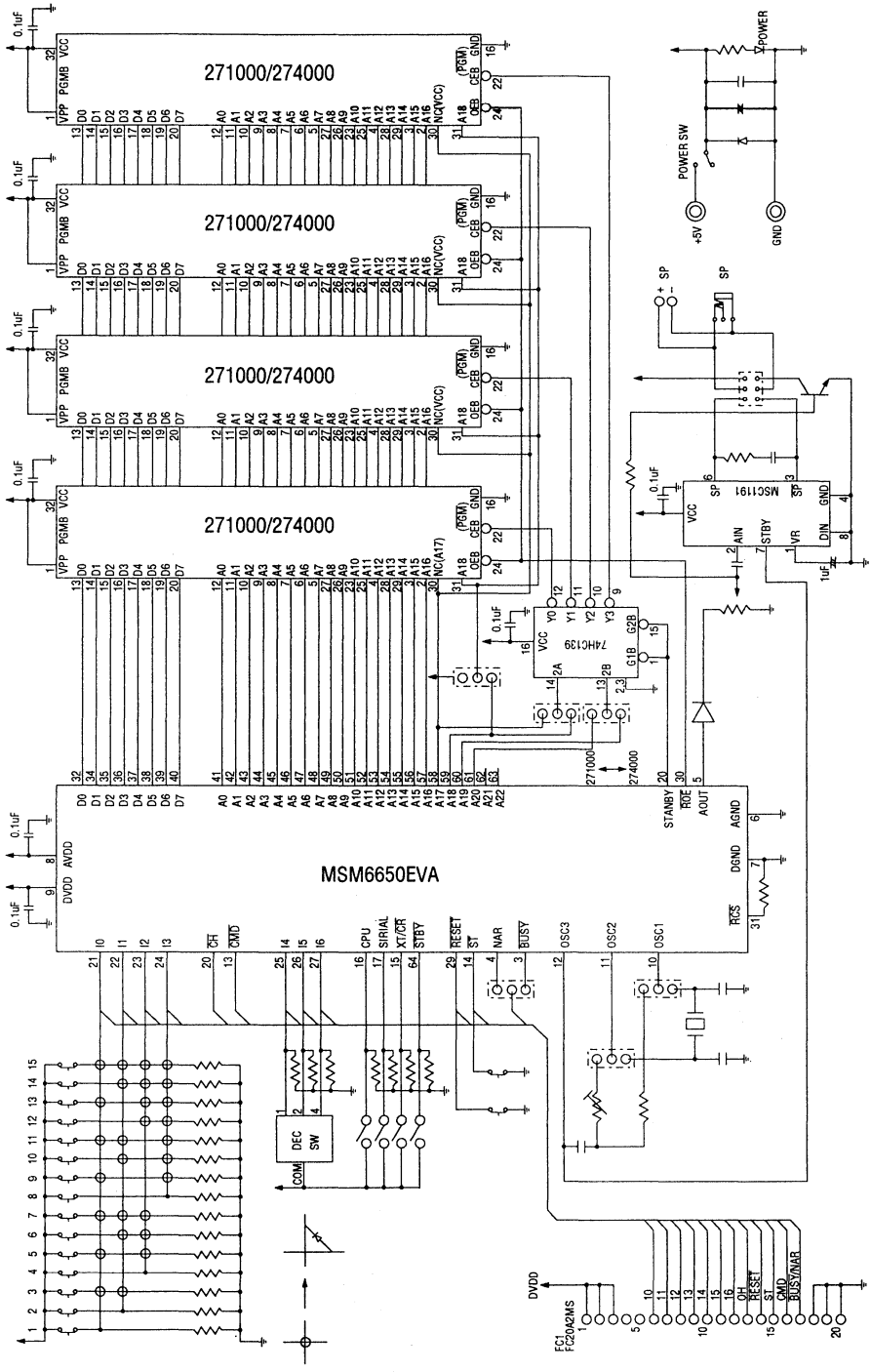
Set the jumper to the upper side.

⑯ Complete SW input interface

When a standalone-mode is used, press the 1~F buttons to reproduce voices corresponding to 1~F of SW3~SW0. Press the lower left ST button (random voice reproduction button) to reproduce voices that are randomly selected from 31 types of phrases corresponding to A0 and SW3~SW0. But, when the ST switch is pressed while turning the power ON or during the input of $\overline{\text{RESET}}$, firstly voice reproduction is made starting from the 1st phrase and beyond secondly it is made randomly.

⑰ Speaker amplifier volume (VR1 shared by AMP/TR)

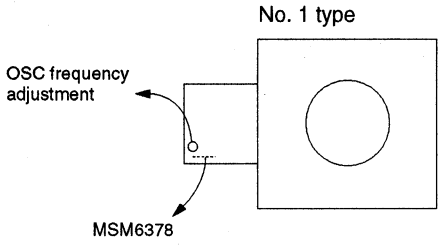
Turn the volume switch to the right to increase the sound volume. Turn the volume switch to the left to reduce the sound volume.

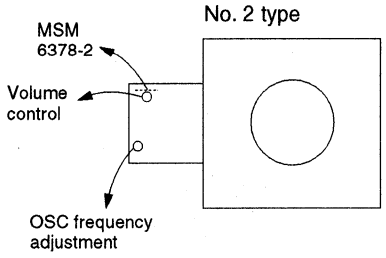

271000/274000
271000/274000
271000/274000
271000/274000
MSM6650EVA
74HC139
MSC1191
POWER
POWER SW
+5V
GND
SP
DEC SW
FG1
FG20A2MS

MSM6378A Demonstration Board

There are two types of MSM6378A (OTP built-in voice synthesis LSI) demonstration boards. The demonstration board using a transistor as a speaker amplifier is the No. 1 type and the board using MSC1191 is the No. 2 type. (Only No. 2 types are being manufactured at present.)

1. Board Outline and Name of Each Unit





2. Voice reproduction procedure

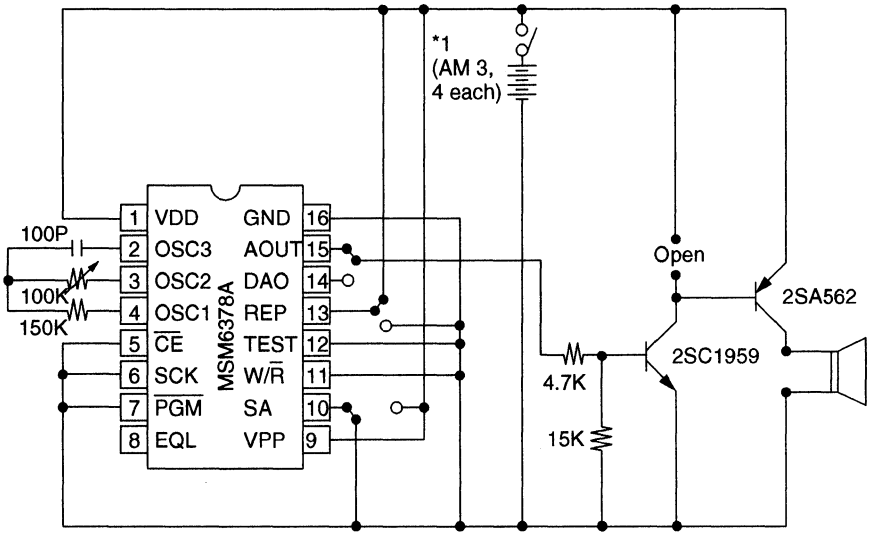
When the power switch is pressed, the voice is output repeatedly.

3. Specifications

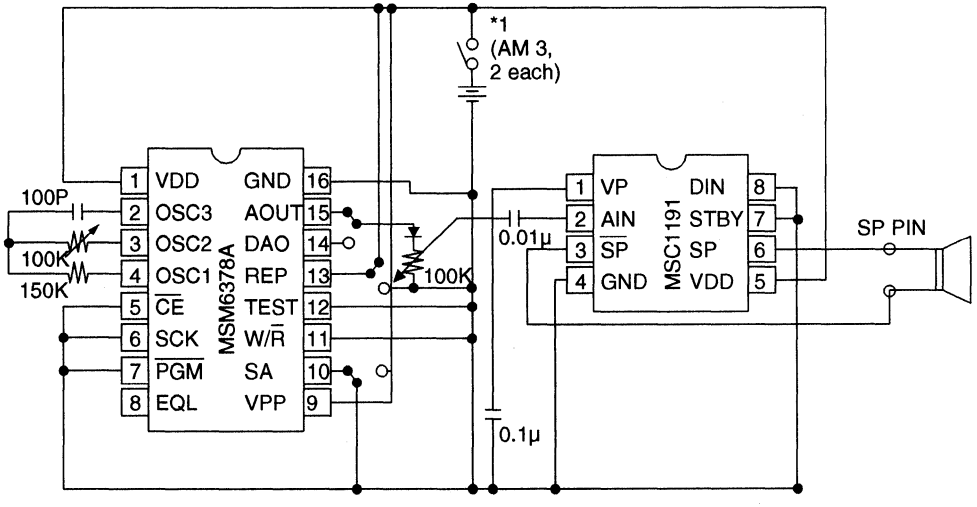
- Power source: No. 1 type: ..... AM 3, 4 each,
  No. 2 type: ..... AM 3, 2 each
  (The guaranteed power supply range for accurate reproduction through the internal LPF is from +2.7V ~ +5.5V.)
- Sampling frequency: The MSM6378A sampling frequency of the demonstration board is 8 kHz.
- Pin option: Repeated output: ..... REP = H
  Output pin: ..... AOUT (LPF output)
- Power amplifier: No. 1 type: ..... 2 transistors,
  No. 2 type: MSC1191
- Speaker: 8 Ω, 2 W

4. Circuit Diagram

No. 1 type



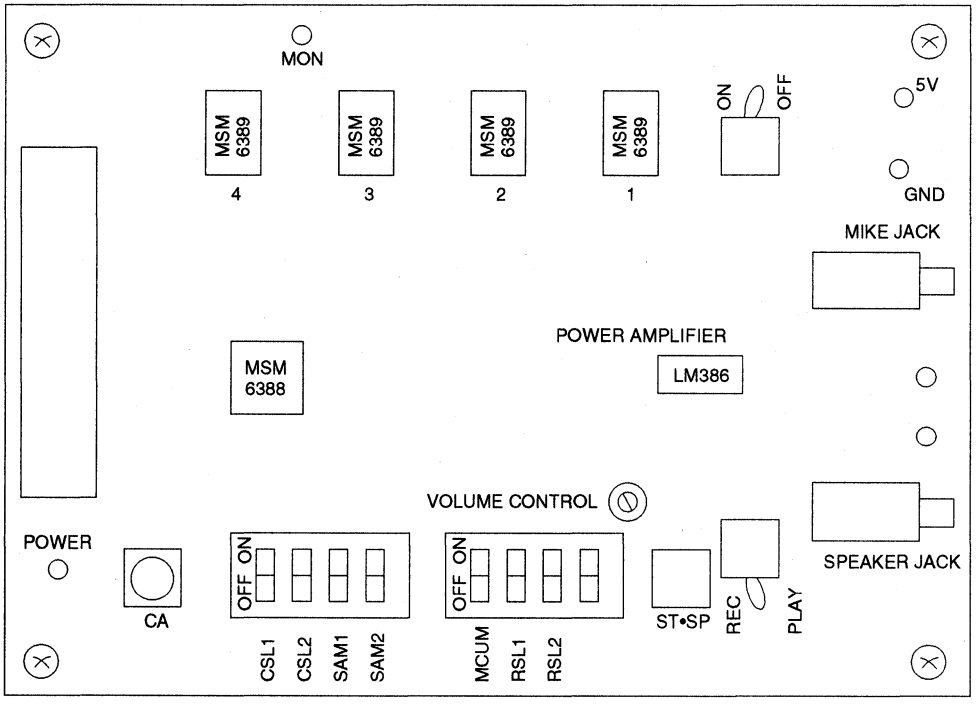
No. 2 type



* Note: The guaranteed voltage of LPF output of MSM6378 ranges from 2.7 V ~ 5.5 V.

MSM6388 Demonstration Board

1. Board Outline



2. Connection

2.1 Insert the mike into the mike jack.

2.2 Insert the speaker into the speaker jack.

3. Set operating parameters

3.1 Set RSL1 and RSL2 of the DIP switch as shown in the tabel below depending on the number of serial registers mounted.

Number of serial registers	1 Each	2 Each	3 Each	4 Each
RSL1	OFF	ON	OFF	ON
RSL2	OFF	OFF	ON	ON

3.2 Set MCUM of the DIP switch to OFF. The MSM6388 enters the stand-alone mode. (When MCUM is set to ON, the MSM6388 enters the microcontroller interface mode.)

3.3 Specify the sampling frequency by SAM1 and SAM2 of the DIP switch.

SAM1	OFF	ON	OFF	ON
SAM2	OFF	OFF	ON	ON
Sampling frequency	$\frac{fosc}{512}$	$\frac{fosc}{288}$	$\frac{fosc}{256}$	$\frac{fosc}{224}$
fsam	(3.9kHz)	(6.9kHz)	(7.8kHz)	(8.9kHz)

( ): sampling frequency at f_{osc} = 2 MHz

3.4 Specify the number of channels by CSL1 and CSL2 of the DIP switch.

The number of channels is as shown in the table below depending on the number of serial registers specified in Section 3.1.

CSL1		OFF	ON	OFF	ON
CSL2		OFF	OFF	ON	ON
Number of channels	1, 2, or 4 serial registers	8-word	4-word	2-word	1-word
	3 serial registers	6-word	3-word	2-word	1-word

The recording time of each channel can be obtained from the following equation:

$$\text{Recording time} = \frac{1.024 \times 1024 \text{ (k bit)} \times \text{No. of serial registers}}{\text{Sampling frequency (kHz)} \times 4 \text{ (bit)} \times \text{No. of channels}} \text{ (sec)}$$

For example, the recording time for each channel with two serial registers on 8-channel at a sampling frequency of 7.8 kHz (RSL1 is set to ON, RSL2 to OFF, CSL1 to OFF, CSL2 to OFF, SAM1 to OFF, and SAM2 to ON) is as follows:

$$\text{Recording time} = \frac{1.024 \times 1024 \text{ (k bit)} \times 2 \text{ (each)}}{7.8 \text{ (kHz)} \times 4 \times 8} \fallingdotseq 8 \text{ (sec)}$$

4. Recording

4.1 Turn the toggle switch on the upper right of the demonstration board to ON to engage power. The LED (POWER) on the lower left of the demonstration board comes on.

4.2 Set the conditions as specified in Section 3, "Set operating parameters".

4.3 Set the rotary switch (CA) to the channel for recording.

Number of channels :	8-word :	0 ~ 7
	6-word :	0 ~ 5
	4-word :	0 ~ 3
	3-word :	0 ~ 2
	2-word :	0 ~ 1

4.4 Set the toggle switch on the lower right of the demonstration board to REC to select the recording mode.

4.5 Press the push button (ST.SP) once and record voice via the mike. During recording, the LED (MON) on the demonstration board is on. When the channel recording time runs short (4 seconds before the end of the recording time for 7.8 kHz sampling), the LED starts blinking, though voice can be recorded until the LED goes off.

To stop recording halfway, press the push button (ST.SP) once again. The recording is terminated.

5. Reproduction

5.1 Set the rotary switch (CA) to the channel for reproduction.

5.2 Set the toggle switch on the lower right of the demonstration board to PLAY to select the reproduction mode.

5.3 Press the push button (ST.SP) once to start reproduction. During reproduction, the LED (MON) is on. To stop reproduction halfway, press the push button (ST.SP) once again. The reproduction is terminated.

5.4 Use the variable resister to adjust.

6. Microcontroller interfacing

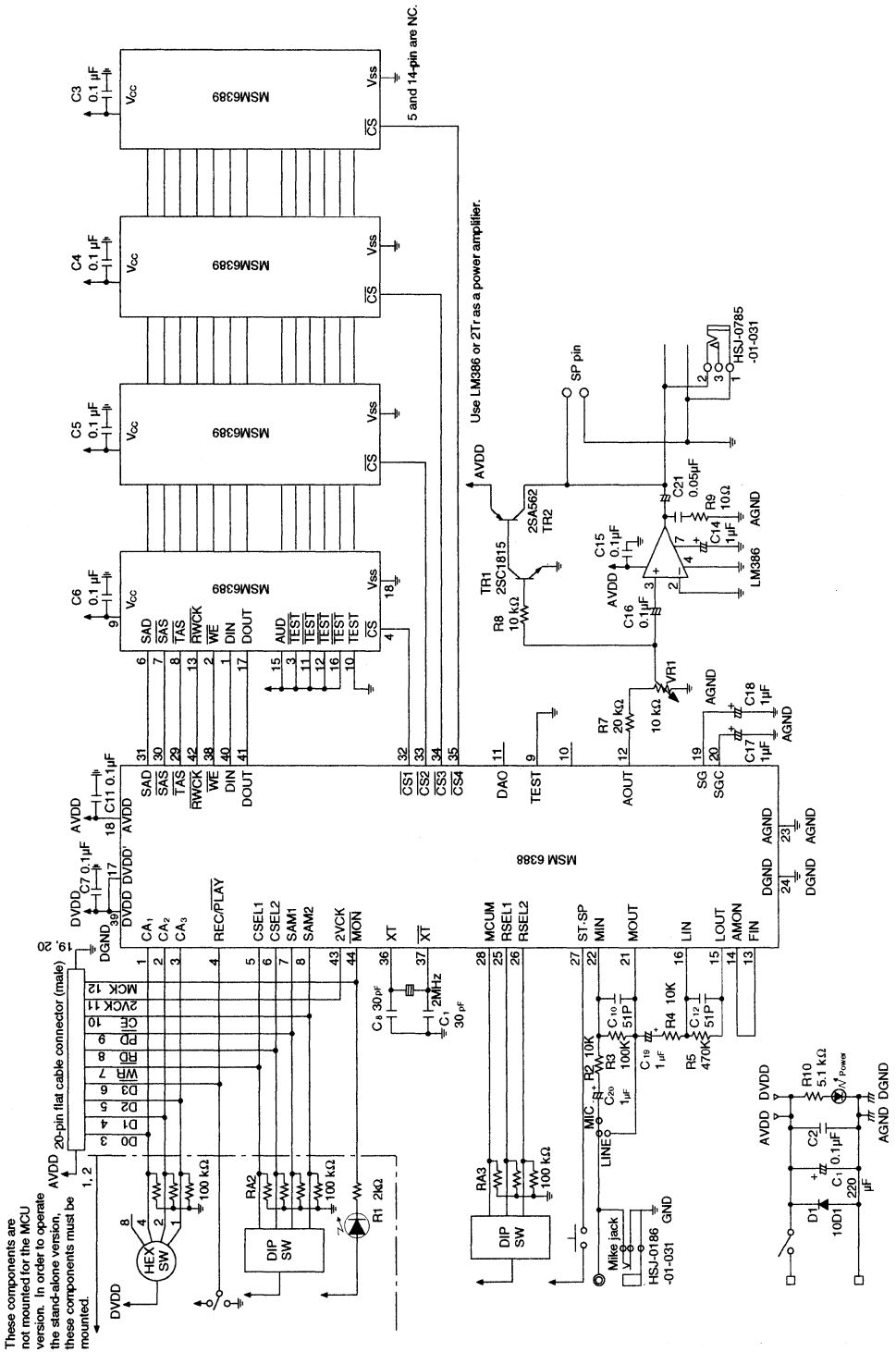
6.1 Set MCUM of the DIP switch to ON.

6.2 Set RSL1 and RSL2 of the DIP switch as specified in Section 3.1.

6.3 Remove the DIP switch (CSL1, CSL2, SAM1, and SAM2), the rotary switch, the pull-down resistors (RA1 and RA2) used for them, LED (MON), and the resistor (R1) from the board.

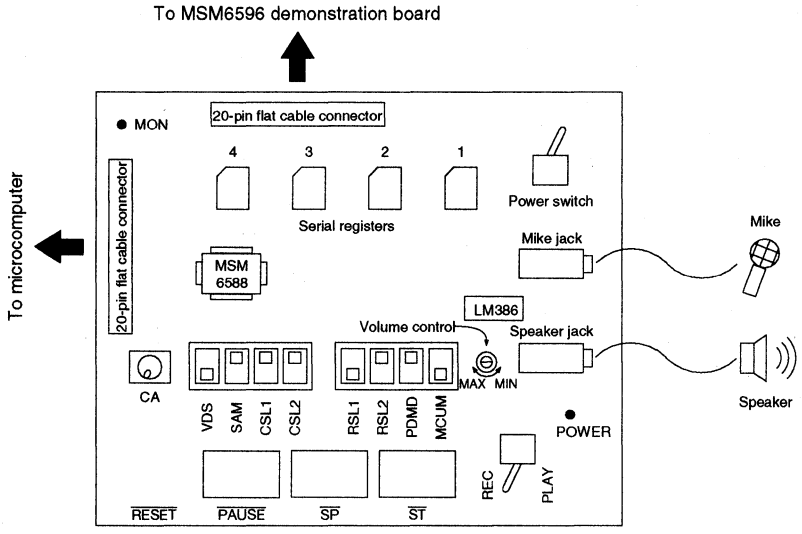
6.4 Mount a 20-pin flat cable connector at the left end of the demonstration board. The pins to be interfaced with the micrcomputer are connected. (Refer to the circuit diagram of the demonstration board on the next page.)

7. Circuit Diagram



MSM6588 Demonstration Board

1. Board Outline



2. Conditions setting method

Set the recording conditions by the 2 DIP switchers and 1 rotary switch. After setting the switches, the recording for 85sec. can carry out by using the 2 serial registers of 1M-bit at 8kHz sampling (3-bit ADPCM 8kHz sampling).

2.1 Set MCUM of the DIP switch to OFF

The MSM6588 enters the stand-alone mode. (When MCUM is set to on, the MSM6588 enters the microcomputer interface mode.

2.2 Set RSL1 and RSl2 of the Dip switches as shown in the table below depending on the number of serial registers mounted.

RSL2	OFF		ON	
RSL1	OFF	ON	OFF	ON
Number of serial registers	256K or 512K-bit 1pc.	1M-bit 1pc.	1M-bit 2pcs.	1M-bit 4pcs.

2.3 Specify the control mode and channel number for recording by CSL1 and CSL2 of the DIP switch.

RSL2	OFF		ON	
RSL1	OFF	ON	OFF	ON
Control mode	Fixed mode			Flex mode
Number of channels	8-word	4-word	2-word	8-word

Fixed mode:

The recording time of each channel is given as the time equivalent to the memory capacity that equally divided the memory capacity of the external serial registers by the number of chnnels.

The recording of each channel can be obtained from the following equations.

$$\text{Recording time} = \frac{1.024 \times 1024\ (\text{k bit}) \times \text{Number of serial registers}}{\text{Sampling frequency (kHz)} \times 3\ (\text{bit}) \times \text{Number of channels}}\ (\text{sec.})$$

For example, the recording time for each channel with 2 serial registers on 2 channels at the sampling frequency of 8kHz (RSL1 = OFF, RSL2 = ON, CSL1 =OFF, CSL2 = ON and SAM = ON) is as shown below.

$$\text{Recording time} = \frac{1.024 \times 1024\ (\text{k bit}) \times 2}{8\ (\text{kHz}) \times 3 \times 2} = 43(\text{sec})$$

Flex mode:

The recording time of each channel becomes free within the range of the memory capacitor for the external serial registers and is recorded to ch0, ch1, ... and ch7.

2.4 Set the rotary switch (CA) to the channel to be recorded.

CA	Fixed mode			Flex mode
	8-word	4-word	2-word	8-word
0	ch0	ch0	ch0	ch0
1	ch1			ch1
2	ch2	ch1		ch2
3	ch3			ch3
4	ch4	ch2	ch1	ch4
5	ch5			ch5
6	ch6	ch3		ch6
7	ch7			ch7

2.5 Specify the sampling frequency at SAM of the DIP switch.

SAM	OFF	ON
Sampling frequency f_{sam}	$\frac{f_{OSC}}{768}$ (5.3kHz)	$\frac{f_{OSC}}{512}$ (8.0kHz)

The frequencies within the parentheses are at the original oscillation f_{OSC} = 4.096MHz.

2.6 Usually, set the PDMD of the DIP switch to ON.

OFF: The MSM6588 enters the power-down state expect recording and playback.

ON: The MSM6588 always enters the stand-by state and the time lag up to starting the playback decreases after input.

2.7 Select whether or not the voice is activated by VDS of the DIP switch

OFF: Ordinary mode, the voice is not activated.

ON: The voice is activated.

Note: When the activation of the voice is required, use the DC stabilized power supply without using the battery driving power. In the case of the battery, the power fluctuation of a few mV in starting the recording is amplified and it results in judgement that there is the voice.

3. Recording method

3.1 Turn the toggle switch on the upper right of the demonstration board to ON to engage power. The LED (power) on the lower left of the demonstration board comes on.

3.2 Set the conditions as specified in section 2 "Conditions setting method."

3.3 Set the toggle switch on the lower right of the demonstration board to REC to select the recording mode.

3.4 Press the $\overline{ST}$ button once and record the voice via the mike. During recording, the LED (MON) on the demonstration board comes on.

3.5 When the voice is recorded till the last of the channel memory, the recording automatically finishes. To stop recording halfway, press the SP button.

4. Playback method

4.1 Set the toggle switch on the lower right of the demonstration board to PLAY to select the playback mode.

4.2 Press the $\overline{ST}$ button once to start the playback. During the playback, the LED (MON) comes on.

4.3 When the playback is achieved till recorded time, the recording is automatically terminated. To step the playback halfway, press the SP button once again.

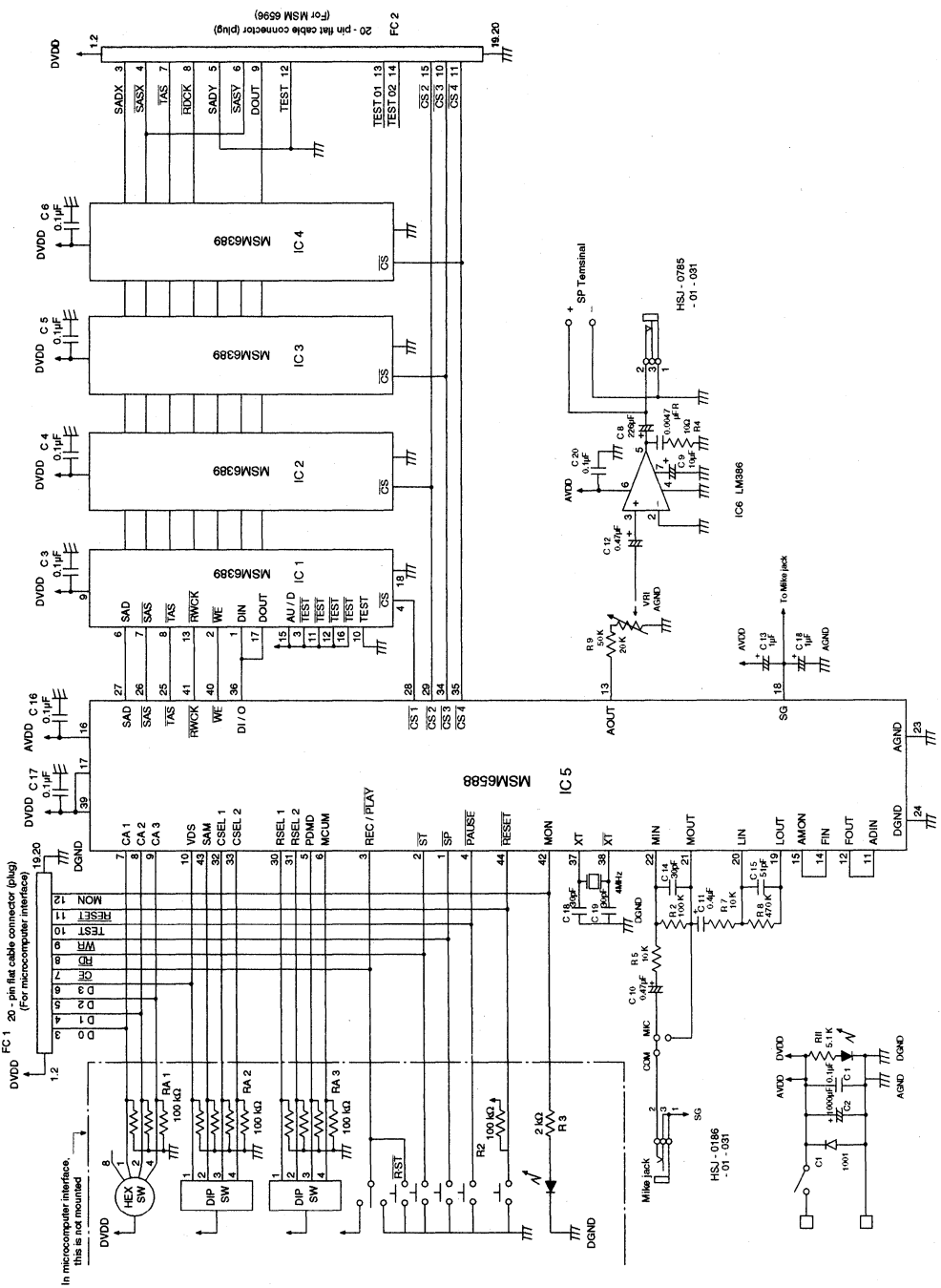
4.4 Use the volume control to adjust the playback volume.

5. Pause method of playback

5.1 During the playback, when the $\overline{PAUSE}$ button is pressed, the playback enters pause.

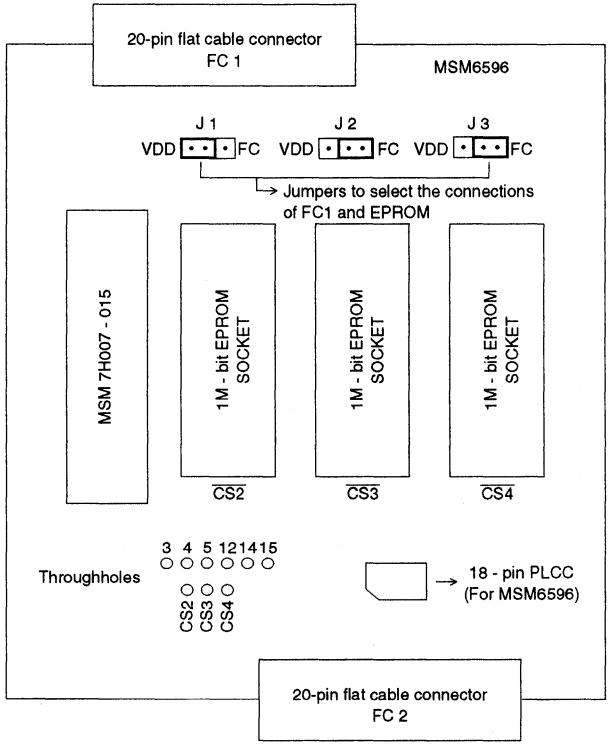
5.2 Press the $\overline{ST}$ button once again, and the playback starts again.

6. Circuit diagram



MSM6596 Demonstration Board

1. Board Outline



2. How to use Board

2.1 EPROM connnecting method

- Position to insert EPROM

  When 1 serial register is used, set the EPROMs at the positions of $\overline{CS2}$ and $\overline{CS3}$ or the positions of $\overline{CS3}$ and $\overline{CS4}$.

- Jumper setting

  When the EPROMs are set at the $\overline{CS2}$ and $\overline{CS3}$, set J1 and J2 of jumpers to the right side (FC side) and J3 of jumper to the left side (VDD side).

  When the EPROMs are set at the $\overline{CS3}$ and $\overline{CS4}$, set J2 and J3 of jumpers to the right side (FC side) and J1 of jumper to the left side (VDD side).

2.2 18-pin PLCC (for MSM6596) connecting method

- 18-pin PLCC

  Mount the MSM6596 of 18-pin PLCC

- Jumper setting

  In the evaluation of EPROM, when EPROMs are set at the positions of $\overline{CS2}$ and $\overline{CS3}$, connect the throughholes $\overline{CS2}$ and 4, and $\overline{CS3}$ and 3 by the jumper wire.

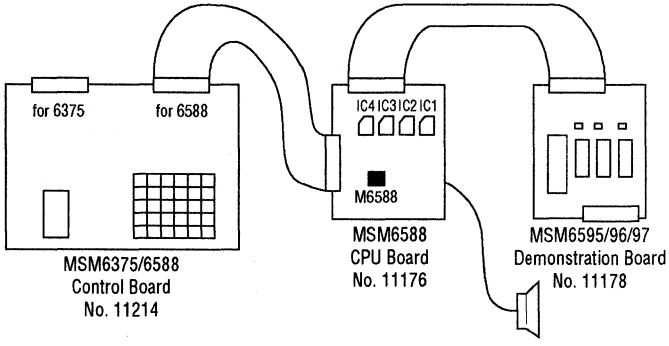
  When EPROMs are set at the positions of $\overline{CS3}$ and $\overline{CS4}$, connect the throughholes $\overline{CS3}$ and 4, and $\overline{CS4}$ and 3 by the jumper wire.

2.3 Connecting method to MSM6588 demonstration board

- When the voice of EPROM is reproduced, connect the 20-pin flat cable connector FC1 to the connector for the MSM6596 of the MSM6588 demonstration board.

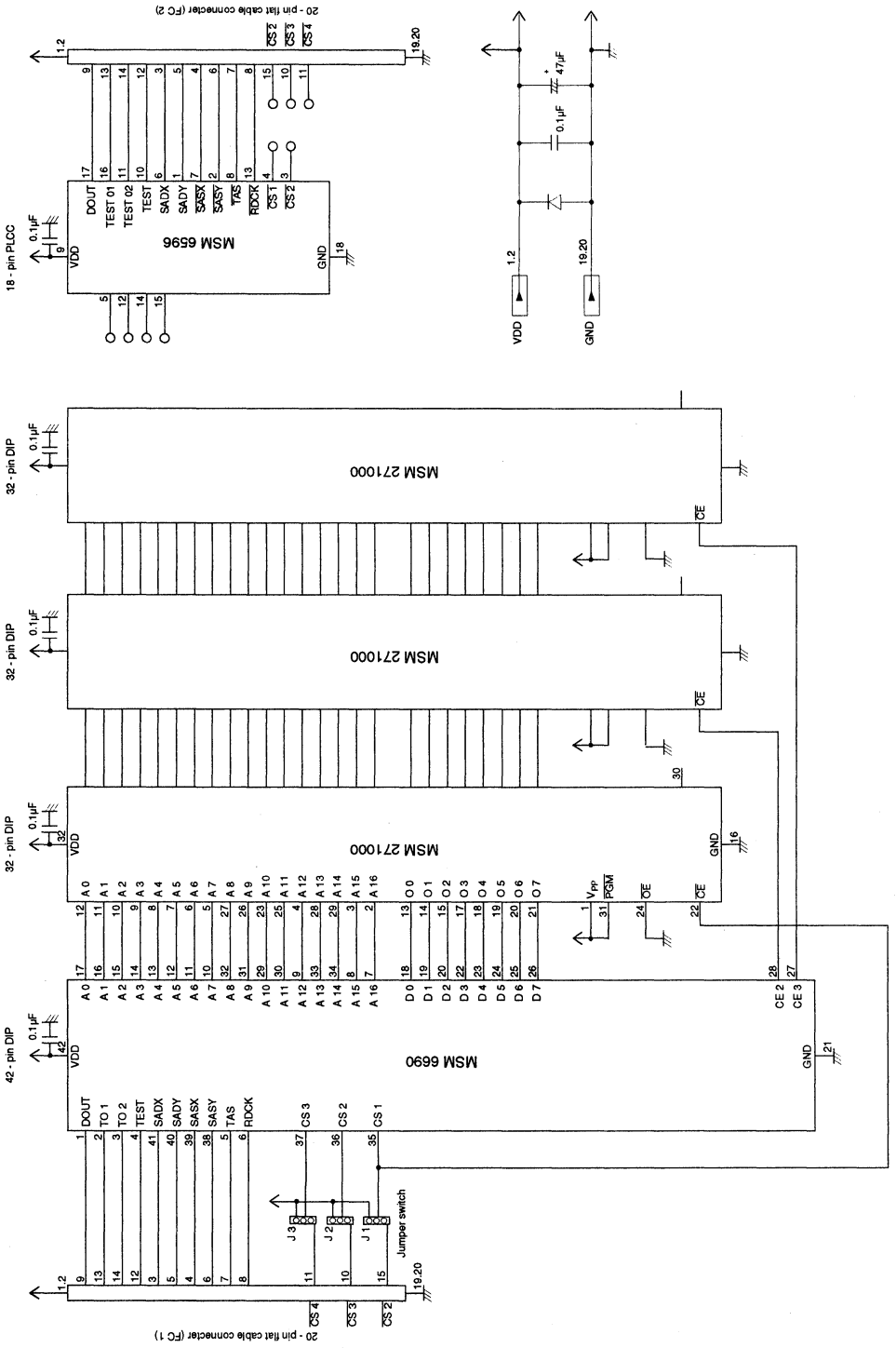
- When the voice of 18-pin PLCC is reproduced, connect the 20-pin flat cable connector FC2 to the connector for the MSM6596 of the MSM6588 demonstration board.

<Connecting Diagram>



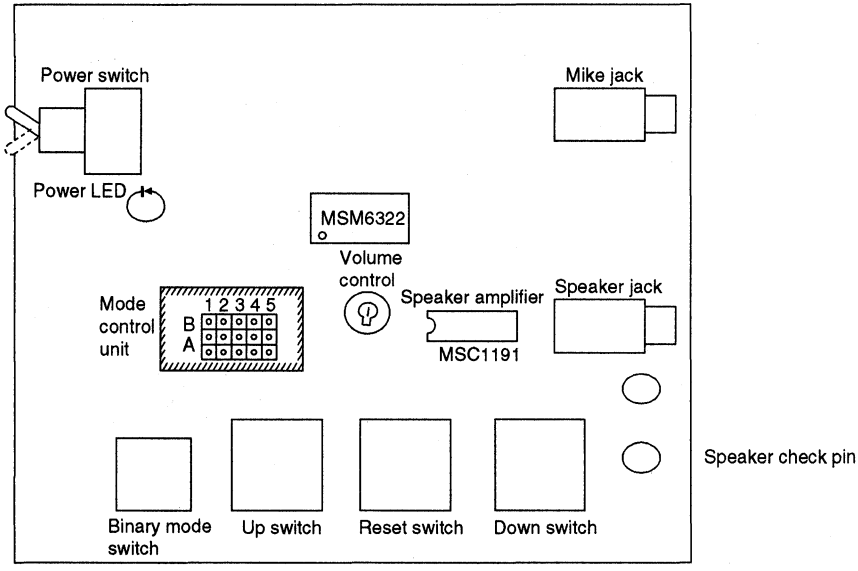
Note: When the serial register is not mounted, to IC1 on the MSM6588 CPU board (No. 11176) the circuit does not operate normally. In the meantime, when the serial register is mounted to IC2 ~ IC4, the normal operation is not obtained either.

3. Circuit diagram



MSM6322 Demonstration Board

1. Board Outline

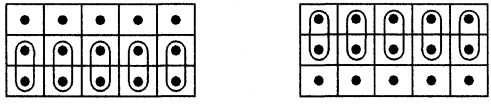


2. Operating procedure

2.1 Set the mode control unit to the mode to be used. Before changing the mode, turn power OFF. (The default setting is the UP/DOWN mode.)

The mode control unit is connected with jumper plugs. The status of the mode control unit in each mode is as follows:

UP/DOWN mode (default) BIN mode



2.2 Turn the power switch on. The power LED comes on.

3.2 UP/DOWN mode

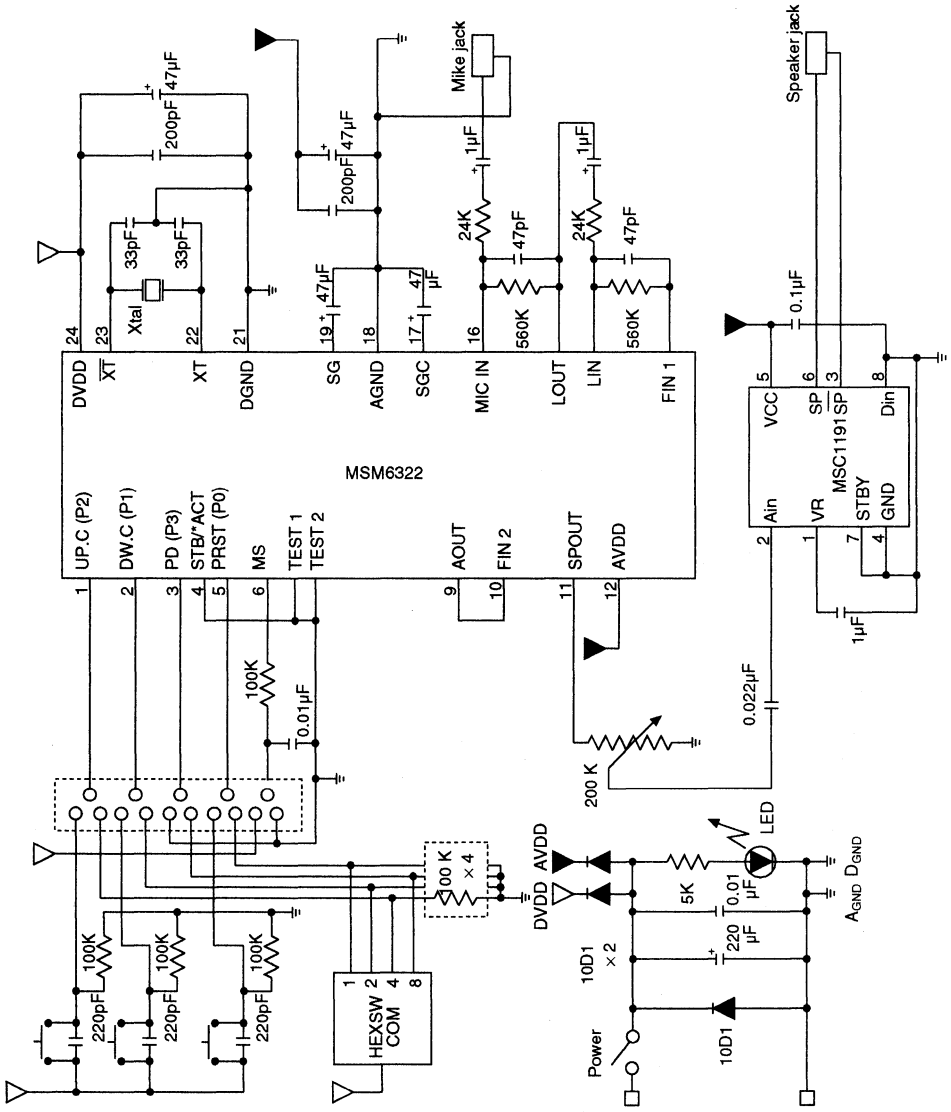
Change the voice pitch using the UP switch, DOWN switch, or RESET switch.

BIN mode

Change the voice pitch using the BIN rotary switch.

2.4 Turn the power switch off. The power LED goes off.

3. Circuit diagram



MEMO

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