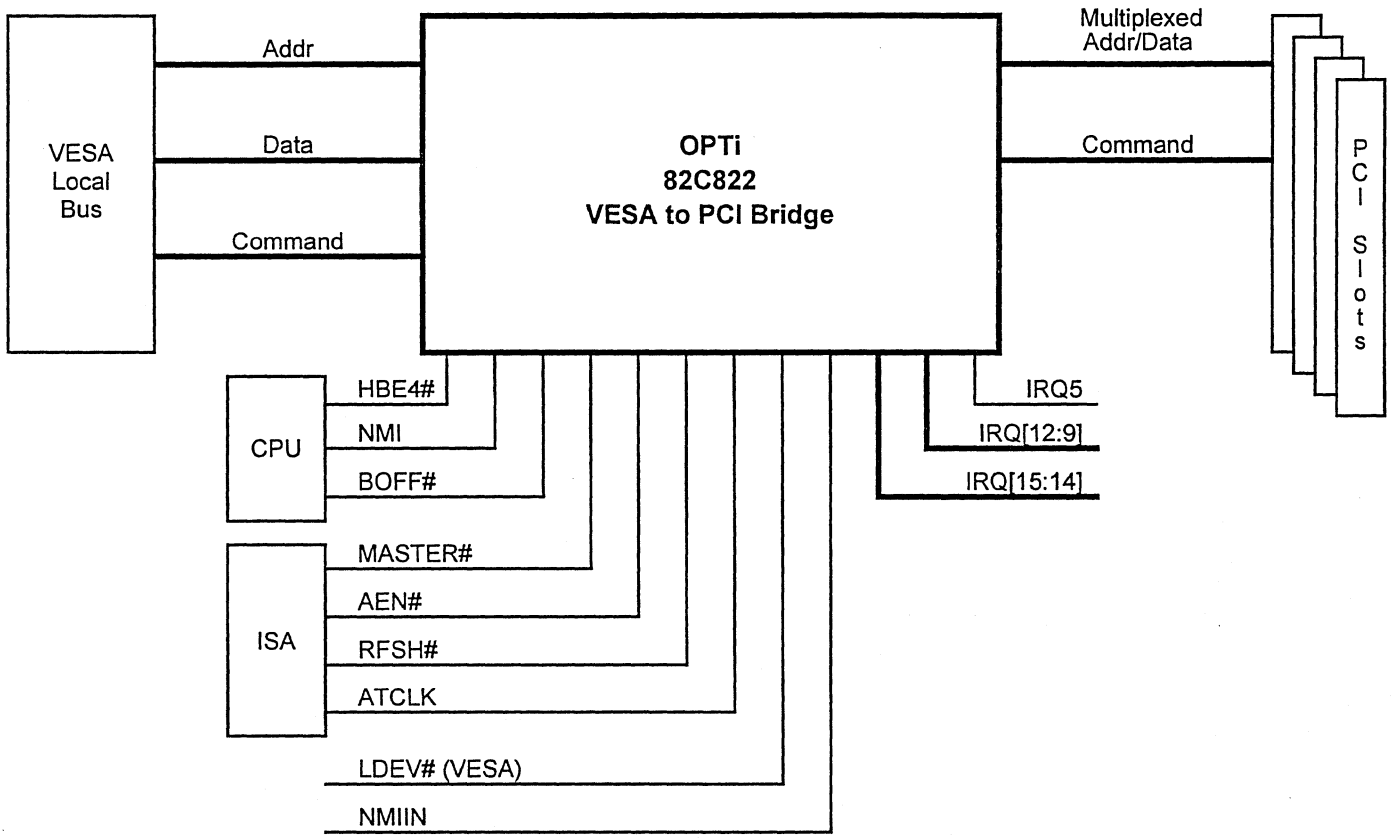
VESA Local Bus to PCI Bridge Interface

1.0 Features

- Fully compliant to the PCI V2.0 Specification
- Up to four PCI masters
- Supports system operational speeds of 25, 33, 40, and 50MHz
- Provides central arbiter to arbitrate the bus requests between:
  - host CPU
  - PCI masters
  - DMA/ISA masters
  - Refresh
- Offers programmable priority scheme for both the central arbiter and DMA channels:
  - Fixed
  - Rotating
  - Fixed/Rotating combination
- Burst mode PCI accesses to local memory support
- Combine host CPU sequential writes into PCI burst write cycles
- Interfaces with all OPTi's VL chipset solutions
- Single 208-pin PQFP (Plastic Quad Flat Pack)

Note: The text in this document applies to Mask #1285, Revision 1 Silicon of the 82C822. This document supersedes all other 82C822 data sheets.

Figure 1-1 82C822-Based System Block Diagram



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2.0 Overview

OPTi's 82C822 VESA local bus to PCI Bridge (PCIB) chip is a high integration 208-pin PQFP device designed to work with VESA VL bus compatible core logic chipsets. The 82C822 PCIB provides interface to the high performance PCI bus and is fully compliant to the PCI Version 2.0 specification. The 82C822 requires no glue logic to implement the PCI bus interface and hence it allows designers to have a highly integrated motherboard with both VESA local bus and PCI local bus support. The PCIB chip offers premium performance and flexibility for VESA VL-based desktop systems running up to 50MHz. The 82C822 PCIB can be used with OPTi's 82C802G core logic and 82C602 buffer chipsets to build a low cost and power efficient 486-based desktop solution. It also works with OPTi 82C546/547 chipset to build a high performance PCI/VL solution based on the Intel P54C processor.

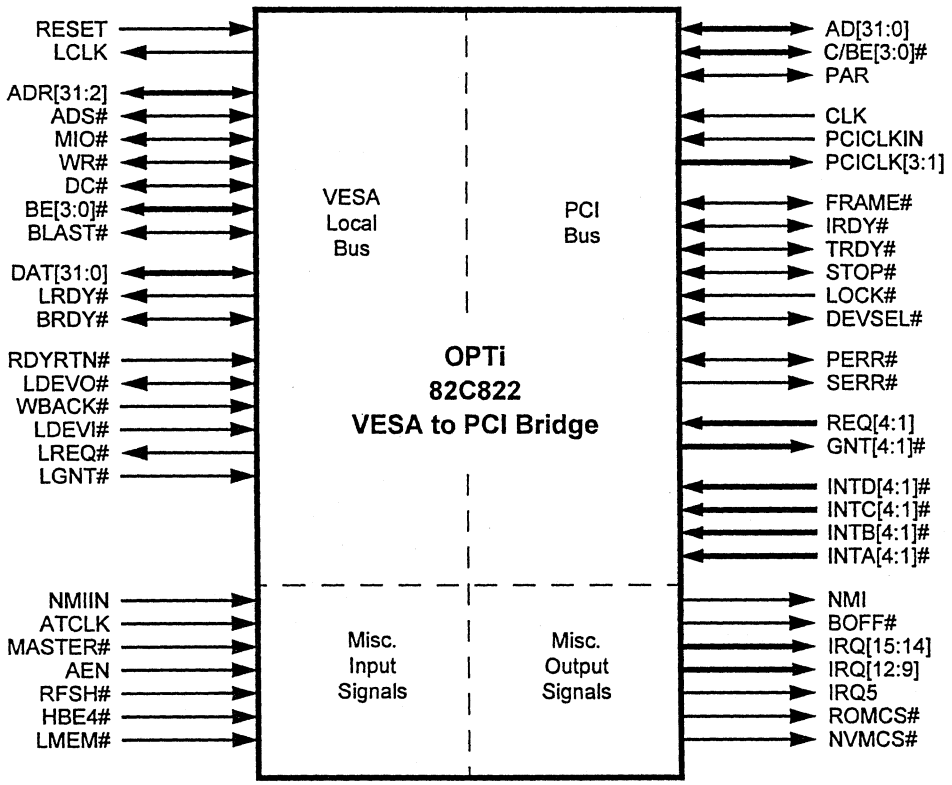
The 82C822 PCIB provides all of the control, address and data paths to access the PCI bus from the VESA Local bus (VL bus). The 82C822 provides a complete solution including data buffering, latching, steering, arbitration, DMA and master functions between the 32-bit VL bus and the 32-bit PCI bus.

The PCIB works seamlessly with the motherboard chipset bus arbiter to handle all requests of the host CPU and PCI bus masters, DMA masters, I/O relocation and refresh. Extensive register and timer support are designed into the 82C822 to implement the PCI specification.

The 82C822 is a true VESA to PCI bridge. It has the highest priority on CPU accesses after cache and system memory. It generates LDEV# automatically and then compares the addresses with its internal registers to determine whether the current cycle is a PCI cycle. When a cycle is identified as PCI cycle, the 82C822 will take over the cycle and then return RDY# to the CPU. If not, the 82C822 will give up the cycle to the local device or, in the case of an ISA slave, generate a BOFF# cycle to the CPU. This action will abort the cycle and allow the CPU to rerun the cycle.

The 82C822 includes registers to determine shadow memory space, hole locations and sizes to allow the 82C822 to determine which memory space should be local and which is located on the ISA bus. Upon access to memory, the 82C822 can determine whether or not the cycle is a PCI access by comparing the cycle with its internal registers.

Figure 2-1 82C822 Block Diagram



3.0 Signal Definitions

Figure 3-1 82C822 Pin Diagram

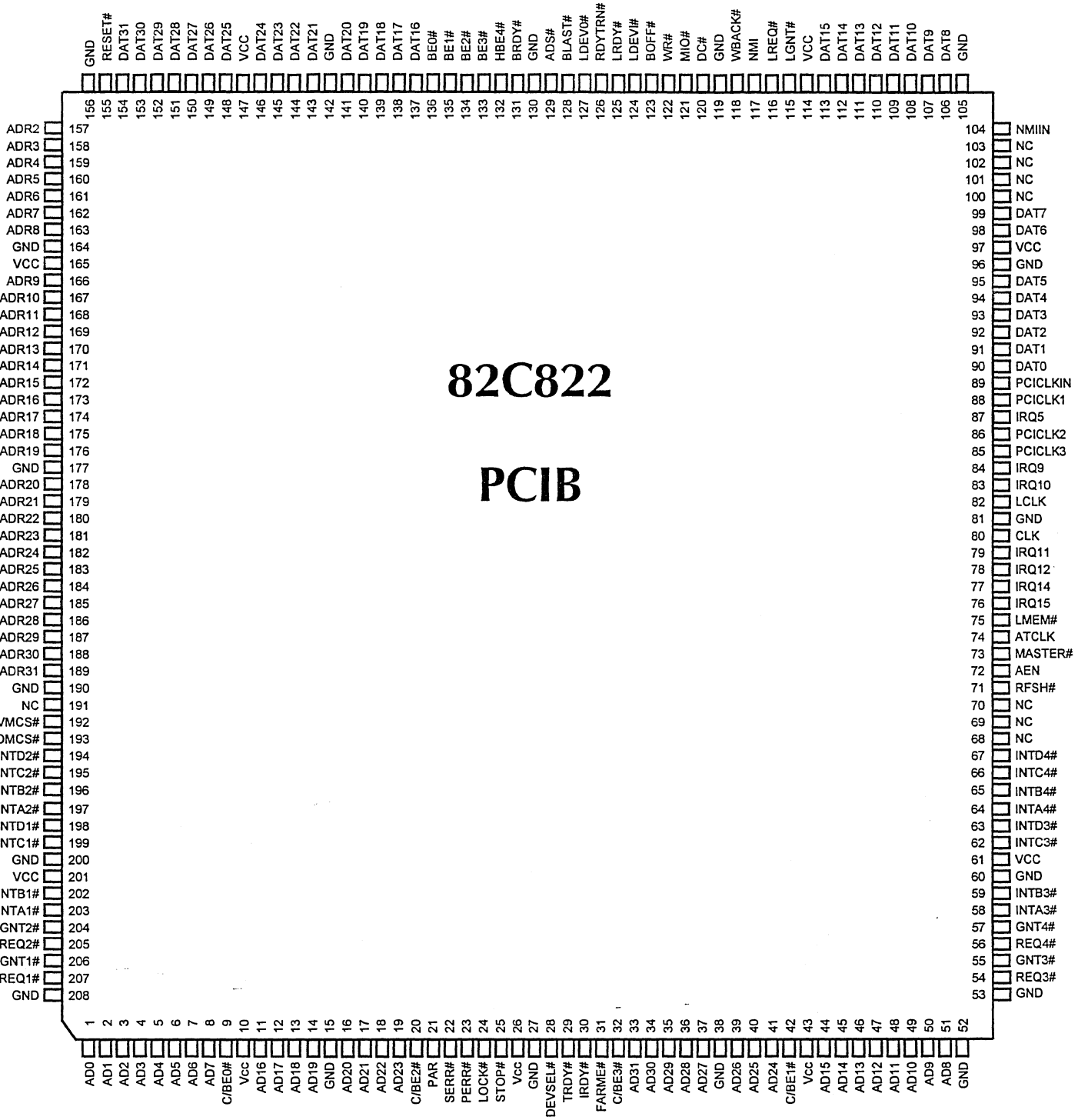


Table 3-1 82C822 Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	AD0	53	GND	105	GND	157	ADR2
2	AD1	54	REQ3#	106	DAT8	158	ADR3
3	AD2	55	GNT3#	107	DAT9	159	ADR4
4	AD3	56	REQ4#	108	DAT10	160	ADR5
5	AD4	57	GNT4#	109	DAT11	161	ADR6
6	AD5	58	INTA3#	110	DAT12	162	ADR7
7	AD6	59	INTB3#	111	DAT13	163	ADR8
8	AD7	60	GND	112	DAT14	164	GND
9	C/BE0#	61	VCC	113	DAT15	165	VCC
10	VCC	62	INTC3#	114	VCC	166	ADR9
11	AD16	63	INTD3#	115	LGNT#	167	ADR10
12	AD17	64	INTA4#	116	LREQ#	168	ADR11
13	AD18	65	INTB4#	117	NMI	169	ADR12
14	AD19	66	INTC4#	118	WBACK#	170	ADR13
15	GND	67	INTD4#	119	GND	171	ADR14
16	AD20	68	NC	120	DC#	172	ADR15
17	AD21	69	NC	121	MIO#	173	ADR16
18	AD22	70	NC	122	WR#	174	ADR17
19	AD23	71	RFSH#	123	BOFF#	175	ADR18
20	C/BE2#	72	AEN	124	LDEVI#	176	ADR19
21	PAR	73	MASTER#	125	LRDY#	177	GND
22	SERR#	74	ATCLK	126	RDYRTN#	178	ADR20
23	PERR#	75	LMEM#	127	LDEVO#	179	ADR21
24	LOCK#	76	IRQ15	128	BLAST#	180	ADR22
25	STOP#	77	IRQ14	129	ADS#	181	ADR23
26	VCC	78	IRQ12	130	GND	182	ADR24
27	GND	79	IRQ11	131	BRDY#	183	ADR25
28	DEVSEL#	80	CLK	132	HBE4#	184	ADR26
29	TRDY#	81	GND	133	BE3#	185	ADR27
30	IRDY#	82	LCLK	134	BE2#	186	ADR28
31	FRAME#	83	IRQ10	135	BE1#	187	ADR29
32	C/BE3#	84	IRQ9	136	BE0#	188	ADR30
33	AD31	85	PCICLK3	137	DAT16	189	ADR31
34	AD30	86	PCICLK2	138	DAT17	190	GND
35	AD29	87	IRQ5	139	DAT18	191	NC
36	AD28	88	PCICLK1	140	DAT19	192	NVMCS#
37	AD27	89	PCICLKIN	141	DAT20	193	ROMCS#
38	GND	90	DAT0	142	GND	194	INTD2#
39	AD26	91	DAT1	143	DAT21	195	INTC2#
40	AD25	92	DAT2	144	DAT22	196	INTB2#
41	AD24	93	DAT3	145	DAT23	197	INTA2#
42	C/BE1#	94	DAT4	146	DAT24	198	INTD1#
43	VCC	95	DAT5	147	VCC	199	INTC1#
44	AD15	96	GND	148	DAT25	200	GND
45	AD14	97	VCC	149	DAT26	201	VCC
46	AD13	98	DAT6	150	DAT27	202	INTB1#
47	AD12	99	DAT7	151	DAT28	203	INTA1#
48	AD11	100	NC	152	DAT29	204	GNT2#
49	AD10	101	NC	153	DAT30	205	REQ2#
50	AD9	102	NC	154	DAT31	206	GNT1#
51	AD8	103	NC	155	RESET#	207	REQ1#
52	GND	104	NMIIN	156	GND	208	GND

Table 3-2 82C822 Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
AD0	1	ADR22	180	DAT27	150	IRQ12	78
AD1	2	ADR23	181	DAT28	151	IRQ14	77
AD2	3	ADR24	182	DAT29	152	IRQ15	76
AD3	4	ADR25	183	DAT30	153	LCLK	82
AD4	5	ADR26	184	DAT31	154	LDEVO#	127
AD5	6	ADR27	185	DC#	120	LDEVI#	124
AD6	7	ADR28	186	DEVSEL#	28	LGNT#	115
AD7	8	ADR29	187	FRAME#	31	LMEM#	75
AD8	51	ADR30	188	GND	15	LOCK#	24
AD9	50	ADR31	189	GND	27	LRDY#	125
AD10	49	ADS#	129	GND	38	LREQ#	116
AD11	48	AEN	72	GND	52	MASTER#	73
AD12	47	ATCLK	74	GND	53	MIO#	121
AD13	46	BE0#	136	GND	60	NC	68
AD14	45	BE1#	135	GND	81	NC	69
AD15	44	BE2#	134	GND	96	NC	70
AD16	11	BE3#	133	GND	105	NC	100
AD17	12	BLAST#	128	GND	119	NC	101
AD18	13	BOFF#	123	GND	130	NC	102
AD19	14	BRDY#	131	GND	142	NC	103
AD20	16	C/BE0#	9	GND	156	NC	191
AD21	17	C/BE1#	42	GND	164	NMI	117
AD22	18	C/BE2#	20	GND	177	NMIIN	104
AD23	19	C/BE3#	32	GND	190	NVMCS#	192
AD24	41	CLK	80	GND	200	PAR	21
AD25	40	DAT0	90	GND	208	PCICLK1	88
AD26	39	DAT1	91	GNT1#	206	PCICLK2	86
AD27	37	DAT2	92	GNT2#	204	PCICLK3	85
AD28	36	DAT3	93	GNT3#	55	PCICLKIN	89
AD29	35	DAT4	94	GNT4#	57	PERR#	23
AD30	34	DAT5	95	HBE4#	132	RDYRTN#	126
AD31	33	DAT6	98	INTA1#	203	REFRESH#	71
ADR2	157	DAT7	99	INTA2#	197	REQ1#	207
ADR3	158	DAT8	106	INTA3#	58	REQ2#	205
ADR4	159	DAT9	107	INTA4#	64	REQ3#	54
ADR5	160	DAT10	108	INTB1#	202	REQ4#	56
ADR6	161	DAT11	109	INTB2#	196	RESET#	155
ADR7	162	DAT12	110	INTB3#	59	ROMCS#	193
ADR8	163	DAT13	111	INTB4#	65	SERR#	22
ADR9	166	DAT14	112	INTC1#	199	STOP#	25
ADR10	167	DAT15	113	INTC2#	195	TRDY#	29
ADR11	168	DAT16	137	INTC3#	62	VCC	10
ADR12	169	DAT17	138	INTC4#	66	VCC	26
ADR13	170	DAT18	139	INTD1#	198	VCC	43
ADR14	171	DAT19	140	INTD2#	194	VCC	61
ADR15	172	DAT20	141	INTD3#	63	VCC	97
ADR16	173	DAT21	143	INTD4#	67	VCC	114
ADR17	174	DAT22	144	IRDY	30	VCC	147
ADR18	175	DAT23	145	IRQ5	87	VCC	165
ADR19	176	DAT24	146	IR9	84	VCC	201
ADR20	178	DAT25	148	IRQ10	83	WBACK#	118
ADR21	179	DAT26	149	IRQ11	79	WR#	122

3.1 Signal Descriptions

Signal Name	Pin No.	Signal Type	Signal Description
3.1.1 VESA Local Bus Interface Signals			
RESET#	155	I	Active low Reset Input
LCLK	82	I	VESA Local Bus Clock
ADS#	129	I/O	Address Data Strobe: Normally an input, this signal is only driven during PCI bus master cycles. ADS# is tristated when WBACK# is sampled active. This signal needs to be reasserted after WBACK# is released in order to restart the cycle.
MIO#	121	I/O	Memory or I/O Status: Normally an input, this signal is an output during PCI bus master cycles. This signal is tristated when WBACK# is sampled active.
WR#	122	I/O	Write or Read Status: Normally an input, this signal is an output during PCI bus master cycles. This signal is tristated when WBACK# is sampled active.
DC#	120	I/O	Data or Code Status: Normally an input, this signal is an output during PCI bus master cycles. This signal is tristated when WBACK# is sampled active.
BE[3:0]#	133:136	I/O	Byte Enables bits 3 through 0: Normally inputs, these signals are outputs during PCI bus master cycles. They are tristated when WBACK# is sampled active.
BLAST#	128	I/O	Burst Last: Normally an input, this signal is an output during PCI bus master cycles. This signal is tristated when WBACK# is sampled active.
DAT[31:0]	154:148, 146:143, 141:137, 113:106, 99:98, 95:90	I/O	Data Lines bits 31 through 0: Normally inputs, these pins are outputs during CPU/ VESA/DMA/ISA master reads from PCI bus slaves (this includes reading the configuration registers of the 82C822) or during PCI bus master write cycles. These pins are tristated when WBACK# is sampled active.
ADR[31:2]	189:178, 176:166, 163:157	I/O	Address Lines bits 31 through 2: Normally inputs, these signals are outputs during PCI bus master cycles. They are tristated when WBACK# is sampled active.

Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
LDEVO#	127	I/O	Local Device Output: this signal is usually connected to the LDEV# input pin of the OPTi VL chipset. When used as an output, LDEVO# is normally asserted in the next clock after ADS#, except during a restarted cycle due to BOFF# being asserted in the previous cycle. During DMA/ISA bus master cycles, the assertion of LDEVO# is dependent on LMEM#, LDEVI#, the enable bit of the DMA/ISA bus master to PCI slave access, and general purpose decoding blocks specified in the configuration register. The assertion of LDEVO# for DMA/ISA bus master cycles is as follows: **LMEM# LDEVI# LDEVO#** 0 1 1 1 0 0 1 1 0 (if enable bit = 1 or 0 and the access address is falling into the region specified in the general purpose decoding blocks) 1 1 1 (if enable bit = 0 and the access address is not falling into the region specified in the general purpose decoding blocks) As an input, it is latched at the trailing edge of the reset time and used to determine the sampling point of LMEM# and LDEVI#. If sampled high during reset, the end of the first T2 is used as the sampling point, otherwise the end of the second T2 is used as the sampling point.
LRDY#	125	O	Local Ready: This signal is asserted when: 1) A CPU/VESA/DMA/ISA master accesses a PCI bus slave. 2) A CPU/VESA/PCI bus master accesses an ISA slave (LRDY# is returned to terminate the back-off cycle). 3) A PCI bus master accesses a PCI bus slave (in this case, LRDY# is asserted to terminate the cycle on the host bus).
BRDY#	131	I/O	Burst Ready: Normally an input, this signal is asserted when a CPU/VESA master accesses a PCI bus slave and the cycle is burst-able.
RDYRTN#	126	I	Ready Return: This signal is used by the 82C822 as a handshake to acknowledge the completion of the current cycle.
WBACK#	118	I	Write-back: When WBACK# is active, the 82C822 floats all the address, data, and control signals which are driven onto the host bus during a PCI bus master cycle. The 82C822 needs to resume the back-off cycle when WBACK# becomes inactive again.
LREQ#	116	O	Local Bus Request: This signal, in conjunction with LGNT#, is used to gain control of the host bus. LREQ# goes active when any one of the PCI bus masters asserts the REQn# to request the host bus.

Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
LGNT#	115	I	Local Bus Grant: This signal, in conjunction with LREQ#, is used to gain control of the host bus. Upon receiving LGNT#, the 82C822 grants the bus request by asserting GNTn# to one of the PCI bus masters. The active PCI bus master can be preempted by removing this signal.
3.1.2 PCI Interface Signals			
CLK	80	I	Clock: This signal is used to provide timing for all transactions on the PCI bus. The clock source for this input can be the same input as LCLK for the synchronized mode, or the feedback of PCICLK or the external oscillator.
PCICLKIN	89	I	PCI Clock Input: This clock input is used to generate the PCICLK[3:1] signals.
PCICLK[3:1]	85, 86, 88	O	PCI Clock [3:1]: In the asynchronous mode, these signals are used as the clock inputs to the PCI slots and should be fedback to the CLK input (pin 80).
AD[31:0]	33:37, 39:41, 19:16, 14:11, 44:51, 8:1	I/O	Multiplexed Address and Data Lines, bits 31 through 0: These pins are the multiplexed PCI address and data lines. During the address phase, these pins are inputs for PCI bus master cycles; otherwise they are outputs. During the data phase, these pins are inputs during PCI bus master write cycles or during CPU/VESA/DMA/ISA reads from a PCI bus slave; otherwise they are outputs.
C/BE[3:0]#	32, 20, 42, 9	I/O	Bus Command and Byte Enables, bits 3 through 0: These pins are the multiplexed PCI command and byte enable lines. Normally outputs, these pins are inputs during PCI bus master cycles.
PAR	21	I/O	Parity: This signal is an input either during PCI bus master cycles for address and write data phases or during PCI bus slave cycles for read data phases; otherwise it is an output.
FRAME#	31	I/O	Cycle Frame: This pin is driven by PCI bus masters to indicate the beginning and duration of an access. Normally an input, FRAME# is driven during CPU/VESA/ DMA/ISA master accesses to PCI bus slaves.
IRDY#	30	I/O	Initiator Ready: This signal is asserted by PCI bus masters to indicate the ability to complete the current data phase of the transaction. Normally an input, this pin is driven during CPU/VESA/DMA/ISA master accesses to PCI bus slaves.
TRDY#	29	I/O	Target Ready: This pin is asserted by the target to indicate the ability to complete the current data phase of the transaction. Normally an input, this pin is driven during PCI bus master accesses to local memory, VESA/ISA slaves, and the configuration register inside the 82C822.
STOP#	25	I/O	Stop: This signal is used by the target to request the master to stop the current transaction. Normally an input, this signal is driven during PCI bus master accesses to local memory and VESA/ISA slaves.
LOCK#	24	I	Lock: This signal is used to indicate an atomic operation that may require multiple transactions to complete. Since the 82C822 will never assert this signal, it is always an input.

Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
DEVSEL#	28	I/O	Device Select: This pin is an output when the 82C822 decodes its address as the target of the current access via either positive or negative decoding; otherwise it is an input.
INTD[4:1]#, INTC[4:1]#, INTB[4:1]#, INTA[4:1]#	67, 63, 194, 198, 66, 62, 195, 199, 65, 59, 196, 202, 64, 58, 197, 203	I	PCI Interrupt Lines D-A for Slots 4-1: These signals are used to generate synchronous interrupt requests to the CPU via the programmable interrupt controllers.
PERR#	23	I/O	Parity Error: This pin is used to report data parity errors during all PCI transactions except during a Special Cycle. Normally an input, PERR# is driven when data parity errors occur either during a PCI bus master write cycle or during a CPU/VESA/DMA/ISA master read from a PCI slave.
SERR#	22	OD	System Error: This signal is used to report address parity errors, or data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. This pin is an open drain.
REQ[4:1]#	56, 54, 205, 207	I	Request Lines, bits 4 through 1: These signals are used by PCI bus masters to request use of the PCI bus.
GNT[4:1]#	57, 55, 204, 206	O	Grant Lines, bits 4 through 1: These signals are used to indicate to a PCI bus master that the access to the bus has been granted.
3.1.3 Miscellaneous Interface Signals			
LDEVI#	124	I	Local Device Input: This input is an ANDed signal of all LDEV# signals from VESA bus slaves; it is used to indicate to the 82C822 whether the current access is to VESA slave.
NMI	117	O	Non-Maskable Interrupt: This output is asserted in response to an active PERR# or SERR# if the enable bit of the NMI generation for an active PERR# or SERR is set. NMI will not be asserted if bit 7 of Port 70 is set to 1. If the NMIIN input pin is connected to the NMI of the other chipset, then this output will go active in response to an active NMIIN also.
NMIIN	104	*I*	Non-Maskable Interrupt Input: This input is the non-maskable interrupt input signal generated from the other chipset. The 82C822 will combine this input with its internal NMI signal and generate a new NMI to the CPU. In the case where this pin is not used, an external pull-down resistor is recommended.
BOFF#	123	O	Back-Off: This output is asserted when the assumed destination of the access for the current cycle turns out to be wrong and the cycle needs to be restarted in order to access the right target; it is asserted during a CPU or VESA bus master cycle to abort the cycle if the current access is to an ISA slave. LDEVO# is asserted as well.
ATCLK	74	I	ISA AT clock: The 8MHz ISA AT clock.

Signal Descriptions (Cont.)

Signal Name	Pin No.	Signal Type	Signal Description
MASTER#	73	I	ISA Master Cycle: This input is used to indicate to the 82C822 the current cycle is an ISA bus master cycle.
AEN	72	I	ISA Address Enable: This input is used to indicate to the 82C822 that the current cycle is either a DMA or refresh cycle.
RFSH#	71	I	ISA Refresh: An input signal used to indicate to the 82C822 that the current cycle is a refresh cycle.
HBE4#	132	I	CPU Byte Enable 4: This signal is used only with Pentium chipsets.
LMEM#	75	I	Local Memory: When the enable bit at the top of the local memory decoding is disabled, this input is used to indicate to the 82C822 if the current access is to local memory. When the enable bit at the top of the local memory decoding is enabled, then internal decoding result for LMEM# is used and this input pin is ignored.
IRQ[15:14], IRQ[12:9], IRQ5	76:79, 83, 84, 87	OD	PIC Interrupt Request Lines, bits 15, 14, 12 through 9, and 5: These outputs are connected to the PC-compatible programmable interrupt controllers (PIC) to generate asynchronous interrupts to the CPU in response to INTD[4:1]#, INTC[4:1]#, INTB[4:1]#, and INTA[4:1]#. The routing of each PCI interrupt line to the PC-compatible interrupts is controlled by four bits specified in the configuration register.
ROMCS#	193	O	PCI ROM BIOS Chip Select: Used to select the BIOS ROM used to configure the chipset.
NVMCS#	192	O	Non-Volatile Memory Chip Select: This output signal is used to select the non-volatile memory in which the system information is stored; the memory address space for the non-volatile memory is always a 16KB chuck and between C8000h and DFFFFh. It is used to select any ROM located in the memory address space from E0000h to EFFFFh.
3.1.4 Power, Ground, and Reserved Pins			
VCC	10, 26, 43, 61, 97, 114, 147, 165, 201	PWR	Power Connection
GND	15, 27, 38, 52, 53, 60, 81, 96, 105, 119, 130, 142, 156, 164, 177, 190, 200, 208	GND	Ground Connection
NC	68:70, 100:103, 191		No Connection: These pins are reserved.

4.0 Functional Description

The following sub-sections will explain the various cycle operations the 82C822 PCIB performs to determine which memory space should be local and which is located on the ISA bus.

4.1 CPU Cycles

Cache/DRAM Accesses

The CPU begins the cycle. The 82C822 asserts LDEVO# on the next clock in response to LADS# (VESA local bus ADS#). In the OPTi Pentium chipsets, LADS# will not be generated for a local memory cycle and therefore, LDEVO# will not be generated by the 82C822. In the OPTi 486 chipsets, the CPU will generate LADS# (LADS# and CPU ADS# are the same in the 486 implementation). The 82C822 will generate LDEVO#, but this will be ignored by the OPTi 486 chipsets during a local memory cycle. In this case, the 82C822 will deassert LDEVO# after the last BRDY#.

VESA Slave Accesses

The CPU begins the cycle. The 82C822 asserts LDEVO# on the next clock in response to ADS#. The VESA slave willgenerate LDEVI# to the 82C822 at the end of the first T2 or second T2 (depending on the VL speed). At this poin, the 82C822 will keep asserting LDEVO# until the VESA slave returns LRDY#/LBRDY#.

PCI Slave Accesses

The CPU begins the cycle. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is a PCI slave cycle and starts the PCI cycle after synchronization. Data is latched into the 82C822 for read cycles. The 82C822 completes the cycle, returns LRDY#, and deasserts LDEVO#.

ISA slave accesses

The CPU begins the cycle. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is not a local memory or VESA slave cycle and starts the PCI cycle after synchronization. The 82C822 receives master-abort termination and asserts LRDY# and BOFF# at the same time after synchronization. The 82C822 returns LRDY# and deasserts LDEVO# on the next clock. The CPU restarts the aborted cycle. The 82C822 ignores the restarted cycle by keeping LDEVO# inactive. The OPTi VL chipset returns RDY# to the CPU at the end of the AT cycle.

4.2 VESA Master Cycles

Cache/DRAM Accesses

The VL bus master begins the cycle. The 82C822 asserts LDEVO# on the next clock. The OPTi VL chipset determines that the cycle is a local memory cycle and ignores LDEVO#. The OPTi VL chipset will then return BRDY# after the data is transferred. The 82C822 also determines that the cycle is a local memory cycle and takes no action other than to deassert LDEVO# after the last BRDY#.

VESA Slave Accesses

The VL bus master begins the cycle. The 82C822 asserts LDEVO# on the next clock. It then samples LDEVI# and, determining that the cycle is a VESA cycle, takes no further action. The VESA slave will then return LRDY#/LBRDY# after the data is transferred. RDYRTN# will be generated by the OPTi VL chipset. The 82C822 deasserts LDEVO# after the last LBRDY#.

PCI slave accesses

The VL bus master begins the cycle. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is a PCI slave cycle and starts the PCI cycle after synchronization. Data is latched into the 82C822 for read cycles. The 82C822 returns LRDY# to the OPTi VL chipset and deasserts LDEVO#.

ISA Slave Accesses

The VL bus master begins the cycle. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is not a local memory or VESA slave cycle and starts the PCI cycle after synchronization. The 82C822 receives a master-abort termination and asserts LRDY# and BOFF# at the same time after synchronization. The 82C822 returns LRDY# and deasserts LDEVO# on the next clock. The CPU restarts the aborted cycle. The 82C822 ignores the restarted cycle by keeping LDEVO# inactive. The OPTi VL chipset returns RDY# to the CPU at the end of the AT cycle.

4.3 PCI Master Cycles

Cache/DRAM Accesses

The PCI master begins the cycle by asserting PCI REQ# to the 82C822. The 82C822 asserts LREQ# to the OPTi VL chipset after arbitration of the bus requests from the PCI bus masters. The 82C822 receives LGNT# from the OPTi VL chipset and generates the appropriate VL bus signals according to the PCI command, address, and status lines. The 82C822 asserts LDEVO# on the next clock. The OPTi VL chipset determines that the cycle is a local memory cycle. The 82C822 also determines that the cycle is a local memory cycle and asserts DEVSEL# to claim the cycle. Data is latched into the 82C822 for read cycles. The OPTi VL chipset returns RDY# to the 82C822 and the 82C822 deasserts LDEVO#. The 82C822 returns TRDY# to the PCI bus master after synchronization. The 82C822 deasserts DEVSEL# after the last transfer.

VESA Slave Accesses

The PCI master begins the cycle by asserting PCI REQ# to the 82C822. The 82C822 asserts LREQ# to the OPTi VL chipset after arbitration of the bus requests from the PCI bus masters. The 82C822 receives LGNT# from the OPTi VL chipset and generates the appropriate VL bus signals according to the PCI command, address, and status lines. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is a VESA slave cycle and asserts DEVSEL# to claim the cycle. Data is latched into the 82C822 for read cycles. The OPTi VL chipset returns RDY# to the 82C822 and the PCIB deasserts LDEVO#. The 82C822 returns TRDY# to the PCI bus master after synchronization. The 82C822 deasserts DEVSEL# after the last transfer.

PCI Slave Accesses

The PCI master begins the cycle by asserting PCI REQ# to the 82C822. The 82C822 asserts LREQ# to the OPTi VL chipset after arbitration of the bus requests from the PCI bus masters. The 82C822 receives LGNT# from the OPTi VL chipset and generates the appropriate VL bus signals according to the PCI command, address, and status lines. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is a PCI slave cycle and waits for DEVSEL# from the PCI slave. On receiving DEVSEL#, the 82C822 generates LRDY# to the OPTi VL chipset. The 82C822 deasserts LDEVO# after RDY#. Any data latched by the 82C822 for read cycles is ignored.

ISA Slave Accesses

The PCI master begins the cycle by asserting PCI REQ# to the 82C822. The 82C822 asserts LREQ# to the OPTi VL chipset after arbitration of the bus requests from the PCI bus masters. The 82C822 receives LGNT# from the OPTi VL chipset and generates the appropriate VL bus signals according to the PCI command, address, and status lines. The 82C822 asserts LDEVO# on the next clock. It then determines that the cycle is a not a local memory or VESA slave cycle and, detecting no DEVSEL# from the PCI slave, realizes the cycle is an ISA slave cycle. The 82C822 then asserts LRDY# to the 802G and generates an internal BOFF# signal after synchronization. RDY# is returned to the 82C822 when LRDY# is generated. The 82C822 deasserts LDEVO# the next clock after RDY#. The 82C822 restarts the aborted cycle by asserting the VL bus address and command signals, keeping LDEVO# high for the restarted cycle. The OPTi VL chipset forwards the restarted cycle to the AT bus. The OPTi VL chipset returns LRDY# to the 82C822 at the end of the AT cycle. The data is latched into the 82C822 for the read cycle when it returns RDY# to the OPTi VL chipset. The 82C822 returns TRDY# to the PCI master after synchronization. The 82C822 deasserts DEVSEL# after the data is transferred.

4.4 DMA/ISA Master Cycles

Cache/DRAM Accesses

The OPTi VL chipset determines that the DMA/ISA master cycle is accessing local memory once the command is asserted. The OPTi VL chipset asserts MEMCS16#. LADS# will not be generated by the OPTi VL chipset. No action is taken by the 82C822.

VESA Slave Accesses

The OPTi VL chipset determines that the DMA/ISA master cycle is a not a local memory cycle once the command is asserted. The OPTi VL chipset will generate the VESA local bus command lines. In response to LADS#, the 82C822 will assert LDEVO#. The 82C822 will receive LDEVI# by the next or subsequent clock. The OPTi chipset pulls IOCHRDY low to stall the command. The OPTi VL chipset samples LDEVO# active. If the cycle is a read cycle, the OPTi VL chipset will start driving the SD bus. LRDY# is asserted by the VESA slave. The OPTi VL chipset releases IOCHRDY and asserts RDY# at the end of the command after synchronization. The 82C822 takes no action other than to deassert LDEVO# as soon as LDEVI# goes inactive. The OPTi VL chipset deasserts MEMCS16# when LDEVO# goes inactive.

PCI Slave Accesses

The OPTi VL chipset determines that the DMA/ISA master cycle is a not a local memory cycle once the command is asserted. The OPTi VL chipset will generate the VESA local bus command lines. In response to LADS#, the 82C822 will assert LDEVO#. The OPTi VL chipset pulls IOCHRDY low to stall the command. The OPTi VL chipset samples LDEVO# active and pulls MEMCS16# low if the command is not an I/O cycle. The 82C822 starts the PCI cycle after synchronization. Data is latched into the 82C822 for read cycles when both TRDY# and IRDY# are active. The 82C822 asserts LRDY# after synchronization. The OPTi VL chipset releases IOCHRDY and asserts RDY# at the end of the command after synchronization. The 82C822 deasserts LDEVO# at the end of the bus cycle. The OPTi chipset deasserts MEMCS16# when LDEVO# goes inactive.

ISA Slave Accesses

The OPTi VL chipset determines that the DMA/ISA master cycle is a not a local memory cycle once the command is asserted. The OPTi VL chipset will generate the VESA local bus command lines. In response to LADS#, the 82C822 will assert LDEVO#. The OPTi VL chipset pulls IOCHRDY low to stall the command. The OPTi VL chipset samples LDEVO# active and pulls MEMCS16# low if the command is not an I/O cycle. The 82C822 starts the PCI cycle after synchronization. The PCI bridge will receive the master-abort termination.

LRDY# is asserted and LDEVO# is deasserted at the same time by the 82C822 after synchronization. The OPTi VL chipset releases IOCHRDY and remains tristated on the SD bus. The OPTi VL chipset asserts RDY# at the end of the command after synchronization.

4.5 Guidelines to Program the 82C822

The following briefly describes how to access the 82C822 and the PCI devices on the slots. The 82C822 uses the PCI Configuration Mechanism #1 to access the configuration spaces. Two double-word I/O locations are used in this mechanism. The first double-word location (CF8h) references a read/write register that is name CONFIG_ADDRESS. The second double-word address (CFCh) references a register name CONFIG_DATA. The general mechanism for accessing the configuration space is to write a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, and the configuration register in that device being accessed. A read or write to CONFIG_DATA will then cause the 82C822 to translate that CONFIG_ADDRESS value to the requested configuration cycle on the PCI bus.

Below is an example to read the address offset 00h of the 82C822 configuration space:

```
MOV   EAX,80008000h   ;specifies device, function,
                      register number
MOV   DX,0CF8h        ;CONFIG_ADDRESS
OUT   EDX,EAX
MOV   DX,0CFCh        ;CONFIG_DATA
IN    EAX,EDX
```

The content of the CONFIG_ADDRESS showing above possesses the following meanings (device number 10000b means OPTi 82C822 chose AD16 as the IDSEL) as shown in Table 4-1.

In the OPTi 82C802G/82C822 demo design, we chose AD17, AD18, and AD19 as the IDSEL line for the three PCI slots. Tables 4-2 through 4-4 show the address to access the PCI slots number 1, 2, and 3, accordingly.

Table 4-1 CONFIG_ADDRESS Example

31	30 24	23 16	15 11	10 8	7 2	1	0
1	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	0000000	00000000	10000	000	000000	0	0
80h		00h	80h		00h		

Table 4-2 PCI Slot 1 Example

31	30 24	23 16	15 11	10 8	7 2	1	0
1	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	0000000	00000000	10001	000/xxx	xxxxxx	0	0
80h		00h	88h/8xh		xxh		

Table 4-3 PCI Slot 2 Example

31	30 24	23 16	15 11	10 8	7 2	1	0
1	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	0000000	00000000	10010	000/xxx	xxxxxx	0	0
80h		00h	90h/9xh		xxh		

Table 4-4 PCI Slot 3 Example

31	30 24	23 16	15 11	10 8	7 2	1	0
1	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	0000000	00000000	10011	000/xxx	xxxxxx	0	0
80h		00h	98h/9xh		xxh		

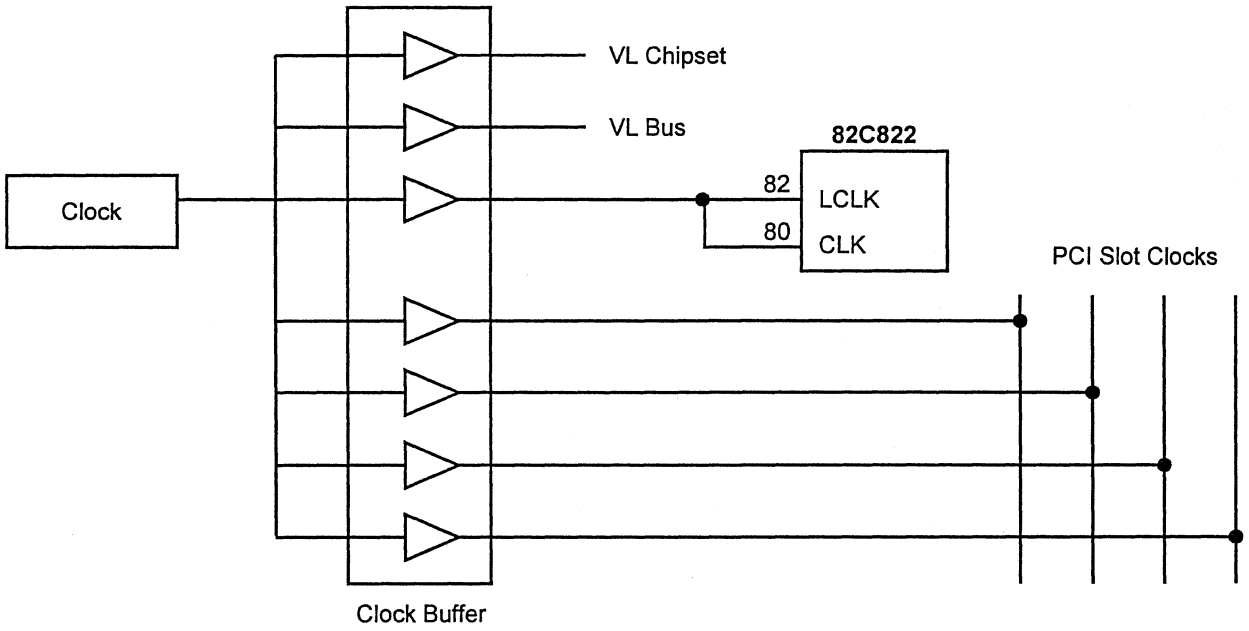
4.6 Asynchronous and Synchronous Modes of Operation

The 82C822 supports both synchronous and asynchronous modes of operation. In the synchronous mode, the PCI bus interfaces runs at the same speed as the VL bus. In the asynchronous mode, the PCI bus can run at a different speed than the VL bus. This facilitates the VL bus to run at 50MHz with the PCI running at 33MHz. The recommended clock circuitry for both asynchronous and synchronous modes are shown in Figure 4-1.

The synchronous mode of operation is recommended when the VL bus is operating below 33MHz. The clock circuitry should follow the block diagram in Figure 4-1 for synchronous mode of operation.

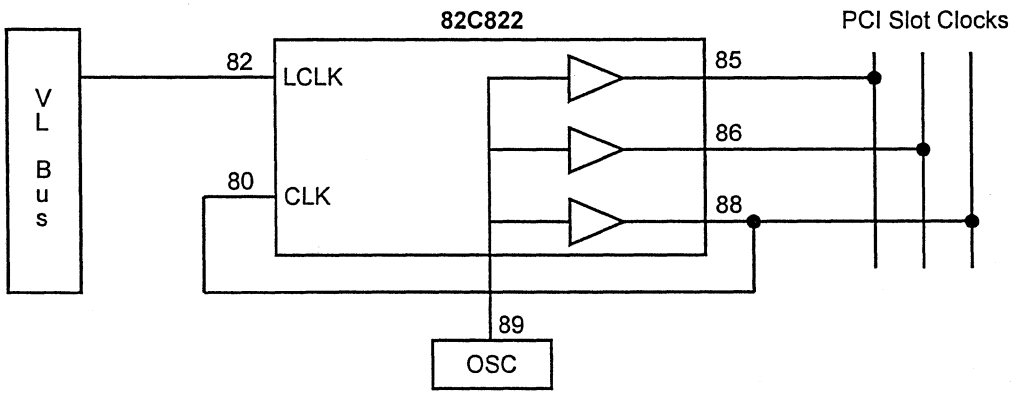
The asynchronous mode of opeation is recommended when the VL bus is running at 50MHz or to implement PCI interface in the riser card. The clock circuitry should follow the block diagram given in Figure 4-2 of the asynchronous mode of opera-

Figure 4-1 Synchronous Mode



Note: Skew between clock buffer outputs should be less than 2ns.

Figure 4-2 Asynchronous Mode



5.0 Configuration Registers

5.1 PCI Configuration Register Space

Note: In the address offsets given below, the most significant bit (MSB) corresponds to the upper address offset. The default values for the address offsets are given on the top right of the tables.

Table 5-1 Address Offset 00h-01h — 1045h

Bit(s)	Type	Default	Function
15:0	RO	1045h	Vendor Identification Register

Table 5-2 Address Offset 02h-03h — C822h

Bit(s)	Type	Default	Function
15:0	RO	C822h	Device Identification Register

Table 5-3 Address Offset 04h-05h: Command Register — 0007h

Bit(s)	Type	Default	Function
15:10	RO	0000 00	Reserved Bits
9	RO	0	Enable Fast Back-to-Back: Must always = 0 otherwise the 82C822 will never generate fast back-to-back transactions to different PCI bus slaves.
8	R/W	0	SERR# Enable: 0 = Disable 1 = Enable
7	RO	0	Wait Cycle Control: Must always = 0 always. No programmable wait states are supported by the 82C822.
6	R/W	0	Enable Parity Error Response: 0 = Disable 1 = Enable
5	RO	0	Reserved Bit
4	RO	0	Enable Memory Write and Invalidate Cycle Generation: Must always = 0. No memory write and invalidate cycles will be generated by the 82C822.
3	RO	0	Enable Special Cycles: Must always = 0. The 82C822 does not respond to the PCI special cycle.
2	RO	1	Enable Bus Master Operations: Must always = 1. The allows the 82C822 to perform bus master operations all the time.
1	RO	1	Enable Memory Access: Must always = 1. The 82C822 allows a PCI bus master access to main memory all the time.
0	RO	1	Enable I/O Access: Must always = 1. The 82C822 allows a PCI bus master access to the PCI I/O all the time.

Table 5-4 Address Offset 06h-07h: Status Register 0280h

Bit(s)	Type	Default	Function
15	R/W	0	Detected Parity Error: 0 = No parity error 1 = Parity error occurred
14	RO	0	SERR# Status: 0 = No system error 1 = System error occurred
13	R/W	0	Master-Abort Status: 0 = No master abort 1 = Master abort occurred
12	RO	0	Received Target-Abort Status: 0 = No target abort 1 = Target abort occurred
11	R/W	0	Signaled Target-Abort Status: 0 = No target abort 1 = Target abort generated
10:9	RO	01	DEVSEL# Timing Status: These bits must always = 01. Medium timing is selected. The 82C822 asserts the DEVSEL# based on medium timing.
8	R/W	0	Data Parity Detected: 0 = No data parity detected 1 = Data parity has detected
7	R/W	1	Fast Back-to-Back Capable: 1 = Capable 0 = Not Capable **Note:** Can be set to 0 only when bit 2 of register at offset 52h is set to 0; for debugging purposes only.
6:0	RO	0000 000	Reserved Bits

Table 5-5 Address Offset 08h 01h

Bit(s)	Type	Default	Function
7:0	RO	01h	Revision Identification Register

Table 5-6 Address Offset 09h-0Bh 060000h

Bit(s)	Type	Default	Function
23:0	RO	060000h	Revision Identification Register

Table 5-7 Address Offset 0Ch 00h

Bit(s)	Type	Default	Function
7:0	RO	00h	Reserved Bits

Table 5-8 Address Offset 0Dh 20h

Bit(s)	Type	Default	Function
7:0	R/W	20h	Master Latency Timer Register

Table 5-9 Address Offset 0Eh — 00h

Bit(s)	Type	Default	Function
7:0	RO	00h	Header Type

Table 5-10 Address Offset 0Fh — 00h

Bit(s)	Type	Default	Function
7:0	RO	00h	BIST

Table 5-11 Address Offset 10h-3Fh — 00h

Bit(s)	Type	Default	Function
7:0	RO	00h	Reserved Bits

Table 5-12 Address Offset 40h-41h — 0C01h

Bit(s)	Type	Default	Function
15	R/W	0	82C822 PCI Bridge Enable: 0 = Disable 1 = Enable
14	R/W	0	CPU Type Select: 0 = L1 Write-through CPU 1 = L1 Write-back CPU
13:12	RO	00	Reserved Bits
11:10	R/W	1X	The delay of LRDY# after the assertion of BOFF#: **11 10 Delay** 0 0 No Delay 0 1 1 LCLK Delay 1 x 2 LCLK Delay
9	R/W	0	Disable LDEVO# Assertion during Local Memory Cycle: 0 = Enable 1 = Disable
8	R/W	0	Disable BOFF# Assertion: 0 = No retry error 1 = Retry error occurred
7	R/W	0	Enable NMIIN Input: 0 = Disable 1 = Enable
6	R/W	0	Enable Back-to-Back CFC read/write without CF8 write: 0 = Disable 1 = Enable
5:3	RO	000	Reserved Bits
2	RO	0	NMI Output Enable (via Port 70h) Status: 0 = NMI Output Disable 1 = NMI Output Enable
1	RO	0	Master Retry Status: 0 = No retry error 1 = Retry error has occurred
0	RO	1	LMEM#/LDEVI# Sampling Point Select: 1 = End of the first T2 0 = End of the second T2

Table 5-13 Address Offset 42h-43h — 0000h

Bit(s)	Type	Default	Function
15:4	R/W	20h	A[31:20] for the Top of Local Memory Decoding.
3	R/W	00h	Enable Top of Local Memory Decoding: 0 = Disable 1 = Enable **Note:** If bit 3 is enabled, then the LMEM# input pin is ignored; otherwise an external LMEM# is used to decide if the access for the current cycle is to local memory
2:0	RO	000	Reserved Bits

Bits 15:4	Top of Memory	Bits 15:4	Top of Memory
000h	1MB	03Fh	64MB
001h	2MB	:	:
002h	3MB	07Fh	128MB
003h	4MB	:	:
:	:	0FFh	256MB
00Fh	16MB	:	:
:	:	100h	Reserved
01Fh	32MB	:	:
:	:	FFFh	Reserved

Table 5-14 Address Offset 44h — 00h

Bit(s)	Type	Default	Function
7:6	R/W	00	Master Retry Timer: 7 6 **Operation** 0 0 Retries unmasked after 8 PCICLKs 0 1 Retries unmasked after 16 PCICLKs 1 0 Retries unmasked after 32 PCICLKs 1 1 Retries unmasked after 64 PCICLKs
5:4	RO	00	Reserved Bits
3	R/W	0	LMEM#/LDEV# sampling point select for PCI master cycle: 0 = 1 PCI clock after FRAME# 1 = 2 PCI clocks after FRAME#
2	RO	0	Reserved Bit
1	R/W	0	Enable Read Shadowed RAM for F0000h-FFFFFh Block: 0 = Disable 1 = Enable
0	R/W	0	Enable Write Shadowed RAM for F0000h-FFFFFh Block: 0 = Disable 1 = Enable

Table 5-15 Address Offset 45h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Read Shadowed RAM for EC000h-EFFFFh Block: 0 = Disable 1 = Enable
6	R/W	0	Enable Read Shadowed RAM for E8000h-EBFFFh Block: 0 = Disable 1 = Enable
5	R/W	0	Enable Read Shadowed RAM for E4000h-E7FFFh Block: 0 = Disable 1 = Enable
4	R/W	0	Enable Read Shadowed RAM for E0000h-E3FFFh Block: 0 = Disable 1 = Enable
3	R/W	0	Enable Write Shadowed RAM for EC000h-EFFFFh Block: 0 = Disable 1 = Enable
2	R/W	0	Enable Write Shadowed RAM for E8000h-EBFFFh Block: 0 = Disable 1 = Enable
1	R/W	0	Enable Write Shadowed RAM for E4000h-E7FFFh Block: 0 = Disable 1 = Enable
0	R/W	0	Enable Write Shadowed RAM for E0000h-E3FFFh Block: 0 = Disable 1 = Enable

Table 5-16 Address Offset 46h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Read Shadowed RAM for DC000h-DFFFFh Block: 0 = Disable 1 = Enable
6	R/W	0	Enable Read Shadowed RAM for D8000h-DBFFFh Block: 0 = Disable 1 = Enable
5	R/W	0	Enable Read Shadowed RAM for D4000h-D7FFFh Block: 0 = Disable 1 = Enable
4	R/W	0	Enable Read Shadowed RAM for D0000h-D3FFFh Block: 0 = Disable 1 = Enable
3	R/W	0	Enable Write Shadowed RAM for DC000h-DFFFFh Block: 0 = Disable 1 = Enable
2	R/W	0	Enable Write Shadowed RAM for D8000h-DBFFFh Block: 0 = Disable 1 = Enable
1	R/W	0	Enable Write Shadowed RAM for D4000h-D7FFFh Block: 0 = Disable 1 = Enable
0	R/W	0	Enable Write Shadowed RAM for D0000h-D3FFFh Block: 0 = Disable 1 = Enable

Table 5-17 Address Offset 47h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Read Shadowed RAM for CC000h-CFFFFh Block: 0 = Disable 1 = Enable
6	R/W	0	Enable Read Shadowed RAM for C8000h-CBFFFh Block: 0 = Disable 1 = Enable
5	R/W	0	Enable Read Shadowed RAM for C4000h-C7FFFh Block: 0 = Disable 1 = Enable
4	R/W	0	Enable Read Shadowed RAM for C0000h-C3FFFh Block: 0 = Disable 1 = Enable
3	R/W	0	Enable Write Shadowed RAM for CC000h-CFFFFh Block: 0 = Disable 1 = Enable
2	R/W	0	Enable Write Shadowed RAM for C8000h-CBFFFh Block: 0 = Disable 1 = Enable
1	R/W	0	Enable Write Shadowed RAM for C4000h-C7FFFh Block: 0 = Disable 1 = Enable
0	R/W	0	Enable Write Shadowed RAM for C0000h-C3FFFh Block: 0 = Disable 1 = Enable

Note: Address offsets 48h-51h are meant for setting the local memory holes 0-3.

Table 5-18 Address Offset 48h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Memory Hole 3: 0 = Disable 1 = Enable
6:4	R/W	000	Block Size for Memory Hole 3
3	R/W	0	Enable Memory Hole 2: 0 = Disable 1 = Enable
2:0	R/W	000	Block Size for Memory Hole 2

Table 5-19 Address Offset 49h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Memory Hole 1: 0 = Disable 1 = Enable
6:4	R/W	00	Block Size for Memory Hole 1
3	R/W	0	Enable Memory Hole 0: 0 = Disable 1 = Enable
2:0	R/W	0	Block Size for Memory Hole 0: Block Size Definition **2 1 0 Size** 0 0 0 64KB 0 0 1 128KB 0 1 0 256KB 0 1 1 512KB 1 0 0 1MB 1 0 1 2MB 1 1 0 4MB 1 1 1 8MB

Table 5-20 Address Offset 4Ah-4Bh — 0000h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[31:16] for Starting Address of Memory Hole 3

Table 5-21 Address Offset 4Ch-4Dh — 0000h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[31:16] for Starting Address of Memory Hole 2

Table 5-22 Address Offset 4Eh-4Fh — 0000h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[31:16] for Starting Address of Memory Hole 1

Table 5-23 Address Offset 50h-51h — 0000h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[31:16] for Starting Address of Memory Hole 0

Table 5-24 Address Offset 52h — 06h

Bit(s)	Type	Default	Function
7	R/W	0	DMA/ISA Bus Master to PCI Bus Slave Access Enable: 0 = Disable 1 = Enable
6	R/W	0	Enable Write Buffers from Host Bus to PCI Bus: 0 = Disable 1 = Enable
5	R/W	0	Enable Write Buffers from PCI Bus to Host Bus: 0 = Disable 1 = Enable
4	R/W	0	Disable NMI Generation Globally: 0 = Disable 1 = Enable
3	R/W	0	Enable SERR# Generation for Target Abort: 0 = Disable 1 = Enable
2	R/W	1	Fast Back-to-Back Capable: 1 = Enable 0 = Disable **Note:** The change on this bit will reflect on bit 7 of the register in address offset 06h.
1:0	R/W	10	Subtractive Decoding Sample Point: **1 0 Operation** 0 0 Fast sample point 0 1 Typical sample point 1 0 Slow sample point

Table 5-25 Address Offset 53h — 90h

Bit(s)	Type	Default	Function
7	R/W	1	PCI Bus Clock Synchronous to System Clock Enable: 1 = Asynchronous Clock 0 = Synchronous Clock
6	R/W	0	Host-to-PCI Bus FIFO Wait State: 0 = No Wait 1 = One Wait
5	R/W	0	Conversion of PERR# to SERR# Enable: 0 = Disable 1 = Enable
4	R/W	1	Enable Address Parity Checking: 1 = Enable 0 = Disable
3	R/W	0	Enable Conversion of PCI Shared Interrupts to ISA Edge Triggered Interrupts: 0 = Disable 1 = Enable
2	R/W	0	Expansion Bus Selection: 0 = ISA bus 1 = EISA
1	R/W	0	PCI Bus Burst Cycle Enable: 0 = Disable 1 = Enable
0	R/W	0	Host Bus to PCI Bus Post Write Enable: 0 = Disable 1 = Enable

Table 5-26 Address Offset 54h-57h — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Starting Address of General Purpose decode Block 3 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Starting Address of General Purpose decode Block 3 for PCI Address Space
1	R/W	0	Enable Block 3 Decoding Function: 0 = Disable 1 = Enable
0	R/W	0	Memory or I/O Space Indicator for Block 3: 0 = Memory Space 1 = I/O Space **Note:** If bit 0 = 0, then A[3:2] are ignored on decoding.

Table 5-27 Address Offset 58h-5Bh — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Ending Address of General Purpose decode Block 3 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Ending Address of General Purpose decode Block 3 for PCI Address Space
1:0	RO	00	Reserved Bits

Table 5-28 Address Offset 5Ch-5Fh — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Starting Address of General Purpose decode Block 2 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Starting Address of General Purpose decode Block 2 for PCI Address Space
1	R/W	0	Enable Block 2 Decoding Function: 0 = Disable 1 = Enable
0	R/W	0	Memory or I/O Space Indicator for Block 2: 0 = Memory Space 1 = I/O Space **Note:** If bit 0 = 0, then A[3:2] are ignored on decoding.

Table 5-29 Address Offset 60h-63h — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Ending Address of General Purpose decode Block 2 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Ending Address of General Purpose decode Block 2 for PCI Address Space
1:0	RO	00	Reserved Bits

Table 5-30 Address Offset 64h-67h — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Starting Address of General Purpose decode Block 1 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Starting Address of General Purpose decode Block 1 for PCI Address Space
1	R/W	0	Enable Block 1 Decoding Function: 0 = Disable 1 = Enable
0	R/W	0	Memory or I/O Space Indicator for Block 1: 0 = Memory Space 1 = I/O Space **Note:** If bit 0 = 0, then A[3:2] are ignored on decoding.

Table 5-31 Address Offset 68h-6Bh — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Ending Address of General Purpose decode Block 1 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Ending Address of General Purpose decode Block 1 for PCI Address Space
1:0	RO	00	Reserved Bits

Table 5-32 Address Offset 6Ch-6Fh — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Starting Address of General Purpose decode Block 0 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Starting Address of General Purpose decode Block 0 for PCI Address Space
1	R/W	0	Enable Block 0 Decoding Function: 0 = Disable 1 = Enable
0	R/W	0	Memory or I/O Space Indicator for Block 0: 0 = Memory Space 1 = I/O Space **Note:** If bit 0 = 0, then A[3:2] are ignored on decoding.

Table 5-33 Address Offset 70h-73h — 00000000h

Bit(s)	Type	Default	Function
31:8	R/W	000000h	A[31:8] for Ending Address of General Purpose decode Block 0 for PCI Address Space
7:2	R/W	0000 00	A[7:2] for Ending Address of General Purpose decode Block 0 for PCI Address Space
1:0	RO	00	Reserved Bits

Table 5-34 Address Offset 74h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	PCI Bus Master to Host Memory Burst Cycle Enable: 0 = Disable 1 = Enable
6	R/W	0	Enable I/O Port 3F7h Write at ISA Bus: 0 = Disable 1 = Enable
5	R/W	0	Enable I/O Port 3F7h Read at ISA Bus: 0 = Disable 1 = Enable
4	R/W	0	Enable I/O Port 377h Write at ISA Bus: 0 = Disable 1 = Enable
3	R/W	0	Enable I/O Port 377h Read at ISA Bus: 0 = Disable 1 = Enable
2:0	RO	000	Reserved Bits

Table 5-35 Address Offset 75h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable E8000h-EFFFFh Memory Block for ROMCS#: 0 = Disable 1 = Enable
6	R/W	0	Enable E0000h-E7FFFh Memory Block for ROMCS#: 0 = Disable 1 = Enable
5	R/W	0	Enable DC000h-DFFFFh Memory Block for NVMCS#: 0 = Disable 1 = Enable
4	R/W	0	Enable D8000h-DBFFFh Memory Block for NVMCS#: 0 = Disable 1 = Enable
3	R/W	0	Enable D4000h-D7FFFh Memory Block for NVMCS#: 0 = Disable 1 = Enable
2	R/W	0	Enable D0000h-D3FFFh Memory Block for NVMCS#. 0 = Disable 1 = Enable
1	R/W	0	Enable CC000h-CFFFFh Memory Block for NVMCS#. 0 = Disable 1 = Enable
0	R/W	0	Enable C8000h-CBFFFh Memory Block for NVMCS#. 0 = Disable 1 = Enable

Table 5-36 Address Offset 76h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Serial Port 1 at ISA Bus (Address Decoded 3F8h-3FFh): 0 = Disable 1 = Enable
6	R/W	0	Enable Serial Port 2 at ISA Bus (Address Decoded 2F8h-2FFh): 0 = Disable 1 = Enable
5	R/W	0	Enable Parallel Port 1 at ISAISA Bus (Address Decoded 3BCh-3BFh): 0 = Disable 1 = Enable
4	R/W	0	Enable Parallel Port 2 at ISA Bus (Address Decoded 378h-37Fh): 0 = Disable 1 = Enable
3	R/W	0	Enable Parallel Port 3 at ISA Bus (Address Decoded 278h-27Fh): 0 = Disable 1 = Enable
2	R/W	0	Enable Primary Floppy Disk at ISA Bus (Address Decoded 3F0h-3F5h): 0 = Disable 1 = Enable
1	R/W	0	Enable Secondary Floppy Disk at ISA Bus (Address Decoded 370h-375h): 0 = Disable 1 = Enable
0	R/W	0	Enable VGA Palette Snooping at ISA Bus (Address Decoded 3C6h-3C9h Write Cycle): 0 = Disable 1 = Enable

Table 5-37 Address Offset 77h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Primary IDE at ISA Bus (Address Decoded 1F0h-1F7h, 3F6h): 0 = Disable 1 = Enable
6	R/W	0	Enable Secondary IDE at ISA Bus (Address Decoded 170h-177h, 376h): 0 = Disable 1 = Enable
5	R/W	0	Enable VGA at ISA Bus (Address Decoded 3C0h-3CFh, 3B4h-3B5h, 3BAh, 3D4h-3D5h and 3DAh): 0 = Disable 1 = Enable
4:3	R/W	00	Reserved Bits
2	R/W	0	Enable System Board Controllers and I/O Address Range for EISA System (Address Decoded 0400h-04FFh, 0800h-08FFh, excluding 0C00h-0CFFh due to the overlap with CF8h and CFCh in PCI configuration read/write): 0 = Disable 1 = Enable
1	R/W	0	Enable System Board I/O Address Range for ISA/EISA System (Address Decoded 000h-0FFh): 0 = Disable 1 = Enable
0	R/W	0	Enable F0000h to FFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable

Table 5-38 Address Offset 78h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable EC000h-EFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
6	R/W	0	Enable E8000h-EBFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
5	R/W	0	Enable E4000h-E7FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
4	R/W	00	Enable E0000h-E3FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
3	R/W	00	Enable DC000h-DFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
2	R/W	0	Enable D8000h-DBFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
1	R/W	0	Enable D4000h-D7FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
0	R/W	0	Enable D0000h-D3FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable

Table 5-39 Address Offset 79h — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable CC000h-CFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
6	R/W	0	Enable C8000h-CBFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
5	R/W	0	Enable C4000h-C7FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
4	R/W	00	Enable C0000h-C3FFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
3	R/W	00	Enable A0000h-AFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
2	R/W	0	Enable B0000h-BFFFFh Memory Block at ISA Bus: 0 = Disable 1 = Enable
1:0	RO	00	Reserved Bits

Note: Offsets 7Ah-87h are for positive decode blocks of ISA bus memory and I/O.

Table 5-40 Address Offset 7Ah — 00h

Bit(s)	Type	Default	Function
7	R/W	0	Enable Memory Space 1 at ISA Bus: 0 = Disable 1 = Enable
6:4	R/W	00	Block Size for Memory Space 1
3	R/W	0	Enable Memory Space 2 at ISA Bus: 0 = Disable 1 = Enable
2:0	R/W	0	Block Size for Memory Space 2: Block Size Definition **2 1 0 Size** 0 0 0 64KB 0 0 1 128KB 0 1 0 256KB 0 1 1 512KB 1 0 0 1MB 1 0 1 2MB 1 1 0 4MB 1 1 1 8MB

Table 5-41 Address Offset 7Bh-7Ch — 00h

Bit(s)	Type	Default	Function
15:0	R/W	00h	A[31:8] for Starting Address of Memory Space 1

Table 5-42 Address Offset 7Dh-7Eh — 00h

Bit(s)	Type	Default	Function
15:0	R/W	00h	A[31:8] for Starting Address of Memory Space 2

Table 5-43 Address Offset 7Fh — 00h

Bit(s)	Type	Default	Function
7:2	RO	0000 00	Reserved Bits
1	R/W	0	Enable I/O Space 1 at ISA Bus: 0 = Disable 1 = Enable
0	R/W	0	Enable I/O Space 2 at ISA Bus: 0 = Disable 1 = Enable

Table 5-44 Address Offset 80h-81h — 00h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[15:0] for Comparison of I/O Space 1

Table 5-45 Address Offset 82h-83h — 00h

Bit(s)	Type	Default	Function
15:8	RO	0000 0000	Reserved Bits
7:0	R/W	0000 0000	A[7:0] for Masking of I/O Space 1

Table 5-46 Address Offset 84h-85h — 00h

Bit(s)	Type	Default	Function
15:0	R/W	0000h	A[15:0] for Comparison of I/O Space 2

Table 5-47 Address Offset 86h-87h — 00h

Bit(s)	Type	Default	Function
15:8	RO	0000 0000	Reserved Bits
7:0	R/W	0000 0000	A[7:0] for Masking of I/O Space 2

Note: Offsets 88h-8Fh are for PCI interrupt to ISA interrupt mapping.

Table 5-48 Address Offset 88h-8Bh — 00000000h

Bit(s)	Type	Default	Function
31:28	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request A2 has been triggered.
27:24	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request B2 has been triggered.
23:20	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request C2 has been triggered.
19:16	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request D2 has been triggered.
15:12	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request A1 has been triggered.
11:8	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request B1 has been triggered.
7:4	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request C1 has been triggered.
3:0	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request D1 has been triggered.

Table 5-49 Address Offset 8Ch-8Fh 00000000h

Bit(s)	Type	Default	Function
31:28	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request A4 has been triggered.
27:24	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request B4 has been triggered.
23:20	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request C4 has been triggered.
19:16	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request D4 has been triggered.
15:12	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request A3 has been triggered.
11:8	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request B3 has been triggered.
7:4	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request C3 has been triggered.
3:0	R/W	0000	Selects which IRQ signal is to be generated when PCI Interrupt Request D3 has been triggered. Routing Definition: **Routing** **Definition** 0 0 0 0 Disabled 0 0 0 1 IRQ5:flow through mode 0 0 1 0 IRQ9:flow through mode 0 0 1 1 IRQ10:flow through mode 0 1 0 0 IRQ11:flow through mode 0 1 0 1 IRQ12:flow through mode 0 1 1 0 IRQ14:flow through mode 0 1 1 1 IRQ15:flow through mode 1 0 0 0 Disabled 1 0 0 1 IRQ5:level 1 0 1 0 IRQ9:level 1 0 1 1 IRQ10:level 1 1 0 0 IRQ11:level 1 1 0 1 IRQ12:level 1 1 1 0 IRQ14:level 1 1 1 1 IRQ15:level

Table 5-50 Address Offset 90h-FFh 00h

Bit(s)	Type	Default	Function
7:0	R/W	00h	Reserved Bits

5.2 Non-Configuration Register Space

Table 5-51 I/O Port Address 70h 1XXXXXXXb

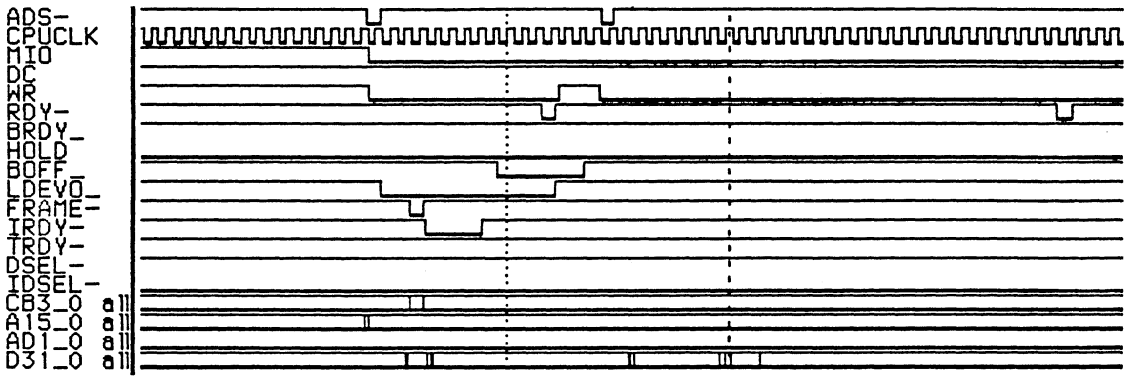
Bit(s)	Type	Default	Function
7	WO	1	Enable NMI: 1 = Disable 0 = Enable
6:0	RO	0000 000	Reserved Bits

6.0 AC Timing Waveforms

NOTE A15_0 are the CPU address pins 15-0.

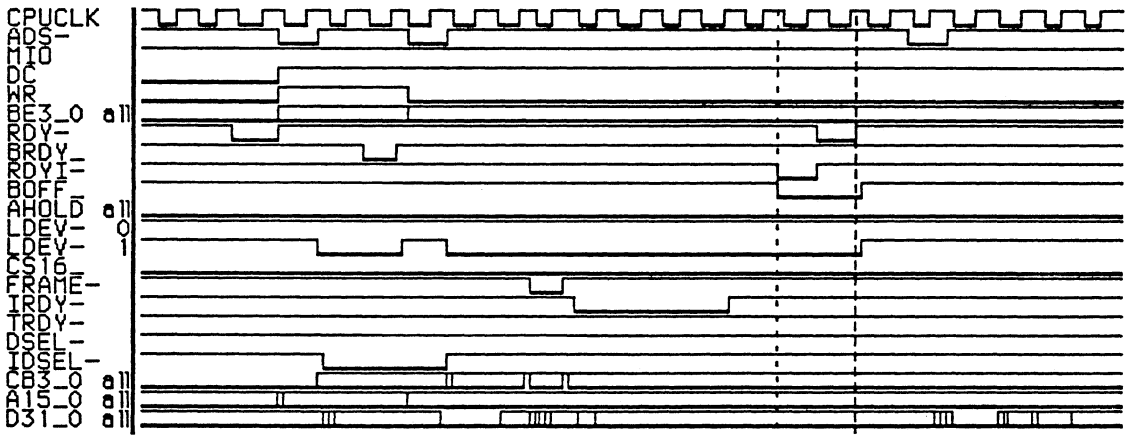
NOTE D31_0 are the CPU data pins 31-0.

Figure 6-1 822 back off ISA Cycle



NOTE LDEV_0 is the LDEV# pin of the 822.

Figure 6-2 0 CLK Delay of LRDY# after the assertion of BUFF#



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

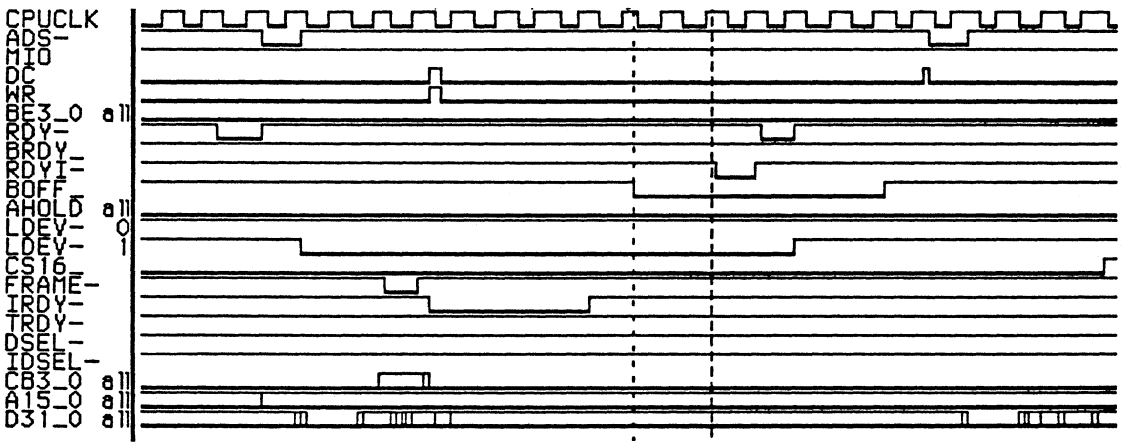
NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

Figure 6-3 1CLK Delay of LRDY# after the assertion of BUFF#

NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

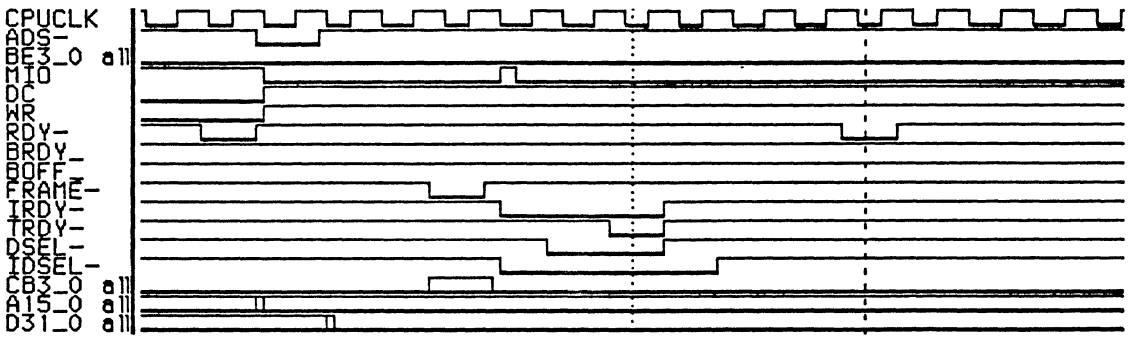
Figure 6-4 2 CLK Delay of LRDY# after the assertion of BUFF#



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

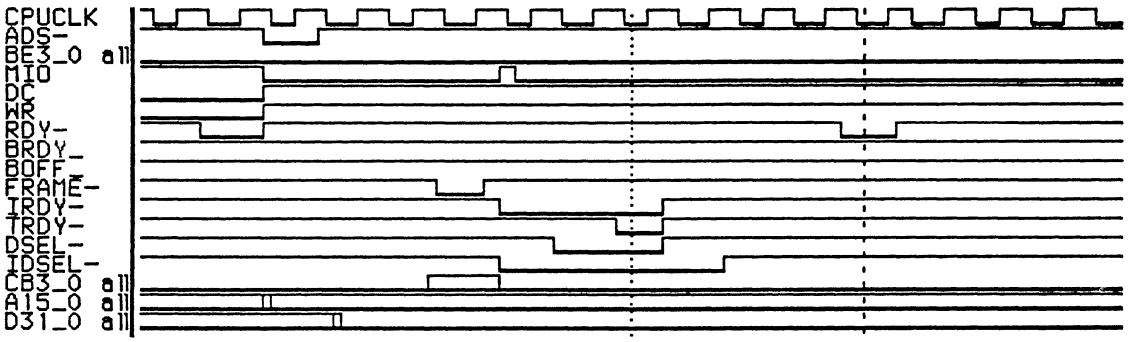
NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

Figure 6-5 PCI Configuration Write Cycle



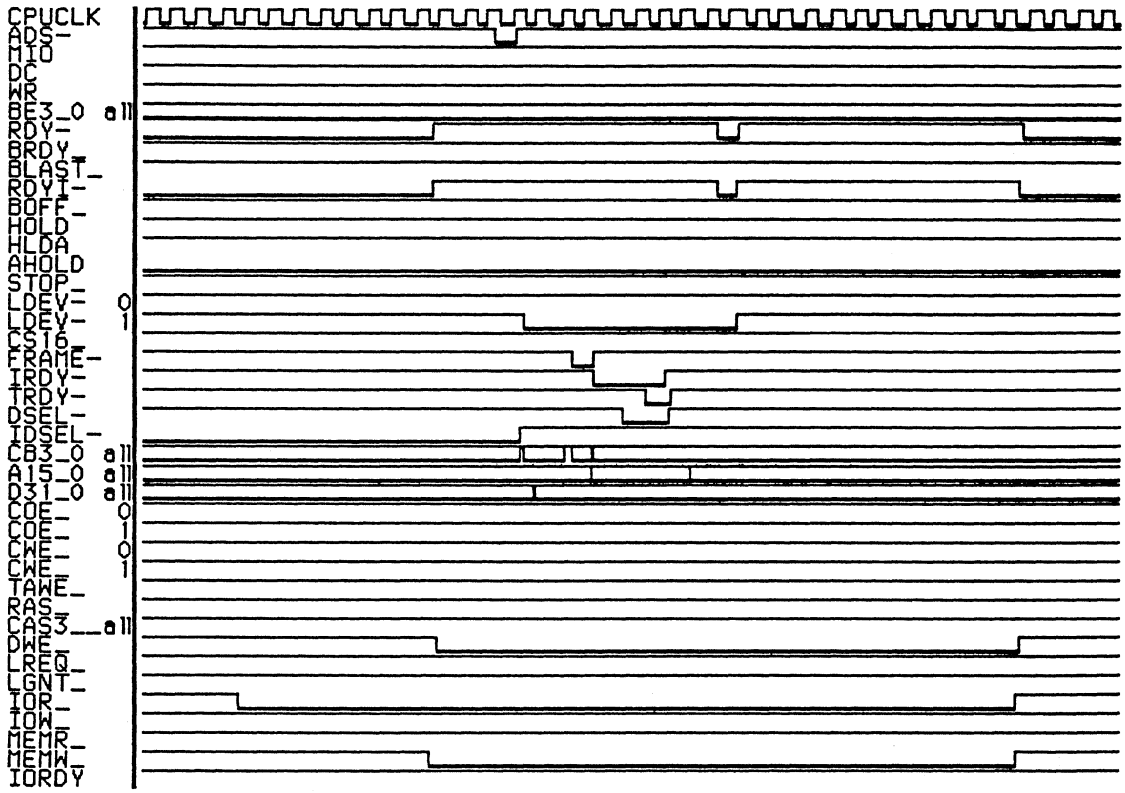
NOTE RDY_ is the RDYRTN# pin of the local bus.

Figure 6-6 PCI Configuration Read Cycle



NOTE RDY_ is the RDYRTN# pin of the lcoal bus.

Figure 6-7 DMA Write to PCI Slave

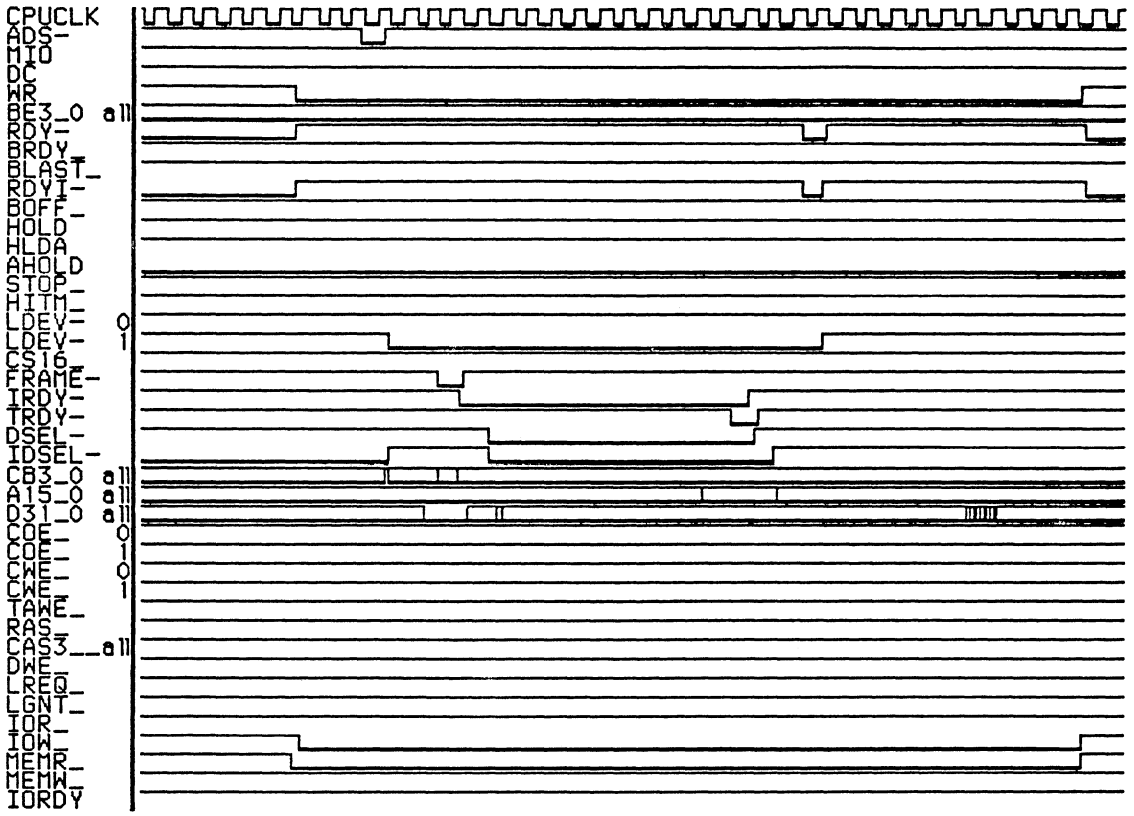


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-8 DMA Read from PCI Slave

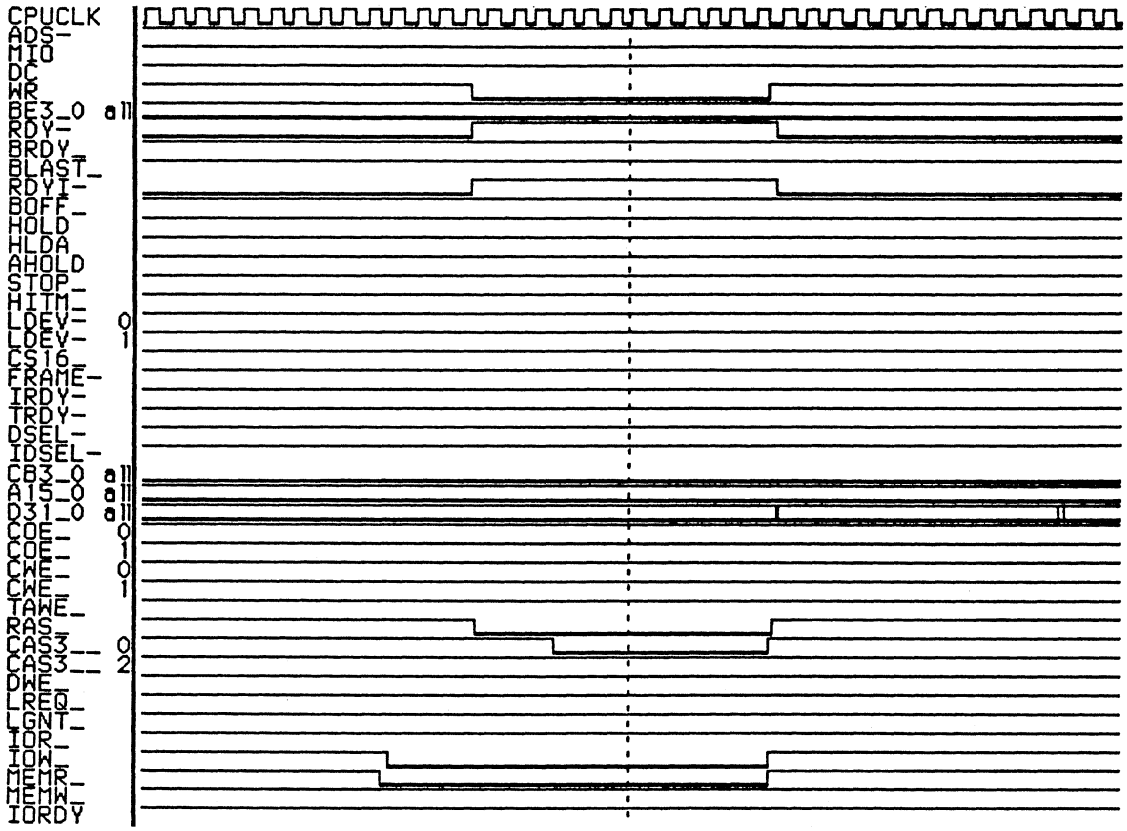


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-9 DMA Read from DRAM

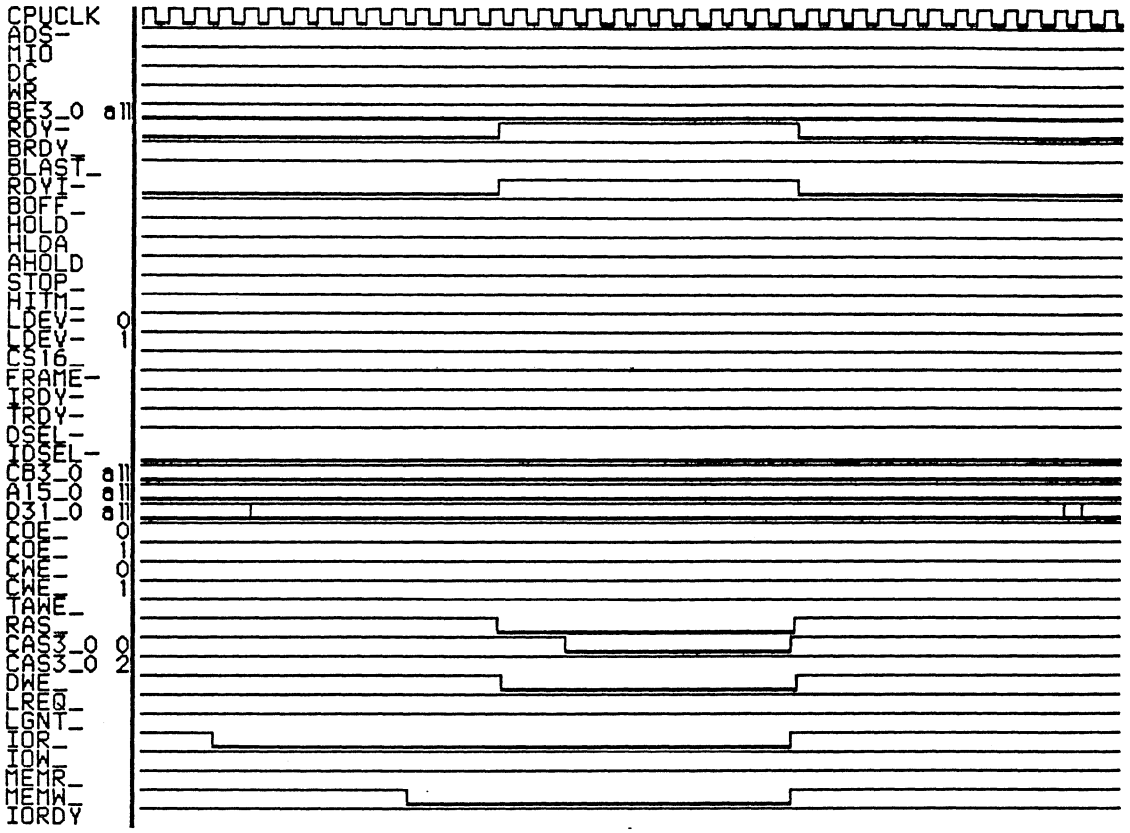


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-10 DMA Write to DRAM

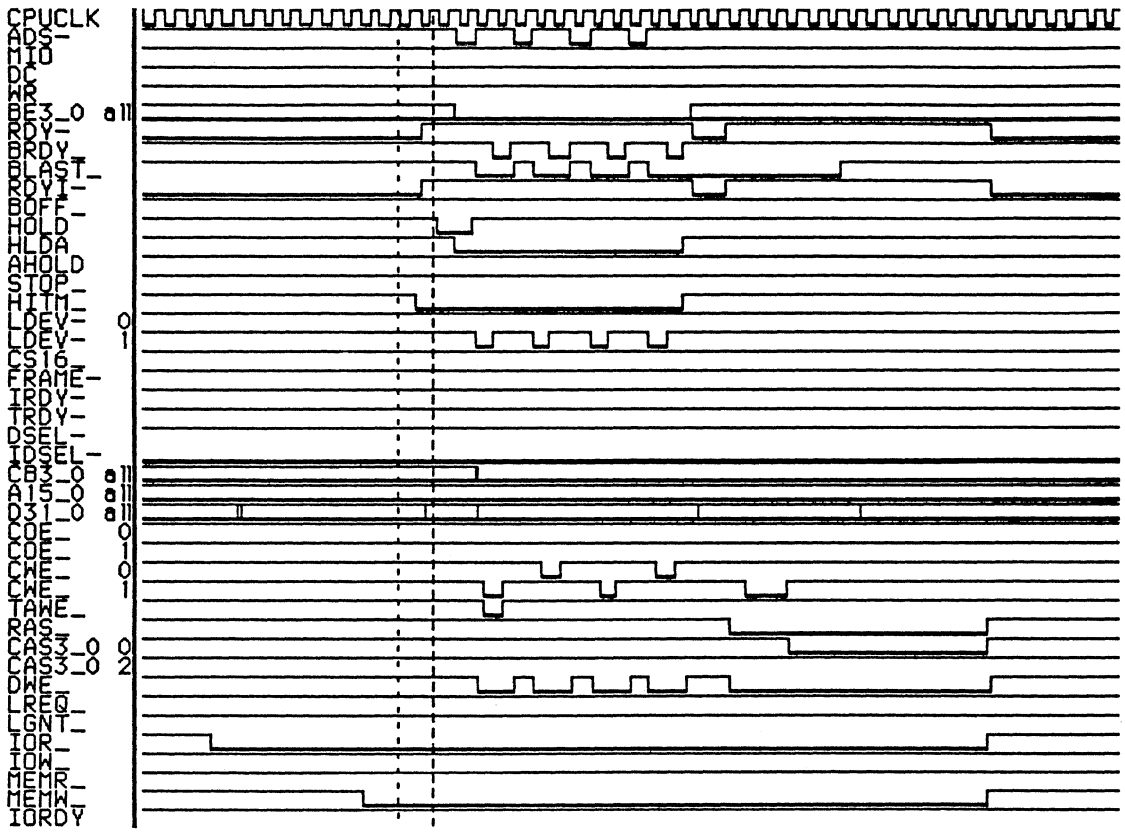


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-11 DMA Write to Cache with Write-Back

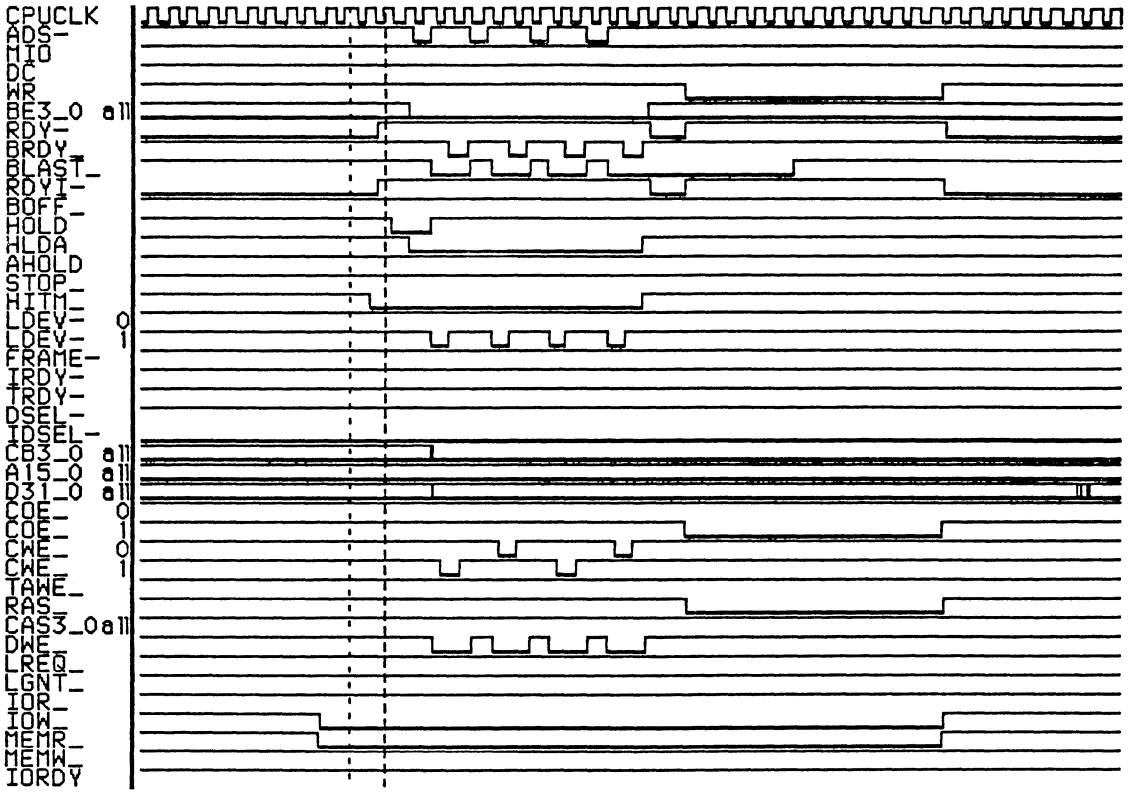


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-12 DMA Read from Cache with Write-Back

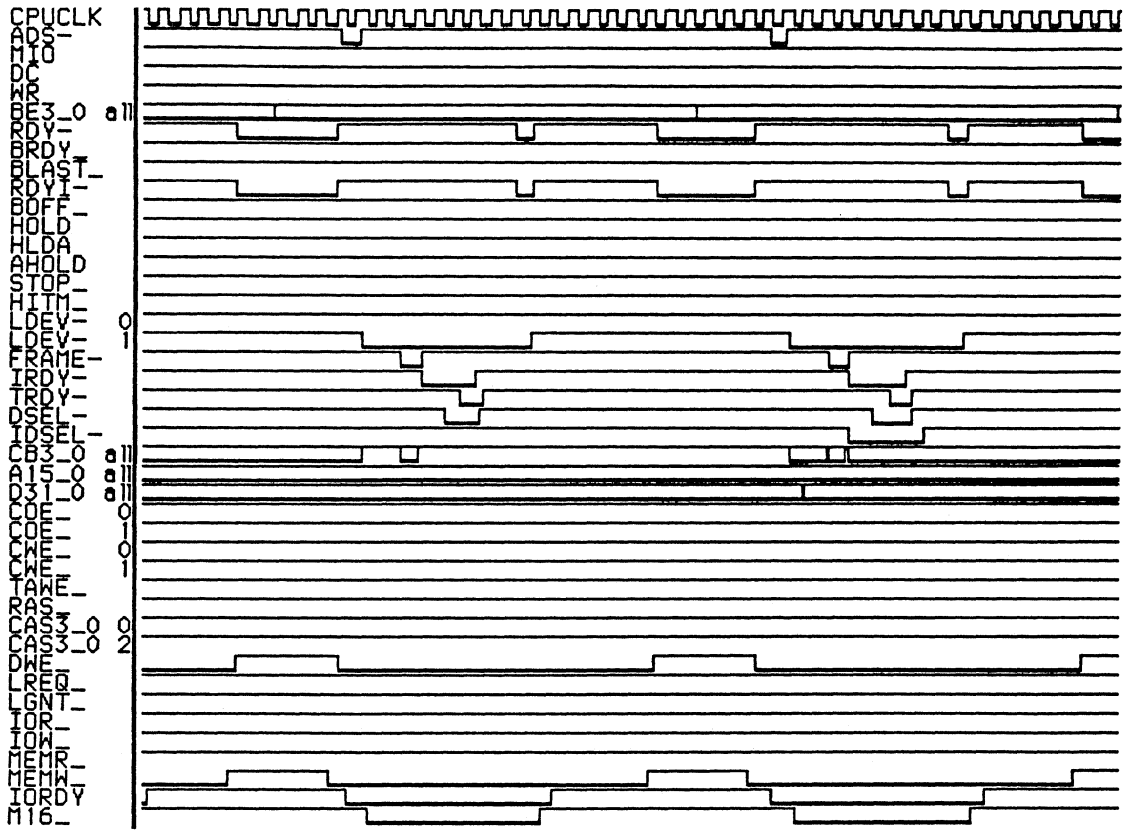


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-13 ISA Master Write to PCI Slave

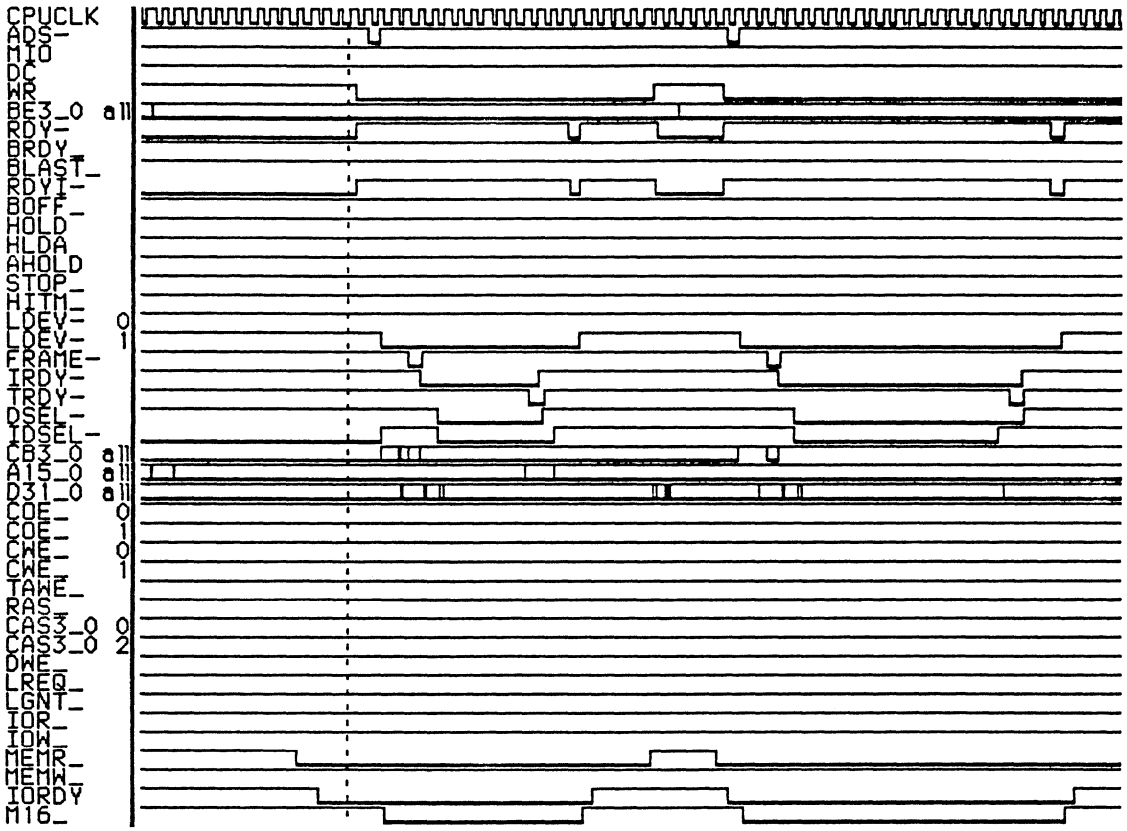


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-14 ISA Mastger Read from PCI Slave

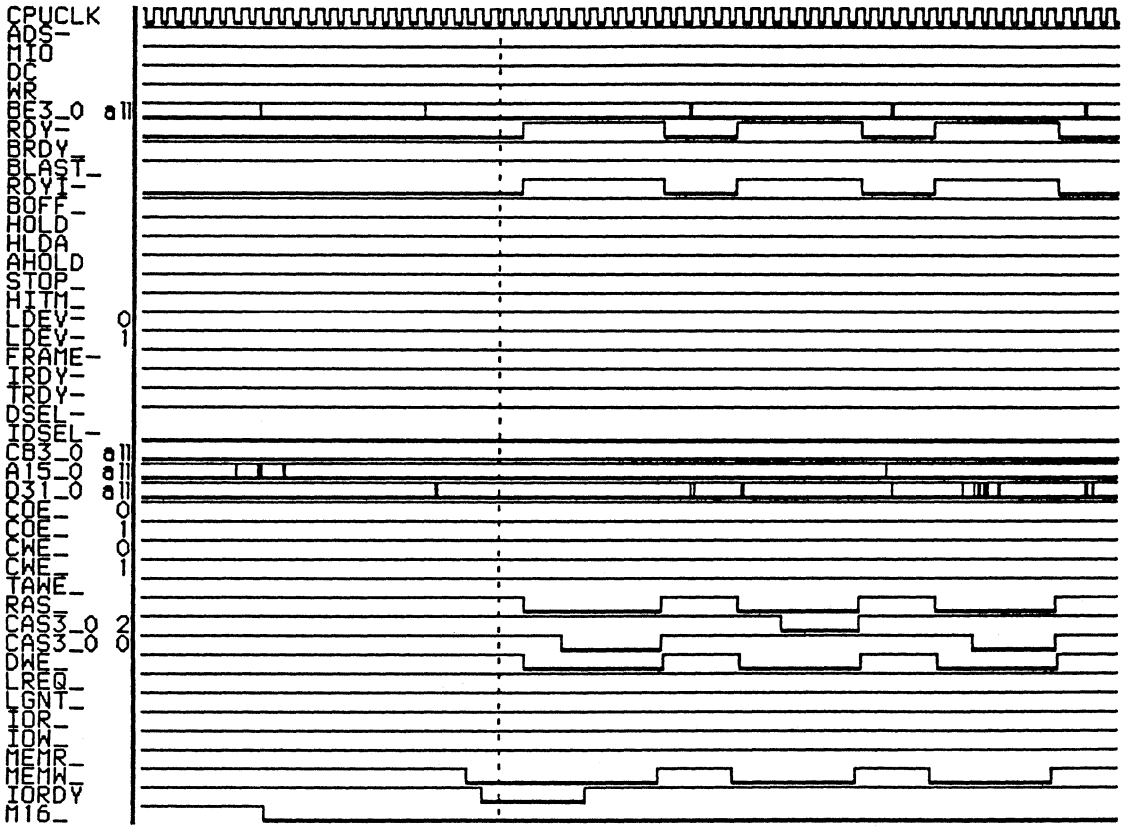


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-15 ISA Master Write to DRAM

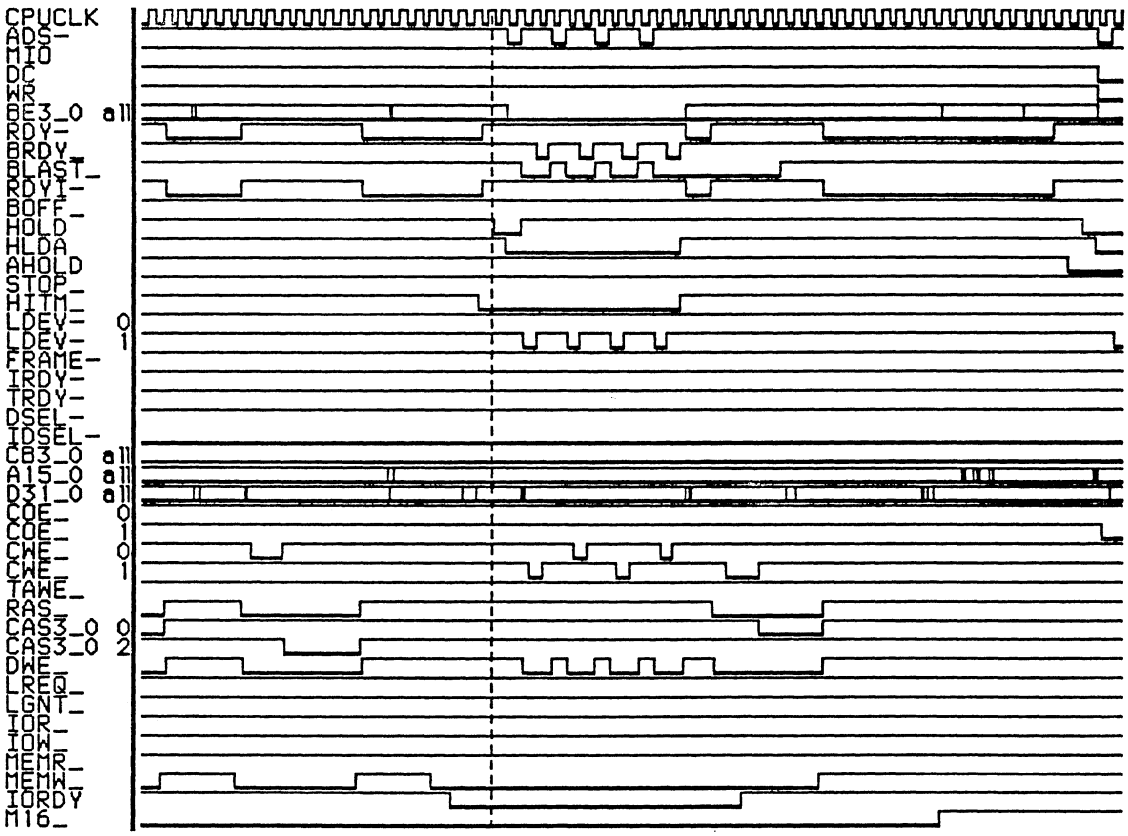


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-16 ISA Master Write to Cache with Write-Back

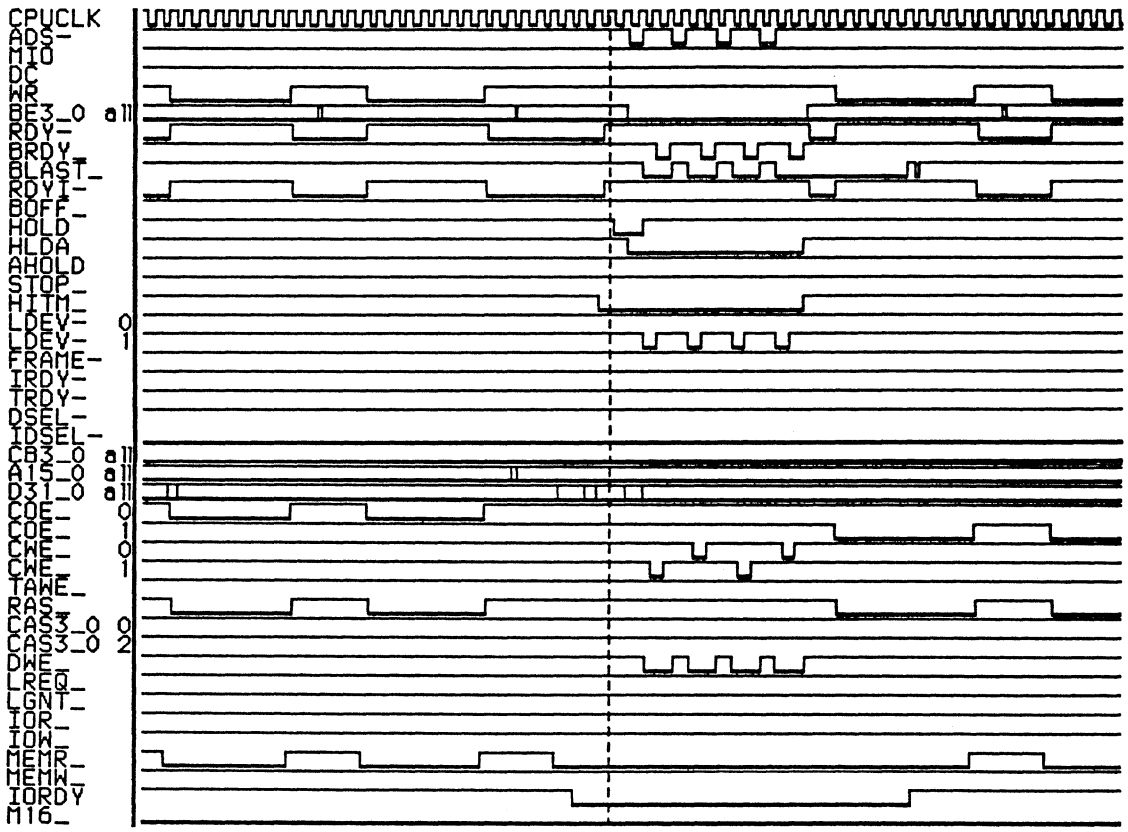


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-17 ISA Master Read from Cache with Write-Back



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

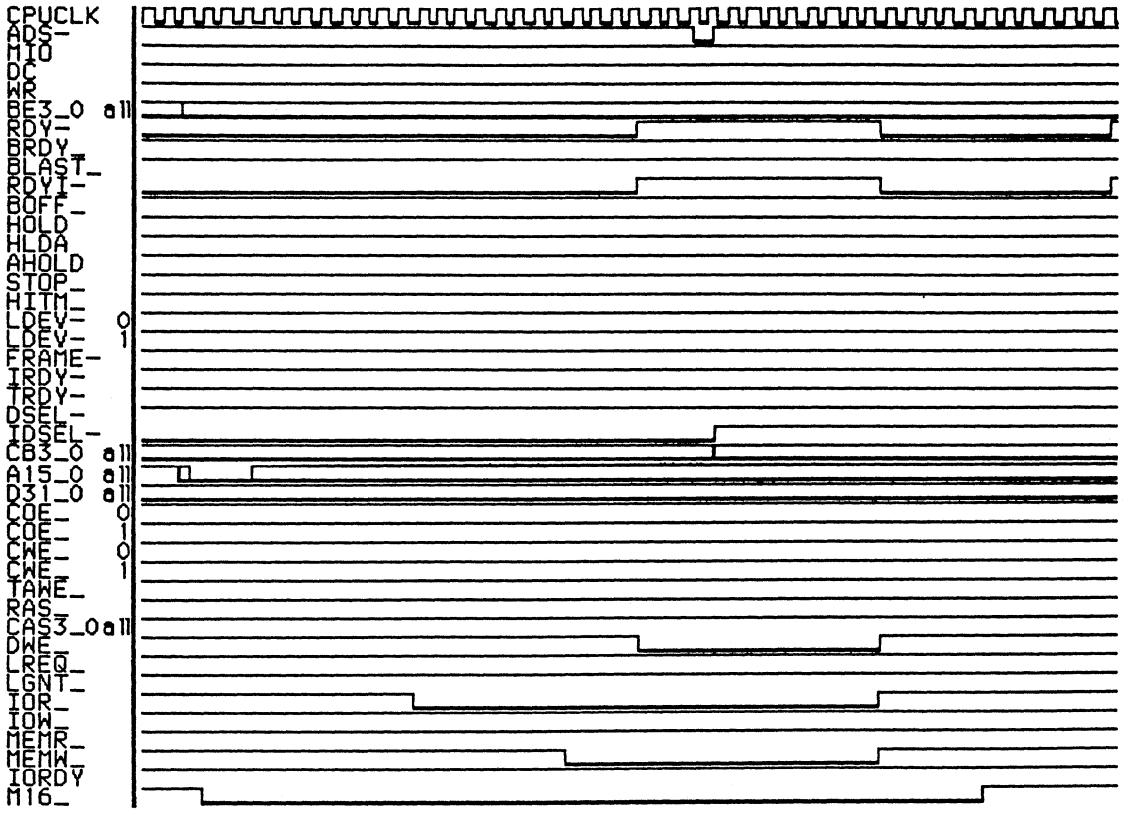
Figure 6-18 VESA Master Write to PCI Slave

NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-19 DMA Write to ISA Slave

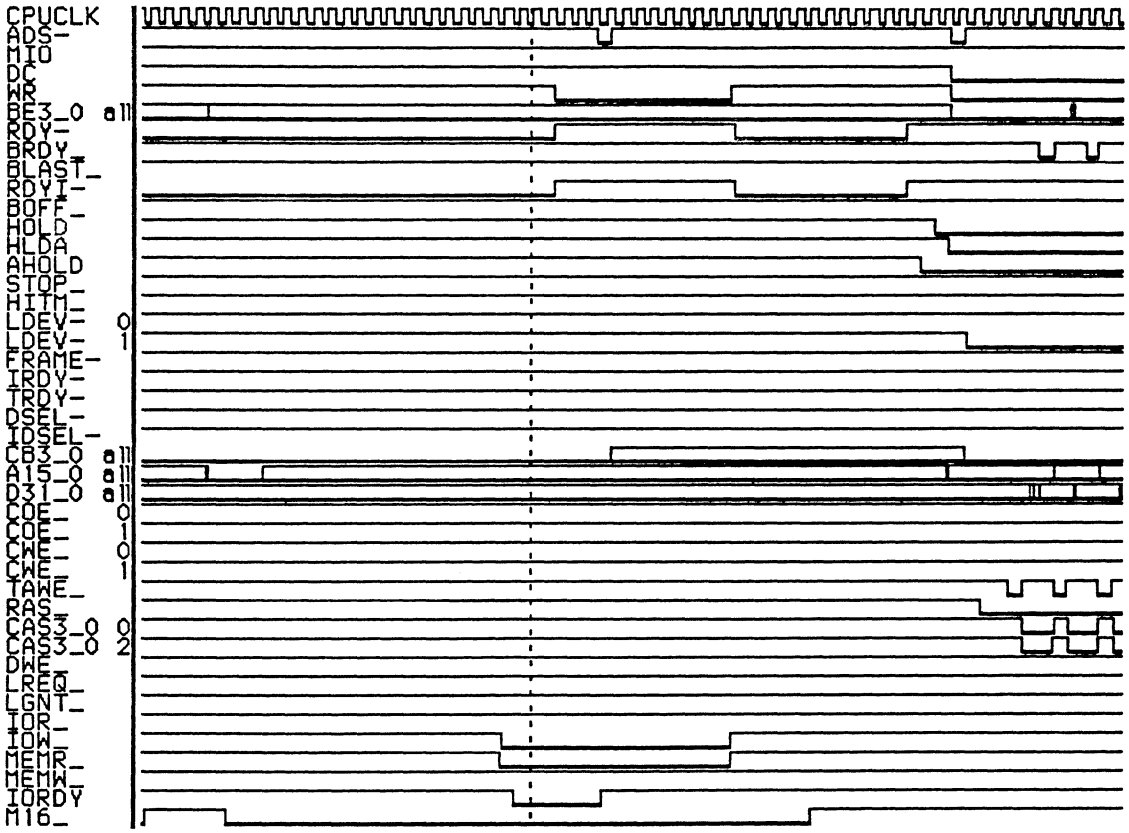


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-20 DMA Read from ISA Slave

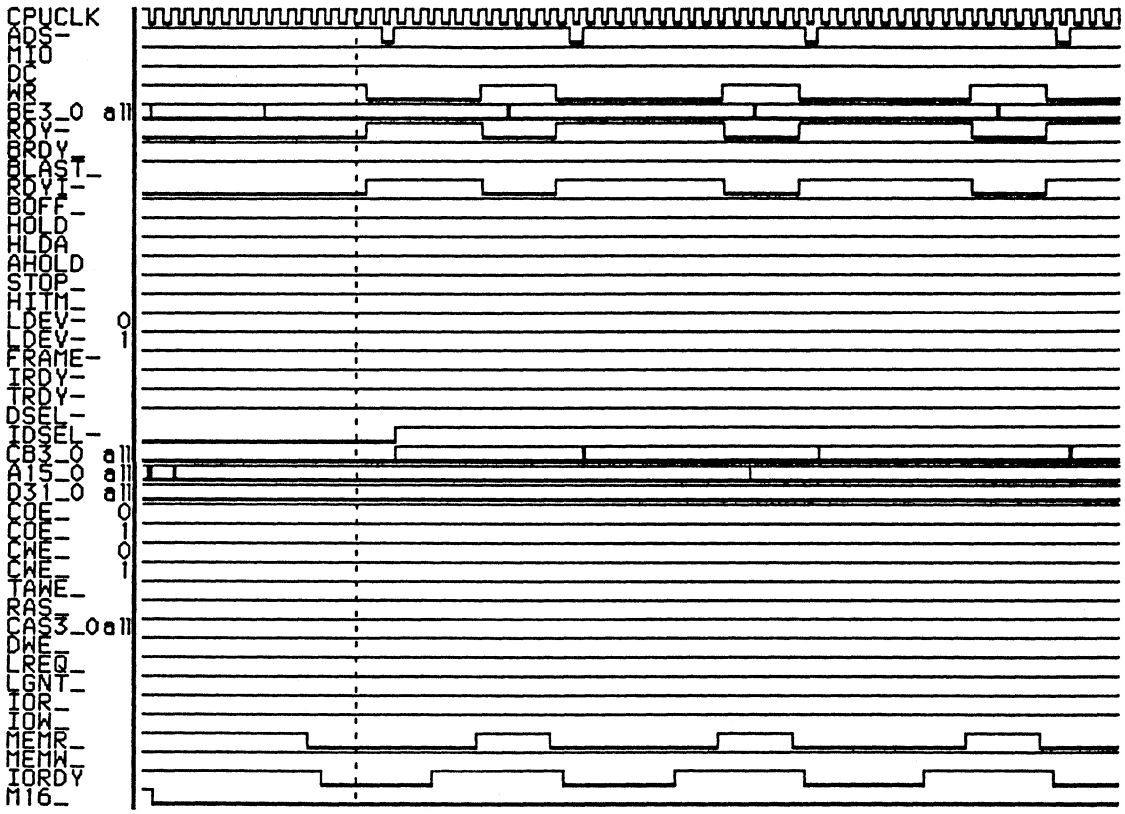


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-21 ISA Master Read from ISA Slave

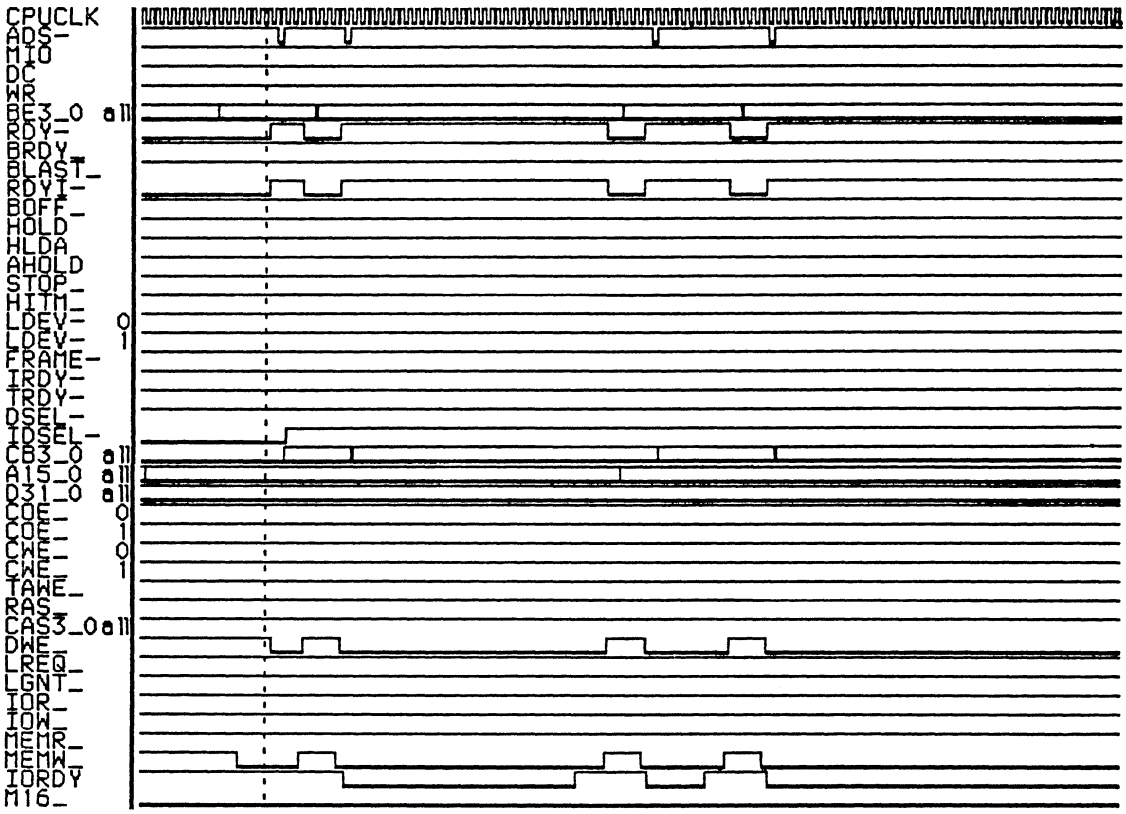


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-22 ISA Master Write to ISA Slave

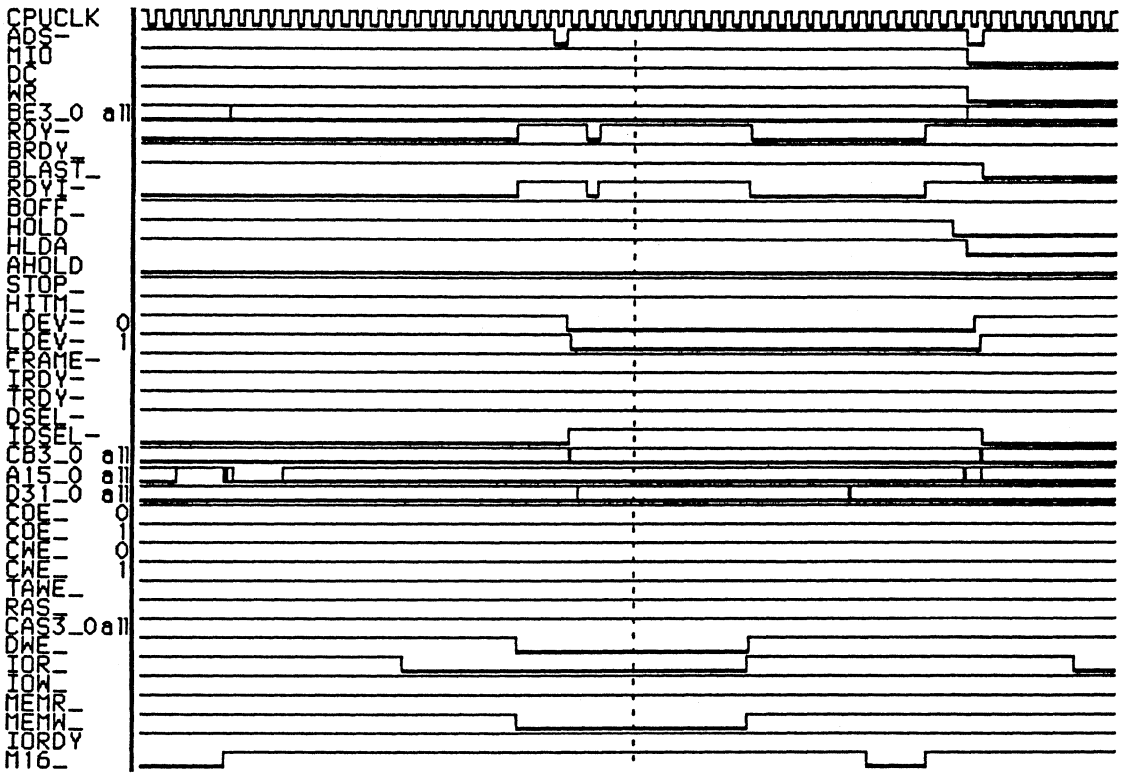


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

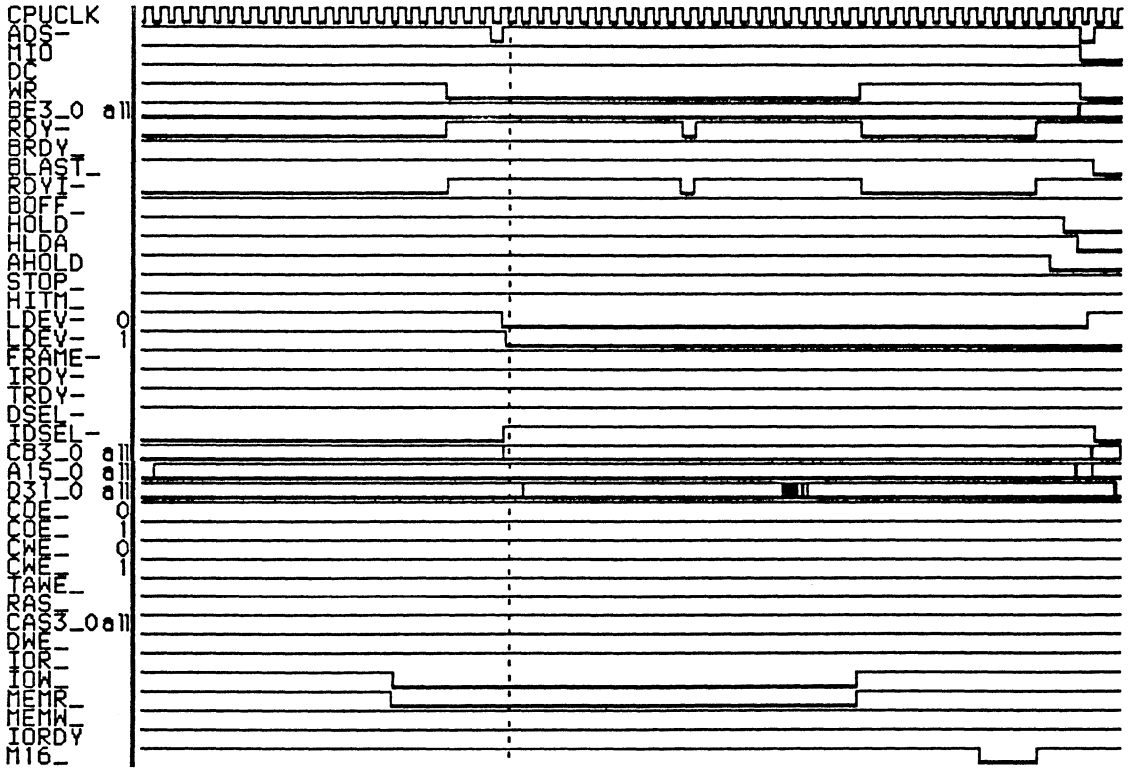
Figure 6-23 DMA Write to VESA Slave



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

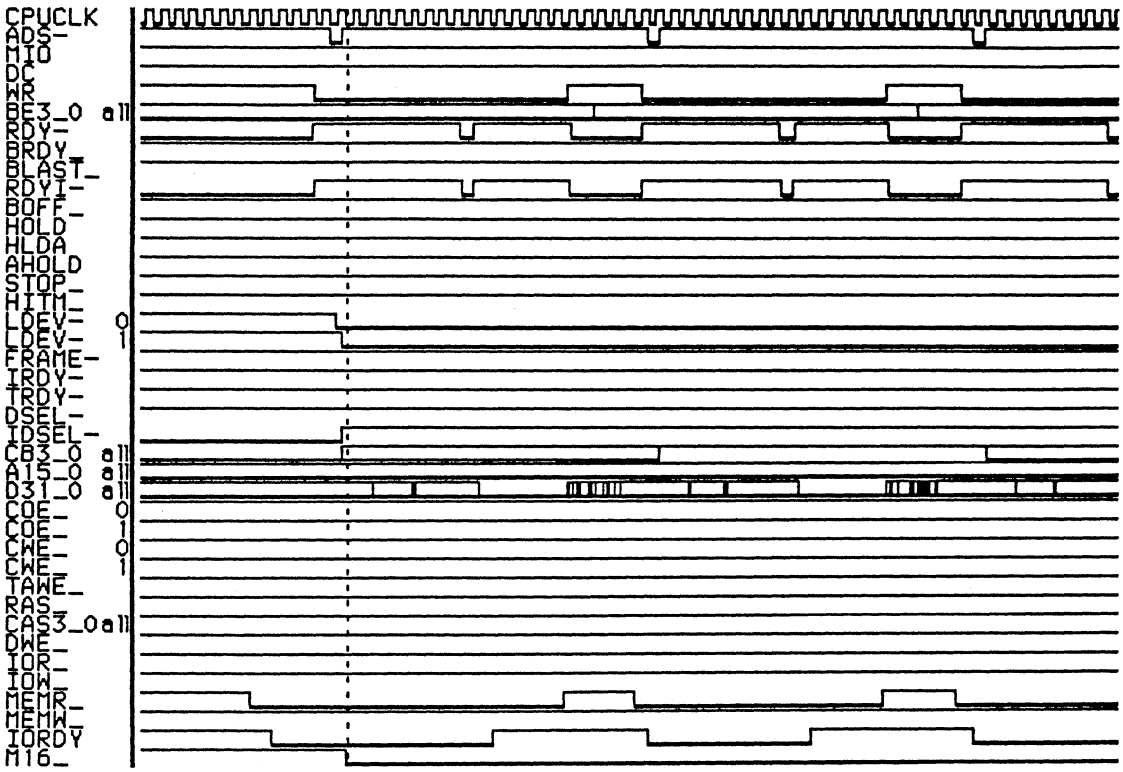
Figure 6-24 DMA Read from VESA Slave



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

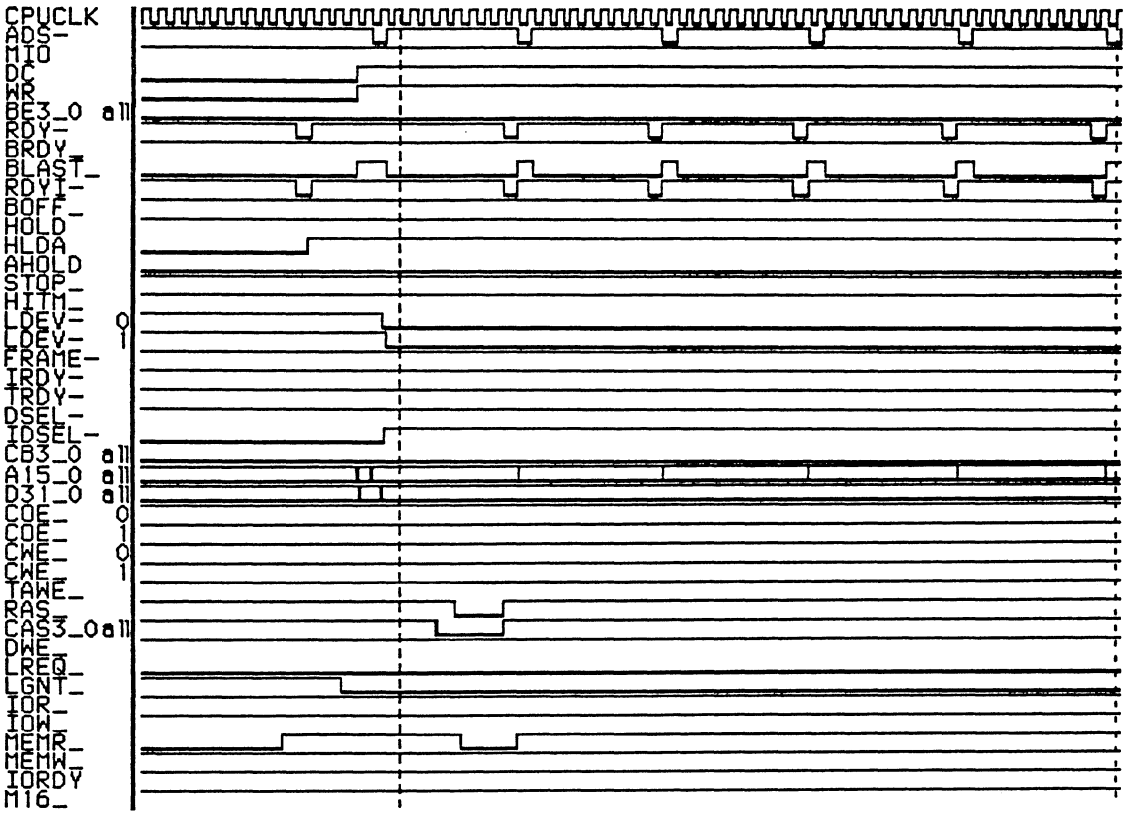
Figure 6-25 ISA Master Read from VESA Slave



NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

Figure 6-26 VESA Master Write to VESA Slave

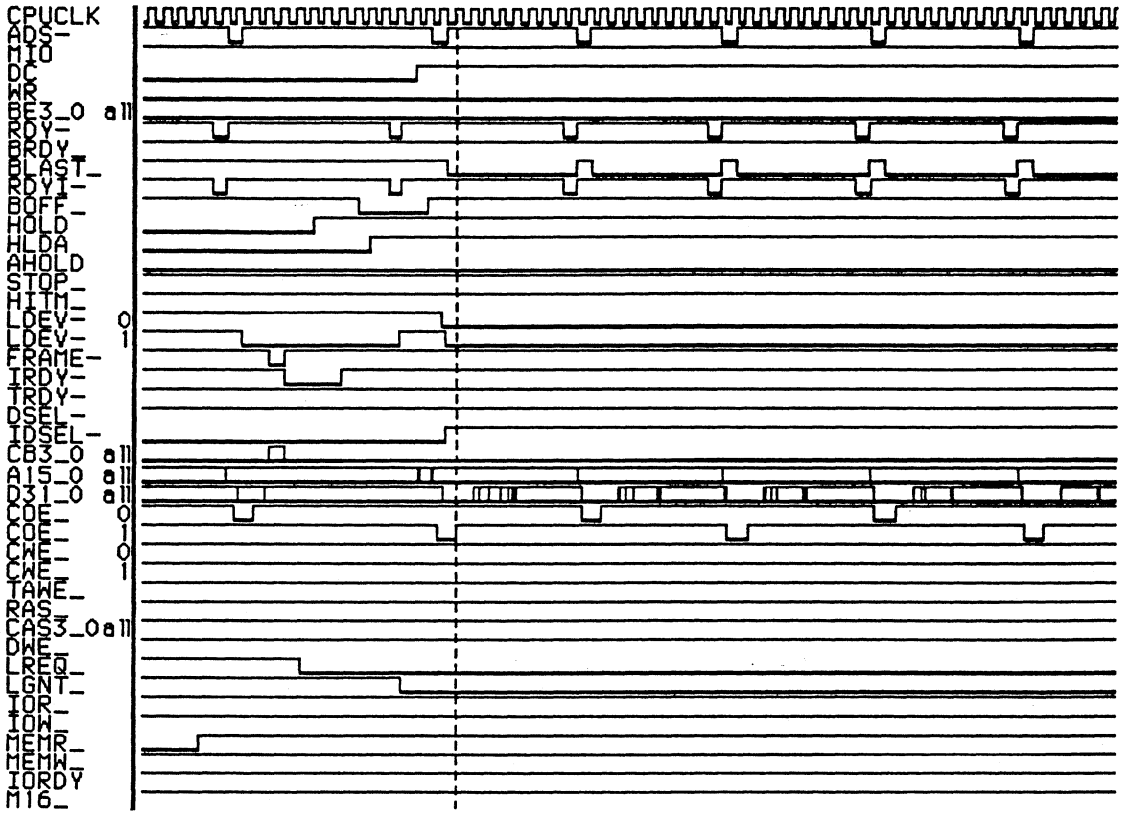


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-27 VESA Master Read from VESA Slave

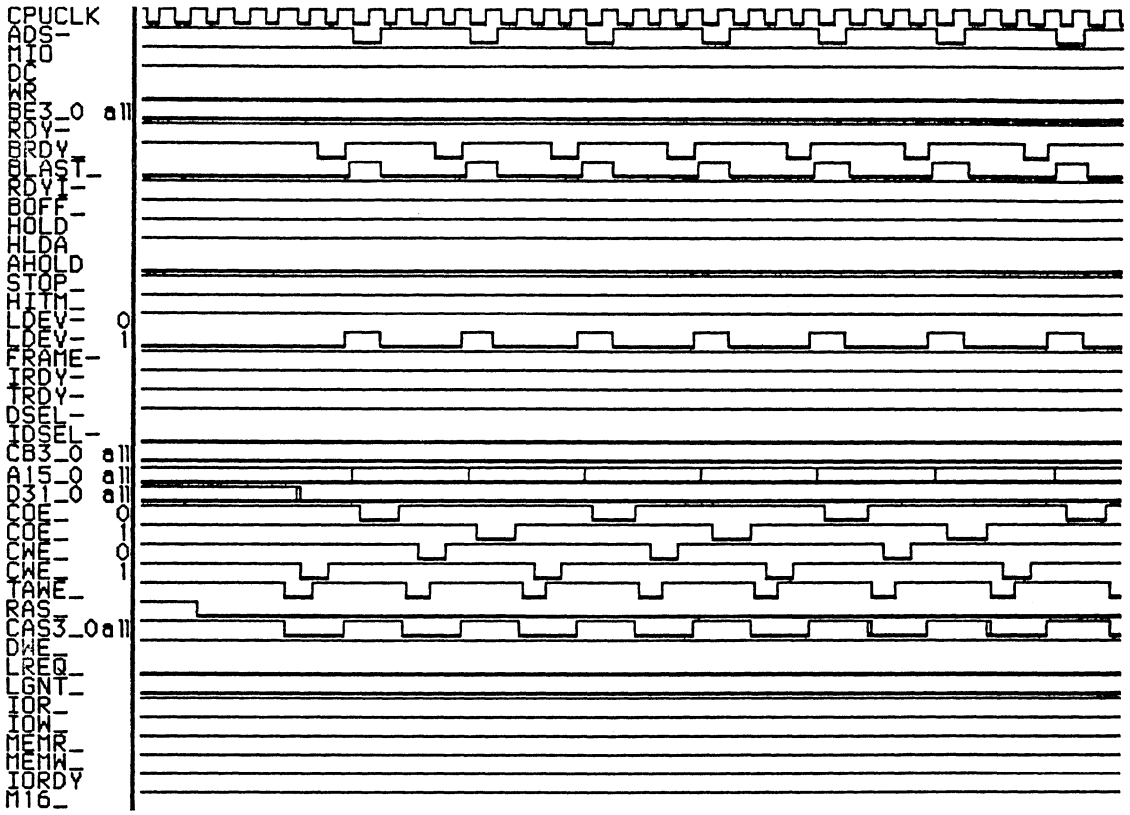


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-28 VESA Master Read from DRAM

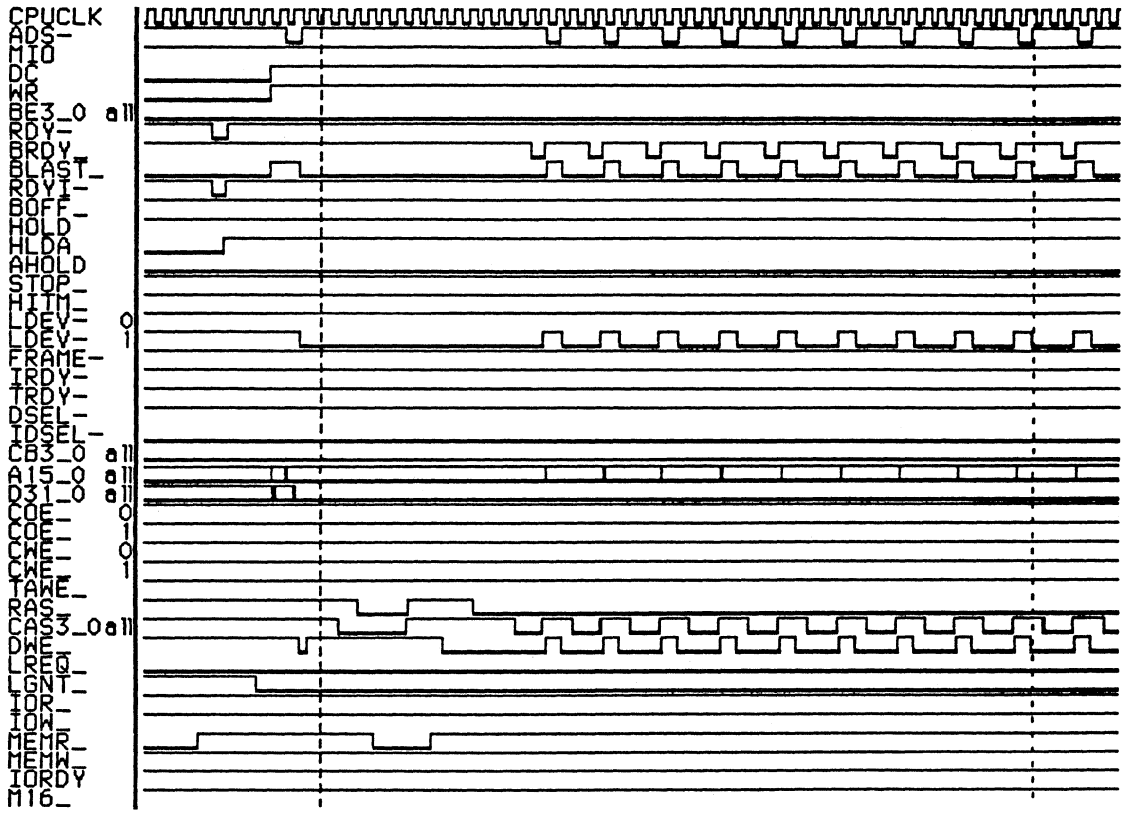


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-29 VESA Master Write to DRAM

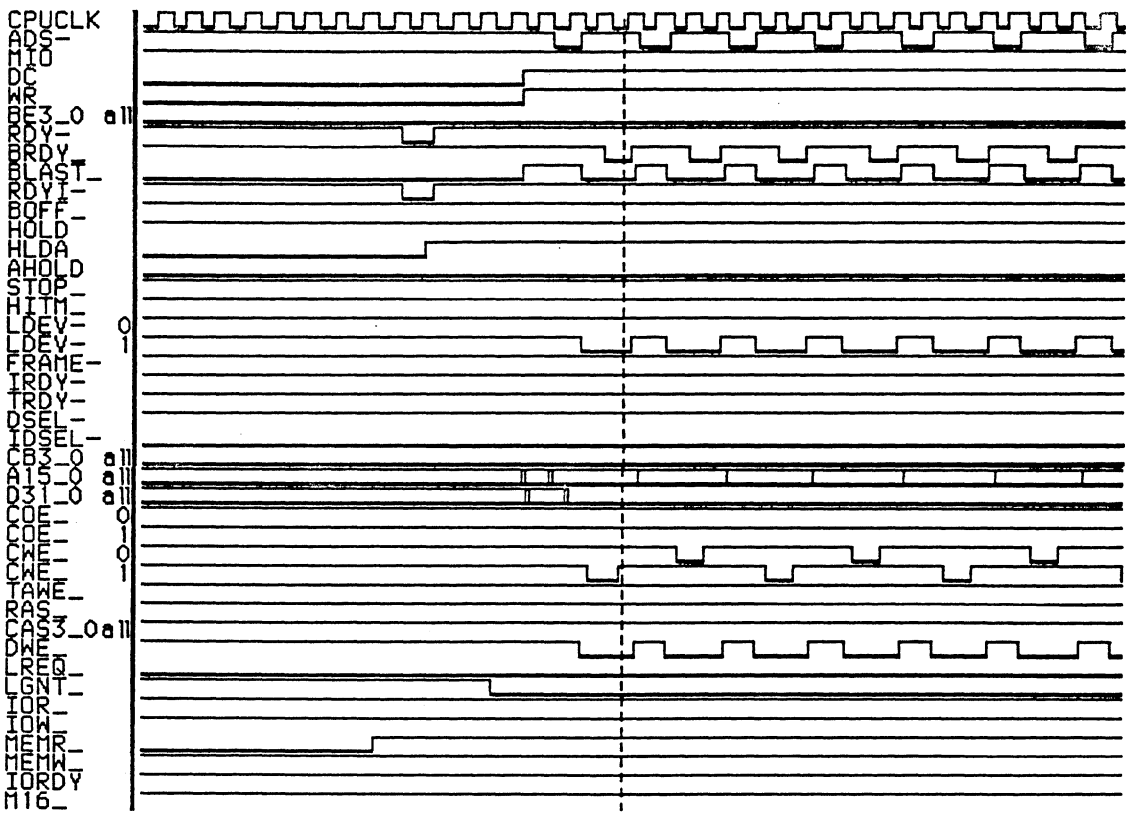


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-30 VESA Master Write to Cache

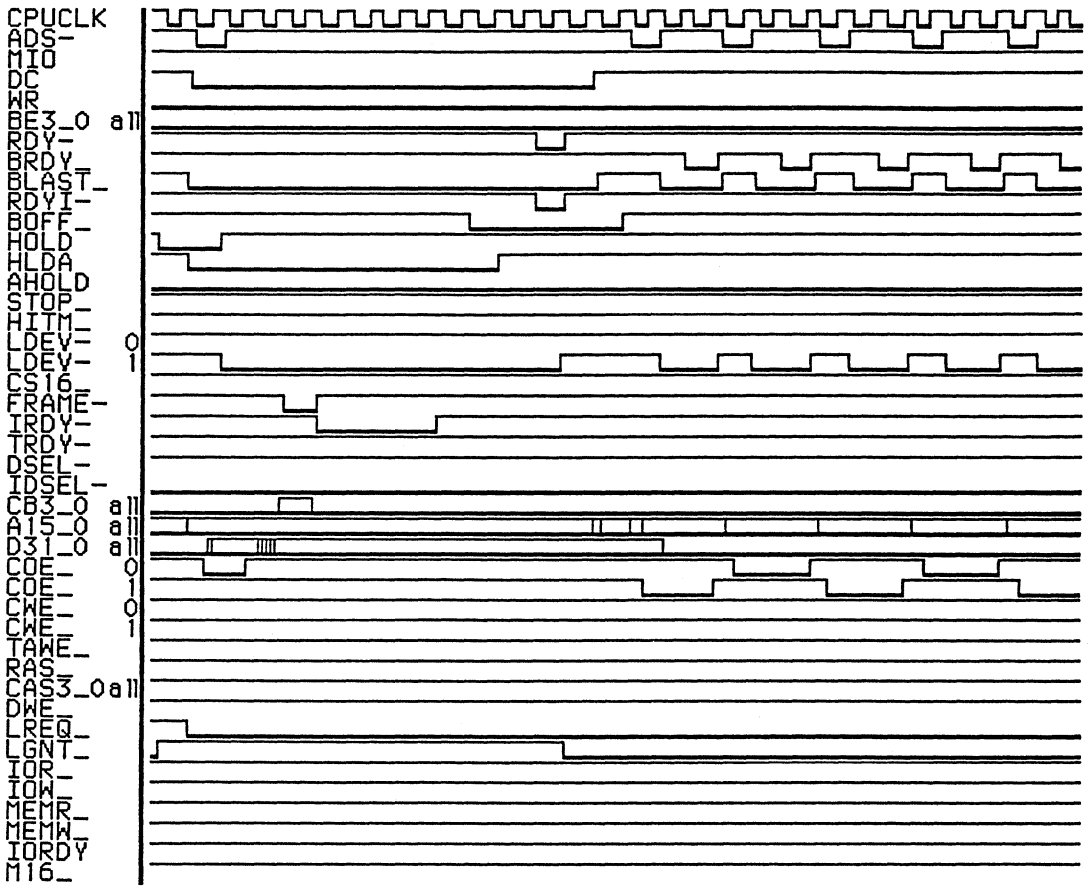


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-31 VESA Master Write to Cache

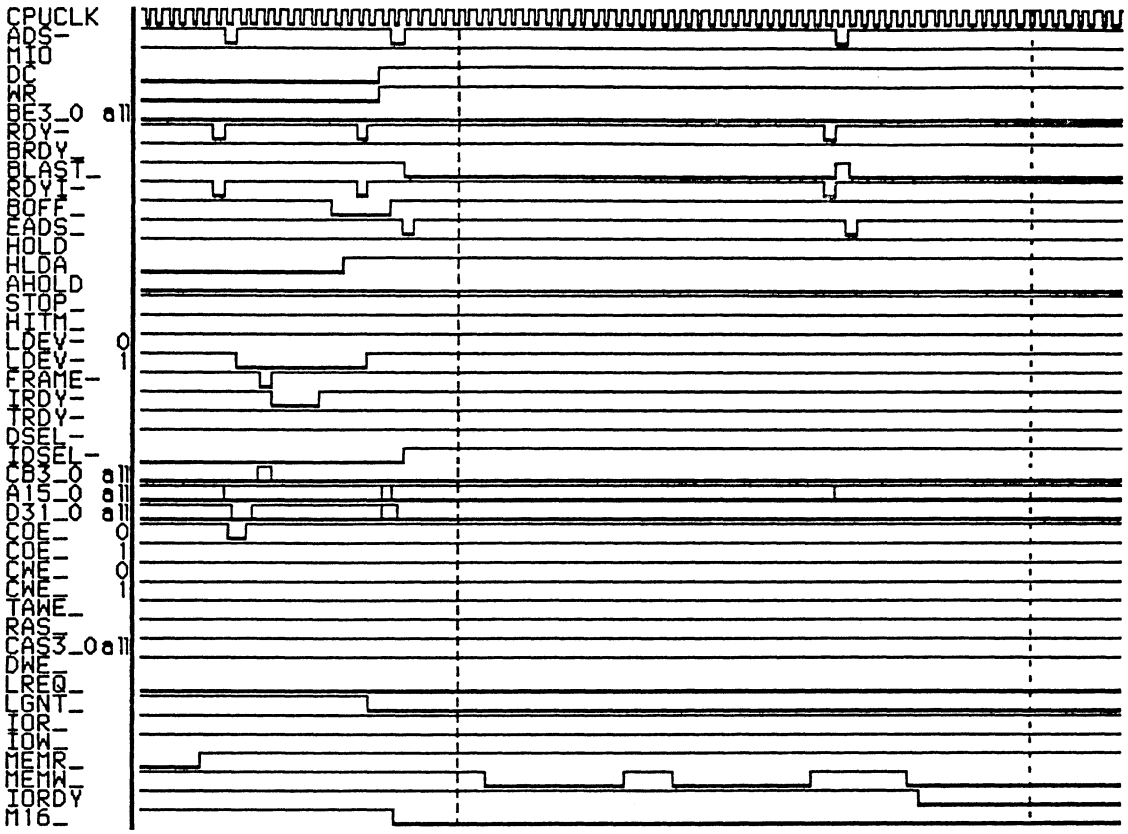


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-32 VESA Master Write to ISA Slave

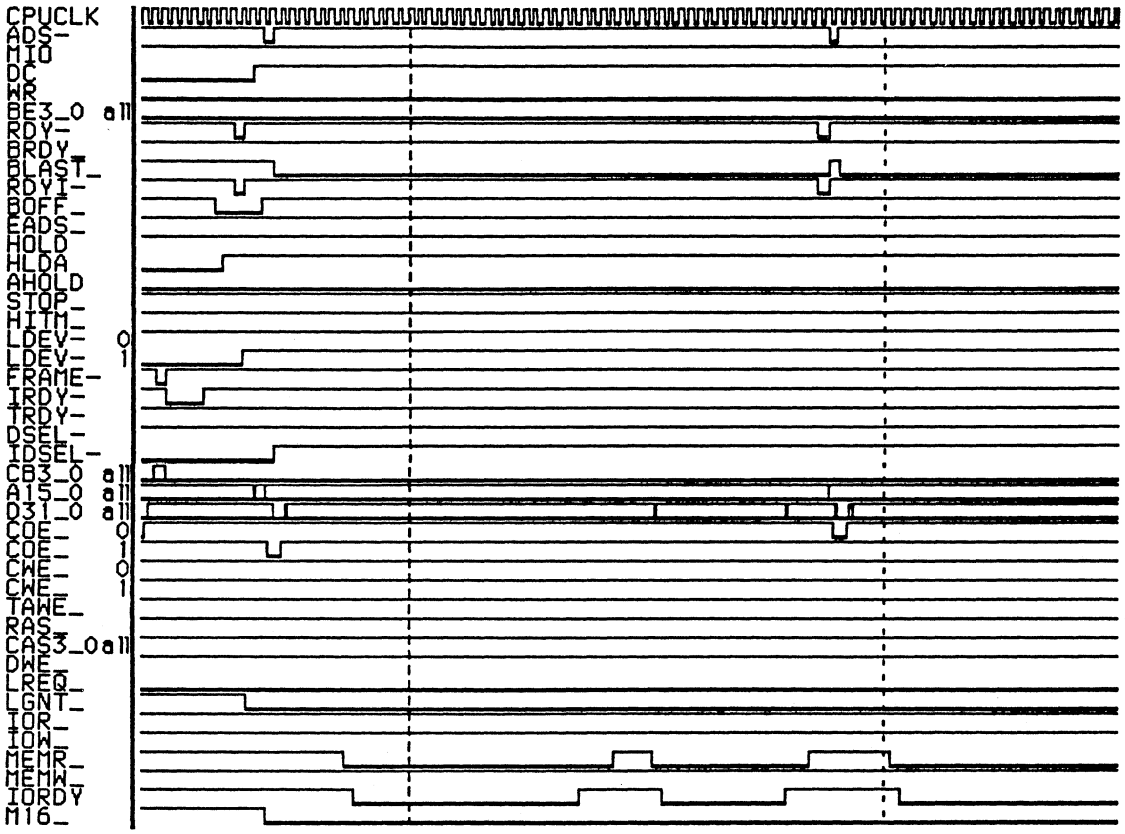


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-33 VESA Master Read from ISA Slave

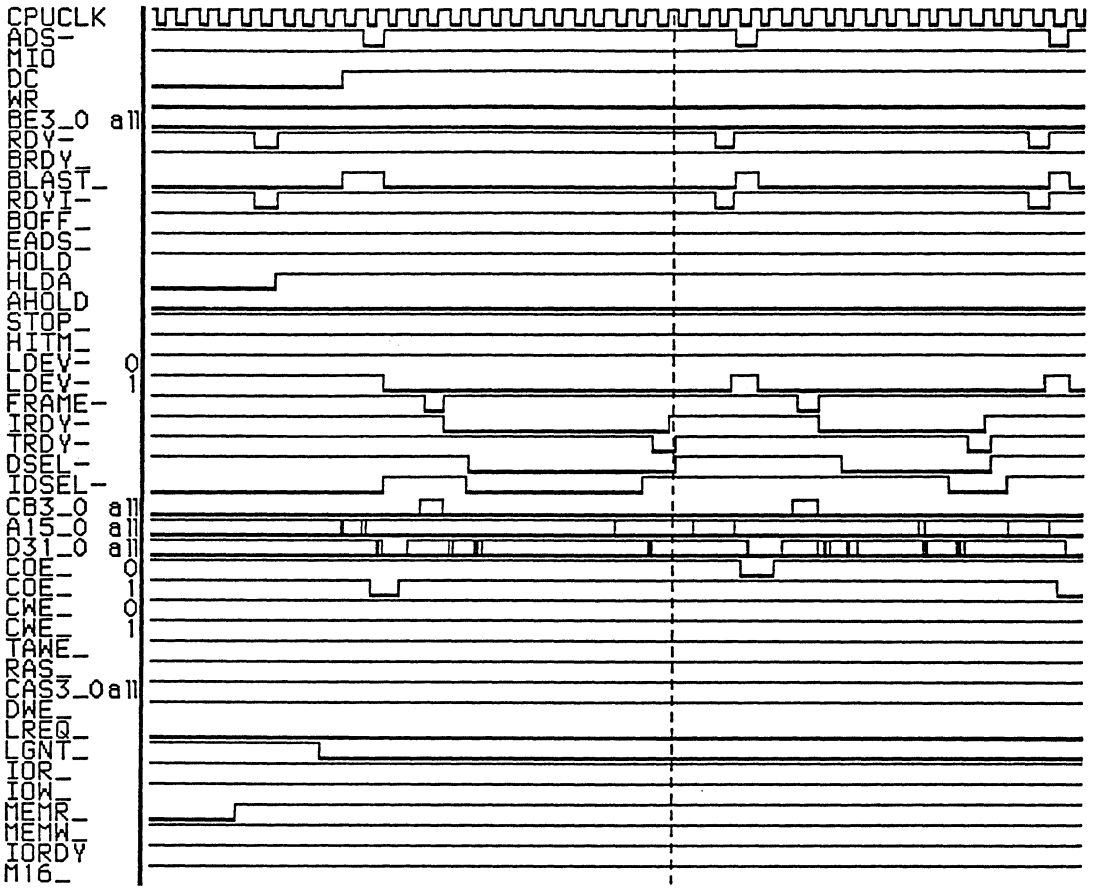


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-34 VESA Master Read from PCI Slave

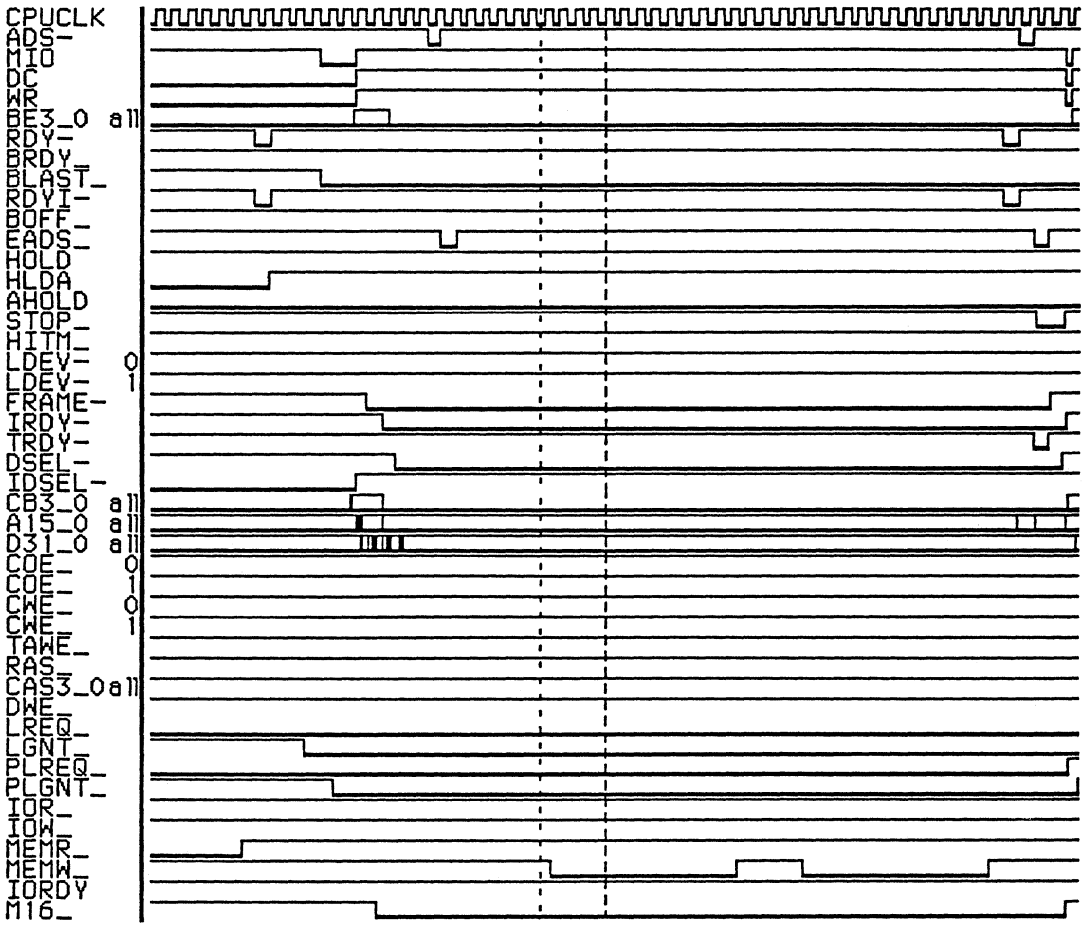


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

Figure 6-35 PCI Master Write to ISA Slave



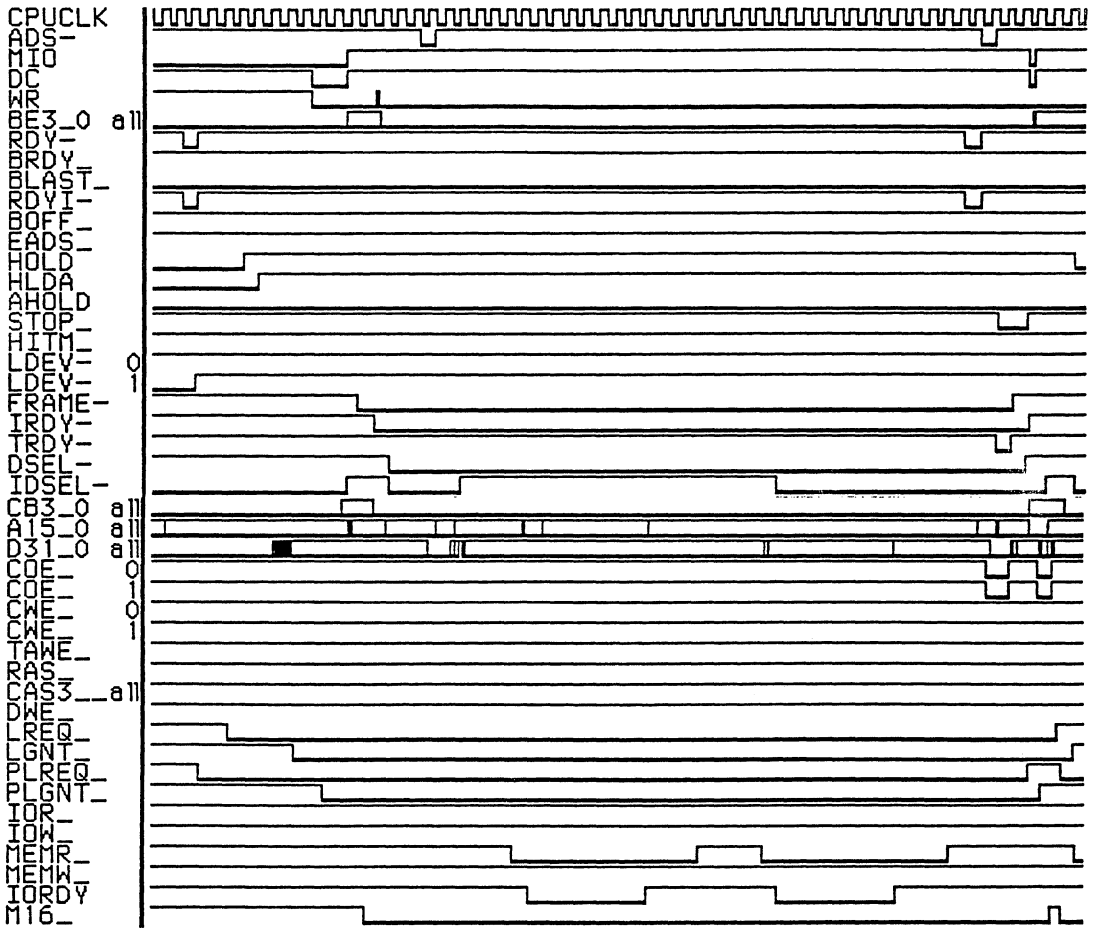
NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-36 PCI Master Read from ISA Slave



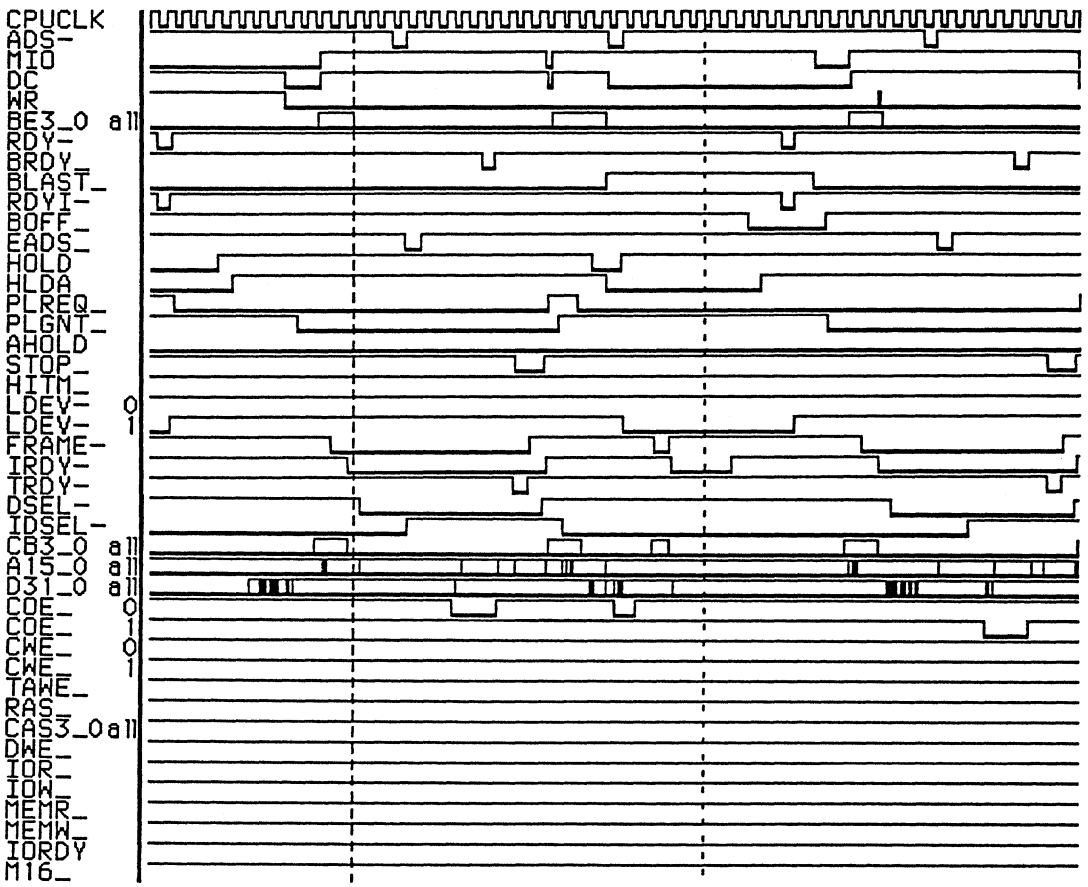
NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-37 PCI Master Read from Cache

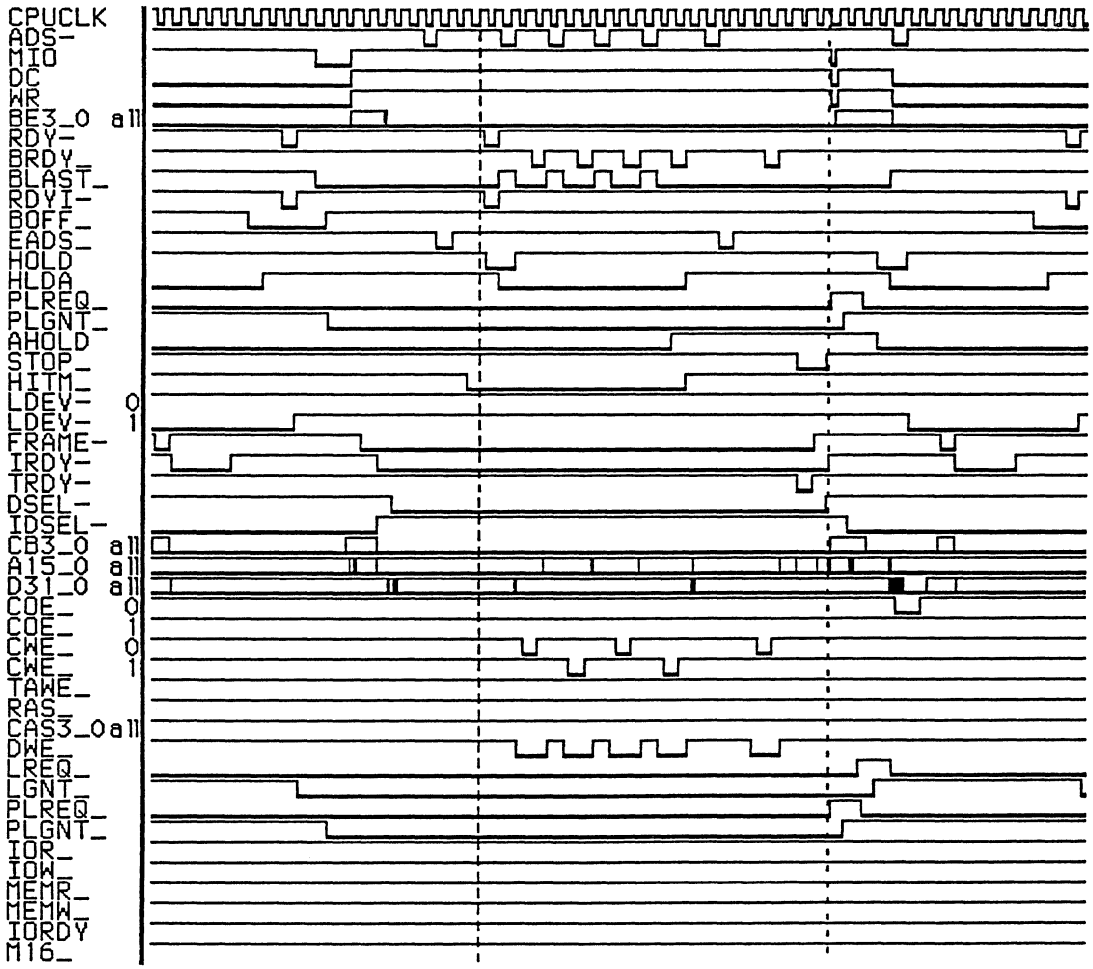


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-38 PCI Master Write to Cache with CPU Write-Back Cycle



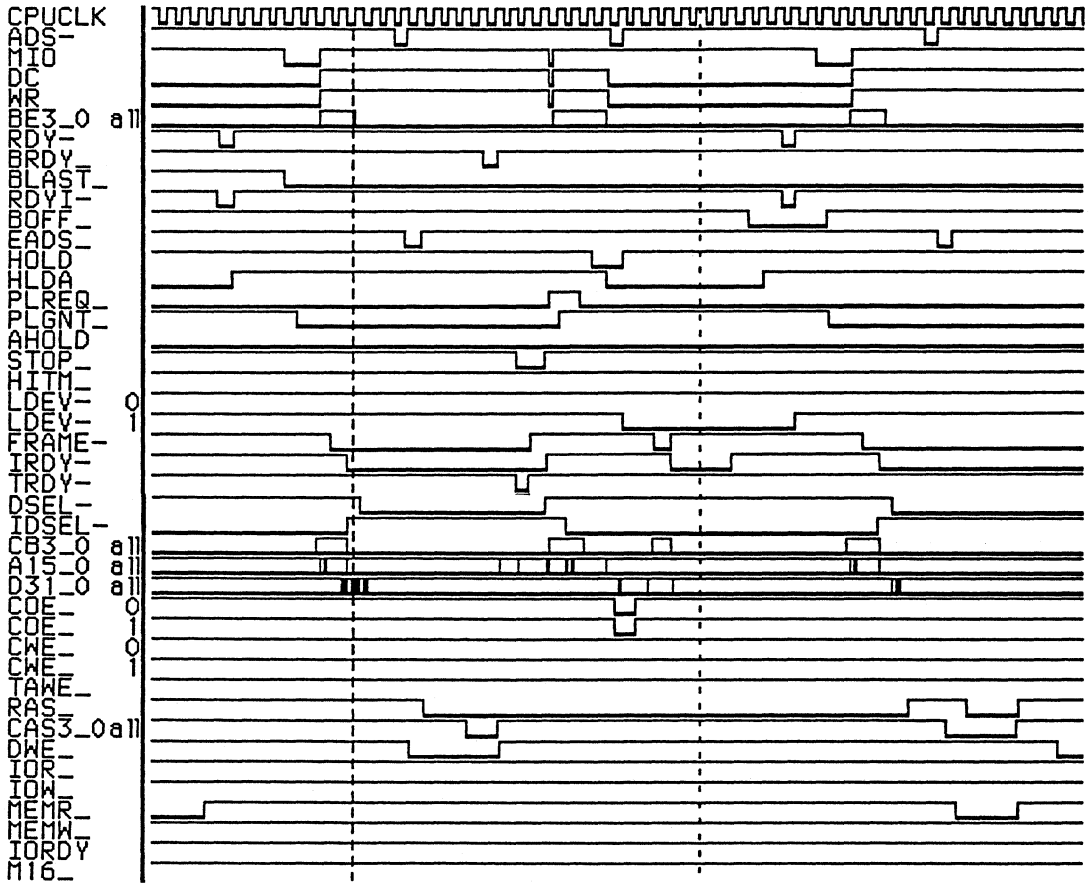
NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE LREQ_ is the LREQ# pin from the 822 to the VL chip set.
LGNT_ is the LGNT# pin from the VL chip set to the 822.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-39 PCI Master Write to DRAM

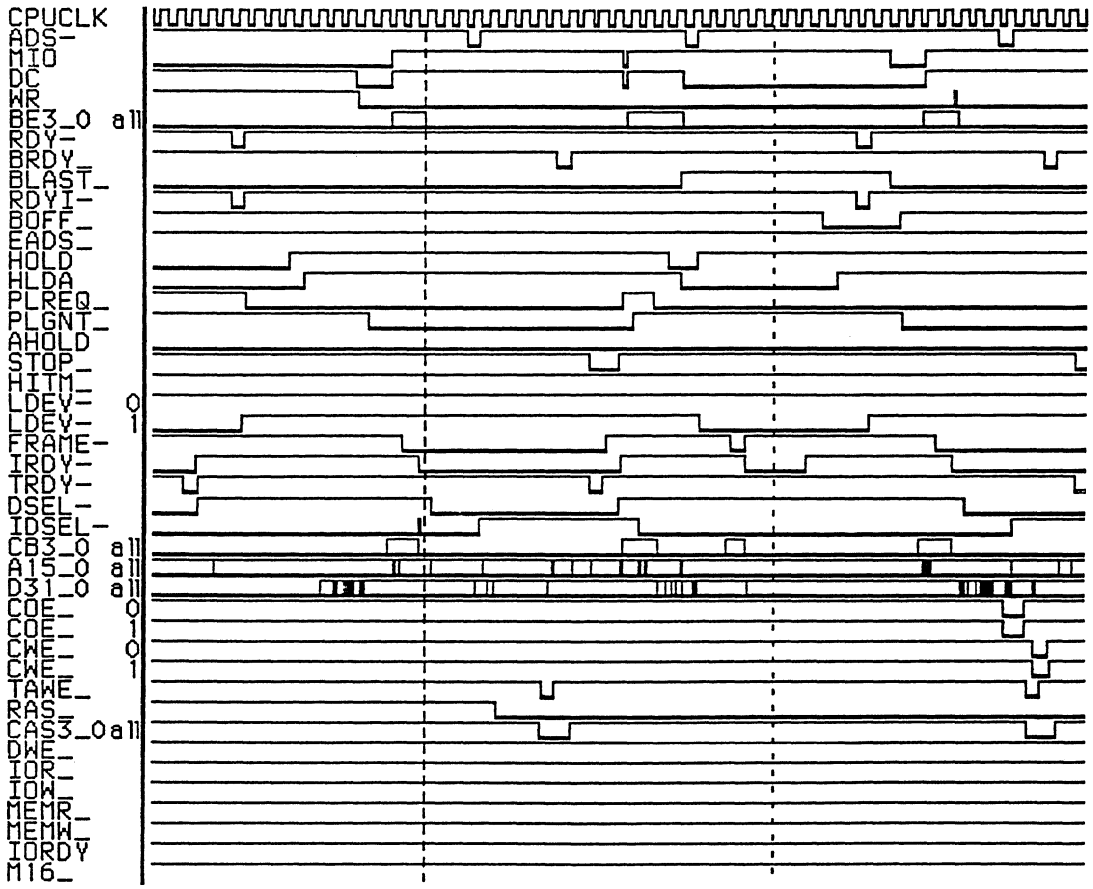


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-40 PCI Master Read from DRAM

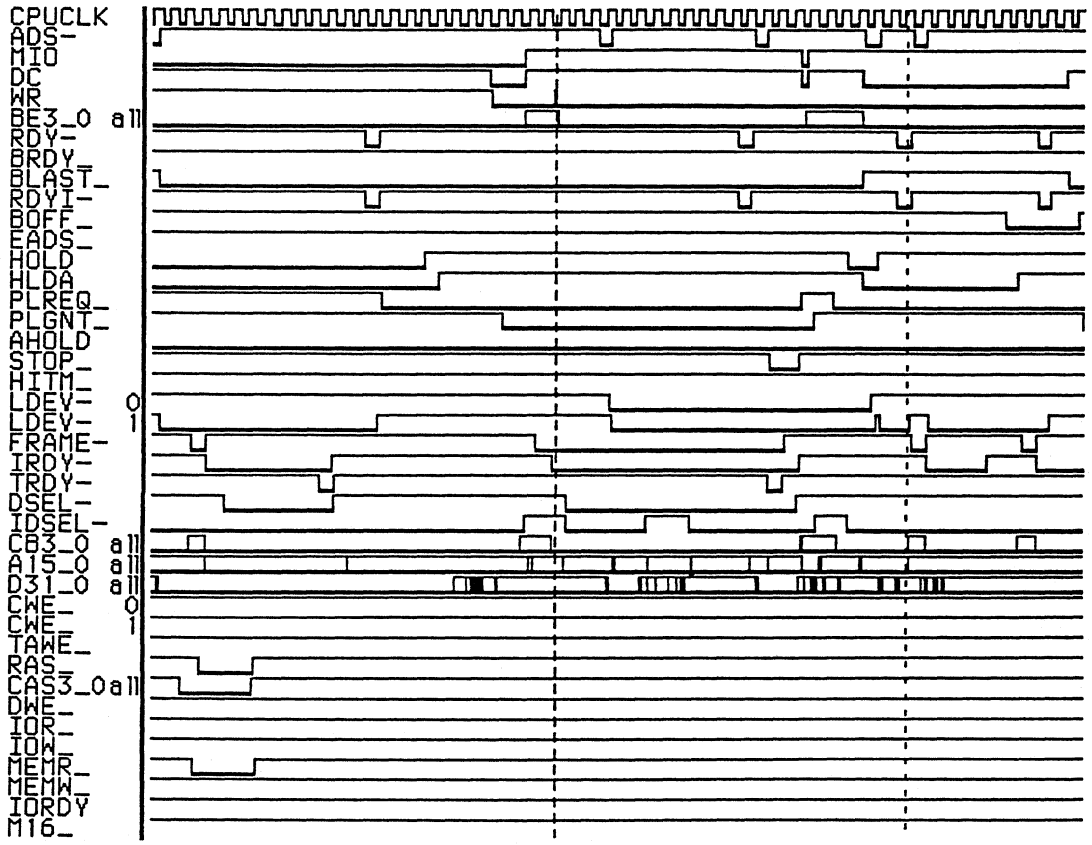


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-41 PCI Master Read from VESA Slave

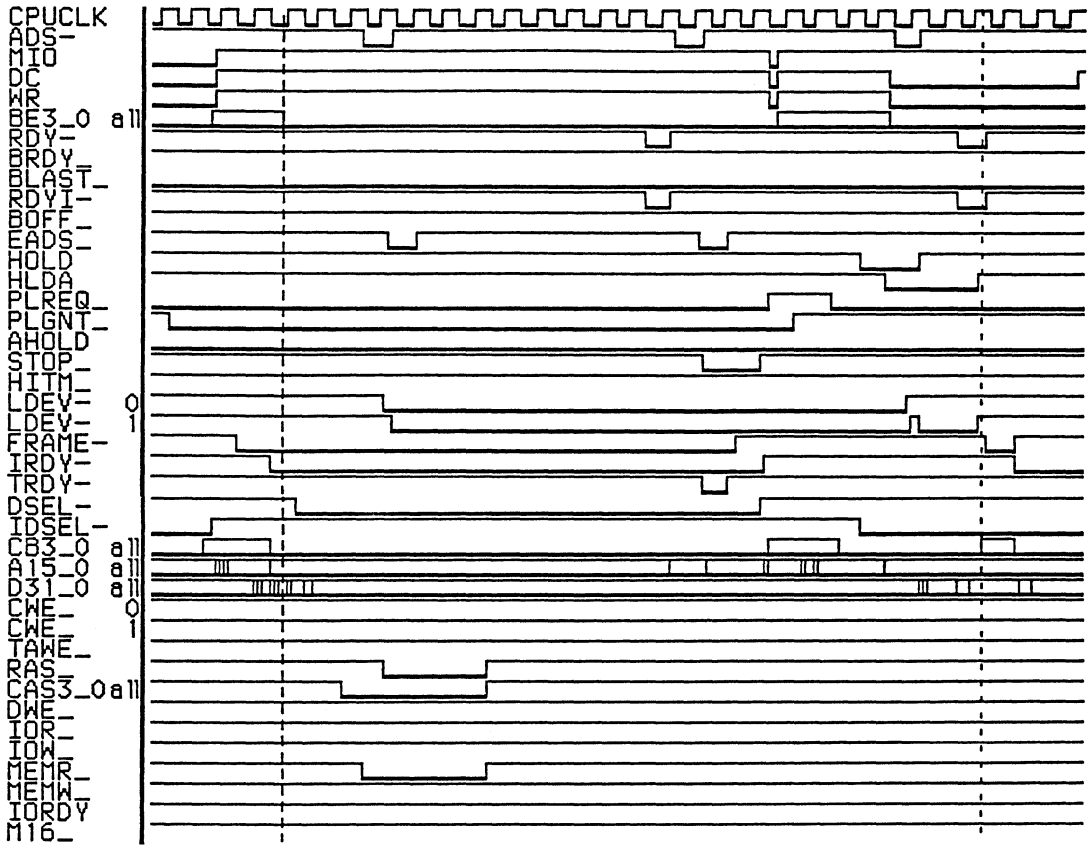


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-42 PCI Master Write to VESA Slave

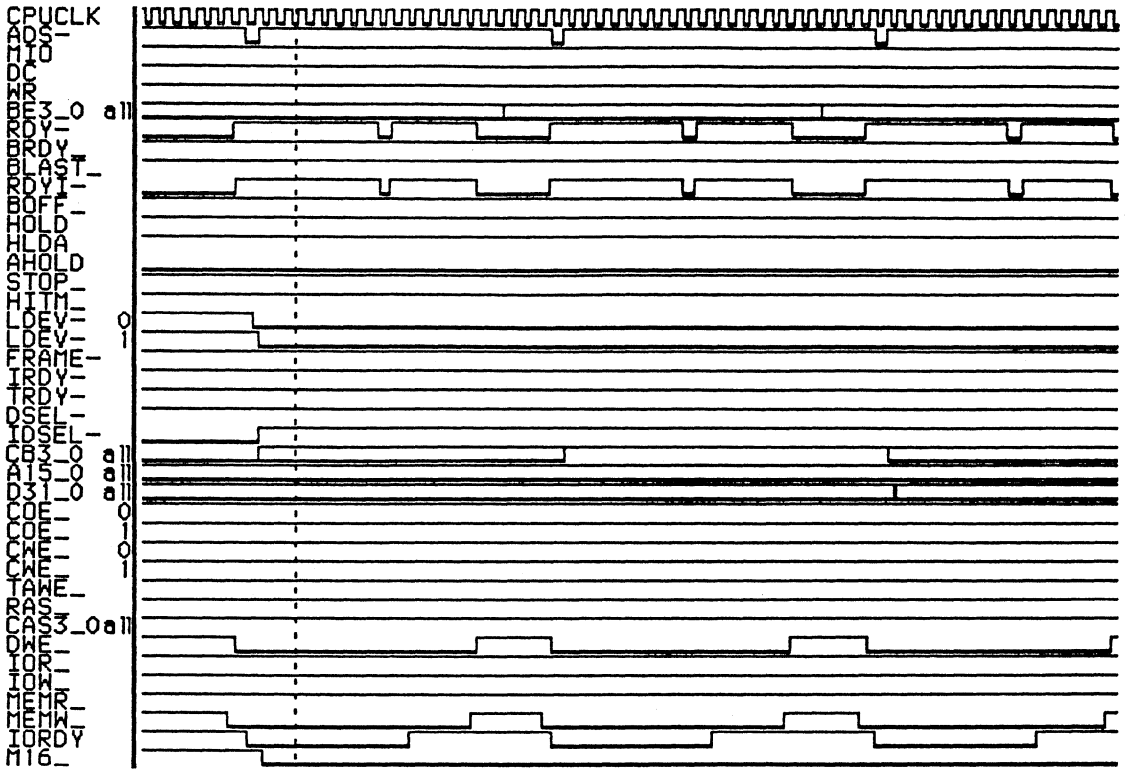


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

NOTE PLREQ_ is the PCI REQ# from the PCI bus master.
PLGNT_ is the PCI GNT# from the 822.

Figure 6-43 ISA Master Write to VESA Slave

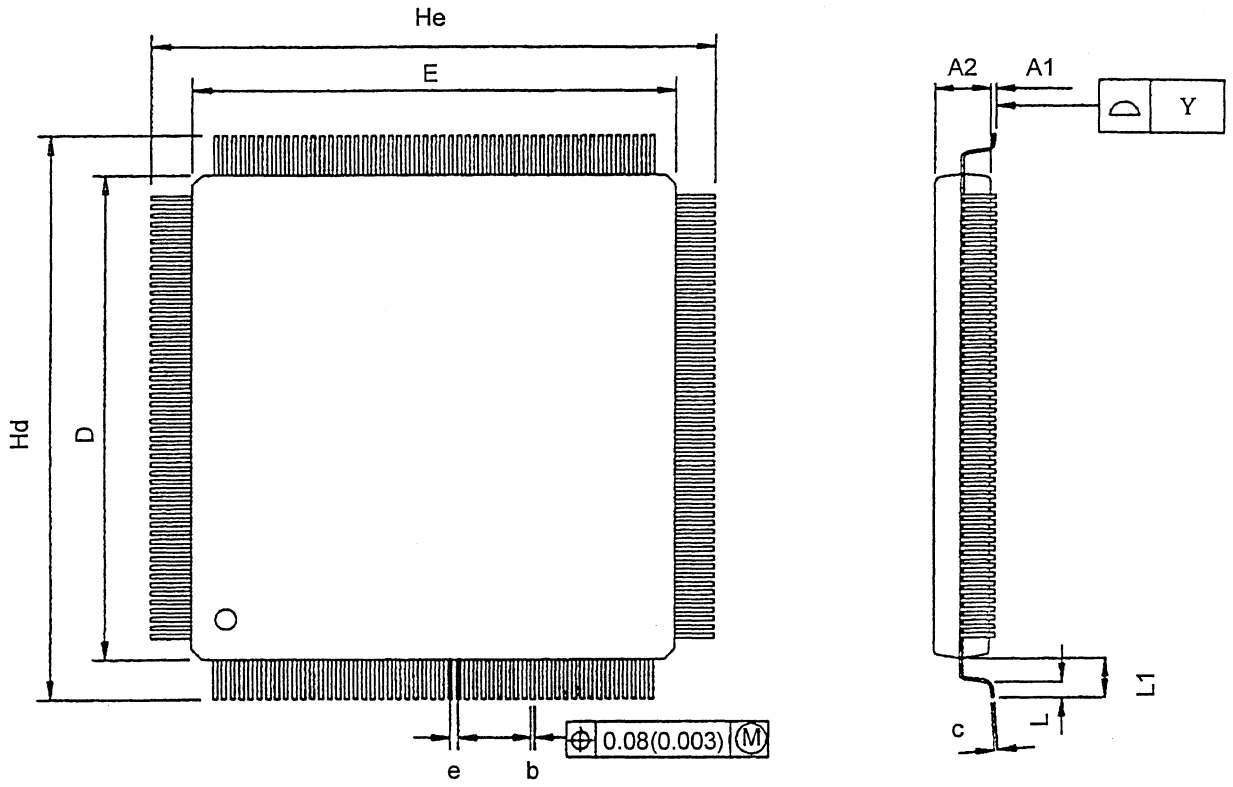


NOTE RDY_ is the RDYRTN# pin of the local bus.
RDYI_ is the LRDY# pin of the local bus.

NOTE LDEV_1 is the LDEV0# pin of the 822.
LDEV_0 is the LDEV# pin of the local bus.

7.0 Mechanical Package Outline

Figure 7-1 208-Pin Plastic Quad Flat Package (PQFP)



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	30.35	30.60	30.85	1.195	1.205	1.215
He	30.35	30.60	30.85	1.195	1.205	1.215
L	0.35	0.50	0.65	0.014	0.020	0.026
L1		1.30			0.051	
Y			0.08			0.003
θ	0		10	0		10

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