OPTi

TriFire

82C842

IEEE 1394 Physical Layer Controller

Preliminary Data Book

MEMBER 1394 TRADE ASSOCIATION THE MULTIMEDIA CONNECTION

OPTi Inc. is a member of the 1394 Trade Association

i.LINK compatible

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TriFire
IEEE 1394 PHY Layer Controller

1.0 Features

- Conforms to the IEEE 1394 -1995 Standard.
- Three 1394 ports each with 100, 200 and 400 Mbit data transmission capabilities.
- Differential receivers and transmitters for each port
- Low-voltage differential signaling
- PLL synthesis of 100, 200 and 400 MHz clocks from standard 25 MHz reference crystals
- Asynchronous packet signaling that provides support for legacy hardware such as printers
- Isochronous packet signaling that provides support for multiple data streams
- Self-ID packets that provide support for power requirements signaling at start-up
- Automatic initialization and configuration of root and client nodes
- PHY-Link-layer Controller (LLC) data communications over 2, 4 or 8 lines
- Single 3.3 V power supply
- Packaged in 64-pin Low-profile Quad Flat Pack (LQFP)

Figure 1-1 TriFire System Block Diagram

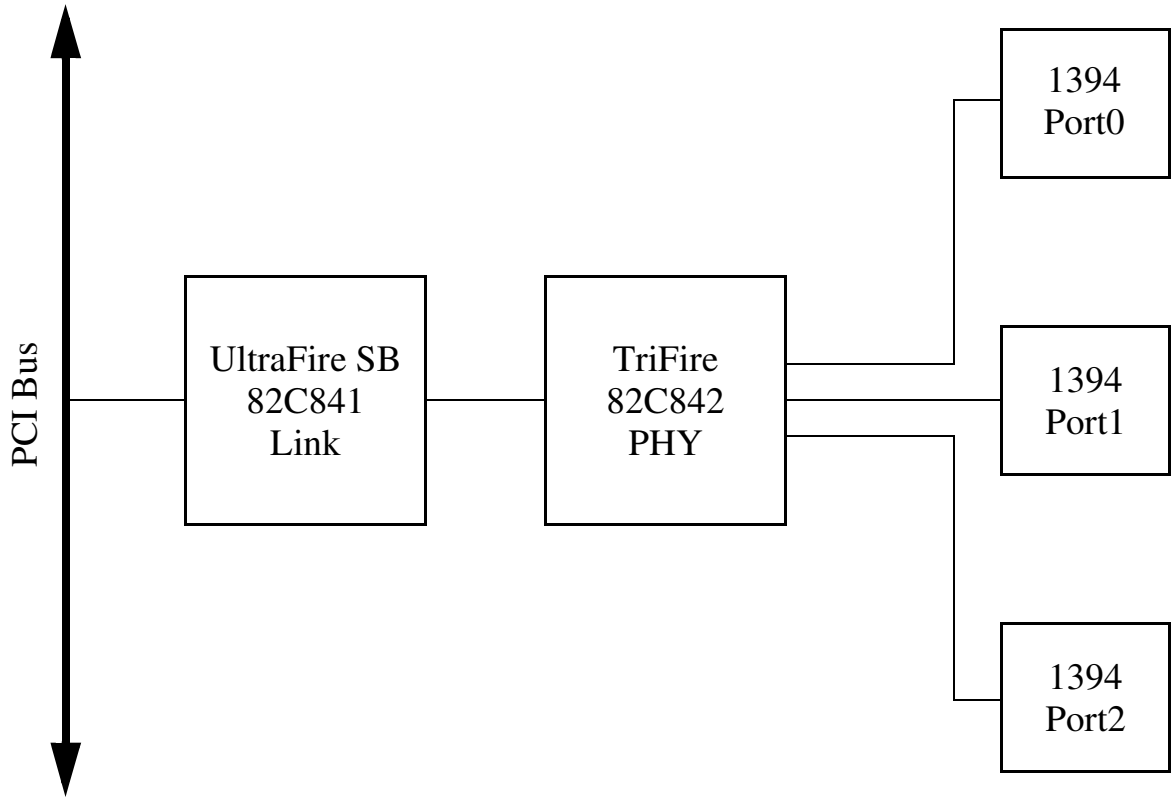
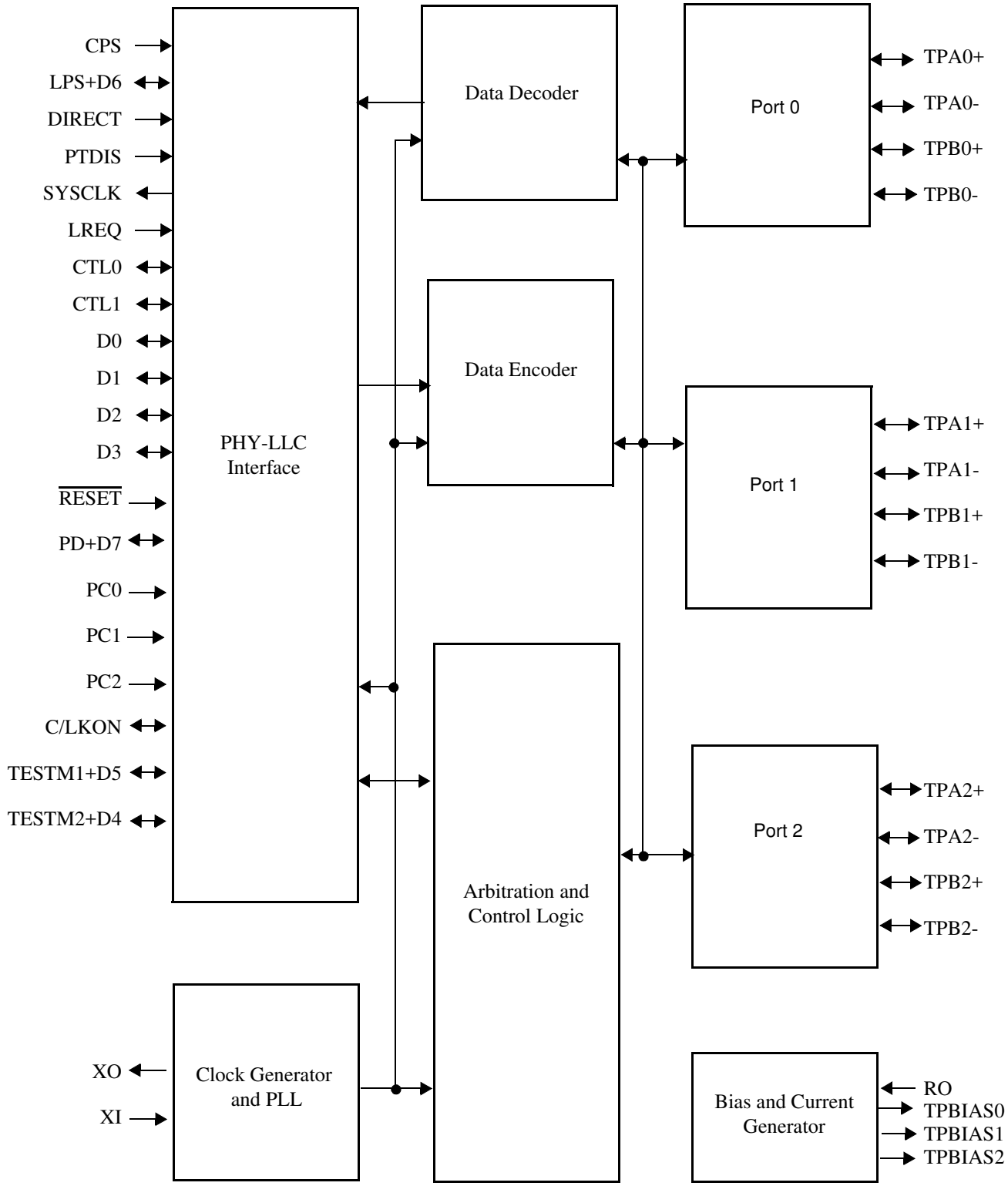


Figure 1-2 TriFire Functional Block Diagram



2.0 Signal Definitions

2.1 Terminology/Nomenclature Conventions

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms “assertion” and “negation” are used extensively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

Some TriFire pins have more than one function. These pins can be time-multiplexed, have strap options, or can be selected via register programming.

The tables in this section use several common abbreviations. Table 2-1 lists the mnemonics and their meanings. Note that TTL/CMOS/Schmitt-trigger levels pertain to inputs only. Outputs are driven at CMOS levels.

Table 2-1 Signal Definitions Legend

Mnemonic	Description
BD	Bidirectional
CMOS	CMOS-level compatible
G	Ground
I	Input
I/O	Input/Output
O	Output
P	Power
S	Schmitt-trigger
TTL	TTL-level compatible

Figure 2-1 TriFire Pin Diagram

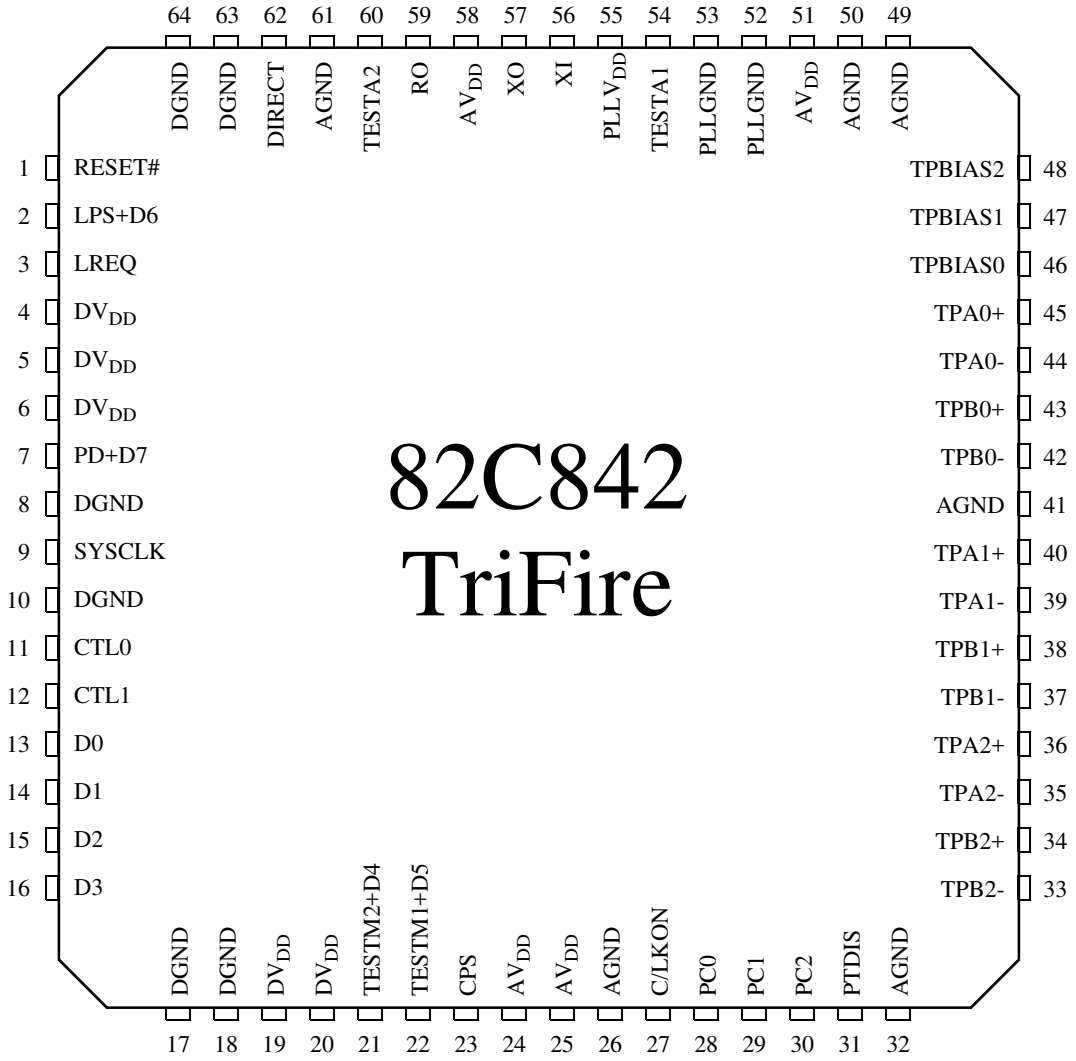
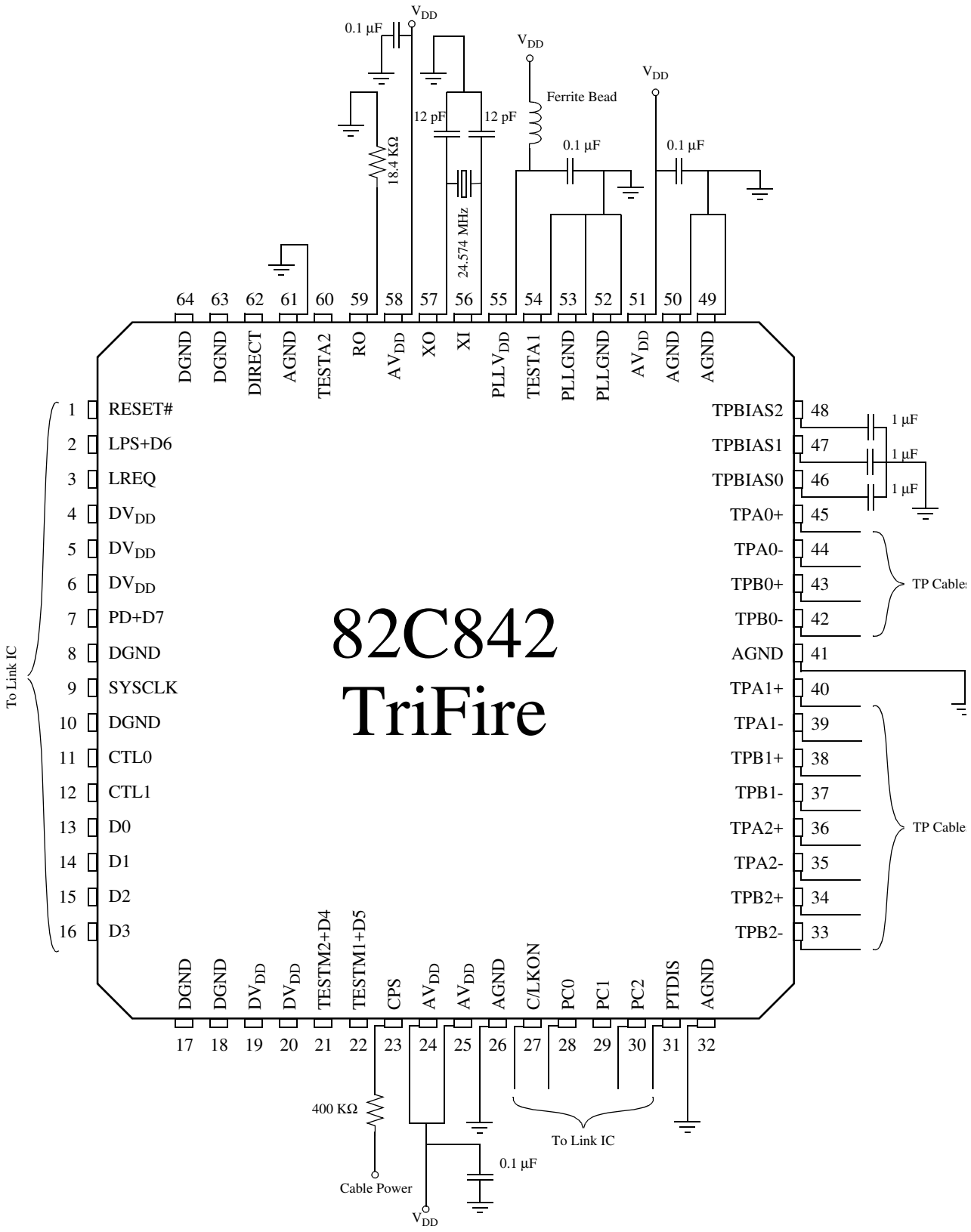


Table 1-1 TriFire Pin Cross-Reference List

Signal Name	Alternative	Pin No.	Pin Type	Power Plane
RESET#		1	I	3.3 V
LPS	D6	2	BD	3.3 V
LREQ		3	I	3.3 V
DV_{DD}		4	P	
DV_{DD}		5	P	
DV_{DD}		6	P	
PD	D7	7	BD	3.3 V
DGND		8	G	
SYSCLK		9	O	3.3 V
DGND		10	G	
CTL0		11	BD	3.3 V
CTL1		12	BD	3.3 V
D0		13	BD	3.3 V
D1		14	BD	3.3 V
D2		15	BD	3.3 V
D3		16	BD	3.3 V
DGND		17	G	
DGND		18	G	
DV_{DD}		19	P	
DV_{DD}		20	P	
TESTM2	D4	21	BD	3.3 V
TESTM1	D5	22	BD	3.3 V
CPS		23	I	Analog
AV_{DD}		24	P	
AV_{DD}		25	P	
AGND		26	P	
C/LKON		27	BD	3.3 V
PC0		28	I	3.3 V
PC1		29	I	3.3 V
PC2		30	I	3.3 V
PTDIS		31	I	3.3 V
AGND		32	G	
TPB2-		33	BD	Analog
TPB2+		34	BD	Analog

Signal Name	Alternative	Pin No.	Pin Type	Power Plane
TPA2-		35	BD	Analog
TPA2+		36	BD	Analog
TPB1-		37	BD	Analog
TPB1+		38	BD	Analog
TPA1-		39	BD	Analog
TPA1+		40	BD	Analog
AGND		41	G	
TPB0-		42	BD	Analog
TPB0+		43	BD	Analog
TPA0-		44	BD	Analog
TPA0+		45	BD	Analog
TPBIAS0		46	O	Analog
TPBIAS1		47	O	Analog
TPBIAS2		48	O	Analog
AGND		49	G	
AGND		50	G	
AV_{DD}		51	G	
PLLGND		52	G	
PLLGND		53	G	
TESTA1		54	O	Analog
$PLLV_{DD}$		55	P	
XI		56	I	Analog
XO		57	O	Analog
AV_{DD}		58	P	
RO		59	O	Analog
TESTA2		60	O	Analog
AGND		61	G	
DIRECT		62	I	3.3 V
DGND		63	G	
DGND		64	G	

Figure 2-2 TTriFire System Implementation Diagram



2.2 TriFire Strapping Options

Four modes have been implemeted in TriFire. Modes 0 and 1 are for internal debugging use only and should never be end-user configurable. Modes 2 and 3 are normal operating modes.

Strap options reflect the corresponding register bits. See Section 5 of this manual for detailed information about the registers.

Table 2-2 Mode Select

Mode	TESTM2 (Pin 21)	TESTM1 (Pin 22)	Description
0	0	0	Reserved - for internal testing only
1	0	1	Reserved - for internal testing only
2	1	0	Speed capability selectable
3	1	1	Speed 200 Mb/s compatible with the TI TSB21LV03

Table 2-3 Mode 2 User Options

Pin No.	Pin Name	Corresponding Register	Description
2 7	LPS+D6 PD+D7	Common page FWR 2 [0:1]	LPS, PD (Speed Control): 00 => S400 (VCO - 400MHz) 01 => S200 (VCO - 400MHz) 10 => S100 (VCO - 400MHz) 11 => S200 (VCO - 200MHz)
31	PTDIS	Page 0 Port 0 FWR 8 [7] Page 0 Port 1 FWR 8 [7] Page 0 Port 2 FWR 8 [7]	1 => disable all ports 0 => enable all ports
28-30	PC[0:2]	Page 2 FWR 8 [0:2]	Power class
11	CTL0	Page 2 FWR 9 [2]	PLL enable: 1 => enable PLL 0 => disable PLL
12	CTL1	Page 2 FWR A [7]	OSC disable: 1 => disable OSC 0 => enable OSC
27	C/LKON	Page 2 FWR 8 [4]	Contender: 1 => contender capable

Table 2-4 Mode 3 User Options

Pin No.	Pin Name	Corresponding Register	Description
28-30	PC[0:2]	Page 2 FWR 8 [0:2]	Power class
27	C/LKON	Page 2 FWR 8 [4]	Contender: 1 => contender capable

3.0 Signal Descriptions

Signal Name	Pin No.	Signal Type (Drive)	Signal Description
AGND	26	G	Analog ground
AGND	32	G	
AGND	41	G	
AGND	49	G	
AGND	50	G	
AGND	61	G	
AV_{DD}	24	P	Analog power
AV_{DD}	25	P	
AV_{DD}	51	P	
AV_{DD}	58	P	
CPS	23	CMOS, Input	Cable power status. Indicates a connection at the input terminal.
CTL0	11	BD, 8 mA	Control I/O.
CTL1	12	BD, 8 mA	
D0	13	BD, 8 mA	Data I/O.
D1	14	BD, 8 mA	
D2	15	BD, 8 mA	
D3	16	BD, 8 mA	
TESTM2 + D4	21	BD, 8 mA	Mode 3: TESTM2 Mode 2: D4
TESTM1 + D5	22	BD, 8 mA	TESTM1 D5
LPS + D6	2	BD, 8 mA	LPS D6
PD + D7	7	BD, 8 mA	PD D7
DGND	8	G	Digital ground.
DGND	10	G	
DGND	17	G	
DGND	18	G	
DGND	63	G	
DGND	64	G	
DV_{DD}	4	P	Digital power.
DV_{DD}	5	P	
DV_{DD}	6	P	
DV_{DD}	19	P	
DV_{DD}	20	P	
DIRECT	62	CMOS Input	Link interface isolation input.
C/LKON	27	BD, 8 mA	

Signal Name	Pin No.	Signal Type (Drive)	Signal Description
LREQ	3	CMOS Input	Link request. The Link Controller signalsTriFire for a data transfer or a service with this pin.
PC0	28	CMOS Input	Power class signals. Self-ID packets encode these inputs to indicate the power class. Pull inputs high to represent a “1” and pull inputs low to represent a “0”.
PC1	29	CMOS Input	
PC2	30	CMOS Input	
PLLGND	52	Analog	PLL ground.
PLLGND	53	Analog	
$PLLV_{DD}$	55	Analog	PLL power.
PTDIS	31	CMOS Input	Port disable. This pin is used as a strapping option.
RESET#	1	Input	Reset input. When this pin receives an active low signal, the bus on the 1394 ports and the internal logic resets.
RO	59	O	Current setting resistor.
SYSCLK	9	8 mA	System clock.
TESTA1	54	Analog Output	Analog test mode control.
TESTA2	60	Analog Output	
TPA0-	44	Analog BD	“A” twisted cable pairs.
TPA0+	45	Analog BD	
TPA1-	39	Analog BD	
TPA1+	40	Analog BD	
TPA2-	35	Analog BD	
TPA2+	36	Analog BD	
TPB0-	42	Analog BD	“B” twisted cable pairs.
TPB0+	43	Analog BD	
TPB1-	37	Analog BD	
TPB1+	38	Analog BD	
TPB2-	33	Analog BD	
TPB2+	34	Analog BD	
TPBIAS0	46	Analog Output	Bias twisted cable pairs. Provides a 1.86 V bias voltage for the 1394 cable drivers.
TPBIAS1	47	Analog Output	
TPBIAS2	48	Analog Output	
XI	56	Analog Input	Crystal oscillator. These pins receive a 24.576 MHz crystal signal.
XO	57	Analog Output	

4.0 Functional Description

The OPTi 82C842 device is a mixed signal Integrated Circuit that contains the full Physical layer implementation of the IEEE1394-1995 standard on a three-port node. This device, also called a PHY, complements the Link Layer Controller IC (LLC) on a IEEE 1394 architecture.

Each port consists of a pair of differential line transceivers and an associated circuitry to accomplish packet reception/transmission as well as perform bus arbitration. The 82C842 is capable of handling both asynchronous and isochronous packets.

An internal PLL circuit generates all necessary clocks for the correct operation under 100, 200 and 400 Mb/s speeds. Only an external 24.576MHz crystal is necessary. The 82C842 also provides the 49.152 MHz clock for communication with the LLC IC.

Some applications require a galvanic isolation between the PHY and the LLC ICs. OPTi's 82C842 implements this function in accordance with Annex J of the IEEE 1394 specification. If pin DIRECT is tied high, normal operation occurs whereas if DIRECT is sensed low, an internal differentiating logic that detects short pulses is engaged.

There are eight data lines between the PHY and the LLC. For 100Mb/s operation, only two lines are used. For 200Mb/s, 4 lines are used and for 400Mb/s, all eight lines transfer valid data between the ICs.

Because the 82C842 was designed to be interchangeable with TI's TSB21LV03x and SONY's CXD1944 PHYs which can operate only up to 200 Mb/s (four data bits used), the upper four data bits necessary for operation at 400 Mb/s were multiplexed with the following functions: PD (power down); LPS (Link Power Status); TESTM1 & TESTM2 (test mode pins). If 400 Mb/s operation is engaged, the alternate pin function is not available.

Four configuration pins are provided in order to set the PC[0:2] bits and the "C" (contender) bit in the self-identification packet The contender bit, if set to one, indicates that this node can be a bus manager. If this bit is set to zero, the node will not try to be a bus manager. The PC[0:2] bits indicate the power requirements or capabilities of the node (sink/source power).

The primary functions of the PHY IC are to serially encode and transmit data packets originated by the LLC and decode serially received data streams forwarding them to the LLC. In addition, the PHY IC has to copy any received data packets at any port to the other two ports (provided a cable is detected), performing clock/data recovery and regeneration.

The common mode voltage present on the TPA pairs is monitored by a special BIAS circuitry that determines if any cable is connected to that port and at what speed the next data packet can be transmitted.

For correct operation of the line drivers, a 112 ohm line-termination is necessary across both TPA and TPB pins. Two 56 ohm serially connected resistors are used for that. The mid-point of the resistor termination on TPA is connected to the TPBIAS voltage pin. The mid-point of the TPB resistor termination is coupled to GND though an RC network.

For complete descriptions of transmitted and received packets as well as PHY-LINK state machine operation, refer to publication number IEEE Std 1394-1995 published by the IEEE Computer Society.

4.1 Self-Loopback Test, Mode 4

Mode 4 can be selected through register selection (Page2, FWR09h) and can be used to transfer up to four bytes of information from one port to another. Parameters such as speed, transmitting port, data packet length, and data to be transmitted can be set. Data to be transmitted is displayed in Page3, FWR08h - FWR0Bh and data received is displayed in Page3, FWR0Ch - FWR0Fh.

5.0 TriFire Register Space

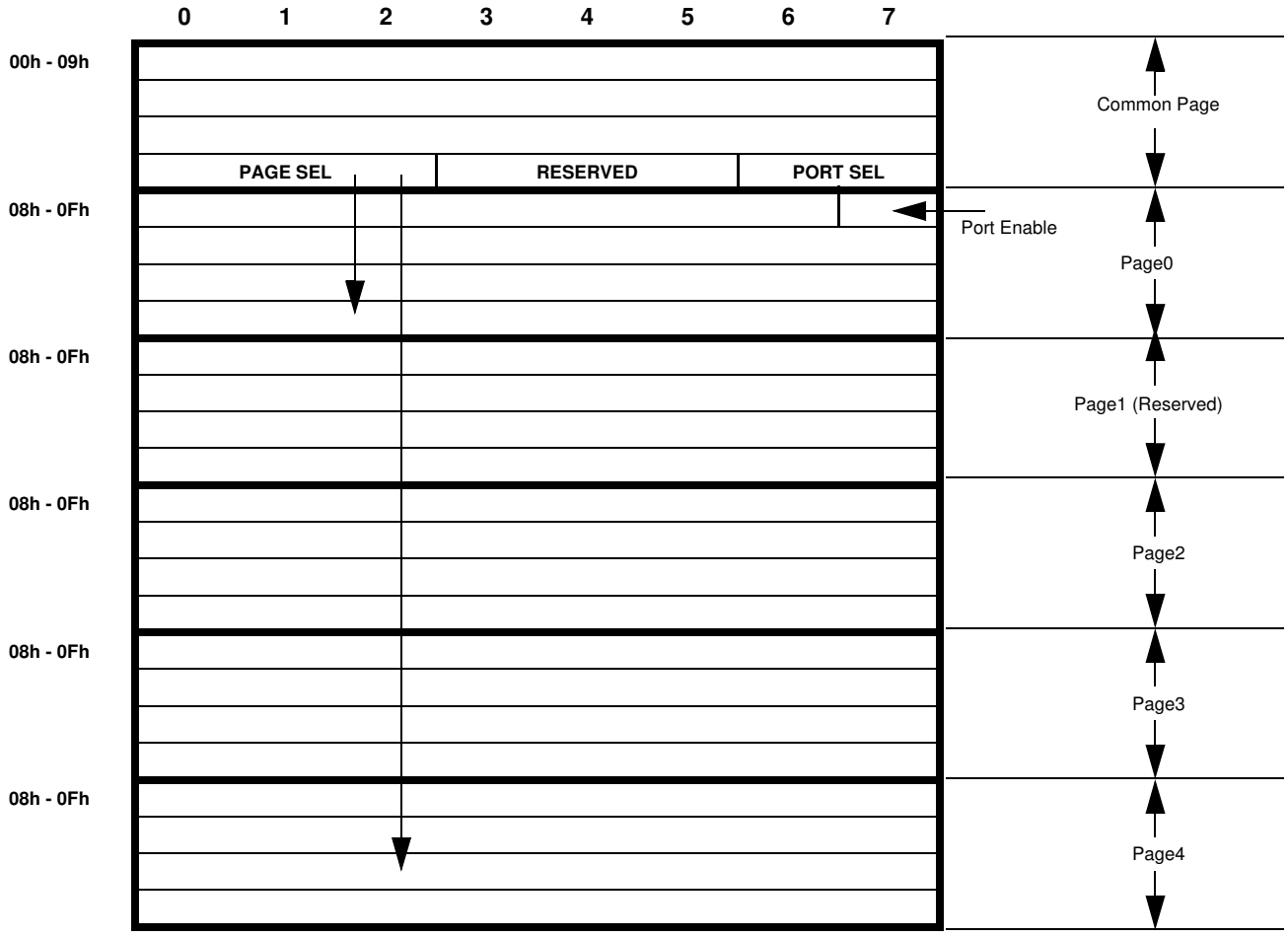
5.1 Register Pages

TriFire registers divide into six pages:

- Common Page Registers
- Page 0 Registers
- Page 1 Registers
- Page 2 Registers
- Page 3 Registers
- Page 4 Registers

The eight Common Page registers are mapped from 0h to 7h. Page 0, 1, 2, 3 and 4 share the same register address range: 08h to 0Fh. Page selection is done through the 3-bit page selection register, 07h[0:2], on the Common Page.

5.1.1 TriFire Register Structure.



5.1.2 Register Access Mechanism
TriFire register space maps through the 1394 link controller. Refer to the data book of the link controller for the design.

5.1.3 Convention
All register bits are read/write with their default value initialized to 0 unless otherwise specified.

All reserve bits should be kept untouched.

5.1.4 Register Bit Description
Section 5.1.4.1 through Section 5.1.4.6 give the bit formats for accessible registers in Trifire

NOTE: "(*)" indicates the power-on strapping option.

5.1.4.1 Common Page Registers

0	1	2	3	4	5	6	7
FWR 00h			**Phy ID and Root Status Register**				**Default = 00h**
Shows physical ID (000000) (RO)						Shows Root: 0 = Not root 1 = Root (RO)	Shows CPS Cable Power Status: 0 = Disable 1 = Enable (RO)
FWR 01h			**Root Hold-Off and Gap Count Registers**				**Default = 3Fh**
Selects root hold-off bit: 0 = Disable 1 = Enable (*)	Initialize Bus Reset: 0 = Disable 1 = Enable (*)	Selects gap count Default = 111111					
FWR 02h			**Phy Speed and Port Quantity Registers**				**Default = 23h**
Shows PHY speed 00 = S100 01 = S200 10 = S400 11 = Reserved (RO) (*)	Shows Enhanced Register Map: Default = 1 (RO) (*)	Shows the number of ports (00011) (RO)					
FWR 03h			**Port 0 Status Register**				**Default = 00h**
Shows the TPA Status of Port 0 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)	Shows the TPB Status of Port 0 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)	Shows the status of the device attached to Port 0 0 = Parent 1 = Child or disconnected (RO)	Shows the status of Port 0 0 = Disconnected 1 = Connected (RO)	Reserved			

5.1.4.1 Common Page Registers (cont.)

0	1	2	3	4	5	6	7
FWR 04h			**Port 1 Status Register**				**Default = 00h**
Shows the TPA Status of Port 1. 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)		Shows the TPB Status of Port 1. 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)		Shows the status of the device attached to Port1. 0 = Parent 1 = Child or disconnected (RO)	Shows the status of Port 1. 0 = Disconnected 1 = Connected (RO)	Reserved	
FWR 05h			**Port 2 Status Register**				**Default = 00h**
Shows TPA Status of Port 2. 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)		Shows the TPB Status of Port 2. 00 = Data 0 01 = High impedence 10 = Not used 11 = Data 1 (RO)		Shows the status of the device attached to Port 2. 0 = Parent 1 = Child or dis connected (RO)	Shows the status of Port 2. 0 = Disconnected 1 = Connected (RO)	Reserved	
FWR 06h			**1394 Environment Register**				**Default = 49h**
Shows the status of the Cable/Back-plane Environment: 00 = Back-plane 01 = Cable (Default) 10 = Reserved 11 = Reserved (RO)		Shows the number of additional registers followed (001001) (RO)					
FWR 07h			**Page and Port Selector Register**				**Default = 00h**
Page Selector: 000 = Page 0 Registers (Default) 001 = Page 1 Registers 010 = Page 2 Registers 011 = Reserved 1xx = Reserved		Reserved Register must be initialized to 000			Port Selector: 00 = Port 0 (Default) 01 = Port 1 10 = Port 2 11 = Reserved (*)		

5.1.4.2 Page0 - Port Status Registers

Port 0 Status Register

0	1	2	3	4	5	6	7
FWR 08h			**Port 0 Status Register**				**Default = 00h**
Reserved Register must be initialized to 000000							Enables Port 0 0 = Enable 1 = Disable
FWR 09h - 0Fh			**Reserved**				**Default = 00h**

Port 1 Status Register

0	1	2	3	4	5	6	7
FWR 08h			**Port 1 Status Register**				**Default = 00h**
Reserved Register must be initialized to 000000							Enables Port 1 0 = Enable 1 = Disable
FWR 09h - 0Fh			**Reserved**				**Default = 00h**

Port 2 Status Register

0	1	2	3	4	5	6	7
FWR 08h			**Port 2 Status Register**				**Default = 00h**
Reserved Register must be initialized to 000000							Enables Port 2 0 = Enable 1 = Disable
FWR 09h - 0Fh			**Reserved**				**Default = 00h**

5.1.4.3 Page1 - Identification Registers

0	1	2	3	4	5	6	7
FWR 08h-09h			**Reserved**				**Default = 00h**
FWR 0Ah			**Vendor ID Low Byte Register**				**Default = 45h**
Vendor ID Low Byte (RO)							
FWR 0Bh			**Vendor ID High Byte Register**				**Default = 10h**
Vendor ID High Byte (RO)							
FWR 0Dh			**Device ID Low Byte Register**				**Default = 42h**
Device ID Low Byte (RO)							
FWR 0Eh			**Device ID High Byte Register**				**Default = 08h**
Device ID High Byte (RO)							

5.1.4.3 Page1 - Identification Registers

0	1	2	3	4	5	6	7
FWR 0Fh			**Revision ID Register**				**Default = 00h**
Revision ID (RO)							

5.1.4.4 Page2 - Vendor Dependent Registers

0	1	2	3	4	5	6	7
FWR 08h			**Power Class and Contender Bit Registers**				**Default = 10h**
Selects power class bits in Self-ID packet. Power consumption and source characteristics: 000 Node does not need power and does not repeat power. 001 Node is self-powered and provides a minimum of 15W to the bus 010 Node is self-powered and provides a minimum of 30W to the bus. 011 Node is self-powered and procides a minimum of 45W to the bus. 100 Node may be powered from the bus and is using up to 1W. 101 Node is powered from the bus and is using up to 1W. An additional 2W is needed to enable the Link and higher layers. 110 Node is powered from the bus and is using up to 1W. An additional 5W is needed to enable the Link and higher layers. 111 Node is powered from the bus and is using up to 1W. An additioanl 9W is needed to enable the Link and higher layers. (*)			Link active bit in self-ID Packet: 0 = Disable 1 = Enable (Default) (*)	Selects contender bit in self-ID packet: 0 = Disable 1 = Enable (*)	Short expiration simulation bits. Reserved for internal use only, not for application use.		Internal simulation bits for arbitration. Reserved for internal use only, not for application use.
FWR 09h			**PLL and Debounce Time Registers**				**Default = 00h**
Selects PLL clock frequency control: 00 = 400MHz (VCO=400MHz) 01 = 200MHz (VCO=400MHz) 10 = 100MHz (VCO=400MHz) 11 = 200MHz (VCO=200MHz) (*)	Enables PLL using external clock source: 0 = Disable PLL 1 = Enable PLL (*)	Enables fast debouncing clock used in port status debouncing circuit. 0 = Disable, using 1.52KHz clock 1 = Enable, using 6.25MHz clock (*)	Selects the number of clocks for debouncing the status port. 000 = 0 CLKs — 6.25MHz: 0us — 1.52KHz: 0ms 001 = 5 CLKs — 0.8us — 3.3ms 010 = 20 CLKs — 3.2us — 13.1ms 011 = 40 CLKs — 6.4us — 26.2ms 100 = 80 CLKs — 12.8us — 52.4ms 101 = 200 CLKs — 32.0us — 131.1ms 110 = 518 CLKs — 82.9us — 339.5ms 111 = 1023 CLKs — 163.7us — 670.4ms (*)			Register Read/Write: Reserved for internal use only. Not for application use. Do not program this bit.

5.1.4.4 Page2 - Vendor Dependent Registers (cont.)

0	1	2	3	4	5	6	7
FWR 0Ah			**Mode 4 Tx Port Select and Port Stauts Registers**				**Default = 00h**
Selects transmitting ports in test Mode 4: 1XX = Port 0 transmits X1X = Port 1 transmits XX1 = Port 2 transmits (Default = 000) NOTE: Multiple transmitting ports can be selected.			Selects link-on event: 0 = P1394A compatible, active-high signal as link-on event 1 = TI compatible 6.25 MHz clock as link-on event (Default = 0)				Disables the on-chip oscillator using external clock source instead of 25 MHz crystal: 0 = Enable oscillator 1 = Disable oscillator (*)
FWR 0Bh			**Mode Select/Status REgisters**				**Default = 00h**
Mode 0 - Simulation mode (RO) (*) Reserved for internal use only. Not for application use.	Mode 1 - Analog transceiver mode (RO) (*) Reserved for internal use only. Not for application use.	Mode 2 - Programmable speed mode (RO) (*) Reserved for internal use only. Not for application use.	Mode 3 - Normal TI TSB21LV03 compatible operation mode: 0 = Disable 1 = Enable (RO) (*)	Mode 4 - Self loopback mode: 0 = Disable 1 = Enable (Default = 0)	Mode 5 - Counter Test Mode: 0 = Disable 1 = Enable (Default = 0) Reserved for internal use only. Not for application use.	Reserved	
FWR Ch			**Mode 4 Parameter 1 Registers**				**Default = 00h**
Selects data-prefix time to be transmitted in Mode 4 0000 = 1 SYSCLK (Default) 0001 = 2 SYSCLK's 0010 = 3 SYSCLK's 0011 = 4 SYSCLK's 0100 = 5 SYSCLK's 0101 = 6 SYSCLK's 0110 = 7 SYSCLK's 0111 = 8 SYSCLK's 1000 = 9 SYSCLK's 1001 = 10 SYSCLK's 1010 = 11 SYSCLK's 1011 = 12 SYSCLK's 1100 = 13 SYSCLK's 1101 = 14 SYSCLK's 1110 = 15 SYSCLK's 1111 = 16 SYSCLK's				Selects length of data packet to be transmitted in Mode 4 000 = 0 byte (Default) 001 = 1 byte 010 = 2 bytes 011 = 3 bytes 100 = 4 bytes 1xx = Reserved			Disables the condition from any state to state R0 (i.e., disable bus reset) 0 = Enable entry to state R0 1 = Disable entry to state R0 (Default = 0)

5.1.4.4 Page2 - Vendor Dependent Registers (cont.)

0	1	2	3	4	5	6	7

FWR Dh — **Mode 4 Parameter 2 and Connection Registers** — **Default = 02h**

Bits 0–3	Bit 4	Bit 5	Bit 6	Bit 7
Selects data-end time to be transmitted in Mode 4: 0000 = 1 SYSCLK (Default) 0001 = 2 SYSCLK's 0010 = 3 SYSCLK's 0011 = 4 SYSCLK's 0100 = 5 SYSCLK's 0101 = 6 SYSCLK's 0110 = 7 SYSCLK's 0111 = 8 SYSCLK's 1000 = 9 SYSCLK's 1001 = 10 SYSCLK's 1010 = 11 SYSCLK's 1011 = 12 SYSCLK's 1100 = 13 SYSCLK's 1101 = 14 SYSCLK's 1110 = 15 SYSCLK's 1111 = 16 SYSCLK's	Selects speed of packet to be transmitted in Mode 4: 00 = S100 (Default) 01 = S200 10 = S400 11 = Reserved		Link-side driving strength: Reserved for internal use only. Not for application use.	Port detection control: Reserved for internal use only. Not for application use.

FWR Eh — **Mode 4 Parameter 3 Register** — **Default = 00h**

Selects low-byte clock data-prefix time for transmitting signals in Mode 4:

00000000 = No speed signals during first 8 CLKs (Default)
1xxxxxxx = Speed signal is active in 1st CLK of data-prefix
x1xxxxxx = Speed signal is active in 2nd CLK of data-prefix
xx1xxxxx = Speed signal is active in 3rd CLK of data-prefix
xxx1xxxx = Speed signal is active in 4th CLK of data-prefix
xxxx1xxx = Speed signal is active in 5th CLK of data-prefix
xxxxx1xx = Speed signal is active in 6th CLK of data-prefix
xxxxxx1x = Speed signal is active in 7th CLK of data-prefix
xxxxxxx1 = Speed signal is active in 8th CLK of data-prefix

Note: Multiple data-prefix times can be selected

FWR Fh — **Mode 4 Parameter 4 Register** — **Default = 00h**

Selects high-byte clock data-prefix time for transmitting signals in Mode 4.

00000000 = No speed signals during second 8 CLKs (Default)
1xxxxxxx = Speed signal is active in 9th CLK of data-prefix
x1xxxxxx = Speed signal is active in 10th CLK of data-prefix
xx1xxxxx = Speed signal is active in 11th CLK of data-prefix
xxx1xxxx = Speed signal is active in 12th CLK of data-prefix
xxxx1xxx = Speed signal is active in 13th CLK of data-prefix
xxxxx1xx = Speed signal is active in 14th CLK of data-prefix
xxxxxx1x = Speed signal is active in 15th CLK of data-prefix
xxxxxxx1 = Speed signal is active in 16th CLK of data-prefix

Note: Multiple data-prefix times can be selected

5.1.4.5 Page3 - Vendor Dependent Registers

0	1	2	3	4	5	6	7
FWR 08h			**Mode 4Mode Parameter 5 Register**				**Default = 00h**
1st byte to be transmitted in Mode 4							
FWR 09h			**Mode 4 Parameter 6 Register**				**Default = 00h**
2nd byte to be transmitted in Mode 4							
FWR 0Ah			**Mode 4 Parameter 7 Register**				**Default = 00h**
3rd byte to be transmitted in Mode 4							
FWR 0Bh			**Mode 4 Parameter 8 Register**				**Default = 00h**
4th byte to be transmitted in Mode 4							
FWR 0Ch			**Mode 4 Parameter 9 Register**				**Default = 00h**
1st byte to be received in Mode 4 (RO)							
FWR 0Dh			**Mode 4 Parameter 10 Register**				**Default = 00h**
2nd byte to be received in Mode 4 (RO)							
FWR 0Eh			**Mode 4 Parameter 11 Register**				**Default = 00h**
3rd byte to be received in Mode 4 (RO)							
FWR 0Fh			**Mode 4 Parameter 12 Register**				**Default = 00h**
4th byte to be received in Mode 4 (RO)							

5.1.4.6 Page4 - Vendor Dependent Registers

0	1	2	3	4	5	6	7
FWR 08h			**Read Maximum Port Speed Register**				**Default = 00h**
Port speed bits during ID process Reserved for internal use only. Not for application use.							
FWR 09h			**Force Maximum Port Speed Register**				**Default = FCh**
Port speed bits Reserved for internal use only. Not for application use.						Data phase / data end condition control. Reserved for internal use only. Not for application use.	Request transition control. Reserved for internal use only. Not for application use.
FWR 0Ah			**Mode 5 Paramenter Registers**				**Default = 00h**
Timer/counter control Reserved for internal use only. Not for application use.				Reset time Reserved for internal use only. Not for application use.		Analog test modes Reserved for internal use only. Not for application use.	

5.1.4.6 Page4 - Vendor Dependent Registers (cont.)

0	1	2	3	4	5	6	7
FWR 0Bh							**Default = FCh**
Port 0 speed. Reserved for internal use only. Not for application use.		Port 1 speed. Reserved for internal use only. Not for application use.		Port 2 speed. Reserved for internal use only. Not for application use.		State time out packet control. Reserved for internal use only. Not for application use.	Idle state register. Reserved for internal use only. Not for application use.
FWR 0Ch - 0Fh				**Reserved**			**Default = 00h**

6.0 Electrical Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VCC	Supply Voltage	0.3	4.0	V
VI	Input Voltage	–0.5	VCC + 0.5	V
VO	Output Voltage	–0.5	VCC + 0.5	V
TOP	Operating Temperature	0	+85	°C
TSTG	Storage Temperature			°C

6.2 Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
VDD	Supply voltage	Source power node	3.0	3.6	V
VIH	High level input voltage	CMOS inputs	+2.0	VDD + 0.5	V
VIL	Low level input voltage	CMOS inputs	-0.5	+0.8	V
VID	Differential input voltage during data reception	100 Mbit operation	142	260	mV
		200 Mbit operation	132	260	
		400 Mbit operation	118	260	
VIC	Common Mode input voltage	100 Mbit operation	1.165	2.515	V
		200 Mbit operation	0.935	2.515	
		400 Mbit operation	0.523	2.515	
	Receive input jitter	100 Mbit operation	-	+/-1.08	ns
		200 Mbit operation		+/-0.5	
		400 Mbit operation		+/-.315	
	Receive input skew	100 Mbit operation	-	+/-0.8	ns
		200 Mbit operation		+/-0.55	
		400 Mbit operation		+/-0.50	

6.2.1 Switching Characteristics

Parameter	Measured	Condition	Min	Max	Units
Jitter, transmit	TPA, TPB	100Mbit operation		+/-0.80	ns
		200Mbit operation		+/-0.25	ns
		400Mbit operation		+/-0.15	ns
Skew rate, transmit	Between TPA and TPB	100Mbit operation		+/-0.40	ns
		200Mbit operation		+/-0.15	
		400Mbit operation		+/-0.10	
Rise time, transmit	10% to 90%	RL = 55ohm, CL = 10pf		2.2	ns
Fall time, transmit	90% to 10%	RL = 55ohm, CL = 10pf		2.2	ns
Setup time, T_{su}, for D_n, CTL_n and LREQ↑↓ relative to SYSCLK↑	50% to 50%	See figure 1	4		ns
Hold time, T_h, for D_n, CTL_n and LREQ↑↓ relative to SYSCLK↑	50% to 50%	See figure 1	1		ns
Delay time T_d for D_n and CTL_n↑↓ relative to SYSCLK↑	50% to 50%	See figure 2	4		ns

Figure 6-1 Dn, CTLn and LREQ Setup Waveforms

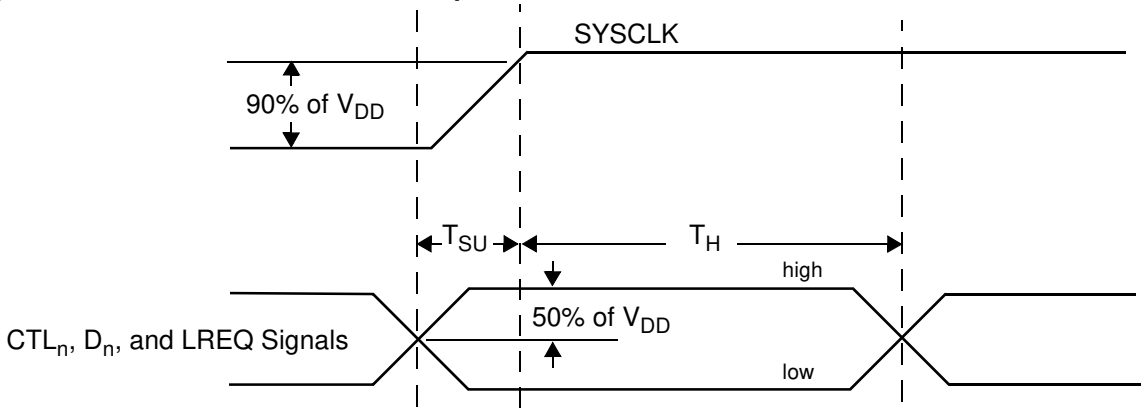
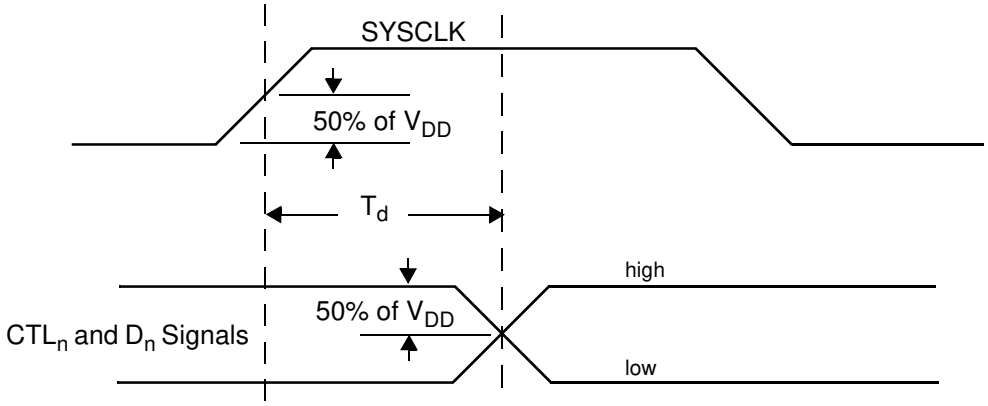


Figure 6-2 CTLn and Dn Hold Timing Waveforms



7.0 Mechanical Package Outlines

Figure 7-1 64-Pin Low Profile Quad Flat Pack (LQFP) -- Units = mm