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MICROCOMPUTER MN101C00

MN101C115/117
LSI User's Manual

Pub. No. 21411-011E

Panasonic

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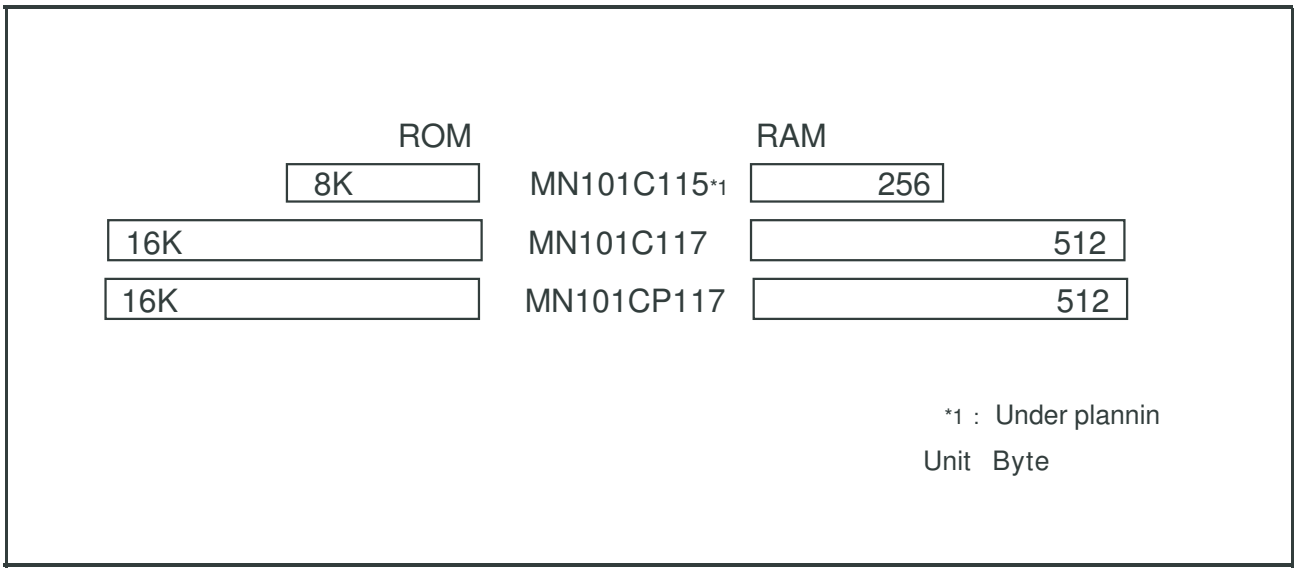
How to Read This Manual

The MN101C11x incorporates more than one ROM/RAM to meet a variety of applications. An EPROM version as well as a Mask ROM version is available so users can write a program by themselves.

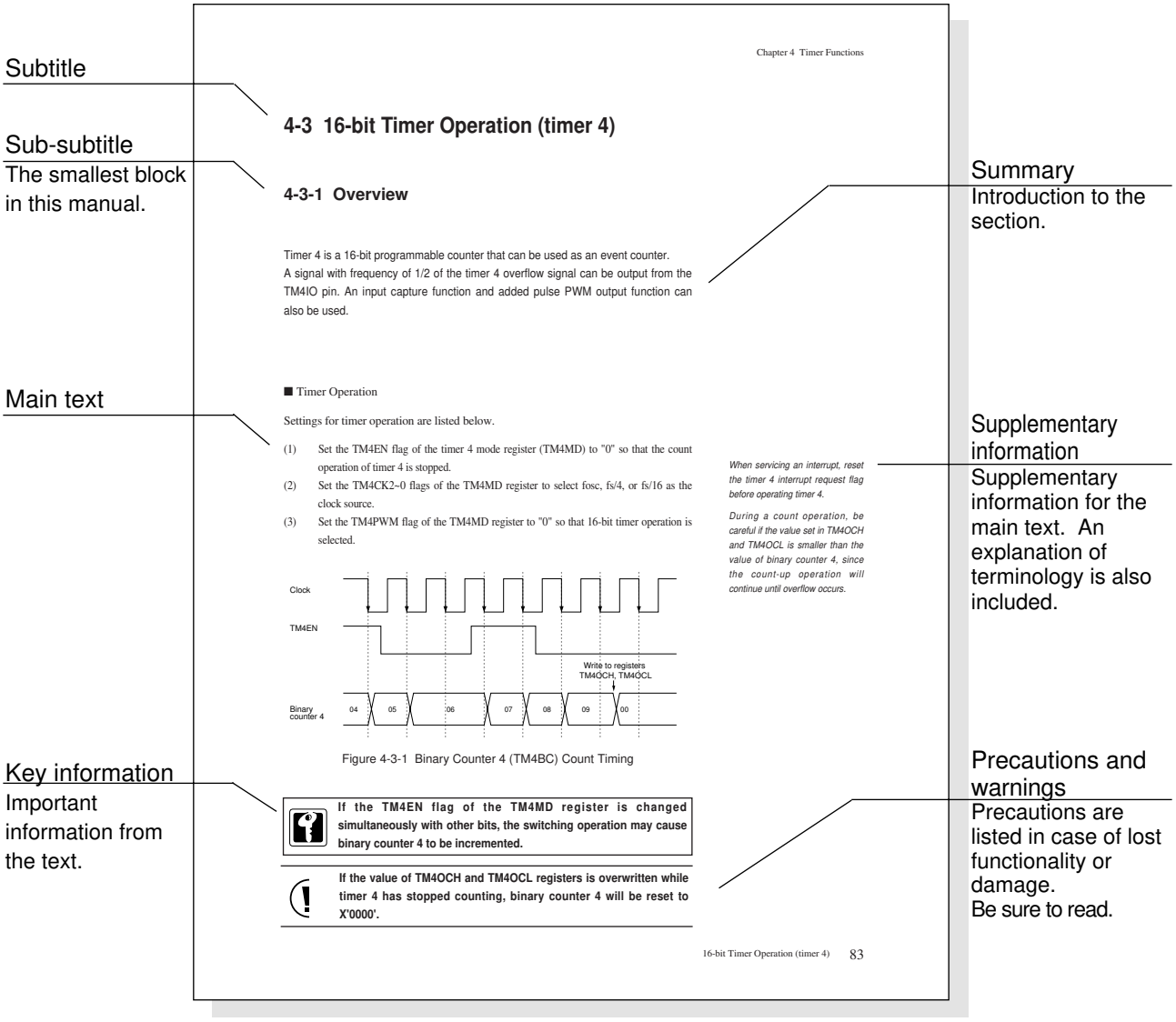


■ Organization

In this LSI manual, the MN101C117 functions are presented in the following order: overview, CPU basic functions, port functions, timer functions, serial functions, and other peripheral hardware functions.

■ Manual Configuration

Each section of this manual consists of a title, summary, main text, supplemental information, precautions and warnings. The layout and definition of each section are shown below.



■ Finding Desired Information

This manual provides four methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.
(2) Consult the table of contents at the front of the manual to locate desired titles.
(3) Consult the list of figures at the front of the manual to locate illustrations and charts by title name.
(4) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■ Related Manuals

The following manuals are also available from Panasonic as part of the MN101C00 series.

MN101C00 Series LSI Manual
<Device Hardware Description>
MN101C00 Series Command Manual
<Command Descriptions>
MN101C00 Series Cross Assembler User's Manual
<Assembler Syntax and Entry Methods>
MN101C00 Series C Compiler User's Manual Operation
<C Compiler Installation, Startup, Option Descriptions>
MN101C00 Series C Compiler User's Manual Language
<C Language Syntax Description>
MN101C00 Series C Compiler User's Manual Library
<C Compiler Standard Library Description>
MN101C00 Series C Source Code Debugger User's Manual
<C Source Code Debugger Usage Methods>
MN101C00 Series PanaX Series Installation Manual
<Installation of C Compiler, Cross Assembler, C Source Code Debugger; In-circuit Emulator>

■ Where to Send Inquires

Please send any inquires or questions concerning the contents of this manual to the Panasonic semiconductor design center closest to you. A list of addresses is provided at the end of this manual for your convenience.

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Chapter 1 Overview

1

1-1 Product Overview

1-1-1 Overview

The MN101C00 series of 8-bit single-chip microcomputers incorporate several types of peripheral functions. This chip series is well suited for VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, remote control, fax machine, musical instrument, and other applications.

The MN101C117 has an internal 16 KB of ROM and 512 bytes of RAM. Peripheral functions include four sets of timers, one set of serial interfaces, an A/D converter, and remote control output. The configuration of this microcomputer is well suited for applications as a system controller in a VCR selection timer, CD player, MD, or portable terminal.

With two oscillation systems (max. 20 MHz/32 kHz) contained on the chip of 48-pin QFP package, the system clock can be switched between high and low speed.

When the oscillation source (fosc) is 8 MHz, a machine cycle lasts for 250 ns. When fosc is 20 MHz, a machine cycle is 100 ns. The package are available with three types of 42-pin SDIP, 44-pin QFP and 48-pin QFH.

1-1-2 Product Summary

This manual describes the following models of the MN101C11 series. These products have identical functions.

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101C115*1	8 KB	256 bytes	Mask ROM version
MN101C117	16 KB	512 bytes	Mask ROM version
MN101CP117	16 KB	512 bytes	EPROM version

*1 Under development

1-2 Hardware Functions

ROM/RAM Size: <Single chip mode>
Internal ROM*2 16,384×8-bit*3
Internal RAM*2 512×8-bit

Machine Cycles: High speed mode 0.10µs/20MHz (4.5V to 5.5V)
0.25µs/8MHz(2.7V to 5.5V)
1.00µs/2MHz(2.0V to 5.5V)
Low speed mode 125µs/32KHz(2.0V to 5.5V)*4

Interrupts: 12 interrupts(11 interrupts except for 48-pin QFH package)
<External interrupts>
The active edge can be selected for all external interrupts
IRQ0 External interrupt (can be connected to noise filter)
IRQ1 External interrupt (can determine zero crossings, can be connected to noise filter)
IRQ2 External interrupt
IRQ3 External interrupt *4
<Timer interrupts>
TM2IRQ Timer 2 (8-bit timer)
TM3IRQ Timer 3 (8-bit timer)
TM4IRQ Timer 4 (16-bit timer)
TM5IRQ Timer 5 (8-bit timer)
TBIRQ Clock timer interrupts
<Serial communication interrupt>
SC0IRQ Serial 0 (synchronous + simple UART
<A/D conversion complete interrupt>
ADIRQ A/D conversion complete
<Watchdog timer interrupt>
NMI Overflow of watchdog timer

Timer/Counters:five timers, all can generate interrupts

Timer 2 8-bit timer

Square wave output, 8-bit PWM output are possible,

Clock source: fs, fs/4, fx*4, TM2IO pin input

Timer 3 8-bit timer

Square wave output, synchronous serial/UART baud rate timer

Clock source: fosc, fs/4, fs/16, TM3IO pin input

Remote control carrier can be generated.

∗2 Differs depending upon the model.
[☞ 1-1-2 "Product Summary"]

**3 Bit 8 of the last address for the built-in ROM of MN101C11X is an optional bit; therefore, this cannot be used as an ordinary ROM.*

**4 Exclusive for a 48-pin QFH product.*

Timers 2 and 3 can be cascaded.

Timer 4 16-bit timer

Square wave output, 16-bit PWM output are possible.
Clock source: fosc, fs/4, fs/16, TM4IO pin input

Input capture function

Time base timer

Clock source: fosc, fs/4, fx*4, fx/2^{13}*4 or fosc/2^{13}

XIOat 32kHz, can be set to measure one minute intervals*4

Can operate independently as timer 5 (8-bit timer).

Watchdog timer

Selected by the mask option as fs/2^{16}, fs/2^{18}, or fs/2^{20}

Remote control carrier output: Based on the timer output, a remote control carrier with duty ratio of 1/2, 1/3 can be output.

Buzzer output: Output frequency can be selected from fs/2^9, fs/2^{10}, fs/2^{11} or fs/2^{12}.

Serial interface: Synchronous/ Simple UART (half-duplex)
Transfer clock: fs/2, fs/4, fs/16, 1/2 of timer 3 output
When using timer 3, the transfer rates for a 12MHz oscillation are 19200/9600/4800/2400/1200/300 bps.
MSB or LSB can be selected as the first bit for transfer. An arbitrary transfer size of 1 to 8 bits can be selected.

A/D converter: 10 bits x 8 channels

LED driver function: 8 pins

Ports: I/O ports 25 ports (8 have dual functions)*5
LED (large current) driver ports:
8 ports (push-pull configuration)
Input ports 11 ports (all have dual functions) *6
Number of pins with dual function for external interrupts: 3*7
(One of which can also be used for zero-cross input.)
Number of pins with dual function for A/D input: 8
Operation mode input pin: 1
Reset input pin: 1

Operation modes: NORMAL mode
SLOW mode*4
HALT mode
STOP mode
and switches operating clock*4

Package: 42-SDIP, 44-QFP, 48-QFH

*5 *26 ports for 44-QFP*
27 ports for 48-QFH

*6 *12 ports for 48-QFH*

*7 *4 ports for 48-QFH*

1-3 Pins

1-3-1 Pin Diagram

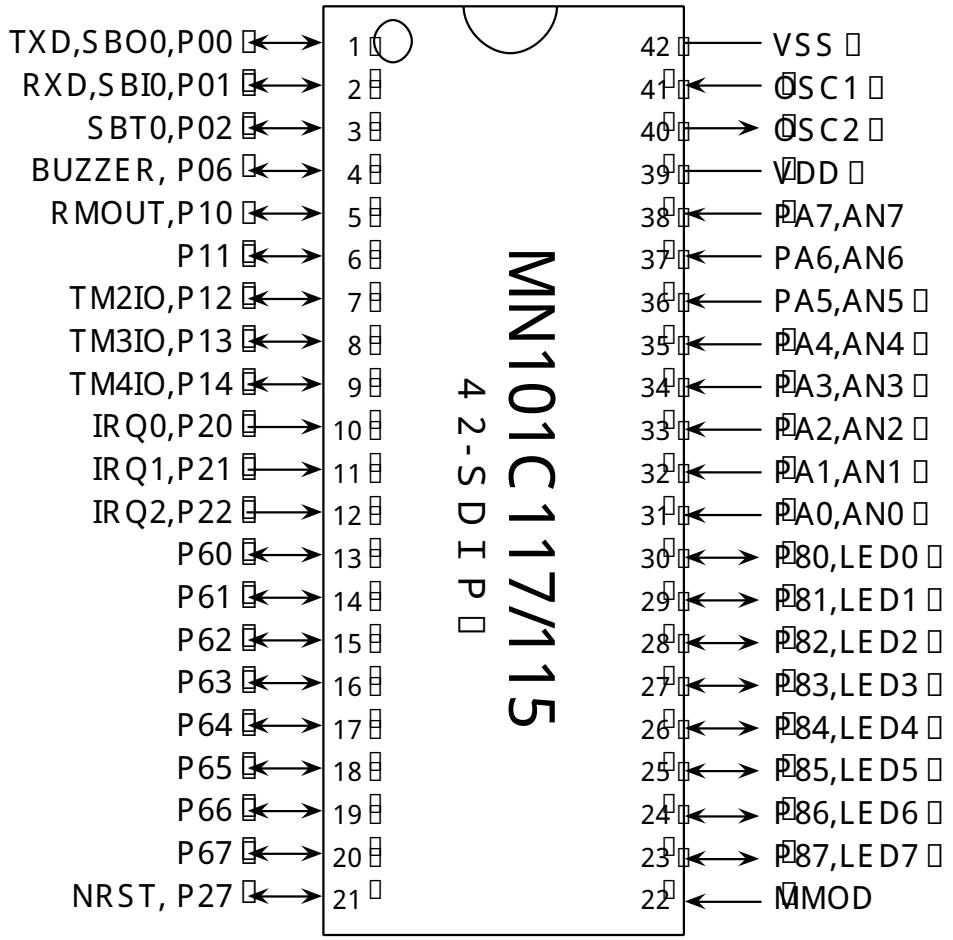


Figure 1-3-1 Pin Diagram (42-SDIP: TOP VIEW)

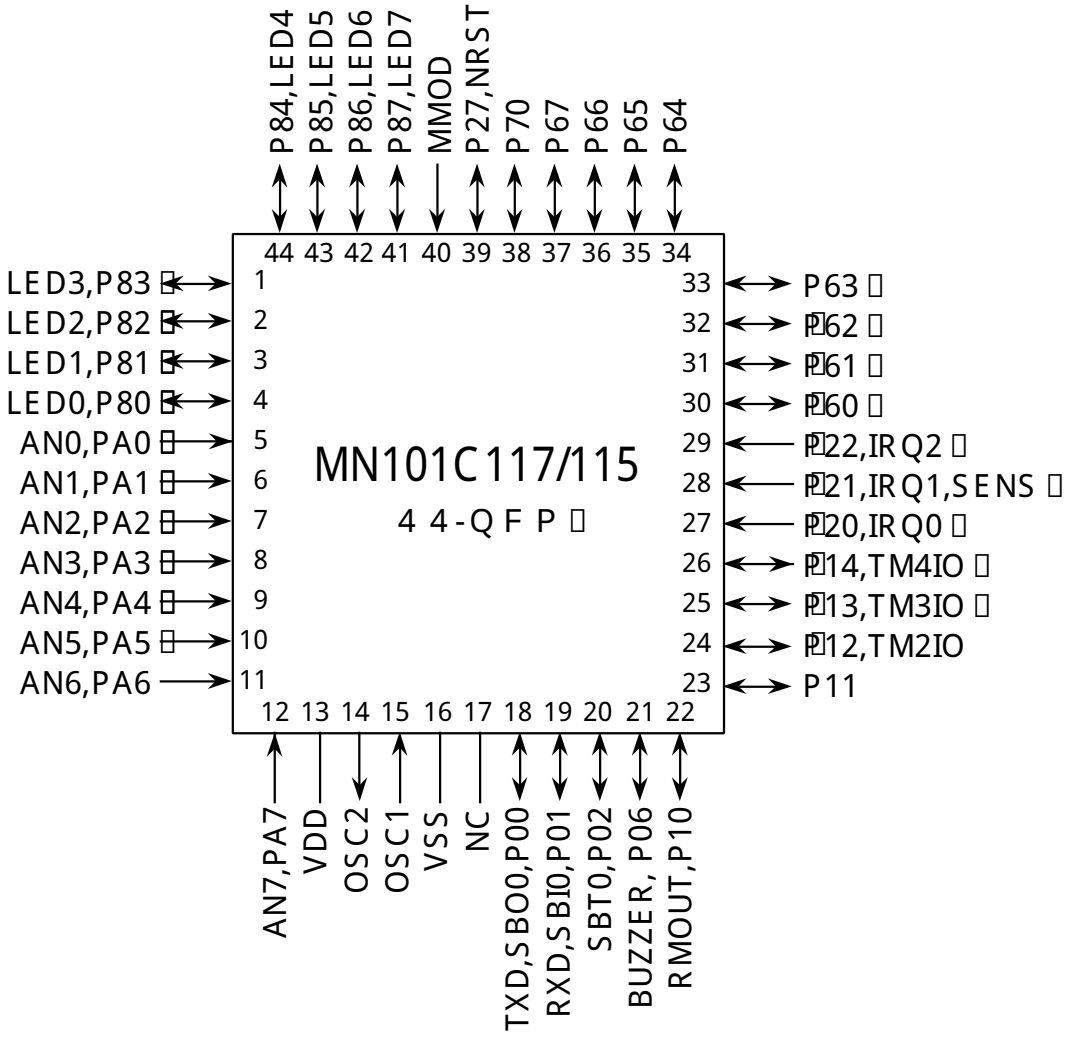


Figure 1-3-2 Pin Diagram (44-QFP: TOP VIEW)

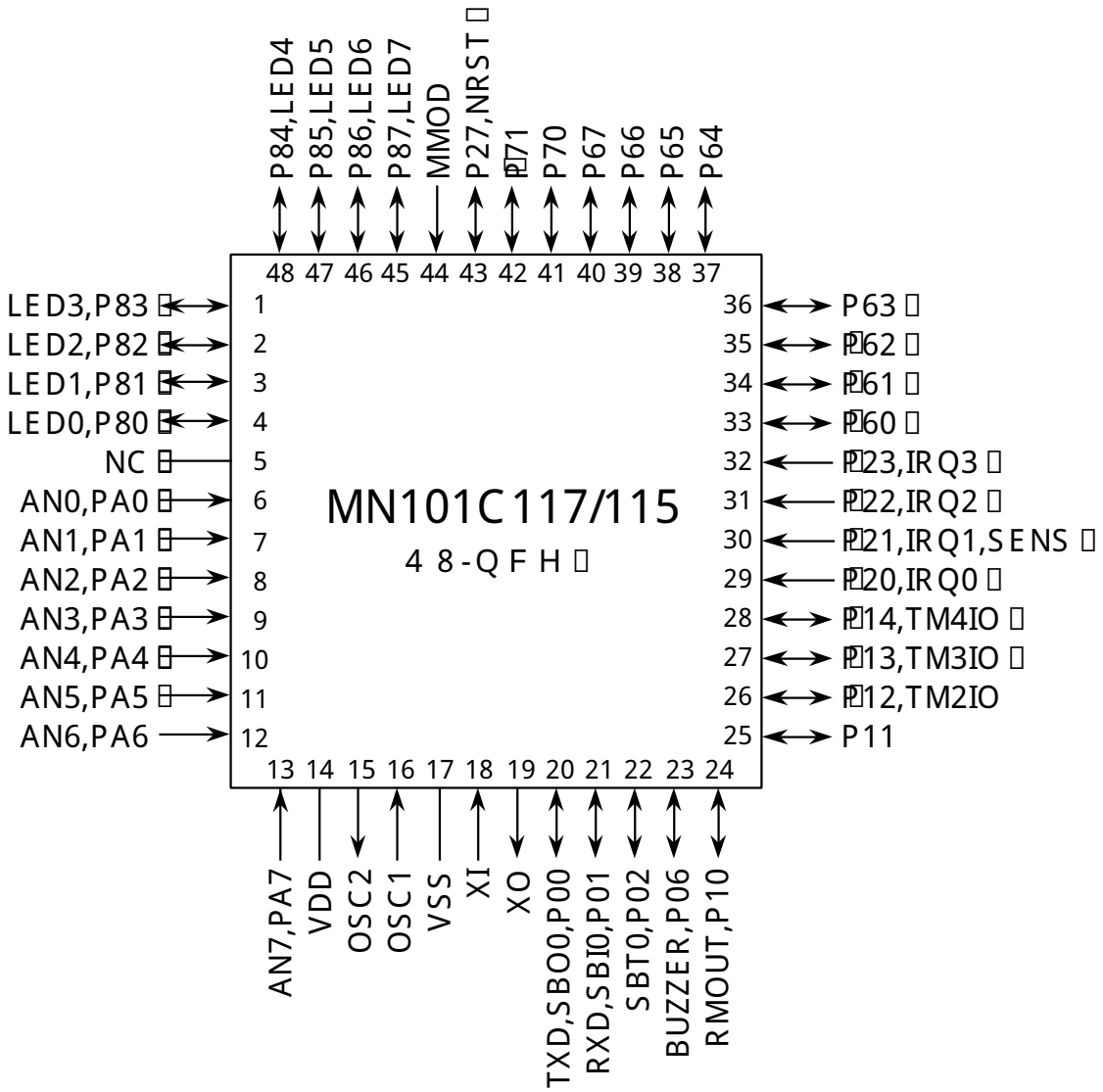


Figure 1-3-3 Pin Diagram (48-QFH: TOP VIEW)

1-3-2 Pin Function Summary

*The pin numbers in the list correspond to the QFH package(Refer to Figure 1-3-3 Pin connection.) Be careful when using SDIP and QFP packages.

Table 1-3-1 Pin Function Summary (1/4)

Pin No.	Name	Type	Dual Function	Function	Description
17 14	VSS VDD	–		Power supply pins	Apply 2.0V to 5.5V to VDD and 0V to VSS.
16 15	OSC1 OSC2	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for high-speed clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
18 19	XI XO	Input Output		Clock input pin Clock output pin	Connect these oscillation pins to ceramic or crystal oscillators for low-speed clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open. *42-SDIP and 44-QFP packages have no pins of this kind.
43	$\overline{RST}$	I/O	P27	Reset pin	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 35 kΩ). Setting this pin low initializes, the internal state of the device is initialized. Thereafter, setting the input to an"H"level release the reset The hardware waits for the system clock to stabilize, and then processes the reset interrupt. Also, if "0" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between RST and VDD, it is recommended that a discharge diode be placed between $\overline{RST}$ and VDD.
20 to 23	P00 to P02	I/O	SBO0(TXD),	I/O port 0	4-bit CMOS tri-state I/O port.
	P06		SBI0(RXD), SBT0, DK (BUZZER)		Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Table 1-3-1 Pin Function Summary (2/4)

Pin No.	Name	Type	Dual Function	Function	Description
24 to 28	P10 to P14	I/O	RMOUT, TM2IO to TM4IO	I/O port 1	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by theP1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
29 to 32	P20 to P23	Input	IRQ0, IRQ1(SENS), IRQ2 to 3	Input port 2	4-bit input port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output). P23 pin does not exist for 42-SDIP, 44-QFP packages.
43	P27	Input	$\overline{\text{RST}}$	Input port 2	Port P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
33 to 40	P60 to P67	I/O		I/O port 6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors for P60 to P67 are disabled (high impedance output).
41 to 42	P70 to P71	I/O		I/O port 7	2-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P7DIR register. A pull-up or pull-down resistor for each bit can be selected individually by the P7PLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output). P70 and P71 pins do not exist for 42-SDIP package. P71 pin does not exist for 44-QFP package, either.
1 to 4 45 to 48	P80 to P87	I/O	LED0 to 7	I/O port 8	8-bit CMOS tri-state I/O port. Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. When configured as outputs, these pins can drive LED segments, directly. At reset, the input mode is selected and pull-up resistors for P80 to P87 are disabled (high impedance output).
6 to 13	PA0 to PA7	Input	AN0 to AN7	Input port A	8-bit input port. A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, the PA0 to PA7 input mode is selected and pull-up resistors are disabled.

Table 1-3-1 Pin Function Summary (3/4)

Pin No.	Name	Type	Dual Function	Function	Description
20 21	TXD RXD	Output Input	SBO0(P00) SBI0(P01)	UART transmit data output pin UART receive data input pin	In the serial interface in UART mode, these pins are configured as the receive data input pin and transmit data output pin. A push-pull or n-channel open-drain configuration can be selected for TXD by the SC0MD1 register. Pull-up resistors can be selected by the P0PLU register. The TXD and RXD pins are also allocated as P00 and P01 respectively. When not used as serial/UART pins, these can be used as normal I/O pins.
20	SBO0	Output	TXD(P00)	Serial interface transmit data output pin	Transmit data output pin for serial interfaces 0. The output configuration, either CMOS push-pull or n-channel open-drain, and pull-up resistors can be selected by the software. Set these pins to the output mode by the P0DIR register. SBO0 is allocated as P00. This may be used as normal I/O pin when the serial interface is not used.
21	SBI0	Input	RXD(P01)	Serial interface receive data input pin	Receive data input pin for serial interfaces 0. Pull-up resistor can be selected by the P0PLU register. Set these pins to the input mode by the P0DIR register. SBI0 is allocated as P01. This can be used as normal I/O pin when the serial interface is not used.
22	SBT0	I/O	P02	Serial interface clock I/O pin	Clock I/O pin for serial interface 0. The output configuration, either CMOS push-pull or n-channel open-drain output, can be selected by the software. The direction of SBT0 is selected by the P0DIR register in accordance with the communication mode. Pull-up resistors can be selected by the P0PLU register. SBT0 is allocated as P02. This can be used as normal I/O pin when the serial interface is not used.
22	Buzzer	I/O	P06	Buzzer output	Piezoelectric buzzer driver pin. The driving frequency can be selected in the range of fs/2 to fs/2 by the DLYCTR register. Select output mode by the P0DIR register and select buzzer output by the DLYCTR register. When not used for buzzer output, this pin can be used as a normal I/O pin.
24	RMOUT	I/O	P10	Remote control transmit signal output pin	Output pin for remote control transmit signal with a carrier signal. Can be used as a normal I/O pin when remote control is not used.
26 to 28	TM2IO to TM4IO	I/O	P12 to P14	Timer I/O pins	Event counter clock input pins, overflow pulse output pins and PWM signal output pins for timer 2 to 4. To use these pins as event clock inputs, configure them as inputs by the P1DIR register. For overflow pulse and PWM output, configure these pins as outputs by the P1DIR register. When the pins are used as inputs, pull-up resistors can be specified by the P1PLU register. When not used for timer I/O, these can be used as normal I/O pins.

Table 1-3-1 Pin Function Summary (4/4)

Pin No.	Name	Type	Dual Function	Function	Description
44	MMOD	Input		Test mode switch input pin	This pin sets the test mode. Must be set to L.
29 to 32	IRQ0 to IRQ3	Input	P20, P21(SENS), P22,P23	External interrupt input pins	The valid edge for these external interrupt input pins can be selected with the IRQnICR registers. IRQ1 is an external interrupt pin that is able to determine AC zero crossings. It can also be used as a normal external interrupt. When IRQ0 to 3 are not used for interrupts, these can be used as normal I/O pins.
6 to 13	AN0 to AN7	Input	PA0 to PA7	Analog input pins	Analog input pins for an 8-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal I/O pins.
30	SENS	Input	IRQ1(P21)	AC zero-cross detection input pin	SENS is an input pin for an AC zero-cross detection circuit. The AC zero-cross circuit outputs a high level when the input is at an intermediate level. It outputs a low level at all other times. SENS is connected to the P21 input circuit and the IRQ1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input. The P21IM flag of the FLOAT1 register sets which input is selected.

1-4 Overview of Functions

1-4-1 Block Diagram

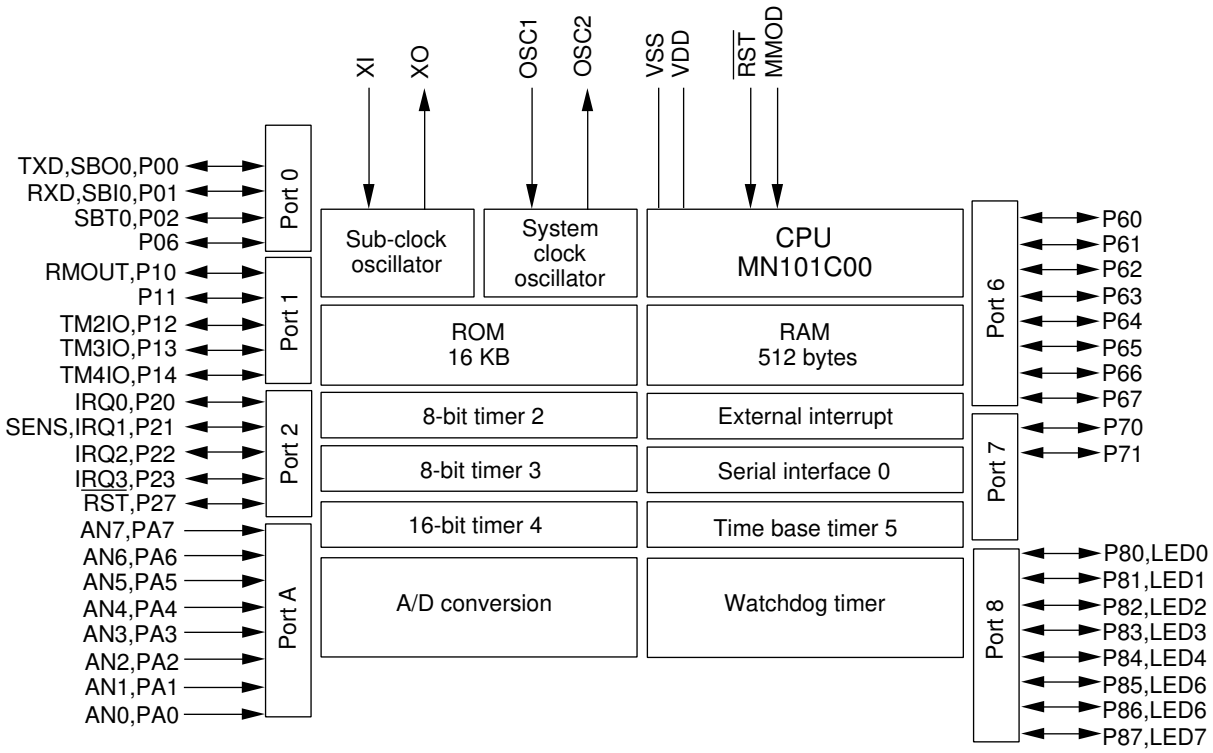


Figure 1-4-1 Block Diagram of Functions)

1-5 Electrical Characteristics

Contents \ Model	MN101C117/115
Classification	CMOS integrated circuit
Use	General purpose
Function	CMOS, 8-bit, single-chip microcomputer

This LSI manual describes standard specifications. Before using the LSI, please obtain product specifications from the sales office.

1-5-1 Absolute Maximum Ratings *2 *3

	Parameter		Symbol	Rating	Unit
1	Supply voltage		V_{DD}	–0.3 to +7.0	V
2	Input clamp current (SENS)		IC	–500 to 500	µA
3	Input pin voltage		V_I	–0.3 to V_{DD}+0.3	V
4	Output pin voltage		V_O	–0.3 to V_{DD}+0.3	V
5	I/O pin voltage		V_{IO1}	–0.3 to V_{DD}+0.3	V
6	Peak output current	P8	I_{OL1} (peak)	30	mA
7		Except P8	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	–10	
9	Average output current*1	P8	I_{OL1} (avg)	20	
10		Other than P8	I_{OL2} (avg)	15	
11		All pins	I_{OH} (avg)	–5	
12	Tolerable loss		PD	400	mW
13	Ambient operating temperature		T_{opr}	–40 to 85	°C
14	Storage temperature		T_{stg}	–55 to +125	°C

Note: *1 Applicable even for an interval of 100ms.
*2 Insert at least one bypass capacitor of 0.1µF or more between a power source pin and GND to prevent from latchup.
*3 Absolute maximum ratings indicate the allowable limit to which applied voltage does not damage a chip, not guarantee the operation.

1-5-2 Operating Conditions

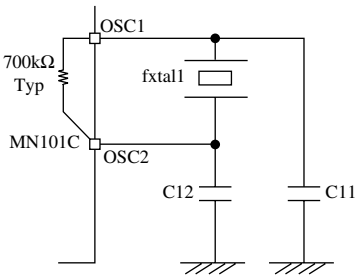
Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Supply voltage							
1	Supply voltage during operation	V_{DD1}	fosc ≤ 20.0MHz	4.5		5.5	V
2		V_{DD2}	fosc ≤ 8.39MHz	2.7		5.5	
3		V_{DD3}	fosc ≤ 2.00MHz	2.0		5.5	
4		V_{DD4} *1	fx = 32.768kHz	2.0		5.5	
5	Voltage to maintain RAM data	V_{DD5}	STOP mode	1.8		5.5	
Operating speed *2							
6	Instruction execution time	tc1	V_{DD}=4.5 to 5.5V	0.100			µs
7		tc2	V_{DD}=2.7 to 5.5V	0.238			
8		tc3	V_{DD}=2.0 to 5.5V	1.00			
9		tc4 *1	V_{DD}=2.0 to 5.5V	40		125	
Crystal oscillator 1 Fig. 1-5-1							
10	Crystal frequency	fxtal 1	V_{DD}=4.5 to 5.5V	1.0		20.0	MHz
11	External capacitors	C_{11}			20		pF
12		C_{12}			20		
13	Internal feedback resistor	RF10			700		kΩ
Crystal oscillator 2 Fig. 1-5-2*1							
14	Crystal frequency	fxtal 2			32.768		kHz
15	External capacitors	C_{21}			20		pF
16		C_{22}			20		
17	Internal feedback resistor	RF20			4.0		MΩ

Note: *1. Only for 48-QFH package

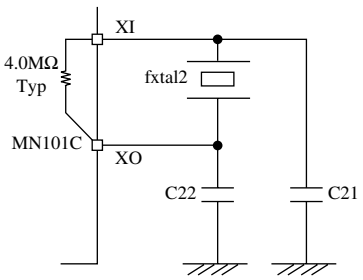
*2 t_{c1}, t_{c2}, t_{c3}: OSC1 is the CPU clock

t_{c4}: XI is the CPU clock



The instruction cycle is twice the clock cycle.
The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The instruction cycle is four times the clock cycle.
The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2 *1

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
18	Clock frequency	f_{OSC}		1.0		20.0	MHz
19	High level pulse width*	twh 1	*1 Fig. 1-5-3	20.0		30.0	ns
20	Low level pulse width*	twl 1		20.0		30.0	
21	Rise time	twr 1	Fig. 1-5-3			5.0	ns
22	Fall time	twf 1				5.0	
External clock input 2 XI (XO is unconnected)*2							
23	Clock frequency	fx		32.768		100	kHz
24	High level pulse width*	twh 2	*1 Fig. 1-5-4	3.5			µs
25	Low level pulse width*	twl 2		3.5			
26	Rise time	twr 2	Fig. 1-5-4			20	ns
27	Fall time	twf 2				20	

*1 Set the clock duty ratio to 45 to 55%.
*2 Applicable only for 48-pin QFH package

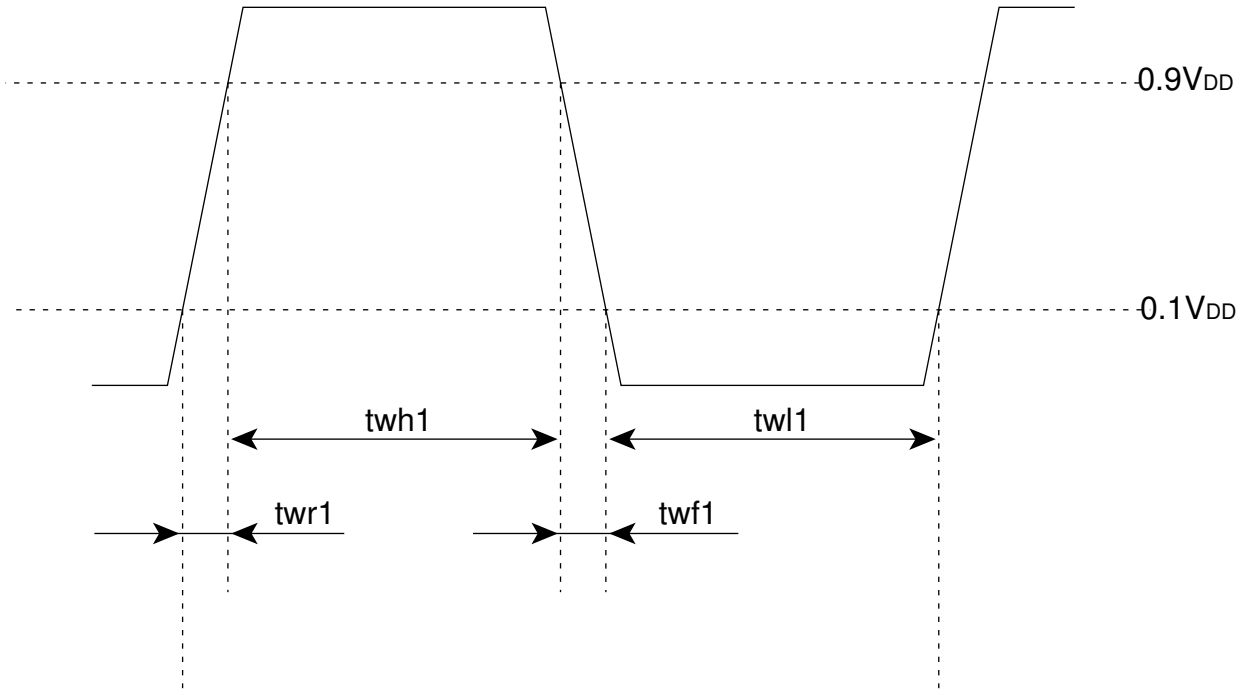


Figure 1-5-3 OSC1 Timing Chart

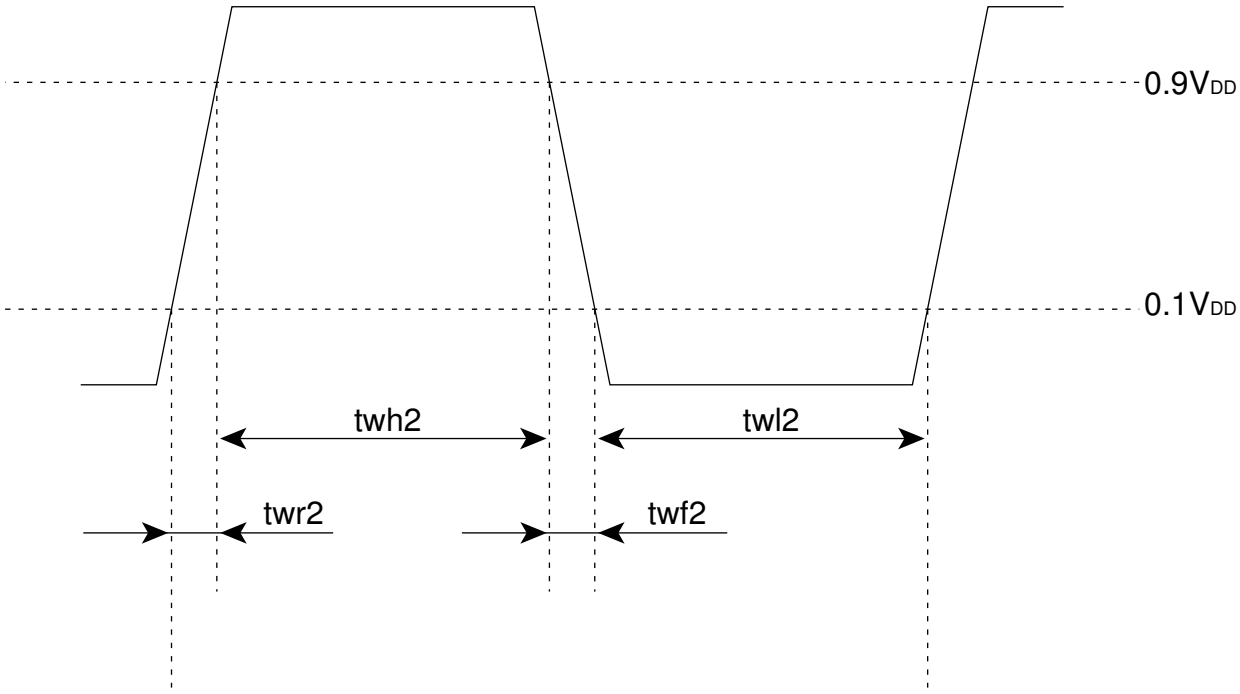


Figure 1-5-4 XI Timing Chart

1-5-3 DC Characteristics

Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Supply current (no load at output)*1							
1	Supply current during operation	I_{DD1}	fosc=20.0MHz,V_{DD}=5V		25	60	mA
2		I_{DD2}	fosc=8.39MHz,V_{DD}=5V		10	25	
3		I_{DD3} *2	fx =32.768kHz,V_{DD}=3V			100	µA
4	Supply current during HALT mode	I_{DD5} *2	fx =32.768kHz,V_{DD}=3V Ta=25℃			8	
5		I_{DD6} *2	Ta=-40 to 85°C			18	
6	Supply current during STOP mode	I_{DD7}	V_{DD}=5V, Ta=25°C		0	2	
7		I_{DD8}	V_{DD}=5V, Ta=-40 to 85°C		0	20	

Notes: *1 Measured under conditions of Ta=25°C and no load.

The supply current during operation, I_{DD1} (I_{DD2}), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is fixed at V_{SS}, the input pins are fixed at V_{DD}, and a 20MHz (8.39MHz) square wave of amplitude V_{DD},V_{SS} is input to the OSC1 pin.

The supply current during operation, I_{DD3}, is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is fixed at V_{SS}, the input pins are fixed at V_{DD}, and a 32.768kHz square wave of amplitude V_{DD},V_{SS} is input to the XI pin.

The supply current during HALT mode, I_{DD5}(I_{DD6}), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is fixed at V_{SS}, the input pins are fixed at V_{DD}, and an 32.768kHz square wave of amplitude V_{DD},V_{SS} is input to the XI pin.

The supply current during STOP mode I_{DD7}(I_{DD8}) is measured under the following conditions: After the oscillation mode is set to <STOP mode>, the MMOD pin is fixed at V_{SS}, the input pins are fixed at V_{DD}, and the OSC1 and XI pins are unconnected.

*2 The items I_{DD5}(I_{DD6}) and I_{DD7}(I_{DD8}) are applicable only for 48-pin QFH package.

Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD							
8	Input high voltage 1	V_{IH1}		0.8V_{DD}		V_{DD}	V
9	Input high voltage 2	V_{IH2}	V_{DD}=4.5 to 5.5V	0.7V_{DD}		V_{DD}	V
10	Input low voltage 1	V_{IL1}		0		0.2V_{DD}	V
11	Input low voltage 2	V_{IL2}	V_{DD}=4.5 to 5.5V	0		0.3V_{DD}	V
12	Input leakage current	I_{LK1}	VIN = 0 to V_{DD}			±10	µA
Input pin 2 P20, P22~P23 (Schmitt trigger input)							
13	Input high voltage	V_{IH3}		0.8V_{DD}		V_{DD}	V
14	Input low voltage	V_{IL3}		0		0.2V_{DD}	V
15	Input leakage current	I_{LK3}	VIN=0 to V_{DD}			±10	µA
16	Input high current	I_{IH3}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
Input pin 3—1 P21 (Schmitt trigger input)							
17	Input high voltage	V_{IH4}		0.8V_{DD}		V_{DD}	V
18	Input low voltage	V_{IL4}		0		0.2V_{DD}	V
19	Input leakage current	I_{LK4}	VIN=0 to V_{DD}			±10	µA
20	Input high current	I_{IH4}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
Input pin 3—2 P21 (when used as SENS)							
21	Input high voltage 1	V_{DHH}	V_{DD}=5.0V Fig. 1-5-5	4.5		V_{DD}	V
22	Input low voltage 1	V_{DLH}		V_{SS}		3.5	
23	Input high voltage 2	V_{DHL}		1.5		V_{DD}	V
24	Input low voltage 2	V_{DLL}		V_{SS}		0.5	
25	Input leakage current	I_{LK10}	VIN=0V to V_{DD}			±10	µA
26	Input clamp current	I_{C10}	V_{DD}=5.0V VIN>V_{DD}, VIN<0V			±400	

SENS pin

27	Rise time	trs	Fig. 1-5-5	30			µs
28	Fall time	tfs		30			

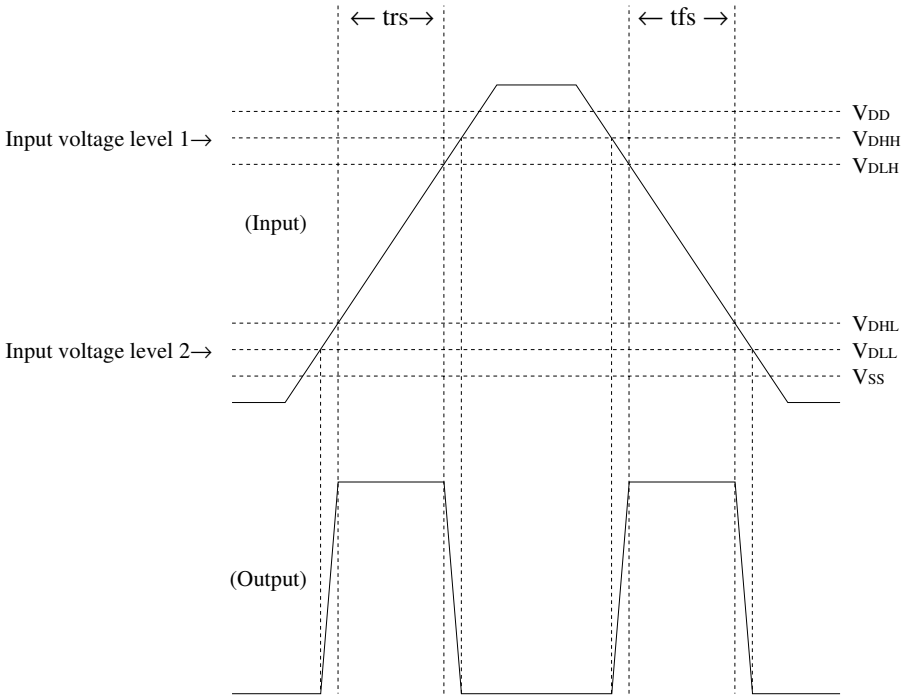


Figure 1-5-5 Operation of AC Zero-Cross Detection Circuit

Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 4 PA0~PA7							
29	Input high voltage 1	V_{IH5}		0.8V_{DD}		V_{DD}	V
30	Input high voltage 2	V_{IH6}	V_{DD}=4.5 to 5.5V	0.7V_{DD}		V_{DD}	V
31	Input low voltage 1	V_{IL5}		0		0.2V_{DD}	V
32	Input low voltage 2	V_{IL6}	V_{DD}=4.5 to 5.5V	0		0.3V_{DD}	V
33	Input leakage current	I_{LK5}	VIN=0 to V_{DD}			±2	µA
34	Input high current	I_{IH5}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
35	Input low current	I_{IL5}	V_{DD}=5V, V_{IN}=3.5V Pull-down resistor ON	80	180	400	µA

Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 5 P27 ($\overline{RST}$)							
36	Input high voltage	V_{IH7}		$0.9V_{DD}$		V_{DD}	V
37	Input low voltage	V_{IL7}		0		$0.2V_{DD}$	V
38	Input leakage current	I_{LK7}	VIN = 0 to V_{DD}			±10	µA
39	Input high current	Iih	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor built in	-30	-100	-300	µA
I/O pin 6 P00 to P06, P10 to P14 (Schmitt trigger input)							
40	Input high voltage	V_{IH8}		$0.8V_{DD}$		V_{DD}	V
41	Input low voltage	V_{IL8}		0		$0.2V_{DD}$	V
42	Input leakage current	I_{LK8}	VIN=0 to V_{DD}			±10	µA
43	Input high current	I_{IH8}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
44	Output high voltage	V_{OH8}	V_{DD} = 5V, I_{OH} = –0.5mA	4.5			V
45	Output low voltage	V_{OL8}	V_{DD} = 5V, I_{OL} = 1.0mA			0.5	V
I/O pin 7 , P60 to P67							
46	Input high voltage 1	V_{IH9}		$0.8V_{DD}$		V_{DD}	V
47	Input high voltage 2	V_{IH10}	V_{DD}=4.5 to 5.5V	$0.7V_{DD}$		V_{DD}	V
48	Input low voltage 1	V_{IL9}		0		$0.2V_{DD}$	V
49	Input low voltage 2	V_{IL10}	V_{DD}=4.5 to 5.5V	0		$0.3V_{DD}$	V
50	Input leakage current	I_{LK9}	VIN=0 to V_{DD}			±10	µA
51	Input high current	I_{IH9}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
52	Output high voltage	V_{OH9}	V_{DD} = 5V, I_{OH} = -0.5mA	4.5			V
53	Output low voltage	V_{OL9}	V_{DD} = 5V, I_{OL} = 1.0mA			0.5	V
I/O pin 8 P70 to P71							
54	Input high voltage 1	V_{IH11}		$0.8V_{DD}$		V_{DD}	V
55	Input high voltage 2	V_{IH12}	V_{DD}=4.5 to 5.5V	$0.7V_{DD}$		V_{DD}	V
56	Input low voltage 1	V_{IL11}		0		$0.2V_{DD}$	V
57	Input low voltage 2	V_{IL12}	V_{DD}=4.5 to 5.5V	0		$0.3V_{DD}$	V
58	Input leakage current	I_{LK11}	VIN = 0 to V_{DD}			±10	µA
59	Input high current	I_{IH11}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
60	Input low current	I_{IL11}	V_{DD}=5V, V_{IN}=3.5V Pull-down resistor ON	30	100	300	µA
61	Output high voltage	V_{OH11}	V_{DD} = 5V, I_{OH} = –0.5mA	4.5			V
62	Output low voltage	V_{OL11}	V_{DD} = 5V, I_{OL} = 1.0mA			0.5	V

Ta=–40 to +85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 9 P80~P87							
63	Input high voltage 1	V_{IH13}		$0.8V_{DD}$		V_{DD}	V
64	Input high voltage 2	V_{IH14}	V_{DD}=4.5 to 5.5V	$0.7V_{DD}$		V_{DD}	V
65	Input low voltage 1	V_{IL113}		0		$0.2V_{DD}$	V
66	Input low voltage 2	V_{IL14}	V_{DD}=4.5 to 5.5V	0		$0.3V_{DD}$	V
67	Input leakage current	I_{LK13}	VIN=0 to V_{DD}			±10	µA
68	Input high current	I_{IH13}	V_{DD}=5V, V_{IN}=1.5V Pull-up resistor ON	–30	–100	–300	µA
69	Output high voltage	V_{OH13}	V_{DD} = 5V, I_{OH} = –0.5mA	4.5			V
70	Output low voltage	V_{OL13}	V_{DD} = 5V, I_{OL} = 15mA			1.0	V

1-5-4 A/D Converter Characteristics

Ta=–40 to+85°C V_{DD}=2.0 to 5.5V V_{SS}=0V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Nonlinear error 1		V_{DD} = 5.0V, V_{SS} = 0V V_{REF+}=5.0V, $V_{REF–}$=0V T_{AD} = 800ns			±3	LSB
3	Differential linear error 1					±3	LSB
4	Nonlinear error 2		V_{DD} = 5.0V, V_{SS} = 0V $V_{REF–}$=5.0V, $V_{REF–}$=0V fx = 32.768kHz			±5	LSB
5	Differential linear error 2					±5	LSB
6	Zero traction voltage		V_{DD} = 5.0V, V_{SS} = 0V V_{REF+}=5.0V, $V_{REF–}$=0V T_{AD} = 800ns		30	100	mV
7	Full-scale transition voltage				30	100	mV
8	A/D conversion time		T_{AD} = 800ns	9.6			µs
9			fx = 32.768kHz			183	µs
10	Sampling time		f_{OSC} = 8MHz	1.0		36	µs
11			fx = 32.768kHz		30.5		µs
12	Analog input leakage current		When V_{DAIN} = 0 to 5V is off			±2	µA

1-6 Option

1-6-1 ROM Option

The product equipped with this LSI or an EPROM with this LSI controls the oscillation mode after resetting as well as the runaway-detection watchdog timer, using bits 2 to 0 of the last address of the built-in ROM.

■ Option bits

7	6	5	4	3	2	1	0
-	-	-	PKG SEL2	PKG SEL1	WDSEL2	WDSEL1	NSSTRT

NSSTRT	Selection of oscillation mode after resetting
0	SLOW mode
1	NORMAL mode

WDSEL2	WDSEL1	Watchdog timer cycle setting
0	0	$fs/2^{16}$
	1	$fs/2^{18}$
1	X	$fs/2^{20}$

PKGSEL2	PKGSEL1	Packages
0	X	SDIP042-P-0600
1	0	QFP044-P-1010
	1	QFH048-P-0707

Figure 1-6 ROM Option (Address:X'7FFF')

1-6-2 Option Form

Date:

SE No.

Model Name	MN101C

Customer		Approval	

1. Oscillation mode

Type A	Type B

Note: Type A: Operation begins from the reset cycle in the NORMAL mode.
Type B: Operation begins from the reset cycle in the SLOW mode.

2. Watchdog timer period setting

Detection Period	Selection
$fs/2^{16}$	
$fs/2^{18}$	
$fs/2^{20}$	
Not used	

3. Package selection

Package	Selection
SDIP042-P-0600 □	
QFP044-P-1010 □	□
QFH048-P-0707	

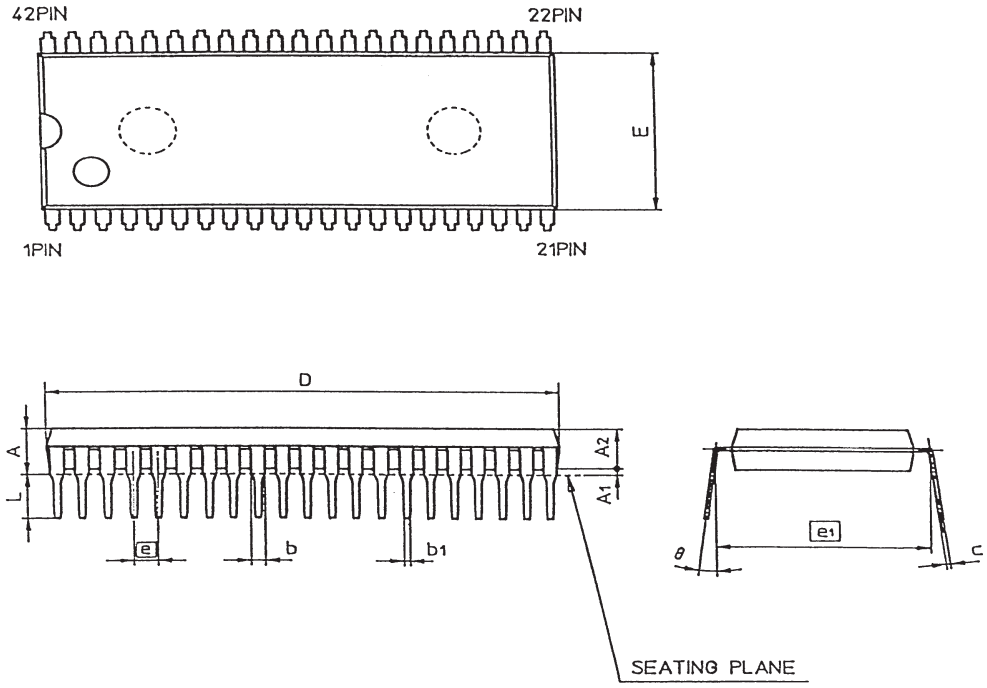
Contents of mask option are subject to change.
When placing an order for masks, please request the most recent option list from the sales office.

Option of this product is used a part of the built-in ROM.
When placing an order for programme, please sed data on the address of the option.

1-7 Outline Drawings

Package code: SDIP042-P-0600

Unit: mm



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	4.0	4.3	4.6
A1	—	1.0	—
A2	3.1	3.3	3.5
b	0.9	1.0	1.1
b1	0.4	0.5	0.6
b2	—	—	—
c	0.25	0.25	0.45
D	36.7	37.0	37.3
E	12.8	13.0	13.2
e	—	1.778	—
e1	—	15.24	—
L	3.0	3.3	3.6
θ	0		15

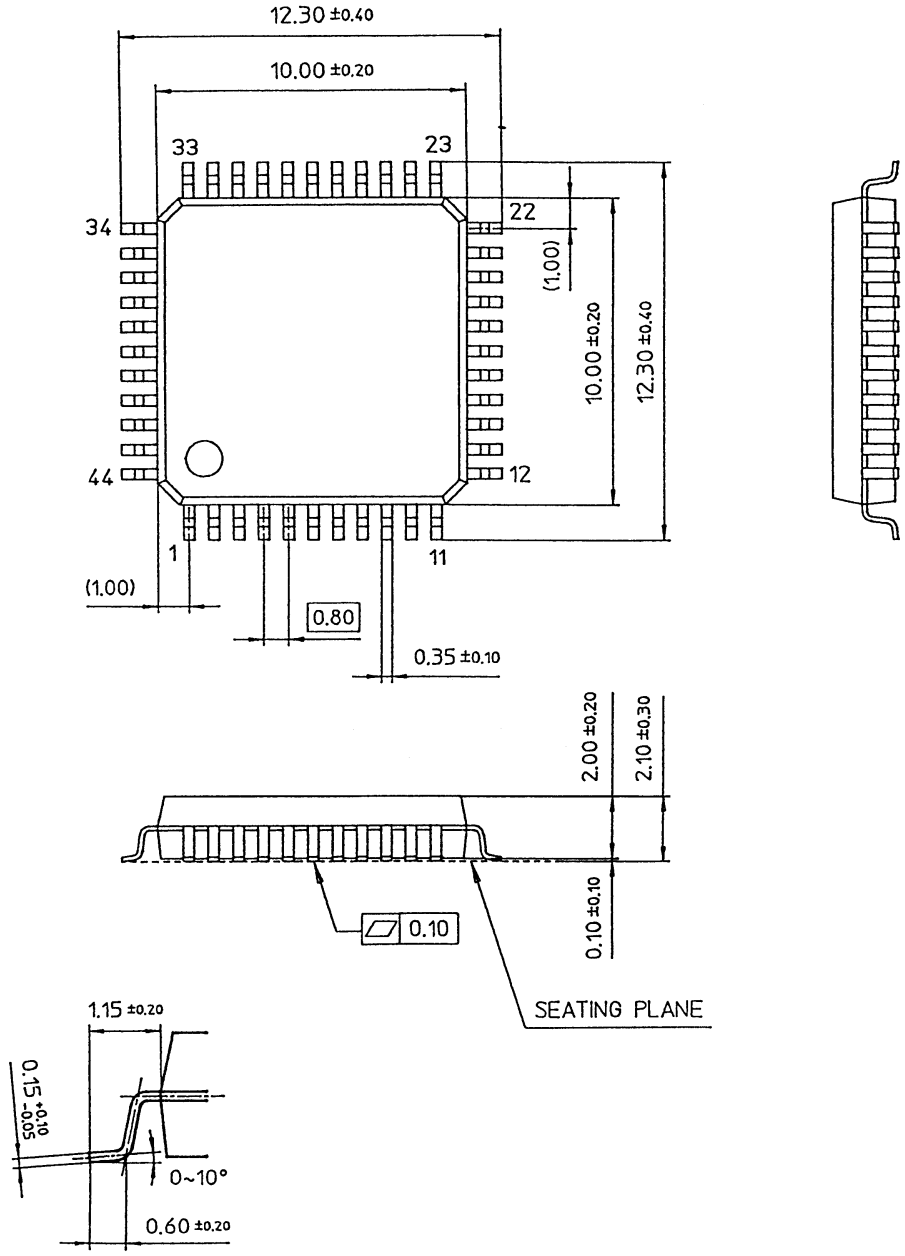
Body Material: Epoxy Resin Lead Material:Fe Ni Lead Finish Method:Soldering dip

Figure 1-7-1 42-SDIP

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.

Package code: QFP044-P-1010

Unit: mm



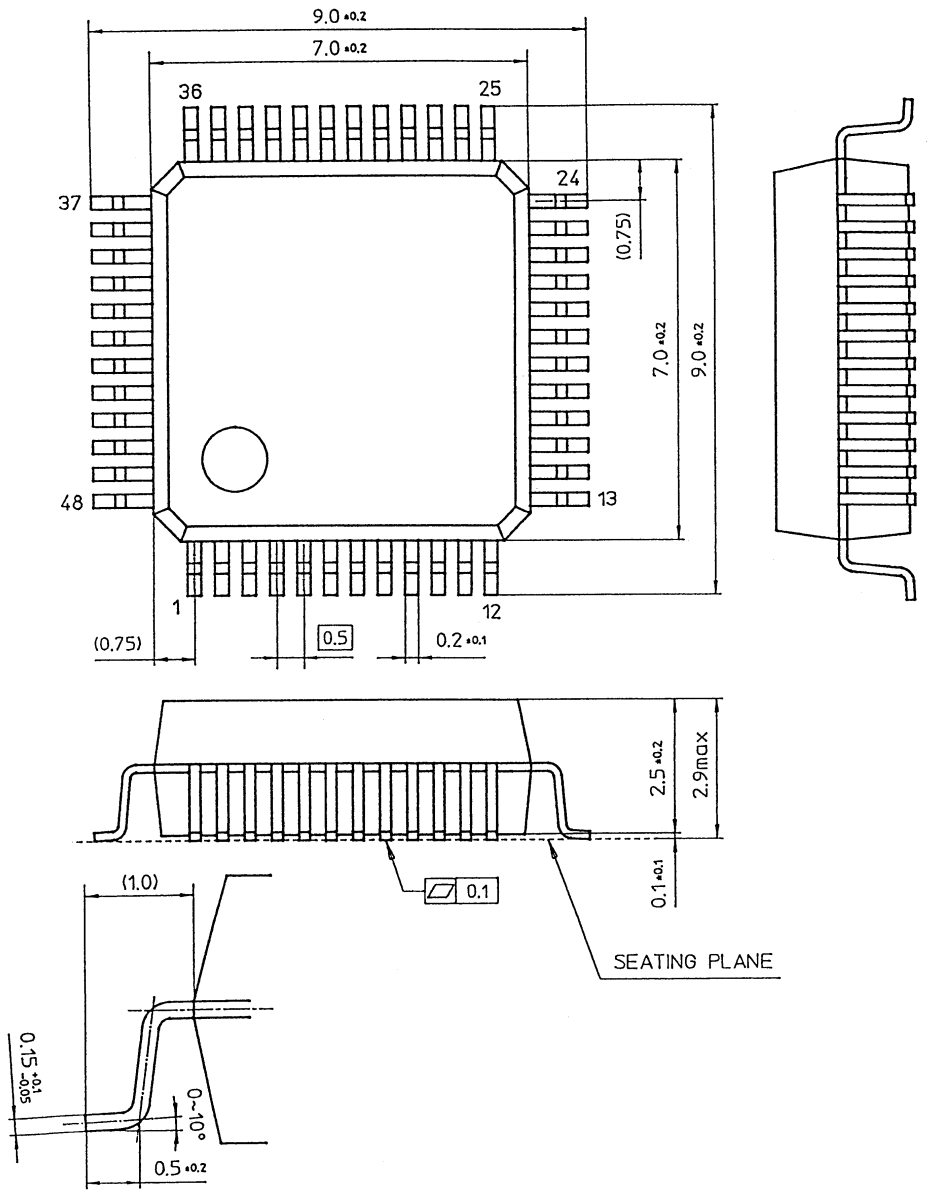
Body Material: Epoxy Resin Lead Material:Fe Ni Lead Finish Method:Soldering dip

Figure 1-7-2 44-QFP

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.

Package code: QFH048-P-0707

Unit: mm



Material: Epoxy Resin Lead Material:Fe Ni-42 Alloy
Lead Finish Method:Soldering dip

Figure 1-7-3 48-QFH

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales office.

Chapter 2 Basic CPU Functions

2

2-1 Overview

Basic CPU functions are in conformance with the MN101C00 series manual (architecture manual). This chapter describes specifications unique to the MN101C117/115.

2-2 Address Space

2-2-1 Memory Configuration

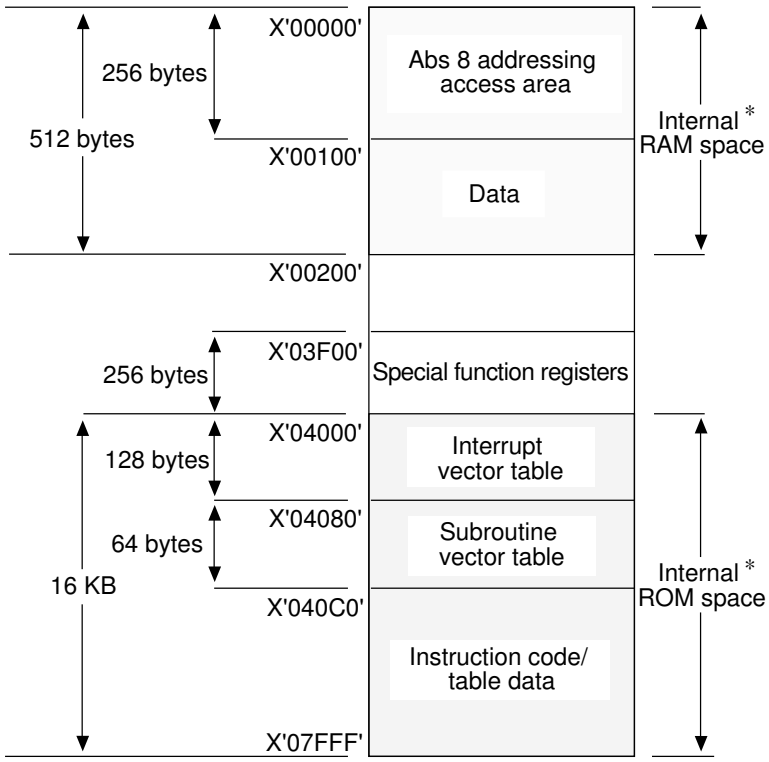


Figure 2-2-1 Memory Map

∗ Differs depending upon the model.

MN101C115	Internal RAM	X'00000' to X'000FF'	256 bytes
	Internal ROM	X'04000' to X'05FFF'	8 KB
MN101CP117	Internal RAM	X'00000' to X'001FF'	512 bytes
	EP ROM	X'04000' to X'01FFF'	16 KB

2-2-2 Special Function Registers

Memory control register(MEMCTR) is a 4-bit register which set up the base

Table 2-2-1 Register Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
03F0X	CPUM	MEMCTR	WDCTR	DLYCTR													CPU mode, memory control	
03F1X	P0OUT	P1OUT	P2OUT				P6OUT	P7OUT	P8OUT								Port output	I/O ports
03F2X	P0IN	P1IN	P2IN				P6IN	P7IN	P8IN		PAIN						Port input	
03F3X	P0DIR	P1DIR					P6DIR	P7DIR	P8DIR	P1OMD	PAIMD						I/O mode control	
03F4X	P0PLU	P1PLU	P2PLU				P6PLU	P7PLUD	P8PLU		PAPLUD	FLOAT1					Resistor control	
03F5X	SC0MD0	SC0MD1	SC0MD2	SC0MD3	SC0CTR	SC0TRB	SC0RXB										Serial interface control	
03F6X			TM2BC	TM3BC	TM4BCL	TM4BCH	TM4ICL	TM4ICH	TM5BC								Timer control	
03F7X			TM2OC	TM3OC	TM4OCL	TM4OCH			TM5OC									
03F8X			TM2MD	TM3MD	TM4MD				TM5MD	RMCTR	NFCTR							
03F9X	ANCTR0	ANCTR1	ANBUF0	ANBUF1													A/D control	
03FAX																	Reserved	
03FBX																		
03FCX																		
03FDX																		
03FEX		NMICR	IRQ0ICR	IRQ1ICR			TM2ICR	TBICR	SC0ICR		ADICR	IRQ2ICR			TM3ICR	TM4ICR	Interrupt control	
03FFX	TM5ICR																	

2-3 Bus Interface

2-3-1 Overview

The MN101C117, unlike other MN101C series microcomputers, does not support memory expansion mode and processor mode.

2-3-2 Control Registers

The memory control register is a four-bit register that sets up wait-count at a time of access to a base address of interrupt vector table and a special register zone.

(1) Memory control register(MEMCTR)

	7	6	5	4	3	2	1	0	
MEMCTR	IOW1	IOW0	IVBA	—	—	IRWE	—	—	(at reset: 11001011)

Must be set to 11.

IRWE	Set software write for interrupt request flag
0	Software write disable Even if data is written to each interrupt control register (xxxICR), the state of the interrupt request flag (xxxIR) will not change.
1	Software write enable

Must be set to 1.

Must be set to 0

IVBA	Base address setting for interrupt vector table
0	Interrupt vector base = X'04000'
1	Interrupt vector base = X'00100'

IOW1 to 0	Number of wait cycles set when accessing special register area	Bus cycle at 20MHz oscillation
00	No wait cycles	100ns
01	1 wait cycle	150ns
10	2 wait cycles	200ns
11	3 wait cycles	250ns

Figure 2-3-1 Memory Control Register MEMCTR:X'03F01'R/W

2-4 Interrupts

2-4-1 Accepting and Returning from Interrupts

In the MN101C00 series, when an interrupt is accepted, the hardware pushes the program's return address and the PSW, on to the stack, and branches to the beginning address of the interrupt program specified by the interrupt vector table.

■ Operation when Interrupt is Accepted

1. The stack pointer (SP) contents are update. (SP–6 → SP)
2. The handy address register (HA) is pushed on to the stack.
   HA upper byte → (SP+5)
   HA lower byte → (SP+4)
3. The program counter (PC = return address) contents are pushed on to the stack.
   PC (bit 18 to bit 17, bit 0) → (SP+3)
   PC (bit 16 to bit 9) → (SP+2)
   PC (bit 8 to bit 1) → (SP+1)
4. The PSW is pushed on to the stack.
   PSW → (SP)
5. xxxLVn of the accepted interrupt is copied to IM of the PSW.
   Interrupt level → IM
6. Execution branches to vector table.

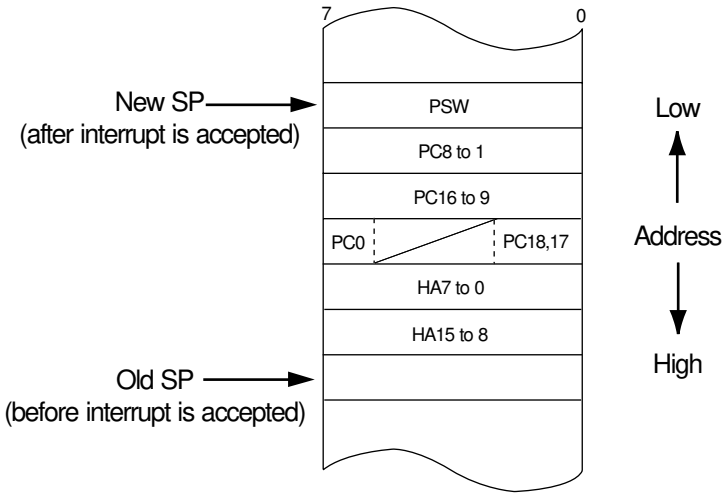


Figure 2-4-1 Stack Status during an Interrupt

Since the contents of data and address registers are not saved, use PUSH instructions in the program to save these values as necessary on the stack.

■ Operation when Returning from Interrupt

After the program POPs the register and other values saved by the interrupt service routine, an RTI instruction is implemented to return to the program that was being executed when the interrupt was received.

The processing sequence for the return from interrupt instruction, RTI, is listed below.

1. The processor status word (PSW) is pulled from the stack. (SP)
2. The program counter(PC = return address) is pulled from the stack. (SP+1 to 3)
3. The handy address register (HA) is pulled from the stack. (SP+4, 5)
4. The SP is pulled. (SP+6 → SP)
5. Execution branches to the address indicated by the PC.

2-4-2 Interrupt Sources and Vector Addresses

In addition to reset, there are 20 interrupt vectors that indicate the starting addresses of interrupt programs. These vectors are located in the 80-byte ROM address area X'04004' to X'04053'.

Table 2-4-1 Interrupt Control Registers

Vector Number	Interrupt Source	Control Register (address)	Vector Address
0	Reset	————	X'04000'
1	Non-maskable interrupt (NMI)	NMICR (X'03FE1')	X'04004'
2	External interrupt 0 (IRQ0)	IRQ0ICR (X'03FE2')	X'04008'
3	External interrupt 1 (IRQ1)	IRQ1ICR (X'03FE3')	X'0400C'
4	Reserved	(X'03FE4')	X'04010'
5	Reserved	(X'03FE5')	X'04014'
6	Timer 2 compare-match (TM2IRQ)	TM2ICR (X'03FE6')	X'04018'
7	Time base period (TBIRQ)	TBICR (X'03FE7')	X'0401C'
8	SC0 transfer complete (SC0IRQ)	SC0ICR (X'03FE8')	X'04020'
9	Reserved	(X'03FE9')	X'04024'
10	A/D conversion complete (ADIRQ)	ADICR (X'03FEA')	X'04028'
11	External interrupt 2 (IRQ2)	IRQ2ICR (X'03FEB')	X'0402C'
12	External interrupt 3 (IRQ3)*	IRQ3ICR (X'03FEC')	X'04030'
13	Reserved	(X'03FED')	X'04034'
14	Timer 3 compare-match (TM3IRQ)	TM3ICR (X'03FEE')	X'04038'
15	Timer 4 compare-match (TM4IRQ)	TM4ICR (X'03FEF')	X'0403C'
16	Timer 5 compare-match (TM5IRQ)	TM5ICR (X'03FF0')	X'04040'
17	Reserved	(X'03FF1')	X'04044'
18	Reserved	(X'03FF2')	X'04048'
19	Reserved	(X'03FF3')	X'0404C'
20	Reserved	(X'03FF4')	X'04050'

**IRQ31CR cannot be used except for 48-pin QFH package.*

Set the vector addresses for reserved and unused interrupts to an address containing an RTI instruction.

2-4-3 Interrupt Control Registers

Be sure to use the MIE flag of the PSW register to write to all interrupt control registers.

Interrupt control registers consist of the following: a non-maskable interrupt control register (NMICR), external interrupt control registers (IRQnICR), and internal interrupt control registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR).

■ Non-maskable Interrupt Control Register (NMICR)

Non-maskable interrupt factors are stored in the non-maskable interrupt control register (NMICR), and are used when a non-maskable interrupt is generated.

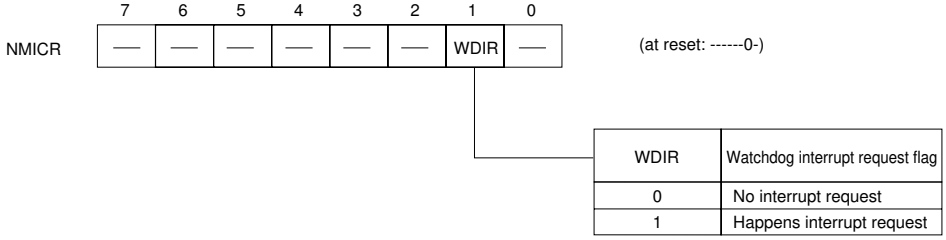


Figure 2-4-2 Non-maskable Interrupt Control Register (NMICR: X'03FE1', R/W)

■ External Interrupt Control Registers (IRQnICR)

The external interrupt control registers (IRQnICR) control the interrupt level, valid edge, and request/enable.

By setting xxxLVn to '11' (level 3), the corresponding interrupt vector will be disabled, regardless of the state of the interrupt enable and interrupt request flags.

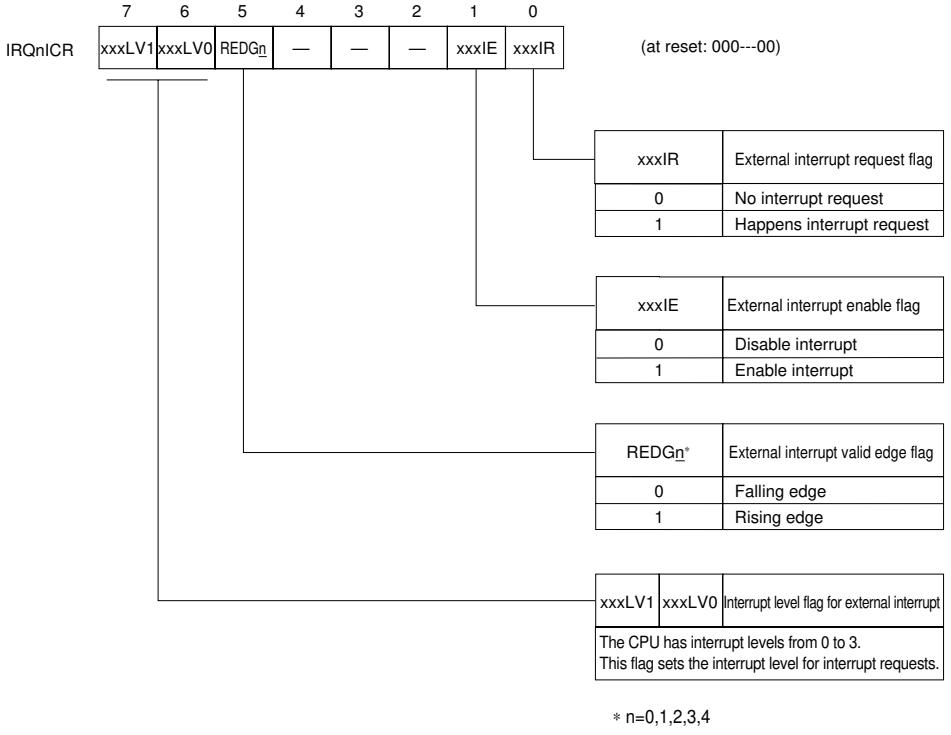


Figure 2-4-3 External Interrupt Control Register
(IRQnICR: X'03FE2' to X'03FE3', X'03FEB' to X'03FED', R/W)

■ Internal Interrupt Control Registers (TMnICR, TBICR, SCOICR, ATCICR, ADICR)

The internal interrupt control registers (TMnICR, TBICR, SCnICR, ATCICR, ADICR) control the interrupt levels of internal interrupts, timer interrupts, serial interrupts, A/D conversion complete interrupts, and interrupt request/enable. Be sure to disable all interrupts before writing to these registors.

By setting xxxLVn to '11' (level 3), the corresponding interrupt vector will be disabled, regardless of the state of the interrupt enable and interrupt request flags.

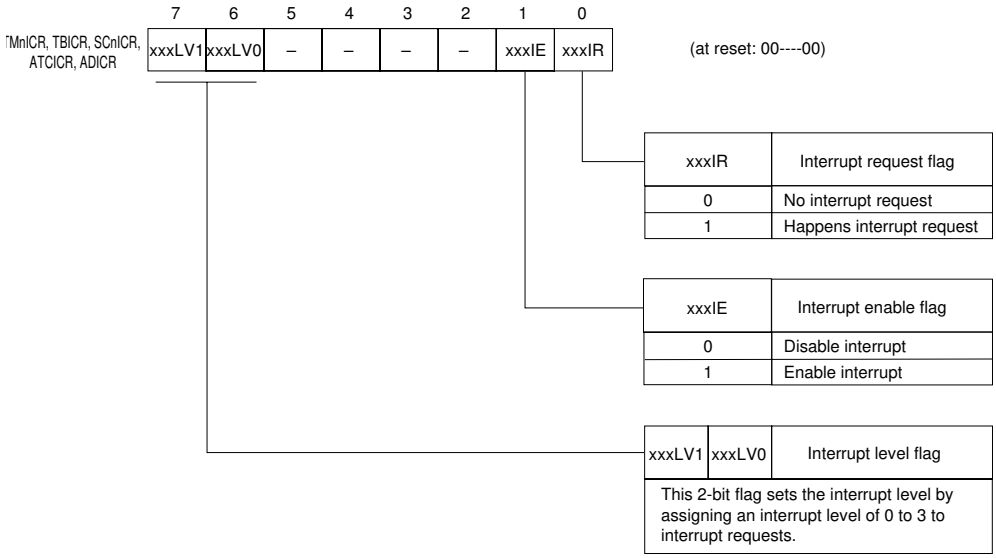


Figure 2-4-4 Internal Interrupt Control Registers (TMnICR, TBICR, SC0ICR,ADICR: X'03FE6' to X'03FEA', X'03FEA' to X'03FF0', R/W)

2-5 Reset

The CPU contents are reset and registers are initialized when the $\overline{RST}$ pin is pulled to low.

■ Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the $\overline{RST}$ pin low for at least four clock cycles.

For the reset to be stable, the low pulse must be maintained for at least four clock cycles. However, it is important to minimize noise, since a reset may occur in a smaller number of clock cycles.

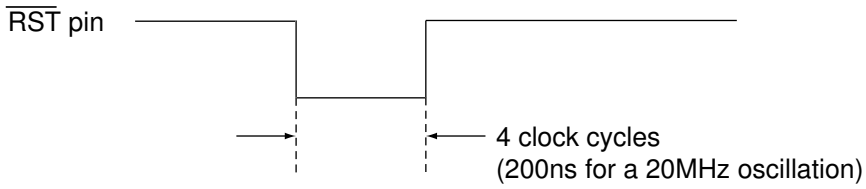


Figure 2-5-1 Minimum Reset Pulse Width

(2) Set bit 7 (P2OUT7 flags) of the P2OUT register to "0." After reset is released, the P2OUT flag will be "1."

■ Releasing the Reset

When the $\overline{RST}$ pin changes from low to high, an internal 15-bit counter begins counting at the oscillation clock frequency. The interval from when this counter begins counting until it overflows is known as the stabilization wait time. After waiting for this amount of time, the internal reset is released and the CPU begins operation.

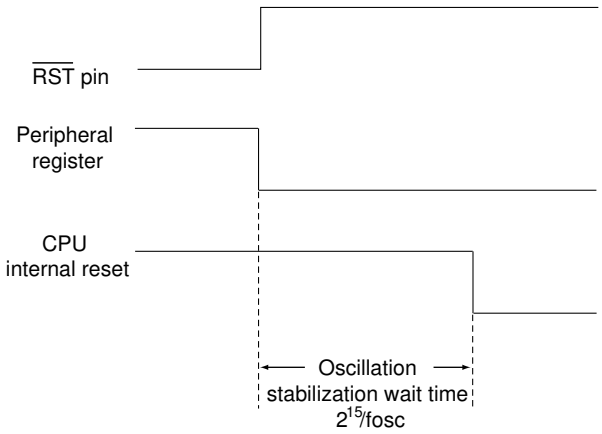


Figure 2-5-2 Reset Release Sequence

When returning from the STOP mode is terminating, the software can use the DLYCTR register to select an oscillation stabilization wait time of 0, 2^7/fosc, 2^{11}/fosc, or 2^{15}/fosc.

Chapter 3 Port Functions

3

3-1 Overview

A total of 39 pins on the MN101C117, including those shared with special function pins, are allocated for the 7 ports of P0 to P2, P6 to P8, and PA.
Each I/O port is assigned according to the special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.

For each I/O port, the PnOUT register (port n output register) that sets the output value is assigned to memory address X'3F1n', and the PnIN register (port n input register) from which the input value is monitored is assigned to memory address X'3F2n'.

• This I/O control is valid even when special functions are selected for the dual function pins.

•Table 3-1-1 Status When Port Is Reset (single-chip mode)

Port	I/O Mode	Pull-up/Pull-down Resistor	I/O Port or Special Function
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up/pull-down resistors	I/O port
Port 8	Input mode	No pull-up/pull-down resistors	I/O port
Port A	Input mode	No pull-up/pull-down resistors	I/O port

■ Port 0 (P0)

4-bit CMOS tri-state I/O port.

Table 3-1-2 Port 0 Functions

Pin Name	Type	Dual Function	Description
P00 to P02 P06	I/O	SBO0(TXD), SBI0(RXD), SBT0 BUZZER	Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

■ Port 1 (P1)

5-bit CMOS tri-state I/O port.

Table 3-1-3 Port 1 Functions

Pin Name	Type	Dual Function	Description
P10 to P14	I/O	RMOUT, TM2IO to TM4IO	Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

■ Port 2 (P2)

4-bit CMOS tri-state input port.

Table 3-1-4 Port 2 Functions

Pin Name	Type	Dual Function	Description
P20 to P23	Input	IRQ0, IRQ1(SENS), IRQ2 to 3	A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode pull-up resisters are disabled (high impedance output). Only 48-QFH has P23.

■ Port 6 (P6)

8-bit CMOS tri-state I/O port.

Table 3-1-5 Port 6 Functions

Pin Name	Type	Dual Function	Description
P60 to P67	I/O		Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode pull-up resisters are disabled (high impedance output).

■ Port 7 (P7)

8-bit CMOS tri-state I/O port.

Table 3-1-6 Port 7 Functions

Pin Name	Type	Dual Function	Description
P70 to P71	I/O		Each individual bit can be switched to an input or output by the P7DIR register. A pull-up or pull-down resistor for each bit can be selected individually by the P7PLU register. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode pull-up resisters are disabled . 42-SDIP has no pins of P70,P71. 44-QFP has no pin of p71.

■ Port 8 (P8)

8-bit CMOS tri-state I/O port.

Table 3-1-7 Port 8 Functions

Pin Name	Type	Dual Function	Description
P80 to P87	I/O	LED0 to 7	Each individual bit can be switched to an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. When configured as outputs, it is possible to LED. At reset, when single chip mode is selected, the input mode pull-up resisters for P80 to P87 are disabled (high impedance output).

■ Port A (PA)

8-bit CMOS tri-state input port.

Table 3-1-8 Port A Functions

Pin Name	Type	Dual Function	Description
PA0 to PA7	Input	AN0 to AN7	A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD register. However, pull-up and pull-down resistors cannot be mixed. At reset, the input mode pull-up resisters for PA0 to PA7 are disabled.

3-2 Port Control Registers

3-2-1 Overview

28 registers control the I/O ports. See table 3-2-1.

Table 3-2-1 I/O Port Control Registers (1/2)

Name	Address	R/W	Function
P0OUT	X'03F10'	R/W	Port 0 output register
P1OUT	X'03F11'	R/W	Port 1 output register
P2OUT	X'03F12'	R/W	Port 2 output register
P6OUT	X'03F16'	R/W	Port 6 output register
P7OUT	X'03F17'	R/W	Port 7 output register
P8OUT	X'03F18'	R/W	Port 8 output register
P0IN	X'03F20'	R	Port 0 input register
P1IN	X'03F21'	R	Port 1 input register
P2IN	X'03F22'	R	Port 2 input register
P6IN	X'03F26'	R	Port 6 input register
P7IN	X'03F27'	R	Port 7 input register
P8IN	X'03F28'	R	Port 8 input register
PAIN	X'03F2A'	R	Port A input register
P0DIR	X'03F30'	R/W	Port 0 direction control register
P1DIR	X'03F31'	R/W	Port 1 direction control register

Table 3-2-1 I/O Port Control Registers (2/2)

Name	Address	R/W	Function
P6DIR	X'03F36'	R/W	Port 6 direction control register
P7DIR	X'03F37'	R/W	Port 7 direction control register
P8DIR	X'03F38'	R/W	Port 8 direction control register
P1OMD	X'03F39'	R/W	Port 1 output mode register
PAIMD	X'03F3A'	R/W	Port A input mode register
P0PLU	X'03F40'	R/W	Port 0 pull-up control register
P1PLU	X'03F41'	R/W	Port 1 pull-up control register
P2PLU	X'03F42'	R/W	Port 2 pull-up control register
P6PLU	X'03F46'	R/W	Port 6 pull-up control register
P7PLUD	X'03F47'	R/W	Port 7 pull-up/pull-down control register
P8PLU	X'03F48'	R/W	Port 8 pull-up control register
PAPLUD	X'03F4A'	R/W	Port A pull-up/pull-down control register
FLOAT1	X'03F4B'	R/W	Pin control register 1

	7	6	5	4	3	2	1	0	
P0OUT	—	P0OUT6	—	—	—	P0OUT2	P0OUT1	P0OUT0	(at reset: -0---000)
P1OUT	—	—	—	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	(at reset: ---00000)
P2OUT	P2OUT7	—	—	—	—	—	—	—	(at reset: 1-------)
P0IN	—	P0IN6	—	—	—	P0IN2	P0IN1	P0IN0	(at reset: -X---XXX)
P1IN	—	—	—	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	(at reset: ---XXXXX)
P2IN	—	—	—	—	—	P2IN2	P2IN1	P2IN0	(at reset: ----XXX)
P0DIR	—	P0DIR6	—	—	—	P0DIR2	P0DIR1	P0DIR0	(at reset: -0---000)
P1DIR	—	—	—	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	(at reset: ---00000)
P1OMD	—	—	—	P14TCO	P13TCO	P12TCO	—	P10TCO	(at reset: ---00000)
P0PLU	—	P0PLU6	—	—	—	P0PLU2	P0PLU1	P0PLU0	(at reset: -0---000)
P1PLU	—	—	—	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	(at reset: ---00000)
P2PLU	—	—	—	—	—	P2PLU2	P2PLU1	P2PLU0	(at reset: -----000)
P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	(at reset: 00000000)
P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	(at reset: XXXXXXXX)
P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	(at reset: 00000000)
P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	(at reset: 00000000)

Figure 3-2-1 Port Control Registers (1/2)

	7	6	5	4	3	2	1	0	
P7OUT		—	—	—	—	—	P7OUT1	P7OUT0	(at reset: - - - - - - 00)
P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	(at reset: 00000000)
P7IN	—	—	—	—	—	—	P7IN1	P7IN0	(at reset: - - - - - - XX)
P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	(at reset: XXXXXXXX)
PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	(at reset: XXXXXXXX)
P7DIR	—	—	—	—	—	—	P7DIR1	P7DIR0	(at reset: - - - - - - 00)
P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	(at reset: 00000000)
PAIMD	PAAIN7	PAAIN6	PAAIN5	PAAIN4	PAAIN3	PAAIN2	PAAIN1	PAAIN0	(at reset: 00000000)
P7PLUD							P7PLUD1	P7PLUD0	(at reset: - - - - - - 00)
P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	(at reset: 00000000)
PAPLUD	PAPLUD7	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	(at reset: 00000000)

Figure 3-2-1 Port Control Registers (2/2)

3-2-2 I/O Port Control Registers

This section describes the special function registers that control the MN101C117's I/O ports.

■ Data Registers

• PnOUT registers

Data registers to output to the ports.

Data written to these registers is output from the ports.

0	Low (Vss level) is output.
1	High (Vdd level) is output.

• PnIN registers

Data registers to input data from the ports.

The value of data at the pins can be input by reading these registers.

These are read-only registers.

0	Pin is low.
1	Pin is high.

Input and output registers are mapped to separate addresses.

To use these ports for I/O, configure them as I/O ports in the PnOMD/PnIMD registers, described in this section.

■ Direction Control Registers

• PnDIR registers

0	Input mode
1	Output mode

These registers set the port for use as an input or output.

■ Pull-up/Pull-down Resistor Control Registers

• PnPLU registers

These register settings determine whether internal pull-up resistors are added to the ports.

0	No pull-up / pull-down resistor
1	Pull-up / Pull down resistor

• PnPLUD registers

These register settings determine whether internal pull-up or pull-down resistors are added to the ports.

0	No pull-up / pull-down resistor
1	Pull-up / Pull down resistor

Setting the PAIMD register prevents unnecessary current from flowing in a pin when an intermediate voltage (analog voltage) is applied to the pin.

■ Port Output/Input Mode Registers

• PnOMD/PnIMD registers

These register settings determine whether the port pins(P10 to P14, PA0 to PA5) are used as I/O ports or as special function pins (dual function).

If the special (dual) functions used, the PnDIR, PnPLU, PnPLUD, and other registers must be set.

0	I/O port
1	Special function pin

■ Pin Control Registers

• FLOAT1 registers

This register specifies whether the resistors-attached to pins P7 and PA are pull-up resistors or pull-down resistors.

In addition, this register selects either zero cross input or Schmitt trigger input for pin P21.

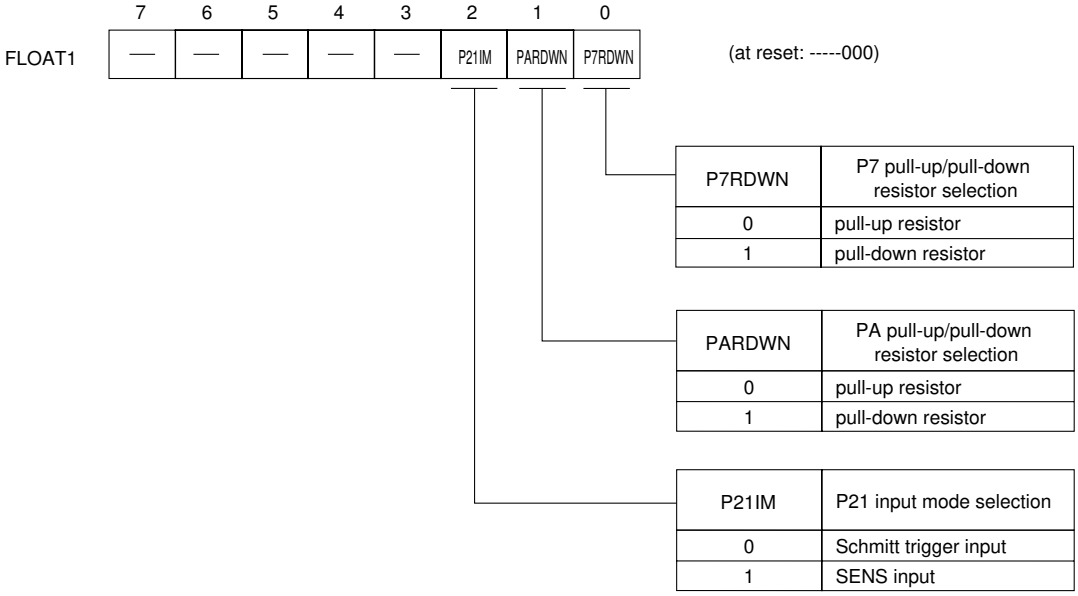
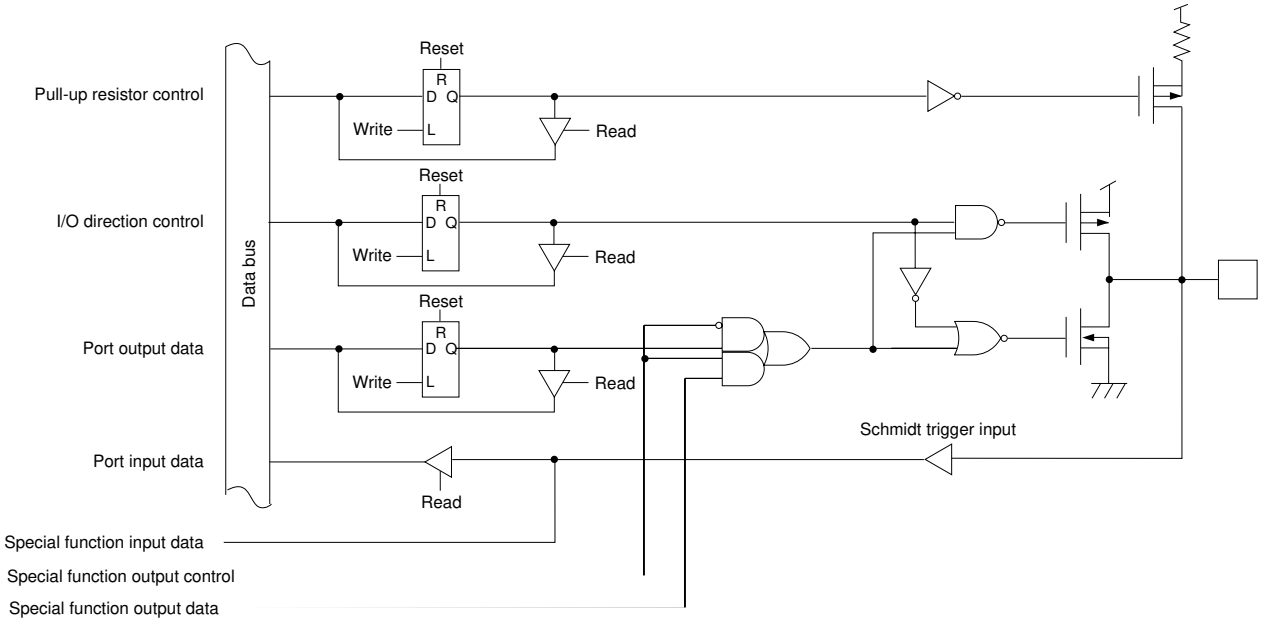


Figure 3-2-2 Pin Control Register 1(FLOAT1: X'03F4B',R/W)

3-3 I/O Port Configuration and Functions

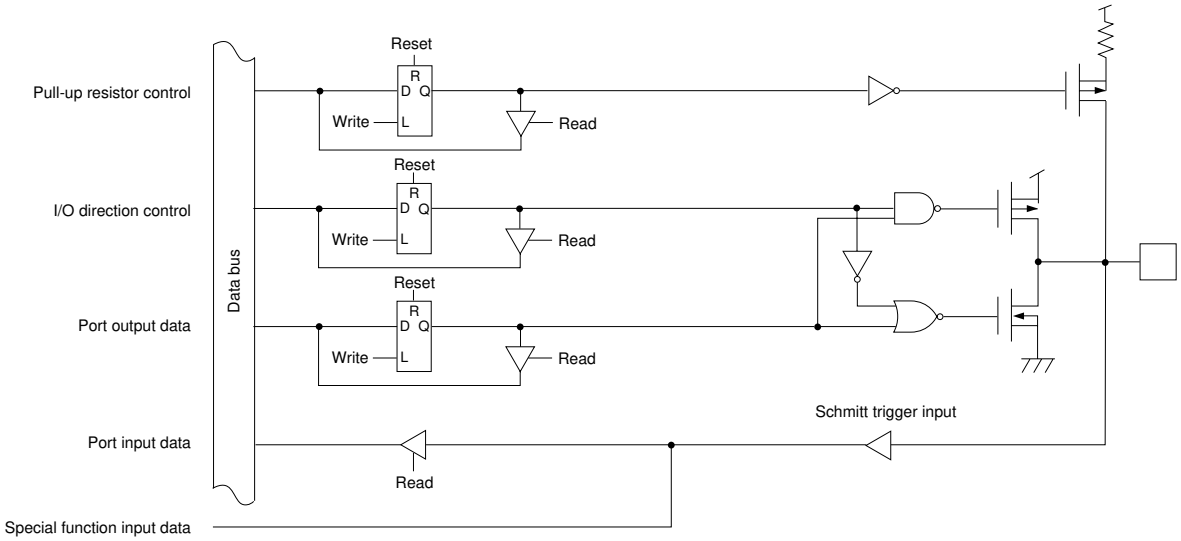
■ P00,P02,P10 to P14



		P00	P02	P10	P11	P12	P13	P14
Pull-up resistor control	Control bit	P0PLU0	P0PLU2	P1PLU0	P1PLU1	P1PLU2	P1PLU3	P1PLU4
	Register (address)	P0PLU (X'03F40')		P1PLU (X'03F41')				
I/O direction control	Control bit	P0DIR0	P0DIR2	P1DIR0	P1DIR1	P1DIR2	P1DIR3	P1DIR4
	Register (address)	P0DIR (X'03F30')		P1DIR (X'03F31')				
Port output	Control bit	P0OUT0	P0OUT2	P1OUT0	P1OUT1	P1OUT2	P1OUT3	P1OUT4
	Register (address)	P0OUT (X'03F10')		P1OUT (X'03F11')				
Port input	Control bit	P0IN0	P0IN2	P1IN0	P1IN1	P1IN2	P1IN3	P1IN4
	Register (address)	P0IN (X'03F20')		P1IN (X'03F21')				
Output format control	Control bit	SC0SBOM	SC0SBTM	——	——	——	——	——
	Register (address)	SC0MD3 (X'03F53')		——				
Special function input	Special function	——	SBT0	——	——	TM2I	TM3I	TM4I
Special function output control (1)	Special function	SBO0(TXD)	SBT0	RMOUT	——	TM2O	TM3O	TM4O
	Control bit	SC0SBOS	SC0SBTS	P10TCO	——	P12TCO	P13TCO	P14TCO
	Register (address)	SC0MD3 (X'03F53')		P1OMD (X'03F39')				
Special function output control (2)	Special function	SBO0/TXD	——	RMOUT	——	——	——	——
	Control bit	SC0CMD	——	RMOEN	——	——	——	——
	Register (address)	SC0CTR (X'03F54')	——	RMCTR (X'3F89)	——	——	——	——

* Both The TM0RM flag of the RMCTR register and the P10TCO flag of the P10MD register are used to switch between remote control output and timer output.

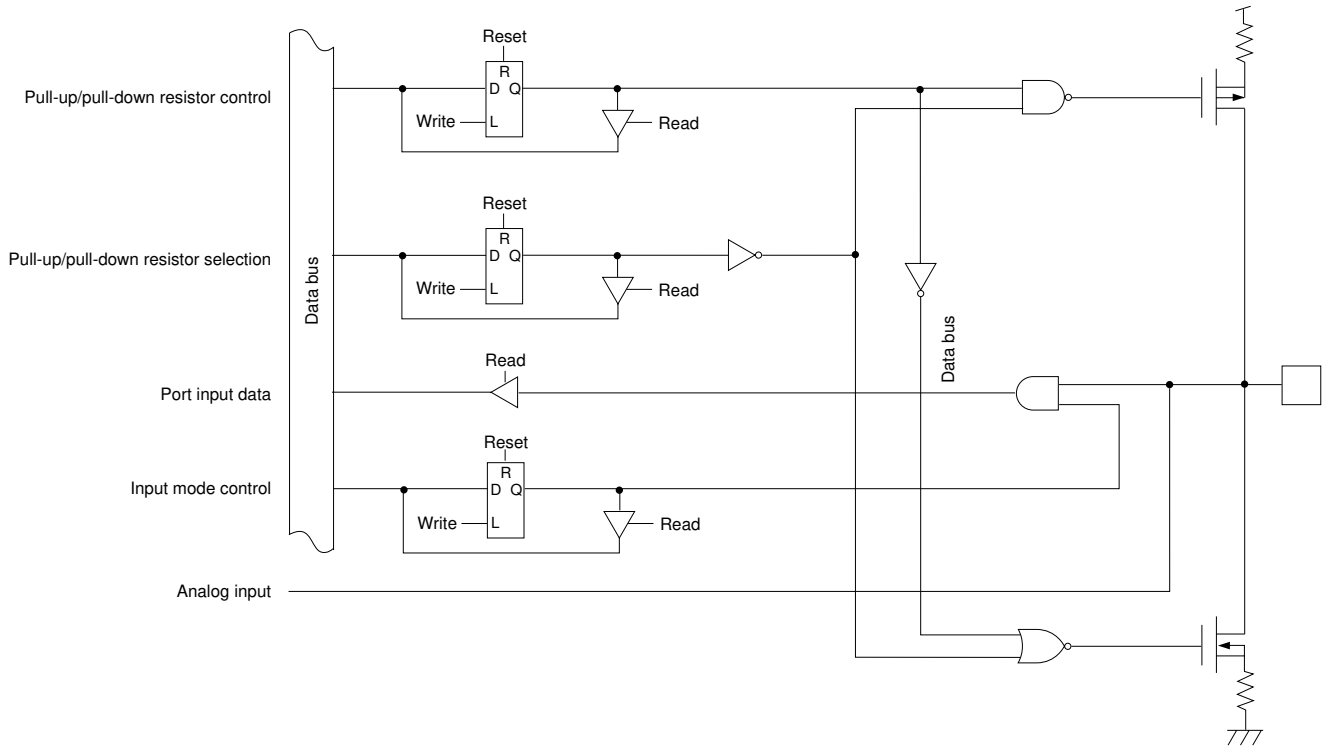
■ P01



		P01
Pull-up resistor control	Control bit	P0PLU1
	Register (address)	P0PLU (X'03F40')
I/O direction control	Control bit	P0DIR1
	Register (address)	P0DIR (X'03F30')
Port output	Control bit	P0OUT1
	Register (address)	P0OUT (X'03F10')
Port input	Control bit	P0IN1
	Register (address)	P0IN (X'03F20')
Special function input	Special function	SBI0/RXD

Figure 3-3-2 Configuration and Functions of P01

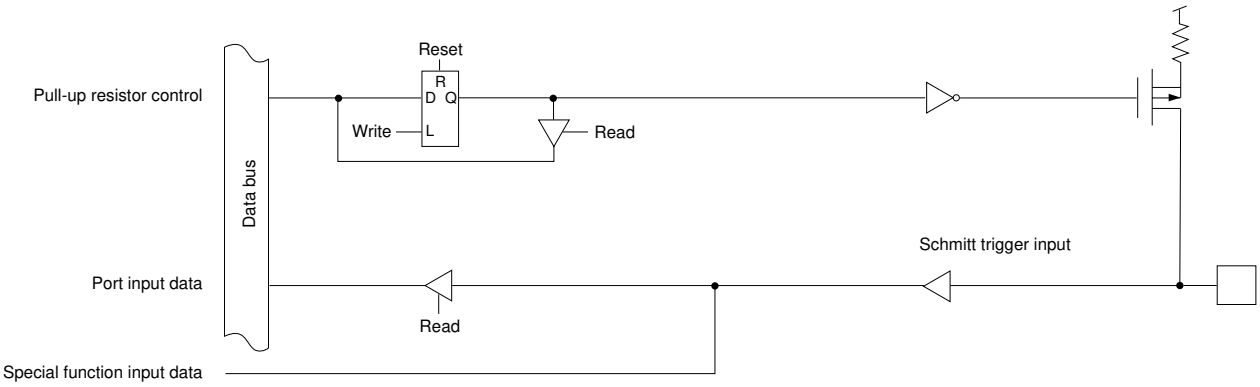
■ PA0 to PA7



		PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
Pull-up resistor control	Control bit	PAPLUD0	PAPLUD1	PAPLUD2	PAPLUD3	PAPLUD4	PAPLUD5	PAPLUD6	PAPLUD7
	Register (address)	PAPLUD (X'03F4A')							
Pull-up/ pull-down resistor control	Control bit	PARDWN							
	Register (address)	FLOAT1 (X'03F4B')							
Input mode control	Control bit	PAAIN0	PAAIN1	PAAIN2	PAAIN3	PAAIN4	PAAIN5	PAAIN6	PAAIN7
	Register (address)	PAIMD (X'03F3A')							
Port input	Control bit	PAIN0	PAIN1	PAIN2	PAIN3	PAIN4	PAIN5	PAIN6	PAIN7
	Register (address)	PAIN (X'03F2A')							
Special function input	Special function	AN0	AN1	AN2	AN3	AN4	AN5	AN6	AN7

Figure 3-3-3 Configuration and Functions of PA0 to PA7

■ Pin Configuration for P20, P22 to P23

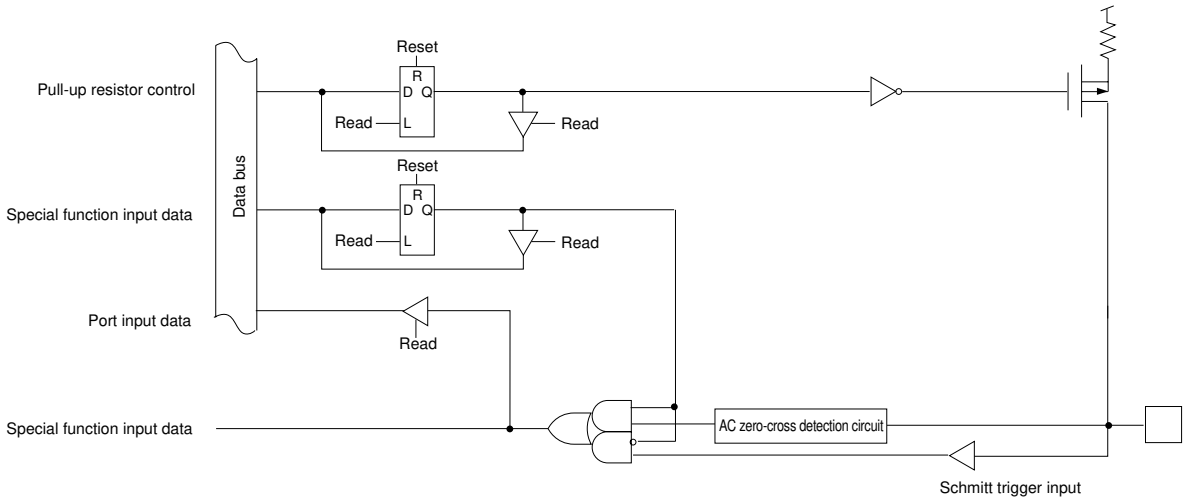


**P23 is only for 48-pin package.*

		P20	P22	P23
Pull-up resistor control	Control bit	P2PLU0	P2PLU2	P2PLU3
	Register (address)	P2PLU (X'03F42')		
Port input	Control bit	P2IN0	P2IN2	P2IN3
	Register (address)	P2IN (X'03F22')		
Special function input	Interrupt input	IRQ0	IRQ2	IRQ3

Figure 3-3-4 Configuration and Functions of P20, P22, P23

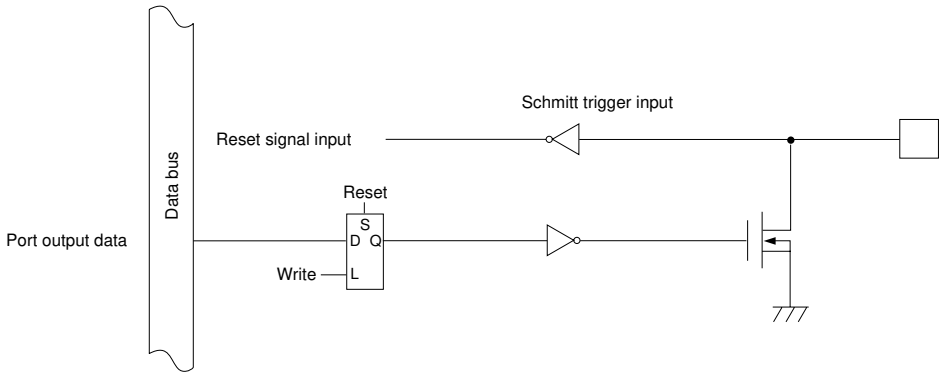
■ P21



		P21
Pull-up resistor control	Control bit	P2PLU1
	Register (address)	P2PLU (x'03F42')
Port input	Control bit	P2IN1
	Register (address)	P2IN (x'03F22')
Special function input selection	Special function	SENS
	Control bit	P21IM
	Register (address)	FLOAT1 (x'03F4B')

Figure 3-3-5 Configuration and Functions of P21

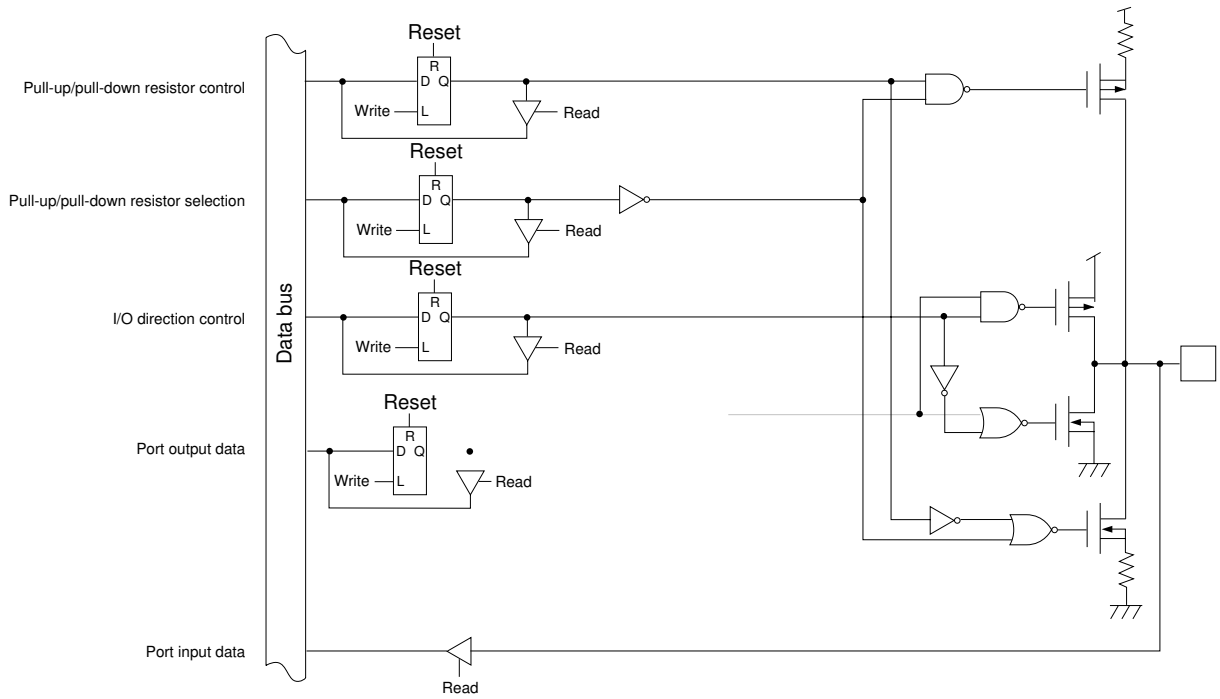
■ P27



		P27
Special input		$\overline{\text{RST}}$
Special function output	Special function	Soft reset output
	Control bit	P2OUT7
	Register (address)	P2OUT (x'03F12')

Figure 3-3-6 Configuration and Functions of P27

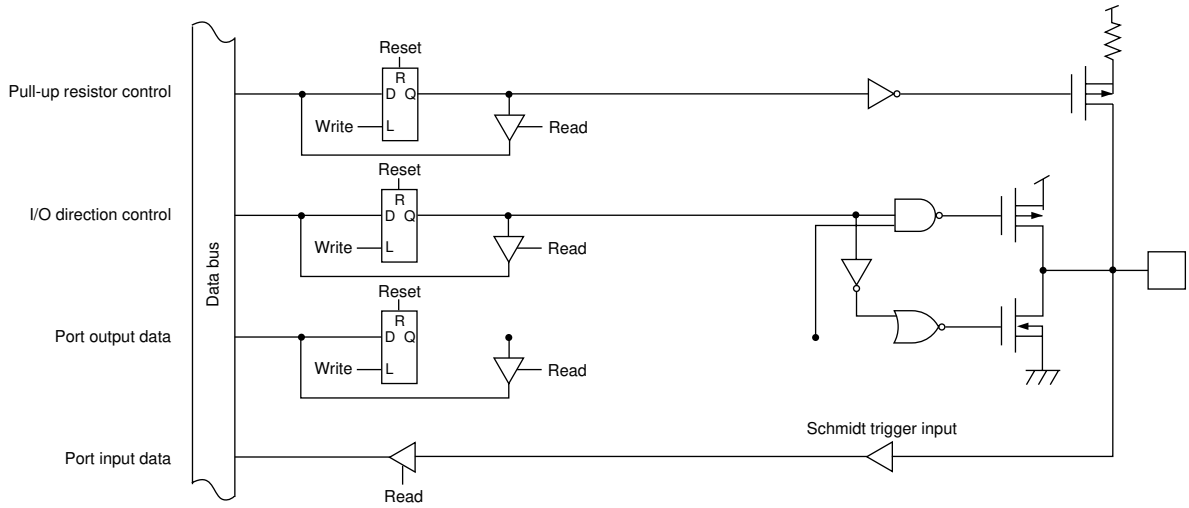
■ P70 to P71



		P70	P71
Pull-up/ pull-down resistor control	Control bit	P7PLUD0	P7PLUD1
	Register (address)	P7PLUD (X'03F47')	
Pull-up/ pull-down resistor control	Control bit	P7RDWN	
	Register (address)	FLOAT1 (X'03F4B')	
I/O direction control	Control bit	P7DIR0	P7DIR1
	Register (address)	P7DIR (X'03F37')	
Port input	Control bit	P7IN0	P7IN1
	Register (address)	P7IN (X'03F27')	
Port output	Control bit	P7OUT0	P7OUT1
	Register (address)	P7OUT (X'03F17')	

Figure 3-3-7 Configuration and Functions of P70

■P60 to P67,P80 to P87



		P60	P61	P62	P63	P64	P65	P66	P67
Pull-up resistor control	Control bit	P6PLU0	P6PLU1	P6PLU2	P6PLU3	P6PLU4	P6PLU5	P6PLU6	P6PLU7
	Register (address)	P6PLU (x'03F46')							
I/O direction control	Control bit	P6DIR0	P6DIR1	P6DIR2	P6DIR3	P6DIR4	P6DIR5	P6DIR6	P6DIR7
	Register (address)	P6DIR (x'03F36')							
Port output	Control bit	P6OUT0	P6OUT1	P6OUT2	P6OUT3	P6OUT4	P6OUT5	P6OUT6	P6OUT7
	Register (address)	P6OUT (x'03F16')							
Port input	Control bit	P6IN0	P6IN1	P6IN2	P6IN3	P6IN4	P6IN5	P6IN6	P6IN7
	Register (address)	P6IN (x'03F26')							

Figure 3-3-8 Configuration and Functions of P60 to P67

		P80	P81	P82	P83	P84	P85	P86	P87
Pull-up resistor control	Control bit	P8PLU0	P8PLU1	P8PLU2	P8PLU3	P8PLU4	P8PLU5	P8PLU6	P8PLU7
	Register (address)	P8PLU (x'03F48')							
I/O direction control	Control bit	P8DIR0	P8DIR1	P8DIR2	P8DIR3	P8DIR4	P8DIR5	P8DIR6	P8DIR7
	Register (address)	P8DIR (x'03F38')							
Port output	Control bit	P8OUT0	P8OUT1	P8OUT2	P8OUT3	P8OUT4	P8OUT5	P8OUT6	P8OUT7
	Register (address)	P8OUT (x'03F18')							
Port input	Control bit	P8IN0	P8IN1	P8IN2	P8IN3	P8IN4	P8IN5	P8IN6	P8IN7
	Register (address)	P8IN (x'03F28')							

Figure 3-3-9 Configuration and Functions of P80 to P87

Chapter 4 Timer Functions

4

4-1 Overview

The MN101C117 contains three 8-bit timers, one 16-bit timer, a watchdog timer, a time base timer, and circuits for remote control output and buzzer output.

Table 4-1-1 Summary of Timer Functions

		Timer 2 (8-bit)	Timer 3 (8-bit)	Timer 4 (16-bit)	Timer 5 (8-bit)	Time Base
Interrupt		TM2IRQ	TM3IRQ	TM4IRQ	TM5IRQ	TBIRQ
Timer operation		○	○	○	○	○
Event counter		○	○	○	×	×
Timer pulse output		○	○	○	×	×
Serial transmission clock		×	○	×	×	×
PWM output		○	×	○	×	×
Cascade connection		○		×	×	×
Capture function		×	×	○	×	×
Clock source	0	fs	fosc	fosc	fosc	fosc
	1	fs/4	fs/4	fs/4	fs/4	fx
	2	fx	fs/16	fs/16	fx	
	3	TM2IO input	TM3IO input	TM4IO input	fosc,fx/2^{13}	
Other			Remote control carrier pulse generation	Pulse added type PWM	Not possible to temporarily halt BC	

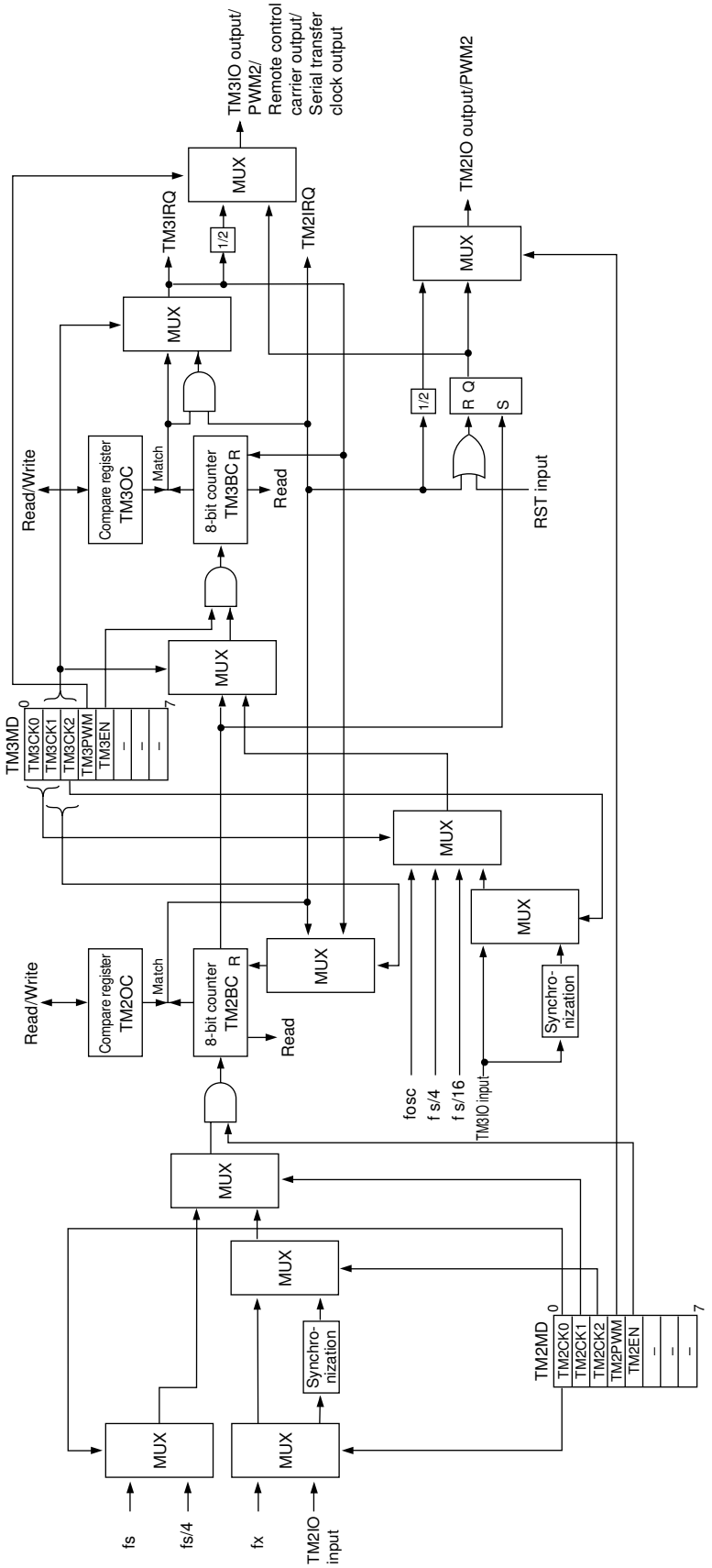


Figure 4-1-1 Timers 2, 3 Block Diagram

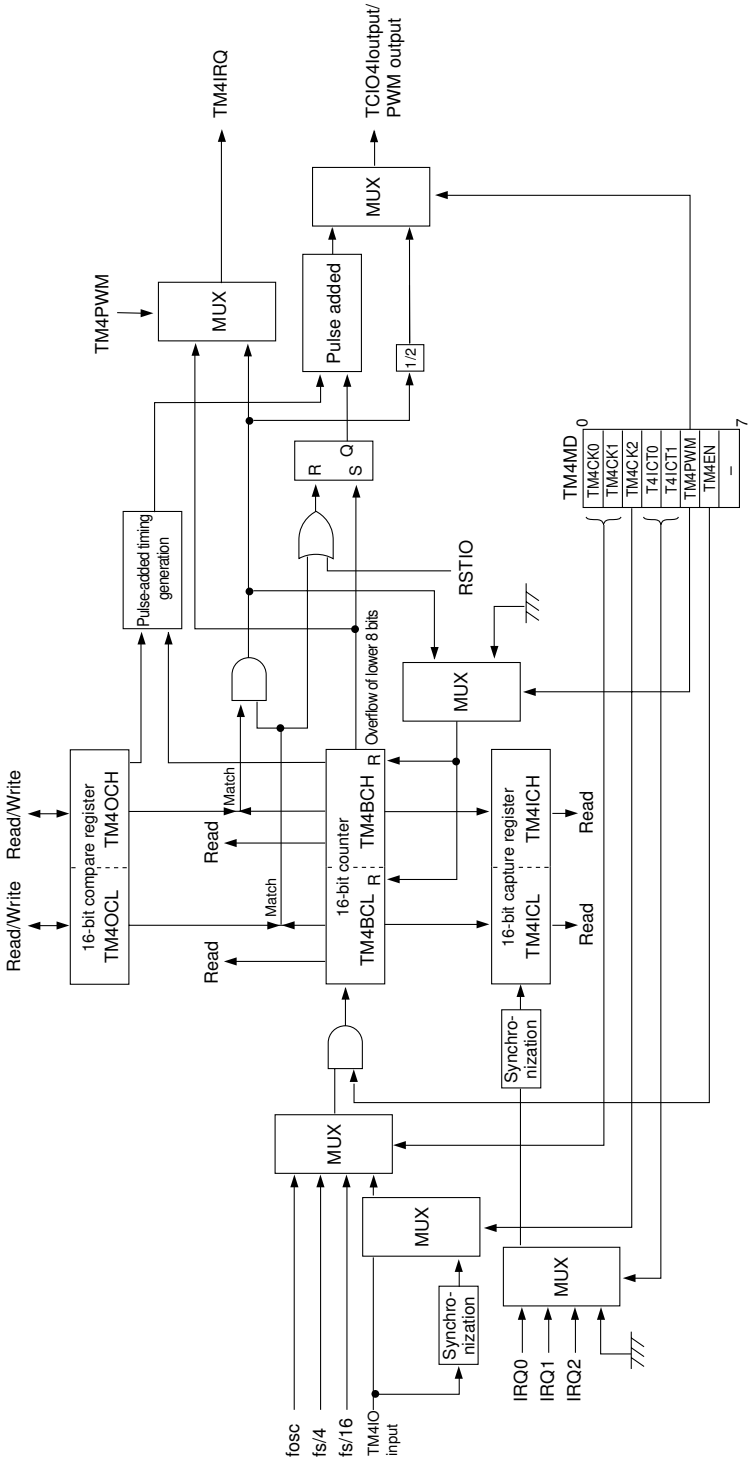


Figure 4-1-2 Timer 4 Block Diagram

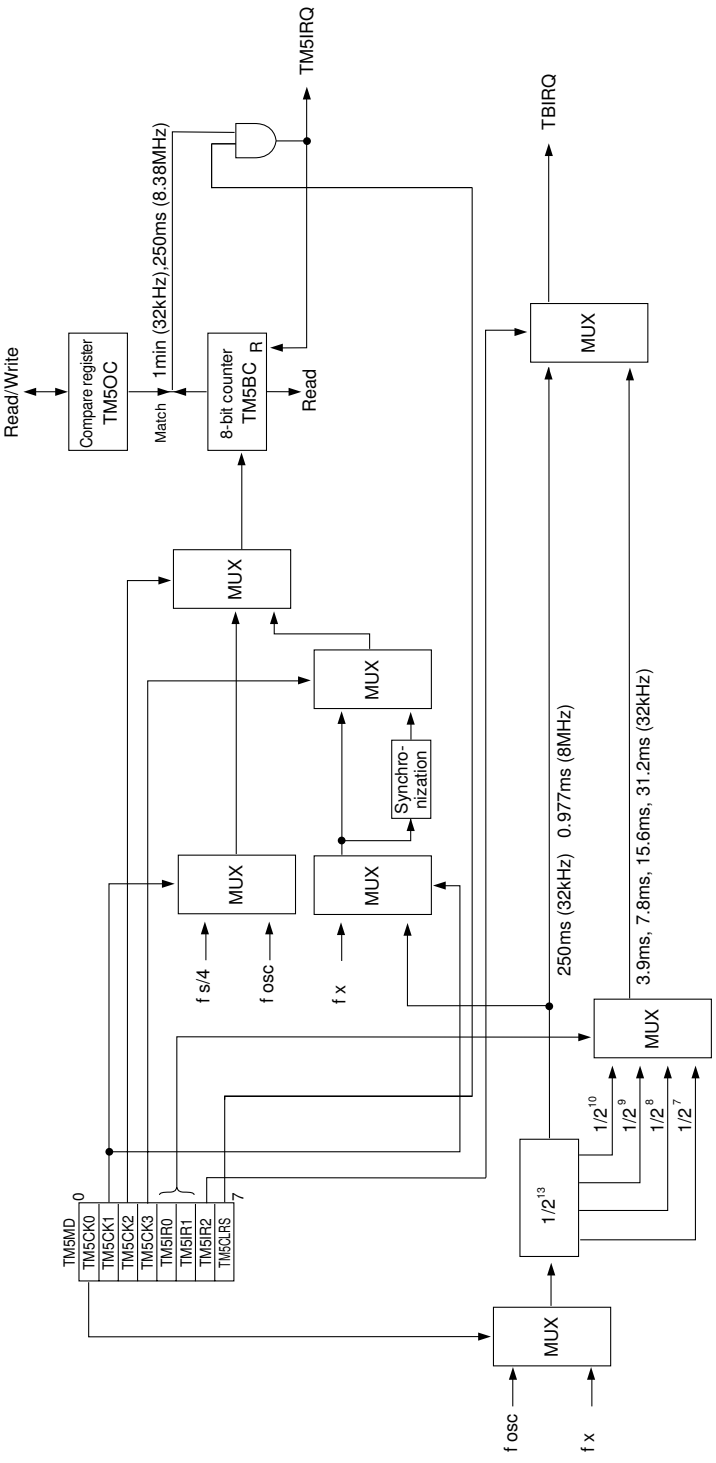


Figure 4-1-3 Timer 5/Time Base Block Diagram

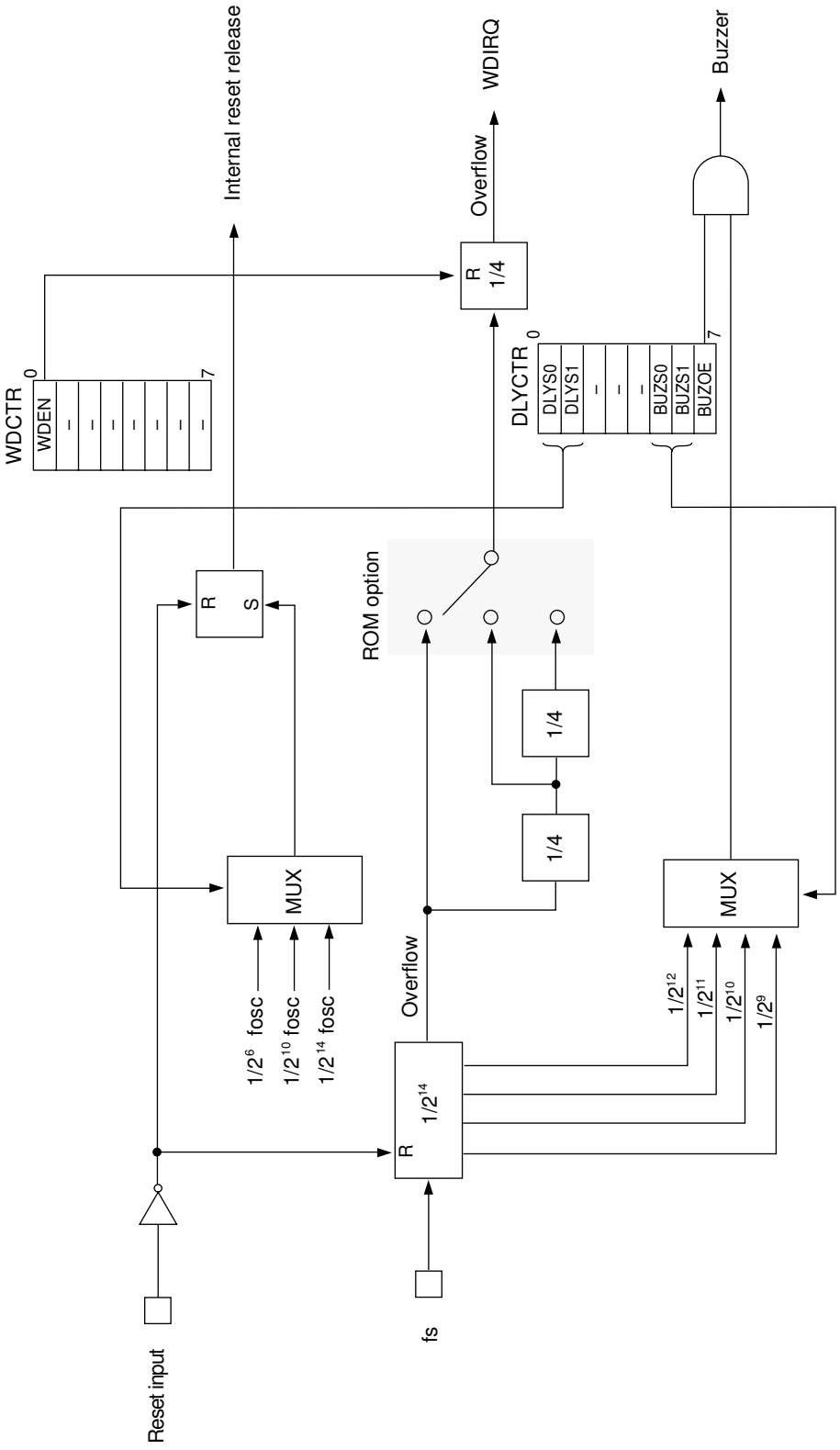


Figure 4-1-4 Watchdog Timer, Buzzer Block Diagram

Refer to the aragraph [1-6-1 ROM option]

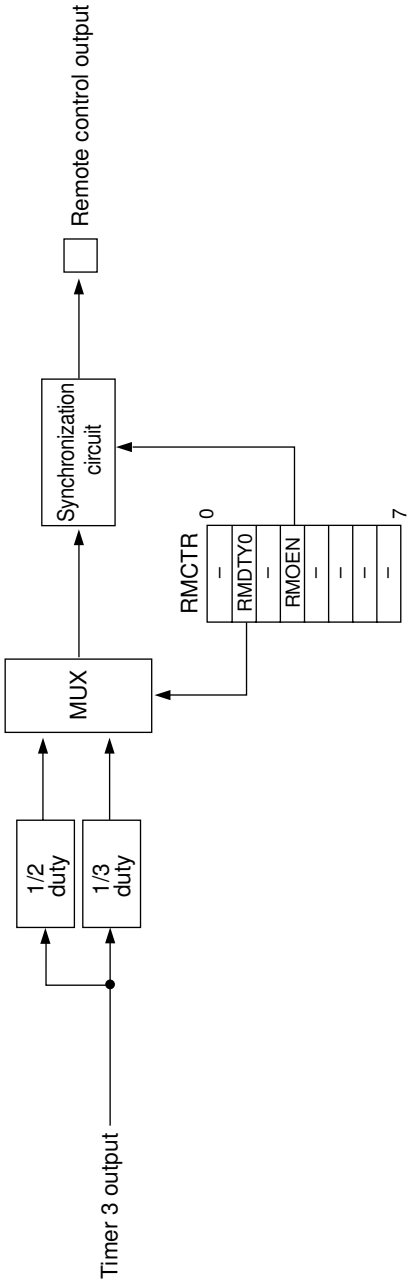


Figure 4-1-5 Remote Control Transmission Block Diagram

4-2 8-bit Timer Operation (timers 2, 3)

4-2-1 Overview

Functions for timers 2 and 3 are listed below.

Table 4-2-1 Summary of 8-bit Timer Functions

	Timer 2 (8-bit)	Timer 3 (8-bit)
Interrupt	TM2IRQ	TM3IRQ
Timer operation	○	○
Event counter	○	○
Timer pulse output	○	○
Serial transmission clock	×	○ (SIF0)
PWM output	○	×
Cascade connection	○	
Remote control carrier pulse generation	×	○

4-2-2 Operation

■ Timer Operation (timers 2, 3)

Settings for timer operation are listed below. Timer 2 is used as an example.

(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.

(2) Set the TM2CK2 to 0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.

(3) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.

(4) Set a value in compare register 2 (TM2OC).

(5) Set the TM2EN flag of the TM2MD register to "1" to start the timer.

(6) When timer 2 begins operation, binary counter 2 (TM2BC) will count upward from X'00'.

(7) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

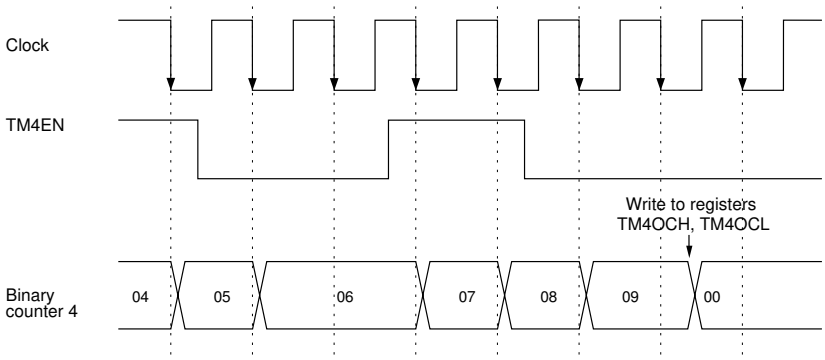


Figure 4-2-1 Binary Counter 2 (TM2BC) Count Timing

If the TM2EN flag of TM2MD register is changed simultaneously with other bits, the switching operation may cause binary counter 2 to be incremented.

If the value of TM2OC register is overwritten while timer 2 has stopped counting, binary counter 2 will be reset to X'00' at the edge of next count clock.

The value of TM3CK0~2 of T3MD register is unsettled. If timer2/ timer 3 is independently used, any mode except cascade connection should be set.

When servicing an interrupt, reset the timer 2 interrupt request flag before starting timer 2.

During a count operation, be careful if the value set in TM2OC is smaller than the value of binary counter 2, since the count-up operation will continue until overflow occurs.

If fx is to be selected as the clock source and the value of binary counter 2 is to be read during operation, select synchronized fx in order to avoid reading data that may be incomplete during count-up transitions. However, with synchronized fx, it is not possible to return from STOP/HALT modes.

If TM2IO input is selected as the clock source and the value of binary counter 2 is to be read during operation, select synchronized TM2IO input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized TM2IO input, it is not possible to return from STOP/HALT modes.

■ Event Count Function (timers 2, 3)

Settings for the event count function are listed below. Timer 2 is used as an example.

(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
(2) Use the TM2CK2 to 0 flags of the TM2MD register to select TM2IO input or synchronous TM2IO input as the clock source.
(3) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
(4) Set a value in compare register 2 (TM2OC).
(5) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
(6) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
(7) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

When synchronized TM2IO is selected, the timer 2 clock source is synchronized with the system clock after a transition of the TM2IO input signal. Binary counter 2 counts upward based on a signal synchronized to the system clock. Therefore, correct values can be read from binary counter 2.

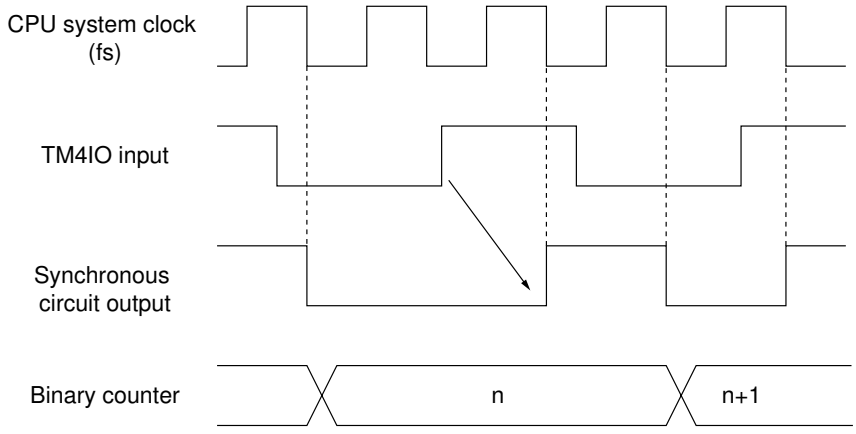


Figure 4-2-2 Timer 2 Event Counter Timing
(when synchronous TM2IO input is selected)

■ Timer Pulse Output Function (timers 2, 3)

The period of a signal output to the port is 1/2 of the period set in the TM2OC register.

If port 1 is to be used as a pulse output pin, it is necessary to set the port 1 output direction control register (P1DIR) and the port 1 pull-up/pull-down resistor control register (P1PLU).

Settings for the timer pulse output function are listed below. Timer 2 is used as an example.

(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
(2) Set bit 2 of the port 1 output/input mode register (P1OMD) to "1" to set the special function pin. Bit 2 of port 1 will be specified as the pulse output pin.
(3) Set the TM2CK2 to 0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.
(4) Set the TM2PWM flag of the TM2MD register to "0" so that normal timer operation is selected.
(5) Set a value in compare register 2 (TM2OC).
(6) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
(7) When timer 2 begins operation, binary counter 2 will count upward from X'00'.
(8) When the value of binary counter 2 matches that of the TM2OC register, the timer 2 interrupt request flag is set, and the binary counter 2 is reset to X'00' and begins to count upward again.

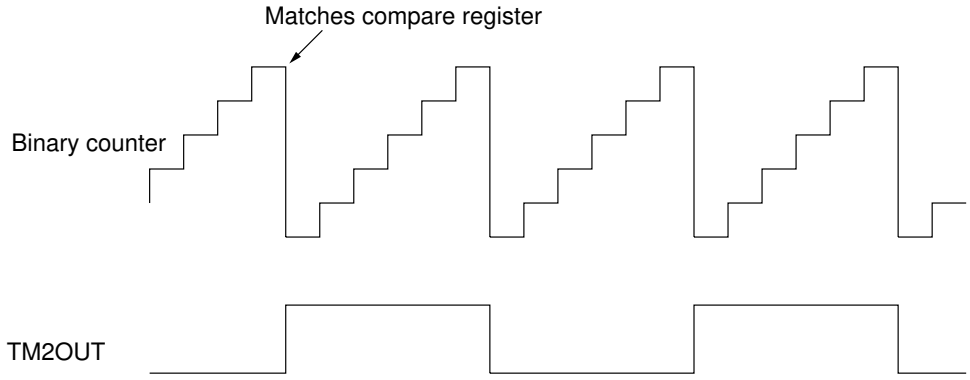


Figure 4-2-3 Timer Pulse Output Timing

If the TM3PWM flag of the TM3MD register is set to "1" and timer 2 PWM output is selected, the PWM output of timer 2 will also be output from the TM3IO pin.

If port 1 is to be used as a PWM output pin, the P1DIR and P1PLU registers must be set.

■ PWM Output Function (Timer 2)

Settings for the PWM output function are listed below.

(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.

(2) Set bit 2 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 2 of port 1 will be specified as the PWM output pin.

(3) Set the TM2CK2 to 0 flags of the TM2MD register to select fs, fs/4, fx, or synchronous fx as the clock source. The period of the output waveform is determined based on the clock source.

(4) Set the TM2PWM flag of the TM2MD register to "1" so that PWM operation is selected.

(5) Set a value in compare register 2 (TM2OC). The high interval of the output waveform is determined based on the value of the TM2OC compare register.

(6) Set the TM2EN flag of the TM2MD register to "1" to start the timer.

(7) When timer 2 begins operation, binary counter 2 will count upward from X'00'.

(8) A high-level signal is output from the port beginning when binary counter 2 starts counting at X'00' and ending when the value of binary counter 2 matches the value set in the TM2OC register.

(9) When the value of binary counter 2 matches that of the TM2OC register, a low-level signal is output from the port.

(10) Binary counter 2 continues to count upward until X'FF' is reached. At the next count-up cycle, the value of binary counter 2 is reset to X'00', a high-level signal is output from the port, and counting begins again.

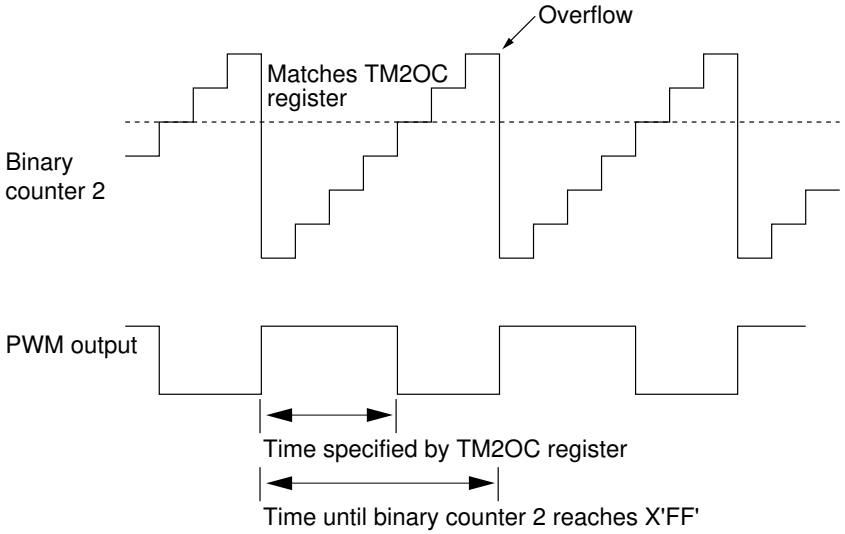


Figure 4-2-4 PWM Output Timing

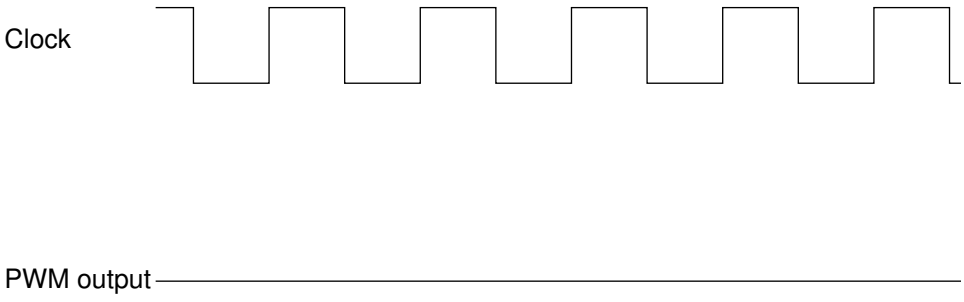


Figure 4-2-5 PWM Output Timing (when TM2OC register is X'00')

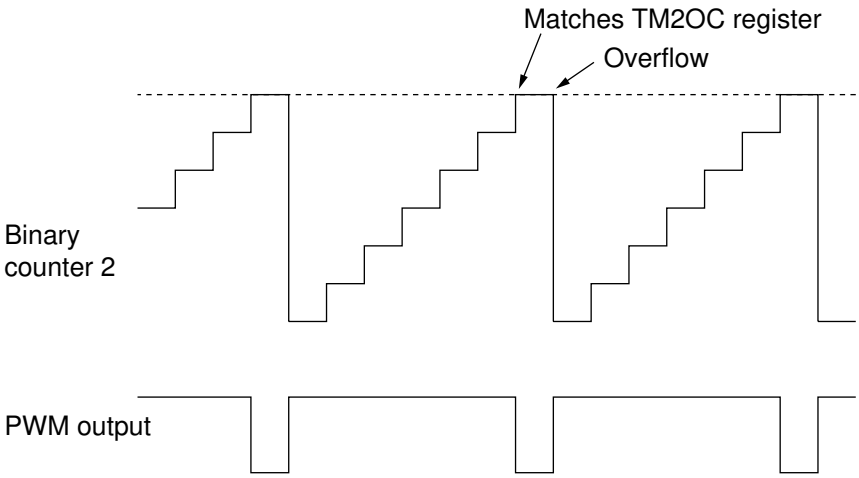


Figure 4-2-6 PWM Output Timing (when TM2OC register is X'FF')

The clock source for the serial interface has a frequency that is 1/2 of the overflow output of timer 3.

For serial interface settings, refer to the chapter on serial functions.

■ Serial Transfer Clock Function(timer 3)

Settings for the serial transfer clock function are listed below.

(1) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop the count operation of timer 3.
(2) Set the SC0CK1 and SC0CK0 flags of the serial interface 0 mode register 1 (SC0MD1) to select 1/2 of the timer 3 overflow frequency as the clock source.
(3) Set the TM3CK2 to 0 flags of the TM3MD register to select fosc, fs, fs/4, or fs/16 as the clock source.
(4) Set the TM3PWM flag of the TM3MD register to "0" to select timer 3 output.
(5) Set a value in compare register 3 (TM3OC).
(6) Set the TM3EN flag of the TM3MD register to "1" to start the timer.

(7) When timer 3 begins operation, binary counter 3 counts upward from X'00'.
(8) When the value of binary counter 3 matches that of the TM3OC register, the timer 3 interrupt request flag is set, the value of binary counter 3 is reset to X'00', and counting begins again.

■ Cascade Connection Function (timer 2 + timer 3)

Settings for the cascade connection function are listed below. Timer 2 and timer 3 are connected to operate as a 16-bit timer.

(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the count operation of timer 2.
(2) Set the TM3EN flag of the timer 3 mode register (TM3MD) to "0" to stop the count operation of timer 3.
(3) Set the TM2CK2 to 0 flags of the TM2MD register to select fs, fs/4, fx, or synchronized fx as the clock source.
(4) Use the TM3CK2 to 0 flags of the TM3MD register to set the clock source as a cascade connection with timer 2.
(5) Set the TM2PWM flag of the TM2MD register to "0" to select normal timer operation.
(6) Set values in compare register 2 (TM2OC) and compare register 3 (TM3OC).
(7) Set the TM2EN flag of the TM2MD register to "1" to start the timer.
(8) Set the TM3EN flag of the TM3MD register to "1" to start the timer.
(9) When timers 2 and 3 begin operation, the binary counters begin counting upward from X'0000' as a 16-bit counter.

Disable the timer 2 interrupt.

(10) When the value of the 16-bit binary counter matches that of the 16-bit register (TM3OC+TM2OC), the timer 3 interrupt request flag is set, the value of the 16-bit binary counter is reset to X'0000', and counting begins again.

Use a 16-bit access instruction to set the (TM3OC+TM2OC) register.

4-3 16-bit Timer Operation (timer 4)

4-3-1 Overview

Timer 4 is a 16-bit programmable counter that can be used as an event counter.
A signal with a frequency of 1/2 of the timer 4 overflow signal can be output from the TM4IO pin. An input capture function and pulse added type PWM output function can also be used.

4-3-2 Operation

■ Timer Operation

Settings for timer operation are listed below.

(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
(2) Set the TM4CK2 to 0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source.
(3) Set the TM4PWM flag of the TM4MD register to "0" to select 16-bit timer operation.
(4) Set a value in compare register 4 (TM4OCH, TM4OCL).
(5) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
(6) When timer 4 begins operation, binary counter 4 counts upward from X'0000'.
(7) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, the value of binary counter 4 is reset to X'0000', and counting begins again.

When servicing an interrupt, reset the timer 4 interrupt request flag before operating timer 4.

During a count operation, be careful if the value set in TM4OCH and TM4OCL is smaller than the value of binary counter 4, since the count-up operation will continue until overflow occurs.

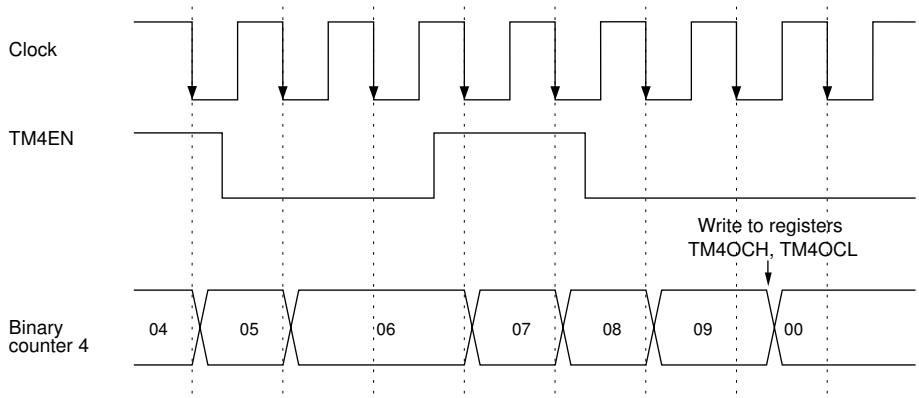


Figure 4-3-1 Binary Counter 4 (TM4BC) Count Timing

If the TM4EN flag of the TM4MD register is changed simultaneously with other bits, the switching operation may cause binary counter 4 to be incremented.

If the value of the TM4OCH, TM4OCL register is overwritten while timer 4 has stopped counting, binary counter 4 will be reset to X'0000'.

■ Event Count Function

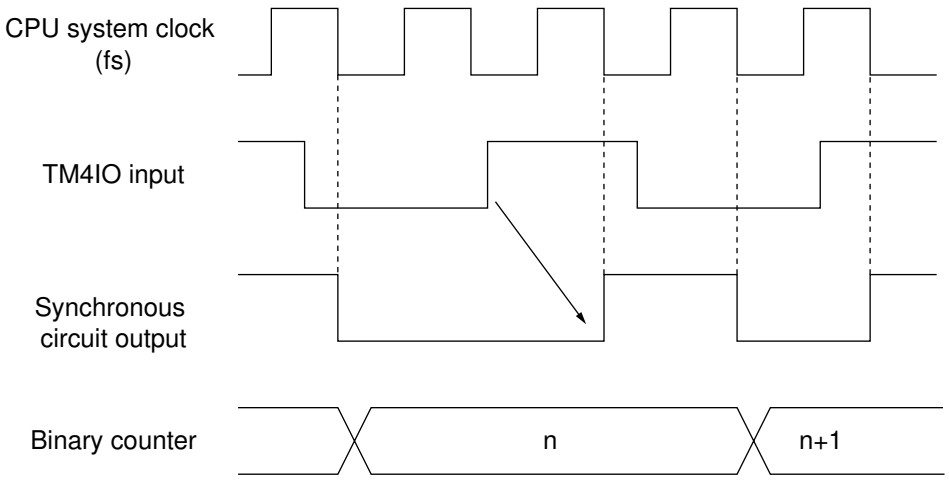
Settings for the event count function are listed below.

(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
(2) Use the TM4CK2 to 0 flags of the TM4MD register to select TM4IO input or synchronized TM4IO input as the clock source.
(3) Set the TM4PWM flag of the TM4MD register to "0" so that 16-bit timer operation is selected.
(4) Set a value in compare register 4 (TM4OCH, TM4OCL).
(5) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
(6) When timer 4 begins operation, binary counter 4 will count upward from X'0000'.
(7) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, and the binary counter 4 is reset to X'0000' and begins to count upward again.

If TM4IO input is selected as the clock source and the value of binary counter 4 is to be read during operation, select synchronized TM4IO input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized TM4IO input, it is not possible to return from STOP/HALT modes.

When synchronized TM4IO is selected, the timer 4 clock source is synchronized with the system clock after a transition of the TM4IO input signal. Timer 4 counts upward based on a signal synchronized to the system clock. Therefore, correct values can be read from binary counter 4.

Figure 4-3-2 Timer 4 Event Counter Timing (when synchronous TM4IO



input is selected)

The period of the output signal from the port is 1/2 of the period set in the TM4OCH, TM4OCL register.

■ Timer Pulse Output Function

Settings for the timer pulse output function are listed below.

(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" so that the count operation of timer 4 is stopped.

(2) Set bit 4 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 4 of port 1 will be specified as the pulse output pin.

(3) Use the TM4CK2 to 0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source.

(4) Set the TM4PWM flag of the TM4MD register to "0" so that 16-bit timer operation is selected.

(5) Set a value in compare register 4 (TM4OCH, TM4OCL).

(6) Set the TM4EN flag of the TM4MD register to "1" to start the timer.

(7) When timer 4 begins operation, binary counter 4 will count upward from X'0000'.

(8) When the value of binary counter 4 matches that of the TM4OCH and TM4OCL registers, the timer 4 interrupt request flag is set, and the binary counter 4 is reset to X'0000' and begins to count upward again.

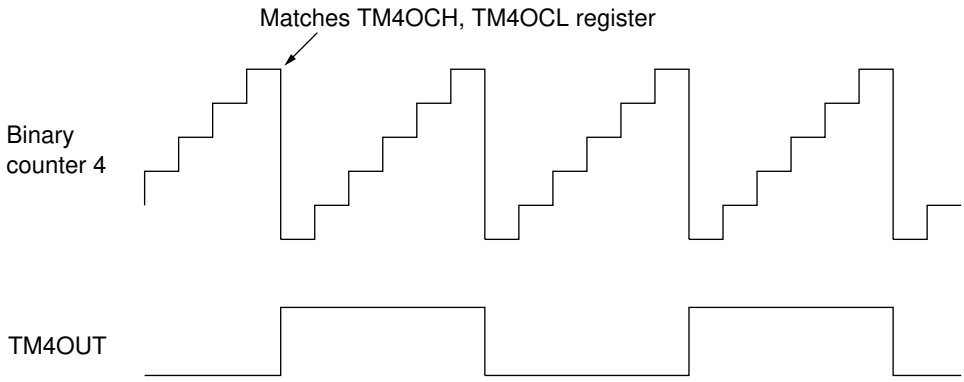


Figure 4-3-3 Timer Pulse Output Timing

■ Pulse Added Type PWM Output Function

If bit 4 of port 1 is to be used as a PWM output pin, set the P1DIR and P1PLU registers.

In the pulse added method, a 1-bit output is appended to the basic component of the 8-bit PWM output. Precise control is possible based on the number of PWM repetitions (256 times) to which this bit is appended. Settings for the pulse added type PWM output function are listed below.

(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.
(2) Set bit 4 of the port 1 output/input mode register (P1OMD) to the special function pin setting. Bit 4 of port 1 will be specified as the PWM output pin.
(3) Use the TM4CK2 to 0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source. The period of the output waveform is determined based on the clock source.
(4) Set the TM4PWM flag of the TM4MD register to "1" so that PWM operation is selected.
(5) Set a value in the lower 8 bits of compare register 4 (TM4OCL). The high interval of the output waveform is determined based on the value of the lower 8 bits of compare register 4 (TM4OCL).
(6) Set the position of the added pulse in the upper 8 bits of compare register 4 (TM4OCH).
(7) Set the TM4EN flag of the TM4MD register to "1" to start the timer.
(8) When timer 4 begins operation, binary counter 4 will count upward from X'00'.
(9) A high-level signal is output from the port beginning when binary counter 4 starts counting from X'00' and ending when the value of binary counter 4 matches the value set in the TM4OCL register.
(10) When the value of binary counter 4 matches that of the TM4OCL register, a low-level signal is output from the port.
(11) Binary counter 4 continues to count upward until X'FF' is reached. At the next count-up cycle, the value of binary counter 4 is reset to X'00', and counting begins again. A high-level signal is output from the port.

PWM4 output is fixed at L with X'FF' set at the lower 8 bits(TM40CL) of compare register. Use of timer 4 at PWM mode disables setting of X'FF' att TM4OCL register.

Use a 16-bit access instruction to set the TM4OCH, TM4OCL register.

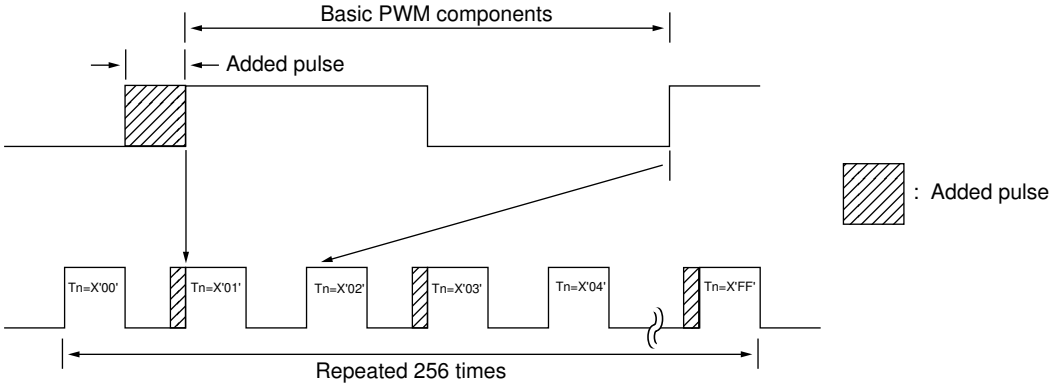


Figure 4-3-4 Pulse Added Type PWM Output

[☞ 5-2-3 "Serial Interface Transfer Timing"]

■ Setting the Added Pulse Position

The upper 8 bits of compare register 4 (TM4OCH) set the position of the added pulse. If the TM4OCH register is set to X'00', an additional bit is not appended to the basic PWM component. If the TM4OCH register is set to X'FF', an additional bit is repeatedly appended to the 255 basic PWM components during the period. The relation between the value set in the TM4OCH register and the added pulse is shown in the table below. If X'03' is set in the TM4OCH register, bits are appended to pulse positions for X'01' and X'02', shown in table 4-3-1. The relation between the value set in the TM4OCH register and the position of the added bit is shown in figure 4-3-5.

Table 4-3-1 Pulse-Added PWM OutputFigure

Value Set in TM4OCH Register	Added Pulse Position (value of Tn)
0 0 0 0 0 0 0 0	
0 0 0 0 0 0 0 1	X'80'
0 0 0 0 0 0 1 0	X'40',X'C0'
0 0 0 0 0 1 0 0	X'20',X'60',X'A0',X'E0'
0 0 0 0 1 0 0 0	X'10',X'30',X'50',X'70',X'90',X'B0',X'D0',X'F0'
0 0 0 1 0 0 0 0	X'08',X'18',X'28',X'38',X'48',X'58' . . . . .,X'E8',X'F8'
0 0 1 0 0 0 0 0	X'04',X'0C',X'14',X'1C',X'24',X'2C' . . . . .,X'F4',X'FC'
0 1 0 0 0 0 0 0	X'02',X'06',X'0A',X'0E',X'12',X'16' . . . . .,X'FA',X'FE'
1 0 0 0 0 0 0 0	X'01',X'03',X'05',X'07',X'09',X'0B' . . . . .,X'FD',X'FF'
(MSB) (LSB)	

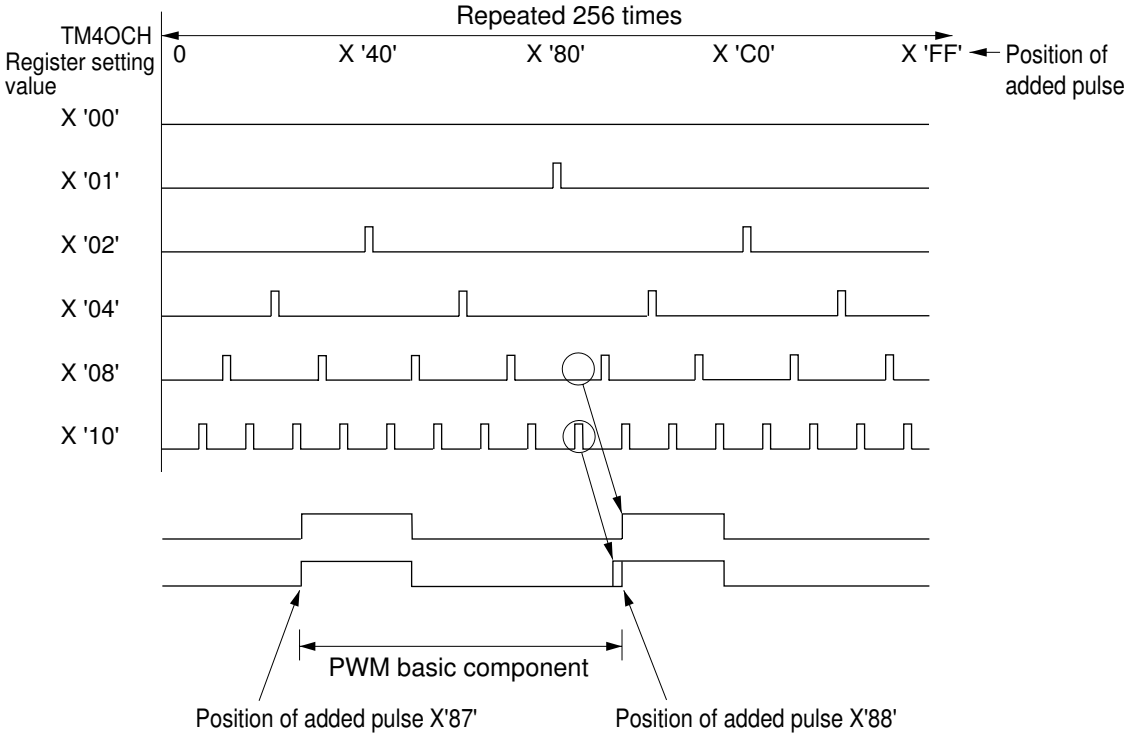


Figure 4-3-5 Pulse Added Type PWM Output

■ Capture Function

Settings for the capture function are listed below.

(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop the count operation of timer 4.

(2) Use the TM4CK2 to 0 flags of the TM4MD register to select fosc, fs/4, or fs/16 as the clock source.

(3) Use the T4ICTS1 and T4ICTS0 flags of the TM4MD register to select IRQ2, IRQ1, or IRQ0 as the input capture trigger.

(4) Set the REDGn flag of the external interrupt control register to specify the valid edge for the interrupt selected as the TM4 input capture trigger.

(5) Set the TM4PWM flag of the TM4MD register to "1" to select 16-bit timer operation.

(6) Set a value in compare register 4 (TM4OCH, TM4OCL).

Setting a value in compare register 4, clears binary counter 4.

(7) Set the TM4EN flag of the TM4MD register to "1" to start the timer.

(8) When timer 4 begins operation, binary counter 4 will count upward from X'0000' until it reaches the value set in compare register 4.

(9) If the binary counter is to be used as a free-running counter that counts from X'0000' to X'FFFF', set the compare register 4 to X'FFFF'.
When the value of binary counter 4 matches that of the TM4OCH, TM4OCL register, the timer 4 interrupt request flag is set, binary counter 4 is reset to X'0000', and counting begins again.

(10) If the external interrupt selected as the TM4 input capture trigger is received during timer 4 operation, the value of binary counter 4 will be written into the input capture register (TM4ICH, TM4ICL).

If the event occurs before a read, that data will be overwritten.

4-4 8-bit Timer Operation (timer 5)

4-4-1 Overview

Timer 5 is an 8-bit timer that can have fosc, fs/4, fx, or time base output as its clock source.

4-4-2 Operation

■ Timer Operation

Settings for timer operation are listed below.

(1) Set the TM5CLRS flag of the timer 5 mode register (TM5MD) to "0."

(2) Use the TM5CK3 to 1 flags of the TM5MD register to select fosc, fs/4, fx, synchronized fx, time base timer output, or time base timer synchronized output as the clock source.

(3) Set a value in compare register 5 (TM5OC). At this time, if the TM5CLRS flag is "0," binary counter 5 will be initialized to X'00'.

(4) Binary counter 5 (TM5OC) counts upward from X'00'.

(5) When the value of binary counter 5 matches that of the TM5OC register, the timer 5 interrupt request flag is set, the binary counter is reset to X'00', and counting begins again.

When servicing an interrupt, reset the timer 5 interrupt request flag before starting timer 5.

When choosing either time base timer output or time base timer synchronized output for the timer 5 clock source, the time base must be set up.

During a count operation, be careful if the value set in TM5OC is smaller than the value of binary counter 5, since the count-up operation will continue until overflow occurs.

If fx input is selected as the clock source and the value of binary counter 5 is to be read during operation, select synchronized fx input to avoid reading data that may be incomplete during count-up transitions. However, with synchronized fx input, it is not possible to return from STOP/HALT modes.

If the TM5CLRS flag of the TM5MD register is set to "0," binary counter 5 will be initialized every time data in the TM5OC register is overwritten. Timer 5 interrupts are disabled in this mode. If timer 5 interrupts are to be used, the TM5CLRS flag must be reset to "1" after writing to the TM5OC register.

Timer 5 operation cannot be halted.

4-5 Time Base Operation

4-5-1 Overview

The clock source for the time base timer can be set to fosc or fx. Also, the interrupt period for time base timer (TBIRQ) can be set to $1/2^7$, $1/2^8$, $1/2^9$, $1/2^{10}$, or $1/2^{13}$ of the clock source.

4-5-2 Operation

■ Time Base Function

Settings for the time base function are listed below.

(1) Use the TM5CK0 flag of the timer 5 mode register (TM5MD) to select fosc or fx as the clock source.
(2) Use the TM5IR2 to 0 flags of the TM5MD register to select the time base timer interrupt source.
(3) When the selected time interval passes, the interrupt request flag of the time base interrupt control register (TBICR) is set.

Time base operation cannot be halted.

Table 4-5-1 Base Time Settings

TM5IR2 to 0 / Clock Source		000 $\frac{1}{2^7}$	001 $\frac{1}{2^8}$	010 $\frac{1}{2^9}$	011 $\frac{1}{2^{10}}$	1XX $\frac{1}{2^{13}}$
fosc	20MHz	6.4µs	12.8µs	25.6µs	51.2µs	409.6µs
	8.38MHz	15.2µs	30.5µs	61.0µs	122.0µs	976.4µs
fx	32.768kHz	3.9ms	7.8ms	15.6ms	31.2ms	250ms

4-6 Watchdog Timer Operation

4-6-1 Overview

The watchdog timer is controlled by the watchdog control register (WDCTR) and can be used for runaway program detection.

4-6-2 Setup and Operation

(1) Set the WDEN flag of the watchdog timer control register (WDCTR) to "1" to start the watchdog timer.

(2) Operate the watchdog timer by clearing the WDEN flag to "0" within the fixed amount of time (T_{WD}), and then resetting the WDEN flag to "1."

If the WDEN flag is not cleared, a WDT interrupt will be generated after the fixed amount of time passes.

(3) When an illegal operation is detected, the program encoded at the location of the WDT interrupt routine is executed.

The upper 2 bits of the watchdog timer are cleared when the WDEN flag is set to "0." Therefore, if WDEN flag is set to 0 when an uppermost bit of a watchdog timer is 1, WDT interrupt occurs depending on the timing of this clear the watchdog timer may be reset at 1/4T_{WD}. If the WDEN bit is to be repeatedly cleared and set at regular intervals, those operations should be performed within 1/4 of the T_{WD} period.

T_{WD} is set by the ROM option as $fs/2^{16}$, $fs/2^{18}$, or $fs/2^{20}$.

Illegal operation detection period vs. WDEN clear period is shown by the following formula:

Illegal operation detection period > [WDEN clear period] x 4

When software resetting is not triggered by WDT interrupt, hardware resetting (low level output at the reset terminal) takes place at the next WDT interrupt.

4-7 Remote Control Output Operation

4-7-1 Overview

A remote control carrier pulse can be generated using the overflow of timer 3. Two duty ratios of 1/2 or 1/3 can be selected.

4-7-2 Setup and Operation

(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR)to "0" so that the remote control carrier output is switched off.

(2) Set timer 3 to select the base period of the remote control carrier (the width that the remote control carrier output pulse is held at a high level).

(3) Set the RMDTY0 flag of the RMCTR register to select the carrier duty.

(4) Set the P10 output data to "0" and set P10 to the output mode. And select the remote control carrier output by setting the TMORM flag of the RMCTR register to "0".

(5) The RMOEN flag of the RMCTR register controls whether the remote control carrier output is on or off.
Even if the carrier output is at a high level, and the RMOEN flag is set to "0" (off), the carrier waveform will be maintained by the synchronous circuit

Set bit 0 of the P1OMD register to "1" at the same time the remote control output is switched on, and to "0" at the same time the remote control output is switched off.

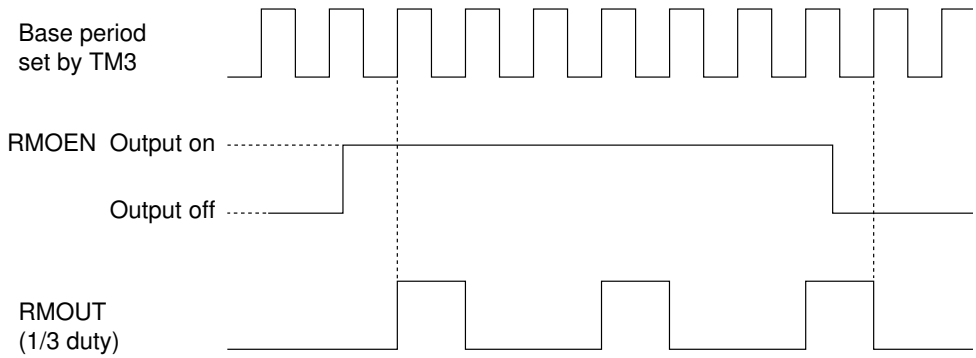


Figure 4-7-1 Remote Control Carrier Output Waveform

4-8 Buzzer Output

4-8-1 Buzzer Output Setup and Operation

The square wave having a frequency $1/2^9$ to $1/2^{12}$ of the system clock can be output from the P06/BUZZER pin.

(1) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "0" so that the buzzer output is turned off.
(2) Set the buzzer output frequency with the BUZCK1 and BUZCK0 flags of the DLYCTR.
(3) Set the BUZOE flag of the DLYCTR register to "1" and set P06 to the buzzer output mode.
(4) The BUZOE flag of the DLYCTR register controls whether the buzzer output is ON or OFF.

4-9 Timer Function Control Registers

4-9-1 Overview

19 registers control the timers. See table 4-9-1.

Table 4-9-1 Timer Control Registers

Name	Address	R/W	Function
TM2OC	X'03F72'	R/W	Compare register 2
TM2BC	X'03F62'	R	Binary counter 2
TM2MD	X'03F82'	R/W	Timer 2 mode register
TM3OC	X'03F73'	R/W	Compare register 3
TM3BC	X'03F63'	R	Binary counter 3
TM3MD	X'03F83'	R/W	Timer 3 mode register
TM4OCL	X'03F74'	R/W	Compare register 4 (lower 8 bits)
TM4OCH	X'03F75'	R/W	Compare register 4 (upper 8 bits)
TM4BCL	X'03F64'	R	Binary counter 4 (lower 8 bits)
TM4BCH	X'03F65'	R	Binary counter 4 (upper 8 bits)
TM4ICL	X'03F66'	R	Input capture register (lower 8 bits)
TM4ICH	X'03F67'	R	Input capture register (upper 8 bits)
TM4MD	X'03F84'	R/W	Timer 4 mode register
TM5OC	X'03F78'	R/W	Compare register 5
TM5BC	X'03F68'	R	Binary counter 5
TM5MD	X'03F88'	R/W	Timer 5 mode register
WDCTR	X'03F02'	R/W	Watchdog timer control register
DLYCTR	X'03F03'	R/W	Oscillation stabilization wait control register
RMCTR	X'03F89'	R/W	Remote control carrier output control register

R/W: Readable and writable

R: Read only

4-9-2 Programmable Timer/Counters

Timers 2~5 all contain a programmable 8-bit timer/counter (16-bit in timer 4). Programmable timer/counters consist of a compare register and a binary counter.

(1) Compare register 2 (TM2OC)

7	6	5	4	3	2	1	0	
TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	(at reset: undefined)

Figure 4-9-1 Compare Register 2 (TM2OC: X'03F72', R/W)

(2) Binary counter 2 (TM2BC)

7	6	5	4	3	2	1	0	
TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	(at reset: 00000000)

Figure 4-9-2 Binary Counter 2 (TM2BC: X'03F62', R)

(3) Compare register 3 (TM3OC)

7	6	5	4	3	2	1	0	
TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	(at reset: undefined)

Figure 4-9-3 Compare Register 3 (TM3OC: X'03F73', R/W)

(4) Binary counter 3 (TM3BC)

7	6	5	4	3	2	1	0	
TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	(at reset: 00000000)

Figure 4-9-4 Binary Counter 3 (TM3BC: X'03F63', R)

(5) Compare register 4 (TM4OCL) (lower 8 bits)

7	6	5	4	3	2	1	0	
TM4OCL7	TM4OCL6	TM4OCL5	TM4OCL4	TM4OCL3	TM4OCL2	TM4OCL1	TM4OCL0	(at reset: undefined)

Figure 4-9-5 Compare Register 4 (TM4OCL: X'03F74', R/W)

(6) Compare register 4 (TM4OCH) (upper 8 bits)

7	6	5	4	3	2	1	0	
TM4OCH7	TM4OCH6	TM4OCH5	TM4OCH4	TM4OCH3	TM4OCH2	TM4OCH1	TM4OCH0	(at reset: undefined)

Figure 4-9-6 Compare Register 4 (TM4OCH: X'03F75', R/W)

(7) Binary counter 4 (TM4BCL) (lower 8 bits)

7	6	5	4	3	2	1	0	
TM4BCL7	TM4BCL6	TM4BCL5	TM4BCL4	TM4BCL3	TM4BCL2	TM4BCL1	TM4BCL0	(at reset: 00000000)

Figure 4-9-7 Binary Counter 4 (TM4BCL: X'03F64', R)

(8) Binary counter 4 (TM4BCH) (upper 8 bits)

7	6	5	4	3	2	1	0	
TM4BCH7	TM4BCH6	TM4BCH5	TM4BCH4	TM4BCH3	TM4BCH2	TM4BCH1	TM4BCH0	(at reset: 00000000)

Figure 4-9-8 Binary Counter 4 (TM4BCH: X'03F65', R)

(9) Input capture register (TM4ICL) (lower 8 bits)

7	6	5	4	3	2	1	0	
TM4ICL7	TM4ICL6	TM4ICL5	TM4ICL4	TM4ICL3	TM4ICL2	TM4ICL1	TM4ICL0	(at reset: undefined)

Figure 4-9-9 Input Capture Register (TM4ICL: X'03F66', R)

(10) Input capture register (TM4ICH) (upper 8 bits)

7	6	5	4	3	2	1	0	
TM4ICH7	TM4ICH6	TM4ICH5	TM4ICH4	TM4ICH3	TM4ICH2	TM4ICH1	TM4ICH0	(at reset: undefined)

Figure 4-9-10 Input Capture Register (TM4ICH: X'03F67', R)

(11) Compare register 5 (TM5OC)

7	6	5	4	3	2	1	0	
TM5OC7	TM5OC6	TM5OC5	TM5OC4	TM5OC3	TM5OC2	TM5OC1	TM5OC0	(at reset: undefined)

Figure 4-9-11 Compare Register 5 (TM5OC: X'03F78', R/W)

(12) Binary counter 5 (TM5BC)

7	6	5	4	3	2	1	0	
TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0	(at reset: 00000000)

Figure 4-9-12 Binary Counter 5 (TM5BC: X'03F68', R)

4-9-3 Timer Mode Registers

Four readable and writable 6-byte timer mode registers. Control timers 2, 3, 4, 5, and the time base.

(1) Timer 2 mode register (TM2MD)

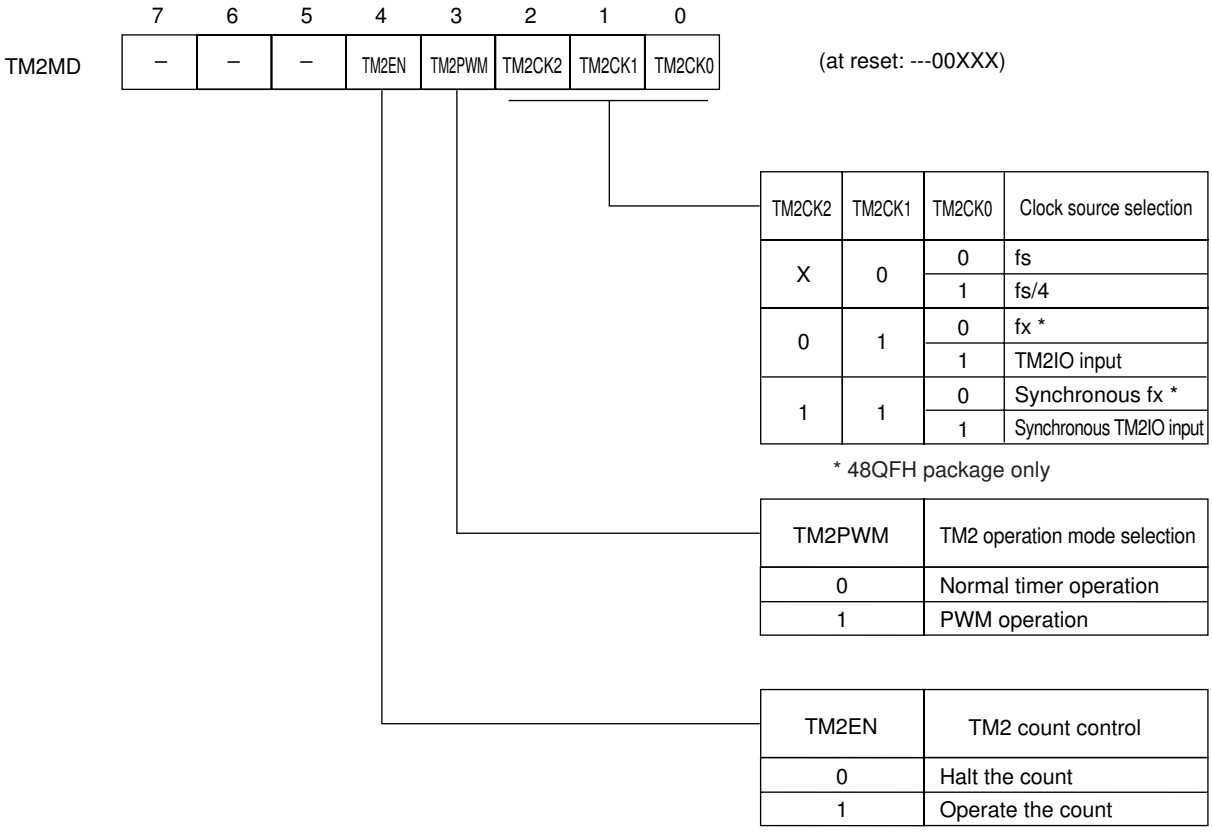
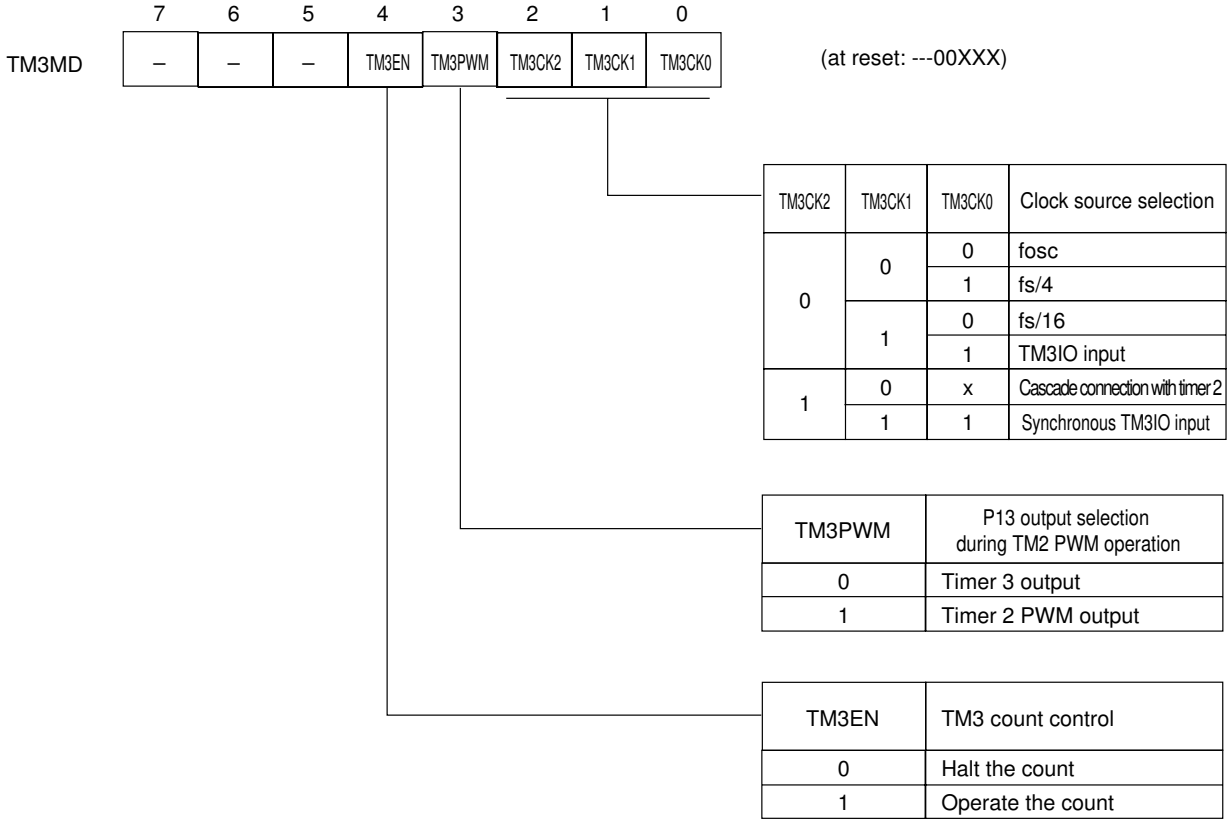


Figure 4-9-13 Timer 2 Mode Register (TM2MD: X'03F82', R/W)

(2) Timer 3 mode register (TM3MD)



TM3CK2	TM3CK1	TM3CK0	Clock source selection
0	0	0	fosc
		1	fs/4
	1	0	fs/16
		1	TM3IO input
1	0	x	Cascade connection with timer 2
	1	1	Synchronous TM3IO input

TM3PWM	P13 output selection during TM2 PWM operation
0	Timer 3 output
1	Timer 2 PWM output

TM3EN	TM3 count control
0	Halt the count
1	Operate the count

Figure 4-9-14 Timer 3 Mode Register (TM3MD: X'03F83', R/W)

(3) Timer 4 mode register (TM4MD)

	7	6	5	4	3	2	1	0
TM4MD	–	TM4EN	TM4PWM	T4ICTS1	T4ICTS0	TM4CK2	TM4CK1	TM4CK0

(at reset: -0000XXX)

TM4CK2	TM4CK1	TM4CK0	Clock source selection
0	0	0	fosc
		1	fs/4
	1	0	fs/16
		1	TM4IO input
1	1	1	Synchronous TM4IO input

T4ICTS1	T4ICTS0	TM4 input capture trigger selection
0	0	Disable input capture operation
	1	IRQ0
1	0	IRQ1
	1	IRQ2

TM4PWM	TM4 operation mode selection
0	16-bit timer operation
1	PWM operation

TM4EN	TM4 count control
0	Halt the count
1	Operate the count

Figure 4-9-15 Timer 4 Mode Register (TM4MD: X'03F84', R/W)

(4) Timer 5 mode register (TM5MD)

	7	6	5	4	3	2	1	0
TM5MD	TM5CLRS	TM5IR2	TM5IR1	TM5IR0	TM5CK3	TM5CK2	TM5CK1	TM5CK0

(at reset: 0XXXXXX0)

TM5CK0	Time base timer clock source selection
0	fosc
1	(Use Prohibited) fx *

* 48QFH package only

TM5CK3	TM5CK2	TM5CK1	Timer 5 clock source selection
X	0	0	fosc
		1	fs/4
0	1	0	(Use Prohibited)
		1	Output of time base timer
1		0	(Use Prohibited)
		1	Synchronous time base timer output

TM5IR2	TM5IR1	TM5IR0	Time base timer interrupt period selection
0	0	0	$1/2^7$ of the clock source
		1	$1/2^8$ of the clock source
	1	0	$1/2^9$ of the clock source
		1	$1/2^{10}$ of the clock source
1	x	x	$1/2^{13}$ of the clock source

TM5CLRS	Binary counter 5 clear selection flag
0	Enable initialization of TM5BC during a write to TM5OC
1	Disable initialization of TM5BC during a write to TM5OC

∗If TM5CLRS=0, TM5IRQ is disabled.

Figure 4-9-16 Timer 5 Mode Register (TM5MD: X'03F88', R/W)

4-9-4 Timer Control Registers

(1) Watchdog timer control register (WDCTR)

	7	6	5	4	3	2	1	0	
WDCTR	–	–	–	–	–	–	–	WDEN	(at reset: -------0)

WDEN	Watchdog timer enable
0	Clear watchdog timer/disable operation
1	Enable WDT timer

Figure 4-9-17 Watchdog Timer Control Register (WDCTR: X'03F02', R/W)

(2) Oscillation stabilization wait control register (DLYCTR)

	7	6	5	4	3	2	1	0	
DLYCTR	BUZOE	BUZCK1	BUZCK0	–	–	–	DLYS1	DLYS0	(at reset: 0XX---00)

DLYS1	DLYS0	Oscillation stabilization wait period setting
0	0	$1/2^{14}$ of the system clock (fs)
	1	$1/2^{10}$ of the system clock (fs)
1	0	$1/2^{6}$ of the system clock (fs)
1	1	Disable use

∗After reset is released, the oscillation stabilization wait period is fixed at $1/2^{15}$.

BUZCK1	BUZCK0	Buzzer output frequency selection
0	0	$1/2^{12}$ of the system clock (fs)
	1	$1/2^{11}$ of the system clock (fs)
1	0	$1/2^{10}$ of the system clock (fs)
	1	$1/2^{9}$ of the system clock (fs)

BUZOE	P06 output selection
0	P06 port output
1	P06 buzzer output

Figure 4-9-18 Oscillation Stabilization Wait Counter Control Register (DLYCTR: X'03F03', R/W)

(3) Remote control carrier output control register (RMCTR)

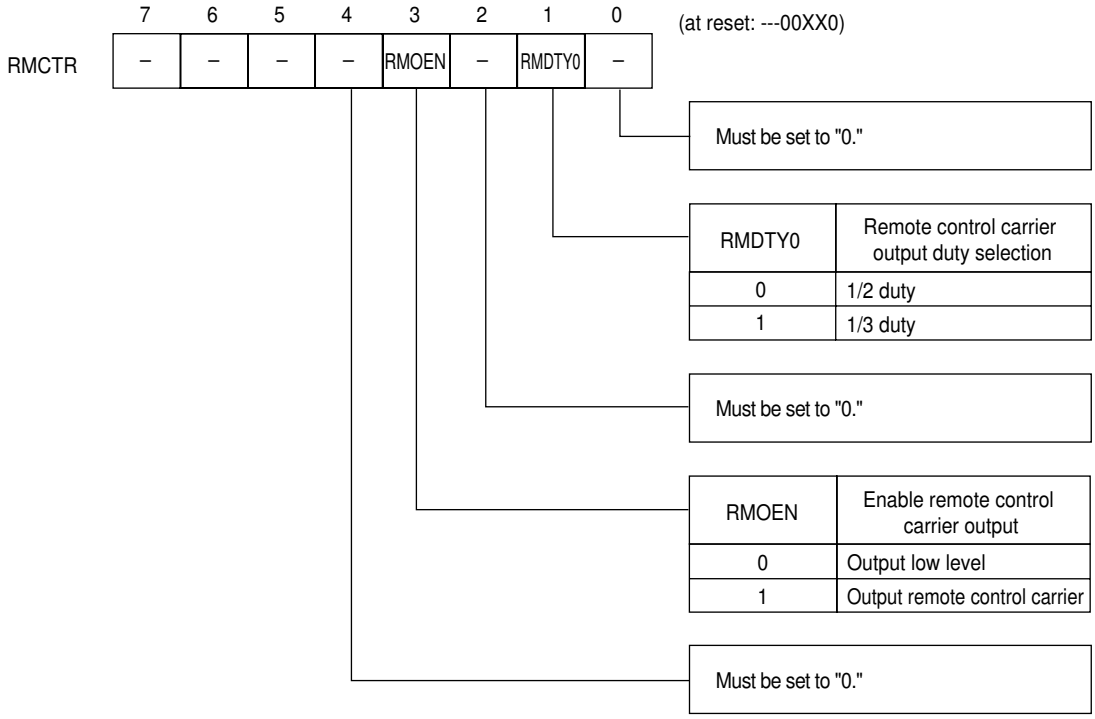


Figure 4-9-19 Remote Control Carrier Control Register (RMCTR: X'03F89', R/W)

Chapter 5 Serial Functions

5

5-1 Overview

The MN101C117 contains a serial interface that can operate in synchronous and simple UART modes.
An overview of serial functions is shown below.

Table 5-1-1 Overview of Serial Functions

	Serial 0
Interrupt	SC0ICR
Synchronous	◯
Simple UART	◯
Clock selection	fs/2 fs/4 fs/16 BC3X1/2 External
1/8 period of clock	◯

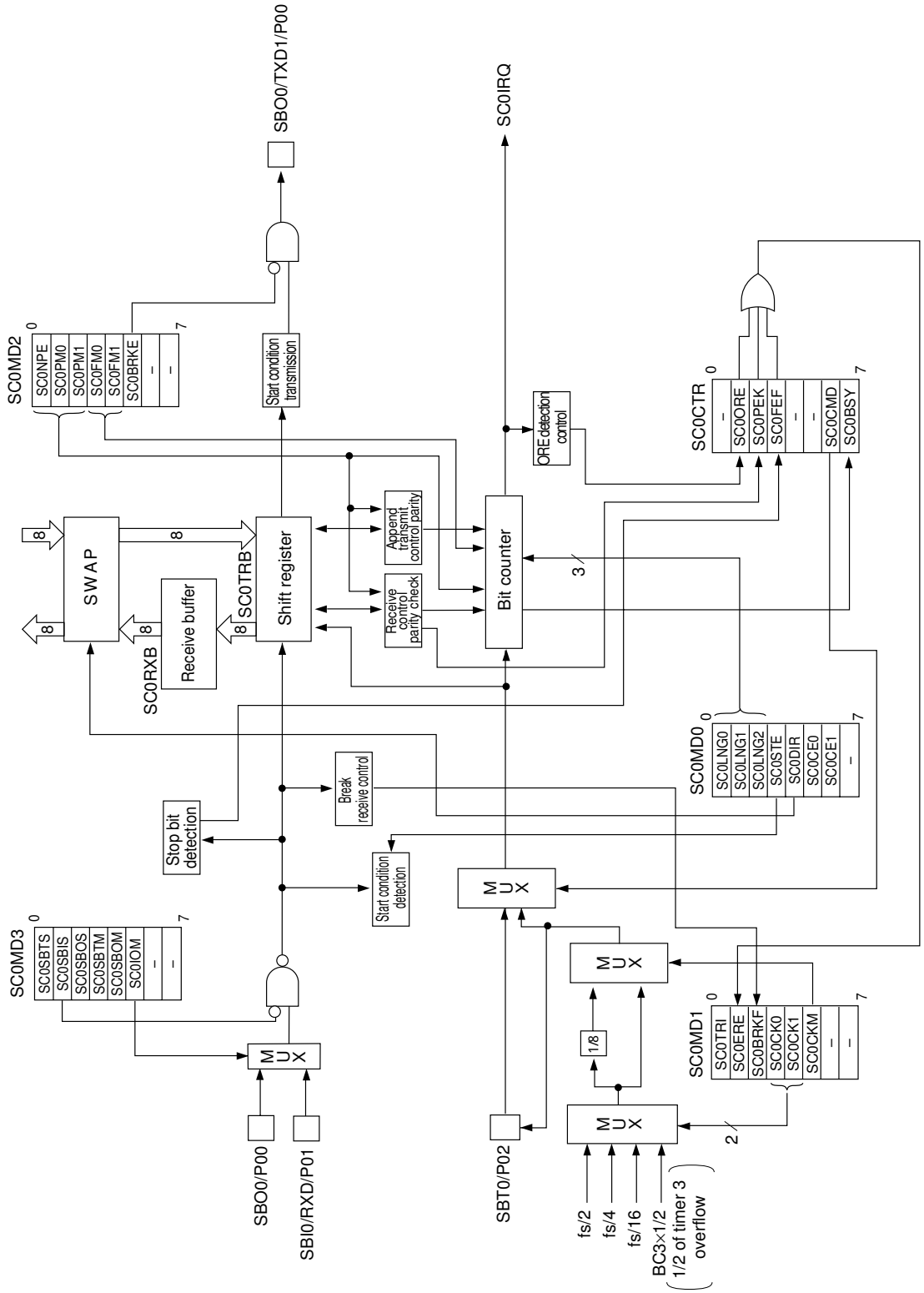


Figure 5-1-1 Serial 0 Block Diagram

5-2 Synchronous Serial Interface

5-2-1 Overview

A serial interface begins operation when data is written to the shift buffer. A bit counter is incremented at each 1-bit transfer. The transfer is complete when the counter overflows.

Bit transfers of an arbitrary 1 to 8 bits can be performed. The transfer bit count must be set before performing the transfer.

5-2-2 Setup and Operation

■ Transmission

(1) Select the synchronous serial interface by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "0."

(2) Select the transfer bit count with the SC0LNG2 to 0 flags of the serial interface 0 mode register 0 (SC0MD0). The transfer bit count can be set as 1 to 8 bits.

(3) Specify whether the start condition is enabled or disabled with the SC0STE flag of the SC0MD0 register.

(4) Specify the first bit to be transferred (MSB first or LSB first) with the SC0DIR flag of the SC0MD0 register.

[☞ Section 5-2-3, "Serial Interface Transfer Timing"]

(5) Select the valid edge of the clock signal with the SC0CE1 to 0 flags of the SC0MD0 register.

(6) When the clock source is an internal clock:
- Select the clock source with the SC0CK1 to 0 flags of serial interface 0 mode register 1 (SC0MD1).
- Set the SC0CKM flag of the SC0MD1 register specify whether or not the clock source frequency will be divided by 8.
- Select serial clock operation by setting the SC0SBTS flag of the serial interface 0 mode register 3 (SC0MD3) to "1."
- Set the SC0SBTM flag of the SC0MD3 register.
- Set bit 0 of the port 0 direction control register (P0DIR) to the output mode.
- Set bit 0 of the port 0 pull-up resistor control register (P0PLU).

When the clock source is an external clock (SBT0 pin input):

- Set the SC0SBTM flag of the SC0MD3 register.
- Set bit 2 of the P0DIR register to input mode.
- Set the P0PLU register, if necessary.

(7) Select the SC0SBOM flag of the SC0MD3 register.

(8) Select the SC0IOM flag of the SC0MD3 register.

(9) Select serial communication by setting the SC0SBOS flag of the SC0MD3 register to "1."

(10) Set transmit data to serial interface 0 transmit/receive shift register (SC0TRB). This will start the serial transmission.

(11) When serial transmission begins, the SC0BSY flag of the SC0CTR register is set to "1," indicating that a serial transfer is in progress.

(12) When the serial transmission has completed, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of SC0MD1 register 1 is cleared to "0."

When the serial port is enabled and the SC0CE1 to 0 flags of the SC0MD0 register are changed, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register may be incremented.

Enabling the start condition drives the SBO0 pin high for a fixed time interval (1/2 the clock source cycle) after the transmission is completed. If the start condition is disabled, the SBO0 pin will remain at the value of the of the last data bit.

If the SC0IOM flag of the SC0MD3 register is set for a pin connection, the SBI0 pin can be used as a port. The SBO0 pin receives data during the input mode and transmits data during the output mode.

After the transfer is complete, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register will be changed. Except in an 8-bit transfer, reset the transfer bit count at the time of the next transmission.

The SC0LNG2 to 0 flags change at the opposite edge of the transmit data output edge.

When switching from transmission to reception, set the SC0SBOS flag of the SC0MD3 register to "0" and then set the SC0SBIS flag to "1." Do not change both of these flags at the same time.

The SC0SBTS flag of the SC0MD3 register must be set to "1" before the SC0SBOS flag of the SC0MD3 register is set to "1."

Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.

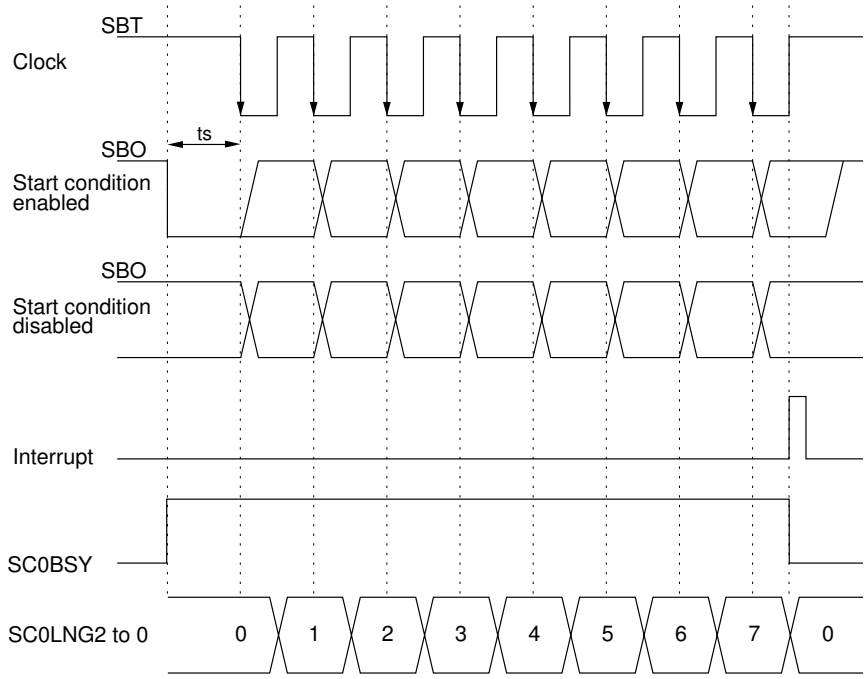


Figure 5-2-1 Synchronous Serial Interface Transmission Timing (falling edge)

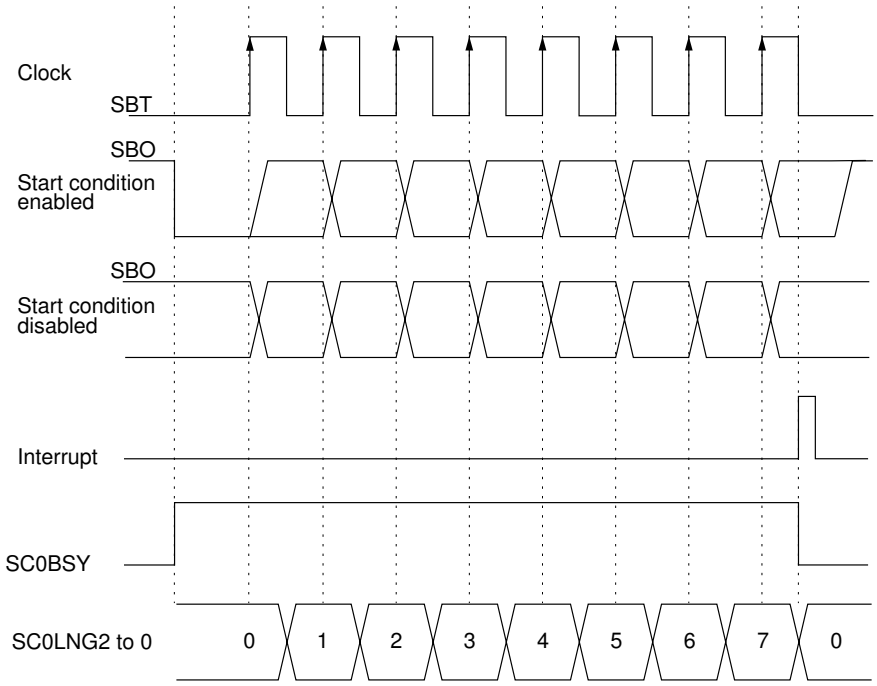


Figure 5-2-2 Synchronous Serial Interface Transmission Timing (rising edge)

■ Reception

(1) Select the synchronous serial interface by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "0."

(2) Select the transfer bit count with the SC0LNG2 to 0 flags of the serial interface 0 mode register 0 (SC0MD0). The transfer bit count can be set as 1 to 8 bits.

When the serial port is enabled and the SC0CE1 to 0 flags of the SC0MD0 register are changed, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register may by incremented.

(3) Specify whether the start condition is enabled or disabled with the SC0STE flag of the SC0MD0 register.

(4) Specify the first bit to be transferred (MSB first or LSB first) with the SC0DIR flag of the SC0MD0 register.

(5) Select the valid edge of the clock signal with the SC0CE1 to 0 flags of the SC0MD0 register.

[☞ Section 5-2-3, "Serial Interface Transfer Timing"]

(6) When the clock source is an internal clock:
- Select the clock source with the SC0CK1 to 0 flags of serial interface 0 mode register 1 (SC0MD1).
- Set the SC0CKM flag of the SC0MD1 register to specify whether or not the clock source frequency will be divided by 8.
- Select serial clock pin operation by setting the SC0SBTS flag of the serial interface 0 mode register 3 (SC0MD3) to "1."
- Set the SC0SBTM flag of the SC0MD3 register.
- Set bit 2 of the port 0 direction control register (P0DIR) to the output mode (P02/SBT0 output mode).
- If necessary, set bit 2 of the port 0 pull-up resistor control register (P0PLU) to add the pull-up resistor.

When the clock source is an external clock (SBT0 pin input):
- Set bit 2 of the P0DIR register to the input mode.
- If necessary, set bit 2 of the P0PLU register.

If the start condition is enabled, the SC0LNG2 to 0 flags of the SC0MD0 register will be cleared when the start condition is received. In this case, the receive bit count is fixed at 8 bits.

The SC0SBTS flag of the SC0MD3 register must be set to "1" before setting the SC0SBIS flag of the SC0MD3 register to "1."

(7) Select the SC0IOM flag of the SC0MD3 register.

(8) Select serial communication by setting the SC0SBIS flag of the SC0MD3 register to "1." (Reception data wait.)

If the internal clock is selected as the clock source, after setting the SC0SBIS flag of the SC0MD3 register to "1," write dummy data to the SC0TRB register. If there is to be another reception, write dummy data again to the SC0TRB register.

(9) When the serial reception begins, the SC0BSY flag of the serial interface 0 control register (SC0CTR) is set to "1," indicating that a serial transfer is in progress.

(10) When the serial reception is complete, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of the SC0MD1 register is set to "1."

The SC0LNG2 to 0 flags change at the opposite edge of the transmit data output edge.

Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.

After the transfer is complete, the transfer bit count in the SC0LNG2 to 0 flags of the SC0MD0 register will be changed. Except in an 8-bit transfer count, reset the transfer bit count at the time of the next reception.

When switching from reception to transmission, set the SC0SBIS flag of the SC0MD3 register to "0" and then set the SC0SBOS flag to "1." Do not change both of these flags at the same time.

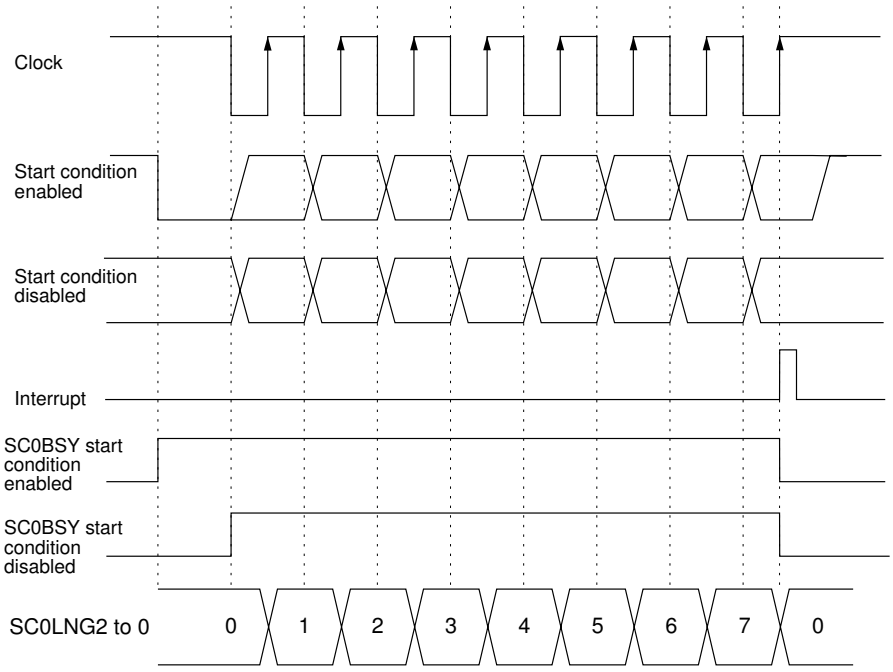


Figure 5-2-3 Synchronous Serial Interface Reception Timing
(reception at rising edge)

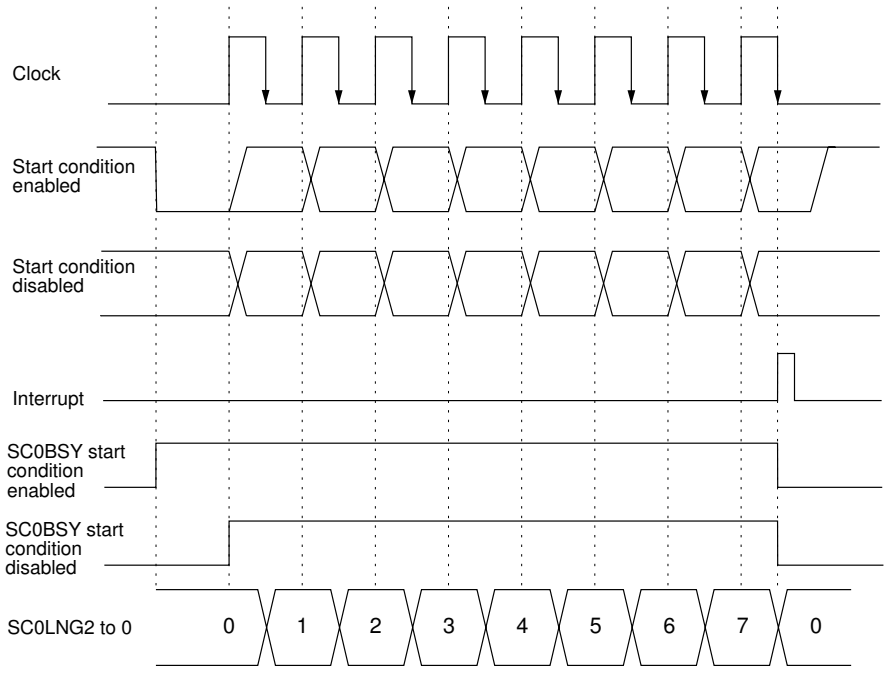
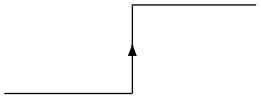
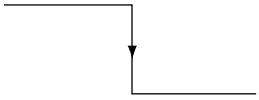
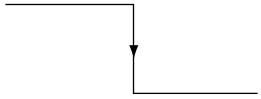
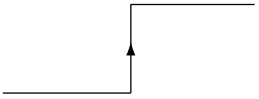
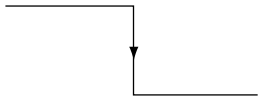
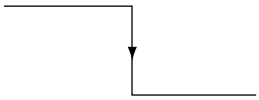
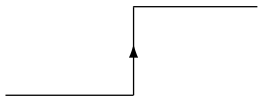
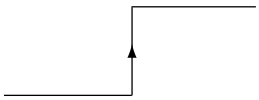


Figure 5-2-4 Synchronous Serial Interface Reception Timing
(reception at falling edge)

5-2-3 Serial Interface Transfer Timing

Serial interface 0 uses the SC0CE0 and SC0CE1 flags of serial interface 0 mode register 0 (SC0MD0), to control the edge at which transmission data is output and the edge at which reception data is input.
During transmission, when the SCnCE1 flag is "0," data output is synchronized to the falling edge of the clock.
During reception, when the SCnCE0 flag is "0," data reception is synchronized to the opposite polarity edge of the transmit data edge. When the SCnCE0 flag is "1," data reception is synchronized to the same polarity edge as the transmit data edge.

Table 5-2-1 Serial Data Input Edge and Output Edge (serial interface 0)

SC0CE0	SC0CE1	Receive Data Input Edge	Transmit Data Output Edge
0	0		
0	1		
1	0		
1	1		

When serial interface 0 is used for simultaneous transmission and reception, set the SCnCE0 and SCnCE1 flags of the SCnMD0 register to "00" or "01", so that the reception data input edge is opposite in polarity to the transmit data output edge. Also, the polarity of the reception data input edge is opposite polarity of the transmit data output edge of the other device.

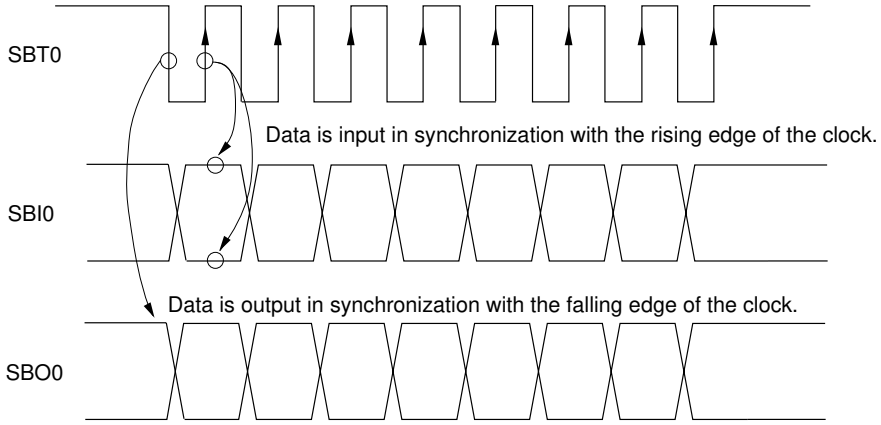


Figure 5-2-5 Synchronous Serial Transmit/Receive Timing
(data is received at the rising edge and transmitted at the falling edge)

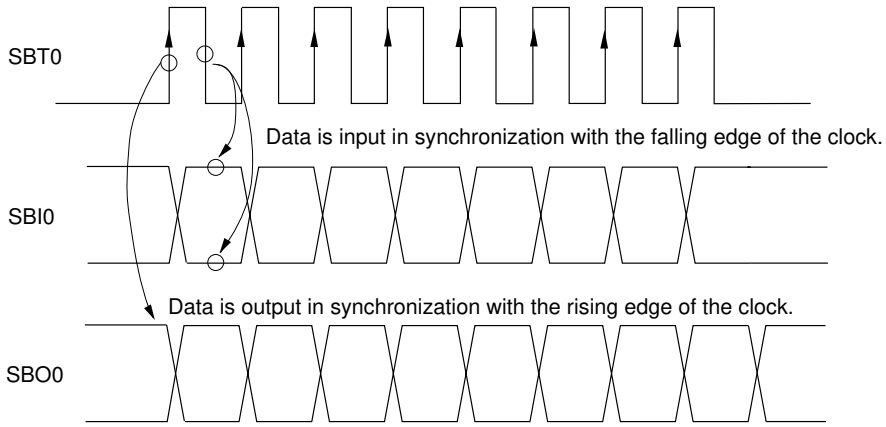


Figure 5-2-6 Synchronous Serial Transmit/Receive Timing
(data is received at the falling edge and transmitted at the rising edge)

5-3 Half-duplex UART Serial Interface

5-3-1 Overview

Setup and operation of UART transmission and reception are described below.

5-3-2 Setup and Operation

■ Transmission

(1) Select UART by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "1."

(2) Specify the first bit to be transferred (MSB first or LSB first) with the SC0DIR flag of the serial interface 0 mode register 0 (SC0MD0).

(3) Select the valid edge of the clock signal with the SC0CE1 to 0 flags of the SC0MD0 register.

(4) Select the clock source with the SC0CK1 to 0 flags of serial interface 0 mode register 1 (SC0MD1).

(5) Set the SC0CKM flags of the SC0MD1 register to "1" to divide the clock source frequency by 8.

(6) Set the SC0NPE flag of the serial interface 0 mode register 2 (SC0MD2) to enable or disable parity.

When the serial port is enabled and the SC0CE1 to 0 flags of the SC0MD0 register are toggled, the transfer bit count may change.

The TXD pin goes to a high level after transmission is complete.

Setting the SC0FM flag of the SC0MD2 register to frame mode automatically sets the SC0LNG2 to 0 flags of the SC0MD0 register.

After the transfer is complete, the SC0LNG2 to 0 flags of the SC0MD0 register are automatically set with the transfer bit count.

Set the SC0CKM flag of the SC0MD1 register to "1" to divide the clock source frequency by 8.

Serial interface 0 begins operation when the SC0SBOS flag or the SC0SBIS flag is set to "1." Set the SC0SBOS flag or the SC0SBIS flag after all conditions have been set.

(7) If parity is enabled by the SC0NPE flag of the SC0MD2 register, set the SC0PM1~0 flags of the SC0MD2 register to specify the added parity bit.

(8) Set the SC0FM1 to 0 flags of the SC0MD2 register to specify the frame mode.

(9) Set the SC0BRKE flag of the SC0MD2 register to control break status transmission.

(10) Select the SC0SBOM flag of the SC0MD3 register.

(11) Select the SC0IOM flag of the SC0MD3 register.

(12) Set bit 0 of the port 0 direction control register (P0DIR) to the output mode.

(13) Select serial communication by setting the SC0SBOS flag of the SC0MD3 register to "1."

(14) Set transmit data to serial interface 0 transmit/receive shift register (SC0TRB). This will start the serial transmission.

(15) When the serial transmission begins, the SC0BSY flag of the SC0CTR register is set to "1," indicating that a serial transfer is in progress.

(16) When the serial transmission is complete, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of the SC0MD1 register is cleared to "0."

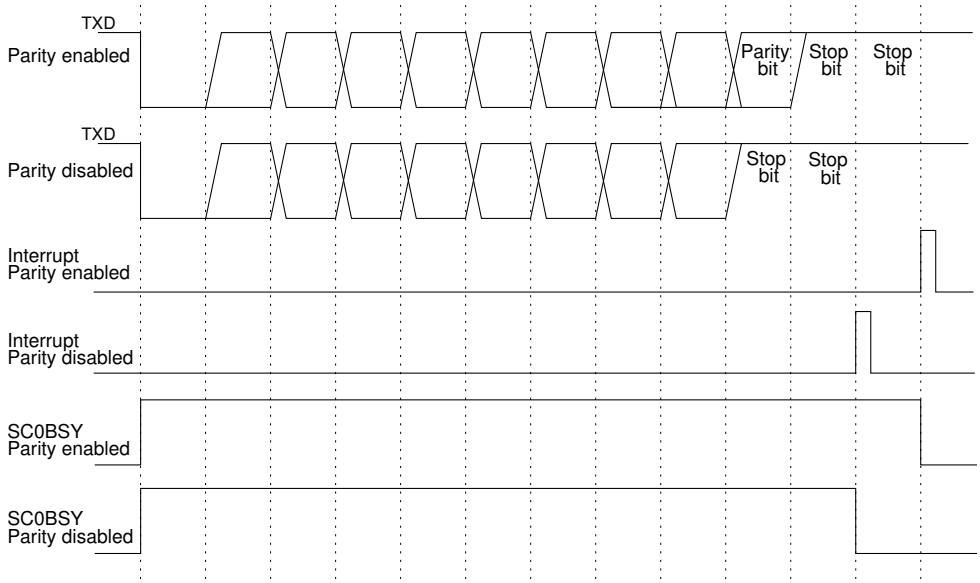


Figure 5-3-1 UART Transmission Timing

■ Reception

(1) Select UART by setting the SC0CMD flag of the serial interface 0 control register (SC0CTR) to "1."
(2) Specify the first bit to be transferred (MSB first or LSB first) with the SC0DIR flag of the serial interface 0 mode register 0 (SC0MD0).
(3) Select the valid edge of the clock signal with the SC0CE1 to 0 flags of the SC0MD0 register.
(4) Select the clock source with the SC0CK1~0 flags of serial interface 0 mode register 1 (SC0MD1).
(5) Set the SC0CKM flags of the SC0MD1 register to "1" to divide the clock source frequency by 8.
(6) Set the SC0NPE flag of the serial interface 0 mode register 2 (SC0MD2) to enable or disable parity.
(7) If parity is enabled by the SC0NPE flag of the SC0MD2 register, set the SC0PM1 to 0 flags of the SC0MD2 register to specify the added parity bit.
(8) Set the SC0FM1 to 0 flags of the SC0MD2 register to specify the frame mode.
(9) Select the SC0IOM flag of the SC0MD3 register.
(10) When the SC0IOM flag of the SC0MD3 register is specified that the pin is independent, set bit 1 of the port 0 direction control register (P0DIR) to the input mode.
(11) Set bit 0 of the port 0 pull-up resistor control register (P0PLU).
(12) Select serial communication by setting the SC0SBIS flag of the SC0MD3 register to "1."
(13) When the serial transmission begins, the SC0BSY flag of the SC0CTR register is set to "1," indicating that a serial transfer is in progress.
(14) When the serial transmission is complete, the SC0BSY flag of the SC0CTR register is cleared to "0" and the SC0 transfer complete interrupt request flag is set to "1." The SC0TRI flag of the SC0MD1 register is cleared to "1."

When the serial port is enabled and the SC0CE1 to 0 flags of the SC0MD0 register are toggled, the transfer bit count may change.

The TXD pin goes to a high level after reception is complete.

Serial interface 0 begins operation when the SC0SBOS or SC0SBIS flag is set to "1." Set the SC0SBOS or SC0SBIS flag after all conditions have been set.

One machine cycle after the stop bit has been received, the start condition will no longer be accepted. Therefore, consecutive reception must be performed carefully.

Setting the SC0FM flag of the SC0MD2 register to frame mode automatically sets the SC0LNG2 to 0 flags of the SC0MD0 register.

After the transfer is complete, the SC0LNG2 to 0 flags of the SC0MD0 register are automatically set with the transfer bit count.

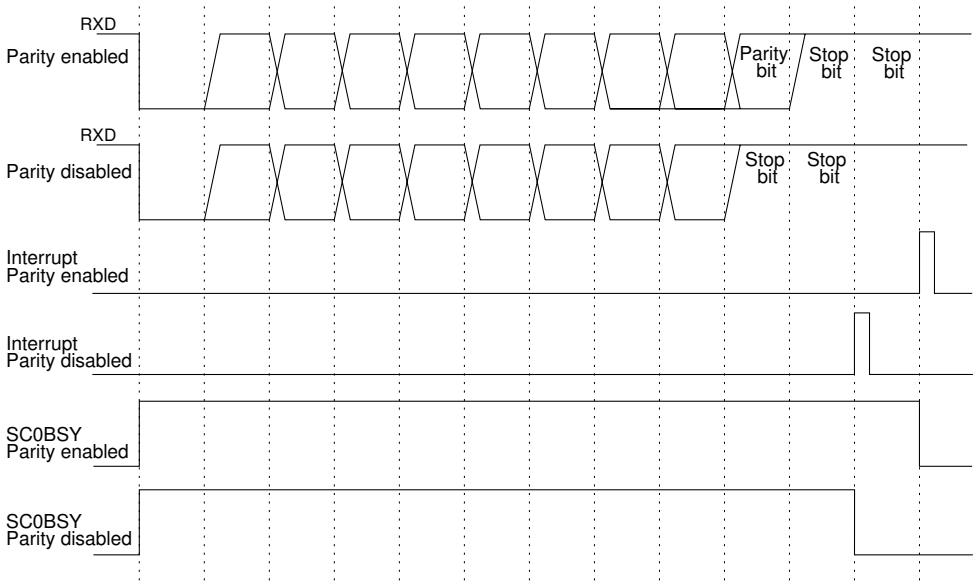


Figure 5-3-2 UART Reception Timing

5-3-3 How to Use the Baud Rate Timer

Refer to the following when using the baud rate timer to set the UART transfer speed.

(1) Specifying the timer clock source
The clock source is specified by the TM3CKS3 to 1 flags of the timer 3 mode register (TM3MD).

(2) Setting the compare register
The compare register value is set in the timer 3 compare register (TM3OC). This set value is computed according to the following formula:

overflow period = (compare register set value + 1) × timer clock period

baud rate = 1/(overflow period × 2 × 8)
↑ SC0MD1(SC0CKM)

compare register set value = timer clock frequency/(baud rate × 2 × 8) – 1

Table 5-3-1 UART Transfer Rate

fosc (MHz) \ Transfer Speed (bps)		300		1200		2400		4800		9600		19200	
		Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value	Set Value	Calculated Value
4.0	fosc	—	—	208	1202	104	2403	52	4807	26	9615	13	19230
	fs/4	104	300	—	—	—	—	—	—	—	—	—	—
	fs/16	—	—	—	—	—	—	—	—	—	—	—	—
4.19	fosc	—	—	218	1201	109	2402	55	4761	27	9699	—	—
	fs/4	109	300	—	—	—	—	—	—	—	—	—	—
	fs/16	—	—	—	—	—	—	—	—	—	—	—	—
8.0	fosc	—	—	—	—	208	2404	104	4807	52	9615	26	19230
	fs/4	208	300	52	1201	—	—	—	—	—	—	—	—
	fs/16	—	—	—	—	—	—	—	—	—	—	—	—
8.38	fosc	—	—	—	—	218	2403	109	4805	55	9523	27	19398
	fs/4	218	300	55	1190	—	—	—	—	—	—	—	—
	fs/16	—	—	—	—	—	—	—	—	—	—	—	—
12.0	fosc	—	—	—	—	—	—	156	4808	78	9615	39	19230
	fs/4	—	—	78	1202	39	2403	—	—	—	—	—	—
	fs/16	78	300	—	—	—	—	—	—	—	—	—	—
16.0	fosc	—	—	—	—	—	—	208	4808	104	9615	52	19230
	fs/4	—	—	104	1202	52	2404	—	—	—	—	—	—
	fs/16	104	300	—	—	—	—	—	—	—	—	—	—
16.76	fosc	—	—	—	—	—	—	218	4805	109	9610	55	19045
	fs/4	—	—	109	1201	55	2381	—	—	—	—	—	—
	fs/16	109	300	—	—	—	—	—	—	—	—	—	—
20.0	fosc	—	—	—	—	—	—	—	—	130	9615	65	19231
	fs/4	—	—	130	1202	65	2404	33	4735	—	—	—	—
	fs/16	130	300	—	—	—	—	—	—	—	—	—	—

Set the values from this table (minus 1) in the compare register.

Example:
The timer 3 clock source is fs/4 (fosc = 8MHz) and a baud rate of 300 bps is desired.

Since fs=fosc/2,

compare register set value = $(8 \times 10^6/2/4)/(300 \times 2 \times 8) - 1$
=207
= X'CF'

5-4 Serial Interface Control Registers

5-4-1 Overview

7 registers control the serial interface. See table 5-4-1.

Table 5-4-1 Serial Interface Registers

Name	Address	R/W	Function
SC0MD0	X'03F50'	R/W	Serial interface 0 mode register 0
SC0MD1	X'03F51'	R/W	Serial interface 0 mode register 1
SC0MD2	X'03F52'	R/W	Serial interface 0 mode register 2
SC0MD3	X'03F53'	R/W	Serial interface 0 mode register 3
SC0CTR	X'03F54'	R/W	Serial interface 0 control register
SC0TRB	X'03F55'	W	Serial interface 0 transmit/receive shift register
SC0RXB	X'03F56'	R	Serial interface 0 receive data buffer

5-4-2 Transmit/Receive Shift Registers, Receive Data Buffer

(1) Serial interface 0 transmit/receive shift register (SC0TRB)

This 8-bit, writable register shifts the transmission data and the reception data. The direction of transfer can be specified as LSB first or MSB first.

	7	6	5	4	3	2	1	0	
SC0TRB	SC0TRB7	SC0TRB6	SC0TRB5	SC0TRB4	SC0TRB3	SC0TRB2	SC0TRB1	SC0TRB0	(at reset: undefined)

Figure 5-4-1 Serial Interface 0 Transmit/Receive Shift Register
(SC0TRB: X'03F55', W)

(2) Serial interface 0 receive data buffer (SC0RXB)

	7	6	5	4	3	2	1	0	
SC0RXB	SC0RXB7	SC0RXB6	SC0RXB5	SC0RXB4	SC0RXB3	SC0RXB2	SC0RXB1	SC0RXB0	(at reset: undefined)

Figure 5-4-2 Serial Interface 0 Receive Data Buffer
(SC0RXB: X'03F56', R)

5-4-3 Serial Interface Mode Registers

(1) Serial interface 0 mode register (SC0MD0)

	7	6	5	4	3	2	1	0
SC0MD0	–	SC0CE0	SC0CE1	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0

(at reset: -00XX000)

SC0LNG2	SC0LNG1	SC0LNG0	Transfer bit count
0	0	0	8 bit
		1	7 bit
	1	0	6 bit
		1	5 bit
1	0	0	4 bit
		1	3 bit
	1	0	2 bit
		1	1 bit

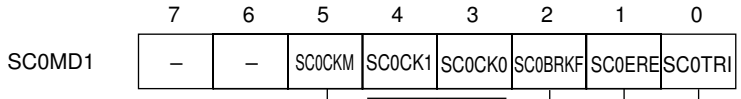
SC0STE	Selection of synchronous serial start condition
0	Disable start condition
1	Enable start condition

SC0DIR	First bit to be transferred
0	MSB first
1	LSB first

SC0CE0	SC0CE1	Receive data input edge	Transmit data output edge
0	0	Rising	Falling
0	1	Falling	Rising
1	0	Falling	Falling
1	1	Rising	Rising

Figure 5-4-3 Serial Interface 0 Mode Register 0 (SC0MD0: X'03F50', R/W)

(2) Serial interface 0 mode register 1 (SC0MD1)



7	6	5	4	3	2	1	0
SC0MD1	–	–	SC0CKM	SC0CK1	SC0CK0	SC0BRKF	SC0ERE	SC0TRI

(at reset: --X00000)

SC0TRI	Transmit/receive interrupt request flag
0	Transmit interrupt request
1	Receive interrupt request

SC0ERE	Error monitor
0	No error
1	Error

SC0BRKF	Break status receive monitor
0	Data
1	Break

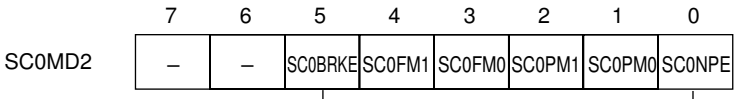
SC0CK1	SC0CK0	Clock source
0	0	fs/2
0	1	fs/4
1	0	fs/16
1	1	BC3×1/2(1/2 of timer 3 overflow)

SC0CKM	Divide clock frequency by 8
0	Do not divide by 8
1	Divide by 8

An external clock can be selected as the clock source by setting the SBT0 pin to the input mode.

Figure 5-4-4 Serial Interface 0 Mode Register 1 (SC0MD1: X'03F51', R/W)

(3) Serial interface 0 mode register 2 (SC0MD2)



SC0NPE	Parity enable
0	Parity enabled
1	Parity disabled

SC0PM1	SC0PM0	Added bit specification	
		Transmission	Reception
0	0	Normally add 0	Check for 0
	1	Normally add 1	Check for 1
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC0FM1	SC0FM0	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bits
	1	8 data bits + 2 stop bits

SC0BRKE	Break status transmit control
0	Data
1	Break

Figure 5-4-5 Serial Interface 0 Mode Register 2 (SC0MD2: X'03F52', R/W)

(4) Serial interface 0 mode register 3 (SC0MD3)

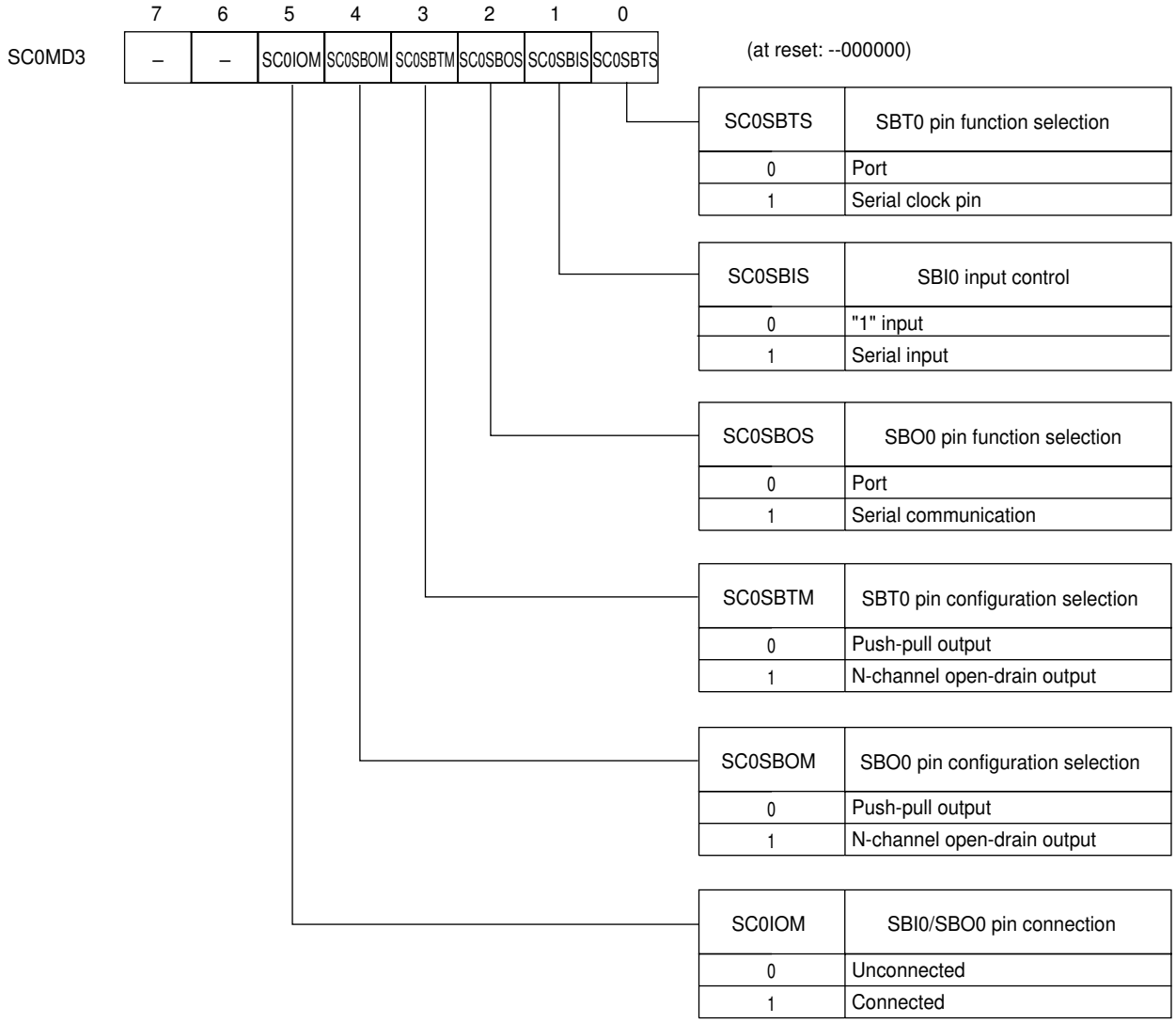


Figure 5-4-6 Serial Interface 0 Mode Register 3 (SC0MD3: X'03F53', R/W)

5-4-4 Serial Interface Control Register

(1) Serial interface 0 control register (SC0CTR)

	7	6	5	4	3	2	1	0	
SC0CTR	SC0BSY	SC0CMD	–	–	SC0FEF	SC0PEK	SC0ORE	–	(at reset: 00XX000X)

SC0ORE	Overrun error detection
0	No Error
1	Error

SC0PEK	Parity error detection
0	No Error
1	Error

SC0FEF	Framing error detection
0	No Error
1	Error

SC0CMD	Synchronous serial/ UART selection
0	Synchronous serial
1	UART

SC0BSY	Serial bus status
0	Other use
1	Serial transmission in progress

Figure 5-4-7 Serial Interface 0 Control Register (SC0CTR: X'03F54', R)
(R/W available with SC0CMD only)

Chapter 6 A/D Conversion Functions

6

6-1 Overview

The MN101C117 has an internal A/D converter with 10-bit resolution. A sample-and-hold circuit is contained on-chip and software can switch the analog input between channels 0 to 7 (AN0 to AN7).
When the A/D converter is stopped, power consumption can be reduced by turning off the internal ladder resistors.

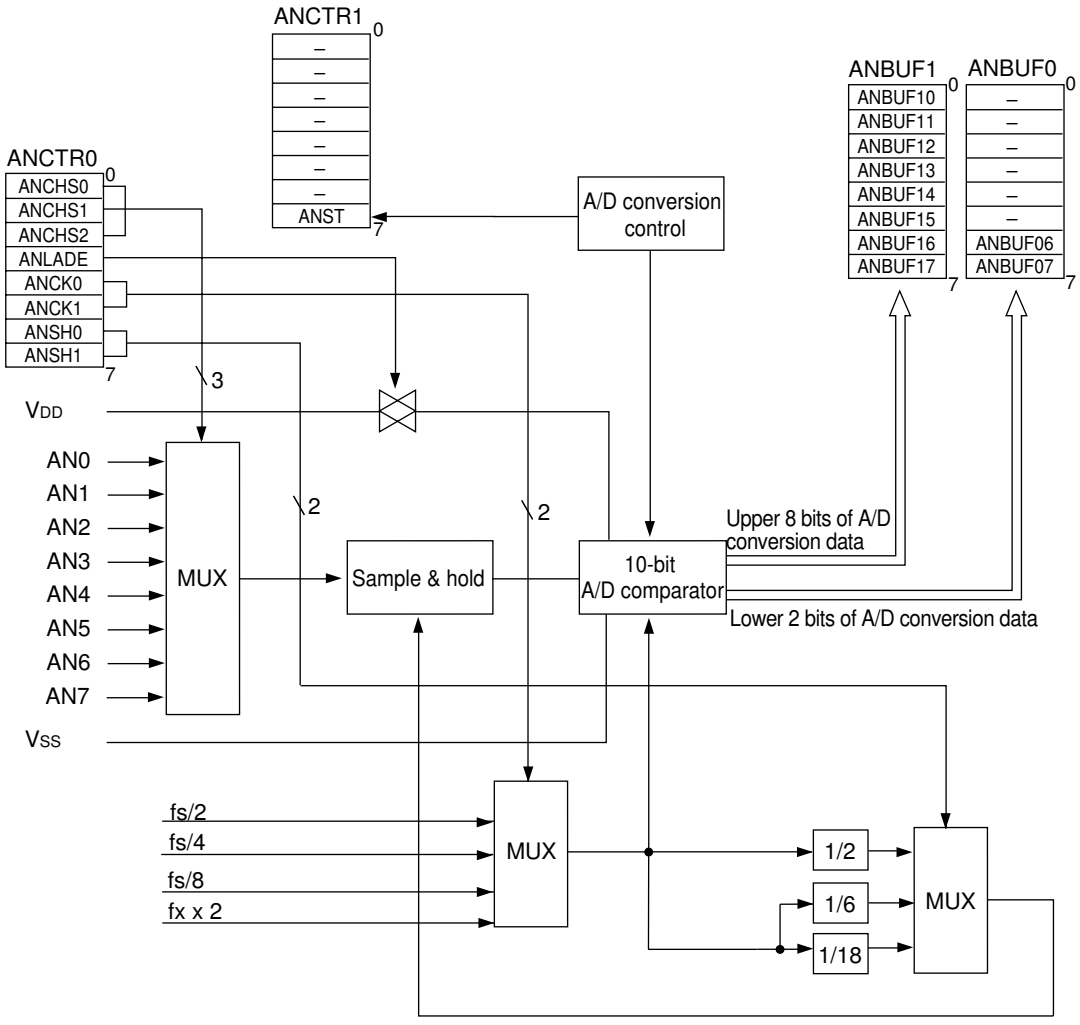


Figure 6-1-1 A/D Converter Block Diagram

6-2 A/D Conversion

The procedures for operating the A/D conversion circuit are listed below.

(1) Set the ANCHS2 to ANCHS0 flags of A/D control register 0 (ANCTR0) to specify one of pins AN7 to AN0 (PA7 to PA0) as the analog input.
(2) Set the ANCK1 and ANCK0 flags of A/D control register 0 to select the A/D conversion clock. Make this setting such that the period of the conversion clock (T_{AD}), which is based on the oscillator, is greater than 800ns.
(3) With the ANSH1 and ANSH0 flags of A/D control register 0, set the sample-and-hold time. Select a value for the sample and hold time that is suitable for the analog input impedance.
(4) Set the ANLADE flag of A/D control register 0 to "1" so that current flows through the ladder resistors and the A/D converter is on standby.
Note: Steps 1 to 4 above may performed all at the same time.
(5) Set the ANST flag of A/D control register 1 (ANCTR1) to "1" to start the A/D conversion.
(6) After the sample-and-hold time set in step 3, the sampled A/D conversion data is sequentially compared to determine its value beginning with the MSB.
(7) When the A/D conversion is complete, the ANST bit is cleared to "0" and conversion results are stored in A/D buffers (ANBUF0, 1). At the same time, an A/D complete interrupt request (ADIRQ) is generated.

Start the A/D conversion after the current flowing through the ladder resistors stabilizes. The time constant calculated time from the ladder resistance (max. 80 kΩ) and the external bypass capacitor connected between Vdd and Vss should be used as the criteria for the wait time.

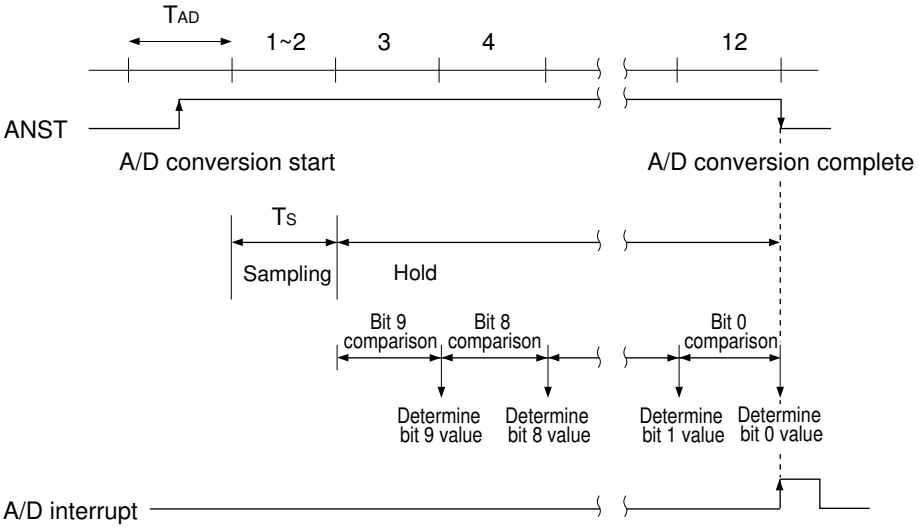
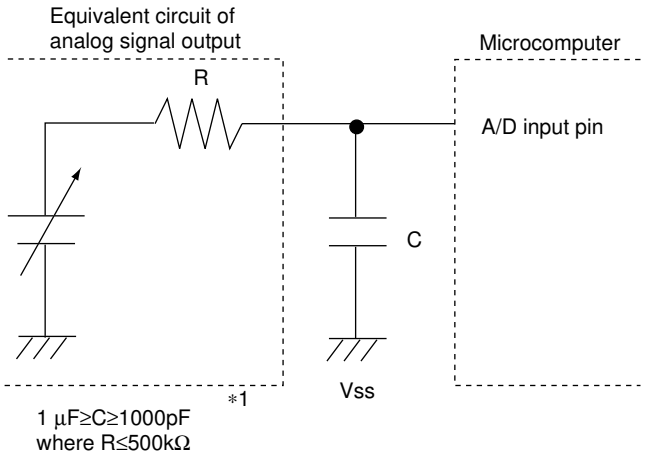


Figure 6-2-1 A/D Conversion Timing

The following items must be implemented to maintain the accuracy of the A/D converter:

1. Use a maximum input pin impedance, R, of 500kΩ*1 with an external capacitor, C, that is minimum 1,000pF and maximum 1μF*1.
2. Take the RC time into consideration when setting the A/D conversion interval.
3. Changing the output level of the microcomputer or switching peripheral circuitry on or off when the A/D converter is in use may cause the analog input pin or current pin to fluctuate resulting in a loss of precision. During setup and evaluation, verify the waveform of the analog input pin.



*1 These values are reference values.

Figure 6-2-2 Recommended Circuit When Using A/D Conversion

6-3 A/D Converter Control Registers

6-3-1 Overview

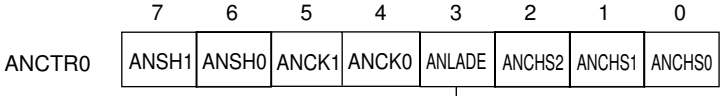
Four registers control the A/D converter. See table 6-3-1.

Table 6-3-1 A/D Converter Control Registers

Name	Address	R/W	Function
ANCTR0	X'03F90'	R/W	A/D control register 0
ANCTR1	X'03F91'	R/W	A/D control register 1
ANBUF0	X'03F92'	R	A/D buffer 0
ANBUF1	X'03F93'	R	A/D buffer 1

6-3-2 A/D Control Register (ANCTR)

This readable and writable 8-bit register controls the operation of the A/D converter.



ANCHS2	ANCHS1	ANCHS0	Analog input selection
0	0	0	AN0
		1	AN1
	1	0	AN2
		1	AN3
1	0	0	AN4
		1	AN5
	1	0	AN6
		1	AN7

ANLADE	A/D ladder resistor control
0	A/D ladder resistors off
1	A/D ladder resistors on

ANCK1	ANCK0	A/D conversion clock selection∗1
0	0	fs/2
	1	fs/4
1	0	fs/8
	1	Use prohibited

ANSH1	ANSH0	Sample and hold time setting∗2
0	0	$T_{AD} \times 2$
	1	$T_{AD} \times 6$
1	0	$T_{AD} \times 18$
	1	Use prohibited

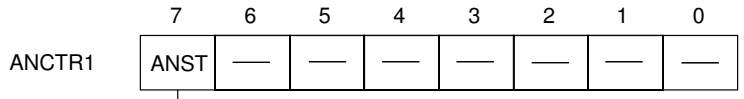
(1) A/D control register 0 (ANCTR0)

∗1: Specify that where the period of the A/D conversion clock is greater than 800ns.

∗2: Sample-and-hold time is determined by the analog input impedance. T_{AD} indicates the period of the A/D conversion clock.

Figure 6-3-1 A/D Control Register 0 (ANCTR0: X'03F90', R/W)

(2) A/D conversion control register 1 (ANCTR1)



ANST	A/D conversion status
0	A/D conversion completed or stopped
1	A/D conversion started or in progress

Figure 6-3-2 A/D Control Register 1 (ANCTR1: X'03F91', R/W)

6-3-3 A/D Buffers (ANBUF)

These read-only registers store the A/D conversion results.

(1) A/D buffer 0 (ANBUF0)

This register stores the lower 2 bits of the A/D conversion results.

	7	6	5	4	3	2	1	0	
ANBUF0	ANBUF07	ANBUF06	—	—	—	—	—	—	(at reset: XX------)

Figure 6-3-3 A/D Buffer 0 (ANBUF0: X'03F92', R)

(2) A/D buffer 1 (ANBUF1)

This register stores the upper 8 bits of the A/D conversion results.

	7	6	5	4	3	2	1	0	
ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	(at reset: XXXXXXXX)

Figure 6-3-4 A/D Buffer 1 (ANBUF1: X'03F93', R)

Chapter 7 AC Zero-Cross Circuit/Noise Filter

7

7-1 Overview

The P21/SENS pin is the input pin for the AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level, and a low level at all other times.

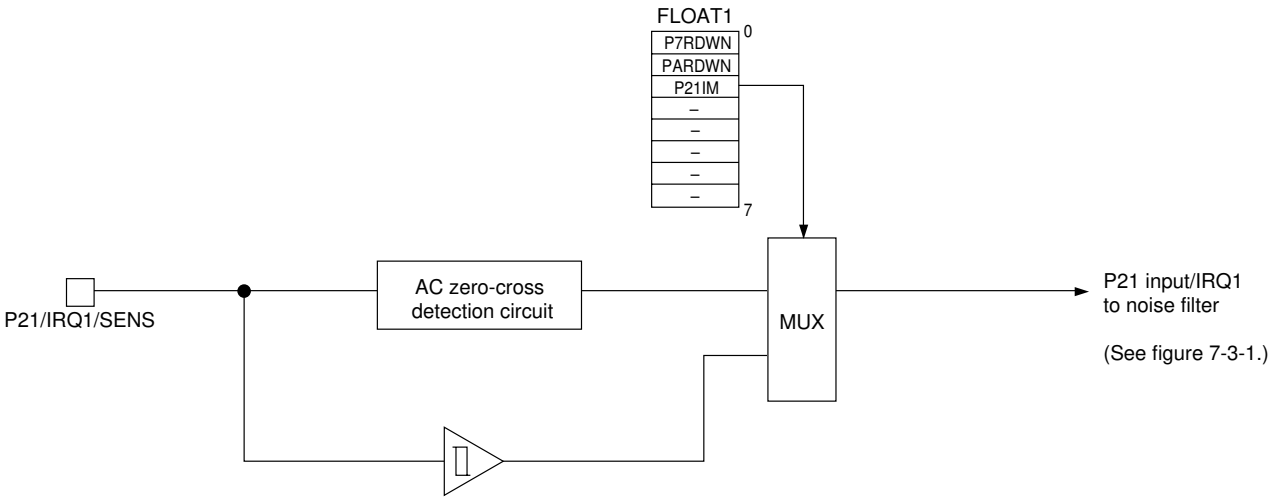


Figure 7-1-1 P21 Input Circuit Block Diagram

7-2 AC Zero-Cross Circuit Operation

7-2-1 Setup and Operation

Settings for zero-cross circuit operation are listed below.

(1) Set the REDG1 flag of the IRQ1ICR register to select the valid edge for IRQ1.
(2) Set the NF1EN and NF1CK1 to 0 flags of the NFCTR register to set the noise filter and its sampling clock.
(3) With the P21IM flag of the FLOAT1 register, set the P21 pin to zero-cross detection.
(4) An IRQ1 interrupt is generated by the falling edge or the rising edge of AC zero-cross detection output.

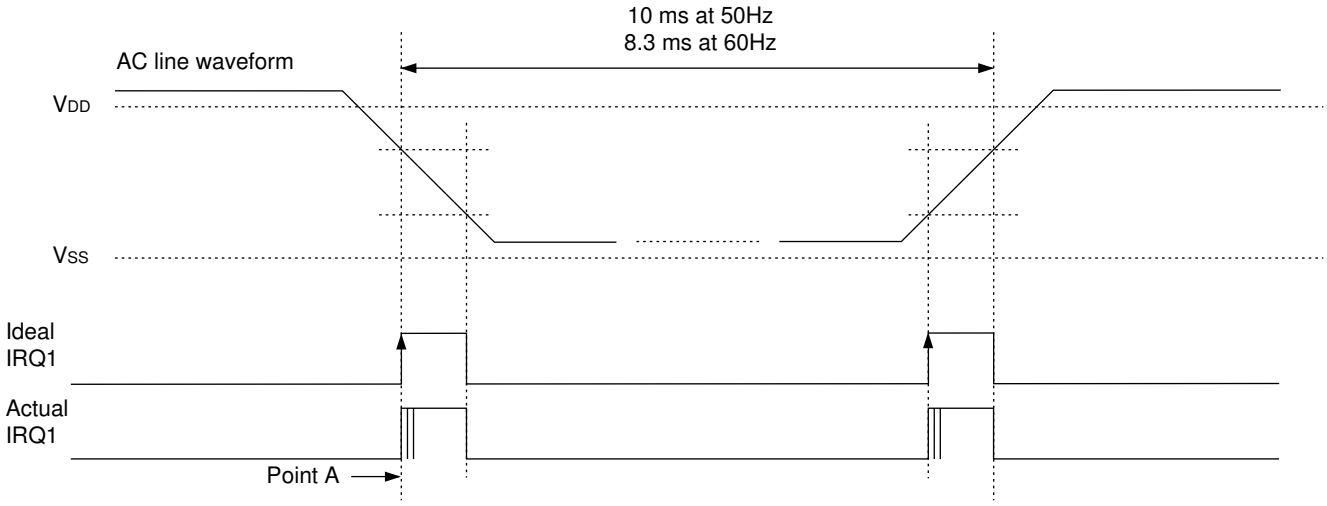


Figure 7-2-1 AC Line Waveform and IRQ Generation Timing

Actual IRQ interrupt requests will be generated multiple times. Therefore, the software must filter this signal before making any evaluations.

When noise filtering is selected for use, the amount of evaluation processing by the software will be reduced. However, if the OSC stops, a return from the backup mode will not be possible.

7-3 Noise Filter

7-3-1 Overview

External interrupt pins IRQ0 and IRQ1 contain noise filtering circuit. This circuitry can be used for remote control signal reception.

IRQ0: External interrupt 0

IRQ1: External interrupt 1

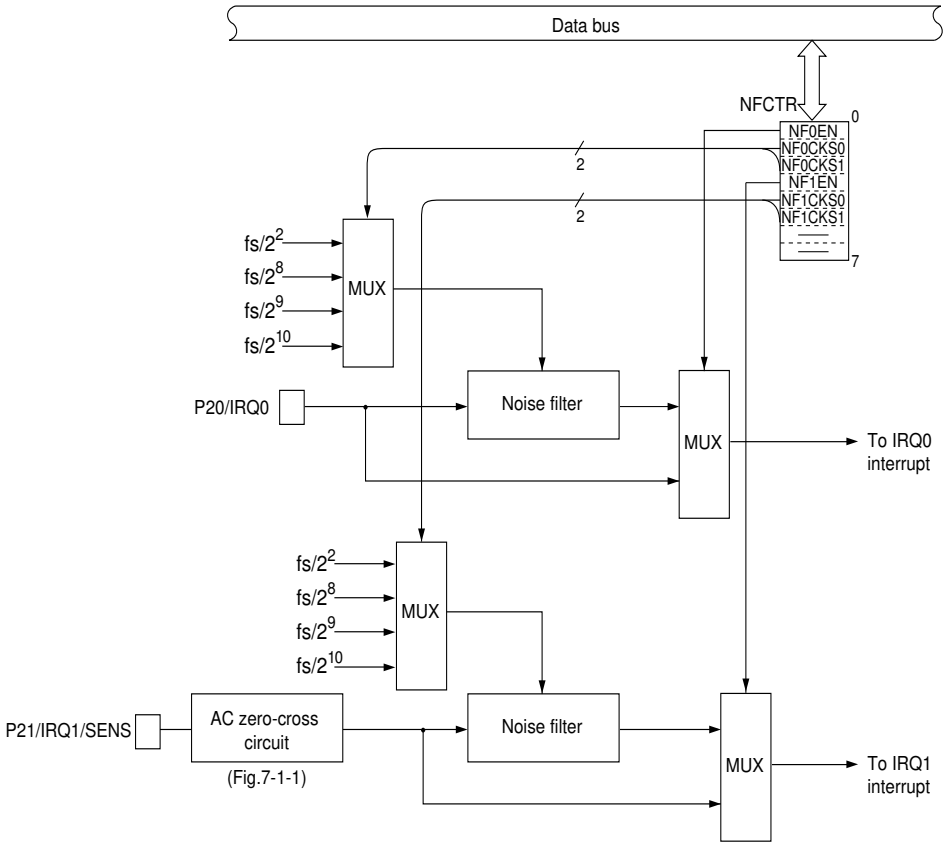


Figure 7-3-1 Noise Filtering Circuit Block Diagram

7-3-2 Example Input and Output Waveforms for Noise Filter

When the noise filter is used, the waveform input to the IRQ0 pin is sampled based on the clock specified by the NF0CKS0 and NF0CKS1 flags of the noise filter control register (NFCTR). The waveform input to the IRQ1 pin is also sampled based on the clock specified by the NF1CKS0 and NF1CKS1 flags. If the sampled level remains the same for 3 consecutive samples, it is sent the CPU; otherwise, the previous level is maintained.

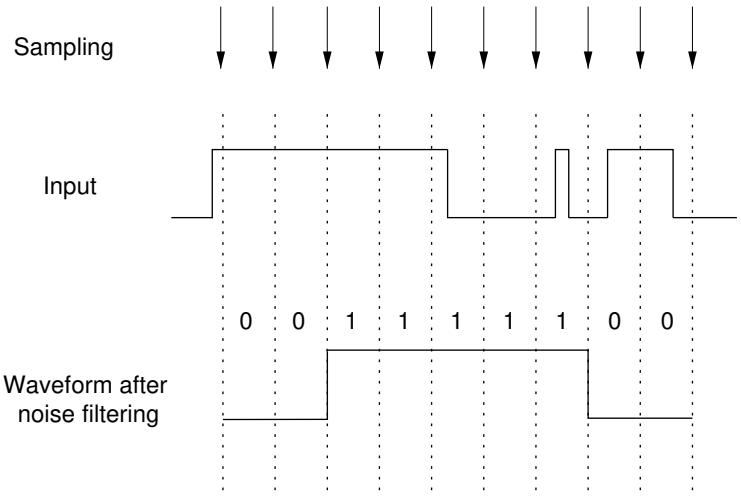


Figure 7-3-2 Noise Filter Input and Output Waveform Example

Noise filtering cannot be used in the STOP or HALT modes.

7-4 AC Zero-Cross Control Register

7-4-1 Overview

Four registers control the AC zero-cross circuit.

[☞ 2-4-3 "Interrupt Control Registers ■ External Interrupt Control Registers"]

[☞ 3-2-2 "I/O Port Control Registers ■ Pin Control Registers"]

Table 7-4-1 AC Zero-Cross Control Register

Name	Address	R/W	Function
IRQOICR	X'03FE2'	R/W	External interrupt control register 0
IRQ1ICR	X'03FE3'	R/W	External interrupt control register 1
FLOAT1	X'03F4B'	R/W	Pin control register 1
NFCTR	X'03F8A'	R/W	Noise filter control register

7-4-2 Noise Filter Control Register (NFCTR)

This 6-bit readable and writable register controls the noise filter.

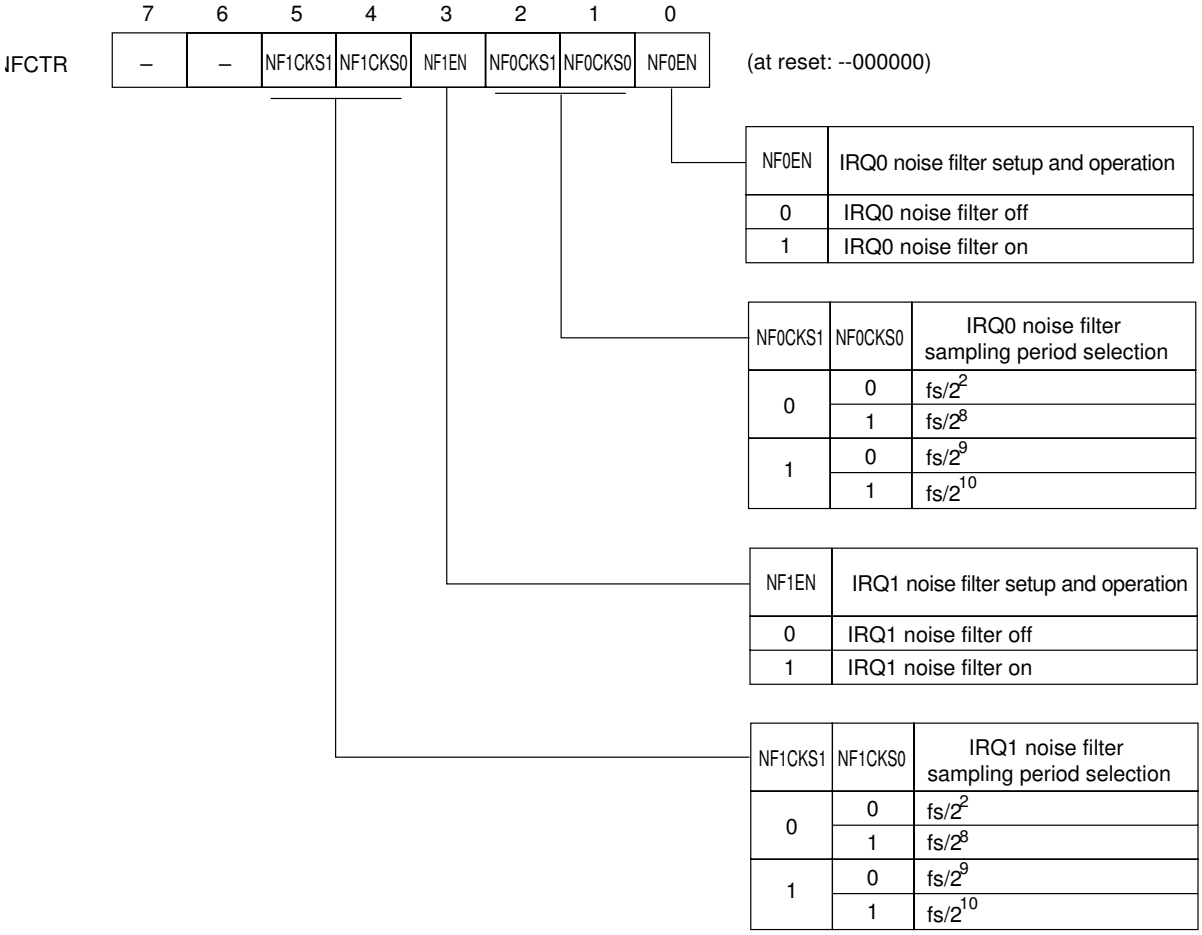


Figure 7-4-1 Noise Filter Control Register (NFCTR: X'03F8A', R/W)

Appendices

8

8-1 EPROM Versions

8-1-1 Overview

EPROM version is microcomputer which was replaced with the mask ROM of the MN101C11 with an electronically programmable 16-KB EPROM.

Because the MN101CP117**(**=DP,BF,HP) is sealed in plastic, once data is written to the internal PROM it cannot be erased.
Because the PX-AP101C11-SDC and PX-AP101C11-FBC are sealed in a ceramic package that has a window, written data can beerased by illumination with ultraviolet light. Plastic package uses a 42-pin shrink DIL package, 44-pin flat package, and 48-pin flat package. Ceramic packages uses a 42-pin shrink DIL package and 44-pin flat package.

Setting the EPROM version to EPROM mode, halts microcomputer functions, and the internal EPROM can be programmed. Refer to the EPROM mode pin diagram in figure 9-4-3 to 5.

The specification for writing to the internal EPROM are the same as for a general-purpose 256Kbit EPROM(Vpp=12.5V, tpw=0.2ms). Therefore, by replacing theEPROM Version's 42-pin socket with a special 28-pin socket adapter(supplied by Panasonic) having the same configuration as a normal EPROM, a general-purpose EPROM writer can be used to perform read and write operations.

The EPROM Version is described on the following items:
- Cautions on use of the internal EPROM
- Erasing written Data in Windowed Package(PX-AP101C11-SDC, PX-AP101C11-FBC)
- Characteristics of EPROM Versions
- Writing to the Microcomputer with Internal EPROM
- Cautions on operating a ROM writer
- Option bit
- Connections of a writing adaptor.

8-1-2 Cautions on Use

EPROM Versions differs from the MN101C11* in some of its electrical characteristics. The user should be aware of these differences.

(1) To prevent data from being erased by ultraviolet light after a program is written, affix seals impermeable to UV rays to the glass sections at the top and side sections of the CPU.
(PX-AP101C11-SDC, PX-AP101C11-FBC)

(2) Due to device characteristics of the MN101CP11XXX, a writing test cannot be performed on all bits. Therefore, storage of the written data cannot be guaranteed in some cases.

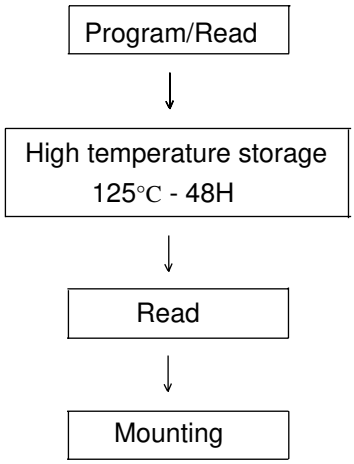
(3) When a program is written, verify that Vc power supply(6V) is connected before applying the Vpp power supply(12.5V). Disconnect the Vpp supply before disconnecting the Vcc supply.

(4) Vpp should never exceed 13.5V including overshoot.

(5) If a device is removed while a Vpp of +12.5V is applied, device reliability may be damaged.

(6) At $\overline{CE}$=VIL, do not change Vpp from VIL to +12.5V or from +12.5V to VIL.

(7) From the time after a program is written until just before mounting, storage at a high temperature is recommended.



8-1-3 Erasing Written Data in Windowed Packages (PX-AP101C11-SDC, PX-AP101C11-FBC)

In an internal EPROM with windowed packaging, data is erased("0" → "1") when UV light at 253.7nm permeates the window to irradiate the chip.

The recommended exposure is 10W · s/cm^2. This coverage can be achieved by using a commercial UV lamp positioned 2 to 3cm above the package for 15-20 minutes(when the illumination intensity of the package surface is12000μW/cm^2). Remove any filters attached to the lamp. By installing a mirrored reflector plate in the lamp, illumination intensity will increase by afactor of 1.4 to 1.8, decreasing the erasure time.

If the window becomes dirty with oil, adhesive, etc., UV light permeability will decrease, causing the erasure time to increase considerably. If this happens, clean with alcohol or another solvent that will not harm the package. The recommended above provides sufficient leeway, with several times the amount of time it takes to erase all the bits. However, this value will reliably erase data over all temperature and voltage ranges, and should not be altered. The level of illumination should be regularly checked and the lamp operation verified.

Erasure begins when EPROM is exposed to light with a wavelength shorter than 400nm. Since fluorescent light and sunlight have wavelengths in this range, exposure to these light sources for extended periods of time could cause inadvertant erasure. To prevent this, cover the window with an opaque label.

Data is not erased at wavelengths longer than 400 to 500nm. However, because of typical semiconductor characteristics, the circuit may malfunction if the chip is exposed to an extremely high illumination intensity. The chip will operate normally if this exposure is stopped. However, for areas where it is continuous, take necessary precautions.

8-1-4 Characteristics of EPROM Version

The MN101C11*(mask ROM version) and the Microcomputer with internal EPROM version have the following differences.

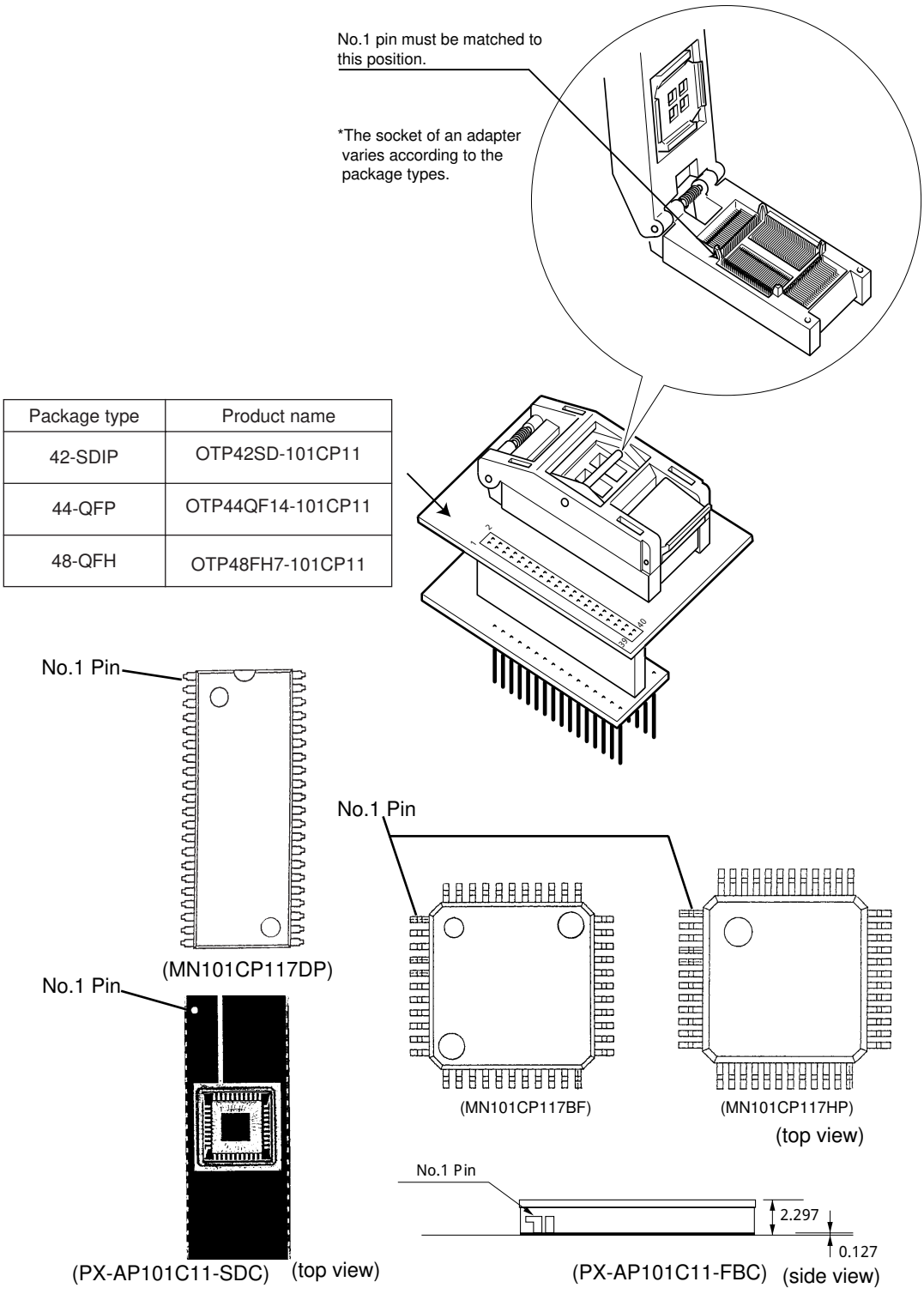
Table 8-1-1 Difference between MN101C*(Mask ROM version) and Internal EPROM version)

	MN101C11* (ROM ver.)	Internal EPROM version
Operating temperature	-40 to 85°C	-20 to 85°C
Operating voltage	4.5 to 5.5V (0.1µs/20MHz) 2.7 to 5.5v (0.25µs/8MHz) 2.0 to 5.5v (1.00µs/2MHz)	4.5 to 5.5V (0.1µs/20MHz) 2.7 to 5.5v (0.25µs/8MHz) 2.7 to 5.5v (1.00µs/2MHz)
Pin DC characteristics	Output current,input current and input judge level are the same.	
Hi-speed,low-speed oscillation start control,runaway detection period settup Package selection	ROM option Internal ROM final address data be used as option data. (Final address =X'07FFF)	EPROM option EPROM final address data be used as option data. (Final address=X'07FFF)

There are no other functional differences.

8-1-5 Writing to Microcomputer with Internal EPROM

■ Fit in the writing adapter and position the No.1 pin.



Package type	Product name
42-SDIP	OTP42SD-101CP11
44-QFP	OTP44QF14-101CP11
48-QFH	OTP48FH7-101CP11

Figure 8-1-1 Mount on the writing adapter and position of No.1 pin.

■ ROM writer Selection

The device names should be set up as listed below.

Table 8-1-2 Device selection

Equip. name	Vendor	Device name	Remarks
Pecker 30	Avarl Data	Hitachi 27C256	
1890A	Minato Electronics	Hitachi 27C256	
Lab Site	Data I/O	Hitachi 27C256	Do not run ID check and pin connection inspection.

The above settings are based on the standard samples.
When you use the other equipment than the ones listed, contact the nearest semiconductor design center.(Refer to the sales office table attached at the end of the manual.)

8-1-6 Cautions on Operating the ROM Writer

■ Cautions on operating the ROM writer

(1)The Vpp programming voltage for the EPROM versions is 12.5V. Programming with a 21-volt ROM writer can lead to damage. The ROM writer specifications must match those for standard 1-megabit EPROMS:Vpp=12.5V V;tpw=0.2ms.

(2)Make sure that the socket adapter matches the ROM writer socket and that the chip is correctly mounted in the socket adapter. Faulty connections can lead to damage.

(3)After clearing all memory of the ROM writer, load the program. (Write the data X'FF' on the address X'0000' to X'7FFF'.)

(4)After confirming the device name, write the addresses from the start to the final address.

(5)The option bits for supporting the mask option are prepared at the final ROM address.

This writer has no internal ID codes of Silicon Signature and Intelligent Identifier of the auto-device selection command of ROM writer. If the auto-device selection command is to be executed for this writer, the device is likely damaged. Therefore, never use this command.

■ When disabling the writing

When disabling the writing, check the following points.

(1)Check that the device is mounted correctly on the socket.(pin bending, connecting failure).

(2)Check that the erase check result is no problem.

(3)Check that the adapter type is identical to the device name.

(4)Check that the writing mode is set correctly.

(5)Check that the data is correctly transferred to the ROM writer.

(6)Recheck the check points (1),(2) and (3) provided on the above paragraph of ìCautions on Handling the ROM writerî.

When the writing is disabled even after the above check points are confirmed and the device is replaced with another one, contact the nearest semiconductor design center.

(See the attached sales office table.)

8-1-7 Option Bit

The MN101C117 and the MN101CP117 control the oscillation mode after resetting as well as the runaway-detection watch dog timer, using bit 2 to 0 of the last address (X'7FFF) of the built-in ROM.

■ Option bit

7	6	5	4	3	2	1	0
—	—	—	PKGSEL2	PKGSEL1	WDSEL2	WDSEL1	NSSTRT

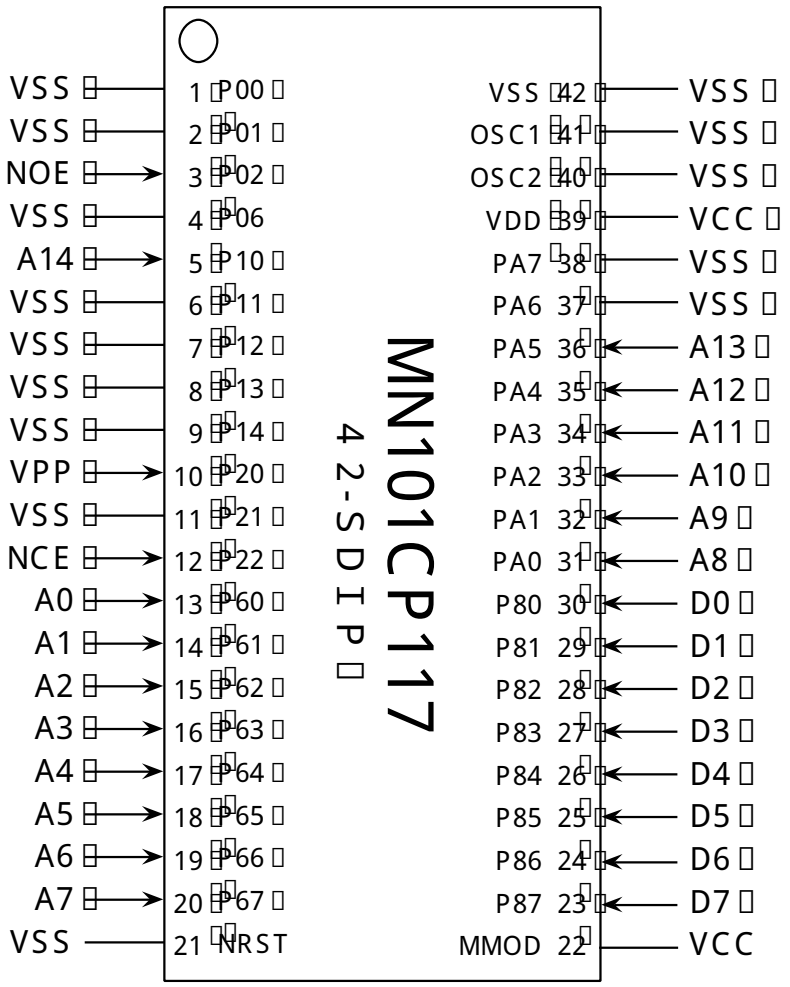
NSSTRT	Selection of oscillation mode after resetting
0	Slow mode
1	NORMAL mode

WDSEL2	WDSEL1	Watchdog timer cycle setting
0	0	$fs/2^{16}$
	1	$fs/2^{18}$
1	X	$fs/2^{20}$

PKGSEL2	PKGSEL1	Package
0	X	SDIP042-P-0600
1	0	QFP044-P-1010
	1	QFH048-P-0707

Fig. 8-1-2 Option bit(Address: X'07FFF')

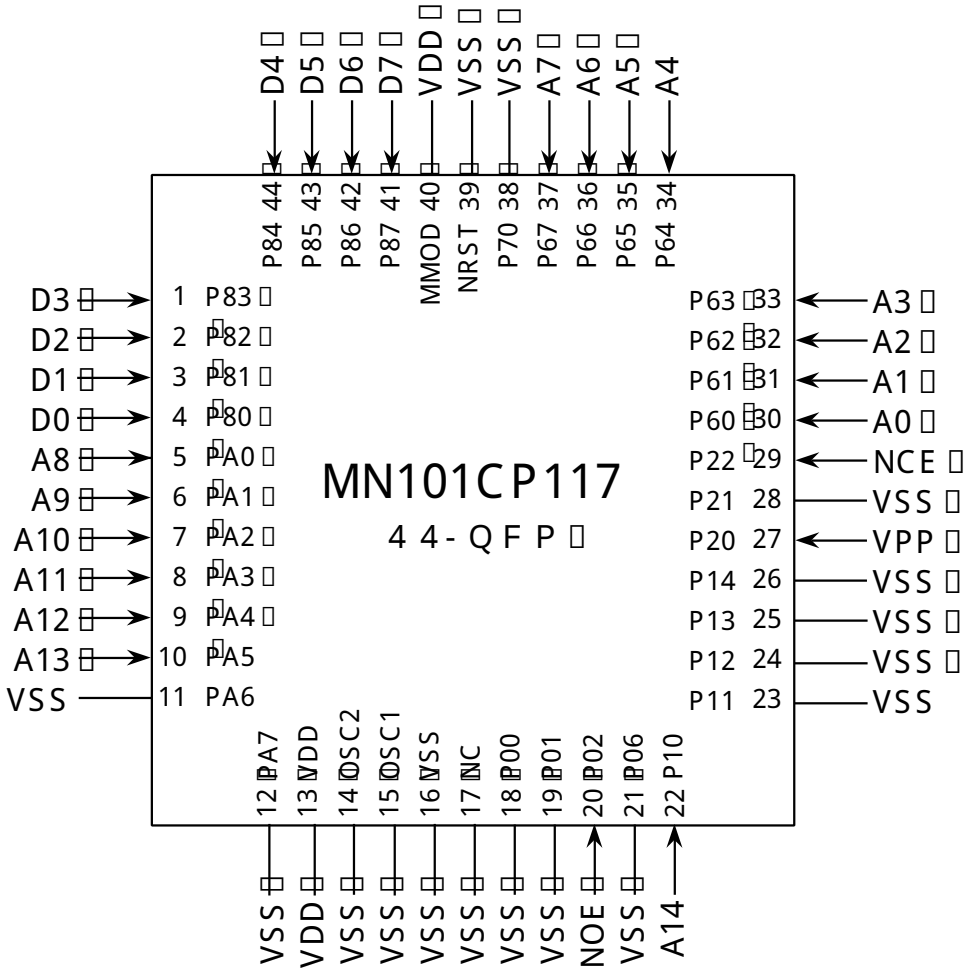
8-1-8 Writing Adapter Connection



Package Code SDIP042-P-0600

Fig. 8-1-3 MN1-1CP117-DP(DC)EPROM Writing Adapter Connections

Refer to the pin connection drawing of the 256-bit EPROM(27C256).

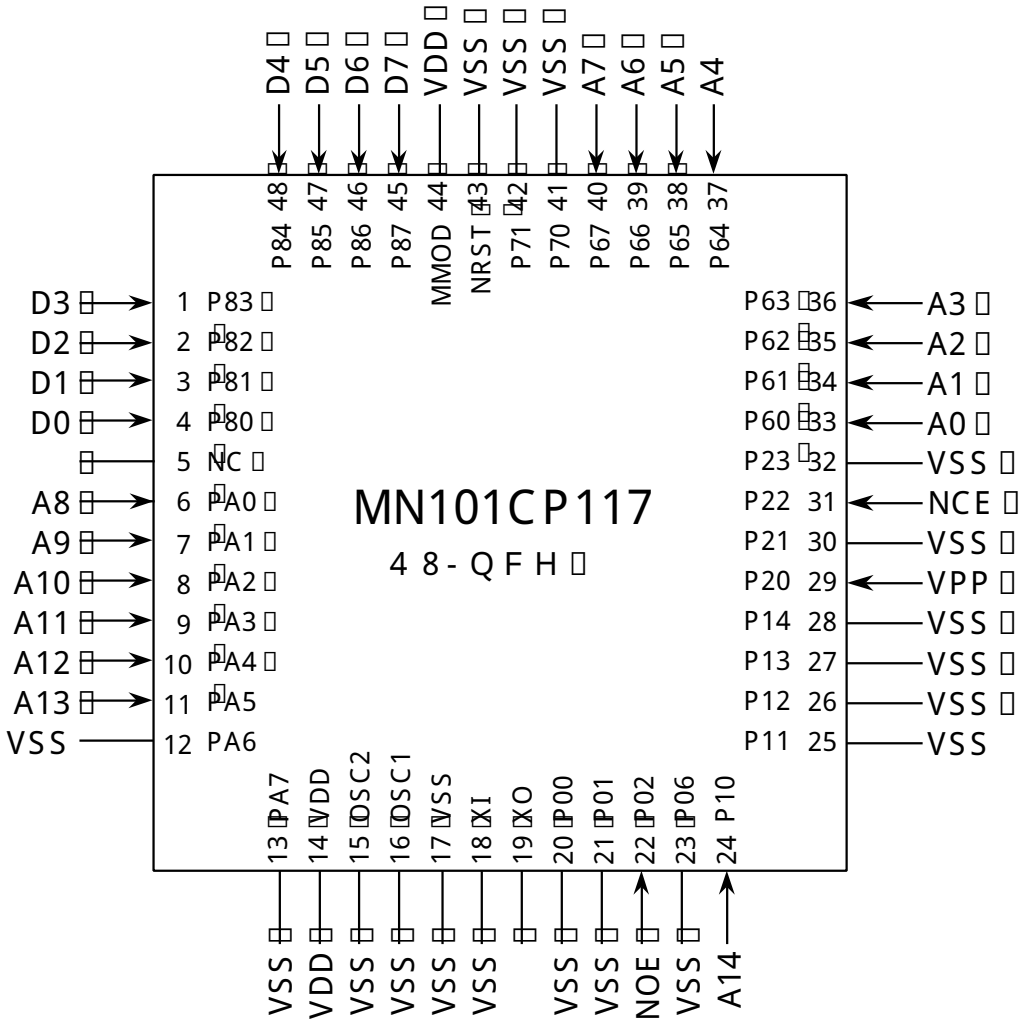


Package code: QFP044-P-1010

Pin pitch: 0.8mm

Fig. 8-1-4 MN101CP117-BL(BC)EPROM Writing Adapter Connections

Refer to the pin connection drawing of the 256-bit EPROM(27C256).



Package code: QFH048-P-0707

Pin pitch: 0.5mm

Fig. 8-1-5 MN101CP117-HP EPROM Writing Adapter connections

Refer to the pin connection drawing of the 256-bit EPROM(27C256).

8-2 Instruction Set

MN101C00 SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Affected Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Machine Code Expand 1 2 3 4 5 6 7 8 9 10 11	Notes	Page
Data move instructions												
MOV	MOV Dn,Dm	Dn→Dm	–	–	–	–	2	1		1010 DnDm		25
	MOV imm8,Dm	imm8→Dm	–	–	–	–	4	2		1010 DmDm <#8. ...>		25
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3		0010 1001 01Dn		26
	MOV PSW,Dm	PSW→Dm	–	–	–	–	3	2		0010 0001 01Dm		26
	MOV (An),Dm	mem8(An)→Dm	–	–	–	–	2	2		0100 1ADm		27
	MOV (d8,An),Dm	mem8(d8+An)→Dm	–	–	–	–	4	2		0110 1ADm <d8. ...>	*1	27
	MOV (d16,An),Dm	mem8(d16+An)→Dm	–	–	–	–	7	4		0010 0110 1ADm <d16 ....>		28
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	–	–	–	–	3	2		0110 01Dm <d4>	*2	28
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	–	–	–	–	5	3		0010 0110 01Dm <d8. ...>	*3	29
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	–	–	–	–	7	4		0010 0110 00Dm <d16 ....>		29
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	–	–	–	–	4	2		0110 00Dm <io8 ...>		30
	MOV (abs8),Dm	mem8(abs8)→Dm	–	–	–	–	4	2		0100 01Dm <abs 8..>		30
	MOV (abs12),Dm	mem8(abs12)→Dm	–	–	–	–	5	2		0100 00Dm <abs 12.. ...>		31
	MOV (abs16),Dm	mem8(abs16)→Dm	–	–	–	–	7	4		0010 1100 00Dm <abs 16.. ....>		31
	MOV Dn,(Am)	Dn→mem8(Am)	–	–	–	–	2	2		0101 1aDn		32
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	–	–	–	–	4	2		0111 1aDn <d8. ...>	*1	32
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	–	–	–	–	7	4		0010 0111 1aDn <d16 ....>		33
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	–	–	–	–	3	2		0111 01Dn <d4>	*2	33
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	–	–	–	–	5	3		0010 0111 01Dn <d8. ...>	*3	34
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	–	–	–	–	7	4		0010 0111 00Dn <d16 ....>		34
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	–	–	–	–	4	2		0111 00Dn <io8 ...>		35
	MOV Dn,(abs8)	Dn→mem8(abs8)	–	–	–	–	4	2		0101 01Dn <abs 8..>		35
	MOV Dn,(abs12)	Dn→mem8(abs12)	–	–	–	–	5	2		0101 00Dn <abs 12.. ...>		36
	MOV Dn,(abs16)	Dn→mem8(abs16)	–	–	–	–	7	4		0010 1101 00Dn <abs 16.. ....>		36
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	–	–	–	–	6	3		0000 0010 <io8 ...> <#8. ...>		37
	MOV imm8,(abs8)	imm8→mem8(abs8)	–	–	–	–	6	3		0001 0100 <abs 8..> <#8. ...>		37
	MOV imm8,(abs12)	imm8→mem8(abs12)	–	–	–	–	7	3		0001 0101 <abs 12.. ...> <#8. ...>		38
	MOV imm8,(abs16)	imm8→mem8(abs16)	–	–	–	–	9	5		0011 1101 1001 <abs 16.. ....> <#8. ...>		38
	MOV Dn,(HA)	Dn→mem8(HA)	–	–	–	–	2	2		1101 00Dn		39
MOVW	MOVW (An),DWm	mem16(An)→DWm	–	–	–	–	2	3		1110 00Ad		40
	MOVW (An),Am	mem16(An)→Am	–	–	–	–	3	4		0010 1110 10Aa	*4	40
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	–	–	–	–	3	3		1110 011d <d4>	*2	41
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	–	–	–	–	3	3		1110 010a <d4>	*2	41
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	–	–	–	–	5	4		0010 1110 011d <d8. ...>	*3	42
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	–	–	–	–	5	4		0010 1110 010a <d8. ...>	*3	42
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	–	–	–	–	7	5		0010 1110 001d <d16 ....>		43
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	–	–	–	–	7	5		0010 1110 000a <d16 ....>		43
	MOVW (abs8),DWm	mem16(abs8)→DWm	–	–	–	–	4	3		1100 011d <abs 8..>		44
	MOVW (abs8),Am	mem16(abs8)→Am	–	–	–	–	4	3		1100 010a <abs 8..>		44
	MOVW (abs16),DWm	mem16(abs16)→DWm	–	–	–	–	7	5		0010 1100 011d <abs 16.. ....>		45
	MOVW (abs16),Am	mem16(abs16)→Am	–	–	–	–	7	5		0010 1100 010a <abs 16.. ....>		45
	MOVW DWn,(Am)	DWn→mem16(Am)	–	–	–	–	2	3		1111 00aD		46
	MOVW An,(Am)	An→mem16(Am)	–	–	–	–	3	4		0010 1111 10aA	*4	46
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	–	–	–	–	3	3		1111 011D <d4>	*2	47
	MOVW An,(d4,SP)	An→mem16(d4+SP)	–	–	–	–	3	3		1111 010A <d4>	*2	47
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	–	–	–	–	5	4		0010 1111 011D <d8. ...>	*3	48
	MOVW An,(d8,SP)	An→mem16(d8+SP)	–	–	–	–	5	4		0010 1111 010A <d8. ...>	*3	48
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	–	–	–	–	7	5		0010 1111 001D <d16 ....>		49
	MOVW An,(d16,SP)	An→mem16(d16+SP)	–	–	–	–	7	5		0010 1111 000A <d16 ....>		49
	MOVW DWn,(abs8)	DWn→mem16(abs8)	–	–	–	–	4	3		1101 011D <abs 8..>		50
	MOVW An,(abs8)	An→mem16(abs8)	–	–	–	–	4	3		1101 010A <abs 8..>		50
	MOVW DWn,(abs16)	DWn→mem16(abs16)	–	–	–	–	7	5		0010 1101 011D <abs 16.. ....>		51
	MOVW An,(abs16)	An→mem16(abs16)	–	–	–	–	7	5		0010 1101 010A <abs 16.. ....>		51
	MOVW DWn,(HA)	DWn→mem16(HA)	–	–	–	–	2	3		1001 010D		52
	MOVW An,(HA)	An→mem16(HA)	–	–	–	–	2	3		1001 011A		52
	MOVW imm8,DWm	sign(imm8)→DWm	–	–	–	–	4	2		0000 110d <#8. ...>	*5	53
	MOVW imm8,Am	zero(imm8)→Am	–	–	–	–	4	2		0000 111a <#8. ...>	*6	53
	MOVW imm16,DWm	imm16→DWm	–	–	–	–	6	3		1100 111d <#16 ....>		54

Note: "Page" refers to the corresponding page in the Instruction Manual.

*1 d8 sign extended
*2 d4 zero extended
*3 d8 zero extended
*4 A=An, a=Am
*5 #8 sign extended
*6 #8 zero extended

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Group	Mnemonic	Operation	Affected Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Machine Code Expand 1 2 3 4 5 6 7 8 9 10 11	Notes	Page
	MOVW imm16,Am	imm16→Am	–	–	–	–	6	3		1101 111a <#16 ....>		54
	MOVW SP,Am	SP→Am	–	–	–	–	3	3		0010 0000 100a		55
	MOVW An,SP	An→SP	–	–	–	–	3	3		0010 0000 101A		55
	MOVW DWn,DWm	DWn→DWm	–	–	–	–	3	3		0010 1000 00Dd	∗1	56
	MOVW DWn,Am	DWn→Am	–	–	–	–	3	3		0010 0100 11Da		56
	MOVW An,DWm	An→DWm	–	–	–	–	3	3		0010 1100 11Ad		57
	MOVW An,Am	An→Am	–	–	–	–	3	3		0010 0000 00Aa	∗2	57
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	–	–	–	–	2	3		1111 10Dn		58
	PUSH An	SP-2→SP,An→mem16(SP)	–	–	–	–	2	5		0001 011A		58
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	–	–	–	–	2	3		1110 10Dn		59
	POP An	mem16(SP)→An,SP+2→SP	–	–	–	–	2	4		0000 011A		59
EXT	EXT Dn,DWm	sign(Dn)→DWm	–	–	–	–	3	3		0010 1001 000d	∗3	60
Arithmetic instructions												
ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2	○	0011 0011 DnDm		61
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2		1000 00Dm <#4>	∗6	61
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2		0000 10Dm <#8. ...>		62
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○	0011 1011 DnDm		63
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○	0010 0101 00Dd	∗1	64
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○	0010 0101 10Da		64
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2		1110 110a <#4>	∗6	65
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3		0010 1110 110a <#8. ...>	∗7	65
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4		0010 0101 011a <#16 ....>		66
	ADDW imm4,SP	SP+sign(imm4)→SP	–	–	–	–	3	2		1111 1101 <#4>	∗6	66
	ADDW imm8,SP	SP+sign(imm8)→SP	–	–	–	–	4	2		1111 1100 <#8. ...>	∗7	67
	ADDW imm16,SP	SP+imm16→SP	–	–	–	–	7	4		0010 1111 1100 <#16 ....>		67
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4		0010 0101 010d <#16 ....>		68
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○	0010 1000 1aDn	∗8	69
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○	0010 1001 1aDn		70
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○	0010 1010 DnDm		71
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1		1000 01Dn		71
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3		0010 1010 DmDm <#8. ...>		72
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○	0010 1011 DnDm		73
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3		0010 0100 00Dd	∗1	74
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3		0010 0100 10Da		74
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4		0010 0100 010d <#16 ....>		75
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4		0010 0100 011a <#16 ....>		75
MULU	MULU Dn,Dm	Dm∗Dn→DWk	0	●	●	●	3	8		0010 1111 111D	∗4	76
DIVU	DIVU Dn,DWm	DWm/Dn→DWm-l...DWm-h	●	●	●	●	3	9		0010 1110 111d	∗5	77
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2		0011 0010 DnDm		78
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2		1100 00Dm <#8. ...>		78
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3		0000 0100 <abs 8..> <#8. ...>		79
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3		0000 0101 <abs 12.. ...> <#8. ...>		79
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5		0011 1101 1000 <abs 16.. ....> <#8. ...>		80
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3		0010 1000 01Dd	∗1	81
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3		0010 0101 11Da		81
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3		0010 0000 01Aa	∗2	82
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3		1100 110d <#16 ....>		82
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3		1101 110a <#16 ....>		83
Logical instructions												
AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2		0011 0111 DnDm		84
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2		0001 11Dm <#8. ...>		84
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3		0010 1001 0010 <#8. ...>		85
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2		0011 0110 DnDm		86
	OR imm8,Dm	DmIimm8→Dm	0	●	0	●	4	2		0001 10Dm <#8. ...>		86
	OR imm8,PSW	PSWIimm8→PSW	●	●	●	●	5	3		0010 1001 0011 <#8. ...>		87
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2		0011 1010 DnDm	∗9	88
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3		0011 1010 DmDm <#8. ...>		88

Note: "Page" refers to the corresponding page in the Instruction Manual.

∗1 D=DWn, d=DWm
∗2 A=An, a=Am
∗3 d=DWm
∗4 D=DWk
∗5 D=DWm
∗6 #4 sign extended
∗7 #8 sign extended
∗8 Dn zero extended
∗9 m≠n

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Group	Mnemonic	Operation	Affected Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Machine Code Expand 1 2 3 4 5 6 7 8 9 10 11	Notes	Page
NOT	NOT Dn	¯Dn→Dn	0	●	0		3	2		0010 0010 10Dn		89
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	–	●	●	3	2	○	0010 0011 10Dn		90
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○	0010 0011 11Dn		91
ROR	ROR Dn	Dn.lsb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○	0010 0010 11Dn		92
Bit manipulation instructions												
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	•	0	•	5	5		0011 1000 0bp. <io8 ...>		93
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	•	0	•	4	4		1011 0bp. <abs 8..>		93
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	•	0	•	7	6		0011 1100 0bp. <abs 16.. ....>		94
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	•	0	•	5	5		0011 1000 1bp. <io8 ...>		95
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	•	0	•	4	4		1011 1bp. <abs 8..>		95
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	•	0	•	7	6		0011 1100 1bp. <abs 16.. ....>		96
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	•	0	•	5	3		0010 0000 11Dm <#8. ...>		97
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	•	0	•	7	5		0011 1101 0bp. <abs 16.. ....>		97
Branch instructions												
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	–	–	–	–	3	2/3		1001 000H <d4>	∗1	98
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	–	–	–	–	4	2/3		1000 1010 <d7. ...H	∗2	98
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	–	–	–	–	5	2/3		1001 1010 <d11 ....H	∗3	99
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	–	–	–	–	3	2/3		1001 001H <d4>	∗1	100
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	–	–	–	–	4	2/3		1000 1011 <d7. ...H	∗2	100
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	–	–	–	–	5	2/3		1001 1011 <d11 ....H	∗3	101
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	–	–	–	–	4	2/3		1000 1000 <d7. ...H	∗2	102
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	–	–	–	–	5	2/3		1001 1000 <d11 ....H	∗3	102
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	–	–	–	–	4	2/3		1000 1100 <d7. ...H	∗2	103
	BCC label	if(CF=0), PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	–	–	–	–	5	2/3		1001 1100 <d11 ....H	∗3	103
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	–	–	–	–	4	2/3		1000 1101 <d7. ...H	∗2	104
	BCS label	if(CF=1), PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	–	–	–	–	5	2/3		1001 1101 <d11 ....H	∗3	104
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	–	–	–	–	4	2/3		1000 1110 <d7. ...H	∗2	105
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	–	–	–	–	5	2/3		1001 1110 <d11 ....H	∗3	105
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	–	–	–	–	4	2/3		1000 1111 <d7. ...H	∗2	106
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	–	–	–	–	5	2/3		1001 1111 <d11 ....H	∗3	106
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	–	–	–	–	5	3/4		0010 0010 0001 <d7. ...H	∗2	107

Note: "Page" refers to the corresponding page in the Instruction Manual.

∗1 d4 sign extended
∗2 d7 sign extended
∗3 d11 sign extended

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Group	Mnemonic	Operation	Affected Flag				Code Size	Cycle	Re-peat	Machine Code											Notes	Page
			VF	NF	CF	ZF				Expand	1	2	3	4	5	6	7	8	9	10	11	
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	–	–	–	–	6	3/4		0010	0011	0001	<d11	....	...H						*3	107
	BHI label	if(CFIZF=0),PC+5+d7(label)+H→PC if(CFIZF=1), PC+5→PC	–	–	–	–	5	3/4		0010	0010	0010	<d7.	...H							*2	108
	BHI label	if(CFIZF=0),PC+6+d11(label)+H→PC if(CFIZF=1), PC+6→PC	–	–	–	-	6	3/4		0010	0011	0010	<d11	....	...H						*3	108
	BLS label	if(CFIZF=1),PC+5+d7(label)+H→PC if(CFIZF=0), PC+5→PC	–	–	–	–	5	3/4		0010	0010	0011	<d7.	...H							*2	109
	BLS label	if(CFIZF=1),PC+6+d11(label)+H→PC if(CFIZF=0), PC+6→PC	–	–	–	–	6	3/4		0010	0011	0011	<d11	....	...H						*3	109
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	–	-	-	-	5	3/4		0010	0010	0100	<d7.	...H							*2	110
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	–	–	–	–	6	3/4		0010	0011	0100	<d11	....	...H						*3	110
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	–	–	–	–	5	3/4		0010	0010	0101	<d7.	...H							*2	111
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	–	–	–	–	6	3/4		0010	0011	0101	<d11	....	...H						*3	111
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	–	–	–	–	5	3/4		0010	0010	0110	<d7.	...H							*2	112
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	–	–	–	–	6	3/4		0010	0011	0110	<d11	....	...H						*3	112
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	–	–	–	–	5	3/4		0010	0010	0111	<d7.	...H							*2	113
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	–	–	–	–	6	3/4		0010	0011	0111	<d11	....	...H						*3	113
	BRA label	PC+3+d4(label)+H→PC	–	–	–	–	3	3		1110	111H	<d4>									*1	114
	BRA label	PC+4+d7(label)+H→PC	–	–	–	–	4	3		1000	1001	<d7.	...H								*2	114
	BRA label	PC+5+d11(label)+H→PC	–	–	–	–	5	3		1001	1001	<d11	....	...H							*3	115
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4		1100	10Dm	<#8.	...>	<d7.	...H						*2	116
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5		0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3	116
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7		0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H			*2	117
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7		0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H		*3	117
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8		0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2	118
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8		0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3	118
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4		1101	10Dm	<#8.	...>	<d7.	..H>						*2	119
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5		0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3	119
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7		0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H			*2	120
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7		0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H		*3	120
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8		0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2	121
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8		0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3	121
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011	0000	0bp.	<abs	8..>	<d7.	...H					*2	122
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011	0000	1bp.	<abs	8..>	<d11	....	...H				*3	122

Note: "Page" refers to the corresponding page in the Instruction Manual.

*1 d4 sign extended
*2 d7 sign extended
*3 d11 sign extended

MN101C00 SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Affected Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	Machine Code Expand 1 2 3 4 5 6 7 8 9 10 11	Notes	Page
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011 0100 0bp. <io8 ...> <d7. ...H	*1	123
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011 0100 1bp. <io8 ...> <d11 ....H	*2	123
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8		0011 1110 0bp. <abs 16.. ....> <d7. ...H	*1	124
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8		0011 1110 1bp. <abs 16.. ....> <d11 ....H	*2	124
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011 0001 0bp. <abs 8..> <d7. ...H	*1	125
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011 0001 1bp. <abs 8..> <d11 ....H	*2	125
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011 0101 0bp. <io8 ...> <d7. ...H	*1	126
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011 0101 1bp. <io8 ...> <d11 ....H	*2	126
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8		0011 1111 0bp. <abs 16.. ....> <d7. ...H	*1	127
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8		0011 1111 1bp. <abs 16.. ....> <d11 ....H	*2	127
JMP	JMP (An)	0→PC.17~16,An→PC.15~0,0→PC.H	–	–	–	–	3	4		0010 0001 00A0		128
	JMP label	abs18(label)+H→PC	–	–	–	–	7	5		0011 1001 0aaH <abs 18.b p15~ 0..>	*5	128
JSR	JSR (An)	SP-3→SP,(PC+3).bp7~0→mem8(SP) (PC+3).bp15~8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6~2, (PC+3).bp17~16→mem8(SP+2).bp1~0 0→PC.bp17~16 An→PC.bp15~0,0→PC.H	–	–	–	–	3	7		0010 0001 00A1		129
	JSR label	SP-3→SP,(PC+5).bp7~0→mem8(SP) (PC+5).bp15~8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6~2, (PC+5).bp17~16→mem8(SP+2).bp1~0 PC+5+d12(label)+H→PC	–	–	–	–	5	6		0001 000H <d12 ....>	*3	129
	JSR label	SP-3→SP,(PC+6).bp7~0→mem8(SP) (PC+6).bp15~8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6~2, (PC+6).bp17~16→mem8(SP+2).bp1~0 PC+6+d16(label)+H→PC	–	–	–	–	6	7		0001 001H <d16 ....>	*4	130
	JSR label	SP-3→SP,(PC+7).bp7~0→mem8(SP) (PC+7).bp15~8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6~2, (PC+7).bp17~16→mem8(SP+2).bp1~0 abs18(label)+H→PC	–	–	–	–	7	8		0011 1001 1aaH <abs 18.b p15~ 0..>	*5	130
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7~0→mem8(SP) (PC+3).bp15~8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6~2, (PC+3).bp17~16→mem8(SP+2).bp1~0 mem8(x'004080+tbl4<<2)→PC.bp7~0 mem8(x'004080+tbl4<<2+1)→PC.bp15~8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp1~0→ PC.bp17~16	–	–	–	–	3	9		1111 1110 <t4>		131
NOP	NOP	PC+2→PC	–	–	–	–	2	1	○	0000 0000		132

Note: "Page" refers to the corresponding page in the Instruction Manual.

*1 d7 sign extended
*2 d11 sign extended
*3 d12 sign extended
*4 d16 sign extended
*5 aa=abs18.17 - 16

MN101C00 SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Machine Code Expand	1	2	3	4	5	6	7	8	9	10	11	Notes	Page
RTS	RTS	mem8(SP)→(PC).bp7 ~ 0	-	-	-	-	2	7			0000	0001											133
		mem8(SP+1)→(PC).bp15 ~ 8																					
		mem8(SP+2).bp7→(PC).H																					
		mem8(SP+2).bp1 ~ 0→(PC).bp17 ~ 16																					
		SP+3→SP																					
RTI	RTI	mem8(SP)→PSW	•	•	•	•	2	11			0000	0011											134
		mem8(SP+1)→(PC).bp7 ~ 0																					
		mem8(SP+2)→(PC).bp15 ~ 8																					
		mem8(SP+3).bp7→(PC).H																					
		mem8(SP+3).bp1 ~ 0→(PC).bp17 ~ 16																					
		mem8(SP+4)→HA-l																					
		mem8(SP+5)→HA-h																					
		SP+6→SP																					
Control instruction																							
REP	REP imm3	imm3→RPC	-	-	-	-	3	2		0010	0001	1rep										※1	135

Note: "Page" refers to the corresponding page in the Instruction Manual.

*1 Number of repeats is 0 when imm3=0.

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8-3 Instruction Map

MN101C00 SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the extension code is b'0010'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nibble\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2		BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3		BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

Extension code: b'0011'
2nd nibble\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)			CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

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8-4 Summary of Special Function Registers

Address	Register	Bit Symbol								Reference page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F00'	CPUM					STOP	HALT	OSC1	OSC0	MN101C00 series LSI Manual
					Must be set to "0"	STOP transfer request	HALT transfer request	Oscillation control		
X'3F01'	MEMCTR	IOW1	IOW0	IVBA			IRWE			30
		I/O bus wait value set		Specifies base address of interrupt vector table						
X'3F02'	WDCTR								WDEN	89
									Watchdog timer table	
X'3F03'	DLYCTR							DLYS1	DLYS0	89
								Sets oscillation stabilization wait period		
X'3F0E'	EXADV									—
X'3F10'	P0OUT		P0OUT6				P0OUT2	P0OUT1	P0OUT0	41, 45
							Port 0 output			
X'3F11'	P1OUT				P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	41, 45
					Port 1 output					
X'3F12'	P2OUT	P2OUT7								41, 45
		Port 2 output								
X'3F13'	Disables to use									—
X'3F14'	Disables to use									—
X'3F15'	Disables to use									—
X'3F16'	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	41, 45
		Port 6 output								
X'3F17'	P7OUT								P7OUT0	41, 45
									Port 7 output	
X'3F18'	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	41, 45
		Port 8 output								
X'3F1F'	Disables to use									—
X'3F20'	P0IN		P0IN6				P0IN2	P0IN1	P0IN0	41, 45
							Port 0 input			
X'3F21'	P1IN				P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	41, 45
					Port 1 input					
X'3F22'	P2IN						P2IN2	P2IN1	P2IN0	41, 45
							Port 2input			
X'3F23'	Disables to use									—

Address	Register	Bit Symbol								Reference Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F24'	Disables to use									—
X'3F25'	Disables to use									—
X'3F26'	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	41, 45
		Port 6 input								
X'3F27'	P7IN								P7IN0	41, 45
									Port 7 input	
X'3F28'	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	41, 45
		Port 8 input								
X'3F2A'	PAIN	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	41, 45
		Port A input								
X'3F30'	P0DIR		P0DIR6				P0DIR2	P0DIR1	P0DIR0	41, 45
							Port 0 I/O direction control			
X'3F31'	P1DIR				P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	41, 45
					Port 1 I/O direction control					
X'3F33'	Disables to use									—
X'3F34'	Disables to use									—
X'3F35'	Disables to use									—
X'3F36'	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	41, 45
		Port 6 I/O direction control								
X'3F37'	P7DIR								P7DIR0	41, 45
									Port 7 I/O direction control	
X'3F38'	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	41, 45
		Port 8 I/O direction control								
X'3F39'	P1OMD				P14TCO	P13TCO	P12TCO		P10TCO	41, 46
					I/O port/Special function pin control					
X'3F3A'	PAIMD			PAAIN5	PAAIN4	PAAIN3	PAAIN2	PAAIN1	PAAIN0	41, 46
				I/O port/Special function pin control						
X'3F3C'	Disables to use									—
X'3F40'	P0PLU		P0PLU6				P0PLU2	P0PLU1	P0PLU0	41, 45
							Port 0 pull-up resistor ON/OFF control			
X'3F41'	P1PLU				P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	42, 45
					Port 1 pull-up resistor ON/OFF control					

Address	Register	Bit Symbol								Reference Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F42'	P2PLU						P2PLU2	P2PLU1	P2PLU0	42, 45
							Port 2 pull-up resistor ON/OFF control			
X'3F43'	Disables to use									—
X'3F44'	Disables to use									—
X'3F45'	Disables to use									—
X'3F46'	P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	42, 45
		Port 6 pull-up resistor ON/OFF control								
X'3F47'	P7PLUD								P7PLUD0	42, 45
									Port pull-up pull down resistor ON/OFF control	
X'3F48'	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	42, 45
		Port 8 pull-up resistor ON/OFF control								
X'3F4A'	PAPLUD	PAPLUD7	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	42, 45
		Port A pull-up pull-down resistor ON/OFF control								
X'3F4B'	FLOAT1						P21M	PARDWN	P7RDWN	42, 46
							P21 input/output mode selection	Port A pullup/pulldown sel.	Port 7 pullup/pulldown sel.	
X'3F4C'	Disables to use									—
X'3F50'	SC0MD0		SC0CE0	SC0CE1	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	108
			Receive data input edge / Transmit data output edge		Start bit set up for transmit	Synchronous serial start edition select	Transfer bit count			
X'3F51'	SC0MD1			SC0CKM	SC0CK1	SC0CK0	SC0BRKF	SC0ERE	SC0TRI	109
				Select 1/8 period of freq.	Clock source selection		Break status rec. monitor	Error monitor	Trans/rec interrupt request flag	
X'3F52'	SC0MD2			SC0BRKE	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	110
				Control break status trans.	Specifies frame mode		Specifies added bit		Enables parity	
X'3F53'	SC0MD3			SC0IOM	SC0SBOM	SC0SBTM	SC0SBOS	SC0SBIS	SC0SBTS	111
				SBI0/SBO0 pin connection	SBO0 pin selection	Select SBT pin format	Select SBO pin function	Control SBI input	Select SBT0 pin function	
X'3F54'	SC0CTR	SC0BSY	SC0CMD			SC0FEF	SC0PEK	SC0ORE		112
		Status of serial bus	Select sync./seroal UART			Detect framing error	Detect parity error	Detect overrun error		
X'3F55'	SC0TRB	SC0TRB7	SC0TRB6	SC0TRB5	SC0TRB4	SC0TRB3	SC0TRB2	SC0TRB1	SC0TRB0	107
		Serial interface 0 transmit/receive shift register								
X'3F56'	SC0RXB	SC0RXB7	SC0RXB6	SC0RXB5	SC0RXB4	SC0RXB3	SC0RXB2	SC0RXB1	SC0RXB0	107
		Serial interface 0 receive data buffer								
X'3F57'	Disables to use									—
X'3F58'	Disables to use									—

Address	Register	Bit Symbol								Reference Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F59'	Disables to use									—
X'3F5A'	Disables to use									—
X'3F5B'	Disables to use									—
X'3F5C'	Disables to use									—
X'3F5D'	Disables to use									—
X'3F60'	Disables to use									—
X'3F61'	Disables to use									-
X'3F62'	TM2BC	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0	82
		Binary counter2								
X'3F63'	TM3BC	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0	82
		Binary counter3								
X'3F64'	TM4BCL	TM4BCL7	TM4BCL6	TM4BCL5	TM4BCL4	TM4BCL3	TM4BCL2	TM4BCL1	TM4BCL0	83
		Binary counter 4 (Lower 8 bits)								
X'3F65'	TM4BCH	TM4BCH7	TM4BCH6	TM4BCH5	TM4BCH4	TM4BCH3	TM4BCH2	TM4BCH1	TM4BCH0	83
		Binary counter4 (Upper 8 bits)								
X'3F66'	TM4ICL	TM4ICL7	TM4ICL6	TM4ICL5	TM4ICL4	TM4ICL3	TM4ICL2	TM4ICL1	TM4ICL0	84
		Input capture register (Lower 8 bits)								
X'3F67'	TM4ICH	TM4ICH7	TM4ICH6	TM4ICH5	TM4ICH4	TM4ICH3	TM4ICH2	TM4ICH1	TM4ICH0	84
		Input capture register(Upper 8 bits)								
X'3F68'	TM5BC	TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0	84
		Binary counter 5								
X'3F70'	Disables to use									-
X'3F71'	Disables to use									-
X'3F72'	TM2OC	TM2OC7	TM2OC6	TM2OC5	TM2OC4	TM2OC3	TM2OC2	TM2OC1	TM2OC0	82
		Compare register 2								
X'3F73'	TM3OC	TM3OC7	TM3OC6	TM3OC5	TM3OC4	TM3OC3	TM3OC2	TM3OC1	TM3OC0	82
		Compare register 3								
X'3F74'	TM4OCL	TM4OCL7	TM4OCL6	TM4OCL5	TM4OCL4	TM4OCL3	TM4OCL2	TM4OCL1	TM4OCL0	83
		Compare register 4 (Lower 8 bits)								

Address	Register	Bit Symbol								Reference Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FE0'	Disables to use									—
X'3FE1'	NMICR							WDIR Watchdog interrupt request flag		34
X'3FE2'	IRQ0ICR	IRQ0LV1 Interrupt level flag for external interrupt	IRQ0LV0	REDG0 External interrupt valid edge flag				IRQ0IE Interrupt enable flag	IRQ0IR Interrupt request flag	34
X'3FE3'	IRQ1ICR	IRQ1LV1 Interrupt level flag for external interrupt	IRQ1LV0	REDG1 External interrupt valid edge flag				IRQ1IE Interrupt enable flag	IRQ1IR Interrupt request flag	34
X'3FE4'	Disables to use									—
X'3FE5'	Disables to use									—
X'3FE6'	TM2ICR	TM2LV1 Interrupt level flag for timer 2 interrupt	TM2LV0					TM2IE Interrupt enable flag	TM2IR Interrupt request flag	35
X'3FE7'	TBICR	TBLV1 Interrupt level flag for time base interrupt	TBLV0					TBIE Interrupt enable flag	TBIR Interrupt request flag	35
X'3FE8'	SC0ICR	SC0LV1 Interrupt level flag for serial 0 interrupt	SC0LV0					SC0IE Interrupt enable flag	SC0IR Interrupt request flag	35
X'3FE9'	Disables to use									—
X'3FEA'	ADICR	ADLV1 Interrupt level flag for A/D interrupt	ADLV0					ADIE Interrupt enable flag	ADIR Interrupt request flag	35
X'3FEB'	IRQ2ICR	IRQ2LV1 Interrupt level flag for external interrupt	IRQ2LV0	REDG2 External interrupt valid edge flag				IRQ2IE Interrupt enable flag	IRQ2IR Interrupt request flag	34
X'3FEC'	IRQ3ICR									—
X'3FED'	Disables to use									—
X'3FEE'	TM3ICR	Interrupt level flag for timer 3 interrupt						TM3IE Interrupt enable flag	Interrupt request flag	35
X'3FEF'	TM4ICR	Interrupt level flag for timer 4 interrupt						TM4IE Interrupt enable flag	Interrupt request flag	35
X'3FF0'	TM5ICR	Interrupt level flag for timer 5 interrupt						TM5IE Interrupt enable flag	Interrupt request flag	35
X'3FF1'	Disables to use									—
X'3FF2'	Disables to use									—

Address	Register	Bit Symbol								Reference Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FE0'	Disables to use									—
X'3FE1'	NMICR							WDIR Watchdog interrupt request flag		34
X'3FE2'	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0				IRQ0IE	IRQ0IR	34
		Interrup level flag for external interrupt		External interrupt valid edge flag				Interrupt enable flag	Interrupt request flag	
X'3FE3'	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1				IRQ1IE	IRQ1IR	34
		Interrupt level flag for external interrupt		External interrupt valud edge flag				Interrupt enable flag	Interrupt request flag	
X'3FE4'	Disables to use									—
X'3FE5'	Disables to use									—
X'3FE6'	TM2ICR	TM2LV1	TM2LV0					TM2IE	TM2IR	35
		Interrupt level flag for timer 2 interrupt						Interrupt enable flag	Interrupt request flag	
X'3FE7'	TBICR	TBLV1	TBLV0					TBIE	TBIR	35
		Interrupt level flag for time base interrupt						Interrupt enable flag	Interrupt request flag	
X'3FE8'	SC0ICR	SC0LV1	SC0LV0					SC0IE	SC0IR	35
		Interrupt level flag for serial 0 interrupt						Interrup enable flag	Interrupt request flag	
X'3FE9'	Disables to use									—
X'3FEA'	ADICR	ADLV1	ADLV0					ADIE	ADIR	35
		Interrup level flag for A/D interrupt						Interrupt enable flag	Interrupt request flag	
X'3FEB'	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2				IRQ2IE	IRQ2IR	34
		Interrupt level flag for external interrupt		External interrupt valid edge flag				Interrup enable flag	Interrupt request flag	
X'3FEC'	IRQ3ICR									—
X'3FED'	Disables to use									—
X'3FEE'	TM3ICR							TM3IE		35
		Interrupt level flag for timer 3 interrupt						Interrupt enable flag	Interrupt request flag	
X'3FEF'	TM4ICR							TM4IE		35
		Interrupt level flag for timer 4 interrupt						Interrupt enable flag	Interrupt request flag	
X'3FF0'	TM5ICR							TM5IE		35
		Interrupt level flag for timer 5 interrupt						Interrupt enable flag	Interrupt request flag	
X'3FF1'	Disables to use									—
X'3FF2'	Disables to use									—

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