

**PHILIPS**

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Data handbook



Electronic  
components  
and materials

Integrated circuits

Book IC06N 1986  
New series

High-speed CMOS  
PC74HC/HCT/HCU

High-speed CMOS

PC74HC/HCT/HCU

Logic family

**NEW HANDBOOK SERIES**

IC06N New series 1986

## HIGH-SPEED CMOS PC74/HC/HCT/HCU LOGIC FAMILY

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## DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

## ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

- T1** Tubes for r.f. heating
- T2a** Transmitting tubes for communications, glass types
- T2b** Transmitting tubes for communications, ceramic types
- T3** Klystrons
- T4** Magnetrons for microwave heating
- T5** Cathode-ray tubes  
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6** Geiger-Müller tubes
- T8** Colour display systems  
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
- T9** Photo and electron multipliers
- T10** Plumbicon camera tubes and accessories
- T11** Microwave semiconductors and components
- T12** Vidicon and Newvicon camera tubes
- T13** Image intensifiers and infrared detectors
- T15** Dry reed switches
- T16** Monochrome tubes and deflection units  
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

## SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

- S1 Diodes**  
Small-signal silicon diodes, voltage regulator diodes ( $< 1,5$  W), voltage reference diodes, tuner diodes, rectifier diodes
- S2a Power diodes**
- S2b Thyristors and triacs**
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Surface mounted semiconductors**
- S8 Devices for optoelectronics**  
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**
- S11 Microwave transistors**
- S12 Surface acoustic wave devices**
- S13 Semiconductor sensors**

## INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

### EXISTING SERIES

Superseded by:

IC1	Bipolar ICs for radio and audio equipment	IC01N
IC2	Bipolar ICs for video equipment	IC02Na and IC02Nb
IC3	ICs for digital systems in radio, audio and video equipment	IC01N, IC02Na and IC02Nb
IC4	Digital integrated circuits CMOS HE4000B family	
IC5	Digital integrated circuits – ECL ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs	IC08N
IC6	Professional analogue integrated circuits	
IC7	Signetics bipolar memories	
IC8	Signetics analogue circuits	IC11N
IC9	Signetics TTL logic	IC09N and IC15N
IC10	Signetics Integrated Fuse Logic (IFL)	IC13N
IC11	Microprocessors, microcomputers and peripheral circuitry	IC14N

## NEW SERIES

<b>IC01N</b>	<b>Radio, audio and associated systems</b> Bipolar, MOS	(published 1985)
<b>IC02Na</b>	<b>Video and associated systems</b> Bipolar, MOS Types MAB8031AH to TDA1524A	(published 1985)
<b>IC02Nb</b>	<b>Video and associated systems</b> Bipolar, MOS Types TDA2501 to TEA1002	(published 1985)
<b>IC03N</b>	<b>Integrated circuits for telephony</b>	(published 1985)
<b>IC04N</b>	<b>HE4000B logic family</b> CMOS	
<b>IC05N</b>	<b>HE4000B logic family – uncased ICs</b> CMOS	(published 1984)
<b>IC06N*</b>	<b>High-speed CMOS; PC74HC/HCT/HCU</b> Logic family	(published 1986)
<b>IC07N</b>	<b>High-speed CMOS; PC74HC/HCT/HCU – uncased ICs</b> Logic family	
<b>IC08N</b>	<b>ECL 10K and 100K logic families</b>	(published 1984)
<b>IC09N</b>	<b>TTL logic series</b>	(published 1984)
<b>IC10N</b>	<b>Memories</b> MOS, TTL, ECL	
<b>IC11N</b>	<b>Linear LSI</b>	(published 1985)
<b>IC12N</b>	<b>Semi-custom gate arrays &amp; cell libraries</b> ISL, ECL, CMOS	
<b>IC13N</b>	<b>Semi-custom</b> Integrated Fuse Logic	(published 1985)
<b>IC14N</b>	<b>Microprocessors, microcontrollers &amp; peripherals</b> Bipolar, MOS	(published 1985)
<b>IC15N</b>	<b>FAST TTL logic series</b>	(published 1984)

### Note

Books available in the new series are shown with their date of publication.

\* Supersedes the IC06N 1985 edition and the Supplement to IC06N issued Autumn 1985.



## COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

- C1 Programmable controller modules**  
PLC modules, PC20 modules
- C2 Television tuners, coaxial aerial input assemblies, surface acoustic wave filters**
- C3 Loudspeakers**
- C4 Ferroxcube potcores, square cores and cross cores**
- C5 Ferroxcube for power, audio/video and accelerators**
- C6 Synchronous motors and gearboxes**
- C7 Variable capacitors**
- C8 Variable mains transformers**
- C9 Piezoelectric quartz devices**
- C10 Connectors**
- C11 Non-linear resistors**
- C12 Potentiometers, encoders and switches**
- C13 Fixed resistors**
- C14 Electrolytic and solid capacitors**
- C15 Ceramic capacitors**
- C16 Permanent magnet materials**
- C17 Stepping motors and associated electronics**
- C18 Direct current motors**
- C19 Piezoelectric ceramics**
- C20 Wire-wound components for TVs and monitors**
- C21\* Assemblies for industrial use**  
HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices
- C22 Film capacitors**

\* To be issued shortly

## INTRODUCTION



## 74HC/HCT/HCU HIGH-SPEED CMOS (HCMOS) LOGIC IC FAMILY

The HCMOS family of logic ICs is manufactured using a self-aligning 3  $\mu\text{m}$  polycrystalline silicon-gate CMOS process combined with local oxidation of silicon (LOCOS). HCMOS ICs have the low power consumption, high immunity to input noise and wide operating temperature range of earlier silicon-gate CMOS circuits together with the high-speed and drive capability of bipolar, low-power Schottky TTL (LSTTL). They are also immune to latch-up and all types are available in DIL packages and in space-saving SO packages.

Many HCMOS circuits are pin-compatible with existing 54/74 LSTTL and HE4000B CMOS logic ICs. HCT types are ideal replacements for LSTTL. HCT types can also interface between TTL and CMOS ICs.

Three types of HCMOS ICs are available:

- 74HC: CMOS input switching levels 30% $V_{CC}$  and 70% $V_{CC}$  (typical switching threshold 50% $V_{CC}$ ), supply voltage 2 V to 6 V
- 74HCT: TTL input switching levels 0.8 V and 2 V (typical switching threshold 28% $V_{CC}$ ), supply voltage 4.5 V to 5.5 V
- 74HCU: CMOS input switching levels 20% $V_{CC}$  and 80% $V_{CC}$  (typical switching threshold 50% $V_{CC}$ ), supply voltage 2 V to 6 V; unbuffered to allow operation in the linear mode

The HCMOS family also includes several complex circuits for switching or multiplexing analog signals. These circuits have low crosstalk and feedthrough, and a very large frequency bandwidth.

There are also two FIFOs and three PLLs in the HCMOS range, of which one (HC/HCT297) is a fully digital type.

## HCMOS FEATURES

- Very low power dissipation
- The switching levels of 74HC types are 30% and 70% of  $V_{CC}$
- DC noise margin of 74HC types three times that of TTL ICs
- Logic output levels 0.1 V and  $V_{CC} - 0.1$  V
- All types, except 74HCU are fully buffered
- Typical gate propagation delay of 8 ns
- Can operate up to 60 MHz (typical)
- Fanout capability of 10 LSTTL loads (4 mA); this is increased to 15 LSTTL loads (6 mA) for types with bus-driver outputs
- Wide supply voltage range
- Latch-up free
- Inputs protected against electrostatic discharge
- Functions and pinning identical to most popular LSTTL and CMOS HE4000B families
- Analog switching types operating up to 10 V
- Symmetrical output sourcing and sinking currents and equal output rise and fall times
- All types available in plastic SO packages for surface mounting and plastic DIL packages
- Choice of operating temperature range:  $-40$  to  $+85$   $^{\circ}\text{C}$  or  $-40$  to  $+125$   $^{\circ}\text{C}$
- Meet JEDEC standard No. 7



## SELECTION GUIDE

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<b>Numerical index</b> . . . . .	<b>12</b>



**HC MOS 74HC/HCT/HCU FAMILY**

Type numbers have a suffix which signifies the type of package:  
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification	page
<b>NAND/NOR gates/EXCLUSIVE-NOR gates</b>				
HC/HCT00	quad 2-input NAND gate	14	SSI	167
HC/HCT02	quad 2-input NOR gate	14	SSI	171
HC/HCT03	quad 2-input NAND gate (with open drain outputs)	14	SSI	175
HC/HCT10	triple 3-input NAND gate	14	SSI	193
HC/HCT20	dual 4-input NAND gate	14	SSI	206
HC/HCT27	triple 3-input NOR gate	14	SSI	211
HC/HCT30	8-input NAND gate	14	SSI	215
HC7266	quad 2-input EXCLUSIVE-NOR gate	14	SSI	511
HC/HCT4002	dual 4-input NOR gate	14	SSI	677
<b>AND/OR/EXCLUSIVE-OR gates</b>				
HC/HCT08	quad 2-input AND gate	14	SSI	190
HC/HCT11	triple 3-input AND gate	14	SSI	196
HC/HCT21	dual 4-input AND gate	14	SSI	209
HC/HCT32	quad 2-input OR gate	14	SSI	219
HC58	dual AND-OR gate	14	SSI	225
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	14	SSI	247
HC/HCT4075	triple 3-input OR gate	14	SSI	812
<b>Inverters/buffers/line drivers/level shifters</b>				
HC/HCT04	hex inverter	14	SSI	181
HCU04	hex inverter (unbuffered)	14	SSI	185
HC/HCT125*	quad buffer/line driver; 3-state; output enable active LOW	14	MSI	281
HC/HCT126*	quad buffer/line driver; 3-state; output enable active HIGH	14	MSI	286
HC/HCT240*	octal buffer/line driver; 3-state; inverting	20	MSI	456
HC/HCT241*	octal buffer/line driver; 3-state; output enable active LOW or HIGH	20	MSI	461
HC/HCT244*	octal buffer/line driver; 3-state; output enable active LOW	20	MSI	478
HC/HCT365*	hex buffer/line driver; 3-state	16	MSI	549
HC/HCT366*	hex buffer/line driver; 3-state; inverting	16	MSI	553
HC/HCT367*	hex buffer/line driver; 3-state	16	MSI	557
HC/HCT368*	hex buffer/line driver; 3-state; inverting	16	MSI	561
HC/HCT540*	octal buffer/line driver; 3-state; inverting	20	MSI	611
HC/HCT541*	octal buffer/line driver; 3-state	20	MSI	612
HC4049	hex inverting HIGH-to-LOW level shifter	16	SSI	747
HC4050	hex HIGH-to-LOW level shifter	16	SSI	753

\* Types with a bus-driver output stage.



Type numbers have a suffix which signifies the type of package:  
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type no.	description	pins	classification	page
<b>Flip-flops/latches/registers</b>				
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	14	FF	226
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	14	FF	231
HC/HCT75	quad bistable transparent latch	16	FF	236
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	14	MSI	257
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	16	FF	262
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger	16	FF	267
HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state	16	MSI	381
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	16	MSI	386
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	16	MSI	391
HC/HCT259	8-bit addressable latch	16	MSI	505
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	20	MSI	514
HC/HCT373*	octal D-type transparent latch; 3-state	20	MSI	565
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state	20	MSI	570
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	20	MSI	575
HC/HCT533*	octal D-type transparent latch; 3-state; inverting	20	MSI	601
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI	606
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out	20	MSI	613
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out	20	MSI	618
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out	20	MSI	623
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out	20	MSI	628
HC/HCT670*	4 x 4 register file; 3-state	16	MSI	665
HC/HCT7030	9-bit x 64-word FIFO register; 3-state	28	MSI	925
HC/HCT40105	4-bit x 16-word FIFO register	16	MSI	973
<b>Shift registers</b>				
HC/HCT164	8-bit serial-in/parallel-out shift register	14	MSI	363
HC/HCT165	8-bit parallel-in/serial-out shift register	16	MSI	369
HC/HCT166	8-bit parallel-in/serial-out shift register; with reset	16	MSI	375
HC/HCT194	4-bit bidirectional universal shift register	16	MSI	435
HC/HCT195	4-bit parallel access shift register	16	MSI	443
HC/HCT299*	8-bit universal shift register; 3-state	20	MSI	537
HC/HCT597	8-bit shift register with input flip-flops	16	MSI	634
HC/HCT7597	8-bit shift register with input latches	16	MSI	635
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	16	MSI	681
HC/HCT4094	8-stage shift-and-store bus register	16	MSI	815
HC/HCT40104*	4-bit bidirectional universal shift register; 3-state	16	MSI	967

\* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:  
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type no.	description	pins	classification	page
<b>Arithmetic circuits</b>				
HC/HCT85	4-bit magnitude comparator	16	MSI	241
HC/HCT181	4-bit arithmetic logic unit	24	MSI	396
HC/HCT182	look-ahead carry generator	16	MSI	398
HC/HCT280	9-bit odd/even parity generator/checker	14	MSI	519
HC/HCT283	4-bit binary full adder with fast carry	16	MSI	523
HC/HCT583	4-bit BCD full adder with fast carry	16	MSI	633
HC/HCT688	8-bit magnitude comparator	20	MSI	671
<b>Counters</b>				
HC/HCT93	4-bit binary ripple counter	14	MSI	251
HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset	16	MSI	337
HC/HCT161	presettable synchronous 4-bit binary counter; asynchronous reset	16	MSI	345
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	16	MSI	351
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	16	MSI	357
HC/HCT190	presettable synchronous BCD decade up/down counter	16	MSI	403
HC/HCT191	presettable synchronous 4-bit binary up/down counter	16	MSI	413
HC/HCT192	presettable synchronous BCD decade up/down counter	16	MSI	423
HC/HCT193	presettable synchronous 4-bit binary up/down counter	16	MSI	429
HC/HCT390	dual decade ripple counter	16	MSI	581
HC/HCT393	dual 4-bit binary ripple counter	14	MSI	587
HC/HCT4017	Johnson decade counter with 10 decoded outputs	16	MSI	695
HC/HCT4020	14-stage binary ripple counter	16	MSI	703
HC/HCT4024	7-stage binary ripple counter	14	MSI	709
HC/HCT4040	12-stage binary ripple counter	16	MSI	715
HC/HCT4059	programmable divide-by-n counter	24	MSI	797
HC/HCT4060	14-stage binary ripple counter with oscillator	16	MSI	800
HC/HCT4510	BCD up/down counter	16	MSI	877
HC/HCT4516	binary up/down counter	16	MSI	899
HC/HCT4518	dual synchronous BCD counter	16	MSI	900
HC/HCT4520	dual synchronous 4-bit binary counter	16	MSI	905
HC/HCT40102	8-stage synchronous BCD down counter	16	MSI	951
HC/HCT40103	8-bit synchronous binary down counter	16	MSI	959
<b>Multiplexers</b>				
HC/HCT151	8-input multiplexer	16	MSI	311
HC/HCT153	dual 4-input multiplexer	16	MSI	316
HC/HCT157	quad 2-input multiplexer	16	MSI	326
HC/HCT158	quad 2-input multiplexer; inverting	16	MSI	331
HC/HCT251	8-input multiplexer; 3-state	16	MSI	488

\* Types with a bus-driver output stage.

# FUNCTIONAL INDEX

Type numbers have a suffix which signifies the type of package:  
 P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification	page
<b>Multiplexers (continued)</b>				
HCT/HCT253B*	dual 4-input multiplexer; 3-state	16	MSI	494
HC/HCT257*	quad 2-input multiplexer; 3-state	16	MSI	499
HC/HCT258	quad 2-input multiplexer; 3-state; inverting	16	MSI	504
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	20	MSI	545
HC/HCT356*	8-input multiplexer/register; 3-state	20	MSI	547
<b>Decoders/demultiplexers</b>				
HC/HCT42	BCD to decimal decoder (1-of-10)	16	MSI	223
HC/HCT137	3-to-8 line decoder/demultiplexer with address latches	16	MSI	296
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	16	MSI	297
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	16	MSI	302
HC/HCT147	10-to-4 line priority encoder	16	MSI	307
HC/HCT154	4-to-6 line decoder/demultiplexer	24	MSI	321
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches	16	MSI	450
HC/HCT238	3-to-8 line decoder/demultiplexer	16	MSI	451
HC/HCT4511	BCD to 7-segment latch/decoder/driver	16	MSI	879
HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	24	MSI	887
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	24	MSI	893
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	16	MSI	915
<b>Switches/multiplexers/demultiplexers</b>				
HC/HCT4016	quad bilateral switches (uncompensated switches)	14	SSI	683
HC/HCT4051	8-channel analog multiplexer/demultiplexer	16	MSI	759
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	16	MSI	771
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	16	MSI	783
HC/HCT4066	quad bilateral switches	14	SSI	809
HC/HCT4067	16-channel analog multiplexer/demultiplexer	24	SSI	810
HC/HCT4316	quad bilateral switches; with separate analog ground	16	MSI	821
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	20	MSI	835
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	20	MSI	849
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	20	MSI	863
<b>Bus transceivers</b>				
HC/HCT242*	quad bus transceiver; 3-state; inverting	14	MSI	467
HC/HCT243*	quad bus transceiver; 3-state	14	MSI	473
HC/HCT245*	octal bus transceiver; 3-state	20	MSI	483
HC/HCT640*	octal bus transceiver; 3-state; inverting	20	MSI	643
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	20	MSI	648
HC/HCT646*	octal bus transceiver/register; 3-state	24	MSI	653
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	24	MSI	659

\* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:  
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type no.	description	pins	classification	page
<b>Schmitt triggers</b>				
HC/HCT14	hex inverting Schmitt trigger	14	SSI	201
HC/HCT132	quad 2-input NAND Schmitt trigger	14	SSI	291
<b>One-shot multivibrators</b>				
HC/HCT123	dual retriggerable monostable multivibrator with reset	16	MSI	273
HC/HCT221	dual non-retriggerable monostable multivibrator with reset	16	MSI	448
HC/HCT423	dual retriggerable monostable multivibrator with reset	16	MSI	593
HC/HCT4538	dual retriggerable precision monostable multivibrator	14	MSI	910
<b>Miscellaneous</b>				
HC/HCT297	digital phase-locked-loop filter	16	MSI	529
HC/HCT4046A	phase-locked-loop with VCO	16	MSI	721
HC/HCT7046A	phase-locked-loop with lock detector	16	MSI	927

\* Types with a bus-driver output stage.

HC MOS 74HC/HCT/HCU FAMILY

type no.	description	page
HC/HCT00	quad 2-input NAND gate	167
HC/HCT02	quad 2-input NOR gate	171
HC/HCT03	quad 2-input NAND gate (with open drain outputs)	175
HC/HCT04	hex inverter	181
HCU04	hex inverter (unbuffered)	185
HC/HCT08	quad 2-input AND gate	190
HC/HCT10	triple 3-input NAND gate	193
HC/HCT11	triple 3-input AND gate	196
HC/HCT14	hex inverting Schmitt trigger	201
HC/HCT20	dual 4-input NAND gate	206
HC/HCT21	dual 4-input AND gate	209
HC/HCT27	triple 3-input NOR gate	211
HC/HCT30	8-input NAND gate	215
HC/HCT32	quad 2-input OR gate	219
HC/HCT42	BCD to decimal decoder (1-of-10)	223
HC58	dual AND-OR gate	225
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	226
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	231
HC/HCT75	quad bistable transparent latch	236
HC/HCT85	4-bit magnitude comparator	241
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	247
HC/HCT93	4-bit binary ripple counter	251
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	257
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	262
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger	267
HC/HCT123	dual retriggerable monostable multivibrator with reset	273
HC/HCT125*	quad buffer/line driver; 3-state; output enable active LOW	281
HC/HCT126*	quad buffer/line driver; 3-state; output enable active HIGH	286
HC/HCT132	quad 2-input NAND Schmitt trigger	291
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HC/HCT139	dual 2-to-4 line decoder/demultiplexer	302
HC/HCT147	10-to-4 line priority encoder	307
HC/HCT151	8-input multiplexer	311
HC/HCT153	dual 4-input multiplexer	316
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HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset	337
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\* Types with a bus driver output stage.

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HC/HCT164	8-bit serial-in/parallel-out shift register	363
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HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state	381
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	386
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	391
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HC/HCT182	look-ahead carry generator	398
HC/HCT190	presetable synchronous BCD decade up/down counter	403
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HC/HCT192	presetable synchronous BCD decade up/down counter	423
HC/HCT193	presetable synchronous 4-bit binary up/down counter	429
HC/HCT194	4-bit bidirectional universal shift register	435
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HC/HCT221	dual non-retriggerable monostable multivibrator with reset	448
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches	450
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HC/HCT240*	octal buffer/line driver; 3-state; inverting	456
HC/HCT241*	octal buffer/line driver; 3-state; output enables active LOW or HIGH	461
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HC/HCT244*	octal buffer/line driver; 3-state; output enable active LOW	478
HC/HCT245*	octal bus transceiver; 3-state	483
HC/HCT251	8-input multiplexer; 3-state	488
HC/HCT253B*	dual 4-input multiplexer; 3-state	494
HC/HCT257*	quad 2-input multiplexer; 3-state	499
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HC/HCT259	8-bit addressable latch	505
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HC/HCT280	9-bit odd/even parity generator/checker	519
HC/HCT283	4-bit binary full adder with fast carry	523
HC/HCT297	digital phase-locked-loop filter	529
HC/HCT299*	8-bit universal shift register; 3-state	537
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	545
HC/HCT356*	8-input multiplexer/register; 3-state	547
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\* Types with a bus driver output stage.

# NUMERICAL INDEX

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HC/HCT390	dual decade ripple counter	581
HC/HCT393	dual 4-bit binary ripple counter	587
HC/HCT423	dual retriggerable monostable multivibrator with reset	593
HC/HCT533*	octal D-type transparent latch; 3-state; inverting	601
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\* Types with a bus driver output stage.

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HC/HCT7046A	phase-locked-loop with lock detector	927
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\* Types with a bus driver output stage.

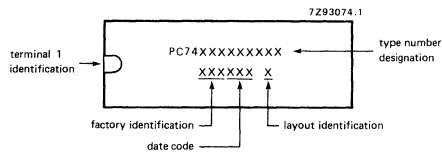
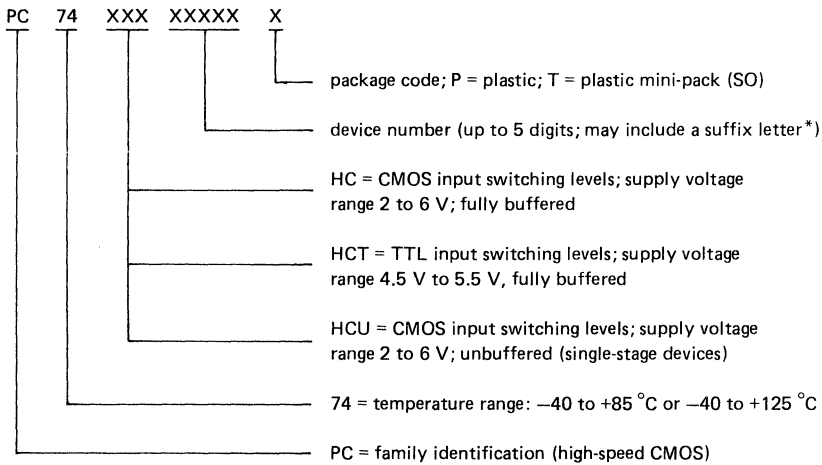




## ORDERING INFORMATION



TYPE NUMBER DESIGNATIONS



\* Example suffix "B": this type has bus driver output capability in contrast with the plane version.



## RATING SYSTEMS



## **RATING SYSTEMS**

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

### **DEFINITIONS OF TERMS USED**

#### **Electronic device.**

An electronic tube or valve, transistor or other semiconductor device.

Note: This definition excludes inductors, capacitors, resistors and similar components.

#### **Characteristic**

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

#### **Bogey electronic device**

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

#### **Rating**

A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note: Limiting conditions may be either maxima or minima.

#### **Rating system**

The set of principles upon which ratings are established and which determine their interpretation.

Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

### **ABSOLUTE MAXIMUM RATING SYSTEM**

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

### **DESIGN MAXIMUM RATING SYSTEM**

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

### **DESIGN CENTRE RATING SYSTEM**

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.



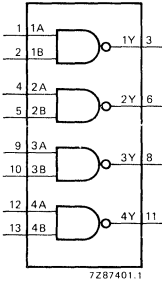


**FUNCTIONAL DIAGRAMS**

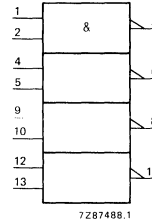
**IEC LOGIC DIAGRAMS**



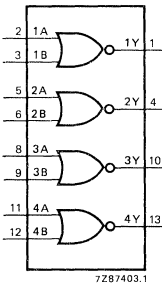
HC/HCT00



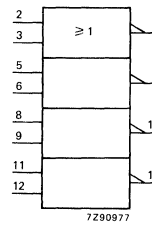
Quad 2-input NAND gate



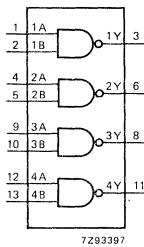
HC/HCT02



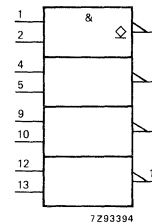
Quad 2-input NOR gate



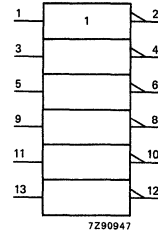
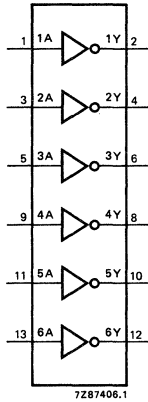
HC/HCT03



Quad 2-input NAND gate

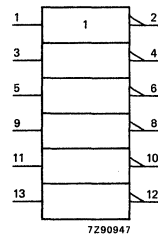
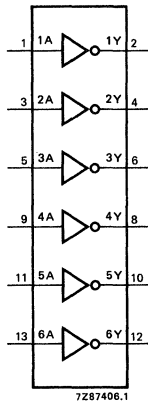


### HC/HCT04



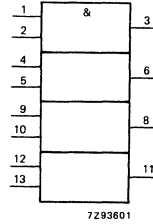
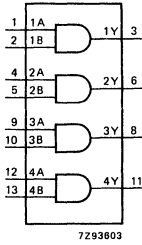
Hex inverter

### HCU04



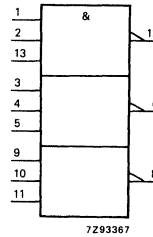
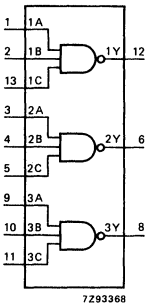
Hex inverter (unbuffered)

HC/HCT08



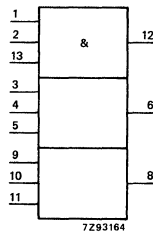
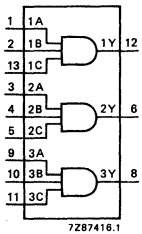
Quad 2-input AND gate

HC/HCT10



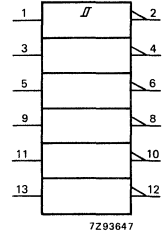
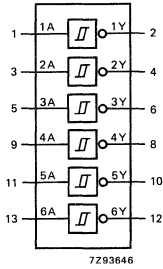
Triple 3-input NAND gate

HC/HCT11



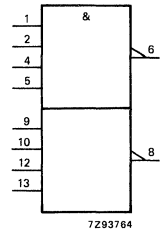
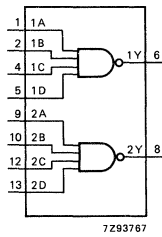
Triple 3-input AND gate

HC/HCT14



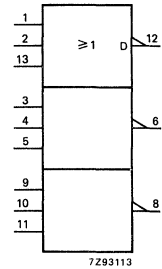
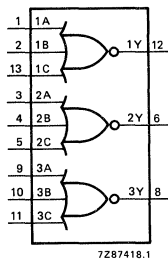
Hex inverting Schmitt trigger

HC/HCT20



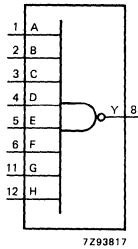
Dual 4-bit NAND gate

HC/HCT27

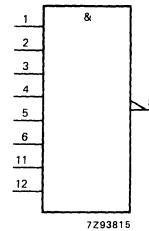


Triple 3-input NOR gate

HC/HCT30



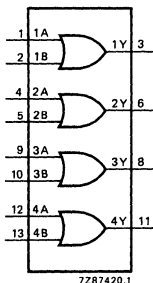
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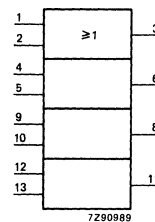
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8-input NAND gate

HC/HCT32



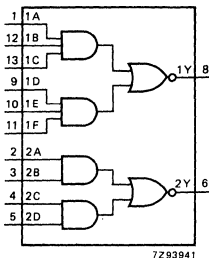
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7290989

Quad 2-input OR gate

HC58



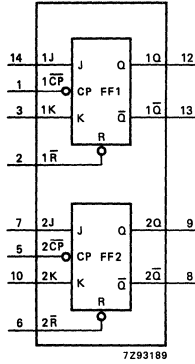
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IEC SYMBOL  
IN  
PROGRESS

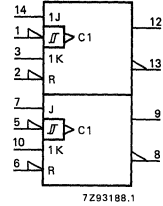
Dual AND-OR gate



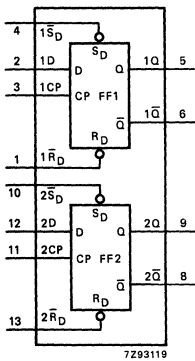
HC/HCT73



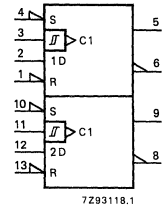
Dual JK flip-flop with reset; negative-edge trigger



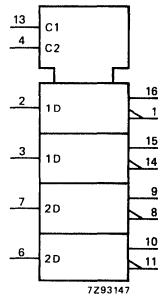
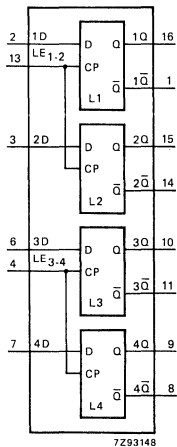
HC/HCT74



Dual D-type flip-flop with set and reset; positive-edge trigger

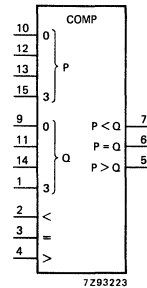
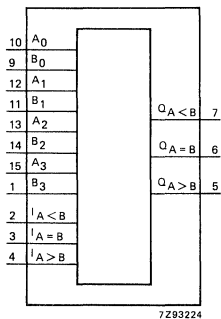


HC/HCT75



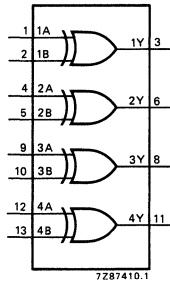
Quad bistable transparent latch

HC/HCT85

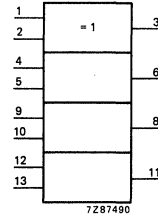


4-bit magnitude comparator

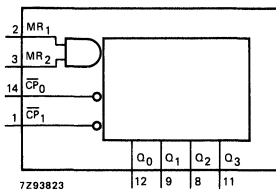
HC/HCT86



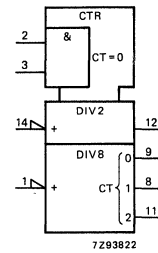
Quad 2-input EXCLUSIVE-OR gate



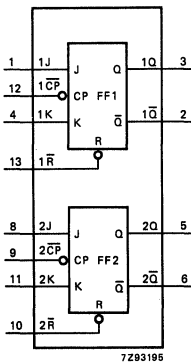
HC/HCT93



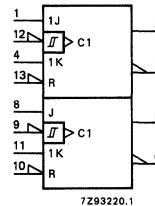
4-bit binary ripple counter



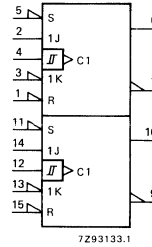
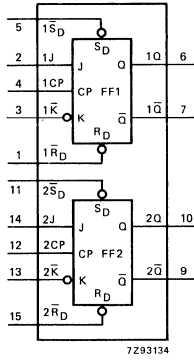
HC/HCT107



Dual JK flip-flop with reset; negative-edge trigger

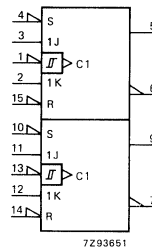
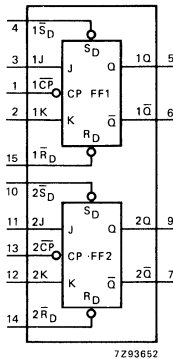


HC/HCT109



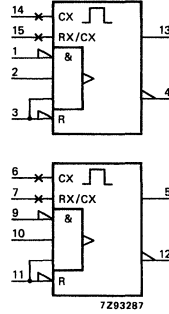
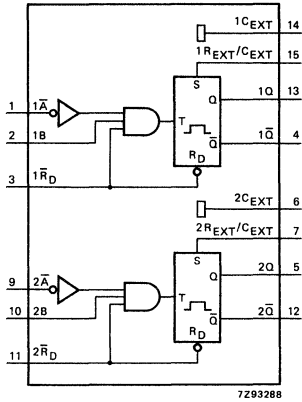
Dual JK flip-flop with set and reset; positive-edge trigger

HC/HCT112



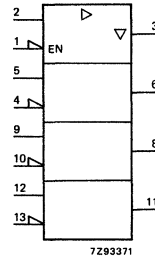
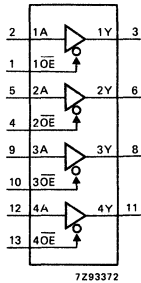
Dual JK flip-flop with set and reset; negative-edge trigger

HC/HCT123



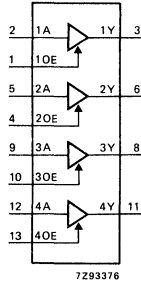
Dual retriggerable monostable multivibrator with reset

HC/HCT125

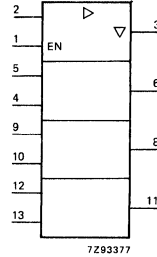


Quad buffer/line driver; 3-state

HC/HCT126



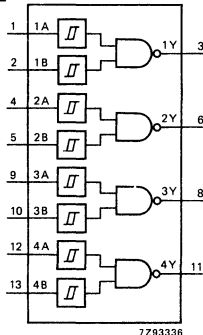
7293376



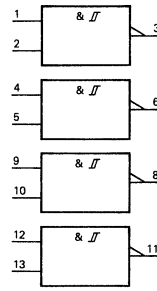
7293377

Quad buffer/line driver; 3-state

HC/HCT132



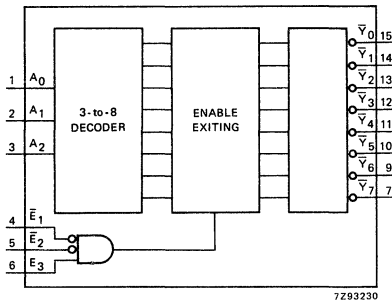
7293336



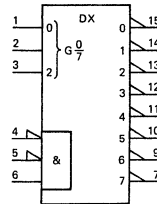
7293335

Quad 2-input NAND Schmitt trigger

HC/HCT138



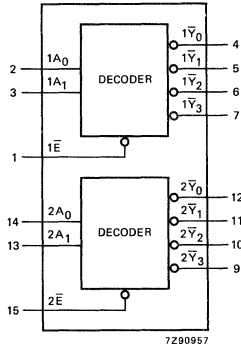
7293230



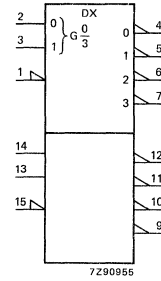
7293229.1

3-to-8 line decoder/demultiplexer; inverting

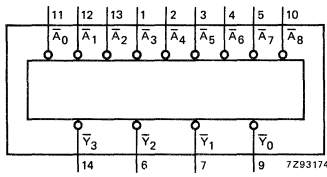
HC/HCT139



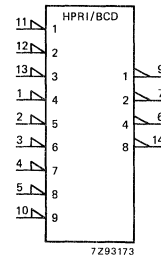
Dual 2-to-4 line decoder/demultiplexer



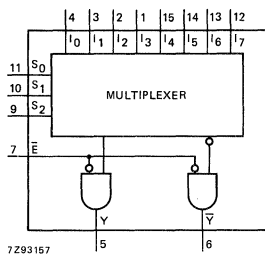
HC/HCT147



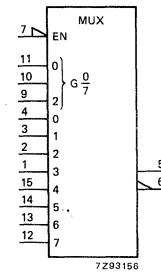
10-to-4 line priority encoder



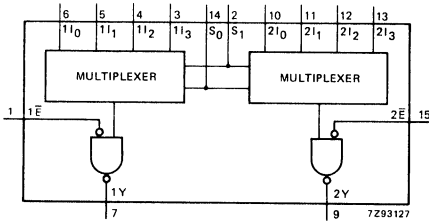
HC/HCT151



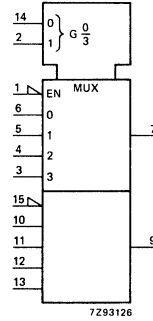
8-input multiplexer



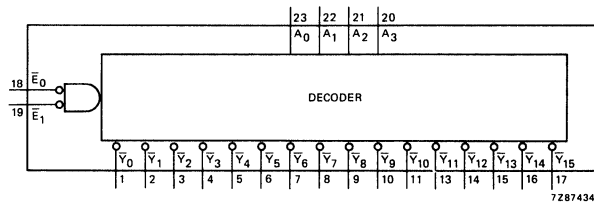
HC/HCT153



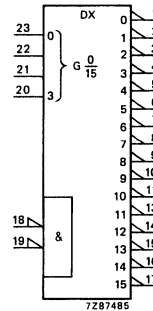
Dual 4-input multiplexer



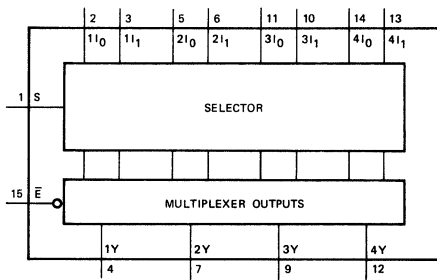
HC/HCT154



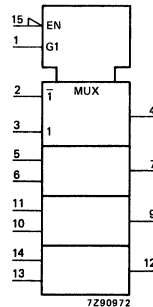
4-to-16 line decoder/demultiplexer



HC/HCT157

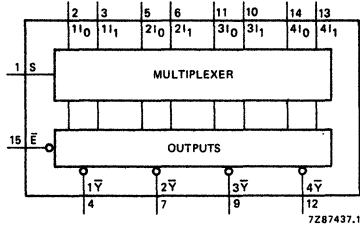


Quad 2-input multiplexer



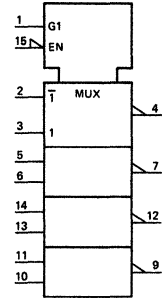


HC/HCT158



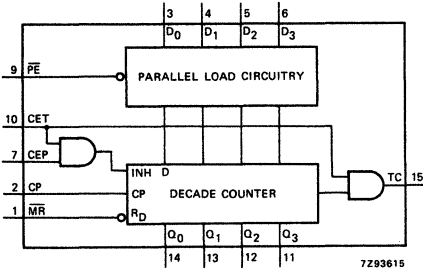
7287437.1

Quad 2-input multiplexer; inverting



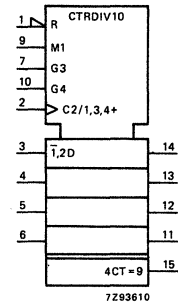
7287494.1

HC/HCT160



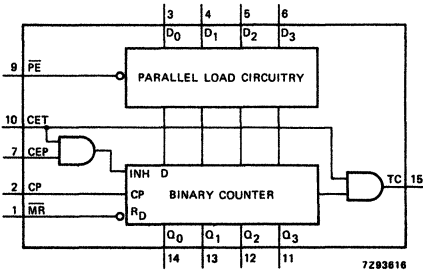
7293615

Presettable synchronous BCD decade counter; asynchronous reset



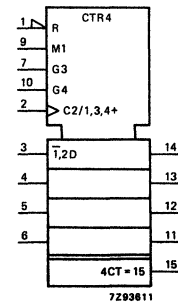
7293610

HC/HCT161



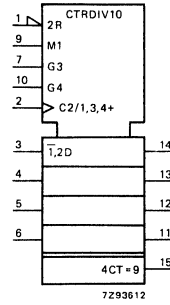
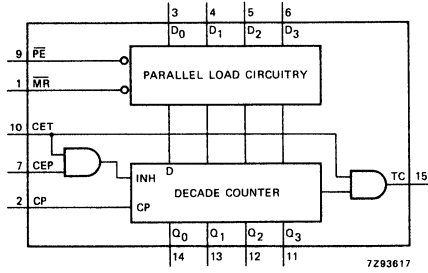
7293816

Presettable synchronous 4-bit binary counter; asynchronous reset



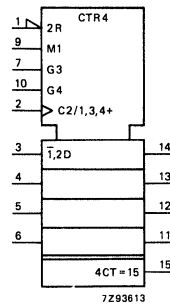
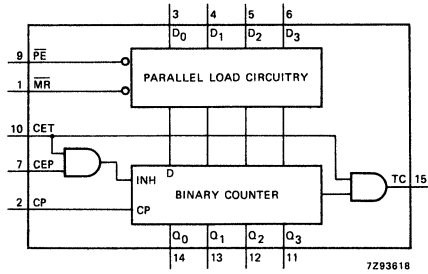
7293811

HC/HCT162



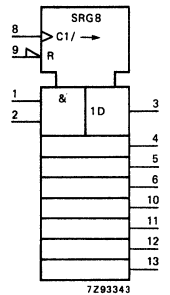
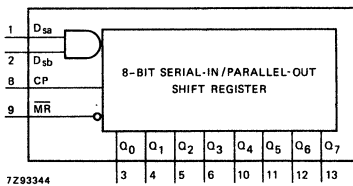
Pre-settable synchronous BCD decade counter; synchronous reset

HC/HCT163



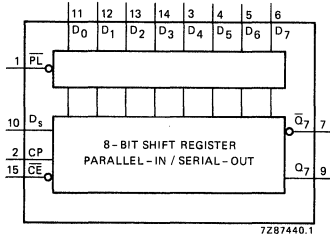
Pre-settable synchronous 4-bit binary counter; synchronous reset

HC/HCT164

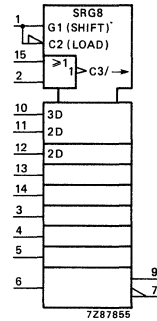


8-bit serial-in/parallel-out shift register

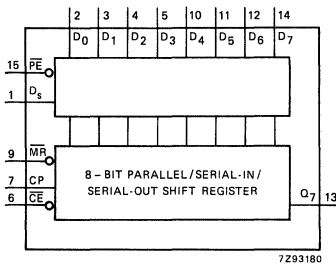
HC/HCT165



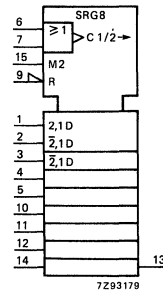
8-bit parallel-in/serial-out shift register



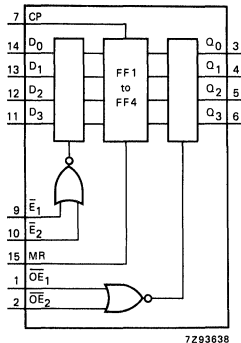
HC/HCT166



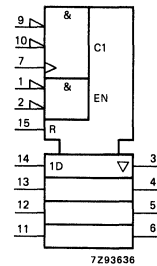
8-bit parallel-in/serial-out shift register



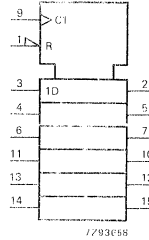
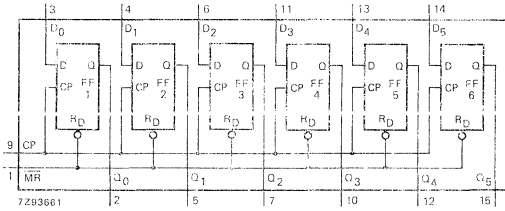
HC/HCT173



Quad D-type flip-flop; positive-edge trigger; 3-state

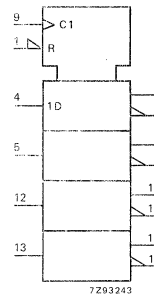
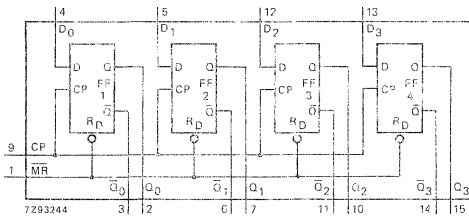


HC/HCT174



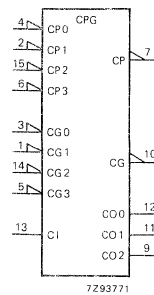
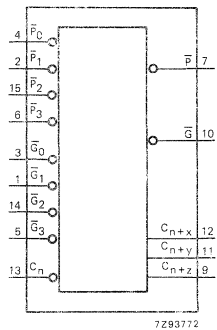
Hex D-type flip-flop with reset; positive-edge trigger

HC/HCT175



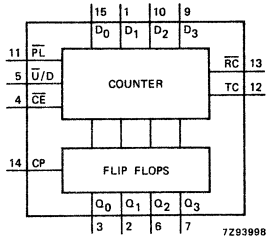
Quad D-type flip-flop with reset; positive-edge trigger

HC/HCT182

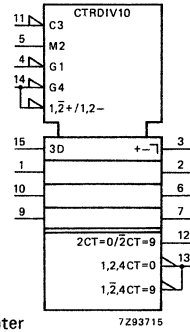


Look-ahead carry generator

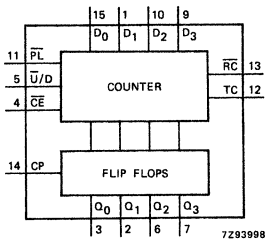
HC/HCT190



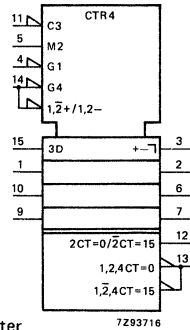
7293988  
Presettable synchronous BCD decade up/down counter



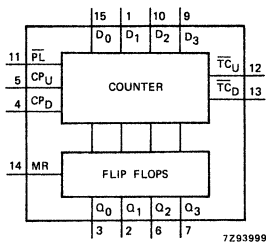
HC/HCT191



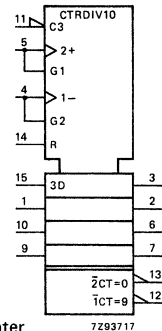
7293988  
Presettable synchronous 4-bit binary up/down counter



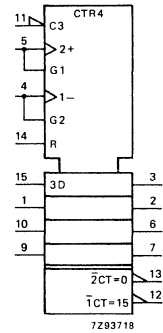
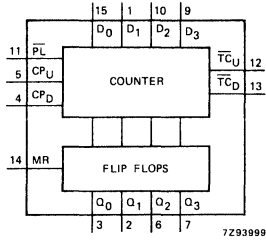
HC/HCT192



7293999  
Presettable synchronous BCD decade up/down counter

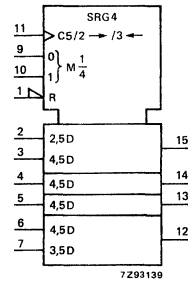
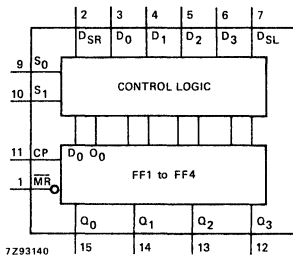


HC/HCT193



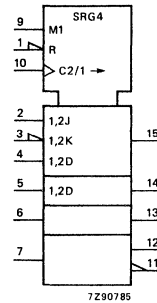
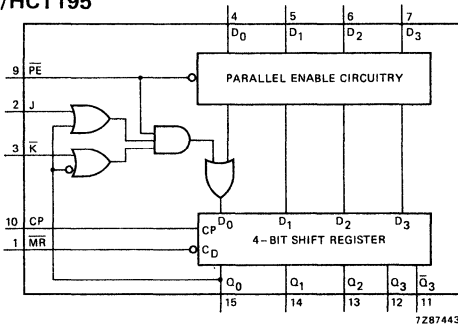
Presettable synchronous 4-bit binary up/down counter

HC/HCT194



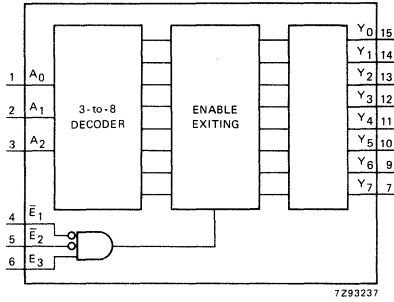
4-bit bidirectional universal shift register

HC/HCT195



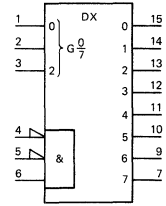
4-bit parallel access shift register

HC/HCT238



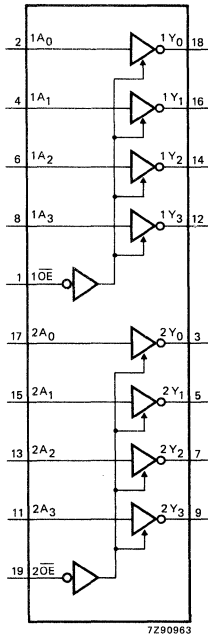
7293237

3-to-8 line decoder/demultiplexer



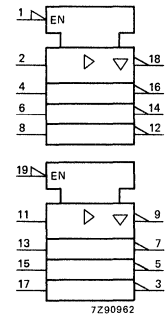
7293236.1

HC/HCT240



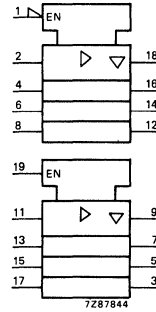
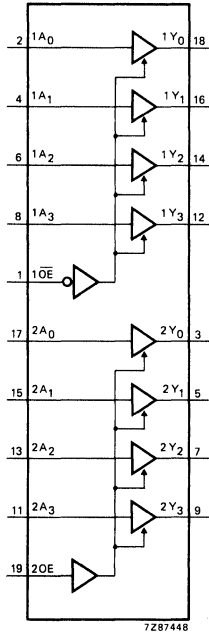
7290963

Octal buffer/line driver; 3-state; inverting



7290962

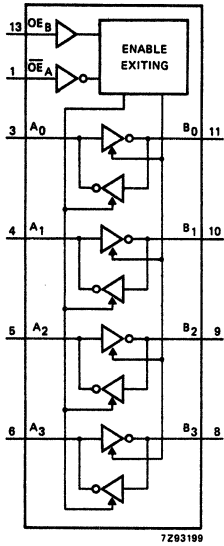
HC/HCT241



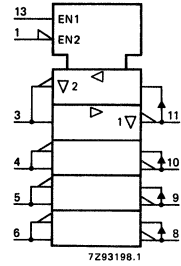
Octal buffer/line driver; 3-state



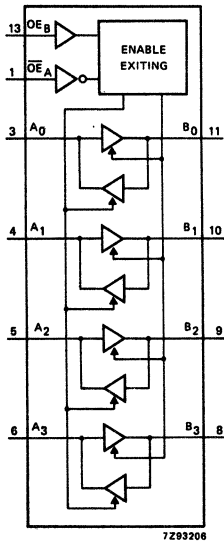
HC/HCT242



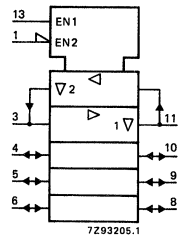
Quad bus transceiver; 3-state; inverting



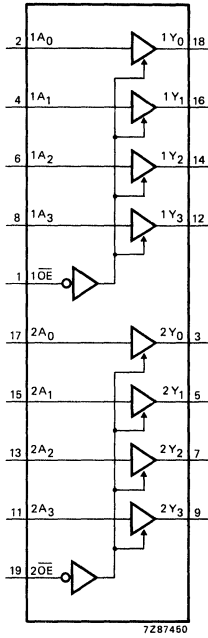
HC/HCT243



Quad bus transceiver; 3-state

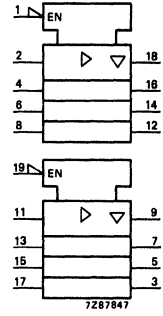


HC/HCT244

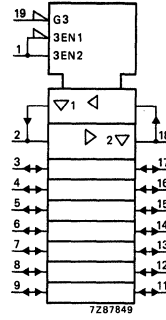
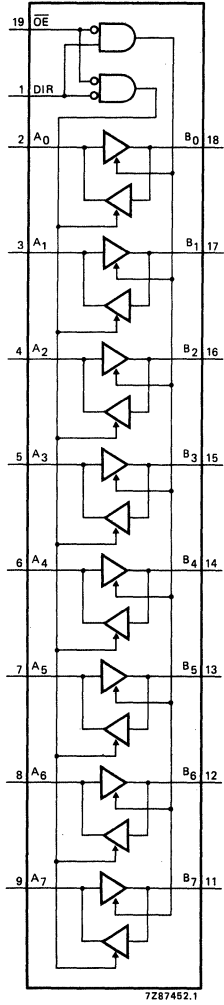


7287460

Octal buffer/line driver; 3-state

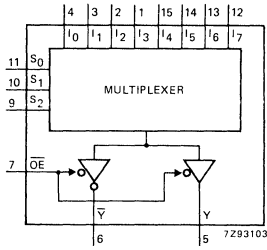


HC/HCT245

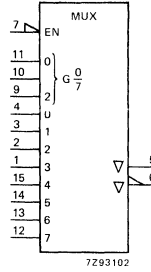


Octal bus transceiver; 3-state

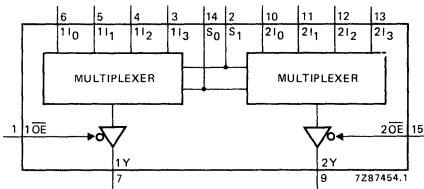
HC/HCT251



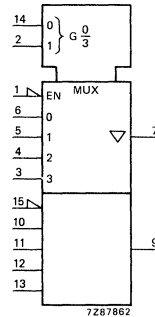
8-input multiplexer; 3-state



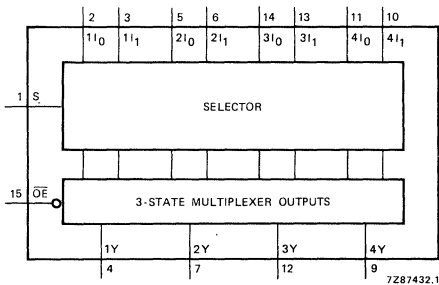
HC/HCT253B



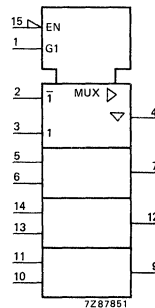
Dual 4-input multiplexer; 3-state



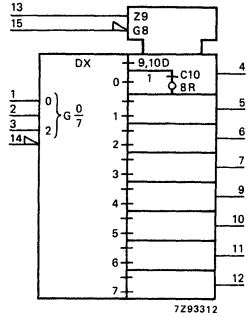
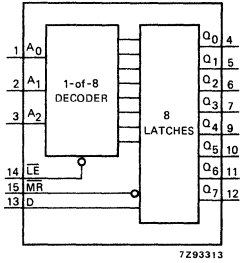
HC/HCT257



Quad 2-input multiplexer; 3-state

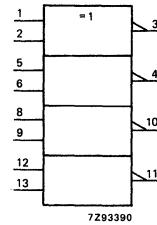
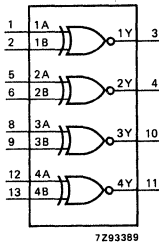


HC/HCT259



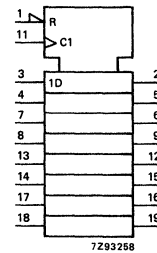
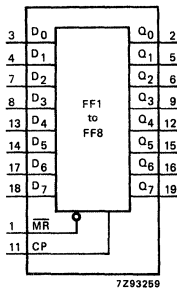
8-bit addressable latch

HC7266



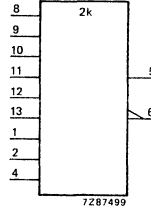
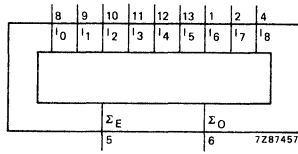
Quad 2-input EXCLUSIVE-NOR gate

HC/HCT273



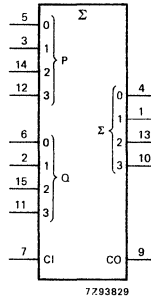
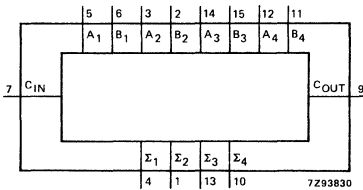
Octal D-type flip-flop with reset; positive-edge trigger

HC/HCT280



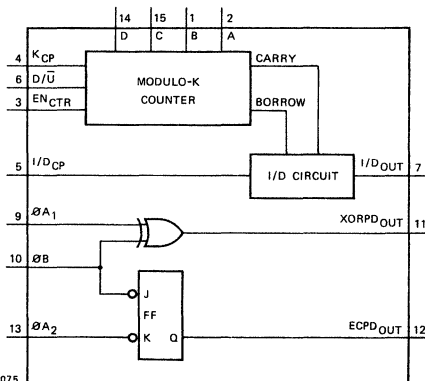
9-bit odd/even parity generator/checker

HC/HCT283



4-bit binary full adder with fast carry

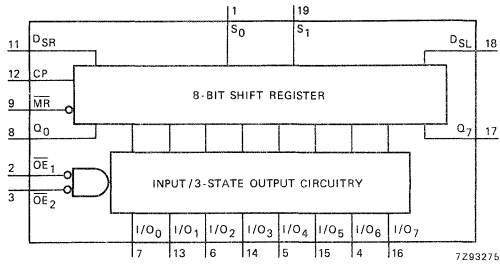
HC/HCT297



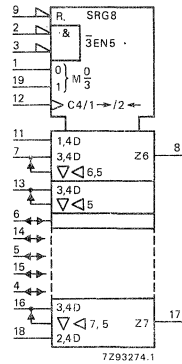
IEC SYMBOL  
IN  
PROGRESS

Digital phase-locked-loop filter

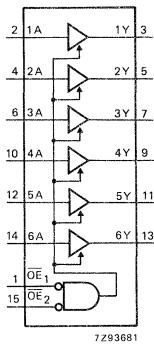
HC/HCT299



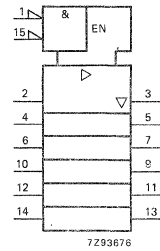
8-bit universal shift register; 3-state



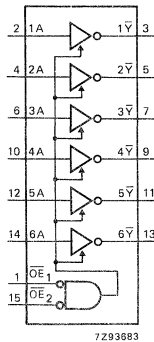
HC/HCT365



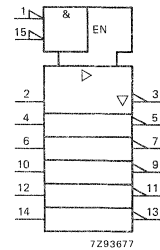
Hex buffer/line driver; 3-state



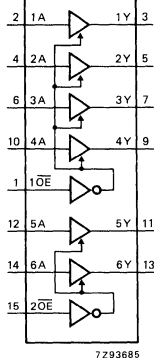
HC/HCT366



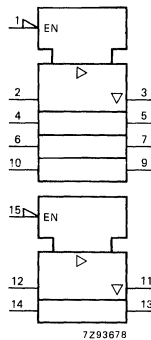
Hex buffer/line driver; 3-state; inverting



HC/HCT367

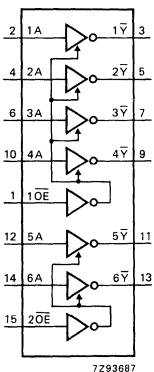


Hex buffer/line driver; 3-state

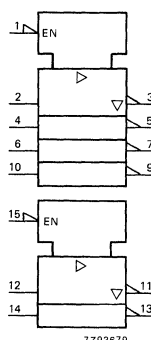


7293678

HC/HCT368

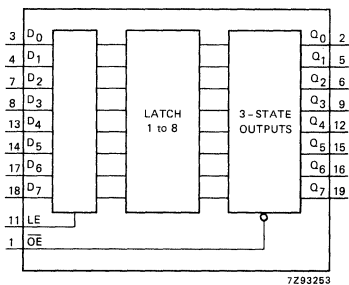


Hex buffer/line driver; 3-state; inverting



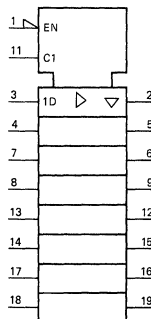
7293679

HC/HCT373



7293263

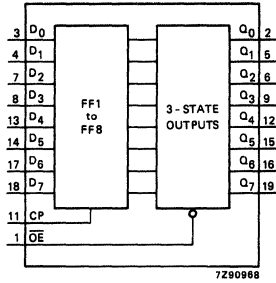
Octal D-type transparent latch; 3-state



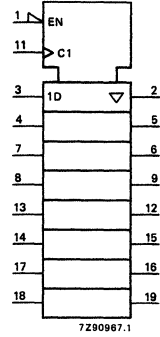
7293262



HC/HCT374

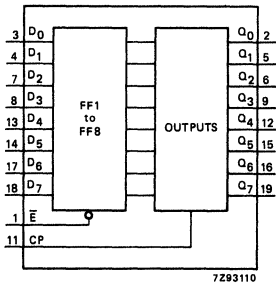


Octal D-type flip-flop; positive-edge trigger; 3-state

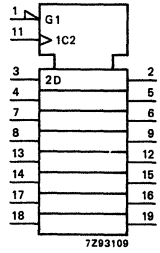


7290967.1

HC/HCT377

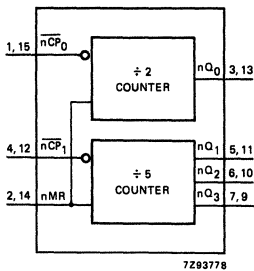


Octal D-type flip-flop with data enable; positive-edge trigger

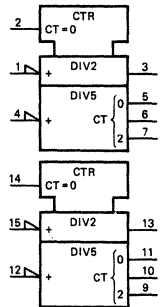


7293109

HC/HCT390

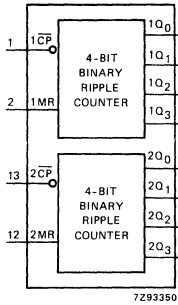


Dual decade ripple counter

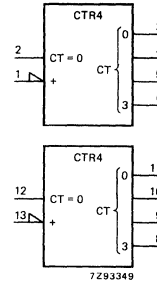


7293777

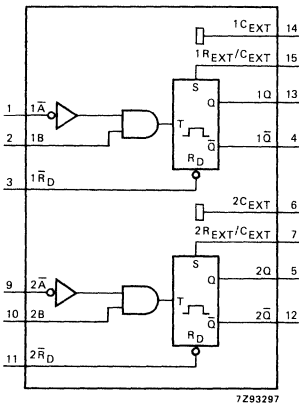
HC/HCT393



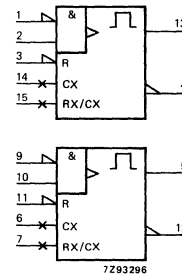
Dual 4-bit binary ripple counter



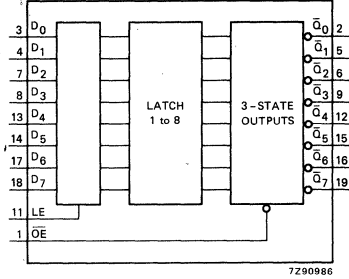
HC/HCT423



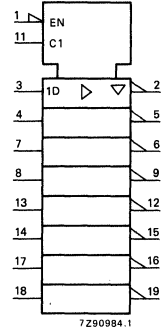
Dual retriggerable monostable multivibrator with reset



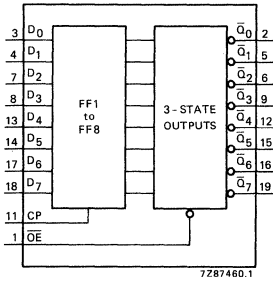
HC/HCT533



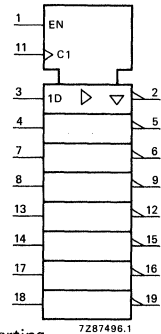
Octal D-type transparent latch; 3-state; inverting



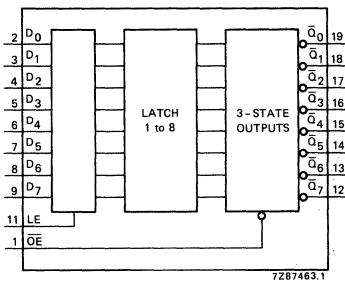
HC/HCT534



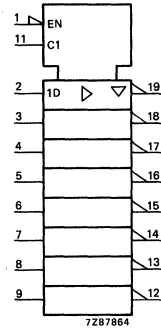
Octal D-type flip-flop; positive-edge trigger; 3-state; inverting



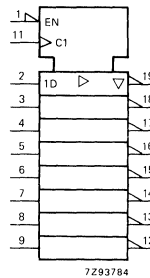
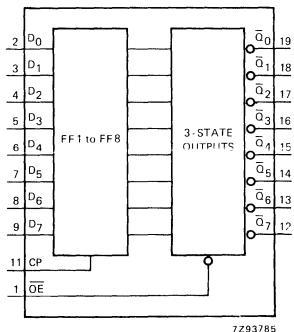
HC/HCT563



Octal D-type transparent latch; 3-state; inverting

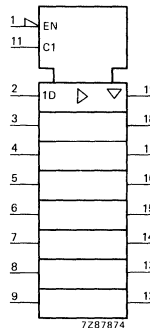
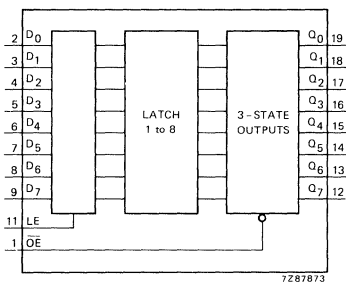


HC/HCT564



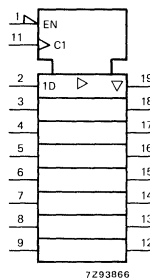
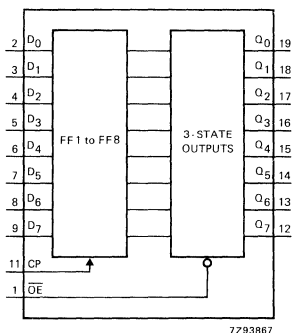
Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

HC/HCT573



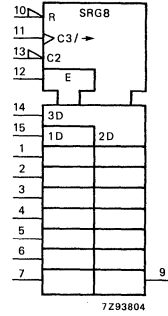
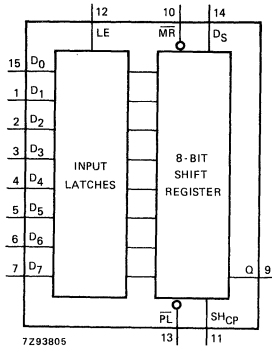
Octal D-type transparent latch; 3-state

HC/HCT574



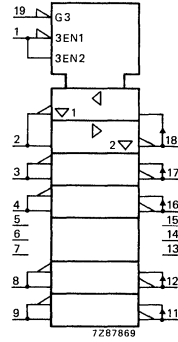
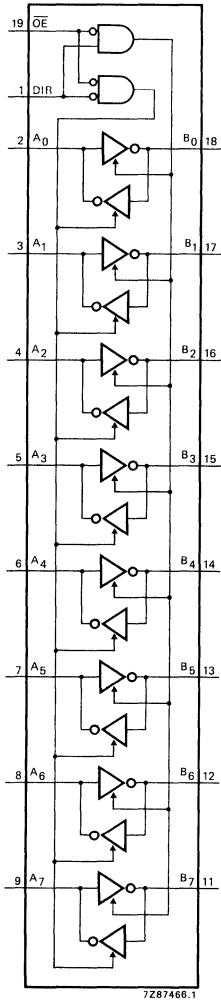
Octal D-type flip-flop; positive-edge trigger; 3-state

HC/HCT7597



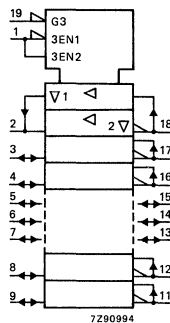
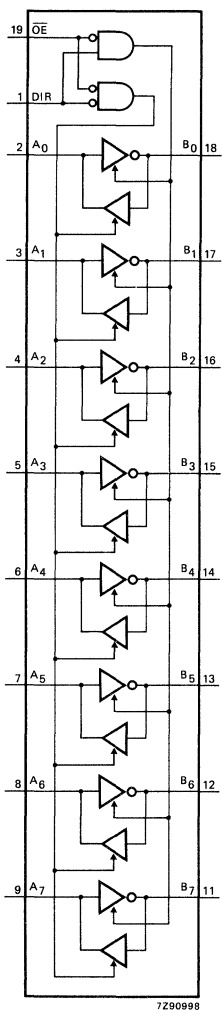
8-bit shift register with input latches

HC/HCT640



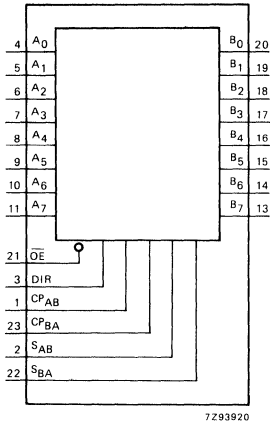
Octal bus transceiver; 3-state; inverting

HC/HCT643



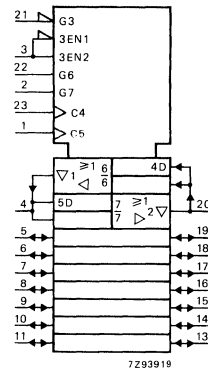
Octal bus transceiver; 3-state; true/inverting

HC/HCT646



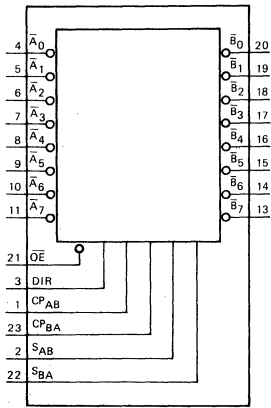
7293920

Octal bus transceiver/register; 3-state



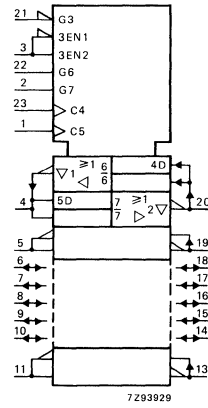
7293919

HC/HCT648



7293930

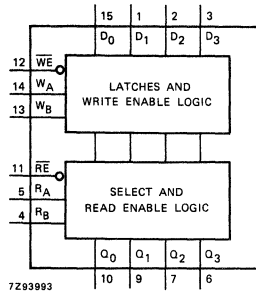
Octal bus transceiver/register; 3-state; inverting



7293929

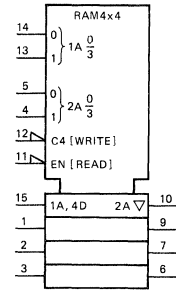


HC/HCT670



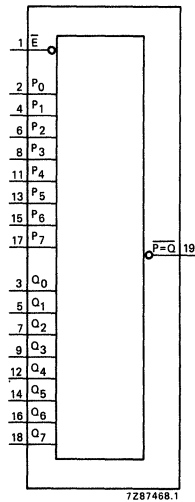
7293993

4 x 4 register file; 3-state



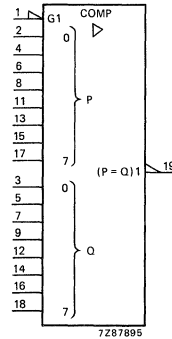
7293912

HC/HCT688



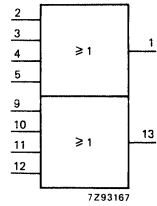
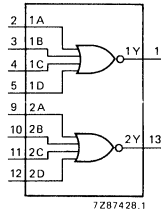
7287468.1

8-bit magnitude comparator



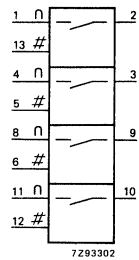
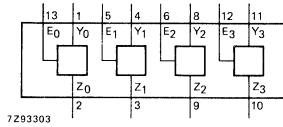
7287885

HC/HCT4002



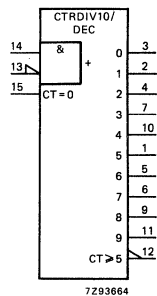
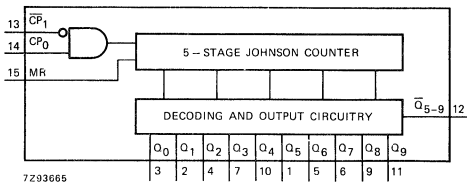
Dual 4-input NOR gate

HC/HCT4016



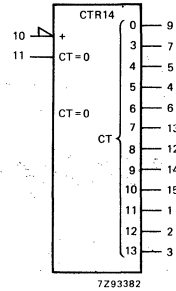
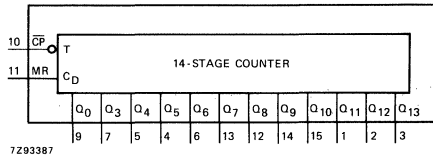
Quad bilateral switches

HC/HCT4017



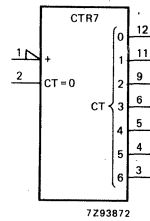
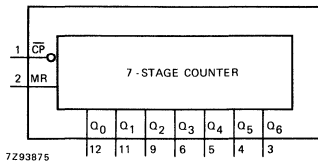
Johnson decade counter with 10 decoded outputs

HC/HCT4020



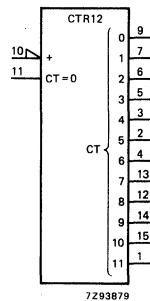
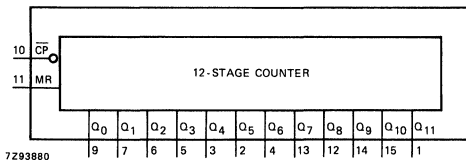
14-stage binary ripple counter

HC/HCT4024



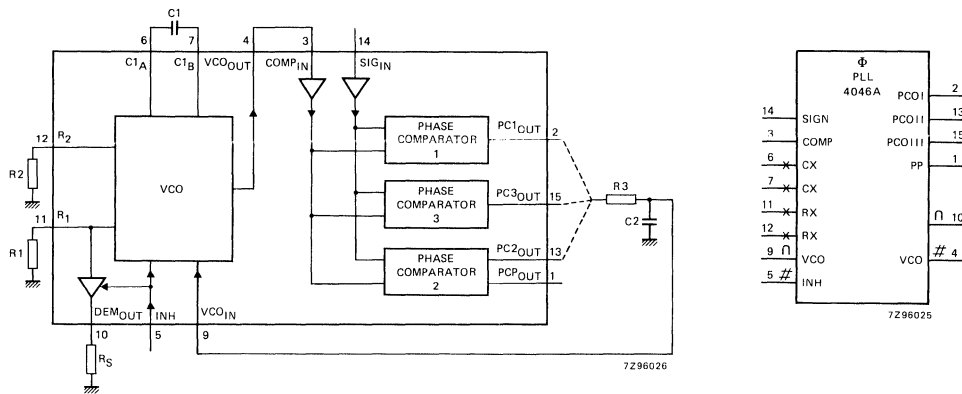
7-stage binary ripple counter

HC/HCT4040



12-stage binary ripple counter

HC/HCT4046A



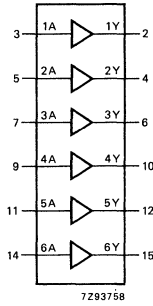
Phase-locked-loop with VCO

HC4049



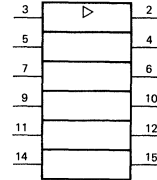
Hex inverting HIGH-to-LOW level shifter

HC4050



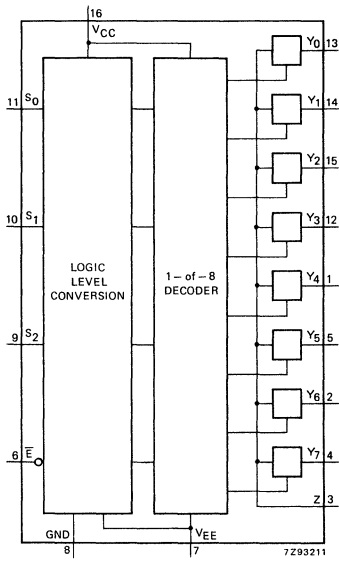
7293758

Hex HIGH-to-LOW level shifter



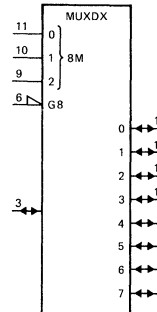
7293759

HC/HCT4051



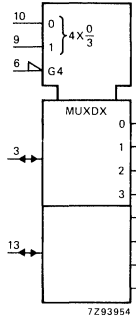
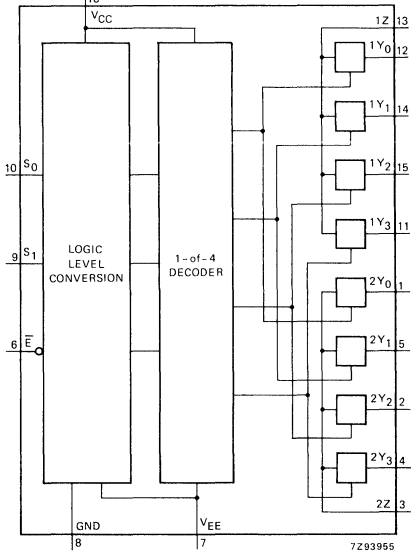
7293211

8-channel analog multiplexer/demultiplexer



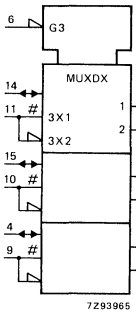
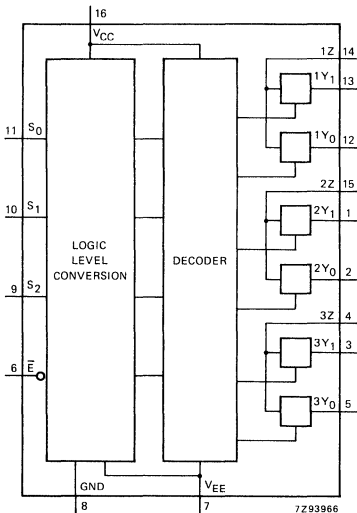
7293210.1

HC/HCT4052



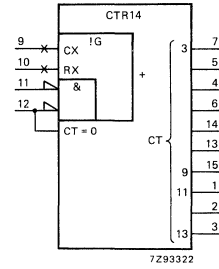
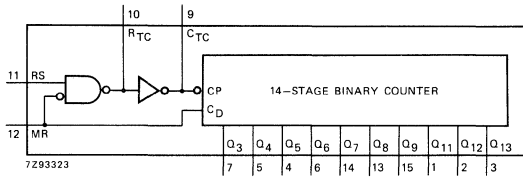
Dual 4-channel analog multiplexer/demultiplexer

HC/HCT4053



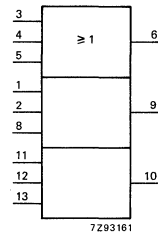
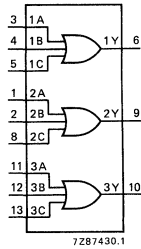
Triple 2-channel analog multiplexer/demultiplexer

HC/HCT4060



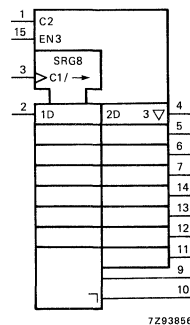
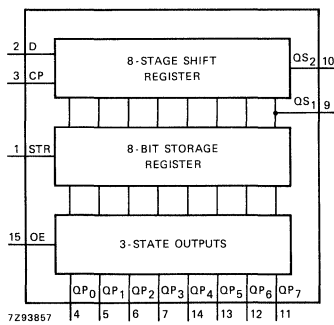
14-stage binary ripple counter with oscillator

HC/HCT4075



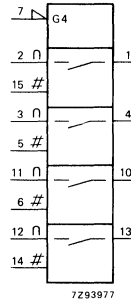
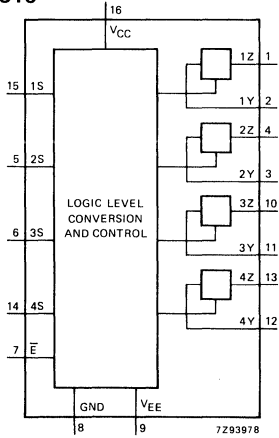
Triple 3-input OR gate

HC/HCT4094



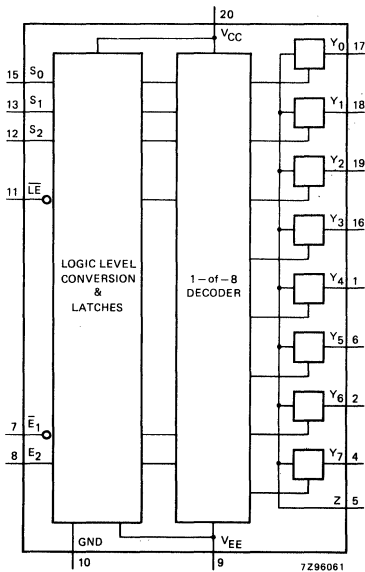
8-stage shift-and-store bus register

HC/HCT4316



Quad bilateral switches

HC/HCT4351

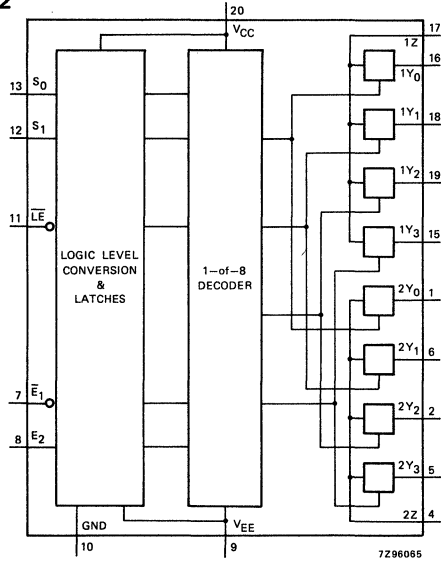


IEC SYMBOL  
IN  
PROGRESS

8-channel analog multiplexer/demultiplexer with latch



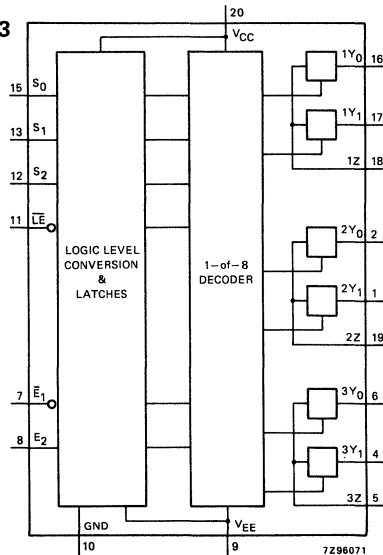
HC/HCT4352



Dual 4-channel analog multiplexer/demultiplexer with latch

IEC SYMBOL  
IN  
PROGRESS

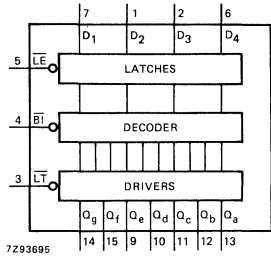
HC/HCT4353



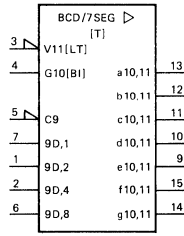
Triple 2-channel analog multiplexer/demultiplexer with latch

IEC SYMBOL  
IN  
PROGRESS

HC/HCT4511



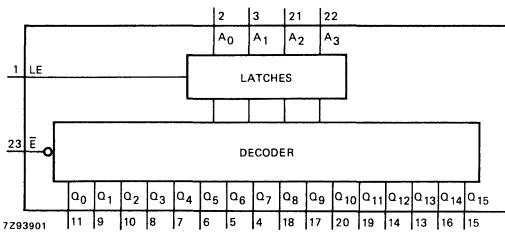
7293695



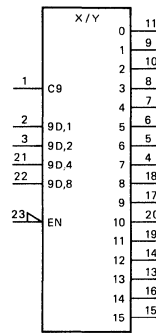
7293694

BCD to 7-segment latch/decoder/driver

HC/HCT4514

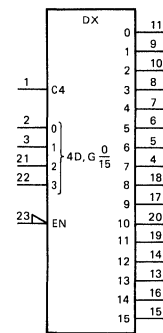


7293901



7293898

decoder

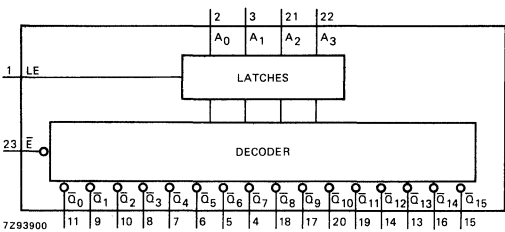


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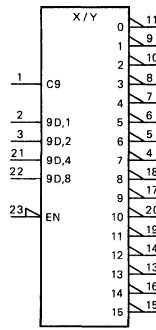
demultiplexer

4-to-16 line decoder/demultiplexer with input latches

HC/HCT4515

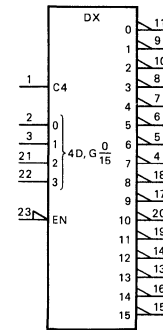


7293900



7293899

decoder

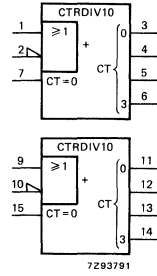
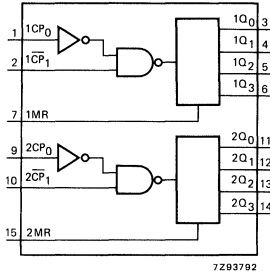


7293938

demultiplexer

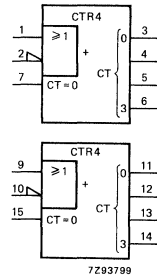
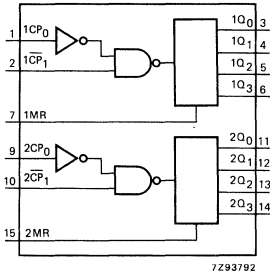
4-to-16 line decoder/demultiplexer with input latches

HC/HCT4518



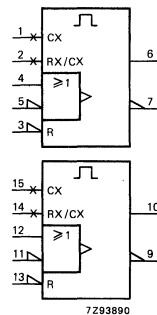
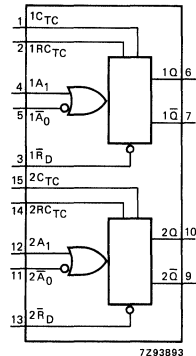
Dual synchronous BCD counter

HC/HCT4520



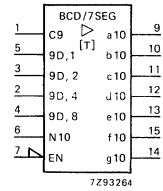
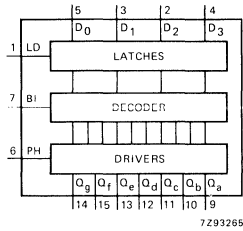
Dual synchronous 4-bit binary counter

HC/HCT4538



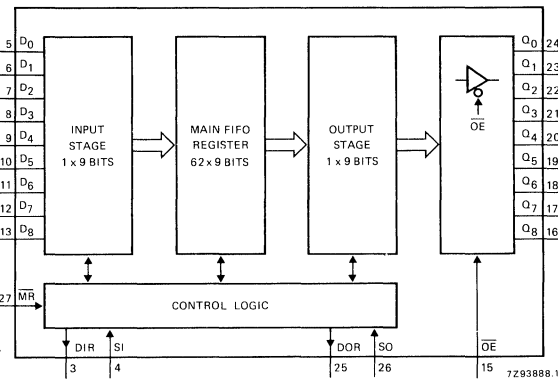
Dual retriggerable precision monostable multivibrator

HC/HCT4543



BCD to 7-segment latch/decoder/driver for LCDs

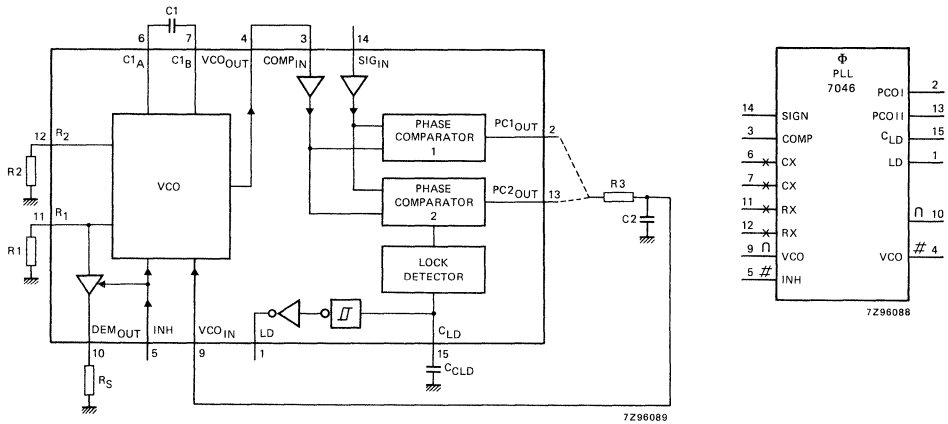
HC/HCT7030



IEC SYMBOL  
IN  
PROGRESS

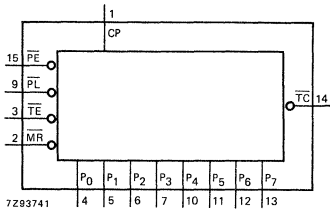
9-bit x 64-word FIFO register; 3-state

HC/HCT7046A



Phase-locked-loop with lock detector

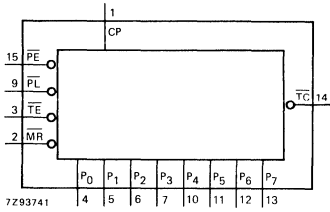
HC/HCT40102



IEC SYMBOL  
IN  
PROGRESS

8-bit synchronous BCD down counter

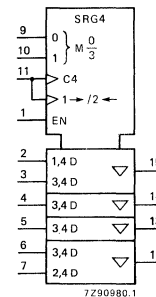
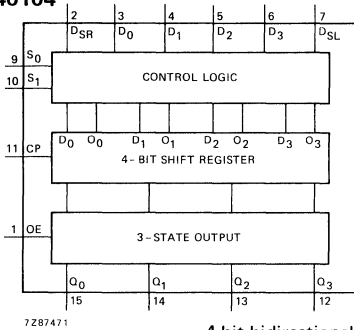
HC/HCT40103



IEC SYMBOL  
IN  
PROGRESS

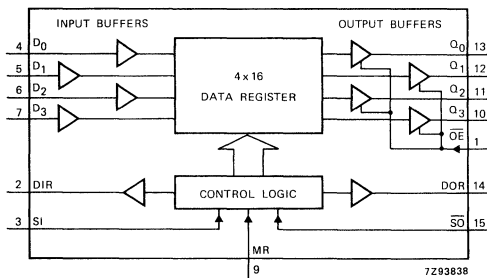
8-bit synchronous binary down counter

HC/HCT40104



4-bit bidirectional universal shift register; 3-state

HC/HCT40105



IEC SYMBOL  
IN  
PROGRESS

4-bit x 16-word FIFO register



## IEC SYMBOLOGY

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SUMMARY OF IEC SYMBOLOGY

INTRODUCTION

The logic symbology used in the HCMOS published data follows the system developed by the International Electro-technical Commission (IEC). The representation is very effective in that it shows the exact relationship between every input and output of digital circuits without having to detail internal logic. Basic logic functions are represented by symbols; in the symbols for more complex functions, use is made of 'dependency notation' that specified inter-relationships of the digital inputs/outputs.

This summary describes the various elements used in symbol construction and the rules and definitions that apply.

SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols (Fig. 1). The purpose of a general qualifying-symbol is to accurately portray the logic function of the element and those used in this handbook are listed in Table 1. The preferred direction of signal flow through symbols and associated circuit is from left to right; inputs are on the left and outputs on the right. Exceptions to this convention are indicated by arrowheads in the signal lines showing the direction of signal flow, as shown in Fig. 12.

All outputs of a single element of a symbol have internal logic states that are determined by the element's function, unless otherwise indicated by an associated qualifying-symbols.

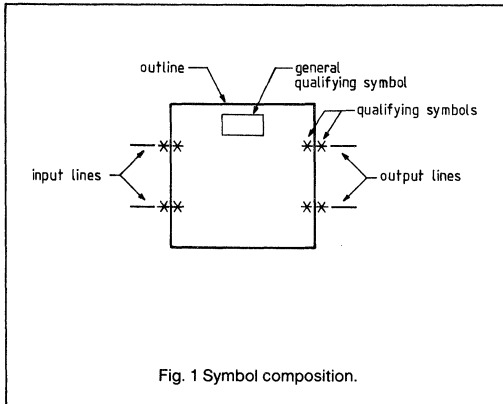


Fig. 1 Symbol composition.

Adjacent elements in a composite symbol may be joined by a common boundary line. When this boundary line is parallel to the direction of signal flow there is no logic connection between the elements, but when the line is perpendicular to the direction of signal flow then there is at least one logic connection between them. The number of logic connections between elements is shown by qualifying-symbols, but if there are no qualifying-symbols on either side of the common line then the elements have just one logic connection.

When a composite symbol contains at least one input common to one or more of the elements, a common-control block can be used. In the example of Fig. 2 the common-control block provides an input to each of the elements below it, this can be otherwise qualified by dependency notation.

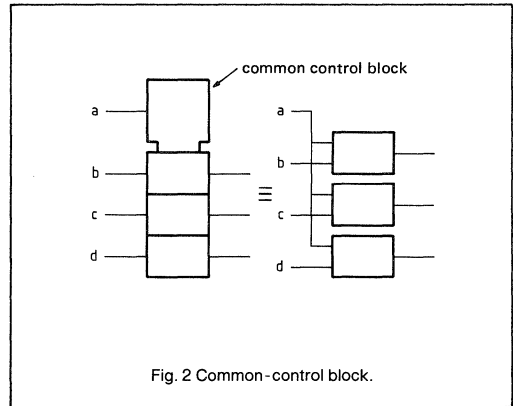


Fig. 2 Common-control block.

An output that depends on all elements of a composite symbol can be shown as an output from a common-output element. This part of the symbol is distinguishable by a double boundary line as shown in Fig. 3. The common-output element may have other inputs. Its function must be indicated by a qualifying-symbols within the outline.

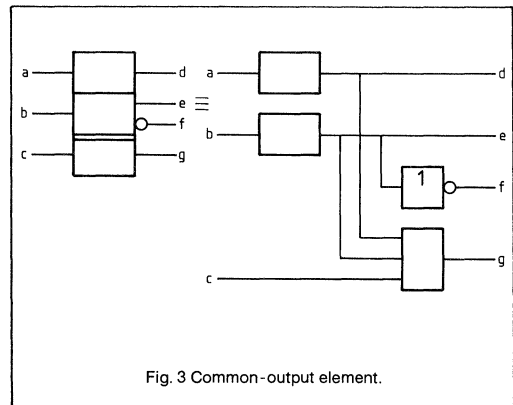










Fig. 3 Common-output element.

QUALIFYING SYMBOLS

General qualifying-symbols

Table 1 shows the general qualifying-symbols used in this publication. These characters are usually placed near the top centre of a symbol element and define the logic function that is represented by the symbol or element.

Table 1 Qualifying-symbols - General

qualifying-symbol	definition	qualifying-symbol	definition
&	AND element. If all inputs are at internal logic "1" then the output is at internal logic "1"	P-Q	Subtractor
> m	Logic threshold element. If at least m inputs are at internal logic "1" then the output is at internal logic "1"	CPG	Look-ahead carry generator
> 1	OR element. If at least one input is at internal logic "1" then the output is at internal logic "1"	II	Multiplier
= m	m-out-of-n element. Given that $m < n$ ; if m inputs are at internal logic "1" then the output is at internal logic "1"	COMP	Comparator
= 1	EXCLUSIVE-OR element. If only one input is at internal logic "1" then the output is at internal logic "1"	ALU	Arithmetic logic unit
=	Logic identity element. If all inputs have the same logic state then the output is at internal logic "1"		Retriggerable monostable element
> n/2	Majority element. If the majority of inputs are at internal logic "1" then the output is at internal logic "1"		Non-retriggerable monostable element
2k	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1"		Astable element
2k + 1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1"		Synchronous-starting astable element
1	Buffer element without amplified output. If the input is at internal logic "1" then the output is at internal logic "1"		Synchronous-stopping astable element
 or 	Buffer element with amplified output. The triangle points in the direction of signal flow	SGRm	Shift register. "m" = number of bits
	Bi-threshold detector. Schmitt-trigger	CTRm	Binary counter. "m" = number of bits or is an indication of the cycle length $2^m$
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used	CTRDIVm	Counter with cycle length m
MUX	Multiplexer/ data selector	ROMm1xm2	Read only memory
DX	Demultiplexer	PROMm1xm2	Programmable read only memory
MUXDX	Bidirectional selector	RAMm1xm2	Random access memory
$\Sigma$	Adder	CAMm1xm2	Associative memory
		FIFOm1xm2	First-in/first-out memory
		I=0	Initial logic "0" state. When power is switched ON, the element goes to internal logic "0"

m1 is the number of words

m2 is the number of bits per word

qualifying-symbol	definition
I = 1	Initial logic "1" state. When power is switched ON, the element goes to internal logic "1"
NV	Non-volatile. The internal logic state is maintained regardless of power ON or OFF
Φ	Very complicated element. Depicted by a 'grey box' symbol. Within the 'grey box' outline, the Φ qualifying-symbol is accompanied by a further qualifying expression, e.g. ERR - for error detector

**Qualifying-symbols for inputs and outputs**

Referring to Table 2, qualifying-symbols for inputs and outputs, the logic negation indicator is used in pure logic diagrams to indicate that an external logic "0" ("1") produces an internal logic "1" ("0") at the input, or that an internal logic "1" ("0") produces an external logic "0" ("1") at the output.

The polarity indicator is used in detailed logic diagrams to indicate which logic level corresponds with the internal logic "1". The following may occur:

- an input or output **with** polarity indicator indicates that the logic level "L" (LOW) corresponds to an internal logic "1".
- an input or output **without** polarity indicator indicates that the logic level "H" (HIGH) corresponds to an internal logic "1".

In an array of elements, if the same general qualifying-symbol and the same qualifying-symbols associated with inputs and outputs should appear inside each element of the array, then they are usually shown only in the first element. Similarly, for large identical elements with subdivisions, the subdivisions may be shown only in the first element. This is done to simplify the array and ease recognition. As an example, omissions of both repeating qualifying-symbols and subdividing lines can be seen in the HC/HCT242 symbol.

**Table 2** Qualifying-symbols - Inputs and Outputs

qualifying-symbol	definition of input or output
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0")
	Logic negation at an output. An internal logic "1" ("0") produces an external logic "0" ("1")
	Polarity indicator at an input. A logic "L" (LOW) level ("H" (HIGH) level) at an input produces an internal logic "1" at that input
	Polarity indicator at an output. An internal logic "1" ("0") at an output produces a logic "L" (LOW) level ("H" (HIGH) level) at that output
	Polarity indicator at an input where the signal flow is from right to left
	Polarity indicator at an output where the signal flow is from right to left
(a)	Indicator for direction of signal flow: (a) from right to left;
(b)	(b) from bottom to top. With no indication of direction, flow is left to right or top to bottom
	Bidirectional information flow (alternate)
	Non-logic connection
	Input for analogue signals
	Input for digital signals (used only to avoid confusion)

### Symbols inside the outline

Table 3 shows some of the symbols used within the symbol- outlines. Other symbols used in this handbook but not shown here are self-explanatory. Generally these are associated with arithmetic operations but all are in accordance with the IEC system. When non-standard information is shown inside a symbol-outline, it is enclosed in square brackets.

It can be seen in Table 3 that open-collector, open-emitter and three-state outputs have distinctive symbols. Note that an enable input (EN) affects all of the circuit outputs and has no effect on the inputs. When an enable input affects only certain outputs and/or one or more inputs, a form of dependency notation will indicate this (see 'Dependency Notation, EN-dependency').






Another important point is that a D-input is always the data input of a storage element. An internal logic "1" at the D-input sets the storage element to its "1" state, and an internal logic "0" at the D-input resets the storage element to its "0" state.

Grouping of inputs or outputs is indicated by the bit-grouping symbol. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. The weights of input and output lines are represented by powers-of-two only when the bit-grouping symbol is used, otherwise decimal equivalents are used. Inputs grouped together by this symbol produce an internal number that is the sum of the individual input weights at logic "1". This number can be a number on which a mathematical function is performed, an identifying number used in dependency notation or a value that becomes the content (CT) of the element (see Fig. 29). A frequent use of the bit-grouping symbol is in memory addressing, see also 'Use of Bit-grouping to Produce Affecting Inputs'. For outputs, usage of the bit-grouping symbol is similar to that of inputs; the number produced by the sum of the output weights is the internal number, or the content (CT) produced by the circuit.

The symbols shown in Table 3 may be used to indicate the internal connections between logic elements abutted together. Each logic connection may be shown by qualifying-symbols at one or both sides of the common line, however, if confusion could arise about the number of connections, one of the internal connection symbols may be used.

The internal (virtual) input is an input originating somewhere within the circuit and not connected directly to a terminal, and similarly the internal (virtual) output is not connected directly to a terminal.

**Table 3** Symbols inside the outline










symbol inside outline	explanation
/	Solidus. Separator used in input and output labels. May be interpreted as an OR function
,	Comma. Separator with no logic significance
	Delayed output symbol for pulse and data-lock-out elements. The output change is delayed until the input that initiated the change (e.g. a "C" input) returns to its initial external state or level
	Bi-threshold inputs. Inputs with hysteresis
	Open output with low-impedance "L" (LOW) level
	Passive pull-up output. Similar to open output with low-impedance "L" level but with a built-in passive pull-up
	Open output with low-impedance "H" (HIGH) level











QUALIFYING-SYMBOLS (continued)

Table 3 Symbols inside the outline (continued)

symbol inside outline	explanation
	Passive pull-down output. Similar to open output with low-impedance "H" level but with a built-in passive pull-up
	Three-state output
	Enable input. When at internal logic "1", all outputs are enabled. When at internal logic "0": open outputs are OFF; three-state outputs retain their normal, defined internal logic state but give an external high-impedance state; all other outputs are at internal logic "0"
R, S, C, T	Control inputs of bistable elements
J, K, R, S, D	Information inputs of bistable elements
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left or up when the arrow points to the left. The number may be omitted when "m" = 1
	Counting input. Count-up and count-down are indicated by + and - respectively. The number "m" is the count per command and may be omitted when "m" = 1
	Bit-grouping symbol. "m" is the highest power of 2 in the group
	Content input. The internal logic "1" sets the element to the value "m"
	Content output. "*" is the value of the element that sets the output to an internal logic "1" (e.g. CT = 0, CT ≥ 5, CT ≠ 4..9)
	Line-grouping symbol. The inputs or outputs enclosed by this symbol form a single logic input or output
	Fixed-mode input. This input is permanently at internal logic "1"

symbol inside outline	explanation
	Fixed-state output. This output is permanently at internal logic "1"
a...g	Seven segments of a display element
	Extension input. Input intended for connection to an extender output
	Extender output. Output to an extension input
	Operand input. This input represents one bit of an operand on which one or more mathematical functions are performed; "m" is the decimal equivalent of the weight of the bit. If the weights of all Pm inputs of the element are powers of 2 then "m" is the exponent of the power of 2
	Operand input. See Pm
	'Smaller-than' input to a magnitude comparator
	'Greater-than' input to a magnitude comparator
	'Equal' input to a magnitude comparator
	'Borrow-in' input to an arithmetic element
	'Borrow-generate' input to an arithmetic element
	'Borrow-generate' output from an arithmetic element

symbol inside outline	explanation
	'Borrow-out' output from an arithmetic element
	'Borrow-propagate' input to an arithmetic element
	'Borrow-propagate' output from an arithmetic element
	'Carry-in' input to an arithmetic element
	'Carry-generate' input to an arithmetic element
	'Carry-generate' output from an arithmetic element
	'Carry-generate' output from an arithmetic element
	'Carry-propagate' input to an arithmetic element
	'Carry-propagate' output from an arithmetic element
$\Pi$	Result of a multiplication
$\Sigma$	Result of an addition
P-Q	Result of a subtraction
[ · · ]	Added information

symbol inside outline	explanation
$\varphi_m$	Clock phase. "m" is the clock phase number
	Connection for external capacitor(s)
	Connection for external resistor(s)
	Dynamic input. A transition from logic "L" level to "H" level produces a transitory internal logic "1"
	Dynamic input. A transition from logic "H" level to "L" level produces a transitory internal logic "1"
	Internal connection. A logic "1" at the left-hand side produces a logic "1" at the right-hand side
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left-hand side produces a transitory logic "1" at the right-hand side
	Negated dynamic internal connection. A transition from internal logic "1" to internal logic "0" at the left-hand side produces a transitory internal logic "1" at the right-hand side
	Internal (virtual) input. This input is always at internal logic "1" state unless this is overridden or modified
	Internal (virtual) output. The effect on the internal input connected to this output must be indicated by dependency notation

**DEPENDENCY NOTATION**

**General conventions of dependency notation**

Dependency notation is the powerful tool that makes IEC symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and other inputs, between outputs and other outputs, and between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying-symbols for an element's function.

In dependency notation, the terms "affecting" and "affected" are used. In cases where it is not evident which inputs must be selected as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the most convenient input has been chosen.

The types of dependency described in this section are "G" (AND); "V" (OR); "N" (negate, or EXCLUSIVE-OR); "Z" (interconnection); "C" (control); "S" and "R" (set and reset); "EN" (enable); "M" (mode); and "A" (address).

The general rules applied to dependency notation are:

- the input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved (e.g. G for AND) followed by an appropriately-chosen identifying number; and
- each input or output affected by that affecting input (or output) is labelled with that same number.

If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together (see Fig. 4).

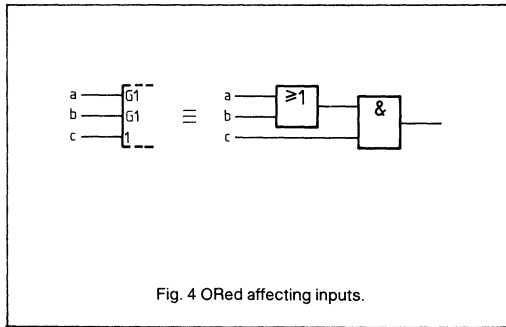


Fig. 4 ORed affecting inputs.

If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships (see Fig. 5).

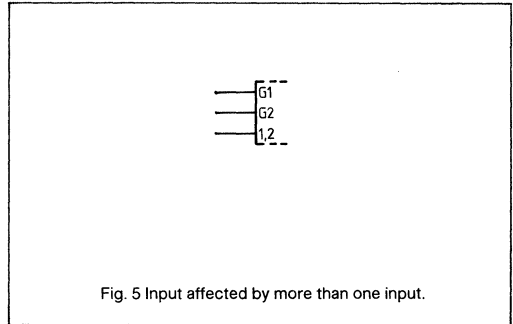


Fig. 5 Input affected by more than one input.

If the labels denoting the function of affected inputs or outputs are numbers, (e.g., outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters (see Fig. 6).

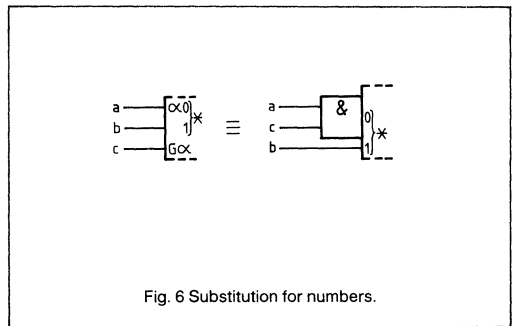


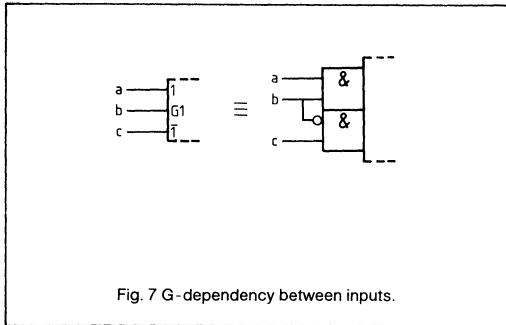
Fig. 6 Substitution for numbers.

If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (see Fig. 7).

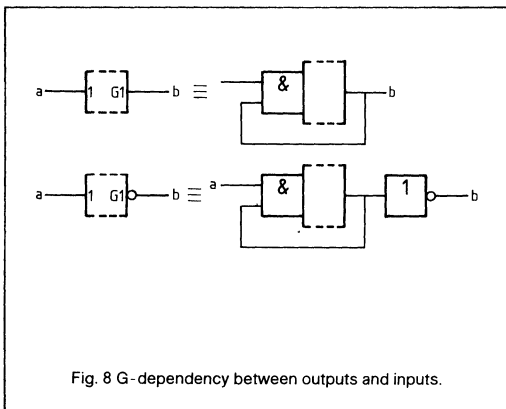
If the affected input or output has a label to denote its function (e.g. "D"), this label will have the identifying number of the affecting input as a prefix (see Fig. 13).

**G-dependency**

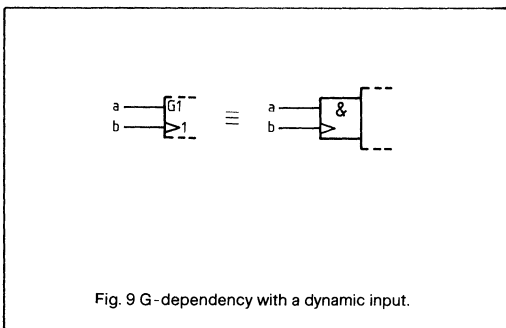
The traditional method of showing an AND relationship was to use an explicit drawing of an AND gate with the signals connected to the inputs of the gate. With IEC symbology (see Fig. 7), input "b" and input "a" are ANDed together and the complement of "b" is ANDed with "c". The letter G has been chosen to indicate AND relationships and is placed at input "b", within the outline. A number considered appropriate by the designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input "c".



In Fig. 8, output "b" affects input "a" with an AND relationship. The lower example shows it is the internal logic state of "b", unaffected by the negation sign, that is ANDed.



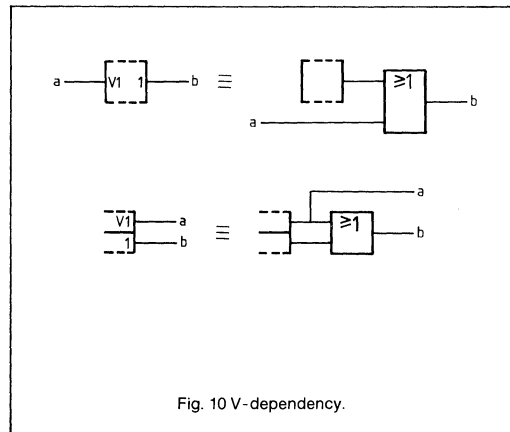
In Fig. 9, input "a" is ANDed with the dynamic input "b".



To summarize G-dependency using input G and allotted number m: when a Gm-input (Gm-output) is at internal logic "1", all inputs and outputs affected by Gm will be at their normally defined internal logic states. When the Gm-input (Gm-output) is at internal logic "0", all inputs and outputs affected will be at internal logic "0".

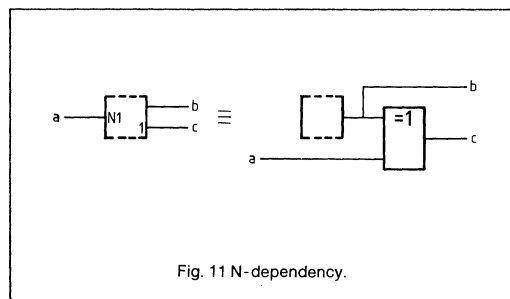
**V-dependency**

When a Vm-input (Vm-output) is at internal logic "1", all inputs and outputs affected by Vm will be at internal logic "1". When the Vm-input (Vm-output) is at internal logic "0", all inputs and outputs affected by Vm will be at their normally defined internal logic states (see Fig. 10).



**N-dependency**

Each input or output affected by an Nm-input (or output) is EXCLUSIVE-ORed with the Nm-input (or output) (see Fig. 11).



When an Nm-input (Nm-output) is at internal logic "1", the internal logic state of each input and each output affected by Nm will be complemented. When an Nm-input (Nm-output) is at internal logic "0", all inputs and outputs affected by Nm will be at their normally defined internal logic states.



**DEPENDENCY NOTATION (continued)**

**Z-dependency**

Interconnection dependency is used to indicate internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

All inputs or outputs affected by a Zm-input (or output) will take on the same internal logic state as the Zm-input (or output), unless modified by additional dependency notation (see Fig. 12).

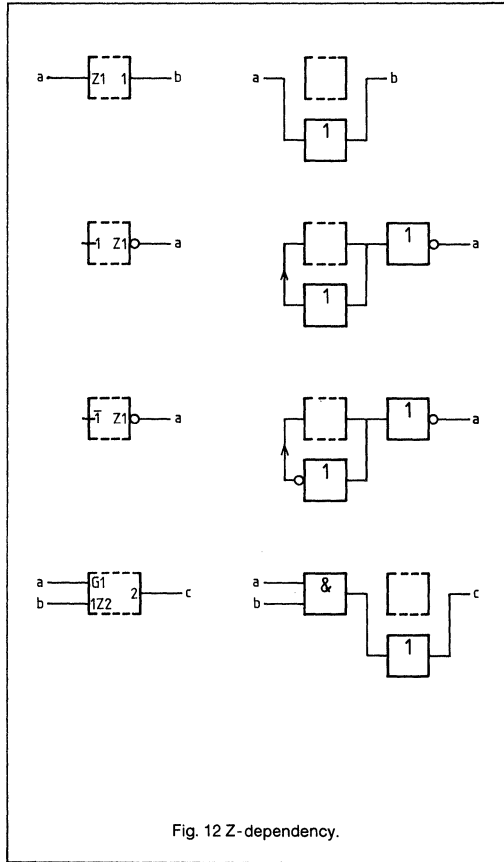


Fig. 12 Z-dependency.

**C-dependency**

Control inputs enable or disable the data (D, J, K, R or S) inputs of storage elements (see Fig. 13).

When a Cm-input is at internal logic "1", the inputs affected by Cm have their normal effect on the function of the element, i.e. these inputs are enabled. When a Cm-input is at internal logic "0", the inputs affected by Cm are disabled and have no effect on the function of the element.

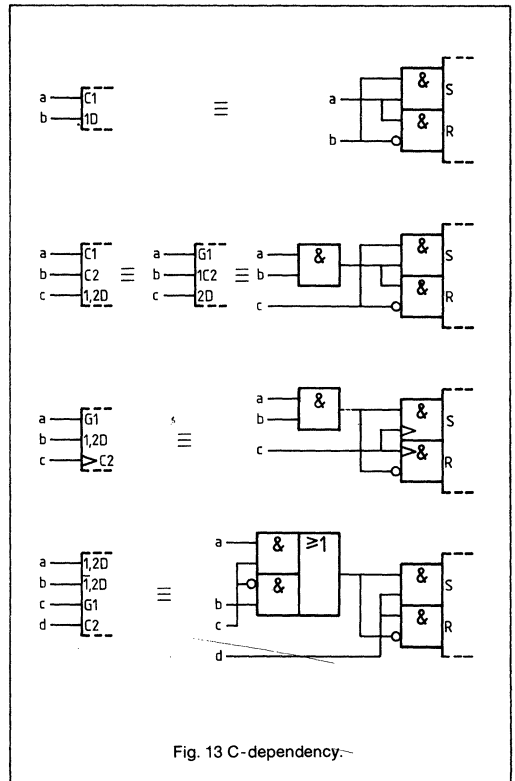


Fig. 13 C-dependency.

**EN-dependency**

An ENm-input has the same effect on outputs as an EN-input (see Table 1) but it affects both inputs and outputs that have the identifying number "m", whereas an EN-input affects all outputs and no inputs.

The effect of an ENm-input on an affected input is identical to that of a Cm-input (see Fig. 14).

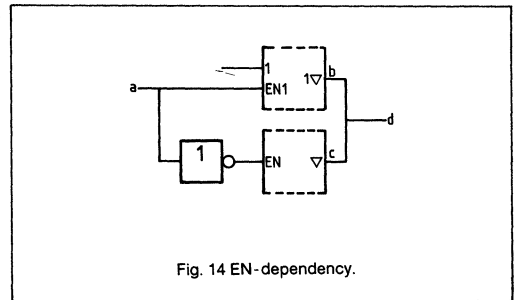


Fig. 14 EN-dependency.

When an ENm-input is at internal logic "1", inputs and outputs affected by ENm are enabled.

When an ENm-input is at internal logic "0": inputs and outputs affected by ENm are disabled; open outputs are turned OFF; passive pull-up outputs will be high-impedance "L" level; passive pull-down outputs will be high-impedance "H" level; 3-state outputs will have their normally defined internal logic states but externally exhibit high-impedance; and all other outputs (e.g., totem-pole outputs) will be at internal logic "0".

### S and R-dependencies

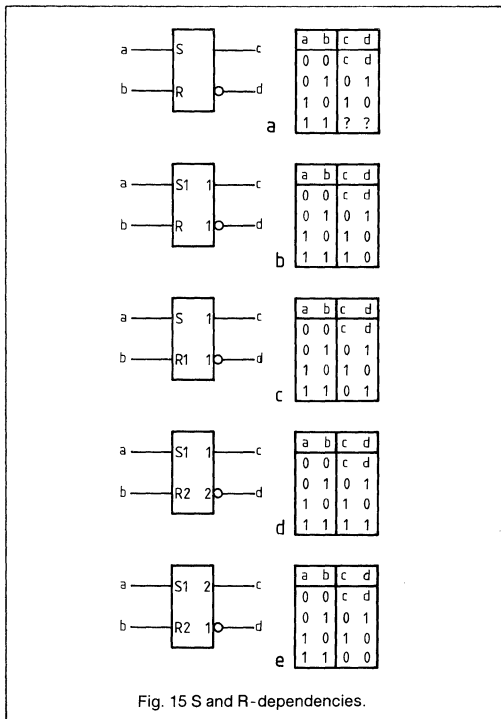
Set and reset dependencies are used if the effect of the combination  $R = S = 1$  on a bistable element must be specified. Figure 15a does not use S or R-dependency (? = not specified).

When an Sm-input is at internal logic "1", outputs affected by the Sm-input will react, regardless of the state of an R-input, as they would normally react to the combination  $S = 1, R = 0$  (see Fig. 15b).

When an Rm-input is at internal logic "1", outputs affected by the Rm-input will react, regardless of the state of an S-input, as they would normally react to the combination  $S = 0, R = 1$  (see Fig. 15c).

The non-complementary output patterns in Figs 15d and 15e are only pseudo-stable. The simultaneous return of the inputs to  $S = R = 0$  produces an unforeseeable stable and complementary output pattern.

When an Sm or Rm input is an internal logic "0", it has no effect.



### M-dependency

Mode dependency indicates that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

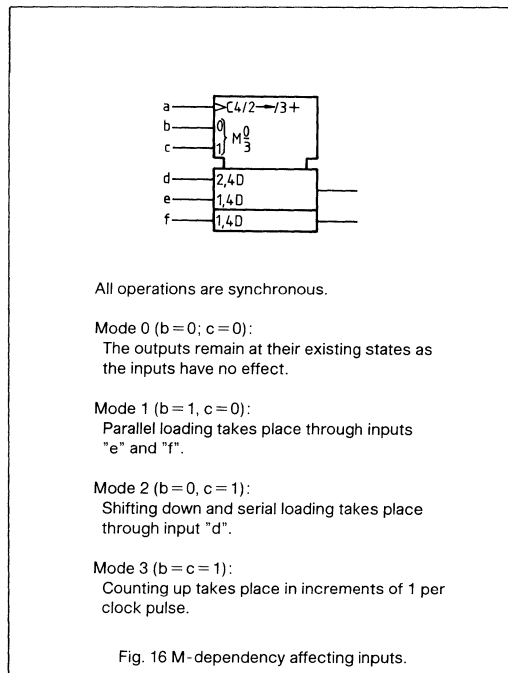
If an input or output has the same affect in different modes of operation, the identifying numbers of the relevant affecting Mm-inputs will appear in parentheses, separated by solidi, in the label of that affecting input or output (see Fig. 20).

#### M-dependency affecting inputs

When an Mm-input (Mm-output) is at internal logic "1", the inputs affected by this Mm-input (Mm-output) will be enabled.

When an Mm-input (Mm-output) is at internal logic "0", the inputs affected by this Mm-input (Mm-output) will be disabled. When an affecting input has several sets of labels separated by solidi (e.g.,  $C4/2 \rightarrow /3+$ ), any set in which the identifying number of the Mm-input (Mm-output) appears has no effect and is to be ignored. This represents the disabling of some of the functions of a multi-function input.

The circuit in Fig. 16 has two inputs, "b" and "c", these control the one of four modes (0, 1, 2 or 3) that will exist at any time. Inputs "d", "e", and "f" are D-inputs subject to dynamic control (clocking) by the "a" input. The numbers 1 and 2 identify the operating modes, and so inputs "e" and "f" are only enabled in mode 1 (for parallel loading) and input "d" is only enabled in mode 2 (for serial loading). Input "a" has three functions: it is the clock for entering data; in mode 2 it causes right-shifting of data (shifts away from the control block); and in mode 3, it causes the contents of the register to be incremented by one.

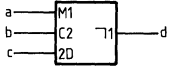


**DEPENDENCY NOTATION (continued)**

**M-dependency affecting outputs**

When an Mm-input (Mm-output) is at internal logic "1", the affected outputs will be enabled.

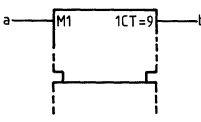
When an Mm-input (Mm-output) is at internal logic "0", the affected outputs will be disabled. When an input or output has several different sets of labels separated by solidi (e.g., 2,4/3,5), any set in which the identifying number of the Mm-input (Mm-output) appears is to be ignored.



Mode 1 (a = 1):  
The delayed output symbol is effective only in mode 1 and therefore the device functions as a pulse-triggered D-element.

Mode 2 (a = 0):  
The delayed output symbol has no effect and therefore the device functions as a transparent latch.

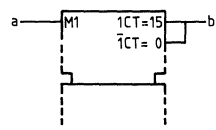
Fig. 17 Flip-flop type determined by mode.



Mode 1 (a = 1):  
Output "b" will be an internal logic "1" only when the register content equals 9.

Mode 2 (a = 0):  
Since output "b" is located in the common-control block with no defined function outside of mode 1, this output will be an internal logic "0" when input "a" is an internal logic "0", regardless of the register content.

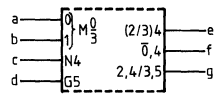
Fig. 18 Disabling an output of the common-control block.



Mode 1 (a = 1):  
Output "b" will be an internal logic "1" only when the register content equals 15.

Mode 2 (a = 0):  
Input "a" is an internal logic "0", output "b" will be an internal logic "1" only when the register content equals 0.

Fig. 19 Determining an output's function.



Inputs "a" and "b" are binary weighted to generate the numbers 0, 1, 2 or 3 to determine which of the four modes exist.

Mode 0 (a = 0, b = 0):  
Since no output label contains a "0", the outputs have their normally defined internal logic states. Output "f" carries a "0" in its label and this means that output "f" is effected by all modes **except** mode 0.

Mode 1 (a = 1, b = 0):  
Only output "f" is affected by mode 1 and is also affected by input "c" (N4).

Mode 2 (a = 0, b = 1):  
The outputs "e" and "g" are affected in this mode. They are also affected by input "c" (N4) which means that the internal logic state of the output will be negated at N4 = 1. Output "f" is affected since M0 stands at its internal "0" state. In addition, output "f" is affected by input "c" (N4).

Mode 3 (a = 1, b = 1):  
All outputs shown are affected in this mode, with outputs "e" and "f" also affected by input "c" (N4) and input "d" also affecting output "g".

Fig. 20 Dependent relationships affected by mode.

**A-dependency**

Using address-dependency gives a clear representation of elements, particularly memories, that use address control inputs to select sections of a multi-dimensional array. Such a section of a memory array is usually called a word. Address-dependency allows a symbolic representation of an entire array. An array input at a particular element of a general section is common to the corresponding elements of all selected sections of the array. An array output at a particular element of a general section is the result of ORing the outputs of the corresponding elements of selected sections. If the label of an array output at a particular element of a general section indicates that this output is an open-circuit or a 3-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any input have their normal effect on all sections of the array, whereas inputs affected by an address input only have their normal effect on the section selected by that address input.

An affecting address input has the label "A" followed by an identifying number which corresponds to the address of the particular section of the array selected by this input. Within the general section represented by the symbol, inputs and outputs affected by an "Am" input have the label "A", which stands for the identifying numbers, i.e. the addresses of the particular sections.

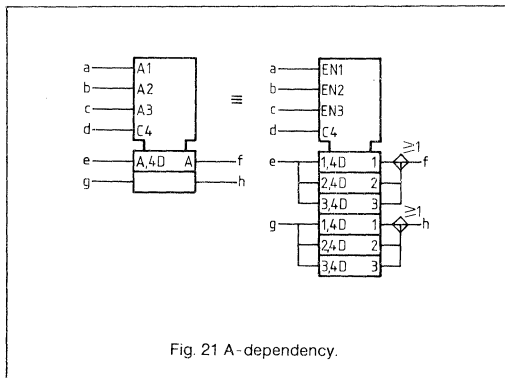


Fig. 21 A-dependency.

Figure 21 shows a 3-word x 2-bit memory having a separate address line for each word; EN-dependency is used to explain the operation. To select word 1, input "a" is forced to logic "1", entering mode 1. Data can now be clocked into the inputs marked "1,4D". Data cannot be clocked into the inputs marked "2,4D" and "3,4D" unless words 2 and 3 are selected. The outputs will be the OR function of the selected outputs, i.e. only those enabled by the active EN functions.

The identifying numbers of affecting inputs correspond to the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, ..), because in the general section represented by the symbol they are replaced by the letter "A".

If there are several sets of affecting "Am" inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter "A" is modified to 1A, 2A, ... These sets of "A" inputs may have the same identifying numbers.

Another illustration of the concept is shown in Fig. 22.

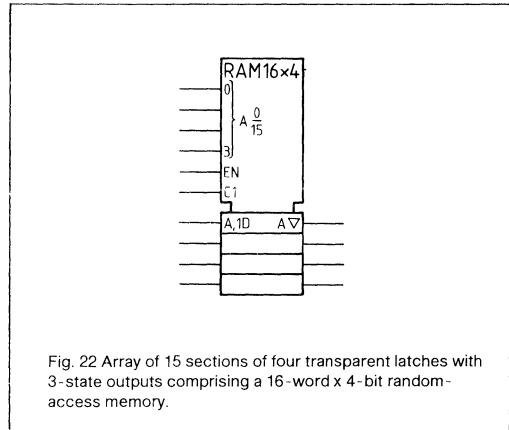


Fig. 22 Array of 15 sections of four transparent latches with 3-state outputs comprising a 16-word x 4-bit random-access memory.

**Table 4** Summary of dependency notation

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
address	A	permits action (address selected)	prevents action (address not selected)
control	C	permits action	prevents action
enable	EN	permits action	prevents action of inputs; open outputs OFF; ▽ outputs at external high impedance, no change in internal logic state; ⊕ outputs high impedance "H" level; ⊖ outputs high impedance "L" level; other outputs at internal "0" state
AND	G	permits action	imposes "0" state
mode	M	permits action (mode selected)	prevents action (mode not selected)
negate (EXCLUSIVE OR)	N	complements state	no effect
reset	R	affected output reacts as it would to S = "0", R = "1"	no effect
set	S	affected output reacts as it would to S = "1", R = "0"	no effect

**DEPENDENCY NOTATION (continued)**

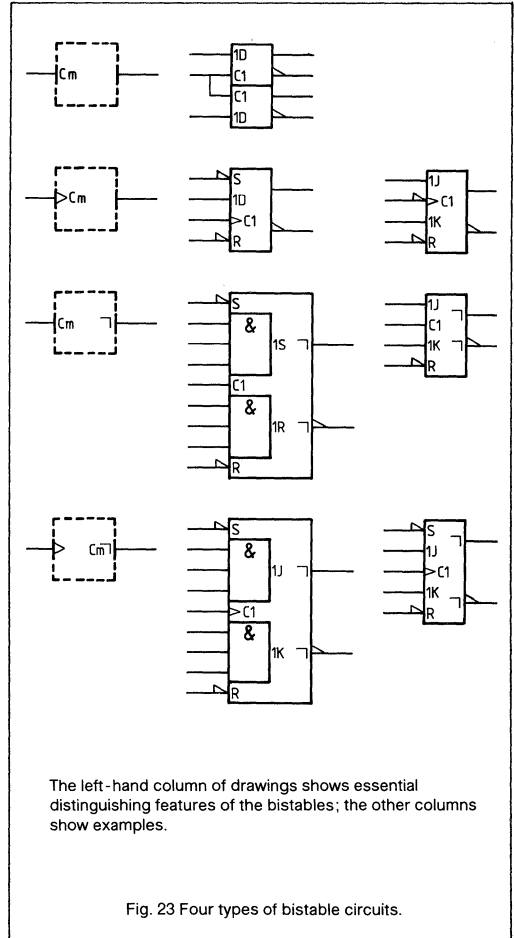
**A-dependency (continued)**

type of dependency symbol*	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
OR	V	imposes "1" state	permits action
inter-connection	Z	imposes "1" state	permits action

\* These letter symbols appear at the **affecting** input (or output) and are followed by a number. Each input (or output) **affected** by that input is labelled with that same number. The descriptions do not apply when the labels "EN", "R" and "S" appear at inputs without numbers following; the action of these inputs is described in 'Symbols inside the outline'.

**BISTABLE ELEMENTS**

The dynamic input symbol, the delayed output symbol and dependency notation allow the four main types of bistable elements to be shown and make synchronous and asynchronous inputs easily recognizable (see Fig. 23). A fifth type of bistable, the direct acting "SR" element, is mentioned in 'S and R-dependencies'.

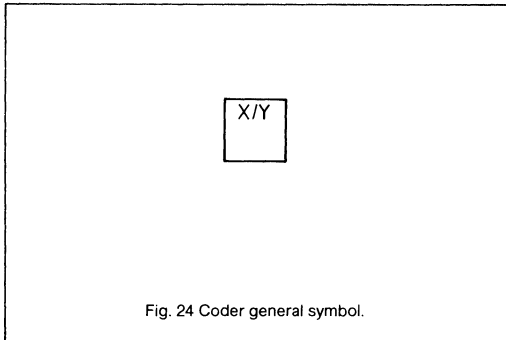


Transparent latches have a level-operated control input. The D-input is active as long as the C-input is at internal logic "1". The outputs respond immediately. Edge-triggered elements accept data from "D", "J", "K", "R" or "S" inputs on the active transition of "C". Pulse-triggered elements require the data to be set up before the start of the control pulse; the "C" input is considered static since the data must be maintained as long as "C" is at logic "1". The output is delayed until "C" returns to logic "0". The data-lock-out element is similar to the pulse-triggered version except that the "C" input is considered to be dynamic, in that shortly after "C" goes through its active transition, the data inputs are disabled and data does not have to be maintained. However the output is still delayed until the "C" input returns to its initial external level.

Note that synchronous inputs can be recognized easily because of labels (1D, 1J, 1K, 1S, 2R) unlike the asynchronous inputs "S", "R", which are not dependent on the "C" inputs.

## CODERS

The general symbol for a coder or code-converter is shown in Fig. 24. The labels "X" and "Y" may be replaced by appropriate indications of the code that is used to represent the information at the respective inputs and outputs.



Indication of code conversion is based on the following rule:

Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

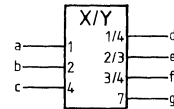
The relationship between the internal logic states of the inputs and the internal value is indicated by:

Labelling the inputs with numbers so that the internal value equals the sum of the weights associated with those inputs that are at internal logic "1"; or by replacing "X" by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationship between the internal value and the internal logic states of the outputs is indicated by:

Labelling each output with a list of numbers representing those internal values that force that output to an internal logic "1". The numbers are separated by solidi (see Fig. 25). This labelling may also be applied when "Y" is replaced by a letter denoting a type of dependency (see 'Use of a coder to produce affecting inputs'). If a continuous range of internal values produces the internal logic "1" at an output, this is indicated by the numbers that begin and end the range, separated by three dots, e.g. "4...9" equals "4/5/6/7/8/9"; or by replacing "Y" with an appropriate indication of the output code and labelling the outputs with characters that refer to this code (see Fig. 26).

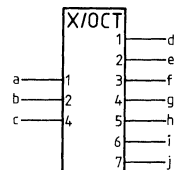
Alternatively the general symbol may be used together with an appropriate reference to a table detailing the relationship between the inputs and outputs. This is a recommended way to symbolize a ROM, or a PROM after it has been programmed.



TRUTH TABLE

inputs			outputs			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Fig. 25 An X/Y code converter.



TRUTH TABLE

inputs			outputs							
c	b	a	j	i	h	g	f	e	d	
0	0	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	1	0	
0	1	1	0	0	0	0	1	0	0	
1	0	0	0	0	0	1	0	0	0	
1	0	1	0	0	1	0	0	0	0	
1	1	0	0	1	0	0	0	0	0	
1	1	1	1	0	0	0	0	0	0	

Fig. 26 An X/octal code converter.

**USE OF A CODER TO PRODUCE AFFECTING INPUTS**

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case the symbols for a coder can be used as an embedded symbol (see Fig. 27).

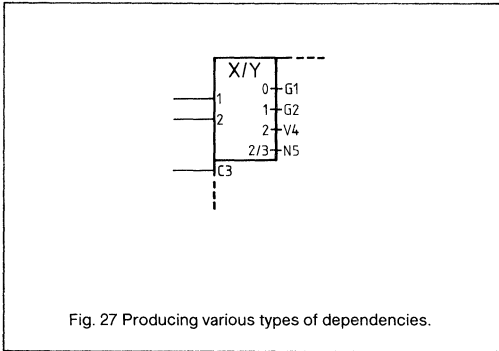


Fig. 27 Producing various types of dependencies.

If all affecting inputs produced by a coder are the same type and their identifying numbers correspond with the numbers shown at the coder outputs, "Y" (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. In this case, affecting input indications should be omitted (see Fig. 28).

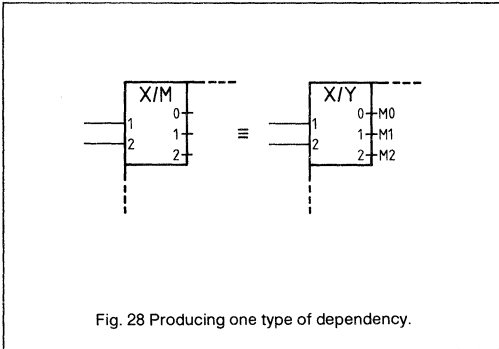


Fig. 28 Producing one type of dependency.

**USE OF BIT-GROUPING TO PRODUCE AFFECTING INPUTS**

If all affecting inputs produced by a coder are the same type and have consecutive identifying numbers (not necessarily corresponding to the numbers that would have been shown at the outputs of the coder) the bit-grouping symbol can be used (see Table 1). Effectively, "k" external lines generate  $2^k$  internal inputs. The bracket precedes the letter denoting the type of dependency which is followed by  $m^1/m_2$ . The "m1" is then replaced by the smallest identifying number and "m2" by the largest (see Fig. 29).

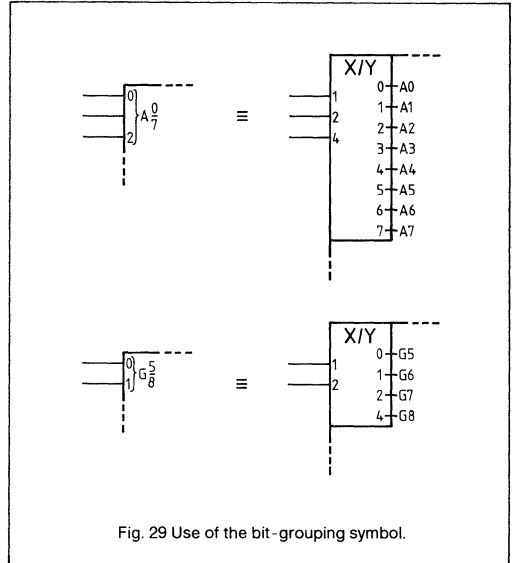


Fig. 29 Use of the bit-grouping symbol.

**SEQUENCE OF INPUT LABELS**

If an input having a single function is affected by other inputs, the qualifying-symbol (if there is one) for that function is preceded by the labels of the affecting inputs. The left-to-right order of these labels is the sequence in which the effects or modifications must be applied. The affected input has no effect on the element if the logic state of any of the affecting inputs (regardless of the logic states of other affecting inputs) would cause the affected input to have no effect.

If an input has several functions or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of representation is undesirable. In these cases, the input may be shown once with the different sets of labels separated by solidi (see Fig. 30). No meaning is attached to the order of these sets of labels. If one of the functions of an input is as an unlabelled input to an element, a solidus will precede the first set of labels.

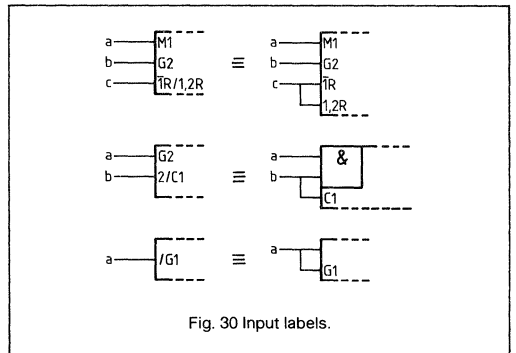


Fig. 30 Input labels.

If all inputs of a combinative element are disabled (have no effect on the function of the element), the internal logic states of the element outputs are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factorized using algebraic techniques (see Fig. 31).

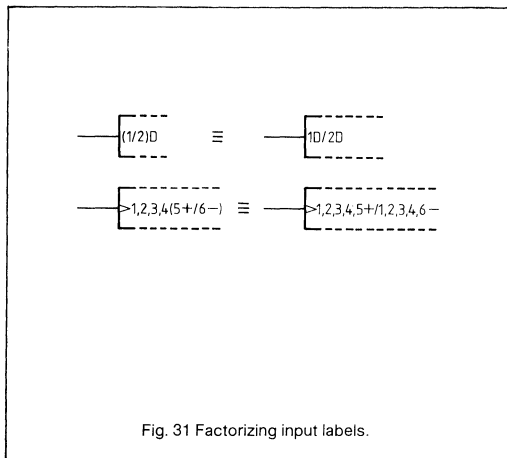


Fig. 31 Factorizing input labels.

When at latched inputs the algebraic factorizing technique is combined with the use of the bit-grouping symbol, the indication "mD" may be placed behind the bit-grouping symbol provided that the proper order of all the other labels is maintained (see Fig. 32).

In "mD", the "m" stands for the identifying numbers of the affecting inputs.

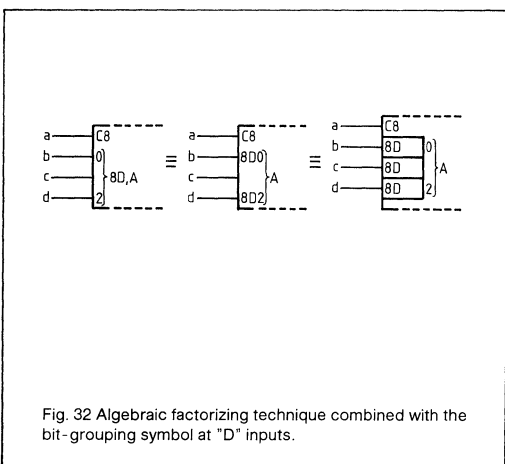


Fig. 32 Algebraic factorizing technique combined with the bit-grouping symbol at "D" inputs.

### SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether or not they are identifying numbers of affecting inputs or outputs, these labels are shown in the following order (see Fig. 33):

the delayed output symbol comes first (if to be shown) preceded if necessary by the indications of the inputs to which it must be applied;

followed by the labels indicating modifications to the internal logic state of the output, such that the left-to-right order of these labels is the sequence in which their effects must be applied;

followed by the label indicating the effect of the output on the inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside boundary of the element adjacent to the output line.

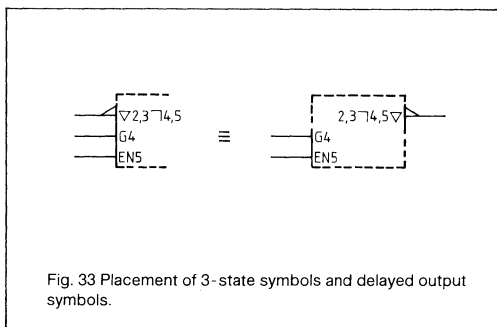


Fig. 33 Placement of 3-state symbols and delayed output symbols.

If an output needs several sets of labels to represent alternative functions, depending on the mode of action, these sets may be shown on different output lines connected together outside the outline. However, there are cases in which this representation is undesirable. In these cases the output may be shown once with the different sets of labels separated by solidi (see Fig. 34).

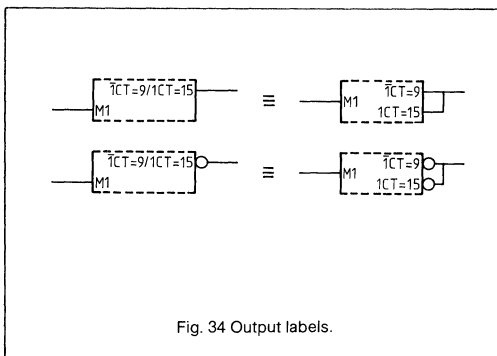


Fig. 34 Output labels.

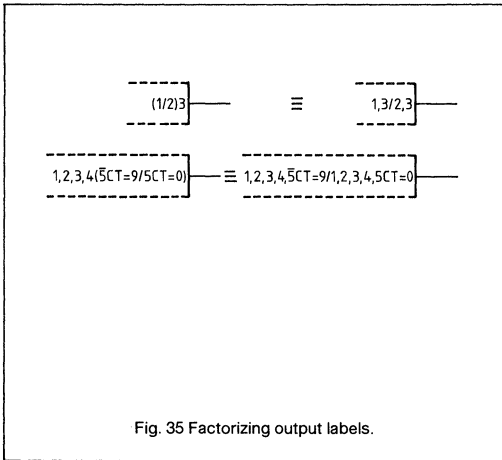


**SEQUENCE OF OUTPUT LABELS** (continued)

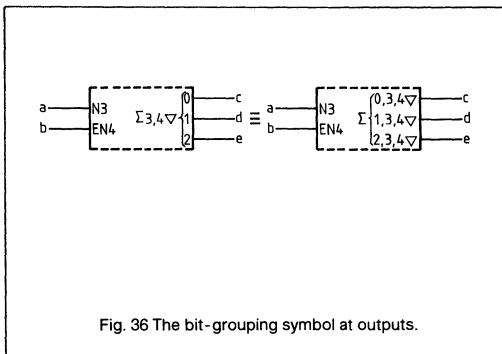
Adjacent identifying numbers of affecting inputs that are not separated by a non-numeric character are separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting "Mm" input at internal logic "0", this set of labels has no effect on the output.

Labels may be factorized using algebraic techniques (see Fig. 35).



If the bit-grouping symbol for outputs is used and the sets of labels of all outputs grouped together differ only in the indications of the weights, the sets of labels may be shown only once between the symbol replacing "\*" and the grouping symbol (see Table 3) provided that, except for the grouping symbol and the weights, the proper order of the labels is maintained (see Fig. 36). These sets of labels, therefore, include the symbols for open-circuit, passive pull-down, passive pull-up and 3-state outputs but exclude the indications of weights.



**RULES FOR SIMPLIFICATION OF SYMBOLS**

**INTRODUCTION**

The IEC symbology can depict a complete integrated circuit but, in many applications, not all available functions are used. For these applications the complete symbol need not be shown and a considerable simplification can be made. To maintain clarity, rules for the simplification of symbols are described in this section.

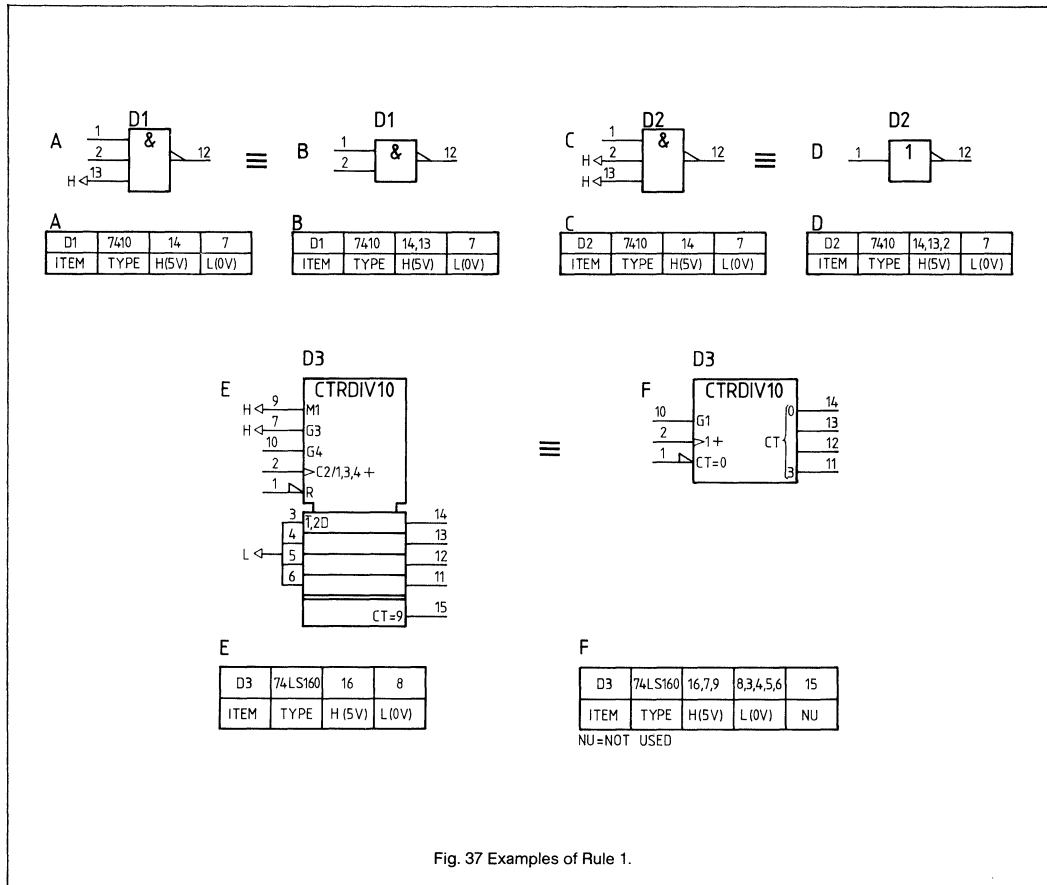
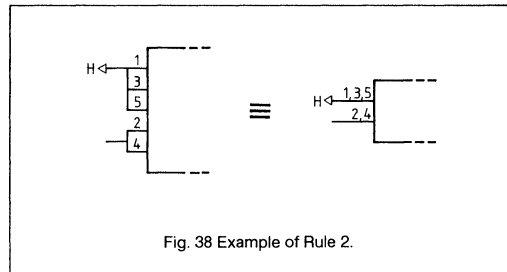
**RULE 1**

For an integrated circuit where not all functions are used, the diagram may contain:

- a. the complete symbol with indications of which pins are connected to a certain voltage level;
- b. a simplified symbol where only the functions used are depicted; the unused pins are detailed in a table including information on whether these pins may remain open (floating) or are to be connected to a certain voltage level.

**RULE 2**

When two or more pins are shown with a single line, then a comma between the pin numbers means that these pins are connected together; when the pin numbers are separated by a solidus, this means they are separate functions.



# RULES FOR SYMBOL SIMPLIFICATION

## RULE 3

The rules for sets of labels at inputs and outputs using solid lines to separate the various parts of a label may be applied when drawing two or more pins with a single line, so the labels must also be joined.

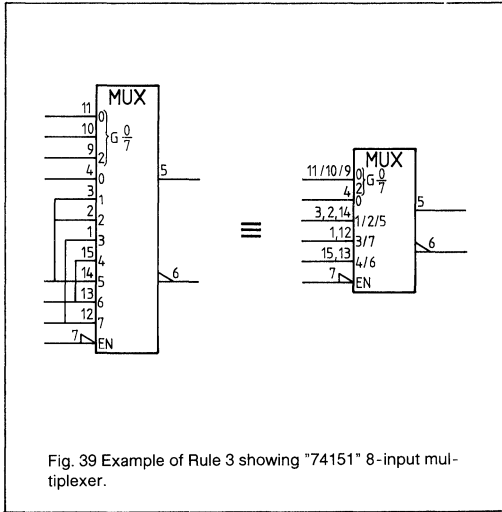


Fig. 39 Example of Rule 3 showing "74151" 8-input multiplexer.

## RULE 4

An output can be connected to an input of equal polarity as shown in Fig. 40C. If the polarity is different this method does not give sufficient information and the methods of Fig.40A or B are then adopted.

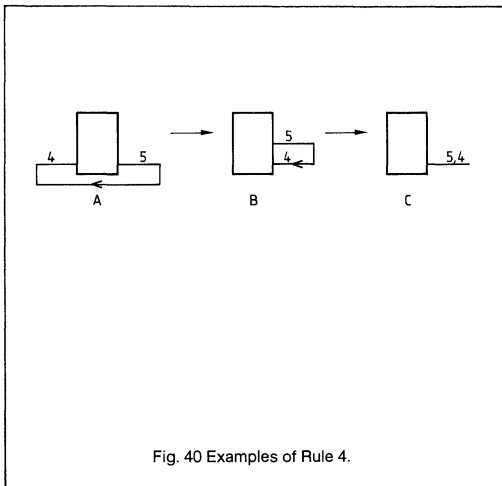


Fig. 40 Examples of Rule 4.

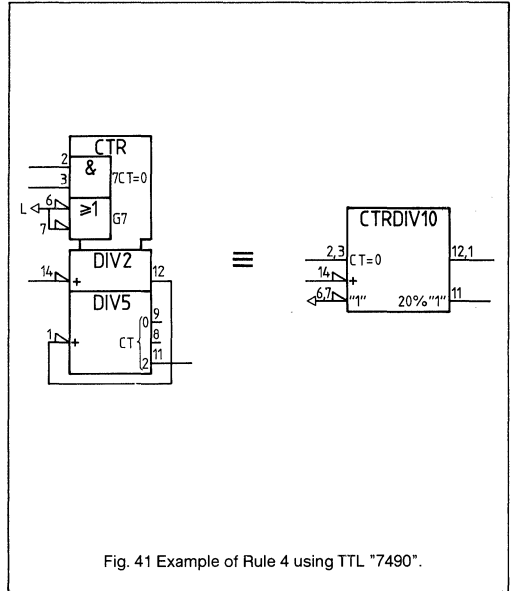


Fig. 41 Example of Rule 4 using TTL "7490".

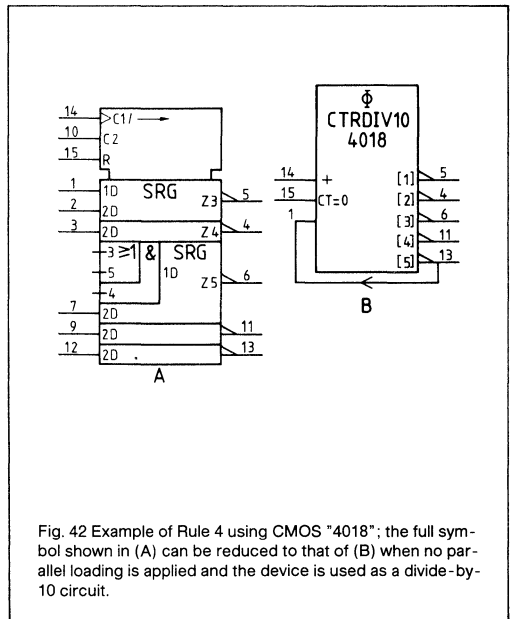


Fig. 42 Example of Rule 4 using CMOS "4018"; the full symbol shown in (A) can be reduced to that of (B) when no parallel loading is applied and the device is used as a divide-by-10 circuit.

**RULE 5**

Combining elements together to form one element is allowed only if all pin numbers can be shown.

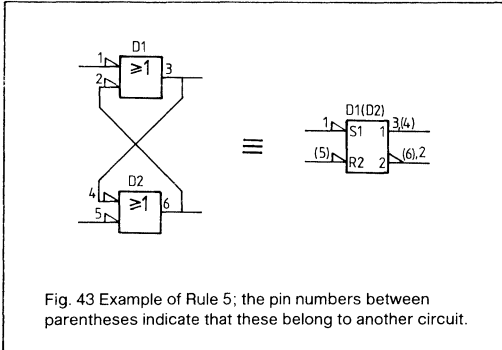


Fig. 43 Example of Rule 5; the pin numbers between parentheses indicate that these belong to another circuit.

**RULE 6**

A circuit consisting of a combination of two or more elements that appear repeatedly on a diagram, may be replaced by a single symbol. This symbol is used on the diagram, while the complete circuit is shown in an auxiliary diagram elsewhere on the drawing.

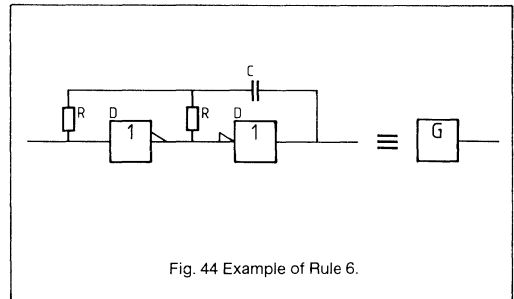


Fig. 44 Example of Rule 6.

**RULE 7**

A multiple symbol may also be applied for logic symbols.

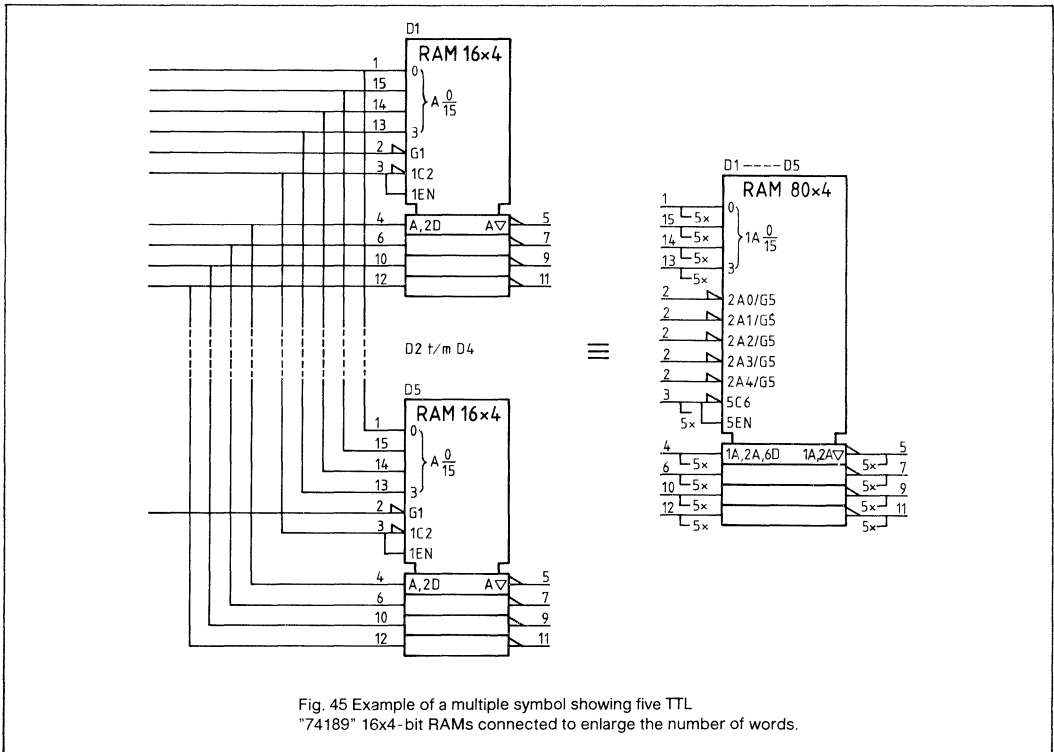


Fig. 45 Example of a multiple symbol showing five TTL "74189" 16x4-bit RAMs connected to enlarge the number of words.

RULE 7 (continued)

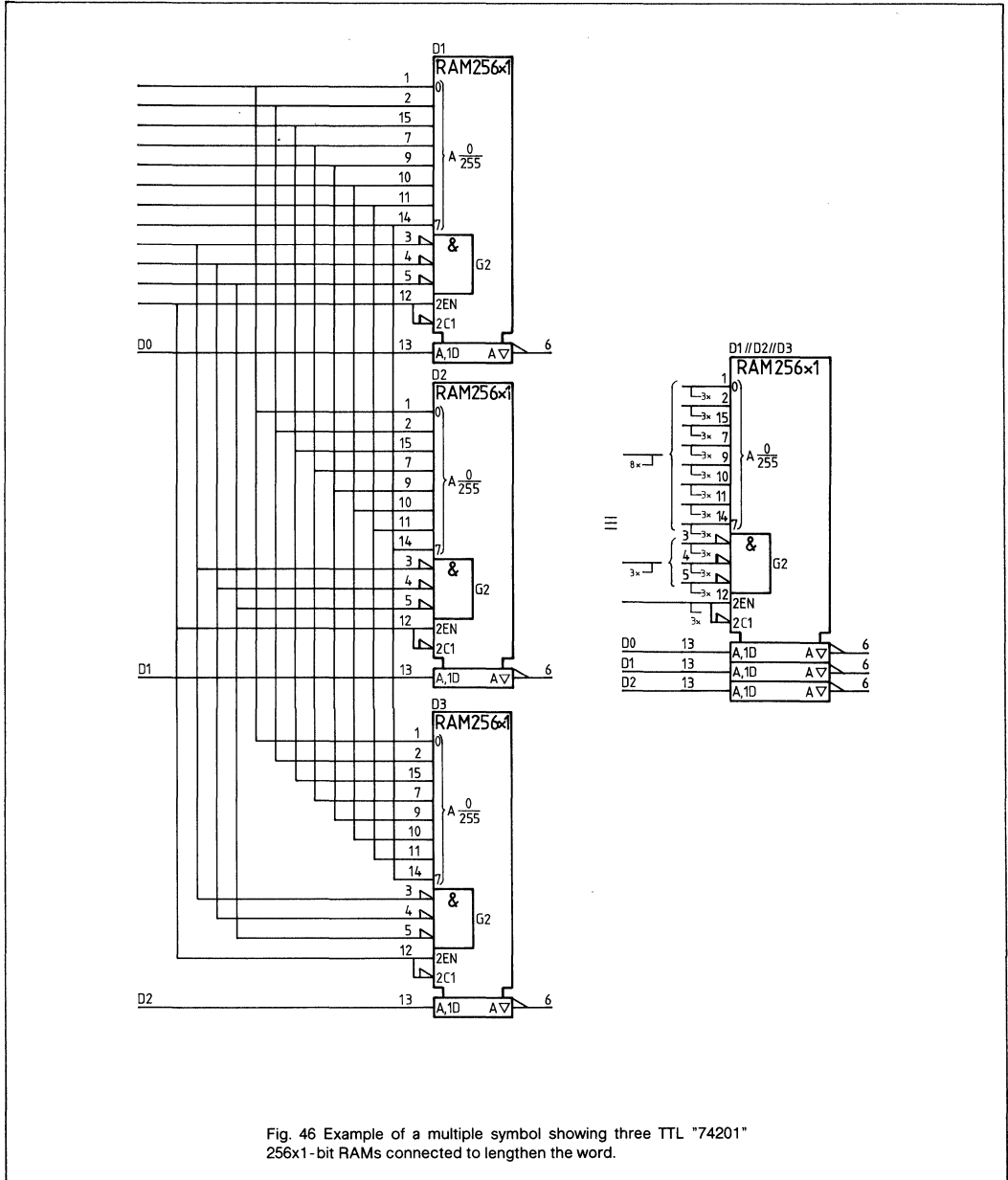


Fig. 46 Example of a multiple symbol showing three TTL "74201" 256x1-bit RAMs connected to lengthen the word.

**RULE 8**

Every (P)ROM may be regarded as an X/Y-code-converter.

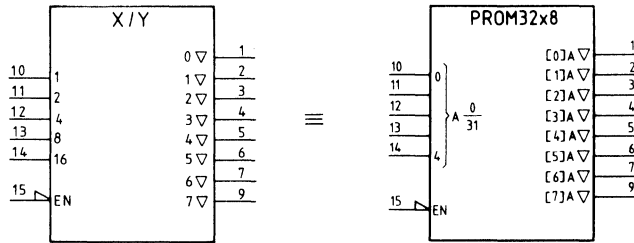
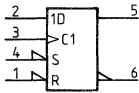


Fig. 47 Example of Rule 8 using Schottky TTL "74S288" PROM.

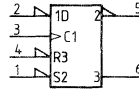
EXAMPLES OF APPLICATION-DEPENDENCY OF SYMBOLS

A symbol depicts the function of an element. In the case of multi-function elements, the functions are depicted separately.

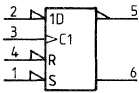
To demonstrate application-dependency of symbols, Fig. 48 shows the basic symbol and eight applications of the "7474" D-element with "S" and "R" inputs.



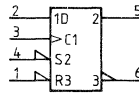
(A) basic symbol



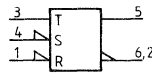
(B) as for (A) but with "R" and "S" dependency



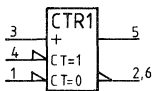
(C) D-input ("L")  
(note change of "R" and "S")



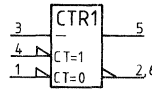
(D) as for (B) but with "S" and "R" dependency



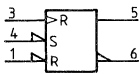
(E) divide-by-2 ("T") element



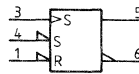
(F) divide-by-2 as a limit case of CTR



(G) as for (F) with down-counter



(H) function at pin 2 = "L", or as indicated in a table



(I) function at pin 2 = "H", or as indicated in a table

Fig. 48 Example of application-dependent symbols for edge-triggered D-element with "R" and "S" inputs.

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**Note:** The information in this user guide is intended as a design-aid and does not constitute a guarantee.



INTRODUCTION

The 74HC/HCT/HCU family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - these circuits have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). An extensive product range (most TTL functions and some devices from the successful HE4000B series: analog multiplexers, long time-constant multivibrators, phase-locked loops) and the aforementioned performance open new avenues in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1. The propagation delay of metal-gate CMOS ruled out CMOS for many applications until the arrival of our HE4000B series. Now, our 3µm gate HCMOS technology has a speed comparable to LSTTL while retaining the important CMOS qualities, see Fig.1.

Table 2 compares the operating characteristics of the 74HC and 74HCT IC types with those of LSTTL in more

detail. 74HC and 74HCT devices are ideal for use in new equipment designs and, as alternatives to TTL devices, in existing designs. The 74HCT circuits which are direct replacements for LSTTL circuits also enhance performance in many respects.

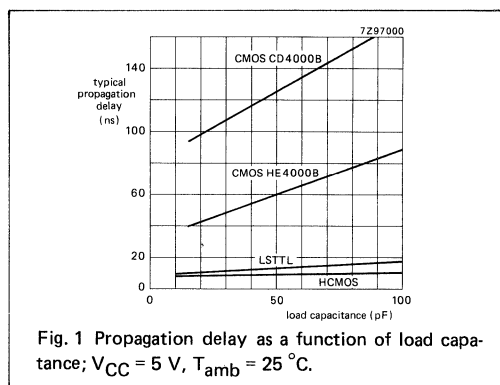


Fig. 1 Propagation delay as a function of load capacitance;  $V_{CC} = 5\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ .

Table 1 Comparison of CMOS and TTL technologies; supply voltage  $V_{CC} = 5\text{ V}$ ; ambient temperature  $T_{amb} = 25^\circ\text{C}$ ; load capacitance  $C_L = 15\text{ pF}$

parameters	technology	HCMOS	metal gate CMOS	standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
	family	74HC	4000 CD HE	74	74LS	74S	74ALS	74AS	74F
<b>Power dissipation, typ. (mW)</b>									
Gate static		0.0000025	0.001	10	2	19	1.2	8.5	5.5
Gate dynamic @ 100 kHz		0.075	0.1	10	2	19	1.2	8.5	5.5
Counter static		0.000005	0.001	300	100	500	60	—	190
Counter dynamic @ 100 kHz		0.125	0.120	300	100	500	60	—	190
<b>Propagation delay (ns)</b>									
Gate typical		8	94 40	10	9.5	3	4	1.5	3
Gate maximum		14	190 80	20	15	5	7	2.5	4
<b>Delay/power product (pJ)</b>									
Gate at 100 kHz		0.52	9 4	100	19	57	4.8	13	16.5
<b>Maximum clock frequency (MHz)</b>									
typical		55	4 12	25	33	100	60	160	125
D-type flip-flop minimum		30	2 6	15	25	75	40	—	100
Counter typical		45	2 6	32	32	70	45	—	125
Counter minimum		25	1 3	25	25	40	—	—	100
<b>Output drive (mA)</b>									
standard outputs		4	0.51 0.8	16	8	20	8	20	20
bus outputs		6	1.6	48	24	64	24	48	64
<b>Fan-out (LS-loads)</b>									
standard outputs		10	1 2	40	20	50	20	50	50
bus outputs		15	4	120	60	160	60	120	160

**Table 2:** Comparison of HCMOS and LSTTL circuits ( $V_{CC} = 5\text{ V}$  unless stated otherwise;  $C_L = 50\text{ pF}$ )

characteristic	74HCXXX (note 1) 74HCTXXX	74LSXXX
Max. quiescent power dissipation over temp. range at $V_{CCmax}$		
per gate (mW)	0.027	6
per flip-flop (mW)	0.11	22
per 4-stage counter (mW)	0.44	175
per transceiver/buffer (mW)	0.055	60
Max. dynamic power dissipation ( $C_L = 50\text{ pF}$ )		
at $f_i$ (MHz)	1    10	0.1 to 1    10
per gate (mW)	2.25    22	6    22
per flip-flop (mW)	2.5    24	22    27
per 4-stage counter (mW)	3    27	175    200
per buffer/transceiver (mW)	2.5    24	60    90
Operating supply voltage (V)	2 to 6 (HC) 4.5 to 5.5 (HCT)	4.75 to 5.25
Operating temperature range ( $^{\circ}\text{C}$ )	-40 to +85 -40 to +125	0 to +70
Max. noise margin ( $V_{NMH}/V_{NML}$ V; $I_{OHCMOS} = 20\text{ }\mu\text{A}$ ; $I_{OLSTTL} = 4\text{ mA}$ )	1.4/1.4 (HC) 2.9/0.7 (HCT)	0.7/0.4
Input switching voltage stability over temp. range	$\pm 60\text{ mV}$	$\pm 200\text{ mV}$
Min. output drive current at $T_{amb\ max}$ and $V_{CCmin}$ (mA)		
source current ( $V_{OH} = 2.7\text{ V}$ ; note 2)		
standard logic	-8	-0.4
bus logic	-12	-2.6
sink current		
standard logic ( $V_{OL} = 0.4\text{ V}$ )	4	4
standard logic ( $V_{OL} = 0.5\text{ V}$ )	6	8
bus logic ( $V_{OL} = 0.4\text{ V}$ )	8	12
bus logic ( $V_{OL} = 0.5\text{ V}$ )	9	24
Typ. output transition time (ns) ( $C_L = 15\text{ pF}$ )		
standard logic		
$t_{TLH}$	6	15
$t_{THL}$	6	6
bus logic		
$t_{TLH}$	4	15
$t_{THL}$	4	6
Typ. propagation delay (ns) ( $C_L = 15\text{ pF}$ ; note 3)		
gate $t_{PHL}/t_{PLH}$	8/8	8/11
flip-flop $t_{PLH}$	14	15
$t_{PHL}$	14	22
Typ. clock rate of a flip-flop; note 5 (MHz)	50	33
Max. input current ( $\mu\text{A}$ )		
$I_{IL}$	-1	-400 to -800
$I_{IH}$	1	40
3-state output leakage current ( $\pm\text{ }\mu\text{A}$ )	5	20
Reliability (%/1000 h at 60% confidence level)	0.0005	0.008 (note 4)

**Notes**

1. Data valid for HCMOS between  $-40\text{ }^{\circ}\text{C}$  and  $+85\text{ }^{\circ}\text{C}$ .
2.  $V_{OH}$  for a few LSTTL bus outputs is specified as 2.4 V.
3. Refer to data sheets for the effect of capacitive loading.
4. RADC report.
5. Measured with a 50% duty factor for HCMOS. For LSTTL, per industry convention, the maximum clock frequency is specified with no constraints on rise and fall times, pulse width or duty factor.

CONSTRUCTION

Our HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate CMOS process. Figure 2 shows the construction of a basic inverter from the HE4000B series and its HCMOS successor.

The polysilicon gate of a HCMOS transistor is deposited over a thin gate oxide before the source and drain diffusions are defined. Source and drain regions are formed using ion implantation, with the polysilicon gates acting as masks for the implantation. The source and drain are automatically aligned to the gate, minimizing gate-to-source and gate-to-drain capacitances. In addition, the junction capacitances, which are proportional to the junction area, are reduced because of the shallower diffusions. Figure 3(c) shows the parasitic capacitances in a CMOS inverter.

In a metal-gate CMOS transistor, the source and drain are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. This is why a metal-gate CMOS

transistor has a higher overlap capacitance than an HCMOS transistor. Furthermore, the deeper diffusions of metal-gate CMOS make the junction capacitance larger.

In a silicon-gate MOS transistor, there are three interconnect layers (diffusion, polysilicon and metal) instead of the two layers (diffusion and metal) in a metal-gate MOS transistor. This makes a silicon-gate MOS transistor more compact. The shorter gate length means higher drive capability, which in turn increases the speed at which a silicon-gate MOS transistor can charge or discharge junction capacitance. The drain current of a saturated MOS transistor which determines the speed of the transistor is:

$$I_{DS} = \frac{-\beta}{2} \times \frac{\text{gate width}}{\text{gate length}} \times (\text{gate voltage} - \text{threshold voltage})^2$$

where  $\beta$  is the current gain factor which is proportional to the thickness of the oxide layer.

The threshold voltage is typically 0.7 V for HCMOS.

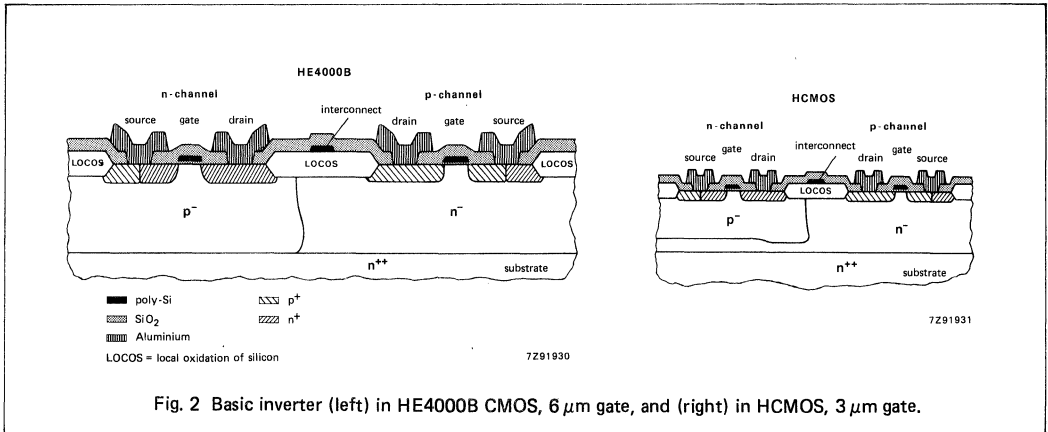


Fig. 2 Basic inverter (left) in HE4000B CMOS, 6 μm gate, and (right) in HCMOS, 3 μm gate.

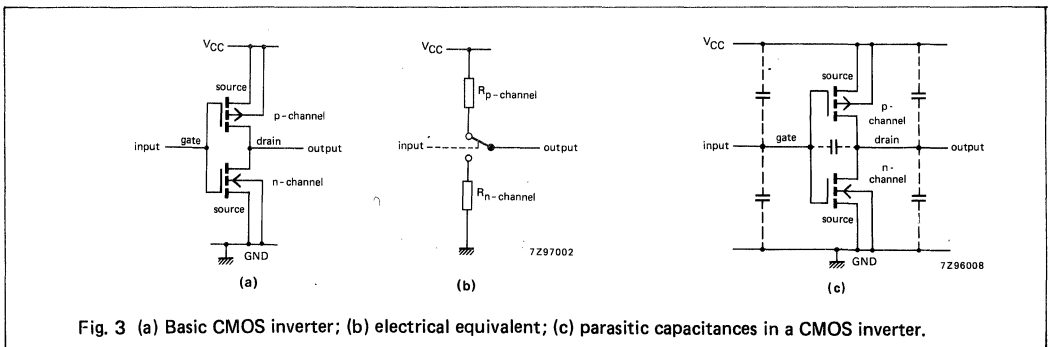


Fig. 3 (a) Basic CMOS inverter; (b) electrical equivalent; (c) parasitic capacitances in a CMOS inverter.

AC CHARACTERISTICS

Test conditions

The propagation delays and transition times specified in the HCMOS data sheets are guaranteed when the circuits are tested according to the conditions stated in the chapter 'Family Characteristics', section 'Family Specifications'. For some circuits such as counters and flip-flops, the test conditions are defined further by the a.c. set-up requirements specified in the data sheet.

Values given in the data sheets are for the whole operating temperature range (-40 to +125°C) and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for 74HC devices, and 4.5 V for 74HCT devices. This is a much tougher specification than that commonly used for LSTTL, where the characteristics are usually only specified at 25°C and for a 5 V supply. Furthermore, the published a.c. characteristics of HCMOS are guaranteed for a capacitive test load of 50 pF, a more realistic load than the 15 pF specified for LSTTL and one that loads the device as the output switcher. The published values for HCMOS are therefore representative of those measured in actual systems.

Comparing the speed of HCMOS and LSTTL

A feature of a HCMOS circuit is its speed - in general, comparable to that of its LSTTL equivalent. Owing to the different (more informative) way of specifying data for HCMOS devices, it will be useful to indicate how to compare the published data for HCMOS and LSTTL.

For example, in an LSTTL specification, the use of a 15 pF load instead of a 50 pF one means the maximum propagation delays and enable times published for the LSTTL device will be up to 2.5 ns (typ. 1.3 ns) shorter than those for the HCMOS equivalent. In addition, measuring at the nominal LSTTL supply voltage of 5 V instead of 4.5 V (HCMOS) reduces propagation delays and enable times by a further 10%. So, a 30 ns propagation delay for a HCMOS device is equivalent to a  $(30 - 2.5)0.9 = 25$  ns delay for an LSTTL device measured at 4.5 V and with a 15 pF load.

Disable times are measured under different test conditions too - for HCMOS with a 50 pF, 1 kΩ load, for LSTTL with a 5 pF, 2 kΩ load or for a 45 pF, 667 Ω load. To compare a HCMOS disable time with that for a LSTTL device with a 5 pF load, subtract 4 ns from the published HCMOS disable time and multiply by 0.9. To compare a value for a 45 pF load, subtract 2 ns and multiply by 0.9. For example, a 30 ns HCMOS disable time is equivalent to  $(30 - 4)0.9 = 23$  ns for a 5 pF load and  $(30 - 2)0.9 = 25$  ns for a 45 pF load.

Set-up hold and removal times are not affected by output load, only by supply voltage. To compare a pub-

lished HCMOS value with an LSTTL value, multiply the HCMOS value by 0.9.

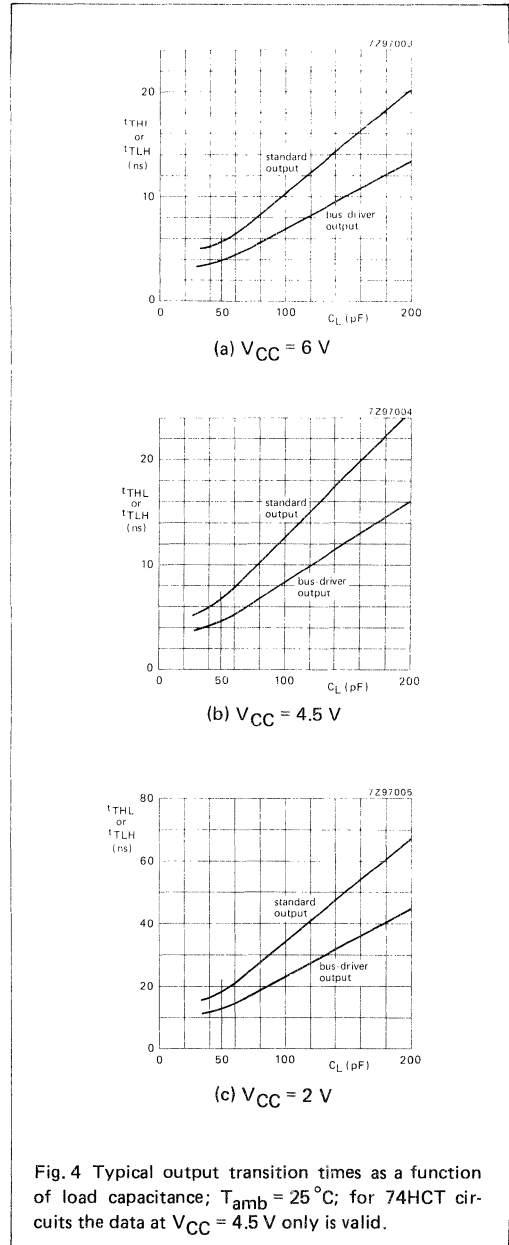


Fig. 4 Typical output transition times as a function of load capacitance; T<sub>amb</sub> = 25°C; for 74HCT circuits the data at V<sub>CC</sub> = 4.5 V only is valid.

Operating frequency is also unaffected by output load, but is affected by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the value for HCMOS at 4.5 V by 1.1.

In general, these guidelines apply both to 74HC and to 74HCT devices. For 74HCT devices however, the propagation delay is the time for the output to reach 1.4 V (compared with 50%V<sub>CC</sub> for 74HC devices), so HIGH-to-LOW output transition times are slightly more dependent on load and the LOW-to-HIGH transition times are slightly less dependent on load than the 74HC versions.

**Propagation delays and transition times**

The symmetrical push-pull output structure of both 74HC and 74HCT devices gives symmetrical rise/fall times and provides for a well-balanced system design. Table 3 shows the maximum output transition times for all standard and bus-driver HCMOS outputs.

The influence of capacitive loading on output transitions is shown in Fig.4; A good approximation of the output transition times can be calculated using the data of Table 4.

**Table 3: Maximum output transition times (C<sub>L</sub> = 50 pF)**

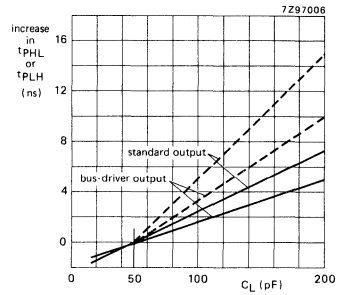
	V <sub>CC</sub> (V)	maximum output transition time (ns)		
		T <sub>amb</sub> = 25 °C	T <sub>amb</sub> = 85 °C	T <sub>amb</sub> = 125 °C
standard output	2	75	95	110
	4.5*	15	19	22
bus-driver output	2	60	75	90
	4.5*	12	15	18
	6	13	16	19

\* 74HC and 74HCT devices; all other data for 74HC devices only.

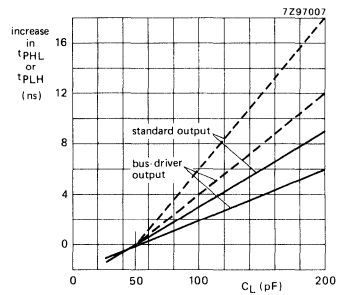
**Table 4: Typical output transition times for load capacitances greater than the standard 50 pF load, see Fig.4**

V <sub>CC</sub>	t <sub>THL</sub> or t <sub>TLH</sub>	
	standard output	bus-driver output
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

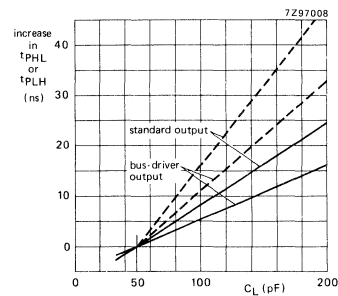
Note: values in pF are the load capacitance minus 50 pF.



(a) V<sub>CC</sub> = 6 V



(b) V<sub>CC</sub> = 4.5 V



(c) V<sub>CC</sub> = 2 V

--- expected maximum  
 ——— typical value

Fig. 5 Increase in propagation delay for 74HC devices as a function of load capacitance; T<sub>amb</sub> = 25 °C.

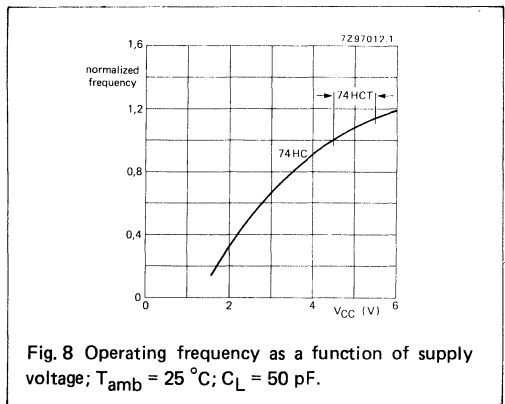
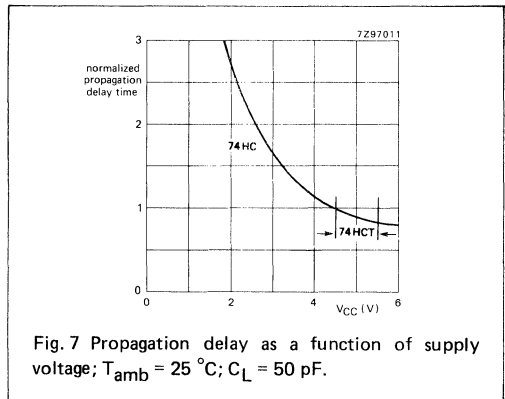
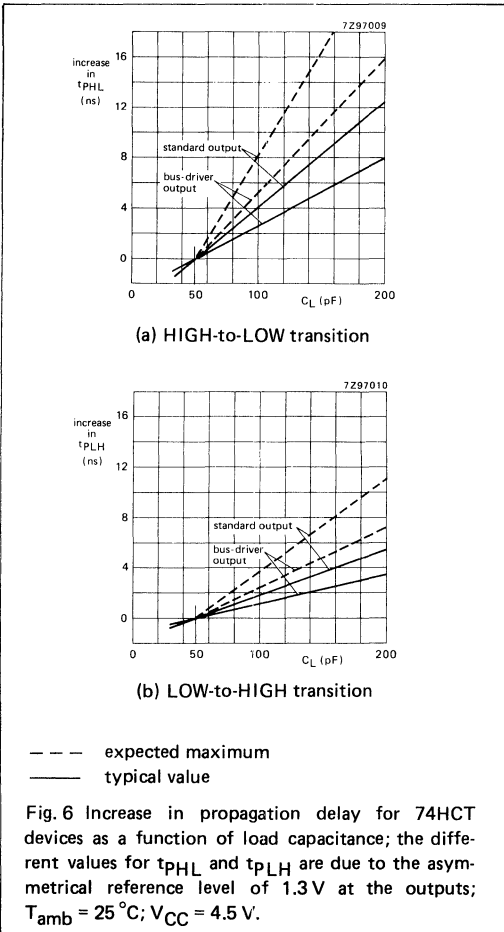
A parameter specified for TTL devices is the output short-circuit current HIGH ( $I_{OS}$ ). Originally intended to reassure the TTL user that the device would withstand accidental grounding, this parameter has become a measure of the ability of the circuit to charge the line capacitance and is used to calculate propagation delays. In CMOS devices however, there is no need to specify  $I_{OS}$  because the purely capacitive loads allow extrapolation of the a.c. parameters over the whole loading range. Figure 5 (for 74HC devices) and Fig.6 (for 74HCT devices) show the increase in propagation delay for loads greater than 50 pF. The additional delay can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs.31 to 34), the propagation delay is the time taken for the output voltage to reach 50%

of  $V_{CC}$  for 74HC devices, or 1.4V for 74HCT devices. Since a saturated output transistor acts as a current source, the additional delay is  $\Delta C/V$ , where  $\Delta C$  is the load capacitance minus 50 pF,  $V$  is the voltage swing at the output to the switching level of the next circuit, and  $I$  is the average source current of the saturated output.

*Supply voltage dependence of propagation delay*

The dynamic performance of a CMOS device depends on its drain characteristics. These are related to the switching thresholds and the gate-to-source voltage  $V_{GS}$  which is equal to the supply voltage  $V_{CC}$ . A reduction in  $V_{CC}$  adversely affects the drain characteristics, increasing the propagation delays.

Over the supply voltage range of 74HCT devices, 4.5 V to 5.5 V, the effects of different propagation delays on performance are minimal. Over the supply voltage range of 74HC circuits, 2 to 6 V, the effects on performance are significant, see Figs.7 and 8.



**Temperature dependence of propagation delay**

In TTL circuits,  $\beta$  (current gain), internal resistances and forward-voltage drops are all temperature-dependent. In HCMOS circuits, essentially only the carrier mobility, which affects the propagation delay, is temperature dependent. In general, propagation delay increases by about 0.3% per °C above 25 °C.

Between 25 °C and 125 °C,

$$t_p = t_p'(1.003)^{T_{amb}-25}$$

where:

$t_p'$  is the propagation delay at 25 °C,

$T_{amb}$  is the ambient temperature in °C.

Between -40 °C and +25 °C,

$$t_p = t_p'(0.997)^{25-T_{amb}}$$

Figure 9 shows the temperature dependence of a characteristic such as propagation delay.

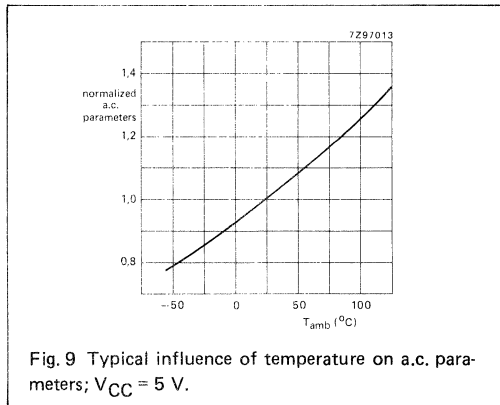


Fig. 9 Typical influence of temperature on a.c. parameters;  $V_{CC} = 5 V$ .

**Derating system for a.c. characteristics**

Because HCMOS devices are a coherent family, manufactured under strictly-controlled conditions, it is possible to have a common set of derating coefficients for temperature and supply voltage that is valid for all a.c. characteristics of all devices. Table 5 shows the derating coefficients which are derived from the published values of the a.c. characteristics at 25 °C for  $V_{CC} = 4.5 V$ , denoted by x in the Table. The coefficients have been established after extensive high-temperature testing at many supply voltages. A temperature coefficient of  $-0.4\%/^{\circ}C$  was established after comparing the test results with worst-case calculations. The voltage derating given in Table 5 is conservative compared with that shown in Fig.7 for propagation delay. For operating frequencies (Fig.8), the reciprocal of the derating coefficients shown should be used.

**Table 5:** Derating coefficients for the a.c. characteristics of HCMOS devices

supply voltage	ambient temperature		
	25 °C	85 °C	125 °C
2 V	5 (5x)	6.25 (5y)	7.5 (5z)
4.5 V*	1 (x)	1.25 ( $y = 1.25x$ )	1.5 ( $z = 1.5x$ )
6 V	0.85 (0.85x)	1.0625 (0.85y)	1.275 (0.85z)

All coefficients are derived from the value of the a.c. characteristic at  $V_{CC} = 4.5 V$  and  $T_{amb} = 25^{\circ}C$  denoted in the table by x.

\* 74HC and 74HCT devices; all other data for 74HC devices only.

**Clock pulse requirements**

All HCMOS flip-flops and counters contain master-slaves with level-sensitive clock inputs. When the voltage at the clock input reaches the voltage threshold of the device, data in the master (input) section is transferred to the slave (output) section. The threshold for 74HC devices is typically 50% of  $V_{CC}$  and that for 74HCT devices is 28% of  $V_{CC}$  (1.4 V at  $V_{CC} = 5 V$ ). The thresholds are virtually independent of temperature.

The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at  $V_{CC} = 4.5 V$ ).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at the clock input, which eliminates the need to specify a maximum rise/fall time. The flip-flops 74HC/HCT73, 74, 107, 109 and 112 have special Schmitt-trigger circuits for increased tolerance to slow rise/fall times and ground noise.

The published maximum input clock frequency ratings for clocked devices are for a 50% duty factor input clock. At these rated frequencies, the outputs will swing between  $V_{CC}$  and GND, assuming no d.c. load on the outputs. This is a very conservative and reliable method of rating the

clock-input-frequency limits for HCMOS devices which are always at least as good as those for LSTLL even though they may appear to be inferior. This is because the maximum operating frequency of a TTL device is published, not for a 50% duty factor clock, but for a minimum clock pulse width.

### System (parallel) clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig.10.

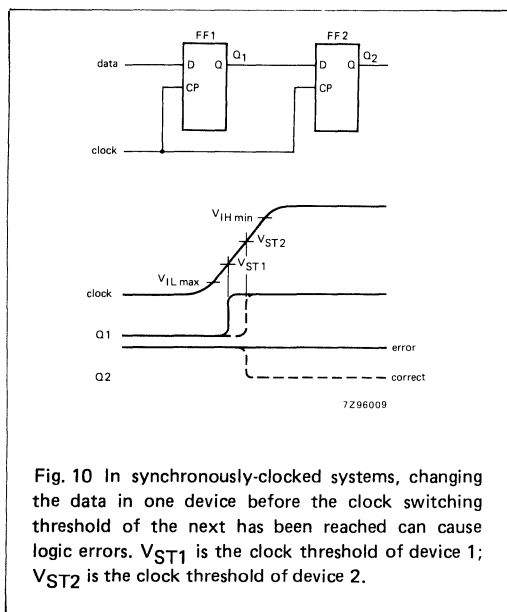


Fig. 10 In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors.  $V_{ST1}$  is the clock threshold of device 1;  $V_{ST2}$  is the clock threshold of device 2.

To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

For a HCMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for  $V_{CC} = 2\text{ V}$ , 4.5 V and 6 V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

### Minimum a.c. characteristics

Minimum values of a.c. characteristics are not specified in the data sheets. However, it is sometimes useful to know

them, for example when checking whether data set-up and hold times are obeyed. At 25 °C and 4.5 V supply voltage, the minimum values are one quarter of the published maximum values. To calculate the minimum values at other temperatures, derate by 0.27%/°C.

Table 6 gives the derating coefficients for calculating the minimum propagation delays of HCMOS devices at various supply voltages and temperatures.

Table 6: Derating coefficient for the expected minimum propagation delay of HCMOS devices

supply voltage	ambient temperature		
	25 °C	85 °C	125 °C
2 V	2 (2x)	2.34 (2y)	2.62 (2z)
4.5 V*	1 (x)	1.17 (y = 1.17x)	1.31 (z = 1.31x)
6 V	0.8 (0.8x)	0.936 (0.8y)	1.048 (0.8z)

All coefficients are derived from the value of the a.c. characteristic at  $V_{CC} = 4.5\text{ V}$  and  $T_{amb} = 25\text{ °C}$  denoted in the table by x.

\* 74HC and 74HCT devices; all other data for 74HC devices only.

### POWER DISSIPATION

#### Static

When a HCMOS device is not switching, the p-channel and n-channel transistors don't conduct at the same time, so leakage current flows between  $V_{CC}$  and GND. Because this leakage current is typically a few nA, HCMOS power dissipation is extremely low.

Static power dissipation can be calculated for both 74HC and 74HCT devices from the maximum quiescent current specified in the data sheets, see Table 7.

Table 7: Maximum quiescent current of HCMOS devices at  $V_{CCmax}^*$  ( $V_I = V_{CC}$  or GND;  $I_O = 0$ )

device complexity	typical at 25 °C	quiescent current maximum		
		25 °C	85 °C	125 °C
SSI	2 nA	2 µA	20 µA	40 µA
FF	4 nA	4 µA	40 µA	80 µA
MSI	8 nA	8 µA	80 µA	160 µA

\* 6 V for 74HC; 5.5 V for 74HCT.



**Dynamic**

When a device is clocked, power is dissipated charging and discharging on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. However, this transient energy loss is typically only 10% of that due to parasitic capacitance.

The total dynamic power dissipation per device ( $P_D$ ) is:

$$P_D = C_{PD}V_{CC}^2f_i + \Sigma(C_LV_{CC}^2f_o) \quad (1)$$

where:

- $C_{PD}$  is the power dissipation capacitance per package
- $f_i$  is the input frequency
- $f_o$  is the output frequency
- $C_L$  is the total external load capacitance per output.

The second term of equation (1) implies summing the product of the effective output load capacitance and frequency for each output. However, a good approximation of the total dynamic power dissipation of an HCMOS system can be obtained by summing the published  $C_{PD}$  values and load capacitance for the HCMOS devices used and, assuming an average frequency, using equation (1).

For one-shot circuits, gates configured as oscillators, phase-locked loops and devices used in a linear mode, additional dissipation is caused by static supply currents ( $I_{CC}$ ) whose values are given in the device data sheets.

**Power dissipation capacitance**

$C_{PD}$  is specified in the device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Fig.11. The worst-case operating conditions for  $C_{PD}$  are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Table 8 gives the pin status for HCMOS devices during a  $C_{PD}$  test. Devices which can be separated into independent sections are measured per section, the others are measured per device.

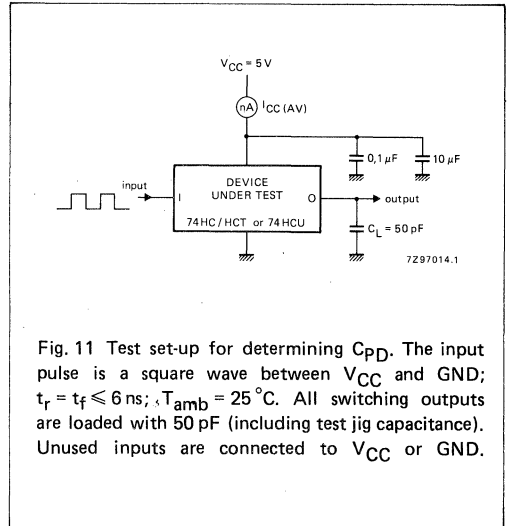


Fig. 11 Test set-up for determining  $C_{PD}$ . The input pulse is a square wave between  $V_{CC}$  and GND;  $t_r = t_f \leq 6$  ns;  $T_{amb} = 25^\circ C$ . All switching outputs are loaded with 50 pF (including test jig capacitance). Unused inputs are connected to  $V_{CC}$  or GND.

The recommended test frequency for determining  $C_{PD}$  is 1 MHz, but this is best increased to 10 MHz when  $I_{CC}$  is low and the device quiescent current influences  $I_{CC(AV)}$ . Loading the switched outputs gives a more realistic value of  $C_{PD}$ , because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

The values of  $C_{PD}$  in the data sheet have been calculated using:

$$C_{PD} = \frac{I_{dyn(device)}}{V_{CC}f_i}$$

where:

$$I_{dyn(device)} = I_{CC(AV)} - I_{dyn(load)}$$

$$I_{dyn(load)} = \Sigma(C_LV_{CC}f_o)$$

Table 8: Pin conditions for  $C_{PD}$  tests.

74HC/ HCT	equiv- alent load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
02	50	C	P	L	O	D	D	G	D	D	O	D	D	O	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
03	0	P	H	B	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
U04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
08	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
14	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
20	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
21	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
27	50	P	L	D	D	D	O	G	O	D	D	D	C	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
30	50	P	H	H	H	H	H	G	C	O	O	H	H	O	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
32	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
42	100	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	-	-	-	-	-	-	-	-	-	-	-	-
58	50	P	D	D	D	D	O	G	O	L	L	L	H	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
73	50	P	H	H	V	D	D	D	O	O	D	G	C	C	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-
74	50	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
75	50	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	-	-	-	-	-	-	-	-	-	-	-	-
85	50	L	H	P	H	O	C	O	G	L	L	L	L	L	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-
86	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	P	-	-	-	-	-	-	-	-	-	-	-	-	-	-
107	50	H	C	C	H	O	O	G	D	D	D	D	P	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
109	50	H	H	L	P	H	C	C	G	O	O	D	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-
112	50	P	H	H	H	C	C	O	G	O	D	D	D	D	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-
123	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	-	-	-	-	-	-	-	-	-	-	-	-
125	50	L	P	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
126	50	H	P	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
132	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
137	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-
138	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-
139	100	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-
147	50	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	-	-	-	-	-	-	-	-	-	-	-	-
151	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-
153	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	-	-	-	-	-	-	-	-	-	-	-	-
154	100	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	L	L	L	L	L	L	P	V	-	-	-	-
157	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	-	-	-	-	-	-	-	-	-	-	-	-
158	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	-	-	-	-	-	-	-	-	-	-	-	-
160	55	H	P	D	D	D	H	G	H	H	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-
161	50	H	P	D	D	D	H	G	H	H	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-

(continued on next page)

Table 8 (continued)

74HC/ HCT	equiv- alent load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
162	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-
163	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-
164	200	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
165	50	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-
166	25	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	-	-	-	-	-	-	-	-	-	-	-	-
173	25	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	-	-	-	-	-	-	-	-	-	-	-	-
174	25	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	-	-	-	-	-	-	-	-	-	-	-	-
175	50	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	-	-	-	-	-	-	-	-	-	-	-	-
181	250	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	L	H	L	H	L	H	V	-	-	-	-	-
182	150	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	-	-	-	-	-	-	-	-	-	-	-	-
190	60	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	-	-	-	-	-	-	-	-	-	-	-	-
191	53	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	-	-	-	-	-	-	-	-	-	-	-	-
192	60	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	-	-	-	-	-	-	-	-	-	-	-	-
193	50	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	-	-	-	-	-	-	-	-	-	-	-	-
194	100	H	Q	D	D	D	D	G	H	L	P	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-
195	125	H	H	L	D	D	D	G	H	P	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-
221	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	-	-	-	-	-	-	-	-	-	-	-	-
237	100	P	L	L	L	L	H	O	G	O	O	O	O	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-
238	100	P	L	L	L	L	H	O	G	O	O	O	O	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-
240	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	-	-	-	-	-	-	-	-
241	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	H	V	-	-	-	-	-	-	-	-
242	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
243	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
244	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	-	-	-	-	-	-	-	-
245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	-	-	-	-	-	-	-	-
251	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-
253B	50	L	L	D	D	L	H	C	G	O	D	D	D	P	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-
257	50	P	L	H	C	D	D	O	G	O	D	D	O	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-
258	50	P	L	H	C	D	D	O	G	O	D	D	O	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-
259	25	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	-	-	-	-	-	-	-	-	-	-	-	-
7266	50	P	L	C	O	D	D	G	D	D	O	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
273	25	H	C	Q	D	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	-	-
280	100	L	L	O	L	C	C	G	P	L	L	L	L	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-
283	250	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	-	-	-	-	-	-	-	-	-	-	-	-
297	12	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	-	-	-	-	-	-	-	-	-	-	-	-
299	250	H	L	L	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	-	-	-	-	-	-	-	-	-
354	100	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	-	-	-	-	-	-	-	-
356	50	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	H	C	C	V	-	-	-	-	-	-	-	-	-	-
365	50	L	P	C	D	O	D	O	G	O	D	O	D	O	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-
366	50	L	P	C	D	O	D	O	G	O	D	O	D	O	L	V	-	-	-	-	-	-	-	-	-	-	-	-	-

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Table 8 (continued)

74HC/ HCT	equiv- alent load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
367	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-
368	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	-	-	-	-	-	-	-	-	-	-	-	-
373	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	-
374	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	-
377	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	-
390	50	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	
393	47	P	L	C	C	C	C	C	G	O	O	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
423	100	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	-	-	-	-	-	-	-	-	-	-	-	
533	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	
534	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	-	-	-	-	-	-	-	
540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	-	-	-	-	-	-	-	
541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	-	-	-	-	-	-	-	
563	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	-	-	-	-	-	-	-	
564	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	-	-	-	-	-	-	-	
573	25	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	-	-	-	-	-	-	-	
574	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	-	-	-	-	-	-	-	
583	250	H	H	H	L	L	C	C	G	C	C	C	H	P	L	L	V	-	-	-	-	-	-	-	-	-	-	-	
597	25	D	D	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	-	-	-	-	-	-	-	-	-	
7597	25	D	D	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	-	-	-	-	-	-	-	-	-	
640	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	L	V	-	-	-	-	-	-	
643	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	O	C	L	V	-	-	-	-	-	-	
646	50	D	L	H	P	D	D	D	D	D	D	D	D	G	O	O	O	O	O	O	C	L	D	D	V	-	-	-	
648	50	D	L	H	P	D	D	D	D	D	D	D	D	D	G	O	O	O	O	O	C	L	D	D	V	-	-	-	
670	100	Q	Q	Q	L	P	C	C	G	C	C	L	L	L	P	Q	V	-	-	-	-	-	-	-	-	-	-	-	
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	C	V	-	-	-	-	-	-	-	
4002	50	C	P	L	L	L	O	G	O	D	D	D	D	O	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4015	100	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	-	-	-	-	-	-	-	-	-	-	-	
4016	0	O	O	O	D	D	D	G	O	O	O	O	D	P	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	-	-	-	-	-	-	-	-	-	-	-	
4020	48	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	
4024	48	P	L	C	C	C	C	G	O	C	O	C	C	O	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4040	48	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	
4046A	50	O	C	L	O	H	O	O	G	O	O	O	O	P	O	V	-	-	-	-	-	-	-	-	-	-	-	-	
4049	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	-	-	-	-	-	-	-	-	-	-	-	-	
4050	50	V	C	P	O	D	O	D	G	D	O	D	O	D	O	-	-	-	-	-	-	-	-	-	-	-	-	-	
4051	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	-	-	-	-	-	-	-	-	-	-	-	
4052	0	O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	-	-	-	-	-	-	-	-	-	-	-	
4053	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	-	-	-	-	-	-	-	-	-	-	-	
4059	17	P	D	H	L	L	L	L	L	L	L	H	G	H	H	L	L	L	L	L	L	L	L	L	C	V	-	-	
4060	106	C	C	C	C	C	C	G	C	C	P	L	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	

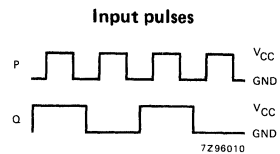
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Table 8 (continued)

74HC/ HCT	equiv- alent load (pF)	pin numbers																												
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
4066	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
4067	0	O	O	O	O	O	O	O	O	O	O	P	L	G	L	L	L	O	O	O	O	O	O	O	O	V	-	-	-	-
4075	50	P	L	D	D	D	O	G	L	C	O	D	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
4094	250	H	Q	P	C	C	C	C	G	C	C	C	C	C	H	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4316	0	O	O	O	O	P	D	L	G	G	O	O	O	D	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4351	0	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	-	-	-	-	-	-	-	-	-	
4352	0	O	O	O	O	O	L	H	G	G	H	P	L	O	O	O	O	O	O	V	-	-	-	-	-	-	-	-	-	
4353	0	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	-	-	-	-	-	-	-	-	-	
4510	55	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	-	-	-	-	-	-	-	-	-	-	-	-	
4511	200	L	L	H	H	L	L	P	G	C	C	O	O	C	O	C	V	-	-	-	-	-	-	-	-	-	-	-	-	
4514	100	H	P	L	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	-	-	-	-	-	
4515	100	H	P	L	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	-	-	-	-	-	
4516	50	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	-	-	-	-	-	-	-	-	-	-	-	-	
4518	50	P	H	C	C	C	L	G	D	D	O	O	O	O	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4520	47	P	H	C	C	C	L	G	D	D	O	O	O	O	D	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
4538	100	G	R	H	P	H	C	C	G	O	O	D	D	L	O	G	V	-	-	-	-	-	-	-	-	-	-	-	-	
4543	50	H	L	L	H	L	P	L	G	C	C	C	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
7030	325	G	G	C	P	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	C	C	C	C	C	C	C	C	C	C	P	H	V	
7046A	50	O	C	L	O	H	O	O	G	O	O	O	O	P	O	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
40102	5	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	-	-	-	-	-	-	-	-	-	-	-	-	
40103	3	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	-	-	-	-	-	-	-	-	-	-	-	-	
40104	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	V	-	-	-	-	-	-	-	-	-	-	-	-	-	
40105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	P	V	-	-	-	-	-	-	-	-	-	-	-	-	-	

**Key**

- V = V<sub>CC</sub> (+5V)
- G = ground
- H = logic 1 (V<sub>CC</sub>) — inputs at V<sub>CC</sub> for HC types; 3.5 V for HCT types
- L = logic 0 (ground)
- D = don't care — either H or L but not switching
- C = a 50 pF load to ground
- O = an open pin; 50 pF to ground is allowed
- P = input pulse (see illustration)
- Q = half frequency pulse (see illustration)
- R = 1 kΩ pull-up resistor to an additional 5 V supply other than the V<sub>CC</sub> supply
- B = both R and C



### Conditions for $C_{pD}$ tests

**Gates.** All inputs except one are held at either  $V_{CC}$  or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency.  $C_{pD}$  is specified per-gate.

**Decoders.** One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to  $V_{CC}$  or GND, whichever enables operation.  $C_{pD}$  is specified per-independent-decoder.

**Multiplexers.** One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With three-state multiplexers,  $C_{pD}$  is specified per output function for enabled outputs.

**Bilateral switches.** The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW.  $C_{pD}$  is specified per switch.

**Three-state buffers and transceivers.**  $C_{pD}$  is specified per buffer with the outputs enabled. Measurement is as for simple gates.

**Latches.** The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. Three-state latches are measured with their outputs enabled.  $C_{pD}$  is specified per-latch.

**Flip-flops.** Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

**Shift registers.** The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at  $V_{CC}$  or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

**Counters.** A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for  $C_{pD}$  are given for each counter in the device.

**Arithmetic circuits.** Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

**Display drivers.**  $C_{pD}$  is not normally required for LED drivers because LEDs consume so much power as to make the effect of  $C_{pD}$  negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed,  $C_{pD}$  is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

**One-shot circuits.** In some cases, when the device  $I_{CC}$  is significant,  $C_{pD}$  is not specified. When it is specified,  $C_{pD}$  is measured by toggling one trigger input to make the output a squarewave. The timing resistor is tied to a separate supply (equal to  $V_{CC}$ ) to eliminate its power contribution.

### Additional power dissipation in 74HCT devices

When the inputs of a 74HCT device are driven by a TTL device at the specified minimum HIGH output level of  $V_{OH} = 2.4$  V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current ( $\Delta I_{CC}$ ). This current has been considerably reduced by proprietary development of 74HCT input stages, see '74HCT inputs'.

The value of  $\Delta I_{CC}$  specified in the data sheets is per input and at the worst-case input voltage of  $V_{CC} - 2.1$  V for  $V_{CC}$  between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum  $V_{CC}$  and minimum  $V_{OH}$ ), see Table 9.

The additional power dissipation P is:

$$P = V_{CC} \times \Delta I_{CC} \times \text{duty factor HIGH} \times \text{unit load coefficient}$$

The unit load coefficient for an input is a factor by which the value of  $\Delta I_{CC}$  given in the data sheet has to be multiplied. A unit load coefficient is published for each 74HCT device. It is a function of the size of the input p-channel transistor.

**Table 9:** Worst-case additional quiescent supply current ( $\Delta I_{CC}$ ) for 74HCT devices

	$T_{amb}$ ( $^{\circ}C$ )				UNIT	TEST CONDITIONS		
	74HCT					$V_{CC}$ V	$V_I$	OTHER
	+25		-40 to +85	-40 to +125				
	typ.	max.	max.	max.				
$\Delta I_{CC}$ per input pin for a unit load coefficient of 1*	100	360	450	490	$\mu A$	4.5 to 5.5	$V_{CC}-2.1 V$	other inputs at $V_{CC}$ or GND $I_O = 0$

\* The additional quiescent supply current per input is determined by the  $\Delta I_{CC}$  unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case ( $V_I = 2.4 V$ ;  $V_{CC} = 5.5 V$ ) specification is:  $\Delta I_{CC} = 0.65 mA$  (typical) and 1.8 mA (maximum) across temperature.

**Power dissipation due to slow input rise/fall times**

When an output stage switches, there is a brief period when both output transistors conduct. The resulting ‘through-current’ is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time.

As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than  $V_{CC}$  minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at  $V_I = 0.5 V_{CC}$  for 74HC devices, and  $V_I = 28\%V_{CC}$  for 74HCT devices, the maximum current being determined by the geometry of the input transistors. The through-current is proportional to  $V_{CC}^n$  where n is about 2.2. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig.12.

When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation, see Schmitt-trigger data sheets. In the case of RC oscillators, or oscillators constructed with Schmitt triggers this contribution to the power dissipation is frequency-dependent.

**Comparison with LSTTL power dissipation**

The dynamic power dissipation of a HCMOS device is frequency-dependent; above 1 MHz, that of an LSTTL device is too. Below 1 MHz, the dynamic component of power dissipation of an LSTTL device is negligible compared to the static component. Figure 13 shows the average power dissipation of four HCMOS devices and their LSTTL equivalents. Because all functions in a multi-functional LSTTL device are biased when power is applied, for comparison, the dissipation of whole HCMOS devices besides individual functions are given.

In Fig.13 it can be seen that:

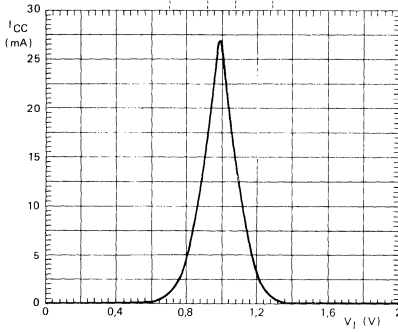
- for SSI gate types, the HCMOS power dissipation is less than LSTTL power dissipation below about 1 MHz
- for more complex types such as a 74HC/HCT138 3-to-8 line decoder HCMOS power dissipation is less than LSTTL power dissipation up to 10 MHz.

In typical microcomputer systems, the operating frequency or the data/address signal rates will usually vary, whereas Fig.13 is for continuous operation at a constant frequency. Average operating frequencies are usually far below the peak frequencies, particularly in the 100 kHz region where the power dissipation of HCMOS is several orders of magnitude less than that of LSTTL.

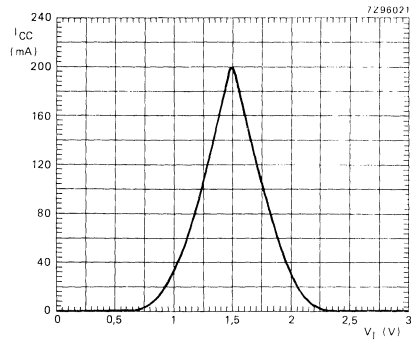
For further information, see chapter ‘Power dissipation’.

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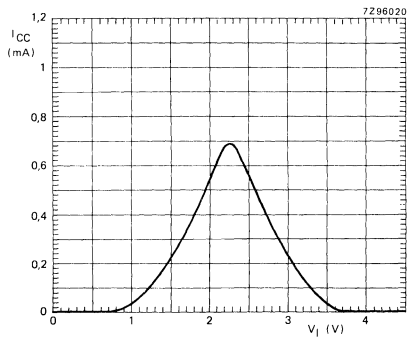
p-channel transistor	triode	triode	saturated	off
n-channel transistor	off	saturated	triode	triode



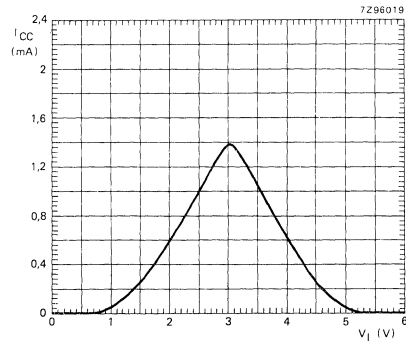
(a)  $V_{CC} = 2\text{ V}$



(b)  $V_{CC} = 3\text{ V}$



(c)  $V_{CC} = 4.5\text{ V}$



(d)  $V_{CC} = 6\text{ V}$

Fig. 12 Typical d.c. supply current as a function of input voltage for 74HC circuits; normalized curves for a unit load coefficient of 1. The  $I_{CC}$  for a specific 74HC circuit can be calculated by multiplying the values of  $I_{CC}$  shown by the unit load coefficient for the 74HCT type given in the data sheet.



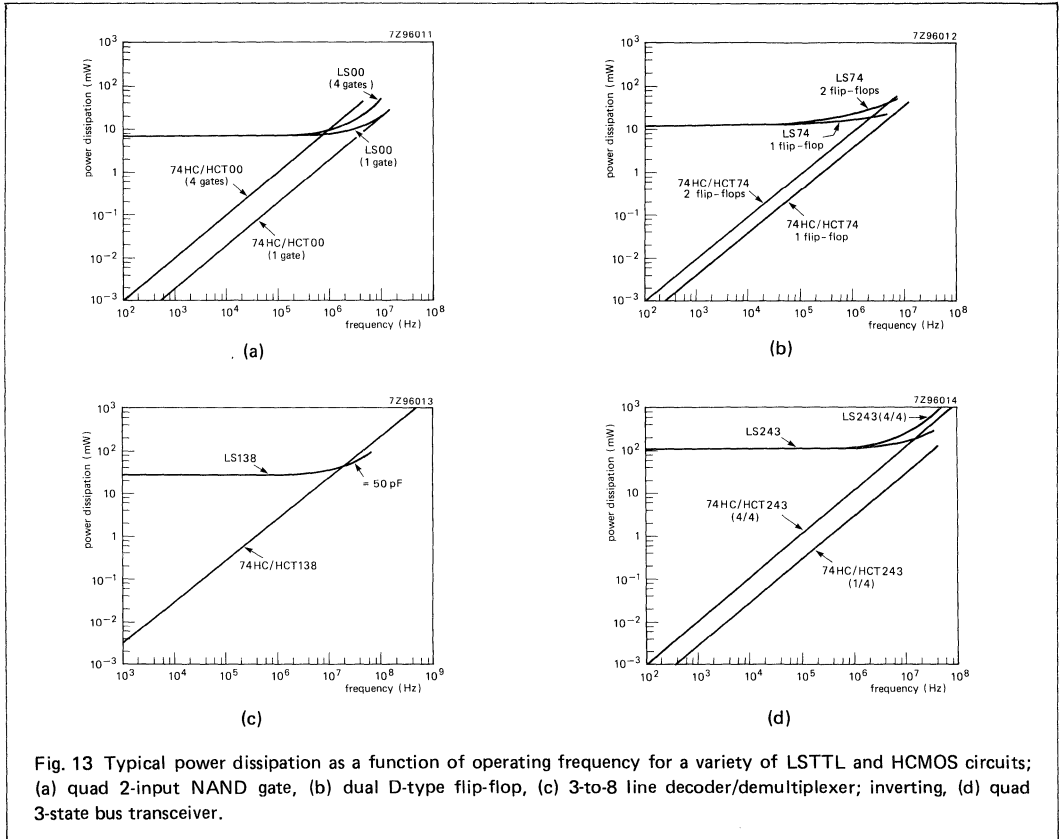


Fig. 13 Typical power dissipation as a function of operating frequency for a variety of LSTTL and HCMOS circuits; (a) quad 2-input NAND gate, (b) dual D-type flip-flop, (c) 3-to-8 line decoder/demultiplexer; inverting, (d) quad 3-state bus transceiver.

**SUPPLY VOLTAGE**

**Range**

The supply voltage range of 74HC devices is 2 V to 6 V (Fig.14). This ensures continued use of HCMOS with future generations of memory and microcomputer requiring supply voltages of less than 5 V, simplifies the regulation requirements of power supplies, facilitates battery operation and allows lithium battery back-up. When 74HC devices are used in linear applications, for example when they are used as RC oscillators, a supply of at least 3 V is recommended to ensure sufficient margin for operation in the linear region.

74HCT devices are pin-compatible with LSTTL circuits and are intended as power-saving replacements for them. The 74HCT devices will operate from the traditional 5 V LSTTL supply, but the voltage range is extended to  $\pm 10\%$  for both LSTTL temperature ranges ( $-40$  to  $+85^\circ\text{C}$  and

$-40$  to  $+125^\circ\text{C}$ ). This allows extended temperature range LSTTL devices to be replaced by 74HCT devices.

The absolute maximum supply or ground current per pin is  $\pm 50$  mA for devices with standard output drive, and  $\pm 70$  mA for devices with bus driver outputs. These currents are only drawn when the outputs of a device are heavily loaded. The average dynamic current at very high frequencies can be calculated using  $C_{PD}$ .

The maximum rated supply voltage of HCMOS devices is 7 V and any voltage above this may destroy the device, even though the on-chip parasitic diode break-down voltage is at least 20 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The  $V_{CC}$  and GND potentials must never be reversed as this can cause excessive currents to flow through the input protection diodes.

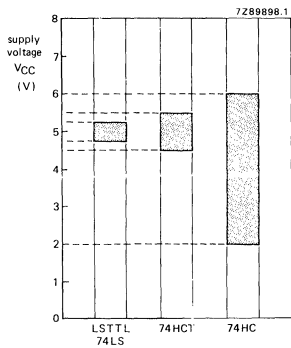


Fig. 14 Supply voltage ranges for LSTTL and HCMOS circuits. The supply voltage range for 74HCT circuits retain the LSTTL nominal supply of 5 V, but the range has been extended from  $\pm 5\%$  to  $\pm 10\%$  for both the standard and the extended temperature range. 74HC circuits operate with a supply voltage as low as 2 V.

**Battery back-up**

A battery back-up for a 74HC system is extremely simple. Figure 15 shows an example. The minimum battery voltage required is only 2 V plus one diode drop.

In the example, HIGH-to-LOW level shifters (74HC4049 or 74HC4050) prevent positive input currents into the system due to input signals greater than one diode drop above V<sub>CC</sub>. If the circuit is such that input voltages can exceed V<sub>CC</sub>, external resistors should be included to limit the input current to 15 mA for one input (7.5 mA per input for two inputs, 5 mA per input for three inputs, etc.).

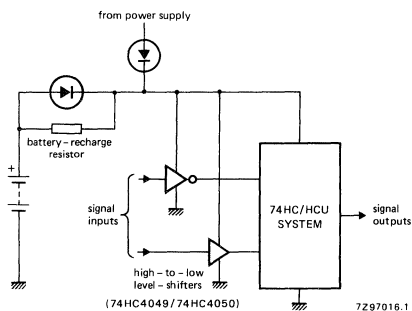


Fig. 15 An HCMOS system with battery back-up.

External resistors may also be necessary in the output circuits to limit the current to 20 mA if the output can be pulled above V<sub>CC</sub> or below GND. These current limits are set by the parasitic V<sub>CC</sub>/GND diodes present in all outputs, including three-state outputs.

For further information, see chapter 'Battery back-up.'

**Power supply regulation and decoupling**

The wide power supply range of 2 V to 6 V may suggest that voltage regulation is unnecessary. However, a changing supply voltage will affect system speed, noise immunity and power consumption. Noise immunity, and even the operation of the circuit, can be affected by spikes on the supply lines, so matched decoupling is always necessary in dynamic systems.

Both 74HC and 74HCT devices have the same power supply regulation and decoupling requirements. The best method of minimizing spikes on the supply lines is simple enough — use a good power supply, provide good ground bussing and low a.c. impedances from the V<sub>CC</sub> and GND pins of each device. The minimum decoupling capacitance depends on the voltage spikes that can be tolerated, which in general should be limited to 400 mV. A local voltage regulator on a printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50  $\mu$ F. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1  $\mu$ F tantalum capacitor for every ten packages. The V<sub>CC</sub> line of bus driver circuits and level-sensitive devices can be decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

For further information, see chapter 'Power supply decoupling'.

**INPUT/OUTPUT PROTECTION**

The gate input of a MOS transistor acts as a capacitor (<1 pF) with very low leakage current (<1 pA). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device.

The integration process of the HCMOS family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance of an HCMOS device is typically 100  $\Omega$  under all biasing conditions, even when V<sub>CC</sub> is short-circuited to GND — an improvement over direct input diode clamps during power-up.

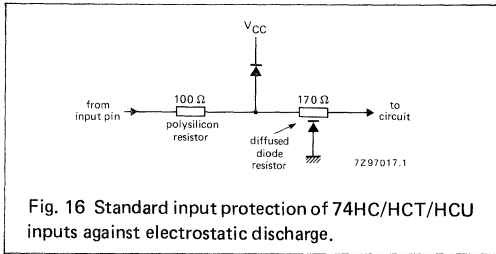


Fig. 16 Standard input protection of 74HC/HCT/HCU inputs against electrostatic discharge.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig.16). The typical forward voltage of the diodes is 0.9V at 2 mA and the reverse breakdown voltage is 20V. In some applications such as oscillators, the diodes conduct during normal operation, in which case the input current should be limited. The maximum positive input current  $+I_{IK}$  per input is 20 mA. For devices with a standard output, the total positive input current is 50 mA; for devices with a bus-driver output, the total input current is 70 mA. The maximum negative input current  $-I_{IK}$  per pin is:

- 14 mA for one input
- 9 mA for two inputs
- 6 mA for three inputs
- 5 mA for four inputs
- 4 mA for five inputs
- 3 mA for six to eight inputs.

High-to-low level shifters 74HC4049 and 74HC4050 have a single-sided input protection network (Fig.17) which protects against electrostatic input voltages. The diode D1 is the parasitic drain-to-GND diode of the thick field oxide protection device.

All input pins can withstand discharge voltages up to 2.5 kV (typ.) when tested according to MIL-STD-883B, method 3015, see Fig.18. The output configurations of standard, bus driver, three-state, open drain and I/O ports can withstand  $>3.5$  kV (typ.) because of the large diodes formed by the drain surfaces of the output transistors.

Fig.19 shows the voltage pulse for the discharge test. The rise time  $t_r$  prescribed by MIL-STD-883B is  $\leq 15$  ns, but in practice it is helpful to adjust the test set-up to give a rise time of  $13 \pm 2$  ns to avoid correlation problems.

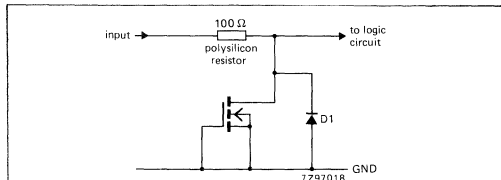
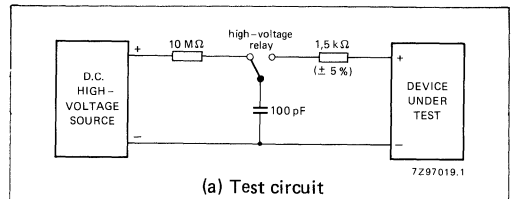


Fig. 17 Input protection of 74HC4049 and 74HC4050.

Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see chapter 'Handling precautions').



(a) Test circuit

mode	device under test	
	+	-
1	input	GND
2	GND	input
3	input	$V_{CC}$
4	$V_{CC}$	input
5	output	GND
6	GND	output
7	output	$V_{CC}$
8	$V_{CC}$	output
9	input	output
10	output	input
11	$V_{CC}$	GND
12	GND	$V_{CC}$

all other pins should be left open circuit

(b) Test modes

Fig. 18 Electrostatic discharge test.

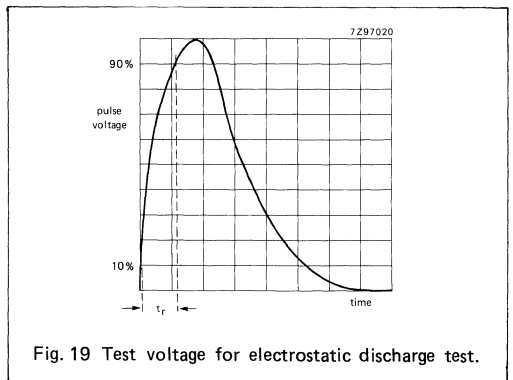


Fig. 19 Test voltage for electrostatic discharge test.

## INPUT CIRCUITS

### 74HC inputs

The 74HC input circuit (Fig.20) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages greater than  $V_{CC}$  or less than GND. The circuit is intended for a.c. working and cannot handle heavy d.c. currents for long periods; the maximum input diode current is 20 mA.

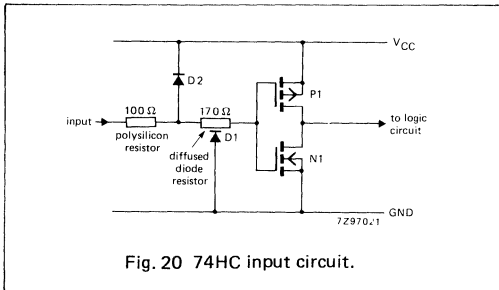


Fig. 20 74HC input circuit.

The 74HC input circuit has no active input current; the only current flowing is through the reversed-biased diodes D1 and D2, typically a few nA reaching a maximum when  $V_I = V_{CC}$  or GND.

The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving a typical switching threshold of 50%  $V_{CC}$ , see Fig.21. This threshold is almost independent of temperature, a  $\pm 60$  mV variation of the switching point from  $-40$  to  $+125$  °C being typical. The temperature dependence of  $V_{IL}$  is  $-0.6$  mV/°C, that of  $V_{IH}$  is  $+0.6$  mV/°C. The only other factors that affect the switching threshold are the spreads of  $\beta$  and  $V_T$  of P1 and N1 between devices.

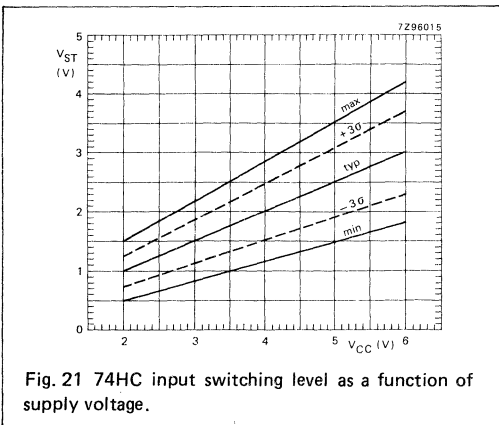


Fig. 21 74HC input switching level as a function of supply voltage.

There is no current path from  $V_{CC}$  to GND when the input is lower than  $V_{TN}$ , or higher than  $V_{CC}-V_{TP}$ . However, when the input voltage is in the linear region, a static current path from  $V_{CC}$  or GND flows in the input stage (Fig.12). This current is negligible under normal operating conditions when the input rise time  $t_r \leq 15$  ns, but the power dissipation should be taken into account for devices operating in the linear region. Owing to the voltage gain of the input stage, there is no static flow-through current in the second and subsequent stages. Small currents do flow in these stages during operation when both n-channel and p-channel transistors conduct for brief periods and their effect is included in the  $C_{pD}$  value in the data sheets.

### 74HCT inputs

The 74HCT input stage is similar to that of a 74HC device. It has the same characteristics for LSTTL levels as a 74HC input has for CMOS levels, so there is no trade-off in speed or power dissipation. The switching threshold is lower, 1.4 V at  $V_{CC} = 5$  V. In addition, the 74HCT input circuit, shown in Fig.22, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural drain voltage of the p-channel transistor (P1) is approximately  $V_{CC}-0.6$  V, but when the input voltage is LOW, an auxiliary pull-up transistor (P2) raises this to  $V_{CC}$ , cutting off p-channel transistor P3 completely. The input stage is well matched to the load presented by the second stage so that symmetrical propagation delays are obtained.

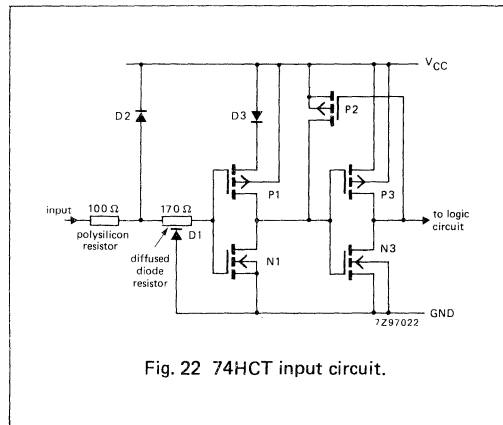


Fig. 22 74HCT input circuit.

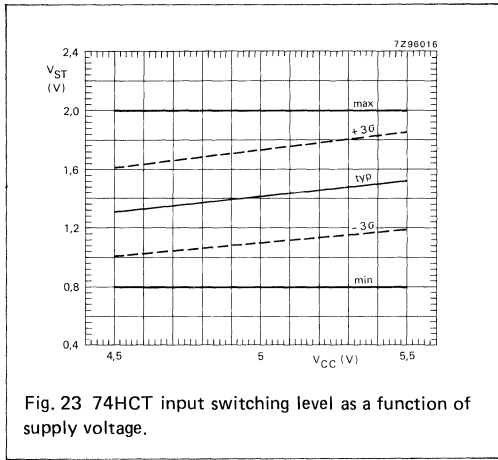


Fig. 23 74HCT input switching level as a function of supply voltage.

Figure 23 shows the switching level as a function of supply voltage.

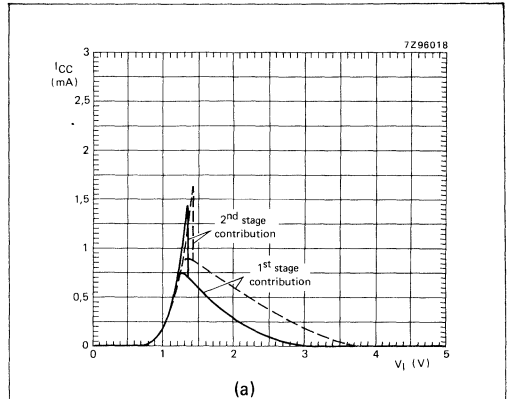
A TTL HIGH level can be as low as 2.4 V. An input of this order to a HCMOS device would not cut off P1 completely, and additional supply current would flow through the input stage. A level-shift diode D3 and the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and gives an input switching level compatible with LSTTL. Figure 24 shows the input stage through-current with and without the diode circuit. The peak in the curve occurs at the input switching threshold.

The input stage through-current is virtually zero for a typical TTL HIGH level input of 3.5 V. Thus, this unique 74HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and maximum through-currents  $\Delta I_{CC}$  per input are given in the data sheets.

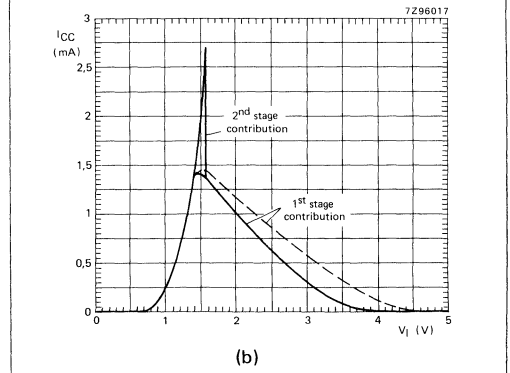
In a system where 74HCT devices are only driven by LSTTL devices,  $V_{OH\ min}$  can be 2.7 V except for some bus drivers. With  $V_{OH} = 2.7\ V$ ,  $\Delta I_{CC}$  is half the published value.

**Maximum input rise/fall times**

All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 500 ns at  $V_{CC} = 4.5\ V$ .



(a)



(b)

--- with no level-shift diode  
 — with standard input structure

Fig. 24 Additional quiescent supply current  $\Delta I_{CC}$  (typ.) per input pin of a 74HCT device as a function of supply voltage (unit load coefficient is 1); (a)  $V_{CC} = 4.5\ V$ , (b)  $V_{CC} = 5.5\ V$ .

The flip-flops 74HC/HCT73, 74, 107, 109 and 112 incorporate Schmitt-trigger input circuits and the 74HC/HCT14 and 132 are dedicated Schmitt triggers with specified input levels.

For further information, see chapter 'Schmitt trigger applications'.

### Termination of unused inputs

To prevent any possibility of linear operation of the input circuitry of an LSTTL device, it is good practice to terminate all unused LSTTL inputs to  $V_{CC}$  via a  $1.2\text{ k}\Omega$  resistor. Inputs should not be connected directly to GND or  $V_{CC}$ , and they should not be left floating.

Unlike LSTTL inputs, the impedance of 74HC and 74HCT inputs is very high and unused inputs must be terminated to prevent the input circuitry floating into the linear mode of operation which would increase the power dissipation and could cause oscillation. Unused 74HC and 74HCT inputs should be connected to  $V_{CC}$  or GND, either directly (a distinct advantage over LSTTL), or via resistors of between  $1\text{ k}\Omega$  and  $1\text{ M}\Omega$ . Since the resistors used to terminate the inputs of LSTTL devices are usually between  $220\ \Omega$  and  $1.2\text{ k}\Omega$ , it is often possible to directly replace LSTTL circuits with their 74HCT counterparts.

Some of the bidirectional (transceiver) logic devices in the HCMOS family have common I/O pins. These pins cannot be connected directly to  $V_{CC}$  or GND. Instead, when defined as inputs, they should be connected via a  $10\text{ k}\Omega$  resistor to  $V_{CC}$  or GND.

### Input current

Figure 25 shows the typical input leakage current of a HCMOS device as a function of ambient temperature for a  $V_{CC}$  of 6 V. Over the total operating temperature range, the input leakage current is well below the rating specified in the JEDEC standard ( $100\text{ nA}$  between  $-55\text{ }^\circ\text{C}$  and  $+25\text{ }^\circ\text{C}$  and  $1\ \mu\text{A}$  at  $+85\text{ }^\circ\text{C}$  and  $+125\text{ }^\circ\text{C}$ ). The reason for this difference is the high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the rating is end-of-line, allowing

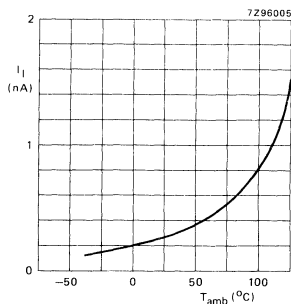


Fig. 25 Typical HCMOS input leakage current  $I_I$  as a function of ambient temperature  $T_{amb}$ .

some leakage current shift due to the ingress of moisture or foreign material.

### Input capacitance

Since CMOS inputs present essentially no load, fan-out is limited only by the input capacitance. This is specified as  $3.5\text{ pF}$  (typ.) and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Figs. 26 and 27 show the typical input capacitances for powered 74HC and 74HCT devices. The initial decrease in capacitance as  $V_I$  rises from zero or falls from  $5\text{ V}$  is due to increased reverse bias on the protection diodes. The peak is caused by internal Miller feedback capacitance when the inverter is in its linear mode. A conservative value for the maximum input capacitance is  $10\text{ pF}$  ( $20\text{ pF}$  for I/O pins owing to the output drain capacitance). Input capacitance is measured with all other inputs tied to ground.

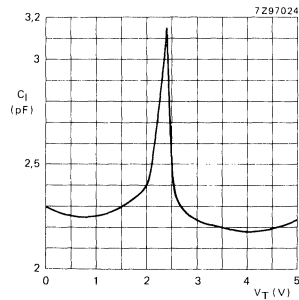


Fig. 26 Typical input capacitance  $C_I$  of a 74HC device as a function of input voltage;  $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

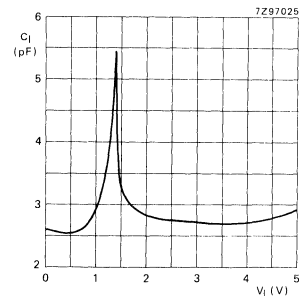


Fig. 27 Typical input capacitance  $C_I$  of a 74HCT device as a function of input voltage;  $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

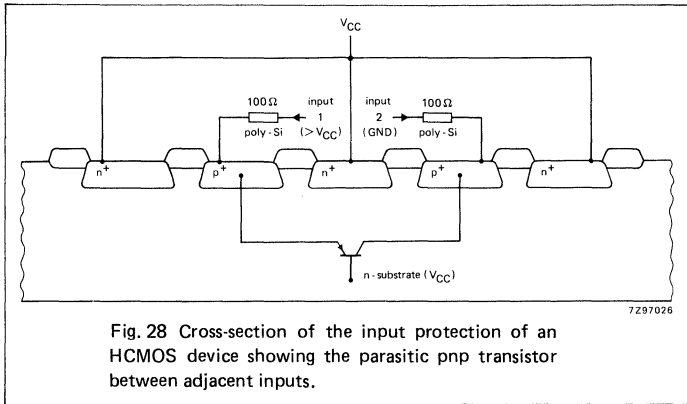


Fig. 28 Cross-section of the input protection of an HCMOS device showing the parasitic pnp transistor between adjacent inputs.

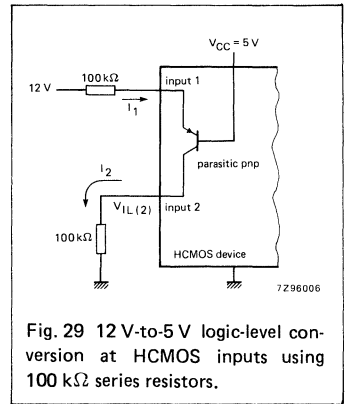


Fig. 29 12 V-to-5 V logic-level conversion at HCMOS inputs using 100 kΩ series resistors.

**Coupling of adjacent inputs**

Parasitic bipolar pnp transistors can be present between adjacent inputs, e.g. between an input protection diode to V<sub>CC</sub> and the same diode at the adjacent input, as shown in Fig.28. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current into the terminal (I<sub>1</sub>) can cause a current I<sub>2</sub> in the parasitic transistor and in the adjacent input (Fig.29). Because I<sub>2</sub> in the adjacent input has to be drained by the source driving that input, the source resistance (R) must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

The ratio of the parasitic adjacent input current (I<sub>2</sub>) to the forced input current (I<sub>1</sub>) denoted α:

$$\alpha = \frac{I_2}{I_1}$$

α has been reduced to less than 0.05 (typically 0.001) in the HCMOS family by the use of deep guard rings and optimum bonding pad spacing.

A low α permits proper logic operation in the presence of transients and also allows HIGH-to-LOW voltage translation simply by adding series input resistors. For example, in Fig.29, 12 V system logic is converted to 5 V system logic by adding a 100 kΩ resistor in each input. Since the logic signals are delayed by 1-2 μs, this arrangement is suitable for rather slow 12 V control logic such as that in automotive applications. When the input diodes are used as clamps for logic level translation, the total input current should be limited to 20 mA.

**Input voltage and forward diode input current**

As a general rule, CMOS logic devices with input clamp diodes (Fig.16) should be operated between the power

supply rails. Neglecting the input series polysilicon resistor shown in Fig.16, this means: -0.5 V ≤ V<sub>I</sub> ≤ V<sub>CC</sub> + 0.5 V.

This rule is JEDEC Std. No. 7 and is intended to prevent users damaging devices similar to HCMOS that do not have the polysilicon resistor. HCMOS devices however meet the tougher rating: -1.5 V ≤ V<sub>I</sub> ≤ V<sub>CC</sub> + 1.5 V. Furthermore, virtually all HCMOS devices can operate reliably up to the rating without logic errors.

The maximum permissible continuous current forced into an input or output of a HCMOS device is ±20 mA (JEDEC rating).

**OUTPUT CIRCUITS**

**Output drive**

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All 74HC and 74HCT outputs are buffered for consistent current drives and a.c. characteristics throughout the HCMOS family. Well-matched output n-channel and p-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of HCMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that a system will operate correctly with worst-case LOW and HIGH input signals and that noise immunity margins will be preserved. HCMOS capability is expressed as the source or sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept is not applicable.

With a specified output drive of 4 mA (at  $V_{OLmax} = 0.4 V$ ), the HCMOS capability exceeds 4000 ULs, and with a  $20\mu A$  (at  $V_{OL} = 0.1 V$ ) specification the HCMOS capability is 20 ULs. A standard HCMOS output can drive ten LSTTL loads and maintain  $V_{OL} \leq 0.4 V$  over the full temperature range. A bus driver output can drive 15 LSTTL loads under the same conditions. Table 10 shows the output drive capabilities of some HCMOS devices expressed in LSTTL unit loads. The output current may be increased for higher output voltages. For example, extrapolating the 6 mA bus driver capability at  $V_{OL} = 0.33 V$  and  $T_{amb} = 85^\circ C$  to a  $V_{OL}$  of 0.5 V gives an output drive capability of 9 mA.

Output current derating as a function of temperature is shown in Fig.30 and is valid for all types of output. Output source and sink drives at  $V_{CC} = 2 V$ , 4.5 V and 6 V are given in Figs.31 to 34 which show the output current as a function of output voltage; these graphs indicate the typical output currents and the expected minimum output currents. They can serve as a design aid when calculating transmission line effects or when charging highly capacitive loads.

The expected minimum curves are not guaranteed; they are tested only at the values given in the data sheets.

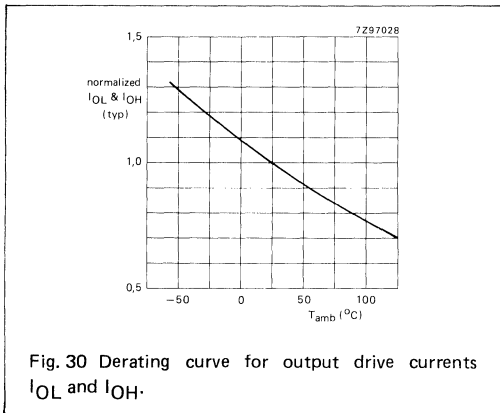


Table 10: Comparison of the output drive capabilities of LSTTL and HCMOS ( $V_{OL} \leq 0.4 V$ )

LS device	output	drive capacity	HCMOS equiv.	type	output	drive capacity
74LS00	4 mA	10 UL	74HC00	standard	4 mA	10 UL
74LS138	4 mA	10 UL	75HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

UL = unit load.

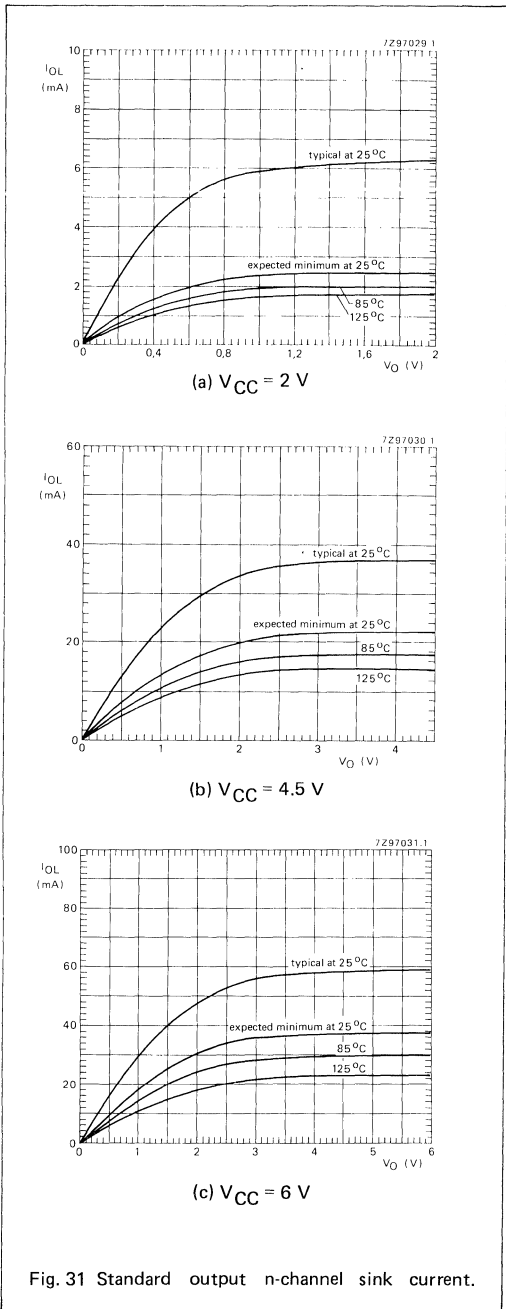
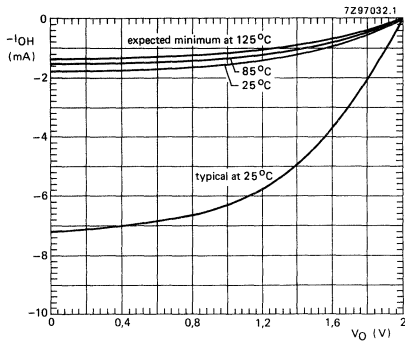
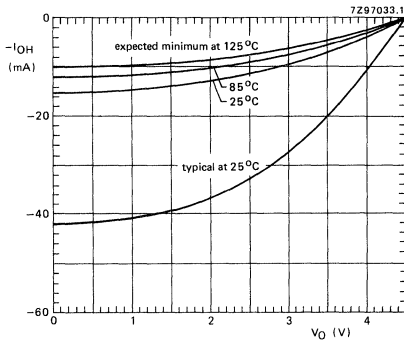


Fig. 31 Standard output n-channel sink current.

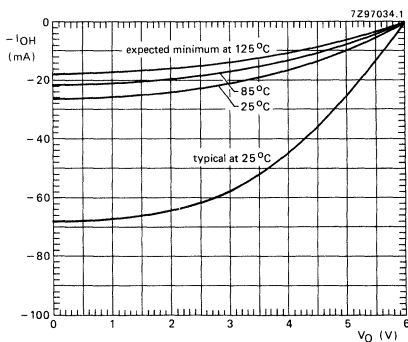




(a)  $V_{CC} = 2\text{ V}$

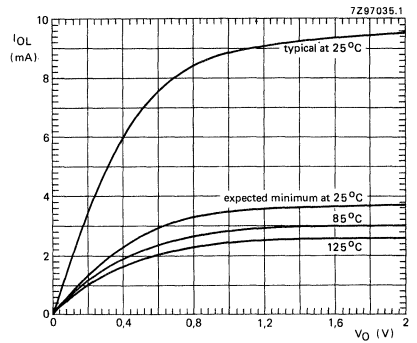


(b)  $V_{CC} = 4.5\text{ V}$

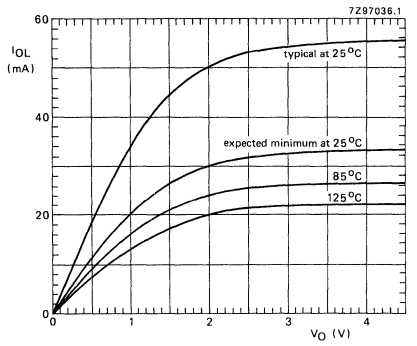


(c)  $V_{CC} = 6\text{ V}$

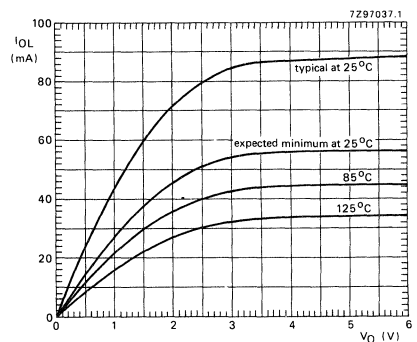
Fig. 32 Standard output p-channel source current.



(a)  $V_{CC} = 2\text{ V}$

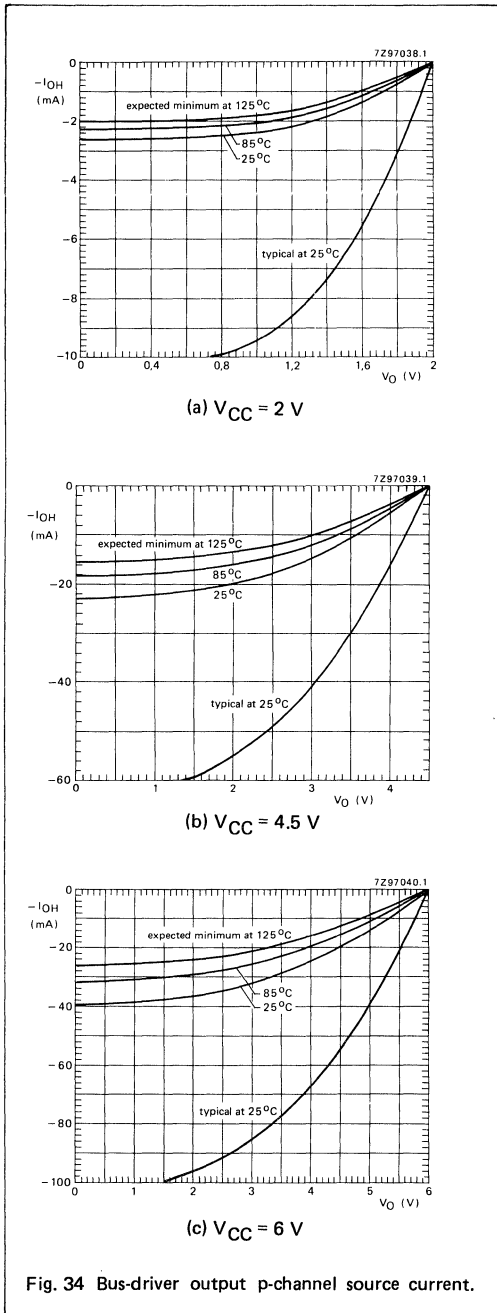


(b)  $V_{CC} = 4.5\text{ V}$



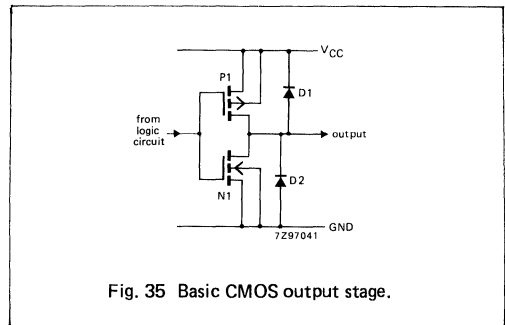
(c)  $V_{CC} = 6\text{ V}$

Fig. 33 Bus-driver output n-channel sink current.



**Push-pull outputs**

A typical push-pull output stage is shown in Fig.35. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage  $V_O$  of all HCMOS devices in the case of externally-forced voltages such that  $-0.5\text{ V} \leq V_O \leq V_{CC} + 0.5\text{ V}$ . For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA d.c., line ringing and power supply spikes in normal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminium traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry.



The maximum rated d.c. current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminium migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum d.c. current rating to be exceeded. However, for logic testing, one output may be shorted for up to five seconds without damaging the device.

**Three-state outputs**

In the typical three-state output circuit shown in Fig.36, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors. A LOW at EO puts the output in the high-impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output and its function table is shown in Fig.37.

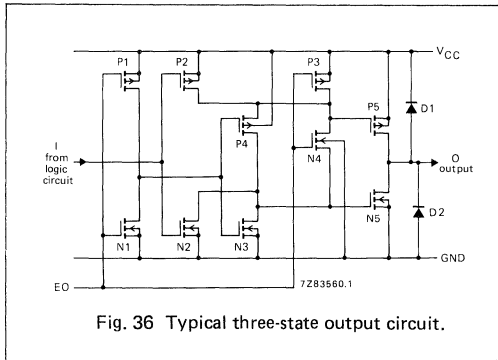


Fig. 36 Typical three-state output circuit.

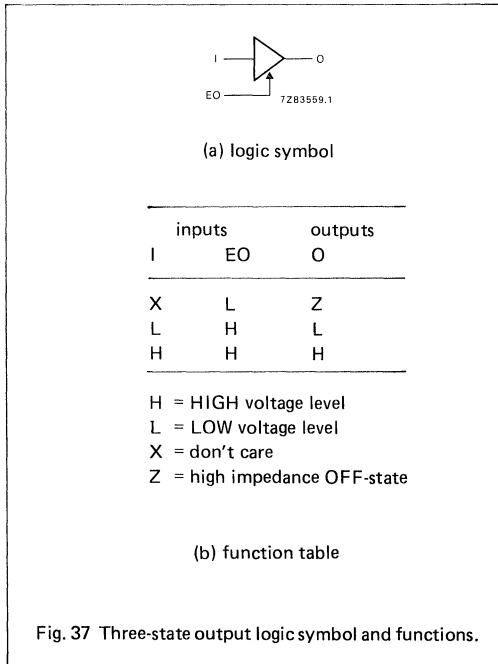


Fig. 37 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. To minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. In general, this requires that the output enable signals should not overlap. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This avoids overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

When designing with three-state outputs, note that disable propagation delays are measured for an RC load when the output voltage has changed by 10% of the voltage swing. This 10% level is adequate to ensure that a device output has turned off. Although this method provides a standard reference for measuring disable times, it implies that the output is already off for 10% of the RC time. Because all disable times are measured with a load of 1 kΩ and 50 pF, subtract the 10% RC time (5 ns) from the values published in the data sheets to obtain the real internal disable propagation delay.

Diodes D1 and D2 are parasitic diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one  $V_{BE}$  above  $V_{CC}$ , of importance in large systems where sections of the system may be powered-down ( $V_{CC} = 0 V$ ), in which case the output diode current has to be limited to 20 mA.

All I/O ports and transceivers have a three-state output as shown in Fig.36. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause  $V_{CC}$  current. If necessary, terminate the input with a 10 kΩ resistor, see 'Termination of unused inputs'.

**Open-drain outputs**

In TTL families, several functions are offered with open-collector outputs to enhance logic functions by using OR-tied logic. The advantage of OR-tied logic is the logic elements saved and hence the lower power dissipation. However, this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not encountered in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, the 74HC/HCT03 (quad 2-input NAND gate) has an open-drain n-channel output, see Fig.38. The parasitic diode D1 is not present (there being no p-channel transistor); this allows the output voltage to be pulled above  $V_{CC}$  to  $V_{Omax}$  making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open-drain output is protected against electrostatic discharge.

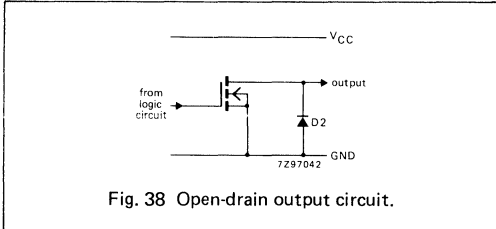


Fig. 38 Open-drain output circuit.

**Increased drive capability of gates**

To increase output drive, the inputs and outputs of gates in the same package may be connected in parallel. It is advisable to restrict parallel connection to gates within one package to avoid large transient supply currents due to different gate-switching times.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

**Output capacitance**

For push-pull outputs, no output capacitance is specified because either the n-channel transistor or the p-channel transistor creates a low-impedance path to the supply rails.

Three-state outputs can be switched to the high impedance OFF-state, and because many of them can be connected to a bus line, the output capacitance is needed to calculate the total capacitive load. For bus-driven 3-state outputs in a DIL package, the output capacitance is 6 pF (typ.) and 20 pF (max.).

**STATIC NOISE IMMUNITY**

The static noise immunity can be divided into:

- the static noise margin LOW. This is the voltage difference between  $V_{ILmax}$  of the driven device and  $V_{OLmax}$  of the driver.
- the static noise margin HIGH. This is the difference between  $V_{OHmin}$  of the driver and  $V_{IHmin}$  of the driven device.

For 74HC devices, both the LOW level noise margin and the HIGH-level noise margin is 28% of  $V_{CC}$ . This is a considerable improvement over LSTTL where the LOW-level noise margin is only 8% of  $V_{CC}$  and the HIGH level noise margin is just 14% of  $V_{CC}$ . The margins are even greater for HCMOS at higher supply voltages as shown in Fig.39. As 74HCT devices have the same switching levels as LSTTL, their noise margins are also the same.

The superior noise immunity of the 74HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs.40 and 41.

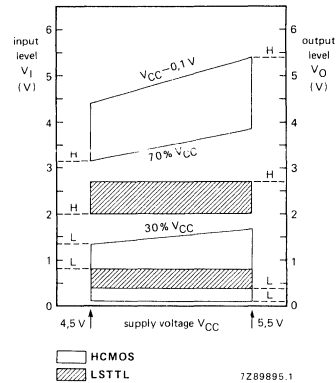


Fig. 39 Worst-case input and output voltages over an operating supply range of 4.5 V to 5.5 V.

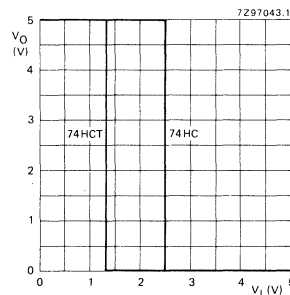


Fig. 40 Typical input-to-output transfer characteristic for 74HC and 74HCT devices.

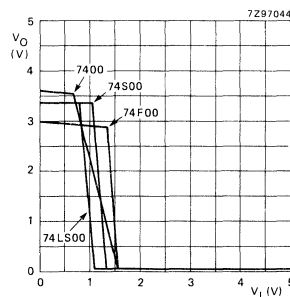


Fig. 41 Input-to-output transfer characteristics for TTL devices.

Table 11 shows the input noise margin of HCMOS devices where like devices are interfaced. Output voltages are also given.

**Table 11:** Noise immunity and noise margin for HCMOS devices ( $V_{CC} = 4.5\text{ V}$ )

		74HC	74HCT	74HCU
$V_{ILmax}$	(V)	1.35	0.8	0.9
$V_{IHmin}$	(V)	3.15	2	3.6
$V_{OLmax}$	(V)	0.1	0.1	0.5
$V_{OHmin}$	(V)	4.4	4.4	4
Noise margin low				
$V_{NML}$	(V)	1.25	0.7	0.4
Noise margin high				
$V_{NMH}$	(V)	1.25	2.4	0.4

Table 12 shows the input noise margin of 74HCT devices interfacing with LSTTL devices; the 74HCT or LSTTL output is fully-loaded,  $V_{CC} = 4.5\text{ V}$  and  $T_{amb}$  is  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  (the only convenient temperature range when using LSTTL characteristics).

**Table 12:** Noise immunity and noise margin for 74HCT and LSTTL device interfacing

		74HCT	LSTTL
$V_{ILmax}$	(V)	0.8	0.8
$V_{IHmin}$	(V)	2	2
$V_{OLmax}$	(V)	0.33 (note 1) 0.1 (note 2)	0.4
$V_{OHmin}$	(V)	3.84 (note 1) 4.4 (note 2)	2.7
Noise margins (V):			
from 74HCT to LS	$V_{NML}$		0.47
	$V_{NMH}$		1.84
from LS to 74HCT	$V_{NML}$		0.4
	$V_{NMH}$		0.7
from LS to LS	$V_{NML}$		0.4
	$V_{NMH}$		0.7
from 74HCT to 74HCT	$V_{NML}$		0.7
	$V_{NMH}$		2.4

**Notes**

1. 4 mA load (i.e. 10 LSTTL inputs).
2. 20  $\mu\text{A}$  load (i.e. 20 74HCT inputs).

Whenever a 74HCT output drives either an LSTTL or a 74HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or 74HCT input. This improvement is larger for  $V_{NMH}$  owing to the superior output sourcing current of the rail-to-rail HCMOS output swing compared with the limited totem-pole pull-up output voltage of LSTTL.

**DYNAMIC NOISE IMMUNITY**

As for static noise immunity, dynamic noise immunity can be divided into two parts:

- a dynamic noise margin LOW
- a dynamic noise margin HIGH.

For 74HC devices, both margins are similar; for 74HCT devices, the dynamic noise margin LOW is the smaller of the two. To plot it, a pulse of known magnitude,  $V_p$ , is applied to the input of a device and its width,  $t_W$ , is increased until the device just begins to switch. The input level on which  $V_p$  is based is equal to the switching voltage minus the worst-case static noise margin LOW. The pulse width is measured at half pulse height,  $V_p/2$ . The rise and fall times,  $t_r$  and  $t_f$  are 0.6 ns.

$V_p$  is then reduced in increments and  $t_W$  for each new value is ascertained.

The test is repeated for different supply voltages – for 74HC devices between 2 V and 6 V, and at 5 V for 74HCT devices. A range of output currents,  $I_O$ , are also used. Increasing the d.c. load reduces the dynamic noise immunity.

Figure 42 shows the amplitude of positive-going pulses that can be withstood in the LOW state for 74HC and 74HCT devices. The curves are worst-case ones with fully-loaded drivers, so a system using only 74HC or 74HCT devices will have 0.23 V more noise margin for all  $t_W$ .

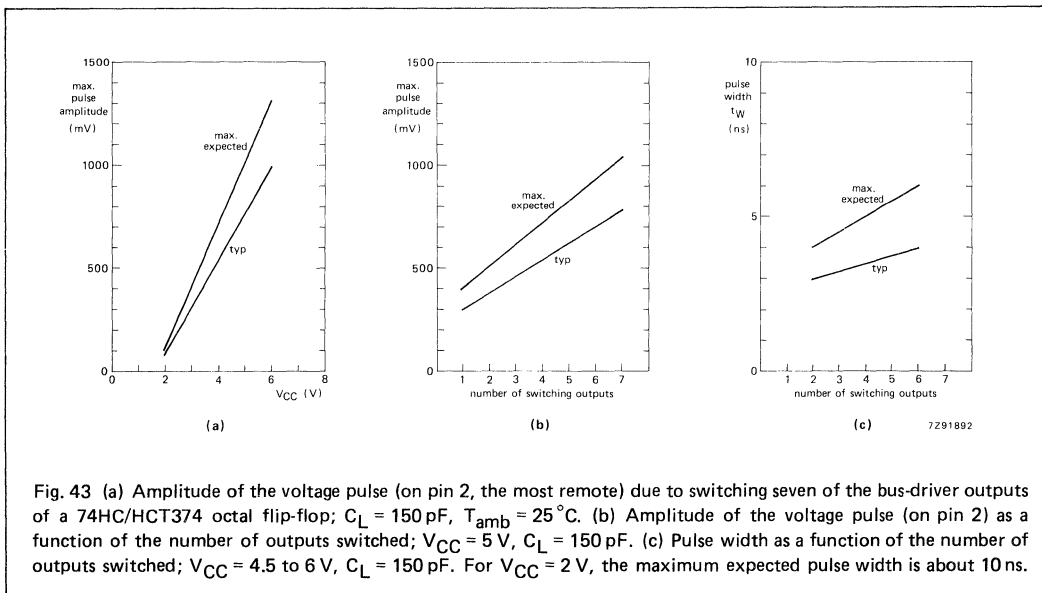
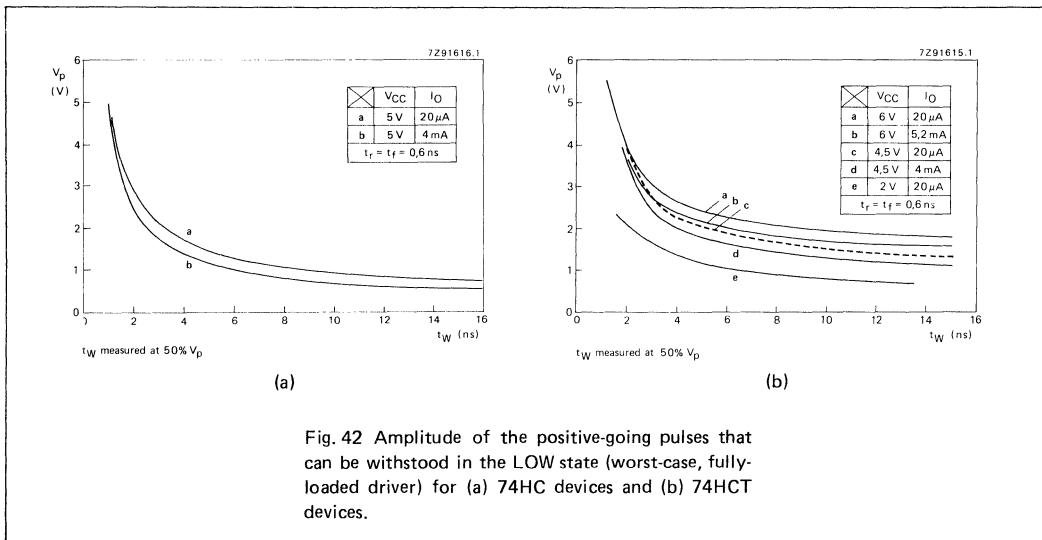
For typical input switching thresholds of 1.4 V and 2.25 V for 74HCT ( $V_{CC} = 5\text{ V}$ ) and 74HC ( $V_{CC} = 4.5\text{ V}$ ) respectively, the noise margins will be 0.83 V [(1.4 – 0.8) + 0.23 V] larger for 74HCT and 1.13 V [(2.25 – 1.35) + 0.23 V] larger for 74HC devices.

The main causes of unwanted input pulses are spikes due to outputs switching, which dumps large currents on the GND lines, or reflections when long lines (longer than about 32 cm) are driven. For more information on the latter, see chapter 'Replacing LSTTL and driving transmission lines'.

The best example of an unwanted pulse generator is an octal device with bus outputs of which seven are switching simultaneously and the eighth, most remote, output is LOW. Figure 43(a) shows the maximum pulse voltage measured on the unswitched output of a 74HC/HCT374 as a function of  $V_{CC}$ . Figures 43(b) and 43(c) show this maximum volt-

age and the pulse width as functions of the number of outputs that are switching. It should be emphasised that any pulses produced by switching outputs won't cause other devices to respond even in worst-case conditions. This is because Fig.42 is based on a worst-case  $V_{OL}$  and the

maximum expected pulse height of Fig.43 occurs for a best-case  $V_{OL}$ . So, even when a pulse of the maximum expected height shown in Fig.43 occurs, there is still a noise margin. This can be verified by plotting the pulse heights of Fig.43 on the curves of Figs.42(a) and 42(b).



## BUFFERED DEVICES

### Definition

Often the terms 'buffer devices', 'buffered inputs' or 'buffered outputs' are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switching levels and output impedances were not constant, so neither were output rise/fall times or propagation delay times. The Jedec JC40.2 committee define a buffered device to be at least two active stages with the output independent of the input logic voltage level and independent of the number of inputs that are HIGH or LOW.

A buffer meeting this definition is the AND-function circuit of Fig.44. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

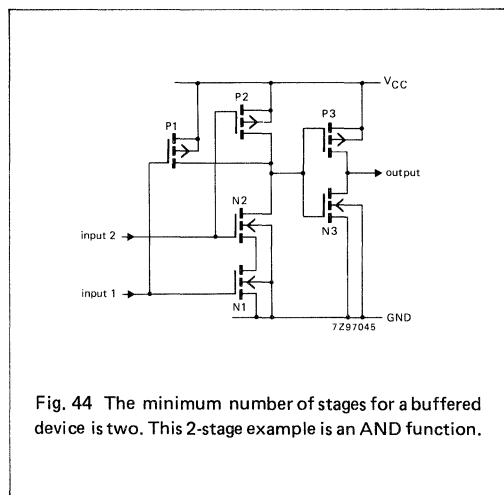


Fig. 44 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

All 74HC and 74HCT devices comprise at least two stages to minimize any pattern sensitivity of propagation delay time. Buffering also improves static noise immunity due to increased voltage gain, giving almost ideal transfer characteristics.

The designation 74HCU is used to denote single-stage devices. These have the same specification as 74HC devices but their input and output voltage parameters are relaxed. 74HCU devices don't have the high gain of 74HC/HCT versions, which makes them more suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

### Output buffering

All 74HC and 74HCT devices have buffered outputs for optimum performance. To demonstrate the benefits of output buffering, consider what would happen without it. In the single-stage device shown in Fig.45, the output impedance depends on the d.c. input voltage. Consequently, the noise margins at the output become a function of the input voltage, even when  $V_I$  is a legal HIGH or LOW level.

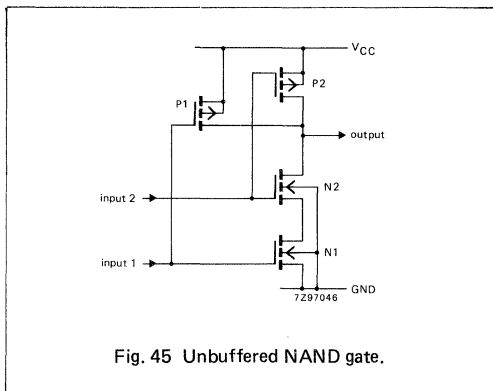


Fig. 45 Unbuffered NAND gate.

The steady-state impedance of the circuit of Fig.45 is also affected by the state of the inputs. Given that P1 and P2 have identical performances (same size), there are two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. Therefore, without output buffering, the state of output conduction depends on the number of inputs that are HIGH or LOW.

### Input buffering

An input is considered to be buffered when its switching threshold is unaffected by the logic states of other inputs. In the example of Fig.45 that has unbuffered inputs, the switching threshold of input 1 varies with a HIGH level at input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching threshold of the device. The result can be seen in Fig.46 where curve 1+2 occurs when the two inputs are tied together, and curve 1 or 2 is the switching threshold when the accompanying input is at  $V_{CC}$ .

For true input buffering, an input must have an inverter stage with sufficient gain to ensure that logic levels give independent on-chip levels. Some gates in the 74HC series (usually AND or OR gates) have unbuffered inputs, however all devices meet the family logic level requirements. All 74HCT devices have buffered inputs.

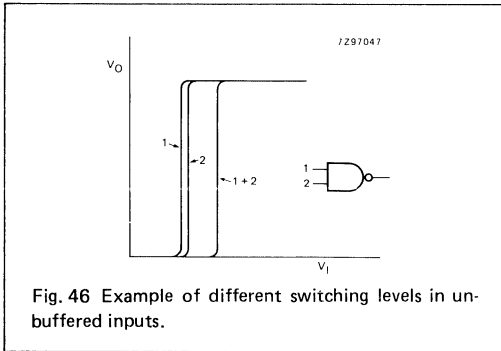


Fig. 46 Example of different switching levels in unbuffered inputs.

**PERFORMANCE OF OSCILLATORS**

When HCMOS devices are used in RC, crystal or Schmitt trigger oscillators or in analog amplifiers:

- a supply voltage of at least 3V is required. Below this value, the transconductance of crystal oscillators is too low to start oscillations. In analog circuits, insufficient output current is available to drive external components;
- slow input rise and fall times cause the input stage of a HCMOS device to draw current. This additional quiescent supply current  $\Delta I_{CC}$  is given in the data sheets for 74HCT devices since these can be used as LSTTL replacements and may be driving a significant load. The total  $I_{CC}$  for 74HC devices can be calculated by multiplying the value of  $I_{CC}$  read from Fig.12 by the unit load coefficient given in the data sheet for the 74HCT device;
- in general, frequency stability won't be affected by supply voltage, so long as the permissible output currents of the devices are not exceeded.

For further information, see chapters 'Crystal oscillators' and 'Astable multivibrators'.

**LATCH-UP FREE**

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply overvoltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating ( $\pm 20$  mA), and that  $V_{CC}$  should also be not more than twice  $V_{CCmax}$  (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC.

In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1  $\mu$ s pulses of 300 mA with a duty factor of 0.001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1  $\mu$ s pulses of 400 mA with a duty factor of 0.001. However, because there is an internal polysilicon 100  $\Omega$  resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ( $V_I = V_{CC} + 0.7 V + 100 I_I$ ) that it is unlikely that they could occur in practice, even in a 6V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires breakdown. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

For further information, see chapter 'Standardizing latch-up immunity tests'.

**DROP-IN REPLACEMENTS FOR LSTTL**

74HCT devices are power-saving, drop-in replacements for LSTTL devices. Because most systems are operated at frequencies far below the maximum possible, 74HCT devices can also be used to good effect in systems using ALS, AS, S, and FAST devices.

Fan-out should be considered when replacing a TTL device by a 74HCT device. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). Table 13 shows the fan-out of 74HCT to the different TTL families.

The fan-outs given in Table 13 are derived at a voltage drop of max. 0.4 V ( $V_{OL}$ ). In the "74" TTL series, an extended  $V_{OL}$  figure is often seen, e.g. 8 mA at 0.5 V voltage drop for LSTTL. If this figure is used to determine the fan-out of the TTL device it can result in a higher fan-out than is possible with 74HCT. This can be resolved by replacing as many of the driven TTL parts as possible by 74HCT devices to reduce the sink current requirement (the 74HCT input current is negligible). In addition, power dissipation is reduced significantly by using 74HCT.

Table 13: Fan-out of 74HCT to TTL circuits

74HCT	TTL	LS	ALS	FAST	S & AS
standard output	2	10	20	6	2
bus-driver output	3	15	30	10	3



**BUS SYSTEMS**

CMOS is being used to an increasing extent in micro-processor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

For optimum results, use only 74HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig.47(b)) which, unlike the conventional TTL bus termination, draws no heavy d.c. current and is more suited to HCMOS outputs.

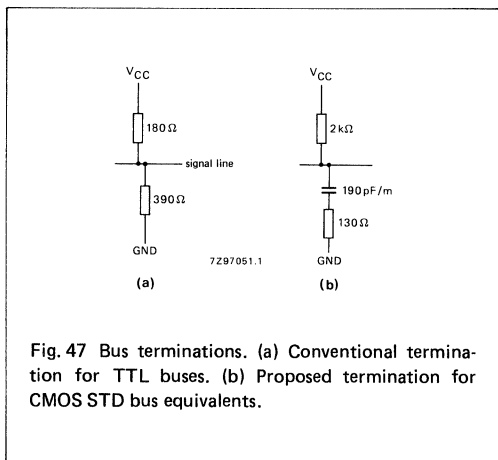


Fig. 47 Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a 10 kΩ series resistor in the HCMOS logic line. This will limit current to ±20 mA for external voltages of up to ±200 V, however, for correct functioning, the d.c. input current should be kept below those values stated in 'Input/output protection'. The recommended board edge input protection is shown in Fig.48.

In the circuit of Fig.48, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. 74HC4049 or 74HC4050).

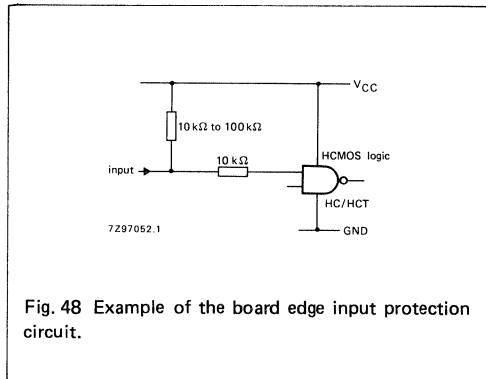


Fig. 48 Example of the board edge input protection circuit.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Since HCMOS bus-drivers do not have built-in hysteresis, slowly-rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series 74HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers 74HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section 'Propagation delays and transition times' of this User Guide.

**PACKAGE PIN CAPACITANCE**

In purely digital circuits, the input capacitance or three-state output capacitance is sufficient to determine the dynamic characteristics. However, when a HCMOS device is used in the linear region, it is necessary to take pin capacitance into account, e.g. to prevent crosstalk in analog switches or peaks in the frequency response of PLLs.

The use of SO packages with their low pin capacitances is recommended for HCMOS analog designs. Table 14 gives the pin-to-pin capacitances for the plastic DIL and SO packages used for HCMOS. Measurements were made using a dummy package with all unused pins connected to ground.

**Table 14:** Typical pin capacitances (pF) of SO and DIL packages

	SO-14 & SO-16	DIL-16	SO-20	DIL-20	SO-24	DIL-24
capacitance to ground of:						
corner pins	0.41	0.97				
all other pins	0.21	0.37				
any end two pins			0.65	1.12		
all other pins			0.25	0.40		
any end three pins					0.65	1.64
all other pins					0.33	0.65
capacitance between adjacent pins:						
including a corner pin	0.15	0.40				
all other pins	0.04	0.13				
any end three pins			0.28	0.49		
all other pins			0.14	0.22		
any end three pins					0.30	0.70
all other pins					0.12	0.28



## QUALITY INFORMATION

*page*

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## QUALITY – HCMOS LOGIC ICs

### QUALITY ASSURANCE

Our Quality Department is fully involved in all stages of the production cycle of our HCMOS family of logic ICs:

- design and development
- wafer fabrication
- assembly
- inspection and testing
- batch release
- customer liaison.

This results in continuous feedback of data which enables us to refine production conditions, test methods and designs to yield optimum quality in the final application.

#### Design and development

Layout rules and design parameters for our HCMOS family of ICs are specified in our Design Manual which reflects more than ten years' experience in CMOS silicon-gate production.

During the CAD generation of new circuit designs, layouts are automatically checked against the rules laid down in the Design Manual. Each layout is further checked by the Quality Department against not only the Design Manual requirements, but also the capabilities of the assembly process and product specifications.

#### Wafer fabrication

To realize the full performance potential of our HCMOS technology we have developed a new organizational structure for the wafer fabrication process. Production flow is now divided between technology-oriented Control Groups that are responsible for

- process control
- equipment engineering
- calibration
- contamination control
- training.

Activities of these Groups are coordinated by Process Engineering and supported by extensive data-processing facilities.

Figure 1 shows the flow of wafers through the various fabrications stages and the associated process controls. Overall wafer fabrication activity, Fig.2, is monitored by frequent audits by the Quality Department.

#### Assembly

Quality control is fully integrated with the assembly process, as shown in Fig.3.

Dice are assembled into packages on highly automated assembly lines. Fully automatic die attach and wire bonding ensure a high and consistent assembly quality. Tube to tube handling after moulding ensures excellent mechanical and visual quality.

#### Quality improvement programme

To develop quality awareness in all areas of our Integrated Circuit Group, we have instituted a 14-step Quality Improvement Programme. This programme, with its regular Quality College courses, is designed to improve all aspects of our IC-business by:

- Monitoring the quality of
  - R&D
  - wafer fabrication
  - assembly
  - marketing and sales
  - support services
  - stores and shipping.
- Extending responsibility for error-cause removal to everyone in the operation.
- Making everyone aware of performance indicators.
- Improving response to customers' problems and improving resultant cause tracing.
- Continuous analysis of product performance to enable continual specification improvement.
- Regular quality audits and analysis.

We are totally committed to quality improvement and invite our customers to share in achieving it.

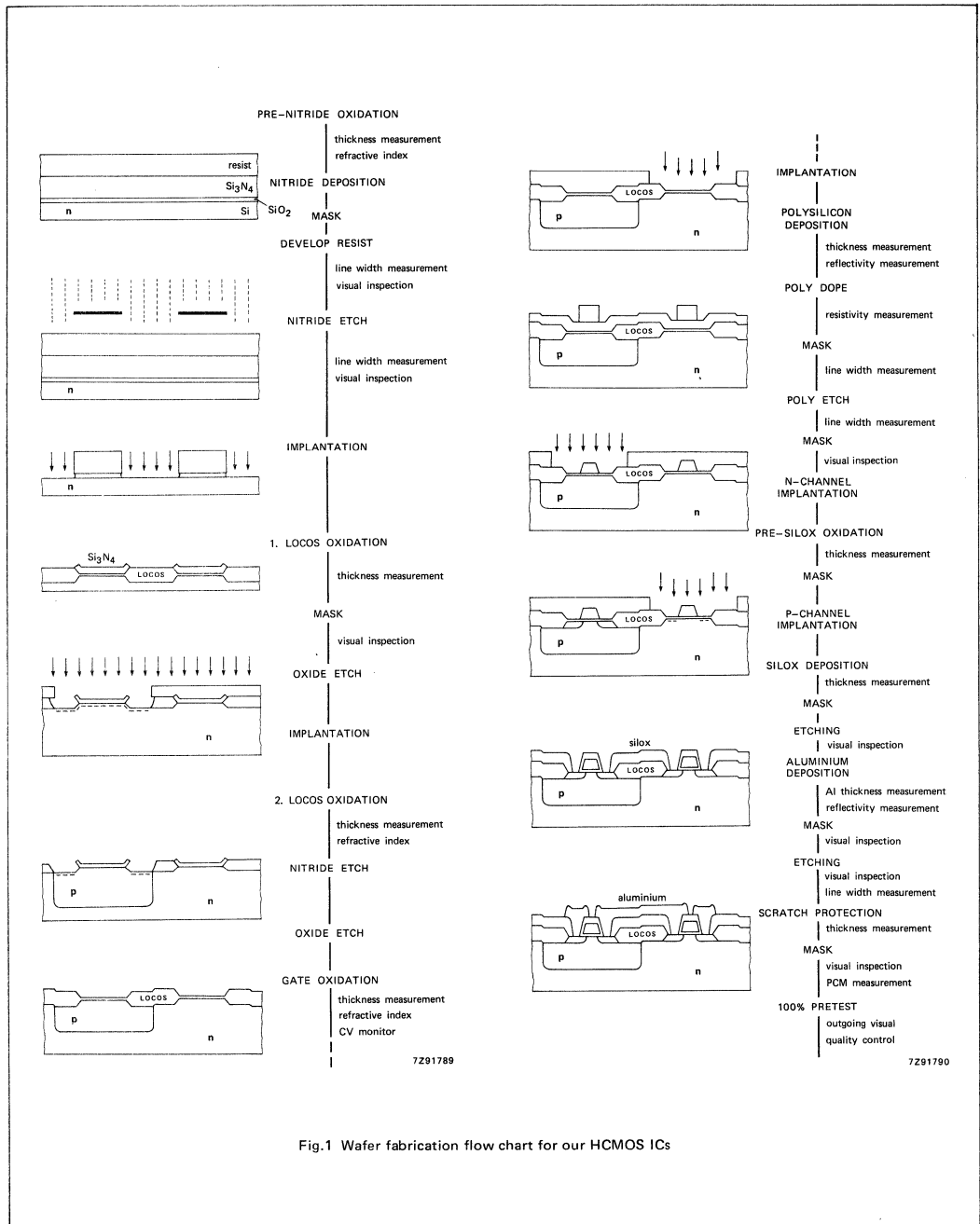


Fig.1 Wafer fabrication flow chart for our HCMOS ICs

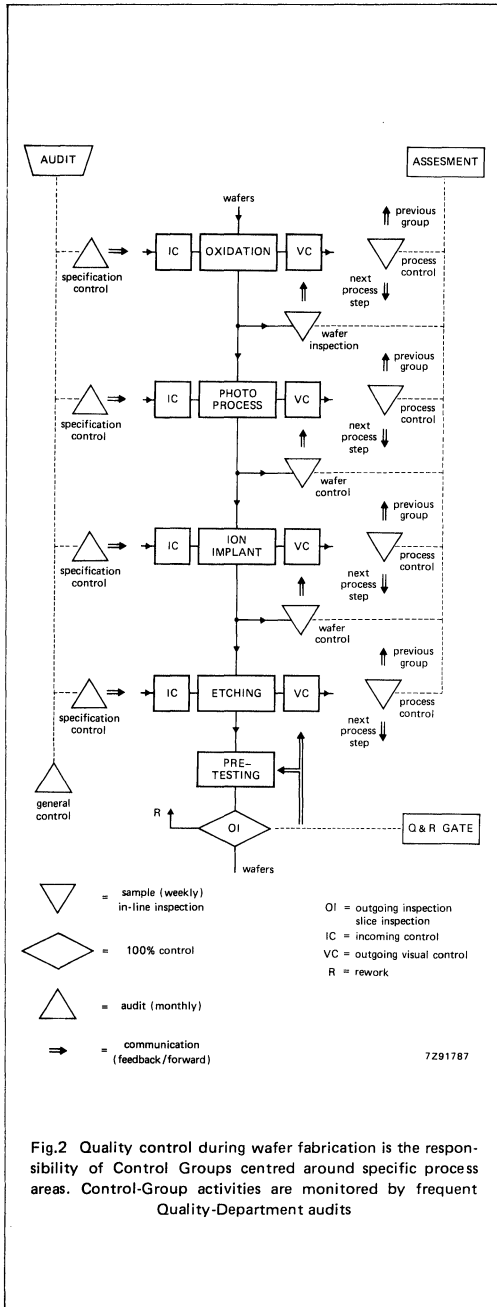


Fig.2 Quality control during wafer fabrication is the responsibility of Control Groups centred around specific process areas. Control-Group activities are monitored by frequent Quality-Department audits

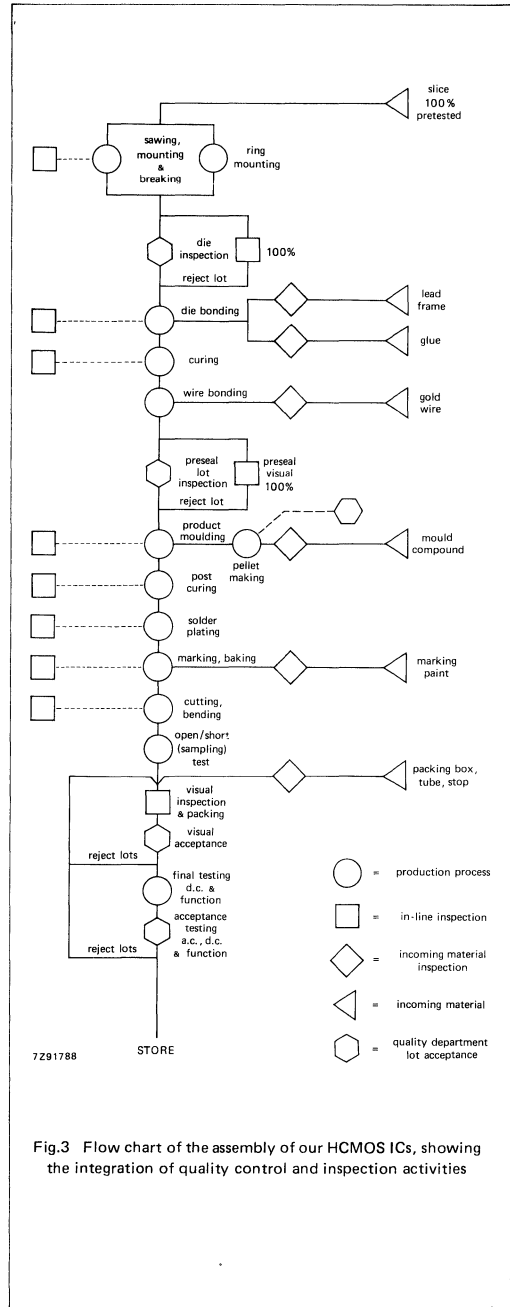


Fig.3 Flow chart of the assembly of our HCMOS ICs, showing the integration of quality control and inspection activities



### NEW PRODUCT RELEASE

The Quality Department is involved not only in the design and development phases of new products, but also in the qualification and approval of new diffusion processes, packages and assembly methods. Improvements or changes in either product or process must be fully specified, qualified and approved before entering production. As an example, Table 1 lists the qualification tests for a new wafer fabrication process.

test	conditions	duration
electrical endurance	150 °C, 6 V	2000 h
electrical endurance	175 °C, 6 V	2000 h
THB	85 °C, 85% RH, 6 V	2000 h
autoclave	132 °C, 85% RH, 6 V	150 h
temperature cycling	-65 °C to 150 °C	1000 cycl.
storage — low temperature	-65 °C	1000 h
storage — high temperature	+150 °C	1000 h
electrostatic discharge	1,5 kΩ, 100 pF, >2 kV	—

### ACCEPTANCE AND PERIODIC TESTING

Following the 100% final electrical test, each lot of our HCMOS ICs is sampled by the Quality Department for Acceptance testing. In Group A, a full inspection over the rated temperature range is performed on each device to the following AQLs:

	AQL (combined (%))	inspection level
functional + electrical parameters	0,1	II
visual + mechanical	0,1	II

Electrical parameters include all those quoted in the device Data Sheet; visual and mechanical inspection includes marking legibility, straightness of pins, plating and appearance.

A further sample is drawn weekly from each structurally-similar group of ICs and subjected to Group B testing:

- dimensions
- solderability
- temperature cycling (10 cycles)
- electrical endurance (168 h at 125 °C).

To explore quality in further depth, each structurally-similar group is further sampled quarterly and subjected to Group C Tests (see Table 8). Some THB tests and endurance tests of longer than 1000 h are also performed to examine long-term effects.

Every reject, found by us or returned by a customer, is subjected to in-depth failure analysis using the most comprehensive and up-to-date equipment. The results obtained provide valuable data that is used for continual product improvement.

### ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The improved CMOS technology used for our HCMOS family allows polysilicon resistors to be used at all inputs to slow down fast input transients due to electrostatic discharges and dissipate some of their energy. Despite the improved protection provided by these resistors, and the use of two stages of diode clamping, Fig.4, the usual CMOS handling precautions should still be observed. (See the section Handling Precautions.)

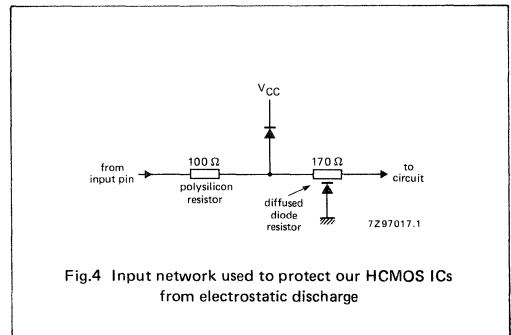
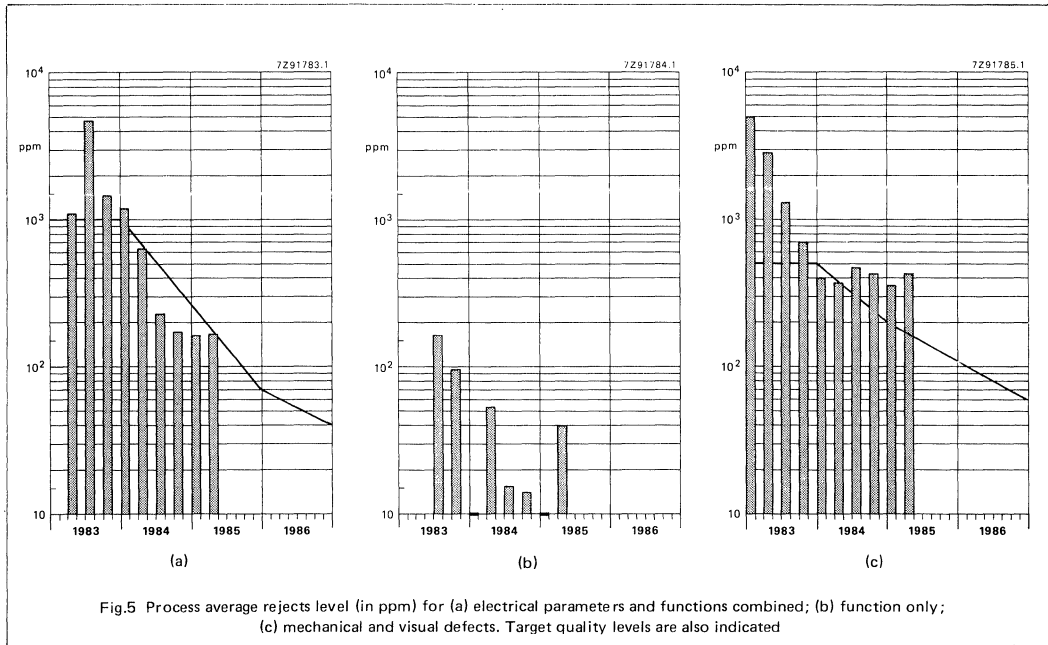


Fig.4 Input network used to protect our HCMOS ICs from electrostatic discharge

ESD resistance of our HCMOS is measured for both positive and negative discharge from a 100 pF capacitor through a 1,5 kΩ resistor. Pulse rise time is 13±2 ns. Results obtained from Acceptance testing are given in Table 2.

	polarity	1% fail	50% fail
inputs	positive	2050 V	2700 V
	negative	2300 V	>3000 V
outputs		>3000 V	>3000 V
supply		>3000 V	>3000 V



## OUTGOING QUALITY

The results from Quality Department Acceptance testing provide a good indication of the outgoing quality of our HCMOS ICs. Figure 5 shows, in terms of 'electrical parameters and functions' and 'mechanical and visual', the reject levels recorded in ppm (parts per million) for 1983, 1984 and the first half of 1985, together with the projected levels for 1985 and 1986.

## ENDURANCE AND ENVIRONMENTAL TEST RESULTS

### Temperature-humidity-bias

THB testing measures the moisture resistance of plastic DIL and SO packages. It is performed at 85°C and 85% relative humidity with  $V_{CC} = 6V$ . Electrical measurements (against the Device Specification) are made after 168 h, 500 h, 1000 h and every 1000 h thereafter. Functional failures are subjected to failure analysis.

Results from tests done from 1983 to September 1985, Table 3, show the excellent moisture resistance of our packages, even after extended test durations.

Results of THB testing confirm that there is no significant difference between the results of tests on ICs in DIL and SO packages.

TABLE 3  
Temperature-humidity-bias (85°C/85% RH/6 V)

#### DIL package

test time (h)	sample N	failures (cum)		cumulative % failure
		param.	function	
1000	1685	3	3	0,36
2000	1018	3	6	0,88
3000	420	5	8	3,10
4000	360	6	5	3,06
6000	120	3	3	5,00

#### SO package

test time (h)	sample N	failure (cum)		cumulative % failure
		param.	function	
1000	350	0	0	0
2000	100	0	0	0
3000	40	0	0	0

#### Failure analysis of rejects:

Parameter:  $I_{CC}$  leakage.

Function: mostly corrosion, some  $I_{CC}$  leakage.

**Autoclave with bias**

This is essentially an accelerated THB test with an acceleration factor of 30. This means that 120 hours' autoclave is comparable with 3600 hours' THB. We have extended the conventional autoclave test to include 6 V bias at a temperature of 132 °C in unsaturated steam at a relative humidity of 85% and a pressure of 250 kPa (2,5 atmospheres). The results given in Table 4 attest to the excellence of the silicon-nitride/polysilicon-gate protection layer and the workmanship of the package.

**TABLE 4**  
**Autoclave with bias (132 °C/85% RH/6 V)**

**DIL package**

test time (h)	sample N	failures (cum)		cumulative % failure
		param.	function	
120	700	6	3	1,29
180	530	1	6	1,32
240	530	5	13	3,40
300	530	3	23	4,91
360	480	3	31	7,08

**SO package**

test time (h)	sample N	failures (cum)		cumulative % failure
		param.	function	
120	355	5	3	2,25
180	210	0	3	1,43
240	150	0	2	1,33
300	150	0	2	1,33
360	60	0	0	0

**Failure analysis of rejects:**

Parameter: I<sub>CC</sub> leakage.

Function: mostly corrosion, some I<sub>CC</sub> leakage.

**Accelerated life testing**

To obtain data for failure rate predictions quickly, some life tests are done at raised temperatures. ICs are powered by their maximum supply voltage; ambient temperatures are up to 150 °C for ICs in plastic packages, and 225 °C for ICs in special/ceramic evaluation packages. ICs are tested for function and electrical parameters before the test starts, and then after 48 h, 168 h, 1000 h, and then every 1000 h. Every failure found is analysed. The results from such testing of many types of 74HC and 74HCT ICs in plastic DIL and SO packages are summarized in Tables 5 and 6. No significant difference between the results obtained from different

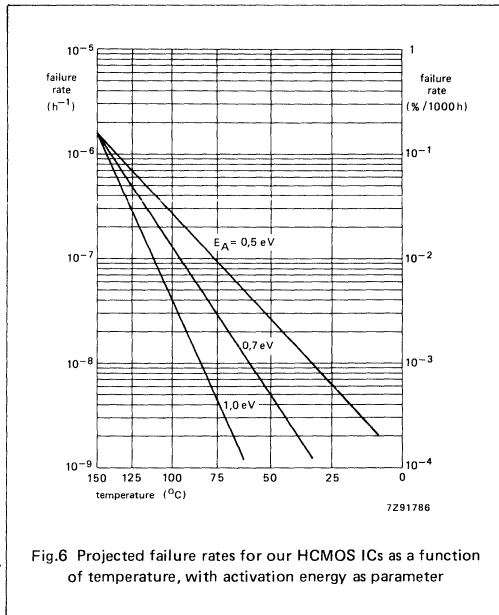
packages has been detected. In Table 6 the results given in Table 5 are derated to 50 °C operating temperature, using an activation energy E<sub>A</sub> of 0,7 eV. Figure 6 gives the derate failure rates for various activation energies.

**TABLE 5**  
**Life test results: HCMOS, 1983/Sept. '85 (cumulative)**

T (°C)	test duration (h)			
	1000	2000	4000	8000
(failures/sample)				
<b>Plastic DIL</b>				
125	0/77			
150	9/3600	8/1289	2/568	2/160
175	2/320	3/320	3/80	
225	0/48			
6 x parameter (I <sub>CC</sub> ), 6 x function (I <sub>CC</sub> , gate oxide)				
<b>SO</b>				
150	2/692	1/176	1/80	1/40
1 x parameter (I <sub>CC</sub> ), 1 x function (gate oxide)				

**TABLE 6**  
**Failure rates (from test data of Table 5)**

test temp. T (°C)	device hours (10 <sup>6</sup> )	50 °C device hours (10 <sup>6</sup> )	failures
<b>Plastic DIL</b>			
125	0,077	8,8	0
150	6,465	2463,1	9
175	0,800	892,6	3
225	0,048	330,7	0
Total:		3695,2	12
<b>SO</b>			
150	1,188	452	2
Extrapolated failure rate at 50 °C for E <sub>A</sub> = 0,7 eV			
Plastic DIL: λ = 3,2 FITS (3,2 x 10 <sup>-9</sup> /h);			
λ = 4,3 FITS (4,3 x 10 <sup>-9</sup> /h) at 60% confidence			
SO: λ = 4,4 FITS (4,4 x 10 <sup>-9</sup> /h);			
λ = 6,8 FITS (6,8 x 10 <sup>-9</sup> /h) at 60% confidence			



### RELIABILITY TEST PROGRAM

Conditions for the endurance tests performed regularly on structurally-similar groups of our HCMOS products are derived from IEC68 and MIL-STD-883C specifications. These are listed in Table 8, together with results obtained during 1983 and 1984.

### CECC RELEASE

The CECC (CENELEC Electronic Components Committee) Quality System, which dates from the early 1970s, harmonizes quality standards throughout Europe; fifteen countries now participate. Electronic components released under CECC must have satisfied the inspection requirements of the appropriate CECC Specification. The inspection and the application of the CECC System by suppliers are monitored by independent National Supervising Inspectorates, such as the British Standards Institute in the UK.

The component specification, which describes the component in sufficient detail to enable a customer to select it for a particular application, includes

- electrical values and their tolerances and limits
- behaviour under defined climatic, mechanical and endurance conditions
- acceptance criteria for batches of the component.

To qualify for the CECC Mark or Certificate of Conformity

### Temperature cycling

Cycling between  $-65^{\circ}\text{C}$  and  $+150^{\circ}\text{C}$  generates stresses that test the structural integrity of dice and packages. We perform this test according to the requirements of MIL-STD-883C, Method 1010, Condition C. Samples are checked before and after the test for function and electrical parameters against the published values. Two failures have been observed in 1200 cycles, as reported in Table 7.

**TABLE 7**  
Temperature cycling:  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  in dry air

no. of cycles	DIL		SO	
	samples	failures (cum)	samples	failures (cum)
200	1686	0	1016	0
400	1492	0	1016	0
800	997	0	1016	1
1200	360	0	594	2
1600	195	0	288	0
2000	195	0	288	
2400	195	0		

failures: 2 x die crack.



a component manufacturer must satisfy the National Supervising Inspectorate that:

- his Quality Department runs strictly according to CECC rules, and especially that it is independent of Production Management
- his production departments run according to CECC rules for each component inspected.

Our HCMOS products received official CECC approval in the second half of 1985.

**TABLE 8**  
**Periodic reliability test program: 1983/1984 results**

sub-group	description	IEC 68	derived from MIL-STD-883C method no.	plastic DIL		SO	
				N	n <sub>F</sub>	N	n <sub>F</sub>
C1	dimensions	—	2016	324	0	36	0
C2	marking permanence	—	2015	440	0	72	0
C3	robustness of termination	68-2-21	2004	234	0	108	0
	— tensile	Test Ua	cond. A				
	— bending	Test Ub	cond. B1				
C4	— lead fatigue	Test Ub	cond. B2				
	temperature treatments (sequential)			1739	0	157	0
	— resistance to soldering heat (10 s at 300 °C)						
	— thermal shock (10 x 0 °C to 100 °C)	68-2-27 Test Nc	1011 cond. A				
C6	— temperature cycling (10 x -65 °C to +150 °C)	68-2-14 Test Na	1011 cond. C				
	— storage to 85 °C and 85% RH for 21 days						
C8	THB* 85 °C/85% RH/6 V/1000 h	68-2-3 Test Ca	1004	(see Table 3)			
C10	electrical endurance 1000 h at 125 °C		1005	(see Tables 5 and 6)			
C11	temperature cycling						
	200 x -65 °C to +150 °C	68-2-14 Test B	1010 cond. C	1686	0	1016	0
C12	storage endurance	68-2-2 Test Ba	1008 cond. C	863	0	105	0
	1000 h at T <sub>a</sub> = 150 °C						
C13	storage endurance	68-2-1 Test Ab		625	0	105	0
	1000 h at T <sub>a</sub> = -65 °C						
C15	transient energy		3015				
C15	salt mist	68-2-11 Test Ka	1009 cond. A				
	solderability	68-2-20 Test T	2003	960	1	384	0
	autoclave 121 °C/100% RH/60 h			548	0	160	0

\* Temperature-humidity-bias. N = sample size.  
n<sub>F</sub> = number failures.

## HCMOS FAMILY CHARACTERISTICS

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**GENERAL**

These family specifications cover the common electrical ratings and characteristics of the entire HC MOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

**INTRODUCTION**

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits. The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

**HANDLING MOS DEVICES**

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

**RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT**

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V <sub>CC</sub>	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V <sub>I</sub>	DC input voltage range	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
V <sub>O</sub>	DC output voltage range	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
T <sub>amb</sub>	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHAR. per device
T <sub>amb</sub>	operating ambient temperature range	-40		+125	-40		+125	°C	
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V

**Note**

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

**RECOMMENDED OPERATING CONDITIONS FOR 74HCU**

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS		
		min.	typ.	max.				
V <sub>CC</sub>	DC supply voltage	2.0	5.0	6.0	V			
V <sub>I</sub>	DC input voltage range	0		V <sub>CC</sub>	V			
V <sub>O</sub>	DC output voltage range	0		V <sub>CC</sub>	V			
T <sub>amb</sub>	operating ambient temperature range			-40		+85	°C	see DC and AC CHAR. per device
T <sub>amb</sub>	operating ambient temperature range			-40		+125	°C	



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs - bus driver outputs		25 35	mA mA	for $-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: - standard outputs - bus driver outputs		50 70	mA mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT/HCU
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

**Note**

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8	0.5 1.35 1.8	V	2.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OH</sub>	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 6.0 mA -I <sub>O</sub> = 7.8 mA	
V <sub>OL</sub>	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 6.0 mA I <sub>O</sub> = 7.8 mA	
±I <sub>I</sub>	input leakage current			0.1		1.0	1.0	μA	6.0	V <sub>CC</sub> or GND		
±I <sub>OZ</sub>	3-state OFF-state current			0.5		5.0	10.0	μA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current SSI flip-flops MSI			2.0 4.0 8.0		20.0 40.0 80.0	40.0 80.0 160.0	μA μA μA	6.0 6.0 6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 0 I <sub>O</sub> = 0 I <sub>O</sub> = 0	

**FAMILY  
SPECIFICATIONS**

**DC CHARACTERISTICS FOR 74HCT**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OH</sub>	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 6.0 mA
V <sub>OL</sub>	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 6.0 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0
I <sub>CC</sub>	quiescent supply current SSI flip-flops MSI			2.0 4.0 8.0		20.0 40.0 80.0		40.0 80.0 160.0	μA μA μA	5.5 5.5 5.5	V <sub>CC</sub> or GND	I <sub>O</sub> = 0 I <sub>O</sub> = 0 I <sub>O</sub> = 0
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0

**Note**

- The additional quiescent supply current per input is determined by the ΔI<sub>CC</sub> unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V<sub>I</sub> = 2.4 V; V<sub>CC</sub> = 5.5 V) specification is: ΔI<sub>CC</sub> = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCU							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>CC</sub> or GND	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current SSI			2.0		20.0		40.0	μA	6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 0

**FAMILY  
SPECIFICATIONS**

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard outputs		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 3 and 4
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver outputs		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 3 and 4

**AC CHARACTERISTICS FOR 74HCU**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCU							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 1

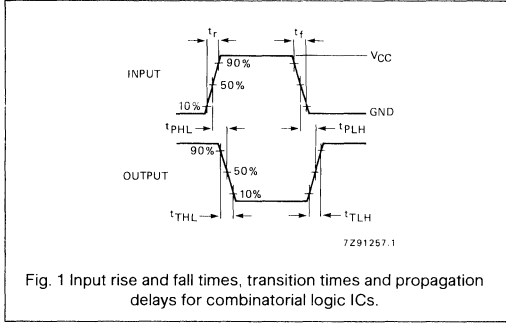
**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard outputs		7	15		19		22	ns	4.5	Figs 8 and 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver outputs		5	12		15		18	ns	4.5	Figs 8 and 9

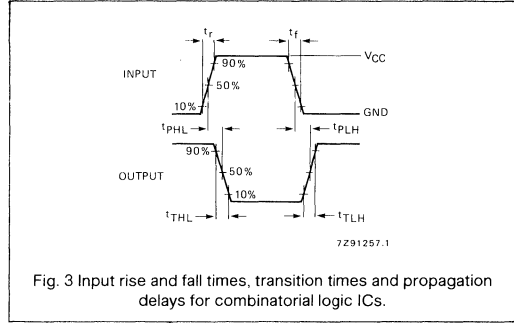
HCU TYPES

AC WAVEFORMS 74HCU

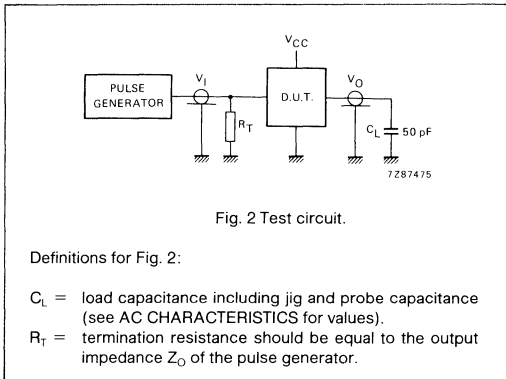


HC TYPES

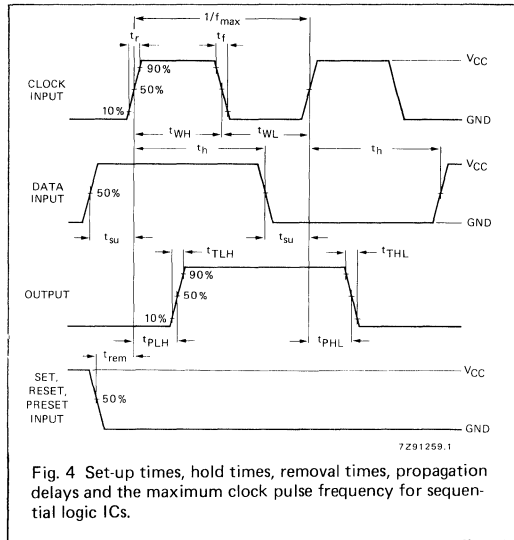
AC WAVEFORMS 74HC



TEST CIRCUIT FOR 74HCU



AC WAVEFORMS 74HC

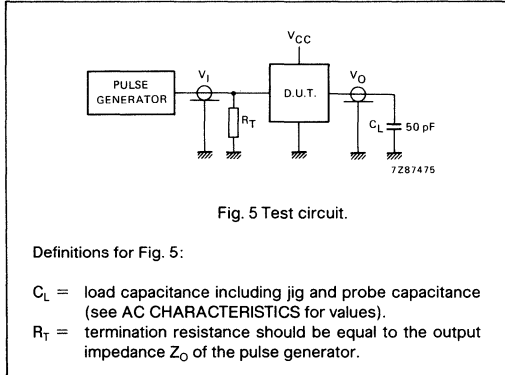


Notes to Fig. 4

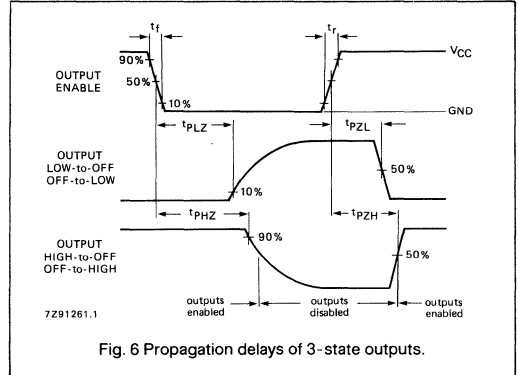
1. In Fig. 4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements:  $t_r = t_f = 6$  ns; when measuring  $f_{max}$ , there is no constraint on  $t_r, t_f$  with 50% duty factor.

HC TYPES (continued)

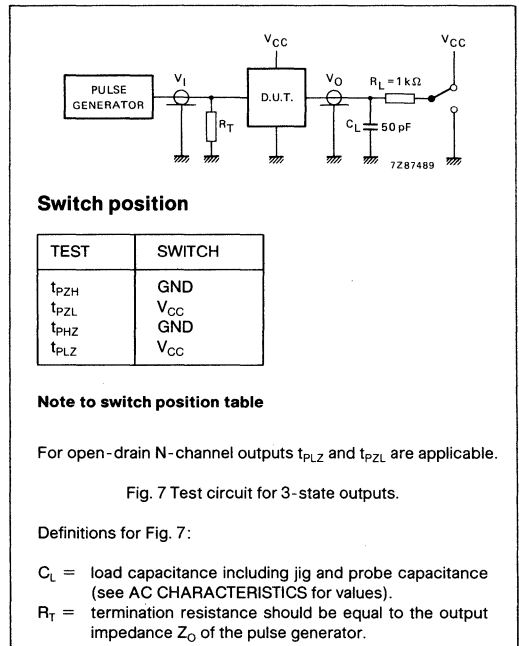
TEST CIRCUIT FOR 74HC



AC WAVEFORMS 74HC (continued)

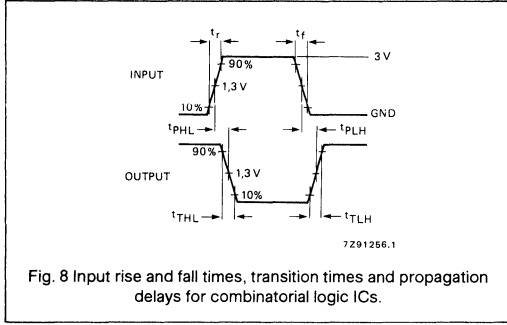


TEST CIRCUIT FOR 74HC



HCT TYPES

AC WAVEFORMS 74HCT



TEST CIRCUIT FOR 74HCT

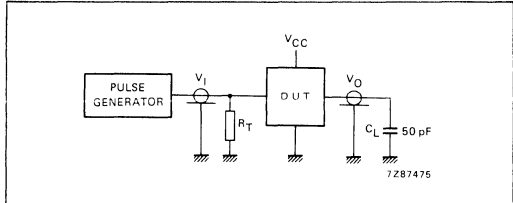


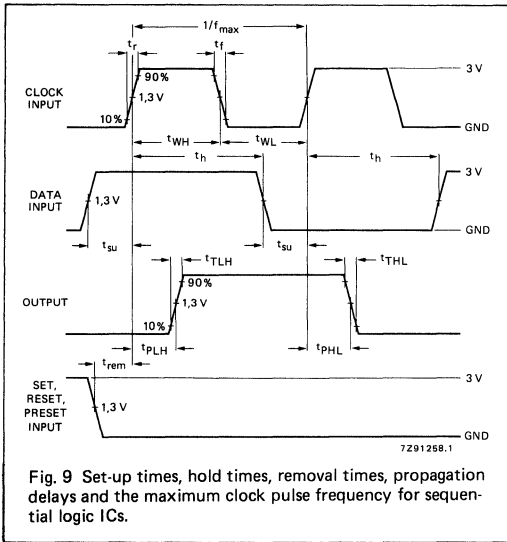
Fig. 10 Test circuit.

Definitions for Fig. 10:

$C_L$  = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

$R_T$  = termination resistance should be equal to the output impedance  $Z_O$  of the pulse generator.

AC WAVEFORMS 74HCT



Notes to Fig. 9

- In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
- For AC measurements:  $t_r = t_f = 6$  ns; when measuring  $f_{max}$ , there is no constraint on  $t_r, t_f$  with 50% duty factor.



HCT TYPES (continued)

AC WAVEFORMS 74HCT (continued)

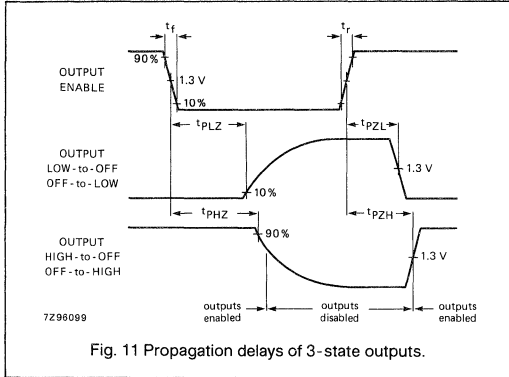
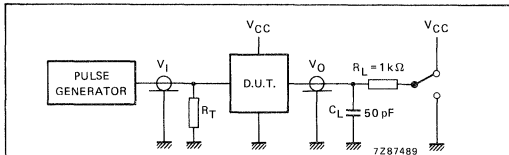


Fig. 11 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HCT



Switch position

TEST	SWITCH
$t_{PZH}$	GND
$t_{PZL}$	$V_{CC}$
$t_{PHZ}$	GND
$t_{PLZ}$	$V_{CC}$

Note to switch position table

For open-drain N-channel outputs  $t_{PLZ}$  and  $t_{PZL}$  are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

$C_L$  = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

$R_T$  = termination resistance should be equal to the output impedance  $Z_O$  of the pulse generator.

## INTRODUCTION

The 74HCMOS data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

## TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of  $t_{PLH}$  and  $t_{PHL}$  for the longest data path through the device with a 15 pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on  $t_r$  and  $t_f$ .

## LOGIC SYMBOLS

Two logic symbols are given for each device — the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEC Logic Symbol as developed by the IEC (International Electrotechnical Commission).

The IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) which supersedes Publication 117-15, published in 1972.

## RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System — IEC134) lists the maximum limits to which the device can be subjected without damage. This doesn't imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won't have been shortened.

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

## RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table lists the operating ambient temperature and the conditions under which the limits in the "DC CHARACTERISTICS" and "AC CHARACTERISTICS" tables will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC CHARACTERISTICS tables.

## DC CHARACTERISTICS

The "DC CHARACTERISTICS" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of  $V_{IH}$  and  $V_{IL}$  can be tested by the user. If  $V_{IH}$  and  $V_{IL}$  are applied to the inputs, the output voltages will be those published in the "DC CHARACTERISTICS" table. There is a tendency, by some, to use the published  $V_{IH}$  and  $V_{IL}$  thresholds to test a device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 metre. Parametric tests, such as those used for the output levels under the  $V_{IH}$  and  $V_{IL}$  conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use  $V_{IH}$  and  $V_{IL}$  to test the functionality of any HCMOS device type; instead, use input voltages of  $V_{CC}$  (for the HIGH state) and 0 V (for the LOW state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical  $V_{IL}$  is higher than the maximum  $V_{IL}$ . However, this is because  $V_{ILmax}$  is the maximum  $V_{IL}$  (guaranteed) for all devices that will be recognized as a logic LOW. However, typically a higher  $V_{IL}$  will also be recognized as a logic LOW. Conversely, the typical  $V_{IH}$  is lower than its minimum guaranteed level.

For 74HCMOS, unlike TTL, no output HIGH short-circuit current is specified. The use of this current, for example, to calculate propagation delays with capacitive loads, is covered by the HCMOS graphs showing the output drive capability and those showing the dependence of propagation delay on load capacitance.

The quiescent supply current  $I_{CC}$  is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors. It is measured with the inputs at  $V_{CC}$  or GND and is typically a few nA.

## AC CHARACTERISTICS

The "AC CHARACTERISTICS" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveforms section.

### TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground-plane) should be used for the same reasons. A  $V_{CC}$  decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to  $V_{CC}$  for 74HC and 0 V to 3 V for 74HCT; a 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing  $f_{max}$ . Two pulse generators are usually required for testing such parameters as set-up time, hold time and removal time.  $f_{max}$  is also tested with 6 ns input rise and fall times, with a 50% duty factor, but for typical  $f_{max}$  as high as 60 MHz, there are no constraints on rise and fall times.

**DEFINITIONS OF SYMBOLS AND TERMS USED IN  
HC MOS DATA SHEETS**

**Currents**

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

$I_{CC}$	Quiescent power supply current; the current flowing into the $V_{CC}$ supply terminal.
$\Delta I_{CC}$	Additional quiescent supply current per input pin at a specified input voltage and $V_{CC}$ .
$I_{GND}$	Quiescent power supply current; the current flowing into the GND terminal.
$I_i$	Input leakage current; the current flowing into a device at a specified input voltage and $V_{CC}$ .
$I_{IK}$	Input diode current; the current flowing into a device at a specified input voltage.
$I_O$	Output source or sink current; the current flowing into a device at a specified output voltage.
$I_{OK}$	Output diode current; the current flowing into a device at a specified output voltage.
$I_{OZ}$	OFF - state output current; the leakage current flowing into the output of a 3 - state device in the OFF - state, when the output is connected to $V_{CC}$ or GND.
$I_S$	Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and $V_{CC}$ .

**Voltages**

All voltages are referenced to GND (ground), which is typically 0 V.

GND	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
$V_{CC}$	Supply voltage; the most positive potential on the device.
$V_{EE}$	Supply voltage; one of two (GND and $V_{EE}$ ) negative power supplies.
$V_H$	Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative - going input signal.
$V_{IH}$	HIGH level input voltage ; the range of input voltages that represents a logic HIGH level in the system.
$V_{IL}$	LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.
$V_{OH}$	HIGH level output voltage ; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

$V_{OL}$  LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

$V_{T+}$  Trigger threshold voltage; positive - going signal.

$V_{T-}$  Trigger threshold voltage; negative - going signal.

**Analog terms**

$R_{ON}$  ON - resistance; the effective ON - state resistance of an analog switch, at a specified voltage across the switch and output load.

$\Delta R_{ON}$   $\Delta$ ON - resistance; the difference in ON - resistance between any two switches of an analog device at a specified voltage across the switch and output load.

**Capacitances**

$C_i$  Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$  Input/Output capacitance; the capacitance measured at a terminal connected to an I/O - pin (e.g. a transceiver).

$C_L$  Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

$C_{PD}$  Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

$C_S$  Switch capacitance; the capacitance of a terminal to a switch of an analog device.

**AC switching parameters**

$f_i$  Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

$f_o$  Output frequency; each output.

$f_{max}$  Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% $V_{CC}$  to 90% $V_{CC}$  in accordance with the device function table.

$t_h$  Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

$t_r$ ,  $t_f$  Clock input rise and fall times; 10% and 90% values.

## DEFINITIONS OF SYMBOLS

### AC switching parameters (continued)

$t_{PHL}$	Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V points for the 74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.	$t_{rem}$	Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74HC devices and the 1.3 V points for the 74HCT devices on both input voltage waveforms.
$t_{PLH}$	Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V point for the 74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.	$t_{su}$	Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
$t_{PHZ}$	3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC and 74HCU devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level ( $V_{OH}$ ) to a high impedance OFF-state (Z).	$t_{THL}$	Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.
$t_{PLZ}$	3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level ( $V_{OL}$ ) to a high impedance OFF-state (Z).	$t_{THH}$	Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.
$t_{PZH}$	3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level ( $V_{OH}$ ).	$t_W$	Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74HC and 74HCU devices and at the 1.3 V points for 74HCT devices.
$t_{PZL}$	3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level ( $V_{OL}$ ).		

DEVICE DATA



**QUAD 2-INPUT NAND GATE**

**FEATURES**

- Output capability: standard
- I<sub>CC</sub> category: SSI

**GENERAL DESCRIPTION**

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT00 provide the 2-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	8	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

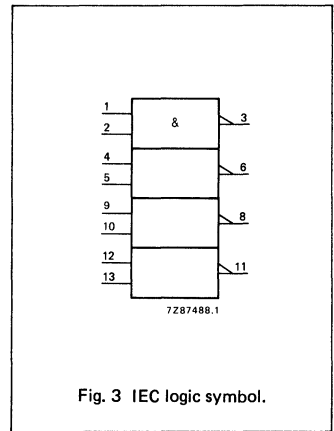
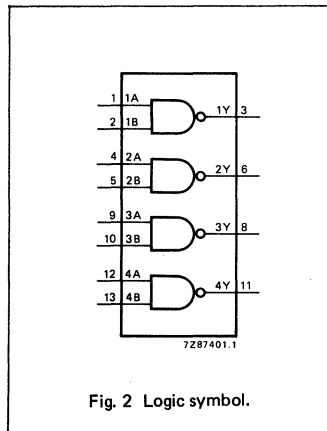
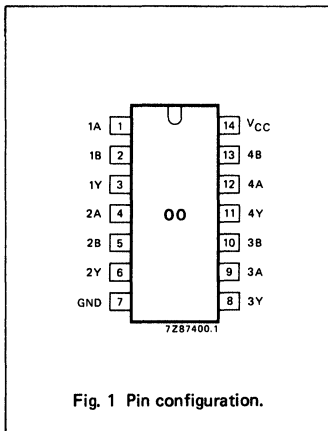
$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT00P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT00T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage





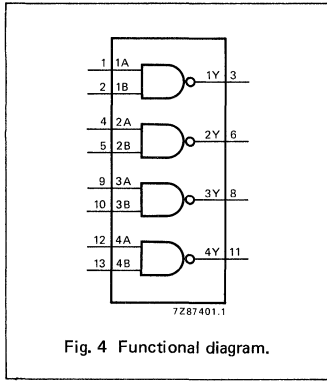


Fig. 4 Functional diagram.

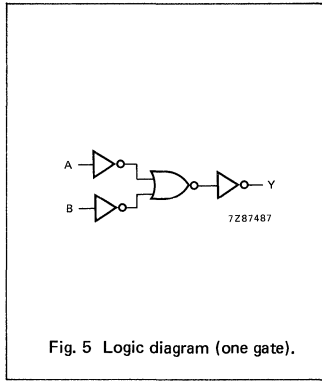


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level  
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nA, nB	2.20

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY		10	19		24		29	ns	4.5	Fig. 6
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

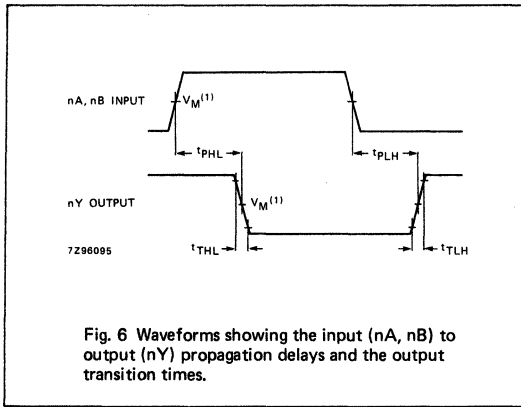


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## QUAD 2-INPUT NOR GATE

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT02 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT02 provide the 2-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	9	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per gate	notes 1 and 2	22	24	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

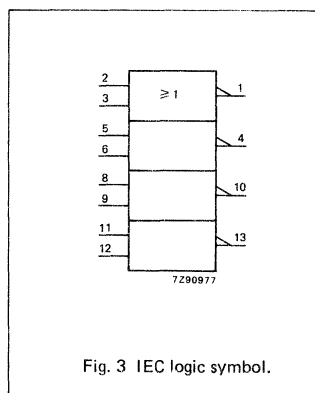
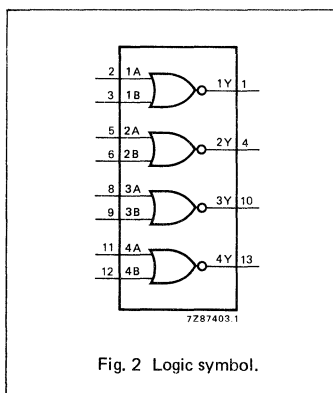
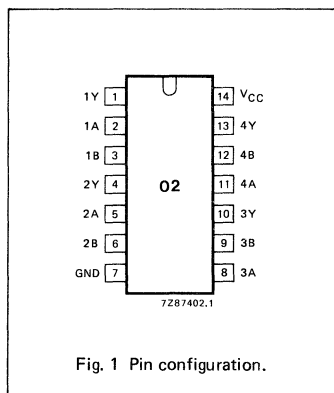
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT02P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT02T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



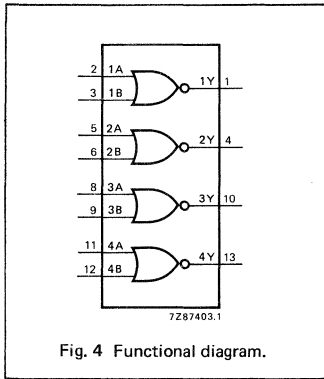


Fig. 4 Functional diagram.

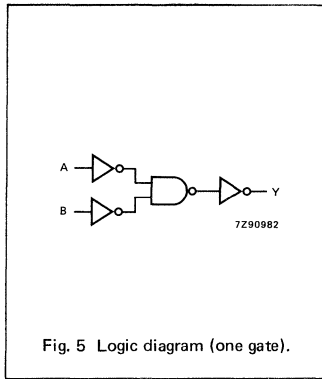


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level  
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

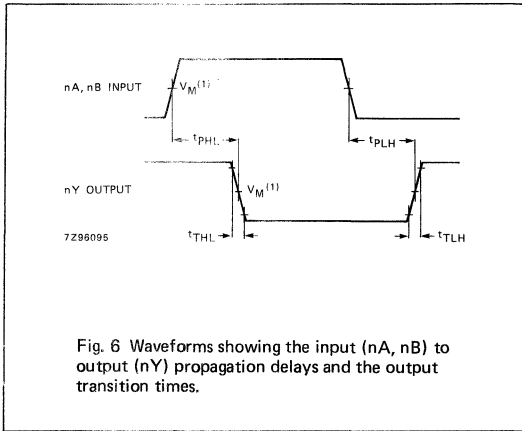
input	unit load coefficient
nA, nB	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay nA, nB to nY		11	19		24		29	ns	4.5	Fig. 6
$t_{THL}/$ $t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**QUAD 2-INPUT NAND GATE**

**FEATURES**

- Level shift capability
- Output capability: standard (open drain)
- ICC category: SSI

**GENERAL DESCRIPTION**

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to V<sub>CC</sub>. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V<sub>Omax</sub>. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PZL</sub> / t <sub>PLZ</sub>	propagation delay	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 kΩ V <sub>CC</sub> = 5 V	8	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_O^2/R_L) \times \text{duty factor LOW, where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

V<sub>O</sub> = output voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

∑ (V<sub>O</sub><sup>2</sup>/R<sub>L</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

R<sub>L</sub> = pull-up resistor in MΩ

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

3. The given value of C<sub>PD</sub> is obtained with:  
C<sub>L</sub> = 0 pF and R<sub>L</sub> = ∞

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT03P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT03T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

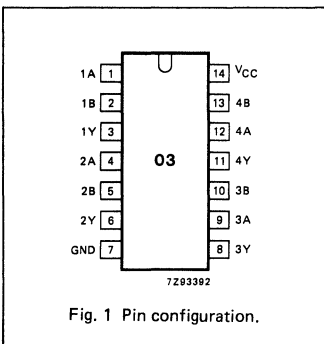


Fig. 1 Pin configuration.

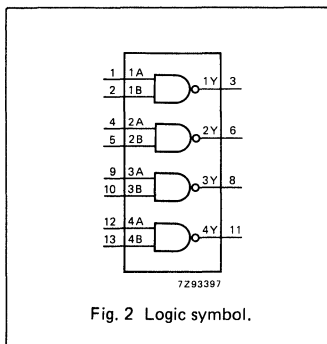


Fig. 2 Logic symbol.

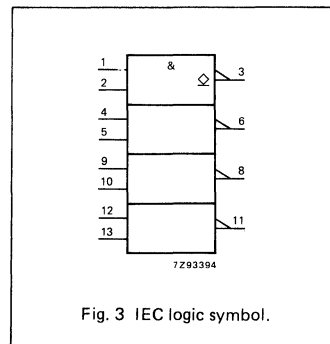
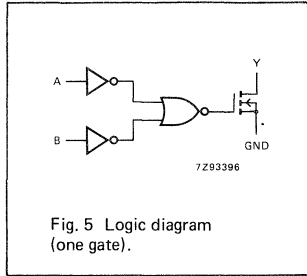
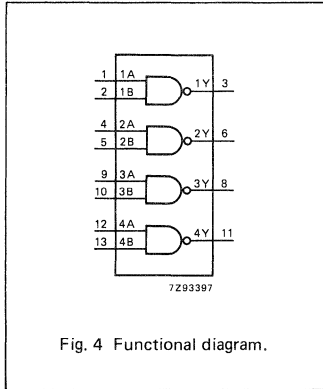


Fig. 3 IEC logic symbol.





FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level  
L = LOW voltage level  
Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)  
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V <sub>CC</sub>	DC supply voltage	-0.5	+7	V	
V <sub>O</sub>	DC output voltage	-0.5	+7	V	
I <sub>IK</sub>	DC input diode current		20	mA	for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V
-I <sub>OK</sub>	DC output diode current		20	mA	for V <sub>O</sub> < -0.5 V
-I <sub>O</sub>	DC output source or sink current		25	mA	for -0.5 V < V <sub>O</sub>
±I <sub>CC</sub> ; ±I <sub>GND</sub>	DC VCC or GND current		50	mA	
T <sub>stg</sub>	storage temperature range	-65	+150	°C	
P <sub>tot</sub>	power dissipation per package				for temperature range; -40 to +125 °C
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the  $V_{OH}$  values are not valid for open drain. They are replaced by  $I_{OH}$  as given below.

Output capability: standard (open drain), excepting  $V_{OH}$

$I_{CC}$  category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_I$	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
$I_{OH}$	HIGH level output leakage current			0.5		5.0		10.0	$\mu A$	2.0 to 6.0	$V_{IL}$	*

\*The maximum operating output voltage ( $V_{Omax}$ ) is 6.0 V.

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PZL}/t_{PLZ}$	propagation delay nA, nB to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
$t_{THL}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications", except that the  $V_{OH}$  values are not valid for open drain. They are replaced by  $I_{OH}$  as given below.

Output capability: standard (open drain), excepting  $V_{OH}$

$I_{CC}$  category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_I$	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
$I_{OH}$	HIGH level output leakage current			0.5		5.0		10.0	$\mu A$	4.5 to 5.5	$V_{IL}$	*

\*The maximum operating output voltage ( $V_{Omax}$ ) is 6.0 V.

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PZL}/t_{PLZ}$	propagation delay nA, nB, to nY		12	24		30		36	ns	4.5	Fig. 6
$t_{THL}$	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

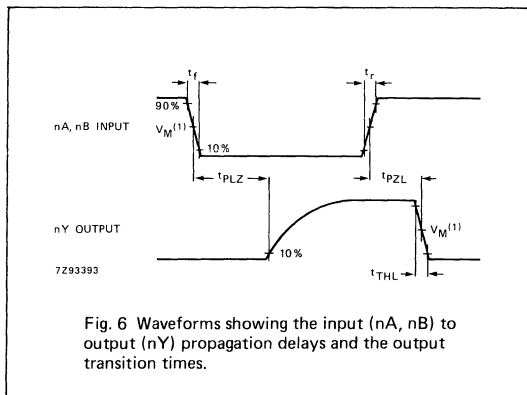


Fig. 6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS

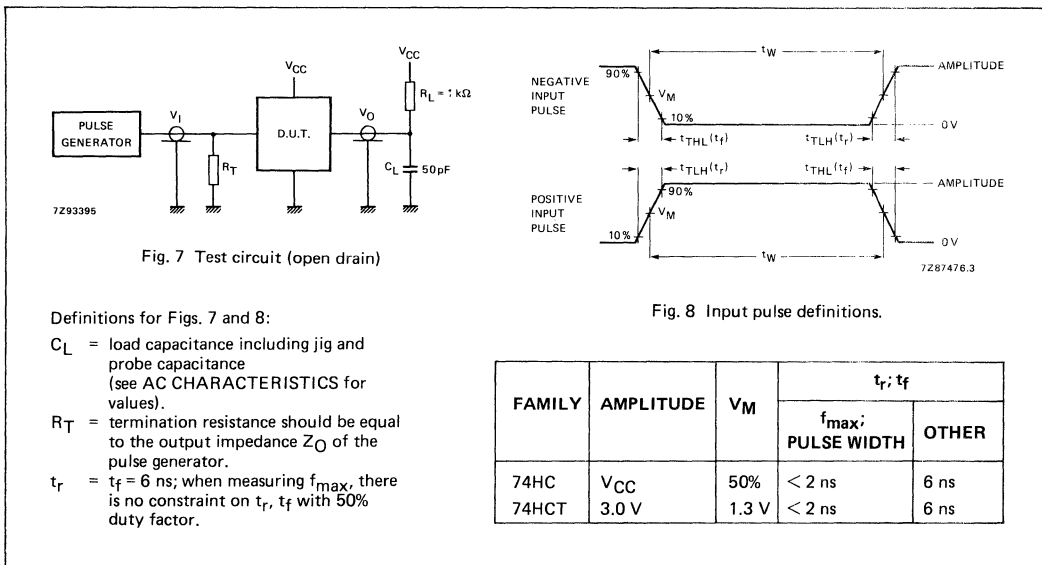


Fig. 7 Test circuit (open drain)

Fig. 8 Input pulse definitions.

Definitions for Figs. 7 and 8:

- $C_L$  = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- $R_T$  = termination resistance should be equal to the output impedance  $Z_O$  of the pulse generator.
- $t_r$  =  $t_f = 6 \text{ ns}$ ; when measuring  $f_{max}$ , there is no constraint on  $t_r$ ,  $t_f$  with 50% duty factor.

FAMILY	AMPLITUDE	$V_M$	$t_r; t_f$	
			$f_{max};$ PULSE WIDTH	OTHER
74HC	$V_{CC}$	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns



## HEX INVERTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT04 provide six inverting buffers.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	8	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT04P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT04T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 4A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

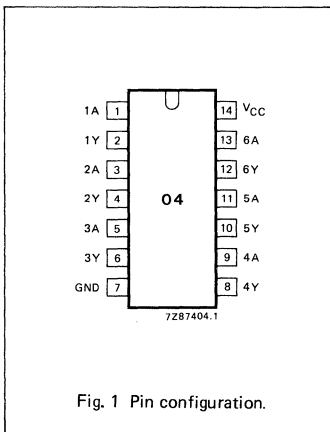


Fig. 1 Pin configuration.

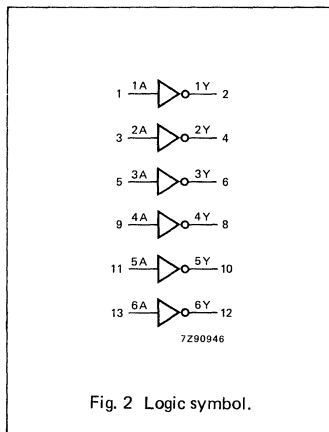


Fig. 2 Logic symbol.

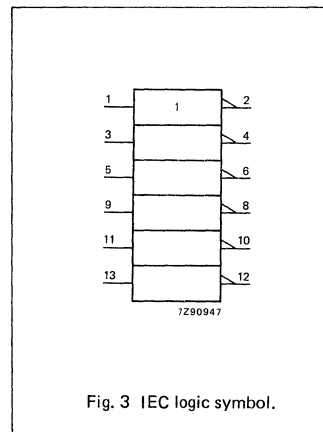


Fig. 3 IEC logic symbol.

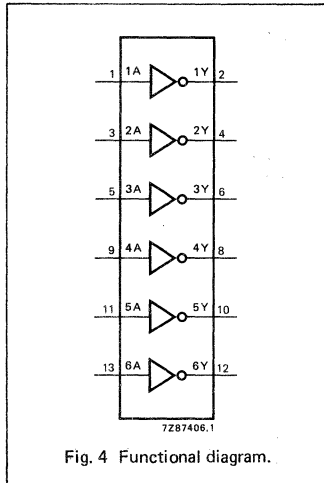


Fig. 4 Functional diagram.

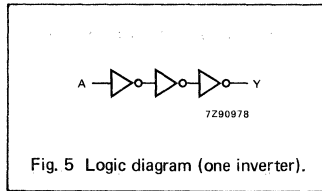


Fig. 5 Logic diagram (one inverter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level  
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nA	1.20

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		10	20		24		29	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6



AC WAVEFORMS

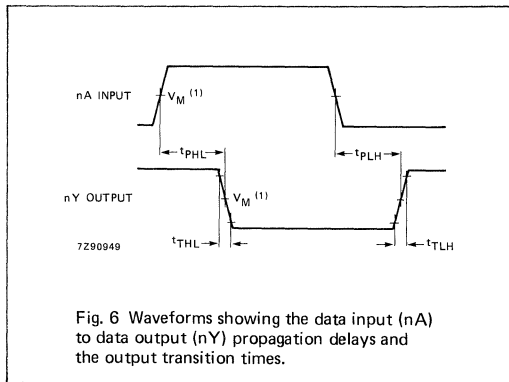


Fig. 6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

**Note to AC waveforms**

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## HEX INVERTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HCU04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7.

The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

### FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level  
L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	5	ns
C <sub>I</sub>	input capacitance		3.5	pF
CPD	power dissipation capacitance per inverter	notes 1 and 2	10	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

- 2.

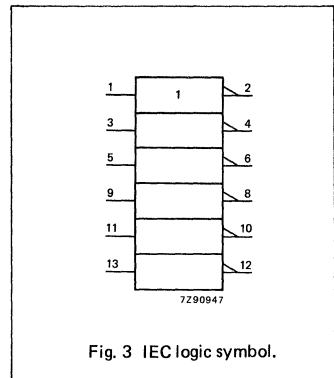
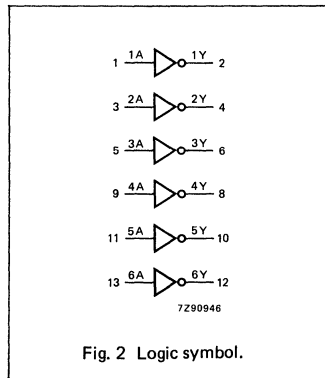
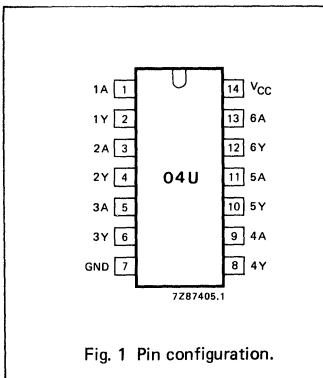
### ORDERING INFORMATION/PACKAGE OUTLINES

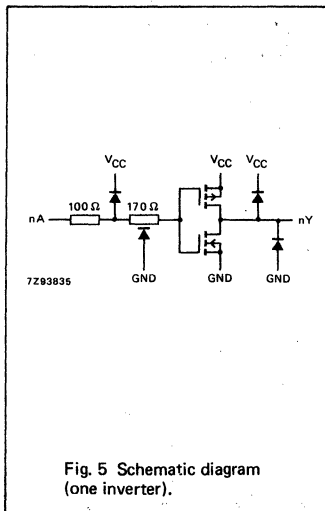
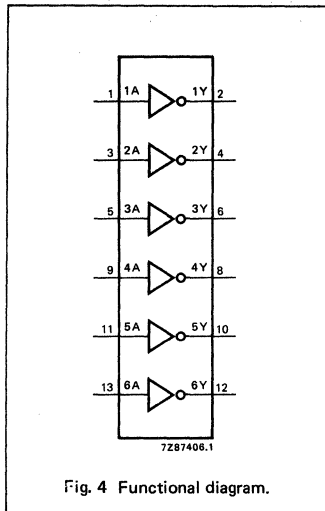
PC74HCU04P: 14-lead DIL; plastic (SOT-27).

PC74HCU04T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage





## DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

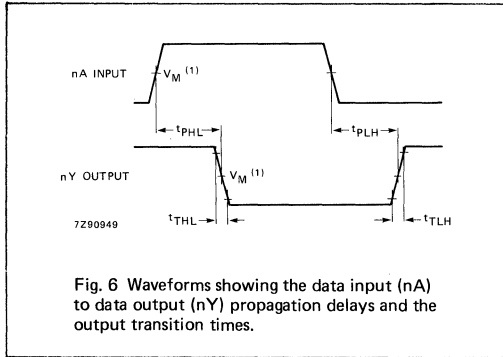
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCU							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>CC</sub> or GND	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current			2.0		20.0		40.0	μA	6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 0

AC CHARACTERISTICS FOR 74HCU

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

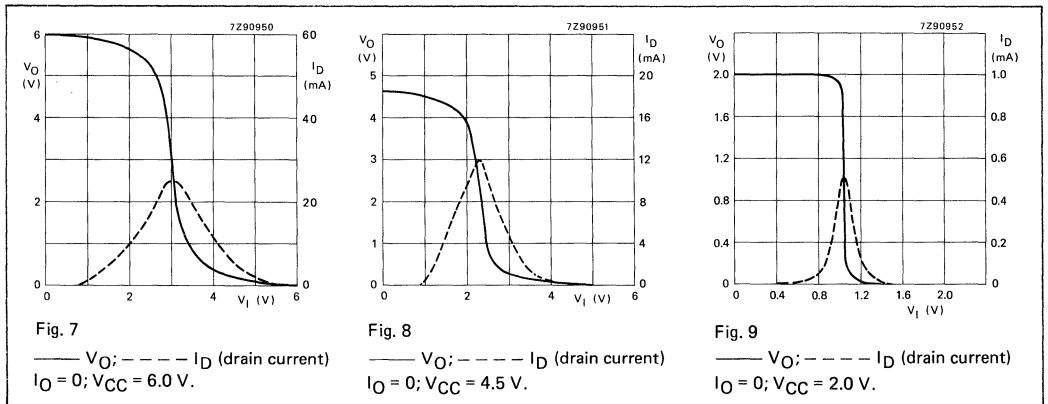
SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCU							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to nY		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

AC WAVEFORMS



Note to AC waveforms  
(1)  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

TYPICAL TRANSFER CHARACTERISTICS



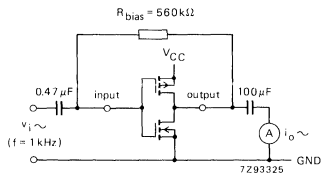


Fig. 10 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig. 11).

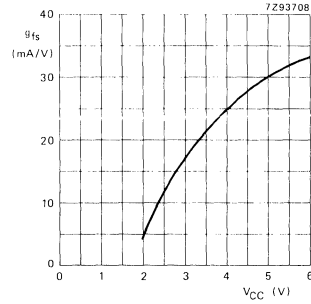


Fig. 11 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage  $V_{CC}$  at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

## APPLICATION INFORMATION

Some applications for the "HCU04" are:

- In crystal oscillator designs
- Linear amplifier (see Fig. 12).

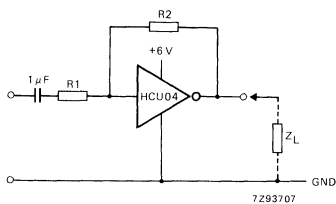


Fig. 12 HCU04 used as a linear amplifier.

### Note to Fig. 12

$Z_L > 10\text{ k}\Omega$ ;  $A_{OL} = 20$  (typ.)

$$A_u = - \frac{A_{OL}}{1 + \frac{R1}{R2} (1 + A_{OL})}; \quad V_{O \text{ max (p-p)}} \approx V_{CC} - 2\text{ V centered at } \frac{1}{2} V_{CC}$$

$3\text{ k}\Omega \leq R1, R2 \leq 1\text{ M}\Omega$

Typical unity gain bandwidth product is 5 MHz.

$C_1 = 20\text{ pF}$  (typ.)

$A_{OL}$  = open loop amplification

$A_u$  = voltage amplification

QUAD 2-INPUT AND GATE

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT08 provide the 2-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

- C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT08P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT08T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

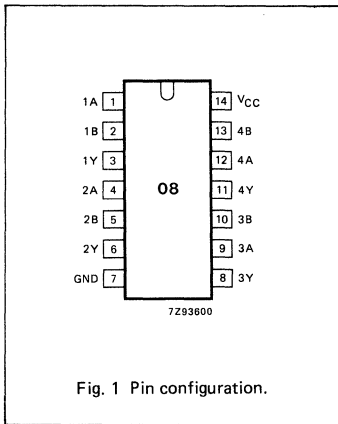


Fig. 1 Pin configuration.

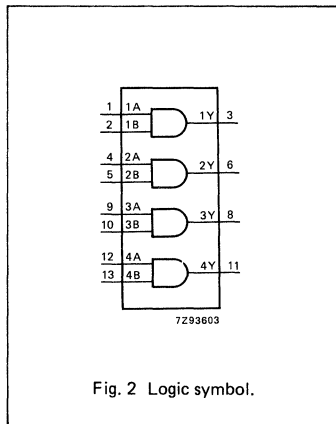


Fig. 2 Logic symbol.

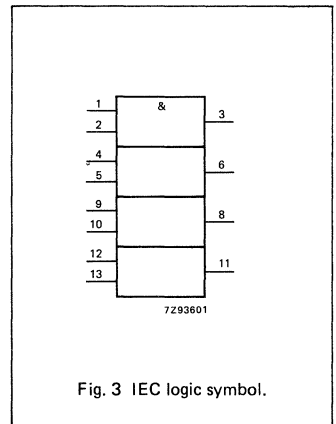
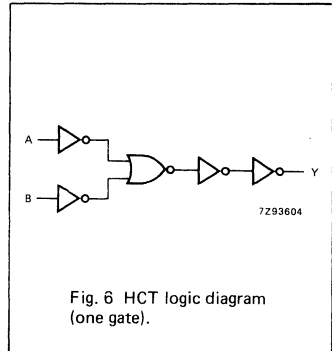
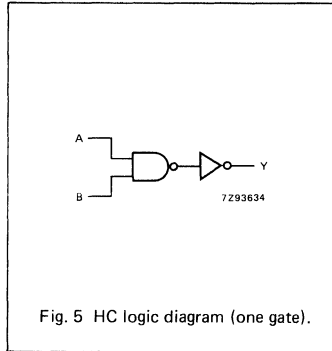
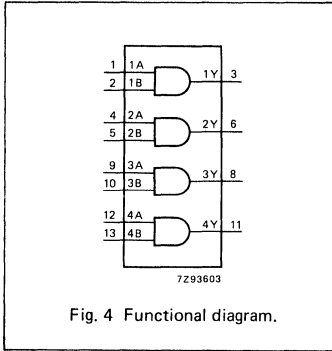


Fig. 3 IEC logic symbol.



**FUNCTION TABLE**

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level  
L = LOW voltage level

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS		
		74HC									V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125		min.				max.
		min.	typ.	max.	min.	max.	min.	max.					
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7		
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7		



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7

**AC WAVEFORMS**

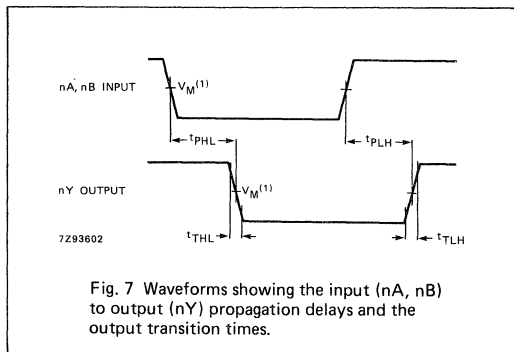


Fig. 7 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3V.

### TRIPLE 3-INPUT NAND GATE

#### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

#### GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT10 provide the 3-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	12	14	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

#### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

#### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT10P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT10T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

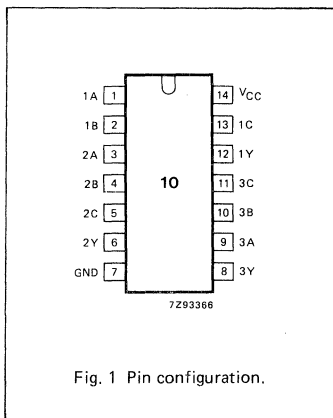


Fig. 1 Pin configuration.

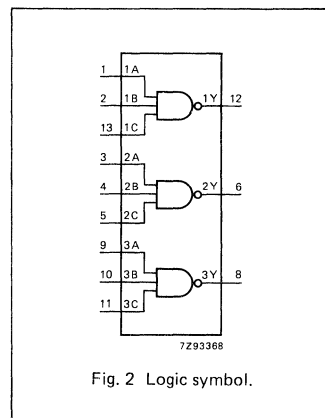


Fig. 2 Logic symbol.

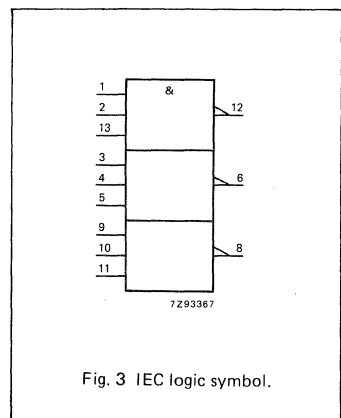
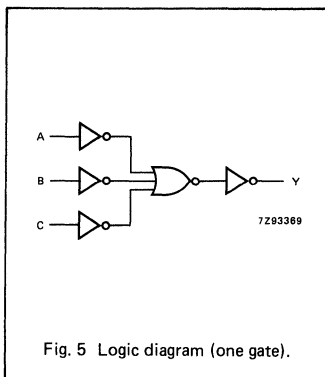
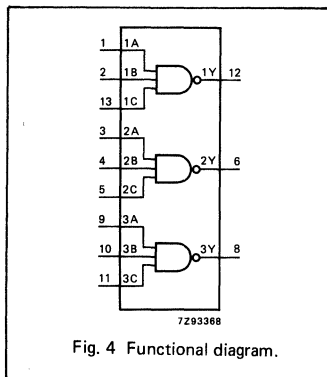


Fig. 3 IEC logic symbol.

**PC74HC/HCT10**  
**SSI**



**FUNCTION TABLE**

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH voltage level  
L = LOW voltage level

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given in the family specifications. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

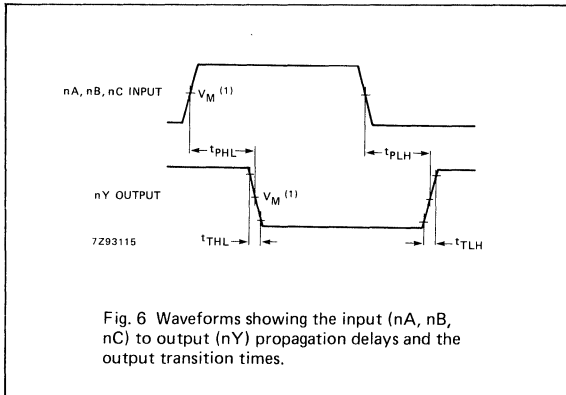
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		14	24		30		36	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

TRIPLE 3-INPUT AND GATE

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT11 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT11 provide the 3-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	10	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	26	28	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

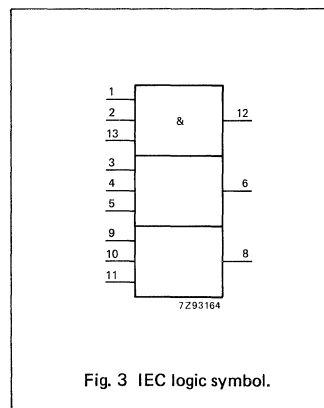
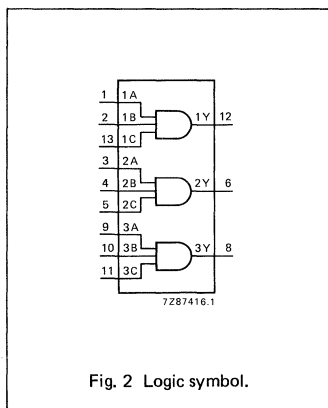
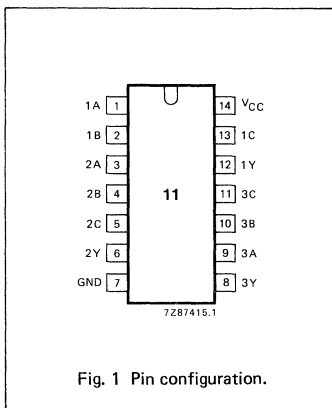
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT11P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT11T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data outputs
14	V <sub>CC</sub>	positive supply voltage



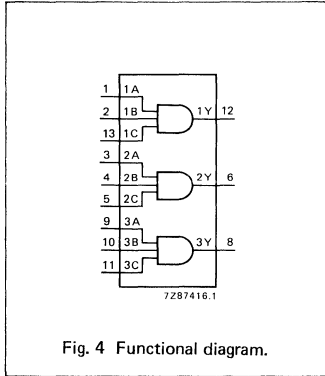


Fig. 4 Functional diagram.

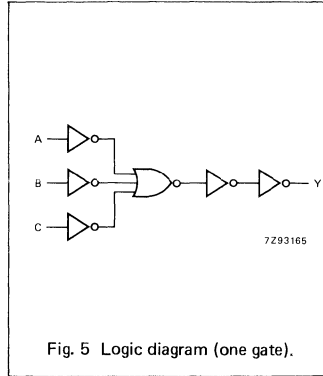


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

H = HIGH voltage level  
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY	32 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition times	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

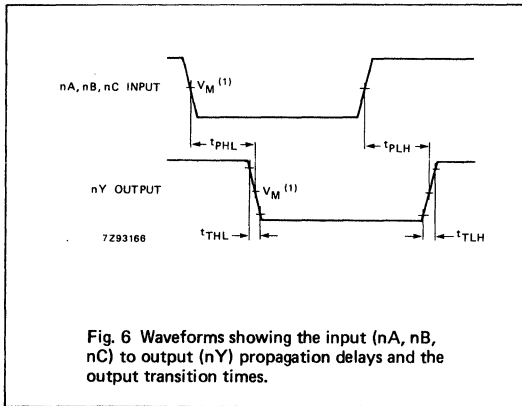
input	unit load coefficient
nA, nB, nC	0.5

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		16	28		35		42	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition times		7	15		19		22	ns	4.5	Fig. 6

## AC WAVEFORMS



## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .HCT:  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND to } 3\text{ V}$ .





## HEX INVERTING SCHMITT TRIGGER

### FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT14 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT14 provide six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA to nY	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	11	15	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	7	8	pF

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  

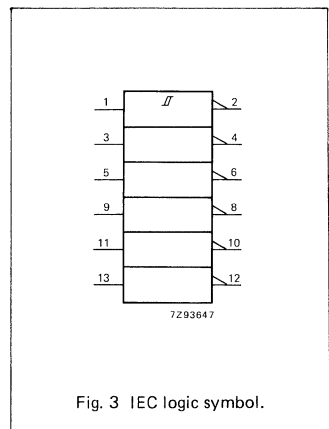
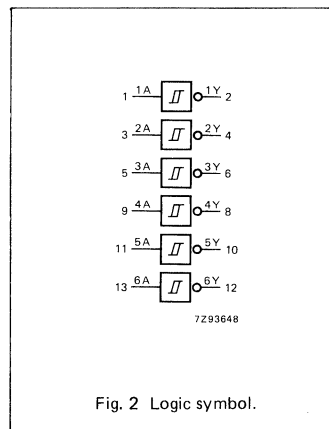
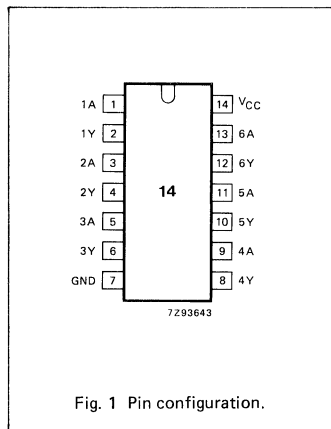
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 $f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT14P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT14T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	$V_{CC}$	positive supply voltage



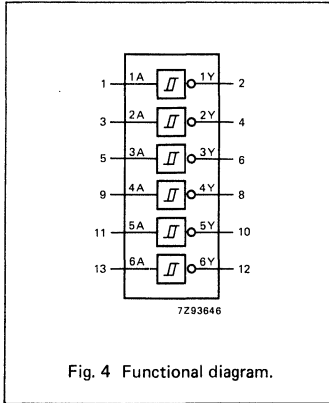


Fig. 4 Functional diagram.

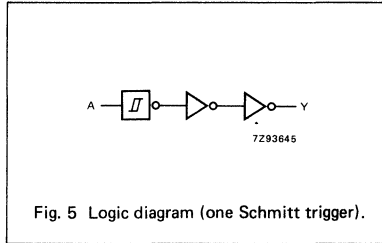


Fig. 5 Logic diagram (one Schmitt trigger).

**FUNCTION TABLE**

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level  
L = LOW voltage level

**APPLICATIONS**

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard

I<sub>CC</sub> category: SSI

## Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
V <sub>T+</sub>	positive-going threshold	0.7 1.7 2.1		1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V <sub>T-</sub>	negative-going threshold	0.3 0.9 1.2		1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	Figs 6 and 7
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.2 0.4 0.6		1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard  
I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA	0.3

**Transfer characteristics for 74HCT**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
V <sub>T+</sub>	positive-going threshold	1.2 1.4		1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5	Figs 6 and 7
V <sub>T-</sub>	negative-going threshold	0.5 0.6		1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.4 0.4		— —	0.4 0.4	— —	0.4 0.4	— —	V	4.5 5.5	Figs 6 and 7

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		18	31		39		47	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 8

## TRANSFER CHARACTERISTIC WAVEFORMS

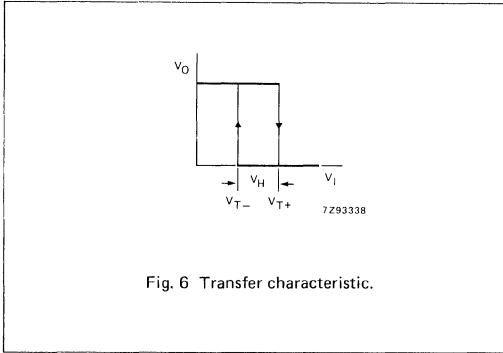
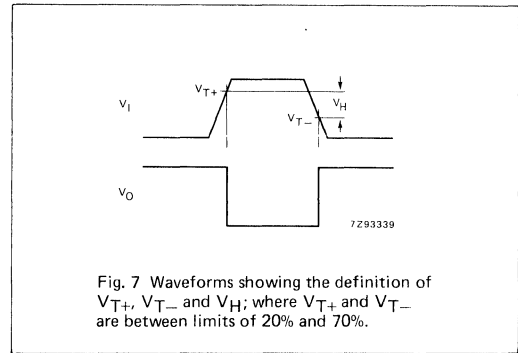


Fig. 6 Transfer characteristic.

Fig. 7 Waveforms showing the definition of  $V_{T+}$ ,  $V_{T-}$  and  $V_H$ ; where  $V_{T+}$  and  $V_{T-}$  are between limits of 20% and 70%.

## AC WAVEFORMS

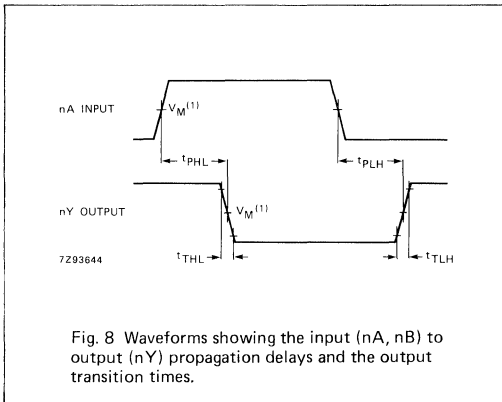


Fig. 8 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL 4-INPUT NAND GATE

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT20 provide the 4-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC, nD to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	22	17	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

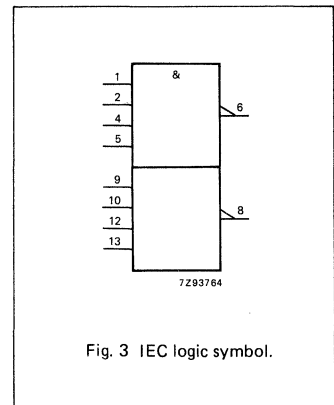
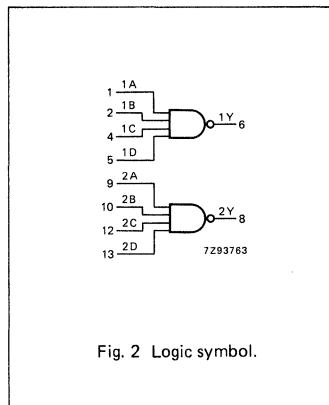
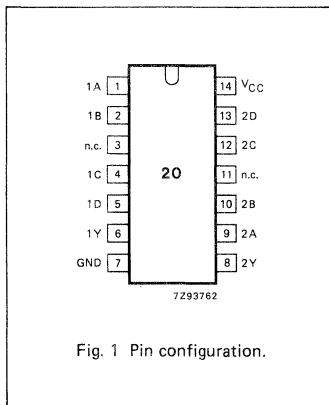
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT20P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT20T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



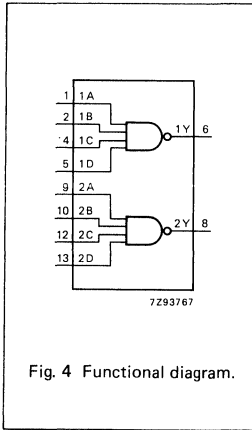


Fig. 4 Functional diagram.

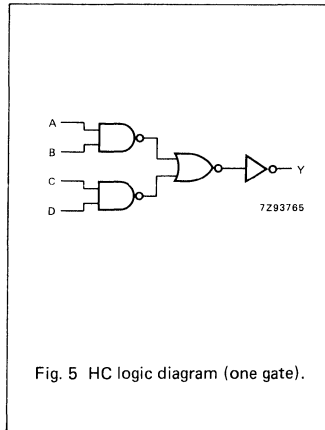


Fig. 5 HC logic diagram (one gate).

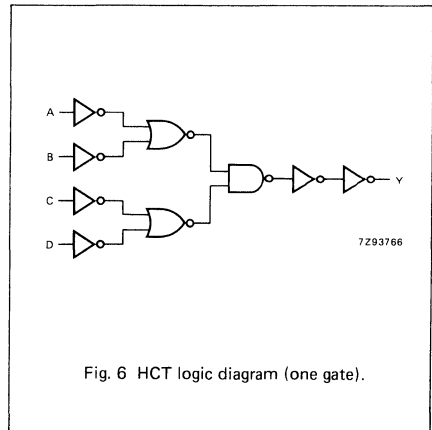


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC, nD to nY		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.3

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC, nD to nY		16	28		35		42	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7

**AC WAVEFORMS**

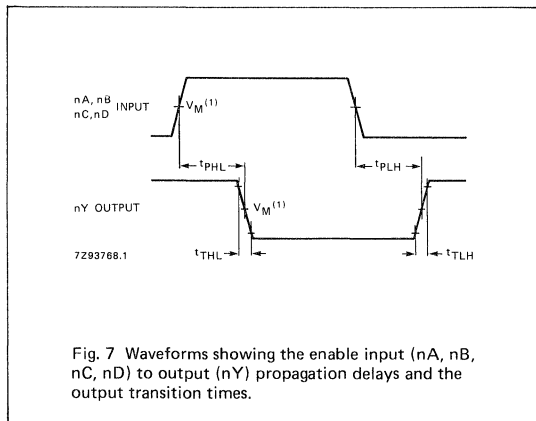


Fig. 7 Waveforms showing the enable input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT21  
SSI

## DUAL 4-INPUT AND GATE

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT21 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT21 provide the 4-input NAND function.

### FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC, nD to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

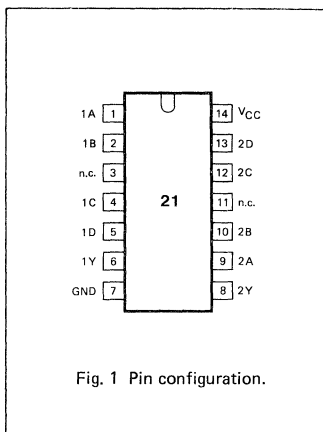
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT21P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT21T: 14-lead mini-pack; plastic (SO-14; SOT108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage





### TRIPLE 3-INPUT NOR GATE

#### FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

#### GÉNÉRAL DESCRIPTION

The 74HC/HCT27 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT27 provide the 3-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB, nC to nY	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	8	10	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	24	30	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

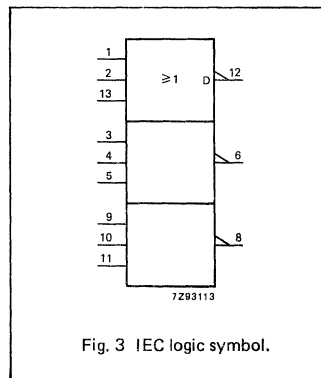
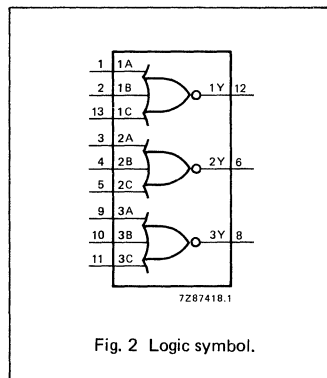
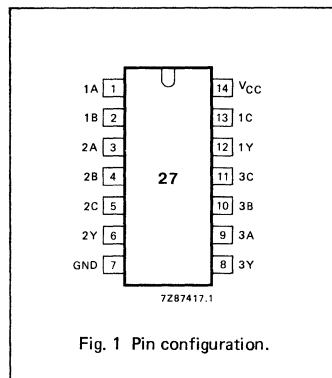
#### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT27P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT27T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
14	$V_{CC}$	positive supply voltage



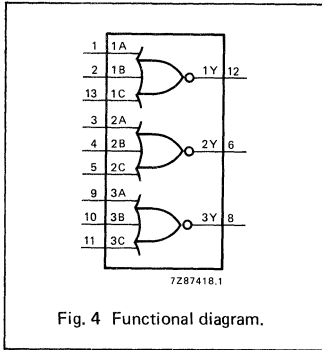


Fig. 4 Functional diagram.

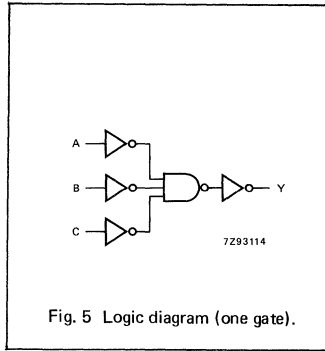


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		28 10 8	90 18 15		115 23 20		135 22 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

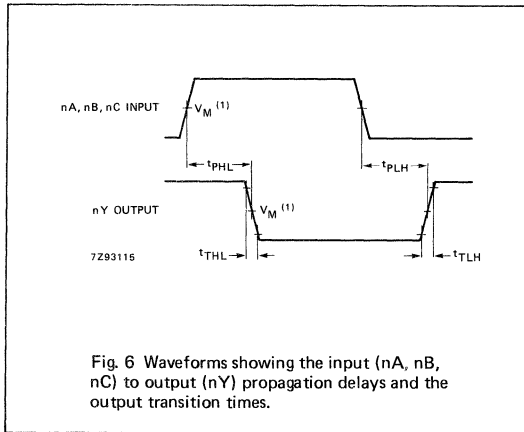
input	unit load coefficient
nA, nB, nC	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		12	21		26		32	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## 8-INPUT NAND GATE

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT30 provide the 8-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A, B, C, D, E, F, G, H to Y	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	15	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	23	24	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

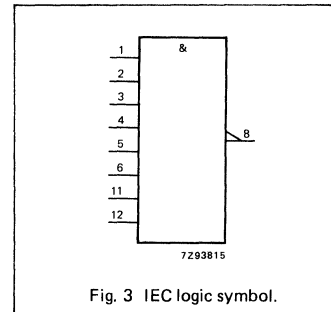
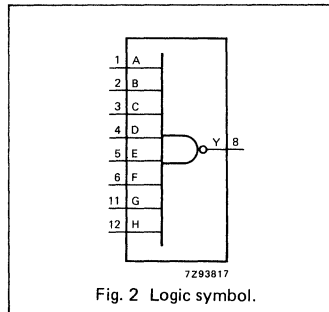
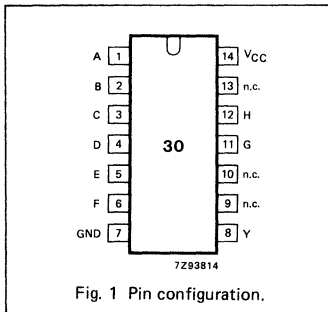
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT30P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT30T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A	data input
2	B	data input
3	C	data input
4	D	data input
5	E	data input
6	F	data input
7	GND	ground (0 V)
8	Y	data output
9, 10, 13	n.c.	not connected
11	G	data input
12	H	data input
14	V <sub>CC</sub>	positive supply voltage





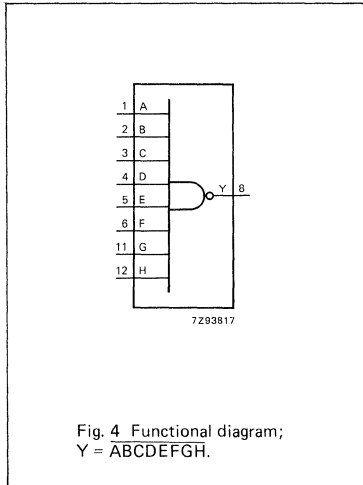


Fig. 4 Functional diagram;  
Y = ABCDEFGH.

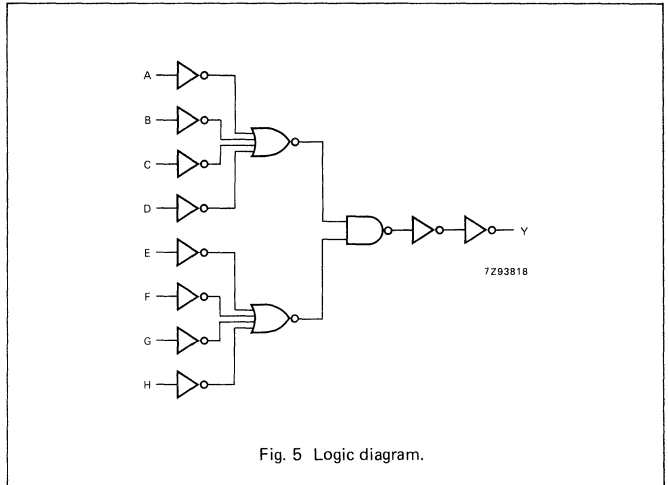


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

**DC CHARACTERISTICS FOR 74 HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A, B, C, D, E, F, G, H to Y	39 14 11	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

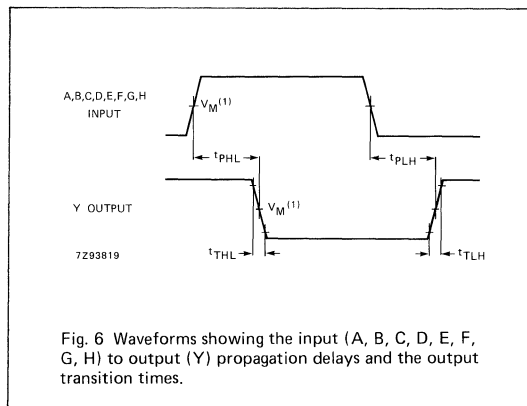
INPUT	UNIT LOAD COEFFICIENT
A, B, C, D, E, F, G, H	0.60

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A, B, C, D, E, F, G, H to Y		18	31		39		47	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

QUAD 2-INPUT OR GATE

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT32 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT32 provide the 2-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	6	9	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT32P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT32T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

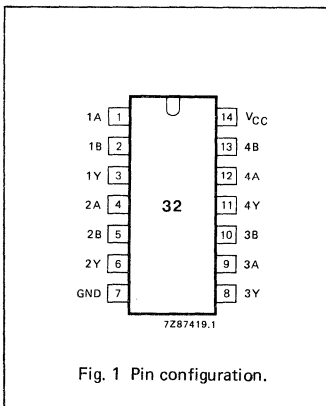


Fig. 1 Pin configuration.

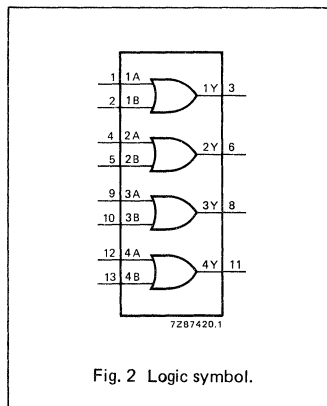


Fig. 2 Logic symbol.

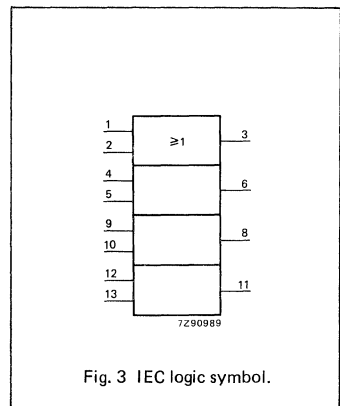


Fig. 3 IEC logic symbol.

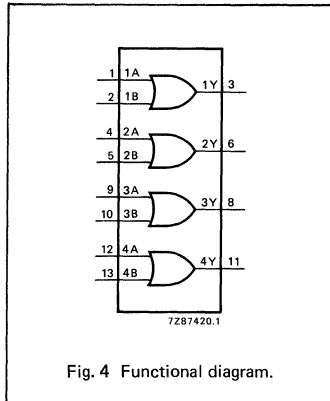


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level  
L = LOW voltage level

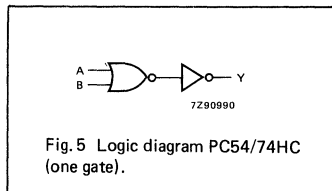


Fig. 5 Logic diagram PC54/74HC (one gate).

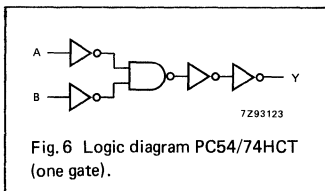


Fig. 6 Logic diagram PC54/74HCT (one gate).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

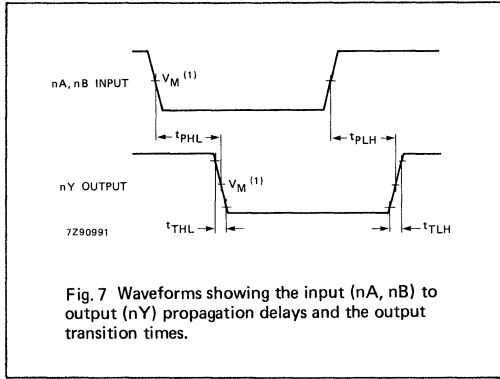
input	unit load coefficient
nA, nB	1.20

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY		11	24		30		36	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .







# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

**PC74HC58**  
SSI

## DUAL AND-OR GATE

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC58 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7.

The "58" provides two sections of AND-OR gates. One section contains a 2-wide, 3-input (1A to 1F) AND-OR gate and the second section contains a 2-wide, 2-input (2A to 2D) AND-OR gate.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1n, 2n to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	10	ns
C <sub>I</sub>	input capacitance		3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	18	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

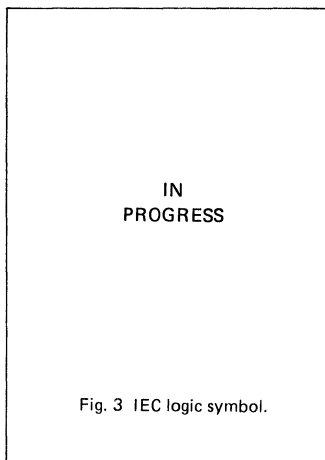
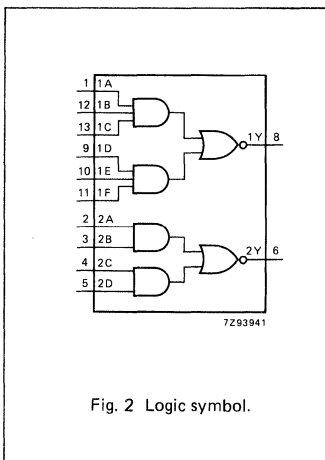
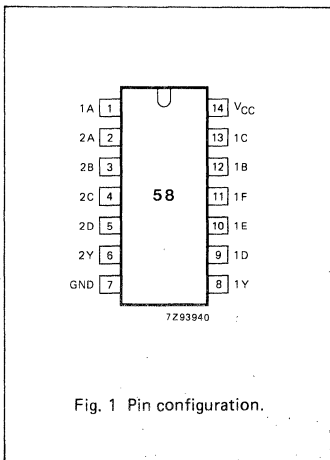
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC58P: 14-lead DIL; plastic (SOT-27).

PC74HC58T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 12, 13, 9, 10, 11	1A to 1F	data inputs
2, 3, 4, 5	2A to 2D	data inputs
8, 6	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT73 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT73 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ( $\overline{nCP}$ ) and reset ( $\overline{nR}$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $\overline{nR}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the  $\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{CP}$ to n $\overline{Q}$ n $\overline{CP}$ to n $\overline{Q}$ n $\overline{R}$ to n $\overline{Q}$ , n $\overline{Q}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
			15	18	ns
			14	17	ns
f <sub>max</sub>	maximum clock frequency		58	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power-dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

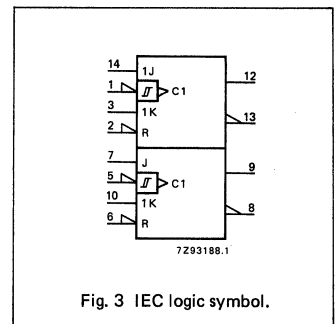
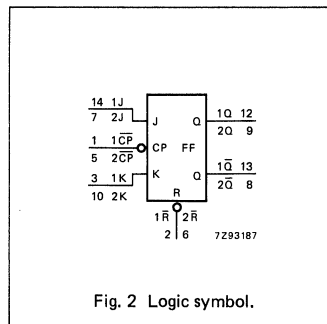
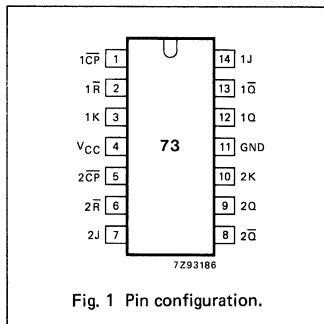
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT73P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT73T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5	1 $\overline{CP}$ , 2 $\overline{CP}$	clock input (LOW-to-HIGH, edge-triggered)
2, 6	1 $\overline{R}$ , 2 $\overline{R}$	asynchronous reset inputs (active LOW)
4	V <sub>CC</sub>	positive supply voltage
11	GND	ground (0 V)
12, 9	1Q, 2Q	true flip-flop outputs
13, 8	1 $\overline{Q}$ , 2 $\overline{Q}$	complement flip-flop outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2



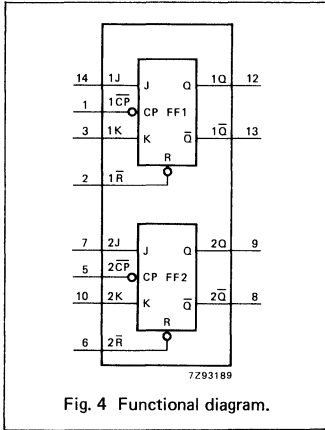


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	nR̄	nCP̄	J	K	Q	Q̄
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	q̄	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	q

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 ↓ = HIGH-to-LOW CP transition

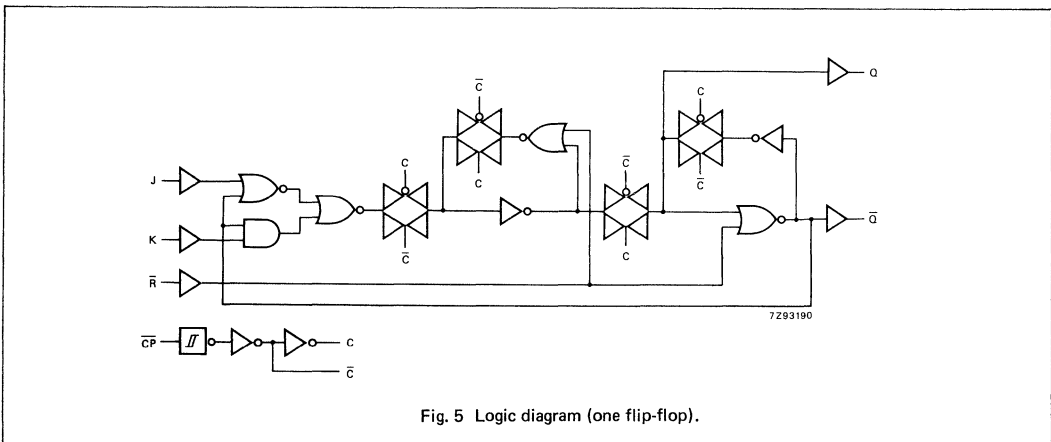


Fig. 5 Logic diagram (one flip-flop).

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ̄		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nR̄ to nQ, nQ̄		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	reset pulse width HIGH or LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time nR̄ to nCP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time nJ, nK to nCP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>h</sub>	hold time nJ, nK to nCP	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum maximum clock pulse frequency	6.0 30 35	18 54 64		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nJ, nK	0.35
n $\bar{R}$	0.35
n $\bar{CP}$	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74 HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{CP}$ to nQ		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{CP}$ to n $\bar{Q}$		21	36		45		54	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{R}$ to nQ, n $\bar{Q}$		20	34		43		51	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	23	12		29			35	ns	4.5	Fig. 6
t <sub>W</sub>	reset pulse width HIGH or LOW	18	9		23			27	ns	4.5	Fig. 7
t <sub>rem</sub>	removal time n $\bar{R}$ to n $\bar{CP}$	12	5		15			18	ns	4.5	
t <sub>su</sub>	set-up time nJ, nK to n $\bar{CP}$	12	5		15			18	ns	4.5	Fig. 6
t <sub>h</sub>	hold time nJ, nK to n $\bar{CP}$	5	0		5			5	ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	27	46		22			18	MHz	4.5	Fig. 6

AC WAVEFORMS

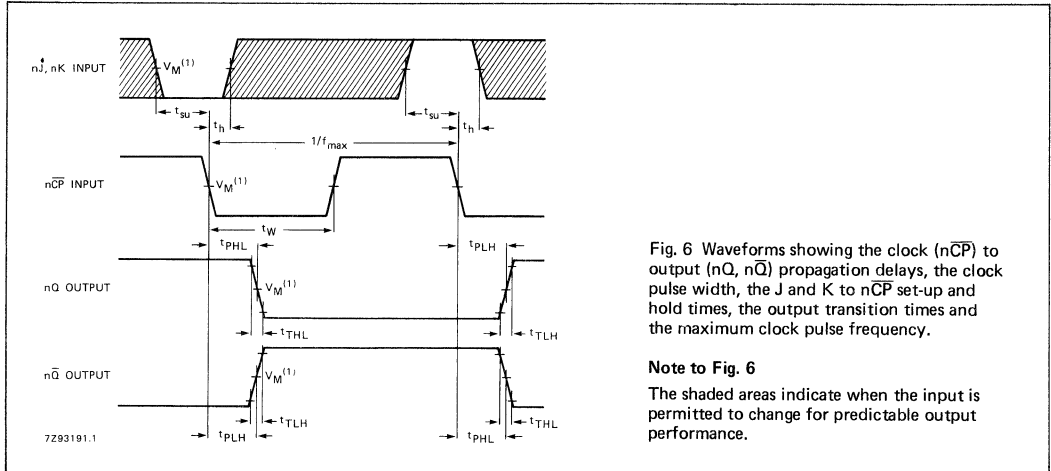


Fig. 6 Waveforms showing the clock ( $n\overline{CP}$ ) to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays, the clock pulse width, the J and K to  $n\overline{CP}$  set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

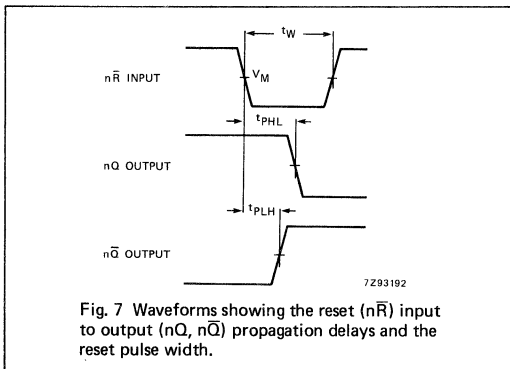


Fig. 7 Waveforms showing the reset ( $n\overline{R}$ ) input to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays and the reset pulse width.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL D-TYPE FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT74 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT74 are dual positive-edge triggered, D-type flip-flops with individual data (D) inputs, clock (CP) inputs, set ( $\overline{S}_D$ ) and reset ( $\overline{R}_D$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay nCP to nQ, n $\overline{Q}$ n $\overline{S}_D$ to nQ, n $\overline{Q}$ n $\overline{R}_D$ to nQ, n $\overline{Q}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	15	ns
			15	18	ns
			16	18	ns
f <sub>max</sub>	maximum clock frequency		76	59	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	24	29	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

- CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

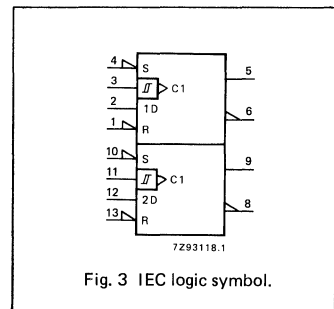
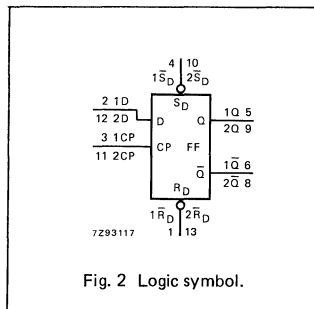
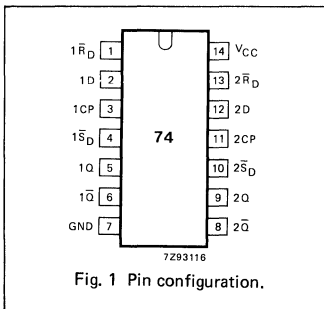
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
- For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

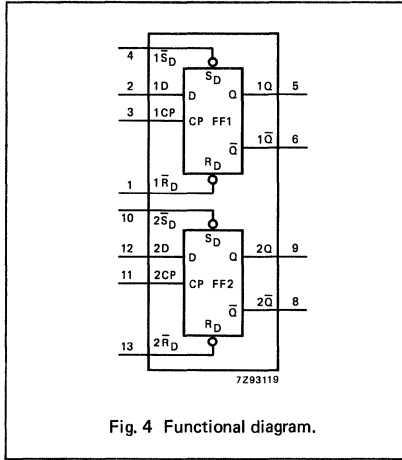
PC74HC/HCT74P: 14-lead DIL; plastic (SOT-27).  
 PC74HC/HCT74T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1 $\overline{R}_D$ , 2 $\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1 $\overline{S}_D$ , 2 $\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1 $\overline{Q}$ , 2 $\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage





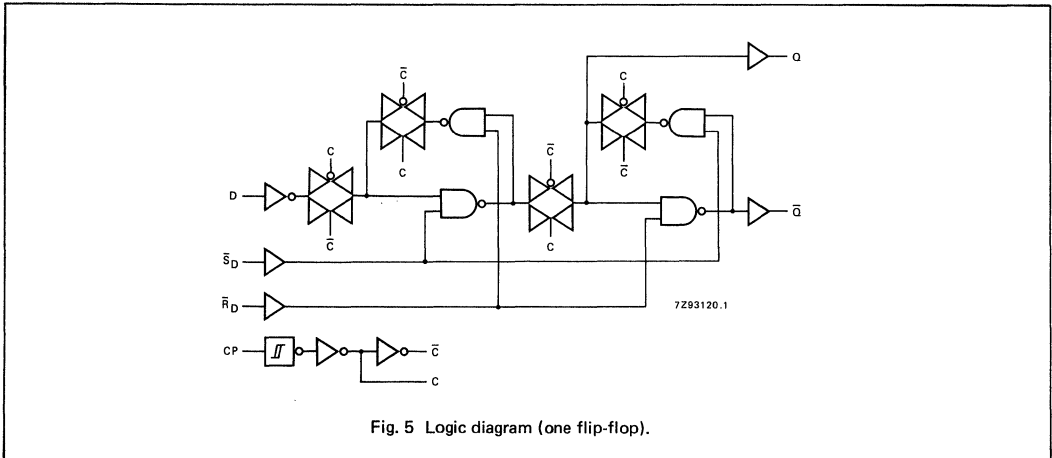


FUNCTION TABLE

INPUTS				OUTPUTS	
$\bar{S}_D$	$\bar{R}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\bar{S}_D$	$\bar{R}_D$	CP	D	$Q_{n+1}$	$\bar{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition  
 $Q_{n+1}$  = state after the next LOW-to-HIGH CP transition



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nS <sub>D</sub> to nQ, nQ̄		50 18 14	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nR <sub>D</sub> to nQ, nQ̄		52 19 15	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	set or reset pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time set or reset	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time nD to nCP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 6
t <sub>h</sub>	hold time nCP to nD	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	23 69 82		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nD	0.70
n $\overline{R}_D$	0.70
n $\overline{S}_D$	0.80
nCP	0.80

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, n $\overline{Q}$		18	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{S}_D$ to nQ, n $\overline{Q}$		21	35		44		53	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{R}_D$ to nQ, n $\overline{Q}$		21	35		44		53	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6
t <sub>W</sub>	set or reset pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time set or reset	6	1		8		9		ns	4.5	
t <sub>su</sub>	set-up time nD to nCP	12	5		15		18		ns	4.5	Fig. 6
t <sub>h</sub>	hold time nCP to nD	3	-3		3		3		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	27	54		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

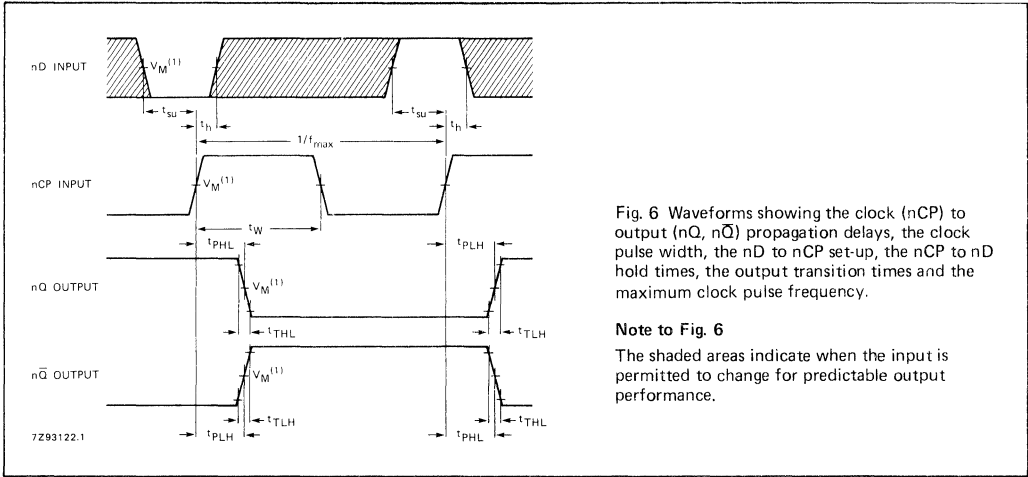


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

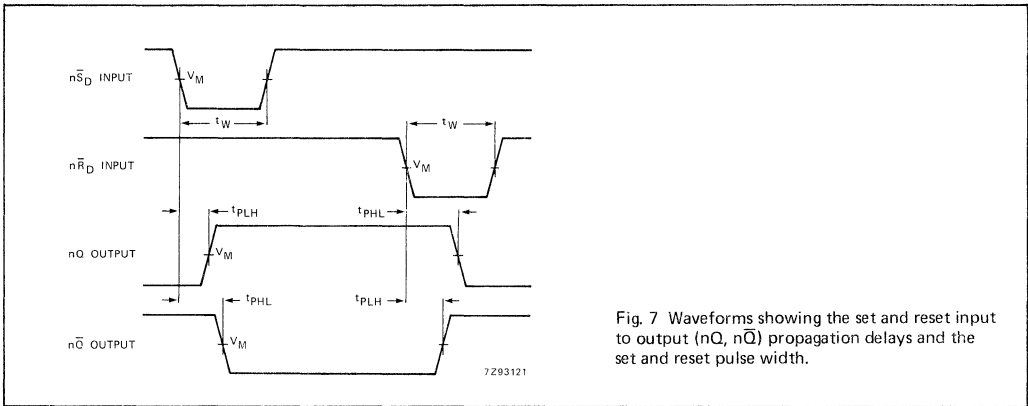


Fig. 7 Waveforms showing the set and reset input to output (nQ, nQ̄) propagation delays and the set and reset pulse width.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND to } 3\text{ V}$ .

**QUAD BISTABLE TRANSPARENT LATCH**

**FEATURES**

- Complementary Q and  $\bar{Q}$  outputs
- VCC and GND on the centre pins
- Output capability: standard
- ICC category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE<sub>1,2</sub> and LE<sub>3,4</sub>). When LE<sub>n-n</sub> is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE<sub>n-n</sub> is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE<sub>n-n</sub> will be stored in the latches. The latched outputs remain stable as long as the LE<sub>n-n</sub> is LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub> , $\bar{Q}_n$ LE <sub>n-n</sub> to Q <sub>n</sub> , $\bar{Q}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11 11	12 11	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT75P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT75T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	1 $\bar{Q}$ to 4 $\bar{Q}$	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE <sub>3,4</sub>	latch enable input, latches 3 and 4 (active HIGH)
5	VCC	positive supply voltage
12	GND	ground (0 V)
13	LE <sub>1,2</sub>	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs

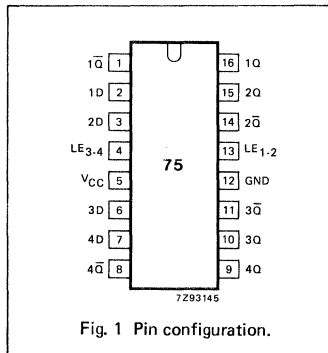


Fig. 1 Pin configuration.

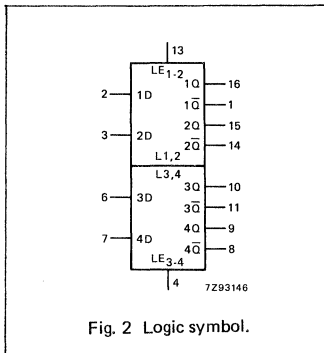


Fig. 2 Logic symbol.

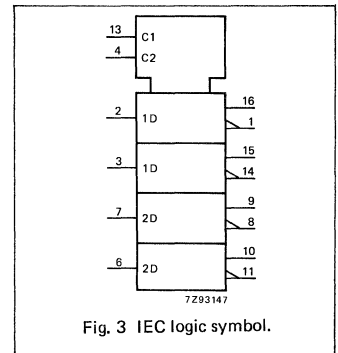


Fig. 3 IEC logic symbol.

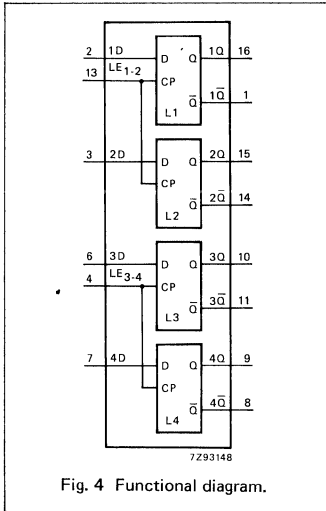


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS		OUTPUTS	
	LE <sub>n-n</sub>	nD	nQ	nQ̄
data enabled	H	L	L	H
data latched	L	X	q	q̄

H = HIGH voltage level  
 L = LOW voltage level  
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH LE<sub>n-n</sub> transition  
 X = don't care

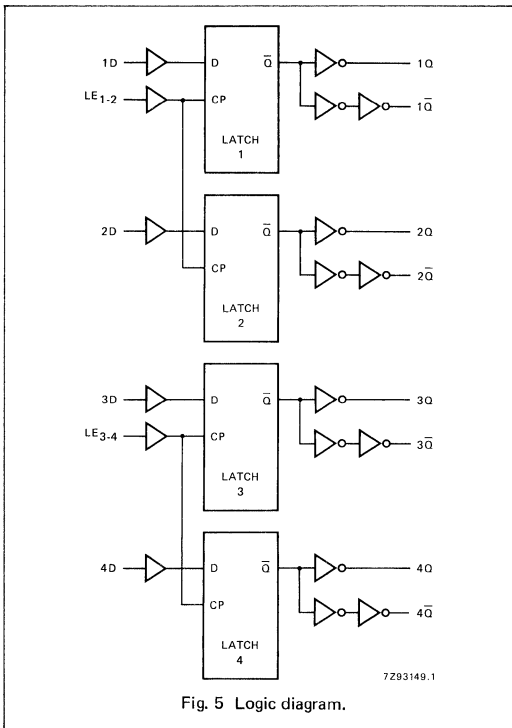


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nD to nQ̄		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE <sub>n-n</sub> to nQ		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE <sub>n-n</sub> to nQ̄		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>W</sub>	enable pulse width HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time nD to LE <sub>n-n</sub>	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t <sub>h</sub>	hold time nD to LE <sub>n-n</sub>	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 9

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nD	0.75
LE <sub>n-n</sub>	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay LE <sub>n-n</sub> to nQ		13	28		35		42	ns	4.5	Fig. 8
$t_{PHL}/t_{PLH}$	propagation delay LE <sub>n-n</sub> to nQ		15	30		38		45	ns	4.5	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
$t_W$	enable pulse width HIGH	16	6		20		24		ns	4.5	Fig. 8
$t_{su}$	set-up time nD to LE <sub>n-n</sub>	12	4		15		18		ns	4.5	Fig. 9
$t_h$	hold time nD to LE <sub>n-n</sub>	3	-2		3		3		ns	4.5	Fig. 9



AC WAVEFORMS

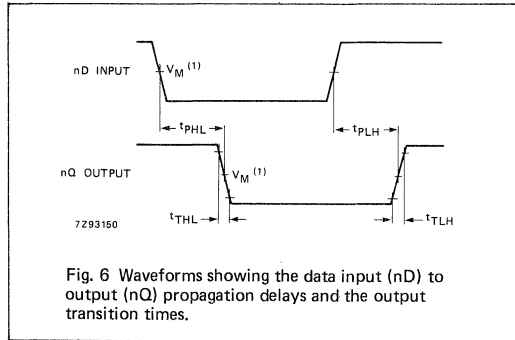


Fig. 6 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

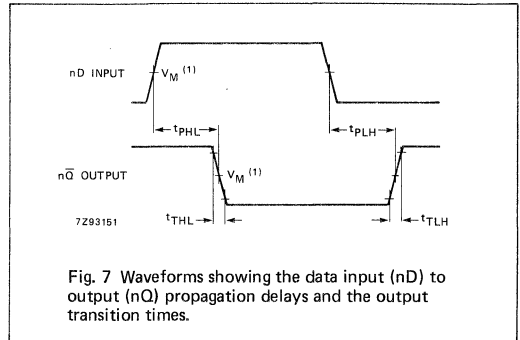


Fig. 7 Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times.

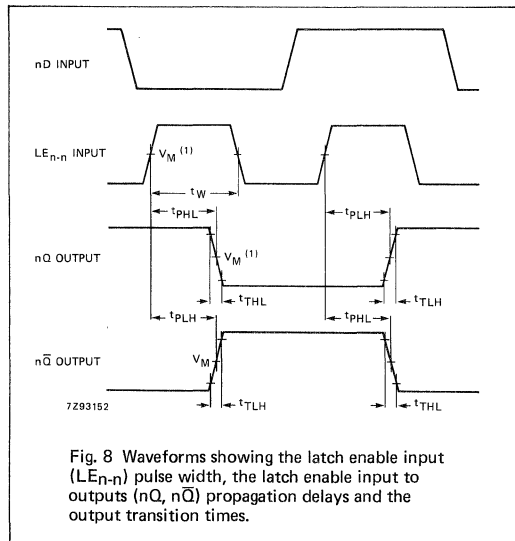


Fig. 8 Waveforms showing the latch enable input ( $LE_{n-n}$ ) pulse width, the latch enable input to outputs (nQ, nQ) propagation delays and the output transition times.

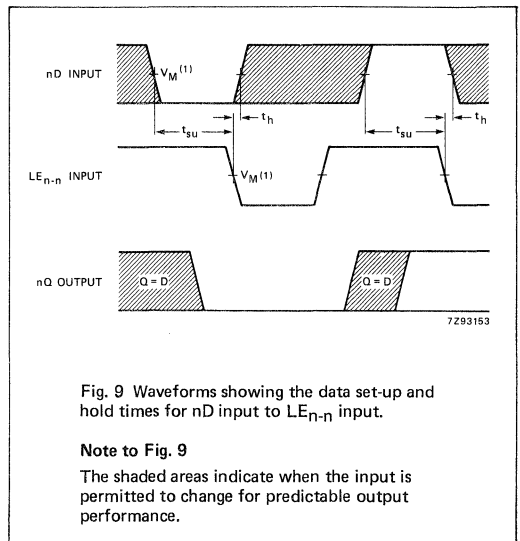


Fig. 9 Waveforms showing the data set-up and hold times for nD input to  $LE_{n-n}$  input.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3\text{V}$ ;  $V_I = \text{GND to } 3\text{V}$ .

## 4-BIT MAGNITUDE COMPARATOR

### FEATURES

- Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs (Q<sub>A>B</sub>, Q<sub>A=B</sub> and Q<sub>A<B</sub>). The 4-bit inputs are weighted (A<sub>0</sub> to A<sub>3</sub> and B<sub>0</sub> to B<sub>3</sub>), where A<sub>3</sub> and B<sub>3</sub> are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs (I<sub>A>B</sub>, I<sub>A=B</sub> and I<sub>A<B</sub>) to the least significant position must be connected as follows: I<sub>A<B</sub> = I<sub>A>B</sub> = LOW and I<sub>A=B</sub> = HIGH.

For words greater than 4-bits, units can be cascaded by connecting outputs Q<sub>A<B</sub>, Q<sub>A>B</sub> and Q<sub>A=B</sub> to the corresponding inputs of the significant comparator.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A&gt;B</sub> , Q <sub>A&lt;B</sub> A <sub>n</sub> , B <sub>n</sub> to Q <sub>A=B</sub> I <sub>A&lt;B</sub> , I <sub>A=B</sub> , I <sub>A&gt;B</sub> to Q <sub>A&lt;B</sub> , Q <sub>A&gt;B</sub> I <sub>A=B</sub> to Q <sub>A=B</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	20	18	ns
			15	20	ns
			13	15	ns
			10	14	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	18	20	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT85P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT85T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	I <sub>A&lt;B</sub>	A < B expansion input
3	I <sub>A=B</sub>	A = B expansion input
4	I <sub>A&gt;B</sub>	A > B expansion input
5	Q <sub>A&gt;B</sub>	A > B output
6	Q <sub>A=B</sub>	A = B output
7	Q <sub>A&lt;B</sub>	A < B output
8	GND	ground (0 V)
9, 11, 14, 1,	B <sub>0</sub> to B <sub>3</sub>	word B inputs
10, 12, 13, 15	A <sub>0</sub> to A <sub>3</sub>	word A inputs
16	V <sub>CC</sub>	positive supply voltage

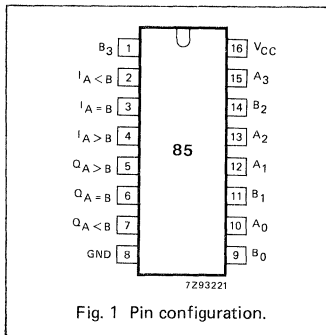


Fig. 1 Pin configuration.

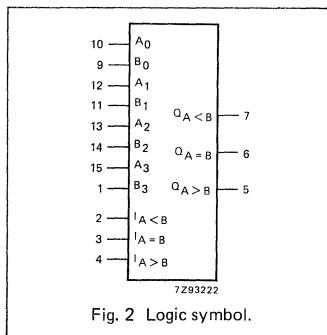


Fig. 2 Logic symbol.

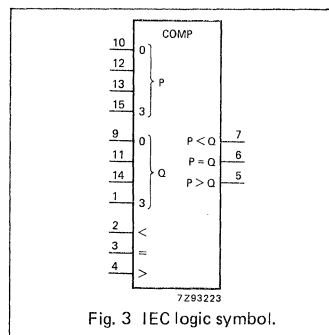


Fig. 3 IEC logic symbol.

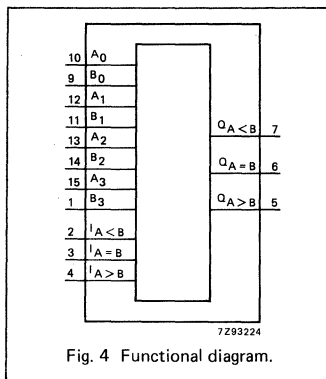


Fig. 4 Functional diagram.

**APPLICATIONS**

- Process controllers
- Servo-motor control

**FUNCTION TABLE**

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A <sub>3</sub> , B <sub>3</sub>	A <sub>2</sub> , B <sub>2</sub>	A <sub>1</sub> , B <sub>1</sub>	A <sub>0</sub> , B <sub>0</sub>	I <sub>A&gt;B</sub>	I <sub>A&lt;B</sub>	I <sub>A=B</sub>	Q <sub>A&gt;B</sub>	Q <sub>A&lt;B</sub>	Q <sub>A=B</sub>
A <sub>3</sub> >B <sub>3</sub>	X	X	X	X	X	X	H	L	L
A <sub>3</sub> <B <sub>3</sub>	X	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> >B <sub>2</sub>	X	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <B <sub>2</sub>	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> >B <sub>1</sub>	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> <B <sub>1</sub>	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> >B <sub>0</sub>	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> <B <sub>0</sub>	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	L	L	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	H	L	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	H	L	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

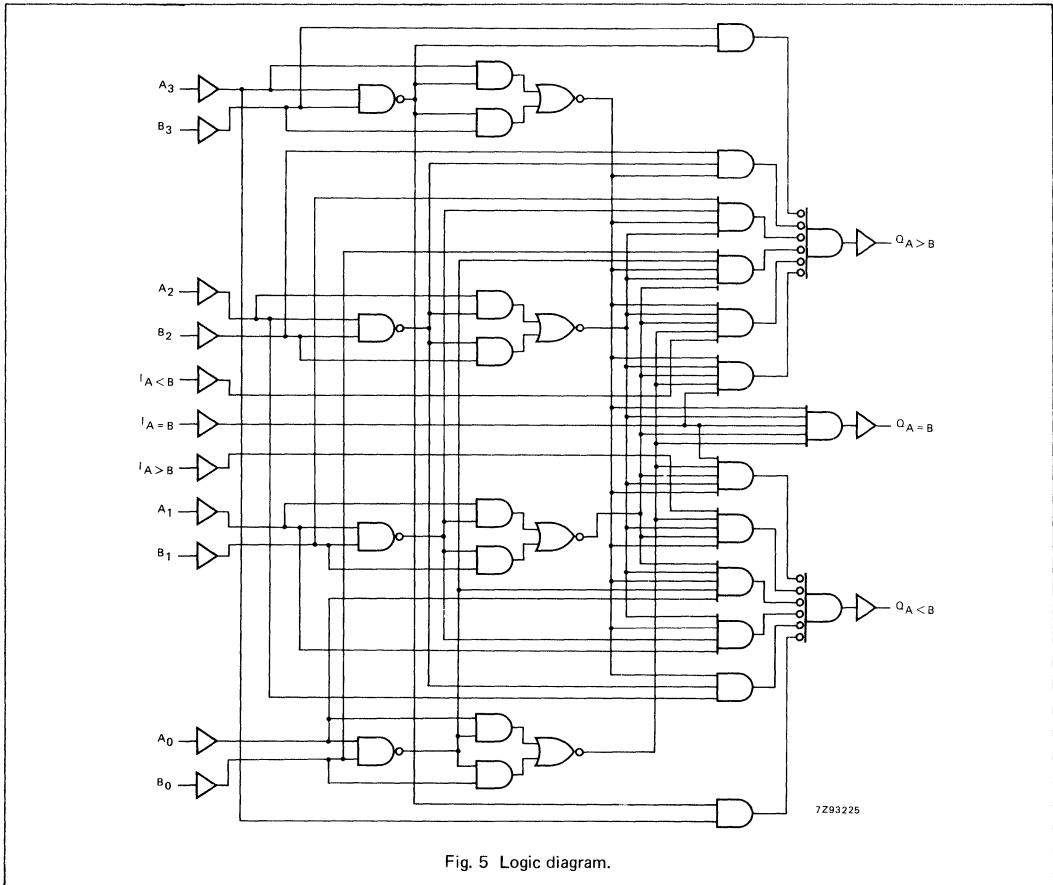


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A</sub> >B or Q <sub>A</sub> <B		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A</sub> =B		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A</sub> <B, I <sub>A</sub> =B, I <sub>A</sub> >B to Q <sub>A</sub> <B, Q <sub>A</sub> >B		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A</sub> =B to Q <sub>A</sub> =B		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below

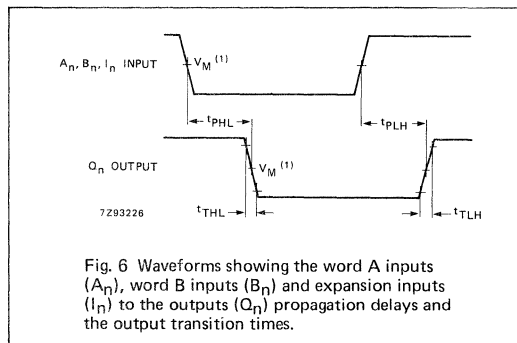
input	unit load coefficient
$I_{A<B}$	1.00
$I_{A>B}$	1.00
$I_{A=B}$	1.50
$A_n, B_n$	1.50

**AC CHARACTERISTICS FOR 74HCT**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $Q_{A>B}$ or $Q_{A<B}$		21	37		46		56	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $A_n, B_n$ to $Q_{A=B}$		23	40		50		60	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $I_{A<B}, I_{A=B}, I_{A>B}$ to $Q_{A<B}, Q_{A>B}$		18	31		39		47	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $I_{A=B}$ to $Q_{A=B}$		17	31		39		47	ns	4.5	Fig. 6
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

## QUAD 2-INPUT EXCLUSIVE-OR GATE

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT86 provide the EXCLUSIVE-OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	14	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

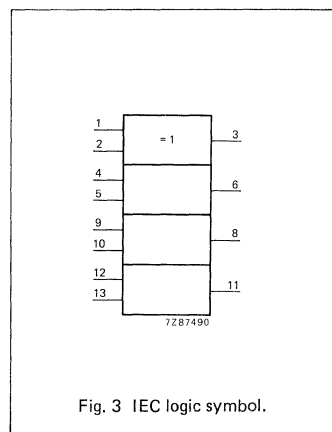
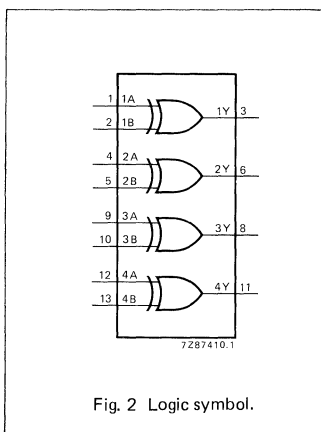
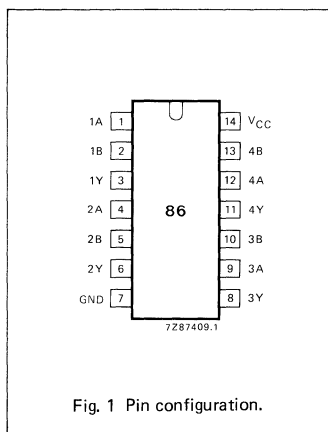
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT86P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT86T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage





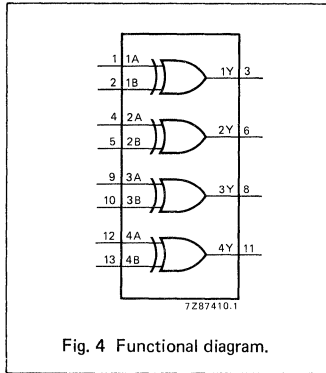


Fig. 4 Functional diagram.

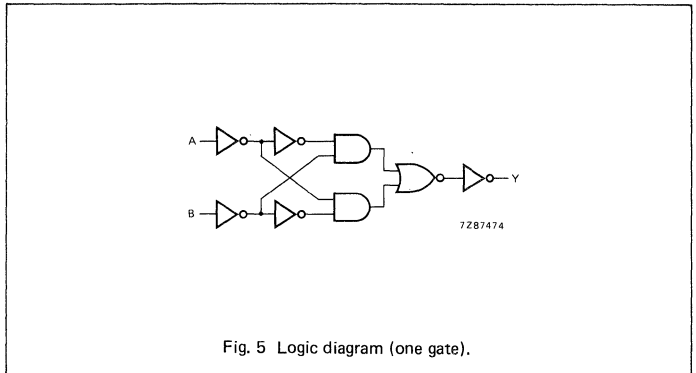


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level  
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay nA, nB to nY		39 14 11	70 24 12		90 18 15		105 21 18	ns	2.0 4.5 6.0	Fig. 6
t <sub>rHL</sub> / t <sub>rLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

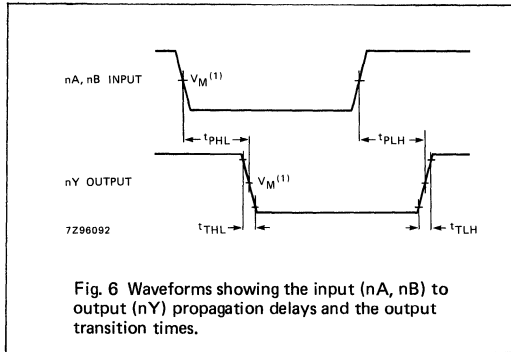
input	unit load coefficient
nA, nB	1.0

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY		17	32		40		48	ns	4.5	Fig. 6
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## 4-BIT BINARY RIPPLE COUNTER

### FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ( $\overline{CP}_0$  and  $\overline{CP}_1$ ) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the  $Q_n$  outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset ( $MR_1$  and  $MR_2$ ) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output  $Q_0$  must be connected externally to input  $\overline{CP}_1$ . The input count pulses are applied to clock input  $\overline{CP}_0$ . Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the  $Q_0, Q_1, Q_2$  and  $Q_3$  outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4 and 8 are available at the  $Q_1, Q_2$  and  $Q_3$  outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

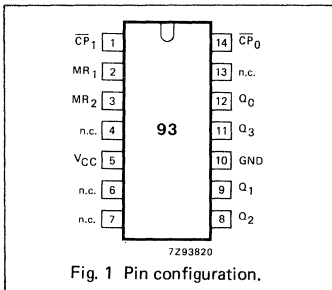


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CP}_0$ to $Q_0$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	12	15	ns
$f_{max}$	maximum clock frequency		100	77	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	22	22	pF

$GND = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT93P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT93T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}_1$	clock input 2 <sup>nd</sup> , 3 <sup>rd</sup> and 4 <sup>th</sup> section (HIGH-to-LOW, edge-triggered)
2, 3	$MR_1, MR_2$	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	$V_{CC}$	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	$Q_0$ to $Q_3$	flip-flop outputs
14	$\overline{CP}_0$	clock input 1 <sup>st</sup> section (HIGH-to-LOW, edge-triggered)

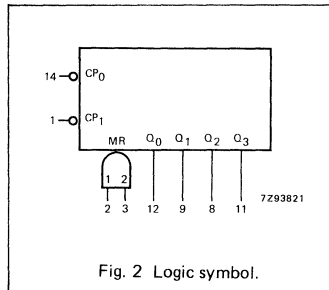


Fig. 2 Logic symbol.

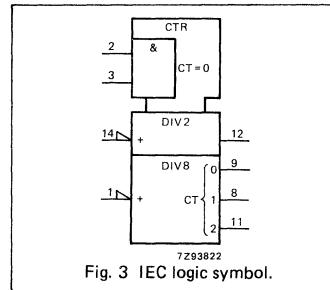


Fig. 3 IEC logic symbol.

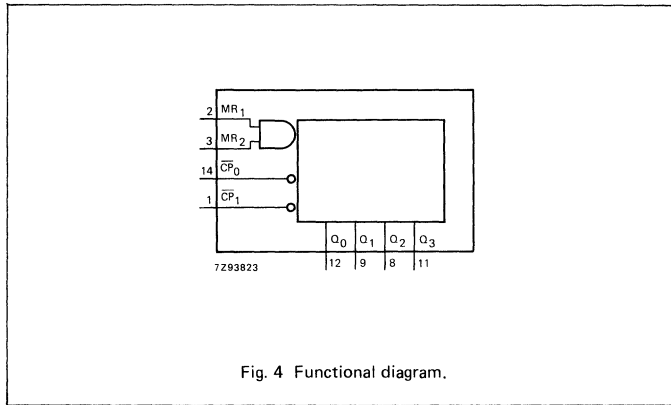


Fig. 4 Functional diagram.

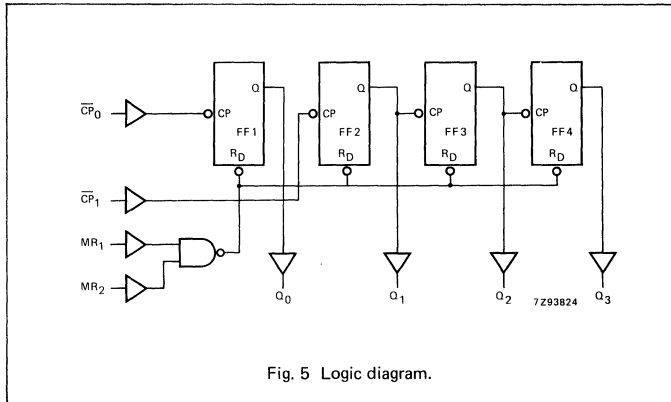


Fig. 5 Logic diagram.

**FUNCTION TABLE**

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

**MODE SELECTION**

RESET INPUTS		OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	L	L	L
L	H				
H	L				
L	L				

count  
count  
count

**Note to function table**  
Output Q<sub>0</sub> connected to  $\overline{CP}_1$ .

H = HIGH voltage level  
L = LOW voltage level

**DC CHARACTERISTICS FOR 74 HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{CP}_0$ to $Q_0$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{CP}_1$ to $Q_1$		49 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{CP}_1$ to $Q_2$		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{CP}_1$ to $Q_3$		80 29 23	245 49 42		305 61 52		370 71 63	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}$	propagation delay $MR_n$ to $Q_n$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
$t_{rem}$	removal time $MR_n$ to $\overline{CP}_0, \overline{CP}_1$	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
$t_W$	pulse width $\overline{CP}_0, \overline{CP}_1$	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
$t_W$	master reset pulse width $MR_n$	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$f_{max}$	maximum clock pulse frequency $\overline{CP}_0, \overline{CP}_1$	6 30 35	30 91 108		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub>-category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_0, \overline{CP}_1$	0.60
$MR_n$	0.40

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}_0$ to Q <sub>0</sub>		18	34		43		51	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}_1$ to Q <sub>1</sub>		18	34		43		51	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}_1$ to Q <sub>2</sub>		24	46		58		69	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}_1$ to Q <sub>3</sub>		30	58		73		87	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR <sub>n</sub> to Q <sub>n</sub>		17	33		41		50	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>rem</sub>	removal time MR <sub>n</sub> to $\overline{CP}_0, \overline{CP}_1$	10	3		13		15		ns	4.5	Fig. 7
t <sub>W</sub>	pulse width $\overline{CP}_0, \overline{CP}_1$	16	7		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width MR <sub>n</sub>	16	5		20		24		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency $\overline{CP}_0, \overline{CP}_1$	30	70		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

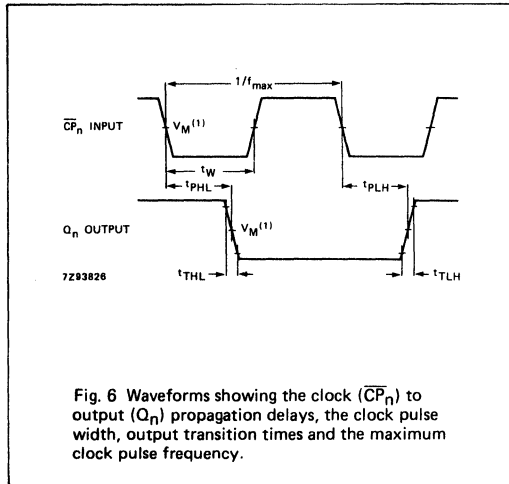


Fig. 6 Waveforms showing the clock ( $\overline{CP}_n$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

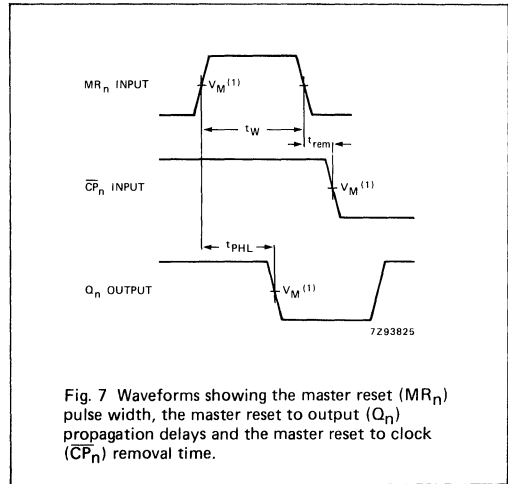


Fig. 7 Waveforms showing the master reset ( $MR_n$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{CP}_n$ ) removal time.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





DUAL JK FLIP-FLOP WITH RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ( $n\overline{CP}$ ) and reset ( $n\overline{R}$ ) inputs; also complementary Q and  $\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $n\overline{R}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the  $\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{CP}$ to $nQ$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	16	16	ns
	$n\overline{CP}$ to $n\overline{Q}$		16	18	ns
	$n\overline{R}$ to $nQ, n\overline{Q}$		15	19	ns
$f_{max}$	maximum clock frequency		74	74	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- $f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

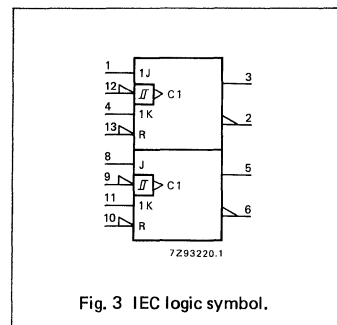
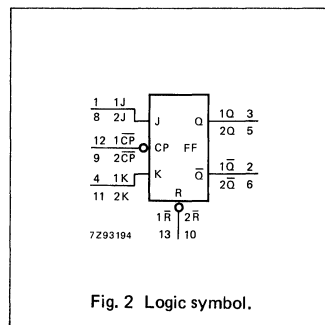
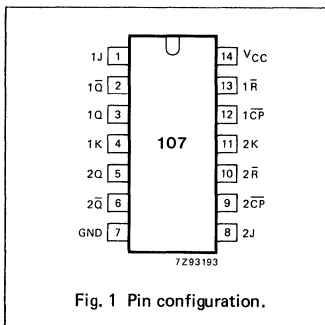
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT107P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT107T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
2, 6	1 $\overline{Q}$ , 2 $\overline{Q}$	complement flip-flop outputs
3, 5	1Q, 2Q	true flip-flop outputs
7	GND	ground (0 V)
12, 9	1 $\overline{CP}$ , 2 $\overline{CP}$	clock input (LOW-to-HIGH, edge-triggered)
13, 10	1 $\overline{R}$ , 2 $\overline{R}$	asynchronous reset inputs (active LOW)
14	V <sub>CC</sub>	positive supply voltage



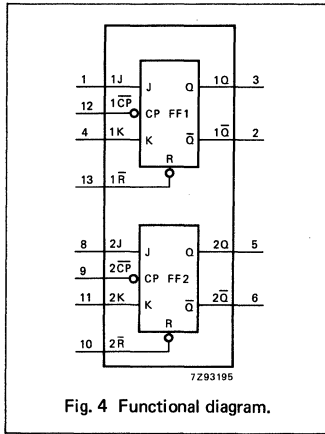


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$n\bar{R}$	$n\bar{CP}$	J	K	Q	$\bar{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\bar{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\bar{q}$

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
X = don't care  
↓ = HIGH-to-LOW CP transition



Fig. 5 Logic diagram (one flip-flop).

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ̄		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nR to nQ, nQ̄		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	reset pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time nR to nCP̄	60 12 10	-22 -8 -6		75 15 13		90 18 15		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time nJ, nK to nCP̄	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 6
t <sub>h</sub>	hold time nJ, nK to nCP̄	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	22 67 80		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nJ, nK	0.35
nR	0.35
nCP	0.35

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ		19	36		45		54	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ̄		21	36		45		54	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nR̄ to nQ, nQ̄		22	38		48		57	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	reset pulse width HIGH or LOW	24	12		30		36		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time nR̄ to nCP̄	12	-6		15		18		ns	4.5	
t <sub>su</sub>	set-up time nJ, nK to nCP̄	20	8		25		30		ns	4.5	Fig. 6
t <sub>h</sub>	hold time nJ, nK to nCP̄	5	0		5		5		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	30	67		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

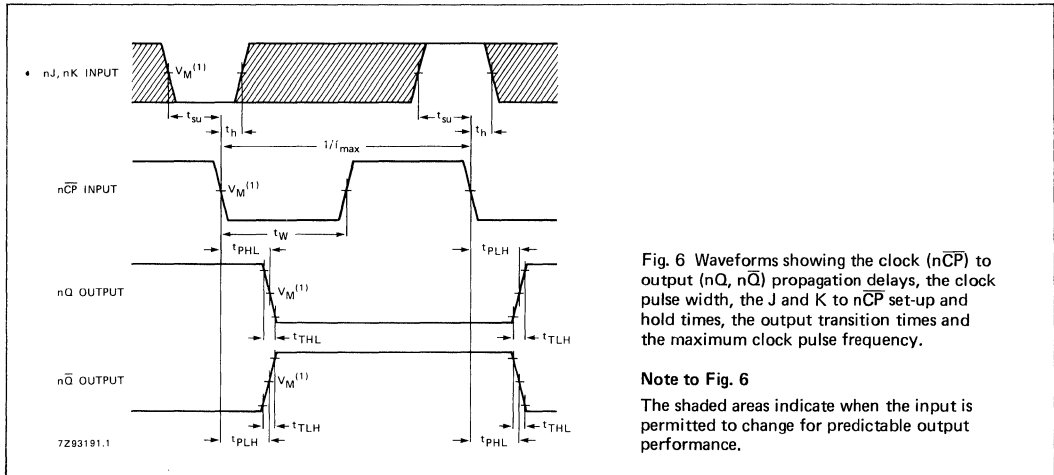


Fig. 6 Waveforms showing the clock ( $n\overline{CP}$ ) to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays, the clock pulse width, the J and K to  $n\overline{CP}$  set-up and hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

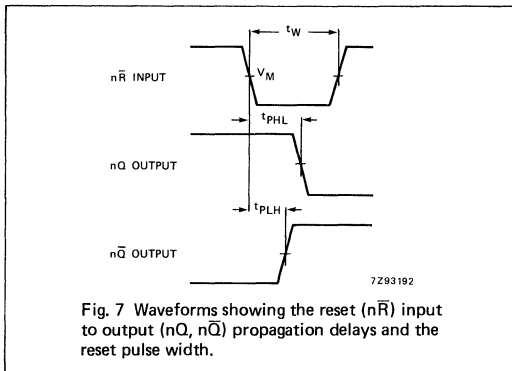


Fig. 7 Waveforms showing the reset ( $n\overline{R}$ ) input to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays and the reset pulse width.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL JK FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, K inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard
- I<sup>CC</sup> category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT109 are dual positive-edge triggered, JK flip-flops with individual J, K inputs, clock (CP) inputs, set (S<sub>D</sub>) and reset (R<sub>D</sub>) inputs; also complementary Q and Q outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and K inputs control the state changes of the flip-flops as described in the mode select function table.

The J and K inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The JK design allows operation as a D-type flip-flop by tying the J and K inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄ nS <sub>D</sub> to nQ, nQ̄ nR <sub>D</sub> to nQ, nQ̄	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	17	ns
			11	14	ns
			11	14	ns
f <sub>max</sub>	maximum clock frequency		75	61	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

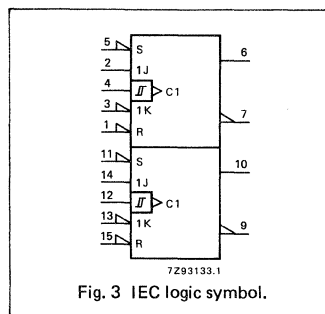
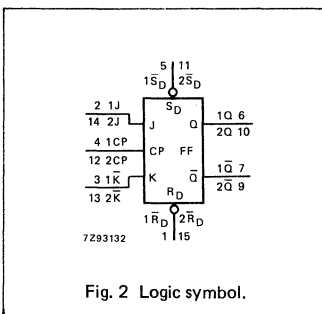
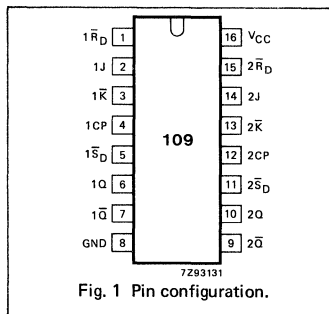
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT109P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT109T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1R <sub>D</sub> , 2R <sub>D</sub>	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1S <sub>D</sub> , 2S <sub>D</sub>	asynchronous set-direct input (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1Q̄, 2Q̄	complement flip-flop outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage



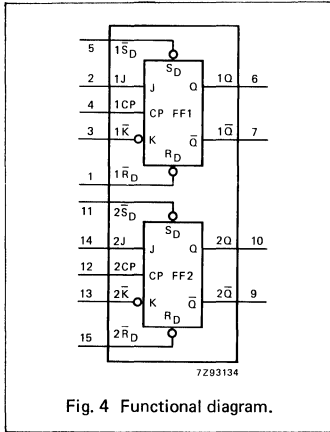


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\bar{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	L
hold "no change"	H	H	↑	l	h	q	$\bar{q}$

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition

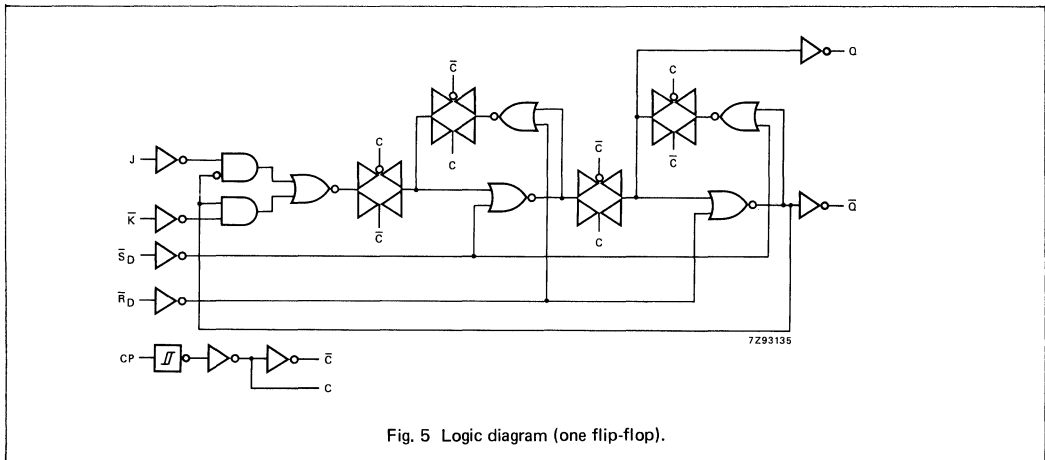


Fig. 5 Logic diagram (one flip-flop).



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: flip-flops

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay nS <sub>D</sub> to nQ		30 11 9	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t <sub>PLH</sub>	propagation delay nS <sub>D</sub> to nQ̄		41 15 12	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub>	propagation delay nR <sub>D</sub> to nQ		41 15 12	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t <sub>PLH</sub>	propagation delay nR <sub>D</sub> to nQ̄		39 14 11	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	set or reset pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time nS <sub>D</sub> , nR <sub>D</sub> to nCP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time nJ, nK̄ to nCP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t <sub>h</sub>	hold time nJ, nK̄ to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	22 68 81		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

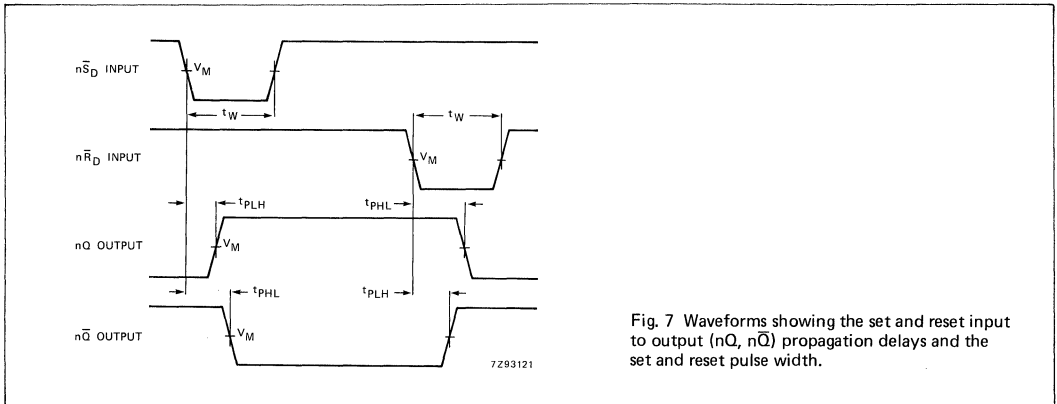
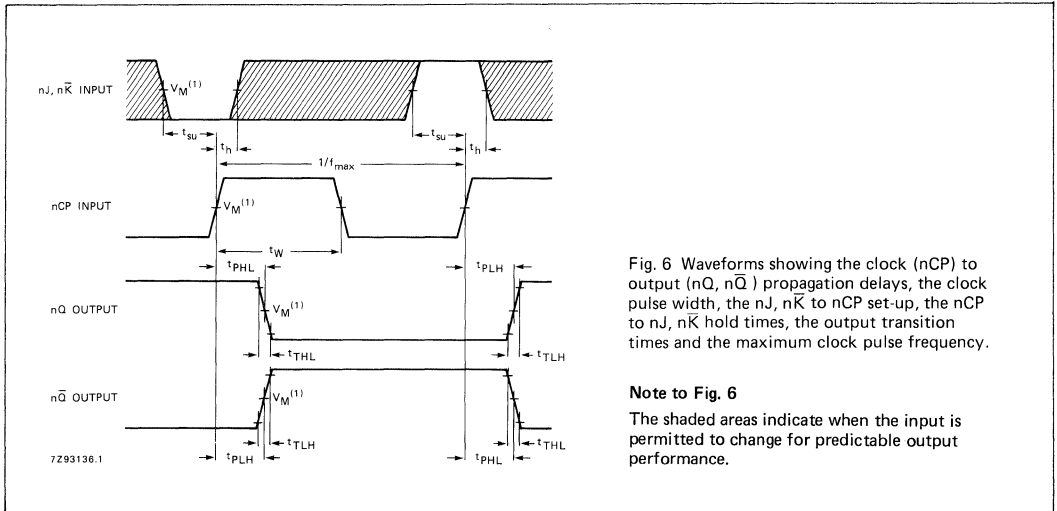
input	unit load coefficient
nJ, nK̄	0.35
nR̄D	0.35
nSD	0.35
nCP	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄		20	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay nSD to nQ		13	26		33		39	ns	4.5	Fig. 7
t <sub>PLH</sub>	propagation delay nSD to nQ̄		19	35		44		53	ns	4.5	Fig. 7
t <sub>PHL</sub>	propagation delay nRD to nQ		19	35		44		53	ns	4.5	Fig. 7
t <sub>PLH</sub>	propagation delay nRD to nQ̄		16	32		40		48	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6
t <sub>W</sub>	set or reset pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time nSD, nRD to nCP	16	8		20		24		ns	4.5	
t <sub>su</sub>	set-up time nJ, nK̄ to nCP	18	8		23		27		ns	4.5	Fig. 6
t <sub>h</sub>	hold time nJ, nK̄ to nCP	3	-3		3		3		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL JK FLIP-FLOP WITH SET AND RESET; NEGATIVE-EDGE TRIGGER

FEATURES

- Asynchronous set and reset
- Output capability: standard
- I<sub>CC</sub> category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT112 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT112 are dual negative-edge triggered JK-type flip-flops featuring individual nJ, nK, clock (nCP), set (nSD) and reset (nRD) inputs. The set and reset inputs, when LOW, set or reset the outputs as shown in the function table regardless of the levels at the other inputs.

A HIGH level at the clock (nCP) input enables the nJ and nK inputs and data will be accepted. The nJ and nK inputs control the state changes of the flip-flops as shown in the function table. The nJ and nK inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Output state changes are initiated by the HIGH-to-LOW transition of nCP.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ, nQ̄ nSD to nQ, nQ̄ nRD to nQ, nQ̄	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
			15	15	ns
			18	19	ns
f <sub>max</sub>	maximum clock frequency		66	70	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	27	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

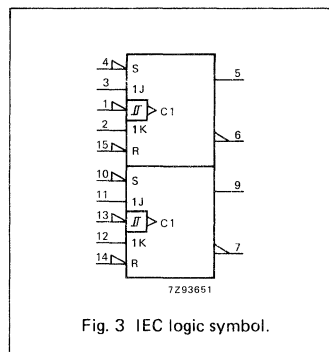
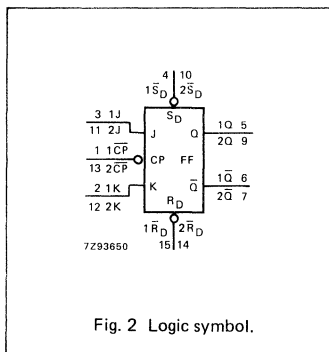
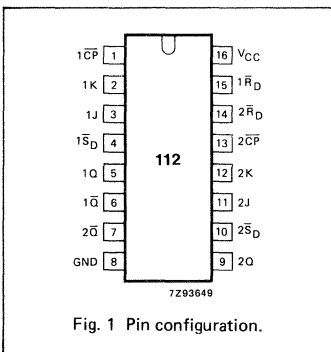
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT112P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT112T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1CP, 2CP	clock input (HIGH-to-LOW, edge triggered)
2, 12	1K, 2K	data inputs; flip-flops 1 and 2
3, 11	1J, 2J	data inputs; flip-flops 1 and 2
4, 10	1SD, 2SD	set inputs (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 7	1Q̄, 2Q̄	complement flip-flop outputs
8	GND	ground (0 V)
15, 14	1RD, 2RD	reset inputs (active LOW)
16	V <sub>CC</sub>	positive supply voltage



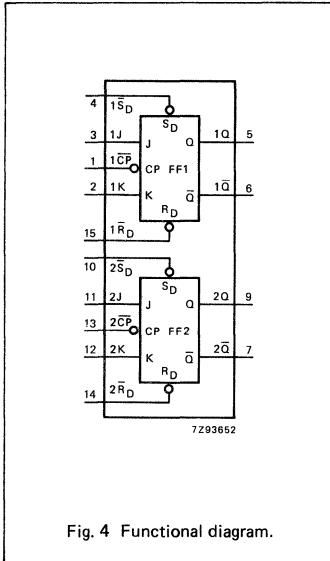


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	nS <sub>D</sub>	nR <sub>D</sub>	nCP	nJ	nK	nQ	nQ̄
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↓	h	h	q̄	q
load "0" (reset)	H	H	↓	l	h	L	H
load "1" (set)	H	H	↓	h	l	H	L
hold "no change"	H	H	↓	l	l	q	q̄

Note to function table

Both outputs will be HIGH while both nS<sub>D</sub> and nR<sub>D</sub> are LOW, but the output states are unpredictable if nS<sub>D</sub> and nR<sub>D</sub> go HIGH simultaneously.

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition

X = don't care

↓ = HIGH-to-LOW CP transition

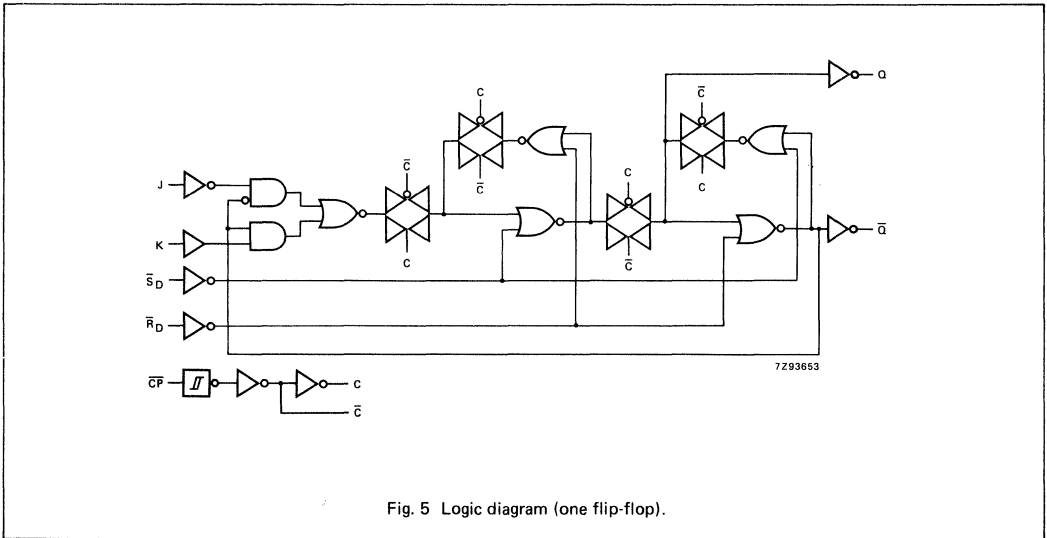


Fig. 5 Logic diagram (one flip-flop).

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: flip-flops

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{CP}$ to $nQ$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{CP}$ to $n\overline{Q}$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{RD}$ to $nQ$ , $n\overline{Q}$		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{SD}$ to $nQ$ , $n\overline{Q}$		50 18 14	155 31 26		295 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
$t_W$	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
$t_W$	set or reset pulse width LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_{rem}$	removal time $n\overline{RD}$ to $n\overline{CP}$	80 16 14	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
$t_{rem}$	removal time $n\overline{SD}$ to $n\overline{CP}$	80 16 14	-19 -7 -6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_{su}$	set-up time $nJ$ , $nK$ to $n\overline{CP}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
$t_h$	hold time $nJ$ , $nK$ to $n\overline{CP}$	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 6
$f_{max}$	maximum clock pulse frequency	6 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: flip-flops

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1 $\overline{S}_D$ , 2 $\overline{S}_D$	0.5
1K, 2K	0.6
1 $\overline{R}_D$ , 2 $\overline{R}_D$	0.65
1J, 2J	1
1 $\overline{CP}$ , 2 $\overline{CP}$	1

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{CP}$ to nQ		21	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{CP}$ to n $\overline{Q}$		23	40		50		60	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{R}_D$ to nQ, n $\overline{Q}$		22	37		46		56	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{S}_D$ to nQ, n $\overline{Q}$		18	32		40		48	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	set or reset pulse width LOW	18	10		23		27		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time n $\overline{R}_D$ to n $\overline{CP}$	20	11		25		30		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time n $\overline{S}_D$ to n $\overline{CP}$	20	-8		25		30		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time nJ, nK to n $\overline{CP}$	16	7		20		24		ns	4.5	Fig. 6
t <sub>h</sub>	hold time nJ, nK to n $\overline{CP}$	0	-7		0		0		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	27	64		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

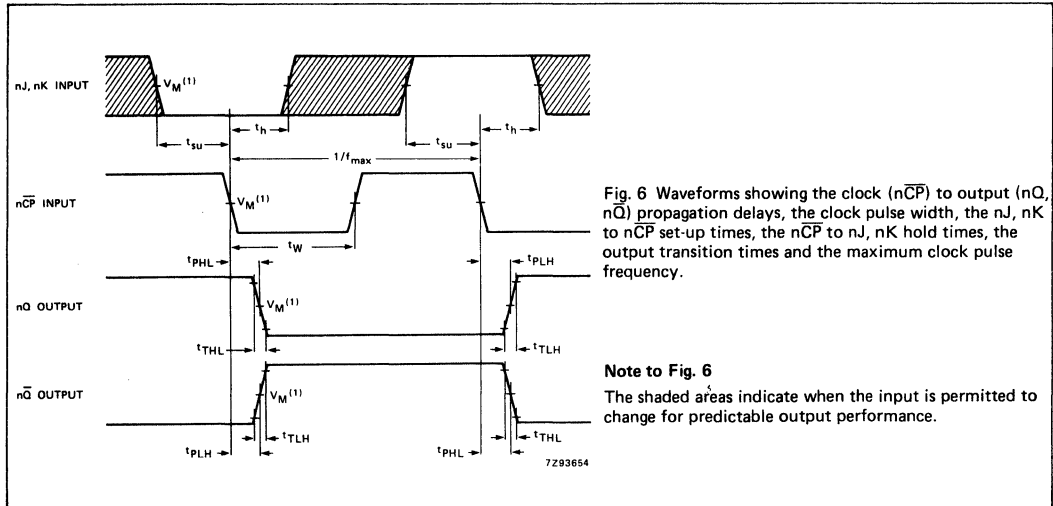


Fig. 6 Waveforms showing the clock ( $n\overline{CP}$ ) to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays, the clock pulse width, the  $nJ$ ,  $nK$  to  $n\overline{CP}$  set-up times, the  $n\overline{CP}$  to  $nJ$ ,  $nK$  hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

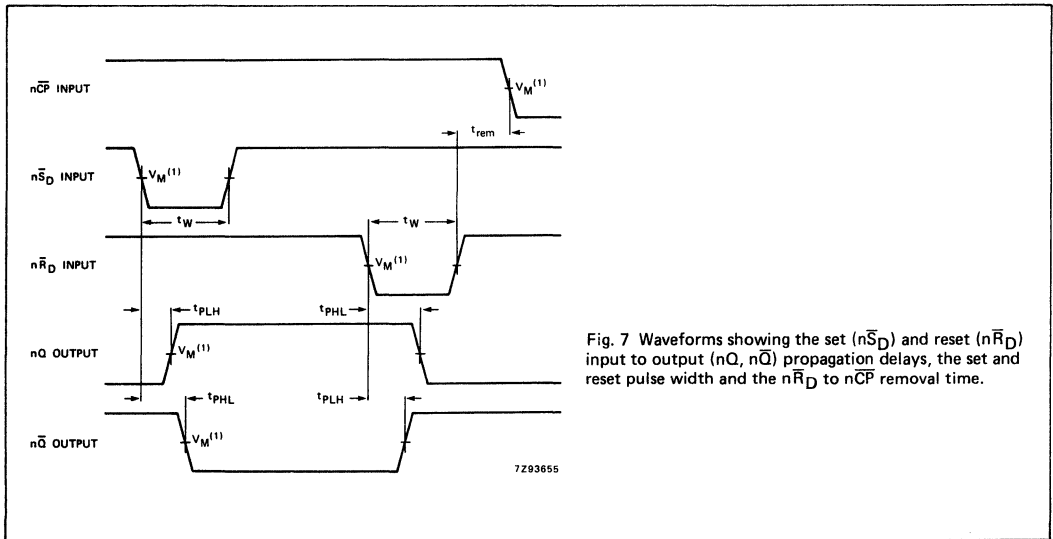


Fig. 7 Waveforms showing the set ( $n\overline{SD}$ ) and reset ( $n\overline{RD}$ ) input to output ( $nQ$ ,  $n\overline{Q}$ ) propagation delays, the set and reset pulse width and the  $n\overline{RD}$  to  $n\overline{CP}$  removal time.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3\text{V}$ ;  $V_I = \text{GND to } 3\text{V}$ .





DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR<sub>EXT</sub>/C<sub>EXT</sub>)
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R<sub>EXT</sub>) and capacitor (C<sub>EXT</sub>). The external resistor and capacitor are normally connected as shown in Fig. 6. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input (nA) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, nQ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input nR<sub>D</sub>, which also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nQ, nQ nR <sub>D</sub> to nQ, nQ	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V R <sub>EXT</sub> = 5 kΩ C <sub>EXT</sub> = 0 pF	26 20	26 23	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
t <sub>W</sub>	minimum output pulse width nQ, nQ		75	75	ns

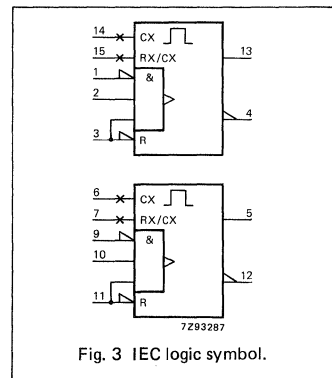
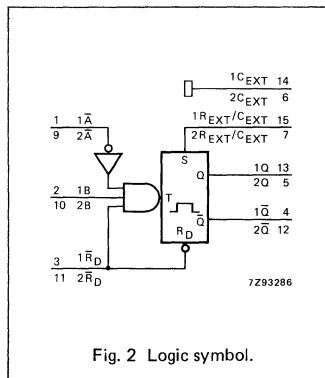
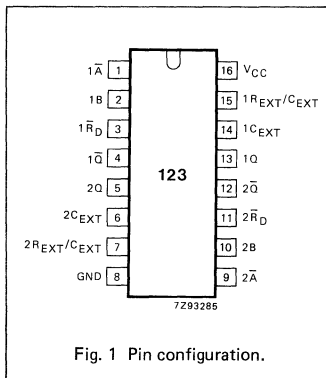
GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT123P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT123T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	1R <sub>D</sub> , 2R <sub>D</sub>	direct reset LOW and trigger action at positive edge
4, 12	1Q, 2Q	outputs (active LOW)
7	2R <sub>EXT</sub> /C <sub>EXT</sub>	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	1C <sub>EXT</sub> , 2C <sub>EXT</sub>	external capacitor connection
15	1R <sub>EXT</sub> /C <sub>EXT</sub>	external resistor/capacitor connection
16	V <sub>CC</sub>	positive supply voltage



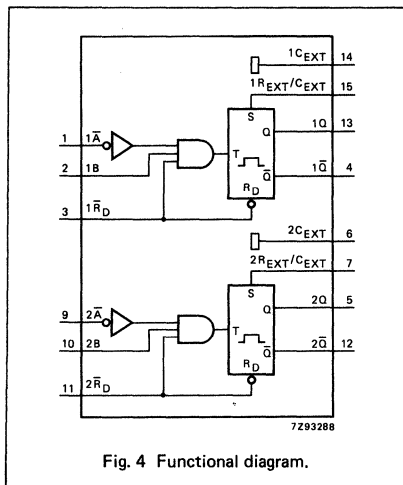


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

An internal connection from  $n\bar{R}_D$  to the input gates makes it possible to trigger the circuit by a positive-going signal at input  $n\bar{R}_D$  as shown in the function table. Figures 7 and 8 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components  $R_{EXT}$  and  $C_{EXT}$ . For pulse widths, when  $C_{EXT} < 10\,000\text{ pF}$ , see Fig. 9.

When  $C_{EXT} > 10\,000\text{ pF}$ , the typical output pulse width is defined as:

$$t_W = 0.45 \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

where,  $t_W$  = pulse width in ns;

$R_{EXT}$  = external resistor in  $k\Omega$ ;

$C_{EXT}$  = external capacitor in pF.

Schmitt-trigger action in the  $n\bar{A}$  and  $nB$  inputs, makes the circuit highly tolerant to slower input rise and fall times.

**FUNCTION TABLE**

INPUTS			OUTPUTS	
$n\bar{R}_D$	$n\bar{A}$	$nB$	$nQ$	$n\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

H = HIGH voltage level

L = LOW voltage level

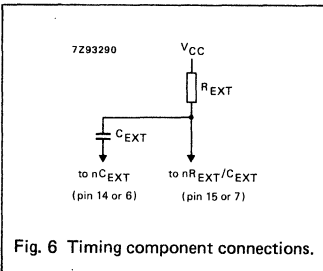
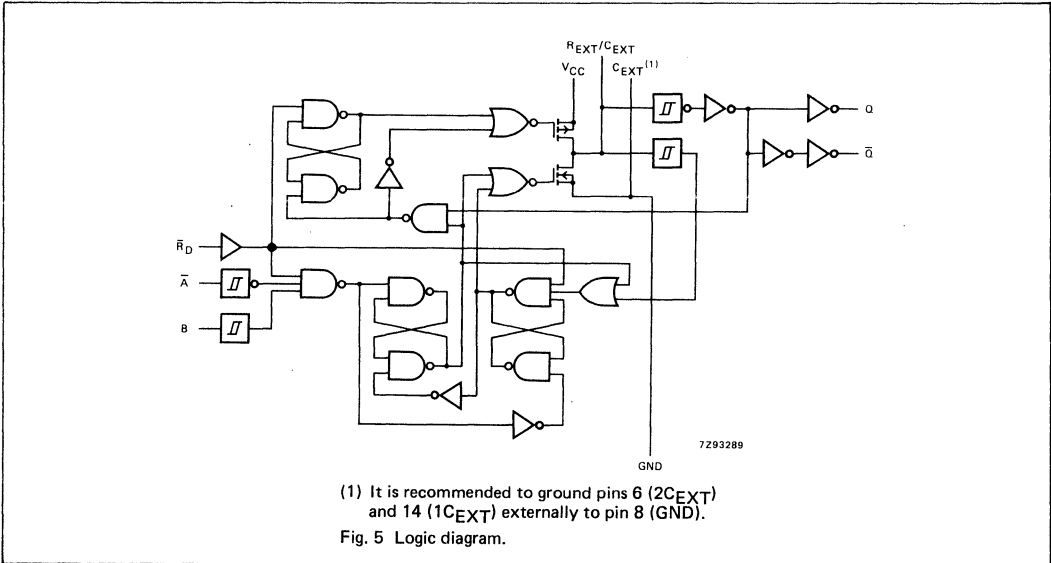
X = don't care

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

= one HIGH level output pulse

= one LOW level output pulse



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nREXT/CEXT)

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS/NOTES	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub>	propagation delay nR <sub>D</sub> , nA, nB to nQ		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ
t <sub>PLH</sub>	propagation delay nR <sub>D</sub> , nA, nB to nQ		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ
t <sub>PHL</sub>	propagation delay nR <sub>D</sub> to nQ		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ
t <sub>PLH</sub>	propagation delay nR <sub>D</sub> to nQ		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
t <sub>W</sub>	trigger pulse width nA = LOW	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	trigger pulse width nB = HIGH	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	reset pulse width nR <sub>D</sub> = LOW	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	output pulse width nQ = HIGH nQ = LOW		450		—		—		μs	5.0	C <sub>EXT</sub> = 100 nF; R <sub>EXT</sub> = 10 kΩ; Figs 7 and 8
t <sub>W</sub>	output pulse width nQ = HIGH nQ = LOW		75		—		—		ns	5.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ; note 1; Figs 7 and 8
t <sub>rt</sub>	retrigger time nA, nB		44		—		—		ns	5.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 kΩ; note 2; Fig. 8
R <sub>EXT</sub>	external timing resistor	10 2		1000 100	—		—		kΩ	2.0 5.0	Fig. 9
C <sub>EXT</sub>	external timing capacitor				no limits				pF	5.0	Fig. 9; note 3

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for nREXT/CEXT)

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
n $\bar{A}$ , nB	0.35
n $\bar{R}_D$	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS/NOTES	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub>	propagation delay n $\bar{R}_D$ , n $\bar{A}$ , nB to n $\bar{Q}$		30	51		64		77	ns	4.5	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$
t <sub>PLH</sub>	propagation delay n $\bar{R}_D$ , n $\bar{A}$ , nB to nQ		30	51		64		77	ns	4.5	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$
t <sub>PHL</sub>	propagation delay n $\bar{R}_D$ to nQ		27	46		58		69	ns	4.5	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$
t <sub>PLH</sub>	propagation delay n $\bar{R}_D$ to n $\bar{Q}$		27	46		58		69	ns	4.5	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	
t <sub>W</sub>	trigger pulse width n $\bar{A}$ = LOW	20	7		25		30		ns	4.5	Fig. 7
t <sub>W</sub>	trigger pulse width nB = HIGH	20	7		25		30		ns	4.5	Fig. 7
t <sub>W</sub>	reset pulse width n $\bar{R}_D$ = LOW	20	8		25		30		ns	4.5	Fig. 8
t <sub>W</sub>	output pulse width n $\bar{Q}$ = HIGH n $\bar{Q}$ = LOW		450		-		-		$\mu$ s	5.0	C <sub>EXT</sub> = 100 nF; R <sub>EXT</sub> = 10 k $\Omega$ ; Figs 7 and 8
t <sub>W</sub>	output pulse width nQ = HIGH n $\bar{Q}$ = LOW		75		-		-		ns	5.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$ ; note 1; Figs 7 and 8
t <sub>rt</sub>	retrigger time n $\bar{A}$ , nB		40		-		-		ns	5.0	C <sub>EXT</sub> = 0 pF; R <sub>EXT</sub> = 5 k $\Omega$ ; note 2; Fig. 8
R <sub>EXT</sub>	external timing resistor	2		100	-		-		k $\Omega$	5.0	Fig. 9
C <sub>EXT</sub>	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

Notes to AC characteristics

1. For other  $R_{EXT}$  and  $C_{EXT}$  combinations see Fig. 9.

If  $C_{EXT} > 10$  nF, the next formula is valid:

$$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

where,  $t_W$  = output pulse width in ns;

$R_{EXT}$  = external resistor in  $k\Omega$ ;  $C_{EXT}$  = external capacitor in pF;

$K$  = constant = 0.45 for  $V_{CC} = 5.0$  V and 0.48 for  $V_{CC} = 2.0$  V.

The inherent test jig and pin capacitance at pins 15 and 7 ( $nR_{EXT}/C_{EXT}$ ) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of  $R_{EXT}$  and  $C_{EXT}$ .

The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If  $C_{EXT} > 10$  nF, the next formula (at  $V_{CC} = 5.0$  V) for the set-up time of a retrigger pulse is valid:

$$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

where,  $t_{rt}$  = retrigger time in ns;

$C_{EXT}$  = external capacitor in pF;

$R_{EXT}$  = external resistor in  $k\Omega$ .

The inherent test jig and pin capacitance at pins 15 and 7 ( $nR_{EXT}/C_{EXT}$ ) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when  $C_{EXT} < 50$  pF.

AC WAVEFORMS

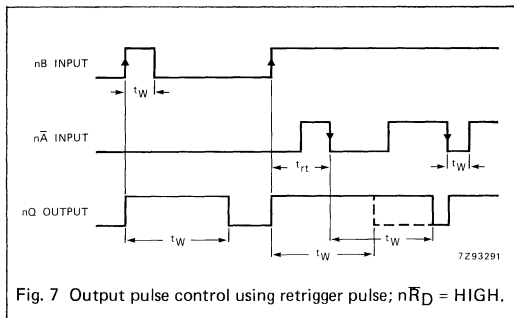


Fig. 7 Output pulse control using retrigger pulse;  $n\bar{R}_D = \text{HIGH}$ .

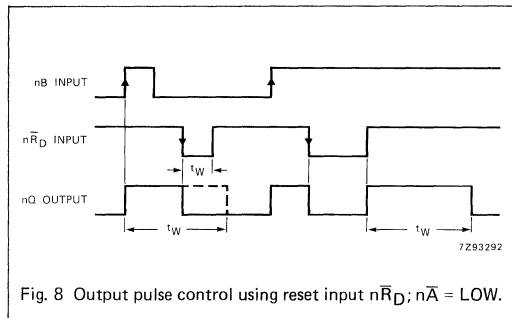


Fig. 8 Output pulse control using reset input  $n\bar{R}_D$ ;  $n\bar{A} = \text{LOW}$ .

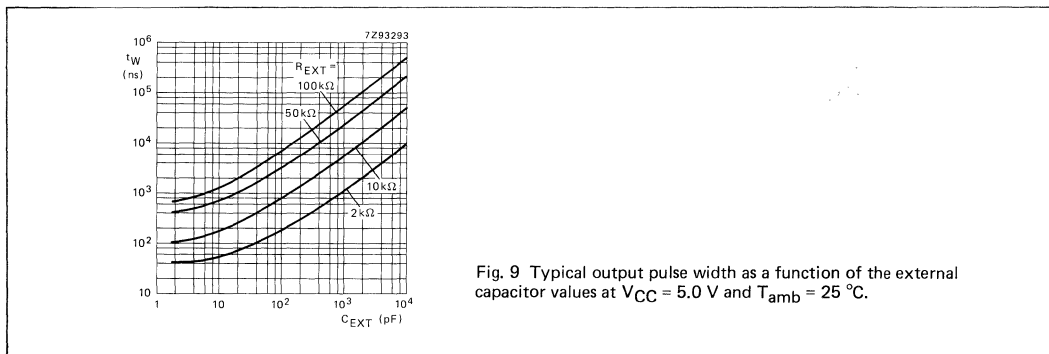


Fig. 9 Typical output pulse width as a function of the external capacitor values at  $V_{CC} = 5.0$  V and  $T_{amb} = 25^\circ\text{C}$ .





**QUAD BUFFER/LINE DRIVER; 3-STATE**

**FEATURES**

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	12	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

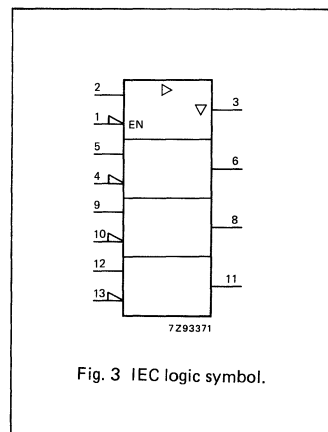
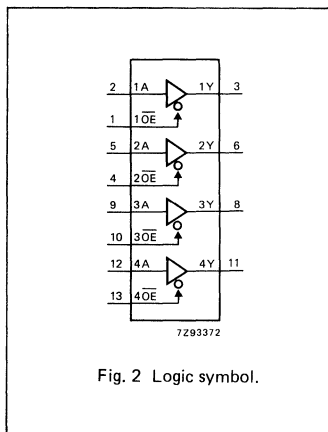
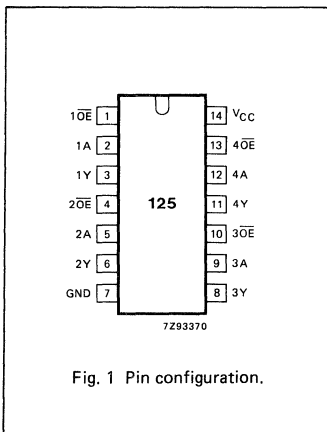
**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT125P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT125T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



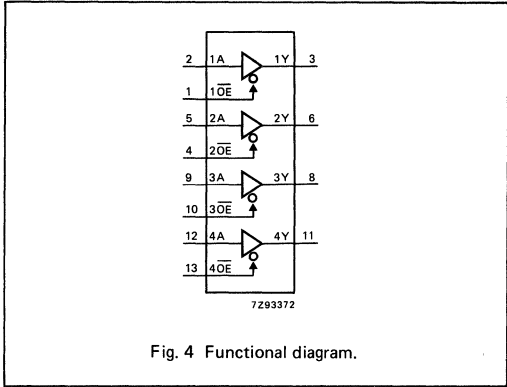


Fig. 4 Functional diagram.

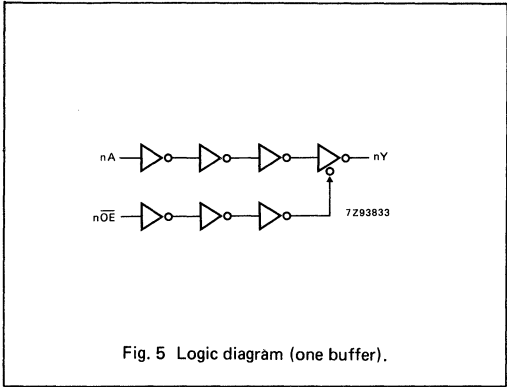


Fig. 5 Logic diagram (one buffer).

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{nOE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>pZH</sub> / t <sub>pZL</sub>	3-state output enable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

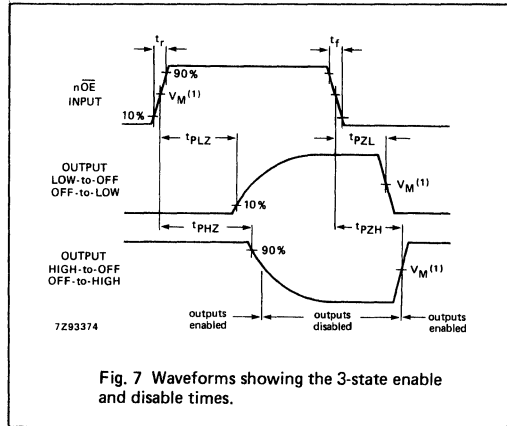
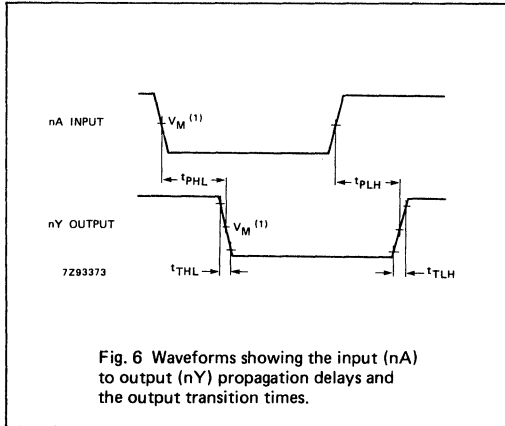
INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay nA to nY		15	26		33		39	ns	4.5	Fig. 6
t <sub>pZH</sub> / t <sub>pZL</sub>	3-state output enable time nOE to nY		15	28		35		42	ns	4.5	Fig. 7
t <sub>pHZ</sub> / t <sub>pLZ</sub>	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**QUAD BUFFER/LINE DRIVER; 3-STATE**

**FEATURES**

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	23	24	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT126P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT126T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

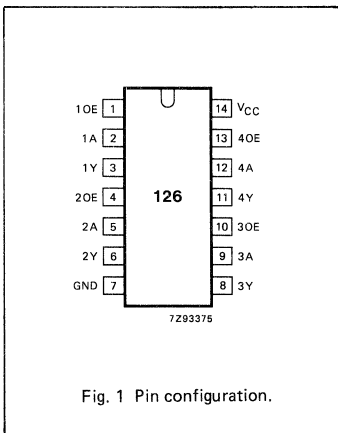


Fig. 1 Pin configuration.

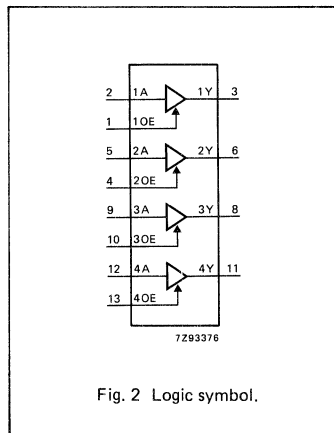


Fig. 2 Logic symbol.

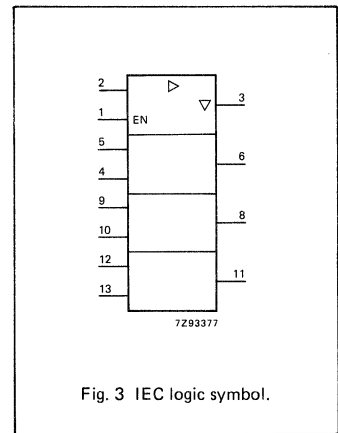
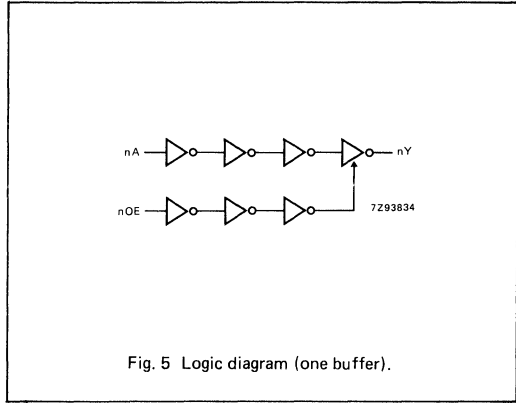
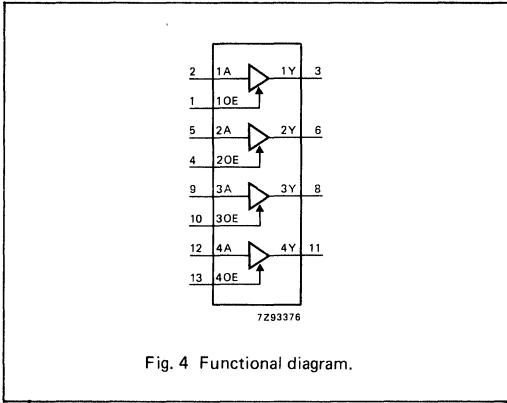


Fig. 3 IEC logic symbol.



**FUNCTION TABLE**

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		14	24		30		36	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		13	25		31		38	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		18	28		35		42	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

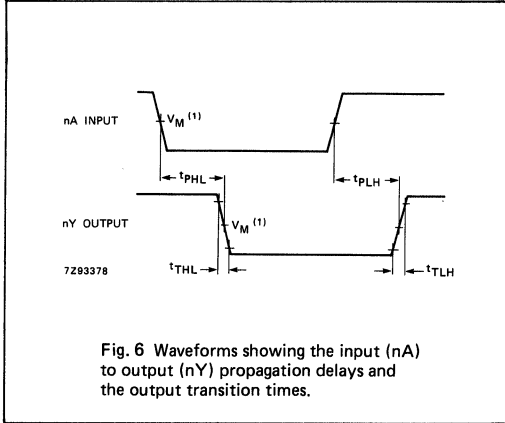


Fig. 6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

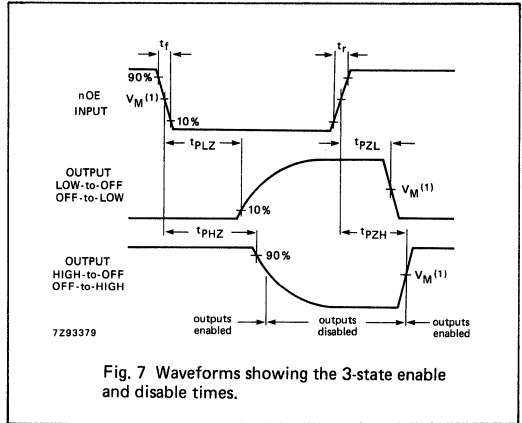


Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## QUAD 2-INPUT NAND SCHMITT TRIGGER

### FEATURES

- Output capability: standard
- ICC category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the hysteresis voltage  $V_H$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	11	17	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	24	20	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT132P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT132T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	$V_{CC}$	positive supply voltage

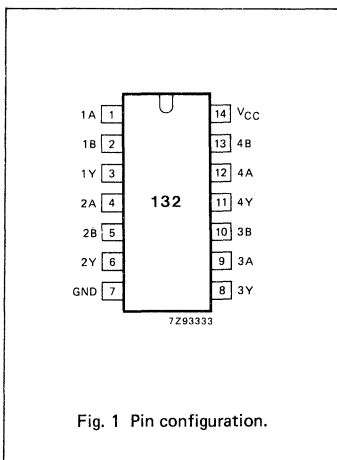


Fig. 1 Pin configuration.

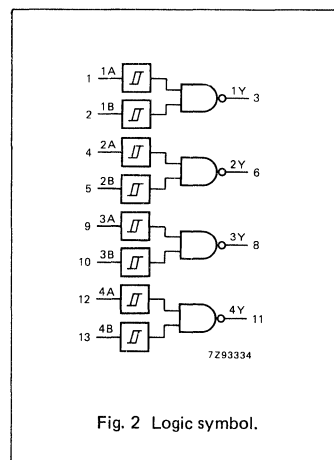


Fig. 2 Logic symbol.

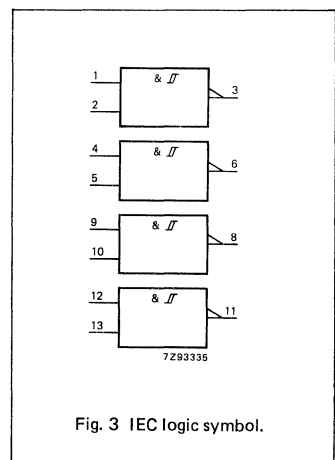
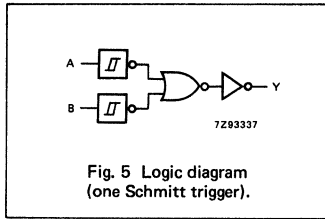
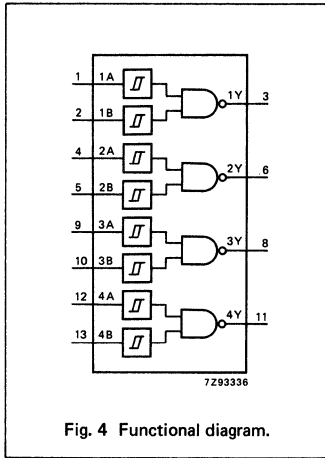


Fig. 3 IEC logic symbol.



**APPLICATIONS**

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

**FUNCTION TABLE**

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level  
L = LOW voltage level

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard  
I<sub>CC</sub> category: SSI

## Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
V <sub>T+</sub>	positive-going threshold	0.7 1.7 2.1		1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	0.7 1.7 2.1	1.5 3.15 4.2	V	2.0 4.5 6.0	Figs 6 and 7
V <sub>T-</sub>	negative-going threshold	0.3 0.9 1.2		1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	0.3 0.9 1.2	1.0 2.2 3.0	V	2.0 4.5 6.0	Figs 6 and 7
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.2 0.4 0.6		1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	0.2 0.4 0.6	1.0 1.4 1.6	V	2.0 4.5 6.0	Figs 6 and 7

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard

I<sub>CC</sub> category: SSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nA, nB	0,3

## Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
V <sub>T+</sub>	positive-going threshold	1.2 1.4		1.9 2.1	1.2 1.9	1.4 2.1	1.2 1.9	1.4 2.1	V	4.5 5.5	Figs 6 and 7
V <sub>T-</sub>	negative-going threshold	0.5 0.6		1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5	Figs 6 and 7
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.4 0.4		— —	0.4 0.4	— —	0.4 0.4	— —	V	4.5 5.5	Figs 6 and 7

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		20	33		41		50	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 8

TRANSFER CHARACTERISTIC WAVEFORMS

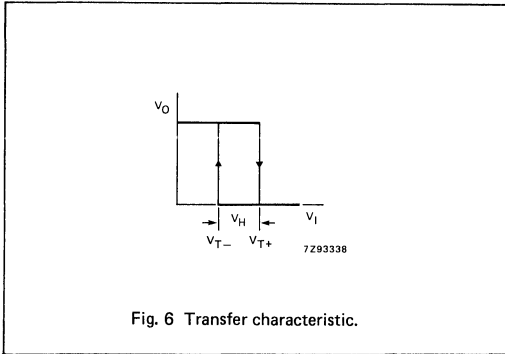


Fig. 6 Transfer characteristic.

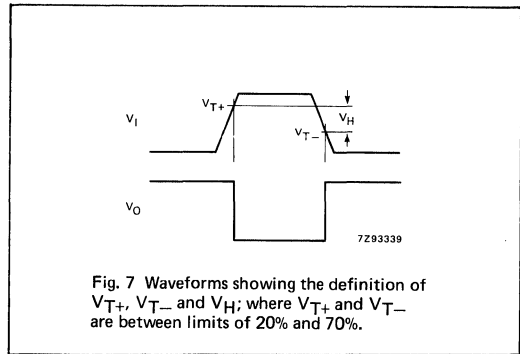


Fig. 7 Waveforms showing the definition of  $V_{T+}$ ,  $V_{T-}$  and  $V_H$ ; where  $V_{T+}$  and  $V_{T-}$  are between limits of 20% and 70%.

AC WAVEFORMS

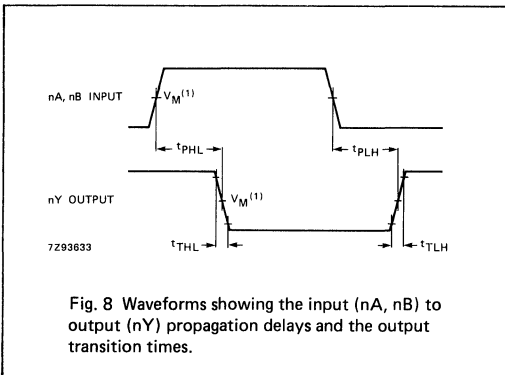


Fig. 8 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



This data sheet contains advance information and specifications are subject to change without notice.

3-TO-8 LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- Combines 3-of-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT137 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT137 are 3-of-8 decoder/demultiplexers with latches at the three address inputs (A<sub>n</sub>). The "137" essentially combines the 3-of-8 decoder function with a 3-bit storage latch. When the latch is enabled ( $\overline{LE}$  = LOW), the "137" acts as a 3-of-8 active LOW decoder. When the latch enable ( $\overline{LE}$ ) goes from LOW-to-HIGH, the last data present at the inputs, before this transition, is stored in the latches. Further address changes are ignored as long as  $\overline{LE}$  remains HIGH.

The output enable input ( $\overline{E}_1$  and  $E_2$ ) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless  $\overline{E}_1$  is LOW and  $E_2$  is HIGH.

The "137" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

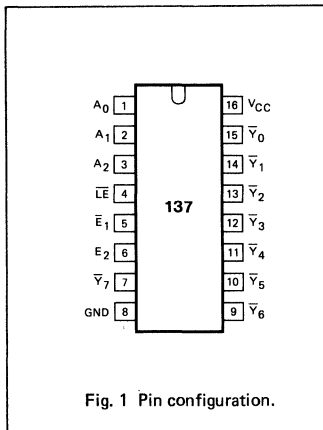


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\overline{Y}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT137P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT137T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	$\overline{E}_1$	data enable input (active LOW)
6	E <sub>2</sub>	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	multiplexer outputs
16	V <sub>CC</sub>	positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E <sub>2</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H
L	L	H	L	H	L	L	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	L	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

### 3-TO-8 LINE DECODER/DEMULTIPLEXER; INVERTING

#### FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>) and when enabled, provide 8 mutually exclusive active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_7$ ).

The "138" features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH (E<sub>3</sub>). Every output will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and E<sub>3</sub> is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12	17	ns
t <sub>PHL</sub> / t <sub>PLH</sub>	E <sub>3</sub> to $\bar{Y}_n$ $\bar{E}_n$ to $\bar{Y}_n$		14	17	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	67	67	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

#### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

#### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT138P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT138T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	address inputs
4, 5	$\bar{E}_1$ , $\bar{E}_2$	enable inputs (active LOW)
6	E <sub>3</sub>	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\bar{Y}_0$ to $\bar{Y}_7$	outputs (active LOW)
16	V <sub>CC</sub>	positive supply voltage

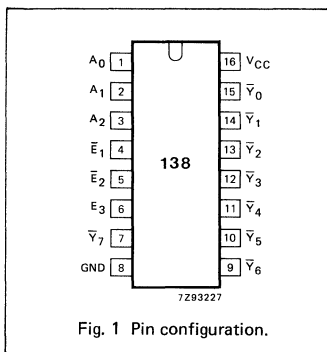


Fig. 1 Pin configuration.

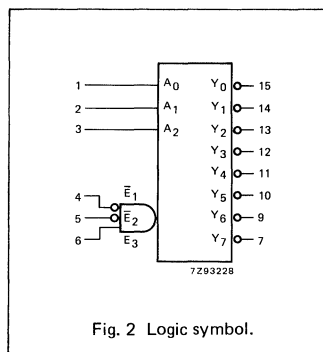


Fig. 2 Logic symbol.

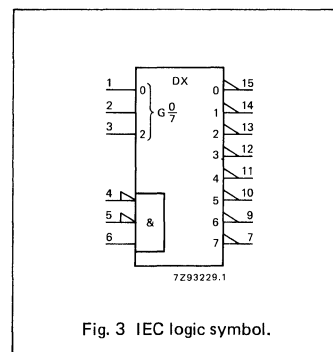


Fig. 3 IEC logic symbol.

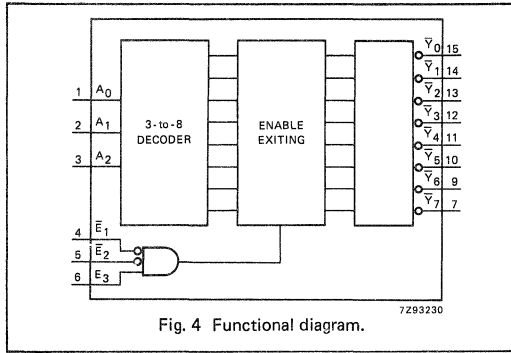


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	L	L	H	H	H	H	H	H
L	L	H	L	L	L	L	L	L	H	H	H	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H
L	L	H	L	L	L	L	L	L	L	L	H	H	H
L	L	H	L	L	L	L	L	L	L	L	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

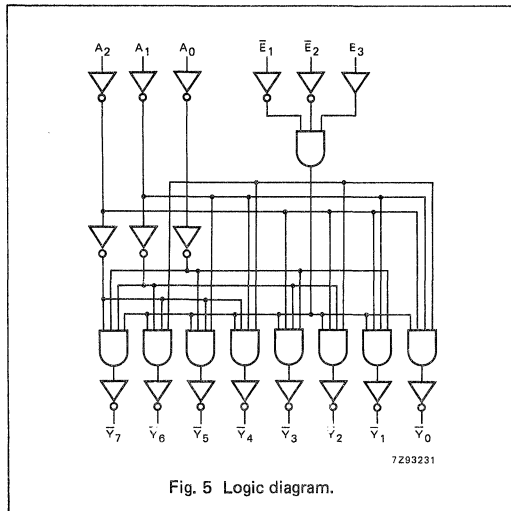


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>3</sub> to $\bar{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to $\bar{Y}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	0.70
E <sub>n</sub>	0.40
E <sub>3</sub>	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$		20	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>3</sub> to $\bar{Y}_n$		18	40		50		60	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E <sub>n</sub> to $\bar{Y}_n$		22	40		50		60	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>T LH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

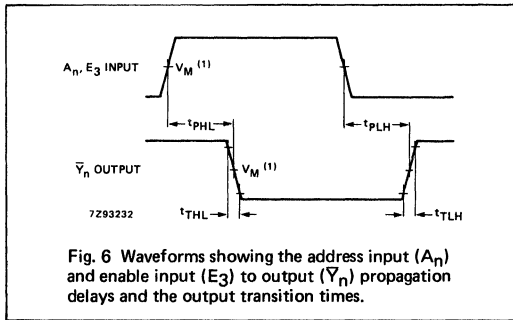


Fig. 6 Waveforms showing the address input ( $A_n$ ) and enable input ( $E_3$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.

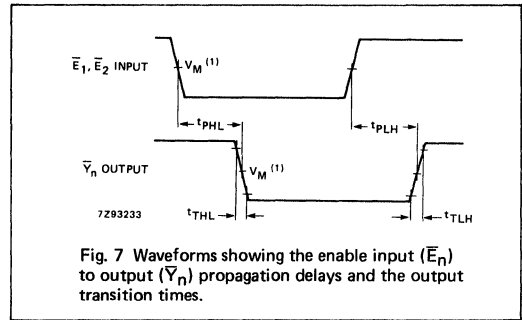


Fig. 7 Waveforms showing the enable input ( $\bar{E}_n$ ) to output ( $\bar{Y}_n$ ) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

FEATURES

- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT139 are high-speed, dual 1-to-4 line decoder/demultiplexers. This device has two independent decoders, each accepting two binary weighted inputs (nA<sub>0</sub> and nA<sub>1</sub>) and providing four mutually exclusive active LOW outputs (nY<sub>0</sub> to nY<sub>3</sub>). Each decoder has an active LOW enable input (nE).

When nE is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

The "139" is identical to the HEF4556 of the HE4000B family.

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to nY <sub>n</sub> nE to nY <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11 10	13 13	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	42	44	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT139P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT139T: 16-lead mini-pack; plastic (SO-16, SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1E, 2E	enable inputs (active LOW)
2, 3	1A <sub>0</sub> , 1A <sub>1</sub>	address inputs
4, 5, 6, 7	1Y <sub>0</sub> to 1Y <sub>3</sub>	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	outputs (active LOW)
14, 13	2A <sub>0</sub> , 2A <sub>1</sub>	address inputs
16	V <sub>CC</sub>	positive supply voltage

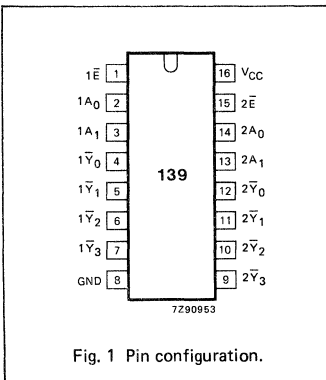


Fig. 1 Pin configuration.

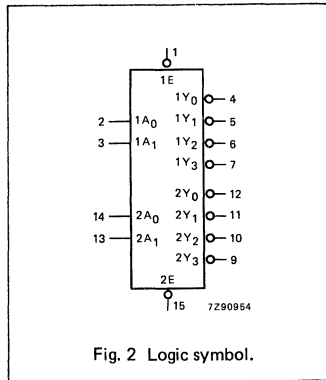


Fig. 2 Logic symbol.

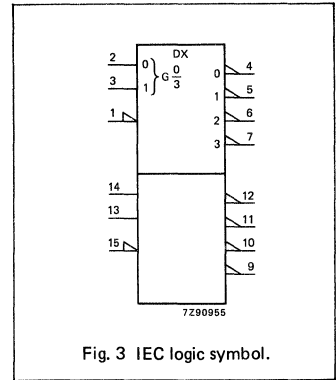


Fig. 3 IEC logic symbol.

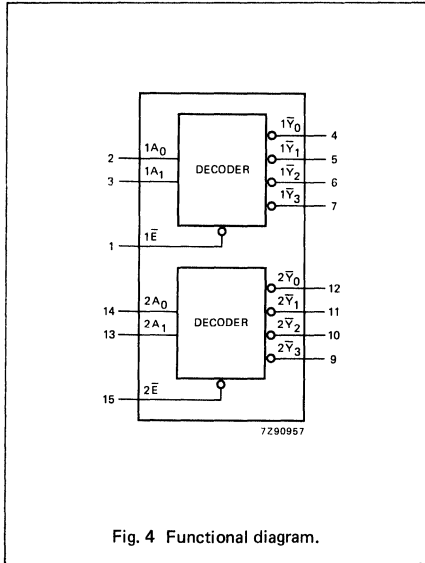


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\bar{E}$	$nA_0$	$nA_1$	$n\bar{V}_0$	$n\bar{V}_1$	$n\bar{V}_2$	$n\bar{V}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

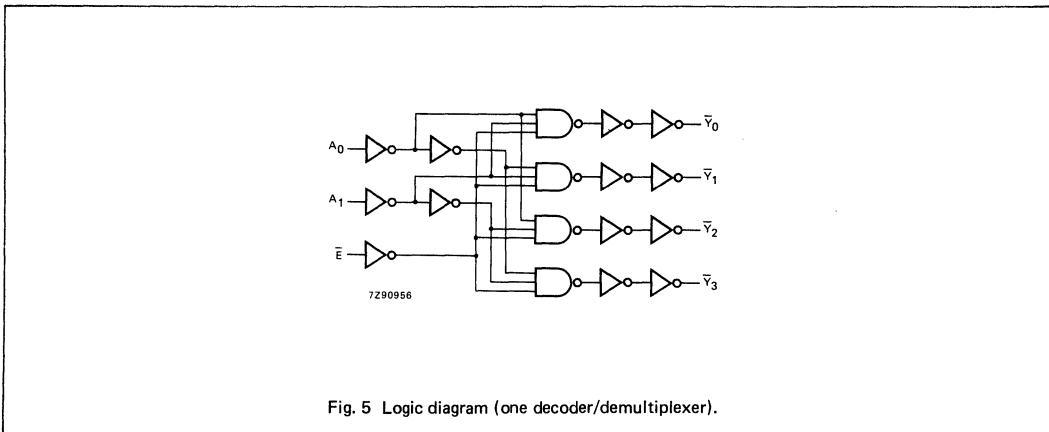


Fig. 5 Logic diagram (one decoder/demultiplexer).



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to $\bar{Y}_n$		39 14 11	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nE to n $\bar{Y}_n$		33 12 10	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
1A <sub>n</sub>	0.70
2A <sub>n</sub>	0.70
nE	0.70

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to $\bar{Y}_n$		16	34		43		51	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nE to n $\bar{Y}_n$		16	34		43		51	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

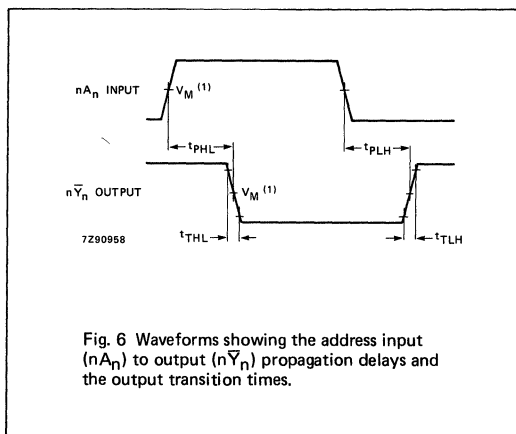


Fig. 6 Waveforms showing the address input ( $nA_n$ ) to output ( $n\bar{Y}_n$ ) propagation delays and the output transition times.

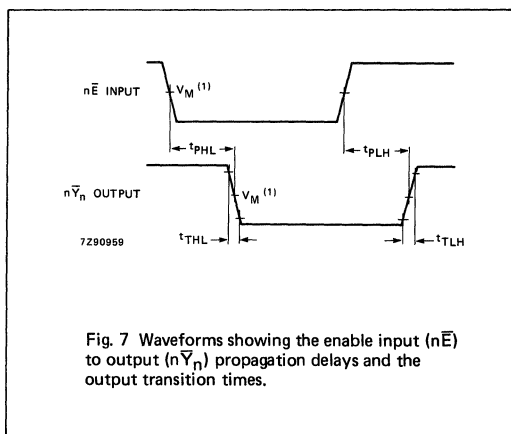


Fig. 7 Waveforms showing the enable input ( $n\bar{E}$ ) to output ( $n\bar{Y}_n$ ) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## 10-TO-4 LINE PRIORITY ENCODER

### FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT147 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT147 9-input priority encoders accept data from nine active LOW inputs ( $\bar{A}_0$  to  $\bar{A}_8$ ) and provide a binary representation on the four active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_3$ ). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line  $\bar{A}_8$  having the highest priority.

The devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\bar{A}_n$ to $\bar{Y}_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15	17	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	30	33	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

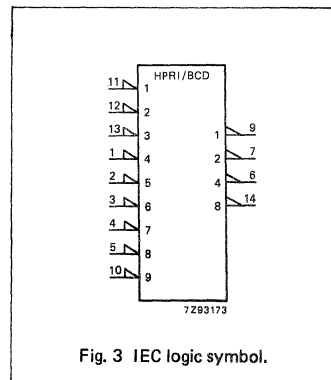
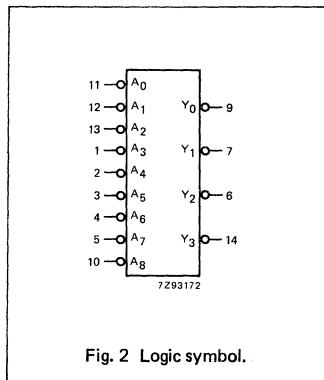
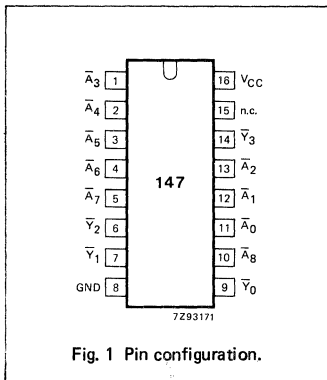
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT147P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT147T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 14	$\bar{Y}_0$ to $\bar{Y}_3$	BCD address outputs (active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	$\bar{A}_0$ to $\bar{A}_8$	decimal data inputs (active LOW)
15	n.c.	not connected
16	V <sub>CC</sub>	positive supply voltage



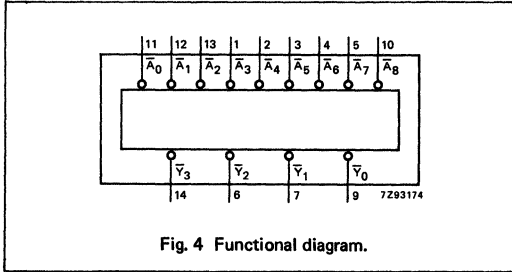


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS									OUTPUTS			
$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{Y}_3$	$\bar{Y}_2$	$\bar{Y}_1$	$\bar{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	L	H	H	H	H	H	L	H	H	L
X	X	L	H	H	H	H	H	H	L	L	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

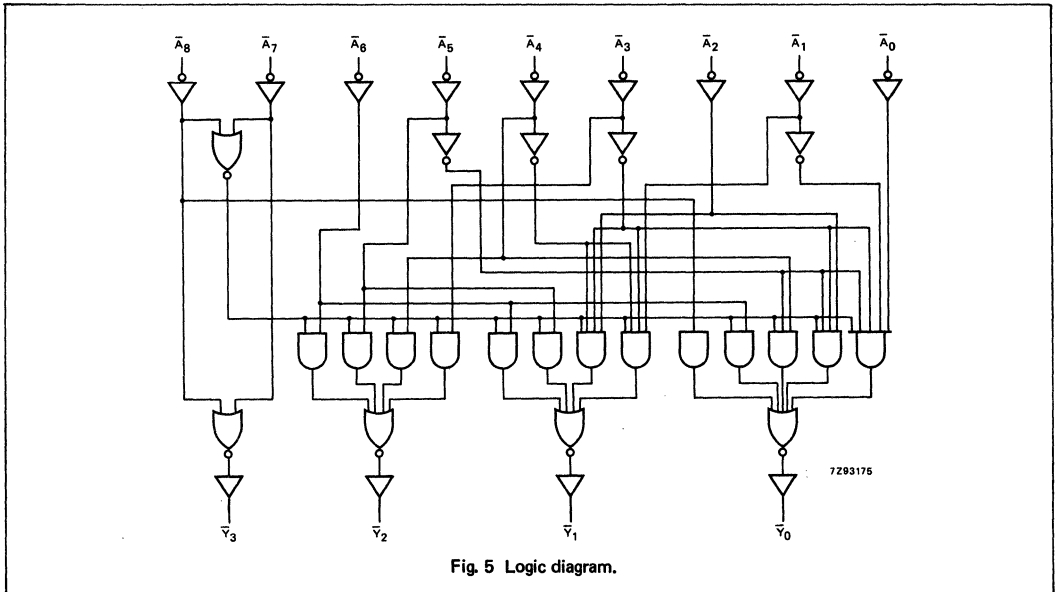


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TTLH</sub>	output transition time		19 7 6	75 15 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

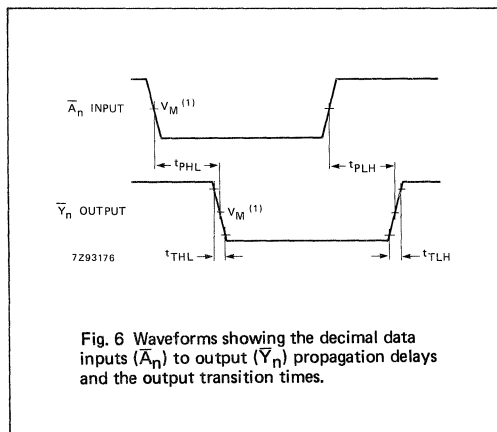
input	unit load coefficient
$\bar{A}_3, \bar{A}_4, A_7, \bar{A}_8$	1.50
$\bar{A}_5, \bar{A}_6, A_0, A_1, A_2$	1.10

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{A}_n$ to $\bar{Y}_n$		20	35		44		53	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

**AC WAVEFORMS**



**Note to AC waveforms**

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

## 8-INPUT MULTIPLEXER

### FEATURES

- True and complement outputs
- Multifunction capability
- Permits multiplexing from n lines to 1 line
- Non-inverting data path
- See the "251" for the 3-state version
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT151 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>) controlling the switch positions.

Assertion (Y) and negation (Ȳ) outputs are both provided.

The enable input (Ē) is active LOW.

When Ē is HIGH, the Y output is HIGH and the Ȳ output is LOW, regardless of all inputs.

The logic function provided at the output, when activated, is:

$$Y = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

The "151" provides in one package the ability to select from eight sources of data or control information. The "151" can provide any logic function of four variables and its negation with correct manipulations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to Y, Ȳ S <sub>n</sub> to Y, Ȳ Ē to Y Ē to Ȳ	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	16 19 12 14	19 20 13 18	ns ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT151P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT151T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I <sub>0</sub> to I <sub>7</sub>	multiplexer inputs
5	Y	multiplexer output
6	Ȳ	complementary multiplexer output
7	Ē	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	select inputs
16	V <sub>CC</sub>	positive supply voltage

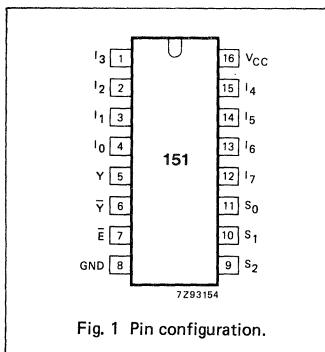


Fig. 1 Pin configuration.

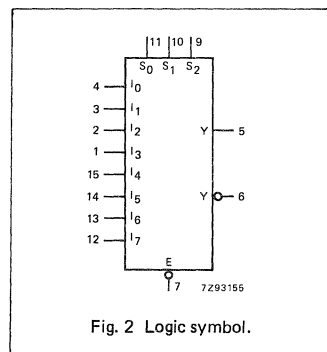


Fig. 2 Logic symbol.

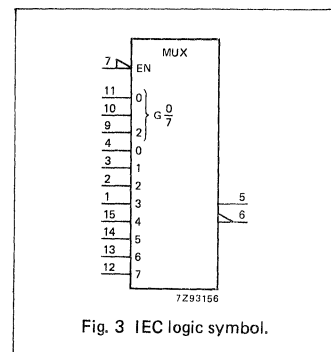
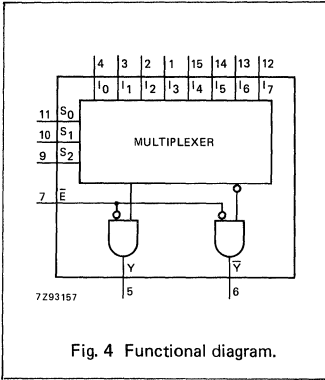


Fig. 3 IEC logic symbol.

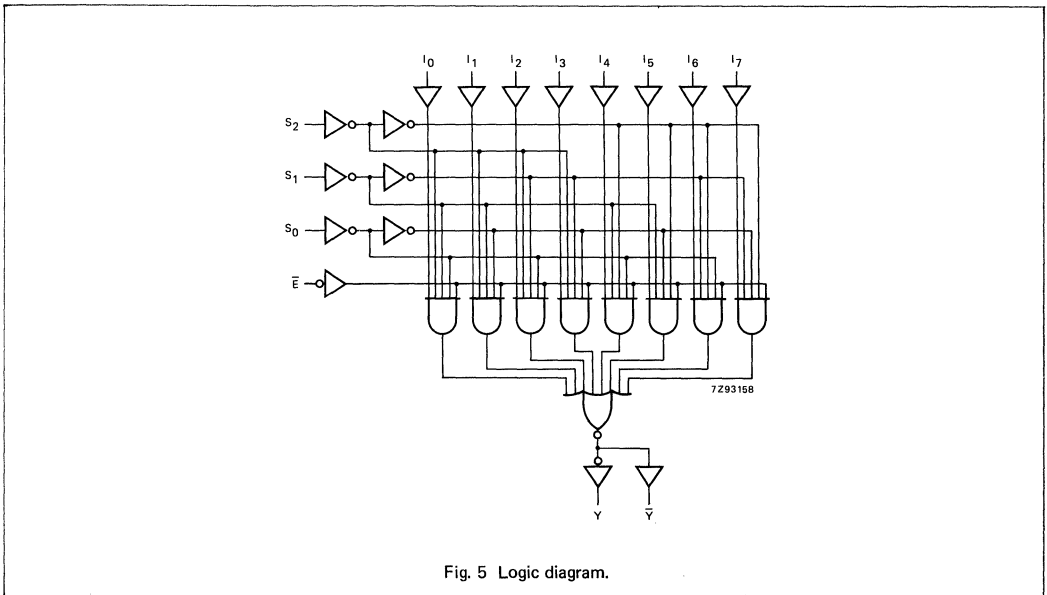




FUNCTION TABLE

INPUTS												OUTPUTS	
$\bar{E}$	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	$\bar{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	L	X	L	X	X	X	X	X	X	H	L
L	L	L	L	X	X	X	X	X	X	X	X	L	H
L	L	L	H	X	X	L	X	X	X	X	X	H	L
L	L	H	H	L	X	X	H	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	X	H	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	L	X	X	X	H	L
L	H	L	H	X	X	X	X	H	X	X	X	L	H
L	H	H	L	X	X	X	X	X	L	X	X	H	L
L	H	H	L	X	X	X	X	X	H	X	X	L	H
L	H	H	H	X	X	X	X	X	X	L	X	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to Y		52 19 15	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to $\bar{Y}$		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to Y		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to $\bar{Y}$		61 22 18	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to Y		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to $\bar{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
I <sub>n</sub>	0.45
S <sub>n</sub>	1.50
E	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to Y		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to $\bar{Y}$		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to Y		23	41		51		62	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to $\bar{Y}$		25	43		54		65	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to Y		16	29		36		44	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to $\bar{Y}$		21	36		45		54	ns	4.5	Fig. 7
t <sup>t</sup> <sub>THL</sub> / t <sup>t</sup> <sub>TLL</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

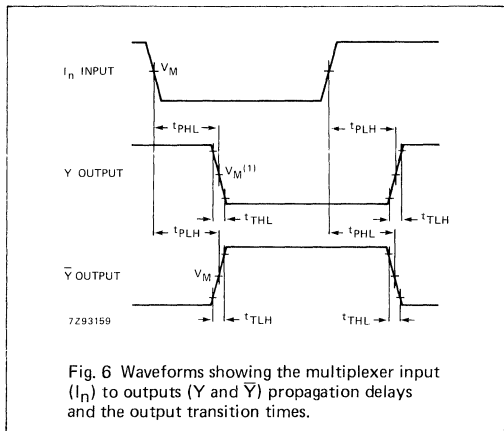


Fig. 6 Waveforms showing the multiplexer input ( $I_n$ ) to outputs (Y and  $\bar{Y}$ ) propagation delays and the output transition times.

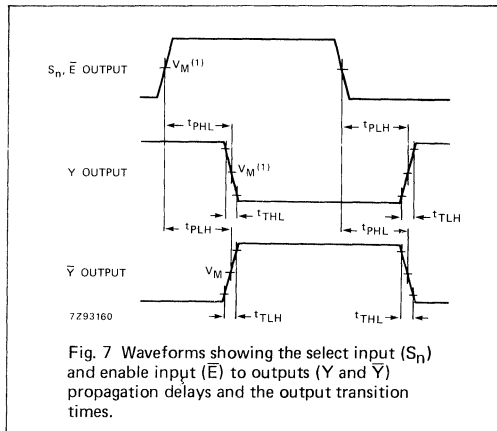


Fig. 7 Waveforms showing the select input ( $S_n$ ) and enable input ( $\bar{E}$ ) to outputs (Y and  $\bar{Y}$ ) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL 4-INPUT MULTIPLEXER

FEATURES

- Non-inverting outputs
- Separate enable for each output
- Common select inputs
- See '253' for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S<sub>0</sub>, S<sub>1</sub>). The two 4-input multiplexer circuits have individual active LOW output enable inputs (1E, 2E) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S<sub>0</sub> and S<sub>1</sub>.

The logic equations for the outputs are:

$$1Y = 1\bar{E} \cdot (1I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 1I_1 \cdot S_1 \cdot \bar{S}_0 + 1I_2 \cdot S_1 \cdot S_0 + 1I_3 \cdot \bar{S}_1 \cdot S_0)$$

$$2Y = 2\bar{E} \cdot (2I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 2I_1 \cdot S_1 \cdot \bar{S}_0 + 2I_2 \cdot S_1 \cdot S_0 + 2I_3 \cdot \bar{S}_1 \cdot S_0)$$

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> , 2I <sub>n</sub> to nY S <sub>n</sub> to nY nE to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 15 10	16 17 11	ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT153P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT153T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1E, 2E	output enable inputs (active LOW)
14, 2	S <sub>0</sub> , S <sub>1</sub>	common data select inputs
6, 5, 4, 3	1I <sub>0</sub> to 1I <sub>3</sub>	data inputs from source 1
7	1Y	multiplexer output from source 1
8	GND	ground (0 V)
9	2Y	multiplexer output from source 2
10, 11, 12, 13	2I <sub>0</sub> to 2I <sub>3</sub>	data inputs from source 2
16	V <sub>CC</sub>	positive supply voltage

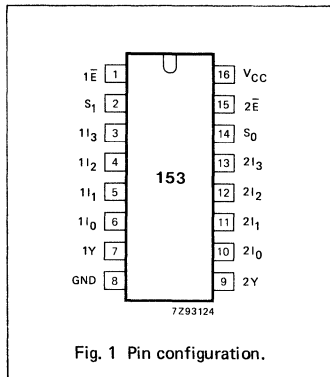


Fig. 1 Pin configuration.

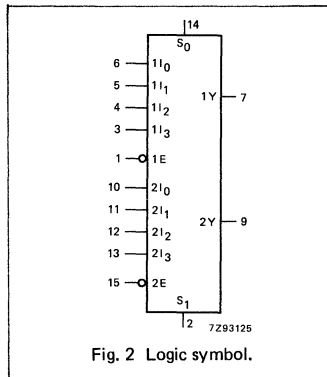


Fig. 2 Logic symbol.

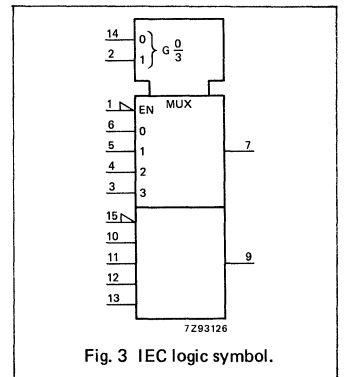


Fig. 3 IEC logic symbol.

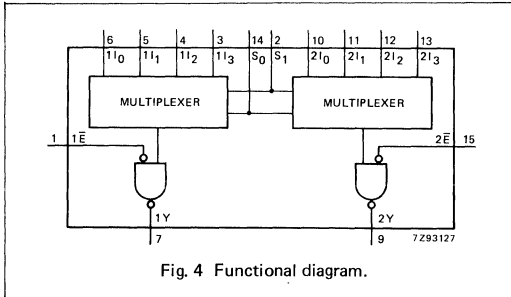


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (cont.'ed)**

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The "153" is similar to the "253" but has standard outputs.

**FUNCTION TABLE**

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S <sub>0</sub>	S <sub>1</sub>	nI <sub>0</sub>	nI <sub>1</sub>	nI <sub>2</sub>	nI <sub>3</sub>	nE	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	L	X	L	X	X	L	L
L	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
L	H	X	X	X	L	L	L
L	H	X	X	X	H	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

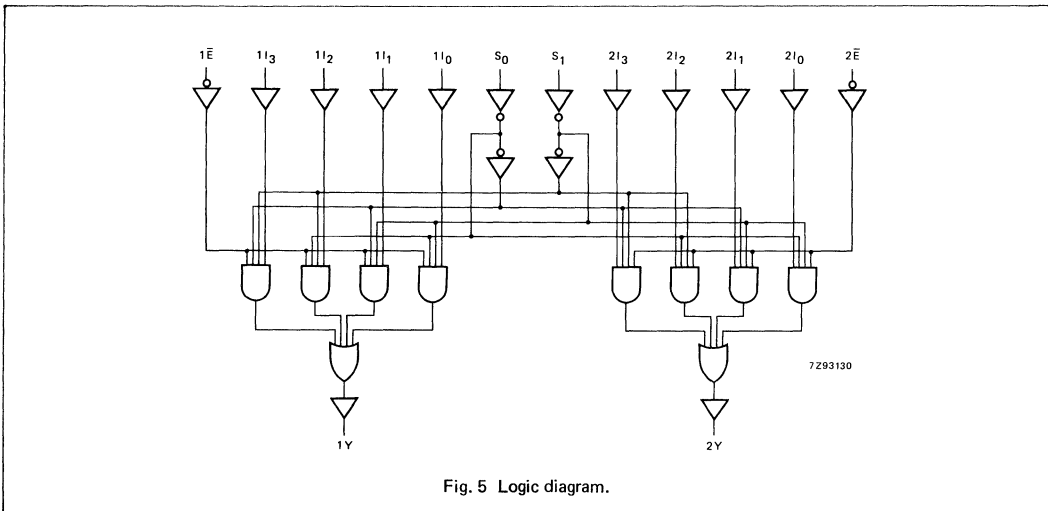


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\bar{E}$ to nY		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
1I <sub>n</sub> , 2I <sub>n</sub>	0.45
nE	0.60
S <sub>n</sub>	1.35

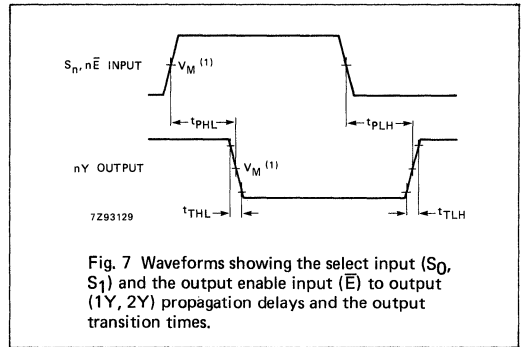
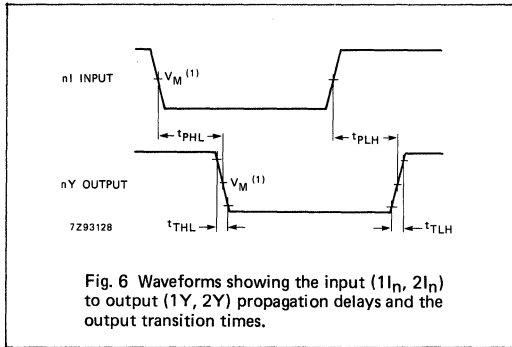
**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		19	34		43		51	ns	4.5	Fig. 6
t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		13	24		30		36	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		20	34		43		51	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nE to nY		14	27		34		41	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7



AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## 4-TO-16 LINE DECODER/DEMULTIPLEXER

### FEATURES

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT154 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for the expansion of the decoder.

The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "154" can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , E <sub>n</sub> to Y <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	60	60	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

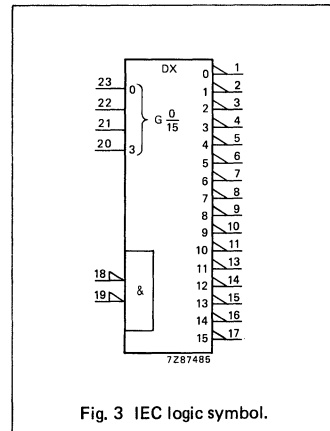
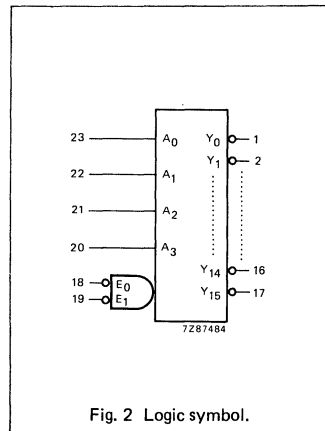
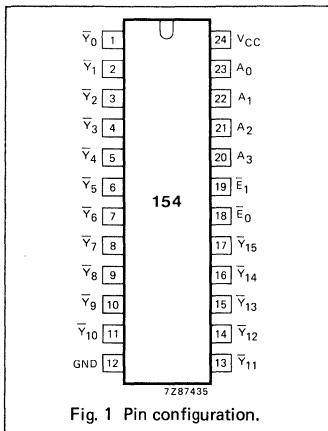
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT154P: 24-lead DIL; plastic (SOT-101A).  
 PC74HC/HCT154T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	Y <sub>0</sub> to Y <sub>15</sub>	outputs (active LOW)
18, 19	E <sub>0</sub> , E <sub>1</sub>	enable inputs (active LOW)
12	GND	ground (0 V)
23, 22, 21, 20	A <sub>0</sub> to A <sub>3</sub>	address inputs
24	V <sub>CC</sub>	positive supply voltage



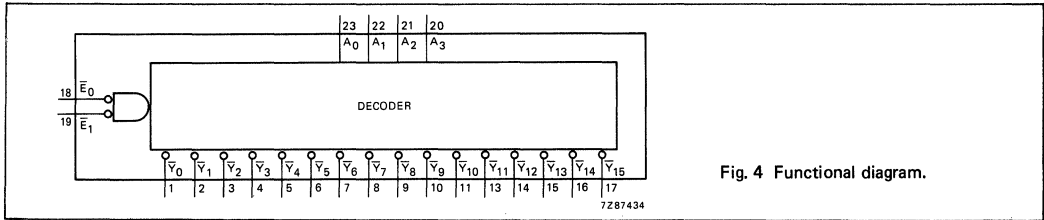


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS																
$E_0$	$\bar{E}_1$	A0	A1	A2	A3	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$	$\bar{Y}_8$	$\bar{Y}_9$	$\bar{Y}_{10}$	$\bar{Y}_{11}$	$\bar{Y}_{12}$	$\bar{Y}_{13}$	$\bar{Y}_{14}$	$\bar{Y}_{15}$	
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H	H

H = HIGH voltage level L = LOW voltage level X = don't care

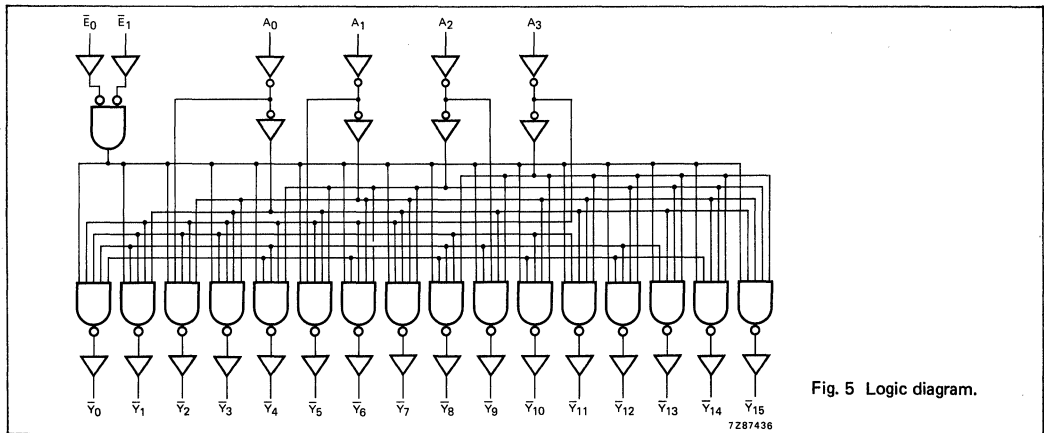


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $A_n$ to $\bar{Y}_n$		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $E_n$ to $\bar{Y}_n$		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

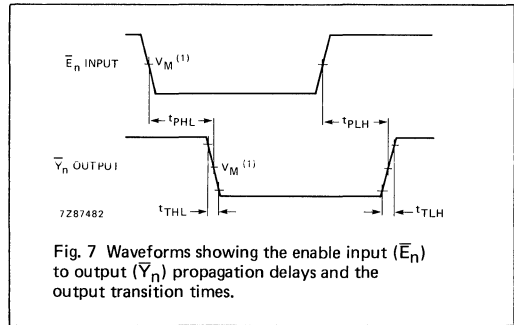
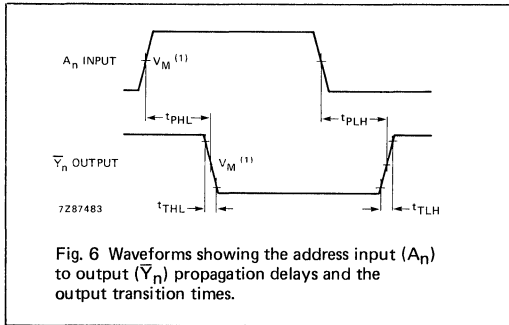
input	unit load coefficient
A <sub>n</sub>	1.0
E <sub>n</sub>	1.0

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$		16	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}_n$ to $\bar{Y}_n$		15	32		40		48	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

QUAD 2-INPUT MULTIPLEXER

FEATURES

- Non-inverting data path
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S).

The four outputs present the selected data in the true (non-inverted) form. The enable input (E) is active LOW. When E is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$$1Y = \bar{E} \cdot (1I_1 \cdot S + 1I_0 \cdot \bar{S})$$

$$2Y = \bar{E} \cdot (2I_1 \cdot S + 2I_0 \cdot \bar{S})$$

$$3Y = \bar{E} \cdot (3I_1 \cdot S + 3I_0 \cdot \bar{S})$$

$$4Y = \bar{E} \cdot (4I_1 \cdot S + 4I_0 \cdot \bar{S})$$

The "157" is identical to the "158" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	13	ns
	nI <sub>0</sub> , nI <sub>1</sub> to nY		11	12	ns
	E to nY		14	19	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	76	70	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz

V<sub>CC</sub> = supply voltage in V

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT157P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT157T: 16-lead mini-pack; plastic (SO-16;SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	1I <sub>0</sub> to 4I <sub>0</sub>	data inputs from source 0
3, 6, 10, 13	1I <sub>1</sub> to 4I <sub>1</sub>	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	E	enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

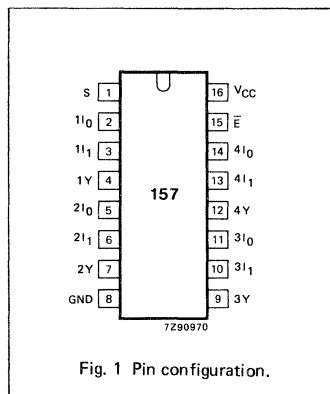


Fig. 1 Pin configuration.

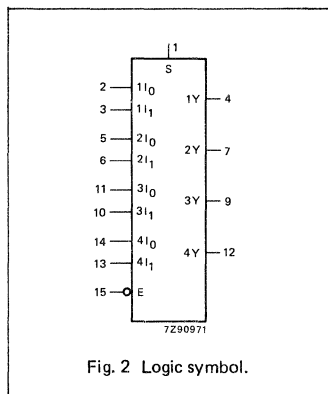


Fig. 2 Logic symbol.

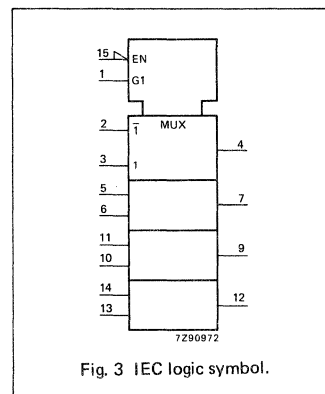


Fig. 3 IEC logic symbol.

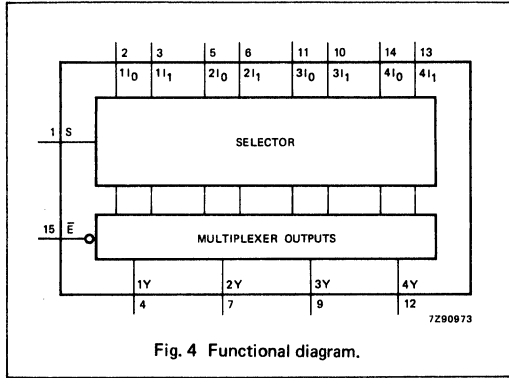


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\bar{E}$	S	$nI_0$	$nI_1$	$nY$
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

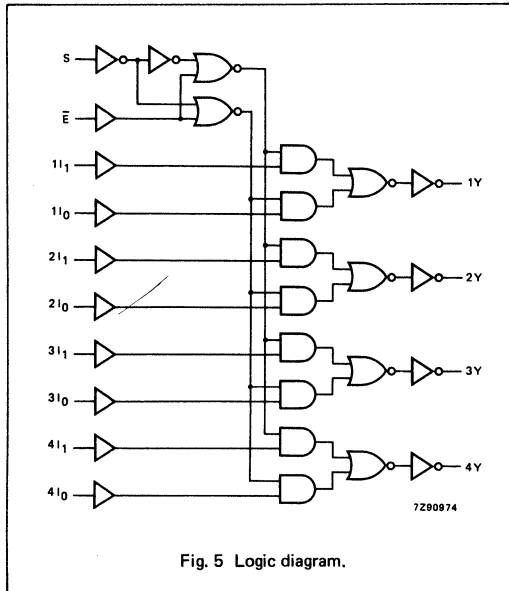


Fig. 5 Logic diagram.



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> to nY; nI <sub>1</sub> to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nI <sub>0</sub>	1.00
nI <sub>1</sub>	1.00
E	0.60
S	3.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> to nY; nI <sub>1</sub> to nY		16	27		34		41	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to nY		15	26		33		39	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY		22	37		46		56	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

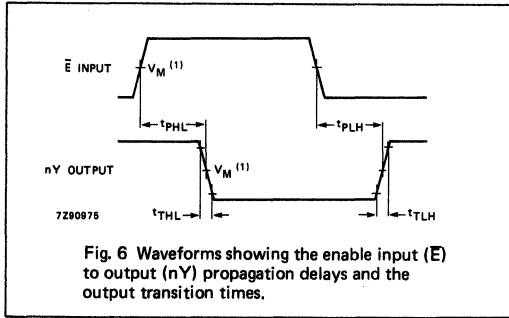


Fig. 6 Waveforms showing the enable input (E) to output (nY) propagation delays and the output transition times.

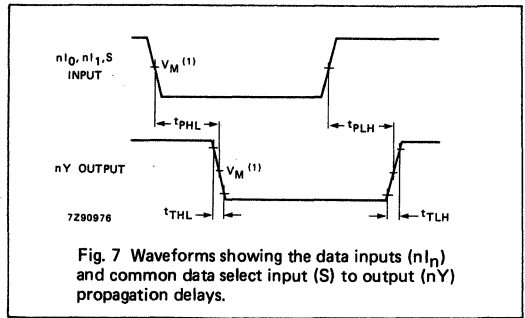


Fig. 7 Waveforms showing the data inputs ( $nI_n$ ) and common data select input (S) to output (nY) propagation delays.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

QUAD 2-INPUT MULTIPLEXER; INVERTING

FEATURES

- Inverting data path
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input (E) is active LOW.

When  $\bar{E}$  is HIGH, all the outputs ( $1\bar{Y}$  to  $4\bar{Y}$ ) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$$1\bar{Y} = \bar{E} \cdot (1I_1 \cdot S + 1I_0 \cdot \bar{S})$$

$$2\bar{Y} = \bar{E} \cdot (2I_1 \cdot S + 2I_0 \cdot \bar{S})$$

$$3\bar{Y} = \bar{E} \cdot (3I_1 \cdot S + 3I_0 \cdot \bar{S})$$

$$4\bar{Y} = \bar{E} \cdot (4I_1 \cdot S + 4I_0 \cdot \bar{S})$$

The "158" is identical to the "157" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> , nI <sub>1</sub> to nY E to nY S to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12 14 14	13 16 16	ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	40	40	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz

V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

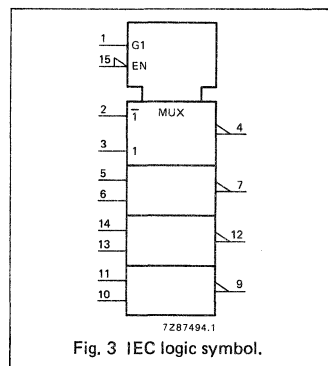
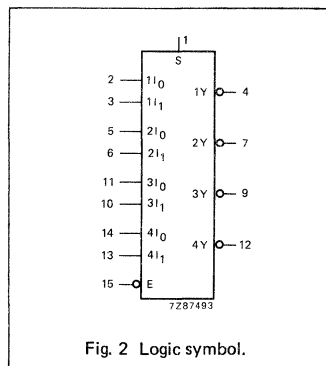
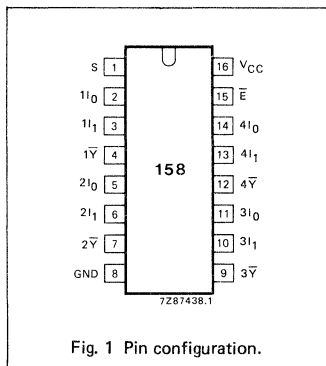
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT158P: 16-lead DIL; plastic (SOT-382).

PC74HC/HCT158T: 16-lead mini-pack, plastic (SO-16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	1I <sub>0</sub> to 4I <sub>0</sub>	data inputs from source 0
3, 6, 10, 13	1I <sub>1</sub> to 4I <sub>1</sub>	data inputs from source 1
4, 7, 9, 12	1Y $\bar{1}$ to 4Y $\bar{4}$	multiplexer outputs
8	GND	ground (0 V)
15	$\bar{E}$	enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage



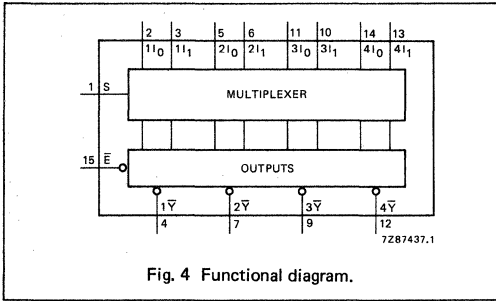


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
E	S	nI <sub>0</sub>	nI <sub>1</sub>	nY
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

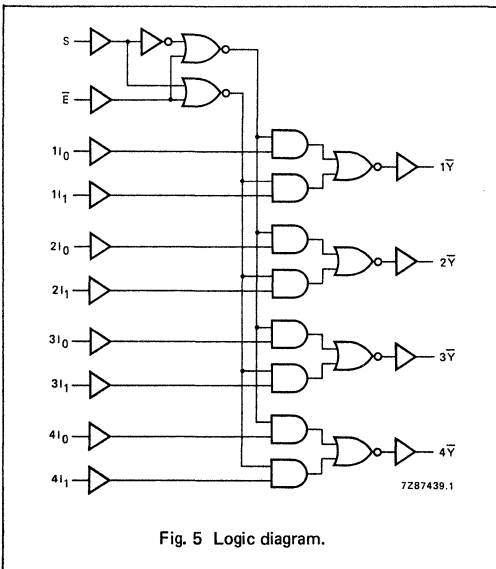


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $n 0, n 1$ to $n\bar{Y}$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/$ $t_{PLH}$	propagation delay E to $n\bar{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay S to $n\bar{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nI <sub>0</sub>	0.40
nI <sub>1</sub>	0.40
S	2.20
E	0.60

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> , nI <sub>1</sub> to nY		16	30		38		45	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to nY		19	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY		19	35		44		53	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

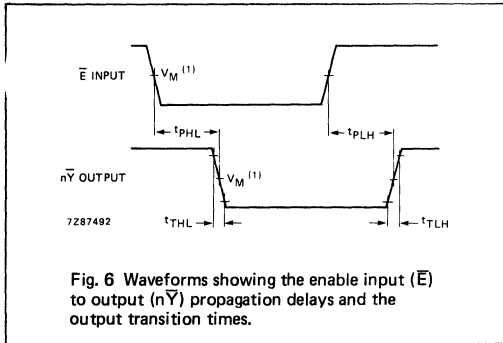


Fig. 6 Waveforms showing the enable input ( $\bar{E}$ ) to output ( $n\bar{Y}$ ) propagation delays and the output transition times.

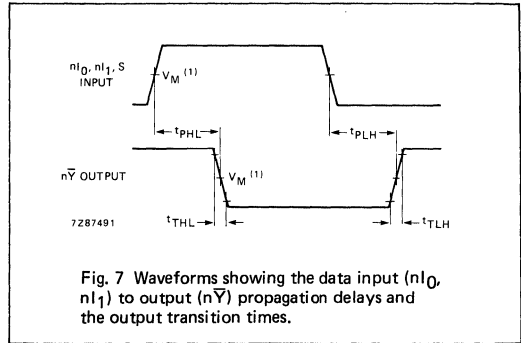


Fig. 7 Waveforms showing the data input ( $nI_0, nI_1, S$ ) to output ( $n\bar{Y}$ ) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; ASYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I<sup>2</sup>C category: MSI

GENERAL DESCRIPTION

The 74HC/HCT160 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT160 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting.

Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub>	propagation delay CP to Q <sub>n</sub> CP to TC MR to Q <sub>n</sub> MR to TC CET to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	19	21	ns
			21	24	ns
			21	23	ns
			21	26	ns
			14	14	ns
t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC CET to TC		19	21	ns
			21	20	ns
			14	7	ns
f <sub>max</sub>	maximum clock frequency		61	31	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	39	34	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

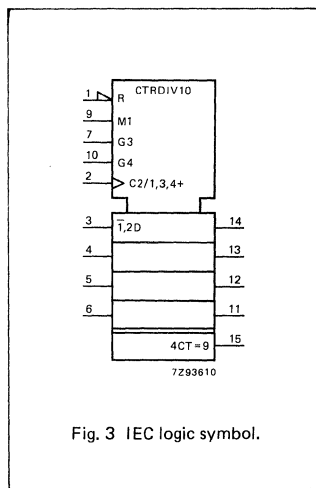
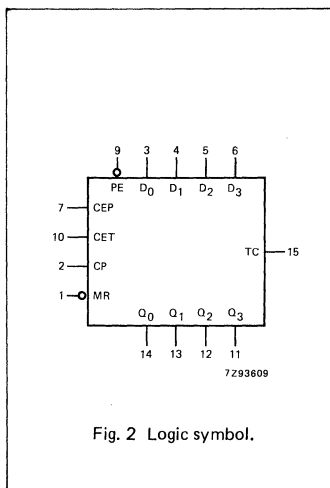
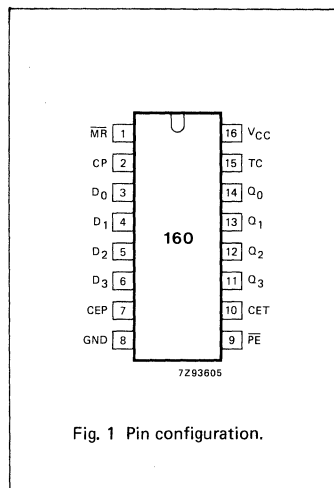
$f_i$  = input frequency in MHz           $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz          $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>1</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>1</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT160P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT160T: 16-lead mini-pack; plastic (SO-16; SOT-109A).



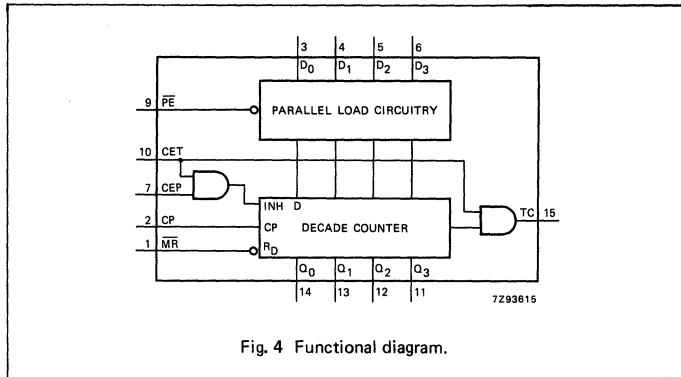


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

A LOW level at the master reset input (MR) sets all four outputs of the flip-flops (Q<sub>0</sub> to Q<sub>3</sub>) to LOW level regardless of the levels at CP, FE, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q<sub>0</sub>. This pulse can be used to enable the next cascaded stage.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	MR	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D <sub>0</sub> to D <sub>3</sub>	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	FE	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
15	TC	terminal count output
16	V <sub>CC</sub>	positive supply voltage

**FUNCTION TABLE**

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	CEP	CET	FE	D <sub>n</sub>	Q <sub>n</sub>	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	q <sub>n</sub>	*
	H	X	X	l	h	X	q <sub>n</sub>	L

**Note to function table**

\* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition

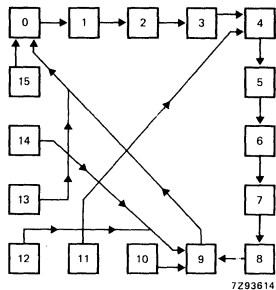


Fig. 5 State diagram.

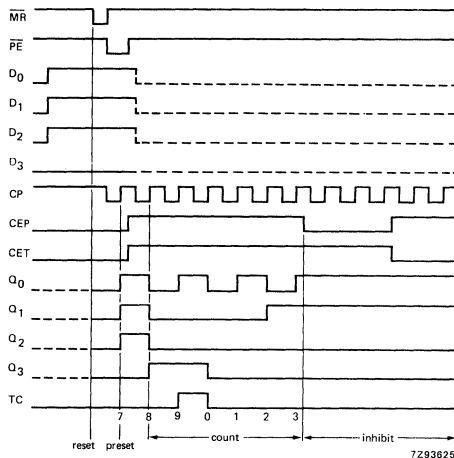


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

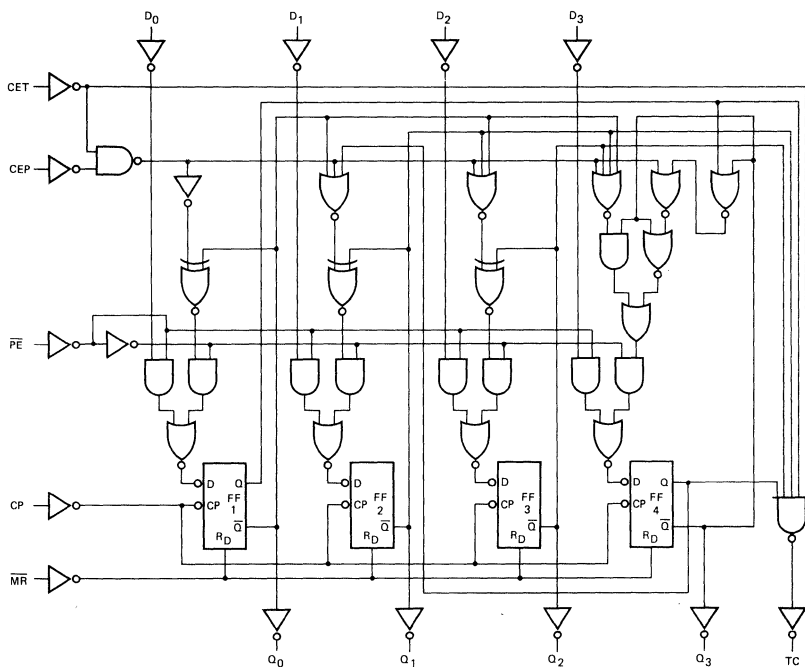


Fig. 7 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 31		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		210 42 36		ns	2.0 4.5 6.0	Fig. 8
t <sub>w</sub>	master reset pulse width LOW	90 18 15	28 10 8		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	22 8 6		100 20 17		120 27 20		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time PE to CP	135 27 23	41 15 12		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time CEP, CET to CP	200 40 34	63 23 18		250 50 43		300 60 51		ns	2.0 4.5 6.0	Fig. 12

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0	-17		0		0		ns	2.0 4.5 6.0	Figs 11 and 12
t <sub>h</sub>	hold time PE to CP	0	-41		0		0		ns	2.0 4.5 6.0	Figs 11 and 12
t <sub>h</sub>	hold time CEP, CET to CP	0	-47		0		0		ns	2.0 4.5 6.0	Figs 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	18 55 66		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
MR	0.95	D <sub>n</sub>	0.25
CP	0.80	CET	1.05
CEP	0.25	PE	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	V <sub>CC</sub> V	TEST CONDITIONS WAVEFORMS	
		74HCT									
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		25	43		54		65	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
t <sub>PLH</sub>	propagation delay CP to TC		23	39		49		59	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		27	50		63		75	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC		30	50		63		75	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
t <sub>PLH</sub>	propagation delay CET to TC		9	17		21		26	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t <sub>W</sub>	clock pulse width HIGH or LOW	31	8		39		47		ns	4.5	Fig. 8
t <sub>W</sub>	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to CP	20	9		25		30		ns	4.5	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	18	10		25		30		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time PE to CP	30	18		44		53		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time CEP, CET to CP	40	23		50		60		ns	4.5	Fig. 12

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0	-8		0		0		ns	4.5	Figs 11 and 12
t <sub>h</sub>	hold time PE to CP	0	-13		0		0		ns	4.5	Figs 11 and 12
t <sub>h</sub>	hold time CEP, CET to CP	0	-27		0		0		ns	4.5	Figs 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	16	28		13		11		MHz	4.5	Fig. 8



AC WAVEFORMS

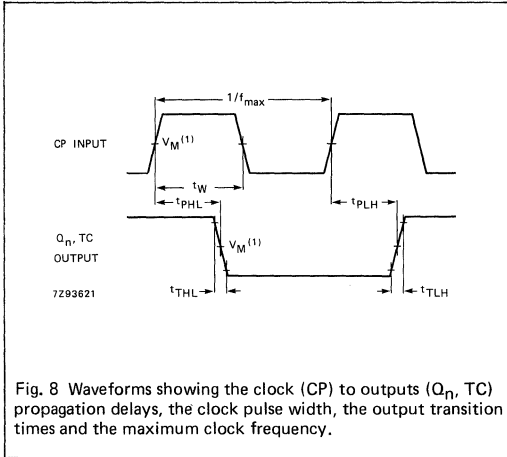


Fig. 8 Waveforms showing the clock (CP) to outputs ( $Q_n$ , TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

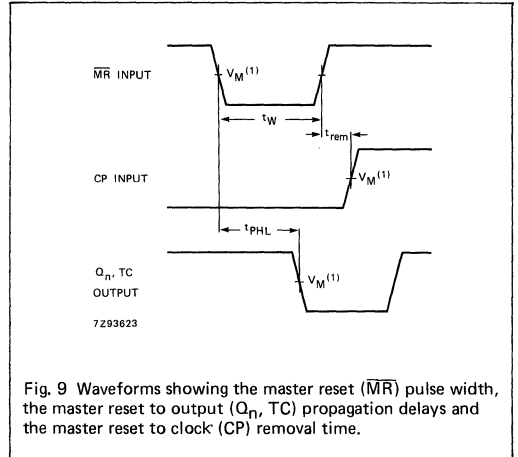


Fig. 9 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_n$ , TC) propagation delays and the master reset to clock (CP) removal time.

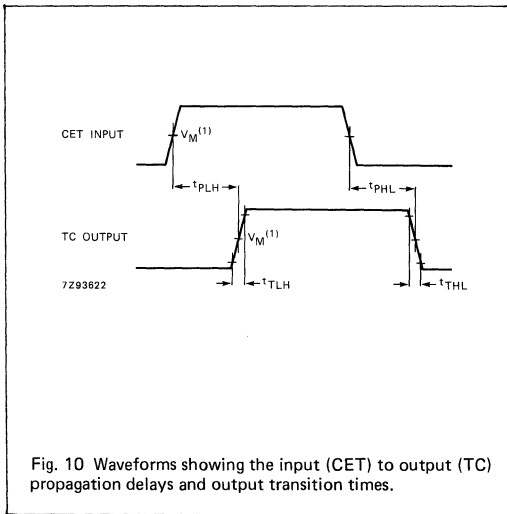


Fig. 10 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

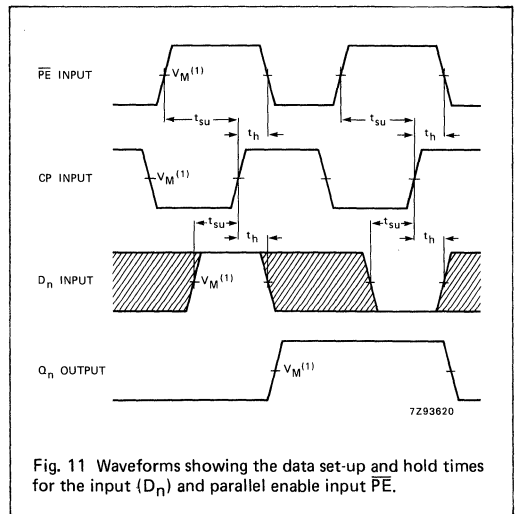


Fig. 11 Waveforms showing the data set-up and hold times for the input ( $D_n$ ) and parallel enable input  $\overline{PE}$ .

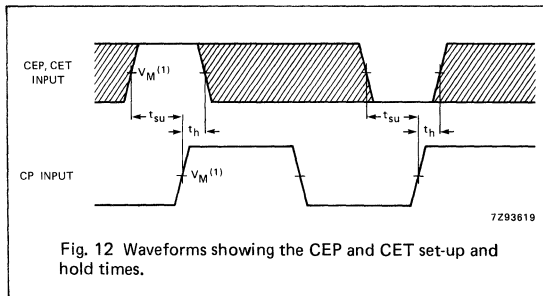


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_1 = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_1 = \text{GND to } 3 \text{ V}$ .

**PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; ASYNCHRONOUS RESET**

**FEATURES**

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ( $\overline{PE}$ ) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for  $\overline{PE}$  are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

*(continued on next page)*

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC $\overline{MR}$ to Q <sub>n</sub> $\overline{MR}$ to TC CET to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	19	20	ns
			21	24	ns
			20	25	ns
			20	26	ns
			10	14	ns
f <sub>max</sub>	maximum clock frequency		44	45	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT161P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT161T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

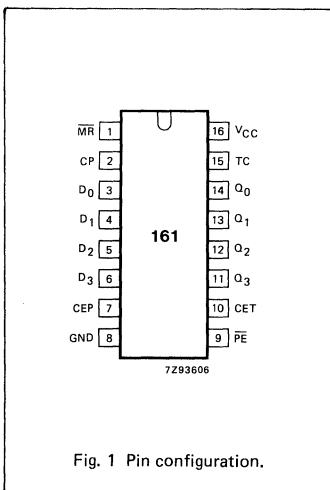


Fig. 1 Pin configuration.

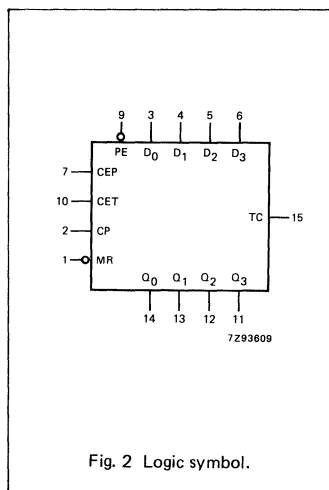


Fig. 2 Logic symbol.

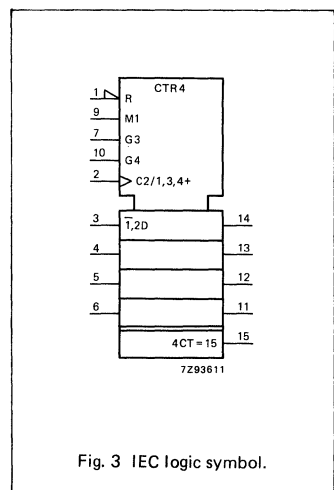


Fig. 3 IEC logic symbol.

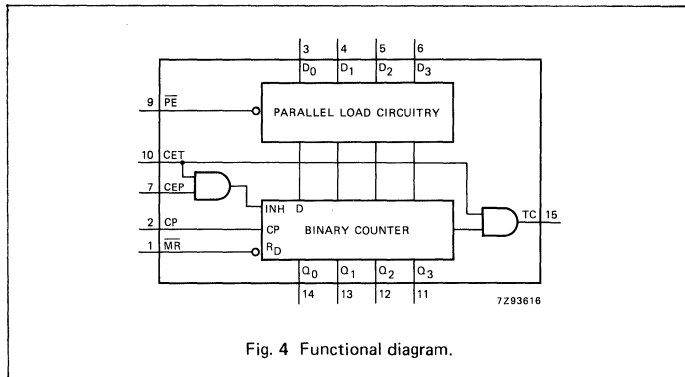


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

A LOW level at the master reset input ( $\overline{MR}$ ) sets all four outputs of the flip-flops ( $Q_0$  to  $Q_3$ ) to LOW level regardless of the levels at CP,  $\overline{PE}$ , CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of  $Q_0$ . This pulse can be used to enable the next cascaded stage.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	$D_0$ to $D_3$	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	$Q_0$ to $Q_3$	flip-flop outputs
15	TC	terminal count output
16	$V_{CC}$	positive supply voltage

**FUNCTION TABLE**

OPERATING MODE	INPUTS					OUTPUTS		
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	$D_n$	$Q_n$	TC
reset (clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
count	H	↑	h	h	h	X	count	*
hold (do nothing)	H	X	l	X	h	X	$q_n$	*
	H	X	X	l	h	X	$q_n$	L

**Note to function table**

\* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition

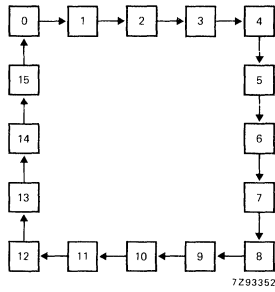


Fig. 5 State diagram.

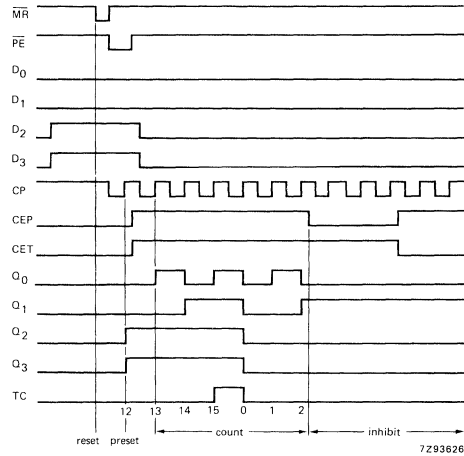


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

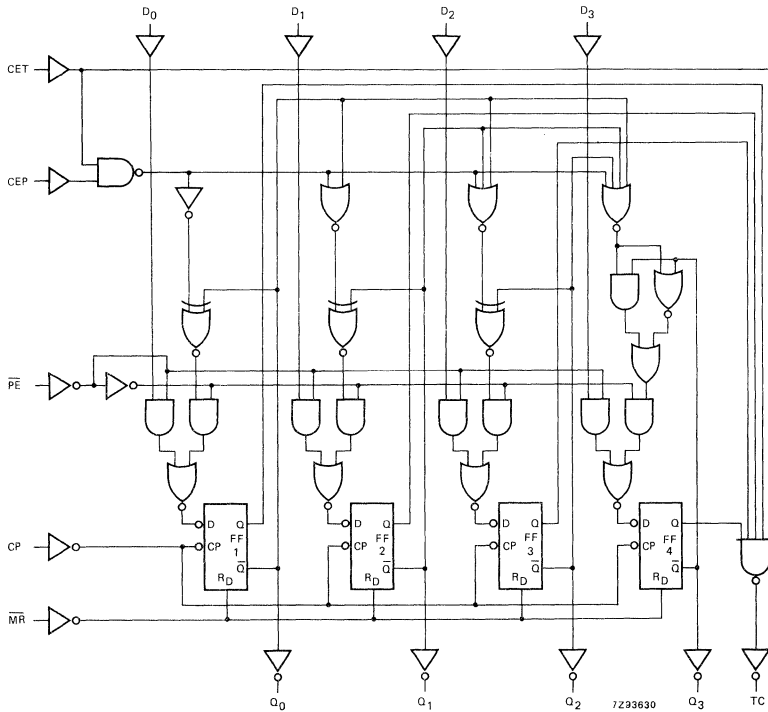


Fig. 7 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		61 22 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		63 23 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 10
t <sub>W</sub>	clock pulse width HIGH or LOW	110 22 19	22 8 6		140 28 24		165 33 28		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	master reset pulse width; LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to CP	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time PE to CP	100 20 17	30 11 9		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time CEP, CET to CP	170 34 29	47 17 14		215 43 37		255 51 43		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	4,6 23 27	13 40 48		3,6 18 21		3,0 15 18		MHz	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

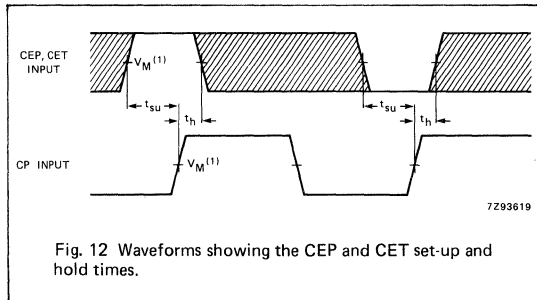
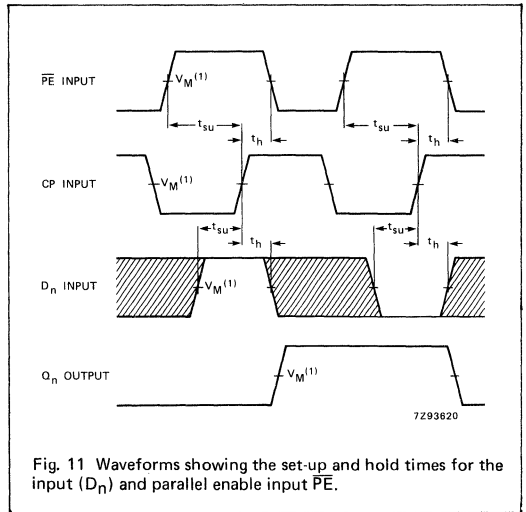
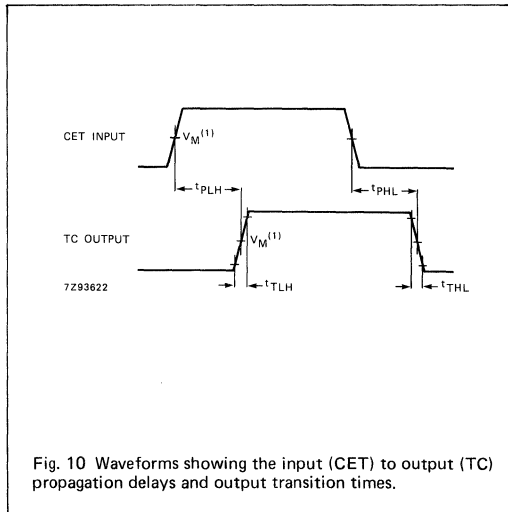
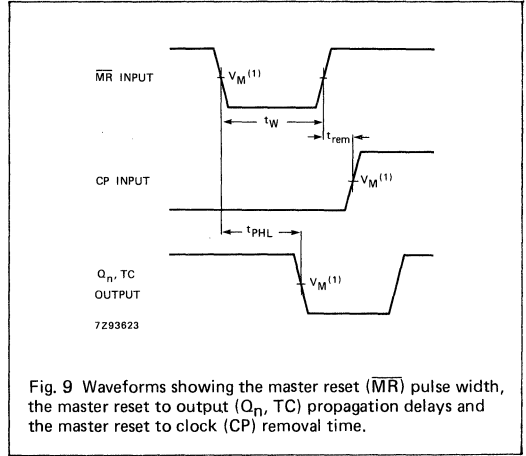
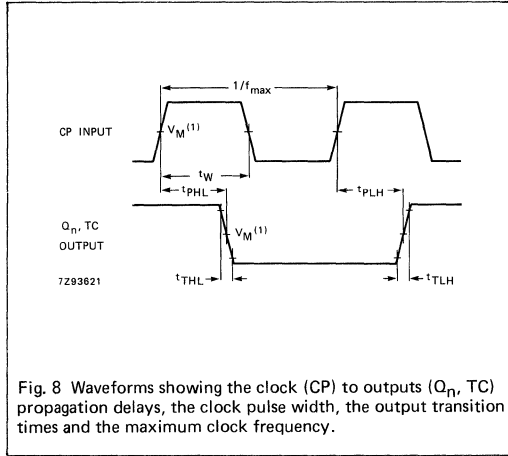
INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
MR	0.95	D <sub>n</sub>	0.25
CP	0.80	CET	0.75
CEP	0.25	PE	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		23	43		54		65	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		29	46		58		69	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC		30	51		64		77	ns	4.5	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t <sub>W</sub>	clock pulse width HIGH or LOW	22	7		28		33		ns	4.5	Fig. 8
t <sub>W</sub>	master reset pulse width; LOW	20	10		25		30		ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to CP	20	6		25		30		ns	4.5	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	18	8		23		27		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time PE to CP	30	17		38		45		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time CEP, CET to CP	40	17		50		60		ns	4.5	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET to CP	0	-7		0		0		ns	4.5	Figs 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	23	41		18		15		MHz	4.5	Fig. 8

AC WAVEFORMS



**Note to Figs 11 and 12**  
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Note to AC waveforms**  
(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND}$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND}$  to  $3V$ .

PRESETTABLE SYNCHRONOUS BCD DECADE COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT162 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT162 are synchronous presettable decade counters which feature an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "162" the clear function is synchronous.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub>	propagation delay CP to Q <sub>n</sub> CP to TC CET to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	18	20	ns
			21	26	ns
			11	15	ns
t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC CET to TC		18	20	ns
			21	19	ns
			11	10	ns
f <sub>max</sub>	maximum clock frequency	63	32	MHz	
C <sub>I</sub>	input capacitance	3.5	3.5	pF	
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	37	37	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

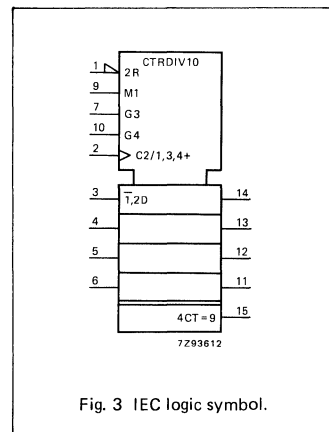
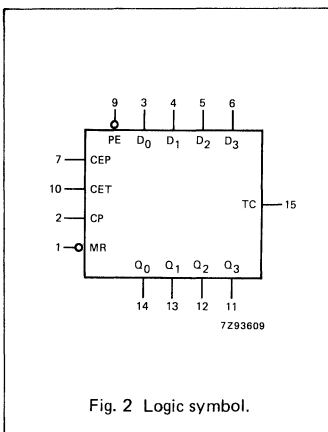
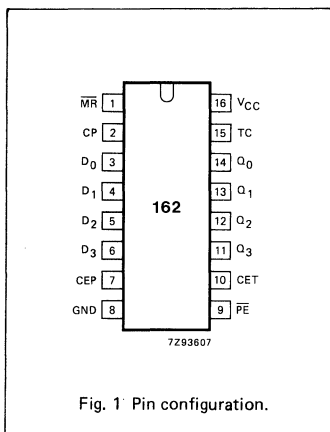
- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT162P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT162T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

(continued on next page)





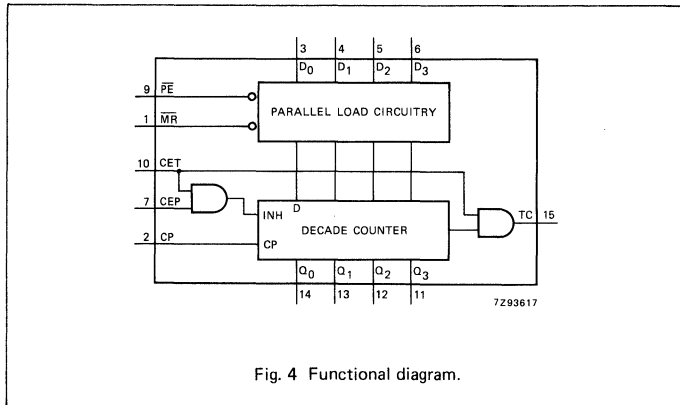


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

A LOW level at the master reset input ( $\overline{MR}$ ) sets all four outputs of the flip-flops ( $Q_0$  to  $Q_3$ ) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for  $\overline{MR}$  are met). This action occurs regardless of the levels at  $\overline{PE}$ , CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of  $Q_0$ . This pulse can be used to enable the next cascaded stage.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	$D_0$ to $D_3$	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
11, 12, 13, 14	$Q_0$ to $Q_3$	flip-flop outputs
15	TC	terminal count output
16	$V_{CC}$	positive supply voltage

**FUNCTION TABLE**

OPERATING MODE	INPUTS					OUTPUTS		
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	$D_n$	$Q_n$	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	$q_n$	*
	h	X	X	l	h	X	$q_n$	L

**Note to function table**

\* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition

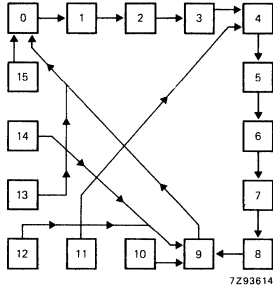


Fig. 5 State diagram.

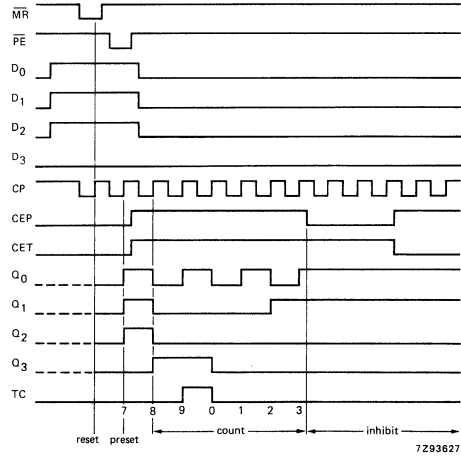


Fig. 6 Typical timing sequence: reset outputs to zero; preset to BCD seven; count to eight, nine, zero, one, two and three; inhibit.

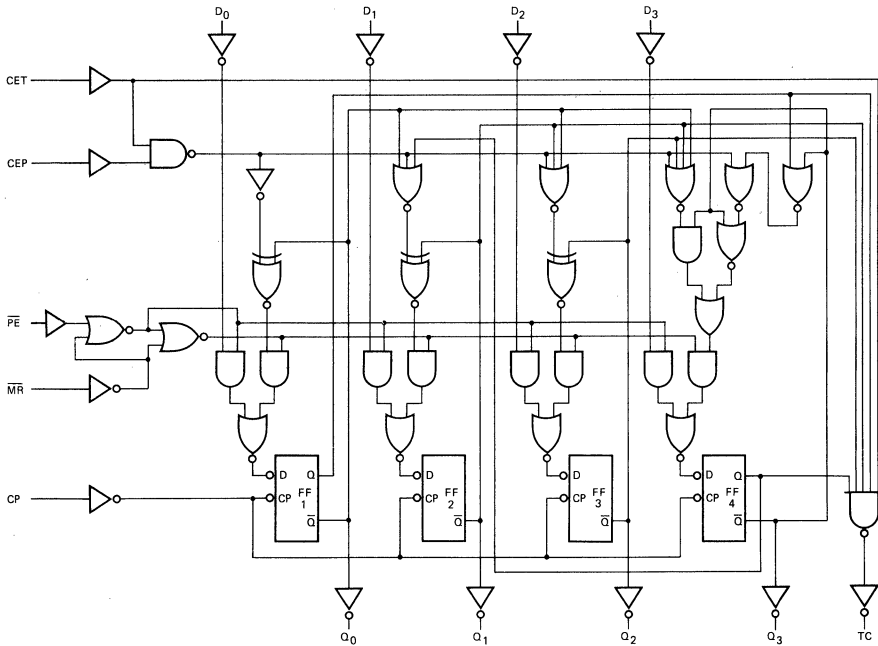


Fig. 7 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		58 21 17	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time MR, D <sub>n</sub> to CP	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 10 and 11
t <sub>su</sub>	set-up time PE to CP	135 27 23	39 14 11		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	175 35 30	58 21 17		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, MR to CP	0 0 0	-22 -8 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95	$D_n$	0.25
CP	0.80	CET	1.05
CEP	0.25	PE	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		24	43		54		65	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay CP to TC		30	51		64		77	ns	4.5	Fig. 8
t <sub>PLH</sub>	propagation delay CP to TC		22	45		56		68	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay CET to TC		18	35		44		53	ns	4.5	Fig. 9
t <sub>PLH</sub>	propagation delay CET to TC		12	24		30		36	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t <sub>W</sub>	clock pulse width HIGH or LOW	31	7		39		47		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	20	9		25		30		ns	4.5	Fig. 10
t <sub>su</sub>	set-up time PE to CP	35	16		44		53		ns	4.5	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	40	23		50		60		ns	4.5	Fig. 12
t <sub>su</sub>	set-up time MR to CP	20	12		25		30		ns	4.5	Fig. 11
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, MR to CP	0	-10		0		0		ns	4.5	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	17	29		14		11		MHz	4.5	Fig. 8

AC WAVEFORMS

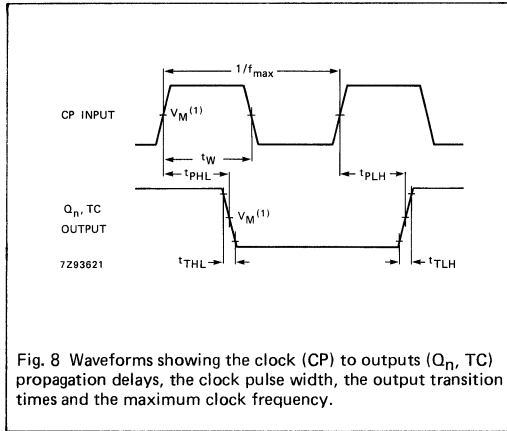


Fig. 8 Waveforms showing the clock (CP) to outputs (Q<sub>n</sub>, TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

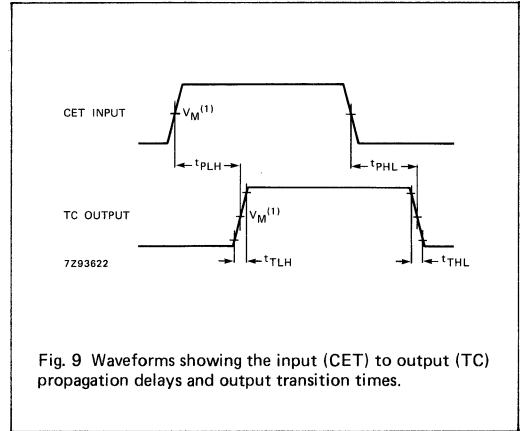


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

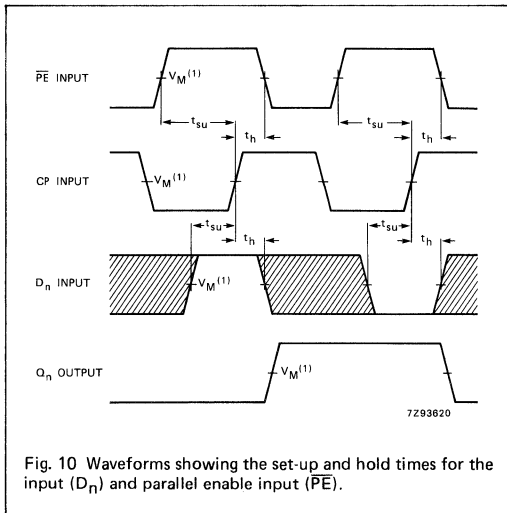


Fig. 10 Waveforms showing the set-up and hold times for the input (D<sub>n</sub>) and parallel enable input (PE).

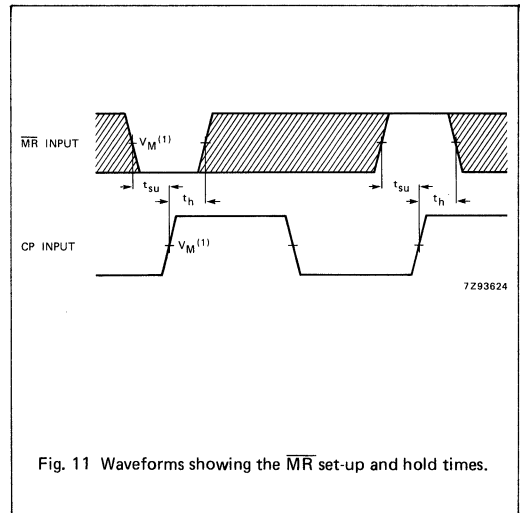


Fig. 11 Waveforms showing the  $\overline{MR}$  set-up and hold times.

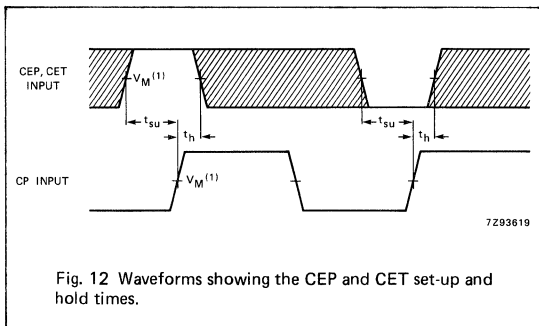


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

**Note to Figs 10, 11 and 12**

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Note to AC waveforms**

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND}$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3\text{V}$ ;  $V_I = \text{GND}$  to 3V.

## PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; SYNCHRONOUS RESET

## FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting.

Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC CET to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	20	ns
			21	25	ns
			11	14	ns
f <sub>max</sub>	maximum clock frequency		51	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

## Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$$f_i = \text{input frequency in MHz} \quad C_L = \text{output load capacitance in pF}$$

$$f_o = \text{output frequency in MHz} \quad V_{CC} = \text{supply voltage in V}$$

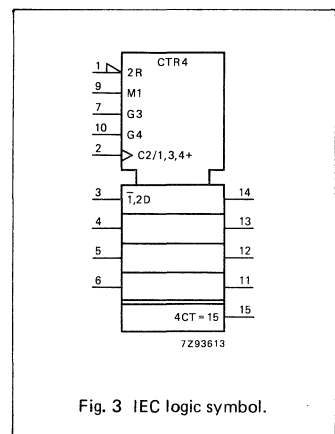
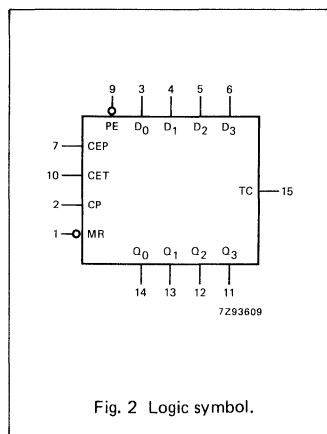
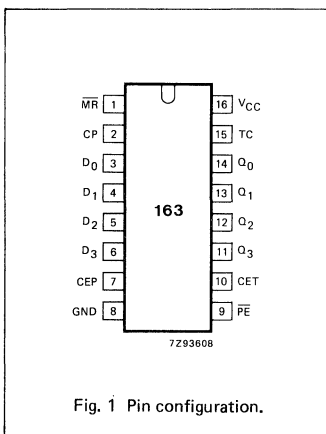
$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT163P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT163T: 16-lead mini-pack; plastic (SO-16; SOT-109A).



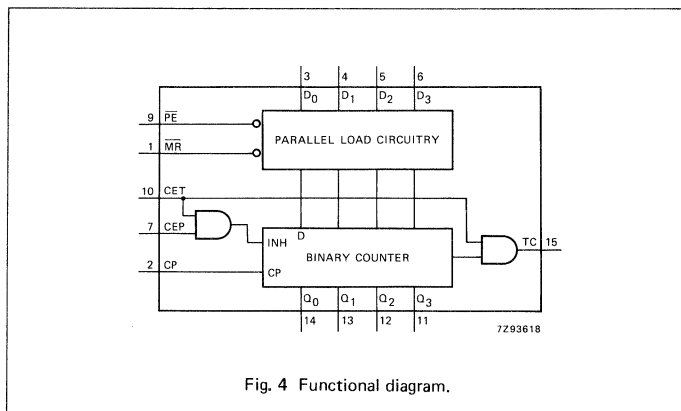


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

A LOW level at the master reset input ( $\overline{MR}$ ) sets all four outputs of the flip-flops ( $Q_0$  to  $Q_3$ ) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for  $\overline{MR}$  are met). This action occurs regardless of the levels at  $\overline{PE}$ , CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of  $Q_0$ . This pulse can be used to enable the next cascaded stage.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	$D_0$ to $D_3$	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	$Q_0$ to $Q_3$	flip-flop outputs
15	TC	terminal count output
16	$V_{CC}$	positive supply voltage

**FUNCTION TABLE**

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	$D_n$	$Q_n$	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	$q_n$	*
	h	X	X	l	h	X	$q_n$	L

**Note to function table**

\* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level

h = HIGH voltage level one set-up-time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition

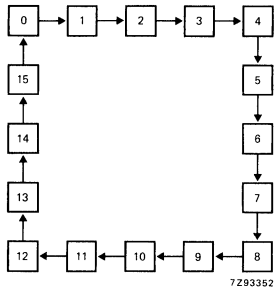


Fig. 5 State diagram.

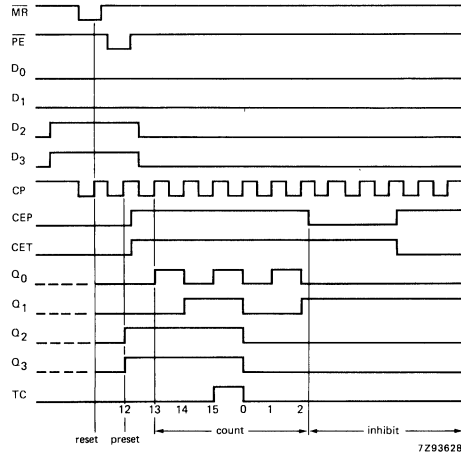


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

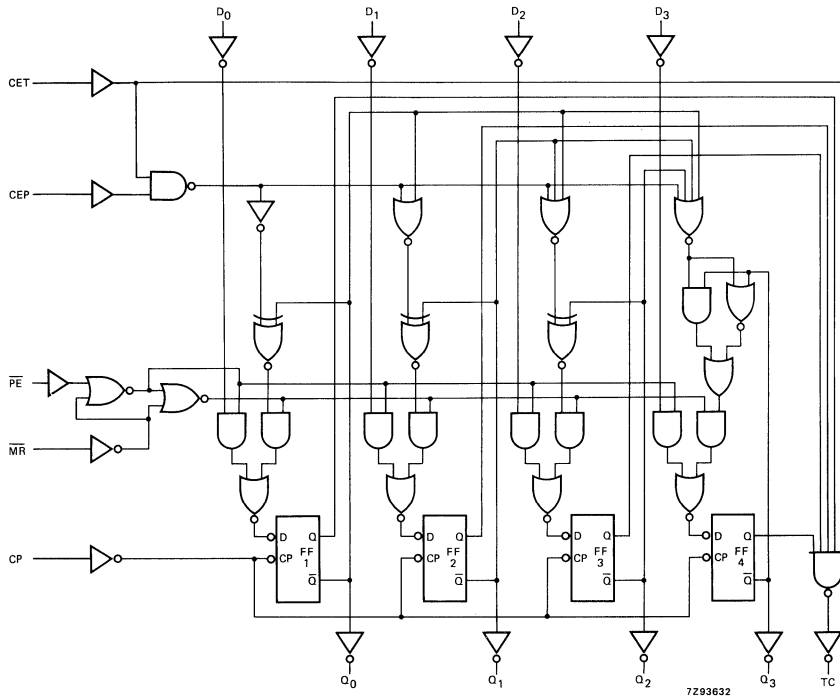


Fig. 7 Logic diagram.



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		55 20 16	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		320 65 55	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t <sub>W</sub>	clock pulse width HIGH or LOW	90 18 15	17 6 5		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time MR, D <sub>n</sub> to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t <sub>su</sub>	set-up time PE to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	110 22 19	36 13 10		140 28 24		165 33 28		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, MR to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	5 27 32	15 46 55		4 22 26		4 18 21		MHz	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95	$D_n$	0.25
CP	1.10	CET	0.75
CEP	0.25	PE	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		23	43		54		65	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		29	49		61		74	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t <sub>W</sub>	clock pulse width HIGH or LOW	22	6		28		33		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time $\overline{MR}$ , D <sub>n</sub> to CP	20	8		25		30		ns	4.5	Figs 10 and 11
t <sub>su</sub>	set-up time PE to CP	20	11		25		30		ns	4.5	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	30	15		38		45		ns	4.5	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, $\overline{MR}$ to CP	0	-5		0		0		ns	4.5	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	26	45		21		17		MHz	4.5	Fig. 8

AC WAVEFORMS

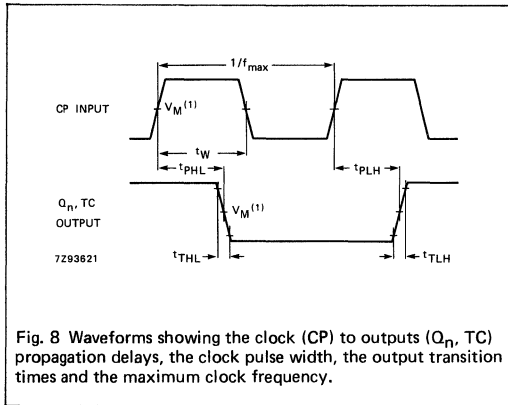


Fig. 8 Waveforms showing the clock (CP) to outputs ( $Q_n$ , TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

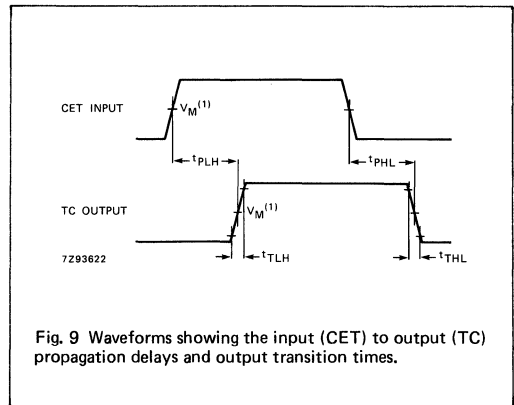


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

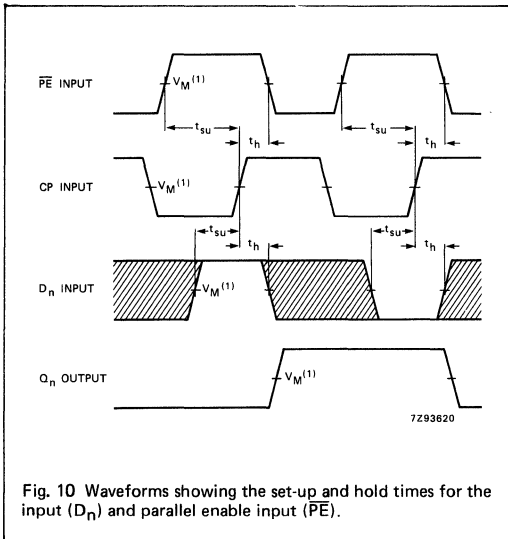


Fig. 10 Waveforms showing the set-up and hold times for the input ( $D_n$ ) and parallel enable input (PE).

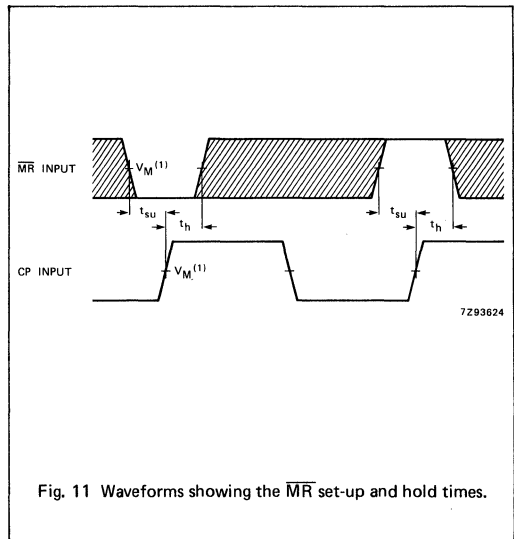


Fig. 11 Waveforms showing the  $\overline{MR}$  set-up and hold times.

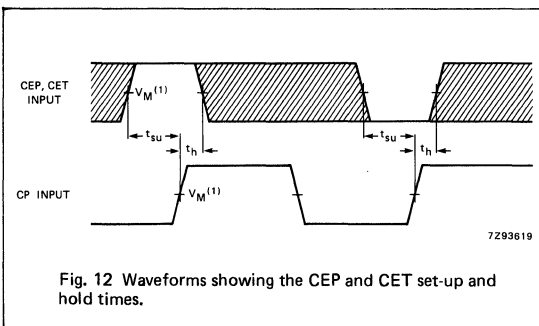


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## 8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

### FEATURES

- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT164 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages.

Data is entered serially through one of two inputs (D<sub>sa</sub> or D<sub>sb</sub>); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q<sub>0</sub>, which is the logical AND of the two data inputs (D<sub>sa</sub>, D<sub>sb</sub>) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> $\overline{MR}$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12 11	14 16	ns ns
f <sub>max</sub>	maximum clock frequency		78	61	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

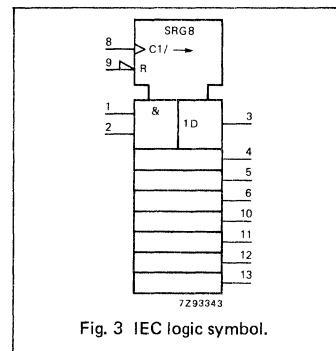
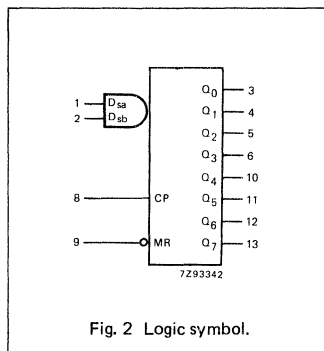
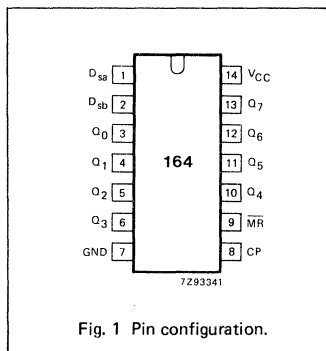
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT164P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT164T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D <sub>sa</sub> , D <sub>sb</sub>	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q <sub>0</sub> to Q <sub>7</sub>	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V <sub>CC</sub>	positive supply voltage



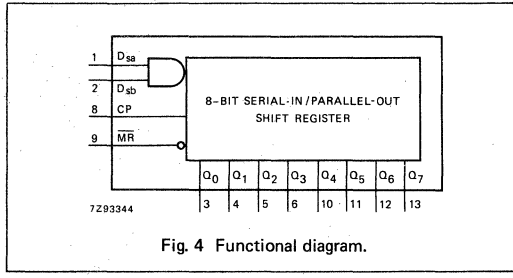


Fig. 4 Functional diagram.

**APPLICATIONS**

- Serial data transfer

**FUNCTION TABLE**

OPERATING MODES	INPUTS				OUTPUTS	
	MR	CP	D <sub>sa</sub>	D <sub>sb</sub>	Q <sub>0</sub>	Q <sub>1</sub> - Q <sub>7</sub>
reset (clear)	L	X	X	X	L	L - L
shift	H	↑	l	l	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	l	h	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	h	l	L	q <sub>0</sub> - q <sub>6</sub>
	H	↑	h	h	H	q <sub>0</sub> - q <sub>6</sub>

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition<sup>5</sup>  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition  
↑ = LOW-to-HIGH clock transition

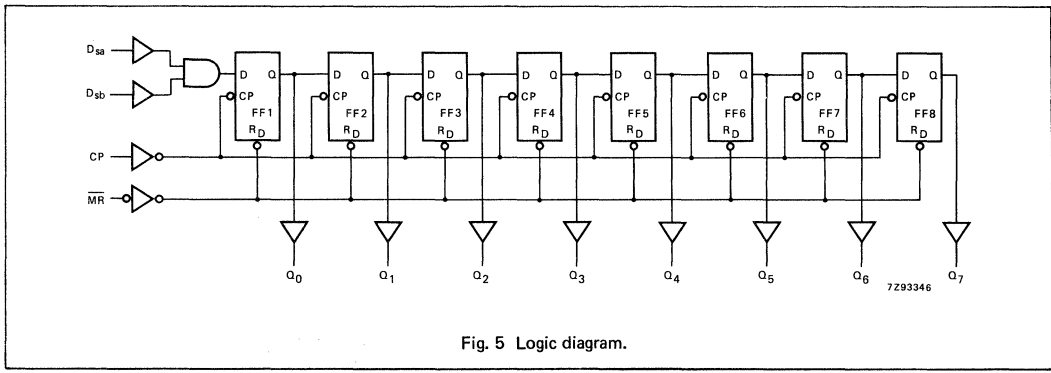


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		41 15 12	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width; LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time MR to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time D <sub>sa</sub> , D <sub>sb</sub> to CP	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>sa</sub> , D <sub>sb</sub> to CP	4 4 4	-6 -2 -2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	23 71 85		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{OC}$  category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$D_{sa}, D_{sb}$	0.25
CP	0.60
MR	0.90

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$		17	36		45		54	ns	4.5	Fig. 6
$t_{PHL}$	propagation delay MR to $Q_n$		19	38		48		57	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6
$t_W$	clock pulse width HIGH or LOW	18	7		23		27		ns	4.5	Fig. 6
$t_W$	master reset pulse width; LOW	18	7		23		27		ns	4.5	Fig. 7
$t_{rem}$	removal time MR to CP	16	7		20		24		ns	4.5	Fig. 7
$t_{su}$	set-up time $D_{sa}, D_{sb}$ to CP	12	6		15		18		ns	4.5	Fig. 8
$t_h$	hold time $D_{sa}, D_{sb}$ to CP	4	-2		4		4		ns	4.5	Fig. 8
$f_{max}$	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

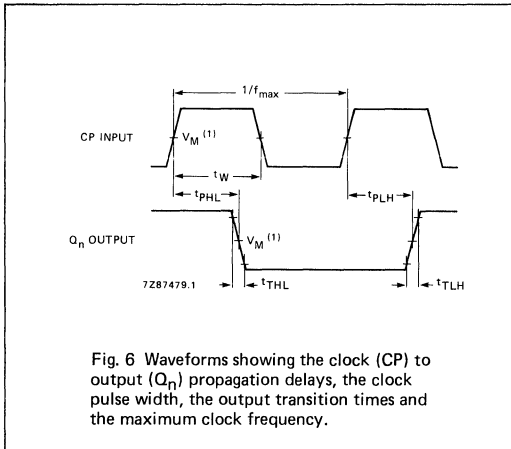


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

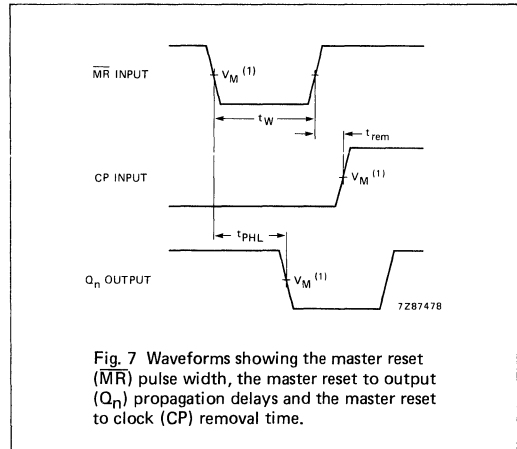


Fig. 7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.

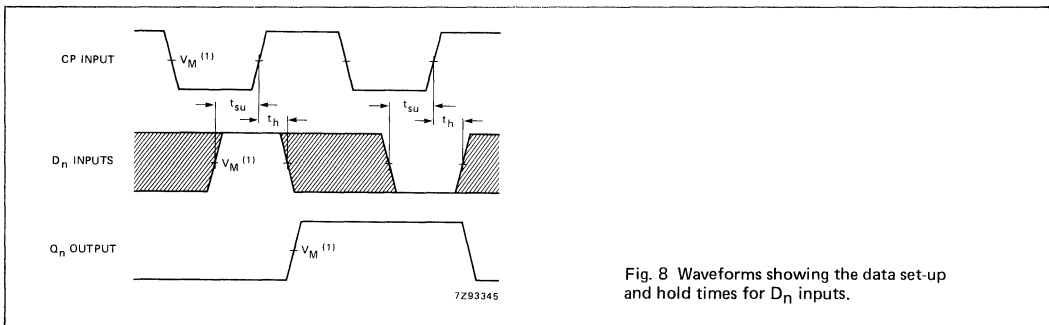


Fig. 8 Waveforms showing the data set-up and hold times for  $D_n$  inputs.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I<sup>2</sup>C category: MSI

GENERAL DESCRIPTION

The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs (Q<sub>7</sub> and  $\bar{Q}_7$ ) available from the last stage. When the parallel load ( $\bar{P}L$ ) input is LOW, parallel data from the D<sub>0</sub> to D<sub>7</sub> inputs are loaded into the register asynchronously.

When  $\bar{P}L$  is HIGH, data enters the register serially at the D<sub>S</sub> input and shifts one place to the right (Q<sub>0</sub> → Q<sub>1</sub> → Q<sub>2</sub>, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q<sub>7</sub> output to the D<sub>S</sub> input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ( $\bar{C}E$ ) input. The pin assignment for the CP and  $\bar{C}E$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input  $\bar{C}E$  should only take place while CP HIGH for predictable operation. Also, the CP and  $\bar{C}E$  should be LOW before the LOW-to-HIGH transition of  $\bar{P}L$  to prevent shifting the data when  $\bar{P}L$  is released.

APPLICATIONS

- Parallel-to-serial data conversion

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	16	14	ns
	CP to Q <sub>7</sub> , $\bar{Q}_7$		15	17	ns
	$\bar{P}L$ to Q <sub>7</sub> , $\bar{Q}_7$ D <sub>7</sub> to Q <sub>7</sub> , $\bar{Q}_7$		11	11	ns
f <sub>max</sub>	maximum clock frequency		56	48	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	35	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

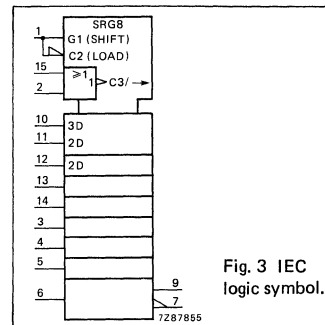
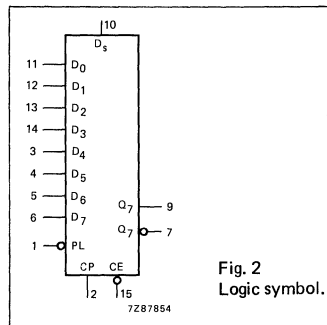
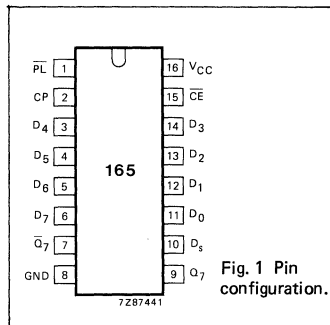
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT165P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT165T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{P}L$	asynchronous parallel load input (active LOW)
7	$\bar{Q}_7$	complementary output from the last stage
9	Q <sub>7</sub>	serial output from the last stage
2	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
10	D <sub>S</sub>	serial data input
11, 12, 13, 14, 3, 4, 5, 6	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
15	$\bar{C}E$	clock enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage



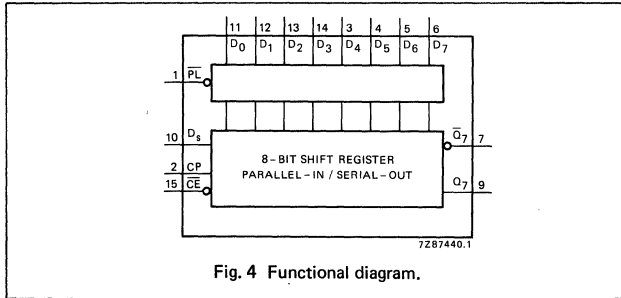


Fig. 4 Functional diagram.

**FUNCTION TABLE**

OPERATING MODES	INPUTS				$Q_n$ REGISTERS			OUTPUTS	
	PL	CE	CP	Ds	D <sub>0</sub> -D <sub>7</sub>	Q <sub>0</sub>	Q <sub>1</sub> -Q <sub>6</sub>	Q <sub>7</sub>	$\bar{Q}_7$
parallel load	L	X	X	X	L	L	L - L	L	H
serial shift	H	L	↑	l	X	L	q <sub>0</sub> -q <sub>5</sub>	q <sub>6</sub>	$\bar{q}_6$
	H	L	↑	h	X	H	q <sub>0</sub> -q <sub>5</sub>	q <sub>6</sub>	$\bar{q}_6$
hold "do nothing"	H	H	X	X	X	q <sub>0</sub>	q <sub>1</sub> -q <sub>6</sub>	q <sub>7</sub>	q <sub>7</sub>

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition  
X = don't care  
↑ = LOW-to-HIGH clock transition

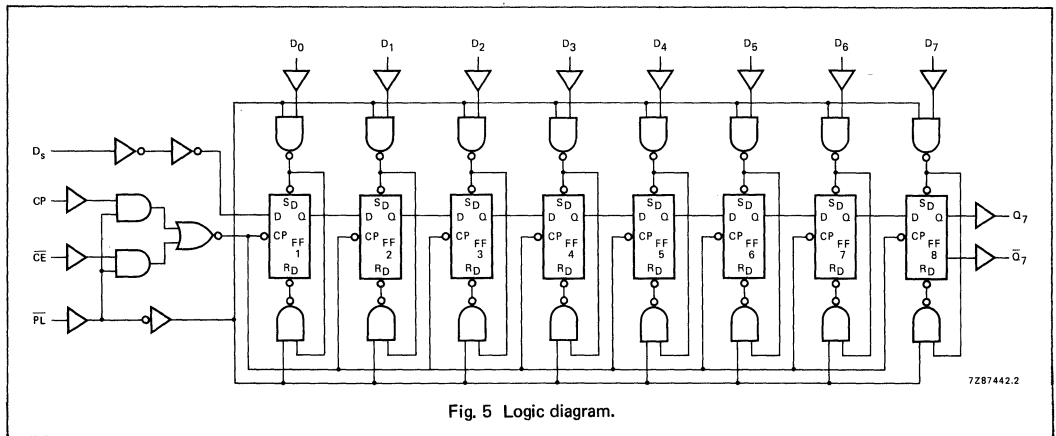


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CE, CP to Q <sub>7</sub> , $\bar{Q}_7$		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{P}L$ to Q <sub>7</sub> , $\bar{Q}_7$		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q <sub>7</sub> , $\bar{Q}_7$		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	parallel load pulse width; LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time D <sub>s</sub> to CP, $\bar{C}E$	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>su</sub>	set-up time $\bar{P}L$ to CP, $\bar{C}E$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t <sub>su(L)</sub>	set-up time $\bar{C}E$ to CP; CP to $\bar{C}E$	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to $\bar{P}L$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t <sub>h</sub>	hold time D <sub>s</sub> to CP, $\bar{C}E$ D <sub>n</sub> to $\bar{P}L$	5 5 5	-3 -1 -1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9
t <sub>h</sub>	hold time $\bar{P}L$ , $\bar{C}E$ to CP $\bar{P}L$ , CP to $\bar{C}E$	35 7 6	-3 -1 -1		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 9
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	17 51 61		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
D <sub>0</sub> to D <sub>7</sub>	0.35
D <sub>s</sub>	0.35
CP	0.65
$\overline{CE}$	0.65
PL	0.65

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CE}$ , CP to $Q_7, \overline{Q}_7$		17	34		43		51	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $\overline{PL}$ to $Q_7, \overline{Q}_7$		20	40		50		60	ns	4.5	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay $D_7$ to $Q_7, \overline{Q}_7$		14	28		35		42	ns	4.5	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 6
$t_W$	clock pulse width HIGH or LOW	20	8		25		30		ns	4.5	Fig. 6
$t_W$	parallel load pulse width; LOW	20	9		25		30		ns	4.5	Fig. 7
$t_{su}$	set-up time $D_s$ to CP, $\overline{CE}$	20	2		25		30		ns	4.5	Fig. 9
$t_{su}$	set-up time $\overline{PL}$ to CP, $\overline{CE}$	20	8		25		30		ns	4.5	Fig. 7
$t_{su}(L)$	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	20	7		25		30		ns	4.5	Fig. 9
$t_{su}$	set-up time $D_n$ to $\overline{PL}$	20	10		25		30		ns	4.5	Fig. 10
$t_h$	hold time $D_s$ to CP, $\overline{CE}$ ; $D_n$ to $\overline{PL}$	7	-1		9		11		ns	4.5	Fig. 9
$t_h$	hold time $\overline{PL}$ , $\overline{CE}$ to CP; $\overline{PL}$ , CP to $\overline{CE}$	0	-7		0		0		ns	4.5	Fig. 9
$f_{max}$	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig. 6

AC WAVEFORMS

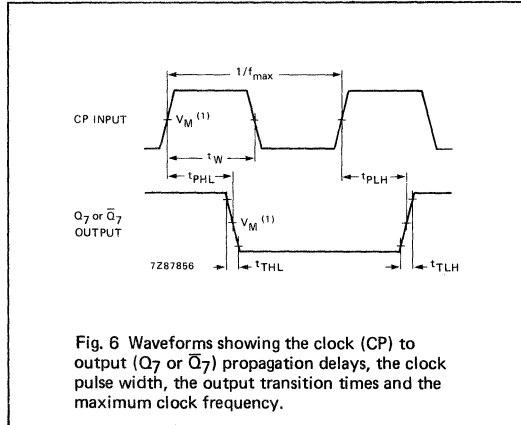


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

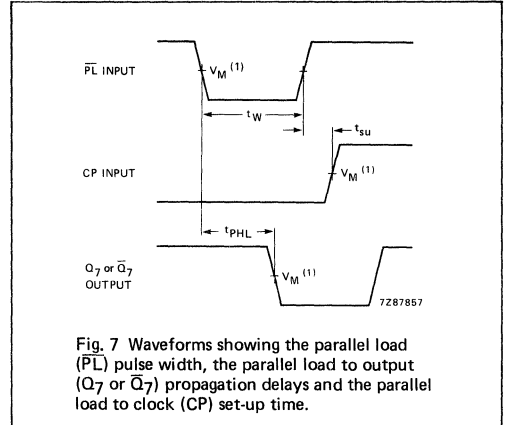


Fig. 7 Waveforms showing the parallel load (PL) pulse width, the parallel load to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays and the parallel load to clock (CP) set-up time.

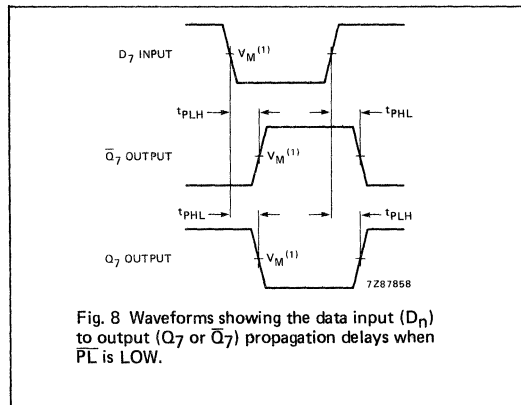


Fig. 8 Waveforms showing the data input ( $D_n$ ) to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays when  $\bar{PL}$  is LOW.

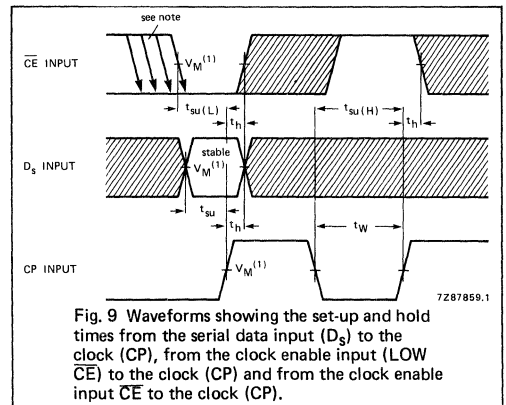


Fig. 9 Waveforms showing the set-up and hold times from the serial data input ( $D_5$ ) to the clock (CP), from the clock enable input (LOW  $\bar{CE}$ ) to the clock (CP) and from the clock enable input  $CE$  to the clock (CP).

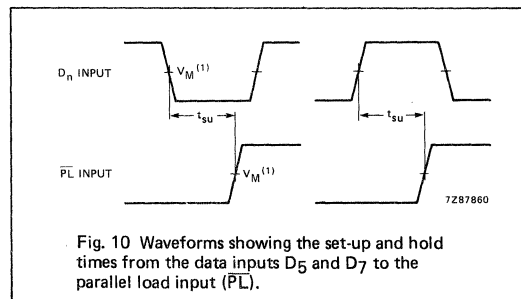


Fig. 10 Waveforms showing the set-up and hold times from the data inputs  $D_5$  and  $D_7$  to the parallel load input ( $\bar{PL}$ ).

Note to Figs 6 and 7

The changing to output assumes internal  $Q_6$  opposite state from  $Q_7$ .

Note to Fig. 9

$\bar{CE}$  may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_1 = GND$  to  $V_{CC}$ .

HCT:  $V_M = 1.3V$ ;  $V_1 = GND$  to  $3V$ .

8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

FEATURES

- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous master reset
- For asynchronous parallel data load see "165"
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by an active LOW parallel enable ( $\overline{PE}$ ) input. When  $\overline{PE}$  is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When  $\overline{PE}$  is HIGH, data is entered into the internal bit position  $Q_0$  from serial data input ( $D_s$ ), and the remaining bits are shifted one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the  $Q_7$  output to the  $D_s$  input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input  $\overline{CE}$  should only take place while CP is HIGH for predictable operation. A LOW on the master reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>7</sub> MR to Q <sub>7</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	20	ns
			14	19	ns
f <sub>max</sub>	maximum clock frequency		63	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	41	41	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT166P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT166T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	D <sub>s</sub>	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
6	$\overline{CE}$	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
13	Q <sub>7</sub>	serial output from the last stage
15	$\overline{PE}$	parallel enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

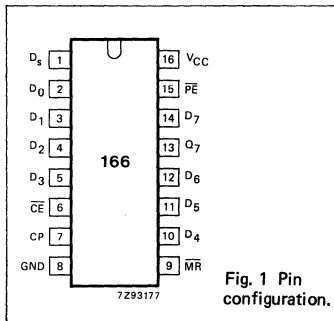


Fig. 1 Pin configuration.

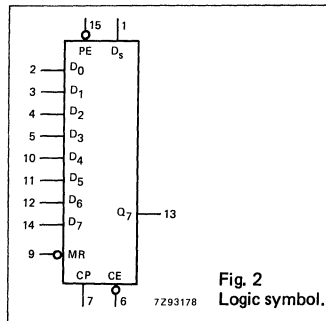


Fig. 2 Logic symbol.

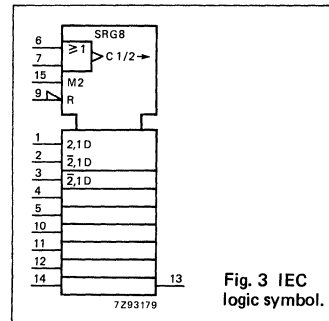


Fig. 3 IEC logic symbol.



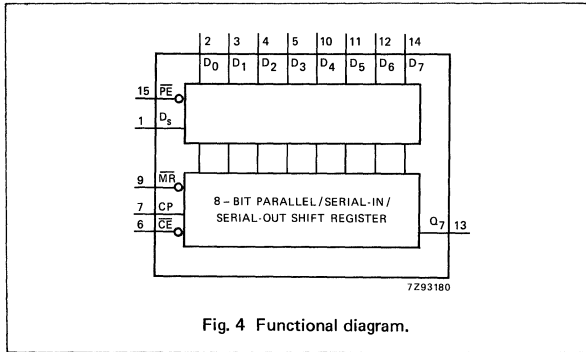


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q <sub>n</sub> REGISTER		OUTPUT
	PE	CE	CP	D <sub>s</sub>	D <sub>0</sub> -D <sub>7</sub>	Q <sub>0</sub>	Q <sub>1</sub> -Q <sub>6</sub>	Q <sub>7</sub>
parallel load	l	l	↑	X	l - l h - h	L H	L - L H - H	L H
serial shift	h	l	↑	l	X - X X - X	L H	q <sub>0</sub> -q <sub>5</sub> q <sub>0</sub> -q <sub>5</sub>	q <sub>6</sub> q <sub>6</sub>
hold "do nothing"	X	h	X	X	X - X	q <sub>0</sub>	q <sub>1</sub> -q <sub>6</sub>	q <sub>7</sub>

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition  
X = don't care  
↑ = LOW-to-HIGH CP transition

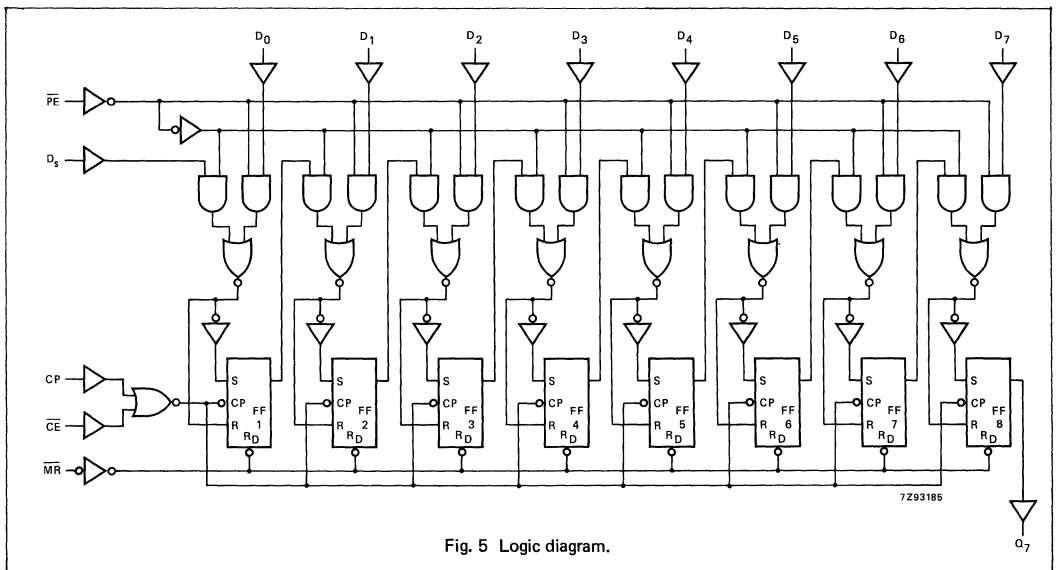


Fig. 5 Logic diagram.

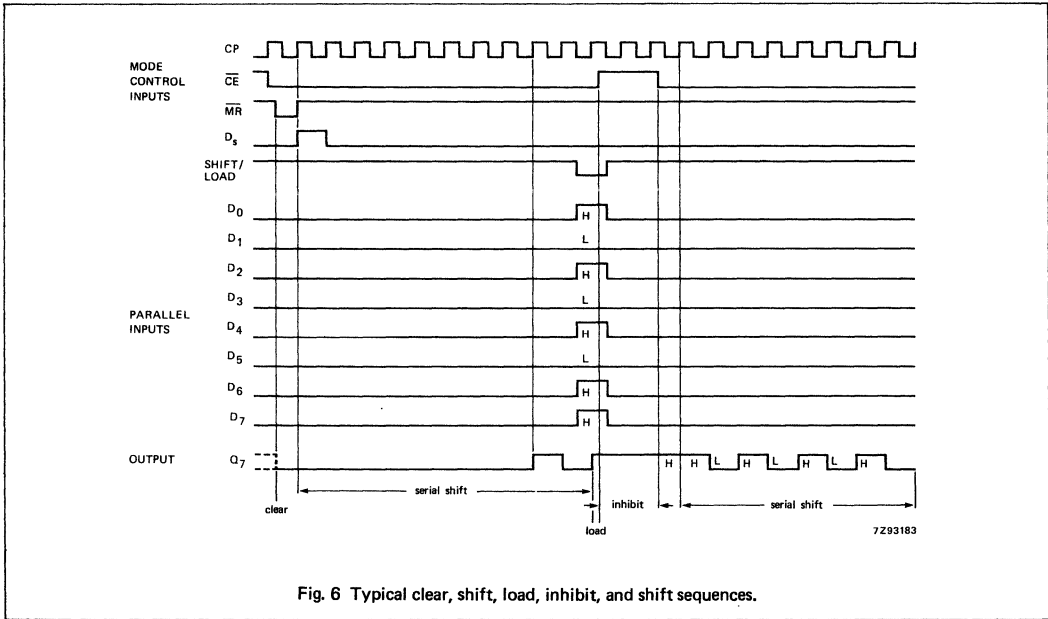


Fig. 6 Typical clear, shift, load, inhibit, and shift sequences.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>7</sub>		50	150		190		225	ns	2.0 4.5 6.0	Fig. 7
			18	30		38		45			
			14	26		33		38			
t <sub>PHL</sub>	propagation delay MR to Q <sub>7</sub>		47	160		200		240	ns	2.0 4.5 6.0	Fig. 8
			17	32		40		48			
			14	27		34		44			
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19	75		95		110	ns	2.0 4.5 6.0	Fig. 7
			7	15		19		22			
			6	13		16		19			
t <sub>W</sub>	clock pulse width HIGH or LOW	80	17		100		120	ns	2.0 4.5 6.0	Fig. 7	
		16	6		20		24				
		14	5		17		20				
t <sub>W</sub>	master reset pulse width	100	25		125		150	ns	2.0 4.5 6.0	Fig. 8	
		20	9		25		30				
		17	7		21		26				
t <sub>rem</sub>	removal time MR to CP	0	-19		0		0	ns	2.0 4.5 6.0	Fig. 8	
		0	-7		0		0				
		0	-6		0		0				
t <sub>su</sub>	set-up time D <sub>n</sub> , CE to CP	80	14		100		120	ns	2.0 4.5 6.0	Fig. 9	
		16	5		20		24				
		14	4		17		20				
t <sub>su</sub>	set-up time PE to CP	100	33		125		150	ns	2.0 4.5 6.0	Fig. 8	
		20	12		25		30				
		17	10		21		26				
t <sub>h</sub>	hold time D <sub>n</sub> , CE to CP	2	-8		2		2	ns	2.0 4.5 6.0	Fig. 8	
		2	-3		2		2				
		2	-2		2		2				
t <sub>h</sub>	hold time PE to CP	0	-28		0		0	ns	2.0 4.5 6.0	Fig. 9	
		0	-10		0		0				
		0	-8		0		0				
f <sub>max</sub>	maximum clock pulse frequency	6.0	19		4.8		4.0	MHz	2.0 4.5 6.0	Fig. 7	
		30	57		24		20				
		35	68		28		24				

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
D <sub>0</sub> to D <sub>7</sub>	0.35
D <sub>s</sub>	0.35
CP	0.80
$\overline{CE}$	0.80
$\overline{MR}$	0.40
$\overline{PE}$	0.60

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay CP to Q <sub>7</sub>		23	40		50		60	ns	4.5	Fig. 7	
$t_{PHL}$	propagation delay $\overline{MR}$ to Q <sub>7</sub>		22	45		56		68	ns	4.5	Fig. 8	
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 7	
$t_W$	clock pulse width HIGH or LOW	20	9		25		30		ns	4.5	Fig. 7	
$t_W$	master reset pulse width	25	11		31		38		ns	4.5	Fig. 8	
$t_{rem}$	removal time $\overline{MR}$ to CP	0	-7		0		0		ns	4.5	Fig. 8	
$t_{su}$	set-up time D <sub>n</sub> , $\overline{CE}$ to CP	16	8		20		24		ns	4.5	Fig. 9	
$t_{su}$	set-up time $\overline{PE}$ to CP	30	15		38		45		ns	4.5	Fig. 8	
$t_h$	hold time D <sub>n</sub> , $\overline{CE}$ to CP	0	-6		0		0		ns	4.5	Fig. 9	
$t_h$	hold time $\overline{PE}$ to CP	0	-13		0		0		ns	4.5	Fig. 9	
$f_{max}$	maximum clock pulse width	25	45		20		17		MHz	4.5	Fig. 7	

AC WAVEFORMS

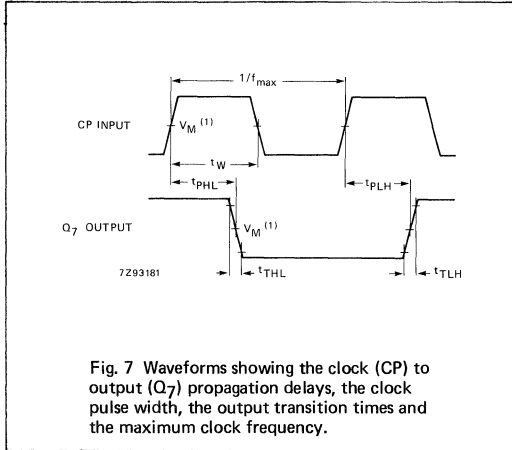


Fig. 7 Waveforms showing the clock (CP) to output (Q<sub>7</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

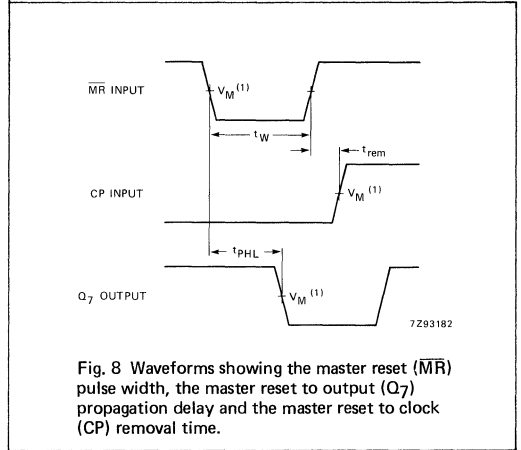


Fig. 8 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output (Q<sub>7</sub>) propagation delay and the master reset to clock (CP) removal time.

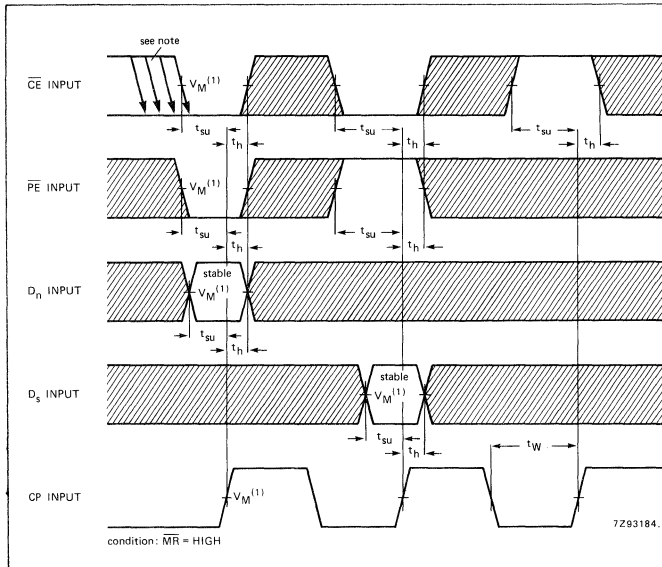


Fig. 9 Waveforms showing the set-up and hold times from the serial data input (D<sub>s</sub>), the data inputs (D<sub>n</sub>), the clock enable input (LOW CE), the clock enable input  $\overline{CE}$  and the parallel enable input to the clock (CP).

Note to Fig. 7

The changing to output assumes internal Q<sub>6</sub> opposite state from Q<sub>7</sub>.

Note to Figs 7, 8 and 9

The number of clock pulses required between the t<sub>PLH</sub> and t<sub>PHL</sub> measurements can be determined from the function table.

Note to Fig. 9

$\overline{CE}$  may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- Gated input enable for hold (do noting) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q<sub>0</sub> to Q<sub>3</sub>) and master reset (MR).

When the two data enable inputs ( $\bar{E}_1$  and  $\bar{E}_2$ ) are LOW, the data on the D<sub>n</sub> inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both  $\bar{E}_n$  inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ( $\bar{OE}_1$  and  $\bar{OE}_2$ ) are LOW, the data in the register is presented to the Q<sub>n</sub> outputs. When one or both  $\bar{OE}_n$  inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the  $\bar{OE}_n$  transition does not affect the clock and reset operations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> MR to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	23 19	22 18	ns ns
f <sub>max</sub>	maximum clock frequency		53	51	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	25	32	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

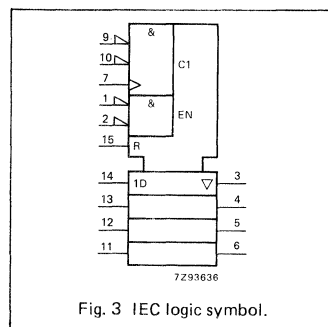
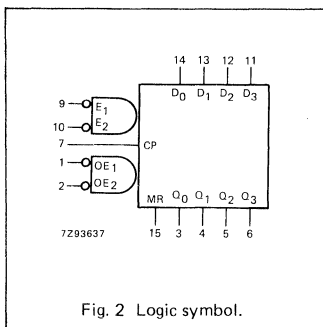
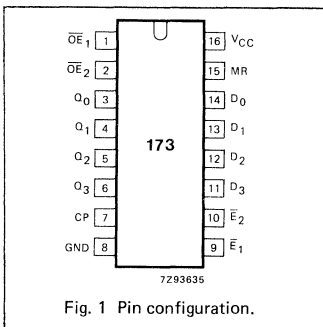
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT173P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT173T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\bar{OE}_1, \bar{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q <sub>0</sub> to Q <sub>3</sub>	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\bar{E}_1, \bar{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D <sub>0</sub> to D <sub>3</sub>	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V <sub>CC</sub>	positive supply voltage



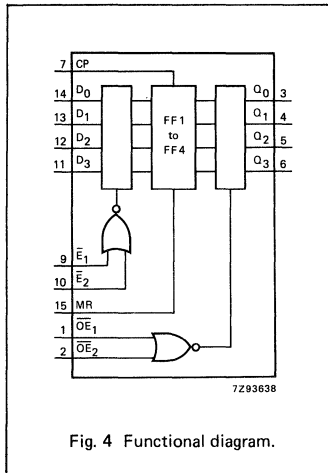


Fig. 4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	E <sub>1</sub>	E <sub>2</sub>	D <sub>n</sub>	Q <sub>n</sub> (register)
reset (clear)	H	X	X	X	X	L
parallel load	L	↑	l	l	l	L H
hold (no change)	L L	X X	h X	X h	X X	q <sub>n</sub> q <sub>n</sub>

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q <sub>n</sub> (register)	OE <sub>1</sub>	OE <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
read	L H	L L	L L	L H	L H	L H	L H
disabled	X X	H X	X H	Z Z	Z Z	Z Z	Z Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
q = lower case letters indicate the state of the referenced input (or output)  
one set-up time prior to the LOW-to-HIGH CP transition  
X = don't care  
Z = high impedance OFF-state  
↑ = LOW-to-HIGH CP transition

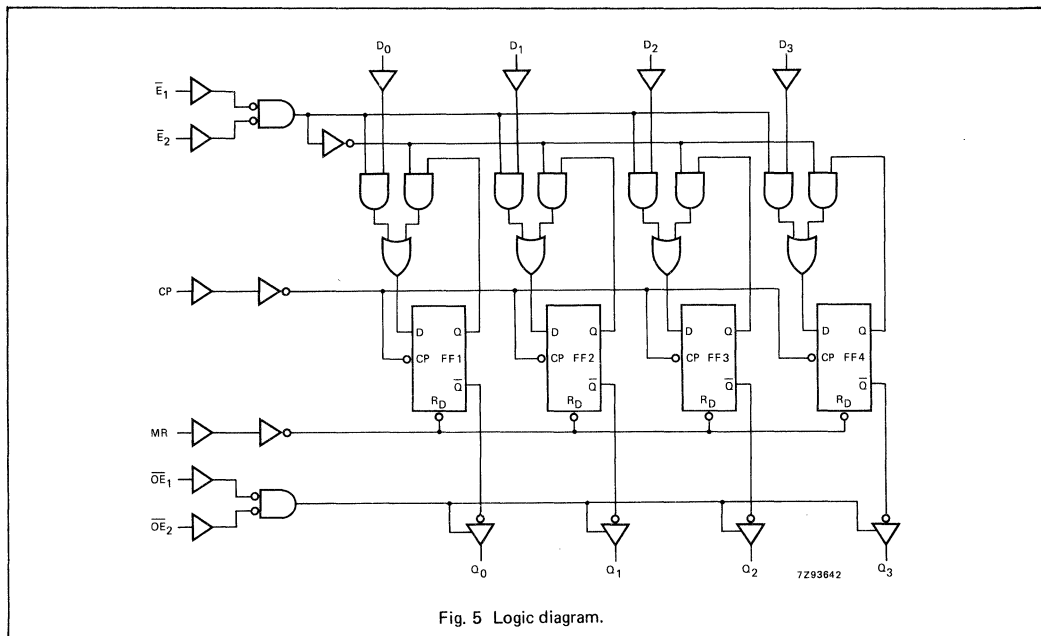


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		74 27 22	225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		61 22 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>n</sub> to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>n</sub> to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	90 18 15	30 11 9		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time MR to CP	75 15 13	-8 -3 -2		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time E <sub>n</sub> to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>h</sub>	hold time E <sub>n</sub> to CP	0 0 0	-28 -10 -8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
f <sub>max</sub>	maximum clock pulse frequency	5.4 27 32	16 48 57		4.4 22 26		3.6 18 21		MHz	2.0 4.5 6.0	Fig. 6



## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1, \overline{OE}_2$	1.00
MR, CP	0.50
$\overline{E}_1, \overline{E}_2$	0.25
D <sub>n</sub>	0.25

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		26	43		54		65	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		21	35		44		53	ns	4.5	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_n$ to Q <sub>n</sub>		17	35		44		53	ns	4.5	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_n$ to Q <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		19	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	11		25		30		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width; HIGH	15	4		19		22		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time MR to CP	15	1		19		22		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time $\overline{E}_n$ to CP	30	16		38		45		ns	4.5	Fig. 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	25	10		31		38		ns	4.5	Fig. 9
t <sub>h</sub>	hold time $\overline{E}_n$ to CP	0	-15		0		0		ns	4.5	Fig. 9
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0	-7		0		0		ns	4.5	Fig. 9
f <sub>max</sub>	maximum clock pulse frequency	25	46		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

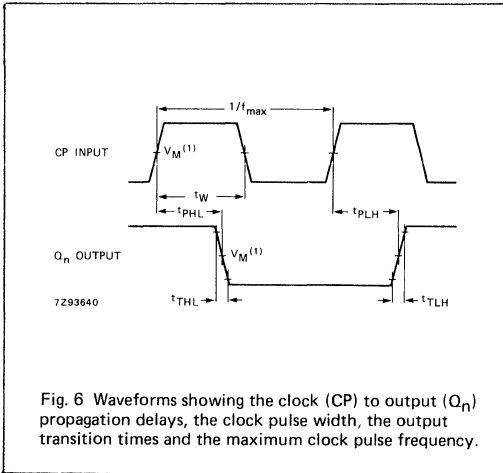


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

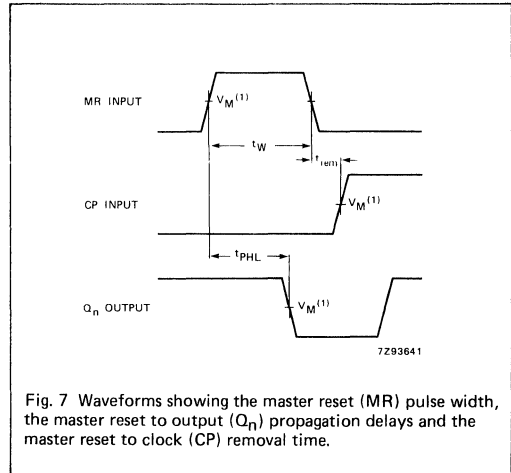


Fig. 7 Waveforms showing the master reset (MR) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.

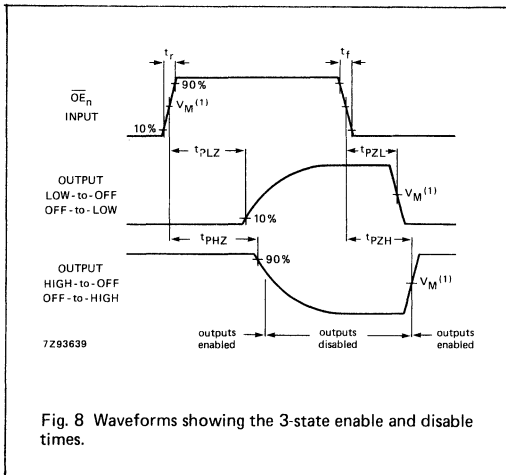


Fig. 8 Waveforms showing the 3-state enable and disable times.

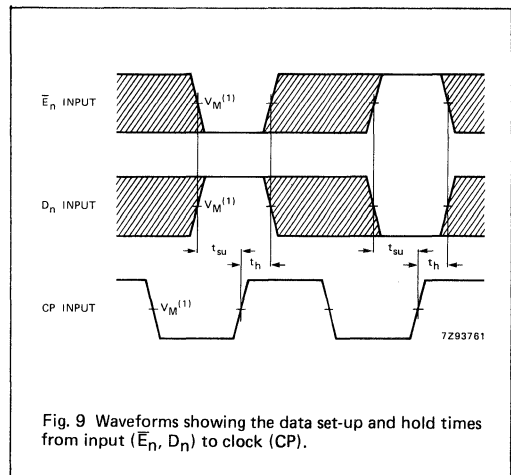


Fig. 9 Waveforms showing the data set-up and hold times from input ( $\overline{E}_n$ ,  $D_n$ ) to clock (CP).

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.



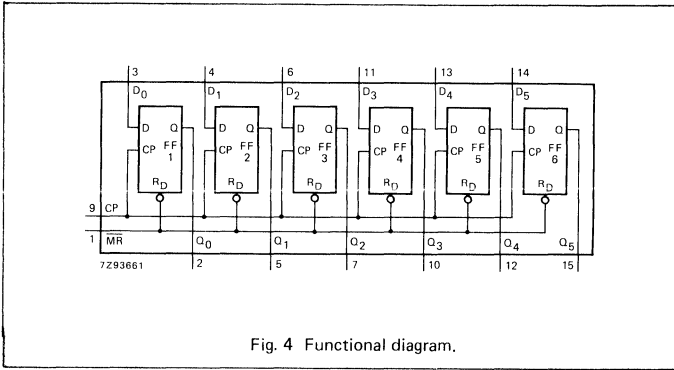


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	MR	CP	D <sub>n</sub>	Q <sub>n</sub>
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition

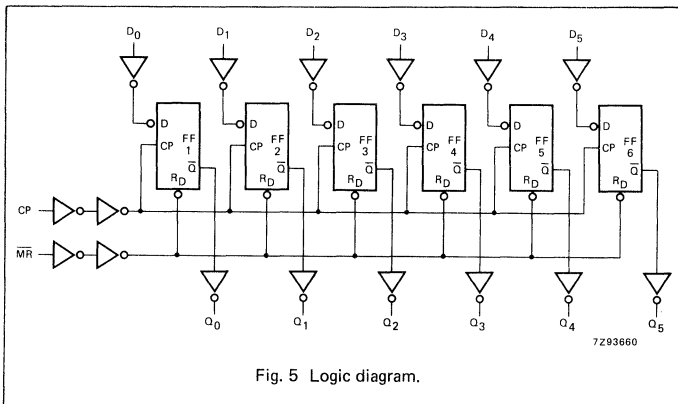


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width; HIGH	80 16 14	12 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time MR to CP	5 5 5	-11 -4 -3		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.25
CP	1.30
MR	1.25

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		21	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		20	35		44		53	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width; HIGH	20	7		25		30		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time MR to CP	12	-3		15		18		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	16	4		20		24		ns	4.5	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5	-3		5		5		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	30	63		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

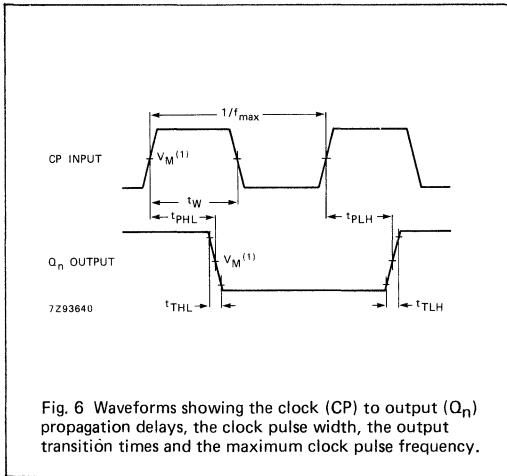


Fig. 6 Waveforms showing the clock (CP) to output (Q<sub>n</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

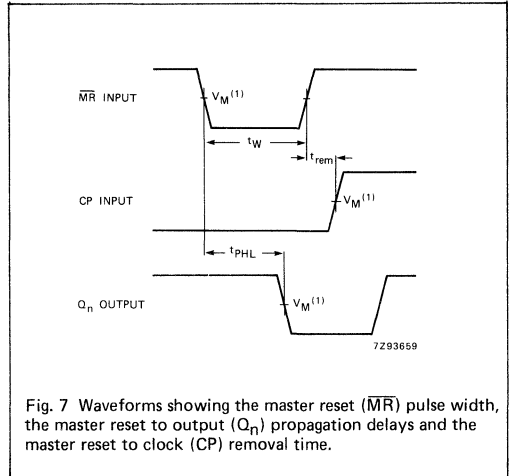


Fig. 7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output (Q<sub>n</sub>) propagation delays and the master reset to clock (CP) removal time.

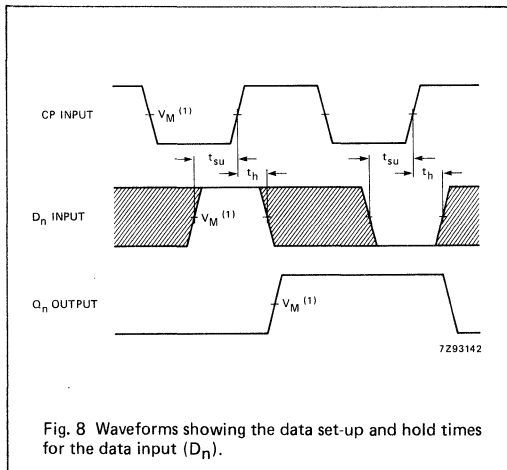


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D<sub>n</sub>).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3V.

QUAD D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Four edge-triggered D flip-flops
- Output capability: standard
- JCC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT175 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT175 have four edge-triggered, D-type flip-flops with individual D inputs and both Q and  $\bar{Q}$  outputs.

The common clock (CP) and master reset ( $\bar{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output ( $Q_n$ ) of the flip-flop.

All  $Q_n$  outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the  $\bar{MR}$  input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}$	propagation delay CP to $Q_n, \bar{Q}_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	17	16	ns
	$\bar{MR}$ to $Q_n, \bar{Q}_n$		15	19	ns
$t_{PLH}$	propagation delay CP to $Q_n, \bar{Q}_n$		17	16	ns
	$\bar{MR}$ to $Q_n, \bar{Q}_n$		15	16	ns
$f_{max}$	maximum clock frequency		83	54	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	32	34	pF

$GND = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t_r = t_f = 6 \text{ ns}$

Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- $f_i$  = input frequency in MHz
- $f_o$  = output frequency in MHz
- $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
- $C_L$  = output load capacitance in pF
- $V_{CC}$  = supply voltage in V

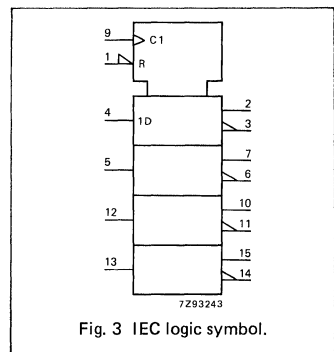
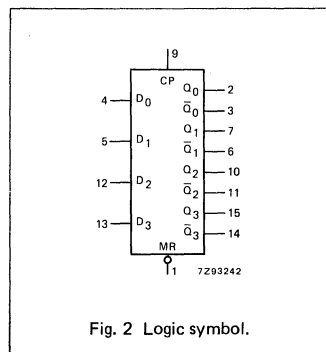
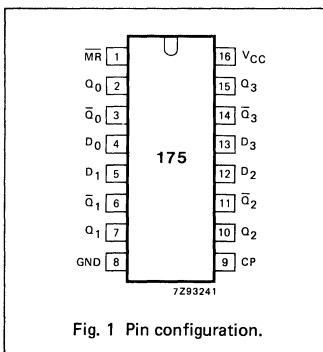
2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

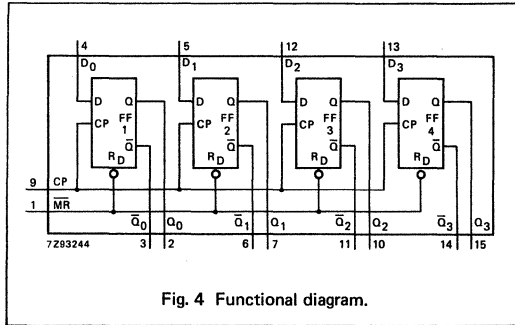
- PC74HC/HCT175P: 16-lead DIL; plastic (SOT-38Z).
- PC74HC/HCT175T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{MR}$	master reset input (active LOW)
2, 7, 10, 15	$Q_0$ to $Q_3$	flip-flop outputs
3, 6, 11, 14	$\bar{Q}_0$ to $\bar{Q}_3$	complementary flip-flop outputs
4, 5, 12, 13	$D_0$ to $D_3$	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	$V_{CC}$	positive supply voltage



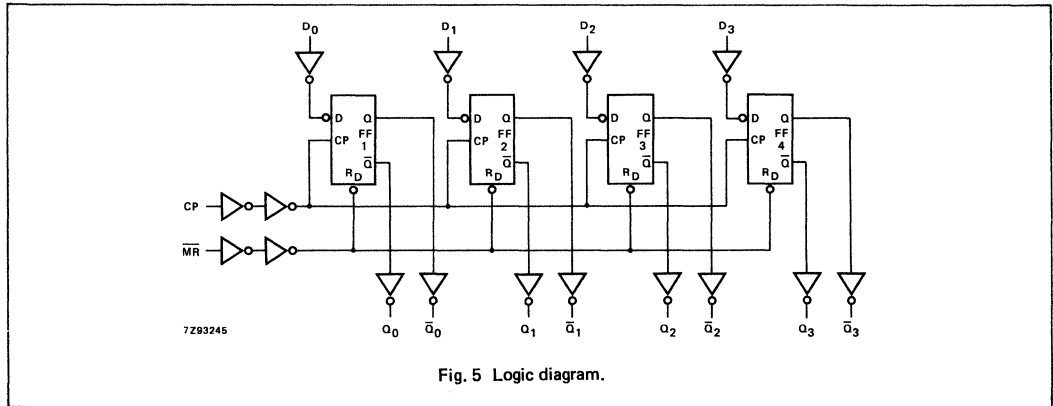




FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	$D_n$	$Q_n$	$\overline{Q}_n$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
↑ = LOW-to-HIGH CP transition  
X = don't care



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> , $\bar{Q}_n$	55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{MR}$ to Q <sub>n</sub> , $\bar{Q}_n$	50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 8
t <sub>rem</sub>	removal time $\bar{MR}$ to CP	5 5 5	-33 -12 -10		5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	80 16 14	3 1 1		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time CP to D <sub>n</sub>	5 5 5	0 0 0		5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	25 75 89		5 24 28		4 20 24	MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
MR	1.00
CP	0.60
D <sub>n</sub>	0.40

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> , $\bar{Q}_n$		19	33		41		50	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		22	38		48		57	ns	4.5	Fig. 8
t <sub>PLH</sub>	propagation delay MR to $\bar{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	12		25		30		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 8
t <sub>rem</sub>	removal time MR to CP	5	-10		5		5		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	16	5		20		24		ns	4.5	Fig. 7
t <sub>h</sub>	hold time CP to D <sub>n</sub>	5	0		5		5		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	25	49		20		17		MHz	4.5	Fig. 6

AC WAVEFORMS

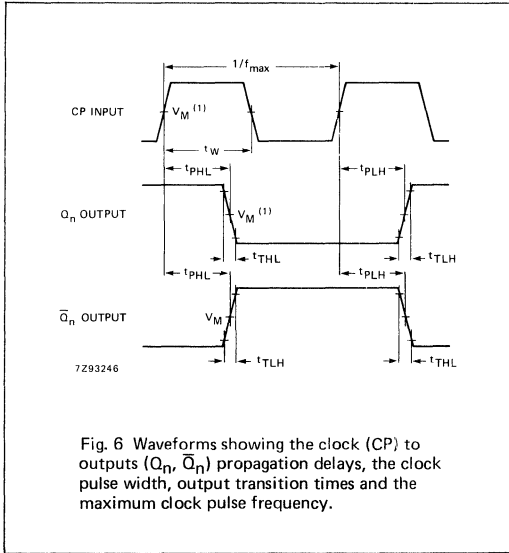


Fig. 6 Waveforms showing the clock (CP) to outputs (Q<sub>n</sub>, Q<sub>n</sub>) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

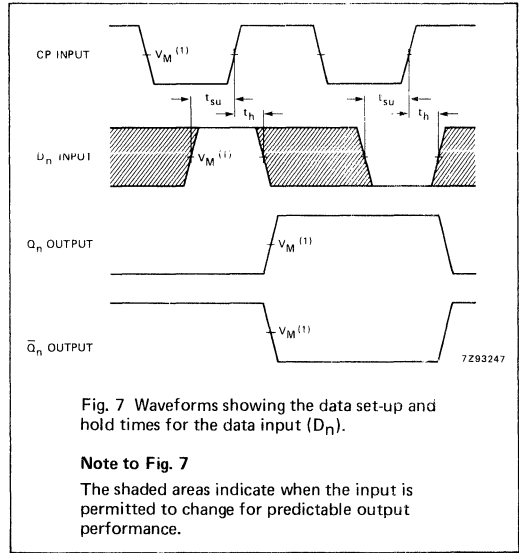


Fig. 7 Waveforms showing the data set-up and hold times for the data input (D<sub>n</sub>).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

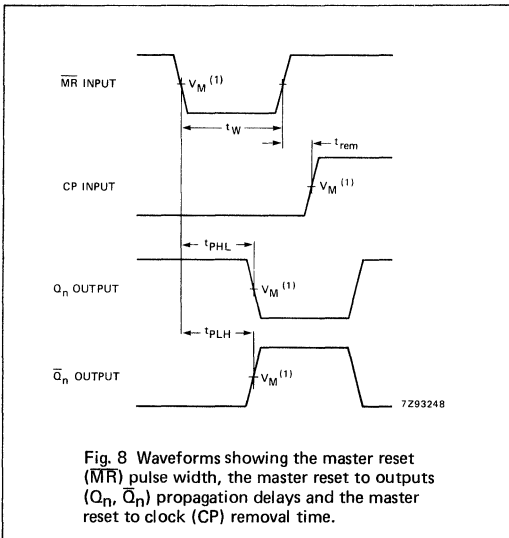


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to outputs (Q<sub>n</sub>, Q<sub>n</sub>) propagation delays and the master reset to clock (CP) removal time.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

4-BIT ARITHMETIC LOGIC UNIT

FEATURES

- Full carry look-ahead for high-speed arithmetic operation on long words
- Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others
- Provides all 16 logic operations of two variables:  
EXCLUSIVE-OR, compare, AND, NAND, NOR, OR plus 10 other logic operations
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT181 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT181 are 4-bit high-speed parallel Arithmetic Logic Units (ALU). Controlled by the four function select inputs (S<sub>0</sub> to S<sub>3</sub>) and the mode control inputs (M), they can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands (see function table).

When the mode control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When M is LOW, the carries are enabled and the "181" performs arithmetic operations on the two 4-bit words. The "181" incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C<sub>n+4</sub> output, or for carry look-ahead between packages using the carry (continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{A}_n$ or $\bar{B}_n$ to A=B	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	34	36	ns
	C <sub>n</sub> to C <sub>n+4</sub>		14	16	ns
	$\bar{A}_n$ or $\bar{B}_n$ to G, P, F, C <sub>n+4</sub>		17	19	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT181P: 24-lead DIL; plastic (SOT-101A).  
PC74HC/HCT181T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\bar{B}_0$ to $\bar{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\bar{A}_0$ to $\bar{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S <sub>0</sub> to S <sub>3</sub>	select inputs
7	C <sub>n</sub>	carry input
8	M	mode control input
9, 10, 11, 13	$\bar{F}_0$ to $\bar{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\bar{P}$	carry propagate output (active LOW)
16	C <sub>n+4</sub>	carry output
17	$\bar{G}$	carry generate output (active LOW)
24	V <sub>CC</sub>	positive supply voltage

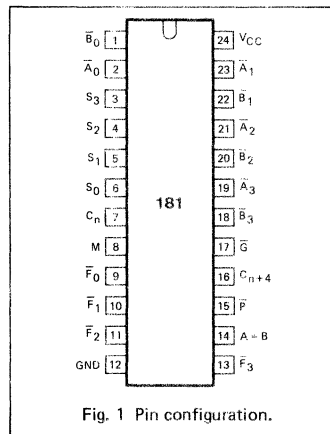


Fig. 1 Pin configuration.

**GENERAL DESCRIPTION (Cont'd)**

propagation ( $\bar{P}$ ) and carry generate ( $\bar{G}$ ) signals.  $\bar{P}$  and  $\bar{G}$  are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the carry output ( $C_{n+4}$ ) signal to the carry input ( $C_n$ ) of the next unit.

For high-speed operation the device is used in conjunction with the "182" carry look-ahead circuit. One carry look-ahead package is required for each group of four "181" devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The comparator output ( $A=B$ ) of the device goes HIGH when all four function outputs ( $\bar{F}_0$  to  $\bar{F}_3$ ) are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode.  $A=B$  is an open drain output and can be wired-AND with other  $A=B$  outputs to give a comparison for more than 4 bits. The  $A=B$  signal can also be used with the  $C_{n+4}$  signal to indicate  $A > B$  and  $A < B$ .

The function table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHLH generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no under-flow and no carry is generated when there is underflow.

As indicated, the "181" can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs.

For either case the table lists the operations that are performed to the operands.

**FUNCTION TABLES**

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	LOGIC (M=H)	ARITHMETIC** (M=L; C <sub>n</sub> =H)
L	L	L	L	$\bar{A}$	A
L	L	L	H	$\bar{A} + \bar{B}$	A + B
L	L	H	L	$\bar{A}B$	A + $\bar{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$
L	H	L	H	$\bar{B}$	(A + B) plus $\bar{A}\bar{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$\bar{A}B$	$\bar{A}B$ minus 1
H	L	L	L	$\bar{A} + B$	A plus AB
H	L	L	H	$\bar{A} \oplus \bar{B}$	A plus B
H	L	H	L	B	(A + $\bar{B}$ ) plus AB
H	L	H	H	$\bar{A}B$	$\bar{A}B$ minus 1
H	H	L	L	logical 1	A plus A*
H	H	L	H	$A + \bar{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\bar{B}$ ) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	LOGIC (M=H)	ARITHMETIC** (M=L; C <sub>n</sub> =L)
L	L	L	L	$\bar{A}$	A minus 1
L	L	L	H	$\bar{A}\bar{B}$	$\bar{A}B$ minus 1
L	L	H	L	$\bar{A} + B$	$\bar{A}\bar{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + $\bar{B}$ )
L	H	L	H	$\bar{B}$	$\bar{A}B$ plus (A + $\bar{B}$ )
L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1
L	H	H	H	A + $\bar{B}$	A + $\bar{B}$
H	L	L	L	$\bar{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	logical 0	A plus A*
H	H	L	H	$\bar{A}B$	$\bar{A}B$ plus A
H	H	H	L	$\bar{A}B$	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A

**Notes to function tables**

- \* Each bit is shifted to the next more significant position.
- \*\* Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level  
L = LOW voltage level

DEVELOPMENT DATA

LOOK-AHEAD CARRY GENERATOR

FEATURES

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high-speed arithmetic operation over long word length
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ( $\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$ ) and carry generate ( $\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$ ) signals and an active HIGH carry input ( $C_n$ ). The devices provide anticipated active HIGH carries ( $C_{n+x}, C_{n+y}, C_{n+z}$ ) across four groups of binary adders.

The "182" also has active LOW carry propagate ( $\overline{P}$ ) and carry generate ( $\overline{G}$ ) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G}_3 + P_3 \overline{G}_2 + P_3 P_2 \overline{G}_1 + P_3 P_2 P_1 \overline{G}_0$$

$$\overline{P} = \overline{P}_3 P_2 P_1 P_0$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> to P C <sub>n</sub> to any output P <sub>n</sub> or G <sub>n</sub> to any output	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	14	ns
			17	21	ns
			14	17	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	50	50	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

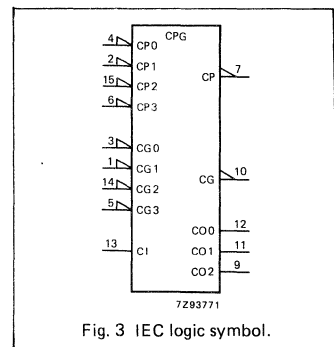
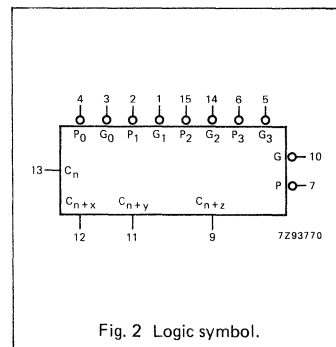
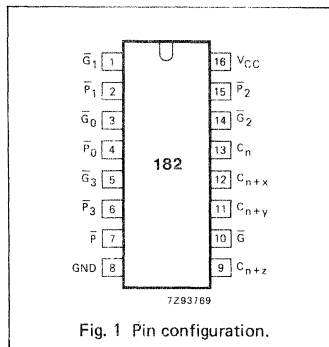
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT182P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT182T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C <sub>n+z</sub>	function output
10	$\overline{G}$	carry generate output (active LOW)
11	C <sub>n+y</sub>	function output
12	C <sub>n+x</sub>	function output
13	C <sub>n</sub>	carry input (active HIGH)
16	V <sub>CC</sub>	positive supply voltage



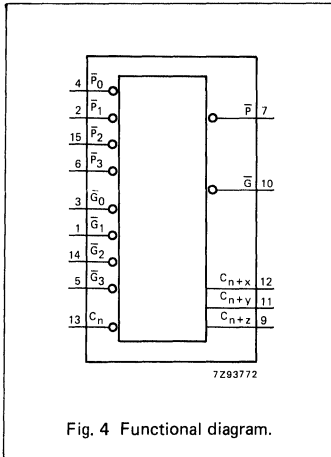


Fig. 4 Functional diagram.

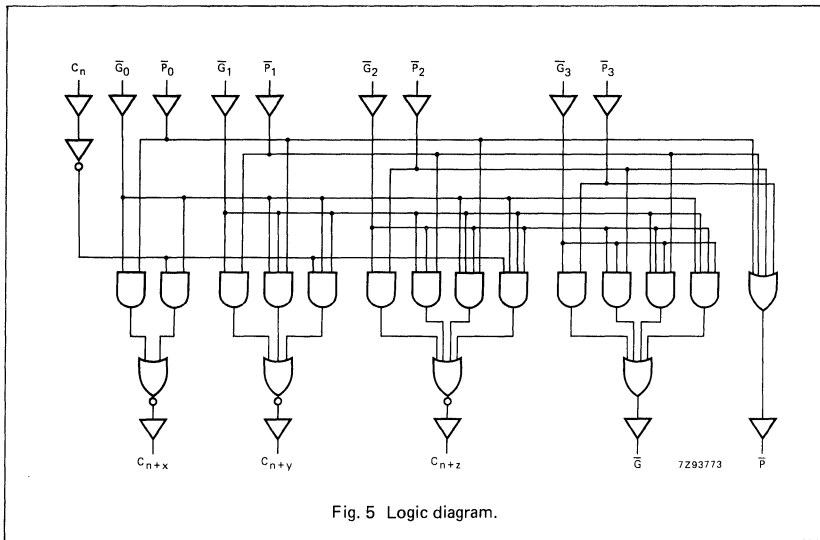


Fig. 5 Logic diagram.



FUNCTION TABLE

INPUTS									OUTPUTS				
C <sub>n</sub>	$\bar{G}_0$	$\bar{P}_0$	$\bar{G}_1$	$\bar{P}_1$	$\bar{G}_2$	$\bar{P}_2$	$\bar{G}_3$	$\bar{P}_3$	C <sub>n+x</sub>	C <sub>n+y</sub>	C <sub>n+z</sub>	$\bar{G}$	$\bar{P}$
X L X H	H H L X	H X X L							L L H H				
X X L X X H	X H H X L X	X H X X L X	H H L X X	H X X L L						L L L H H H			
X X X L	X X H H	X X H X	X H H H	X X X X	H H H H	H X X X					L L L L		
X X X H	X X L X	X X X L	X L X X	X X L L	L X X X	X L L L					H H H H		
	X X X H		X X H H	X X H X	X H H H	X H X X	H H H H	H X X X				H H H H	
	X X X L		X X L X	X X X L	X L X X	X X L L	L X X X	X L L L				L L L L	
		H X X L		X H X L		X X H X		X X X H					H H H L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> to P̄		30 14 11	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>n</sub> to any output		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P̄ <sub>n</sub> or Ḡ <sub>n</sub> to Ḡ		47 17 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P̄ <sub>n</sub> or Ḡ <sub>n</sub> to C <sub>n+n</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>T LH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

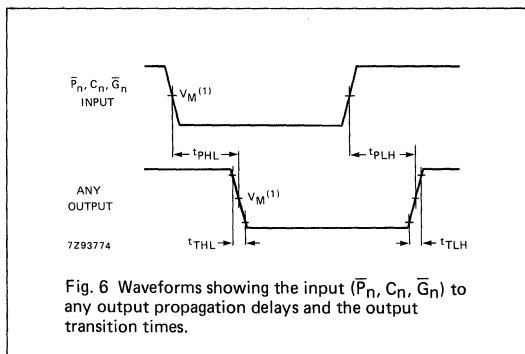
INPUT	UNIT LOAD COEFFICIENT
$\bar{G}_0, \bar{G}_1, \bar{P}_0, \bar{P}_1, \bar{P}_2$	1.50
$\bar{G}_3$	0.30
$\bar{G}_2, \bar{P}_3, C_n$	1.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> to P̄		17	31		39		47	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>n</sub> to any output		25	45		56		68	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> or G <sub>n</sub> to G		20	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> or G <sub>n</sub> to C <sub>n</sub> +n		19	34		43		51	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

**AC WAVEFORMS**



**Note to AC waveforms**

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

## PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

## FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- ICC category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT190 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT190 are asynchronously presettable up/down BCD decade counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs ( $D_0$  to  $D_3$ ) is loaded into the counter and appears on the outputs when the parallel load (PL) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (CE) input. When CE is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ( $\bar{U}/D$ ) input signal determines the direction of counting as indicated in the function table. The CE input may go LOW when the clock is in either state, however, the LOW-to-HIGH CE transition must occur only when the clock is HIGH. Also, the  $\bar{U}/D$  input should be changed only when either CE or CP is HIGH.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	22	24	ns
$f_{max}$	maximum clock frequency		28	30	MHz
$C_I$	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	36	38	pF

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

## Notes

1. CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF

$f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

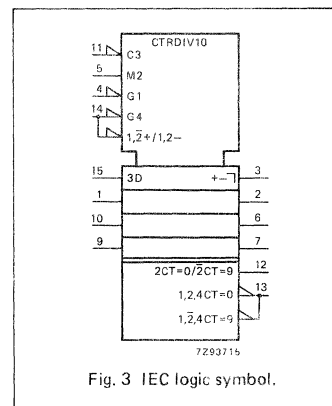
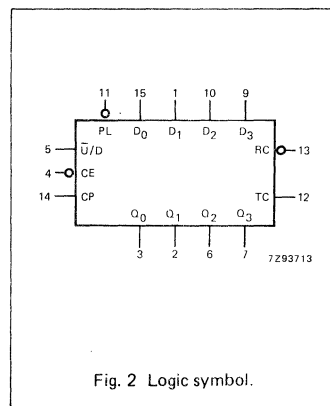
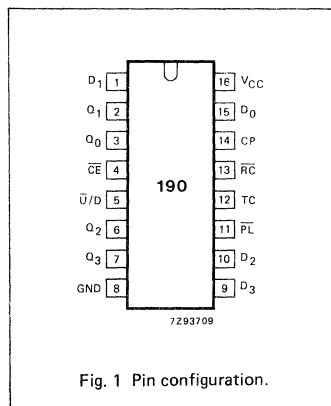
## ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT190P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT190T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	$Q_0$ to $Q_3$	flip-flop outputs
4	CE	count enable input (active LOW)
5	$\bar{U}/D$	up/down input
8	GND	ground (0 V)
11	PL	parallel load input (active LOW)
12	TC	terminal count output
13	$\bar{R}C$	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	$D_0$ to $D_3$	data inputs
16	$V_{CC}$	positive supply voltage



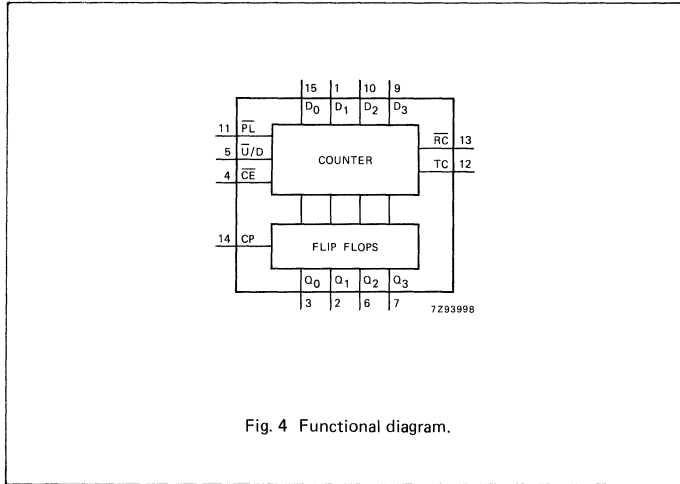


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ( $\overline{RC}$ ). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until  $\overline{U/D}$  is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the  $\overline{RC}$  output. When TC is HIGH and  $\overline{CE}$  is LOW, the  $\overline{RC}$  output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig. 5, each  $\overline{RC}$  output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on  $\overline{CE}$  inhibits the  $\overline{RC}$  output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The  $\overline{RC}$  outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the  $\overline{RC}$  output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the  $\overline{CE}$  input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own  $\overline{CE}$  signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

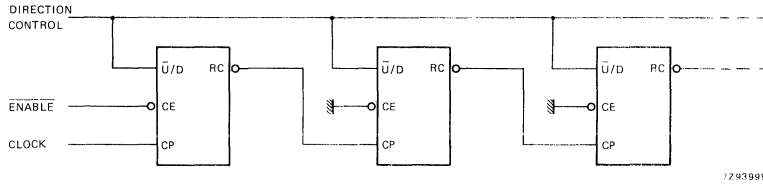
**FUNCTION TABLE**

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U/D}$	$\overline{CE}$	CP	$D_n$	
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

**TC AND RC FUNCTION TABLE**

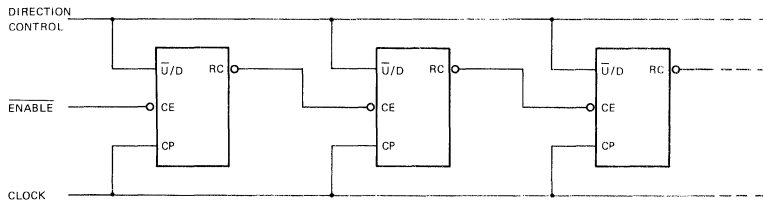
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	$\overline{CE}$	CP	$Q_0$	$Q_1$	$Q_2$	$Q_3$	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌊	H	X	X	H	⌊	⌊
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	L	H
H	L	⌊	L	L	L	L	⌊	⌊

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition
- ⌊ = one LOW level pulse
- ⌊ = TC goes LOW on a LOW-to-HIGH CP transition



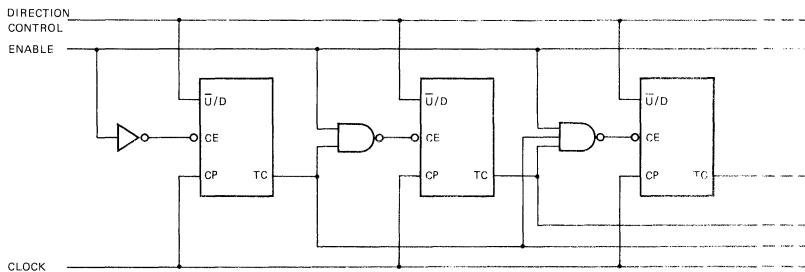
7293995

Fig. 5 N-stage ripple counter using ripple clock.



7293996

Fig. 6 Synchronous n-stage counter using ripple carry/borrow.



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Fig. 7 Synchronous n-stage counter with parallel gated carry/borrow.

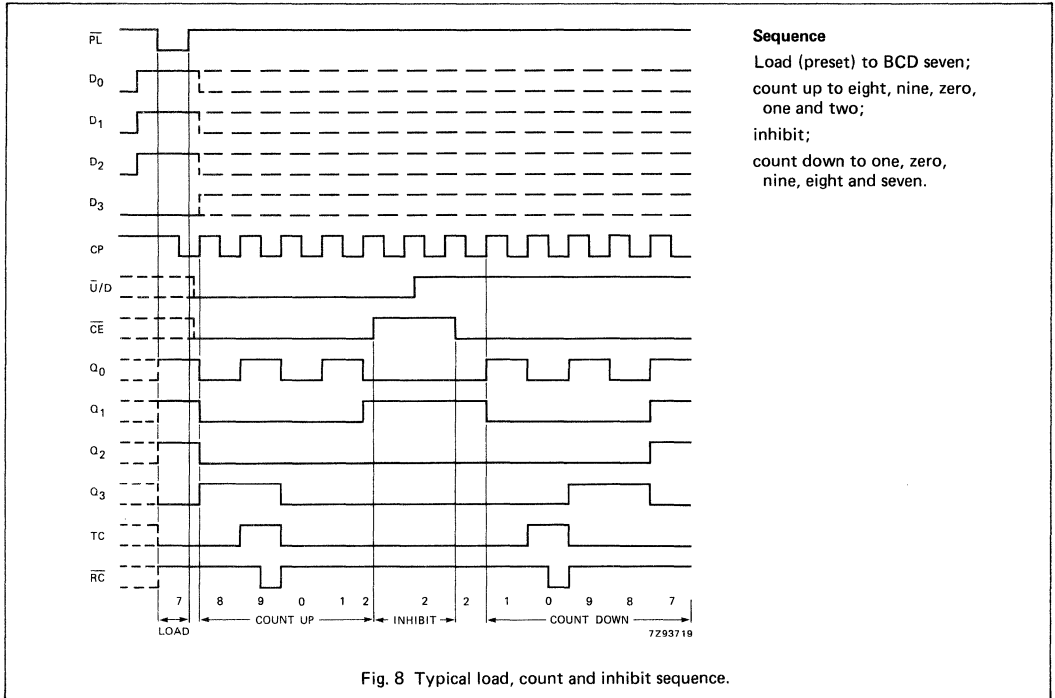


Fig. 8 Typical load, count and inhibit sequence.

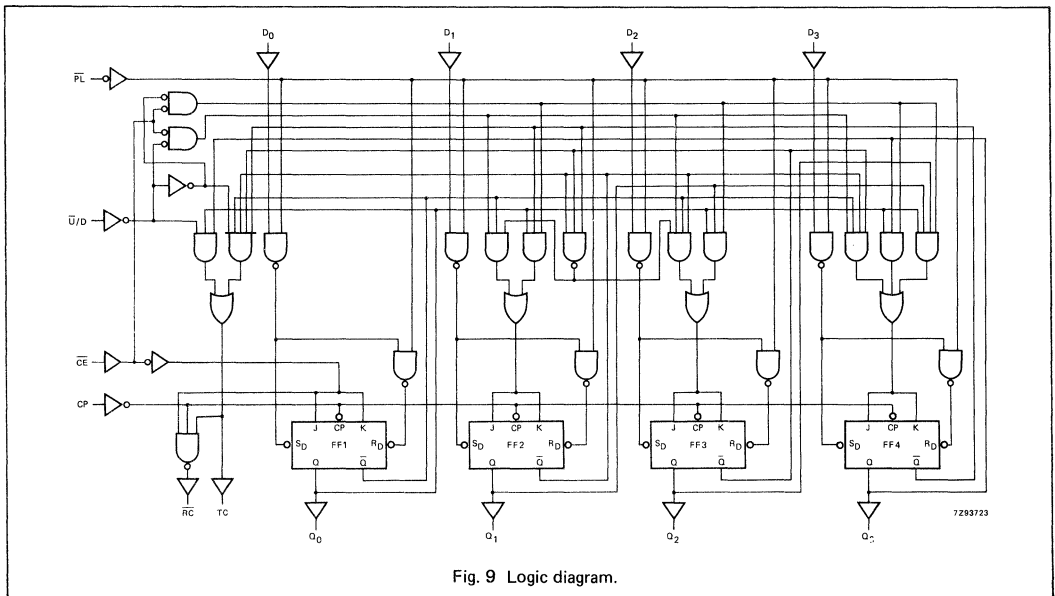


Fig. 9 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		83 30 24	255 51 43		320 64 54		395 77 65	ns	2.0 4.5 6.0	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to RC		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CE to RC		33 12 10	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 12
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>n</sub>		63 23 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay U/D to TC		44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay U/D to RC		50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15
t <sub>w</sub>	clock pulse width HIGH or LOW	155 31 26	28 10 8		195 39 33		235 47 40		ns	2.0 4.5 6.0	Fig. 10
t <sub>w</sub>	count enable pulse width LOW	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 11
t <sub>w</sub>	parallel load pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 15
t <sub>rem</sub>	removal time PL to CP	35 7 6	8 3 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 15



AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.			
t <sub>su</sub>	set-up time U/D to CP	205 41 35	61 22 18		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 17
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{PL}$	100 20 17	19 7 6		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 16
t <sub>su</sub>	set-up time $\overline{CE}$ to CP	140 28 24	39 14 11		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 17
t <sub>h</sub>	hold time U/D to CP	0 0 0	-44 -16 -13		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 17
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{PL}$	0 0 0	-14 -5 -4		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 16
t <sub>h</sub>	hold time $\overline{CE}$ to CP	0 0 0	-19 -7 -6		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 17
f <sub>max</sub>	maximum clock pulse frequency	3.0 15 18	8.3 25 30		2.4 12 14		2.0 10 12	MHz	2.0 4.5 6.0	Fig. 10

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications."

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$D_n$	0.5
CP	0.65
$\overline{U/D}$	1.15
$\overline{CE}, \overline{PL}$	1.5

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$		28	48		60		72	ns	4.5	Fig. 10
$t_{PHL}/t_{PLH}$	propagation delay CP to TC		34	58		73		87	ns	4.5	Fig. 10
$t_{PHL}/t_{PLH}$	propagation delay CP to $\overline{RC}$		20	35		44		53	ns	4.5	Fig. 11
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CE}$ to $\overline{RC}$		18	33		41		50	ns	4.5	Fig. 11
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$		24	44		55		66	ns	4.5	Fig. 12
$t_{PHL}/t_{PLH}$	propagation delay $\overline{PL}$ to $Q_n$		29	49		61		74	ns	4.5	Fig. 13
$t_{PHL}/t_{PLH}$	propagation delay $\overline{U/D}$ to TC		24	45		56		68	ns	4.5	Fig. 14
$t_{PHL}/t_{PLH}$	propagation delay $\overline{U/D}$ to $\overline{RC}$		26	45		56		68	ns	4.5	Fig. 14
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 15
$t_W$	clock pulse width HIGH or LOW	31	10		39			47	ns	4.5	Fig. 10
$t_W$	count enable pulse width LOW	25			31			38	ns	4.5	Fig. 11
$t_W$	parallel load pulse width LOW	22	12		28			33	ns	4.5	Fig. 15
$t_{rem}$	removal time $\overline{PL}$ to CP	7	1		9			11	ns	4.5	Fig. 15
$t_{su}$	set-up time $\overline{U/D}$ to CP	42	25		53			63	ns	4.5	Fig. 17
$t_{su}$	set-up time $D_n$ to $\overline{PL}$	20	10		25			30	ns	4.5	Fig. 16
$t_{su}$	set-up time $\overline{CE}$ to CP	31	18		39			47	ns	4.5	Fig. 17
$t_h$	hold time $\overline{U/D}$ to CP	0	-18		0			0	ns	4.5	Fig. 17
$t_h$	hold time $D_n$ to $\overline{PL}$	0	-6		0			0	ns	4.5	Fig. 16
$t_h$	hold time $\overline{CE}$ to CP	0	-10		0			0	ns	4.5	Fig. 17
$f_{max}$	maximum clock pulse frequency	16	27		13			11	MHz	4.5	Fig. 10

AC WAVEFORMS

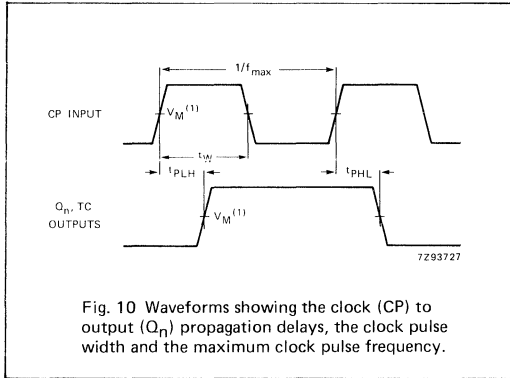


Fig. 10 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width and the maximum clock pulse frequency.

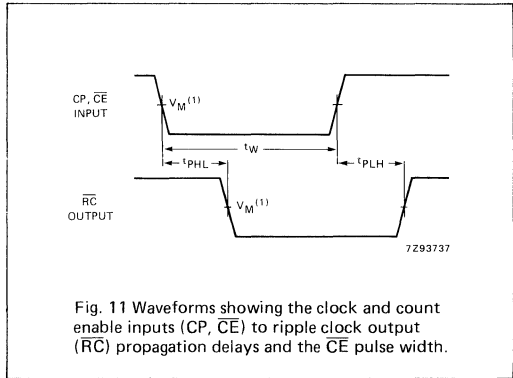


Fig. 11 Waveforms showing the clock and count enable inputs (CP,  $\overline{CE}$ ) to ripple clock output ( $\overline{RC}$ ) propagation delays and the  $\overline{CE}$  pulse width.

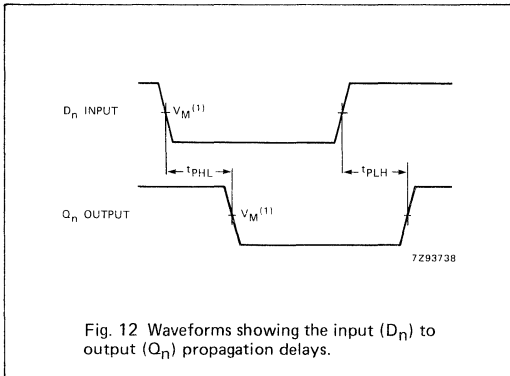


Fig. 12 Waveforms showing the input ( $D_n$ ) to output ( $Q_n$ ) propagation delays.

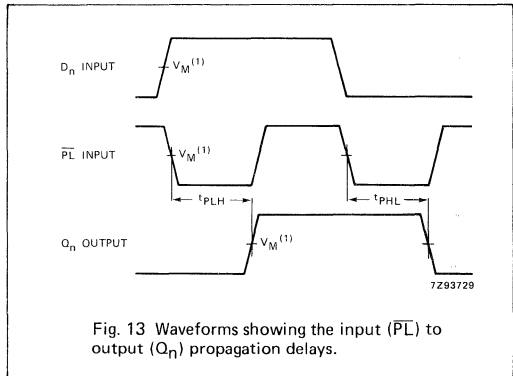


Fig. 13 Waveforms showing the input ( $\overline{PL}$ ) to output ( $Q_n$ ) propagation delays.

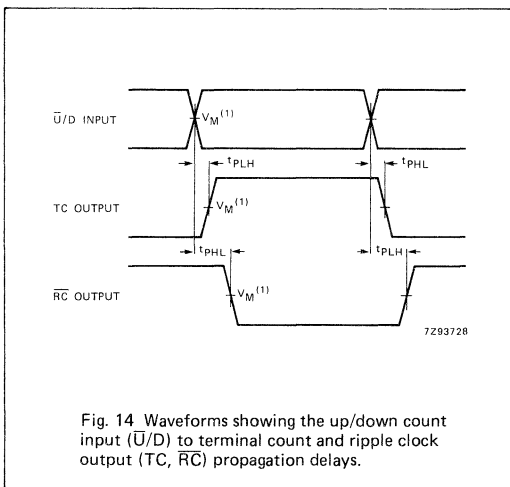


Fig. 14 Waveforms showing the up/down count input ( $\overline{U/D}$ ) to terminal count and ripple clock output (TC,  $\overline{RC}$ ) propagation delays.

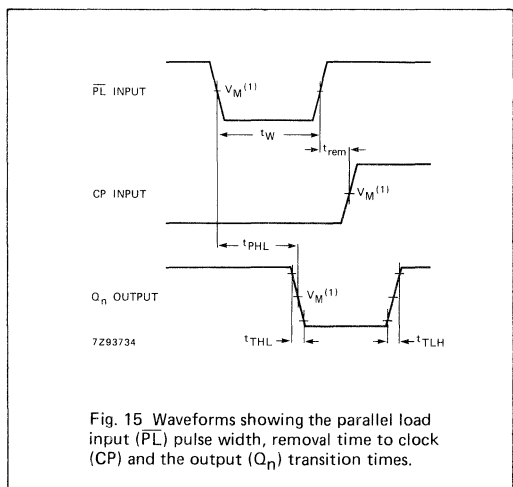


Fig. 15 Waveforms showing the parallel load input ( $\overline{PL}$ ) pulse width, removal time to clock (CP) and the output ( $Q_n$ ) transition times.

AC WAVEFORMS (Continued)

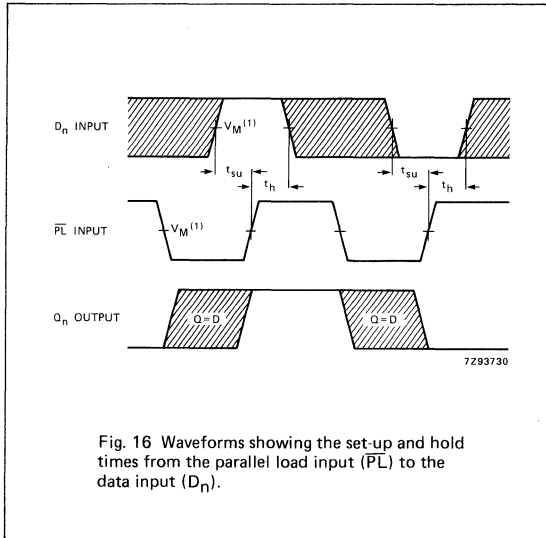


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input ( $\overline{PL}$ ) to the data input ( $D_n$ ).

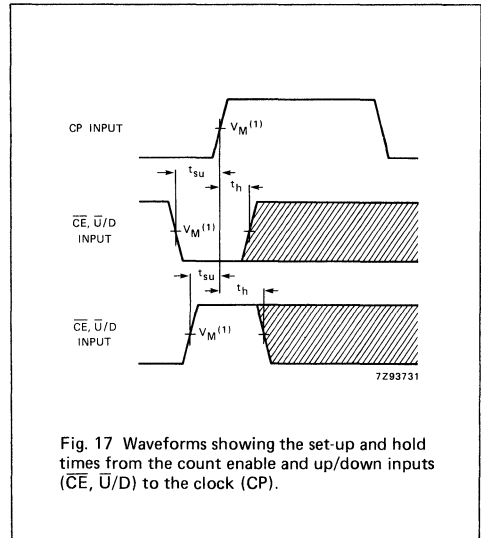


Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ( $\overline{CE}, \overline{U/D}$ ) to the clock (CP).

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Figs 16 and 17

The shaded areas indicate when the input is permitted to change for predictable output performance.

PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTER

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D<sub>0</sub> to D<sub>3</sub>) is loaded into the counter and appears on the outputs when the parallel load (PL) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (CE) input. When CE is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down (U/D) input signal determines the direction of counting as indicated in the function table. The CE input may go LOW when the clock is in either state, however, the LOW-to-HIGH CE transition must occur only when the clock is HIGH. Also, the U/D input should be changed only when either CE or CP is HIGH.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	22	22	ns
f <sub>max</sub>	maximum clock frequency		36	36	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	31	33	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

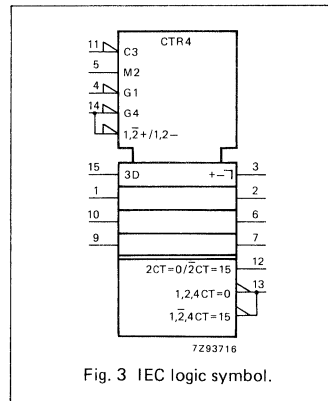
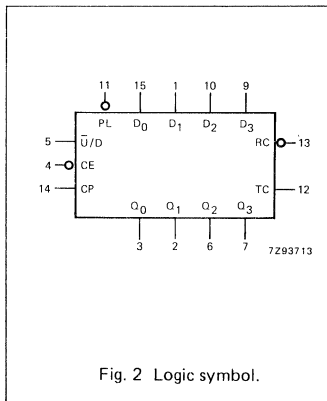
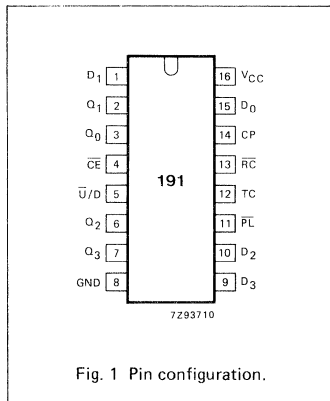
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT191P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT191T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
4	CE	count enable input (active LOW)
5	U/D	up/down input
8	GND	ground (0 V)
11	PL	parallel load input (active LOW)
12	TC	terminal count output
13	RC	ripple clock output (active LOW)
14	CP	clock input (LOW-to-HIGH, edge triggered)
15, 1, 10, 9	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage



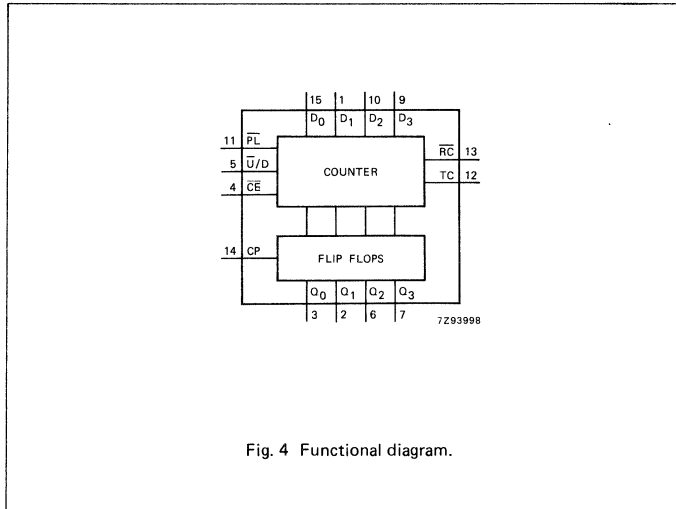


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ( $\overline{RC}$ ). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the  $\overline{RC}$  output. When TC is HIGH and  $\overline{CE}$  is LOW, the  $\overline{RC}$  output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig. 5, each  $\overline{RC}$  output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on  $\overline{CE}$  inhibits the  $\overline{RC}$  output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The  $\overline{RC}$  outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the  $\overline{RC}$  output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the  $\overline{CE}$  input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own  $\overline{CE}$  signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

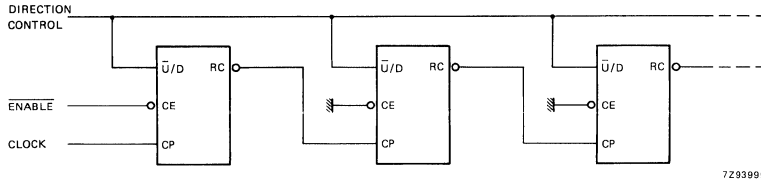
**FUNCTION TABLE**

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U/D}$	$\overline{CE}$	CP	$D_n$	$Q_n$
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	I	↑	X	count up
count down	H	H	I	↑	X	count down
hold (do nothing)	H	X	H	X	X	no change

**TC AND RC FUNCTION TABLE**

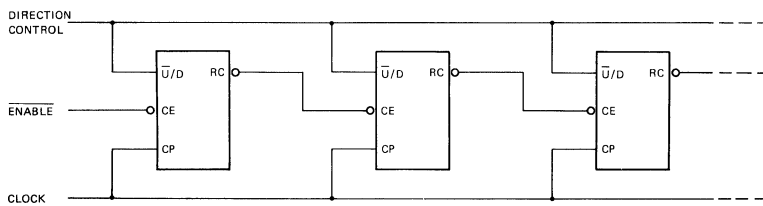
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	$\overline{CE}$	CP	$Q_0$	$Q_1$	$Q_2$	$Q_3$	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⌋	H	H	H	H	⌋	⌋
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌋	L	L	L	L	⌋	⌋

- H = HIGH voltage level
- L = LOW voltage level
- I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition
- ⌋ = one LOW level pulse
- ⌋ = TC goes LOW on a LOW-to-HIGH CP transition



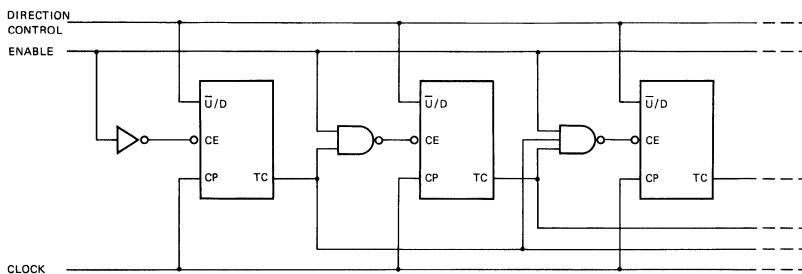
7293995

Fig. 5 N-stage ripple counter using ripple clock.



7293996

Fig. 6 Synchronous n-stage counter using ripple carry/borrow.



7293997

Fig. 7 Synchronous n-stage counter with parallel gated carry/borrow.



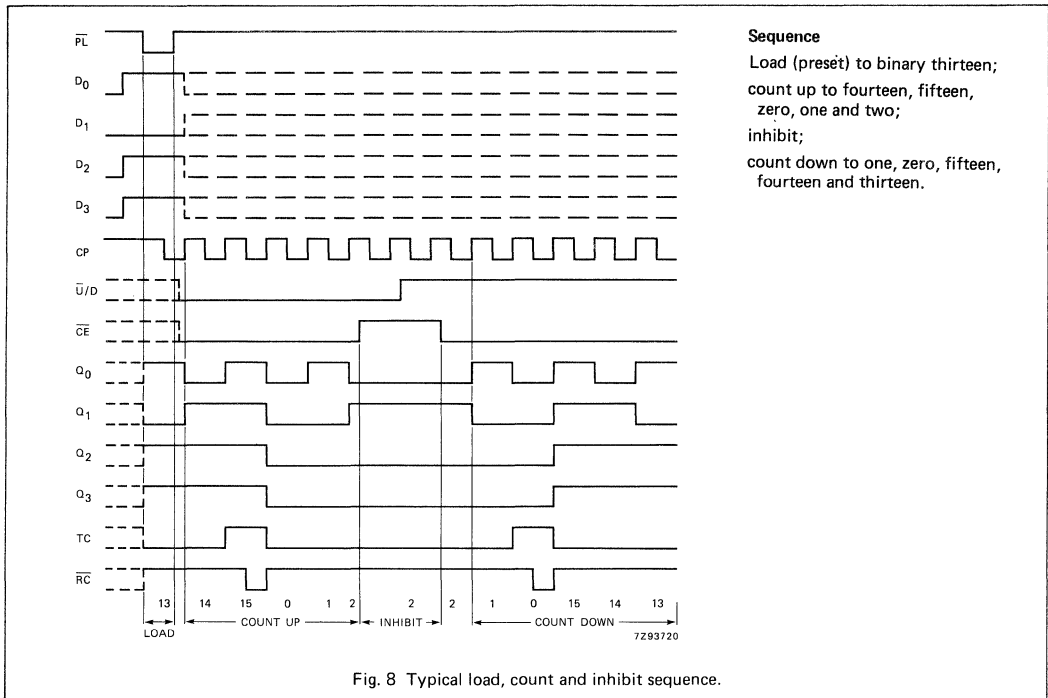


Fig. 8 Typical load, count and inhibit sequence.

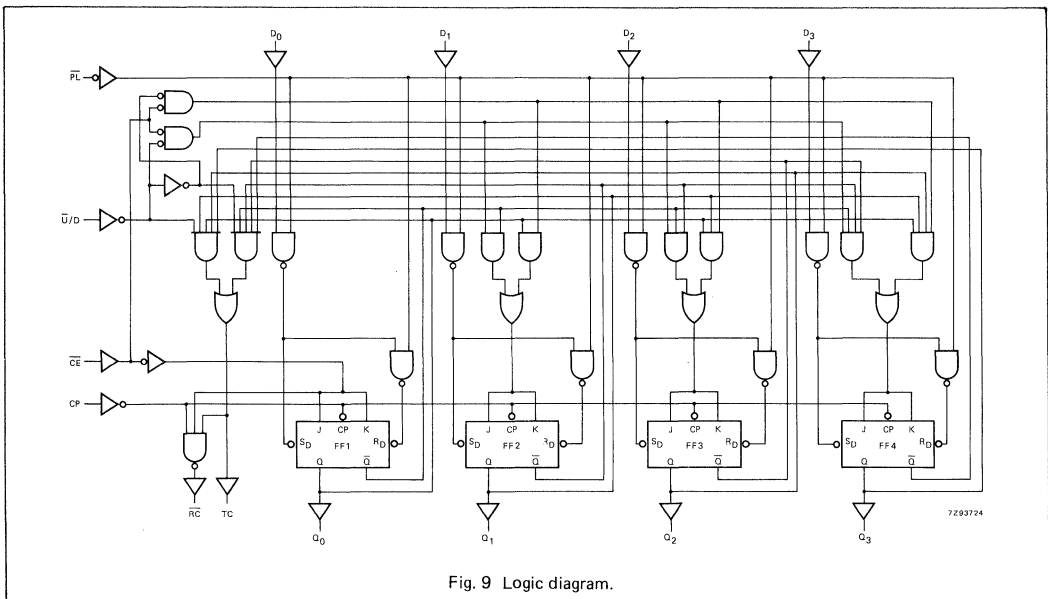


Fig. 9 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications."

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.			
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay CP to Q <sub>n</sub>	72 26 21	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay CP to TC	83 30 24	255 51 43		320 64 54		395 77 65	ns	2.0 4.5 6.0	Fig. 10
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay CP to $\bar{R}\bar{C}$	47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 11
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay CE to $\bar{R}\bar{C}$	33 12 10	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 11
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	47 17 14	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 12
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay $\bar{P}\bar{L}$ to Q <sub>n</sub>	61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay $\bar{U}/\bar{D}$ to TC	44 16 13	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 14
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay $\bar{U}/\bar{D}$ to $\bar{R}\bar{C}$	50 18 14	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 14
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 15
t <sub>w</sub>	clock pulse width HIGH or LOW	130 26 22	28 10 8		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 10
t <sub>w</sub>	count enable pulse width LOW	125 25 21			155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 11
t <sub>w</sub>	parallel load pulse width LOW	100 20 17	22 8 6		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 15
t <sub>rem</sub>	removal time PL to CP	35 7 6	8 3 2		45 9 8		55 11 9	ns	2.0 4.5 6.0	Fig. 15

AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.			
t <sub>su</sub>	set-up time U/D to CP	205 41 35	50 18 14		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig. 17
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{PL}$	100 20 17	19 7 6		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 16
t <sub>su</sub>	set-up time $\overline{CE}$ to CP	140 28 24	44 16 13		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 17
t <sub>h</sub>	hold time U/D to CP	0 0 0	-39 -14 -11		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 17
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{PL}$	0 0 0	-11 -4 -3		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 16
t <sub>h</sub>	hold time $\overline{CE}$ to CP	0 0 0	-28 -10 -8		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig. 17
f <sub>max</sub>	maximum clock pulse frequency	4.0 20 24	11 33 39		3.2 16 19		2.6 13 15	MHz	2.0 4.5 6.0	Fig. 10

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$D_n$	0.5
$CP$	0.65
$\bar{U}/D$	1.15
$\bar{CE}, \bar{PL}$	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		26	48		60		72	ns	4.5	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		32	51		64		77	ns	4.5	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{RC}$		19	35		44		53	ns	4.5	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CE to $\overline{RC}$		19	33		41		50	ns	4.5	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		20	44		55		66	ns	4.5	Fig. 12
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{PL}$ to Q <sub>n</sub>		27	46		58		69	ns	4.5	Fig. 13
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{U/D}$ to TC		23	45		56		68	ns	4.5	Fig. 14
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{U/D}$ to $\overline{RC}$		24	45		56		68	ns	4.5	Fig. 14
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 15
t <sub>W</sub>	clock pulse width HIGH or LOW	26	9		33		39		ns	4.5	Fig. 10
t <sub>W</sub>	count enable pulse width LOW	25			31		38		ns	4.5	Fig. 11
t <sub>W</sub>	parallel load pulse width LOW	22	11		28		33		ns	4.5	Fig. 15
t <sub>rem</sub>	removal time $\overline{PL}$ to CP	7	1		9		11		ns	4.5	Fig. 15
t <sub>su</sub>	set-up time $\overline{U/D}$ to CP	41	20		51		62		ns	4.5	Fig. 17
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{PL}$	20	9		25		30		ns	4.5	Fig. 16
t <sub>su</sub>	set-up time CE to CP	31	18		39		47		ns	4.5	Fig. 17
t <sub>h</sub>	hold time $\overline{U/D}$ to CP	0	-18		0		0		ns	4.5	Fig. 17
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{PL}$	0	-5		0		0		ns	4.5	Fig. 16
t <sub>h</sub>	hold time CE to CP	0	-10		0		0		ns	4.5	Fig. 17
f <sub>max</sub>	maximum clock pulse frequency	20	33		16		13		MHz	4.5	Fig. 10

AC WAVEFORMS

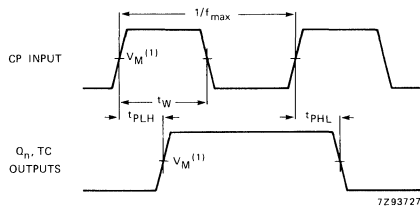


Fig. 10 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width and the maximum clock pulse frequency.

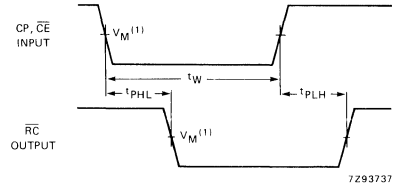


Fig. 11 Waveforms showing the clock and count enable inputs (CP,  $\overline{CE}$ ) to ripple clock output ( $\overline{RC}$ ) propagation delays and the CE pulse width.

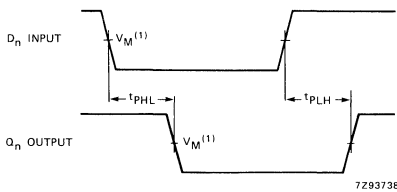


Fig. 12 Waveforms showing the input ( $D_n$ ) to output ( $Q_n$ ) propagation delays.

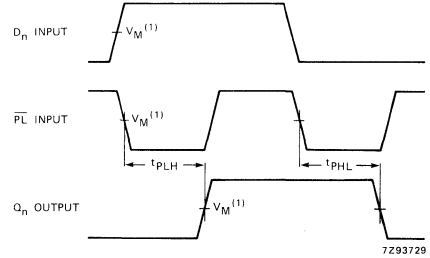


Fig. 13 Waveforms showing the input ( $\overline{PL}$ ) to output ( $Q_n$ ) propagation delays.

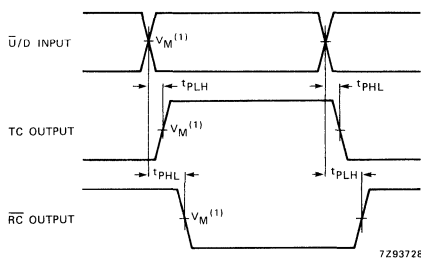


Fig. 14 Waveforms showing the up/down count input ( $\overline{U/D}$ ) to terminal count and ripple clock output (TC,  $\overline{RC}$ ) propagation delays.

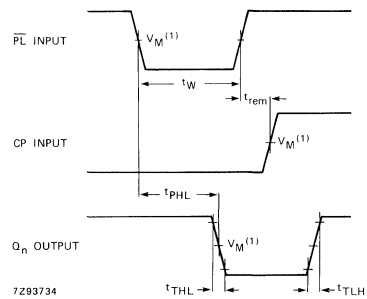


Fig. 15 Waveforms showing the parallel load input ( $\overline{PL}$ ) pulse width, removal time to clock (CP) and the output ( $Q_n$ ) transition times.

AC WAVEFORMS (Continued)

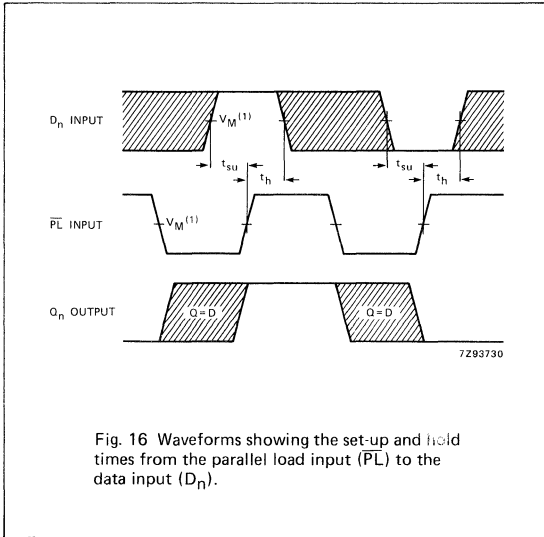


Fig. 16 Waveforms showing the set-up and hold times from the parallel load input ( $\overline{PL}$ ) to the data input ( $D_n$ ).

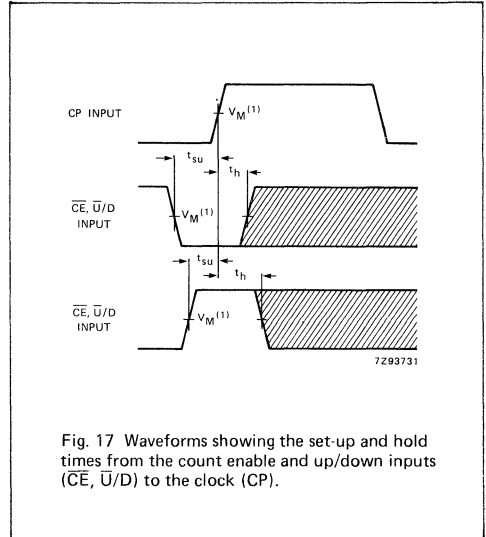


Fig. 17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ( $\overline{CE}, \overline{U/D}$ ) to the clock (CP).

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Figs 16 and 17

The shaded areas indicate when the input is permitted to change for predictable output performance.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT192

MSI

## PRESETTABLE SYNCHRONOUS BCD DECADE UP/DOWN COUNTER

### FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT192 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT192 are synchronous BCD up/down counters.

Separate up/down clocks, CP<sub>U</sub> and CP<sub>D</sub> respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP<sub>U</sub> clock is pulsed while CP<sub>D</sub> is held HIGH, the device will count up. If the CP<sub>D</sub> clock is pulsed while CP<sub>U</sub> is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (PL).

The "192" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP<sub>D</sub> input will decrease the count by one, while a similar transition on the CP<sub>U</sub> input will advance the count by one.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> , CP <sub>U</sub> to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	19	19	ns
f <sub>max</sub>	maximum clock frequency		40	40	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CP <sub>D</sub>	power dissipation capacitance per package	notes 1 and 2	42	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CP<sub>D</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CP_D \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT192P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT192T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
4	CP <sub>D</sub>	count down clock input*
5	CP <sub>U</sub>	count up clock input*
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage

\* LOW-to-HIGH, edge triggered

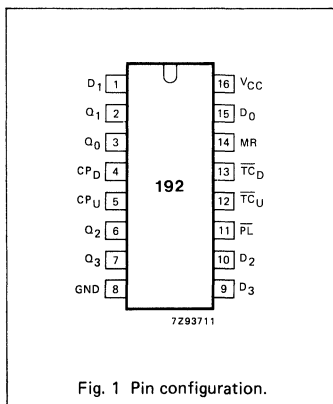


Fig. 1 Pin configuration.

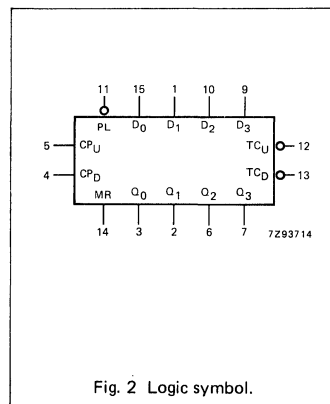


Fig. 2 Logic symbol.

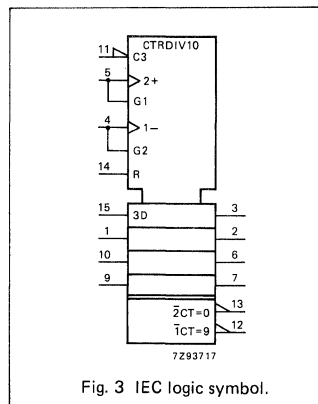


Fig. 3 IEC logic symbol.



**GENERAL DESCRIPTION (Cont'd)**

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ( $\overline{TC}_U$ ) and terminal count down ( $\overline{TC}_D$ ) outputs are normally HIGH. When the circuit has reached the maximum count state of 9, the next HIGH-to-LOW transition of  $CP_U$  will cause  $\overline{TC}_U$  to go LOW.  $\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again, duplicating the count up clock.

Likewise, the  $\overline{TC}_D$  output will go LOW when the circuit is in the zero state and the  $CP_D$  goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a

multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs ( $D_0$  to  $D_3$ ) is loaded into the counter and appears on the outputs ( $Q_0$  to  $Q_3$ ) regardless of the conditions of the clock inputs when the parallel load ( $\overline{PL}$ ) input is LOW. A HIGH level on the master reset ( $MR$ ) input will disable the parallel load gates, override both clock inputs and set all outputs ( $Q_0$  to  $Q_3$ ) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

**FUNCTION TABLE**

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	$CP_U$	$CP_D$	$D_0$	$D_1$	$D_2$	$D_3$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H H	X X	X X	L H	X X	X X	X X	X X	L L	L L	L L	L L	H H	L H
parallel load	L L L	L L L	X X H	L H X	L L H	L L X	L L X	L L H	L L L	L L L	L L L	L L L	H H L	L H H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition

\*  $\overline{TC}_U = CP_U$  at terminal count up (HLLH)  
 \*\*  $\overline{TC}_D = CP_D$  at terminal count down (LLLL)

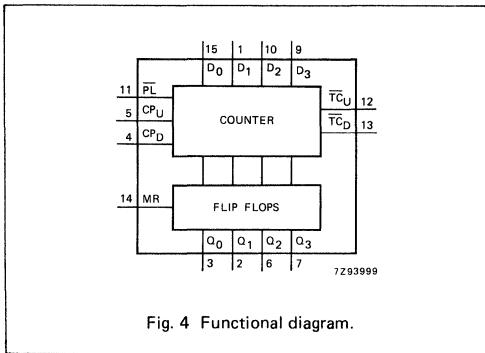
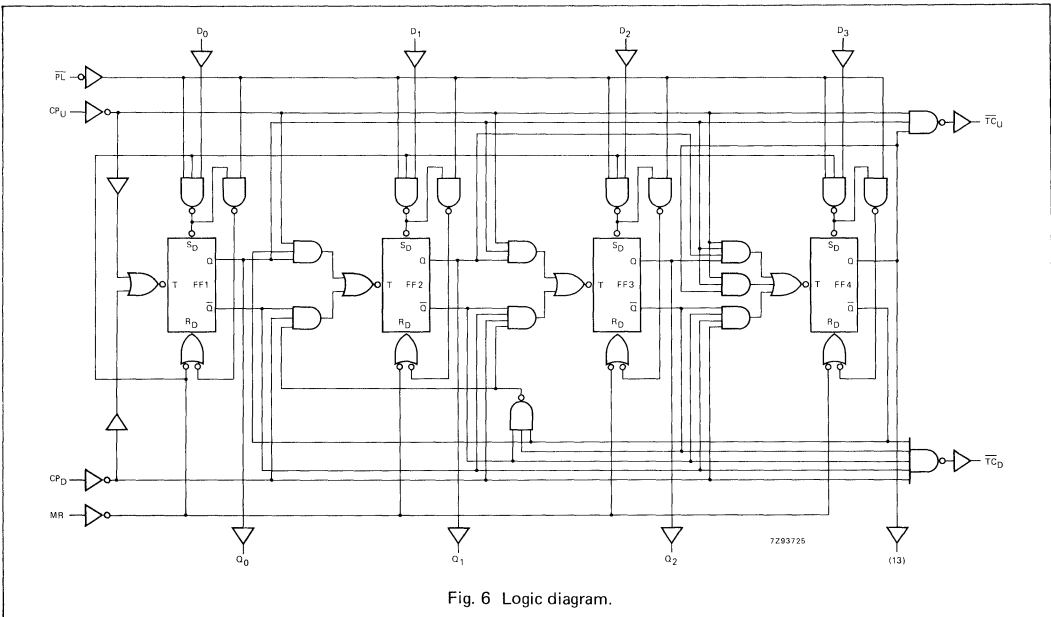
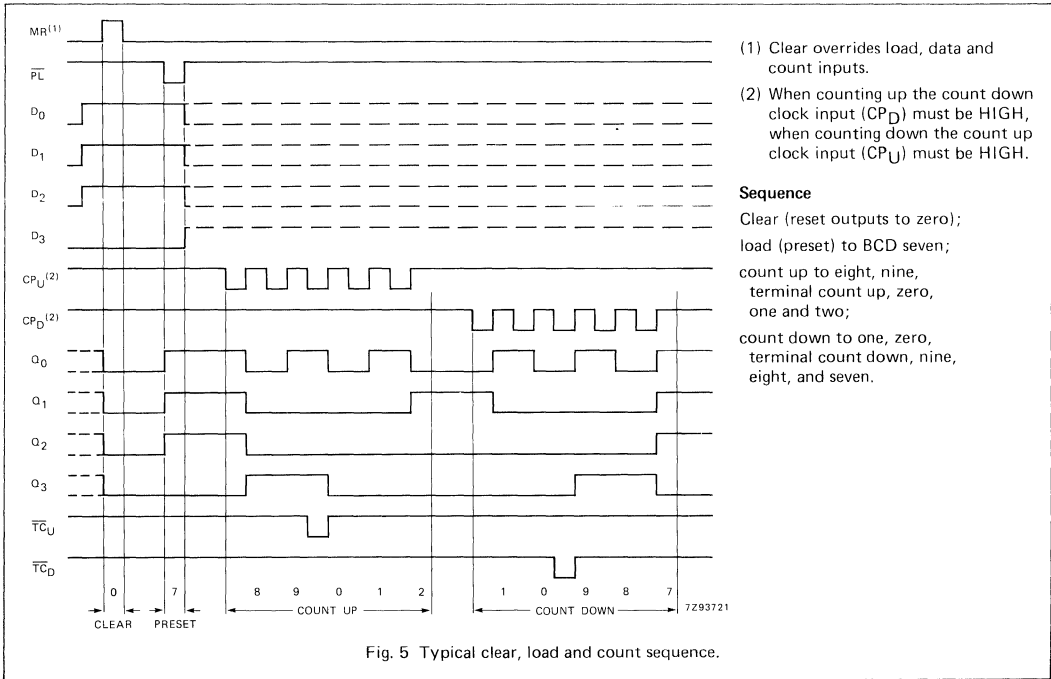


Fig. 4 Functional diagram.



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications."

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> , CP <sub>D</sub> to Q <sub>n</sub>			215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> to TC <sub>U</sub>			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> to TC <sub>D</sub>			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>n</sub>			215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t <sub>W</sub>	up, down clock pulse width HIGH or LOW	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	120 24 20			150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 10
t <sub>W</sub>	parallel load pulse width LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time PL to CP <sub>U</sub> , CP <sub>D</sub>	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to CP <sub>U</sub> , CP <sub>D</sub>	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t <sub>h</sub>	hold time D <sub>n</sub> to PL	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
f <sub>max</sub>	maximum up, down clock pulse frequency	100 20 17			125 25 21		150 30 26		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.35
CP <sub>U</sub> , CP <sub>D</sub>	1.40
PL	0.65
MR	1.05

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> , CP <sub>D</sub> to Q <sub>n</sub>			43		54		65	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> to TC <sub>U</sub>			30		38		45	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> to TC <sub>D</sub>			30		38		45	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>n</sub>			44		55		66	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>			40		50		60	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			15		19		22	ns	4.5	Fig. 10
t <sub>W</sub>	up, down clock pulse width HIGH or LOW	25			31			38	ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	24			30			36	ns	4.5	Fig. 10
t <sub>W</sub>	parallel load pulse width LOW	20			25			30	ns	4.5	Fig. 9
t <sub>rem</sub>	removal time PL to CP <sub>U</sub> , CP <sub>D</sub>	10			13			15	ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to CP <sub>U</sub> , CP <sub>D</sub>	10			13			15	ns	4.5	Fig. 10
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	20			25			30	ns	4.5	Fig. 11
t <sub>h</sub>	hold time D <sub>n</sub> to PL	0			0			0	ns	4.5	Fig. 11
f <sub>max</sub>	maximum up, down clock pulse frequency	20			25			30	MHz	4.5	Fig. 7

AC WAVEFORMS

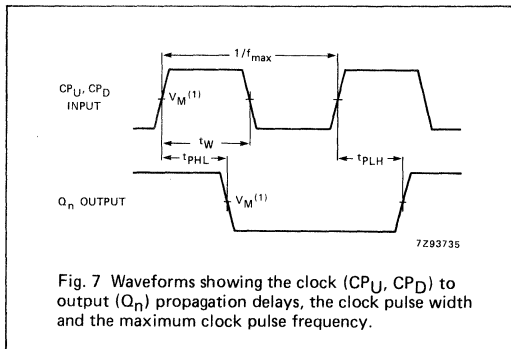


Fig. 7 Waveforms showing the clock ( $CP_U, CP_D$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width and the maximum clock pulse frequency.

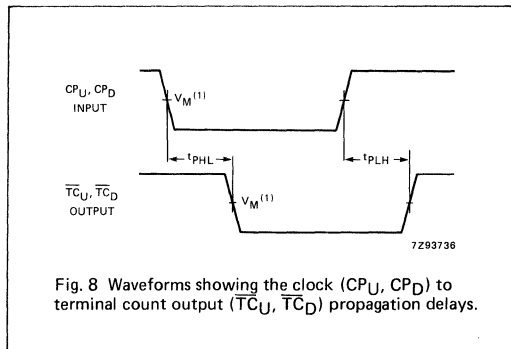


Fig. 8 Waveforms showing the clock ( $CP_U, CP_D$ ) to terminal count output ( $TC_U, TC_D$ ) propagation delays.

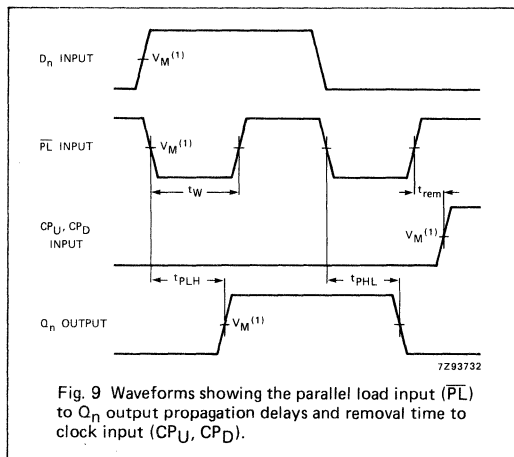


Fig. 9 Waveforms showing the parallel load input ( $PL$ ) to  $Q_n$  output propagation delays and removal time to clock input ( $CP_U, CP_D$ ).

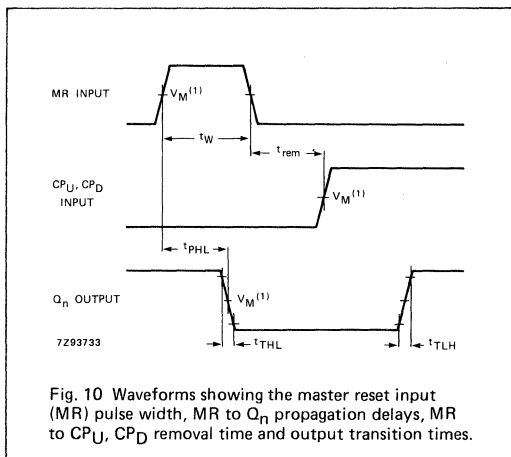


Fig. 10 Waveforms showing the master reset input ( $MR$ ) pulse width,  $MR$  to  $Q_n$  propagation delays,  $MR$  to  $CP_U, CP_D$  removal time and output transition times.

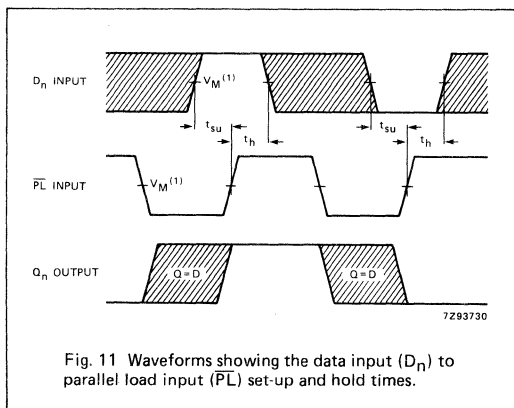


Fig. 11 Waveforms showing the data input ( $D_n$ ) to parallel load input ( $PL$ ) set-up and hold times.

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT193

MSI

## PRESETTABLE SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

### FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CP<sub>U</sub> and CP<sub>D</sub> respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP<sub>U</sub> clock is pulsed while CP<sub>D</sub> is held HIGH, the device will count up. If the CP<sub>D</sub> clock is pulsed while CP<sub>U</sub> is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (PL).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP<sub>D</sub> input will decrease the count by one, while a similar transition on the CP<sub>U</sub> input will advance the count by one.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> , CP <sub>U</sub> to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	19	19	ns
f <sub>max</sub>	maximum clock frequency		40	40	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CP <sub>D</sub>	power dissipation capacitance per package	notes 1 and 2	42	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CP<sub>D</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CP_D \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

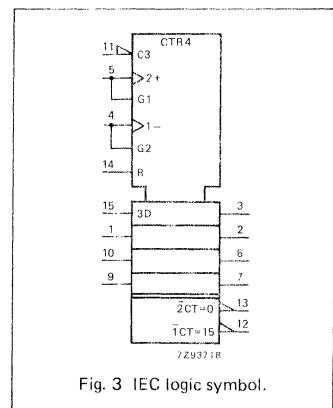
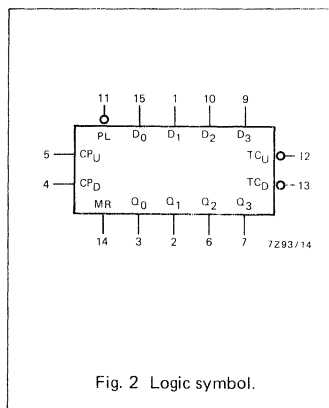
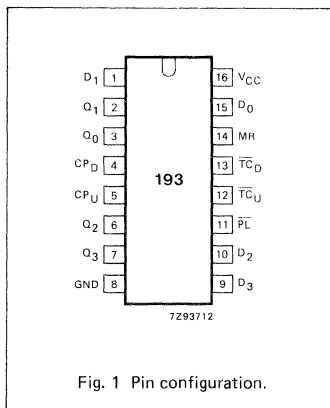
PC74HC/HCT193P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT193T: 16-lead mini-pack; plastic (SO-16, SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q <sub>0</sub> to Q <sub>3</sub>	flip-flop outputs
4	CP <sub>D</sub>	count down clock input*
5	CP <sub>U</sub>	count up clock input*
8	GND	ground (0 V)
11	PL	asynchronous parallel load input (active LOW)
12	TC <sub>U</sub>	terminal count up (carry) output (active LOW)
13	TC <sub>D</sub>	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage

\* LOW-to-HIGH, edge triggered



**GENERAL DESCRIPTION (Cont'd)**

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ( $\overline{TC}_U$ ) and terminal count down ( $\overline{TC}_D$ ) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of  $CP_U$  will cause  $\overline{TC}_U$  to go LOW.

$\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again, duplicating the count up clock.

Likewise, the  $\overline{TC}_D$  output will go LOW when the circuit is in the zero state and the  $CP_D$  goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a

multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs ( $D_0$  to  $D_3$ ) is loaded into the counter and appears on the outputs ( $Q_0$  to  $Q_3$ ) regardless of the conditions of the clock inputs when the parallel load ( $\overline{PL}$ ) input is LOW. A HIGH level on the master reset ( $\overline{MR}$ ) input will disable the parallel load gates, override both clock inputs and set all outputs ( $Q_0$  to  $Q_3$ ) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

**FUNCTION TABLE**

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	$CP_U$	$CP_D$	$D_0$	$D_1$	$D_2$	$D_3$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H H	X X	X X	L H	X X	X X	X X	X X	L L	L L	L L	L L	H H	L H
parallel load	L L L L	L L L L	X X L H	L H X X	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	H H L H	L H H H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X	X	count down				H	H**

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

\*  $\overline{TC}_U = CP_U$  at terminal count up (HHHH)

\*\*  $\overline{TC}_D = CP_D$  at terminal count down (LLLL)

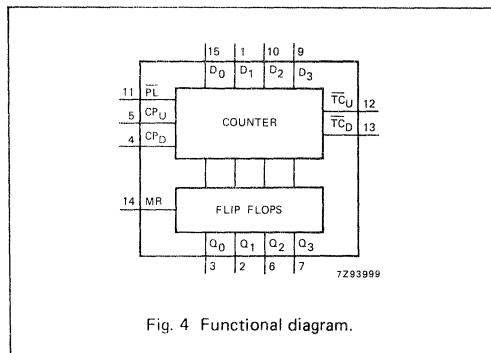


Fig. 4 Functional diagram.

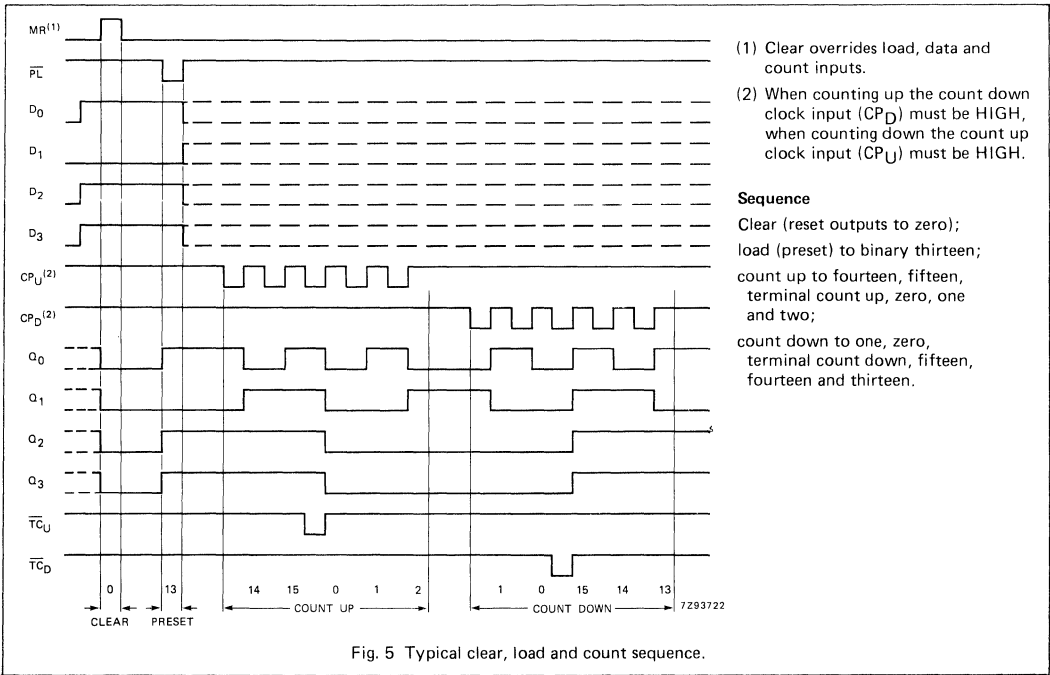


Fig. 5 Typical clear, load and count sequence.

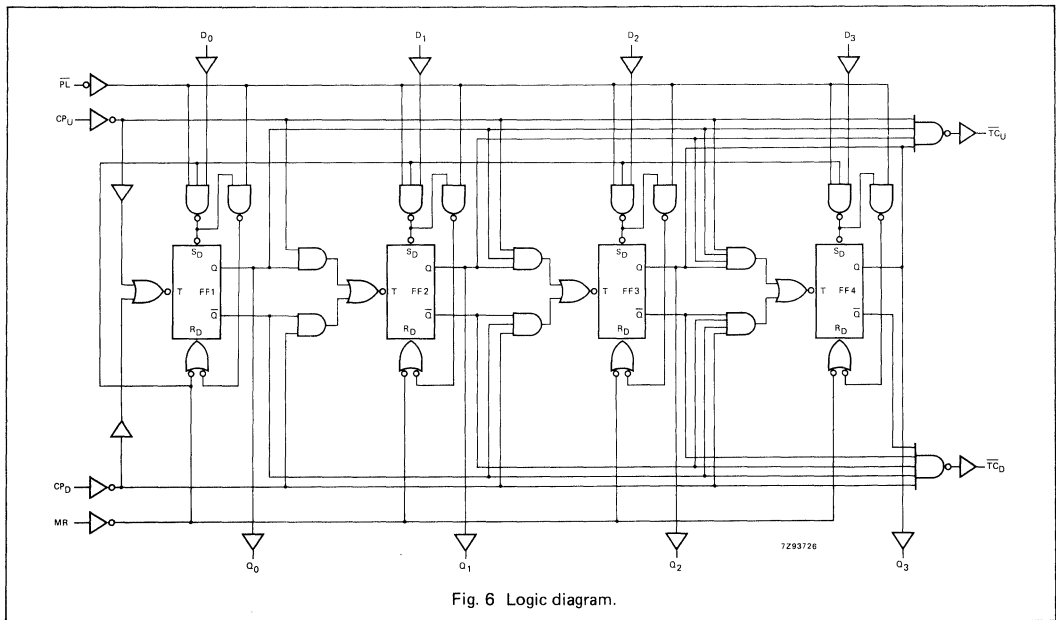


Fig. 6 Logic diagram.



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> , CP <sub>D</sub> to Q <sub>n</sub>			215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> to $\overline{TC}_U$			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> to $\overline{TC}_D$			125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>n</sub>			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 10
t <sub>W</sub>	up, down clock pulse width HIGH or LOW	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	120 24 20			150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 10
t <sub>W</sub>	parallel load pulse width LOW	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time PL to CP <sub>U</sub> , CP <sub>D</sub>	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to CP <sub>U</sub> , CP <sub>D</sub>	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t <sub>h</sub>	hold time D <sub>n</sub> to PL	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
f <sub>max</sub>	maximum up, down clock pulse frequency	4.0 20 24			3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.35
CP <sub>U</sub> , CP <sub>D</sub>	1.40
PL	0.65
MR	1.05

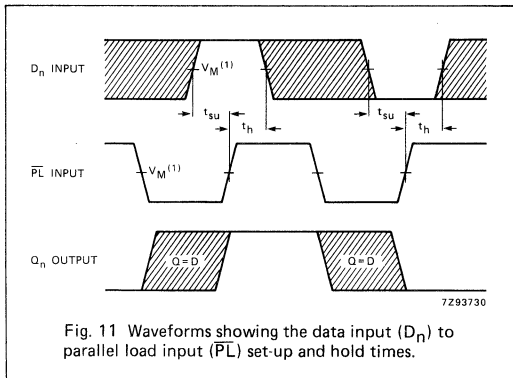
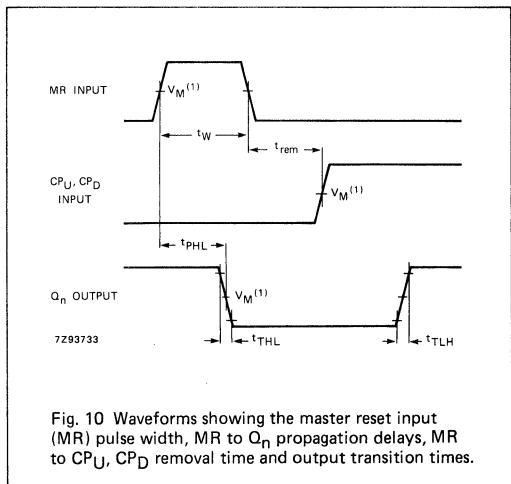
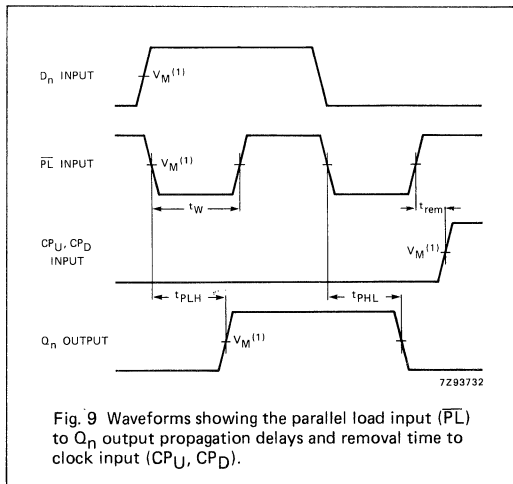
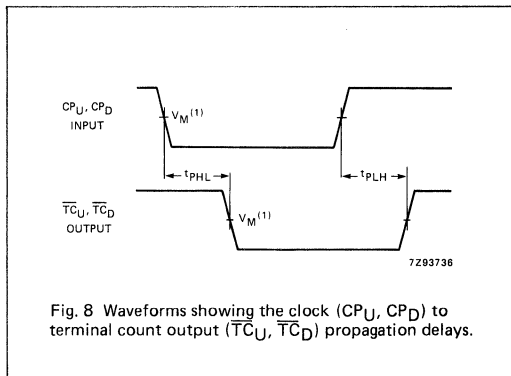
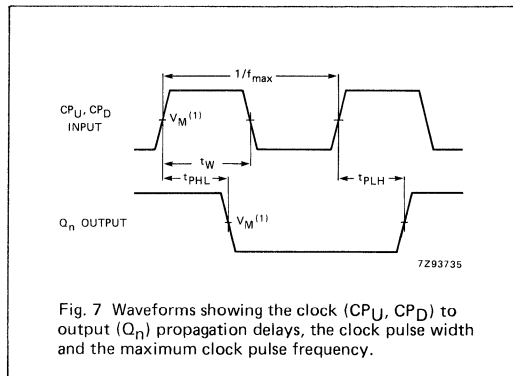
**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> , CP <sub>D</sub> to Q <sub>n</sub>			43		54		65	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>U</sub> to $\overline{TC}_U$			30		38		45	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>D</sub> to $\overline{TC}_D$			30		38		45	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>n</sub>			46		58		69	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>			40		50		60	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			15		19		22	ns	4.5	Fig. 10
t <sub>W</sub>	up, down clock pulse width HIGH or LOW	25			31			38	ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	24			30			36	ns	4.5	Fig. 10
t <sub>W</sub>	parallel load pulse width LOW	20			25			30	ns	4.5	Fig. 9
t <sub>rem</sub>	removal time PL to CP <sub>U</sub> , CP <sub>D</sub>	10			13			15	ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to CP <sub>U</sub> , CP <sub>D</sub>	10			13			15	ns	4.5	Fig. 10
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	20			25			30	ns	4.5	Fig. 11
t <sub>h</sub>	hold time D <sub>n</sub> to PL	0			0			0	ns	4.5	Fig. 11
f <sub>max</sub>	maximum up, down clock pulse frequency	20			16			13	MHz	4.5	Fig. 7

AC WAVEFORMS



**Note to Fig. 11**  
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Note to AC waveforms**  
(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

### FEATURES

- Shift-left and shift-right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold ("do nothing") mode
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The "194" design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs (S<sub>0</sub>, S<sub>1</sub>). As shown in the mode select table, data can be entered and shifted from left to right (Q<sub>0</sub> → Q<sub>1</sub> → Q<sub>2</sub>, etc.) or, right to left (Q<sub>3</sub> → Q<sub>2</sub> → Q<sub>1</sub>, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S<sub>0</sub> and S<sub>1</sub> are LOW, existing data is retained in a hold ("do nothing") mode. The first and last stages provide D-type serial data inputs (D<sub>SR</sub>, D<sub>SL</sub>) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data (continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	15	ns
t <sub>PHL</sub>	$\overline{MR}$ to Q <sub>n</sub>		11	15	ns
f <sub>max</sub>	maximum clock frequency		102	77	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	40	40	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT194P: 16-lead DIL, plastic (SOT-38Z).

PC74HC/HCT194T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset input (active LOW)
2	D <sub>SR</sub>	serial data input (shift right)
3, 4, 5, 6	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
7	D <sub>SL</sub>	serial data input (shift left)
8	GND	ground (0 V)
9, 10	S <sub>0</sub> , S <sub>1</sub>	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
16	V <sub>CC</sub>	positive supply voltage

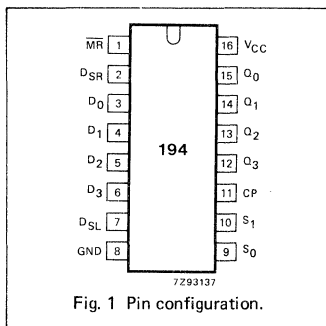


Fig. 1 Pin configuration.

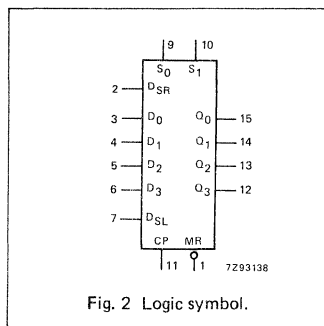


Fig. 2 Logic symbol.

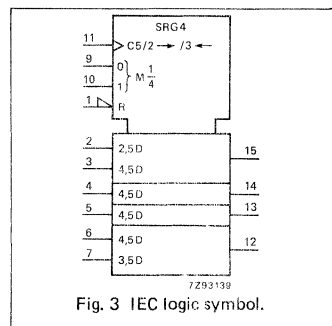


Fig. 3 IEC logic symbol.

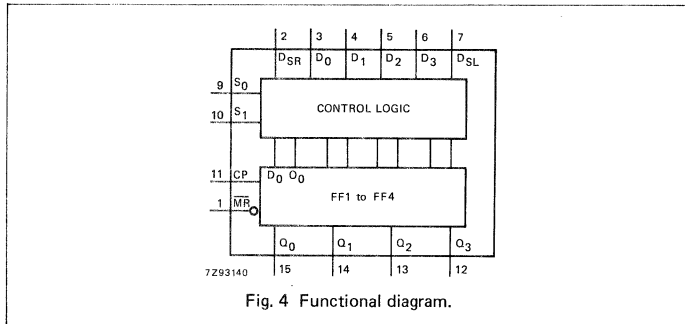


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS			
	CP	MR	S <sub>1</sub>	S <sub>0</sub>	DSR	DSL	D <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	l	l	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>
shift left	↑	H	h	l	X	l	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	L
	↑	H	h	l	X	h	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	H
shift right	↑	H	l	h	l	X	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
	↑	H	l	h	h	X	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
parallel load	↑	H	h	h	X	X	d <sub>n</sub>	d <sub>0</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>

GENERAL DESCRIPTION (Cont'd.)

inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D<sub>0</sub> to D<sub>3</sub>) are D-type inputs. Data appearing on the D<sub>0</sub> to D<sub>3</sub> inputs, when S<sub>0</sub> and S<sub>1</sub> are HIGH, is transferred to the Q<sub>0</sub> to Q<sub>3</sub> outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset (MR) overrides all other input conditions and forces the Q outputs LOW.

The "194" is similar in operation to the "195" universal shift register, with added features of shift-left without external connections and hold ("do nothing") modes of operation.

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
- X = don't care
- ↑ = LOW-to-HIGH CP transition

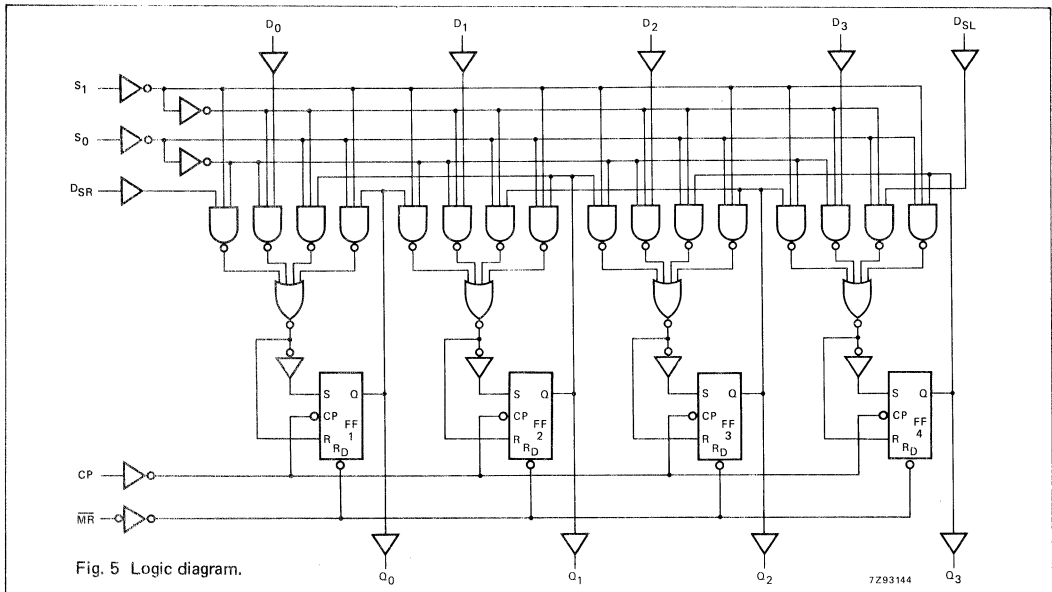


Fig. 5 Logic diagram.

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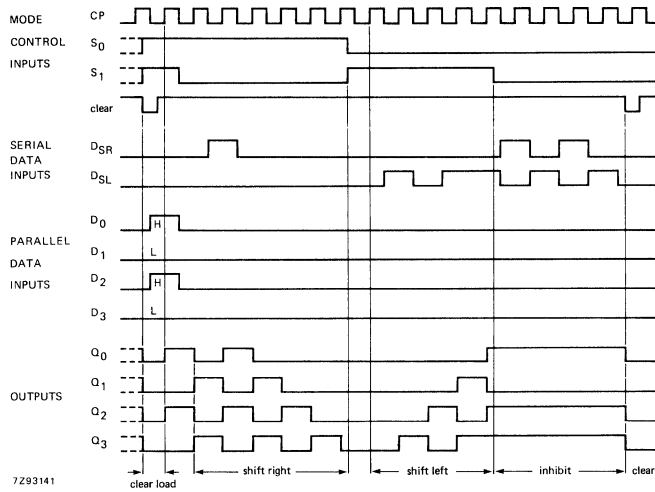


Fig. 6 Typical clear, clear-load, shift-right, shift-left, inhibit and clear timing sequences.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/$ $t_{PLH}$	propagation delay CP to $Q_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}$	propagation delay MR to $Q_n$		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
$t_W$	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_W$	master reset pulse width; LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
$t_{rem}$	removal time MR to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
$t_{su}$	set-up time $D_n$ to CP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 9
$t_{su}$	set-up time $S_0, S_1$ to CP	80 16 12	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
$t_{su}$	set-up time $D_{SR}, D_{SL}$ to CP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	
$t_h$	hold time $D_n$ to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
$t_h$	hold time $S_0, S_1$ to CP	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
$t_h$	hold time $D_{SR}, D_{SL}$ to CP	0 0 0	-17 -6 -5		0 0 0		0 0 0		ns	2.0 4.5 6.0	
$f_{max}$	maximum clock pulse frequency	6 30 35	31 93 100		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$D_n$	0.15
$D_{SR}, D_{SL}$	0.15
CP	0.50
$\overline{MR}$	0.45
$S_n$	0.90



## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	32		40		48	ns	4.5	Fig. 7
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		18	32		40		48	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20			24	ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width; LOW	16	7		20			24	ns	4.5	Fig. 8
t <sub>rem</sub>	removal time MR to CP	12	6		15			18	ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	14	7		18			21	ns	4.5	Fig. 9
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	20	7		25			30	ns	4.5	Fig. 10
t <sub>su</sub>	set-up time D <sub>SR</sub> , D <sub>SL</sub> to CP	14	10		18			21	ns	4.5	
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0	-7		0			0	ns	4.5	Fig. 9
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	0	-5		0			0	ns	4.5	Fig. 10
t <sub>h</sub>	hold time D <sub>SR</sub> , D <sub>SL</sub> to CP	0	-7		0			0	ns	4.5	
f <sub>max</sub>	maximum clock pulse frequency	30	70		24			20	MHz	4.5	Fig. 7

AC WAVEFORMS

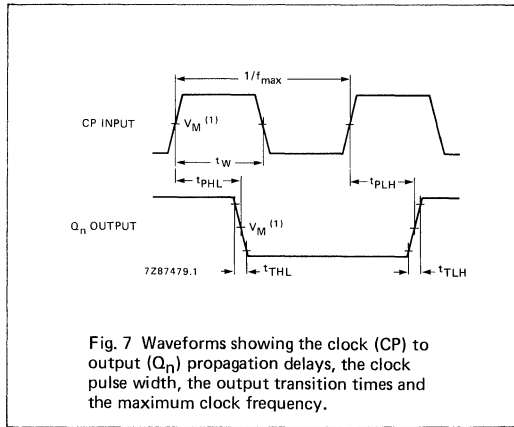


Fig. 7 Waveforms showing the clock (CP) to output (Q<sub>n</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

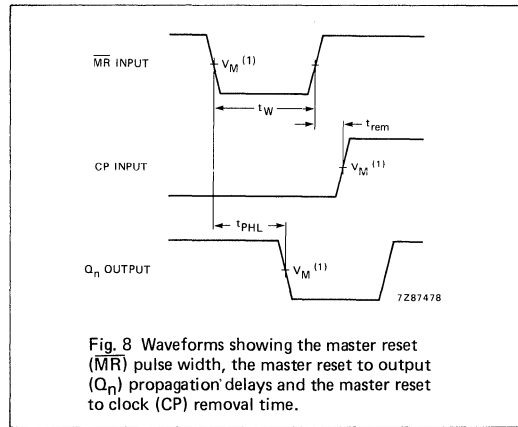


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q<sub>n</sub>) propagation delays and the master reset to clock (CP) removal time.

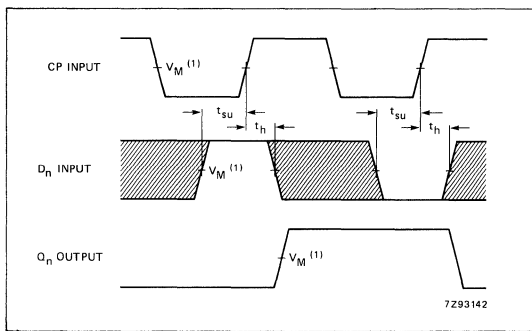


Fig. 9 Waveforms showing the set-up and hold times from the data inputs (D<sub>n</sub>) to the clock (CP).

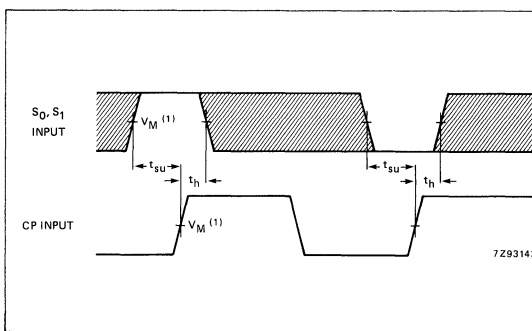


Fig. 10 Waveforms showing the set-up and hold times from the mode control inputs (S<sub>0</sub>, S<sub>1</sub>) to the clock input (CP).

Note to Figs 9 and 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3V.



## 4-BIT PARALLEL ACCESS SHIFT REGISTER

### FEATURES

- Asynchronous master reset
- J,  $\bar{K}$ , (D) inputs to the first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complement output from the last stage
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-to-serial data transfer at very high speeds. The "195" operates on two primary modes: shift right (Q<sub>0</sub> → Q<sub>1</sub>) and parallel load, which are controlled by the state of the parallel load enable ( $\bar{PE}$ ) input. Serial data enters the first flip-flop (Q<sub>0</sub>) via the J and  $\bar{K}$  inputs when the  $\bar{PE}$  input is HIGH and shifted one bit in the direction Q<sub>0</sub> → Q<sub>1</sub> → Q<sub>2</sub> → Q<sub>3</sub> following each LOW-to-HIGH clock transition. The J and  $\bar{K}$  inputs provide the flexibility of the JK type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the  $\bar{PE}$  input is LOW.

After the LOW-to-HIGH clock transition, data on the parallel inputs (D<sub>0</sub> to D<sub>3</sub>) is transferred to the respective Q<sub>0</sub> to Q<sub>3</sub> outputs. Shift left operation (Q<sub>3</sub> → Q<sub>2</sub>) can be achieved by tying the Q<sub>n</sub> outputs to the D<sub>n-1</sub> inputs and holding the  $\bar{PE}$  input LOW.

(continued on next page)

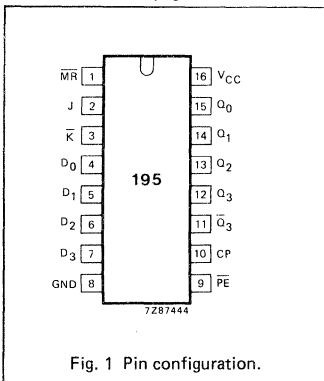


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	15	ns
f <sub>max</sub>	maximum clock frequency		57	57	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	105	105	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT195P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT195T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{MR}$	master reset input (active LOW)
2	J	first stage J-input (active HIGH)
3	$\bar{K}$	first stage $\bar{K}$ -input (active LOW)
4, 5, 6, 7	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
8	GND	ground (0 V)
9	$\bar{PE}$	parallel enable input (active LOW)
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	$\bar{Q}_3$	inverted output from the last stage
15, 14, 13, 12	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
16	V <sub>CC</sub>	positive supply voltage

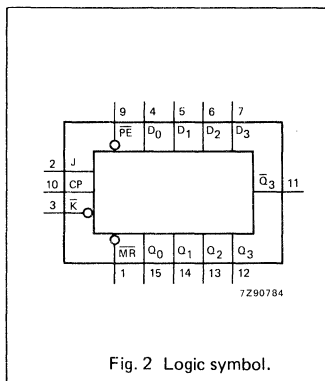


Fig. 2 Logic symbol.

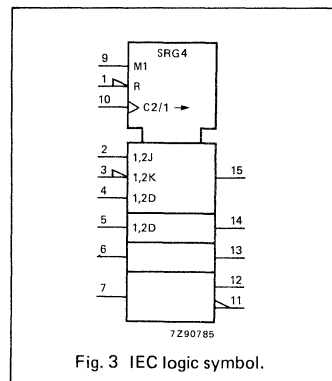


Fig. 3 IEC logic symbol.

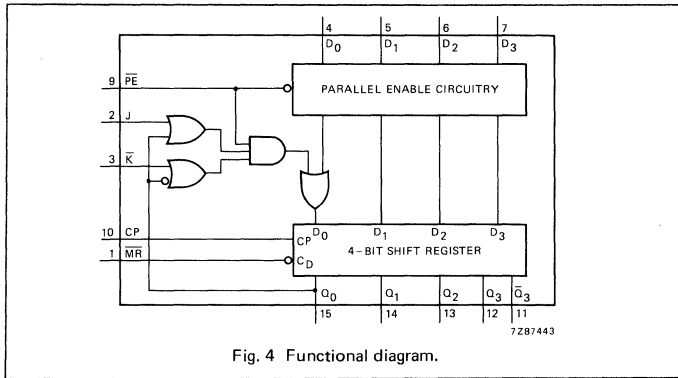


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. There is no restriction on the activity of the J, K, D<sub>n</sub> and PE inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset (MR) input sets all Q outputs LOW, independent of any other input condition.

**APPLICATIONS**

- Serial data transfer
- Parallel data transfer
- Serial-to-parallel data transfer
- Parallel-to-serial data transfer

**FUNCTION TABLE**

OPERATING MODES	INPUTS						OUTPUTS				
	MR	CP	PE	J	K	D <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>3</sub> <sup>bar</sup>
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub> <sup>bar</sup>
shift, reset first stage	H	↑	h	l	l	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub> <sup>bar</sup>
shift, toggle first stage	H	↑	h	h	l	X	q <sub>0</sub> <sup>bar</sup>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub> <sup>bar</sup>
shift, retain first stage	H	↑	h	l	h	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub> <sup>bar</sup>	
parallel load	H	↑	l	X	X	d <sub>n</sub>	d <sub>0</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>	d <sub>3</sub> <sup>bar</sup>

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition  
X = don't care  
↑ = LOW-to-HIGH clock transition

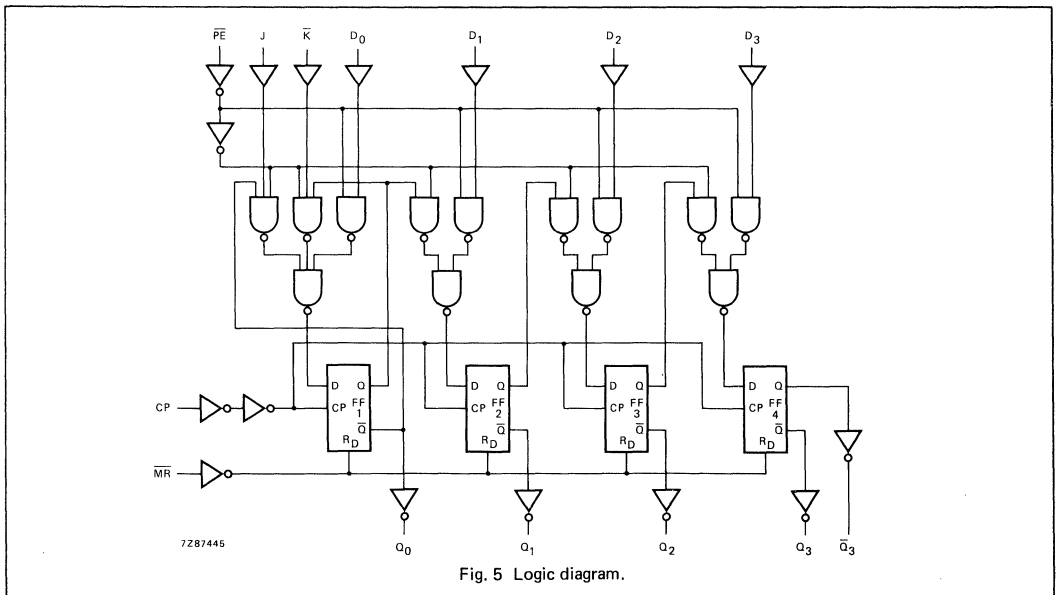


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25		-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{MR}$ to Q <sub>n</sub>	41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width; LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time $\overline{MR}$ to CP	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time J to CP	100 20 17	33 12 10		125 25 21		150 30 26	ns	2.0 4.5 6.0	Figs. 8 and 9
t <sub>su</sub>	set-up time $\overline{K}$ , $\overline{PE}$ , D <sub>n</sub> to CP	80 16 14	22 8 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Figs. 8 and 9
t <sub>h</sub>	hold time J, $\overline{K}$ , $\overline{PE}$ , D <sub>n</sub> to CP	3 3 3	-8 -3 -2		3 3 3		3 3 3	ns	2.0 4.5 6.0	Figs. 8 and 9
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	17 52 62		5 24 28		4 20 24	MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$\overline{PE}$	0.65
all others	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	32		40		48	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{MR}$ to Q <sub>n</sub>		17	35		44		53	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width; LOW	16	6		20		24		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time $\overline{MR}$ to CP	16	6		20		24		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time J, $\overline{K}$ , $\overline{PE}$ to CP	20	10		25		30		ns	4.5	Figs. 8 and 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	16	6		20		24		ns	4.5	Figs. 8 and 9
t <sub>h</sub>	hold time J, $\overline{K}$ , $\overline{PE}$ , D <sub>n</sub> to CP	3	-5		3		3		ns	4.5	Figs. 8 and 9
f <sub>max</sub>	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

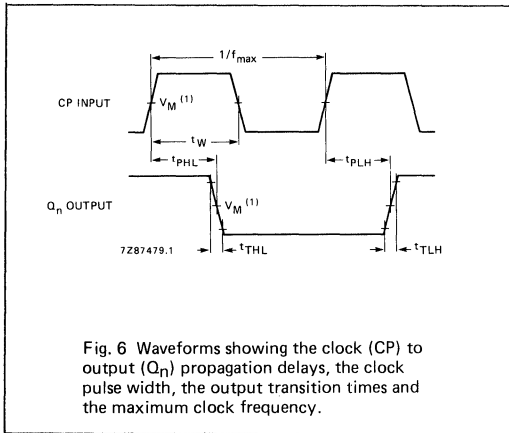


Fig. 6 Waveforms showing the clock (CP) to output (Q<sub>n</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

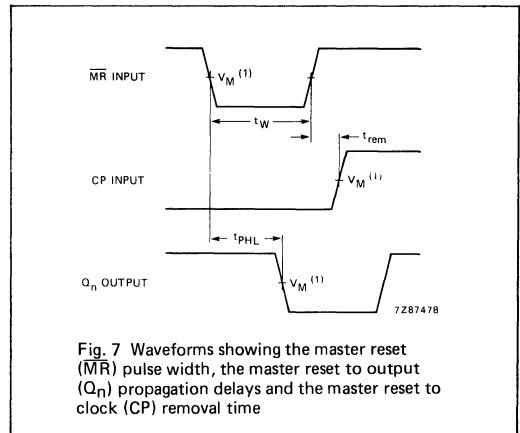


Fig. 7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output (Q<sub>n</sub>) propagation delays and the master reset to clock (CP) removal time

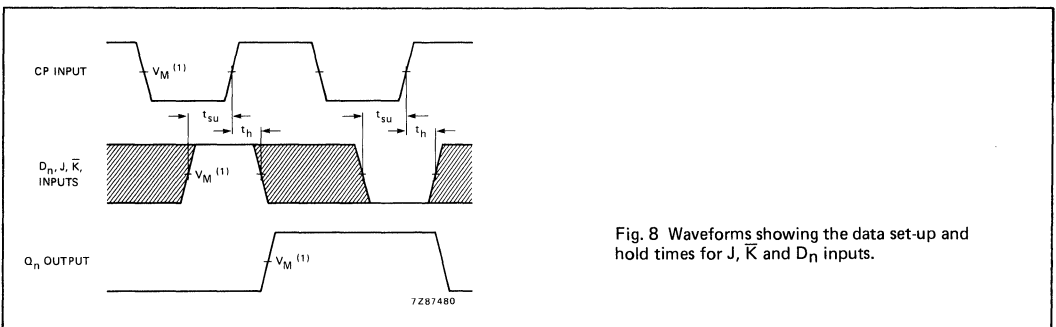


Fig. 8 Waveforms showing the data set-up and hold times for J,  $\overline{K}$  and D<sub>n</sub> inputs.

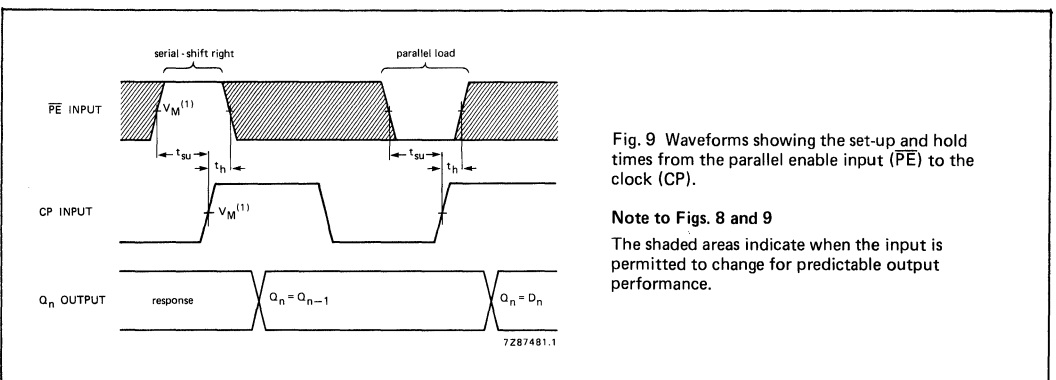


Fig. 9 Waveforms showing the set-up and hold times from the parallel enable input (PE) to the clock (CP).

Note to Figs. 8 and 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.

HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.



DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

FEATURES

- Pulse width variance is typically less than  $\pm 5\%$
- Pin-out identical to "123"
- Overriding reset terminates output pulse
- nB inputs have hysteresis for improved noise immunity
- Wide pulse range: 70 ns (typ) to  $\infty$
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT221 are dual non-retriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input (nA) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs (nQ, nQ) are independent of further transitions of nA and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs (nRD). Input pulses may be of any duration relative to the output pulse. The output pulse length may be varied from 35 ns to the maximum shown in the features by choosing appropriate timing components. With R<sub>EXT</sub> = 2 kΩ and C<sub>EXT</sub> = 28 pF, an output pulse of typical 70 ns is achieved which may be used as a DC triggered reset signal.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nRD to nQ, nQ	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V R <sub>EXT</sub> = 5 kΩ C <sub>EXT</sub> = 0 pF	30	32	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT221P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT221T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	1RD, 2RD	direct reset inputs (active LOW)
4, 12	1Q, 2Q	outputs (active LOW)
7	2REXT/CEXT	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	1CEXT, 2CEXT	external capacitor connection
15	1REXT/CEXT	external resistor/capacitor connection
16	VCC	positive supply voltage

Note

It is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

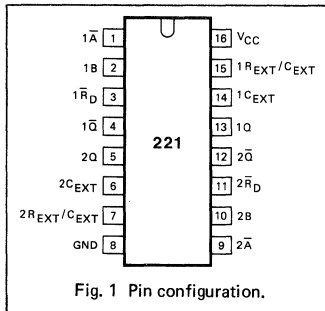


Fig. 1 Pin configuration.

**GENERAL DESCRIPTION (Cont'd)**

Pulse width stability is achieved through internal compensation and is virtually independent of  $V_{CC}$  and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

Jitter-free operation is maintained over the full temperature and  $V_{CC}$  ranges for more than six decades of timing capacitance (10 pF to 10  $\mu$ F) and more than two decade of timing resistance (2 k $\Omega$  to any practical value) for the 74HC/HCT221.

Throughout these ranges the output pulse width is defined by the following relationship:

$$t_W = C_{EXT}R_{EXT} \ln 2$$

$$t_W = 0.7C_{EXT}R_{EXT}$$

In circuits where pulse cut-off is not critical, timing capacitance up to 1000  $\mu$ F and timing resistance as low as 1.4 k $\Omega$  may be used.

Pin assignments for the "221" are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of  $R_{EXT}$  and/or  $C_{EXT}$ .

DEVELOPMENT DATA

**FUNCTION TABLE**

INPUTS			OUTPUTS	
$n\bar{R}_D$	$n\bar{A}$	$nB$	$nQ$	$n\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

= one HIGH-level output pulse

= one LOW-level output pulse

3-TO-8 DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

FEATURES

- Combines 1-of-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT237 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT237 are 3-of-8 decoder/demultiplexers with latches at the three address inputs (A<sub>n</sub>). The "237" essentially combines the 3-of-8 decoder function with a 3-bit storage latch. When the latch is enabled ( $\overline{LE} = \text{LOW}$ ), the "237" acts as a 3-of-8 active LOW decoder. When the latch enable ( $\overline{LE}$ ) goes from LOW-to-HIGH, the last data present at the inputs, before this transition, is stored in the latches. Further address changes are ignored as long as  $\overline{LE}$  remains HIGH.

The output enable input ( $\overline{E}_1$  and E<sub>2</sub>) controls the state of the outputs independent of the address inputs or latch operation. All outputs are LOW unless  $\overline{E}_1$  is LOW and E<sub>2</sub> is HIGH.

The "237" is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

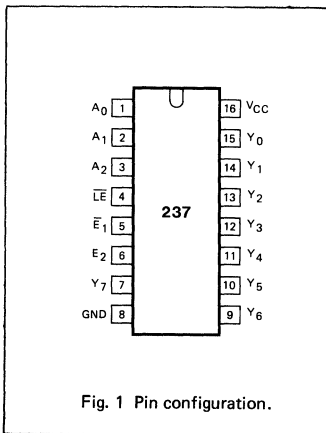


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT237P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT237T: 16-lead mini-pack; plastic (SO-16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	data inputs
4	$\overline{LE}$	latch enable input (active LOW)
5	E <sub>1</sub>	data enable input (active LOW)
6	E <sub>2</sub>	data enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	Y <sub>0</sub> to Y <sub>7</sub>	multiplexer outputs
16	V <sub>CC</sub>	positive supply voltage

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{LE}$	$\overline{E}_1$	E <sub>2</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>	Y <sub>4</sub>	Y <sub>5</sub>	Y <sub>6</sub>	Y <sub>7</sub>
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

### 3-TO-8 LINE DECODER/DEMULTIPLEXER

#### FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active HIGH mutually exclusive outputs
- Output capability: standard
- ICC category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT238 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT238 decoders accept three binary weighted address inputs ( $A_0, A_1, A_2$ ) and when enabled, provide 8 mutually exclusive active HIGH outputs ( $Y_0$  to  $Y_7$ ).

The "238" features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH ( $E_3$ ). Every output will be LOW unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH.

This multiple enable function allows easy parallel expansion of the "238" to a 1-of-32 (5 lines to 32 lines) decoder with just four "238" ICs and one inverter.

The "238" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "238" is identical to the "138" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15	20	ns
	$A_n$ to $Y_n$		17	21	ns
	$E_3$ to $Y_n$ $E_n$ to $Y_n$		17	21	ns
$C_I$	input capacitance		3.5	3.5	pF
$CPD$	power dissipation capacitance per package	notes 1 and 2	72	76	pF

$GND = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t_r = t_f = 6 \text{ ns}$

#### Notes

1.  $CPD$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

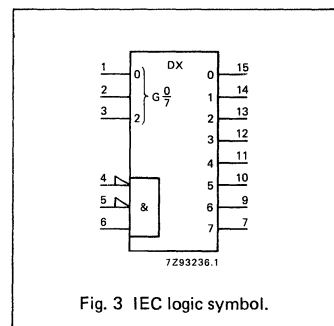
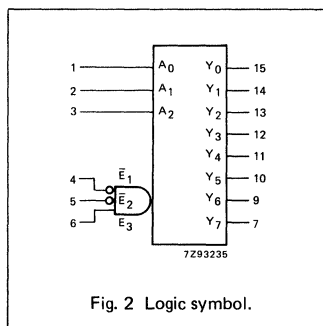
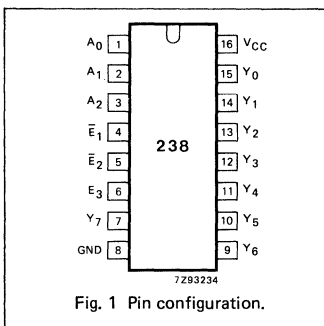
#### ORDERING INFORMATION/PACKAGE OUTLINES

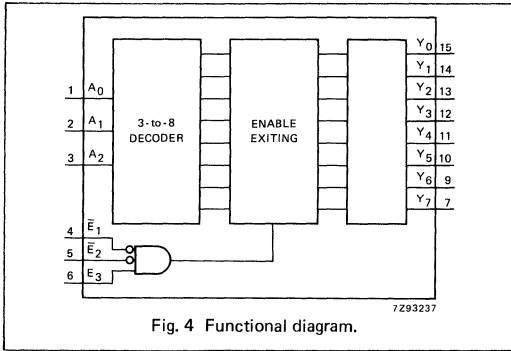
PC74HC/HCT238P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT238T: 16-lead mini-pack; plastic (SO-16, SOT109A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	$A_0$ to $A_2$	address inputs
4, 5	$\bar{E}_1, \bar{E}_2$	enable inputs (active LOW)
6	$E_3$	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12	$Y_0$ to $Y_7$	outputs (active HIGH)
11, 10, 9, 7		
16	$V_{CC}$	positive supply voltage

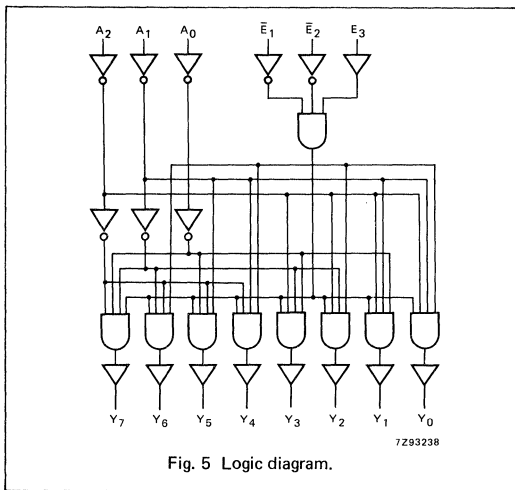




FUNCTION TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	L	L	L	L	H	L	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	L	H	L	L	L
L	L	H	L	L	L	L	L	L	L	L	H	L	L
L	L	H	L	L	L	L	L	L	L	L	L	H	L
L	L	H	L	L	L	L	L	L	L	L	L	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $A_n$ to $Y_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $E_3$ to $Y_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay $\bar{E}_n$ to $Y_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	0.70
E <sub>n</sub>	0.40
E <sub>3</sub>	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		20	35		53		63	ns	4.5	Fig. 6
t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		20	35		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay E <sub>3</sub> to Y <sub>n</sub>		25	40		60		72	ns	4.5	Fig. 6
t <sub>PLH</sub>	propagation delay E <sub>3</sub> to Y <sub>n</sub>		18	34		43		51	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay E <sub>n</sub> to Y <sub>n</sub>		25	40		55		66	ns	4.5	Fig. 7
t <sub>PLH</sub>	propagation delay E <sub>n</sub> to Y <sub>n</sub>		25	40		65		78	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

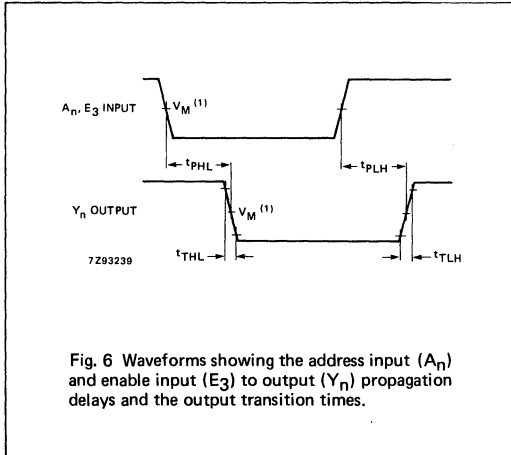


Fig. 6 Waveforms showing the address input (A<sub>n</sub>) and enable input (E<sub>3</sub>) to output (Y<sub>n</sub>) propagation delays and the output transition times.

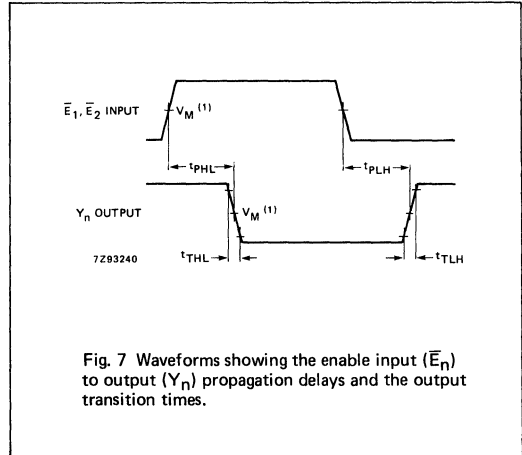


Fig. 7 Waveforms showing the enable input (E<sub>n</sub>) to output (Y<sub>n</sub>) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.



**OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING**

**FEATURES**

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT240 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT240 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1 $\overline{O}E$  and 2 $\overline{O}E$ . A HIGH on n $\overline{O}E$  causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

**FUNCTION TABLE**

INPUTS		OUTPUT
n $\overline{O}E$	nA <sub>n</sub>	nY <sub>n</sub>
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	9	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

- CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

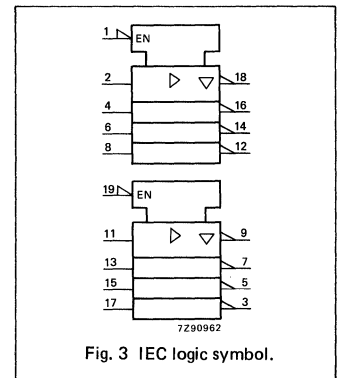
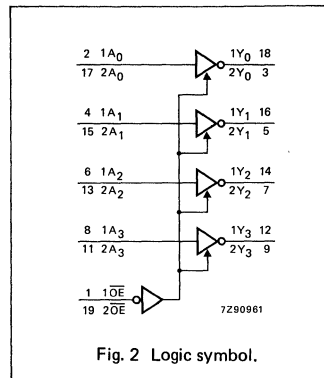
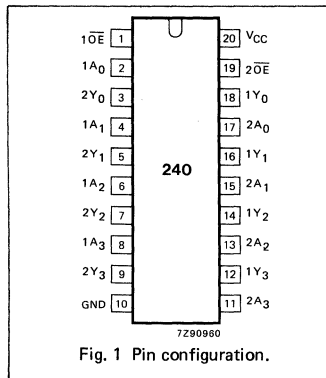
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
- For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT240P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT240T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1 $\overline{O}E$	output enable input (active LOW)
2, 4, 6, 8	1A <sub>0</sub> to 1A <sub>3</sub>	data inputs
3, 5, 7, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A <sub>0</sub> to 2A <sub>3</sub>	data inputs
18, 16, 14, 12	1Y <sub>0</sub> to 1Y <sub>3</sub>	bus outputs
19	2 $\overline{O}E$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage



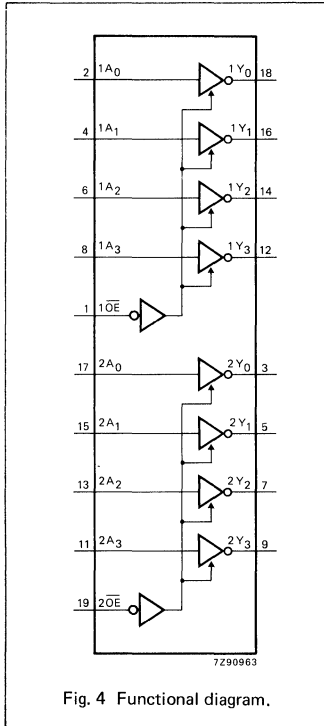


Fig. 4 Functional diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		30 11	100 20		125 25		150 30	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
1A <sub>n</sub>	1.50
2A <sub>n</sub>	1.50
1 $\overline{O}E$	0.70
2 $\overline{O}E$	0.70

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		11	20		25		30	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1 $\overline{O}E$ to 1Y <sub>n</sub> ; 2 $\overline{O}E$ to 2Y <sub>n</sub>		13	30		38		45	ns	4.5	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1 $\overline{O}E$ to 1Y <sub>n</sub> ; 2 $\overline{O}E$ to 2Y <sub>n</sub>		13	25		31		38	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

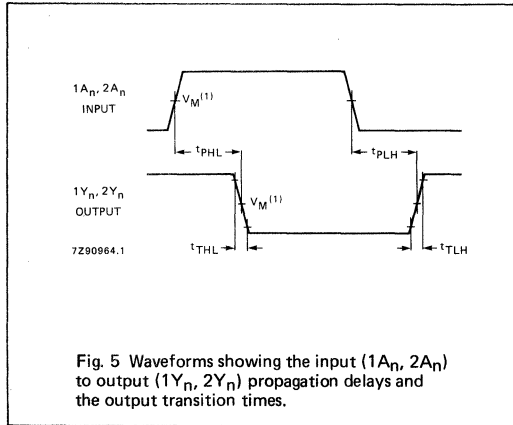


Fig. 5 Waveforms showing the input (1A<sub>n</sub>, 2A<sub>n</sub>) to output (1Y<sub>n</sub>, 2Y<sub>n</sub>) propagation delays and the output transition times.

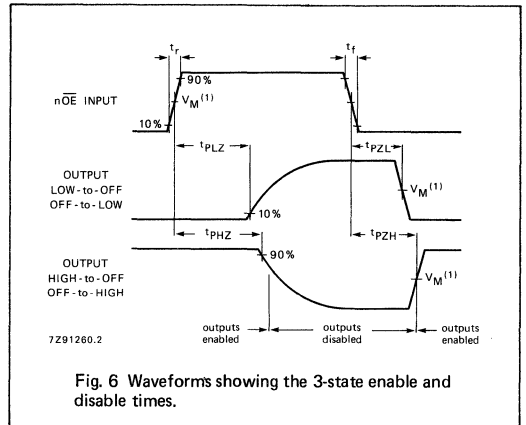


Fig. 6 Waveforms showing the 3-state enable and disable times.

**OCTAL BUFFER/LINE DRIVER; 3-STATE**

**FEATURES**

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT241 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT241 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE.

**FUNCTION TABLES**

INPUTS		OUTPUT
1OE	1A <sub>n</sub>	1Y <sub>n</sub>
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	2A <sub>n</sub>	2Y <sub>n</sub>
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT241P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT241T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1OE	output enable input (active LOW)
2, 4, 6, 8	1A <sub>0</sub> to 1A <sub>3</sub>	data inputs
3, 5, 7, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A <sub>0</sub> to 2A <sub>3</sub>	data inputs
18, 16, 14, 12	1Y <sub>0</sub> to 1Y <sub>3</sub>	bus outputs
19	2OE	output enable input (active HIGH)
20	V <sub>CC</sub>	positive supply voltage

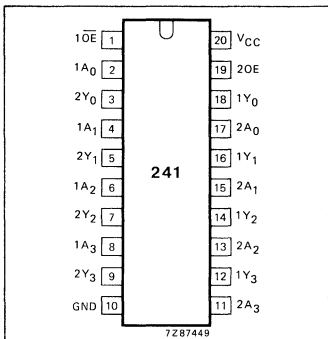


Fig. 1 Pin configuration.

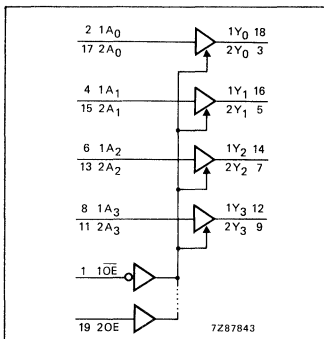


Fig. 2 Logic symbol.

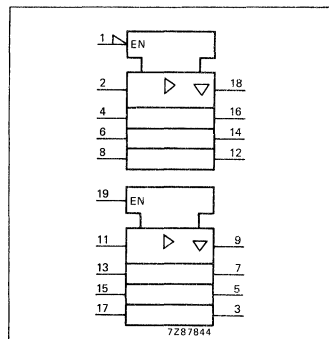


Fig. 3 IEC logic symbol.

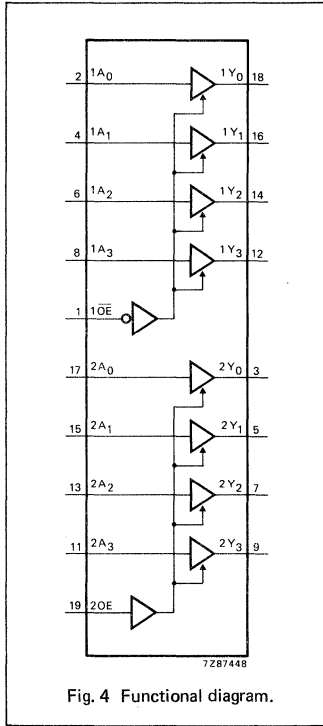


Fig. 4 Functional diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		25 9 7	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

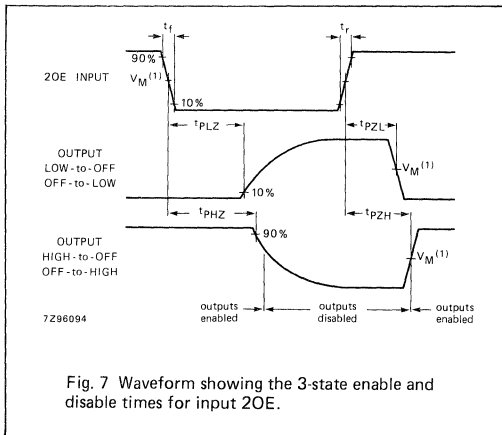
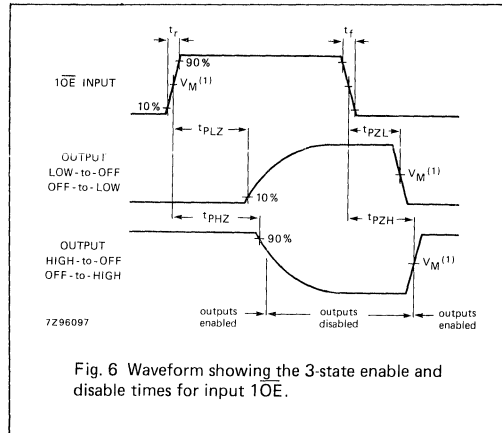
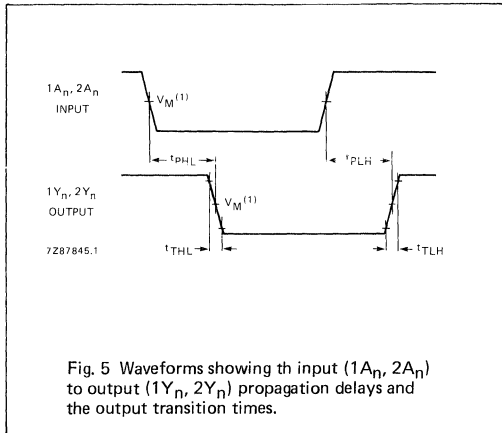
input	unit load coefficient
1A <sub>n</sub>	0.70
2A <sub>n</sub>	0.70
1O <sub>E</sub>	0.70
2O <sub>E</sub>	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		13	22		28		33	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1O <sub>E</sub> to 1Y <sub>n</sub> ; 2O <sub>E</sub> to 2Y <sub>n</sub>		15	30		38		45	ns	4.5	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1O <sub>E</sub> to 1Y <sub>n</sub> ; 2O <sub>E</sub> to 2Y <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



**QUAD BUS TRANSCEIVER; 3-STATE; INVERTING**

**FEATURES**

- Inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT242 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT242 are quad bus transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ( $\overline{OE}_A$  and  $OE_B$ ) can be used to isolate the buses.

The "242" is similar to the "243" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	50	58	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT242P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT242T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	A <sub>0</sub> to A <sub>3</sub>	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B <sub>0</sub> to B <sub>3</sub>	data inputs/outputs
13	$OE_B$	output enable input
14	V <sub>CC</sub>	positive supply voltage

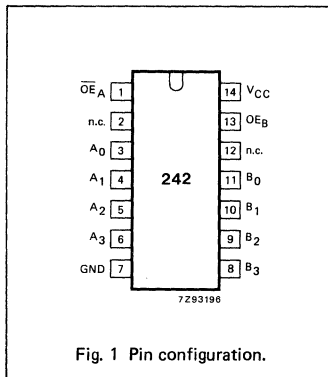


Fig. 1 Pin configuration.

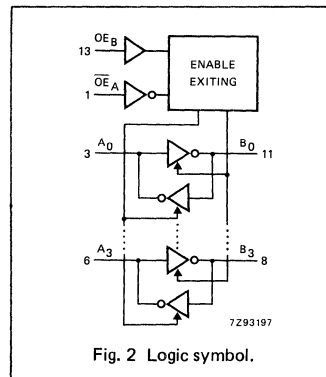


Fig. 2 Logic symbol.

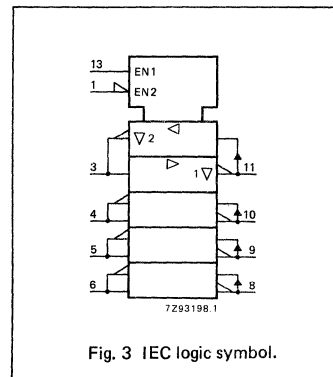
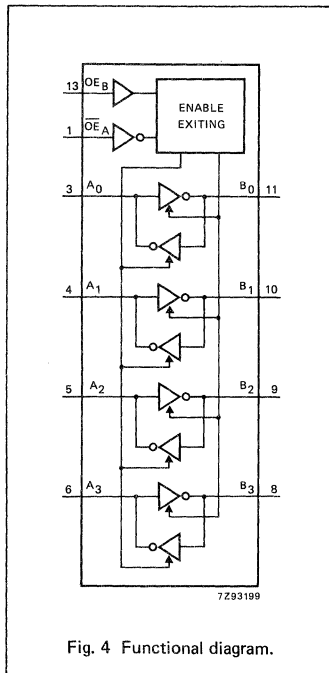


Fig. 3 IEC logic symbol.



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	$OE_B$	$A_n$	$B_n$
L	L	inputs	$B = \overline{A}$
H	L	Z	Z
L	H	Z	Z
H	H	$A = \overline{B}$	inputs

H = HIGH voltage level  
L = LOW voltage level  
Z = high impedance OFF-state

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		30 11	100 20		125 25		150 30	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		61 22 18	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	0.75
B <sub>n</sub>	0.75
OE <sub>A</sub>	0.75
OE <sub>B</sub>	0.75

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		16	28		35		42	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		24	40		50		60	ns	4.5	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		26	40		50		60	ns	4.5	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

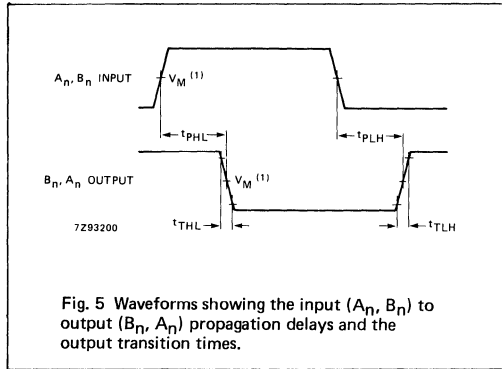


Fig. 5 Waveforms showing the input ( $A_n, B_n$ ) to output ( $B_n, A_n$ ) propagation delays and the output transition times.

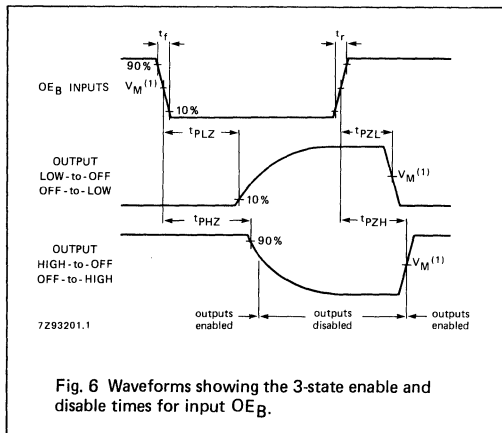


Fig. 6 Waveforms showing the 3-state enable and disable times for input  $OE_B$ .

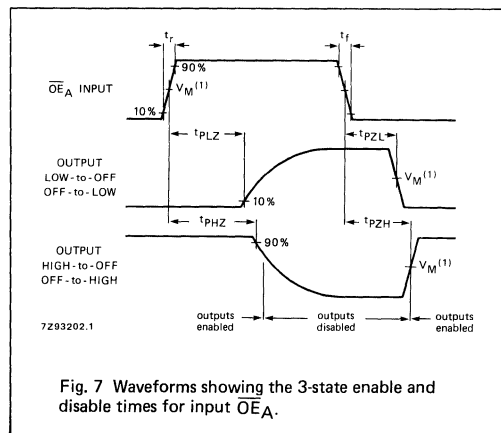


Fig. 7 Waveforms showing the 3-state enable and disable times for input  $OE_A$ .

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





## QUAD BUS TRANSCEIVER; 3-STATE

### FEATURES

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ( $\overline{OE}_A$  and  $OE_B$ ) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 15$ pF $V_{CC} = 5$ V	11	14	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
CPD	power dissipation capacitance per transceiver	notes 1 and 2	50	54	pF

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns

### Notes

1. CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5$  V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT243P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT243T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	$A_0$ to $A_3$	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	$B_0$ to $B_3$	data inputs/outputs
13	$OE_B$	output enable input
14	$V_{CC}$	positive supply voltage

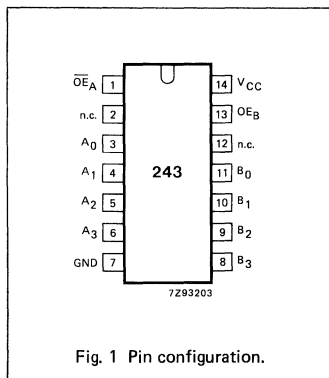


Fig. 1 Pin configuration.

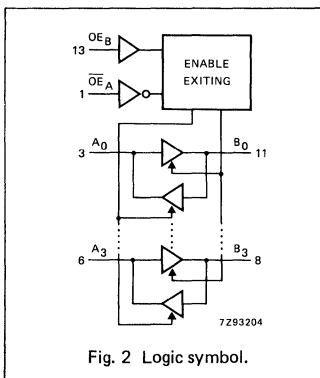


Fig. 2 Logic symbol.

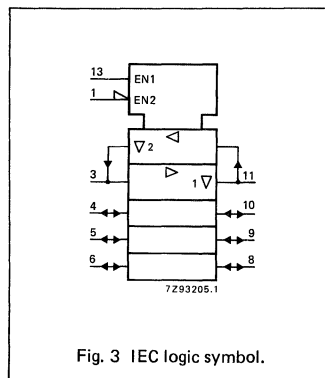
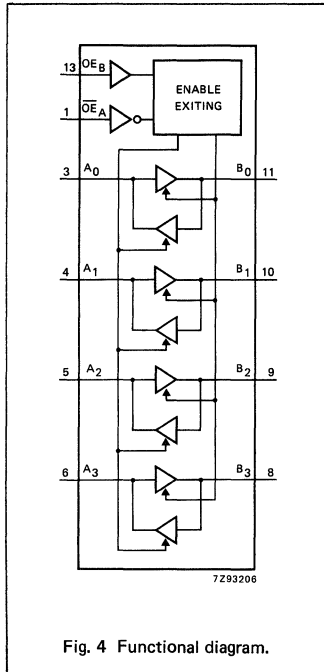


Fig. 3 IEC logic symbol.



**FUNCTION TABLE**

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	$\overline{OE}_B$	$A_n$	$B_n$
L	L	inputs	$B = A$
H	L	Z	Z
L	H	Z	Z
H	H	$A = B$	inputs

H = HIGH voltage level  
L = LOW voltage level  
Z = high impedance OFF-state

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		61 22 18	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		63 23 18	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	0.75
B <sub>n</sub>	0.75
OE <sub>A</sub>	0.75
OE <sub>B</sub>	0.75

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		17	27		34		41	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		24	40		50		60	ns	4.5	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>A</sub> to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		22	40		50		60	ns	4.5	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS

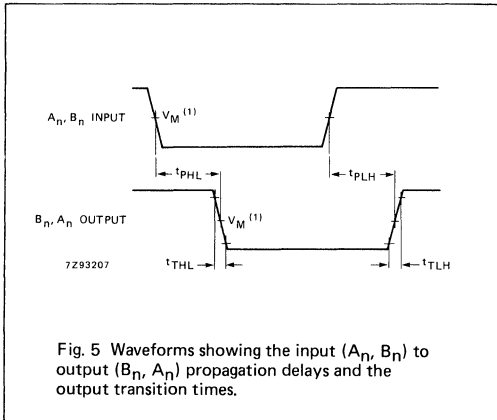


Fig. 5 Waveforms showing the input ( $A_n, B_n$ ) to output ( $B_n, A_n$ ) propagation delays and the output transition times.

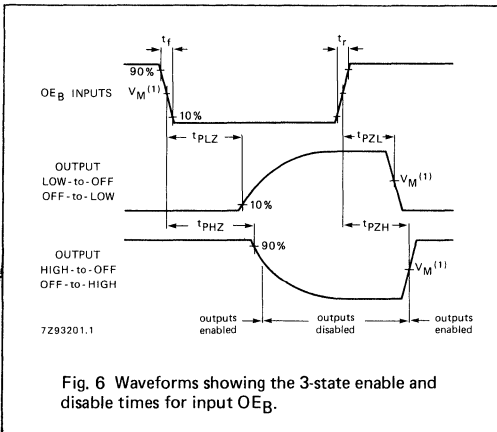


Fig. 6 Waveforms showing the 3-state enable and disable times for input  $OE_B$ .

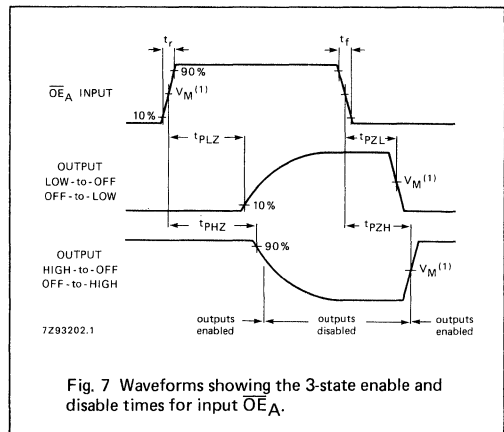


Fig. 7 Waveforms showing the 3-state enable and disable times for input  $OE_A$ .

OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT244 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT244 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state. The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA <sub>n</sub>	nY <sub>n</sub>
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT244P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT244T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1OE	output enable input (active LOW)
2, 4, 6, 8	1A <sub>0</sub> to 1A <sub>3</sub>	data inputs
3, 5, 7, 9	2Y <sub>0</sub> to 2Y <sub>3</sub>	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A <sub>0</sub> to 2A <sub>3</sub>	data inputs
18, 16, 14, 12	1Y <sub>0</sub> to 1Y <sub>3</sub>	bus outputs
19	2OE	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage

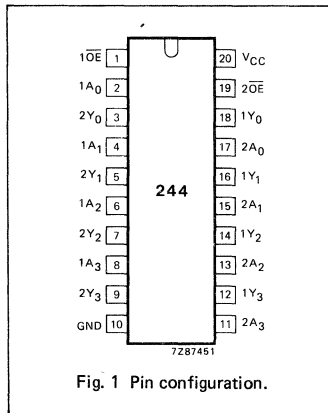


Fig. 1 Pin configuration.

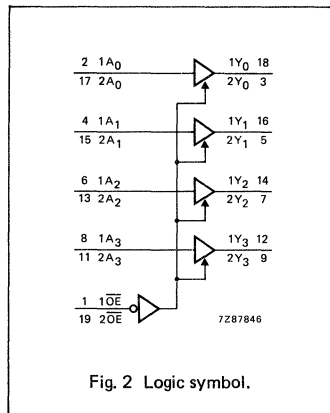


Fig. 2 Logic symbol.

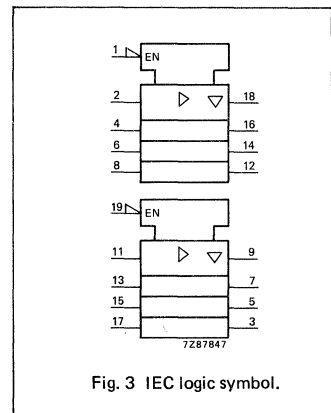
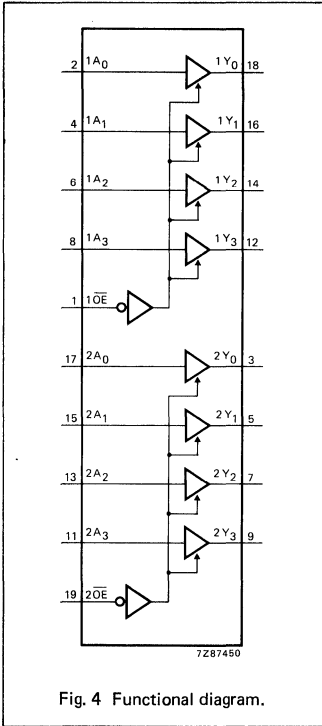


Fig. 3 IEC logic symbol.





**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		30 11 9	110 22 19		145 28 24		165 33 28	ns	2.0 4.5 6.0 Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		36 13 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0 Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0 Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0 Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

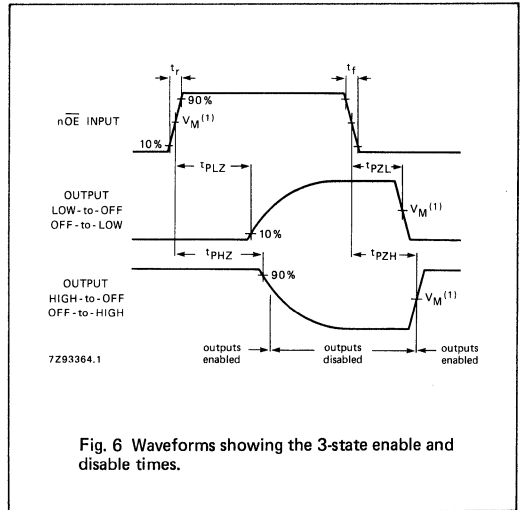
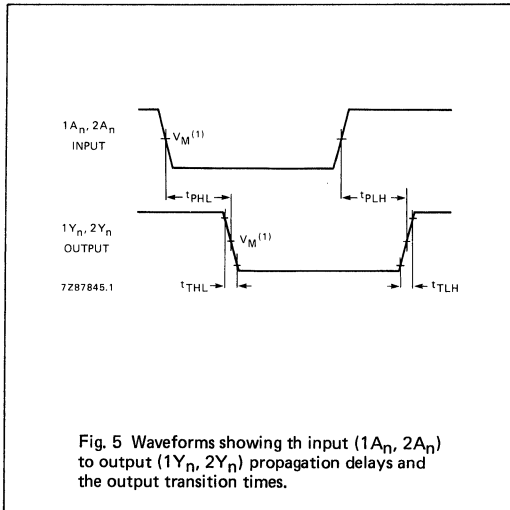
input	unit load coefficient
1A <sub>n</sub>	0.70
2A <sub>n</sub>	0.70
1OE	0.70
2OE	0.70

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		13	22		28		33	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		15	30		38		45	ns	4.5	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		15	25		31		38	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**OCTAL BUS TRANSCEIVER; 3-STATE**

**FEATURES**

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The "245" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated. The "245" is similar to the "640" but has true (non-inverting) outputs.

**FUNCTION TABLE**

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT245P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT245T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage

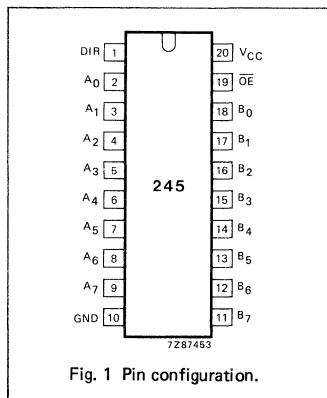


Fig. 1 Pin configuration.

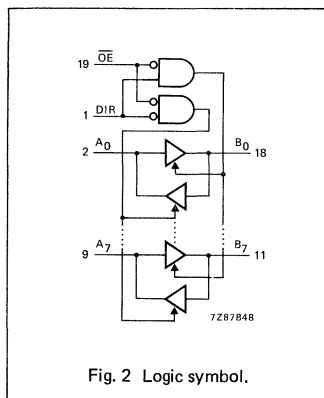


Fig. 2 Logic symbol.

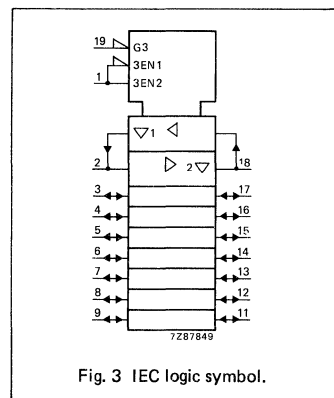


Fig. 3 IEC logic symbol.

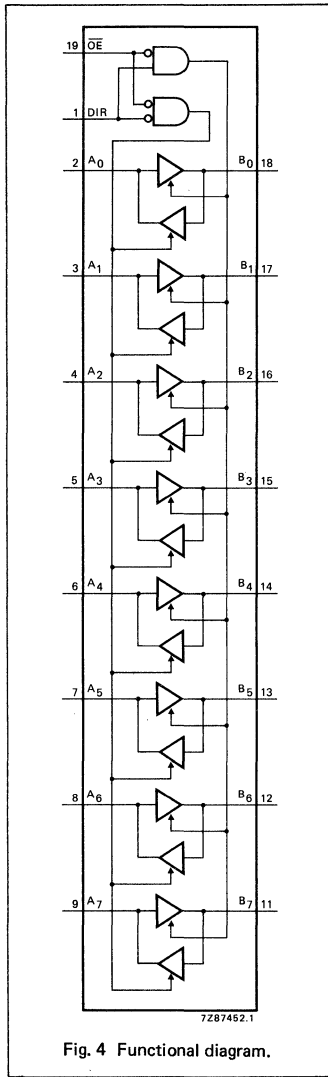


Fig. 4 Functional diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to A <sub>n</sub> ; $\overline{OE}$ to B <sub>n</sub>		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output enable time $\overline{OE}$ to A <sub>n</sub> ; $\overline{OE}$ to B <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

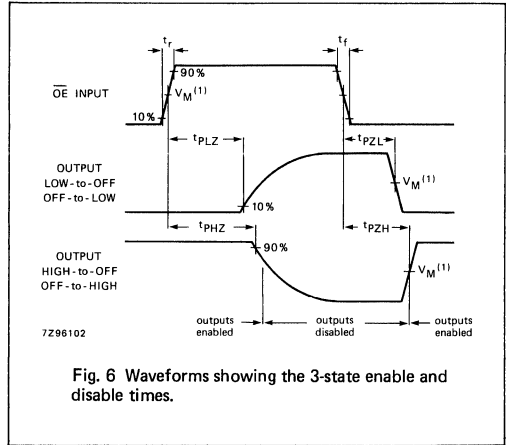
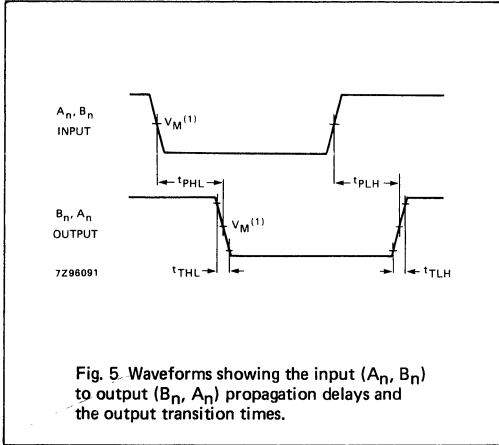
input	unit load coefficient
A <sub>n</sub>	0.40
B <sub>n</sub>	0.40
OE	1.50
DIR	0.90

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		12	23		29		35	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> ; OE to B <sub>n</sub>		16	30		38		45	ns	4.5	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output enable time OE to A <sub>n</sub> ; OE to B <sub>n</sub>		15	30		38		45	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



8-INPUT MULTIPLEXER; 3-STATE

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub>) controlling the switch positions.

Assertion (Y) and negation (Ȳ) outputs are both provided.

The output enable input (OE) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to Y I <sub>n</sub> to Ȳ S <sub>n</sub> to Y S <sub>n</sub> to Ȳ	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	18	ns
			14	18	ns
			24	24	ns
			24	24	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	40	42	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT251P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT251T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I <sub>0</sub> to I <sub>7</sub>	multiplexer inputs
5	Y	multiplexer output
6	Ȳ	complementary multiplexer output
7	OE	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	select inputs
16	V <sub>CC</sub>	positive supply voltage

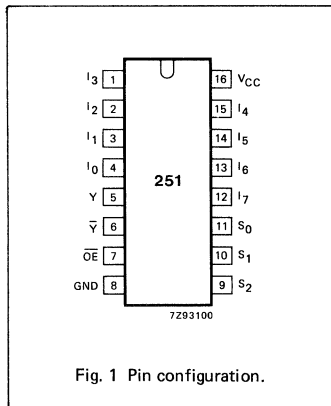


Fig. 1 Pin configuration.

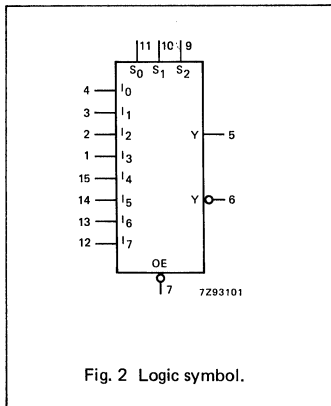


Fig. 2 Logic symbol.

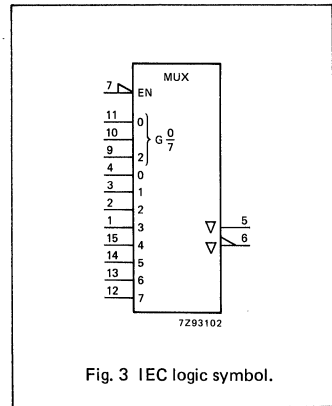


Fig. 3 IEC logic symbol.

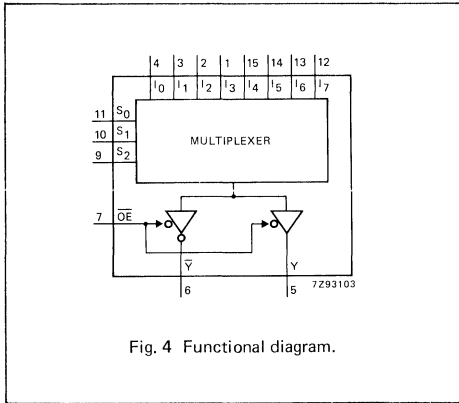


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS												OUTPUTS	
OE	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	Y-bar	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

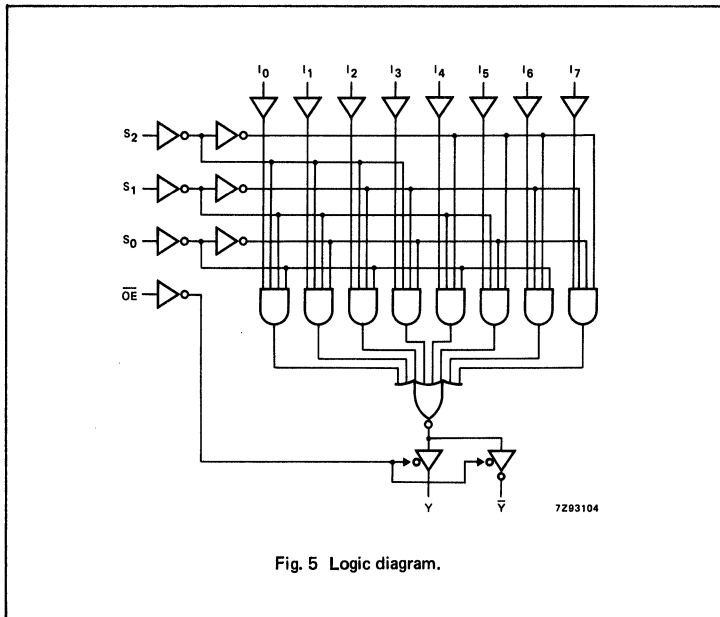


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/t_{PLH}$	propagation delay $I_n$ to Y		47 17 14	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $I_n$ to $\bar{Y}$		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay $S_n$ to Y		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $S_n$ to $\bar{Y}$		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 7
$t_{PZH}/t_{PZL}$	3-state output enable time $\bar{O}E$ to Y, $\bar{Y}$		33 12 10	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\bar{O}E$ to Y, $\bar{Y}$		36 13 10	140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
I <sub>n</sub>	0.55
S <sub>0</sub>	0.55
S <sub>1</sub> , S <sub>2</sub>	0.55
OE	2.65

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to Y		21	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to $\bar{Y}$		21	35		44		53	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to Y		28	48		60		72	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to $\bar{Y}$		28	48		60		72	ns	4.5	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Y, $\bar{Y}$		15	30		38		45	ns	4.5	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Y, $\bar{Y}$		14	28		35		42	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS

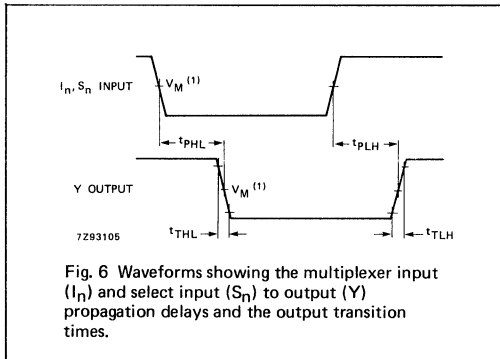


Fig. 6 Waveforms showing the multiplexer input ( $I_n$ ) and select input ( $S_n$ ) to output ( $Y$ ) propagation delays and the output transition times.

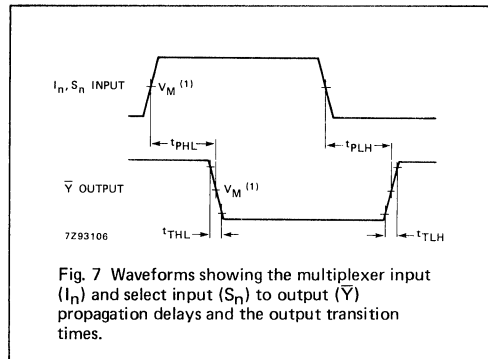


Fig. 7 Waveforms showing the multiplexer input ( $I_n$ ) and select input ( $S_n$ ) to output ( $\bar{Y}$ ) propagation delays and the output transition times.

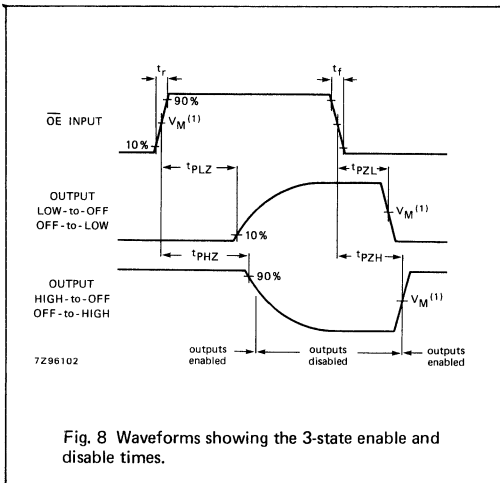


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DUAL 4-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253B are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT253B have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S<sub>0</sub>, S<sub>1</sub>).

When the individual output enable (1OE, 2OE) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state. The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S<sub>0</sub> and S<sub>1</sub>.

The logic equations for the outputs are:

$$1Y = 1\overline{OE}(1I_0\overline{S_1}\overline{S_0} + 1I_1\overline{S_1}S_0 + 1I_2S_1\overline{S_0} + 1I_3S_1S_0)$$

$$2Y = 2\overline{OE}(2I_0\overline{S_1}\overline{S_0} + 2I_1\overline{S_1}S_0 + 2I_2S_1\overline{S_0} + 2I_3S_1S_0)$$

APPLICATIONS

- Data selectors
- Data multiplexers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> , 2I <sub>n</sub> to nY; S <sub>n</sub> to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	17	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz

V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT253BP: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT253BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1OE, 2OE	output enable inputs (active LOW)
14, 2	S <sub>0</sub> , S <sub>1</sub>	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	1I <sub>0</sub> to 1I <sub>3</sub>	data inputs from source 1
10, 11, 12, 13	2I <sub>0</sub> to 2I <sub>3</sub>	data inputs from source 2
16	V <sub>CC</sub>	positive supply voltage

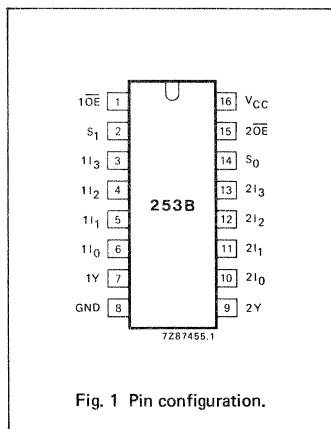


Fig. 1 Pin configuration.

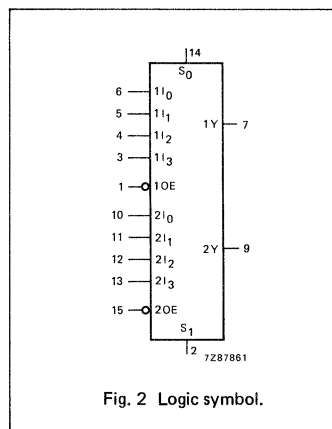


Fig. 2 Logic symbol.

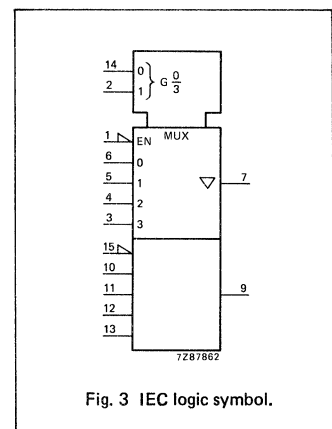
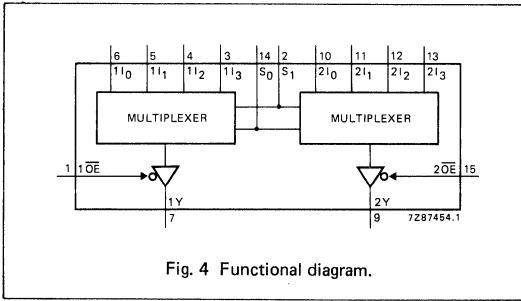


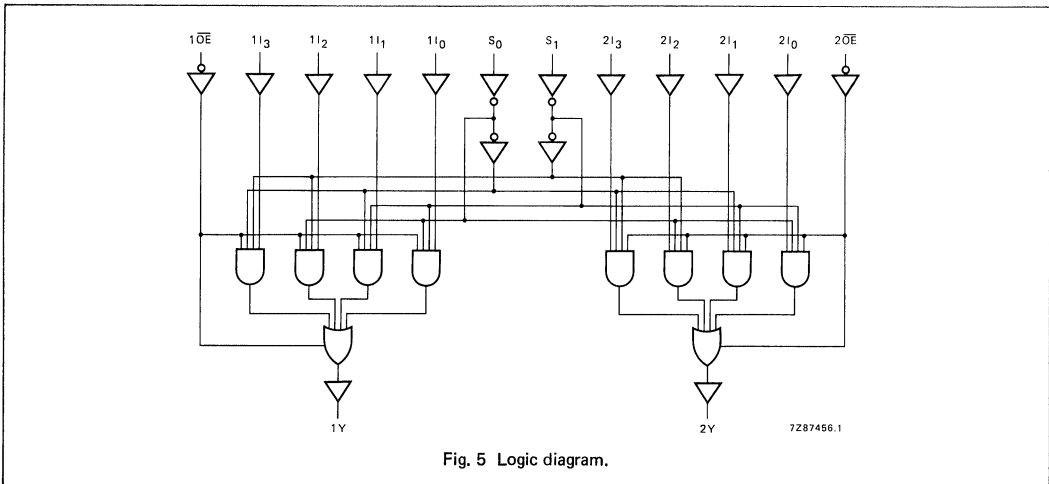
Fig. 3 IEC logic symbol.



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S <sub>0</sub>	S <sub>1</sub>	nI <sub>0</sub>	nI <sub>1</sub>	nI <sub>2</sub>	nI <sub>3</sub>	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state





**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

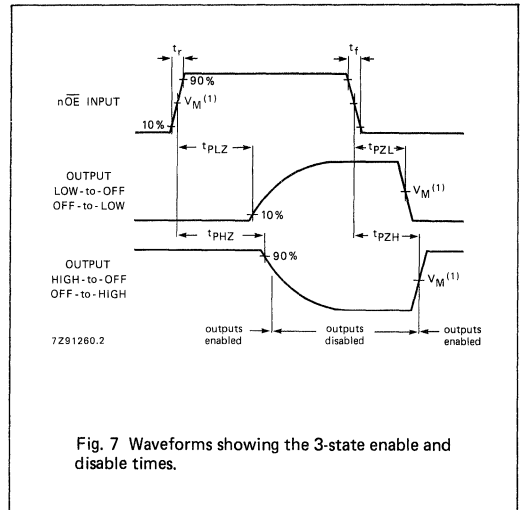
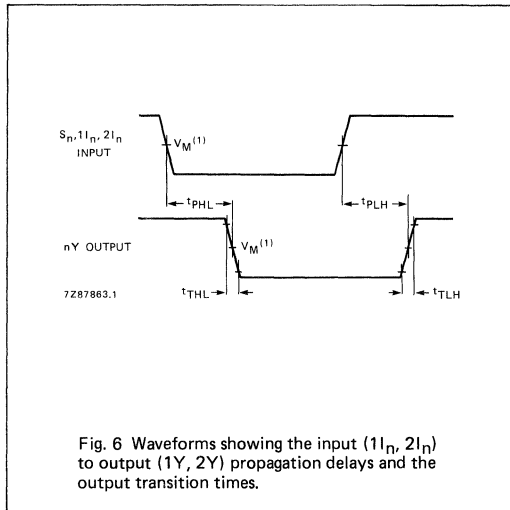
input	unit load coefficient
1I <sub>n</sub>	0.35
2I <sub>n</sub>	0.35
nOE	1.00
S <sub>0</sub>	1.00
S <sub>1</sub>	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		20	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		22	40		50		60	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		14	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		13	30		38		45	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 (1I<sub>0</sub> to 4I<sub>0</sub>) are selected when input S is LOW and the data inputs from source 1 (1I<sub>1</sub> to 4I<sub>1</sub>) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when  $\overline{OE}$  is HIGH.

The logic equations for the outputs are:

$$1Y = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \overline{S})$$

$$2Y = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \overline{S})$$

$$3Y = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \overline{S})$$

$$4Y = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \overline{S})$$

The "257" is identical to the "258" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> , nI <sub>1</sub> to nY S to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11 14	13 17	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	45	45	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT257P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT257T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	1I <sub>0</sub> to 4I <sub>0</sub>	data inputs from source 0
3, 6, 13, 10	1I <sub>1</sub> to 4I <sub>1</sub>	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

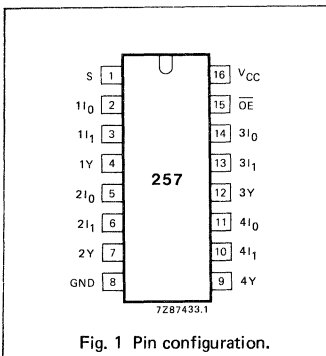


Fig. 1 Pin configuration.

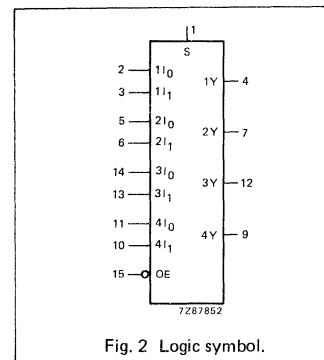


Fig. 2 Logic symbol.

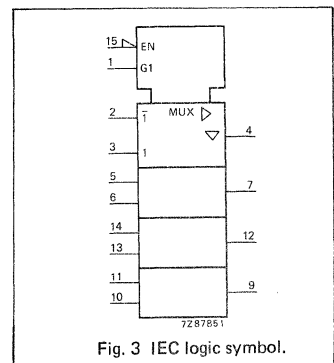
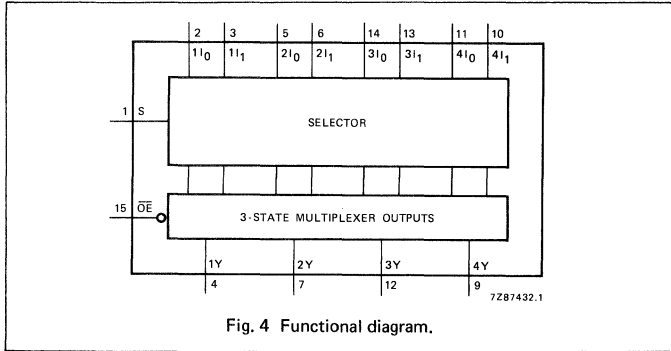


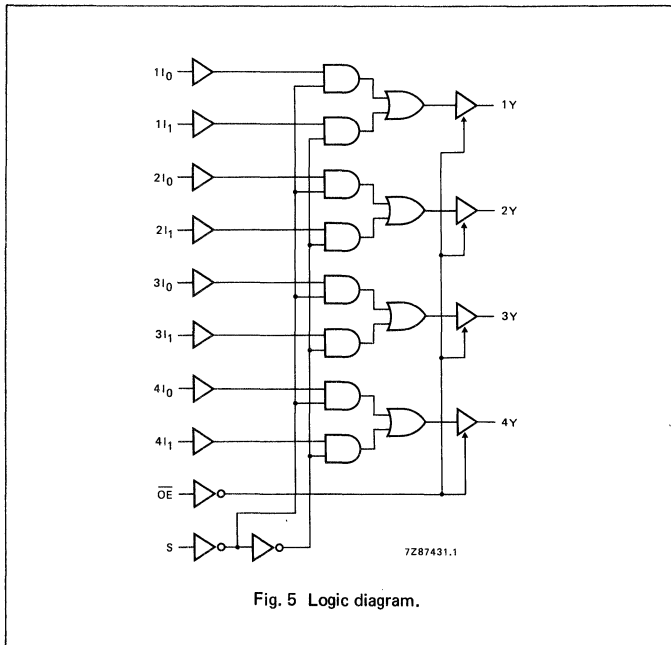
Fig. 3 IEC logic symbol.



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI <sub>0</sub>	nI <sub>1</sub>	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> to nY; nI <sub>1</sub> to nY	36 13 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY	47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to nY	33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to nY	41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

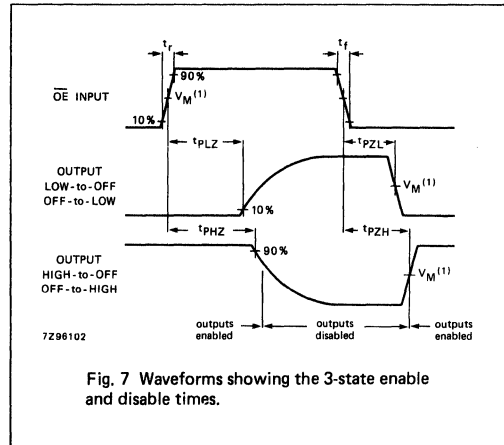
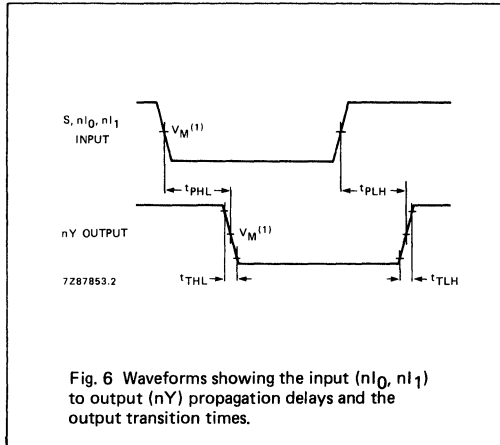
input	unit load coefficient
nI <sub>0</sub>	0.40
nI <sub>1</sub>	0.40
OE	1.35
S	0.65

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> to nY; nI <sub>1</sub> to nY		16	30		38		45	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S to nY		20	35		44		53	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to nY		15	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to nY		16	30		38		45	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



QUAD 2-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT258 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT258 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 (1I<sub>0</sub> to 4I<sub>0</sub>) are selected when input S is LOW and the data inputs from source 1 (1I<sub>1</sub> to 4I<sub>1</sub>) are selected when S is HIGH.

Data appears at the outputs (1Y to 4Y) in inverted form from the select inputs. The "258" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The outputs are forced to a high impedance OFF-state when OE is HIGH.

The logic equations for the outputs are:

$$1\bar{Y} = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \bar{S})$$

$$2\bar{Y} = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \bar{S})$$

$$3\bar{Y} = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \bar{S})$$

$$4\bar{Y} = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \bar{S})$$

The "258" is identical to the "257" but has inverting outputs.

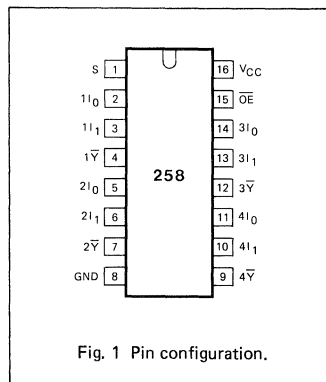


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nI <sub>0</sub> , nI <sub>1</sub> , S to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	16	ns
C <sub>i</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT258P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT258T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 14, 11	1I <sub>0</sub> to 4I <sub>0</sub>	data inputs from source 0
3, 6, 13, 10	1I <sub>1</sub> to 4I <sub>1</sub>	data inputs from source 1
4, 7, 12, 9	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	OE	3-state output enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

FUNCTION TABLE

OE	INPUTS			OUTPUT
	S	nI <sub>0</sub>	nI <sub>1</sub>	nY
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## 8-BIT ADDRESSABLE LATCH

### FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT259 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT259 are high-speed 8-bit addressable latches designed for general purpose storage applications in digital systems. The "259" are multifunctional devices capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q<sub>0</sub> to Q<sub>7</sub>), functions are available.

The "259" also incorporates an active LOW common reset ( $\overline{MR}$ ) for resetting all latches, as well as, an active LOW enable input (LE).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D to Q <sub>n</sub> A <sub>n</sub> , $\overline{LE}$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	18 17	20 20	ns ns
t <sub>PHL</sub>	$\overline{MR}$ to Q <sub>n</sub>		15	20	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V

Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

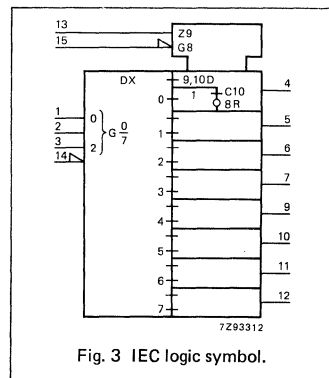
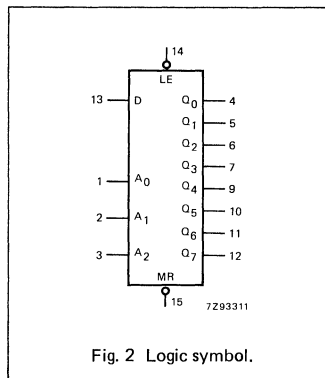
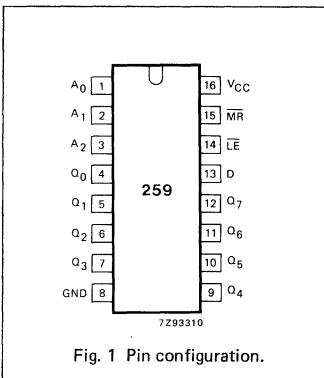
### ORDERING INFORMATION/PACKAGE OUTLINES

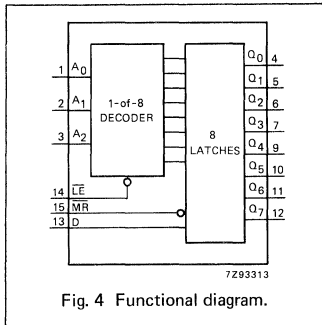
PC74HC/HCT259P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT259T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A <sub>0</sub> to A <sub>2</sub>	address inputs
4, 5, 6, 7, 9 10, 11, 12	Q <sub>0</sub> to Q <sub>7</sub>	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V <sub>CC</sub>	positive supply voltage





MODE SELECT TABLE

LE	MR	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	MR	LE	D	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
store (do nothing)	L	L	d	L	H	L	L	L	L	L	Q=d	L	L	L
	L	L	d	H	H	L	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
addressable latch	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	L	L	Q=d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	L	q <sub>0</sub>	Q=d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q=d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q=d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q=d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q=d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q=d	q <sub>6</sub>	q <sub>7</sub>

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition  
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

GENERAL DESCRIPTION (Cont'd.)

The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A<sub>0</sub> to A<sub>2</sub>) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

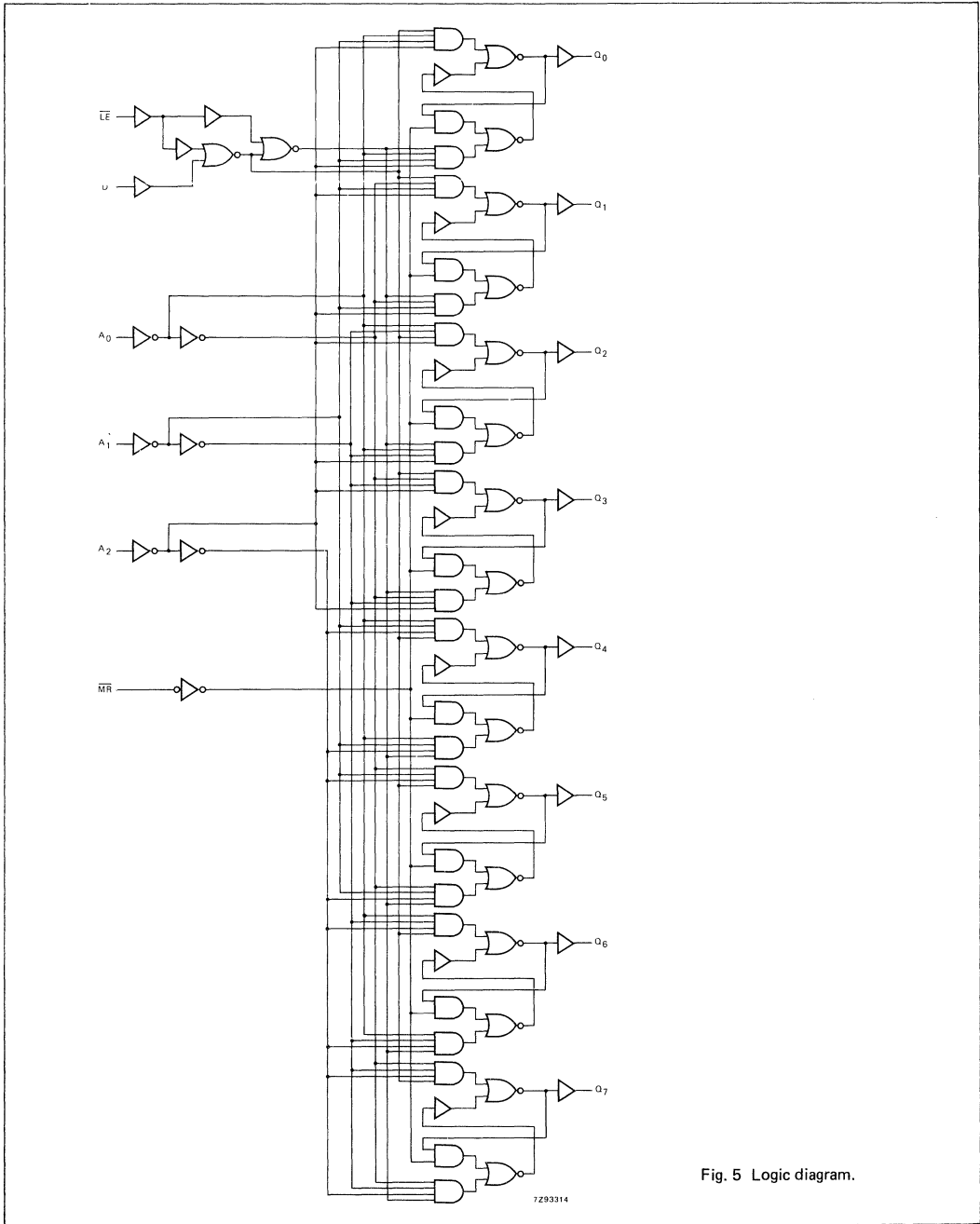


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay D to $Q_n$		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $Q_n$		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
$t_{PHL}/t_{PLH}$	propagation delay $\overline{LE}$ to $Q_n$		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}$	propagation delay $\overline{MR}$ to $Q_n$		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 9
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		119 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
$t_W$	$\overline{LE}$ pulse width HIGH or LOW	70 14 12	17 6 5		90 18 15		105 21 12		ns	2.0 4.5 6.0	Fig. 6
$t_W$	$\overline{MR}$ pulse width LOW	70 14 12	17 6 5		90 18 15		105 21 12		ns	2.0 4.5 6.0	Fig. 9
$t_{su}$	set-up time D, $A_n$ to $\overline{LE}$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
$t_h$	hold time D to $\overline{LE}$	0 0 0	-19 -6 -5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 10
$t_h$	hold time $A_n$ to $\overline{LE}$	2 2 2	-11 -4 -3		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 11

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
A <sub>n</sub>	1.50
LE	1.50
D	1.20
MR	0.75

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D to Q <sub>n</sub>		23	39		49		59	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		25	42		53		63	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		23	39		49		59	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t <sub>W</sub>	LE pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig. 6
t <sub>W</sub>	MR pulse width LOW	18	10		23		27		ns	4.5	Fig. 9
t <sub>su</sub>	set-up time D to LE	17	10		21		26		ns	4.5	Fig. 10
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	17	10		21		26		ns	4.5	Fig. 11
t <sub>h</sub>	hold time D to LE	0	-8		0		0		ns	4.5	Fig. 10
t <sub>h</sub>	hold time A <sub>n</sub> to LE	0	-5		0		0		ns	4.5	Fig. 11

AC WAVEFORMS

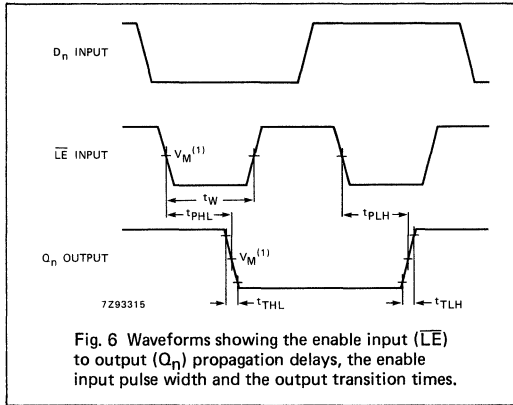


Fig. 6 Waveforms showing the enable input ( $\overline{LE}$ ) to output ( $Q_n$ ) propagation delays, the enable input pulse width and the output transition times.

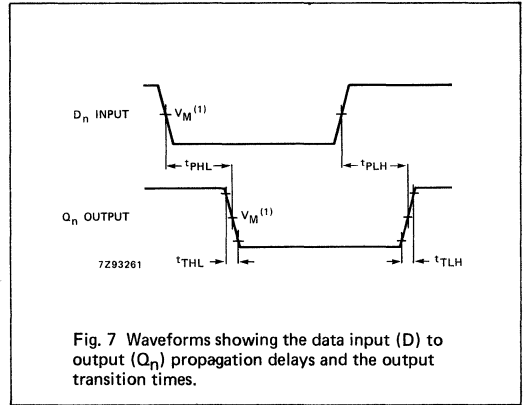


Fig. 7 Waveforms showing the data input ( $D$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

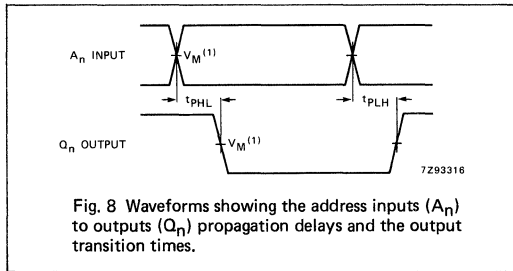


Fig. 8 Waveforms showing the address inputs ( $A_n$ ) to outputs ( $Q_n$ ) propagation delays and the output transition times.

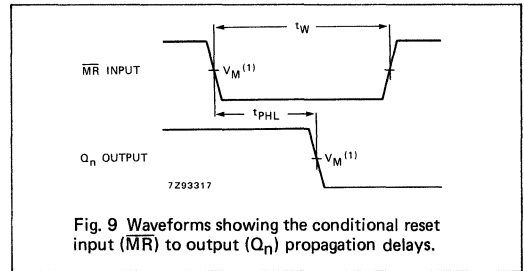


Fig. 9 Waveforms showing the conditional reset input ( $\overline{MR}$ ) to output ( $Q_n$ ) propagation delays.

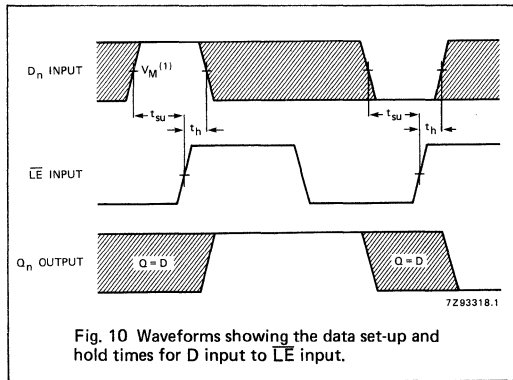


Fig. 10 Waveforms showing the data set-up and hold times for  $D$  input to  $\overline{LE}$  input.

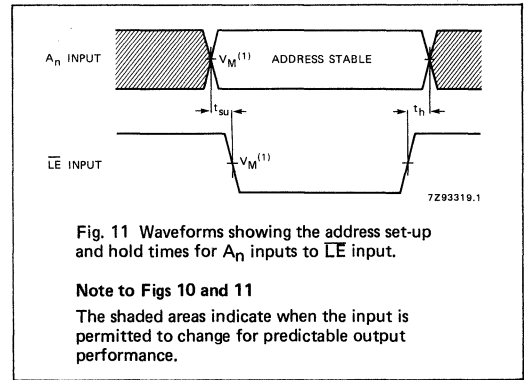


Fig. 11 Waveforms showing the address set-up and hold times for  $A_n$  inputs to  $\overline{LE}$  input.

Note to Figs 10 and 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND to } 3V$ .

**QUAD 2-INPUT EXCLUSIVE-NOR GATE**

**FEATURES**

- Output capability: standard
- I<sub>CC</sub> category: SSI

**GENERAL DESCRIPTION**

The 74HC7266 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC7266 provide the EXCLUSIVE-NOR function with active push-pull output.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	11	ns
C <sub>I</sub>	input capacitance		3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	note 1	17	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC7266P: 14-lead DIL; plastic (SOT-27).  
 PC74HC7266T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 8, 12	1A to 4A	data inputs
2, 6, 9, 13	1B to 4B	data inputs
3, 4, 10, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

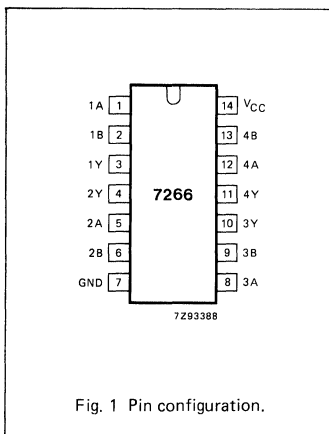


Fig. 1 Pin configuration.

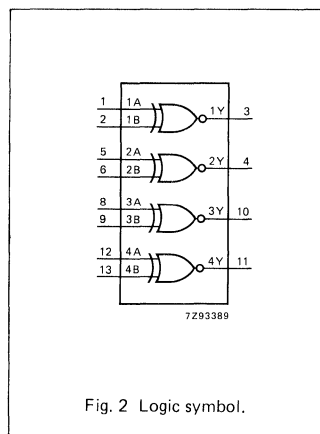


Fig. 2 Logic symbol.

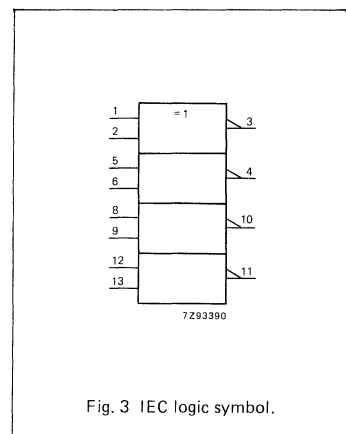


Fig. 3 IEC logic symbol.



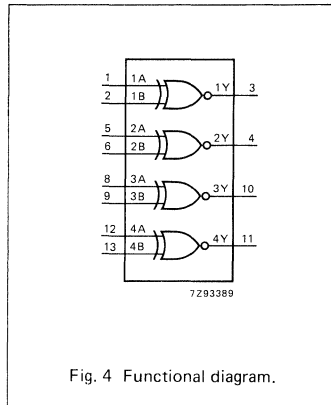


Fig. 4 Functional diagram.

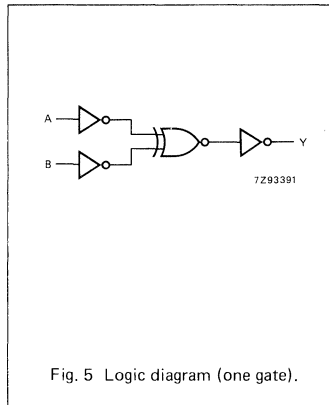


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level  
L = LOW voltage level

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

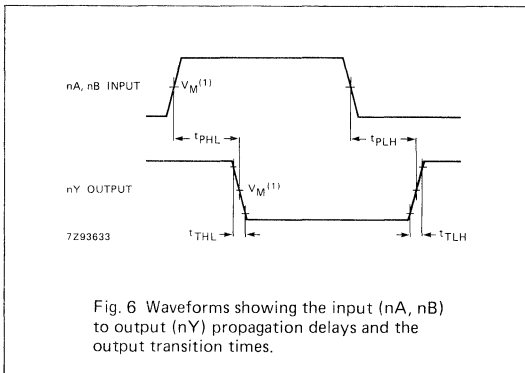
I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB to nY		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**AC WAVEFORMS**



**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.

OCTAL D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See "377" for clock enable version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability; standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q<sub>n</sub>) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the  $\overline{MR}$  input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> $\overline{MR}$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15 15	15 20	ns ns
f <sub>max</sub>	maximum clock frequency		66	36	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

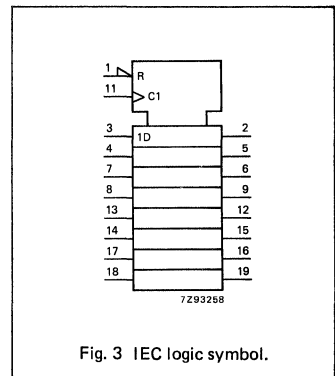
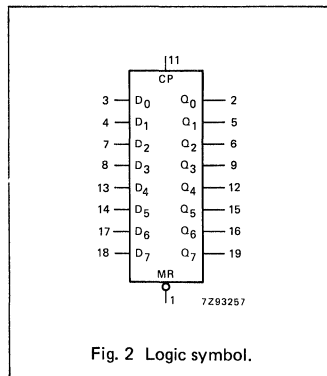
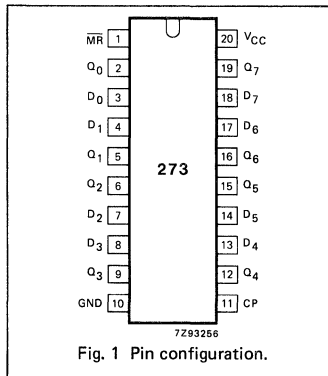
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT273P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT273T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q <sub>0</sub> to Q <sub>7</sub>	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V <sub>CC</sub>	positive supply voltage



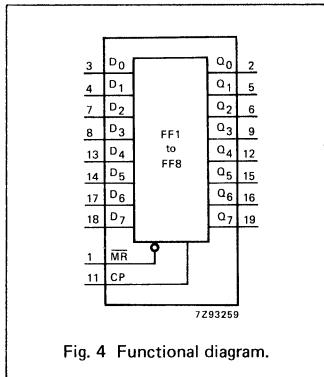


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	$D_n$	$Q_n$
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 ↑ = LOW-to-HIGH transition  
 X = don't care

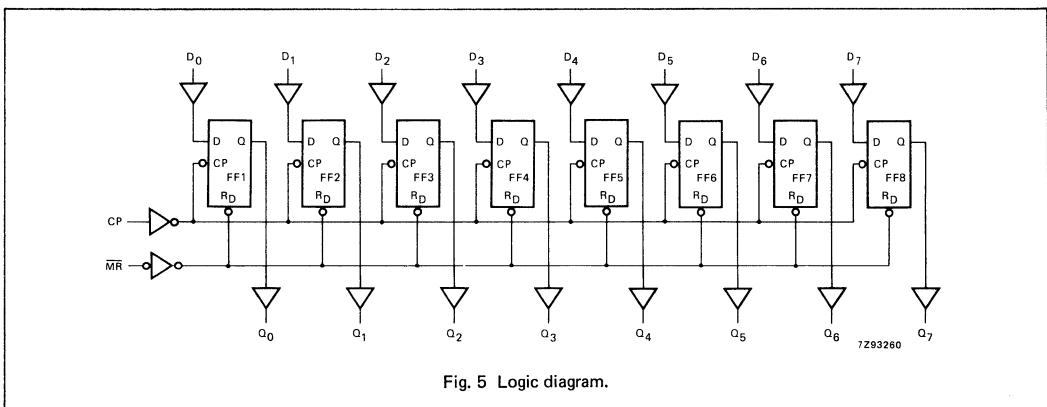


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay $\overline{MR}$ to $Q_n$		50 18 14	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
$t_W$	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
$t_W$	master reset pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_{rem}$	removal time $\overline{MR}$ to CP	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
$t_{su}$	set-up time $D_n$ to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
$t_h$	hold time CP to $D_n$	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
$f_{max}$	maximum clock pulse frequency	6 30 35	20 60 71		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$\overline{MR}$	1.00
CP	1.75
$D_n$	0.15

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	18	35		44		53	ns	4.5	Fig. 6	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{MR}$ to $Q_n$	23	39		49		59	ns	4.5	Fig. 7	
$t_{THL}/t_{TLH}$	output transition time	7	15		19		22	ns	4.5	Fig. 6	
$t_W$	clock pulse width HIGH or LOW	26	15		33		39	ns	4.5	Fig. 6	
$t_W$	master reset pulse width LOW	17	10		21		26	ns	4.5	Fig. 7	
$t_{rem}$	removal time $\overline{MR}$ to CP	15	4		19		22	ns	4.5	Fig. 7	
$t_{su}$	set-up time $D_n$ to CP	16	9		20		24	ns	4.5	Fig. 8	
$t_h$	hold time CP to $D_n$	3	-3		3		3	ns	4.5	Fig. 8	
$f_{max}$	maximum clock pulse frequency	19	33		15		13	MHz	4.5	Fig. 6	

AC WAVEFORMS

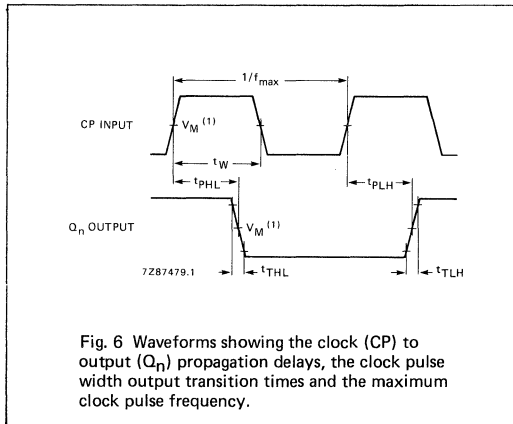


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

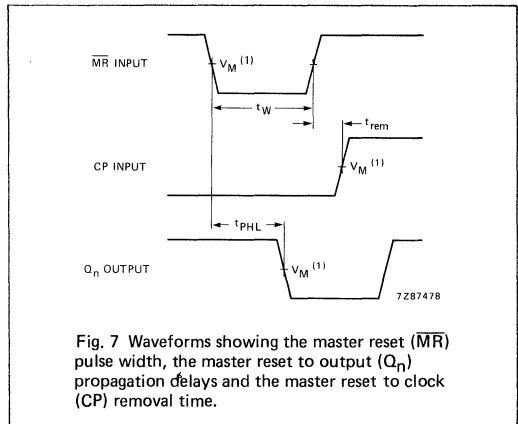


Fig. 7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.

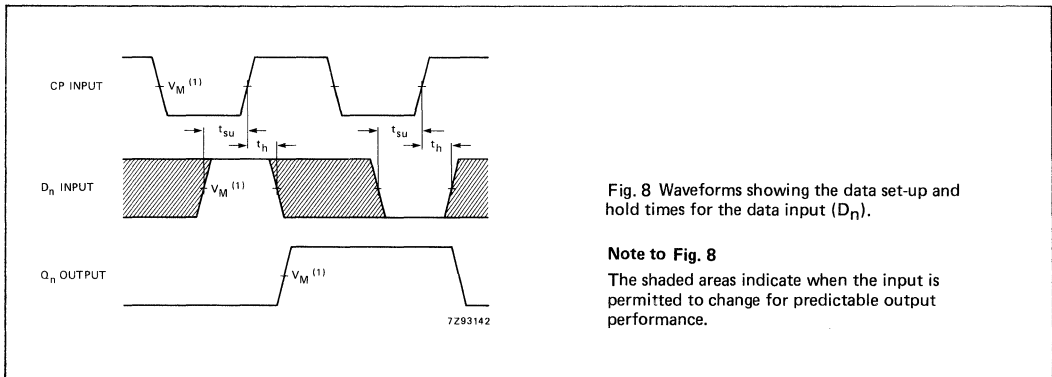


Fig. 8 Waveforms showing the data set-up and hold times for the data input ( $D_n$ ).

**Note to Fig. 8**  
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Note to AC waveforms**

- (1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .
- HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

## 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

### FEATURES

- Word-length easily expanded by cascading
- Similar pin configuration to the "180" for easy system up-grading
- Generates either odd or even parity for nine data bits
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT280 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT280 are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits.

The even parity output ( $\Sigma_E$ ) is HIGH when an even number of data inputs ( $I_0$  to  $I_8$ ) are HIGH. The odd parity output ( $\Sigma_O$ ) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the even outputs ( $\Sigma_E$ ) of up to nine parallel devices to the data inputs of the final stage.

### APPLICATIONS

- 25-line parity generator/checker
- 81-line parity generator/checker

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $I_n$ to $\Sigma_E$ $I_n$ to $\Sigma_O$	$C_L = 15$ pF $V_{CC} = 5$ V	17 20	18 22	ns ns
$C_i$	input capacitance		3.5	3.5	pF
$C_{pD}$	power dissipation capacitance per package	notes 1 and 2	65	65	pF

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns

### Notes

1.  $C_{pD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = C_{pD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$$f_i = \text{input frequency in MHz} \quad C_L = \text{output load capacitance in pF}$$

$$f_o = \text{output frequency in MHz} \quad V_{CC} = \text{supply voltage in V}$$

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5$  V

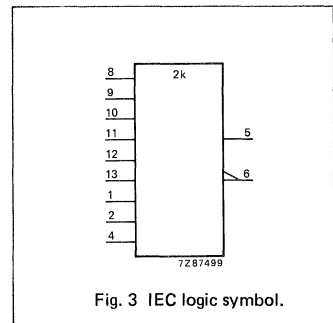
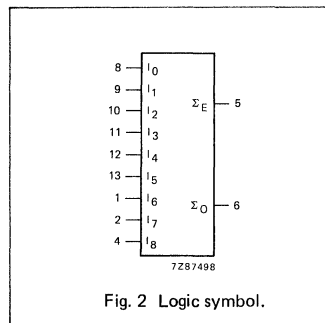
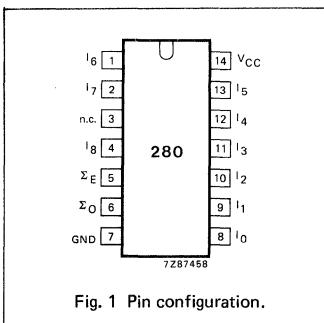
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT280P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT280T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 9, 10, 11, 12, 13, 1, 2, 4	$I_0$ to $I_8$	data inputs
5, 6	$\Sigma_E, \Sigma_O$	parity outputs
7	GND	ground (0 V)
14	$V_{CC}$	positive supply voltage





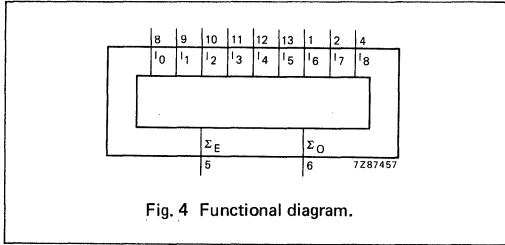


Fig. 4 Functional diagram.

**FUNCTION TABLE**

INPUTS	OUTPUTS	
number of HIGH data inputs (I <sub>0</sub> to I <sub>7</sub> )	Σ <sub>E</sub>	Σ <sub>O</sub>
even	H	L
odd	L	H

H = HIGH voltage level  
L = LOW voltage level

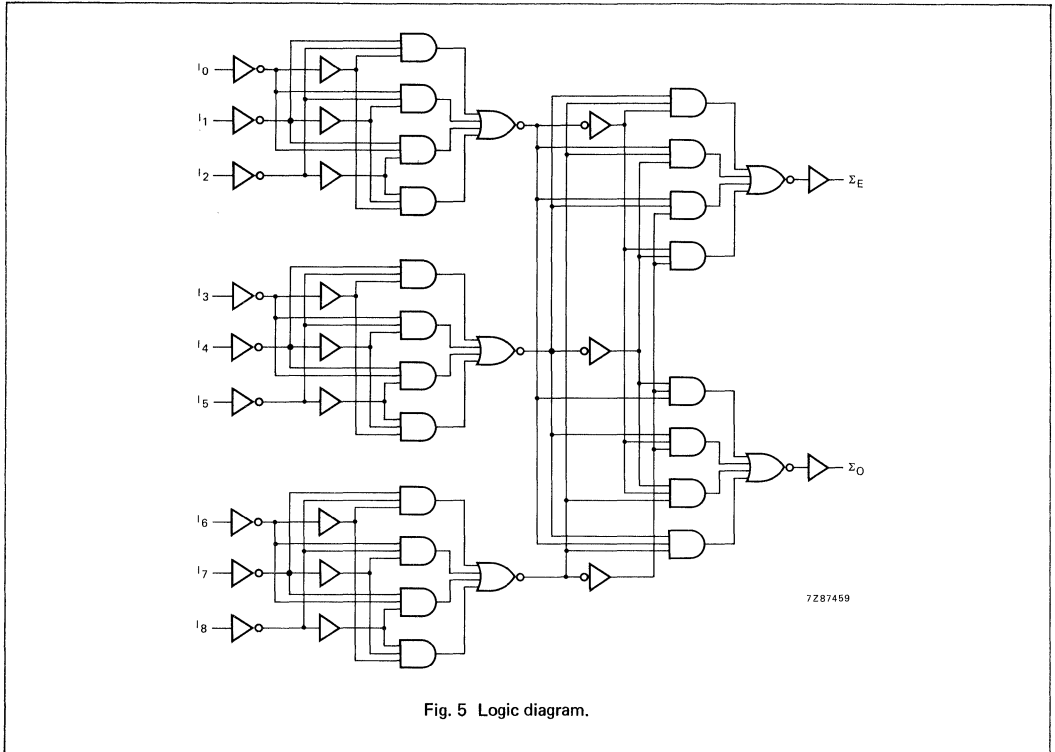


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to $\Sigma$ E		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to $\Sigma$ O		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

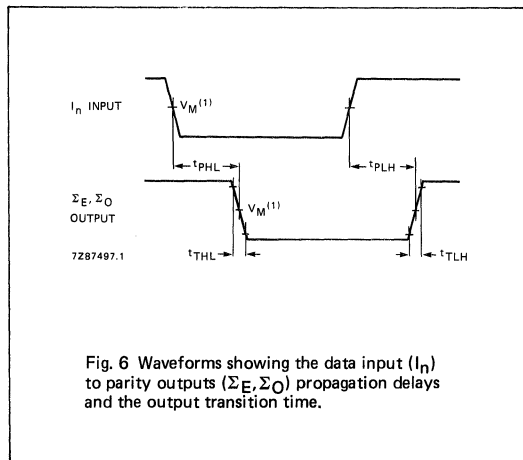
input	unit load coefficient
I <sub>n</sub>	1.0

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to ΣE		21	42		53		63	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>n</sub> to ΣO		26	45		56		68	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

**AC WAVEFORMS**



**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

4-BIT FULL ADDER WITH FAST CARRY

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT283 add two 4-bit binary words (A<sub>n</sub> plus B<sub>n</sub>) plus the incoming carry. The binary sum appears on the sum outputs (Σ<sub>1</sub> to Σ<sub>4</sub>) and the out-going carry (C<sub>OUT</sub>) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the "283" can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ<sub>1</sub> to Σ<sub>4</sub> and C<sub>OUT</sub> should be interpreted also as active LOW. With active HIGH inputs, C<sub>IN</sub> must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C<sub>IN</sub>, A<sub>1</sub>, B<sub>1</sub> can be assigned arbitrarily to pins 5, 6, 7, etc.

See the "583" for the BCD version.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>1</sub> C <sub>IN</sub> to Σ <sub>2</sub> C <sub>IN</sub> to Σ <sub>3</sub> C <sub>IN</sub> to Σ <sub>4</sub> A <sub>n</sub> or B <sub>n</sub> to Σ <sub>n</sub> C <sub>IN</sub> to C <sub>OUT</sub> A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	16 18 20 23 21 20 20	15 21 23 27 25 23 24	ns ns ns ns ns ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	88	92	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT283P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT283T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ <sub>1</sub> to Σ <sub>4</sub>	sum outputs
5, 3, 14, 12	A <sub>1</sub> to A <sub>4</sub>	A operand inputs
6, 2, 15, 11	B <sub>1</sub> to B <sub>4</sub>	B operand inputs
7	C <sub>IN</sub>	carry input
8	GND	ground (0 V)
9	C <sub>OUT</sub>	carry output
16	V <sub>CC</sub>	positive supply voltage

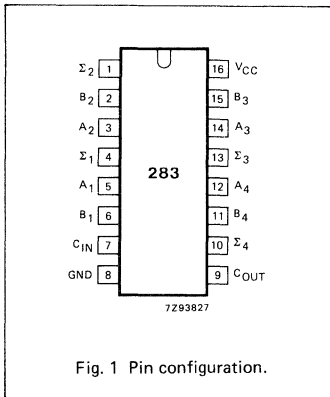


Fig. 1 Pin configuration.

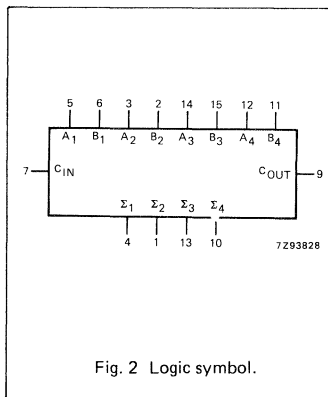


Fig. 2 Logic symbol.

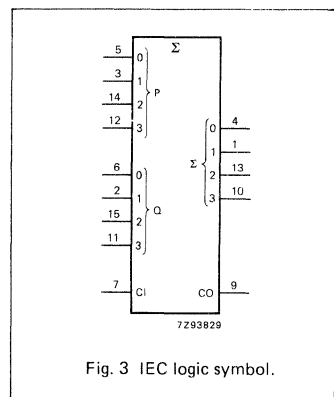


Fig. 3 IEC logic symbol.

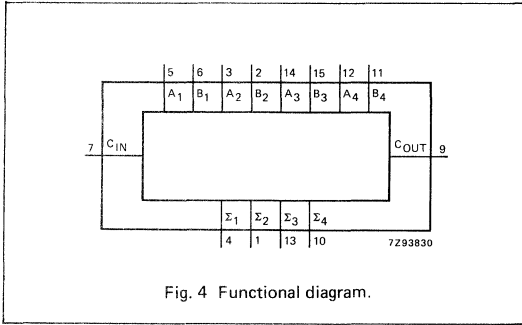


Fig. 4 Functional diagram.

**FUNCTION TABLE**

PINS	C <sub>IN</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	Σ <sub>1</sub>	Σ <sub>2</sub>	Σ <sub>3</sub>	Σ <sub>4</sub>	C <sub>OUT</sub>	EXAMPLE
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(a)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(b)

H = HIGH voltage level  
L = LOW voltage level

Example    1001  
             1010  
                       
             10011  
(a) for active HIGH,  
example = (9 + 10 = 19)  
(b) for active LOW,  
example = (carry + 6 + 5 = 12)

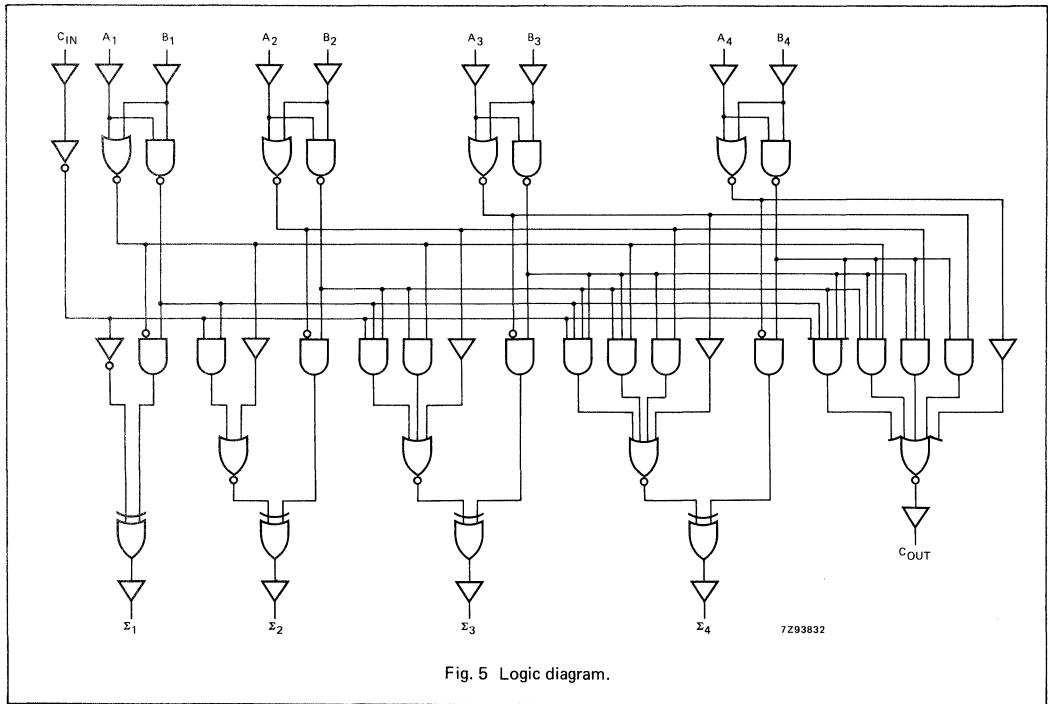


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>1</sub>		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>2</sub>		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>3</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to Σ <sub>4</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to Σ <sub>n</sub>		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to C <sub>OUT</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 16	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

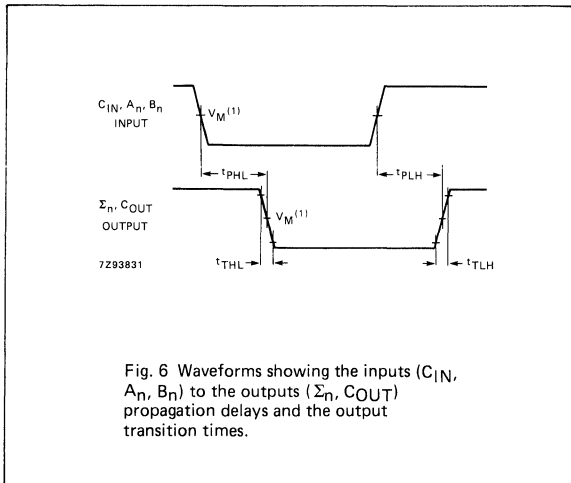
INPUT	UNIT LOAD COEFFICIENT
C <sub>IN</sub>	1.50
B <sub>2</sub> , A <sub>2</sub> , A <sub>1</sub>	1.00
B <sub>1</sub>	0.40
B <sub>4</sub> , A <sub>4</sub> , A <sub>3</sub> , B <sub>3</sub>	0.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_1$		18	31		39		47	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_2$		25	43		54		65	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_3$		27	46		58		69	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to $\Sigma_4$		31	53		66		80	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to $\Sigma_n$		29	49		61		74	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>IN</sub> to C <sub>OUT</sub>		27	46		58		69	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> or B <sub>n</sub> to C <sub>OUT</sub>		28	48		60		72	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

## AC WAVEFORMS



## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





## DIGITAL PHASE-LOCKED-LOOP FILTER

## FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency range:  
DC to 55 MHz typical (K-clock)  
DC to 35 MHz typical (I/D-clock)
- Dynamically variable bandwidth
- Very narrow bandwidth attainable
- Power-on reset
- Output capability:  
standard/bus driver
- I<sup>2</sup>C category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay I/D <sub>CP</sub> to I/D <sub>OUT</sub> $\phi A_1$ , $\phi B$ to XORPD <sub>OUT</sub> $\phi B$ , $\phi A_2$ to ECPD <sub>OUT</sub>	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15 13 19	18 13 19	ns
$f_{max}$	maximum clock frequency $K_{CP}$ I/D <sub>CP</sub>		63 41	68 40	MHz
$C_I$	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

## Notes

1. CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$$f_i = \text{input frequency in MHz} \quad C_L = \text{output load capacitance in pF}$$

$$f_o = \text{output frequency in MHz} \quad V_{CC} = \text{supply voltage in V}$$

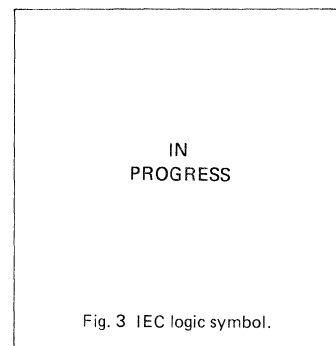
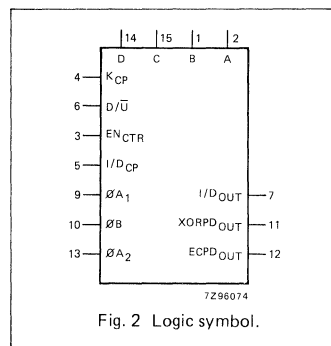
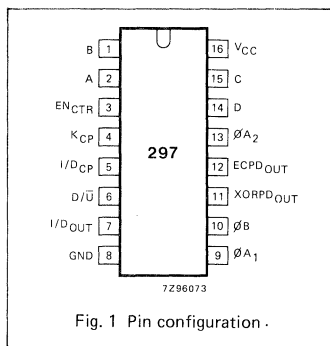
$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

## ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT297P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT297T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).



**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1, 15, 14	A, B, C, D	modulo control inputs
3	ENCTR	K-counter enable input
4	KCP	K-counter clock input (LOW-to-HIGH, edge-triggered)
5	I/D <sub>CP</sub>	increment/decrement clock input (HIGH-to-LOW, edge-triggered)
6	D/Ū	down/up control
7	I/D <sub>OUT</sub>	increment/decrement bus output
8	GND	ground (0 V)
9, 10, 13	φA <sub>1</sub> , φB, φA <sub>2</sub>	phase inputs
11	XORPD <sub>OUT</sub>	EXCLUSIVE-OR phase detector output
12	ECPD <sub>OUT</sub>	edge-controlled phase detector output
16	V <sub>CC</sub>	positive supply voltage

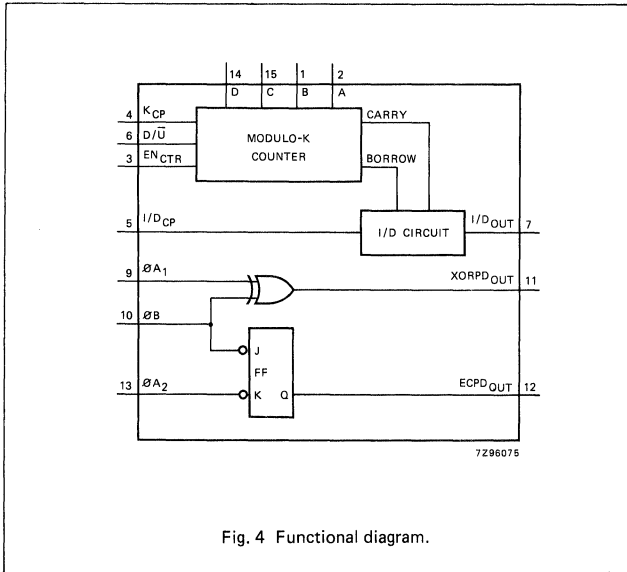


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth

or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V<sub>CC</sub> and temperature variations but depends solely on

**K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE**

D	C	B	A	MODULO (K)
L	L	L	L	inhibited
L	L	L	H	2 <sup>3</sup>
L	L	H	L	2 <sup>4</sup>
L	L	H	H	2 <sup>5</sup>
L	H	L	L	2 <sup>6</sup>
L	H	L	H	2 <sup>7</sup>
L	H	H	L	2 <sup>8</sup>
L	H	H	H	2 <sup>9</sup>
H	L	L	L	2 <sup>10</sup>
H	L	L	H	2 <sup>11</sup>
H	L	H	L	2 <sup>12</sup>
H	L	H	H	2 <sup>13</sup>
H	H	L	L	2 <sup>14</sup>
H	H	L	H	2 <sup>15</sup>
H	H	H	L	2 <sup>16</sup>
H	H	H	H	2 <sup>17</sup>

**EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE**

φA <sub>1</sub>	φB	XORPD <sub>OUT</sub>
L	L	L
L	H	H
H	L	H
H	H	L

**EDGE-CONTROLLED PHASE DETECTOR TABLE**

φA <sub>2</sub>	φB	ECPD <sub>OUT</sub>
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level  
L = LOW voltage level  
↓ = HIGH-to-LOW transition  
↑ = LOW-to-HIGH transition

accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error (φ<sub>IN</sub> - φ<sub>OUT</sub>). Within these limits the phase detector output varies linearly with the input phase

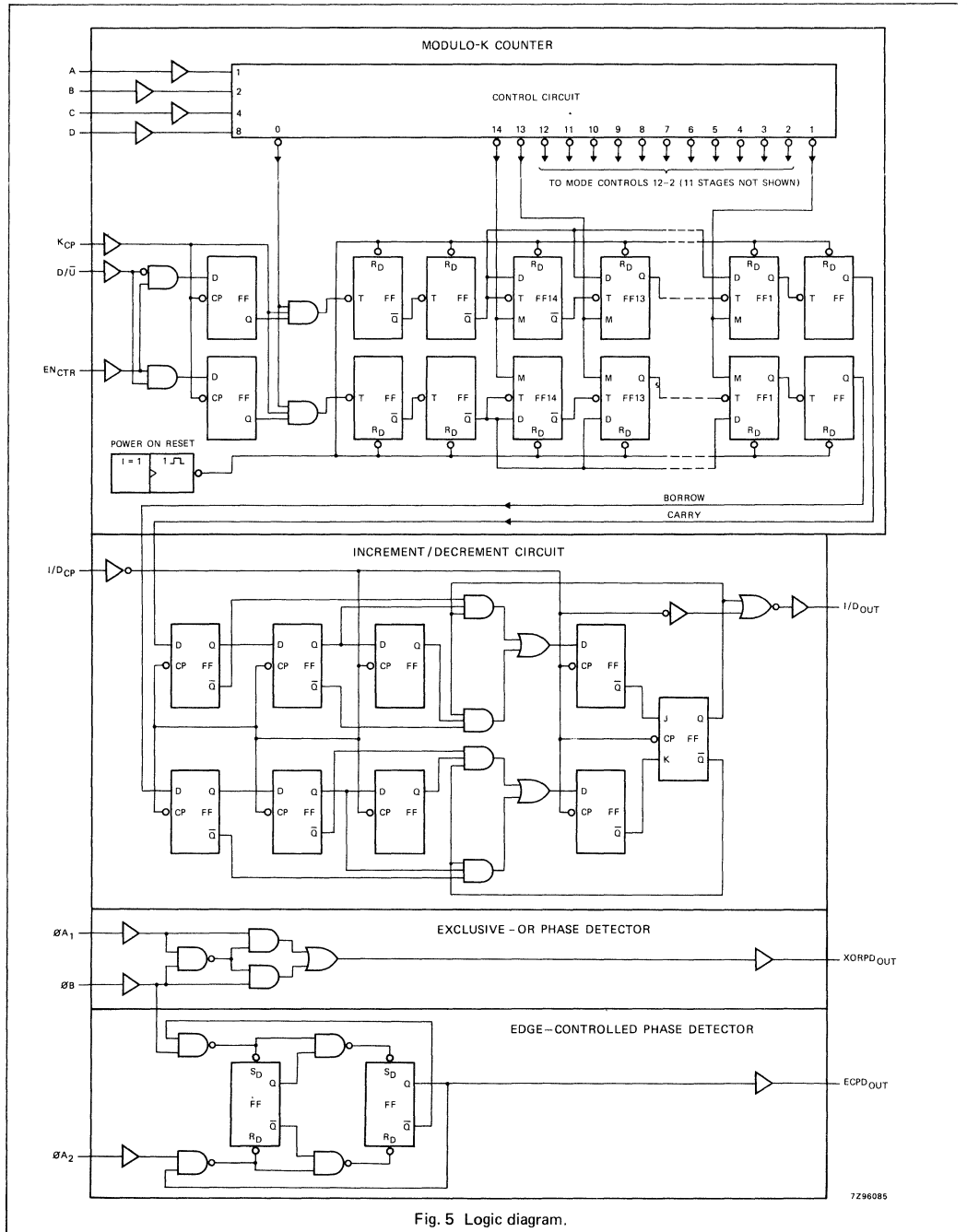


Fig. 5 Logic diagram.

**GENERAL DESCRIPTION (Cont'd)**

error according to the gain  $k_d$ , which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between  $\pm 1$  according to the relation:

$$\text{phase detector output} = \frac{\% \text{ HIGH} - \% \text{ LOW}}{100}$$

The output of the phase detector will be  $k_d\phi_e$ , where the phase error  $\phi_e = \phi_{IN} - \phi_{OUT}$ .

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex

than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain ( $k_d$ ) for an XORPD is 4 because its output remains HIGH (XORPD<sub>OUT</sub> = 1) for a phase error of 1/4 cycle.

Similarly,  $k_d$  for the ECPD is 2 since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a  $\phi_e$  defined to be zero. For the basic DPLL system of Fig. 6  $\phi_e = 0$  when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD,  $\phi_e = 0$  when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency  $Mf_c$ , which is a multiple M of the loop centre frequency  $f_c$ . When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio  $Mf_c/K$ , the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is  $(k_d\phi_e Mf_c)/K$ .

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is 1/2 of the input clock (I/D<sub>CP</sub>). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D<sub>OUT</sub>. Thus the output of the I/D circuit will be  $Nf_c + (k_d\phi_e Mf_c)/2K$ .

The output of the N-counter (or the output of the phase-locked-loop) is thus:  $f_c = f_c + (k_d\phi_e Mf_c)/2KN$ .

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just  $Mf_c/2KN$  or  $f_c/K$  for  $M = 2N$ .

Thus the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

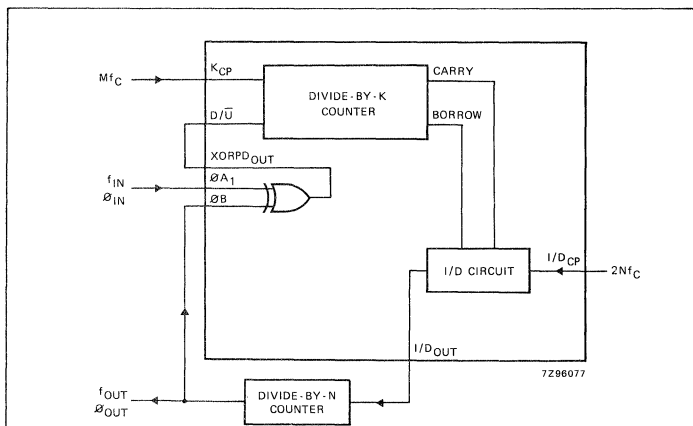


Fig. 6 DPLL using EXCLUSIVE-OR phase detection.

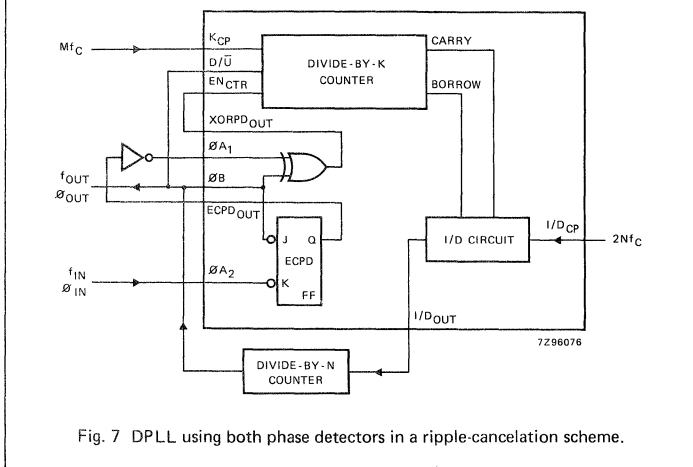
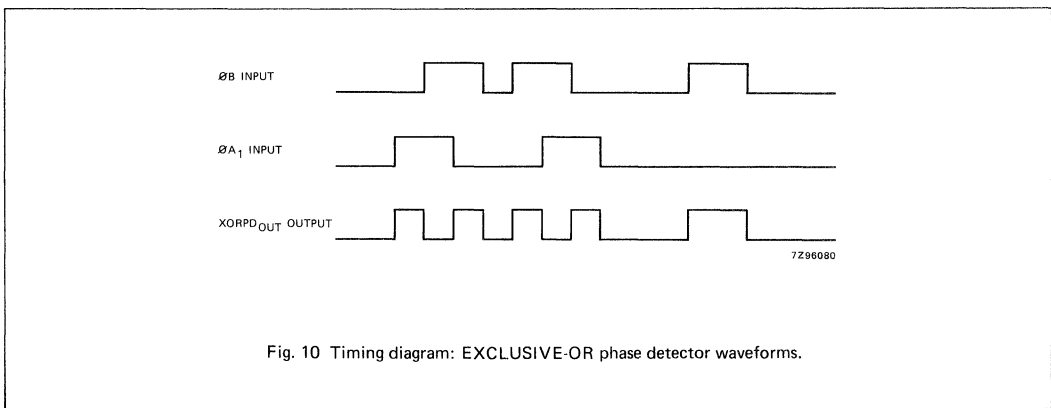
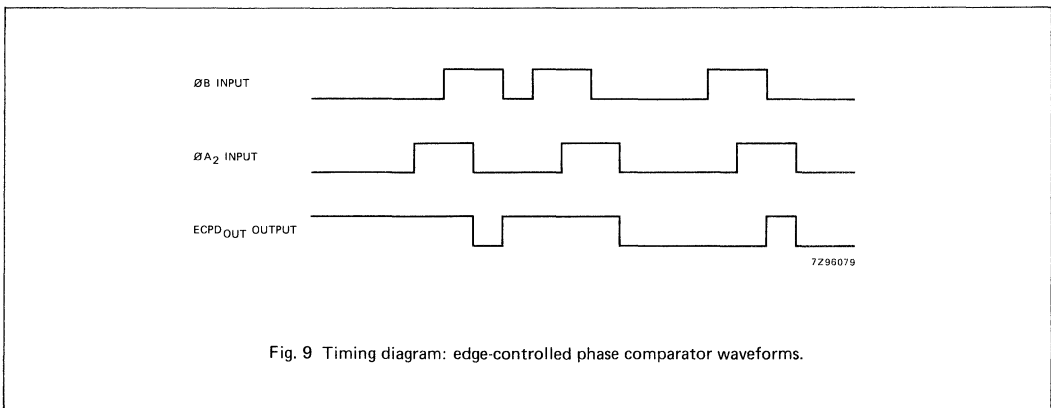
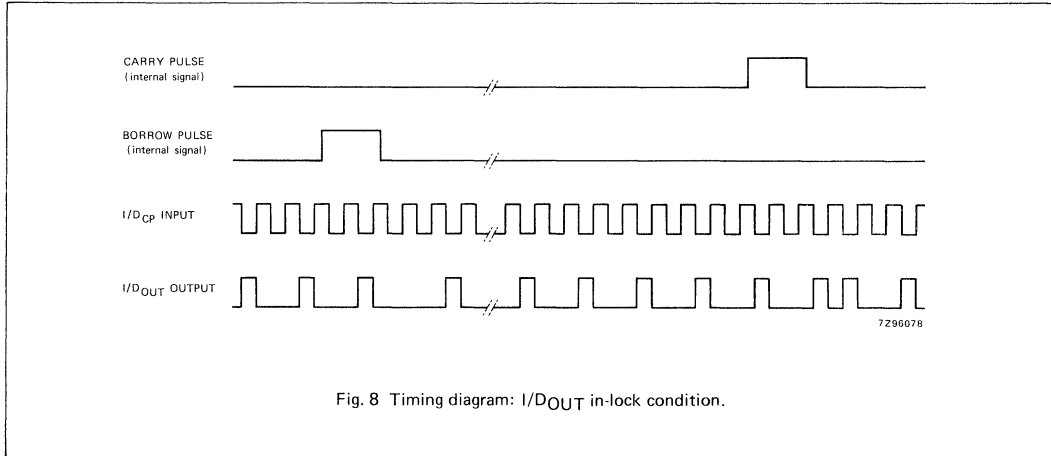


Fig. 7 DPLL using both phase detectors in a ripple-cancellation scheme.



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I/D <sub>CP</sub> to I/D <sub>OUT</sub>		50 18 14	175 35 30		220 44 34		265 53 43	ns	2.0 4.5 6.0	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay φA <sub>1</sub> , φB to XORP <sub>OUT</sub>		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 12
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay φB, φA <sub>2</sub> to ECP <sub>OUT</sub>		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time: bus driver output; I/D <sub>OUT</sub> (pin 7)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 11
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time: standard outputs; XORP <sub>OUT</sub> , ECP <sub>OUT</sub> (pins 11, 12)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12 and 13
t <sub>W</sub>	clock pulse width K <sub>CP</sub>	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14
t <sub>W</sub>	clock pulse width I/D <sub>CP</sub>	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time D/U, EN <sub>CTR</sub> to K <sub>CP</sub>	120 24 20	33 12 10		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 14
t <sub>h</sub>	hold time D/U, EN <sub>CTR</sub> to K <sub>CP</sub>	0 0 0	-19 -7 -6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 14
f <sub>max</sub>	maximum clock pulse frequency K <sub>CP</sub>	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 14
f <sub>max</sub>	maximum clock pulse frequency I/D <sub>CP</sub>	4.0 20 24	12 37 44		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 11

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
EN <sub>CTR</sub> , D/ $\bar{U}$	0.3
A, B, C, D, K <sub>CP</sub> , $\phi A_2$	0.6
I/D <sub>CP</sub> , $\phi A_1$ , $\phi B$	1.5

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V, t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I/D <sub>CP</sub> to I/D <sub>OUT</sub>		21	35		44		53	ns	4.5	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\phi A_1$ , $\phi B$ to XORPD <sub>OUT</sub>		16	32		40		48	ns	4.5	Fig. 12
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\phi B$ , $\phi A_2$ to ECPD <sub>OUT</sub>		22	44		55		66	ns	4.5	Fig. 13
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver output I/D <sub>OUT</sub> (pin 7)		5	12		15		18	ns	4.5	Fig. 11
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard outputs XORPD <sub>OUT</sub> , ECPD <sub>OUT</sub> (pins 11, 12)		7	15		95		110	ns	4.5	Figs 12 and 13
t <sub>W</sub>	clock pulse width K <sub>CP</sub>	16	8		20		24		ns	4.5	Fig. 14
t <sub>W</sub>	clock pulse width I/D <sub>CP</sub>	25	13		31		38		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time D/ $\bar{U}$ , EN <sub>CTR</sub> to K <sub>CP</sub>	24	13		31		38		ns	4.5	Fig. 14
t <sub>h</sub>	hold time D/ $\bar{U}$ , EN <sub>CTR</sub> to K <sub>CP</sub>	0	-8		0		0		ns	4.5	Fig. 14
f <sub>max</sub>	maximum clock pulse frequency K <sub>CP</sub>	30	62		38		45		MHz	4.5	Fig. 14
f <sub>max</sub>	maximum clock pulse frequency I/D <sub>CP</sub>	20	36		16		13		MHz	4.5	Fig. 11



AC WAVEFORMS

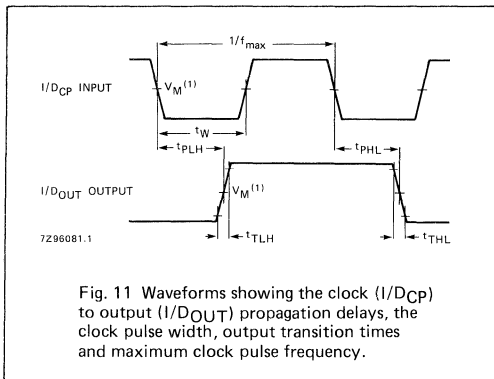


Fig. 11 Waveforms showing the clock (I/D<sub>CP</sub>) to output (I/D<sub>OUT</sub>) propagation delays, the clock pulse width, output transition times and maximum clock pulse frequency.

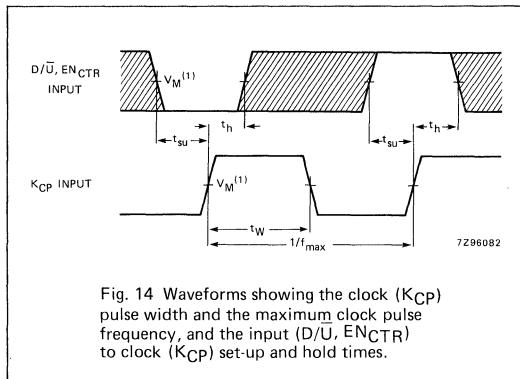


Fig. 14 Waveforms showing the clock (K<sub>CP</sub>) pulse width and the maximum clock pulse frequency, and the input (D/U\_ENCTR) to clock (K<sub>CP</sub>) set-up and hold times.

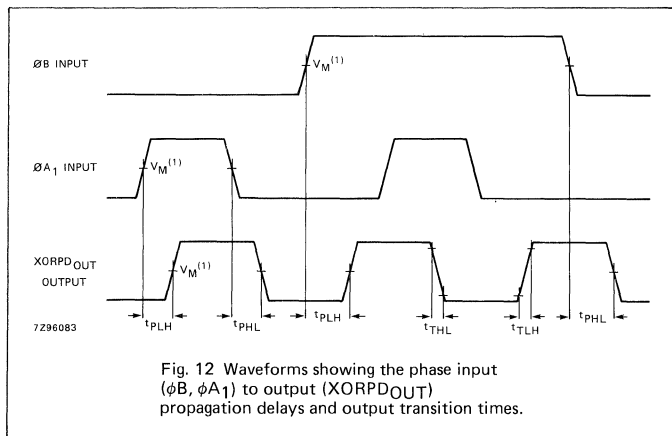


Fig. 12 Waveforms showing the phase input (φB, φA<sub>1</sub>) to output (XORPD<sub>OUT</sub>) propagation delays and output transition times.

Note to Fig. 14

The shaded areas indicate when the input is permitted to change for predictable output performance.

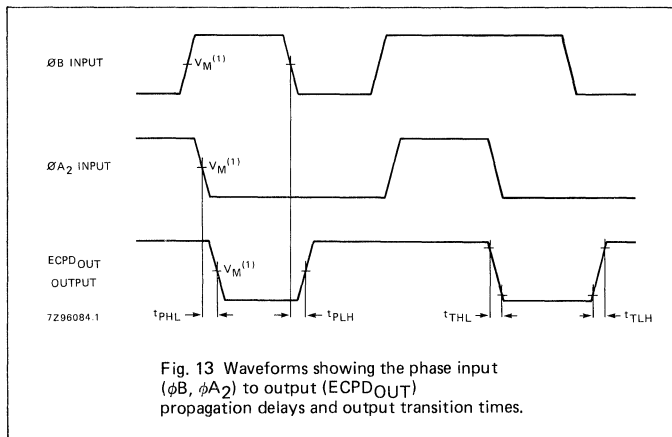


Fig. 13 Waveforms showing the phase input (φB, φA<sub>2</sub>) to output (ECPD<sub>OUT</sub>) propagation delays and output transition times.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

8-BIT UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes: shift left, shift right, hold (store), load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os), standard (serial outputs)
- I<sub>CC</sub> category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> , Q <sub>7</sub> CP to I/O <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	20	18	ns
			20	18	ns
t <sub>PHL</sub>	$\overline{MR}$ to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		21	21	ns
f <sub>max</sub>	maximum clock frequency		43	43	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	170	170	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S<sub>0</sub> and S<sub>1</sub>), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O<sub>0</sub> to I/O<sub>7</sub>) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q<sub>0</sub> and Q<sub>7</sub>) are used for expansion in serial shifting of longer words.

(continued on next page)

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT299P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT299T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION See next page

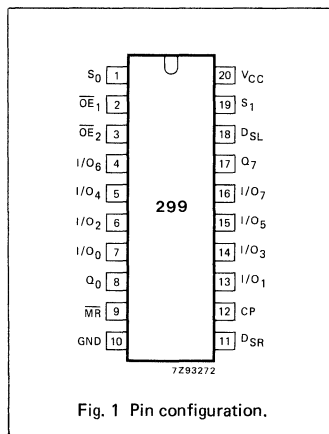


Fig. 1 Pin configuration.

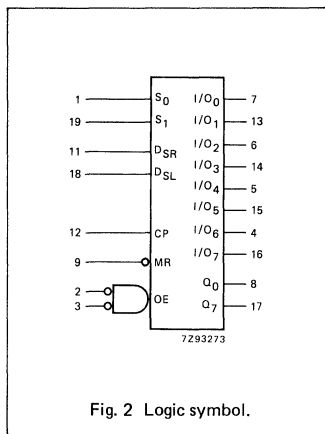


Fig. 2 Logic symbol.

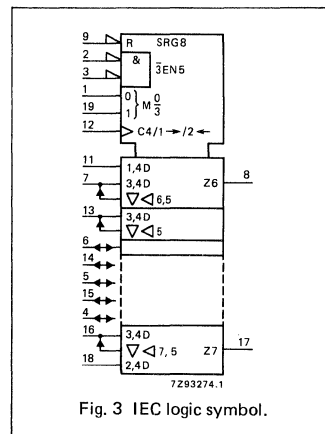


Fig. 3 IEC logic symbol.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S <sub>0</sub> , S <sub>1</sub>	mode select inputs
2, 3	$\overline{OE}_1, \overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O <sub>0</sub> to I/O <sub>7</sub>	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q <sub>0</sub> , Q <sub>7</sub>	serial outputs (standard output)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D <sub>SR</sub>	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D <sub>SL</sub>	serial data shift-left input
20	V <sub>CC</sub>	positive supply voltage

**GENERAL DESCRIPTION (Cont'd.)**

A LOW signal on the asynchronous master reset input ( $\overline{MR}$ ) overrides the S<sub>n</sub> and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ( $\overline{OE}_1$  or  $\overline{OE}_2$ ) disables the 3-state buffers and the I/O<sub>n</sub> outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub>, when in preparation for a parallel load operation.

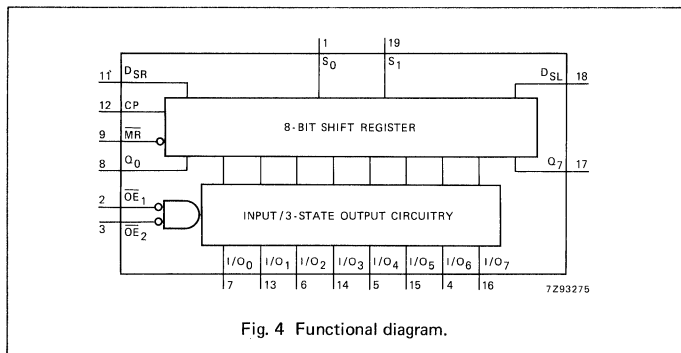


Fig. 4 Functional diagram.

**MODE SELECT TABLE**

INPUTS				RESPONSE
$\overline{MR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	asynchronous reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↑	parallel load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↑	shift right; D <sub>SR</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> etc.
H	H	L	↑	shift left; D <sub>SL</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> etc.
H	L	L	X	hold

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH CP transition



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os)  
standard (serial outputs)

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> , Q <sub>7</sub>		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to I/O <sub>n</sub>		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>n</sub> to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>n</sub> to Q <sub>0</sub> , Q <sub>7</sub> or I/O <sub>n</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time bus driver (I/O <sub>n</sub> )		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time standard (Q <sub>0</sub> , Q <sub>7</sub> )		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	clock pulse width HIGH or LOW	115 23 20	22 8 6		145 29 25		175 35 30		ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	master reset pulse width LOW	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
t <sub>rem</sub>	removal time MR to CP	75 15 13	19 7 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time I/O <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	135 27 23	44 16 13		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	150 30 26	50 18 14		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 8

## AC CHARACTERISTICS FOR 74HC (continued)

GND = 0 V;  $t_r = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_h$	hold time $I/O_n$ , $D_{SR}$ , $D_{SL}$ to CP	0	-30		0		0		ns	2.0 4.5 6.0	Fig. 6
$t_h$	hold time $S_0$ , $S_1$ to CP	0	-33		0		0		ns	2.0 4.5 6.0	Fig. 8
$f_{max}$	maximum clock pulse frequency	4	13		4		3		MHz	2.0 4.5 6.0	Fig. 6
		22	39		18		15				
		26	46		21		18				

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver (parallel I/Os)  
standard (serial outputs) $I_{CC}$  category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$I/O_n$	0.20
$D_{SR}$ , $D_{SL}$	0.20
CP, $S_0$	0.60
$\overline{MR}$ , $S_1$	0.20
$\overline{OE}_n$	0.30

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_0, Q_7$		20	35		44		53	ns	4.5	Fig. 6
$t_{PHL}/t_{PLH}$	propagation delay CP to $I/O_n$		20	43		54		65	ns	4.5	Fig. 6
$t_{PHL}$	propagation delay MR to $Q_0, Q_7$ or $I/O_n$		25	46		58		69	ns	4.5	Fig. 7
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}_n$ to $Q_0, Q_7$ or $I/O_n$		20	37		46		56	ns	4.5	Fig. 9
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}_n$ to $Q_0, Q_7$ or $I/O_n$		22	37		46		56	ns	4.5	Fig. 9
$t_{THL}/t_{TLH}$	output transition time bus driver ( $I/O_n$ )		5	12		15		18	ns	4.5	Fig. 6
$t_{THL}/t_{TLH}$	output transition time standard ( $Q_0, Q_7$ )		7	15		19		22	ns	4.5	Fig. 6
$t_W$	clock pulse width HIGH or LOW	25	13		33		39		ns	4.5	Fig. 6
$t_W$	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig. 7
$t_{rem}$	removal time MR to CP	10	2		9		11		ns	4.5	Fig. 7
$t_{su}$	set-up time $I/O_n, D_{SR}, D_{SL}$ to CP	25	14		31		38		ns	4.5	Fig. 6
$t_{su}$	set-up time $S_0, S_1$ to CP	32	19		40		48		ns	4.5	Fig. 8
$t_h$	hold time $I/O_n, D_{SR}, D_{SL}$ to CP	0	-12		0		0		ns	4.5	Fig. 6
$t_h$	hold time $S_0, S_1$ to CP	0	-13		0		0		ns	4.5	Fig. 8
$f_{max}$	maximum clock pulse frequency	22	40		18		15		MHz	4.5	Fig. 6

AC WAVEFORMS

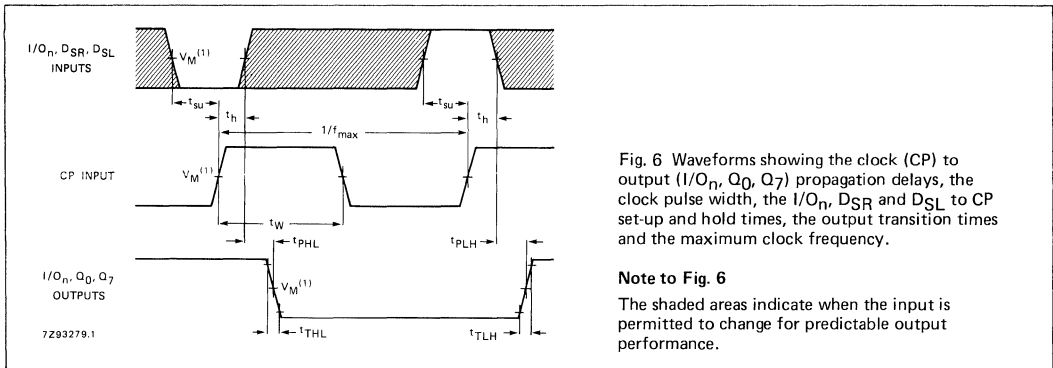


Fig. 6 Waveforms showing the clock (CP) to output ( $I/O_n$ ,  $Q_0$ ,  $Q_7$ ) propagation delays, the clock pulse width, the  $I/O_n$ ,  $D_{SR}$  and  $D_{SL}$  to CP set-up and hold times, the output transition times and the maximum clock frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

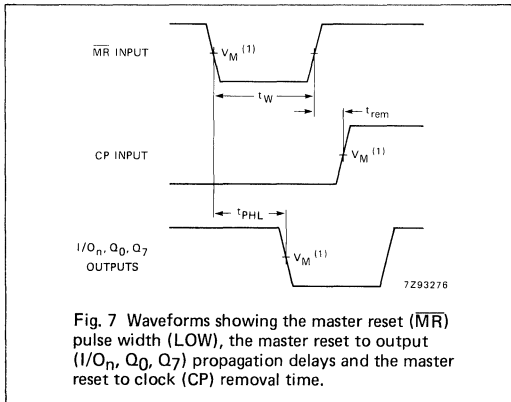


Fig. 7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width (LOW), the master reset to output ( $I/O_n$ ,  $Q_0$ ,  $Q_7$ ) propagation delays and the master reset to clock (CP) removal time.

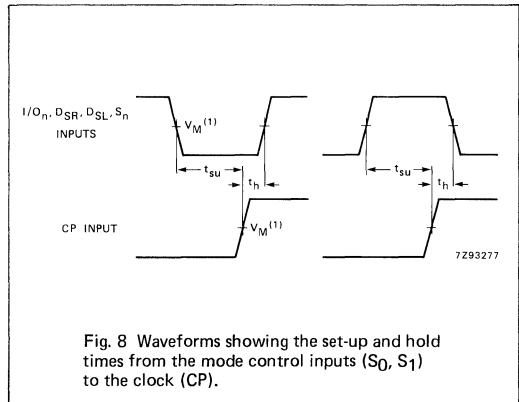


Fig. 8 Waveforms showing the set-up and hold times from the mode control inputs ( $S_0$ ,  $S_1$ ) to the clock (CP).

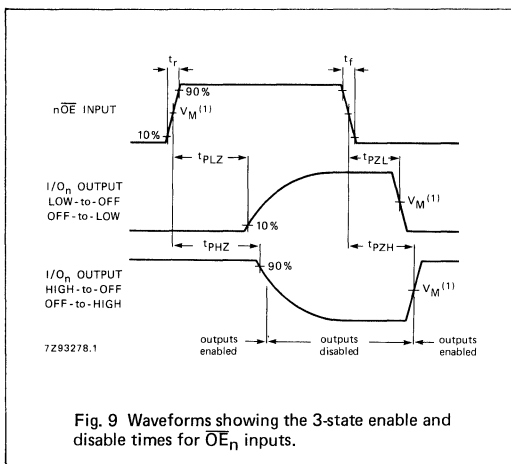


Fig. 9 Waveforms showing the 3-state enable and disable times for  $OE_n$  inputs.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_1 = GND$  to  $V_{CC}$ .  
 HCT:  $V_M = 1.3V$ ;  $V_1 = GND$  to  $3V$ .





# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT354

MSI

## 8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

### FEATURES

- Transparent data latch
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input (LE).

The transparent 8-bit data latches are enabled when the active LOW data enable input ( $\bar{E}$ ) is LOW.

When the output enable input  $\overline{OE}_1 = \text{HIGH}$ ,  $\overline{OE}_2 = \text{HIGH}$  or  $\overline{OE}_3 = \text{LOW}$ , the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $S_n, D_n$ to $Y, \bar{Y}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	23	25	ns
$C_i$	input capacitance		3.5	3.5	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT354P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT354T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	$D_0$ to $D_7$	data inputs
9	$\bar{E}$	data enable input (active LOW)
10	GND	ground (0 V)
11	$\bar{LE}$	latch enable input (active LOW)
14, 13, 12	$S_0, S_1, S_2$	select inputs
15, 16	$\overline{OE}_1, \overline{OE}_2$	output enable inputs (active LOW)
17	$\overline{OE}_3$	output enable input (active HIGH)
18	$\bar{Y}$	3-state multiplexer output (active LOW)
19	$Y$	3-state multiplexer output (active HIGH)
20	$V_{CC}$	positive supply voltage

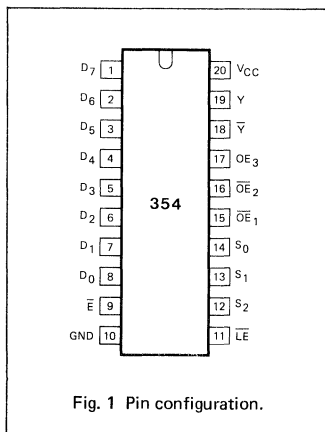


Fig. 1 Pin configuration.

## FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION	
ADDRESS *			$\bar{E}$	OUTPUT ENABLE			Y	$\bar{Y}$		
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>		$\bar{OE}_1$	$\bar{OE}_2$	OE <sub>3</sub>				
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state	
X	X	X	X	X	H	X	Z	Z		
X	X	X	X	X	X	L	Z	Z		
L	L	L	L	L	L	H	D <sub>0</sub>	$\bar{D}_0$	data latch is transparent	
L	L	H	L	L	L	H	D <sub>1</sub>	$\bar{D}_1$		
L	H	L	L	L	L	H	D <sub>2</sub>	$\bar{D}_2$		
L	H	H	L	L	L	H	D <sub>3</sub>	$\bar{D}_3$		
H	L	L	L	L	L	H	D <sub>4</sub>	$\bar{D}_4$		
H	L	H	L	L	L	H	D <sub>5</sub>	$\bar{D}_5$		
H	H	L	L	L	L	H	D <sub>6</sub>	$\bar{D}_6$		
H	H	H	L	L	L	H	D <sub>7</sub>	$\bar{D}_7$		
L	L	L	H	L	L	H	D <sub>0n</sub>	$\bar{D}_{0n}$		data is latched
L	L	H	H	L	L	H	D <sub>1n</sub>	$\bar{D}_{1n}$		
L	H	L	H	L	L	H	D <sub>2n</sub>	$\bar{D}_{2n}$		
L	H	H	H	L	L	H	D <sub>3n</sub>	$\bar{D}_{3n}$		
H	L	L	H	L	L	H	D <sub>4n</sub>	$\bar{D}_{4n}$		
H	L	H	H	L	L	H	D <sub>5n</sub>	$\bar{D}_{5n}$		
H	H	L	H	L	L	H	D <sub>6n</sub>	$\bar{D}_{6n}$		
H	H	H	H	L	L	H	D <sub>7n</sub>	$\bar{D}_{7n}$		

D<sub>0</sub> to D<sub>7</sub> = data at inputs D<sub>0</sub> to D<sub>7</sub>

D<sub>0n</sub> to D<sub>7n</sub> = data at inputs D<sub>0</sub> to D<sub>7</sub> before the most recent LOW-to-HIGH transition of  $\bar{E}$

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

\* This column shows the input address set-up with  $\bar{E}$  = LOW

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT356  
MSI

## 8-INPUT MULTIPLEXER/REGISTER; 3-STATE

### FEATURES

- Non-transparent data latch
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT356 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT356 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input  $\overline{LE}$ .

Data on the 8 input lines ( $D_0$  to  $D_7$ ) is clocked into a edge-triggered data register by a LOW-to-HIGH transition of the clock (CP).

When the output enable input  $\overline{OE}_1 = \text{HIGH}$ ,  $\overline{OE}_2 = \text{HIGH}$  or  $\overline{OE}_3 = \text{LOW}$ , the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches and register.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> , CP to Y, $\overline{Y}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	23	25	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT356P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT356T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D <sub>0</sub> to D <sub>7</sub>	data inputs
9	CP	clock input (LOW-to-HIGH, edge-triggered)
10	GND	ground (0 V)
11	$\overline{LE}$	latch enable input (active LOW)
14, 13, 12	S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub>	select inputs
15, 16	$\overline{OE}_1$ , $\overline{OE}_2$	output enable inputs (active LOW)
17	OE <sub>3</sub>	output enable input (active HIGH)
18	$\overline{Y}$	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V <sub>CC</sub>	positive supply voltage

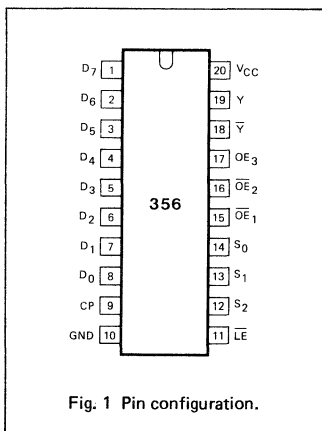


Fig. 1 Pin configuration.

FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION	
ADDRESS *			CP	OUTPUT ENABLE			Y	$\bar{Y}$		
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>		$\bar{OE}_1$	$\bar{OE}_2$	OE <sub>3</sub>				
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state	
X	X	X	X	X	H	X	Z	Z		
X	X	X	X	X	X	L	Z	Z		
L	L	L	↑	L	L	H	D <sub>0n</sub>	$\bar{D}_{0n}$	data is clocked into latch	
L	L	H	↑	L	L	H	D <sub>1n</sub>	$\bar{D}_{1n}$		
L	H	L	↑	L	L	H	D <sub>2n</sub>	$\bar{D}_{2n}$		
L	H	H	↑	L	L	H	D <sub>3n</sub>	$\bar{D}_{3n}$		
H	L	L	↑	L	L	H	D <sub>4n</sub>	$\bar{D}_{4n}$		
H	L	H	↑	L	L	H	D <sub>5n</sub>	$\bar{D}_{5n}$		
H	H	L	↑	L	L	H	D <sub>6n</sub>	$\bar{D}_{6n}$		
H	H	H	↑	L	L	H	D <sub>7n</sub>	$\bar{D}_{7n}$		
L	L	L	**	L	L	H	D <sub>0p</sub>	$\bar{D}_{0p}$		outputs do not change states
L	L	H	**	L	L	H	D <sub>1p</sub>	$\bar{D}_{1p}$		
L	H	L	**	L	L	H	D <sub>2p</sub>	$\bar{D}_{2p}$		
L	H	H	**	L	L	H	D <sub>3p</sub>	$\bar{D}_{3p}$		
H	L	L	**	L	L	H	D <sub>4p</sub>	$\bar{D}_{4p}$		
H	L	H	**	L	L	H	D <sub>5p</sub>	$\bar{D}_{5p}$		
H	H	L	**	L	L	H	D <sub>6p</sub>	$\bar{D}_{6p}$		
H	H	H	**	L	L	H	D <sub>7p</sub>	$\bar{D}_{7p}$		

D<sub>0n</sub> to D<sub>7n</sub> = data present at inputs D<sub>0</sub> to D<sub>7</sub> when the data latch clock made the transition from LOW-to-HIGH

D<sub>0p</sub> to D<sub>7p</sub> = data previously latched into the data latch by the LOW-to-HIGH transition of the data latch clock

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH CP transition

↓ = HIGH-to-LOW CP transition

Z = high impedance OFF-state

\* This column shows the input address set-up with  $\bar{CE} = \text{LOW}$ .

\*\* CP is HIGH, LOW or ↓.

## HEX BUFFER/LINE DRIVER; 3-STATE

### FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT365 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT365 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ( $\overline{OE}_1$ ,  $\overline{OE}_2$ ).

A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The "365" is identical to the "366" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3,5	3,5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	40	40	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

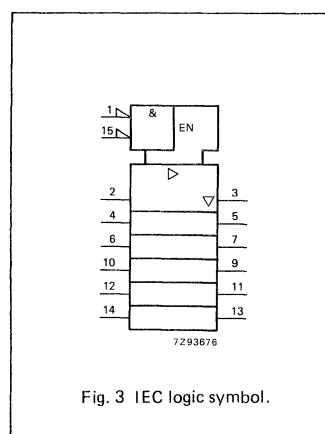
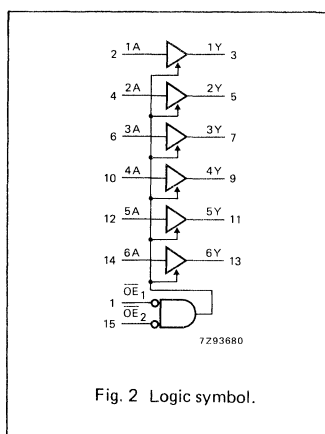
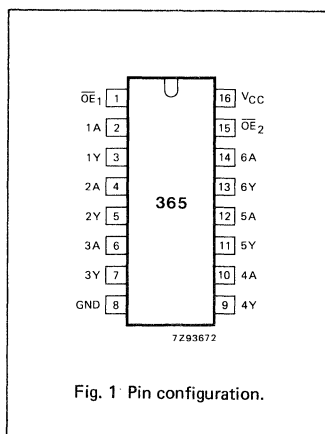
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT365P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT365T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$ , $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage



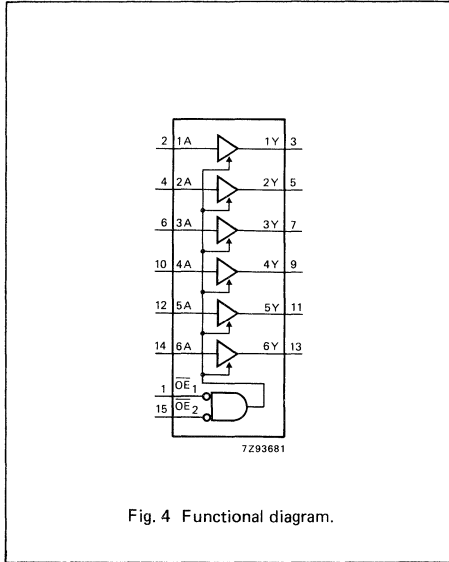


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

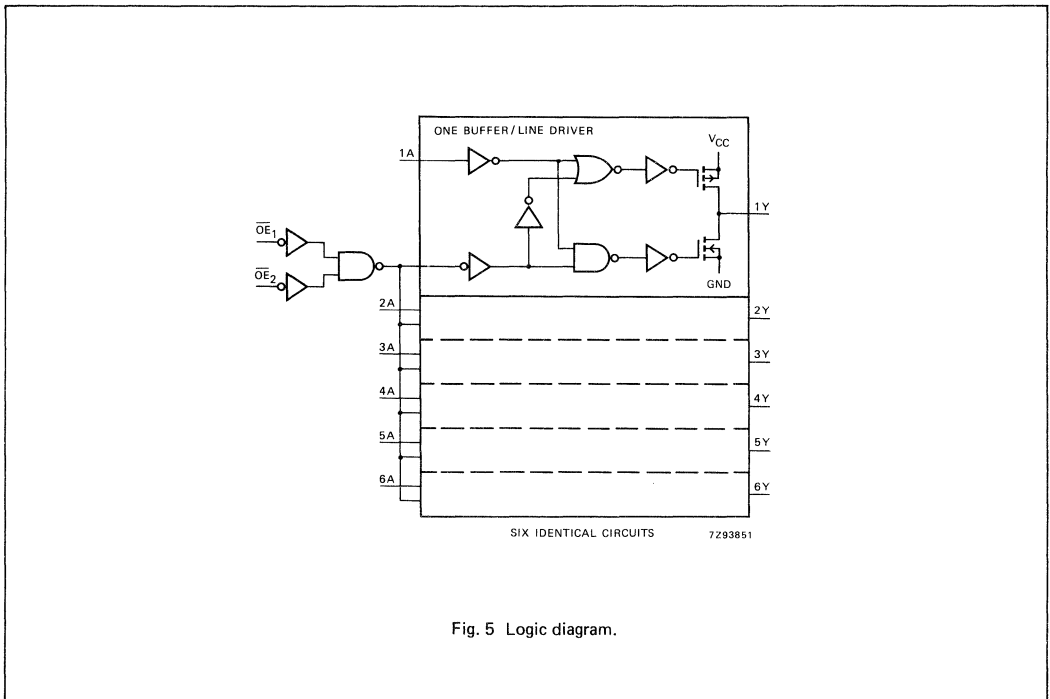


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>n</sub> to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>n</sub> to nY		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>T LH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types.**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE <sub>1</sub>	1.00
OE <sub>2</sub>	0.90
nA	1.00

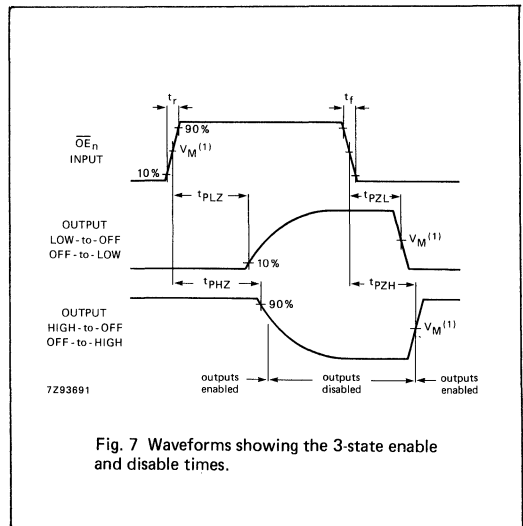
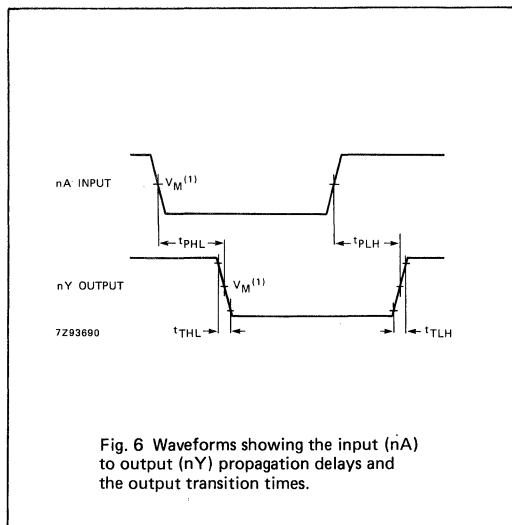


AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig. 6
$t_{pZH}/t_{pZL}$	3-state output enable time $\overline{OE}_n$ to nY		16	35		44		53	ns	4.5	Fig. 7
$t_{pHZ}/t_{pLZ}$	3-state output disable time $\overline{OE}_n$ to nY		20	35		44		53	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

FEATURES

- Inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT366 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT366 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ( $\overline{OE}_1, \overline{OE}_2$ ).

A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The "366" is identical to the "365" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	10	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT366P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT366T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1, \overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage

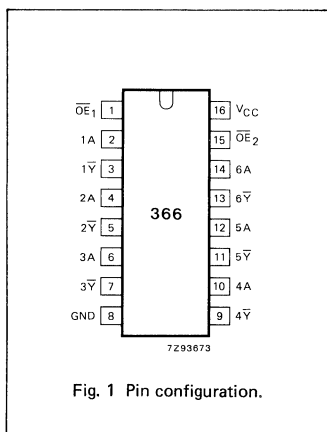


Fig. 1 Pin configuration.

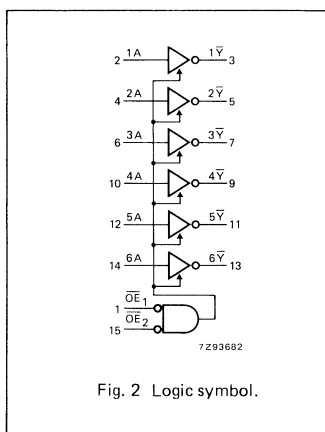


Fig. 2 Logic symbol.

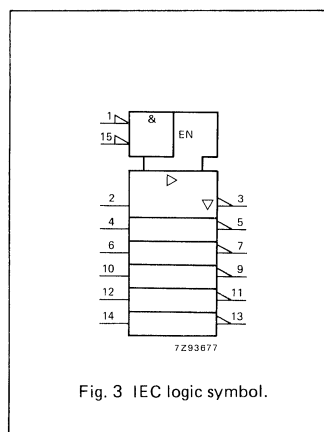


Fig. 3 IEC logic symbol.



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE <sub>n</sub> to nY		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE <sub>n</sub> to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given in the family specifications. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

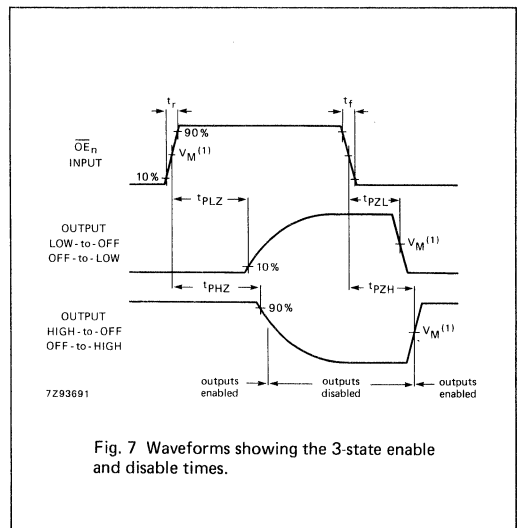
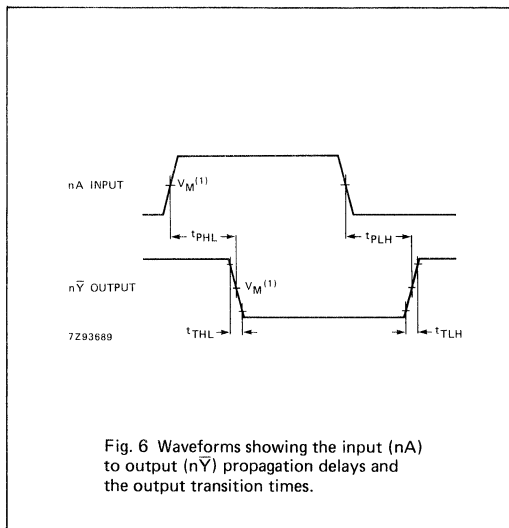
INPUT	UNIT LOAD COEFFICIENT
OE <sub>1</sub>	1.00
OE <sub>2</sub>	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to nY		13	24		30		36	ns	4.5	Fig. 6
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}_n$ to nY		16	35		44		53	ns	4.5	Fig. 7
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}_n$ to nY		20	35		44		53	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

HEX BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs (1OE, 2OE). A HIGH on nOE causes the outputs to assume a high impedance OFF-state. The "367" is identical to the "368" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT367P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT367T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1OE, 2OE	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage

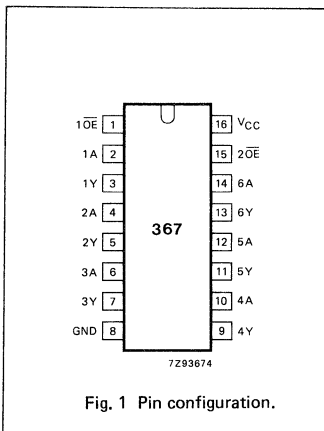


Fig. 1 Pin configuration.

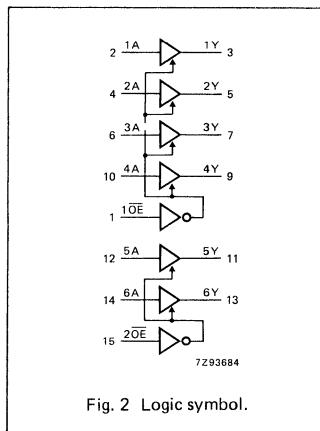


Fig. 2 Logic symbol.

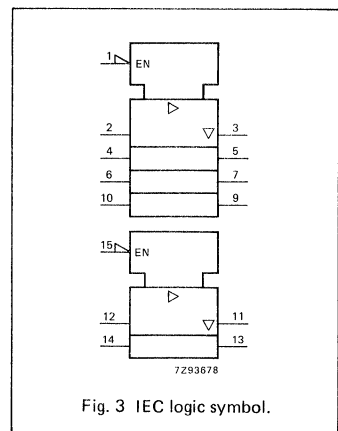


Fig. 3 IEC logic symbol.

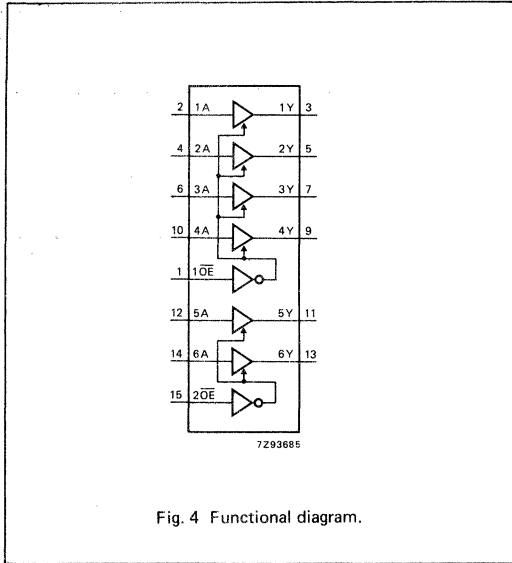


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

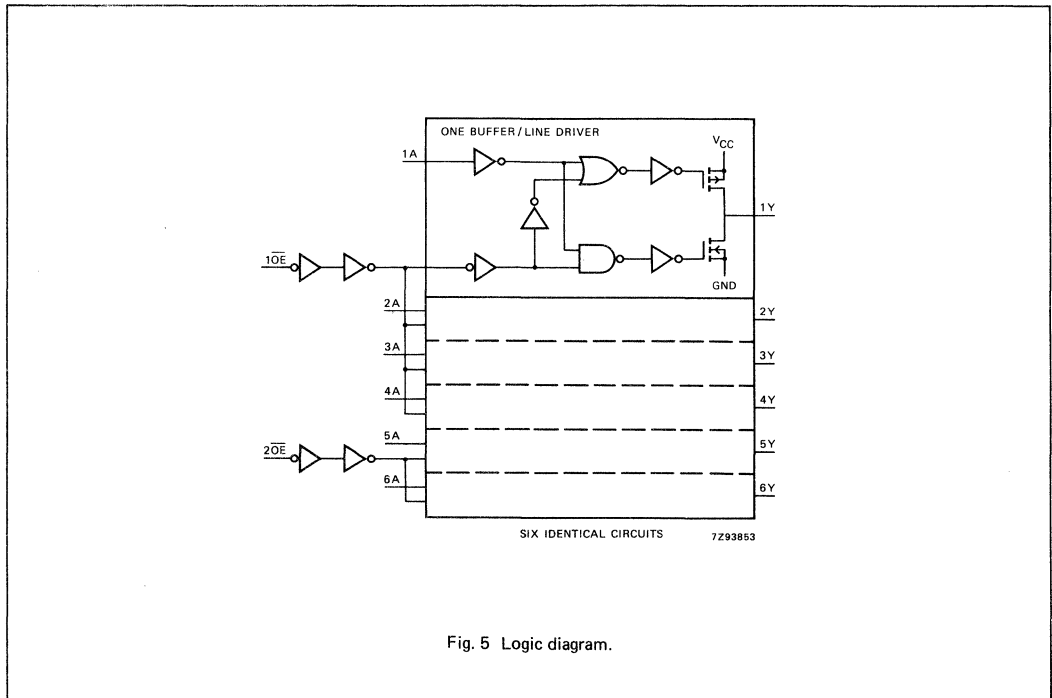


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY	44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY	55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1OE	1.00
2OE	0.90
nA	1.00

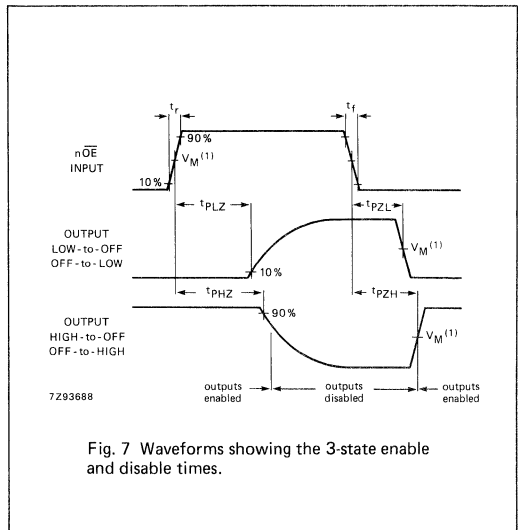
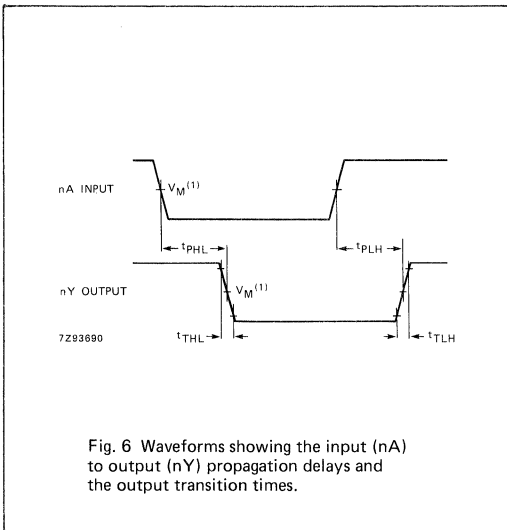


AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig. 6
$t_{pZH}/t_{pZL}$	3-state output enable time nOE to nY		16	35		44		53	ns	4.5	Fig. 7
$t_{pHZ}/t_{pLZ}$	3-state output disable time nOE to nY		21	35		44		53	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.

## HEX BUFFER/LINE DRIVER; 3-STATE; INVERTING

### FEATURES

- Inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT368 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT368 are hex inverting buffer/line drivers with 3-state outputs. The 3-state outputs (n $\bar{Y}$ ) are controlled by the output enable inputs (1 $\bar{O}E$ , 2 $\bar{O}E$ ).

A HIGH on n $\bar{O}E$  causes the outputs to assume a high impedance OFF-state.

The "368" is identical to the "367" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to n $\bar{Y}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

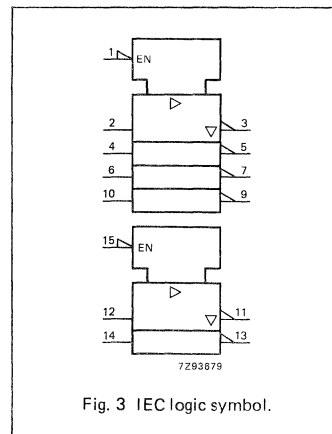
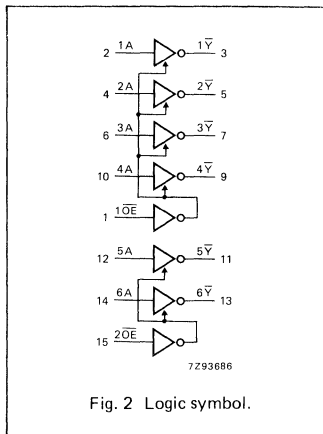
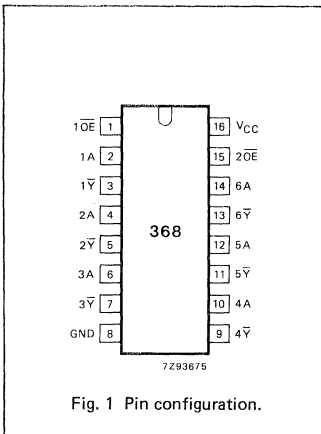
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT368P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT368T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1 $\bar{O}E$ , 2 $\bar{O}E$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1 $\bar{Y}$ to 6 $\bar{Y}$	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage



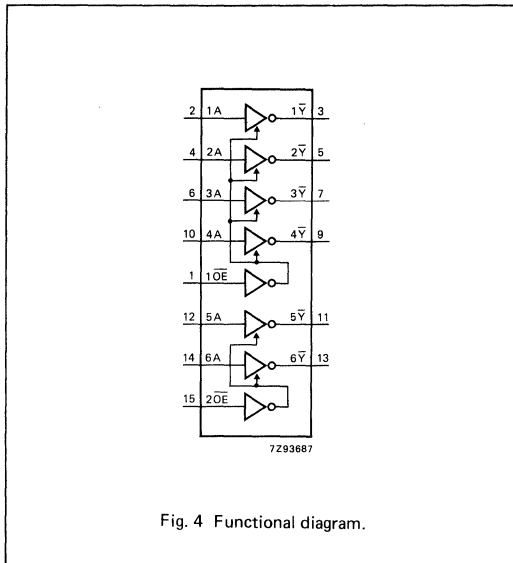


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nA	nY
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

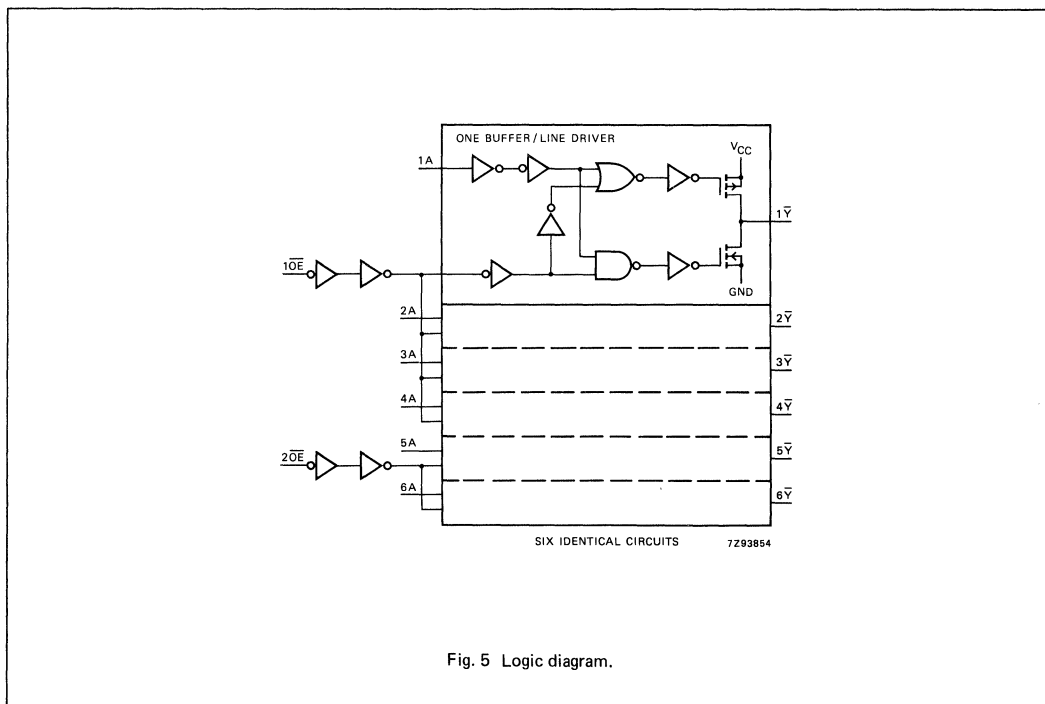


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		30 11 9	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

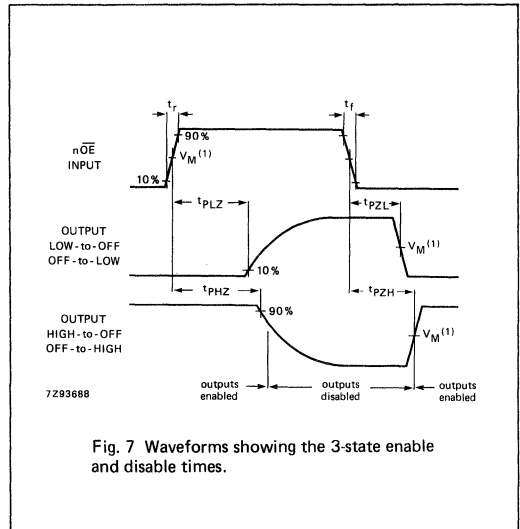
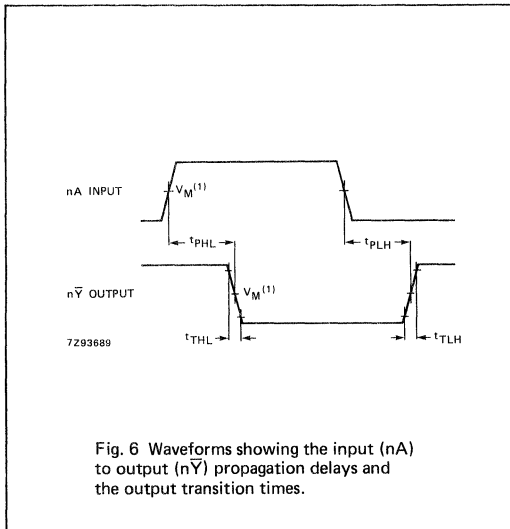
INPUT	UNIT LOAD COEFFICIENT
1OE	1.00
2OE	0.90
nA	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to n $\bar{Y}$		13	24		30		36	ns	4.5	Fig. 6
$t_{PZH}/t_{PZL}$	3-state output enable time n $\bar{OE}$ to n $\bar{Y}$		17	35		44		53	ns	4.5	Fig. 7
$t_{PHZ}/t_{PLZ}$	3-state output disable time n $\bar{OE}$ to n $\bar{Y}$		20	35		44		53	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .
- HCT:  $V_M = 1.3$  V;  $V_I = GND$  to 3 V.

## OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

### FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563", "573" and "533"
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

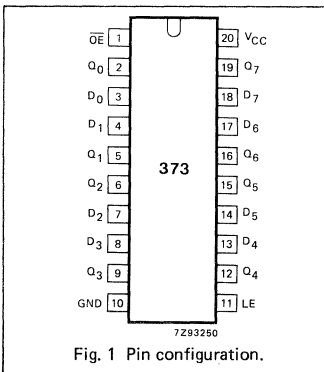
The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The "373" is functionally identical to the "533", "563" and "573", but the "563" and "533" have inverted outputs and the "563" and "573" have a different pin arrangement.



SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub> LE to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12 15	14 13	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	45	41	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

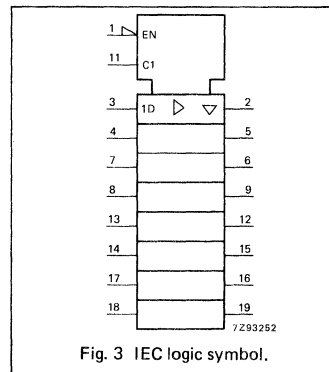
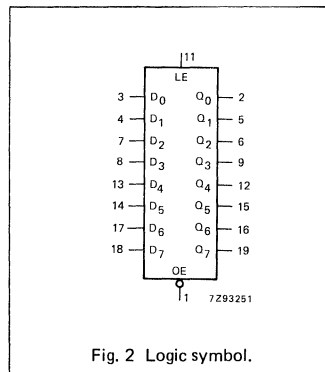
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT373P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT373T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q <sub>0</sub> to Q <sub>7</sub>	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V <sub>CC</sub>	positive supply voltage



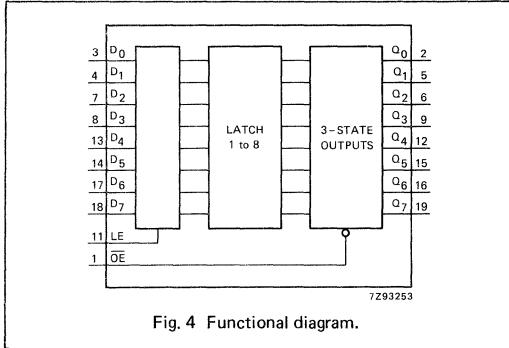


Fig. 4 Functional diagram.

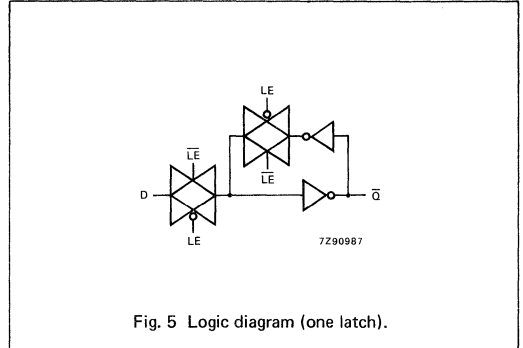


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	$D_n$		$Q_0$ to $Q_7$
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW transition  
Z = high impedance OFF-state

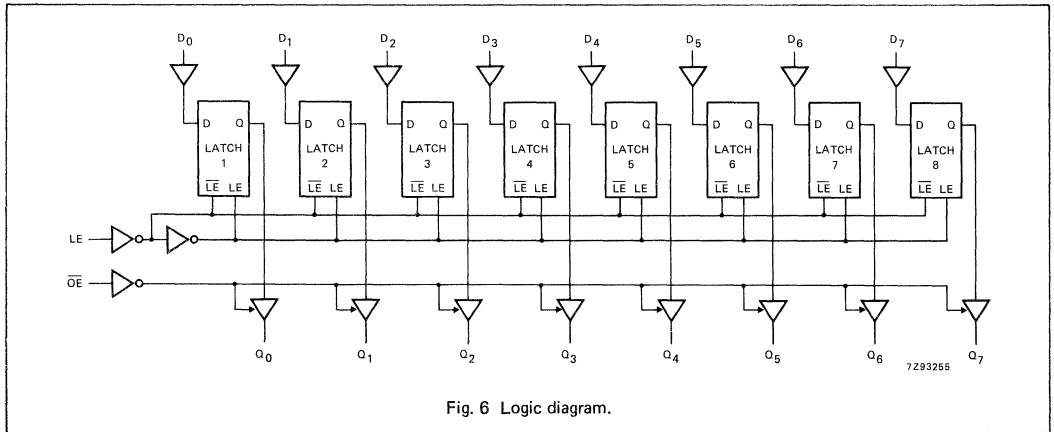


Fig. 6 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/$ $t_{PLH}$	propagation delay $D_n$ to $Q_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/$ $t_{PLH}$	propagation delay LE to $Q_n$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
$t_{PZH}/$ $t_{PZL}$	3-state output enable time $\overline{OE}$ to $Q_n$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
$t_{PHZ}/$ $t_{PLZ}$	3-state output disable time $\overline{OE}$ to $Q_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
$t_{THL}/$ $t_{TLH}$	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
$t_W$	LE pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
$t_{su}$	set-up time $D_n$ to LE	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
$t_h$	hold time $D_n$ to LE	5 5 5	-8 -3 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
D <sub>n</sub>	0.30
LE	1.50
OE	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74CHT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		17	30		38		45	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		16	32		40		48	ns	4.5	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		19	32		40		48	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 7
t <sub>W</sub>	LE pulse width HIGH	16	6		20		24		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	12	6		15		18		ns	4.5	Fig. 10
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4	-1		4		4		ns	4.5	Fig. 10

AC WAVEFORMS

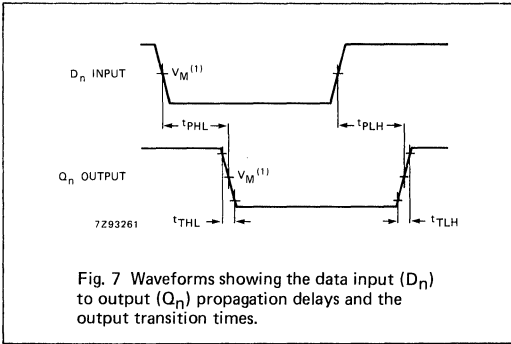


Fig. 7 Waveforms showing the data input ( $D_n$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

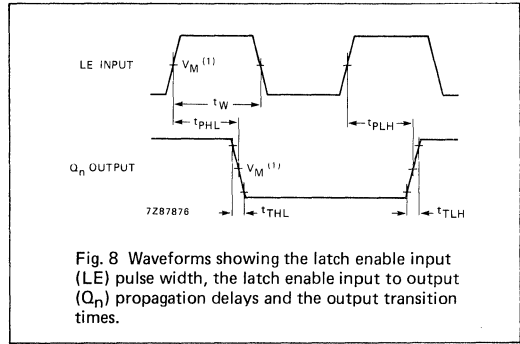


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ( $Q_n$ ) propagation delays and the output transition times.

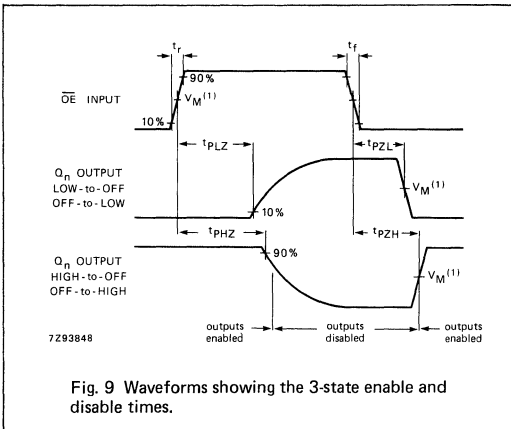


Fig. 9 Waveforms showing the 3-state enable and disable times.

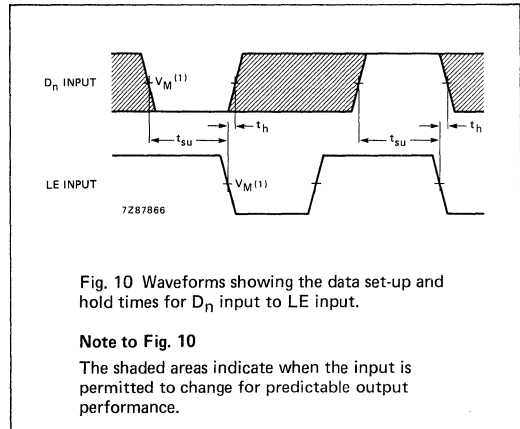


Fig. 10 Waveforms showing the data set-up and hold times for  $D_n$  input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.

A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	13	ns
f <sub>max</sub>	maximum clock frequency		77	48	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

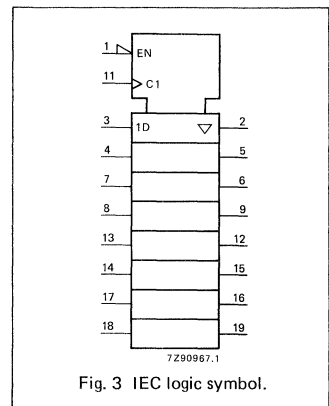
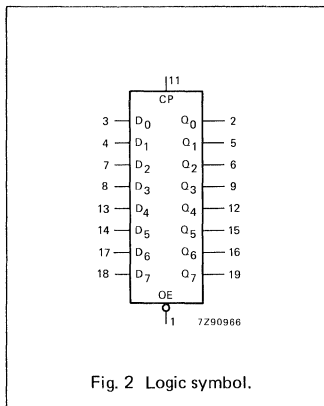
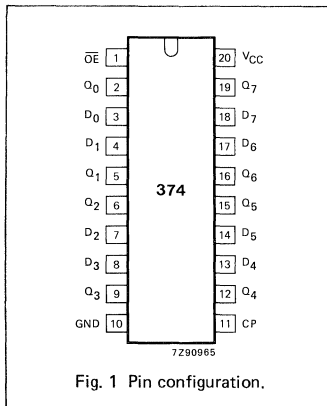
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT374P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT374T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q <sub>0</sub> to Q <sub>7</sub>	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V <sub>CC</sub>	positive supply voltage



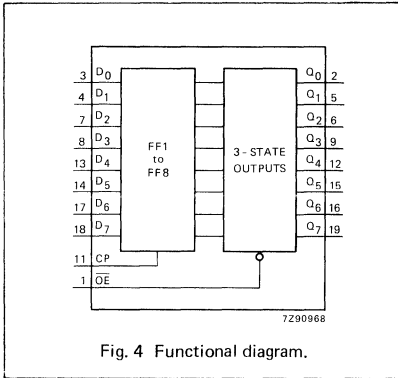


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS Q <sub>0</sub> to Q <sub>7</sub>
	OE	CP	D <sub>n</sub>		
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 Z = high impedance OFF-state  
 ↑ = LOW-to-HIGH CP transition

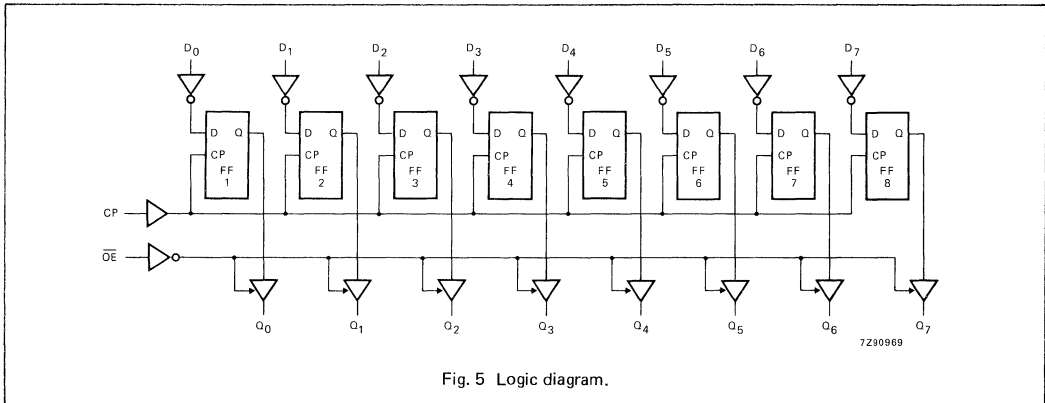


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		50 18 14	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5 5 5	-6 -2 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	23 70 83		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$\overline{OE}$	1.25
CP	0.90
D <sub>n</sub>	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		16	32		40		48	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Q <sub>n</sub>		16	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Q <sub>n</sub>		18	28		35		42	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	7		15		18		ns	4.5	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5	-3		5		5		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig. 6

AC WAVEFORMS

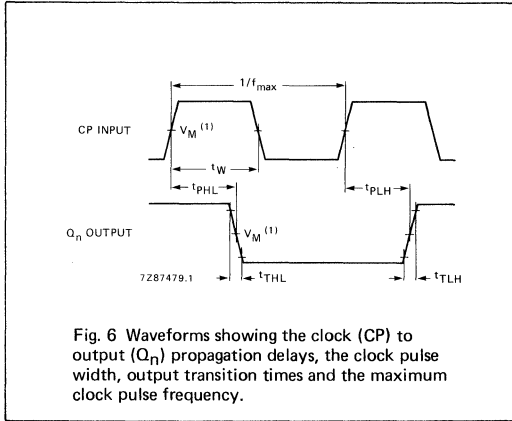


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

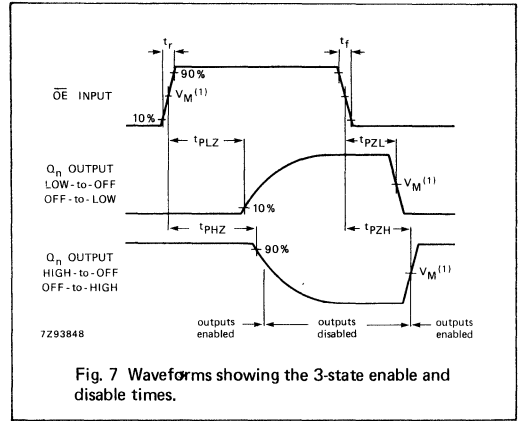


Fig. 7 Waveforms showing the 3-state enable and disable times.

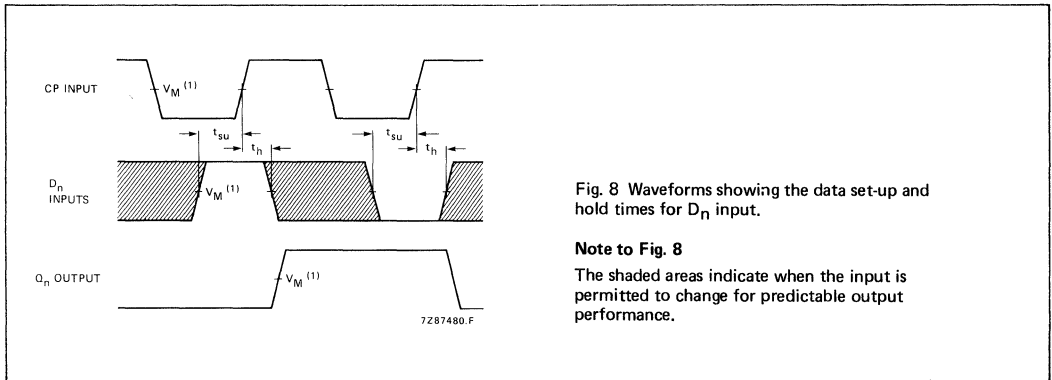


Fig. 8 Waveforms showing the data set-up and hold times for  $D_n$  input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**OCTAL D-TYPE FLIP-FLOP WITH DATA ENABLE; POSITIVE-EDGE TRIGGER**

**FEATURES**

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See "273" for master reset version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability: standard
- I<sup>CC</sup> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

A common clock (CP) input loads all flip-flops simultaneously when the data enable ( $\bar{E}$ ) is LOW.

The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output ( $Q_n$ ) of the flip-flop.

The  $\bar{E}$  input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	13	14	ns
$f_{max}$	maximum clock frequency		76	54	MHz
$C_I$	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

**Notes**

1. CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz                       $C_L$  = output load capacitance in pF

$f_o$  = output frequency in MHz

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT377P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT377T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$Q_0$ to $Q_7$	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	$V_{CC}$	positive supply voltage

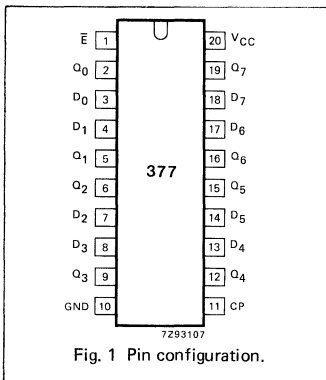


Fig. 1 Pin configuration.

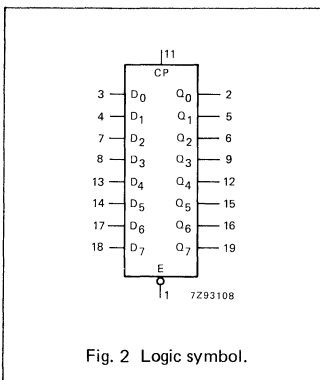


Fig. 2 Logic symbol.

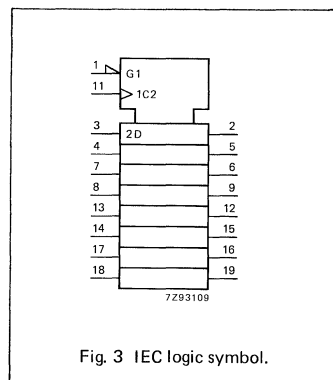


Fig. 3 IEC logic symbol.



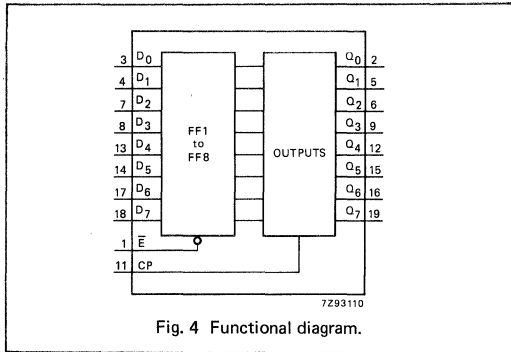


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	$\bar{E}$	D <sub>n</sub>	Q <sub>n</sub>
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
↑ = LOW-to-HIGH CP transition  
X = don't care

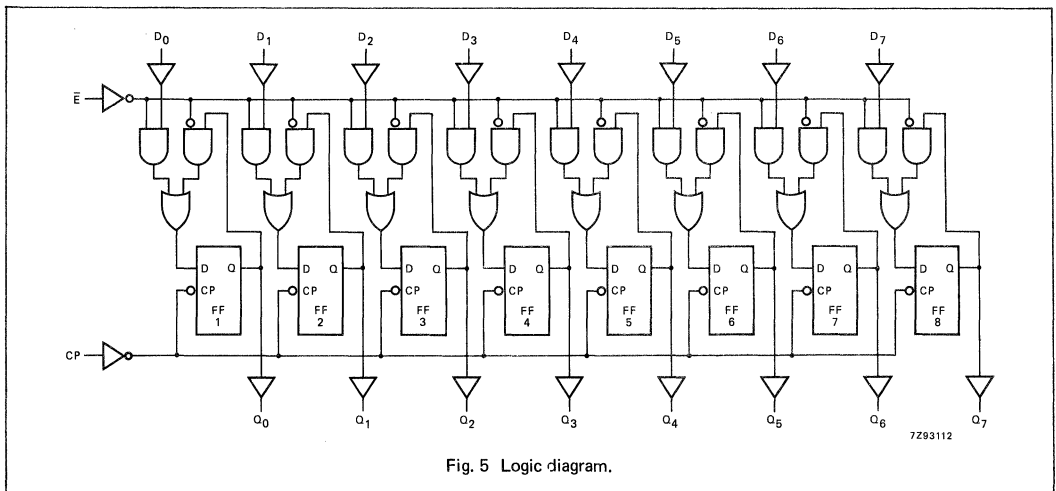


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time E to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time E to CP	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	23 70 83		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

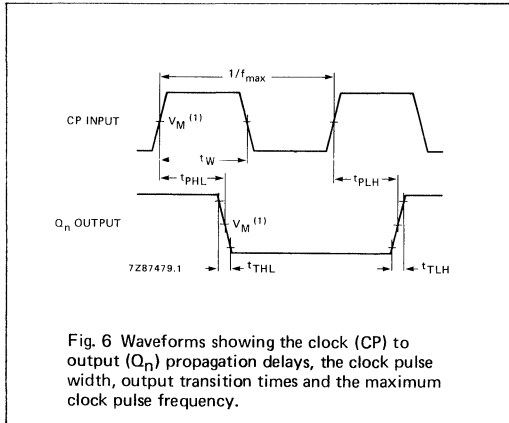
input	unit load coefficient
$\bar{E}$	1.50
CP	0.50
D <sub>n</sub>	0.20

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

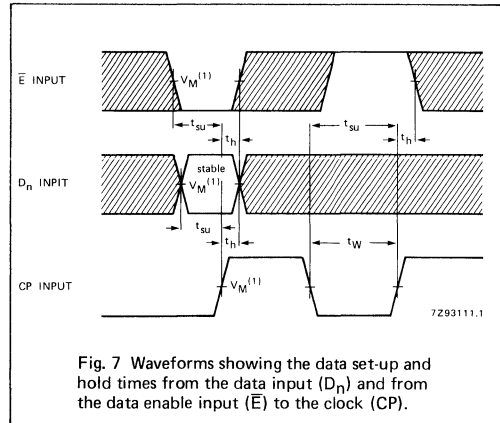
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		17	32		40		48	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	9		25		30		ns	4.5	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	4		15		18		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time $\bar{E}$ to CP	22	12		28		33		ns	4.5	Fig. 7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	2	-4		2		2		ns	4.5	Fig. 7
t <sub>h</sub>	hold time $\bar{E}$ to CP	3	-2		3		3		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.



## DUAL DECADE RIPPLE COUNTER

### FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks (nCP<sub>0</sub> and nCP<sub>1</sub>) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>0</sub> nCP <sub>1</sub> to nQ <sub>1</sub> nCP <sub>1</sub> to nQ <sub>2</sub> nCP <sub>1</sub> to nQ <sub>3</sub> nMR to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 15 23 15 16	18 19 26 19 18	ns ns ns ns ns
f <sub>max</sub>	maximum clock frequency nCP <sub>0</sub> , nCP <sub>1</sub>		66	61	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per counter	notes 1 and 2	20	21	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

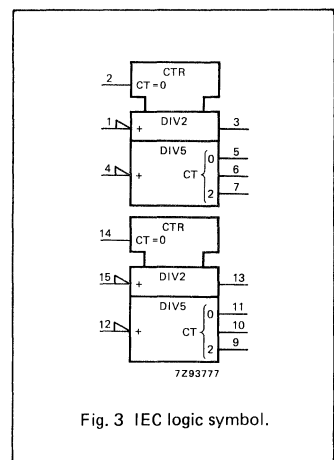
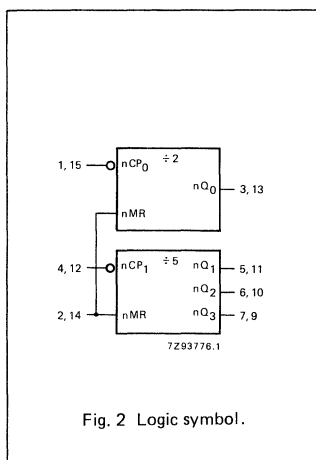
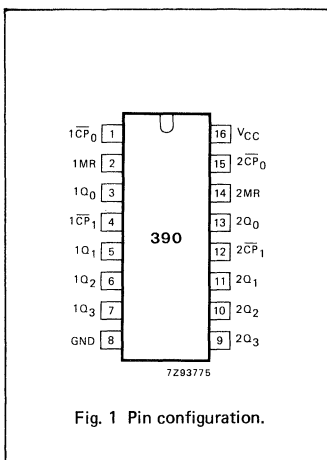
### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
where:  
f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT390P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT390T: 16-lead mini-pack; plastic (SO-16; SOT-109A).



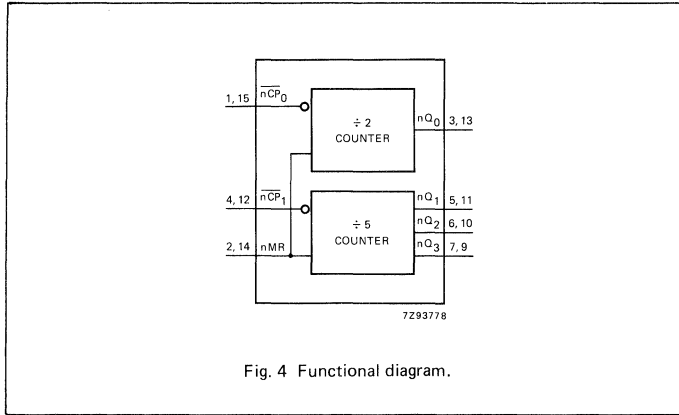


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ( $n\overline{CP}_0$  and  $n\overline{CP}_1$ ).

For BCD decade operation, the  $nQ_0$  output is connected to the  $n\overline{CP}_1$  input of the divide-by-5 section. For bi-quinary decade operation, the  $nQ_3$  output is connected to the  $n\overline{CP}_0$  input and  $nQ_0$  becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0, 2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1, 2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	$V_{CC}$	positive supply voltage

**BCD COUNT SEQUENCE FOR 1/2 THE "390"**

COUNT	OUTPUTS			
	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

**Note**

Output  $Q_0$  connected to  $n\overline{CP}_1$  with counter input on  $n\overline{CP}_0$ .

H = HIGH voltage level  
L = LOW voltage level

**BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"**

COUNT	OUTPUTS			
	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

**Note**

Output  $Q_3$  connected to  $n\overline{CP}_0$  with counter input on  $n\overline{CP}_1$ .





## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>0</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>1</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>2</sub>		74 27 22	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>3</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width nCP <sub>0</sub> , nCP <sub>1</sub>	80 16 14	19 7 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6	
t <sub>W</sub>	master reset pulse width nMR	80 17 14	28 10 8		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7	
t <sub>rem</sub>	removal time nMR to nCP <sub>n</sub>	75 15 13	22 8 6		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig. 6	

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP <sub>0</sub>	0.45
nCP <sub>1</sub> , nMR	0.60

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>0</sub>		21	34		43		51	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>1</sub>		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>2</sub>		30	51		64		77	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>3</sub>		22	38		48		57	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		21	36		45		54	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width nCP <sub>0</sub> , nCP <sub>1</sub>	18	8		23		27		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width nMR	17	10		21		26		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time nMR to nCP <sub>n</sub>	15	8		19		22		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

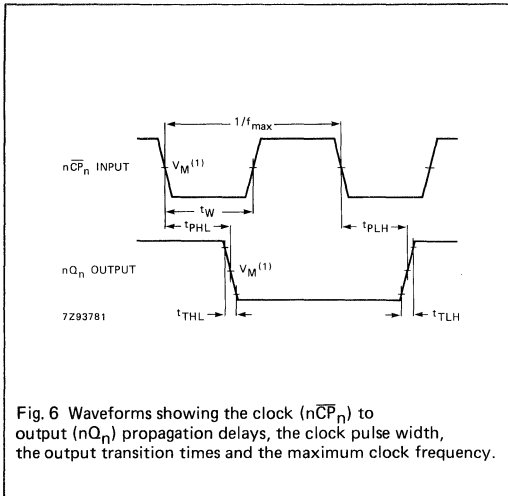


Fig. 6 Waveforms showing the clock ( $n\overline{CP}_n$ ) to output ( $nQ_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

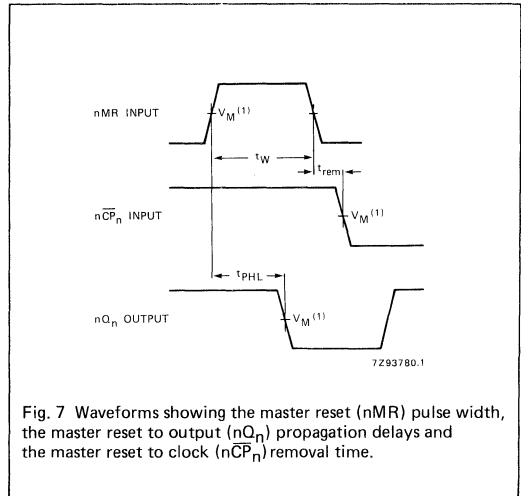


Fig. 7 Waveforms showing the master reset ( $nMR$ ) pulse width, the master reset to output ( $nQ_n$ ) propagation delays and the master reset to clock ( $n\overline{CP}_n$ ) removal time.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .
- HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

## DUAL 4-BIT BINARY RIPPLE COUNTER

### FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks (1CP and 2CP) and master reset (1MR and 2MR) inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.

A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ <sub>0</sub> nQ to nQ <sub>n+1</sub> nMR to nQ <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12	20	ns
			5	6	ns
			11	15	ns
f <sub>max</sub>	maximum clock frequency		99	53	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	23	25	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT393P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT393T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1CP, 2CP	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	1Q <sub>0</sub> to 1Q <sub>3</sub> , 2Q <sub>0</sub> to 2Q <sub>3</sub>	flip-flop outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

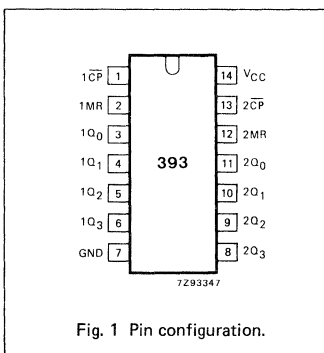


Fig. 1 Pin configuration.

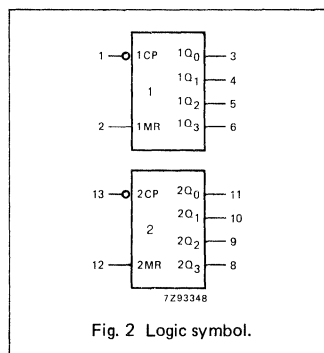


Fig. 2 Logic symbol.

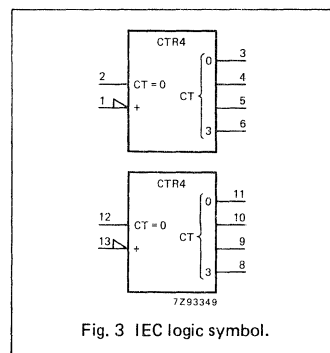


Fig. 3 IEC logic symbol.

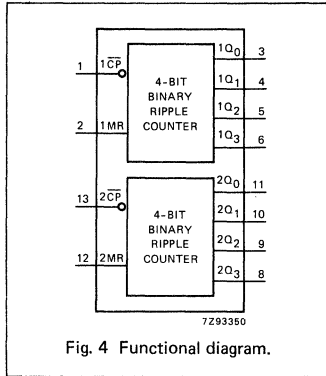


Fig. 4 Functional diagram.

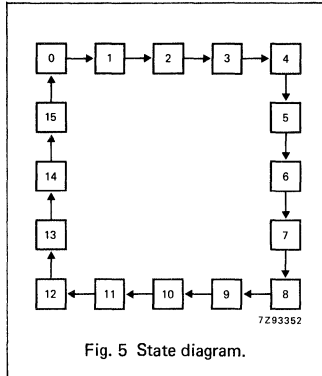


Fig. 5 State diagram.

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	H	H
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level  
L = LOW voltage level

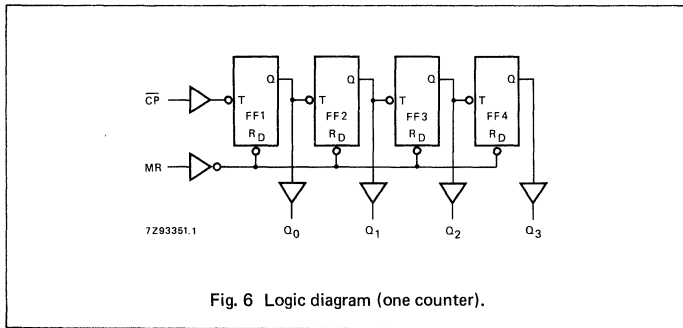


Fig. 6 Logic diagram (one counter).

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{CP}$ to $nQ_0$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/t_{PLH}$	propagation delay $nQ_n$ to $nQ_{n+1}$		14 5 4	45 9 8		55 11 9		70 14 12	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}$	propagation delay $nMR$ to $nQ_n$		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
$t_W$	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_W$	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
$t_{rem}$	removal time $nMR$ to $n\overline{CP}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
$f_{max}$	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

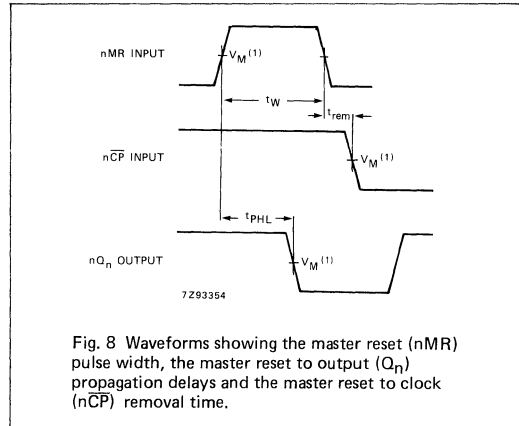
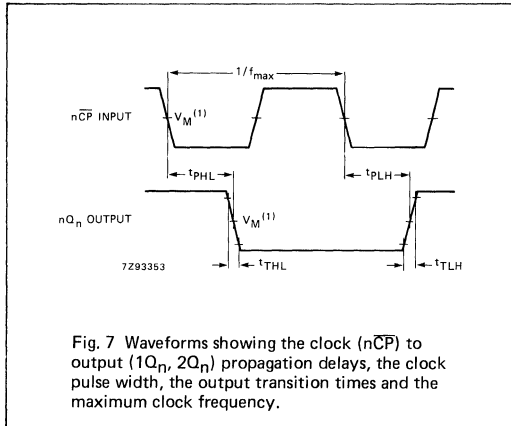
input	unit load coefficient
1CP	0.4
2CP	0.4
1MR	1.0
2MR	1.0

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ <sub>0</sub>		24	32		40		48	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nQ <sub>n</sub> to nQ <sub>n+1</sub>		6	12		15		18	ns	4.5	Fig. 7
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		18	32		40		48	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7
t <sub>W</sub>	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width; HIGH	16	7		20		24		ns	4.5	Fig. 8
t <sub>rem</sub>	removal time nMR to nCP	5	0		5		5		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig. 7

## AC WAVEFORMS



## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .





## DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

### FEATURES

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for  $n\overline{R}_{EXT}/C_{EXT}$ )
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT423 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT423 are dual retriggerable monostable multivibrators with output pulse width control by two methods. The basic pulse time is programmed by selection of an external resistor ( $R_{EXT}$ ) and capacitor ( $C_{EXT}$ ). The external resistor and capacitor are normally connected as shown in Fig. 6.

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ( $n\overline{A}$ ) or the active HIGH-going edge input ( $nB$ ). By repeating this process, the output pulse period ( $nQ = \text{HIGH}$ ,  $n\overline{Q} = \text{LOW}$ ) can be made as long as desired. When  $n\overline{R}_D$  is LOW, it forces the  $nQ$  output LOW, the  $n\overline{Q}$  output HIGH and also inhibits the triggering.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $n\overline{A}$ , $nB$ to $nQ$ , $n\overline{Q}$ $n\overline{R}_D$ to $nQ$ , $n\overline{Q}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$ $R_{EXT} = 5 \text{ k}\Omega$ $C_{EXT} = 0 \text{ pF}$	26 20	26 22	ns ns
$C_i$	input capacitance		3.5	3.5	pF
$t_W$	minimum output pulse width $nQ$ , $n\overline{Q}$		75	75	ns

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT423P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT423T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$ , $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	$1B$ , $2B$	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$ , $2\overline{R}_D$	direct reset action (active LOW)
4, 12	$1\overline{Q}$ , $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	$1Q$ , $2Q$	outputs (active HIGH)
14, 6	$1C_{EXT}$ , $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	$V_{CC}$	positive supply voltage

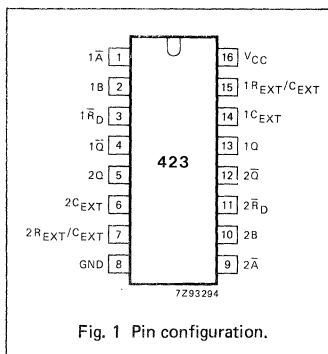


Fig. 1 Pin configuration.

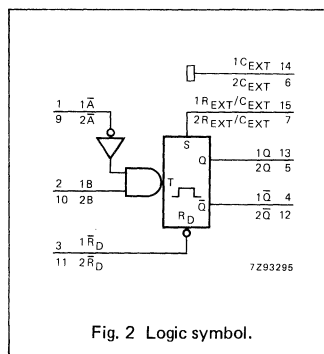


Fig. 2 Logic symbol.

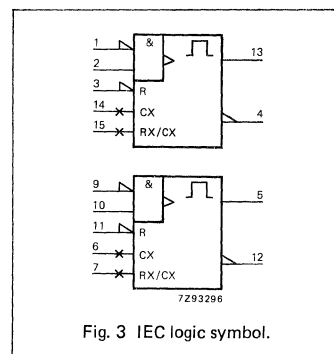


Fig. 3 IEC logic symbol.

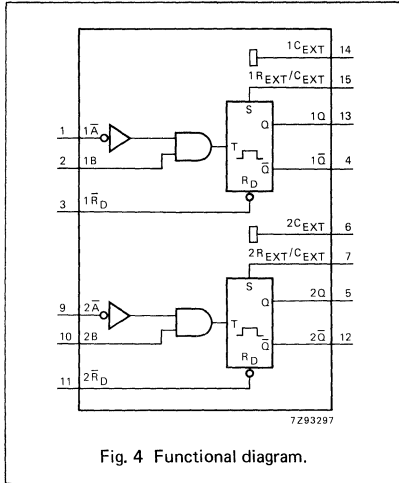


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

Figures 7 and 8 illustrate pulse control by reset. The basic output pulse width is essentially determined by the values of the external timing components  $R_{EXT}$  and  $C_{EXT}$ . For pulse widths, when  $C_{EXT} < 10\,000\text{ pF}$ , see Fig. 9. When  $C_{EXT} > 10\,000\text{ pF}$ , the typical output pulse width is defined as:

$$t_W = 0.45 \times R_{EXT} \times C_{EXT} \text{ (typ.)},$$

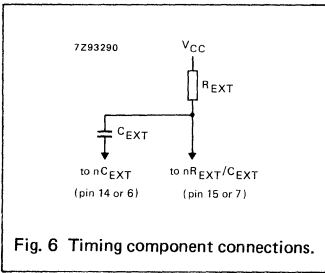
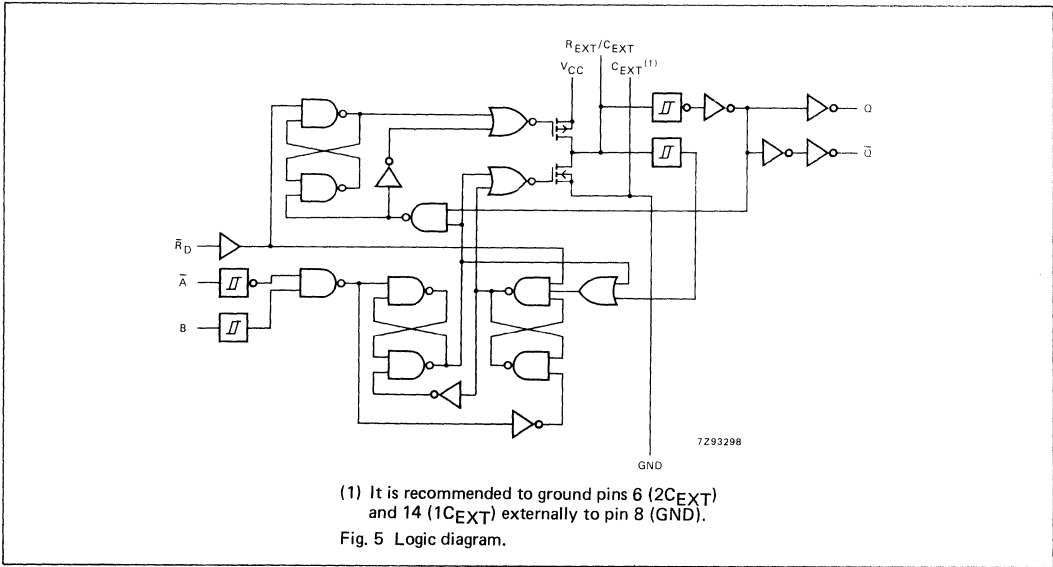
where,  $t_W$  = pulse width in ns;  
 $R_{EXT}$  = external resistor in  $k\Omega$ ;  
 $C_{EXT}$  = external capacitor in pF.

Schmitt-trigger action in the  $n\bar{A}$  and  $nB$  inputs, makes the circuit highly tolerant to slower input rise and fall times.

**FUNCTION TABLE**

INPUTS			OUTPUTS	
$n\bar{R}_D$	$n\bar{A}$	$nB$	$nQ$	$n\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH transition  
 ↓ = HIGH-to-LOW transition  
 = one HIGH level output pulse  
 = one LOW level output pulse



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for  $nR_{EXT}/C_{EXT}$ )

$I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HC

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS/NOTES	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/t_{PLH}$	propagation delay $nA, nB$ to $nQ, nQ$		83 30 24	255 51 43		320 64 54		385 77 65	ns	2.0 4.5 6.0	$C_{EXT} = 0\text{ pF}$ ; $R_{EXT} = 5\text{ k}\Omega$
$t_{PHL}/t_{PLH}$	propagation delay $nR_D$ to $nQ, nQ$		66 24 19	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	$C_{EXT} = 0\text{ pF}$ ; $R_{EXT} = 5\text{ k}\Omega$
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	
$t_W$	trigger pulse width $nA = \text{LOW}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
$t_W$	trigger pulse width $nB = \text{HIGH}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 7
$t_W$	reset pulse width $nR_D = \text{LOW}$	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 8
$t_W$	output pulse width $nQ = \text{HIGH}$ $nQ = \text{LOW}$		450		—		—		$\mu\text{s}$	5.0	$C_{EXT} = 100\text{ nF}$ ; $R_{EXT} = 10\text{ k}\Omega$ ; Figs 7 and 8
$t_W$	output pulse width $nQ = \text{HIGH}$ $nQ = \text{LOW}$		75		—		—		ns	5.0	$C_{EXT} = 0\text{ pF}$ ; $R_{EXT} = 5\text{ k}\Omega$ ; note 1; Figs 7 and 8
$t_{rt}$	retrigger time $nA, nB$		44		—		—		ns	5.0	$C_{EXT} = 0\text{ pF}$ ; $R_{EXT} = 5\text{ k}\Omega$ ; note 2; Fig. 8
$R_{EXT}$	external timing resistor	10 2		1000 1000	—		—		$\text{k}\Omega$	2.0 5.0	Fig. 9
$C_{EXT}$	external timing capacitor	no limits							pF	5.0	Fig. 9; note 3

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard (except for  $nR_{EXT}/C_{EXT}$ )

$I_{CC}$  category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\bar{A}$ , $nB$ $n\bar{R}_D$	0.35 0.35

## AC CHARACTERISTICS FOR 74HCT

$GND = 0 V$ ;  $t_r = t_f = 6 ns$ ;  $C_L = 50 pF$

SYMBOL	PARAMETER	$T_{amb} (°C)$						UNIT	$V_{CC}$ V	TEST CONDITIONS WAVEFORMS/NOTES	
		74HCT									
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $n\bar{A}$ , $nB$ to $n\bar{Q}$ , $nQ$		30	51		64		77	ns	4.5	$C_{EXT} = 0 pF$ ; $R_{EXT} = 5 k\Omega$
$t_{PHL}/t_{PLH}$	propagation delay $n\bar{R}_D$ to $nQ$ , $n\bar{Q}$		26	46		58		69	ns	4.5	$C_{EXT} = 0 pF$ ; $R_{EXT} = 5 k\Omega$
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	
$t_W$	trigger pulse width $n\bar{A} = LOW$	20	7		25		30		ns	4.5	Fig. 7
$t_W$	trigger pulse width $nB = HIGH$	20	7		25		30		ns	4.5	Fig. 7
$t_W$	reset pulse width $n\bar{R}_D = LOW$	20	8		25		30		ns	4.5	Fig. 8
$t_W$	output pulse width $nQ = HIGH$ $n\bar{Q} = LOW$		450		—		—		$\mu s$	5.0	$C_{EXT} = 100 nF$ ; $R_{EXT} = 10 k\Omega$ ; Figs 7 and 8
$t_W$	output pulse width $nQ = HIGH$ $n\bar{Q} = LOW$		75		—		—		ns	5.0	$C_{EXT} = 0 pF$ ; $R_{EXT} = 5 k\Omega$ ; note 1; Figs 7 and 8
$t_{rt}$	retrigger time $n\bar{A}$ , $nB$		75		—		—		ns	5.0	$C_{EXT} = 0 pF$ ; $R_{EXT} = 5 k\Omega$ ; note 2; Fig. 8
$R_{EXT}$	external timing resistor	2		1000	—	—			$k\Omega$	5.0	Fig. 9
$C_{EXT}$	external timing capacitor				no limits				$pF$	5.0	Fig 9; note 3

**Notes to AC characteristics**

1. For other  $R_{EXT}$  and  $C_{EXT}$  combinations see Fig. 9.

If  $C_{EXT} > 10$  nF, the next formula is valid:

$$t_W = K \times R_{EXT} \times C_{EXT} \text{ (typ.)}$$

where,  $t_W$  = output pulse width in ns;

$R_{EXT}$  = external resistor in k $\Omega$ ;  $C_{EXT}$  = external capacitor in pF;

$K$  = constant = 0.45 for  $V_{CC} = 5.0$  V and 0.48 for  $V_{CC} = 2.0$  V.

The inherent test jig and pin capacitance at pins 15 and 7 ( $nR_{EXT}/C_{EXT}$ ) is approximately 7 pF.

2. The time to retrigger the monostable multivibrator depends on the values of  $R_{EXT}$  and  $C_{EXT}$ .

The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time.

If  $C_{EXT} > 10$  nF, the next formula (at  $V_{CC} = 5.0$  V) for the set-up time of a retrigger pulse is valid:

$$t_{rt} = 35 + (0.11 \times C_{EXT}) + (0.04 \times R_{EXT} \times C_{EXT}) \text{ (typ.)}$$

where,  $t_{rt}$  = retrigger time in ns;

$C_{EXT}$  = external capacitor in pF;

$R_{EXT}$  = external resistor in k $\Omega$ .

The inherent test jig and pin capacitance at pins 15 and 7 ( $nR_{EXT}/C_{EXT}$ ) is approximately 7 pF.

3. When the device is powered-up, initiate the device via a reset pulse, when  $C_{EXT} < 50$  pF.

AC WAVEFORMS

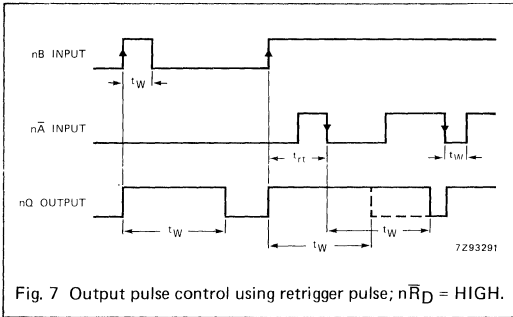


Fig. 7 Output pulse control using retrigger pulse;  $n\bar{R}_D = \text{HIGH}$ .

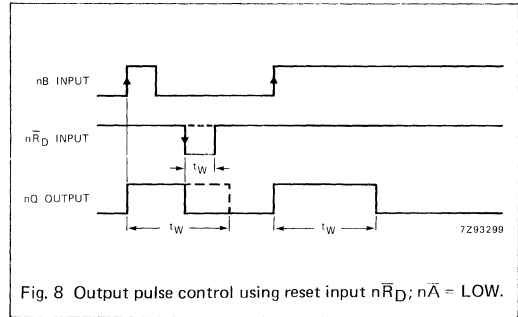


Fig. 8 Output pulse control using reset input  $n\bar{R}_D$ ;  $n\bar{A} = \text{LOW}$ .

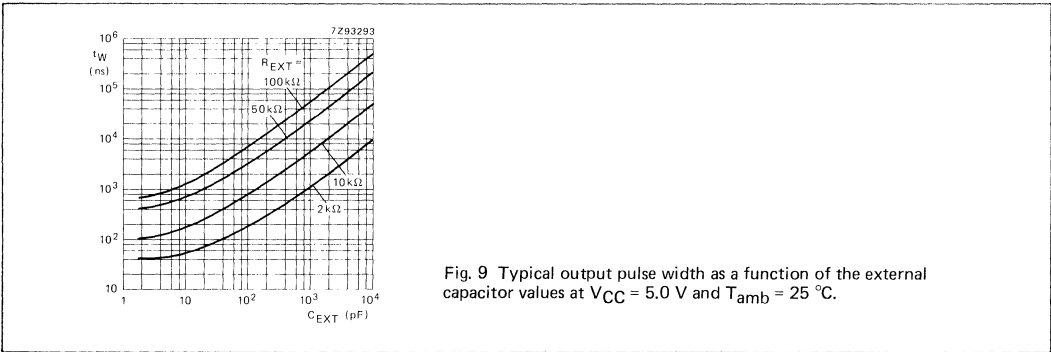


Fig. 9 Typical output pulse width as a function of the external capacitor values at  $V_{CC} = 5.0\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .





OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Common 3-state output enable input
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT533 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\bar{O}E$ ) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When  $\bar{O}E$  is LOW, the contents of the 8 latches are available at the outputs. When  $\bar{O}E$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\bar{O}E$  input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to $\bar{Q}_n$ LE to $\bar{Q}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 17	16 19	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	34	34	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

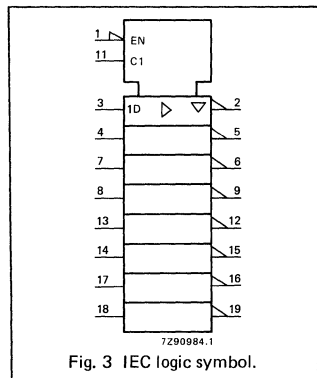
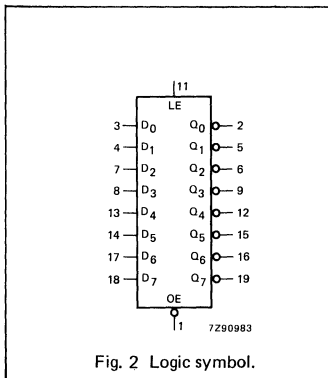
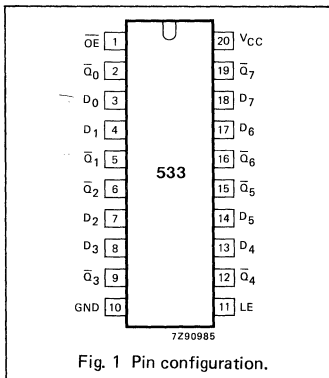
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT533P: 20-lead DIL; plastic (SOT-146).  
PC74HC/HCT533T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{O}E$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\bar{Q}_0$ to $\bar{Q}_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V <sub>CC</sub>	positive supply voltage



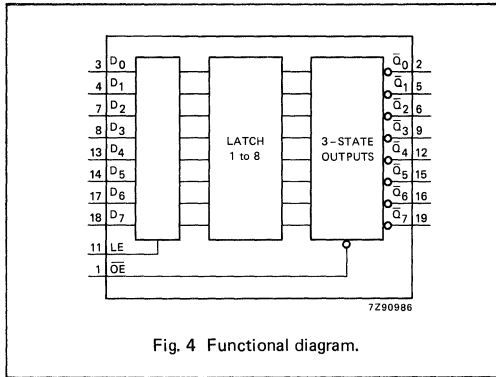


Fig. 4 Functional diagram.

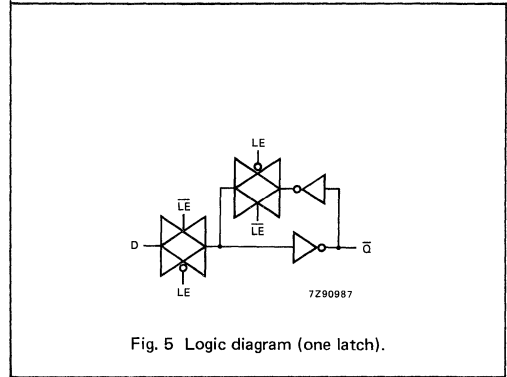


Fig. 5 Logic diagram (one latch).

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS $\bar{Q}_0$ to $\bar{Q}_7$
	$\bar{OE}$	LE	$D_n$		
enable and read register (transparent mode)	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	X	X	X	Z
	H	X	X	X	Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition or the HIGH-to-LOW  $\bar{OE}$  transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition or the HIGH-to-LOW  $\bar{OE}$  transition  
X = don't care  
Z = high impedance OFF-state

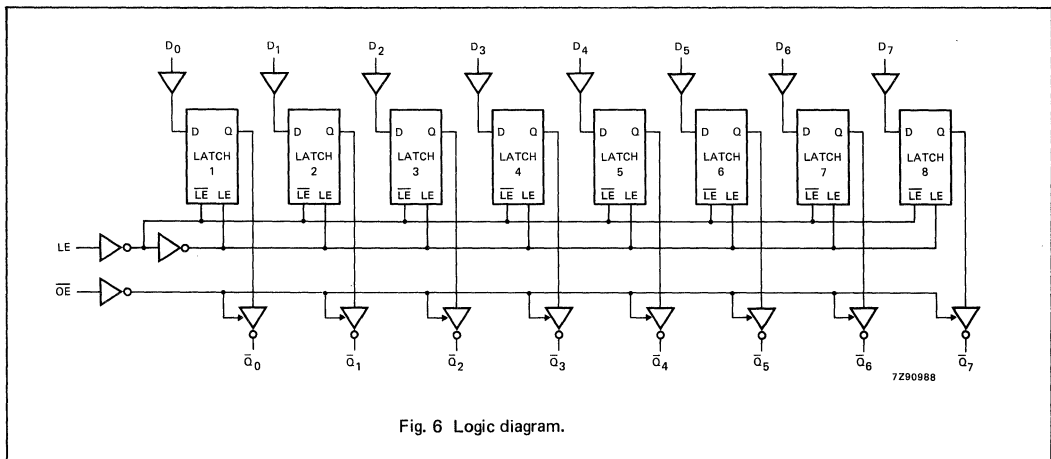


Fig. 6 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to $\bar{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\bar{Q}_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\bar{OE}$ to $\bar{Q}_n$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\bar{OE}$ to $\bar{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	LE pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>h</sub>	hold time D <sub>n</sub> to LE	35 7 6	3 1 1		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 10

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

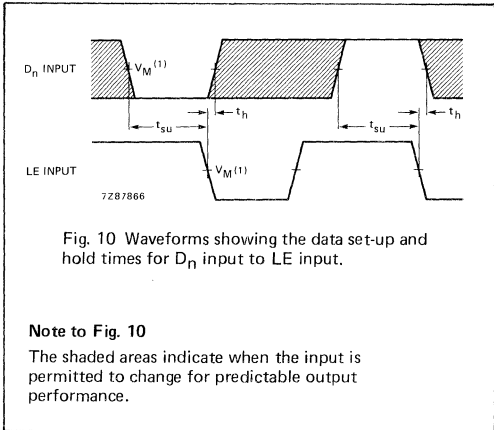
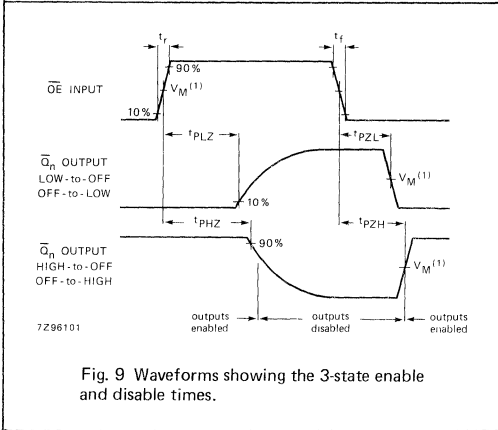
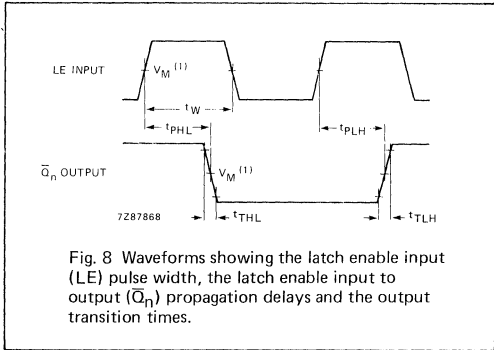
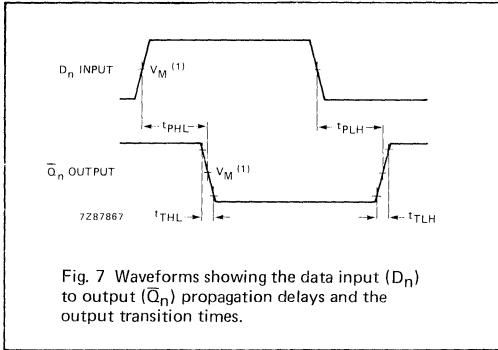
INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.15
LE	0.30
OE	0.55

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		19	34		43		51	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		22	38		48		57	ns	4.5	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		18	35		44		53	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 7
t <sub>W</sub>	LE pulse width HIGH	16	6		20		24		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	10	1		13		15		ns	4.5	Fig. 10
t <sub>h</sub>	hold time D <sub>n</sub> to LE	8	2		10		12		ns	4.5	Fig. 10

AC WAVEFORMS



Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

**OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE; INVERTING**

**FEATURES**

- 3-state inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT534 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops. The "534" is functionally identical to the "374", but has inverted outputs. The "534" consists of eight flip-flops with individual D-type inputs and 3-state inverting outputs. The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{Q}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	12	13	ns
f <sub>max</sub>	maximum clock frequency		61	40	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	19	19	pF

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

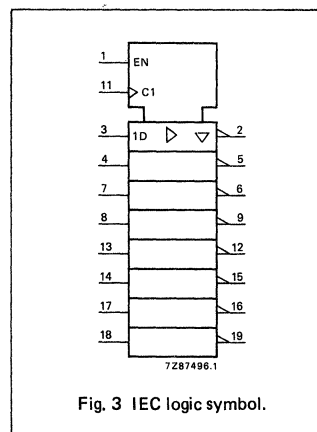
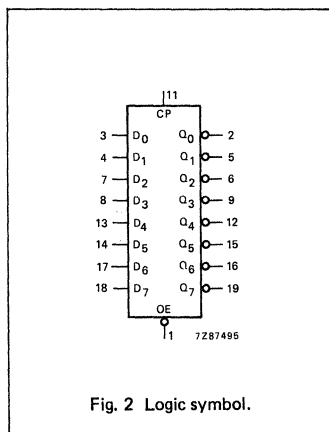
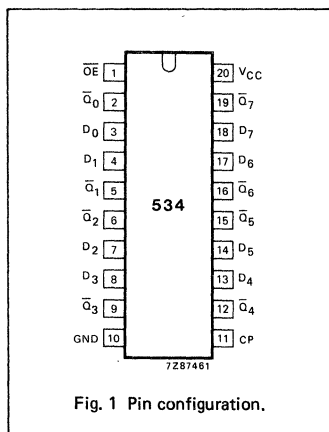
**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT534P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT534T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}_0$ to $\overline{Q}_7$	3-state outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V <sub>CC</sub>	positive supply voltage



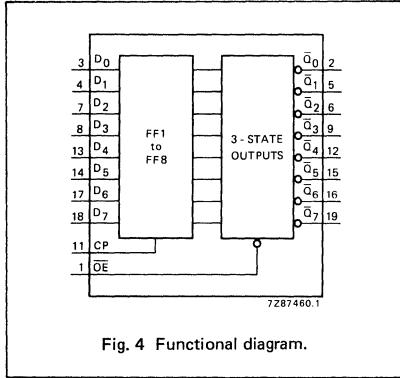


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS $\bar{Q}_0$ to $\bar{Q}_7$
	OE	CP	D <sub>n</sub>		
load and read register	L L	↑ ↑	l h	L H	H L
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state  
↑ = LOW-to-HIGH clock transition

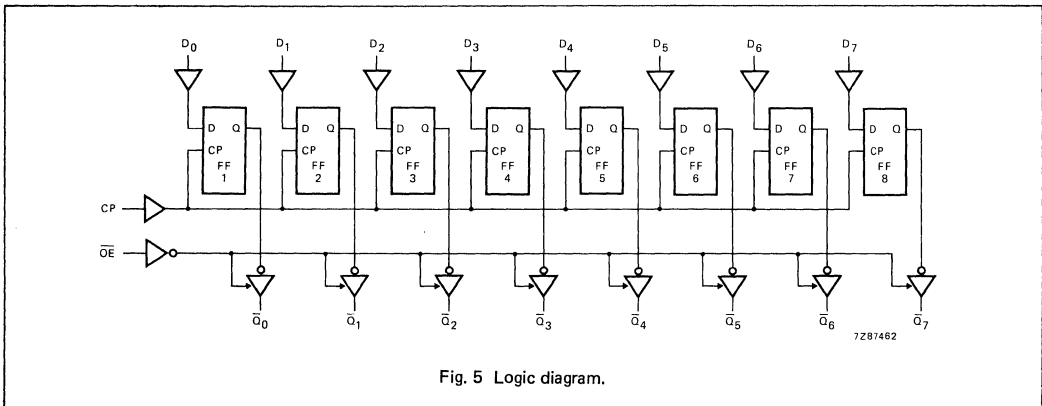


Fig. 5 Logic diagram.



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		41 15 12	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	18 55 66		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$\overline{OE}$	1.25
CP	0.90
D <sub>n</sub>	0.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		16	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	23	14		29		35		ns	4.5	Fig. 6
t <sub>SU</sub>	set-up time D <sub>n</sub> to CP	12	4		15		18		ns	4.5	Fig. 8
t <sub>H</sub>	hold time D <sub>n</sub> to CP	3	-2		3		3		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	22	36		18		15		MHz	4.5	Fig. 6

AC WAVEFORMS

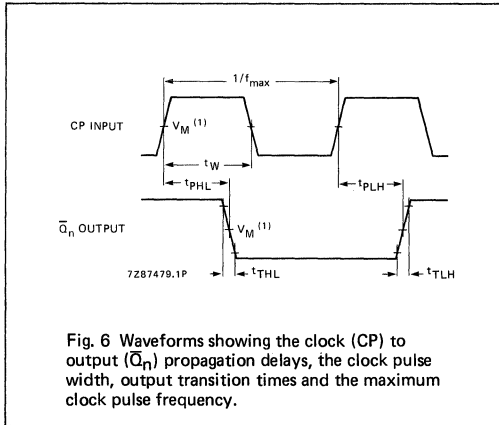


Fig. 6 Waveforms showing the clock (CP) to output ( $\bar{Q}_n$ ) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

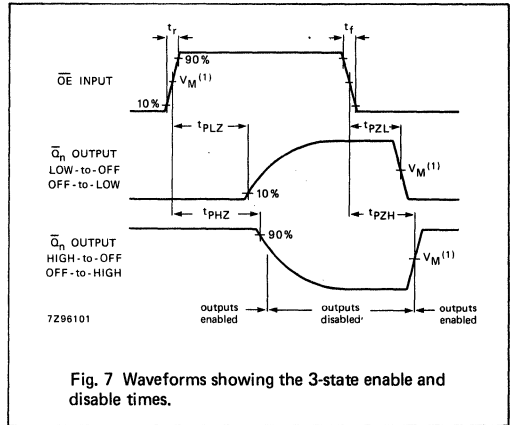


Fig. 7 Waveforms showing the 3-state enable and disable times.

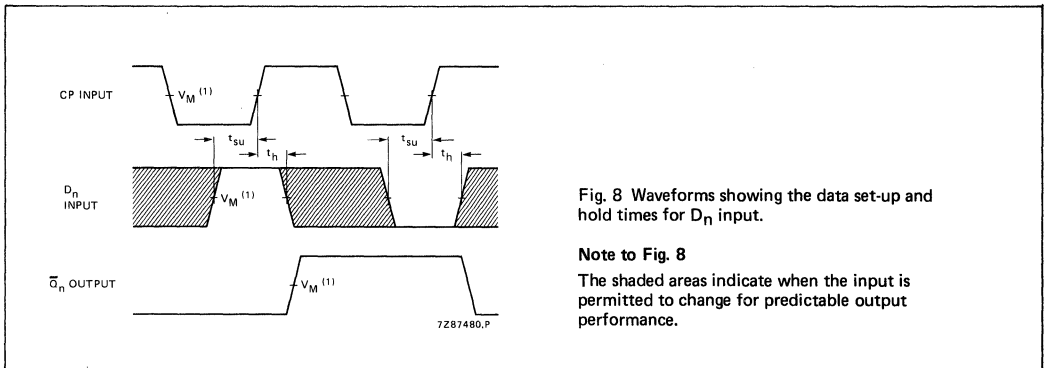


Fig. 8 Waveforms showing the data set-up and hold times for  $D_n$  input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT540  
MSI

## OCTAL BUFFER/LINE DRIVER; 3-STATE; INVERTING

### FEATURES

- Inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT540 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT540 are octal inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{OE}_1$  and  $\overline{OE}_2$ . A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The "540" is identical to the "541" but has inverting outputs.

### FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	A <sub>n</sub>	$\overline{Y}_n$
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\overline{Y}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

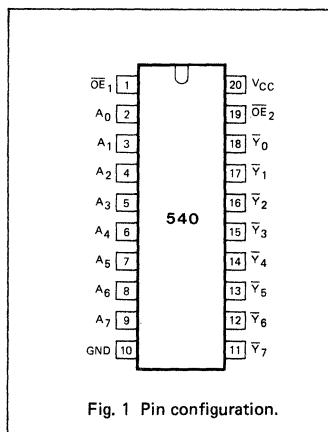
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT540P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT540T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y}_0$ to $\overline{Y}_7$	bus outputs
20	V <sub>CC</sub>	positive supply voltage



OCTAL BUFFER/LINE DRIVER; 3-STATE

FEATURES

- Non-inverting outputs
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT541 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT541 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{OE}_1$  and  $\overline{OE}_2$ .

A HIGH on  $\overline{OE}_n$  causes the outputs to assume a high impedance OFF-state.

The "541" is identical to the "540" but has non-inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	$A_n$	$Y_n$
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $Y_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	10	ns
$C_I$	input capacitance		3.5	3.5	pF

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT541P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT541T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	$A_0$ to $A_7$	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$Y_0$ to $Y_7$	bus outputs
20	$V_{CC}$	positive supply voltage

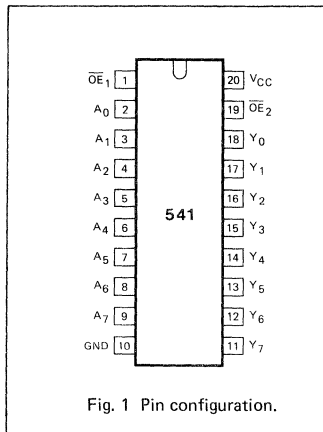


Fig. 1 Pin configuration.

## OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE; INVERTING

### FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and  $\overline{OE}$  are common to all latches.

When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> , LE to $\overline{Q}_n$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	16	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT563P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT563T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D <sub>0</sub> to D <sub>7</sub>	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
20	V <sub>CC</sub>	positive supply voltage

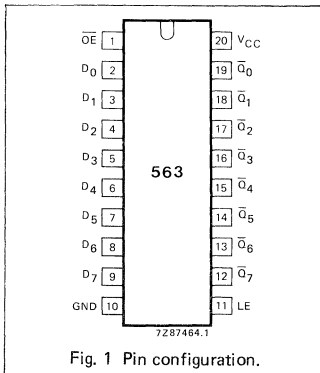


Fig. 1 Pin configuration.

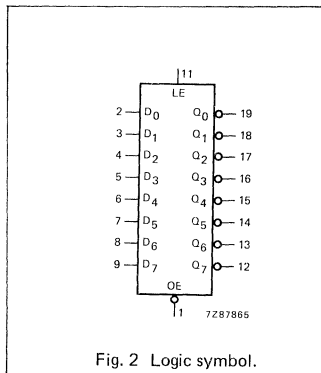


Fig. 2 Logic symbol.

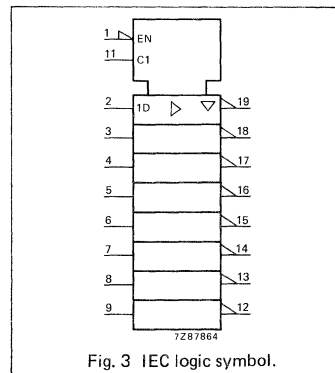


Fig. 3 IEC logic symbol.

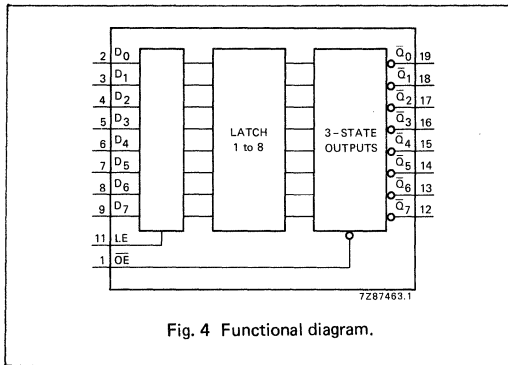


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS Q <sub>0</sub> to Q <sub>7</sub>
	OE	LE	D <sub>n</sub>		
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	H	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition

L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition

Z = high impedance OFF-state

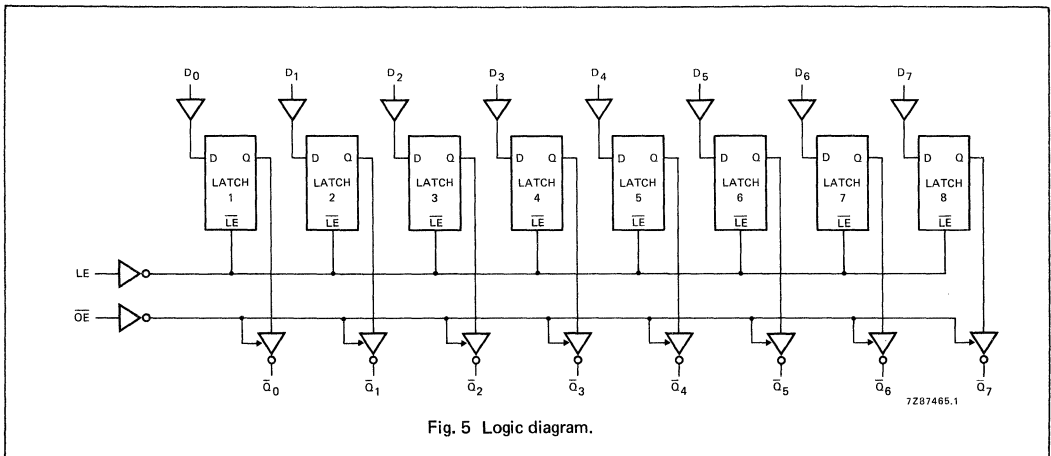


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $D_n$ to $\bar{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ $t_{PLH}$	propagation delay LE to $\bar{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
$t_{pZH}/$ $t_{pZL}$	3-state output enable time $\bar{OE}$ to $\bar{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
$t_{pHZ}/$ $t_{pLZ}$	3-state output disable time $\bar{OE}$ to $\bar{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
$t_{THL}/$ $t_{TLH}$	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
$t_W$	enable pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
$t_{su}$	set-up time $D_n$ to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
$t_h$	hold time $D_n$ to LE	4 4 4	-6 -2 -2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig. 9



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

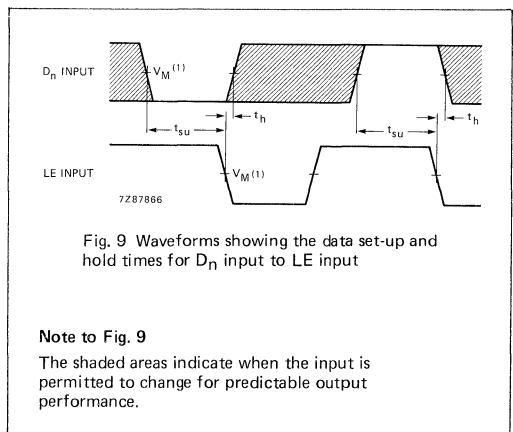
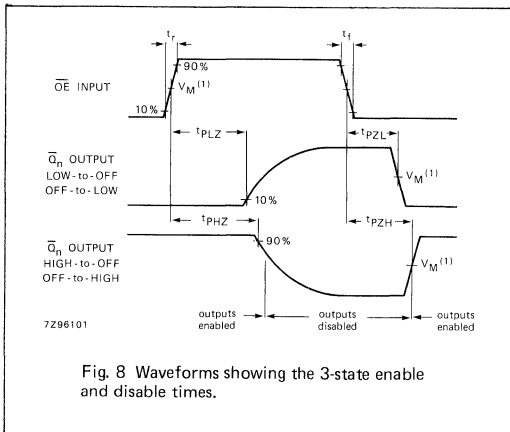
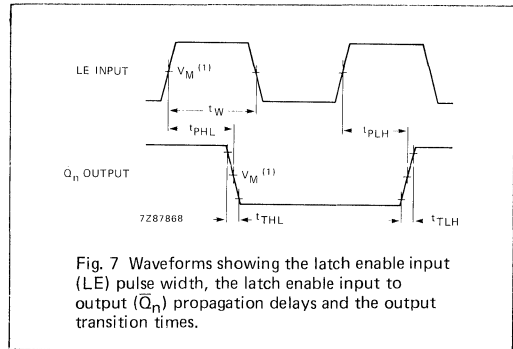
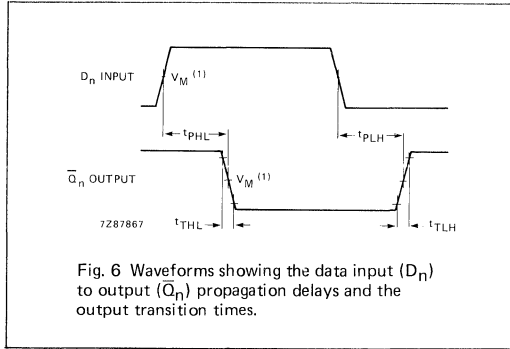
input	unit load coefficient
D <sub>n</sub>	0.35
LE	0.65
OE	1.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to $\bar{Q}_n$		18	30		38		45	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\bar{Q}_n$		19	35		44		53	ns	4.5	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\bar{OE}$ to $\bar{Q}_n$		20	35		44		53	ns	4.5	Fig. 8
t <sub>PZH</sub> / t <sub>PLZ</sub>	3-state output disable time $\bar{OE}$ to $\bar{Q}_n$		22	35		44		53	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	10	3		13		15		ns	4.5	Fig. 9
t <sub>h</sub>	hold time D <sub>n</sub> to LE	5	-1		5		5		ns	4.5	Fig. 9

AC WAVEFORMS



Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

**OCTAL D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE; INVERTING**

**FEATURES**

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I<sup>2</sup>C category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574", but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $\overline{Q}_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15	16	ns
$f_{max}$	maximum clock frequency		115	62	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	27	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz                       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz                       $V_{CC}$  = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT564P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT564T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state flip-flop outputs
20	$V_{CC}$	positive supply voltage

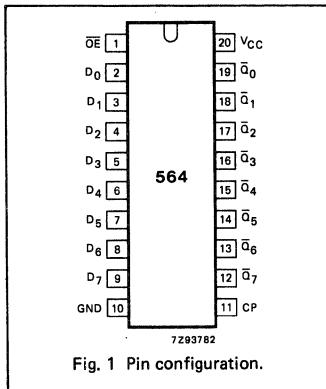


Fig. 1 Pin configuration.

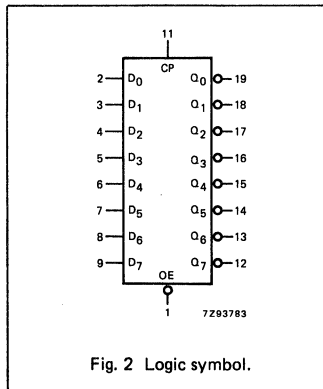


Fig. 2 Logic symbol.

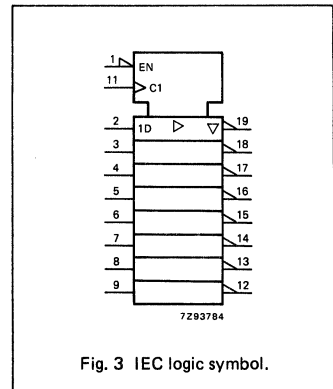


Fig. 3 IEC logic symbol.

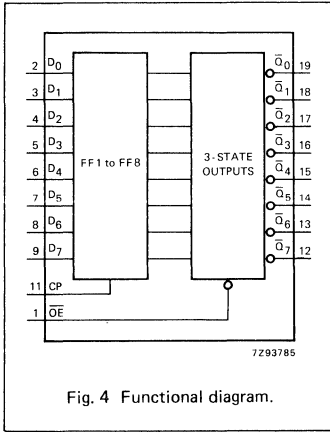


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{Q\bar{E}}$	CP	$D_n$		$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	L	H
	L	↑	h	H	L
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 Z = high impedance OFF-state  
 ↑ = LOW-to-HIGH clock transition

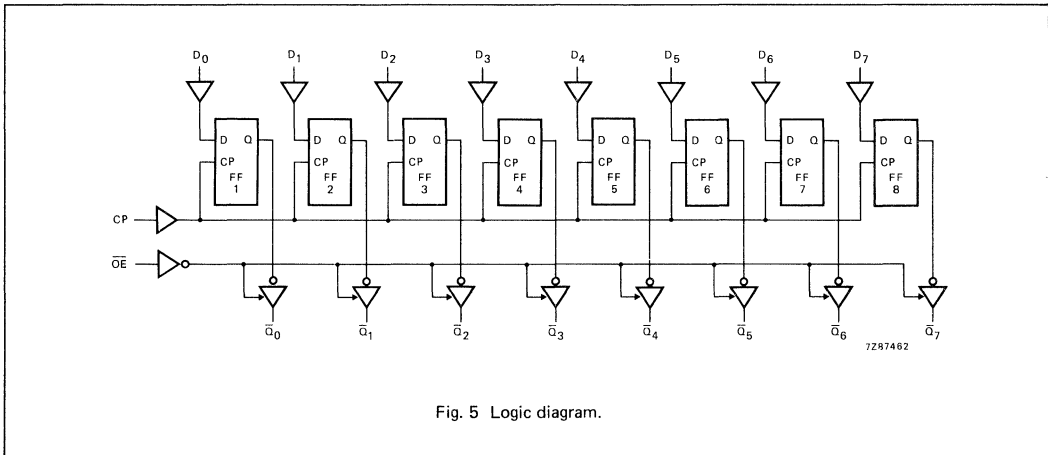


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\bar{Q}_n$		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\bar{O}E$ to $\bar{Q}_n$		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\bar{O}E$ to $\bar{Q}_n$		50 18 14	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	38 105 125		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	0.80
D <sub>0</sub> to D <sub>7</sub>	0.25
CP	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		19	30		38		45	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	18	8		23		27		ns	4.5	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	3		15		18		ns	4.5	Fig. 7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3	-2		3		3		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	27	56		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

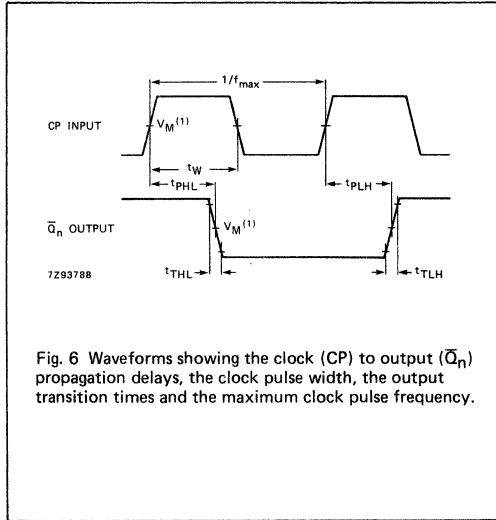


Fig. 6 Waveforms showing the clock (CP) to output ( $\bar{Q}_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

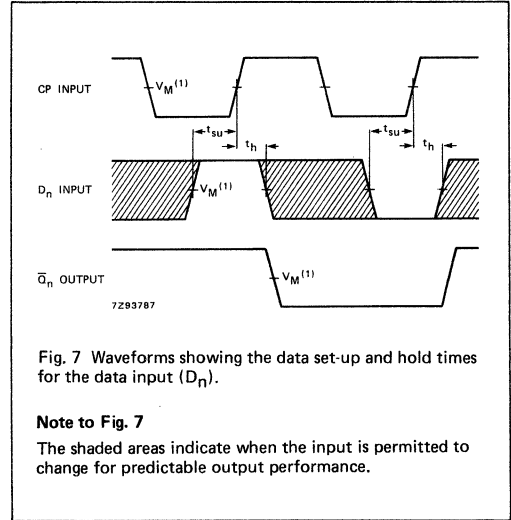


Fig. 7 Waveforms showing the data set-up and hold times for the data input ( $D_n$ ).

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

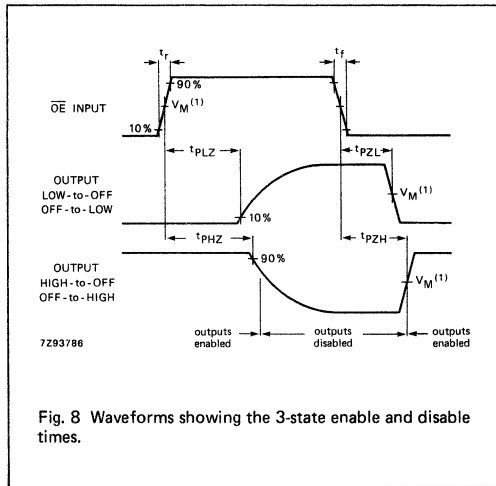


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## OCTAL D-TYPE TRANSPARENT LATCH; 3-STATE

### FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches. *(continued on next page)*

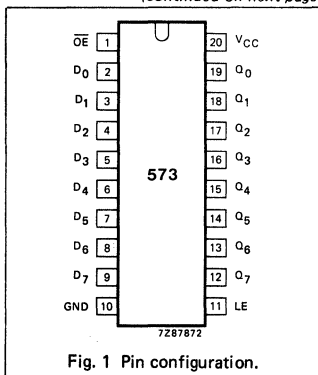


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub> LE to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 15	17 15	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	26	26	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT573P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT573T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D <sub>0</sub> to D <sub>7</sub>	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q <sub>0</sub> to Q <sub>7</sub>	3-state latch outputs
20	V <sub>CC</sub>	positive supply voltage

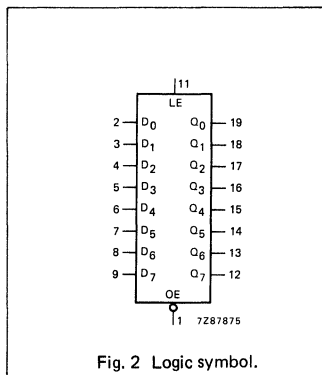


Fig. 2 Logic symbol.

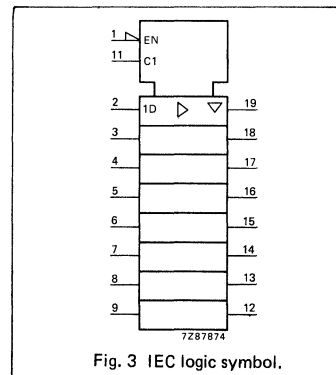


Fig. 3 IEC logic symbol.



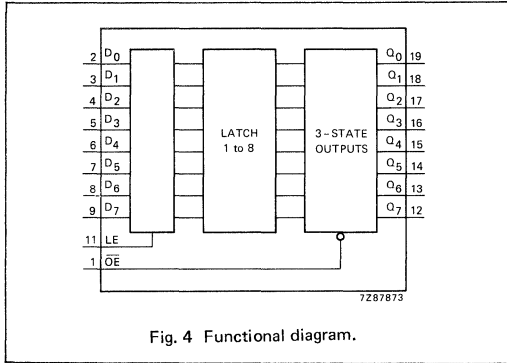


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd.)**

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

**FUNCTION TABLE**

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS Q <sub>0</sub> to Q <sub>7</sub>
	$\overline{OE}$	LE	D <sub>n</sub>		
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	L	l	L	L
	L	L	h	H	H
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

Z = high impedance OFF-state

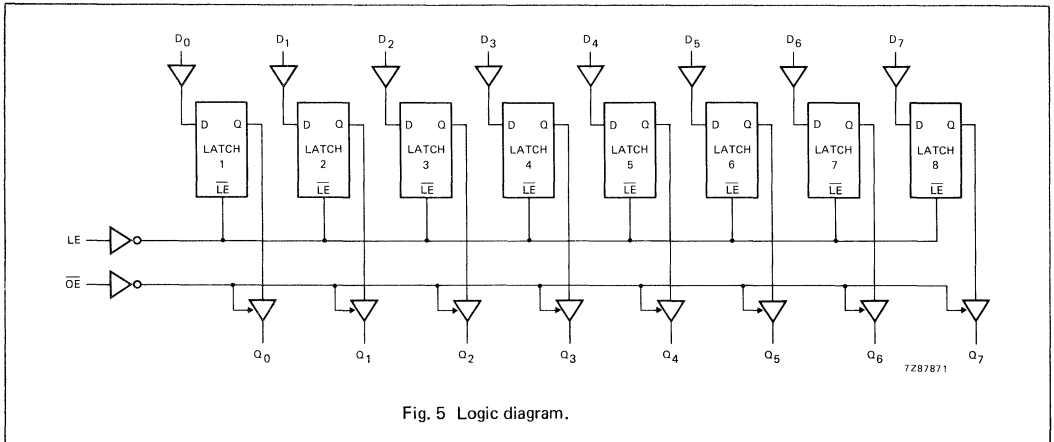


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 9
t <sub>h</sub>	hold time D <sub>n</sub> to LE	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 9

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
D <sub>n</sub>	0.35
LE	0.65
OE	1.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		20	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		18	35		44		53	ns	4.5	Fig. 7
t <sub>pZH</sub> / t <sub>pZL</sub>	3-state output enable time OE to Q <sub>n</sub>		17	30		38		45	ns	4.5	Fig. 8
t <sub>pHZ</sub> / t <sub>pLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>w</sub>	enable pulse width HIGH	16	6		20		24		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	13	7		16		20		ns	4.5	Fig. 9
t <sub>h</sub>	hold time D <sub>n</sub> to LE	9	4		11		14		ns	4.5	Fig. 9

AC WAVEFORMS

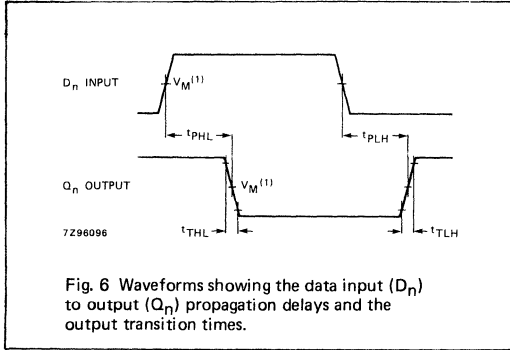


Fig. 6 Waveforms showing the data input ( $D_n$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

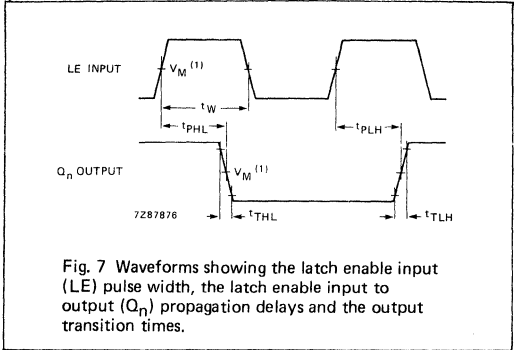


Fig. 7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ( $Q_n$ ) propagation delays and the output transition times.

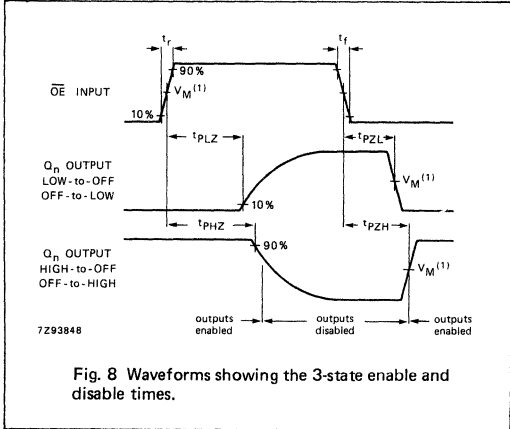
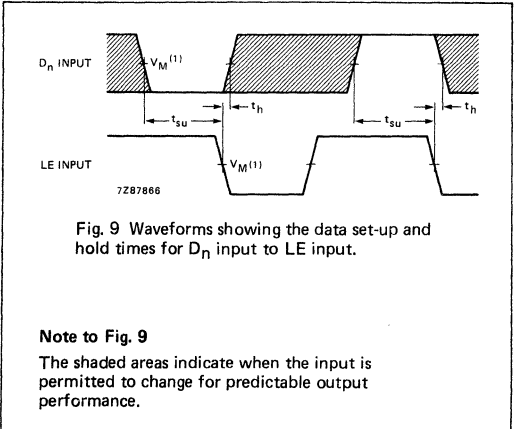


Fig. 8 Waveforms showing the 3-state enable and disable times.



Note to Fig. 9  
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE-TRIGGER; 3-STATE

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT574 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The "574" is functionally identical to the "564", but has non-inverting outputs. The "574" is functionally identical to the "374", but has a different pinning.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	12	14	ns
$f_{max}$	maximum clock frequency		60	60	MHz
$C_i$	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	35	40	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT574P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT574T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	$D_0$ to $D_7$	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	$Q_0$ to $Q_7$	3-state flip-flop outputs
20	$V_{CC}$	positive supply voltage

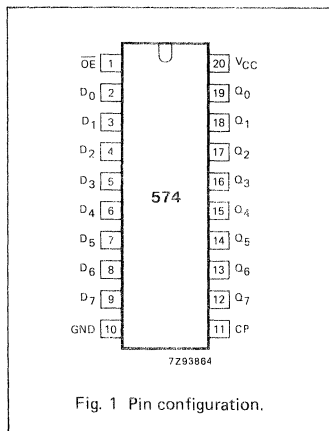


Fig. 1 Pin configuration.

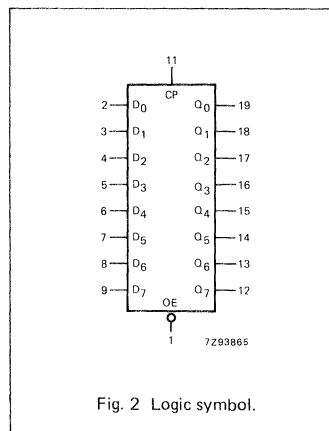


Fig. 2 Logic symbol.

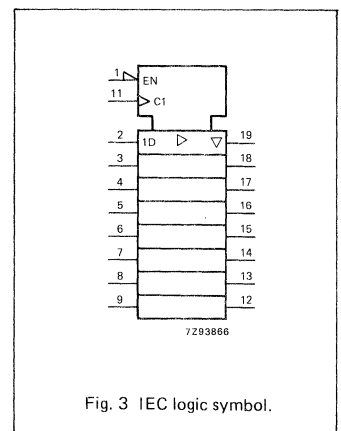


Fig. 3 IEC logic symbol.

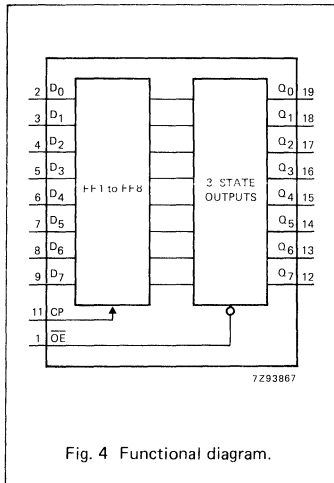


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	$D_n$		$Q_0$ to $Q_7$
load and read register	L	$\uparrow$	l	L	H
	L	$\uparrow$	h	H	L
load register and disable outputs	H	$\uparrow$	l	L	Z
	H	$\uparrow$	h	H	Z

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 Z = high impedance OFF-state  
 $\uparrow$  = LOW-to-HIGH clock transition

DEVELOPMENT DATA

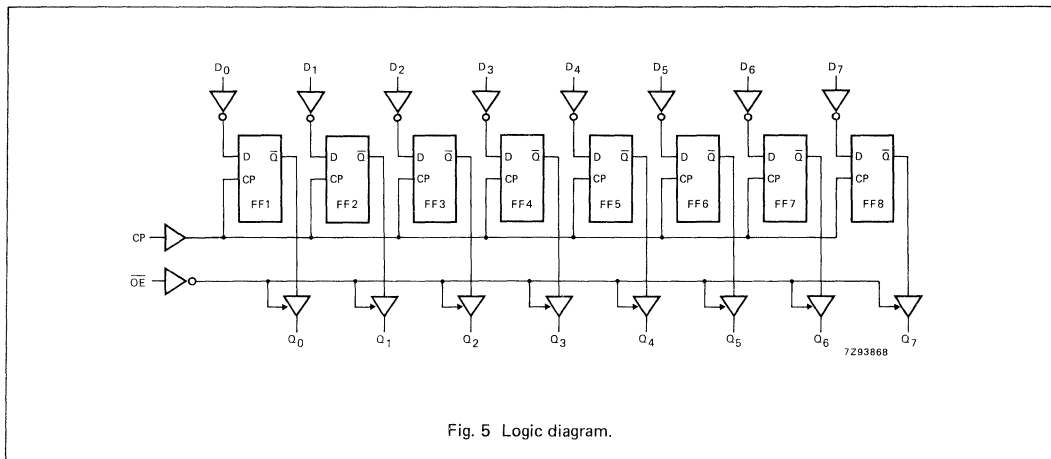


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>			150 30 26		190 35 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6 30 35			5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.5
OE	1.25
CP	1.5

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>			35		44		53	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>			35		44		53	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>			30		38		45	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16			20			24	ns	4.5	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12			15			18	ns	4.5	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5			5			5	ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	30			24			20	MHz	4.5	Fig. 6



AC WAVEFORMS

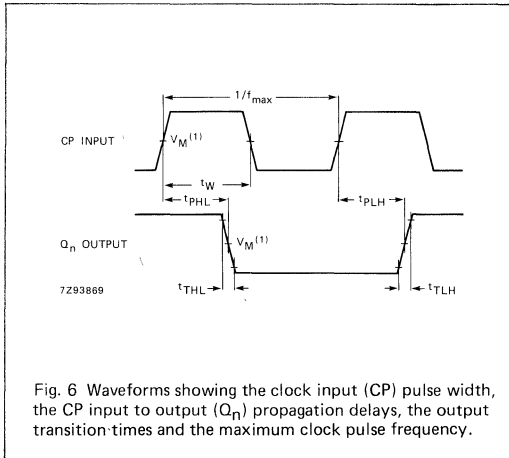


Fig. 6 Waveforms showing the clock input (CP) pulse width, the CP input to output (Q<sub>n</sub>) propagation delays, the output transition times and the maximum clock pulse frequency.

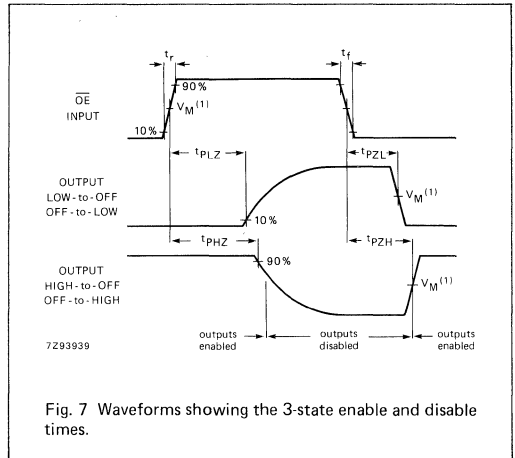


Fig. 7 Waveforms showing the 3-state enable and disable times.

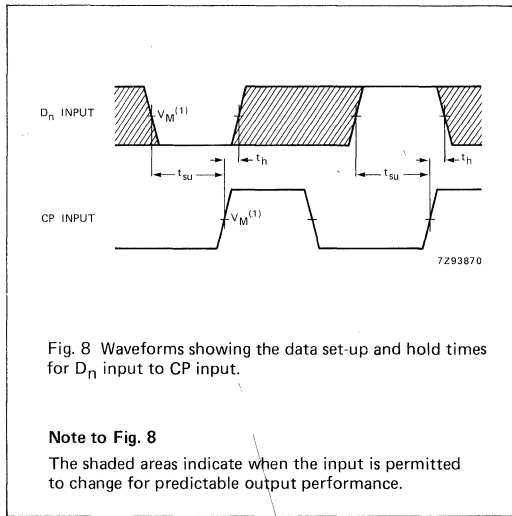


Fig. 8 Waveforms showing the data set-up and hold times for D<sub>n</sub> input to CP input.

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V<sub>M</sub> = 50%; V<sub>1</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>1</sub> = GND to 3 V.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT583  
MSI

## 4-BIT FULL ADDER WITH FAST CARRY

### FEATURES

- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT583 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT583 are high-speed 4-bit BCD full adders with internal carry look-ahead. They accept two 4-bit decimal numbers ( $A_0$  to  $A_3$  and  $B_0$  to  $B_3$ ) and a carry input ( $C_{IN}$ ).

The "583" generates the decimal sum outputs ( $\Sigma_0$  to  $\Sigma_3$ ) and a carry output ( $C_{n+4}$ ) if the sum is greater than 9. See the "283" for the binary version.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}$ / $t_{PLH}$	propagation delay $A_n, B_n, C_{IN}$ to $\Sigma_n$ $C_{IN}$ to $C_{n+4}$ $A_n, B_n$ to $C_{n+4}$	$C_L = 15$ pF $V_{CC} = 5$ V	17 10 12	21 14 17	ns ns ns
$C_I$	input capacitance		3.5	3.5	pF

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns

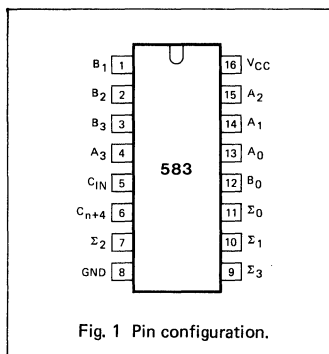
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT583P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT583T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5	$C_{IN}$	carry input
6	$C_{n+4}$	carry output
8	GND	ground (0 V)
11, 10, 7, 9	$\Sigma_0$ to $\Sigma_3$	sum outputs
12, 1, 2, 3	$B_0$ to $B_3$	B operand inputs
13, 14, 15, 4	$A_0$ to $A_3$	A operand inputs
16	$V_{CC}$	positive supply voltage



8-BIT SHIFT REGISTER WITH INPUT FLIP-FLOPS

FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
f <sub>max</sub>	maximum clock frequency		50	45	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT597P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT597T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH <sub>CP</sub>	shift clock input (LOW-to-HIGH, edge-triggered)
12	ST <sub>CP</sub>	storage clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	parallel load input (active LOW)
14	D <sub>s</sub>	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
16	V <sub>CC</sub>	positive supply voltage

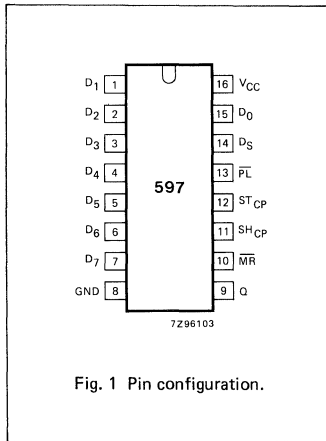


Fig. 1 Pin configuration.

FUNCTION TABLE

ST <sub>CP</sub>	SH <sub>CP</sub>	$\overline{PL}$	$\overline{MR}$	FUNCTION
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Q <sub>n</sub> = Q <sub>n-1</sub> , Q <sub>0</sub> = D <sub>s</sub>

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH CP transition

## 8-BIT SHIFT REGISTER WITH INPUT LATCHES

### FEATURES

- 8-bit parallel input latches
- Shift register has direct overriding load and clear
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT7597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LS TTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7597 both consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register.

When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs, a set-up time preceding the HIGH-to-LOW transition of LE.

The shift register has a positive edge-triggered clock, direct load (from storage) and clear inputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	17	ns
	LE to Q		22	27	ns
	$\overline{PL}$ to Q		20	23	ns
	D <sub>7</sub> to Q		20	24	ns
f <sub>max</sub>	maximum clock frequency SH <sub>CP</sub>		99	79	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package		29	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT7597P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT7597T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous reset input (active LOW)
11	SH <sub>CP</sub>	shift clock input (LOW-to-HIGH, edge-triggered)
12	LE	latch enable input (active HIGH)
13	$\overline{PL}$	parallel load input (active LOW)
14	D <sub>S</sub>	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
16	V <sub>CC</sub>	positive supply voltage

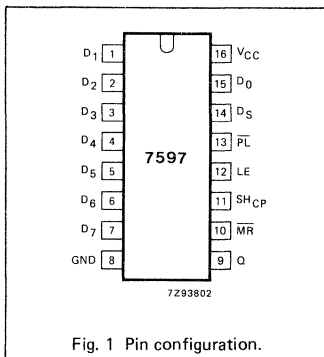


Fig. 1 Pin configuration.

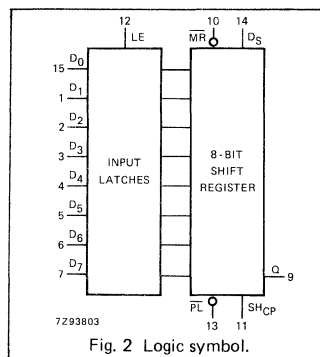


Fig. 2 Logic symbol.

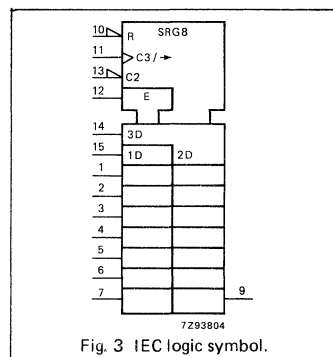


Fig. 3 IEC logic symbol.

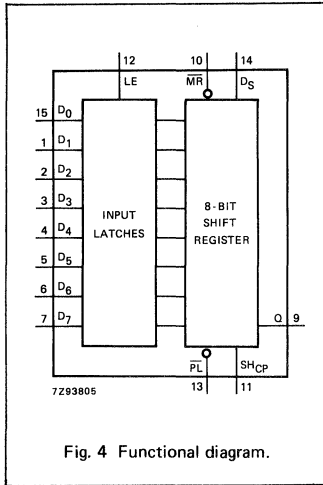
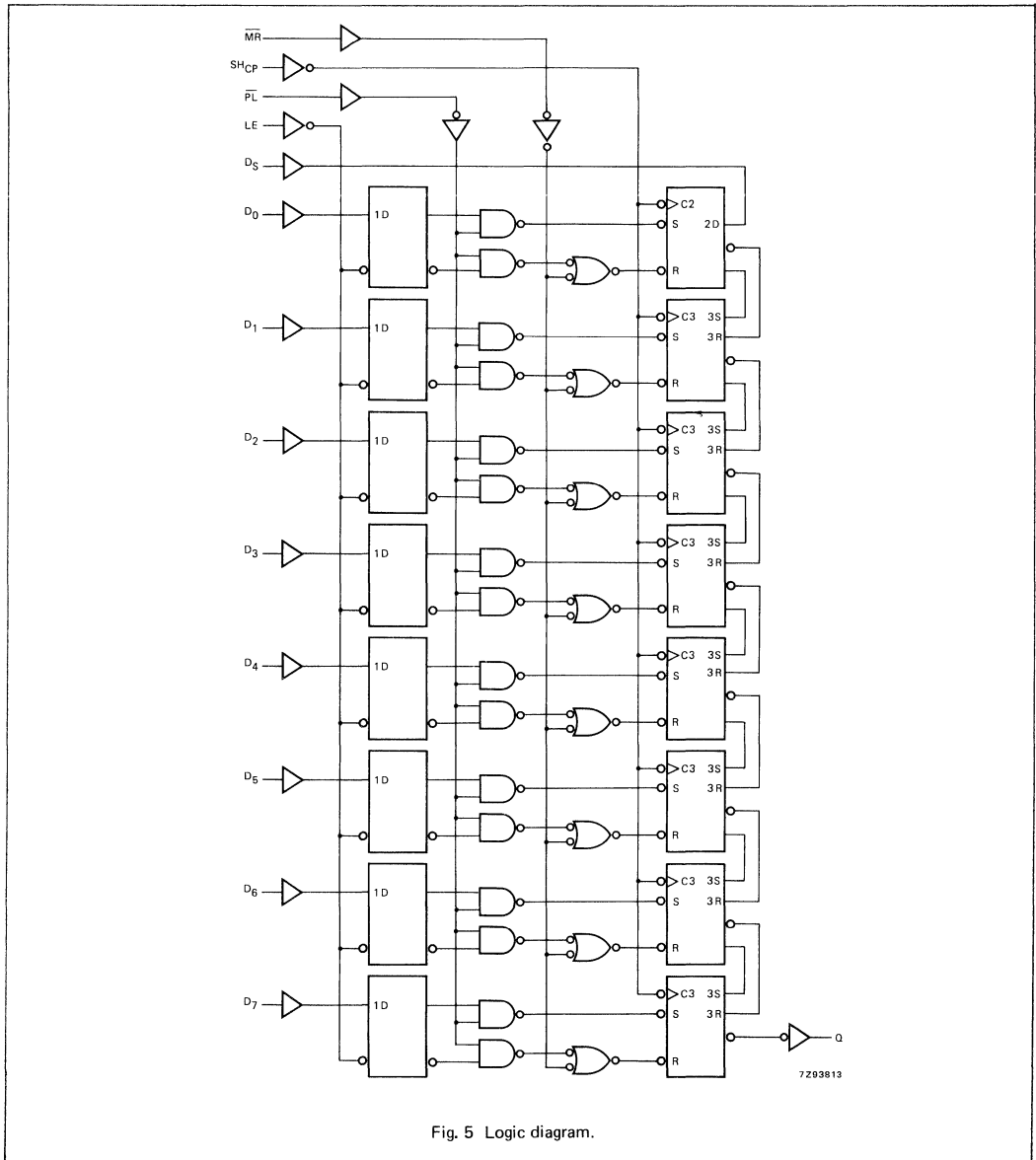


Fig. 4 Functional diagram.

**FUNCTION TABLE**

LE	SH <sub>CP</sub>	$\overline{PL}$	$\overline{MR}$	FUNCTION
H	X	X	X	data loaded to input latches
H	X	L	H	data loaded from inputs to shift register
L	X	L	H	stored data loaded to shift register
X	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$ , $Q_0 = D_S$

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH CP transition



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q		72 26 21	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	SH <sub>CP</sub> pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	LE pulse width HIGH	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	MR pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	PL pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to SH <sub>CP</sub>	50 10 9	-3 -1 -1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 11
t <sub>rem</sub>	removal time MR to PL	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	80 16 14	6 2 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t <sub>su</sub>	set-up time D <sub>S</sub> to SH <sub>CP</sub>	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
t <sub>su</sub>	set-up time LE, PL to SH <sub>CP</sub>	80 16 14	8 3 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	

## AC CHARACTERISTICS FOR 74HC (Continued)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.			
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4 4 4	-3 -1 -1		4 4 4		4 4 4	ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time D <sub>S</sub> to SH <sub>CP</sub>	2 2 2	-8 -3 -2		2 2 2		2 2 2	ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time LE, PL to SH <sub>CP</sub>	2 2 2	-8 -3 -2		2 2 2		2 2 2	ns	2.0 4.5 6.0	
f <sub>max</sub>	maximum pulse frequency SH <sub>CP</sub>	6.0 30 35	30 90 107		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>S</sub>	0.25
D <sub>n</sub>	0.40
PL, MR, LE, SH <sub>CP</sub>	1.50



AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q		20	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q		25	42		53		63	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q		31	53		66		80	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q		27	46		58		69	ns	4.5	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q		28	49		61		74	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 9
t <sub>W</sub>	SH <sub>CP</sub> pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	LE pulse width HIGH	16	7		20		24		ns	4.5	Fig. 8
t <sub>W</sub>	MR pulse width LOW	20	11		25		30		ns	4.5	Fig. 7
t <sub>W</sub>	PL pulse width LOW	18	9		23		27		ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to SH <sub>CP</sub>	10	-1		13		15		ns	4.5	Fig. 11
t <sub>rem</sub>	removal time MR to PL	20	9		25		30		ns	4.5	
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	16	5		20		24		ns	4.5	Fig. 12
t <sub>su</sub>	set-up time D <sub>S</sub> to SH <sub>CP</sub>	16	5		20		24		ns	4.5	Fig. 12
t <sub>su</sub>	set-up time LE, PL to SH <sub>CP</sub>	16	3		20		24		ns	4.5	
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4	-2		4		4		ns	4.5	Fig. 12
t <sub>h</sub>	hold time D <sub>S</sub> to SH <sub>CP</sub>	2	-4		2		2		ns	4.5	Fig. 12
t <sub>h</sub>	hold time LE, PL to SH <sub>CP</sub>	2	-3		2		2		ns	4.5	
f <sub>max</sub>	maximum pulse frequency SH <sub>CP</sub>	30	72		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

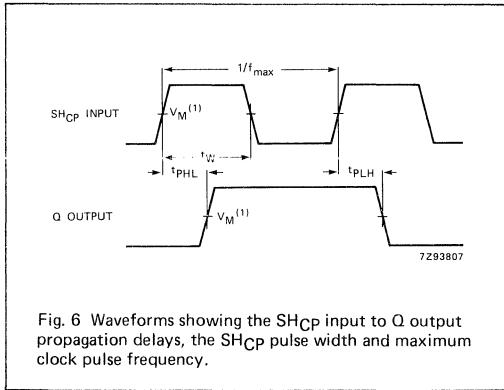


Fig. 6 Waveforms showing the SH<sub>Cp</sub> input to Q output propagation delays, the SH<sub>Cp</sub> pulse width and maximum clock pulse frequency.

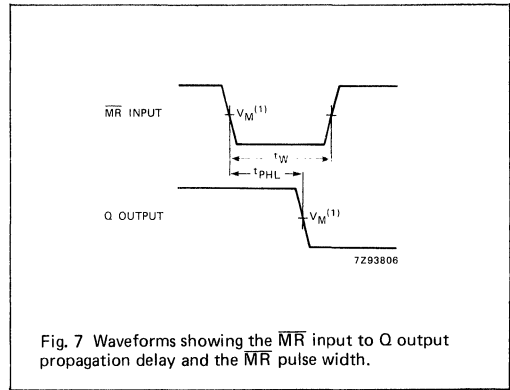


Fig. 7 Waveforms showing the MR input to Q output propagation delay and the MR pulse width.

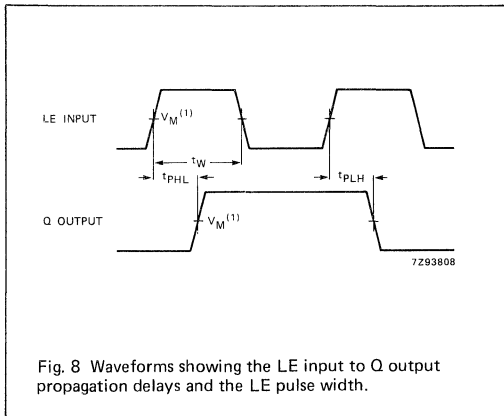


Fig. 8 Waveforms showing the LE input to Q output propagation delays and the LE pulse width.

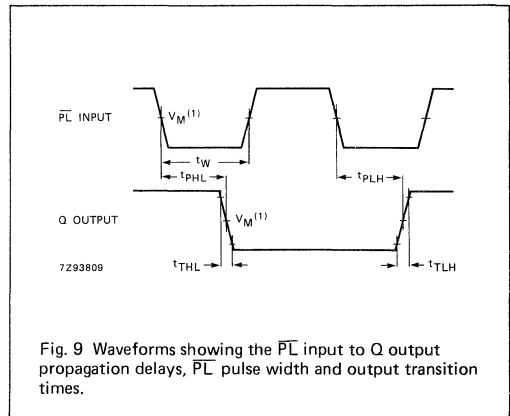


Fig. 9 Waveforms showing the PL input to Q output propagation delays, PL pulse width and output transition times.

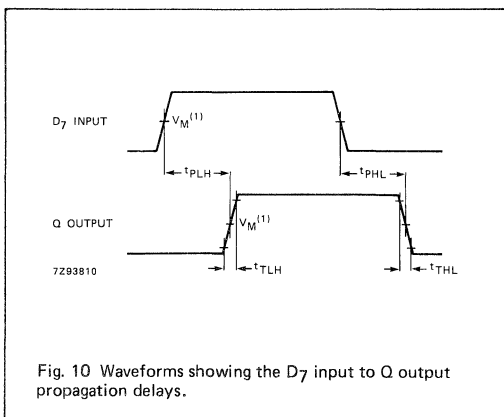


Fig. 10 Waveforms showing the D<sub>7</sub> input to Q output propagation delays.

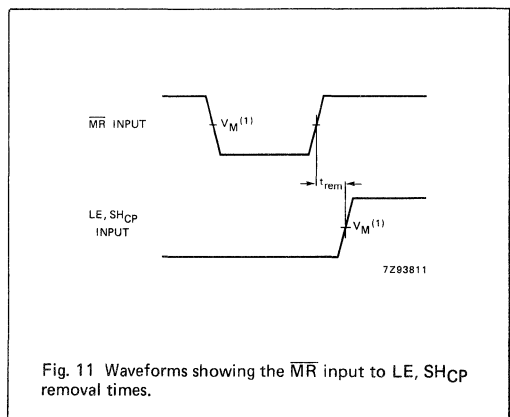


Fig. 11 Waveforms showing the MR input to LE, SH<sub>Cp</sub> removal times.

AC WAVEFORMS (Continued)

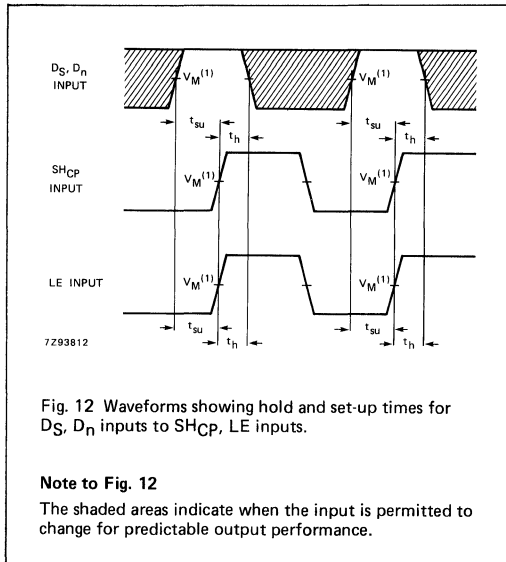


Fig. 12 Waveforms showing hold and set-up times for  $D_S, D_n$  inputs to  $SH_{CP}, LE$  inputs.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
 HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

**OCTAL BUS TRANSCEIVER; 3-STATE; INVERTING**

**FEATURES**

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated.

The "640" is similar to the "245" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	9	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT640P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT640T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

**PIN DESCRIPTION (see next page)**

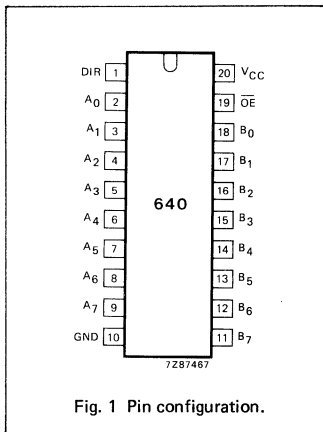


Fig. 1 Pin configuration.

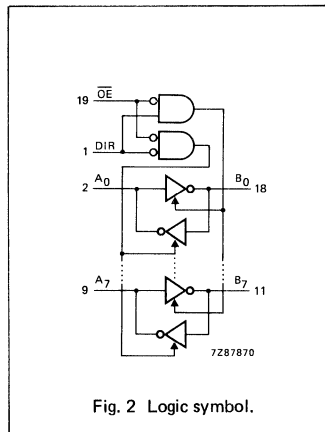


Fig. 2 Logic symbol.

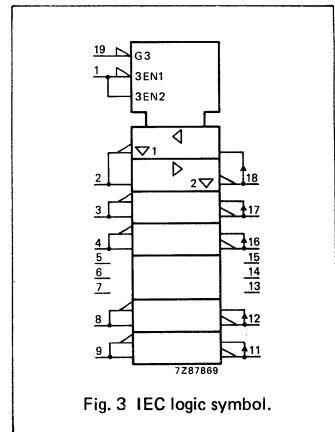


Fig. 3 IEC logic symbol.

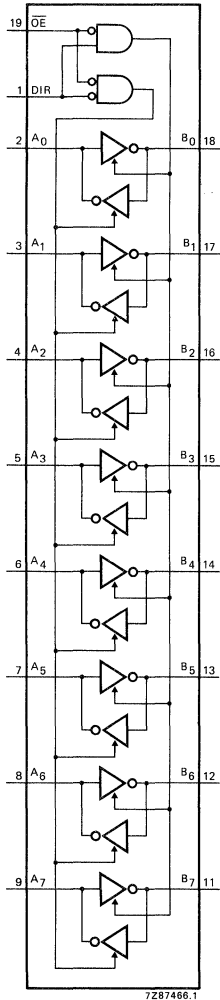


Fig. 4 Functional diagram.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage

**FUNCTION TABLE**

inputs		inputs/outputs	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A = $\overline{B}$	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 5

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

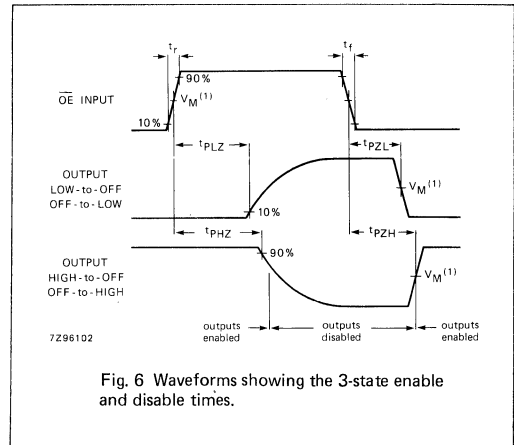
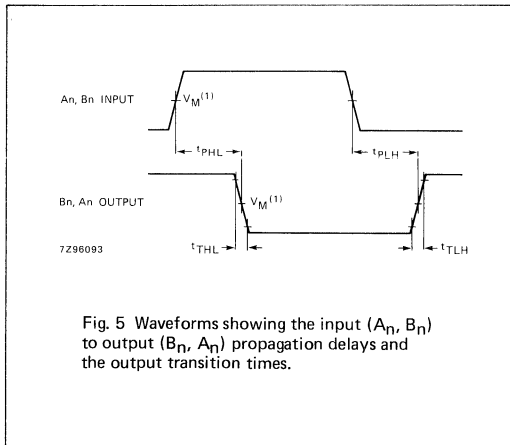
input	unit load coefficient
A <sub>n</sub>	1.50
B <sub>n</sub>	1.50
OE	1.50
DIR	0.90

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		11	22		28		33	ns	4.5	Fig. 5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>		18	30		38		45	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLL</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 5

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



OCTAL BUS TRANSCEIVER; 3-STATE; TRUE/INVERTING

FEATURES

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A <sub>n</sub>	B <sub>n</sub>
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; inverting B <sub>n</sub> to A <sub>n</sub> ; true	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7 8	8 11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

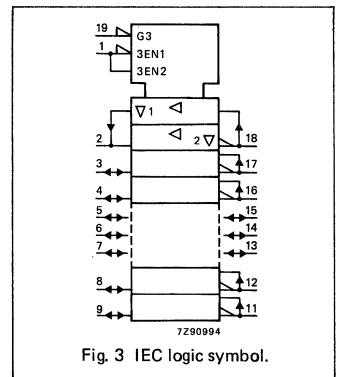
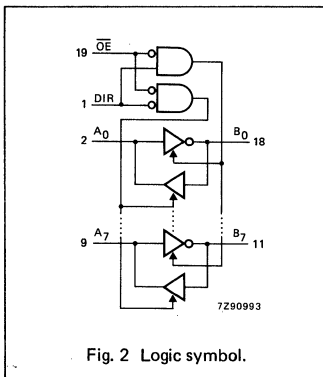
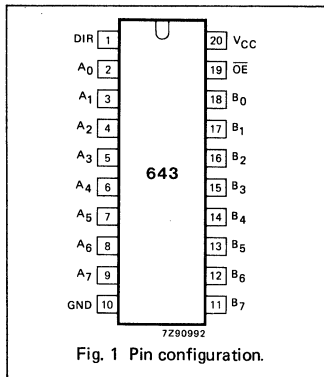
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT643P: 20-lead DIL; plastic (SOT-146).  
PC74HC/HCT643T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage



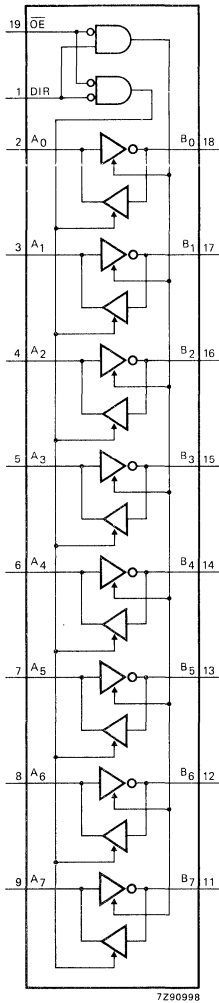


Fig. 4 Functional diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; inverting		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 5
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay B <sub>n</sub> to A <sub>n</sub> ; non-inverting (true)		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ , DIR to A <sub>n</sub> ; $\overline{OE}$ , DIR to B <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 5 and 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
$A_n$	1.50
$B_n$	0.40
$\overline{OE}$	1.50
DIR	0.90

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; inverting		10	20		25		30	ns	4.5	Fig. 5
$t_{PHL}/t_{PLH}$	propagation delay $B_n$ to $A_n$ ; non-inverting (true)		13	23		29		35	ns	4.5	Fig. 6
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}$ , DIR to $A_n$ ; $\overline{OE}$ , DIR to $B_n$		16	30		38		45	ns	4.5	Fig. 7
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}$ , DIR to $A_n$ ; $\overline{OE}$ , DIR to $B_n$		17	30		38		45	ns	4.5	Fig. 7
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Figs 5 and 6

AC WAVEFORMS

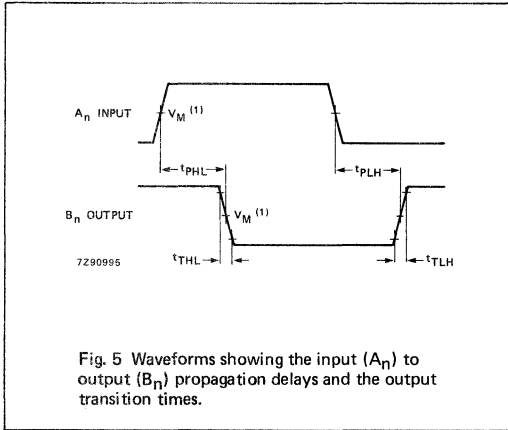


Fig. 5 Waveforms showing the input ( $A_n$ ) to output ( $B_n$ ) propagation delays and the output transition times.

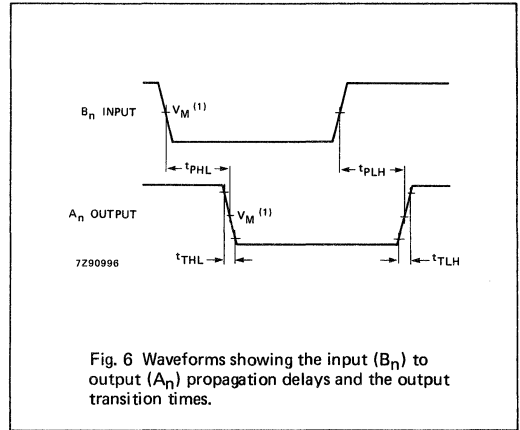


Fig. 6 Waveforms showing the input ( $B_n$ ) to output ( $A_n$ ) propagation delays and the output transition times.

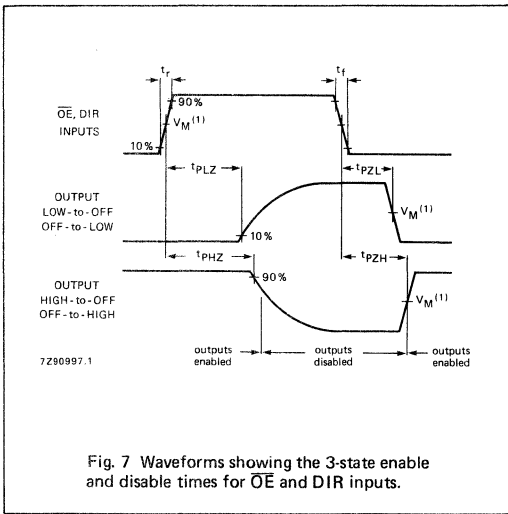


Fig. 7 Waveforms showing the 3-state enable and disable times for OE and DIR inputs.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT646

MSI

## OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE

### FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I<sup>2</sup>C category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT646 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT646 consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP<sub>AB</sub> and CP<sub>BA</sub>) goes to a HIGH logic level. Output enable ( $\overline{OE}$ ) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S<sub>AB</sub> and S<sub>BA</sub>) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when  $\overline{OE}$  is active (LOW). In the isolation mode ( $\overline{OE}$  = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
f <sub>max</sub>	maximum clock frequency		60	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	52	52	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$$f_i = \text{input frequency in MHz} \quad C_L = \text{output load capacitance in pF}$$

$$f_o = \text{output frequency in MHz} \quad V_{CC} = \text{supply voltage in V}$$

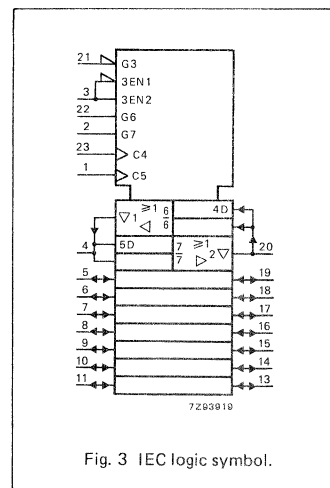
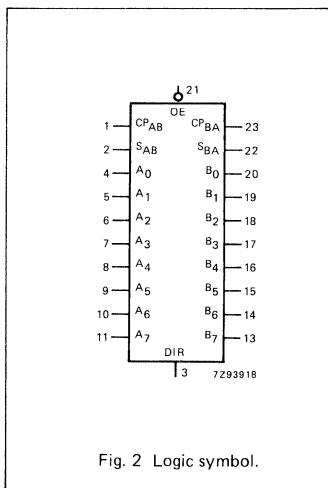
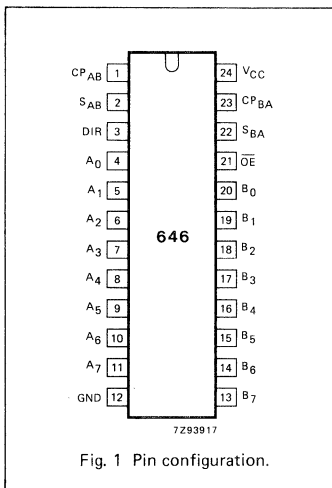
$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT646P: 24-lead DIL; plastic (SOT-101A).

PC74HC/HCT646T: 24-lead mini-pack; plastic (SO-24; SOT-137A).



**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP <sub>AB</sub>	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S <sub>AB</sub>	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	A <sub>0</sub> to A <sub>7</sub>	A data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	B <sub>0</sub> to B <sub>7</sub>	B data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S <sub>BA</sub>	select B to A source input
23	CP <sub>BA</sub>	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V <sub>CC</sub>	positive supply voltage

**GENERAL DESCRIPTION (Cont'd)**

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The "646" is functionally identical to the "648", but has non-inverting data paths.

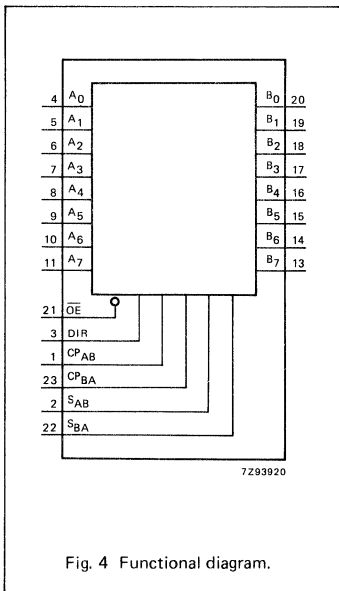


Fig. 4 Functional diagram.

**FUNCTION TABLE**

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A <sub>0</sub> to A <sub>7</sub>	B <sub>0</sub> to B <sub>7</sub>	
H	X	H or L	H or L	X	X	input	input	isolation store A and B data
L	L	X	X	X	L	output	input	real-time B data to A bus stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus stored A data to B bus

\* The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH level transition

DEVELOPMENT DATA

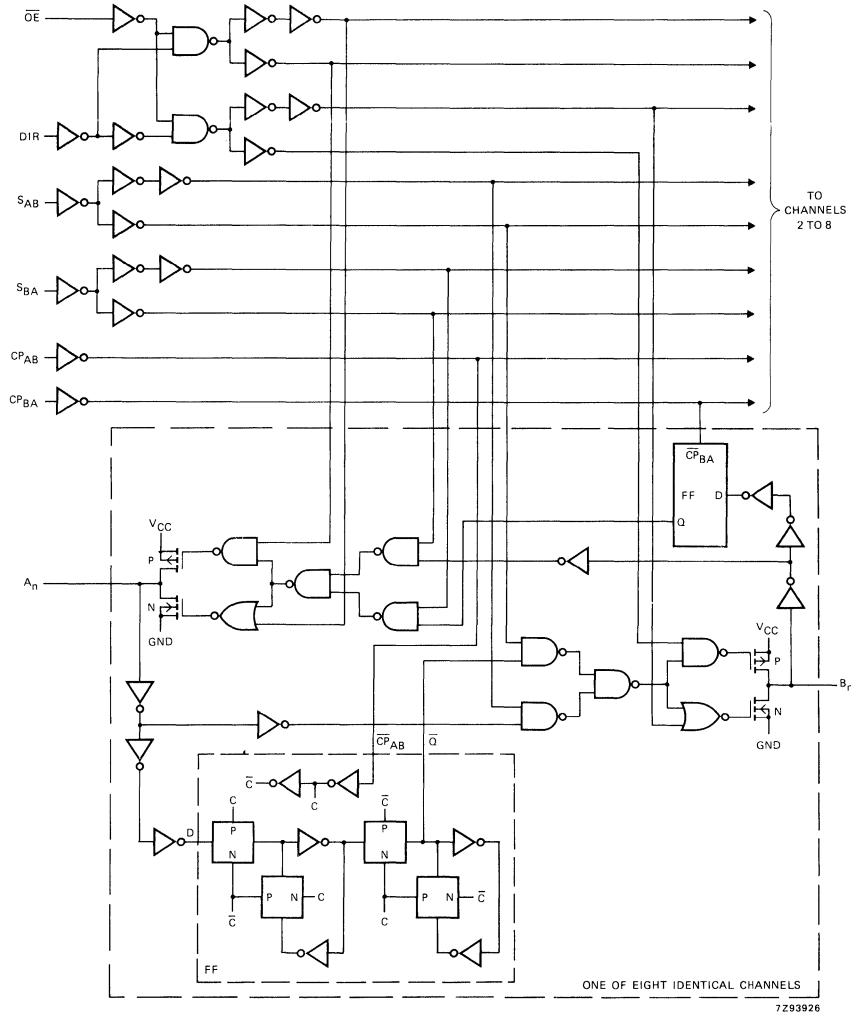


Fig. 5 Logic diagram.



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> , B <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> , B <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to A <sub>n</sub> , B <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to A <sub>n</sub> , B <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	90 18 15				115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	90 18 15				115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	5 5 5				5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	5.4 27 32				4.4 22 26		3.6 18 21	MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
S <sub>AB</sub> , S <sub>BA</sub> A <sub>0</sub> to A <sub>7</sub> and B <sub>0</sub> to B <sub>7</sub>	0.60  0.75	CP <sub>AB</sub> , CP <sub>BA</sub> OE DIR	1.50 1.50 1.50 1.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>			37		46		56	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			44		55		66	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			51		64		77	ns	4.5	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> , B <sub>n</sub>			45		56		68	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> , B <sub>n</sub>			35		44		53	ns	4.5	Fig. 9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to A <sub>n</sub> , B <sub>n</sub>			45		56		68	ns	4.5	Fig. 10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to A <sub>n</sub> , B <sub>n</sub>			35		44		53	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	25				31		38	ns	4.5	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	25				31		38	ns	4.5	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	5				5		5	ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	20				25		30	MHz	4.5	Fig. 7

AC WAVEFORMS

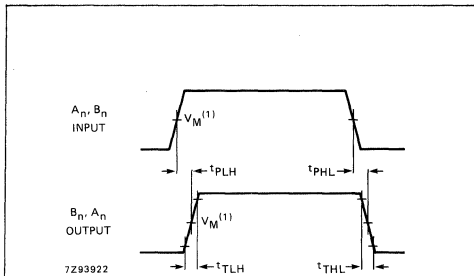


Fig. 6 Waveforms showing the input  $A_n, B_n$  to output  $B_n, A_n$  propagation delays and the output transition times.

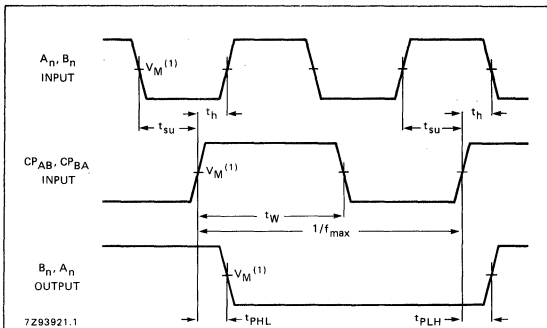


Fig. 7 Waveforms showing the  $A_n, B_n$  to  $CP_{AB}, CP_{BA}$  set-up and hold times, clock  $CP_{AB}, CP_{BA}$  pulse width, maximum clock pulse frequency and the  $CP_{AB}, CP_{BA}$  to output  $B_n, A_n$  propagation delays.

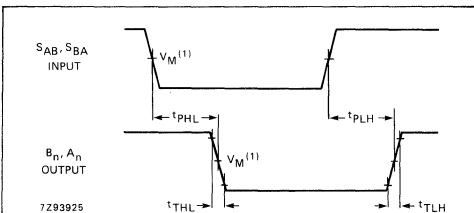


Fig. 8 Waveforms showing the input  $S_{AB}, S_{BA}$  to output  $B_n, A_n$  propagation delays and output transition times.

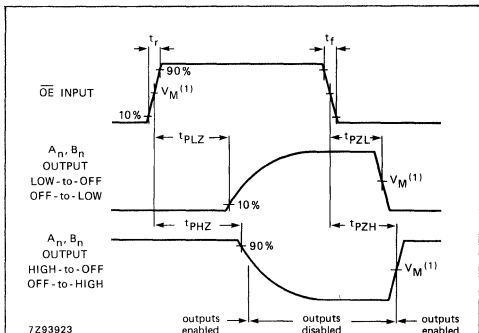


Fig. 9 Waveforms showing the input  $\overline{OE}$  to output  $A_n, B_n$  3-state enable and disable times.

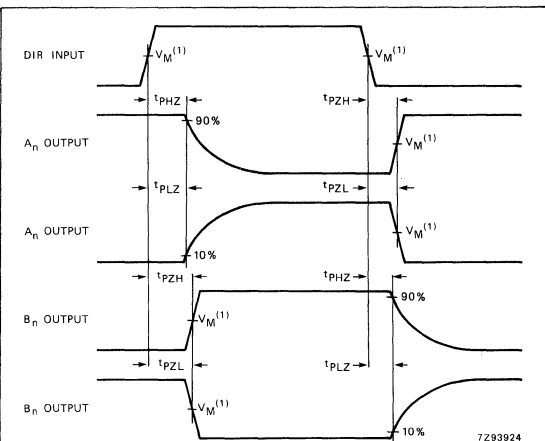


Fig. 10 Waveforms showing the input  $DIR$  to output  $A_n, B_n$  3-state enable and disable times.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
 HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT648

MSI

## OCTAL BUS TRANSCEIVER/REGISTER; 3-STATE; INVERTING

### FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I<sup>CC</sup> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT648 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT648 consist of bus transceiver circuits with 3-state inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the "A" or "B" bus will be clocked into the registers as the appropriate clock (CP<sub>AB</sub> and CP<sub>BA</sub>) goes to a HIGH logic level. Output enable ( $\overline{OE}$ ) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the "A" or "B" register, or in both. The select source inputs (S<sub>AB</sub> and S<sub>BA</sub>) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when  $\overline{OE}$  is active (LOW). In the isolation mode ( $\overline{OE}$  = HIGH), "A" data may be stored in the "B" register and/or "B" data may be stored in the "A" register.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	18	ns
f <sub>max</sub>	maximum clock frequency		60	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	52	52	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT648P: 24-lead DIL; plastic (SOT-101A).

PC74HC/HCT648T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

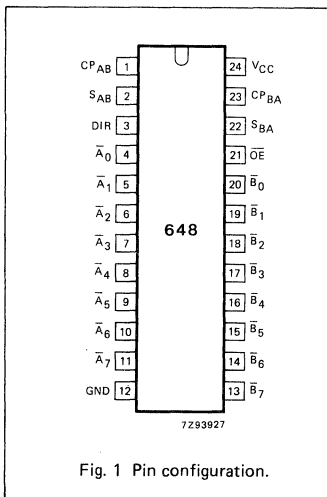


Fig. 1 Pin configuration.

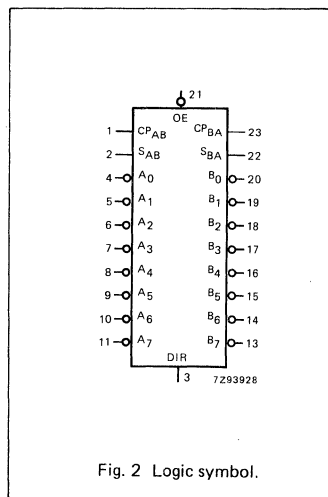


Fig. 2 Logic symbol.

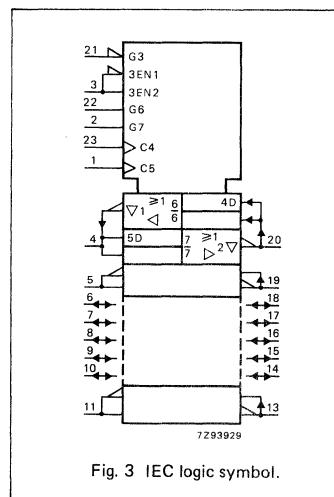


Fig. 3 IEC logic symbol.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CPAB	A to B clock input (LOW-to-HIGH, edge-triggered)
2	SAB	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	$\bar{A}_0$ to $\bar{A}_7$	$\bar{A}$ data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	$\bar{B}_0$ to $\bar{B}_7$	$\bar{B}$ data inputs/outputs
21	$\bar{O}E$	output enable input (active LOW)
22	SBA	select B to A source input
23	CPBA	B to A clock input (LOW-to-HIGH, edge-triggered)
24	VCC	positive supply voltage

**GENERAL DESCRIPTION (Cont'd)**

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The "648" is functionally identical to the "646", but has inverting data paths.

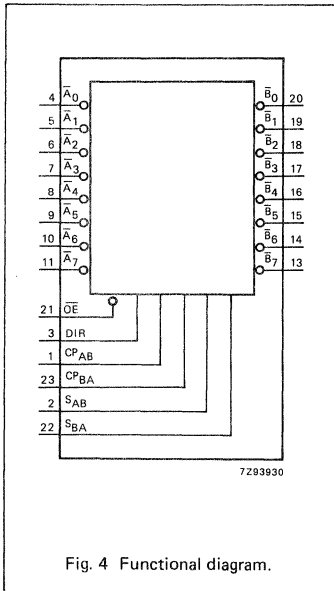


Fig. 4 Functional diagram.

**FUNCTION TABLE**

INPUTS						DATA I/O *		FUNCTION
$\bar{O}E$	DIR	CPAB	CPBA	SAB	SBA	$\bar{A}_0$ to $\bar{A}_7$	$\bar{B}_0$ to $\bar{B}_7$	
H	X	H or L	H or L	X	X	input	input	isolation store $\bar{A}$ and $\bar{B}$ data
H	X	↑	↑	X	X	input	input	isolation store $\bar{A}$ and $\bar{B}$ data
L	L	X	X	X	L	output	input	real-time $\bar{B}$ data to A bus stored $\bar{B}$ data to A bus
L	L	X	X	X	H	output	input	real-time $\bar{B}$ data to A bus stored $\bar{B}$ data to A bus
L	H	X	X	L	X	input	output	real-time $\bar{A}$ data to B bus stored $\bar{A}$ data to B bus
L	H	H or L	X	H	X	input	output	real-time $\bar{A}$ data to B bus stored $\bar{A}$ data to B bus

\* The data output functions may be enabled or disabled by various signals at the  $\bar{O}E$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↑ = LOW-to-HIGH level transition

DEVELOPMENT DATA

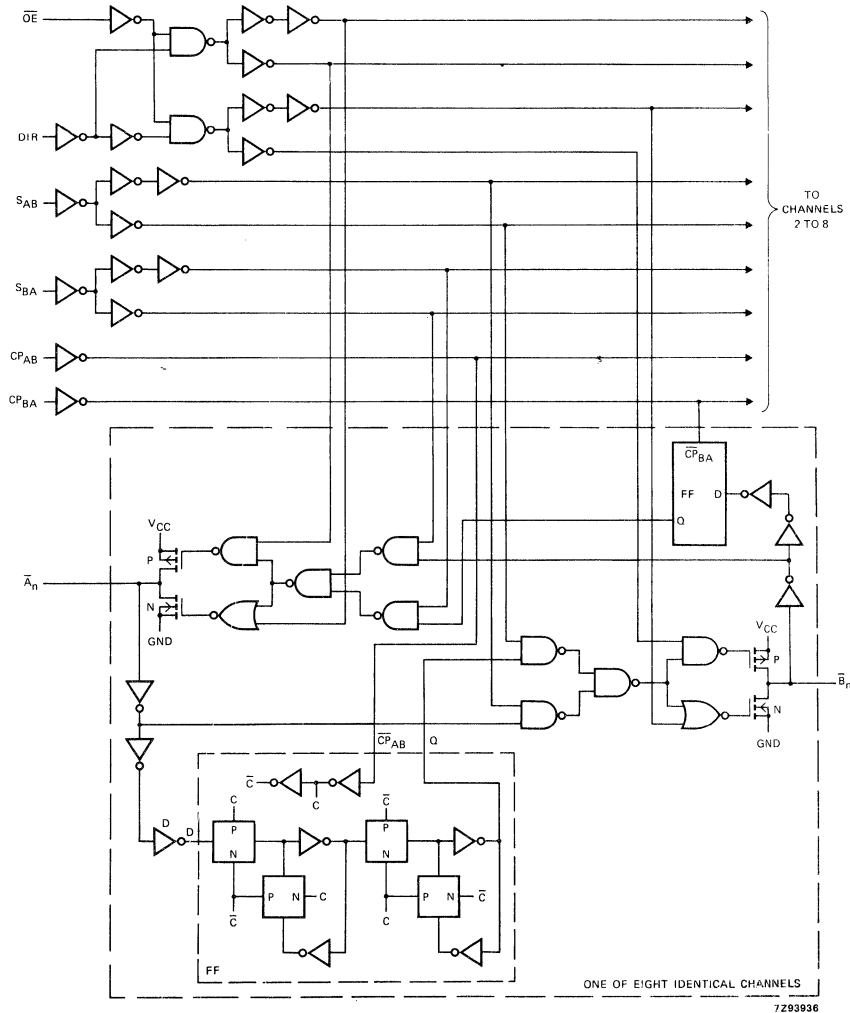


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{A}_n, \bar{B}_n$ to $\bar{B}_n, \bar{A}_n$			150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to $\bar{B}_n, \bar{A}_n$			240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> , S <sub>BA</sub> to $\bar{B}_n, \bar{A}_n$			220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\bar{O}E$ to $\bar{A}_n, \bar{B}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\bar{O}E$ to $\bar{A}_n, \bar{B}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to $\bar{A}_n, \bar{B}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to $\bar{A}_n, \bar{B}_n$			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 6 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	90 18 15				115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time $\bar{A}_n, \bar{B}_n$ to CP <sub>AB</sub> , CP <sub>BA</sub>	90 18 15				115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time $\bar{A}_n, \bar{B}_n$ to CP <sub>AB</sub> , CP <sub>BA</sub>	5 5 5				5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	5.4 27 32				4.4 22 26		3.6 18 21	MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
S <sub>AB</sub> , S <sub>BA</sub> A <sub>0</sub> to A <sub>7</sub> and B <sub>0</sub> to B <sub>7</sub>	0.60  0.75	CP <sub>AB</sub> , CP <sub>BA</sub> OE DIR	1.50 1.50 1.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>			37		46		56	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			54		68		81	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>			51		64		77	ns	4.5	Fig. 8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> , B <sub>n</sub>			45		56		68	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> , B <sub>n</sub>			35		44		53	ns	4.5	Fig. 9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to A <sub>n</sub> , B <sub>n</sub>			45		56		68	ns	4.5	Fig. 10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to A <sub>n</sub> , B <sub>n</sub>			35		44		53	ns	4.5	Fig. 10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Figs 6 and 8
t <sub>w</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	25				31		38	ns	4.5	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	25				31		38	ns	4.5	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> , B <sub>n</sub> to CP <sub>AB</sub> , CP <sub>BA</sub>	5				5		5	ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	20				16		13	MHz	4.5	Fig. 7



AC WAVEFORMS

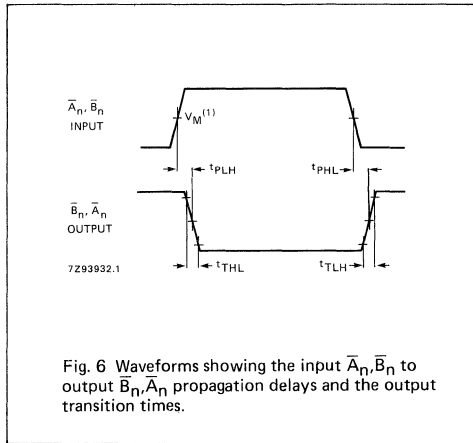


Fig. 6 Waveforms showing the input  $\bar{A}_n, \bar{B}_n$  to output  $\bar{B}_n, \bar{A}_n$  propagation delays and the output transition times.

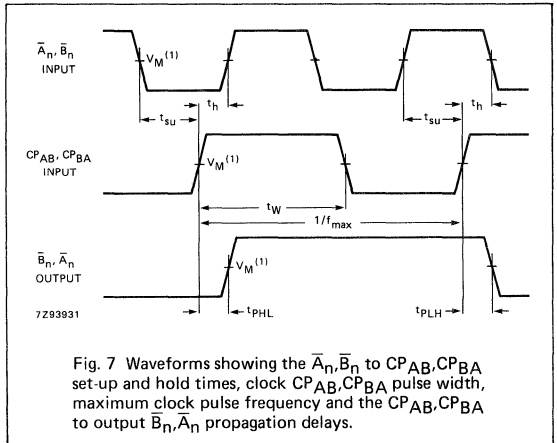


Fig. 7 Waveforms showing the  $\bar{A}_n, \bar{B}_n$  to  $CP_{AB}, CP_{BA}$  set-up and hold times, clock  $CP_{AB}, CP_{BA}$  pulse width, maximum clock pulse frequency and the  $CP_{AB}, CP_{BA}$  to output  $\bar{B}_n, \bar{A}_n$  propagation delays.

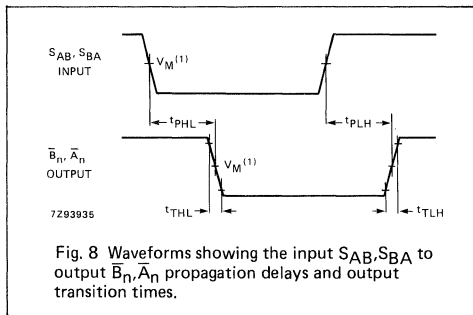


Fig. 8 Waveforms showing the input  $S_{AB}, S_{BA}$  to output  $\bar{B}_n, \bar{A}_n$  propagation delays and output transition times.

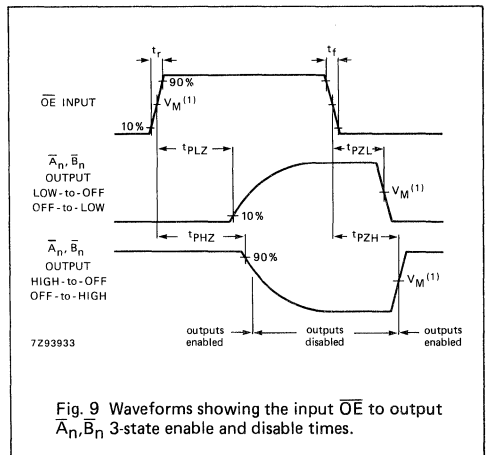


Fig. 9 Waveforms showing the input  $\bar{OE}$  to output  $\bar{A}_n, \bar{B}_n$  3-state enable and disable times.

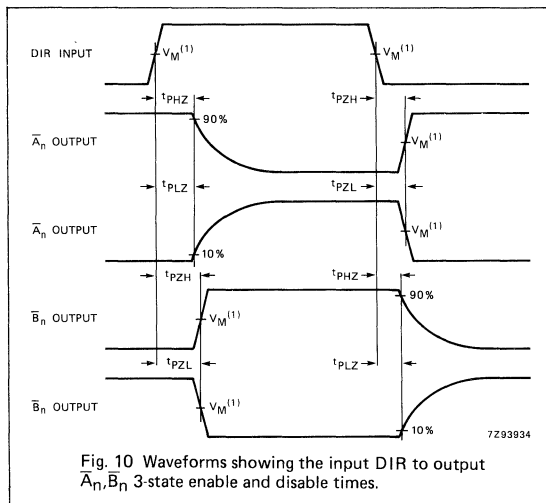


Fig. 10 Waveforms showing the input DIR to output  $\bar{A}_n, \bar{B}_n$  3-state enable and disable times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_1 = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_1 = \text{GND to } 3 \text{ V}$ .

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT670  
MSI

## 4 x 4 REGISTER FILE; 3-STATE

### FEATURES

- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R<sub>A</sub>, R<sub>B</sub> and W<sub>A</sub>, W<sub>B</sub>) and enable inputs (R<sub>E</sub> and W<sub>E</sub>) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D<sub>0</sub> to D<sub>3</sub>). The W<sub>A</sub> and W<sub>B</sub> inputs determine the location of the stored word. When the W<sub>E</sub> input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the W<sub>E</sub> input is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs (Q<sub>0</sub> to Q<sub>3</sub>). D<sub>n</sub> and W<sub>n</sub> inputs are inhibited when W<sub>E</sub> is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R<sub>A</sub> and R<sub>B</sub>). The addressed word appears at the four outputs when the R<sub>E</sub> is LOW. Data outputs are in the high impedance OFF-state when R<sub>E</sub> is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	21	21	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	—	—	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT670P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT670T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4	R <sub>A</sub> , R <sub>B</sub>	read address inputs
8	GND	ground (0 V)
10, 9, 7, 6	Q <sub>0</sub> to Q <sub>3</sub>	data outputs
11	R <sub>E</sub>	3-state output read enable input (active LOW)
12	W <sub>E</sub>	write enable input (active LOW)
14, 13	W <sub>A</sub> , W <sub>B</sub>	write address inputs
15, 1, 2, 3	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage

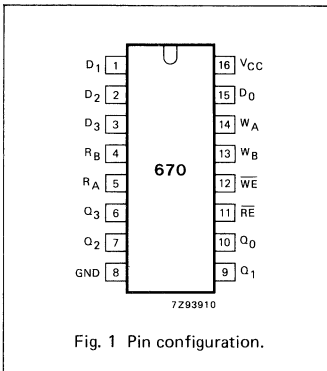


Fig. 1 Pin configuration.

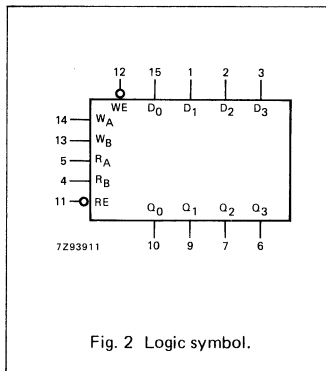


Fig. 2 Logic symbol.

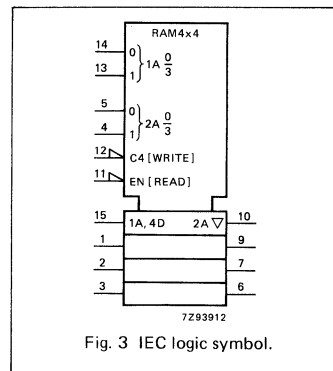


Fig. 3 IEC logic symbol.

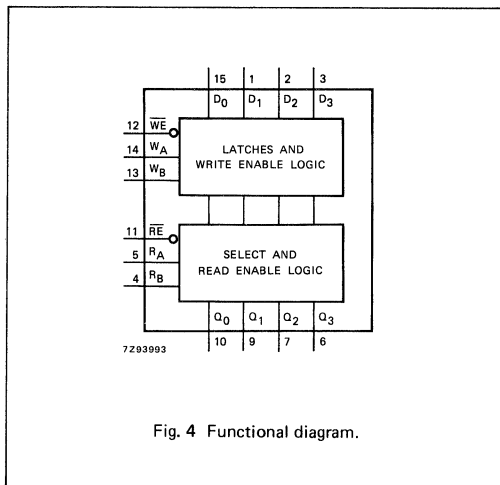


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

**WRITE MODE SELECT TABLE**

OPERATING MODE	INPUTS		INTERNAL LATCHES*
	WE	D <sub>n</sub>	
write data	L L	L H	L H
data latched	H	X	no change

\* The write address (W<sub>A</sub> and W<sub>B</sub>) to the "internal latches" must be stable while WE is LOW for conventional operation.

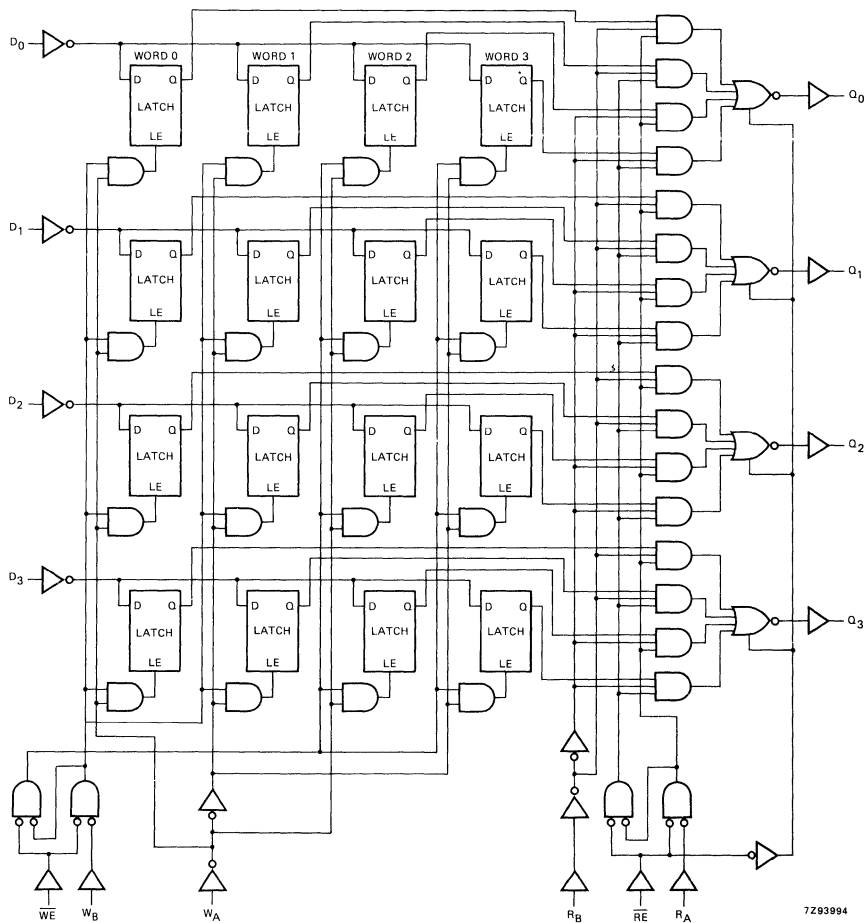
**READ MODE SELECT TABLE**

OPERATING MODE	INPUTS		OUTPUT
	RE	INTERNAL LATCHES**	
read	L L	L H	L H
disabled	H	X	Z

\*\* The selection of the "internal latches" by read address (R<sub>A</sub> and R<sub>B</sub>) are not constrained by WE or RE operation.

- H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state

DEVELOPMENT DATA



7293994

Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	V <sub>CC</sub> V	TEST CONDITIONS WAVEFORMS	
		74HC									
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay R <sub>A</sub> , R <sub>B</sub> to Q <sub>n</sub>			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay WE to Q <sub>n</sub>			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time RE to Q <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time RE to Q <sub>n</sub>			175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	read enable pulse width LOW	90 18 15			115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	write enable pulse width LOW	90 18 15			115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to WE	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time W <sub>A</sub> , W <sub>B</sub> to WE	60 12 10			75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to WE	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time W <sub>A</sub> , W <sub>B</sub> to WE	5 5 5			5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t <sub>latch</sub>	latch time WE to R <sub>A</sub> , R <sub>B</sub>	225 45 38			230 56 48		340 68 58		ns	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.25	R <sub>A</sub>	0.70
$\overline{WE}$ , W <sub>A</sub>	0.40	R <sub>B</sub>	1.10
W <sub>B</sub>	0.60	$\overline{RE}$	1.35

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay R <sub>A</sub> , R <sub>B</sub> to Q <sub>n</sub>			50		63		75	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{WE}$ to Q <sub>n</sub>			53		66		80	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>			50		63		75	ns	4.5	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{RE}$ to Q <sub>n</sub>			40		50		60	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{RE}$ to Q <sub>n</sub>			35		44		53	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	read enable pulse width LOW	25			31			38	ns	4.5	Fig. 9
t <sub>W</sub>	write enable pulse width LOW	25			31			38	ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{WE}$	12			15			18	ns	4.5	Fig. 8
t <sub>su</sub>	set-up time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	18			23			27	ns	4.5	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{WE}$	5			5			5	ns	4.5	Fig. 8
t <sub>h</sub>	hold time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	5			5			5	ns	4.5	Fig. 8
t <sub>latch</sub>	latch time $\overline{WE}$ to R <sub>A</sub> , R <sub>B</sub>	50			63			75	ns	4.5	Fig. 8

AC WAVEFORMS

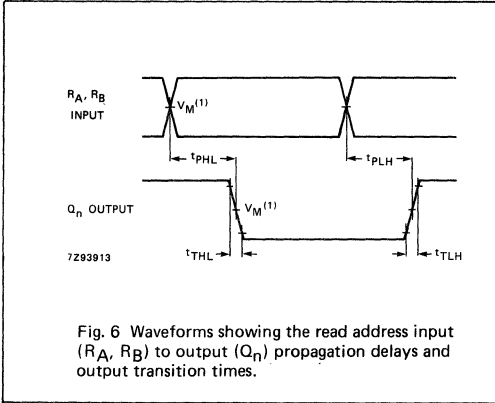


Fig. 6 Waveforms showing the read address input ( $R_A$ ,  $R_B$ ) to output ( $Q_n$ ) propagation delays and output transition times.

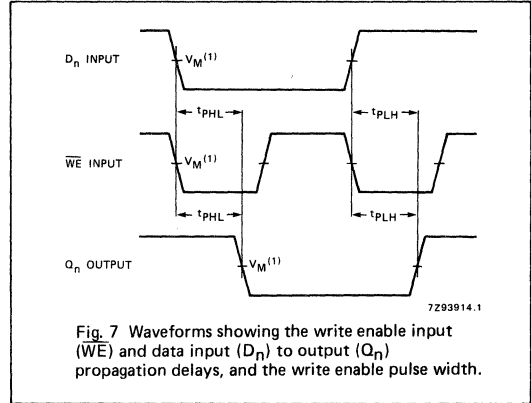
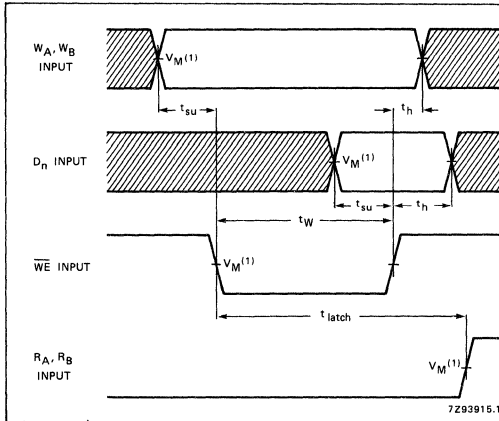


Fig. 7 Waveforms showing the write enable input ( $\overline{WE}$ ) and data input ( $D_n$ ) to output ( $Q_n$ ) propagation delays, and the write enable pulse width.



Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

The time allowed for the internal output of the latch to assume the state of the new data ( $t_{latch}$ ) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of  $\overline{WE}$  to the rising edge of  $R_A$  or  $R_B$ .  $\overline{RE}$  must be LOW.

Fig. 8 Waveforms showing the write address input ( $W_A$ ,  $W_B$ ) and data input ( $D_n$ ) to write enable ( $\overline{WE}$ ) set-up, hold and latch times.

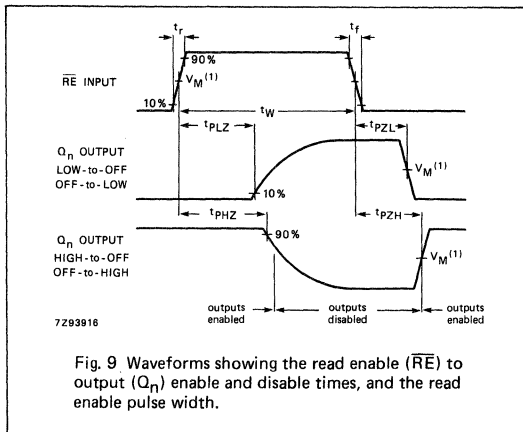


Fig. 9 Waveforms showing the read enable ( $\overline{RE}$ ) to output ( $Q_n$ ) enable and disable times, and the read enable pulse width.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

### 8-BIT MAGNITUDE COMPARATOR

#### FEATURES

- Compare two 8-bit words
- Output capability: standard
- I<sub>CC</sub> category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT688 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT688 are 8-bit magnitude comparators. They perform comparison of two 8-bit binary or BCD words. The output provides  $\overline{P=Q}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> , Q <sub>n</sub> to $\overline{P=Q}$ E to $\overline{P=Q}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 8	13 9	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	30	30	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

#### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

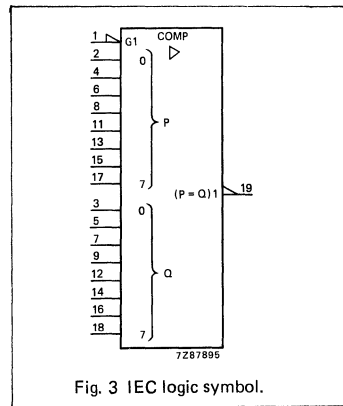
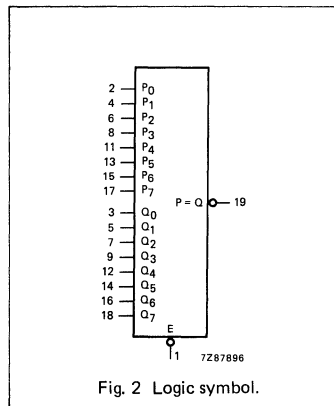
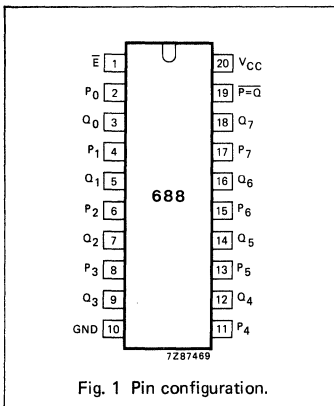
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

#### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT688P: 20-lead DIL; plastic (SOT-146).  
 PC74HC/HCT688T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	E	enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P <sub>0</sub> to P <sub>7</sub>	word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q <sub>0</sub> to Q <sub>7</sub>	word inputs
10	GND	ground (0 V)
19	$\overline{P=Q}$	equal to output
20	V <sub>CC</sub>	positive supply voltage





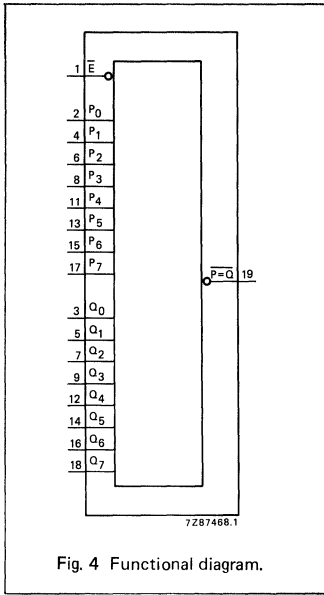


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P <sub>n</sub> , Q <sub>n</sub>	ENABLE E	$\overline{P=Q}$
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

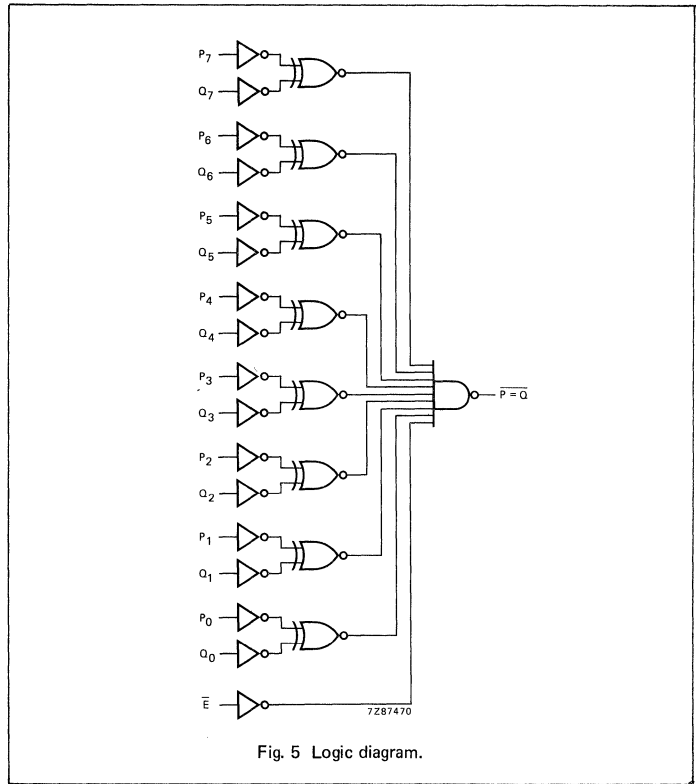


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> , Q <sub>n</sub> to $\overline{P} = \overline{Q}$		47 17 14	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{E}$ to $\overline{P} = \overline{Q}$		28 10 8	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
P <sub>n</sub>	0.35
Q <sub>n</sub>	0.35
E	0.70

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay P <sub>n</sub> , Q <sub>n</sub> to P = Q		16	31		39		47	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to P = Q		11	20		25		30	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

## AC WAVEFORMS

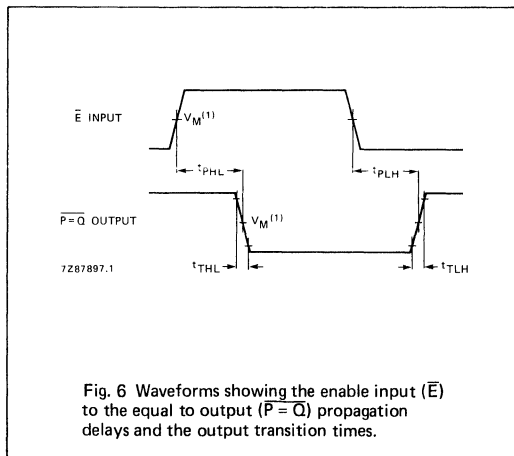


Fig. 6 Waveforms showing the enable input ( $\bar{E}$ ) to the equal to output ( $\overline{P=Q}$ ) propagation delays and the output transition times.

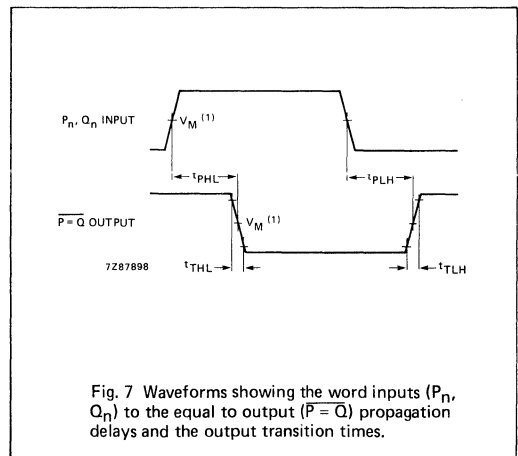


Fig. 7 Waveforms showing the word inputs ( $P_n, Q_n$ ) to the equal to output ( $\overline{P=Q}$ ) propagation delays and the output transition times.

## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



## DUAL 4-INPUT NOR GATE

### FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT4002 are high-speed Si-gate CMOS devices and are pin compatible with "4002" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4002 provide the 4-input NOR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB, nC, nD to nY	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	9	11	ns
$C_i$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	16	22	pF

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

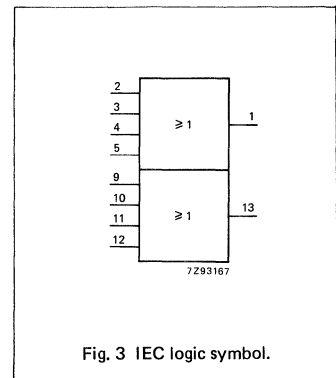
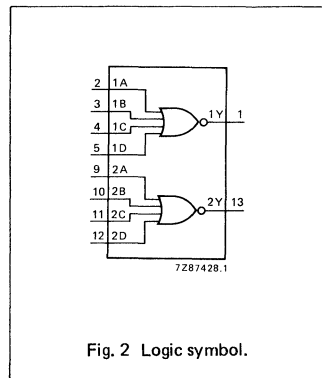
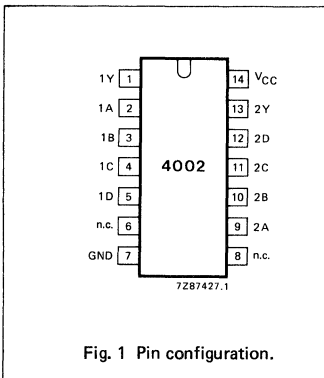
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4002P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT4002T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1Y, 2Y	data outputs
2, 9	1A, 2A	data inputs
3, 10	1B, 2B	data inputs
4, 11	1C, 2C	data inputs
5, 12	1D, 2D	data inputs
6, 8	n.c.	not connected
7	GND	ground (0 V)
14	$V_{CC}$	positive supply voltage



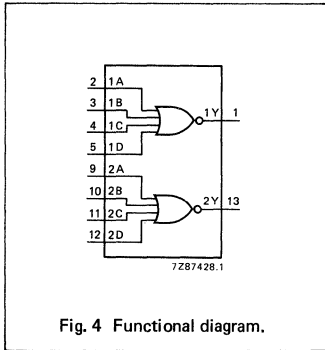


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

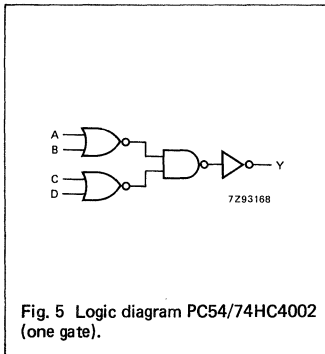


Fig. 5 Logic diagram PC54/74HC4002 (one gate).

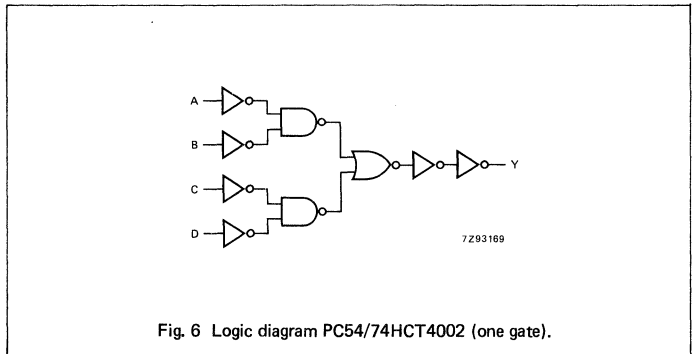


Fig. 6 Logic diagram PC54/74HCT4002 (one gate).

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: SSI

**AC CHARACTERISTICS FOR 74HC**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay nA, nB, nC, nD to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

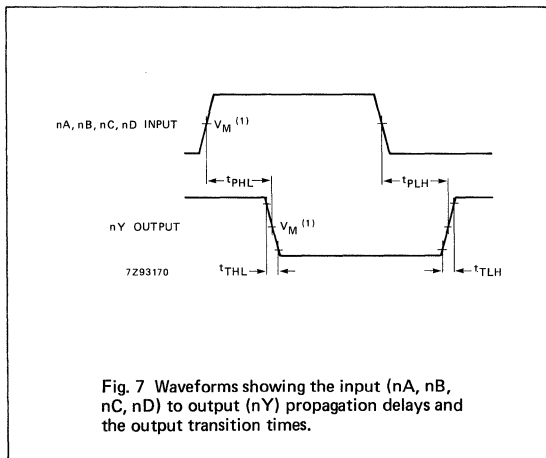
input	unit load coefficient
nA, nB, nC, nD	0.45

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC, nD to nY		13	22		28		33	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7

**AC WAVEFORMS**



**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.

HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4015  
MSI

## DUAL 4-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

### FEATURES

- Output capability: standard
- ICC category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4015 are high-speed Si-gate CMOS devices and are pin compatible with the "4015" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4015 are dual edge-triggered 4-bit static shift registers (serial-to-parallel converters). Each shift register has a serial data input (1D and 2D), a clock input (1CP and 2CP), four fully buffered parallel outputs (1Q<sub>0</sub> to 1Q<sub>3</sub> and 2Q<sub>0</sub> to 2Q<sub>3</sub>) and an overriding asynchronous master reset (1MR and 2MR). Information present on nD is shifted to the first register position, and all data in the register is shifted one position to the right on the LOW-to-HIGH transition of nCP. A HIGH on nMR clears the register and forces nQ<sub>0</sub> to nQ<sub>3</sub> to LOW, independent of nCP and nD.

### APPLICATIONS

- Serial-to-parallel converter
- Buffer stores
- General purpose register

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	16	ns
f <sub>max</sub>	maximum clock frequency		104	73	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4015P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4015T: 16-lead mini-pack; plastic (SO-16; SOT109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4, 3, 10	1Q <sub>0</sub> to 1Q <sub>3</sub>	flip-flop outputs
6, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
7, 15	1D, 2D	serial data inputs
8	GND	ground (0 V)
9, 1	1CP, 2CP	clock inputs (LOW-to-HIGH, edge-triggered)
13, 12, 11, 2	2Q <sub>0</sub> to 2Q <sub>3</sub>	flip-flop outputs
16	V <sub>CC</sub>	positive supply voltage

### FUNCTION TABLE

INPUTS				OUTPUTS			
n	nCP	nD	nMR	nQ <sub>0</sub>	nQ <sub>1</sub>	nQ <sub>2</sub>	nQ <sub>3</sub>
1	↑	D <sub>1</sub>	L	D <sub>1</sub>	X	X	X
2	↑	D <sub>2</sub>	L	D <sub>2</sub>	D <sub>1</sub>	X	X
3	↑	D <sub>3</sub>	L	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	X
4	↑	D <sub>4</sub>	L	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
	↓	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition

n = number of clock pulse transitions

D<sub>n</sub> = either HIGH or LOW

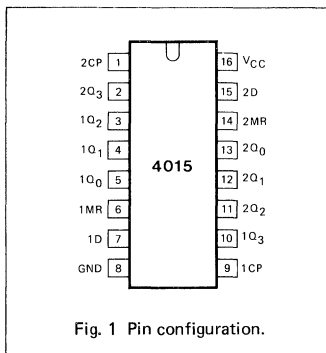


Fig. 1 Pin configuration.



QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance:  
90 Ω (typ.) at V<sub>CC</sub> = 4.5 V  
80 Ω (typ.) at V<sub>CC</sub> = 6.0 V  
65 Ω (typ.) at V<sub>CC</sub> = 9.0 V
- Individual switch controls
- Typical "break before make" built in
- Output capability: non-standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the "4016" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4016 have four independent analog switches (transmission gates).

Each switch has two input/output terminals (Y<sub>n</sub>, Z<sub>n</sub>) and an active HIGH enable input (E<sub>n</sub>). When E<sub>n</sub> is connected to V<sub>CC</sub>, a low bidirectional path between Y<sub>n</sub> and Z<sub>n</sub> is established (ON condition). When E<sub>n</sub> is connected to ground (GND), the switch is disabled and a high impedance between Y<sub>n</sub> and Z<sub>n</sub> is established (OFF condition).

Current through a switch will not cause additional V<sub>CC</sub> current provided the voltage at the terminals of the switch is maintained within the supply voltage range; V<sub>CC</sub> ≥ (V<sub>Y</sub>, V<sub>Z</sub>) ≥ GND. Inputs Y<sub>n</sub> and Z<sub>n</sub> are electrically equivalent terminals.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time E <sub>n</sub> to V <sub>OS</sub>	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 kΩ V <sub>CC</sub> = 5 V	17	21	ns
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time E <sub>n</sub> to V <sub>OS</sub>		14	16	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per switch	notes 1 and 2	12	12	pF
C <sub>S</sub>	max. switch capacitance		5	5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
Σ{(C<sub>L</sub> + C<sub>S</sub>) × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>} = sum of outputs  
C<sub>L</sub> = output load capacitance in pF  
C<sub>S</sub> = max. switch capacitance in pF  
V<sub>CC</sub> = supply voltage in V

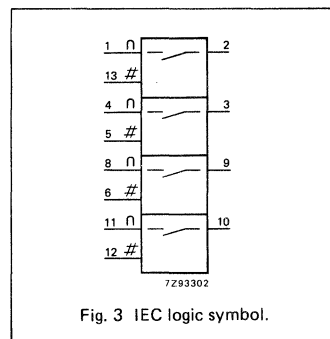
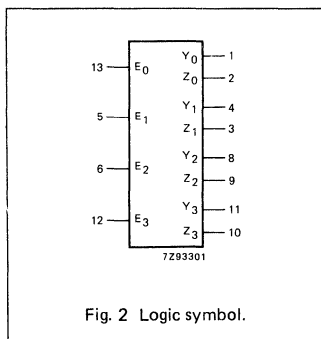
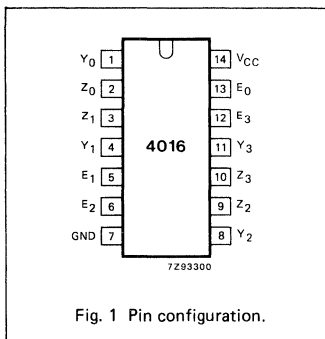
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4016P: 14-lead DIL; plastic (SOT-27).  
PC74HC/HCT4016T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	Y <sub>0</sub> to Y <sub>3</sub>	independent inputs/outputs
7	GND	ground (0 V)
2, 3, 9, 10	Z <sub>0</sub> to Z <sub>3</sub>	independent inputs/outputs
13, 5, 6, 12	E <sub>0</sub> to E <sub>3</sub>	enable inputs (active HIGH)
14	V <sub>CC</sub>	positive supply voltage



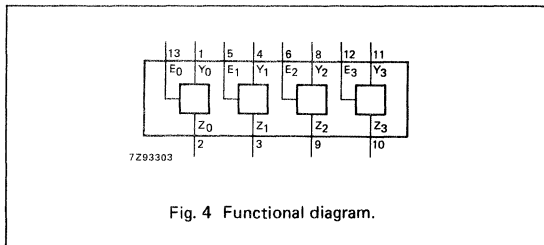


Fig. 4 Functional diagram.

**APPLICATIONS**

- Signal gating
- Modulation
- Demodulation
- Chopper

**FUNCTION TABLE**

INPUT $E_n$	CHANNEL IMPEDANCE
L	high
H	low

H = HIGH voltage level

L = LOW voltage level

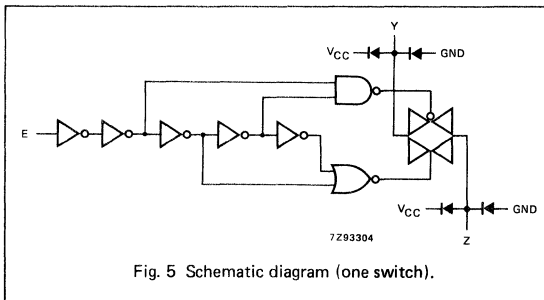


Fig. 5 Schematic diagram (one switch).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V <sub>CC</sub>	DC supply voltage	-0.5	+11.0	V	
±I <sub>IK</sub>	DC digital input diode current		20	mA	for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V
±I <sub>SK</sub>	DC switch diode current		20	mA	for V <sub>S</sub> < -0.5 V or V <sub>S</sub> > V <sub>CC</sub> + 0.5 V
±I <sub>S</sub>	DC switch current		25	mA	for -0.5 V < V <sub>S</sub> < V <sub>CC</sub> + 0.5 V
±I <sub>CC</sub> ; ±I <sub>GND</sub>	DC V <sub>CC</sub> or GND current		50	mA	
T <sub>stg</sub>	storage temperature range	-65	+150	°C	
P <sub>tot</sub>	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K
P <sub>S</sub>	power dissipation per switch		100	mW	

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V <sub>CC</sub>	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V <sub>I</sub>	DC input voltage range	GND		V <sub>CC</sub>	GND		V <sub>CC</sub>	V	
V <sub>S</sub>	DC switch voltage range	GND		V <sub>CC</sub>	GND		V <sub>CC</sub>	V	
T <sub>amb</sub>	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T <sub>amb</sub>	operating ambient temperature range	-40		+125	-40		+125	°C	
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V V <sub>CC</sub> = 10.0 V

**DC CHARACTERISTICS FOR 74HC/HCT**

For 74HC:  $V_{CC} = 2.0, 4.5, 6.0$  and  $9.0$  V

For 74HCT:  $V_{CC} = 4.5$  V

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC/HCT							$V_{CC}$ V	$I_S$ $\mu A$	$V_{is}$	$V_I$
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$R_{ON}$	ON resistance	-	-	-	-	-	-	$\Omega$	2.0	100	$V_{CC}$ to GND	$V_{IH}$ or $V_{IL}$
		160	320	400	480	$\Omega$	4.5	1000				
		120	240	300	360	$\Omega$	6.0	1000				
		85	170	213	255	$\Omega$	9.0	1000				
$R_{ON}$	ON resistance	160	-	-	-	-	-	$\Omega$	2.0	100	GND	$V_{IH}$ or $V_{IL}$
		80	160	200	240	$\Omega$	4.5	1000				
		70	140	175	210	$\Omega$	6.0	1000				
		60	120	150	180	$\Omega$	9.0	1000				
$R_{ON}$	ON resistance	170	-	-	-	-	-	$\Omega$	2.0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		90	180	225	270	$\Omega$	4.5	1000				
		80	160	200	240	$\Omega$	6.0	1000				
		65	135	170	205	$\Omega$	9.0	1000				
$\Delta R_{ON}$	maximum $\Delta R_{ON}$ resistance between any two channels	-	-	-	-	-	-	$\Omega$	2.0	-	$V_{CC}$ to GND	$V_{IH}$ or $V_{IL}$
		16	-	-	-	-	-	$\Omega$	4.5	-		
		12	-	-	-	-	-	$\Omega$	6.0	-		
		9	-	-	-	-	-	$\Omega$	9.0	-		

**Notes to DC characteristics**

1. At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring  $R_{ON}$  see Fig. 6.

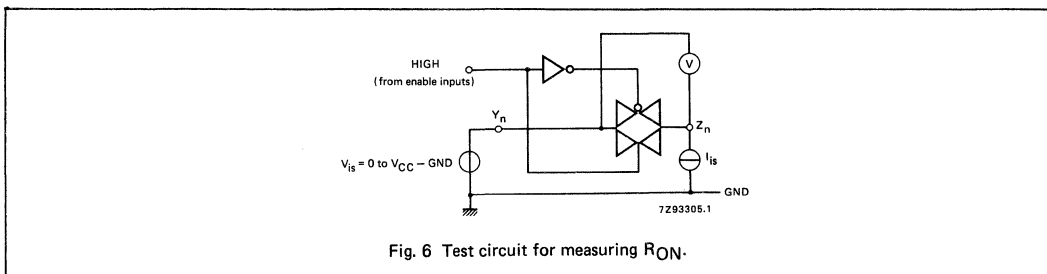


Fig. 6 Test circuit for measuring  $R_{ON}$ .

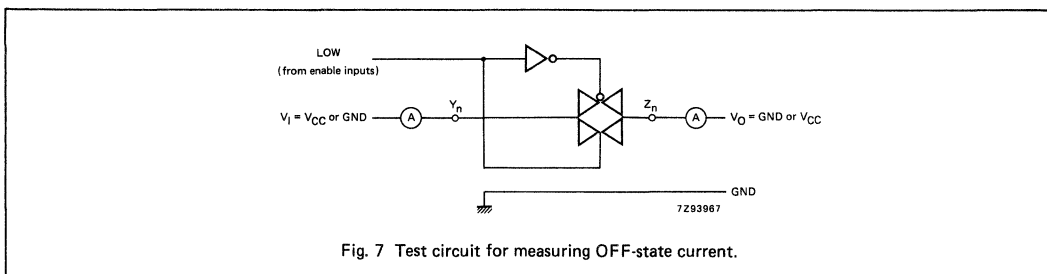


Fig. 7 Test circuit for measuring OFF-state current.

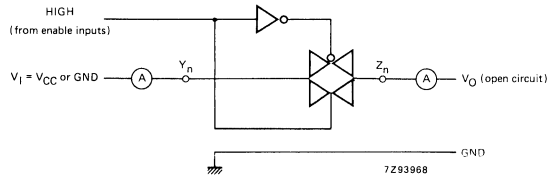


Fig. 8 Test circuit for measuring ON-state current.

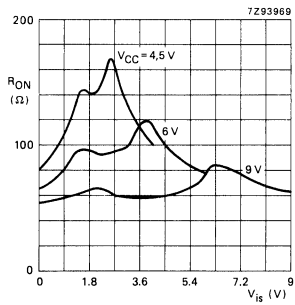


Fig. 9 Typical  $R_{ON}$  as a function of input voltage  $V_{is}$  for  $V_{is} = 0$  to  $V_{CC}$ .



**DC CHARACTERISTICS FOR 74HC**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS		
		74HC									V <sub>CC</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V <sub>CC</sub> or GND		
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - GND (see Fig. 7)	
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - GND (see Fig. 8)	
I <sub>CC</sub>	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	μA	6.0 10.0	V <sub>CC</sub> or GND	V <sub>is</sub> = GND or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or GND	

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Fig. 16)	
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time E <sub>n</sub> to V <sub>os</sub>		55 20 16 14	190 38 32 28		240 48 41 35		235 57 48 42	ns	2.0 4.5 6.0 9.0	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 17 and 18)	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time E <sub>n</sub> to V <sub>os</sub>		47 17 14 11	145 29 25 22		180 36 31 28		220 44 38 33	ns	2.0 4.5 6.0 9.0	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 17 and 18)	

## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HCT							$V_{CC}$ V	$V_I$	OTHER		
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
$V_{IH}$	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
$V_{IL}$	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
$\pm I_I$	input leakage current			0.1		1.0		1.0	$\mu A$	5.5	$V_{CC}$ or GND		
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	$\mu A$	5.5	$V_{IH}$ or $V_{IL}$	$ V_S  =$ $V_{CC} - GND$ (see Fig. 7)	
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	$\mu A$	5.5	$V_{IH}$ or $V_{IL}$	$ V_S  =$ $V_{CC} - GND$ (see Fig. 8)	
$I_{CC}$	quiescent supply current			2.0		20.0		40.0	$\mu A$	4.5 to 5.5	$V_{CC}$ or GND	$V_{is} = GND$ or $V_{CC}$ ; $V_{os} =$ $V_{CC}$ or GND	
$\Delta I_{CC}$	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	$\mu A$	4.5 to 5.5	$V_{CC}$ -2.1V	other inputs at $V_{CC}$ or GND	

## Note

1. The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given here.  
To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$E_n$	1.00

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{Os}$		6	12		15		18	ns	4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 16)
$t_{PZH}$	turn "ON" time $E_n$ to $V_{Os}$		17	35		44		53	ns	4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 17 and 18)
$t_{PZL}$	turn "ON" time $E_n$ to $V_{Os}$		25	52		65		78	ns	4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 17 and 18)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $E_n$ to $V_{Os}$		19	35		44		53	ns	4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 17 and 18)

## ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V;  $t_r = t_f = 6$  ns

SYMBOL	PARAMETER	typ.	UNIT	$V_{CC}$ V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion $f = 1$ kHz	0.80 0.40	% %	4.5 9.0	4.0 8.0	$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 14)
	sine-wave distortion $f = 10$ kHz	2.40 1.20	% %	4.5 9.0	4.0 8.0	$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	4.5 9.0	note 1	$R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f = 1$ MHz (see Figs 10 and 15)
	crosstalk between any two switches	-60 -60	dB dB	4.5 9.0	note 1	$R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f = 1$ MHz (see Fig. 12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		$R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f = 1$ MHz ( $E_n$ , square wave between $V_{CC}$ and GND, $t_r = t_f = 6$ ns) (see Fig. 13)
$f_{max}$	minimum frequency response (-3dB)	150 160	MHz MHz	4.5 9.0	note 2	$R_L = 50$ $\Omega$ ; $C_L = 10$ pF (see Figs 11 and 14)
$C_S$	maximum switch capacitance	5	pF			

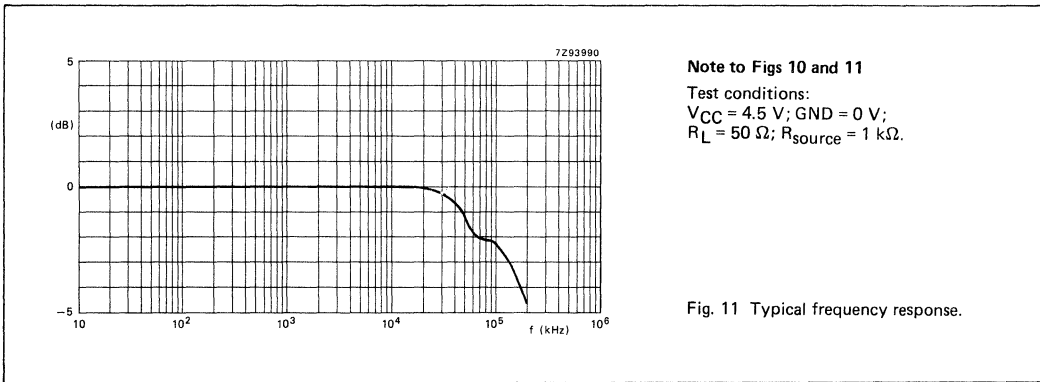
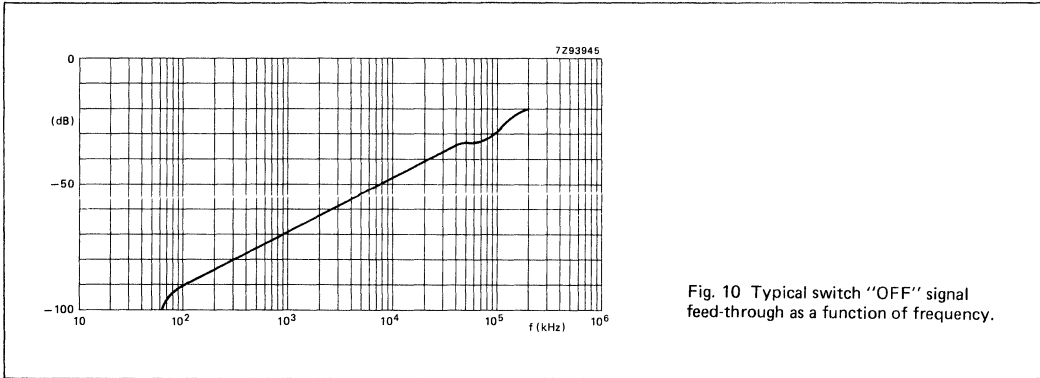
## Notes to AC characteristics

## General note

$V_{is}$  is the input voltage at a  $Y_n$  or  $Z_n$  terminal, whichever is assigned as an input.  
 $V_{Os}$  is the output voltage at a  $Y_n$  or  $Z_n$  terminal, whichever is assigned as an output.

## Notes

- Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).
- Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{Os}$  for 10 kHz (0 dBm = 1 mW into 50  $\Omega$ ).



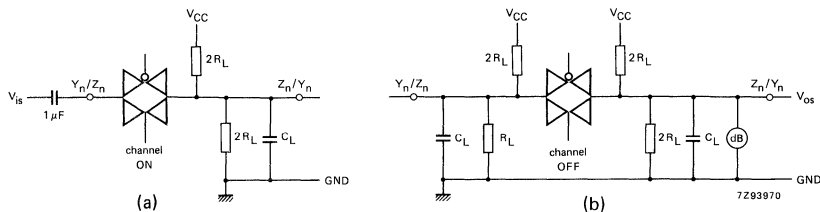


Fig. 12 Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

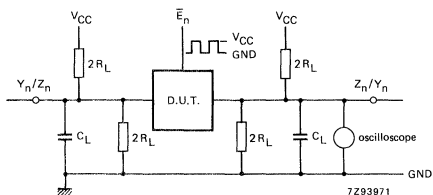


Fig. 13 Test circuit for measuring crosstalk between control and any switch.

**Note to Fig. 13**

The crosstalk is defined as follows (oscilloscope output):

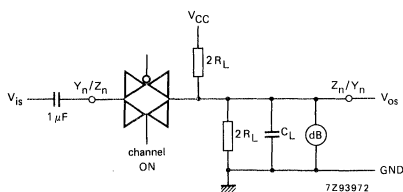
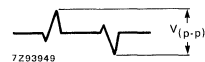


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

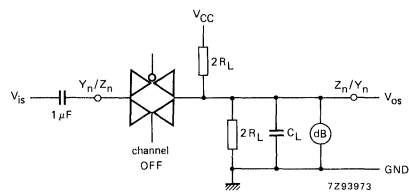


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

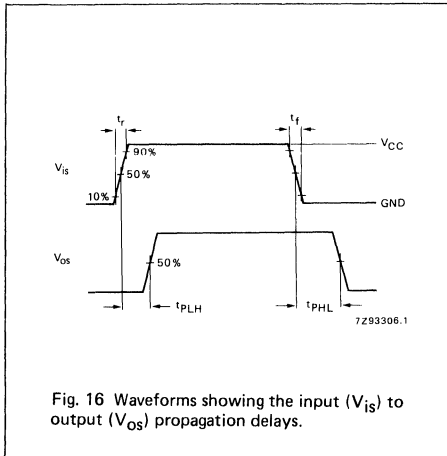


Fig. 16 Waveforms showing the input ( $V_{1S}$ ) to output ( $V_{Os}$ ) propagation delays.

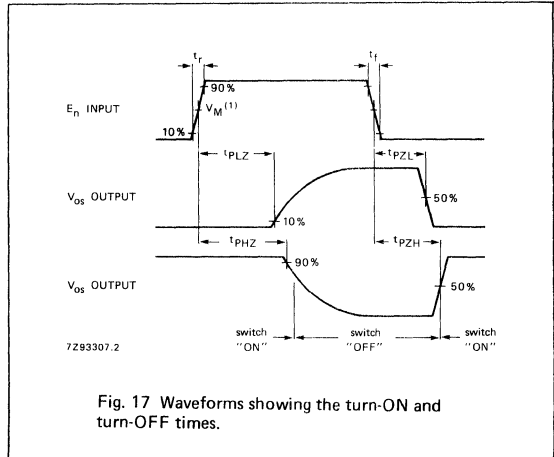
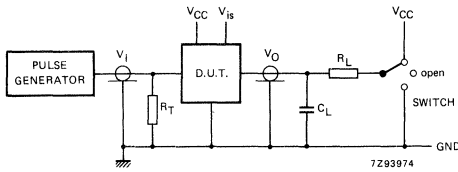


Fig. 17 Waveforms showing the turn-ON and turn-OFF times.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>pZH</sub>	GND	V <sub>CC</sub>
t <sub>pZL</sub>	V <sub>CC</sub>	GND
t <sub>pHZ</sub>	GND	V <sub>CC</sub>
t <sub>pLZ</sub>	V <sub>CC</sub>	GND
others	open	pulse

Fig. 18 Test circuit for measuring AC performance.

Definitions for Figs 18 and 19:

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.

t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

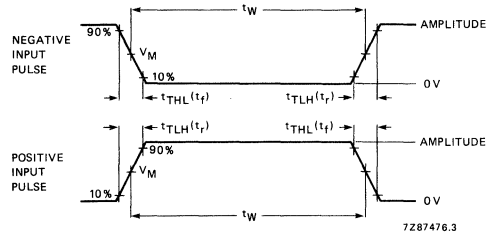


Fig. 19 Input pulse definitions.

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q<sub>0</sub> to Q<sub>9</sub>), an active LOW output from the most significant flip-flop ( $\bar{Q}_{5-9}$ ), active HIGH and active LOW clock inputs (CP<sub>0</sub> and  $\bar{CP}_1$ ) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP<sub>0</sub> while  $\bar{CP}_1$  is LOW or a HIGH-to-LOW transition at  $\bar{CP}_1$  while CP<sub>0</sub> is HIGH (see also function table).

When cascading counters, the  $\bar{Q}_{5-9}$  output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP<sub>0</sub> input of the next counter.

A HIGH on MR resets the counter to zero (Q<sub>0</sub> =  $\bar{Q}_{5-9}$  = HIGH; Q<sub>1</sub> to Q<sub>9</sub> = LOW) independent of the clock inputs (CP<sub>0</sub> and  $\bar{CP}_1$ ).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>0</sub> , $\bar{CP}_1$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	20	21	ns
f <sub>max</sub>	maximum clock frequency		77	67	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	35	36	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  
 $P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4017P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT4017T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q <sub>0</sub> to Q <sub>9</sub>	decoded outputs
8	GND	ground (0 V)
12	$\bar{Q}_{5-9}$	carry output (active LOW)
13	$\bar{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP <sub>0</sub>	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V <sub>CC</sub>	positive supply voltage

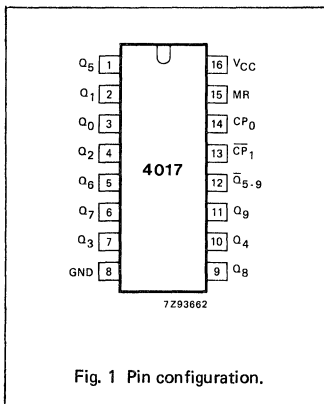


Fig. 1 Pin configuration.

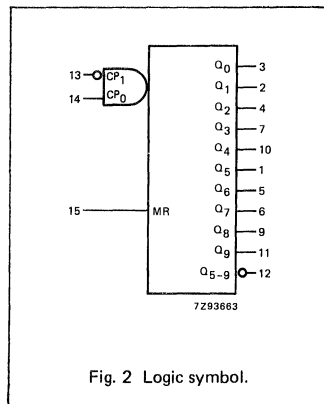


Fig. 2 Logic symbol.

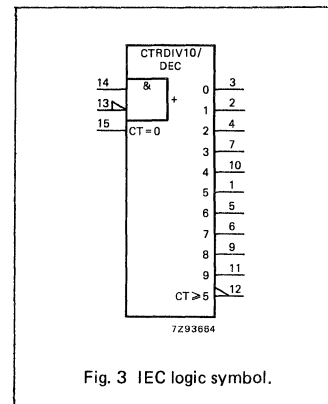


Fig. 3 IEC logic symbol.



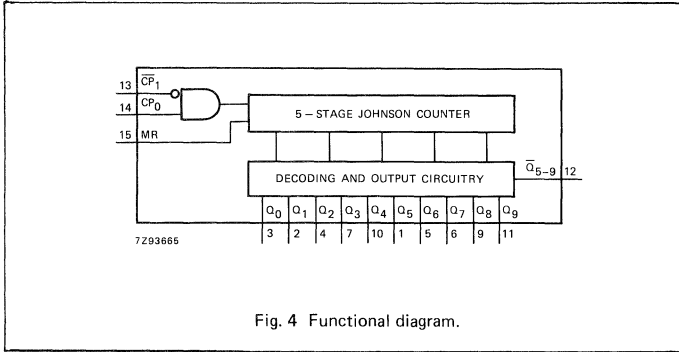


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	CP <sub>0</sub>	$\overline{\text{CP}}_1$	OPERATION
H	X	X	Q <sub>0</sub> = Q <sub>5-9</sub> = H; Q <sub>1</sub> to Q <sub>9</sub> = L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH clock transition  
↓ = HIGH-to-LOW clock transition

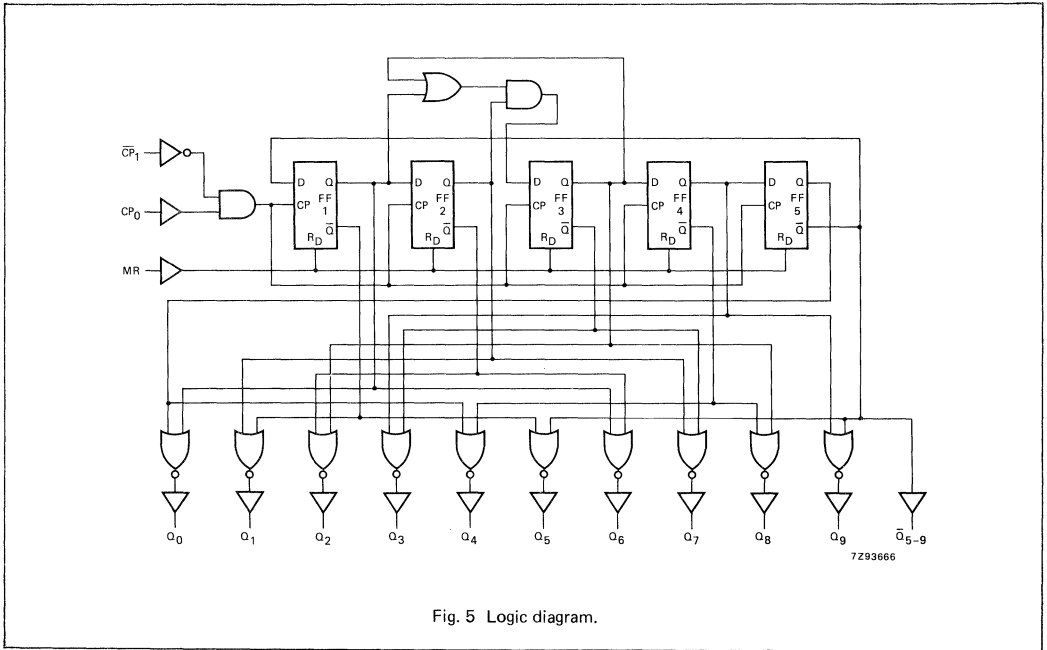


Fig. 5 Logic diagram.

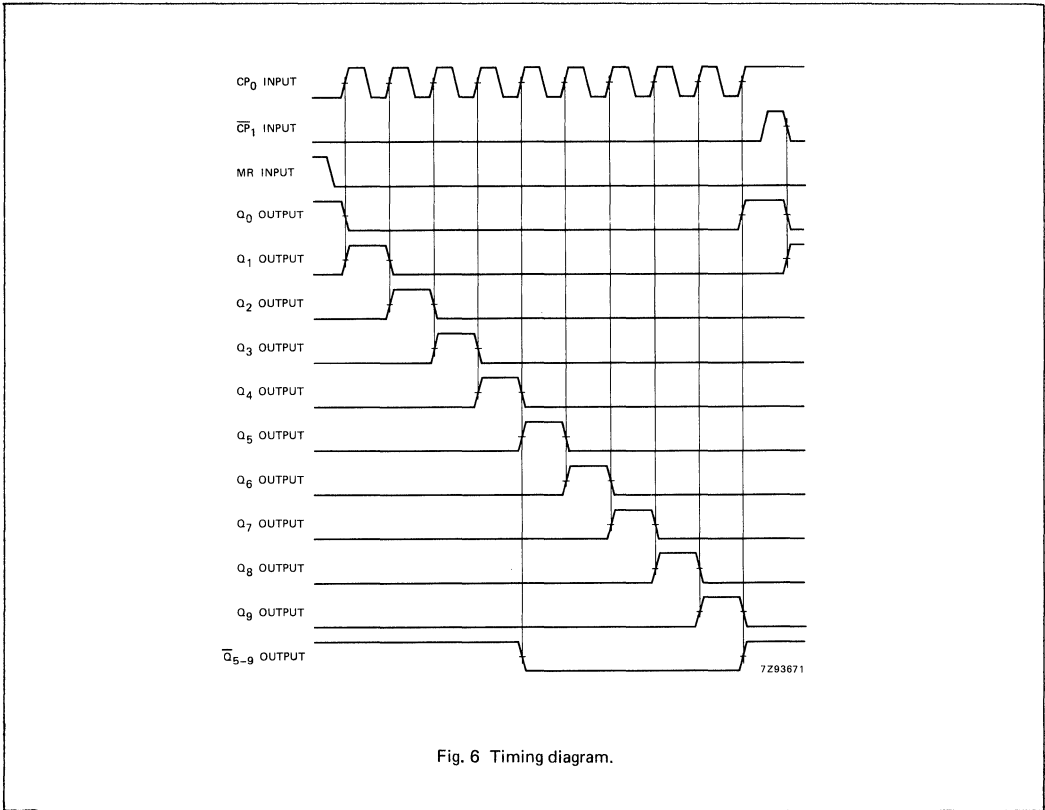


Fig. 6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>0</sub> to Q <sub>n</sub>		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>0</sub> to $\overline{Q}_{5,9}$		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>1</sub> to Q <sub>n</sub>		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>1</sub> to $\overline{Q}_{5,9}$		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to Q <sub>1-9</sub>		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t <sub>PLH</sub>	propagation delay MR to $\overline{Q}_{5,9}$ , Q <sub>0</sub>		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>rem</sub>	removal time MR to CP <sub>0</sub> , $\overline{CP}_1$	5 5 5	-17 -6 -5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time CP <sub>1</sub> to CP <sub>0</sub> ; CP <sub>0</sub> to $\overline{CP}_1$	50 10 9	-8 -3 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time CP <sub>0</sub> to $\overline{CP}_1$ ; CP <sub>1</sub> to CP <sub>0</sub>	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_1$	0.40
$CP_0$	0.25
MR	0.50

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $CP_0$ to $Q_n$		25	46		58		69	ns	4.5	Fig. 9
$t_{PHL}/t_{PLH}$	propagation delay $CP_0$ to $\overline{Q}_{5-9}$		25	46		58		69	ns	4.5	Fig. 9
$t_{PHL}/t_{PLH}$	propagation delay $CP_1$ to $Q_n$		25	50		63		75	ns	4.5	Fig. 9
$t_{PHL}/t_{PLH}$	propagation delay $CP_1$ to $\overline{Q}_{5-9}$		25	50		63		75	ns	4.5	Fig. 9
$t_{PHL}/t_{PLH}$	propagation delay MR to $Q_{1-9}$		22	46		58		69	ns	4.5	Fig. 8
$t_{PLH}$	propagation delay MR to $\overline{Q}_{5-9}, Q_0$		20	46		58		69	ns	4.5	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig. 9
$t_W$	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
$t_W$	master reset pulse width; HIGH	16	4		20		24		ns	4.5	Fig. 8
$t_{rem}$	removal time MR to $CP_0, \overline{CP}_1$	5	-5		5		5		ns	4.5	Fig. 8
$t_{su}$	set-up time $CP_1$ to $CP_0$ ; $CP_0$ to $\overline{CP}_1$	10	-3		13		15		ns	4.5	Fig. 7
$t_h$	hold time $CP_0$ to $\overline{CP}_1$ ; $\overline{CP}_1$ to $CP_0$	10	6		13		15		ns	4.5	Fig. 7
$f_{max}$	maximum clock pulse frequency	30	61		24		20		MHz	4.5	Fig. 8

AC WAVEFORMS

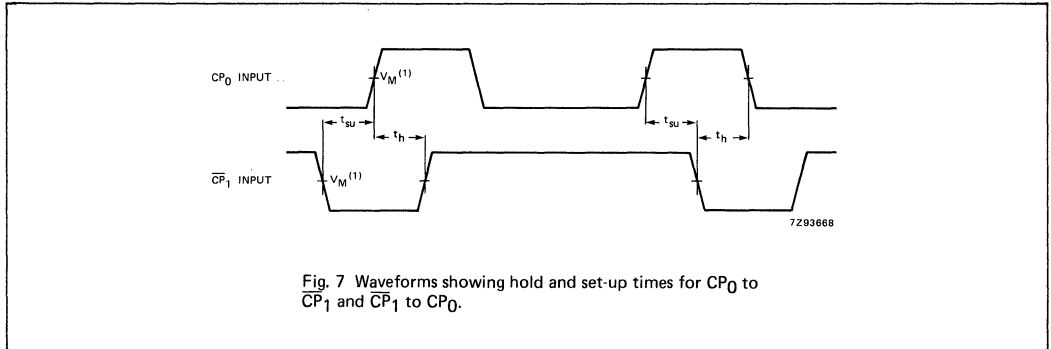


Fig. 7 Waveforms showing hold and set-up times for CP<sub>0</sub> to CP<sub>1</sub> and CP<sub>1</sub> to CP<sub>0</sub>.

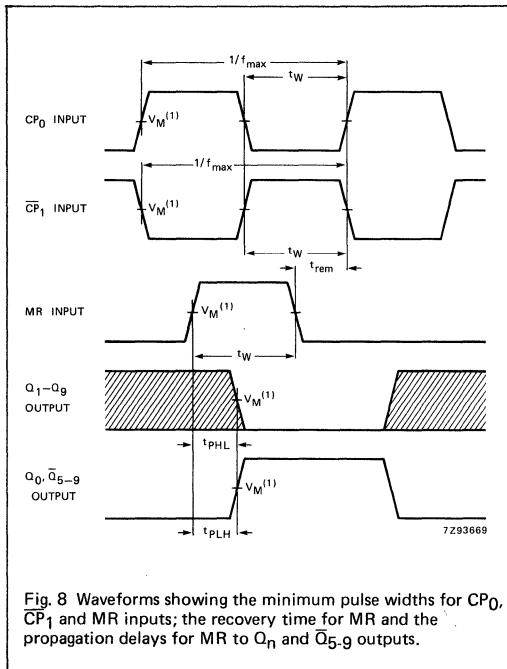


Fig. 8 Waveforms showing the minimum pulse widths for CP<sub>0</sub>, CP<sub>1</sub> and MR inputs; the recovery time for MR and the propagation delays for MR to Q<sub>n</sub> and Q<sub>5.9</sub> outputs.

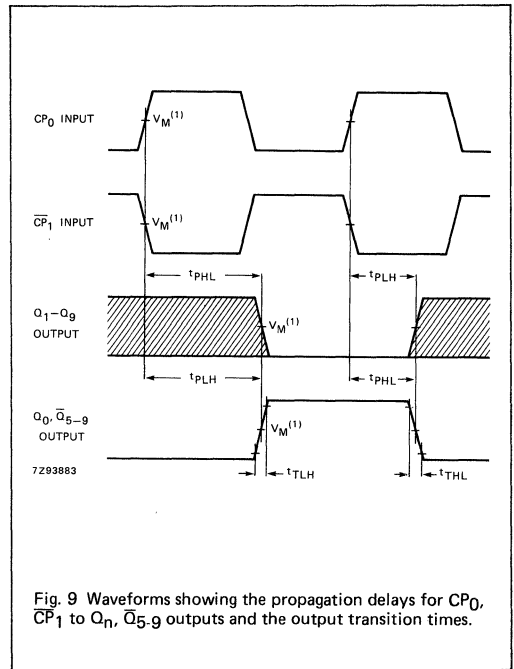


Fig. 9 Waveforms showing the propagation delays for CP<sub>0</sub>, CP<sub>1</sub> to Q<sub>n</sub>, Q<sub>5.9</sub> outputs and the output transition times.

Note to Figs 8 and 9

Conditions:  
CP<sub>1</sub> = LOW while CP<sub>0</sub> is triggered on a LOW-to-HIGH transition and CP<sub>0</sub> = HIGH, while CP<sub>1</sub> is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

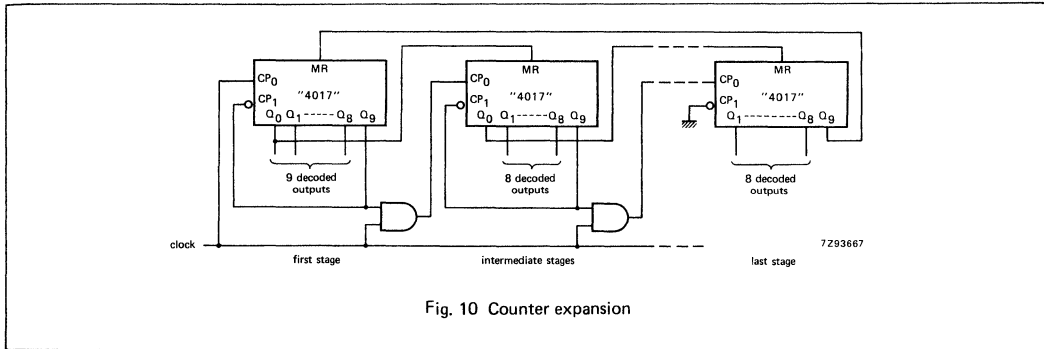
(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

## APPLICATION INFORMATION

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017". Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

**Note to Fig. 10**

It is essential not to enable the counter on  $\overline{CP_1}$  when  $CP_0$  is HIGH, or on  $CP_0$  when  $\overline{CP_1}$  is LOW, as this would cause an extra count.



## 14-STAGE BINARY RIPPLE COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs ( $Q_0, Q_3$  to  $Q_{13}$ ). The counter is advanced on the HIGH-to-LOW transition of  $\overline{CP}$ .

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ .

Each counter stage is a static toggle flip-flop.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{CP}$ to $Q_0$ $Q_n$ to $Q_{n+1}$ MR to $Q_n$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	11	15	ns
			6	6	ns
			17	19	ns
$f_{max}$	maximum clock frequency		101	52	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	19	20	pF

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz       $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

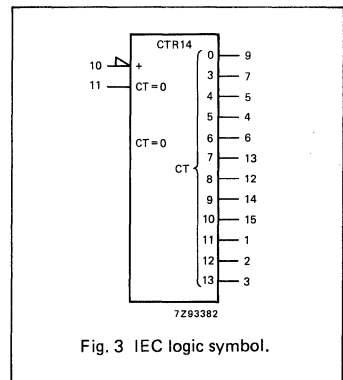
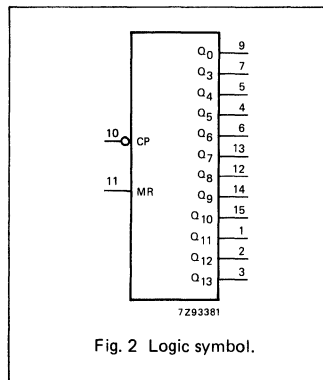
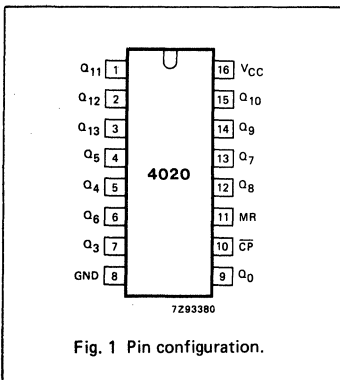
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4020P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4020T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	$Q_0, Q_3$ to $Q_{13}$	parallel outputs
8	GND	ground (0 V)
10	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	$V_{CC}$	positive supply voltage





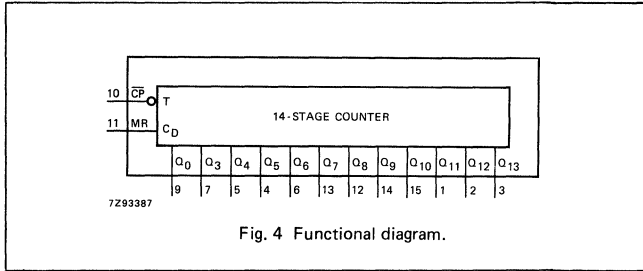


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	$Q_0, Q_3$ to $Q_{13}$
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition  
 ↓ = HIGH-to-LOW clock transition

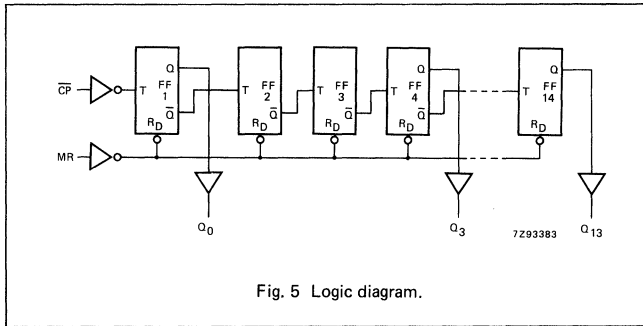


Fig. 5 Logic diagram.

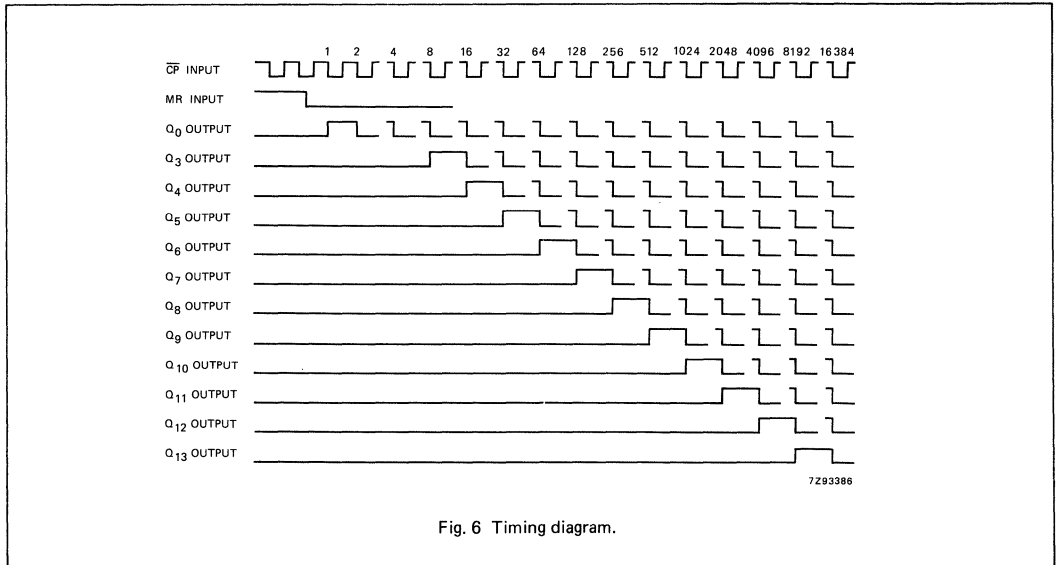


Fig. 6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		22 8 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		55 20 16	170 34 29		215 43 37		225 51 43	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	clock pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>rem</sub>	removal time MR to $\overline{CP}$	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	30 92 109		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{CP}$ to Q <sub>0</sub>		18	36		45		54	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		8	15		19		22	ns	4.5	Fig. 7
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		22	45		56		68	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7
t <sub>W</sub>	clock pulse width HIGH	20	7		25		30		ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	20	8		25		30		ns	4.5	Fig. 8
t <sub>rem</sub>	removal time MR to $\overline{CP}$	10	2		13		15		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	25	47		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS

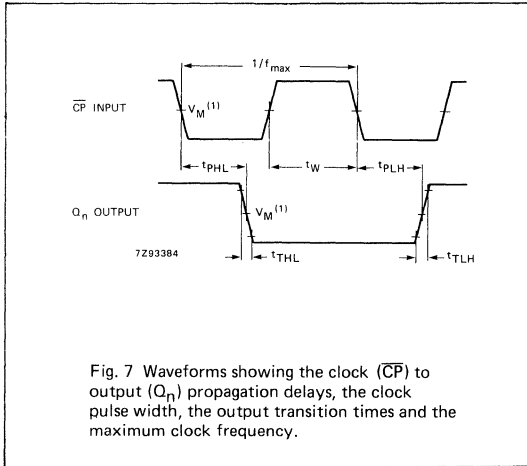


Fig. 7 Waveforms showing the clock ( $\overline{CP}$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

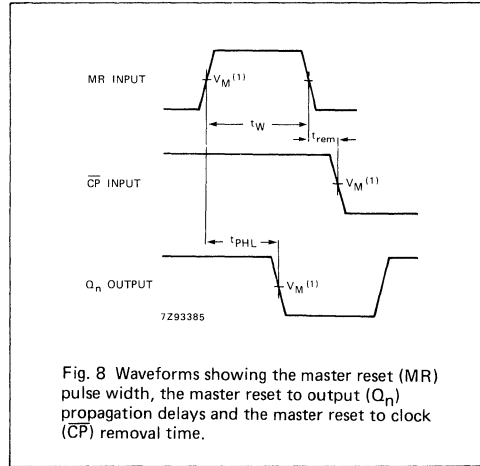


Fig. 8 Waveforms showing the master reset (MR) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{CP}$ ) removal time.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

ASOTIC



ASOTIC

ASOTIC

## 7-STAGE BINARY RIPPLE COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the "4024" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4024 are 7-stage binary ripple counters with a clock input (CP), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q<sub>0</sub> to Q<sub>6</sub>).

The counter advances on the HIGH-to-LOW transition of CP.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP.

Each counter stage is a static toggle flip-flop.

### APPLICATIONS

- Frequency dividing circuits
- Time delay circuits

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14	14	ns
f <sub>max</sub>	maximum clock frequency		90	70	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	25	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

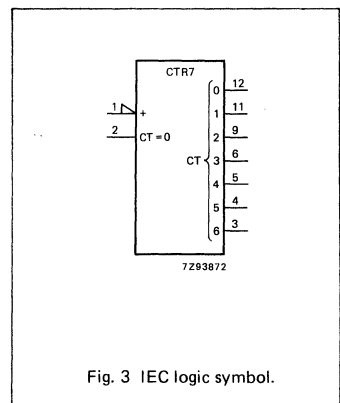
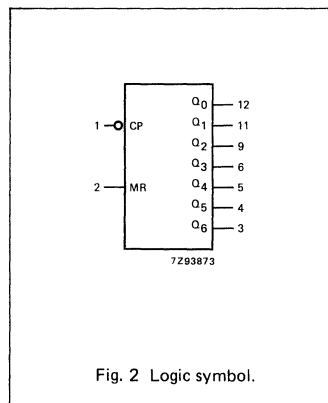
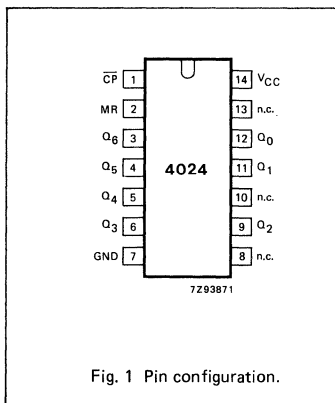
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4024P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT4024T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q <sub>0</sub> to Q <sub>6</sub>	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	V <sub>CC</sub>	positive supply voltage



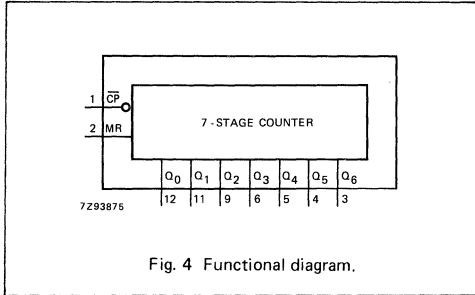


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	$Q_n$
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

↓ = HIGH-to-LOW clock transition

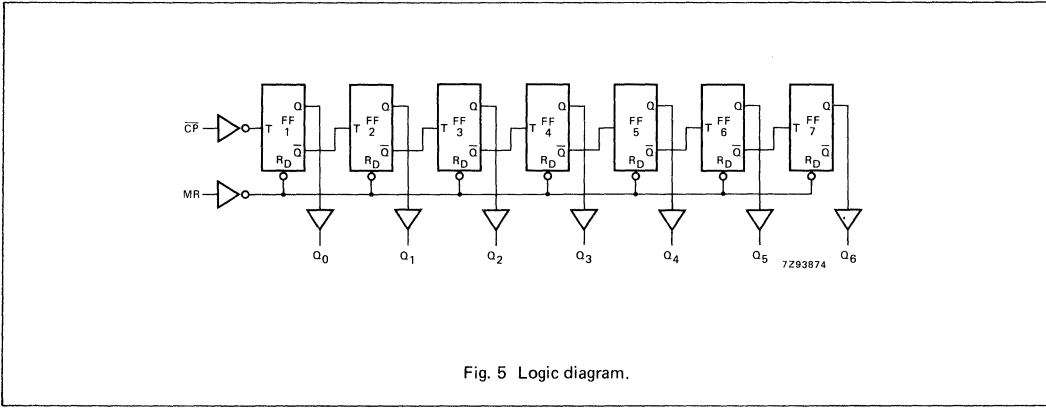


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>0</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		25 9 7	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>rem</sub>	removal time MR to CP	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6



**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

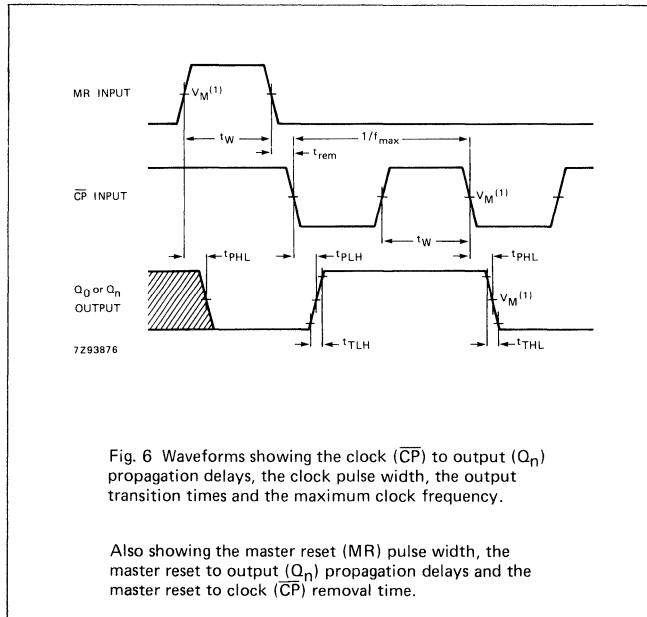
INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.75
MR	0.85

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		17	35		44		53	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>0</sub>		21	40		50		60	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		9	16		20		24	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig. 6
t <sub>rem</sub>	removal time MR to CP	10	0		13		15		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig. 6

## AC WAVEFORMS



## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



## 12-STAGE BINARY RIPPLE COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the "4040" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4040 are 12-stage binary ripple counters with a clock input (CP), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q<sub>0</sub> to Q<sub>11</sub>).

The counter advances on the HIGH-to-LOW transition of CP.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP.

Each counter stage is a static toggle flip-flop.

### APPLICATIONS

- Frequency dividing circuits
- Time delay circuits
- Control counters

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub> Q <sub>n</sub> to Q <sub>n+1</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	14 8	16 8	ns ns
f <sub>max</sub>	maximum clock frequency		90	79	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	20	20	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

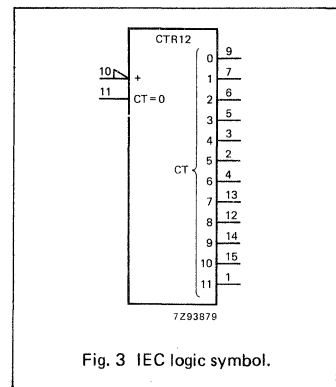
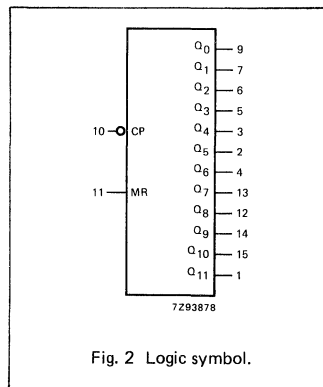
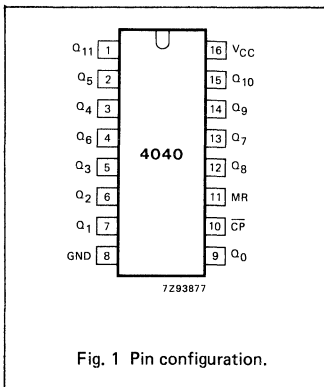
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4040P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4040T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q <sub>0</sub> to Q <sub>11</sub>	parallel outputs
10	CP	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V <sub>CC</sub>	positive supply voltage



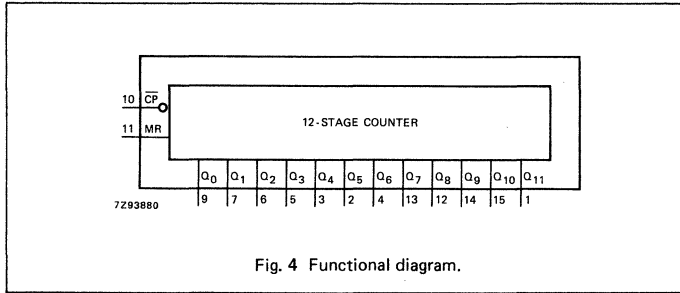


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	$Q_n$
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition  
 ↓ = HIGH-to-LOW clock transition

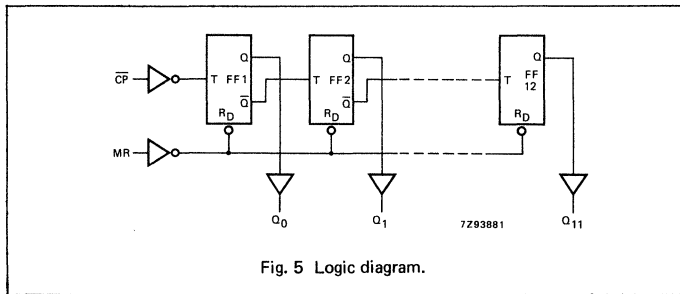


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	master reset pulse width; HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>rem</sub>	removal time MR to CP	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.85
MR	1.10

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>0</sub>		19	40		50		60	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		10	20		25		30	ns	4.5	Fig. 6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		23	45		56		68	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t <sub>W</sub>	master reset pulse width; HIGH	16	6		20		24		ns	4.5	Fig. 6
t <sub>rem</sub>	removal time MR to CP	10	2		13		15		ns	4.5	Fig. 6
f <sub>max</sub>	maximum clock pulse frequency	30	72		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

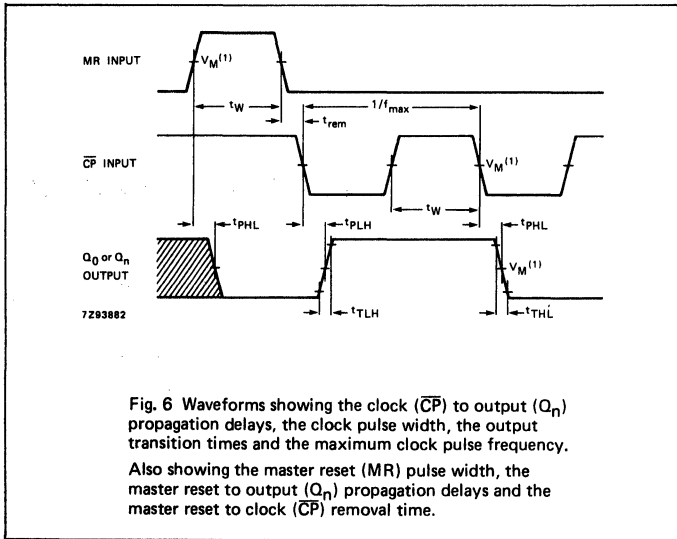


Fig. 6 Waveforms showing the clock ( $\overline{CP}$ ) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency. Also showing the master reset (MR) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock ( $\overline{CP}$ ) removal time.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





PHASE-LOCKED-LOOP WITH VCO

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at  $V_{CC} = 4.5\text{ V}$
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- $I_{CC}$  category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$f_o$	VCO centre frequency	$C1 = 40\text{ pF}$ $R1 = 3\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	18	18	MHz
$C_I$	input capacitance (pin 5)		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	note 1	38	39	pF

$GND = 0\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$

Note 1

Applies to phase comparator section only (VCO disabled). For power dissipation of VCO and demodulator sections see Figs 22, 23 and 24.

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4046AP: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT4046AT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

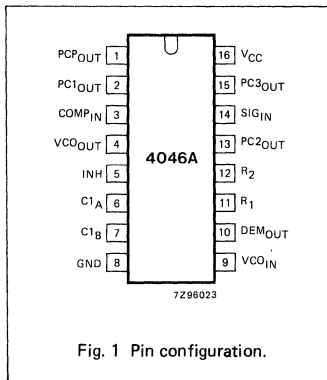


Fig. 1 Pin configuration.

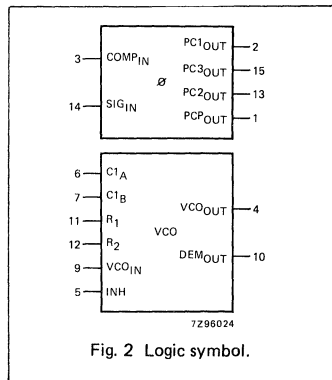


Fig. 2 Logic symbol.

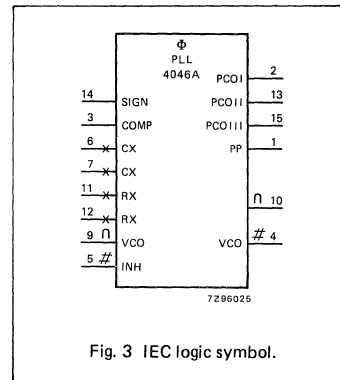


Fig. 3 IEC logic symbol.

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP <sub>OUT</sub>	phase comparator pulse output
2	PC1 <sub>OUT</sub>	phase comparator 1 output
3	COMP <sub>IN</sub>	comparator input
4	VCO <sub>OUT</sub>	VCO output
5	INH	inhibit input
6	C1 <sub>A</sub>	capacitor C1 connection A
7	C1 <sub>B</sub>	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO <sub>IN</sub>	VCO input
10	DEM <sub>OUT</sub>	demodulator output
11	R <sub>1</sub>	resistor R1 connection
12	R <sub>2</sub>	resistor R2 connection
13	PC2 <sub>OUT</sub>	phase comparator 2 output
14	SIG <sub>IN</sub>	signal input
15	PC3 <sub>OUT</sub>	phase comparator 3 output
16	V <sub>CC</sub>	positive supply voltage

## GENERAL DESCRIPTION (Cont'd)

## VCO

The VCO requires one external capacitor C1 (between C1<sub>A</sub> and C1<sub>B</sub>) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM<sub>OUT</sub>). In contrast to conventional techniques where the DEM<sub>OUT</sub> voltage is one threshold voltage lower than the VCO input voltage, here the DEM<sub>OUT</sub> voltage equals that of the VCO input. If DEM<sub>OUT</sub> is used, a load resistor (R<sub>S</sub>) should be connected from DEM<sub>OUT</sub> to GND; if unused, DEM<sub>OUT</sub> should be left open. The VCO output (VCO<sub>OUT</sub>) can be connected directly to the comparator input (COMP<sub>IN</sub>), or connected via a frequency-divider. The VCO output signal has a guaranteed duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

## Phase comparators

The signal input (SIG<sub>IN</sub>) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

## Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f<sub>i</sub>) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple (f<sub>r</sub> = 2f<sub>i</sub>) is suppressed, is:

$$V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where V<sub>DEMOUT</sub> is the demodulator output at pin 10;

V<sub>DEMOUT</sub> = V<sub>PC1OUT</sub> (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V<sub>DEMOUT</sub>'), is the resultant of the phase differences of signals (SIG<sub>IN</sub>) and the comparator input (COMP<sub>IN</sub>) as shown in Fig. 6. The average of V<sub>DEMOUT</sub>' is equal to 1/2 V<sub>CC</sub> when there is no signal

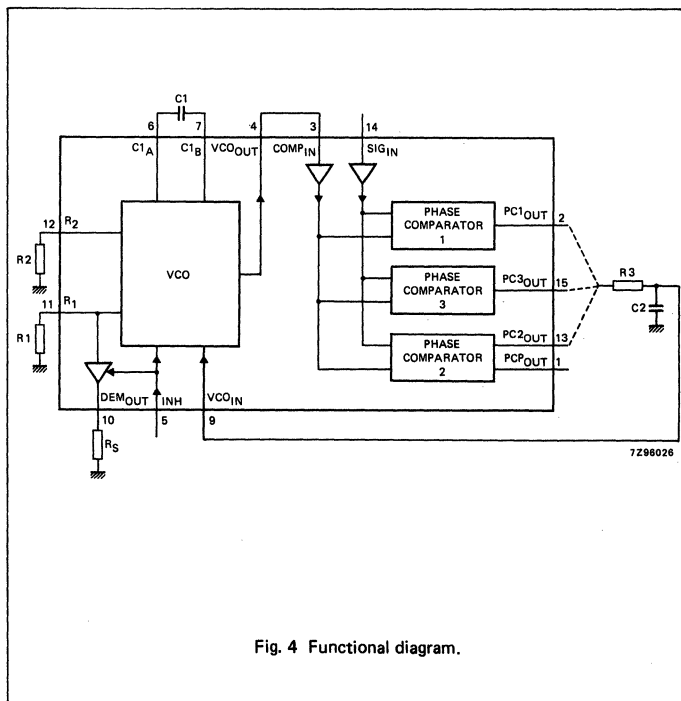


Fig. 4 Functional diagram.

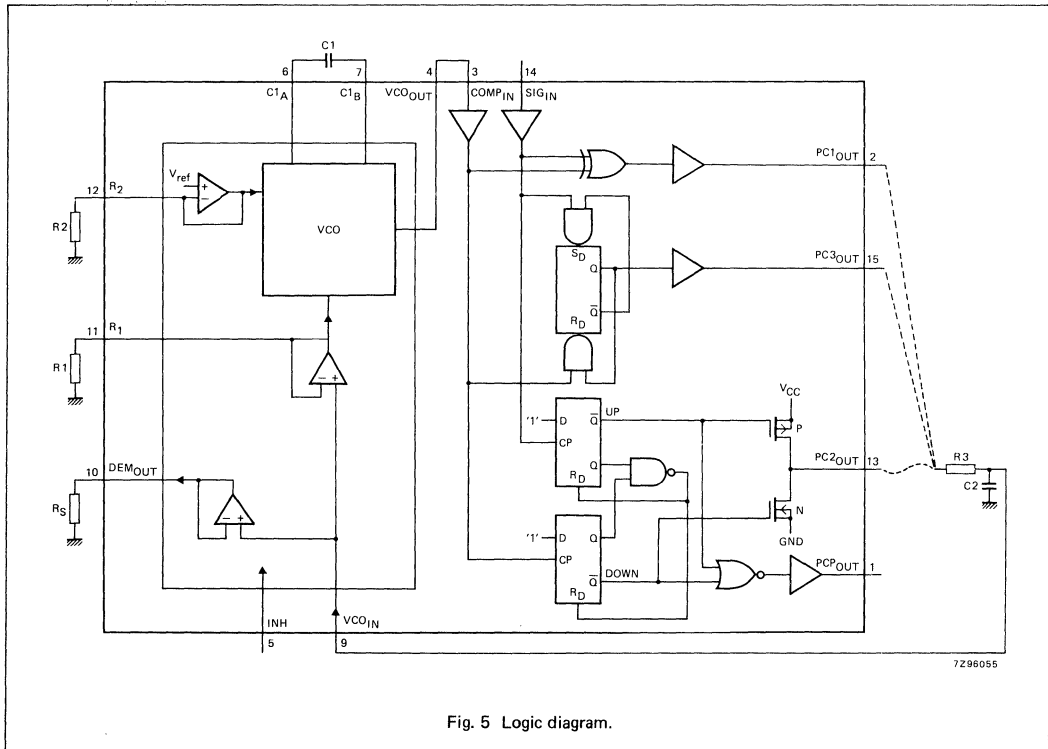


Fig. 5 Logic diagram.

or noise at SIG<sub>IN</sub> and with this input the VCO oscillates at the centre frequency (f<sub>0</sub>). Typical waveforms for the PC1 loop locked at f<sub>0</sub> are shown in Fig. 7.

The frequency capture range (2f<sub>c</sub>) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range (2f<sub>L</sub>) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. One typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

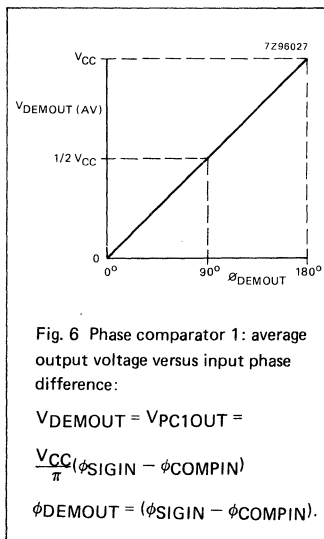


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$$V_{DEMOUT} = V_{PC1OUT} =$$

$$\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\theta_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN}).$$

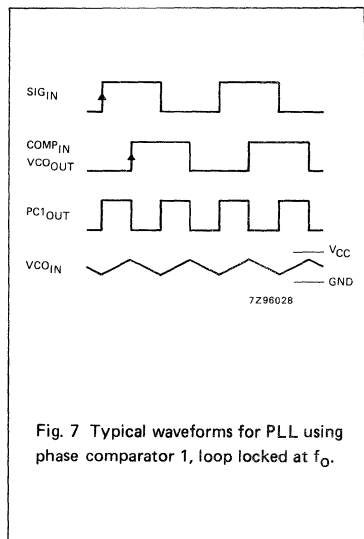


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f<sub>0</sub>.

**GENERAL DESCRIPTION (Cont'd)**

**Phase comparators (Cont'd)**

*Phase comparator 2 (PC2)*

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG<sub>IN</sub> and COMP<sub>IN</sub> are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG<sub>IN</sub> causes an up-count and COMP<sub>IN</sub> a down-count. The transfer function of PC2, assuming ripple ( $f_r = f_i$ ) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where  $V_{DEMOUT}$  is the demodulator output at pin 10;

$V_{DEMOUT} = V_{PC2OUT}$  (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{DEMOUT}$ ), is the resultant of the phase differences of SIG<sub>IN</sub> and COMP<sub>IN</sub> as shown in Fig. 8. Typical waveforms for the PC2 loop locked at  $f_0$  are shown in Fig. 9.

When the frequencies of SIG<sub>IN</sub> and COMP<sub>IN</sub> are equal but the phase of SIG<sub>IN</sub> leads that of COMP<sub>IN</sub>, the p-type output driver at PC2OUT is held "ON" for a time corresponding to the phase difference ( $\phi_{DEMOUT}$ ). When the phase of SIG<sub>IN</sub> lags that of COMP<sub>IN</sub>, the n-type driver is held "ON".

When the frequency of SIG<sub>IN</sub> is higher than that of COMP<sub>IN</sub>, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the SIG<sub>IN</sub> frequency is lower than the COMP<sub>IN</sub> frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the

voltage at the capacitor (C2) of the low-pass filter connected to PC2OUT varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCPOUT) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG<sub>IN</sub> and COMP<sub>IN</sub> over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG<sub>IN</sub> the VCO adjusts, via PC2, to its lowest frequency.

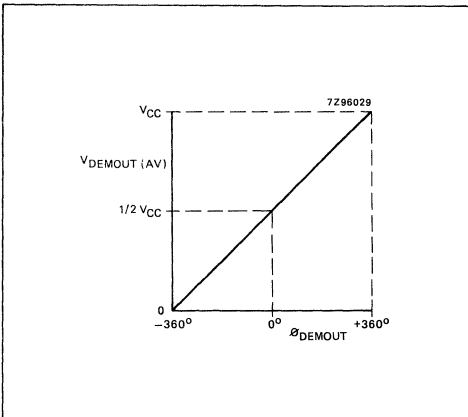


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:

$$V_{DEMOUT} = V_{PC2OUT} =$$

$$\frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN}).$$

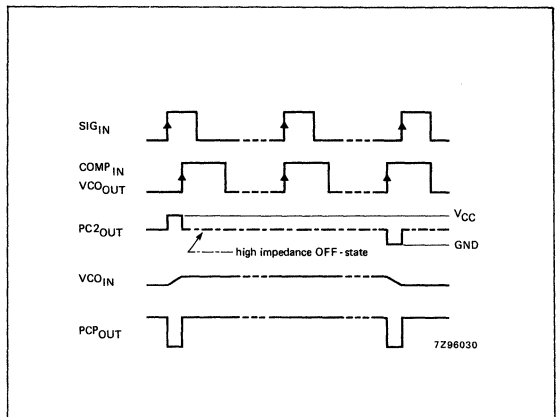


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at  $f_0$ .

**Phase comparator 3 (PC3)**

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG<sub>IN</sub> and COMP<sub>IN</sub> are not important. The transfer characteristic of PC3, assuming ripple ( $f_r = f_i$ ) is suppressed, is:

$$V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{2\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where  $V_{\text{DEMOUT}}$  is the demodulator output at pin 10;

$V_{\text{DEMOUT}} = V_{\text{PC3OUT}}$  (via low-pass filter).

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of SIG<sub>IN</sub> and COMP<sub>IN</sub> as shown in Fig. 10. Typical waveforms for the PC3 loop locked at  $f_0$  are shown in Fig. 11.

The phase-to-output response characteristic of PC3 (Fig. 10) differs from that of PC2 in that the phase angle between SIG<sub>IN</sub> and COMP<sub>IN</sub> varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple

content of the VCO input signal is higher. With no signal present at SIG<sub>IN</sub> the VCO adjusts, via PC3, to its highest frequency.

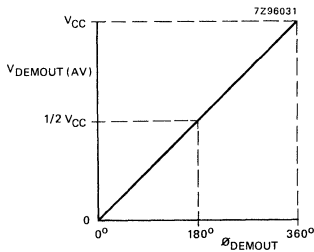


Fig. 10 Phase comparator 3: average output voltage versus input phase difference:

$$V_{\text{DEMOUT}} = V_{\text{PC3OUT}} =$$

$$\frac{V_{\text{CC}}}{2\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}}).$$

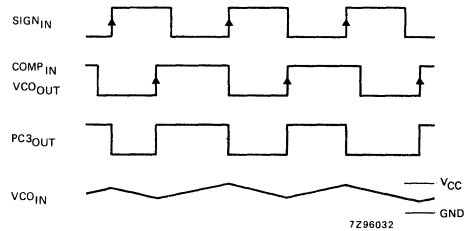


Fig. 11 Typical waveforms for PLL using phase comparator 3, loop locked at  $f_0$ .

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V <sub>CC</sub>	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V <sub>CC</sub>	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V <sub>I</sub>	DC input voltage range	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
V <sub>O</sub>	DC output voltage range	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V	
T <sub>amb</sub>	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T <sub>amb</sub>	operating ambient temperature range	-40		+125	-40		+125	°C	
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V <sub>CC</sub>	DC supply voltage	-0.5	+7	V	
±I <sub>IK</sub>	DC input diode current except C1 <sub>A</sub> , C1 <sub>B</sub>		20	mA	for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V
±I <sub>IK</sub>	DC input diode current C1 <sub>A</sub> , C1 <sub>B</sub>		10	mA	for V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V
±I <sub>OK</sub>	DC output diode current		20	mA	for V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V
±I <sub>O</sub>	DC output source or sink current		25	mA	for -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V
±I <sub>CC</sub> ; ±I <sub>GND</sub>	DC V <sub>CC</sub> or GND current		50	mA	
T <sub>stg</sub>	storage temperature range	-65	+150	°C	
P <sub>tot</sub>	power dissipation per package				for temperature range: -40 to +125 °C
	plastic DIL		500	mW	74HC/HCT above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

## DC CHARACTERISTICS FOR 74HC

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded

## Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8	0.5 1.35 1.8	V	2.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage PC <sub>OUT</sub> , PC <sub>nOUT</sub>	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage PC <sub>OUT</sub> , PC <sub>nOUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage PC <sub>OUT</sub> , PC <sub>nOUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage PC <sub>OUT</sub> , PC <sub>nOUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0	5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V <sub>CC</sub> or GND		
±I <sub>OZ</sub>	3-state OFF-state current PC <sub>2OUT</sub>			0.5		5.0	10.0	μA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		800 250 150					kΩ	3.0 4.5 6.0		V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 12, 13 and 14	



## DC CHARACTERISTICS FOR 74HC (Cont'd)

## VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS		
		74HC									V <sub>CC</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V <sub>IH</sub>	HIGH level input voltage INH	2.1 3.15 4.2	1.2 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage INH		0.8 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND		
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1	
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1	
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0			
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	0.9 0.9 0.9		1.9 3.2 4.6					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21. Refer to note 2	

## Notes

1. The parallel value of R1 and R2 should be more than 2.7 kΩ.
2. The maximum operating voltage can be as high as V<sub>CC</sub> - 0.9 V, however, this may result in an increased offset voltage.

**Demodulator section**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
R <sub>S</sub>	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>
V <sub>OFF</sub>	offset voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>		±30 ±20 ±10						mV	3.0 4.5 6.0	V <sub>I</sub> = V <sub>COIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig. 15
R <sub>D</sub>	dynamic output resistance at V <sub>DEMOUT</sub>		25 25 25						Ω	3.0 4.5 6.0	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC1 <sub>OUT</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 16
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC <sub>2OUT</sub>		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 16
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC3 <sub>OUT</sub>		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 16
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 16
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC2 <sub>OUT</sub>		83 30 24	280 56 48		350 70 60		420 84 71.4	ns	2.0 4.5 6.0	Fig. 17
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC2 <sub>OUT</sub>		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 17
V <sub>I(p-p)</sub>	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>1IN</sub> or COMP <sub>1IN</sub>		0.05 0.05 0.05 0.05						V	2.0 3.0 4.5 6.0	f <sub>i</sub> = 1 MHz C <sub>L</sub> = 15 pF

VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.				max.
Δf/T	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	V <sub>I</sub> = V <sub>VCO1N</sub> = 1/2 V <sub>CC</sub> ; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18
f <sub>o</sub>	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V <sub>VCO1N</sub> = 1/2 V <sub>CC</sub> ; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf <sub>VCO</sub>	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ <sub>VCO</sub>	duty factor at VCO <sub>OUT</sub>		50 50 50						%	3.0 4.5 6.0	

## DC CHARACTERISTICS FOR 74HCT

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded

## Note

1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given above.  
To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT (Cont'd)

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	3.15	2.4					V	4.5			
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		2.1	1.35				V	4.5			
V <sub>OH</sub>	HIGH level output voltage PC <sub>POUT</sub> , PC <sub>nOUT</sub>	4.4	4.5		4.4		4.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage PC <sub>POUT</sub> , PC <sub>nOUT</sub>	3.98	4.32		3.84		3.7	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA	
V <sub>OL</sub>	LOW level output voltage PC <sub>POUT</sub> , PC <sub>nOUT</sub>		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage PC <sub>POUT</sub> , PC <sub>nOUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			30		38		45	μA	5.5	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current PC <sub>2OUT</sub>			0.5		5.0		10.0	μA	5.5	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		250						kΩ	4.5	V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 12, 13 and 14	

## DC CHARACTERISTICS FOR 74HCT (Cont'd)

## VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	4.4	4.5		4.4		4.4		<sup>s</sup> V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40		0.47		0.54	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0		1.0	μA	5.5	V <sub>CC</sub> or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	0.9		3.2					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21. Refer to note 2

## Notes

1. The parallel value of R1 and R2 should be more than 2.7 kΩ.
2. The maximum operating voltage can be as high as V<sub>CC</sub> - 0.9 V, however, this may result in an increased offset voltage.

DC CHARACTERISTICS FOR 74HCT (Cont'd)

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
R <sub>S</sub>	resistor range	50		300				kΩ	4.5	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>	
V <sub>OFF</sub>	offset voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>		±20					mV	4.5	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig. 15	
R <sub>D</sub>	dynamic output resistance at DEM <sub>OUT</sub>		25					Ω	4.5	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>	

## AC CHARACTERISTICS FOR 74HCT

## Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>		26	45		56		68	ns	4.5	Fig. 16
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		38	68		85		102	ns	4.5	Fig. 16
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC3 <sub>OUT</sub>		34	60		75		90	ns	4.5	Fig. 16
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 16
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		35	60		75		90	ns	4.5	Fig. 17
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		40	70		88		105	ns	4.5	Fig. 17
V <sub>I</sub> (p-p)	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>		0.05						V	4.5	f <sub>i</sub> = 1 MHz C <sub>L</sub> = 15 pF

## VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.				max.
Δf/T	frequency stability with temperature change				0.15				%/K	4.5	V <sub>I</sub> = V <sub>VCOIN</sub> within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18b
f <sub>o</sub>	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf <sub>VCO</sub>	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ <sub>VCO</sub>	duty factor at VCO <sub>OUT</sub>		50						%	4.5	



FIGURE REFERENCES FOR DC CHARACTERISTICS

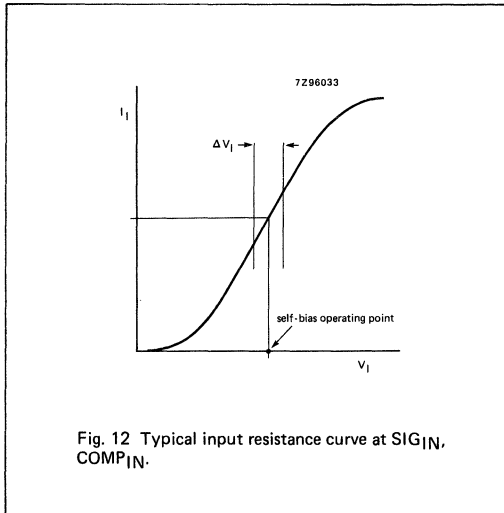


Fig. 12 Typical input resistance curve at SIG<sub>1N</sub>, COMP<sub>1N</sub>.

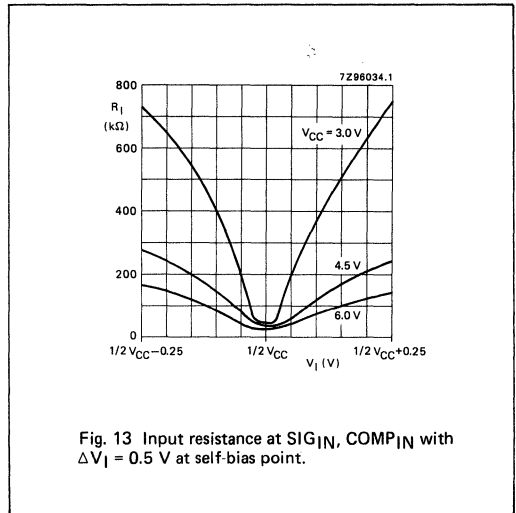


Fig. 13 Input resistance at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_I = 0.5$  V at self-bias point.

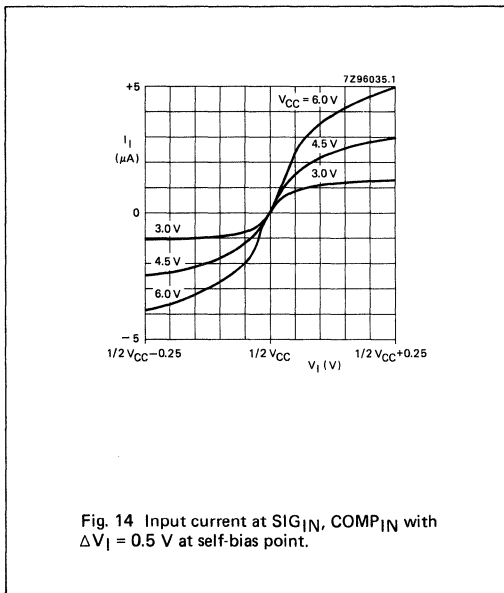


Fig. 14 Input current at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_I = 0.5$  V at self-bias point.

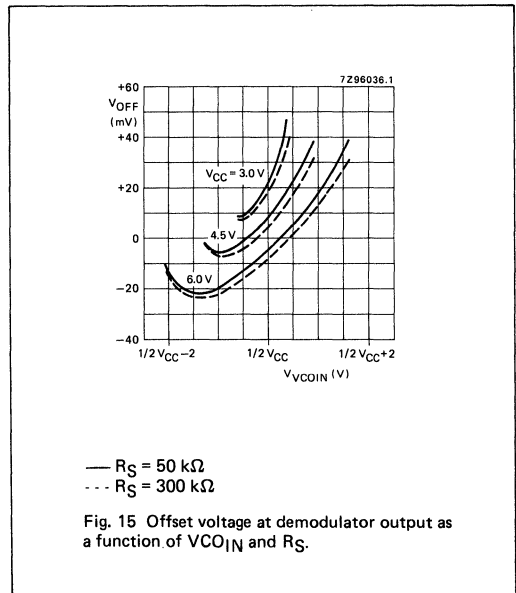


Fig. 15 Offset voltage at demodulator output as a function of VCO<sub>1N</sub> and  $R_S$ .

AC WAVEFORMS

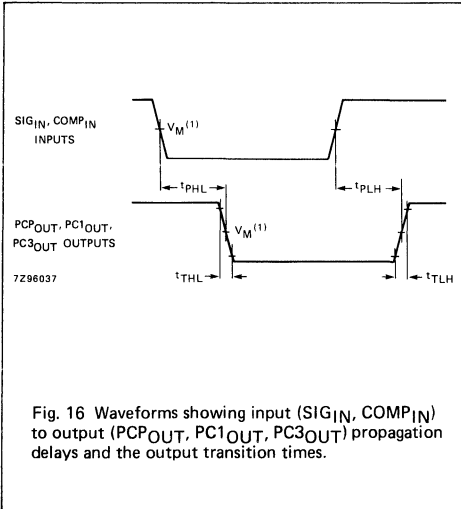


Fig. 16 Waveforms showing input (SIG1N, COMP1N) to output (PCP0UT, PC10UT, PC30UT) propagation delays and the output transition times.

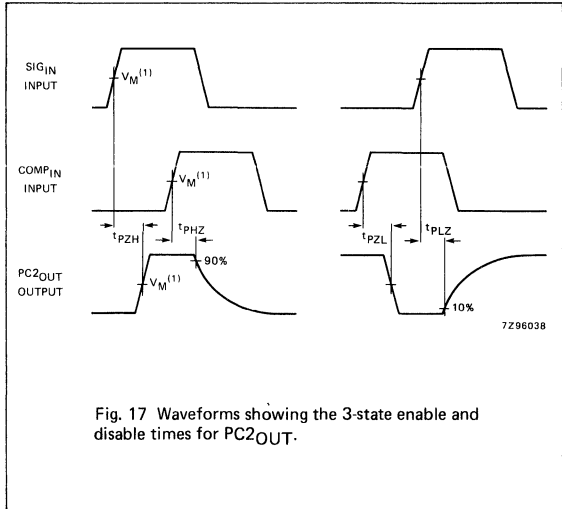
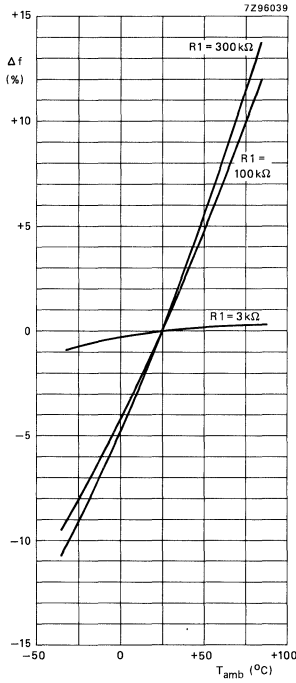


Fig. 17 Waveforms showing the 3-state enable and disable times for PC20UT.

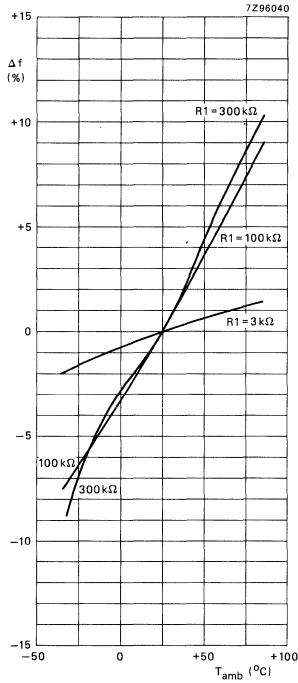
Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

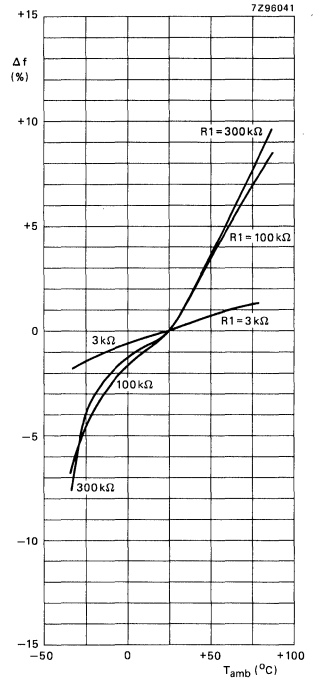
AC WAVEFORMS (Continued)



(a)  $V_{CC} = 3.0\text{ V}$

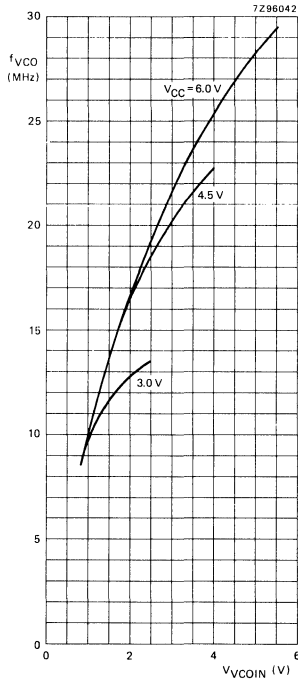


(b)  $V_{CC} = 4.5\text{ V}$

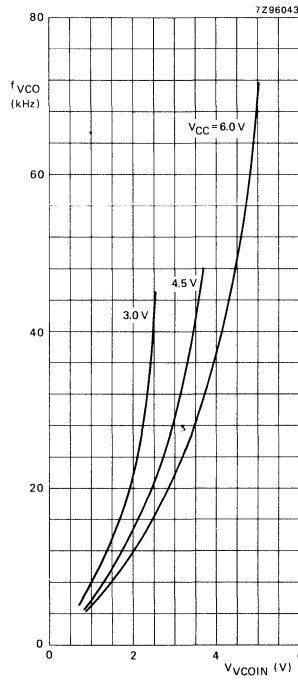


(c)  $V_{CC} = 6.0\text{ V}$

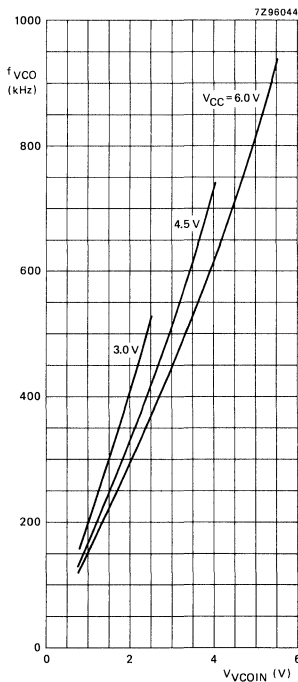
Fig. 18 Frequency stability versus ambient temperature:  $C1 = 100\text{ pF}$ ;  $R2 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ .



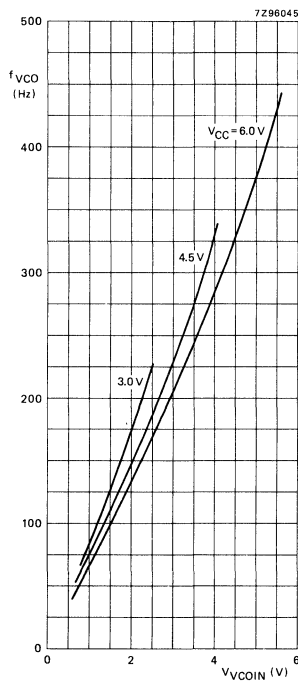
(a)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(b)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$



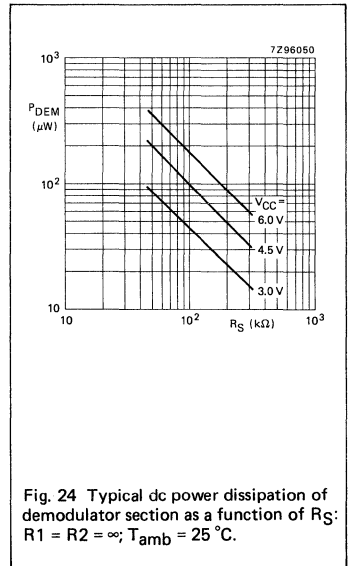
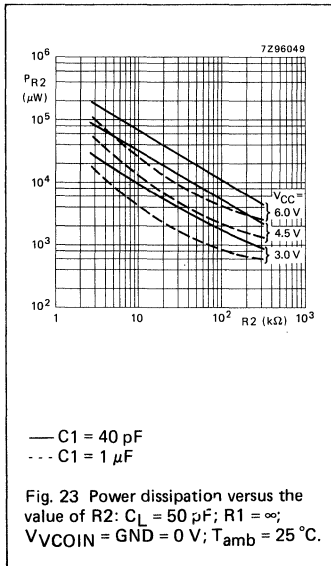
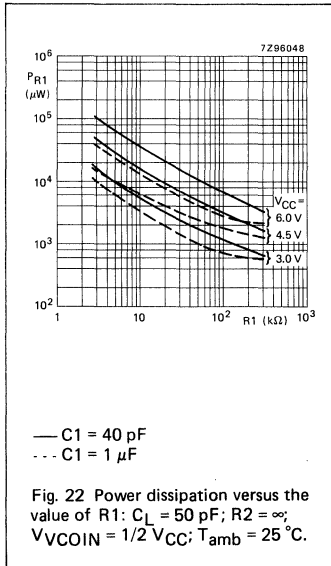
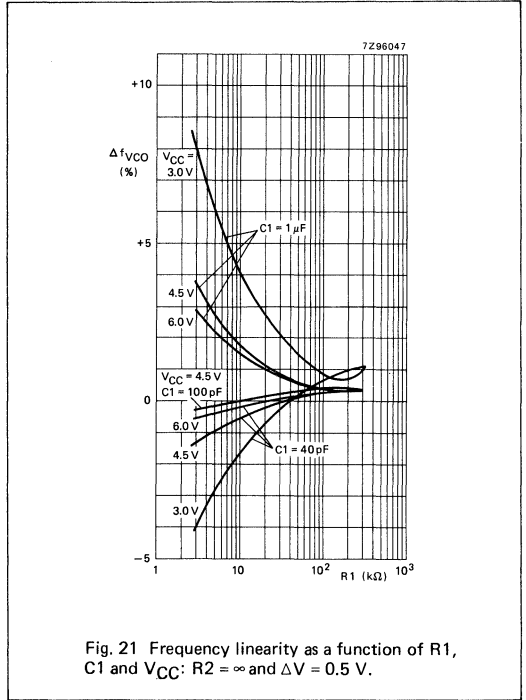
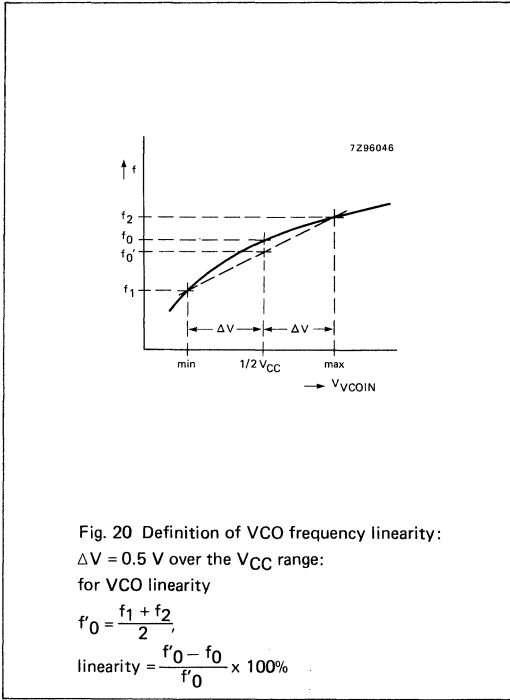
(c)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(d)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$

Fig. 19 Graphs showing VCO frequency ( $f_{VCO}$ ) as a function of the VCO input voltage ( $V_{VCOIN}$ ).

AC WAVEFORMS (Continued)



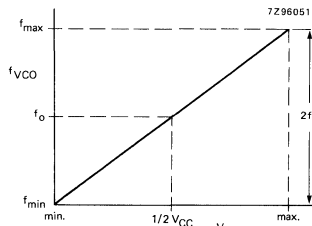
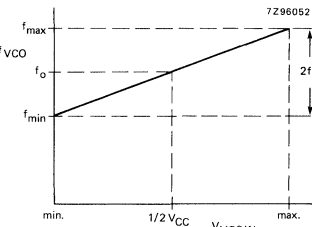
## APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-locked-loop system.

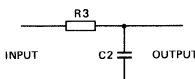
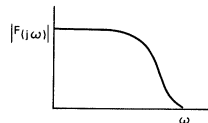
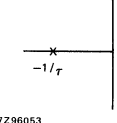
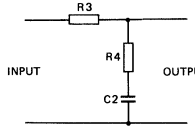
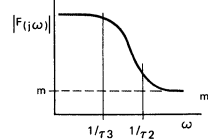
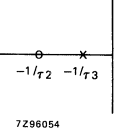
References should be made to Figs 29, 30 and 31 as indicated in the table.

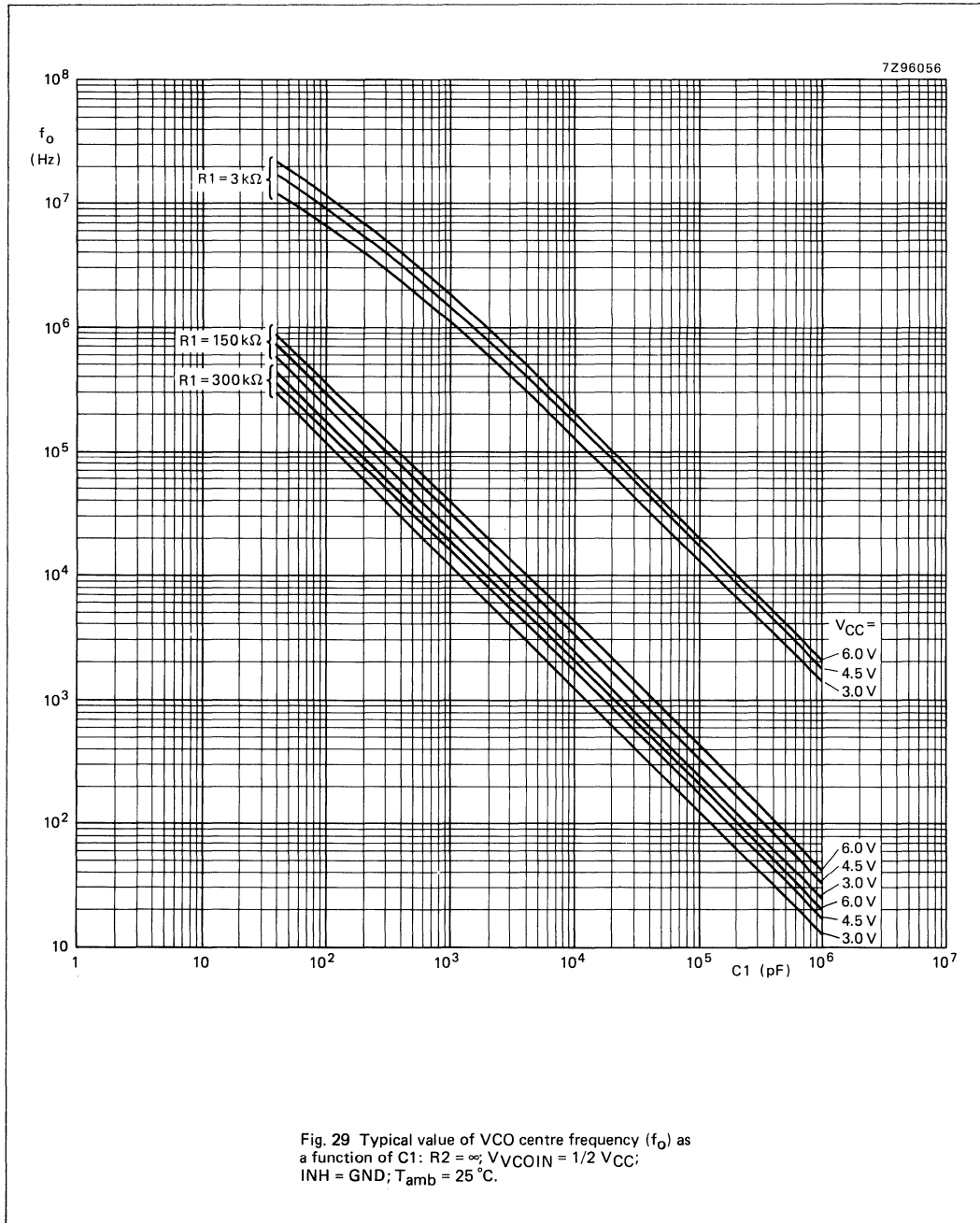
Values of the selected components should be within the following ranges:

- R1 between  $3\text{ k}\Omega$  and  $300\text{ k}\Omega$ ;
- R2 between  $3\text{ k}\Omega$  and  $300\text{ k}\Omega$ ;
- R1 + R2 parallel value  $> 2.7\text{ k}\Omega$ ;
- C1 greater than  $40\text{ pF}$ .

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency without extra offset	PC1, PC2 or PC3	<p><b>VCO frequency characteristic</b></p> <p>With <math>R2 = \infty</math> and <math>R1</math> within the range <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 25. (Due to <math>R1, C1</math> time constant a small offset remains when <math>R2 = \infty</math>.)</p>  <p style="text-align: center;">7296051</p> <p style="text-align: center;">Fig. 25 Frequency characteristic of VCO operating without offset: <math>f_o</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	PC1	<p><b>Selection of R1 and C1</b></p> <p>Given <math>f_o</math>, determine the values of <math>R1</math> and <math>C1</math> using Fig. 29.</p>
	PC2 or PC3	<p>Given <math>f_{max}</math> and <math>f_o</math>, determine the values of <math>R1</math> and <math>C1</math> using Fig. 29, use Fig. 31 to obtain <math>2f_L</math> and then use this to calculate <math>f_{min}</math>.</p>
VCO frequency with extra offset	PC1, PC2 or PC3	<p><b>VCO frequency characteristic</b></p> <p>With <math>R1</math> and <math>R2</math> within the ranges <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, <math>3\text{ k}\Omega &lt; R2 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 26.</p>  <p style="text-align: center;">7296052</p> <p style="text-align: center;">Fig. 26 Frequency characteristic of VCO operating with offset: <math>f_o</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	PC1, PC2 or PC3	<p><b>Selection of R1, R2 and C1</b></p> <p>Given <math>f_o</math> and <math>f_L</math>, determine the value of product <math>R1C1</math> by using Fig. 31. Calculate <math>f_{off}</math> from the equation <math>f_{off} = f_o - 4.3f_L</math>. Obtain the values of <math>C1</math> and <math>R2</math> by using Fig. 30. Calculate the value of <math>R1</math> from the value of <math>C1</math> and the product <math>R1C1</math>.</p>

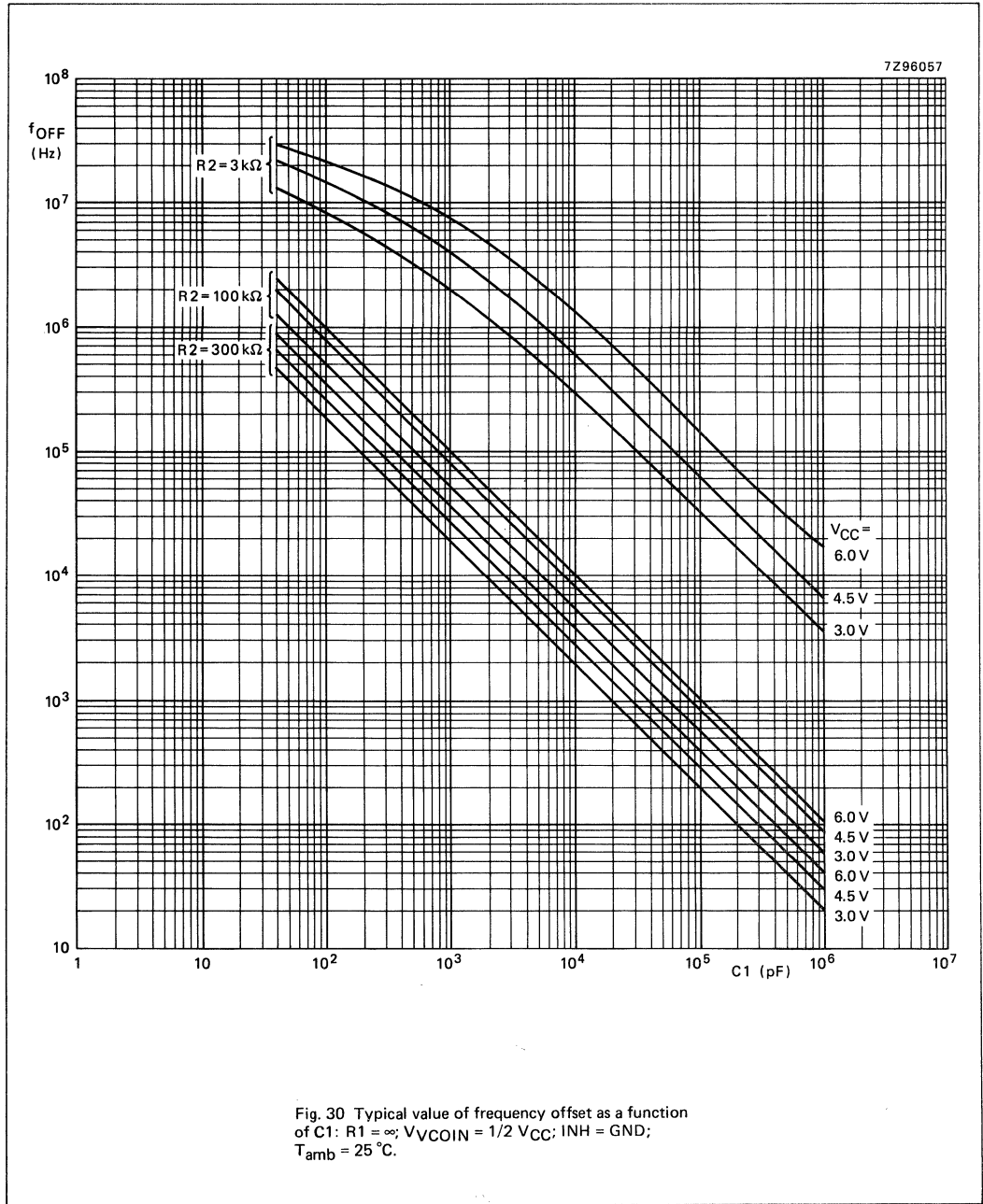
APPLICATION INFORMATION (Continued)

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG <sub>IN</sub> input	PC1	VCO adjusts to $f_0$ with $\phi_{\text{DEMOUT}} = 90^\circ$ and $V_{\text{VCOIN}} = 1/2 V_{\text{CC}}$ (see Fig. 6).
	PC2	VCO adjusts to $f_0$ with $\phi_{\text{DEMOUT}} = -360^\circ$ and $V_{\text{VCOIN}} = 0 \text{ V}$ (see Fig. 8).
	PC3	VCO adjusts to $f_0$ with $\phi_{\text{DEMOUT}} = +360^\circ$ and $V_{\text{VCOIN}} = V_{\text{CC}}$ (see Fig. 10).
PLL frequency capture range	PC1, PC2 or PC3	<p><b>Loop filter component selection</b></p>    <p>(a) <math>\tau = R3 \times C2</math>      (b) amplitude characteristic      (c) pole-zero diagram</p> <p>7296053</p> <p>A small capture range (<math>2f_c</math>) is obtained if <math>\tau &gt; 2f_c \approx 1/\pi\sqrt{2\pi f_L/\tau}</math>.</p> <p>Fig. 27 Simple loop filter for PLL without offset.</p>    <p>(a) <math>\tau_1 = R3 \times C2</math>;      (b) amplitude characteristic      (c) pole-zero diagram  <math>\tau_2 = R4 \times C2</math>;  <math>\tau_3 = (R3 + R4) \times C2</math></p> <p>7296054</p> <p>Fig. 28 Simple loop filter for PLL with offset.</p>
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$ , large ripple content at $\phi_{\text{DEMOUT}} = 90^\circ$
	PC2	$f_r = f_i$ , small ripple content at $\phi_{\text{DEMOUT}} = 0^\circ$
	PC3	$f_r = f_{\text{SIGIN}}$ , large ripple content at $\phi_{\text{DEMOUT}} = 180^\circ$





APPLICATION INFORMATION (Continued)



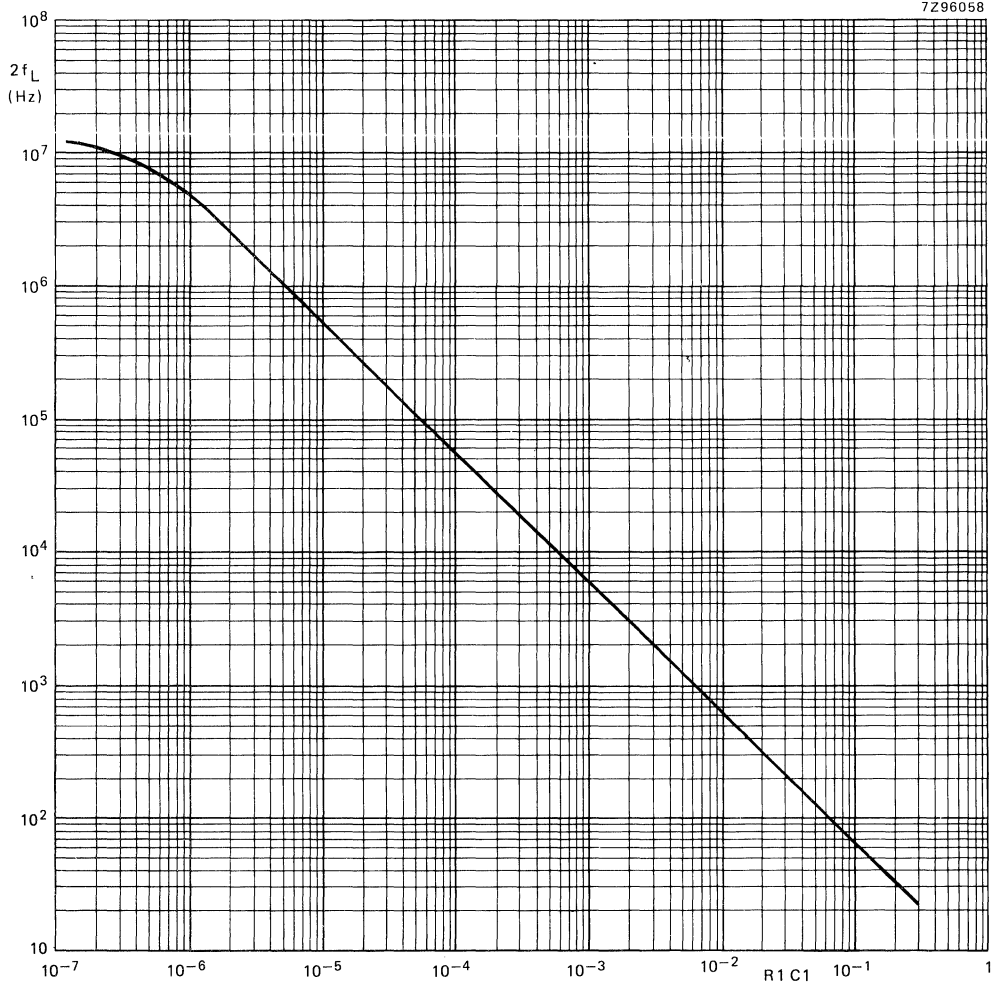


Fig. 31 Typical frequency lock range ( $2f_L$ ) versus the product  $R1C1$ :  $V_{VCOIN}$  range = 0.9 to  $(V_{CC} - 0.9)$  V;  $V_{CC} = 4.5$  V;  $R2 = \infty$ .



## HEX INVERTING HIGH-TO-LOW LEVEL SHIFTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC4049 is a high-speed Si-gate CMOS device and is pin compatible with the "4049" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7.

The 74HC4049 provides six inverting buffers with a modified input protection structure, which has no diode connected to V<sub>CC</sub>. Input voltages of up to 15 V may therefore be used.

This feature enables the inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V<sub>CC</sub> and is the same as mentioned in the family characteristics. At the same time each part can be used as a simple inverter without level translation.

### APPLICATIONS

- Converting 15 V logic ("4000B" series) down to 2 V logic.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to n $\bar{Y}$	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	ns
C <sub>I</sub>	input capacitance		3.5	pF
CPD	power dissipation capacitance per buffer	note 1	14	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6ns

### Note

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in V

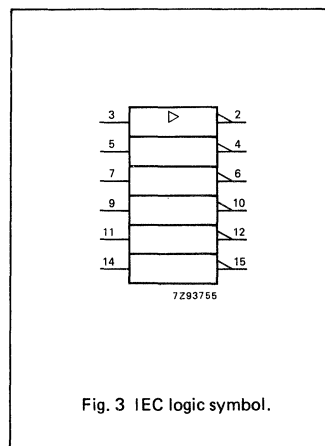
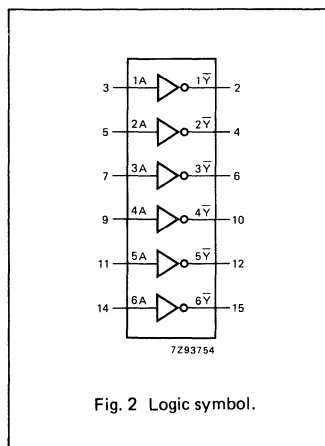
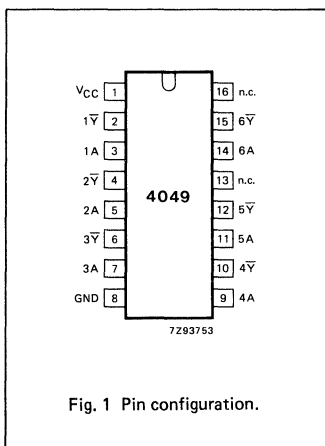
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC4049P: 16-lead DIL; plastic (SOT-38Z).

PC74HC4049T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V <sub>CC</sub>	positive supply voltage
2, 4, 6, 10, 12, 15	1 $\bar{Y}$ to 6 $\bar{Y}$	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected



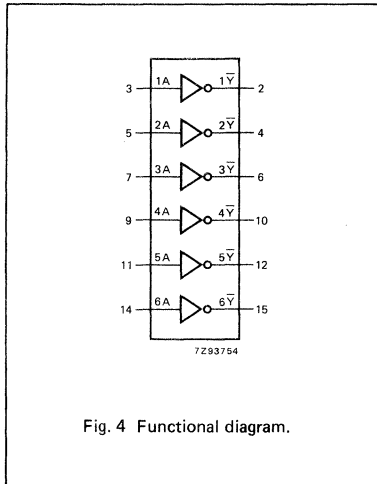


Fig. 4 Functional diagram.

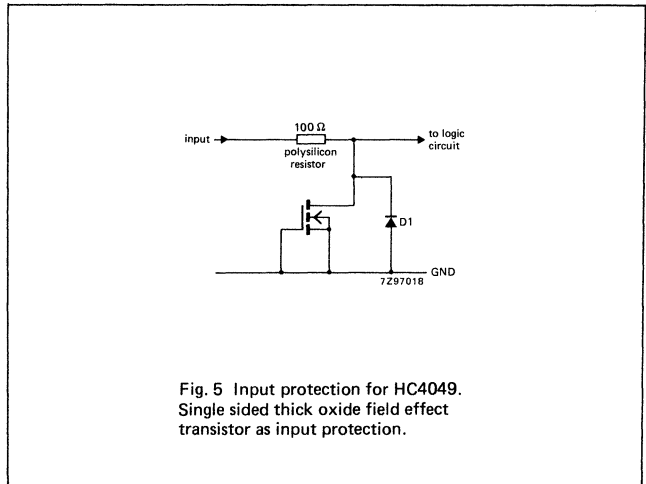


Fig. 5 Input protection for HC4049. Single sided thick oxide field effect transistor as input protection.

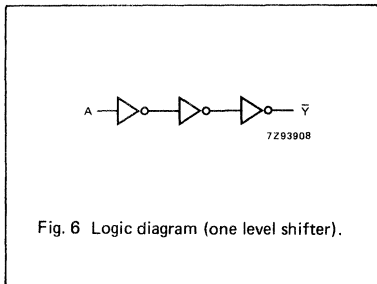


Fig. 6 Logic diagram (one level shifter).

FUNCTION TABLE

INPUT	OUTPUT
nA	n $\bar{Y}$
L	H
H	L

H = HIGH voltage level  
L = LOW voltage level

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$V_{IK}$	DC input voltage range	-0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for $-0.5$ V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: - standard outputs		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

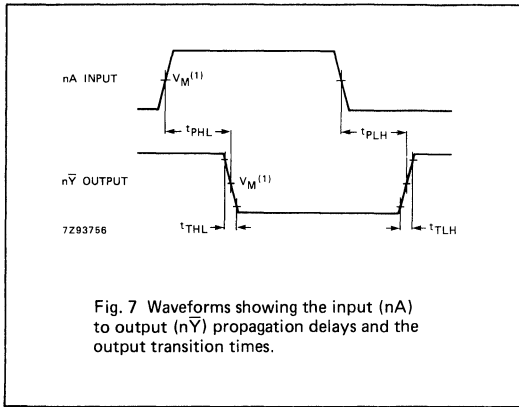
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V <sub>IL</sub>	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
± I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V	
I <sub>CC</sub>	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND	

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		28 10 8	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

## AC WAVEFORMS



## Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .

HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .





## HEX HIGH-TO-LOW LEVEL SHIFTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC4050 is a high-speed Si-gate CMOS device and is pin compatible with the "4050" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7.

The 74HC4050 provides six non-inverting buffers with a modified input protection structure, which has no diode connected to V<sub>CC</sub>. Input voltages of up to 15 V may therefore be used. This feature enables the non-inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V<sub>CC</sub> and is the same as mentioned in the family characteristics.

### APPLICATIONS

- Converting 15 V logic ("4000B" series) down to 2 V logic.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	7	ns
C <sub>I</sub>	input capacitance		3.5	pF
CPD	power dissipation capacitance per buffer	* note 1	14	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Note

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

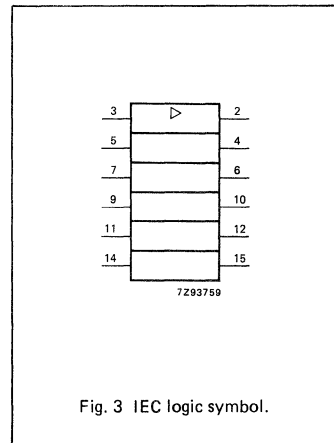
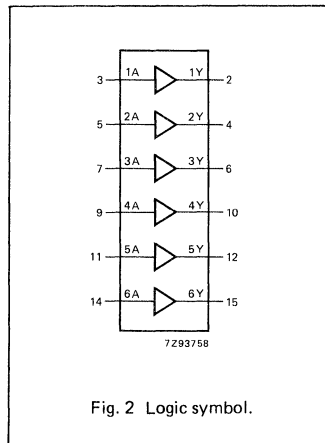
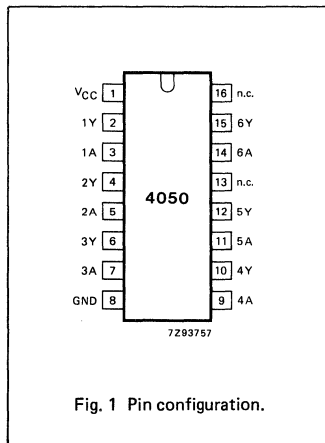
### ORDERING INFORMATION/PACKAGE OUTLINES

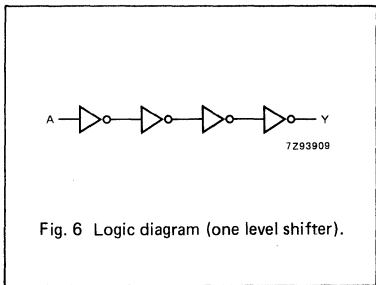
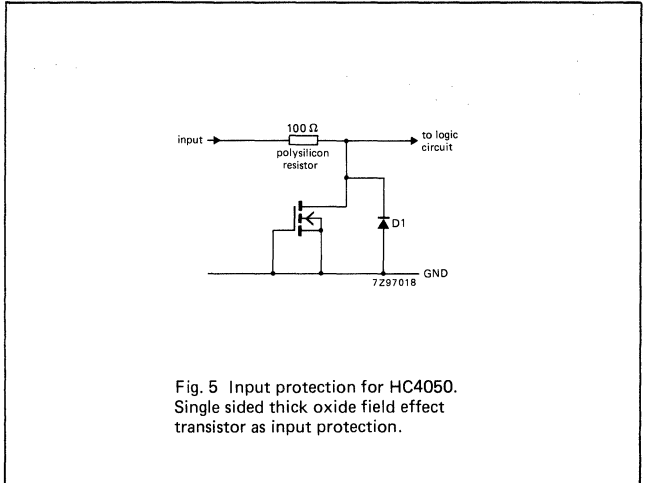
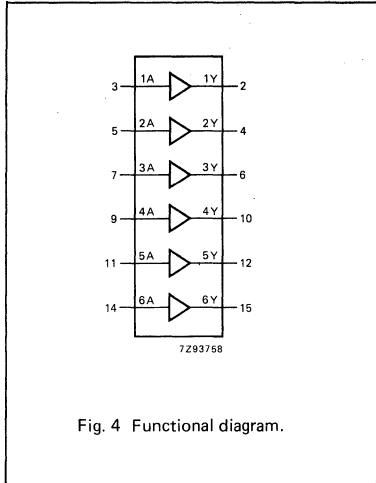
PC74HC4050P: 16-lead DIL; plastic (SOT-38Z).

PC74HC4050T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V <sub>CC</sub>	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected





**FUNCTION TABLE**

INPUT	OUTPUT
nA	nY
L	L
H	H

H = HIGH voltage level  
L = LOW voltage level

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$V_{IK}$	DC input voltage range	-0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for $-0.5$ V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: - standard outputs		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

**DC CHARACTERISTICS FOR 74HC**

Voltages are referenced to GND (ground = 0 V)

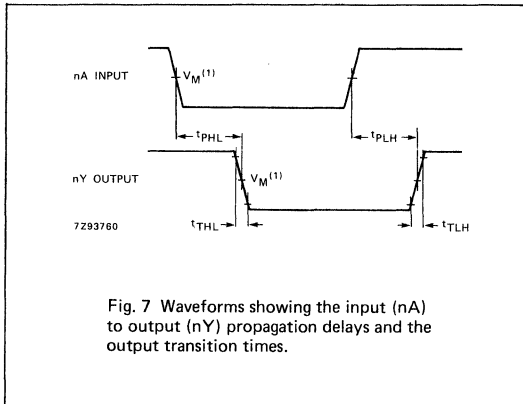
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS		
		74HC									V <sub>CC</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage all outputs			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage standard outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
± I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND		
				0.5		5.0		5.0	μA	2.0 to 6.0	15 V		
I <sub>CC</sub>	quiescent supply current			2.0		20.0		40.0	μA	6.0	15 V or GND		

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	

## AC WAVEFORMS



## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



## 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

### FEATURES

- Wide analog input voltage range:  $\pm 5$  V.
- Low "ON" resistance:  
80  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5$  V  
70  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0$  V  
60  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0$  V
- Logic level translation:  
to enable 5 V logic to communicate  
with  $\pm 5$  V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4051 are high-speed Si-gate CMOS devices and are pin compatible with the "4051" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4051 are 8-channel analog multiplexers/demultiplexers with three digital select inputs ( $S_0$  to  $S_2$ ), an active LOW enable input ( $\bar{E}$ ), eight independent inputs/outputs ( $Y_0$  to  $Y_7$ ) and a common input/output ( $Z$ ).

With  $\bar{E}$  LOW, one of the eight switches is selected (low impedance ON-state) by  $S_0$  to  $S_2$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $S_0$  to  $S_2$ .

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs ( $S_0$  to  $S_2$ , and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs ( $Y_0$  to  $Y_7$ , and  $Z$ ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{OS}$ $S_n$ to $V_{OS}$	$C_L = 15$ pF $R_L = 1$ k $\Omega$ $V_{CC} = 5$ V	22 20	22 24	ns ns
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{OS}$ $S_n$ to $V_{OS}$		18 19	16 20	ns ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	22	24	pF
$C_S$	max. switch capacitance independent common		5 25	5 25	pF pF

$V_{EE} = GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L + C_S) \times V_{CC}^2 \times f_o$$

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $C_S$  = max. switch capacitance in pF  
 $\sum (C_L + C_S) \times V_{CC}^2 \times f_o$  = sum of outputs  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5$  V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4051P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4051T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\bar{E}$	enable input (active LOW)
7	$V_{EE}$	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	$S_0$ to $S_2$	select inputs
13, 14, 15, 12, 1, 5, 2, 4	$Y_0$ to $Y_7$	independent inputs/outputs
16	$V_{CC}$	positive supply voltage

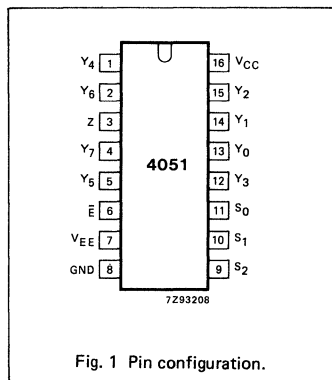


Fig. 1 Pin configuration.

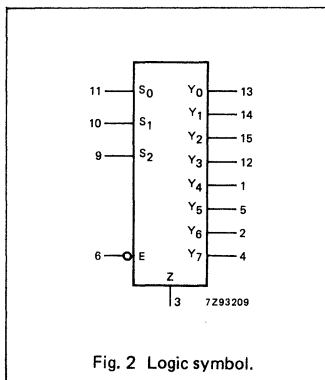


Fig. 2 Logic symbol.

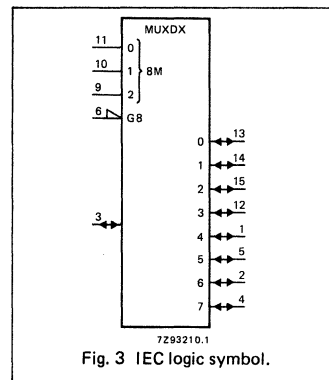
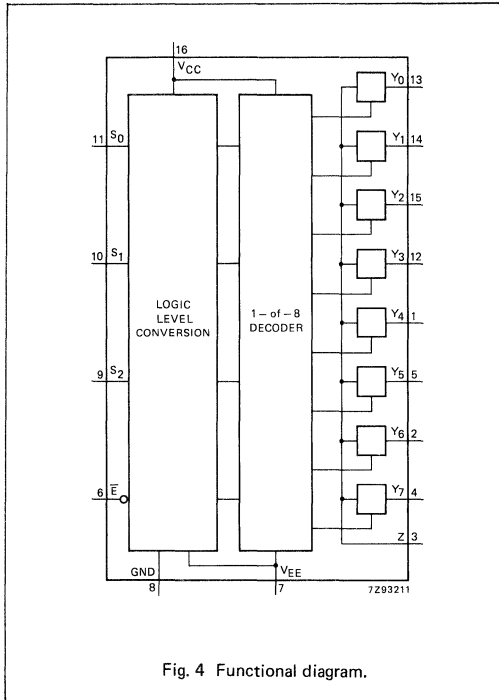


Fig. 3 IEC logic symbol.





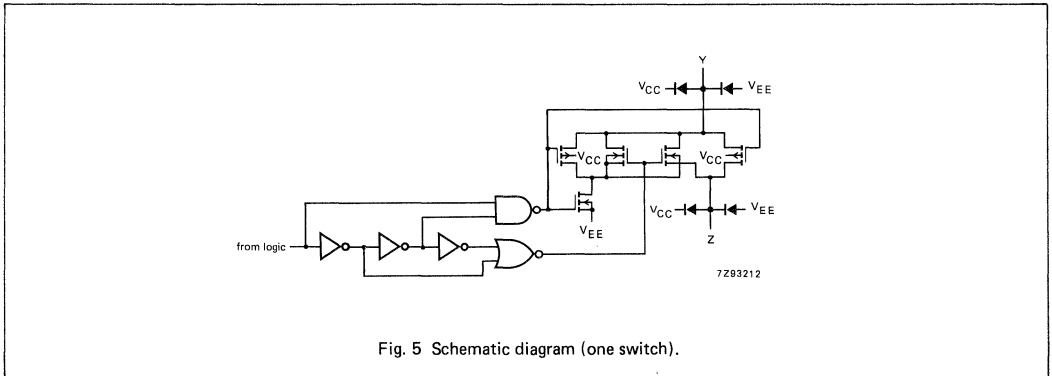
**APPLICATIONS**

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

**FUNCTION TABLE**

INPUTS				channel ON
$\bar{E}$	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	
L	L	L	L	Y <sub>0</sub> - Z
L	L	L	H	Y <sub>1</sub> - Z
L	L	H	L	Y <sub>2</sub> - Z
L	L	H	H	Y <sub>3</sub> - Z
L	H	L	L	Y <sub>4</sub> - Z
L	H	L	H	Y <sub>5</sub> - Z
L	H	H	L	Y <sub>6</sub> - Z
L	H	H	H	Y <sub>7</sub> - Z
H	X	X	X	none

H = HIGH voltage level  
L = LOW voltage level  
X = don't care



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

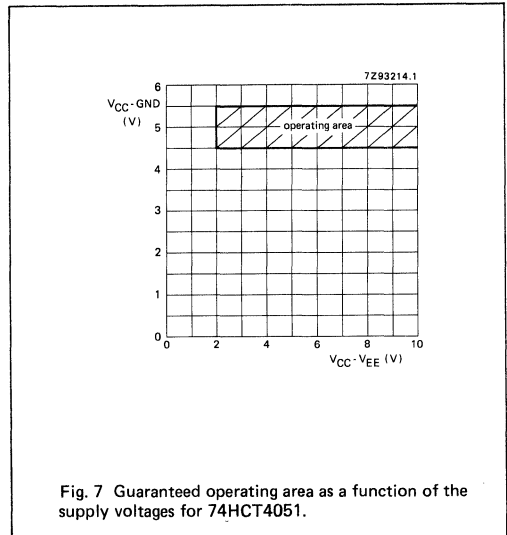
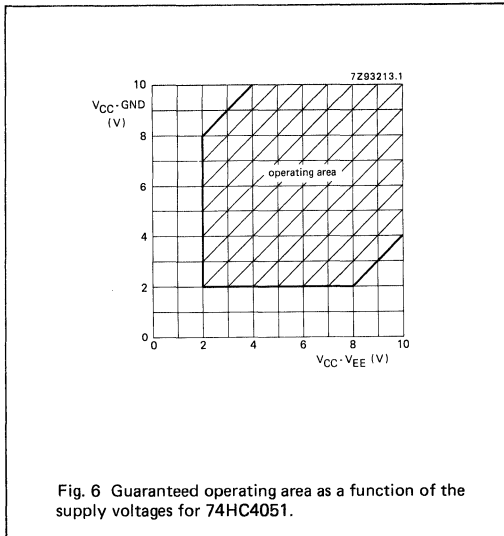
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

**Note to ratings**

To avoid drawing  $V_{CC}$  current out of terminal Z, when switch current flows in terminals  $Y_n$ , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{CC}$  current will flow out of terminals  $Y_n$ . In this case there is no limit for the voltage drop across the switch, but the voltages at  $Y_n$  and Z may not exceed  $V_{CC}$  or  $V_{EE}$ .

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$



**DC CHARACTERISTICS FOR 74HC/HCT**

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V  
 For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_S$ $\mu A$	$V_{is}$	$V_I$
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
RON	ON resistance (peak)	-	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IN}$ or $V_{IL}$
		100	180	225	270	240	270	$\Omega$	4.5	0	1000		
		90	160	200	240	200	240	$\Omega$	6.0	0	1000		
		70	130	165	195	195	195	$\Omega$	4.5	-4.5	1000		
RON	ON resistance	150	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{EE}$	$V_{IH}$ or $V_{IL}$
		80	140	175	210	180	210	$\Omega$	4.5	0	1000		
		70	120	150	180	150	180	$\Omega$	6.0	0	1000		
		60	105	130	160	160	160	$\Omega$	4.5	-4.5	1000		
RON	ON resistance	150	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		90	160	200	240	210	240	$\Omega$	4.5	0	1000		
		80	140	175	210	180	210	$\Omega$	6.0	0	1000		
		65	120	150	180	180	180	$\Omega$	4.5	-4.5	1000		
$\Delta R_{ON}$	maximum $\Delta R_{ON}$ resistance between any two channels	-	-	-	-	-	-	$\Omega$	2.0	0	-	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		9	-	-	-	-	-	$\Omega$	4.5	0	-		
		8	-	-	-	-	-	$\Omega$	6.0	0	-		
		6	-	-	-	-	-	$\Omega$	4.5	-4.5	-		

**Notes to DC characteristics**

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{Os}$		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 17)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{Os}$		72 26 21 16	225 45 38 32		280 56 48 40		340 68 58 48	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $S_n$ to $V_{Os}$		66 24 19 16	225 45 38 32		280 56 48 40		340 68 58 48	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{Os}$		58 21 17 16	225 45 38 32		280 56 48 40		340 68 58 48	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $S_n$ to $V_{Os}$		61 22 18 16	225 45 38 32		280 56 48 40		340 68 58 48	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)

## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1V	other inputs at V <sub>CC</sub> or GND

## Note to HCT types

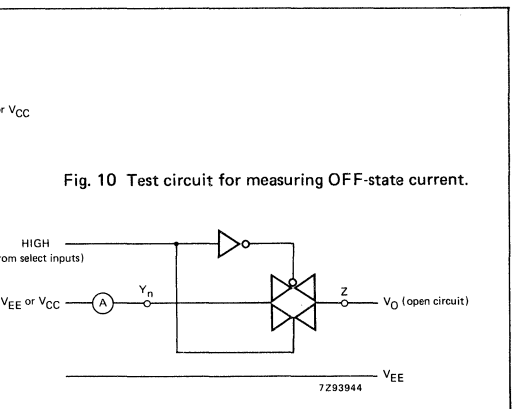
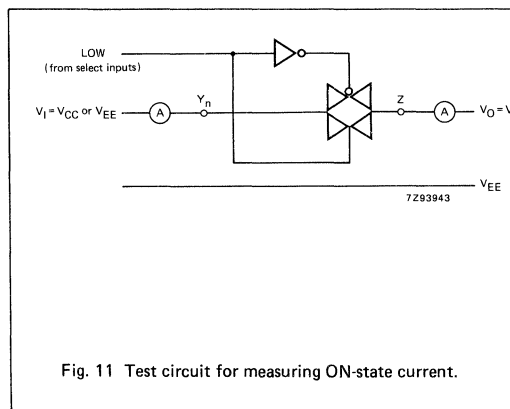
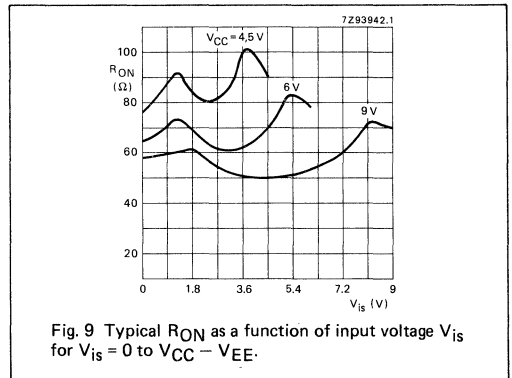
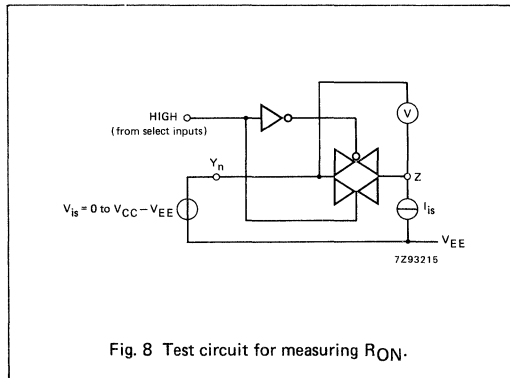
1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S <sub>n</sub>	0.50
E	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{Os}$		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 17)
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{Os}$		26 16	55 39		69 49		83 59	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PZH}/t_{PZL}$	turn "ON" time $S_n$ to $V_{Os}$		28 16	55 39		69 49		83 59	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{Os}$		19 16	45 32		56 40		68 48	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $S_n$ to $V_{Os}$		23 16	45 32		56 40		68 48	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 18, 19 and 20)



**ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT**

Recommended conditions and typical values

GND = 0 V; T<sub>amb</sub> = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>is(p-p)</sub>	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF (see Figs 12 and 15)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E or S <sub>n</sub> , square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig. 16)
f <sub>max</sub>	minimum frequency response (-3dB)	170 180	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance independent common	5 25	pF pF				

**Notes to AC characteristics**

**General note**

V<sub>is</sub> is the input voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an input.  
V<sub>Os</sub> is the output voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an output.

**Notes**

1. Adjust input voltage V<sub>is</sub> to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V<sub>is</sub> to 0 dBm level at V<sub>Os</sub> for 10 kHz (0 dBm = 1 mW into 50 Ω).

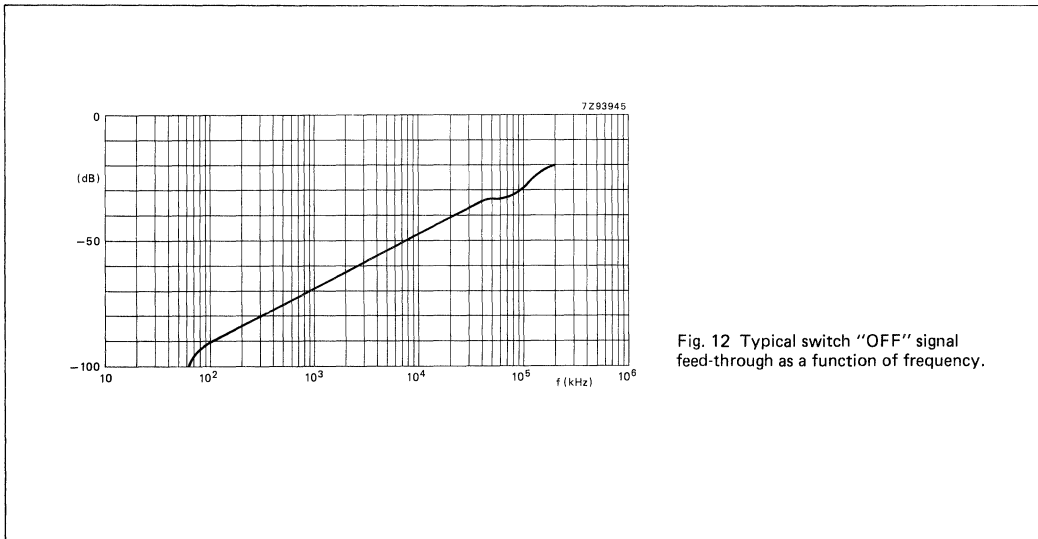
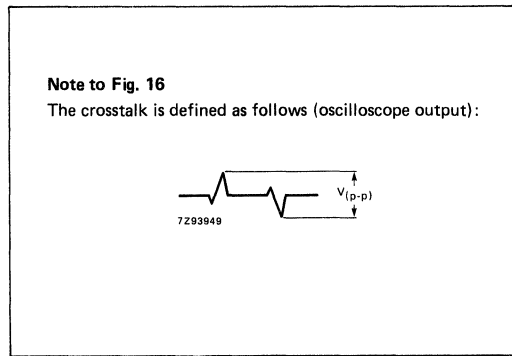
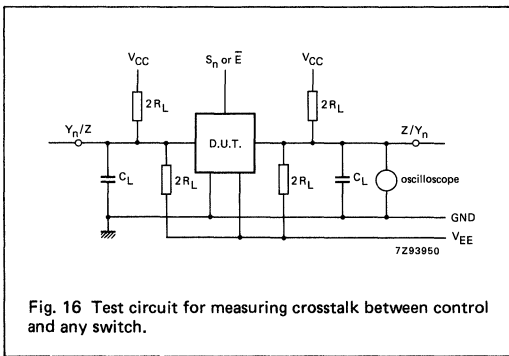
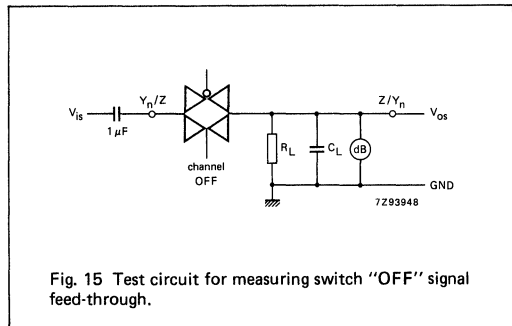
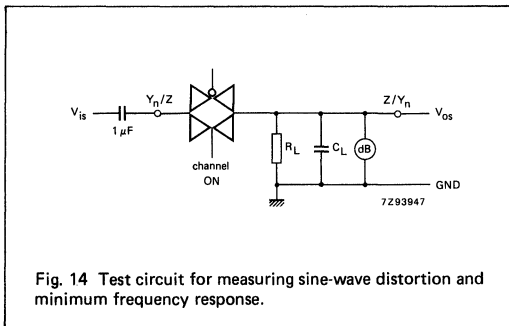
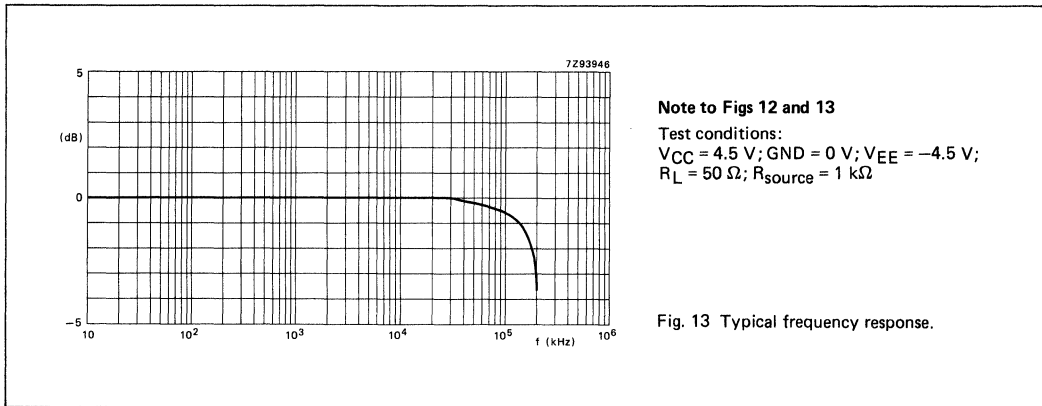


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.





AC WAVEFORMS

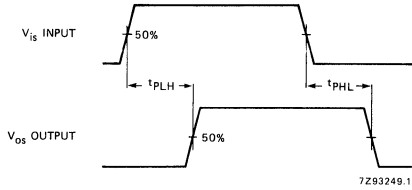


Fig. 17 Waveforms showing the input ( $V_{iS}$ ) to output ( $V_{oS}$ ) propagation delays.

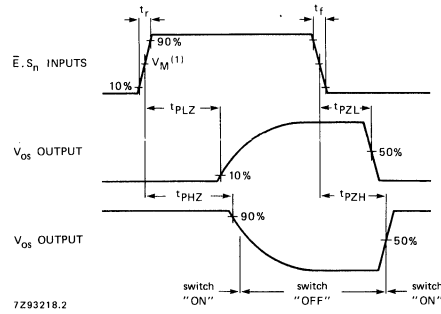
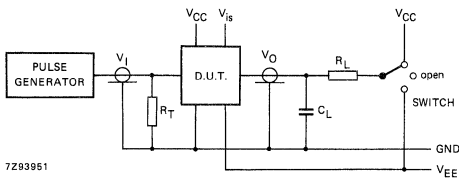


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

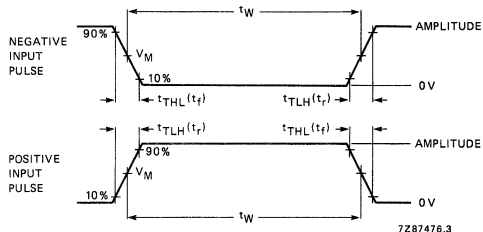
- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS



7Z69951

Fig. 19 Test circuit for measuring AC performance.



7Z87476.3

Fig. 20 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> , t <sub>f</sub>	
			f <sub>max</sub> : PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 19 and 20:

- C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.
- t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint to t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULPLEXER

FEATURES

- Wide analog input voltage range:  $\pm 5$  V.
- Low "ON" resistance:  
80  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5$  V  
70  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0$  V  
60  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0$  V
- Logic level translation:  
to enable 5 V logic to communicate  
with  $\pm 5$  V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the "4052" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY<sub>0</sub> to nY<sub>3</sub>) and a common input/output (nZ). The common channel select logics include two digital select inputs (S<sub>0</sub> and S<sub>1</sub>) and an active LOW enable input (E).

With E LOW, one of the four switches is selected (low impedance ON-state) by S<sub>0</sub> and S<sub>1</sub>. With E HIGH, all switches are in the high impedance OFF-state, independent of S<sub>0</sub> and S<sub>1</sub>.

V<sub>CC</sub> and GND are the supply voltage pins for the digital control inputs (S<sub>0</sub> and S<sub>1</sub>, and E). The V<sub>CC</sub> to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY<sub>0</sub> to nY<sub>3</sub>, and nZ) can swing between V<sub>CC</sub> as a positive limit and V<sub>EE</sub> as a negative limit. V<sub>CC</sub> - V<sub>EE</sub> may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V<sub>EE</sub> is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
tPZH/ tPZL	turn "ON" time E or S <sub>n</sub> to V <sub>OS</sub>	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 k $\Omega$ V <sub>CC</sub> = 5 V	28	18	ns
tPHZ/ tPLZ	turn "OFF" time E or S <sub>n</sub> to V <sub>OS</sub>		21	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
C <sub>S</sub>	max. switch capacitance independent common		5	5	pF
			12	12	pF

V<sub>EE</sub> = GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

where:

f<sub>i</sub> = input frequency in MHz  
f<sub>o</sub> = output frequency in MHz  
 $\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF  
C<sub>S</sub> = max. switch capacitance in pF  
V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4052P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4052T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	2Y <sub>0</sub> to 2Y <sub>3</sub>	independent inputs/outputs
6	E	enable input (active LOW)
7	V <sub>EE</sub>	negative supply voltage
8	GND	ground (0 V)
10, 9	S <sub>0</sub> , S <sub>1</sub>	select inputs
12, 14, 15, 11	1Y <sub>0</sub> to 1Y <sub>3</sub>	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	V <sub>CC</sub>	positive supply voltage

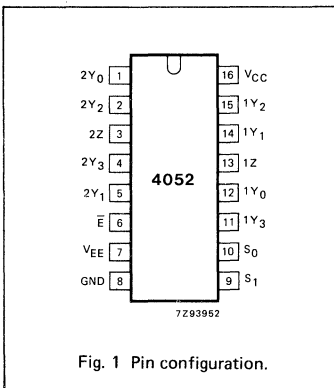


Fig. 1 Pin configuration.

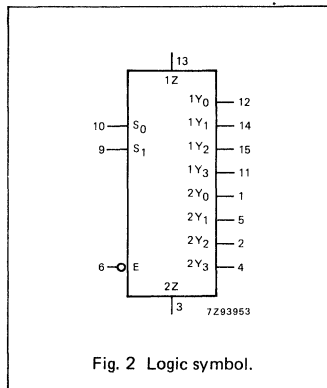


Fig. 2 Logic symbol.

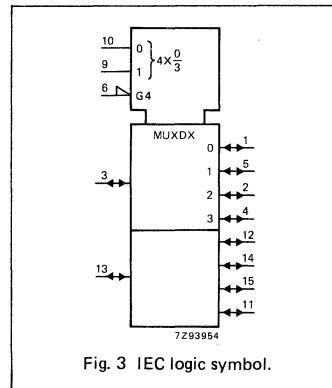


Fig. 3 IEC logic symbol.

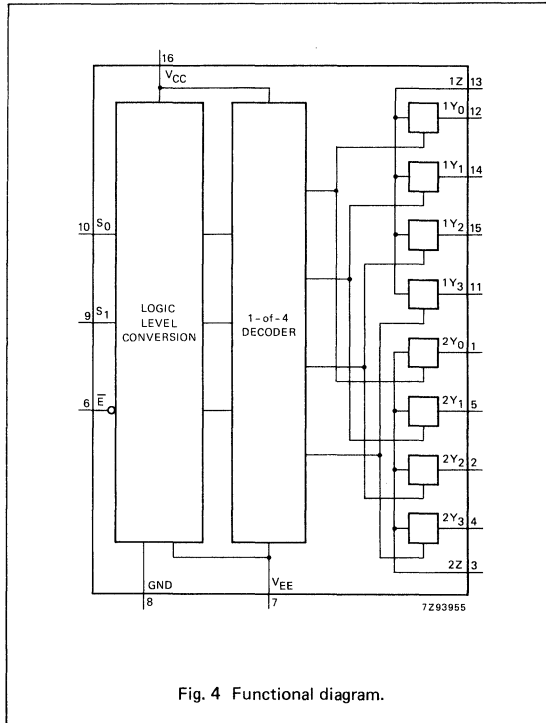


Fig. 4 Functional diagram.

**APPLICATIONS**

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

**FUNCTION TABLE**

$\bar{E}$	INPUTS		CHANNEL ON
	$S_1$	$S_0$	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	none

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

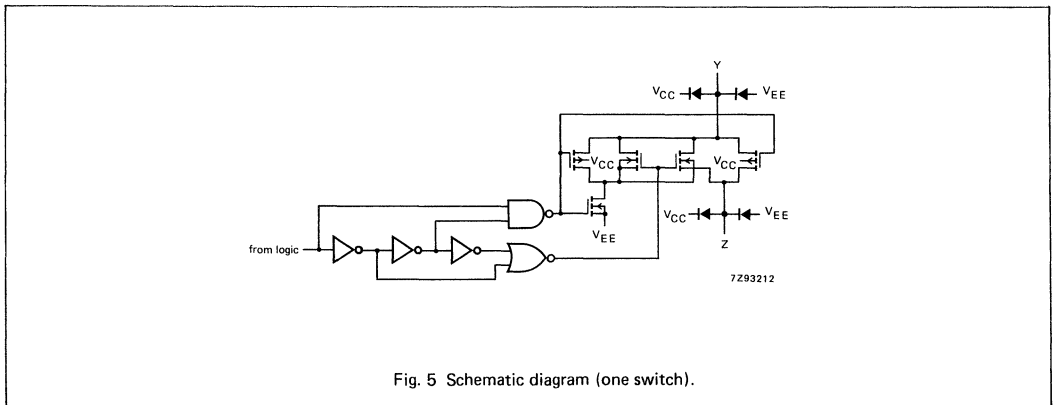


Fig. 5 Schematic diagram (one switch).

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	$^{\circ}\text{C}$	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 $^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		500	mW	above +70 $^{\circ}\text{C}$ : derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 $^{\circ}\text{C}$ : derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

**Note to ratings**

To avoid drawing  $V_{CC}$  current out of terminals nZ, when switch current flows in terminals nY<sub>n</sub>, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no  $V_{CC}$  current will flow out of terminals nY<sub>n</sub>. In this case there is no limit for the voltage drop across the switch, but the voltages at nY<sub>n</sub> and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}$ -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}$ - $V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

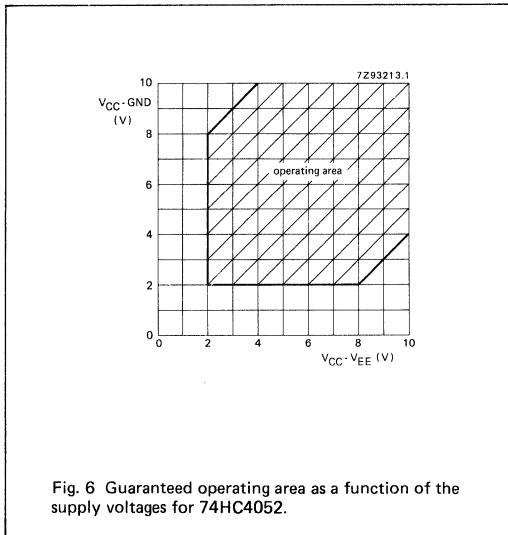


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4052.

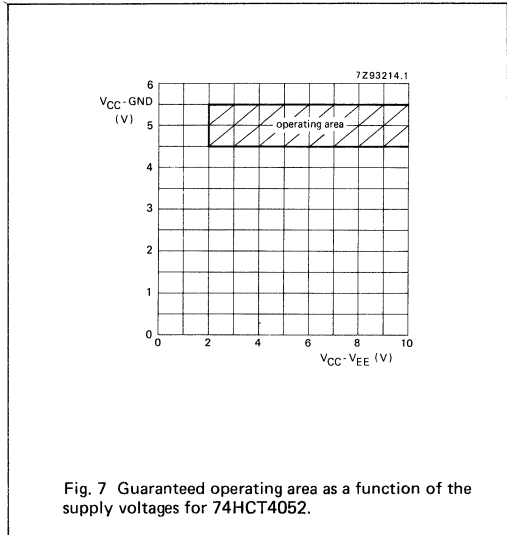


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

**DC CHARACTERISTICS FOR 74HC/HCT**

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS					
		74HC/HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	I <sub>S</sub> μA	V <sub>is</sub>	V <sub>I</sub>	
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.		max.					
R <sub>ON</sub>	ON resistance (peak)	—	100	180	—	225	—	270	Ω	2.0	0	100	V <sub>CC</sub> to V <sub>EE</sub>	V <sub>IH</sub> or V <sub>IL</sub>
		90	160	200	240	Ω	4.5	0	1000					
		70	130	165	195	Ω	6.0	0	1000					
R <sub>ON</sub>	ON resistance	150	—	—	—	—	—	—	Ω	2.0	0	100	V <sub>EE</sub>	V <sub>IH</sub> or V <sub>IL</sub>
		80	140	175	210	Ω	4.5	0	1000					
		70	120	150	180	Ω	6.0	0	1000					
R <sub>ON</sub>	ON resistance	150	—	—	—	—	—	—	Ω	2.0	0	100	V <sub>CC</sub>	V <sub>IH</sub> or V <sub>IL</sub>
		90	160	200	240	Ω	4.5	0	1000					
		80	140	175	210	Ω	6.0	0	1000					
ΔR <sub>ON</sub>	maximum ΔON resistance between any two channels	—	—	—	—	—	—	—	Ω	2.0	0	—	V <sub>CC</sub> to V <sub>EE</sub>	V <sub>IH</sub> or V <sub>IL</sub>
		9	—	—	—	—	—	—	—	Ω	4.5	0		
		8	—	—	—	—	—	—	—	Ω	6.0	0		
		6	—	—	—	—	—	—	Ω	4.5	-4.5	1000		

**Notes to DC characteristics**

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R<sub>ON</sub> see Fig. 8.

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
t <sub>pHL</sub> / t <sub>pLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>		14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Fig. 18)
t <sub>pZH</sub> / t <sub>pZL</sub>	turn "ON" time E to V <sub>os</sub> S <sub>n</sub> to V <sub>os</sub>		105 38 30 26	325 65 55 46		405 81 69 58		490 98 83 69	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>pHZ</sub> / t <sub>pLZ</sub>	turn "OFF" time E to V <sub>os</sub> S <sub>n</sub> to V <sub>os</sub>		74 27 22 22	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)



DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
I <sub>S</sub>	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> - 2.1V	other inputs at V <sub>CC</sub> or GND

Note to HCT types

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S <sub>n</sub>	0.45
E	0.45

AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{os}$ $S_n$ to $V_{os}$		41 28	70 48		88 60		105 72	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{os}$ $S_n$ to $V_{os}$		26 21	50 38		63 48		75 57	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)

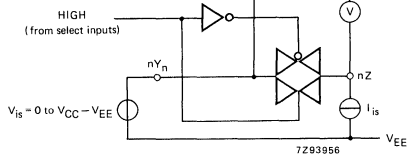


Fig. 8 Test circuit for measuring  $R_{ON}$ .

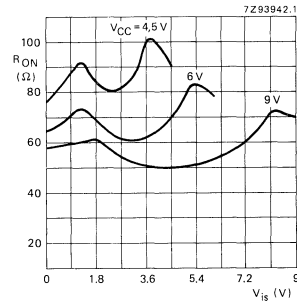


Fig. 9 Typical  $R_{ON}$  as a function of input voltage  $V_{is}$  for  $V_{is} = 0$  to  $V_{CC} - V_{EE}$ .

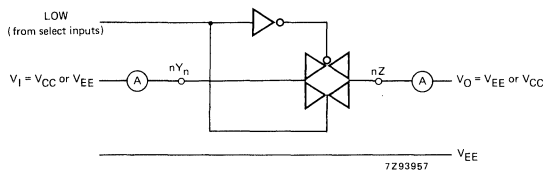
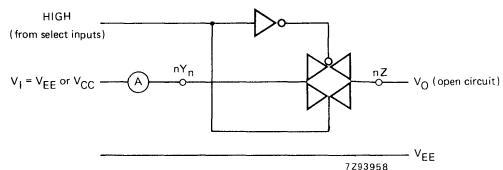


Fig. 10 Test circuit for measuring OFF-state current.

Fig. 11 Test circuit for measuring ON-state current.



## ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

SYMBOL	PARAMETER	typ.	UNIT	$V_{CC}$ V	$V_{EE}$ V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion $f = 1\text{ kHz}$	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$ ; $C_L = 50\text{ pF}$ (see Fig. 14)
	sine-wave distortion $f = 10\text{ kHz}$	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$ ; $C_L = 50\text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ( $\bar{E}$ or $S_n$ , square-wave between $V_{CC}$ and GND, $t_r = t_f = 6\text{ ns}$ ) (see Fig. 17)
$f_{max}$	minimum frequency response (-3dB)	170 180	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50\text{ }\Omega$ ; $C_L = 50\text{ pF}$ (see Figs 13 and 14)
$C_S$	maximum switch capacitance independent common	5 12	pF pF				

## Notes to AC characteristics

## General note

 $V_{is}$  is the input voltage at an  $nY_n$  or  $nZ$  terminal, whichever is assigned as an input. $V_{os}$  is the output voltage at an  $nY_n$  or  $nZ$  terminal, whichever is assigned as an output.

## Notes

1. Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).
2. Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for 10 kHz (0 dBm = 1 mW into 50  $\Omega$ ).

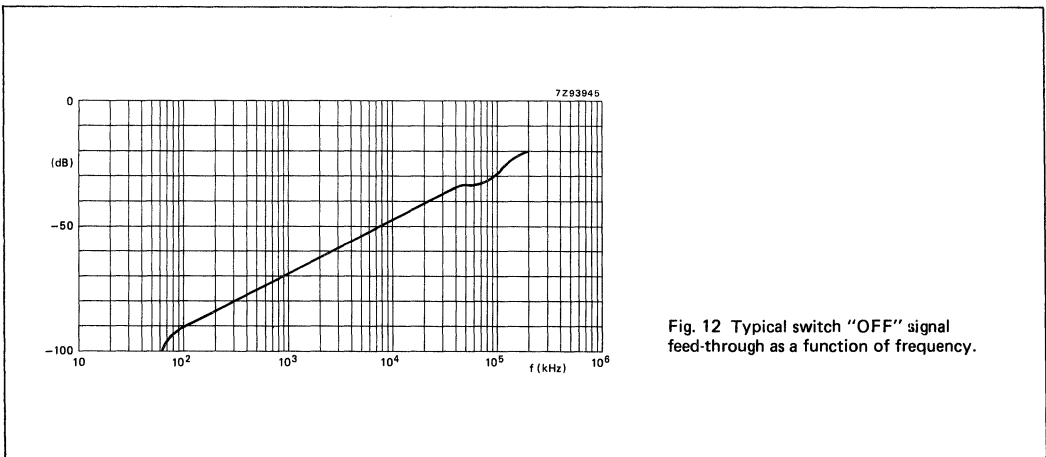
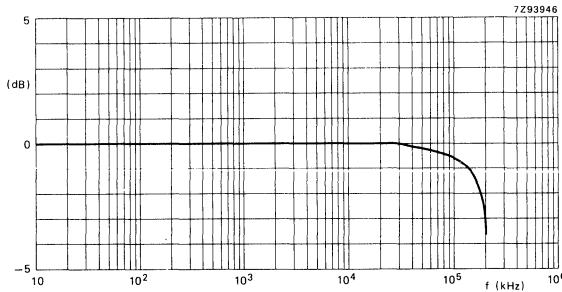


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:  
 $V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -4.5\text{ V}$ ;  
 $R_L = 50\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

Fig. 13 Typical frequency response.

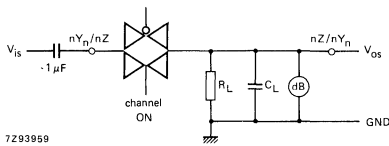


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

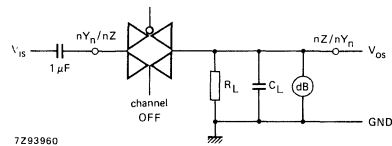


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

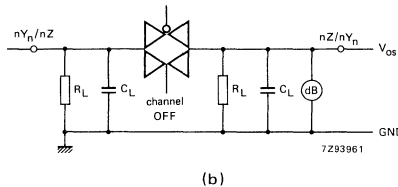
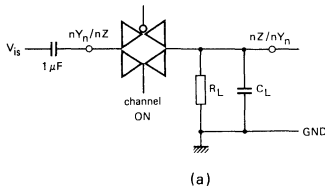


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.  
 (a) channel ON condition; (b) channel OFF condition.

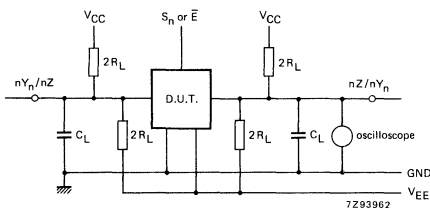
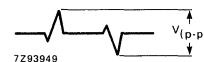


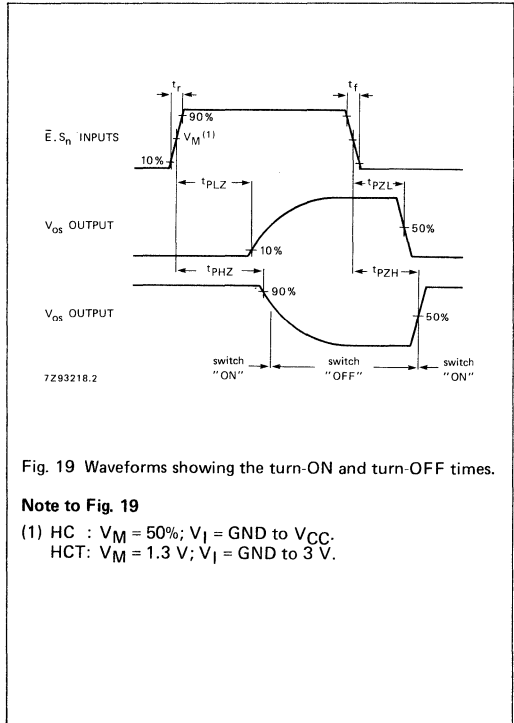
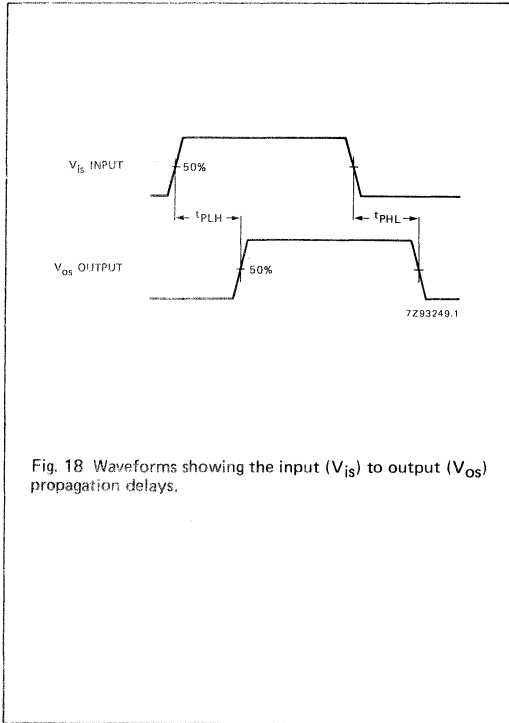
Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



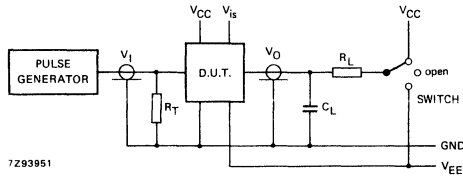
AC WAVEFORMS



**Note to Fig. 19**

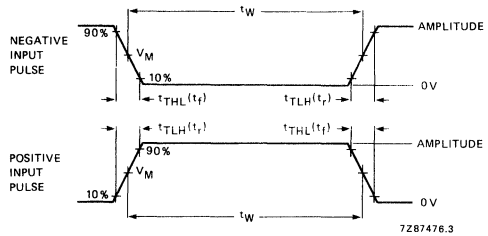
- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS



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Fig. 20 Test circuit for measuring AC performance.



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Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	V <sub>EE</sub> pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.

t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint to t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.



TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

FEATURES

- Low "ON" resistance:  
80 Ω (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$   
70 Ω (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$   
60 Ω (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation:  
to enable 5 V logic to communicate  
with ±5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I<sup>CC</sup> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input ( $\bar{E}$ ). Each multiplexer/demultiplexer has two independent inputs/outputs ( $nY_0$  and  $nY_1$ ), a common input/output ( $nZ$ ) and three digital select inputs ( $S_0$  to  $S_2$ ).

With  $\bar{E}$  LOW, one of the two switches is selected (low impedance ON-state) by  $S_0$  to  $S_2$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $S_0$  to  $S_2$ .

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs ( $S_0$  to  $S_2$ , and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs ( $nY_0$  and  $nY_1$ , and  $nZ$ ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{OS}$ $S_n$ to $V_{OS}$	$C_L = 15\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	17	23	ns
			21	21	ns
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{OS}$ $S_n$ to $V_{OS}$		18	20	ns
			17	19	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	36	36	pF
$C_S$	max. switch capacitance independent common		5	5	pF
			8	8	pF

$V_{EE} = \text{GND} = 0\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

$f_i$  = input frequency in MHz

$C_L$  = output load capacitance in pF

$f_o$  = output frequency in MHz

$C_S$  = max. switch capacitance in pF

$\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND}$  to  $V_{CC}$   
For HCT the condition is  $V_I = \text{GND}$  to  $V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4053P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4053T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

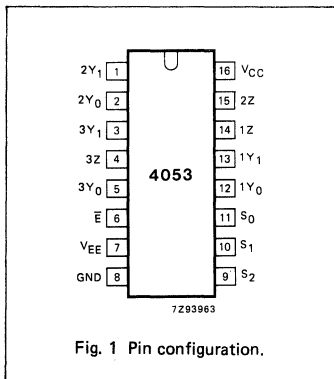


Fig. 1 Pin configuration.

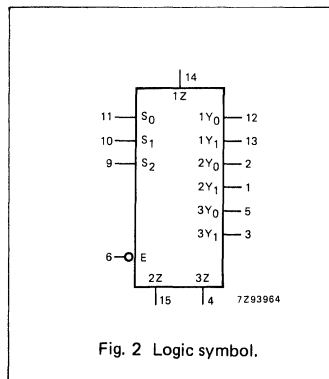


Fig. 2 Logic symbol.

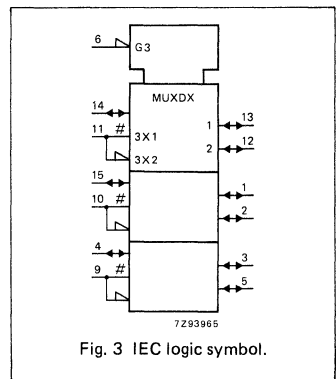


Fig. 3 IEC logic symbol.



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	2Y <sub>0</sub> , 2Y <sub>1</sub>	independent inputs/outputs
5, 3	3Y <sub>0</sub> , 3Y <sub>1</sub>	independent inputs/outputs
6	$\bar{E}$	enable input (active LOW)
7	V <sub>EE</sub>	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S <sub>0</sub> to S <sub>2</sub>	select inputs
12, 13	1Y <sub>0</sub> , 1Y <sub>1</sub>	independent inputs/outputs
14, 15, 4	1Z to 3Z	common inputs/outputs
16	V <sub>CC</sub>	positive supply voltage

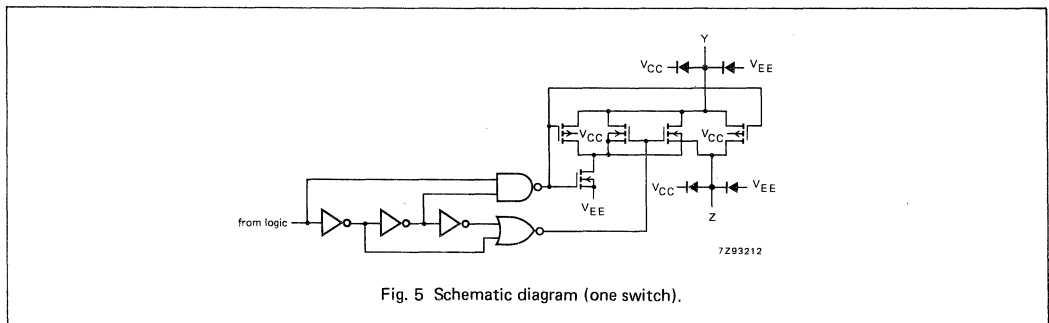
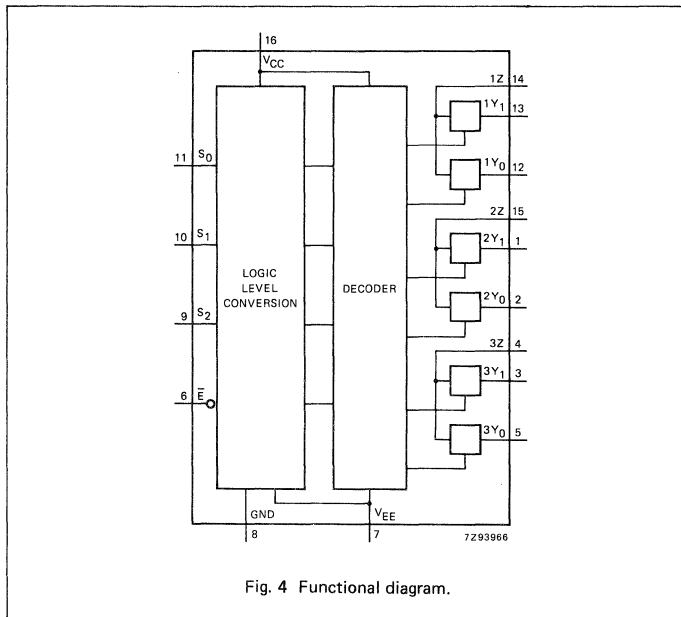
APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS		CHANNEL ON
$\bar{E}$	S <sub>n</sub>	
L	L	nY <sub>0</sub> – nZ
L	H	nY <sub>1</sub> – nZ
H	X	none

H = HIGH voltage level  
L = LOW voltage level  
X = don't care



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	$^{\circ}\text{C}$	
$P_{tot}$	power dissipation per package				for temperature range: $-40$ to $+125^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		500	mW	above $+70^{\circ}\text{C}$ : derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above $+70^{\circ}\text{C}$ : derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

**Note to ratings**

To avoid drawing  $V_{CC}$  current out of terminals nZ, when switch current flows in terminals  $nY_n$ , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no  $V_{CC}$  current will flow out of terminals  $nY_n$ . In this case there is no limit for the voltage drop across the switch, but the voltages at  $nY_n$  and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

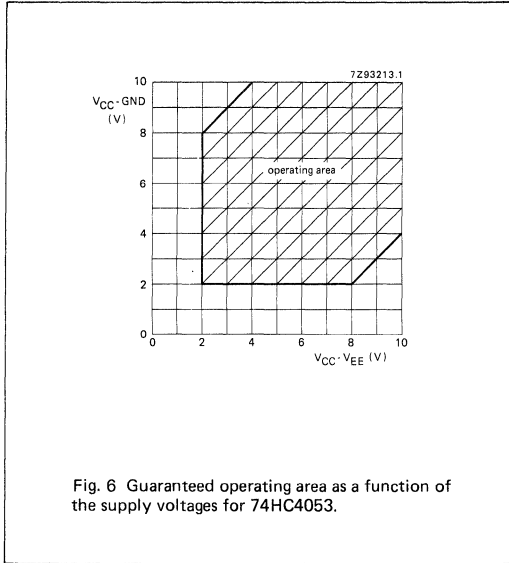


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4053.

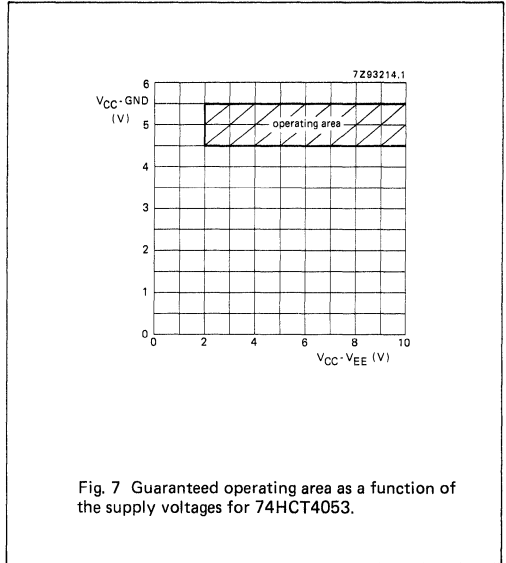


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4053.

**DC CHARACTERISTICS FOR 74HC/HCT**

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V  
 For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_S$ $\mu A$	$V_{is}$	$V_I$
		+25		-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.		max.				
$R_{ON}$	ON resistance (peak)	—	—	—	—	—	—	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IN}$ or $V_{IL}$
		100	180	225	270	—	—	$\Omega$	4.5	0	1000		
		90	160	200	240	—	—	$\Omega$	6.0	0	1000		
		70	130	165	195	—	—	$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance	150	—	—	—	—	—	$\Omega$	2.0	0	100	$V_{EE}$	$V_{IH}$ or $V_{IL}$
		80	140	175	210	—	—	$\Omega$	4.5	0	1000		
		70	120	150	180	—	—	$\Omega$	6.0	0	1000		
		60	105	130	160	—	—	$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance	150	—	—	—	—	—	$\Omega$	2.0	0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		90	160	200	240	—	—	$\Omega$	4.5	0	1000		
		80	140	175	210	—	—	$\Omega$	6.0	0	1000		
		65	120	150	180	—	—	$\Omega$	4.5	-4.5	1000		
$\Delta R_{ON}$	maximum $\Delta R_{ON}$ resistance between any two channels	—	—	—	—	—	—	$\Omega$	2.0	0	—	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		9	—	—	—	—	—	$\Omega$	4.5	0	—		
		8	—	—	—	—	—	$\Omega$	6.0	0	—		
		6	—	—	—	—	—	$\Omega$	4.5	-4.5	—		

**Notes to DC characteristics**

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	OTHER	
		+25		-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>Os</sub>		15 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Fig. 18)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time E̅ to V <sub>Os</sub>		60 20 16 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time S <sub>n</sub> to V <sub>Os</sub>		75 25 20 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time E̅ to V <sub>Os</sub>		63 21 17 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time S <sub>n</sub> to V <sub>Os</sub>		60 20 16 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)

## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND

## Note to HCT types

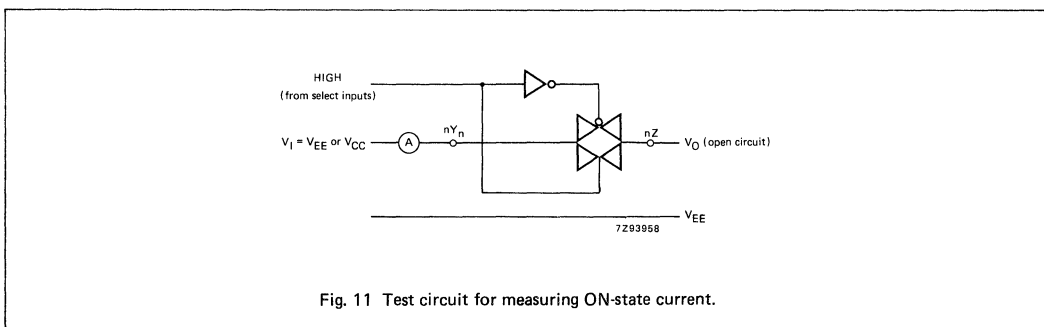
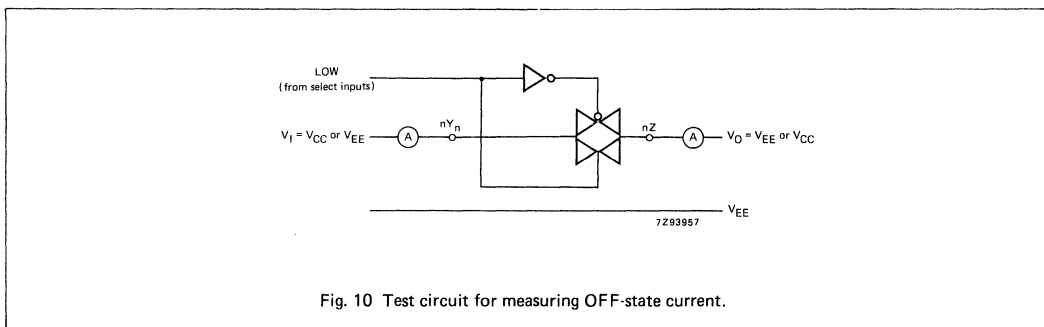
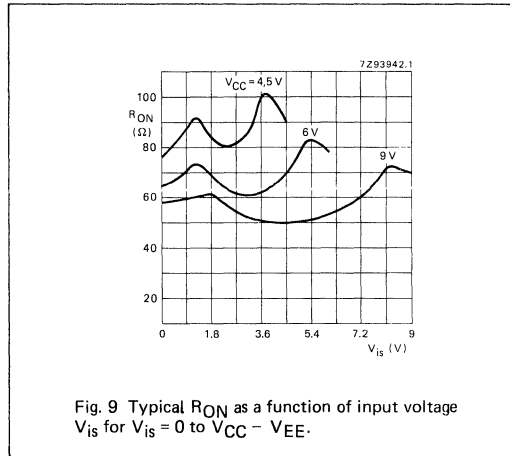
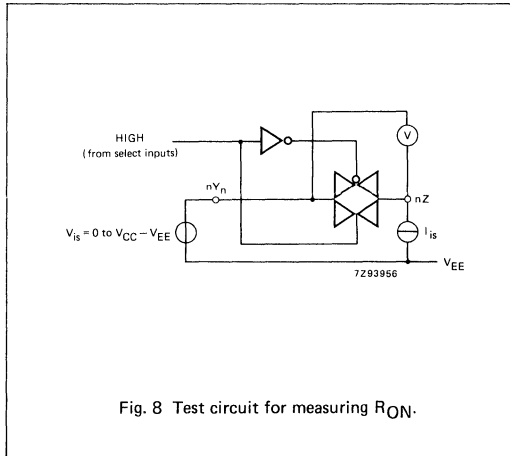
1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.  
To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S <sub>n</sub>	0.50
E	0.50

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Fig. 18)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time Ē to V <sub>os</sub>		27 16	48 34		60 43		72 51	ns	4.5 4.5	0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time S <sub>n</sub> to V <sub>os</sub>		25 16	48 34		60 43		72 51	ns	4.5 4.5	0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time Ē to V <sub>os</sub>		24 15	44 31		55 39		66 47	ns	4.5 4.5	0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time S <sub>n</sub> to V <sub>os</sub>		22 15	44 31		55 39		66 47	ns	4.5 4.5	0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Figs 19, 20 and 21)





**ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT**

Recommended conditions and typical values

GND = 0 V; T<sub>amb</sub> = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	VCC V	VEE V	V <sub>is(p-p)</sub> V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (see Fig. 16)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E or S <sub>n</sub> , square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig. 17)
f <sub>max</sub>	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance independent common	5 8	pF pF				

**Notes to AC characteristics**

**General note**

V<sub>is</sub> is the input voltage at an nY<sub>n</sub> or nZ terminal, whichever is assigned as an input.  
V<sub>os</sub> is the output voltage at an nY<sub>n</sub> or nZ terminal, whichever is assigned as an output.

**Notes**

1. Adjust input voltage V<sub>is</sub> to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V<sub>is</sub> to 0 dBm level at V<sub>os</sub> for 10 kHz (0 dBm = 1 mW into 50 Ω).

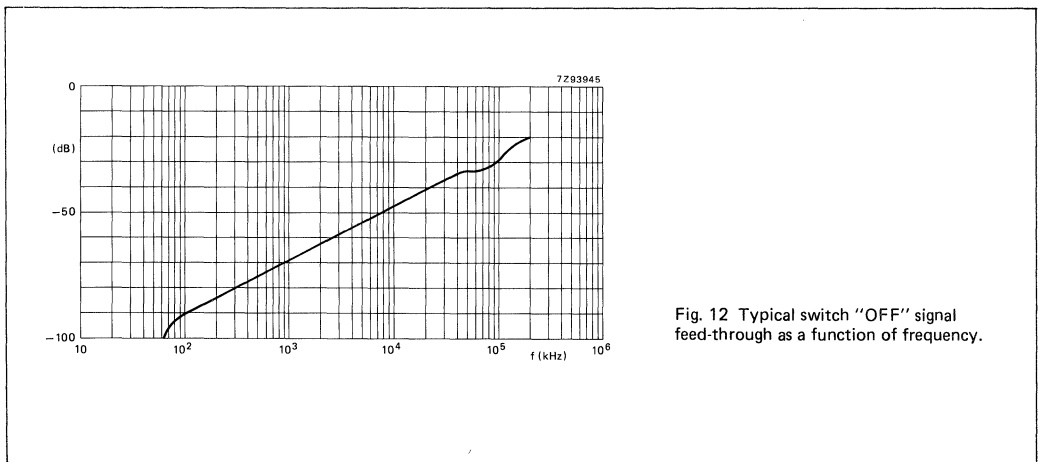
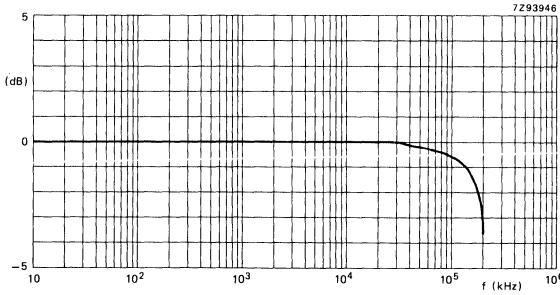


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



Note to Figs 12 and 13

Test conditions:  
 $V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -4.5\text{ V}$ ;  
 $R_L = 50\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

Fig. 13 Typical frequency response.

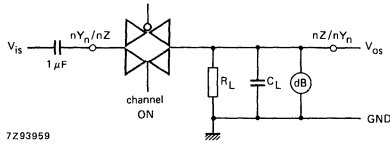


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

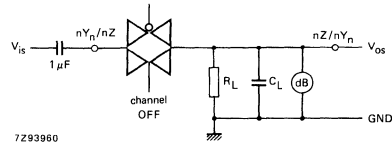


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

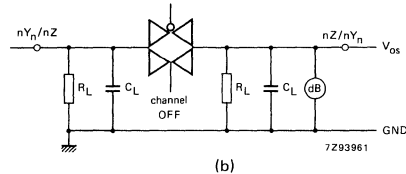
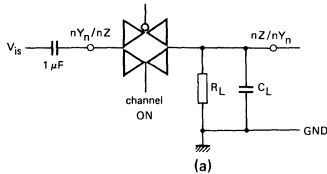


Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers. (a) channel ON condition; (b) channel OFF condition.

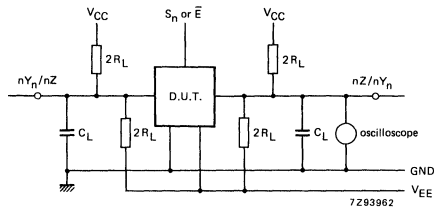
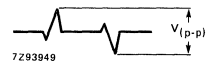


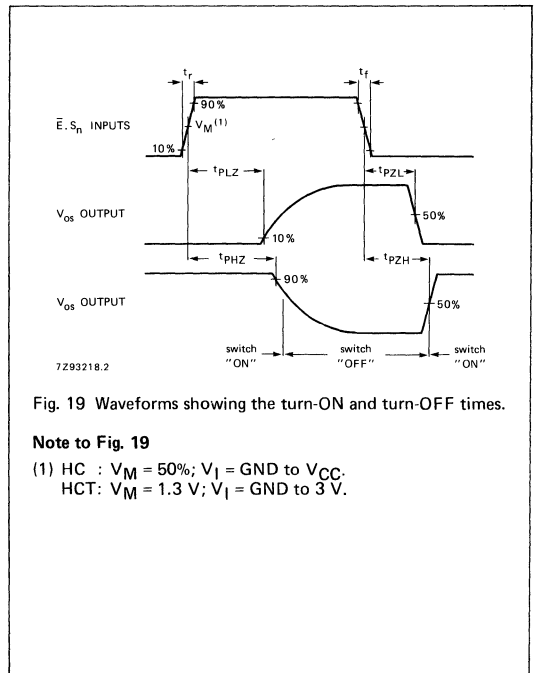
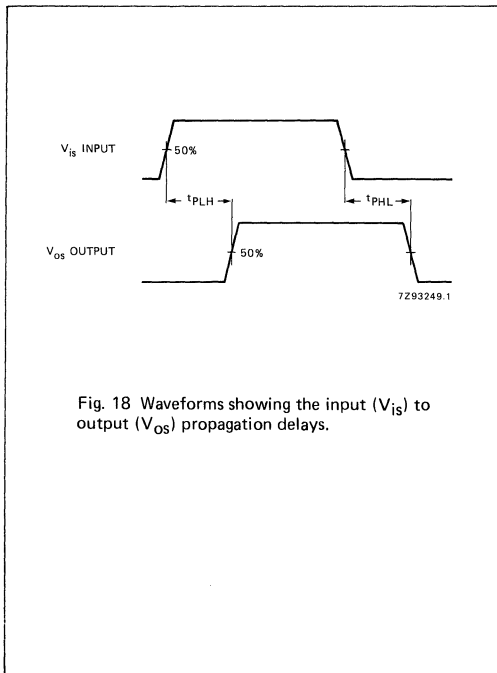
Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows (oscilloscope output):



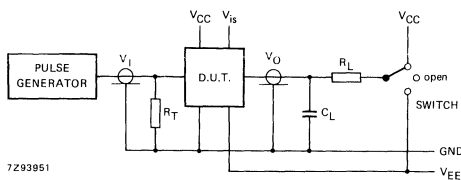
AC WAVEFORMS



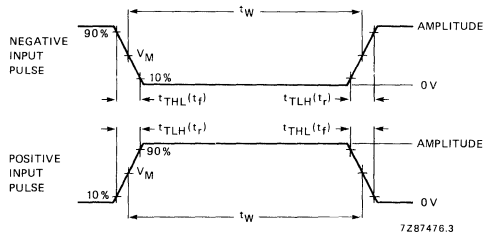
**Note to Fig. 19**

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS



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Fig. 20 Test circuit for measuring AC performance.

Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>pZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>pZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

- C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.
- t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4059

MSI

## PROGRAMMABLE DIVIDE-BY-N COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4059 are high-speed Si-gate CMOS devices and are pin compatible with the "4059" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4059 are divide-by-n counters which can be programmed to divide an input frequency by any number (n) from 3 to 15 999. The output signal is a one clock-cycle wide pulse and occurs at a rate equal to the input frequency divided by n. The down counter is preset by means of 16 jam inputs (J<sub>1</sub> to J<sub>16</sub>).

The three mode selection inputs (S<sub>1</sub> to S<sub>3</sub>) determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the function table. Every time the first (fastest) counting section goes through one cycle, it reduces by 1, the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section (which consists of flip-flops that are not needed for operating the first counting section).

For example, in divide-by-2 mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands.

This counting mode is selected when S<sub>1</sub>, S<sub>2</sub> and S<sub>3</sub> are set HIGH. In this case input J<sub>1</sub> is used to preset the first counting section and J<sub>2</sub> to J<sub>4</sub> are used to preset the last (5th) counting section.

(continued on next page)

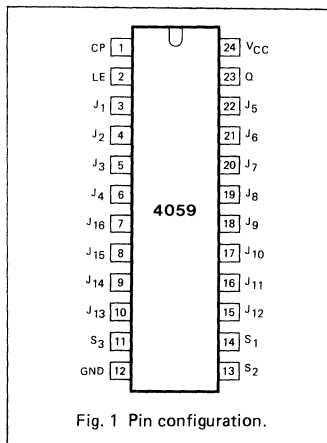


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
f <sub>max</sub>	maximum clock frequency		40	40	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4059P: 24-lead DIL; plastic (SOT-101A).

PC74HC/HCT4059T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	LE	latch enable (active HIGH)
3, 4, 5, 6, 22, 21, 20, 19, 18, 17, 16, 15, 10, 9, 8, 7	J <sub>1</sub> to J <sub>16</sub>	programmable jam inputs (BCD)
12	GND	ground (0 V)
14, 13, 11	S <sub>1</sub> to S <sub>3</sub>	mode select inputs
23	Q	divide-by-n output
24	V <sub>CC</sub>	positive supply voltage

**GENERAL DESCRIPTION (Cont'd)**

If divide-by 10 mode is desired for the first section, S<sub>1</sub> is set HIGH, S<sub>2</sub> HIGH and S<sub>3</sub> LOW. The jam inputs J<sub>1</sub> to J<sub>4</sub> are used to preset the first counting section and there is no last counting section.

The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters, presettable by means of the jam inputs J<sub>5</sub> to J<sub>16</sub>.

When clock pulses are applied to the clock input (CP) after a number "n" has been preset into the counter, the counter counts down until the DETECTION circuit detects the zero state. At this time the PRESET ENABLE circuit is enabled to preset again the number "n" into the counter and to produce an output pulse.

The preset of the counter to a desired divide-by-n is achieved as follows:

$$n = (\text{MODE}^*) (1000 \times \text{decade 5 preset} + 100 \times \text{decade 4 preset} + 10 \times \text{decade 3 preset} + 1 \times \text{decade 2 preset} + \text{decade 1 preset})$$

\* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any "n" count, divide the "n" count by the selected mode. The resultant is the corresponding preset value of the 5th to the 2nd decade with the remainder being equal to the 1st decade value; preset value = n/mode.

If n = 8479, and the selected mode = 5, the preset value = 8479/5 = 1695 with a remainder of 4, thus the jam inputs must be set as shown in Table 1.

The mode select inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25 and 50 parts. These inputs set the maximum value of "n" at 9999 (when the first counting section divides by 5 or 10) or at 15 999 (when the first counting section divides by 8, 4 or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 counting pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the divide-by-8 mode, the number from which the

intermediate counting section begins to count-down can be preset to:

- 3rd decade: 1500
  - 2nd decade: 150
  - 1st decade: 15
- 1665

The last counting section can be preset to a maximum of 1, with a place value of 1000. The total of these numbers (2665) times 8 equals 21 320. The first counting section can be preset to a maximum of 7. Therefore, 21 327 is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the function table, in the column entitled "extended counter range". Control inputs S<sub>2</sub> and S<sub>3</sub> can be used to initiate and lock the counter in the "master preset" mode. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that mode as long as S<sub>2</sub> and S<sub>3</sub> both remain LOW. The counter begins to run down from the preset state when a counting mode other than the "master preset" mode is selected. Whenever the "master preset" mode is used, control signals S<sub>2</sub> = S<sub>3</sub> = LOW must be applied for at least 3 full clock pulses. After the master preset mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down can begin at the second positive-going clock transition. Thus, after a "master preset" mode, there is always one extra count before the output goes HIGH. Figure 2 illustrates the operation of the counter in the divide-by-8 mode starting from the preset state 3.

If the "master preset" mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the "master preset" mode is not used the counter is preset in accordance with the jam inputs when the output pulse appears. A HIGH level at the latch enable input (LE) will cause the counter output to remain in the HIGH state until the LE input returns to LOW. If the LE input is LOW, the output pulse will remain HIGH for only one cycle of the clock input signal.

When S<sub>1</sub> = LOW, S<sub>2</sub> = HIGH, S<sub>3</sub> = LOW and LE = LOW, the counter operates in the "preset inhibit" mode, with which the dividend of the counter is fixed to 10 000, independent of the state of the jam inputs.

When in the same state of mode select inputs LE = HIGH, the counter operates in the normal divide-by-10 mode, however, without the latch operation at the output.

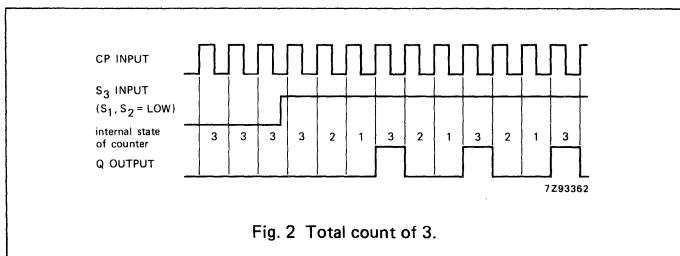


Fig. 2 Total count of 3.

Table 1

4				1	5				9				6			
J <sub>1</sub>	J <sub>2</sub>	J <sub>3</sub>	J <sub>4</sub>	J <sub>5</sub>	J <sub>6</sub>	J <sub>7</sub>	J <sub>8</sub>	J <sub>9</sub>	J <sub>10</sub>	J <sub>11</sub>	J <sub>12</sub>	J <sub>13</sub>	J <sub>14</sub>	J <sub>15</sub>	J <sub>16</sub>	
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L	

FUNCTION TABLE

LATCH ENABLE INPUT	MODE SELECT INPUTS			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	MODE DIVIDES BY	MAX. PRESET STATE	JAM INPUTS USED	MODE DIVIDES BY	MAX. PRESET STATE	JAM INPUTS USED	DESIGN MAX.	EXTENDED MAX.
X	H	H	H	2	1	J <sub>1</sub>	8	7	J <sub>2</sub> J <sub>3</sub> J <sub>4</sub>	15 999	17 331
X	L	H	H	4	3	J <sub>1</sub> J <sub>2</sub>	4	3	J <sub>3</sub> J <sub>4</sub>	15 999	18 663
X	H	L	H	5	4	J <sub>1</sub> J <sub>2</sub> J <sub>3</sub>	2	1	J <sub>4</sub>	9 999	13 329
X	L	L	H	8	7	J <sub>1</sub> J <sub>2</sub> J <sub>3</sub>	2	1	J <sub>4</sub>	15 999	21 327
X	H	H	L	10	9	J <sub>1</sub> J <sub>2</sub> J <sub>3</sub> J <sub>4</sub>	1	0	—	9 999	16 659
H	L	H	L	10	9	J <sub>1</sub> J <sub>2</sub> J <sub>3</sub> J <sub>4</sub>	1	0	—	9 999	16 659
L	L	H	L	preset inhibited			preset inhibited			fixed 10 000	—
X	X	L	L	master preset			master preset			—	—

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care



14-STAGE BINARY RIPPLE COUNTER WITH OSCILLATOR

FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for  $R_{TC}$  and  $C_{TC}$ )
- $I_{CC}$  category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS,  $R_{TC}$  and  $C_{TC}$ ), ten buffered outputs ( $Q_3$  to  $Q_9$  and  $Q_{11}$  to  $Q_{13}$ ) and an overriding asynchronous master reset (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins ( $R_{TC}$  and  $C_{TC}$ ) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter ( $Q_3$  to  $Q_9$  and  $Q_{11}$  to  $Q_{13}$  = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to  $V_{CC}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay RS to $Q_3$ $Q_n$ to $Q_{n+1}$	$C_L = 15$ pF $V_{CC} = 5$ V	31	31	ns
$t_{PHL}$	MR to $Q_n$		6	6	ns
$t_{PHL}$			17	18	ns
$f_{max}$	maximum clock frequency		87	87	MHz
$C_i$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6$  ns

Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz                       $C_L$  = output load capacitance in pF  
 $f_o$  = output frequency in MHz                     $V_{CC}$  = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_1 = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_1 = \text{GND to } V_{CC} - 1.5$  V
3. For formula on dynamic power dissipation see next page.

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4060P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT4060T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	$Q_{11}$ to $Q_{13}$	counter outputs
7, 5, 4, 6, 14, 13, 15	$Q_3$ to $Q_9$	counter outputs
8	GND	ground (0 V)
9	$C_{TC}$	external capacitor connection
10	$R_{TC}$	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	$V_{CC}$	positive supply voltage

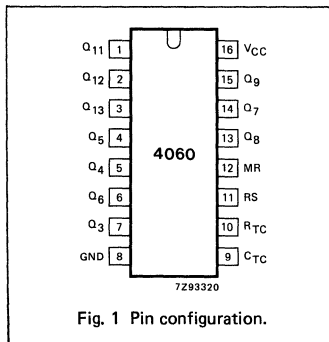


Fig. 1 Pin configuration.

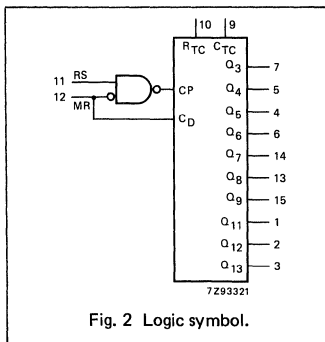


Fig. 2 Logic symbol.

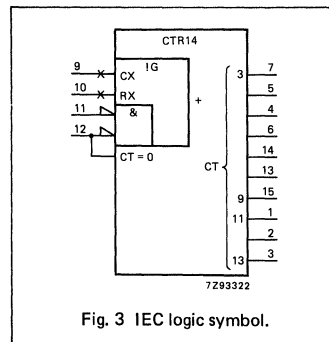


Fig. 3 IEC logic symbol.

**DYNAMIC POWER DISSIPATION FOR 74HC**

PARAMETER	V <sub>CC</sub> V	TYPICAL FORMULA FOR P <sub>D</sub> (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P <sub>D</sub> )	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1750 \times V_{CC}$
	6.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3800 \times V_{CC}$

GND = 0 V; T<sub>amb</sub> = 25 °C

**DYNAMIC POWER DISSIPATION FOR 74HCT**

PARAMETER	V <sub>CC</sub> V	TYPICAL FORMULA FOR P <sub>D</sub> (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P <sub>D</sub> )	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma(C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1750 \times V_{CC}$

GND = 0 V; T<sub>amb</sub> = 25 °C

**Notes**

1. Where: f<sub>o</sub> = output frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>osc</sub> = oscillator frequency in MHz      C<sub>t</sub> = timing capacitance in pF  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs      V<sub>CC</sub> = supply voltage in V

**APPLICATIONS**

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

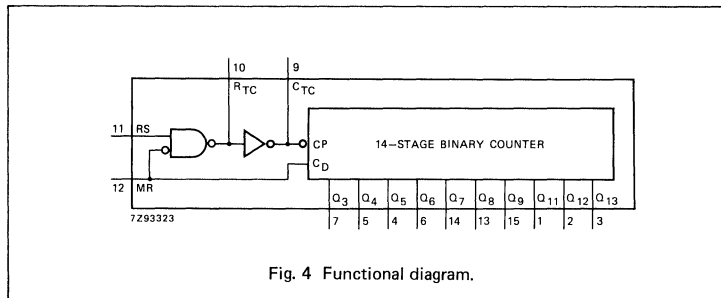


Fig. 4 Functional diagram.

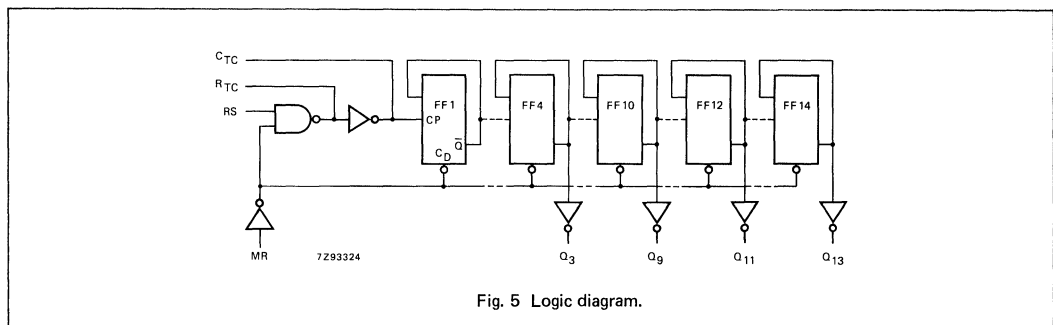


Fig. 5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

Output capability: standard (except for  $R_{TC}$  and  $C_{TC}$ ) $I_{CC}$  category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage MR input	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage MR input		0.7 1.8 2.3	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V <sub>IH</sub>	HIGH level input voltage RS input	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage RS input			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage R <sub>TC</sub> output	3.98 5.48			3.84 5.34		3.7 5.2	V	4.5 6.0	RS=GND and MR=GND	-I <sub>O</sub> = 2.6 mA -I <sub>O</sub> = 3.3 mA	
		3.98 5.48			3.84 5.34		3.7 5.2	V	4.5 6.0	RS=V <sub>CC</sub> and MR=V <sub>CC</sub>	-I <sub>O</sub> = 0.65 mA -I <sub>O</sub> = 0.85 mA	
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	RS=GND and MR=GND	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	RS=V <sub>CC</sub> and MR=V <sub>CC</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage C <sub>TC</sub> output	3.98 5.48			3.84 5.34		3.7 5.2	V	4.5 6.0	RS=V <sub>IH</sub> and MR=V <sub>IL</sub>	-I <sub>O</sub> = 3.2 mA -I <sub>O</sub> = 4.2 mA	
V <sub>OH</sub>	HIGH level output voltage except R <sub>TC</sub> output	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage except R <sub>TC</sub> and C <sub>TC</sub> outputs	3.98 5.48			3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage R <sub>TC</sub> output			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	RS=V <sub>CC</sub> and MR=GND	I <sub>O</sub> = 2.6 mA I <sub>O</sub> = 3.3 mA
			0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	RS=V <sub>CC</sub> and MR=GND	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
				0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	RS=V <sub>IL</sub> and MR=V <sub>IH</sub>	I <sub>O</sub> = 3.2 mA I <sub>O</sub> = 4.2 mA

(continued on next page)

DC CHARACTERISTICS FOR 74HC (continued)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>OL</sub>	LOW level output voltage except R <sub>TC</sub> output	0	0	0.1	0.1	0.1	0.1	0.1	2.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage except R <sub>TC</sub> and C <sub>TC</sub> outputs			0.26	0.26	0.33	0.33	0.4	0.4	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current			8.0		80.0		160.0	μA	6.0	V <sub>CC</sub> or GND I <sub>O</sub> = 0	

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/t_{PLH}$	propagation delay RS to $Q_3$		99 36 29	30 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 11
$t_{PHL}/t_{PLH}$	propagation delay $Q_n$ to $Q_{n+1}$		22 8 6	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 13
$t_{PHL}$	propagation delay MR to $Q_n$		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 12
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 11
$t_W$	clock pulse width RS; HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 11
$t_W$	master reset pulse width MR; HIGH	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 12
$t_{rem}$	removal time MR to RS	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
$f_{max}$	maximum clock pulse frequency	6 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

Output capability: standard (except for  $R_{TC}$  and  $C_{TC}$ )

$I_{CC}$  category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HCT							$V_{CC}$ V	$V_I$	OTHER		
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.					max.	
$V_{IH}$	HIGH level input voltage	2.0			2.0			2.0		V	4.5 to 5.5		note 2
$V_{IL}$	LOW level input voltage			0.8		0.8		0.8		V	4.5 to 5.5		note 2
$V_{OH}$	HIGH level output voltage $R_{TC}$ output	3.98			3.84			3.7		V	4.5	RS=GND and MR=GND	$-I_O = 2.6$ mA
		3.98			3.84			3.7		V	4.5	RS= $V_{CC}$ and MR= $V_{CC}$	$-I_O = 0.65$ mA
		4.4	4.5		4.4			4.4		V	4.5	RS=GND and MR=GND	$-I_O = 20$ $\mu$ A
		4.4	4.5		4.4			4.4		V	4.5	RS= $V_{CC}$ and MR= $V_{CC}$	$-I_O = 20$ $\mu$ A
$V_{OH}$	HIGH level output voltage $C_{TC}$ output	3.98			3.84			3.7		V	4.5	RS= $V_{IH}$ and MR= $V_{IL}$	$-I_O = 3.2$ mA
$V_{OH}$	HIGH level output voltage except $R_{TC}$ output	4.4	4.5		4.4			4.4		V	4.5	$V_{IH}$ or $V_{IL}$	$-I_O = 20$ $\mu$ A
$V_{OH}$	HIGH level output voltage except $R_{TC}$ and $C_{TC}$ outputs	3.98			3.84			3.7		V	4.5	$V_{IH}$ or $V_{IL}$	$-I_O = 4.0$ mA
$V_{OL}$	LOW level output voltage $R_{TC}$ output			0.26		0.33		0.4		V	4.5	RS= $V_{CC}$ and MR=GND	$I_O = 2.6$ mA
			0	0.1		0.1		0.1		V	4.5	RS= $V_{CC}$ and MR=GND	$I_O = 20$ $\mu$ A
$V_{OL}$	LOW level output voltage $C_{TC}$ output			0.26		0.33		0.4		V	4.5	RS= $V_{IL}$ and MR= $V_{IH}$	$I_O = 3.2$ mA
$V_{OL}$	LOW level output voltage except $R_{TC}$ output		0	0.1		0.1		0.1		V	4.5	$V_{IH}$ or $V_{IL}$	$I_O = 20$ $\mu$ A
$V_{OL}$	LOW level output voltage except $R_{TC}$ and $C_{TC}$ outputs			0.26		0.33		0.4		V	4.5	$V_{IH}$ or $V_{IL}$	$I_O = 4.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0		$\mu$ A	5.5	$V_{CC}$ or GND	

(continued on next page)

DC CHARACTERISTICS FOR 74HCT (continued)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
I <sub>CC</sub>	quiescent supply current			8.0		80.0		160.0	μA	5.5	V <sub>CC</sub> or GND	I <sub>O</sub> = 0
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0

Notes to HCT types

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.  
To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.
- Only input MR (pin 12) has TTL input switching levels for the HCT versions.

input	unit load coefficient
MR	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay RS to Q <sub>3</sub>		33	66		83		99	ns	4.5	Fig. 11
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay Q <sub>n</sub> to Q <sub>n+1</sub>		8	16		20		24	ns	4.5	Fig. 13
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		21	44		55		66	ns	4.5	Fig. 12
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 11
t <sub>W</sub>	clock pulse width RS; HIGH or LOW	16	6		20		24		ns	4.5	Fig. 11
t <sub>W</sub>	master reset pulse width MR; HIGH	16	7		20		24		ns	4.5	Fig. 12
t <sub>rem</sub>	removal time MR to RS	26	13		33		39		ns	4.5	Fig. 12
f <sub>max</sub>	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 11

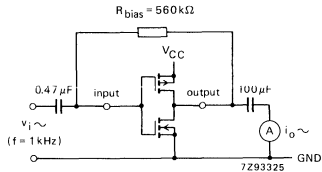


Fig. 6 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig. 7);  $MR = LOW$ .

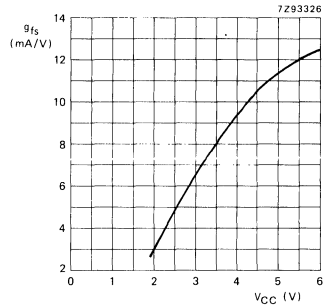


Fig. 7 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage  $V_{CC}$  at  $T_{amb} = 25^\circ C$ .

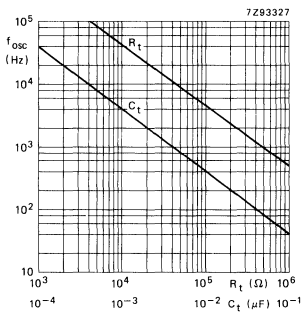


Fig. 8 RC oscillator frequency as a function of  $R_t$  and  $C_t$  at  $V_{CC} = 2.0$  to  $6.0$  V;  $T_{amb} = 25^\circ C$ .  
 $C_t$  curve at  $R_t = 100$  kΩ;  $R_2 = 200$  kΩ.  
 $R_t$  curve at  $C_t = 1$  nF;  $R_2 = 2 \times R_t$ .

RC OSCILLATOR

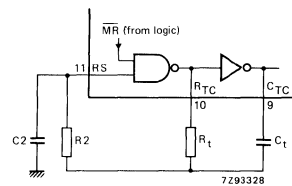


Fig. 9 Example of a RC oscillator.  
 Typical formula for oscillator frequency:  

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

TIMING COMPONENT LIMITATIONS

The oscillator frequency is mainly determined by  $R_t C_t$ , provided  $R_2 \approx 2R_t$  and  $R_2 C_2 \ll R_t C_t$ . The function of  $R_2$  is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance  $C_2$  should be kept as small as possible. In consideration of accuracy,  $C_t$  must be larger than the inherent stray capacitance.  $R_t$  must be larger than the "ON" resistance in series with it, which typically is 280 Ω at  $V_{CC} = 2.0$  V, 130 Ω at  $V_{CC} = 4.5$  V and 100 Ω at  $V_{CC} = 6.0$  V. The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t > 50$  pF, up to any practical value,

$10$  kΩ  $< R_t < 1$  MΩ.



**TYPICAL CRYSTAL OSCILLATOR**

In Fig. 10, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

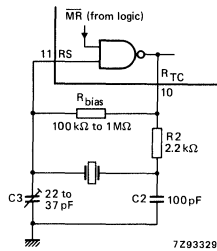


Fig. 10 External components connection for a crystal oscillator.

**AC WAVEFORMS**

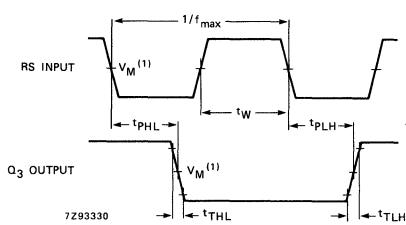


Fig. 11 Waveforms showing the clock (RS) to output (Q<sub>3</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

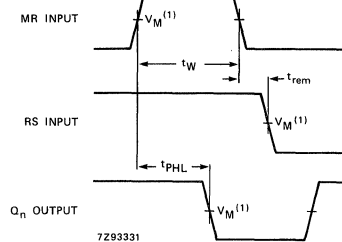


Fig. 12 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q<sub>n</sub>) propagation delays and the master reset to clock (RS) removal time.

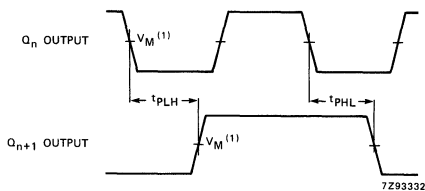


Fig. 13 Waveforms showing the output (Q<sub>n</sub>) to Q<sub>n+1</sub> propagation delays.

**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4066

SSI

## QUAD BILATERAL SWITCHES

### FEATURES

- Very low "ON" resistance:  
 $50 \Omega$  (typ.) at  $V_{CC} = 4.5 \text{ V}$   
 $45 \Omega$  (typ.) at  $V_{CC} = 6.0 \text{ V}$   
 $35 \Omega$  (typ.) at  $V_{CC} = 9.0 \text{ V}$
- Output capability: non-standard
- I<sub>CC</sub> category: SSI

### GENERAL DESCRIPTION

The 74HC/HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the "4066" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4066 have four independent analog switches.

Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the belonging analog switch is turned off.

The "4066" is pin compatible with the "4016" but exhibits a much lower "ON" resistance. In addition, the "ON" resistance is relatively constant over the full input signal range.

### FUNCTION TABLE

INPUT nE	SWITCH
L	off
H	on

H = HIGH voltage level  
 L = LOW voltage level

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>pZL</sub> / t <sub>pZH</sub>	propagation delay turn-on time	$R_L = 1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$ $V_{CC} = 5 \text{ V}$	17	19	ns
t <sub>pLZ</sub> / t <sub>pHZ</sub>	propagation delay turn-off time		15	17	ns
C <sub>i</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4066P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT4066T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
7	GND	ground (0 V)
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
14	V <sub>CC</sub>	positive supply voltage

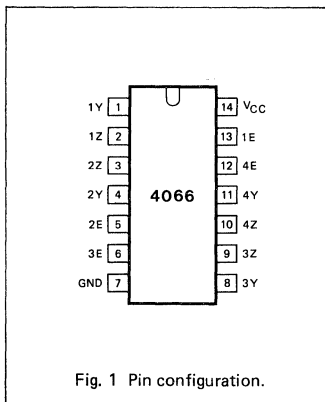


Fig. 1 Pin configuration.

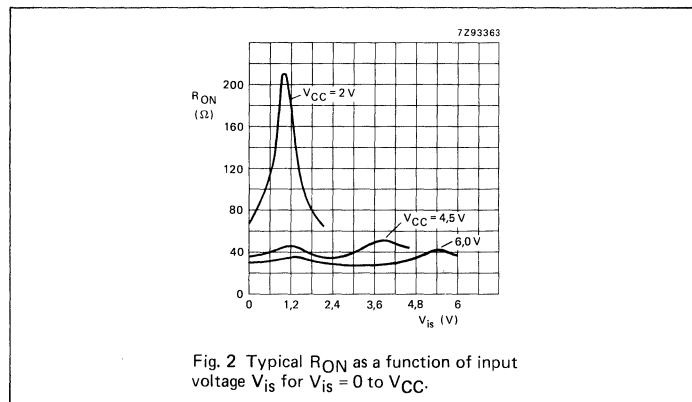


Fig. 2 Typical R<sub>ON</sub> as a function of input voltage V<sub>is</sub> for V<sub>is</sub> = 0 to V<sub>CC</sub>.

16-CHANNEL ANALOG MULTIPLEXER/DEMULPLEXER

FEATURES

- Low "ON" resistance:  
80 Ω (typ.) at V<sub>CC</sub> = 4.5 V  
70 Ω (typ.) at V<sub>CC</sub> = 6.0 V  
60 Ω (typ.) at V<sub>CC</sub> = 9.0 V
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S<sub>0</sub> to S<sub>3</sub>), an active LOW enable input ( $\bar{E}$ ), sixteen independent inputs/outputs (Y<sub>0</sub> to Y<sub>15</sub>) and a common input/output (Z).

The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y<sub>0</sub> to Y<sub>15</sub>) and the other side connected to a common input/output (Z).

With  $\bar{E}$  LOW, one of the sixteen switches is selected (low impedance ON-state) by S<sub>0</sub> to S<sub>3</sub>. All unselected switches are in the high impedance OFF-state. With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of S<sub>0</sub> to S<sub>3</sub>.

The analog inputs/outputs (Y<sub>0</sub> to Y<sub>15</sub>, and Z) can swing between V<sub>CC</sub> as a positive limit and GND as a negative limit. V<sub>CC</sub> to GND may not exceed 6.0 V.

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

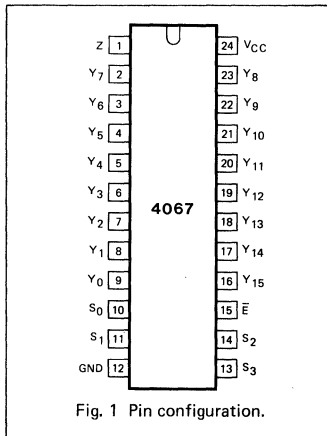


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
tpZL/ tpZH	propagation delay turn-on time	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF V <sub>CC</sub> = 5 V	27	29	ns
tpLZ/ tpHZ	propagation delay turn-off time		25	27	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4067P: 24-lead DIL; plastic (SOT-101A).  
PC74HC/HCT4067T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Z	common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y <sub>0</sub> to Y <sub>15</sub>	independent inputs/outputs
10, 11, 14, 13	S <sub>0</sub> to S <sub>3</sub>	address inputs
12	GND	ground (0 V)
15	$\bar{E}$	enable input (active LOW)
24	V <sub>CC</sub>	positive supply voltage

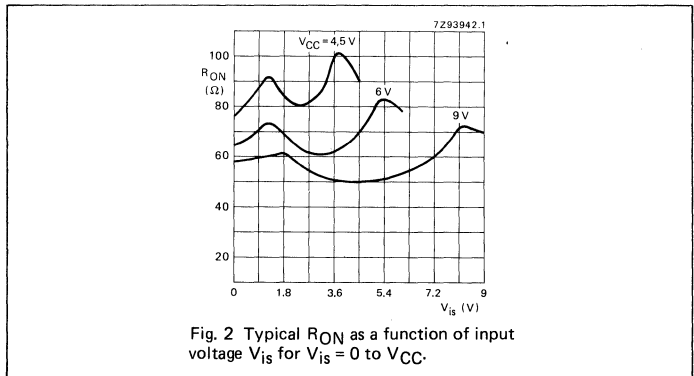


Fig. 2 Typical R<sub>ON</sub> as a function of input voltage V<sub>is</sub> for V<sub>is</sub> = 0 to V<sub>CC</sub>.

FUNCTION TABLE

$\bar{E}$	INPUTS				CHANNEL ON
	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	
L	L	L	L	L	Y <sub>0</sub> - Z
L	L	L	L	H	Y <sub>1</sub> - Z
L	L	L	H	L	Y <sub>2</sub> - Z
L	L	L	H	H	Y <sub>3</sub> - Z
L	L	H	L	L	Y <sub>4</sub> - Z
L	L	H	L	H	Y <sub>5</sub> - Z
L	L	H	H	L	Y <sub>6</sub> - Z
L	L	H	H	H	Y <sub>7</sub> - Z
L	H	L	L	L	Y <sub>8</sub> - Z
L	H	L	L	H	Y <sub>9</sub> - Z
L	H	L	H	L	Y <sub>10</sub> - Z
L	H	L	H	H	Y <sub>11</sub> - Z
L	H	H	L	L	Y <sub>12</sub> - Z
L	H	H	L	H	Y <sub>13</sub> - Z
L	H	H	H	L	Y <sub>14</sub> - Z
L	H	H	H	H	Y <sub>15</sub> - Z
H	X	X	X	X	none

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

DEVELOPMENT DATA

TRIPLE 3-INPUT OR GATE

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4075 are high-speed Si-gate CMOS devices and are pin compatible with the "4075" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4075 provide the 3-input OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per gate	notes 1 and 2	28	32	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4075P: 14-lead DIL; plastic (SOT-27).

PC74HC/HCT4075T: 14-lead mini-pack; plastic (SO-14; SOT-108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	data inputs
4, 2, 12	1B to 3B	data inputs
5, 8, 13	1C to 3C	data inputs
6, 9, 10	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage

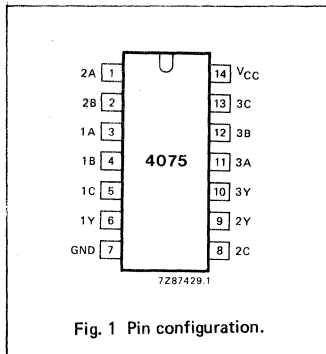


Fig. 1 Pin configuration.

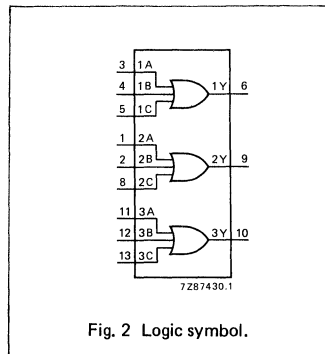


Fig. 2 Logic symbol.

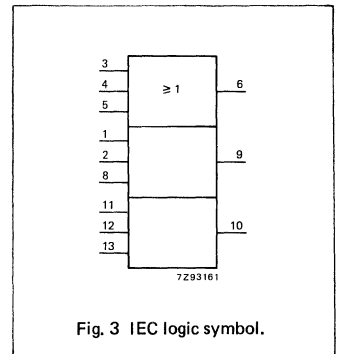


Fig. 3 IEC logic symbol.

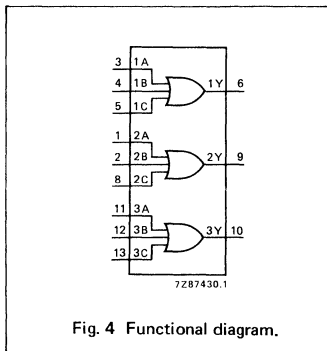


Fig. 4 Functional diagram.

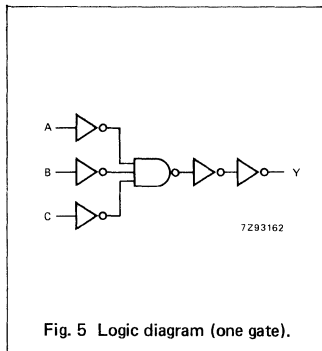


Fig. 5 Logic diagram (one gate).

FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		28 10 8	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
nA, nB, nC	1.60

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA, nB, nC to nY		12	24		30		36	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6

**AC WAVEFORMS**

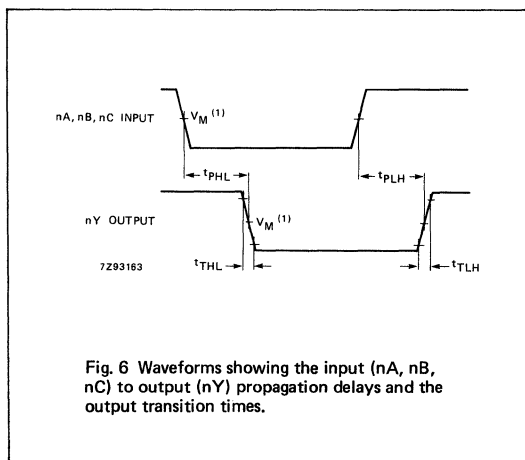


Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

**Note to AC waveforms**

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

## 8-STAGE SHIFT-AND-STORE BUS REGISTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4094 are high-speed Si-gate CMOS devices and are pin compatible with the "4094" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP<sub>0</sub> to QP<sub>7</sub>). The parallel outputs may be connected directly to common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS<sub>1</sub> and QS<sub>2</sub>) are available for cascading a number of "4094" devices. Data is available at QS<sub>1</sub> on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS<sub>2</sub> on the next negative-going clock edge and is for cascading "4094" devices when the clock rise time is slow.

### APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>1</sub> CP to QS <sub>2</sub> CP to QP <sub>n</sub> STR to QP <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	15	19	ns
			13	18	ns
			20	21	ns
			18	19	ns
f <sub>max</sub>	maximum clock frequency		95	86	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	83	92	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

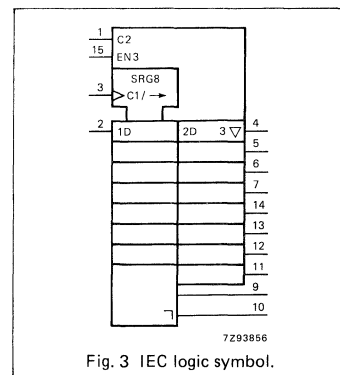
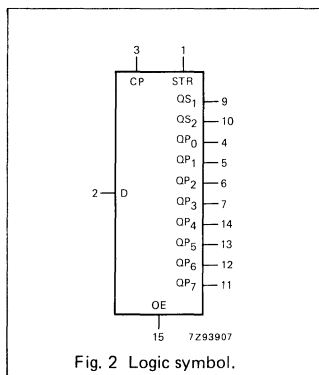
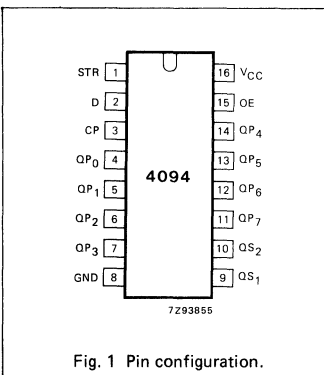
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4094P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4094T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP <sub>0</sub> to QP <sub>7</sub>	parallel outputs
8	GND	ground (0 V)
9, 10	QS <sub>1</sub> , QS <sub>2</sub>	serial outputs
15	OE	output enable input
16	V <sub>CC</sub>	positive supply voltage





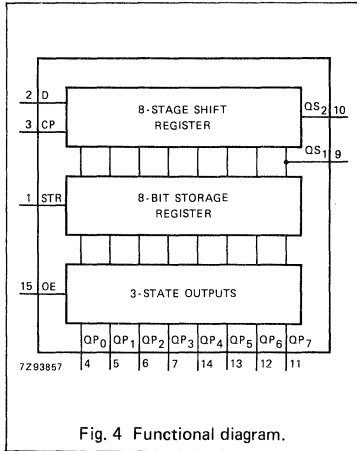


Fig. 4 Functional diagram.

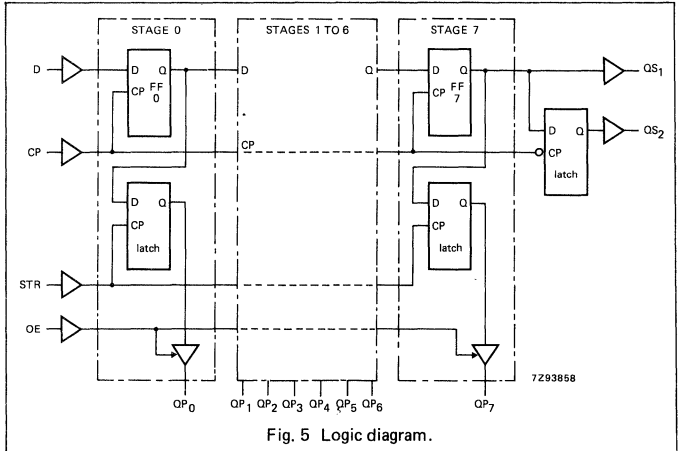


Fig. 5 Logic diagram.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP <sub>0</sub>	QP <sub>n</sub>	QS <sub>1</sub>	QS <sub>2</sub>
↑	L	X	X	Z	Z	Q' <sub>6</sub>	NC
↓	L	X	X	Z	Z	NC	QP <sub>7</sub>
↑	H	L	X	NC	NC	Q' <sub>6</sub>	NC
↑	H	H	L	L	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↑	H	H	H	H	QP <sub>n-1</sub>	Q' <sub>6</sub>	NC
↓	H	H	H	NC	NC	NC	QP <sub>7</sub>

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

NC = no change

↑ = LOW-to-HIGH CP transition

↓ = HIGH-to-LOW CP transition

Q'<sub>6</sub> = the information in the seventh register stage is transferred to the 8th register stage and QS<sub>n</sub> output at the positive clock edge

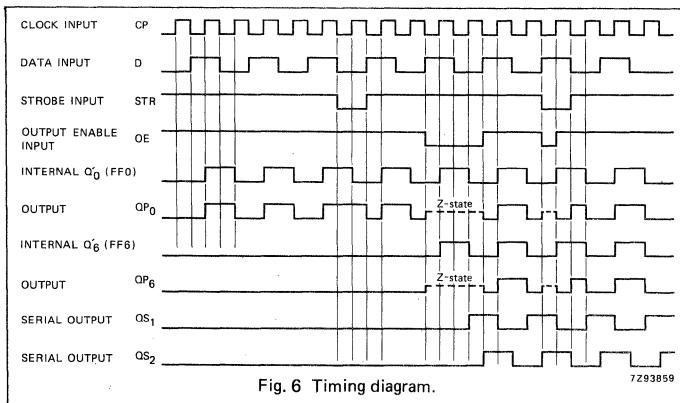


Fig. 6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>1</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>2</sub>		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QP <sub>n</sub>		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay STR to QP <sub>n</sub>		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig. 8
t <sup>THL</sup> / t <sup>TLH</sup>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to QP <sub>n</sub>		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to QP <sub>n</sub>		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	strobe pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time D to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>h</sub>	hold time D to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 10
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	28 87 103		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE, CP	1.50
D	0.40
STR	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>1</sub>		22	39		49		59	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QS <sub>2</sub>		21	36		45		54	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to QP <sub>n</sub>		25	43		54		65	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay STR to QP <sub>n</sub>		22	39		49		59	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to QP <sub>n</sub>		20	35		44		53	ns	4.5	Fig. 9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to QP <sub>n</sub>		20	35		44		53	ns	4.5	Fig. 9
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 7
t <sub>W</sub>	strobe pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time D to CP	10	4		13		15		ns	4.5	Fig. 10
t <sub>h</sub>	hold time D to CP	4	-1		4		4		ns	4.5	Fig. 10
f <sub>max</sub>	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 7

AC WAVEFORMS

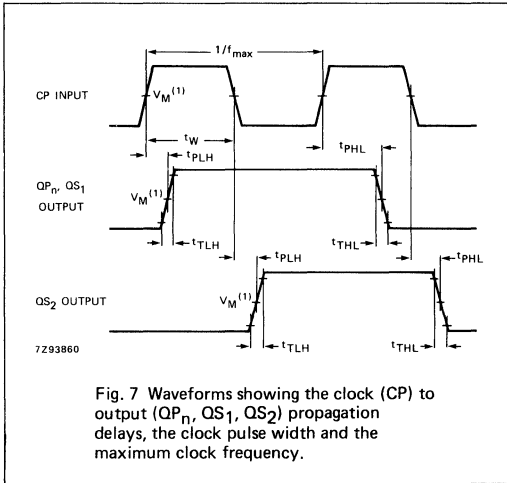


Fig. 7 Waveforms showing the clock (CP) to output (QP<sub>n</sub>, QS<sub>1</sub>, QS<sub>2</sub>) propagation delays, the clock pulse width and the maximum clock frequency.

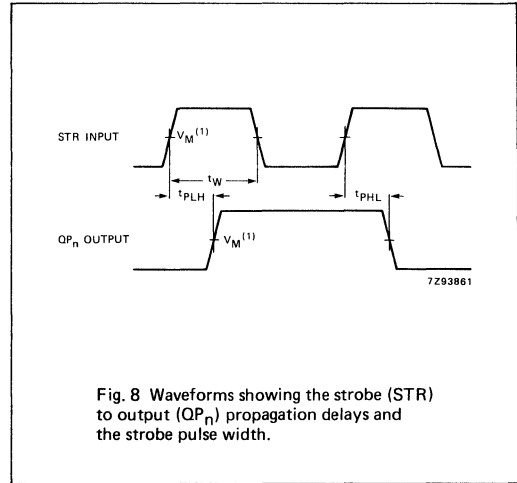


Fig. 8 Waveforms showing the strobe (STR) to output (QP<sub>n</sub>) propagation delays and the strobe pulse width.

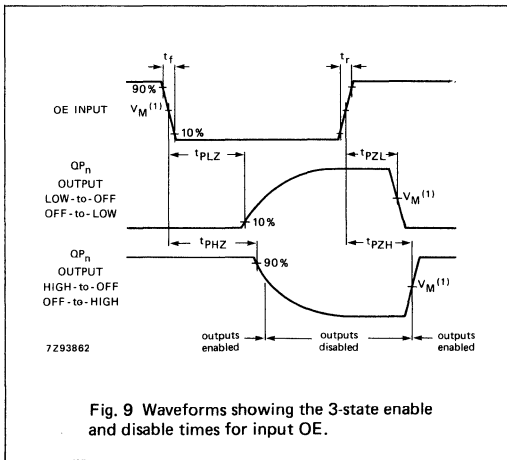


Fig. 9 Waveforms showing the 3-state enable and disable times for input OE.

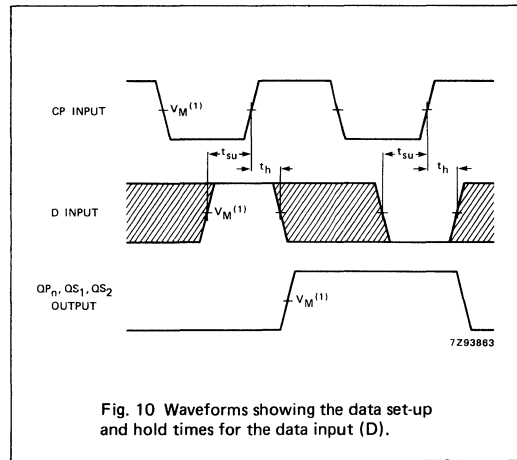


Fig. 10 Waveforms showing the data set-up and hold times for the data input (D).

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_1 = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3\text{ V}$ ;  $V_1 = \text{GND to } 3\text{ V}$ .

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.



QUAD BILATERAL SWITCHES

FEATURES

- Low "ON" resistance:  
90 Ω (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$   
80 Ω (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$   
65 Ω (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation:  
to enable 5 V logic to communicate  
with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4316 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4316 have four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input (E) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V<sub>CC</sub> current provided the voltage at the terminals of the switch is maintained within the supply voltage range;  $V_{CC} \gg (V_Y, V_Z) \gg V_{EE}$ . Inputs nY and nZ are electrically equivalent terminals.

V<sub>CC</sub> and GND are the supply voltage pins for the digital control inputs ( $\bar{E}$  and nS). The V<sub>CC</sub> to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY and nZ) can swing between V<sub>CC</sub> as a positive limit and V<sub>EE</sub> as a negative limit. V<sub>CC</sub> - V<sub>EE</sub> may not exceed 10.0 V. See the "4016" for the version without logic level translation.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PZH</sub>	turn "ON" time E to V <sub>OS</sub> nS to V <sub>OS</sub>	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 kΩ V <sub>CC</sub> = 5 V	19	19	ns
			16	17	ns
t <sub>PZL</sub>	turn "ON" time E to V <sub>OS</sub> nS to V <sub>OS</sub>		19	24	ns
			16	21	ns
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time E to V <sub>OS</sub> nS to V <sub>OS</sub>		20	21	ns
			16	19	ns
C <sub>I</sub>	input capacitance	3.5	3.5	pF	
C <sub>PD</sub>	power dissipation capacitance per switch	notes 1 and 2	13	14	pF
C <sub>S</sub>	max. switch capacitance		5	5	pF

V<sub>EE</sub> = GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

where:  
 $f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $C_S$  = max. switch capacitance in pF  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4316P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT4316T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

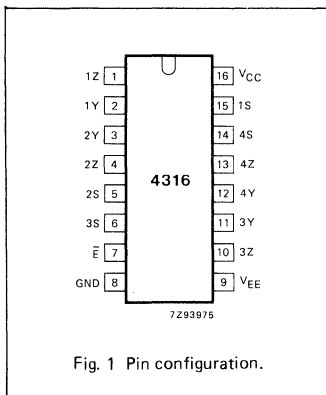


Fig. 1 Pin configuration.

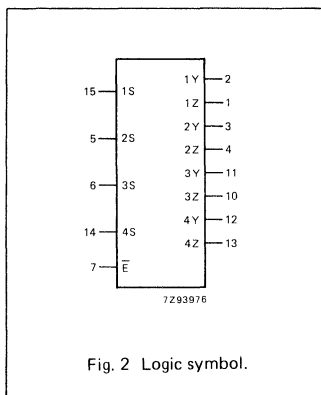


Fig. 2 Logic symbol.

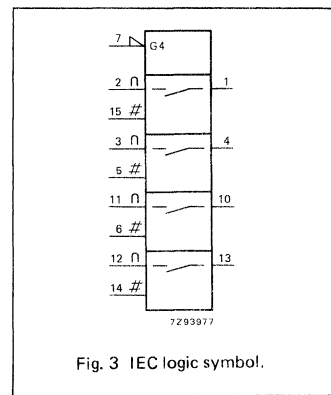


Fig. 3 IEC logic symbol.

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	$\bar{E}$	enable input (active LOW)
8	GND	ground (0 V)
9	$V_{EE}$	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	$V_{CC}$	positive supply voltage

**FUNCTION TABLE**

INPUTS		SWITCH
$\bar{E}$	nS	
L	L	off
L	H	on
H	X	off

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

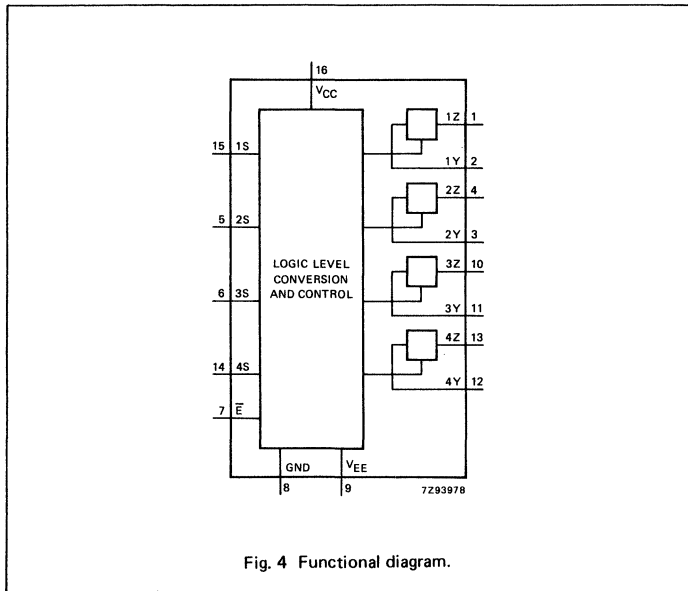


Fig. 4 Functional diagram.

**APPLICATIONS**

- Signal gating
- Modulation
- Demodulation
- Chopper

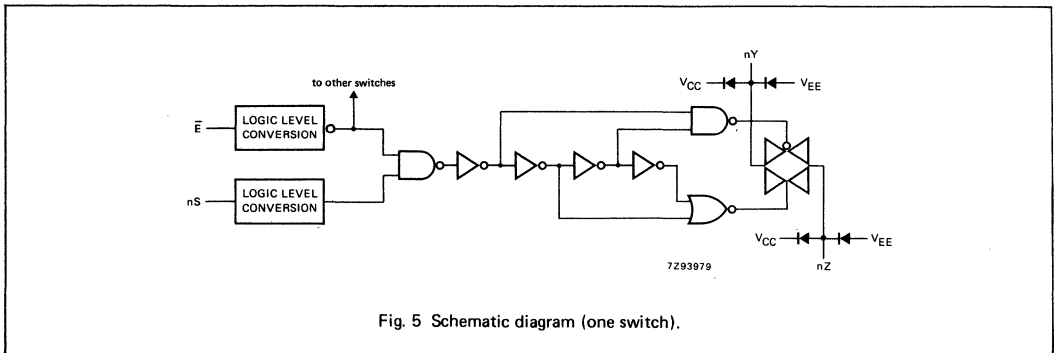


Fig. 5 Schematic diagram (one switch).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	$^{\circ}\text{C}$	
$P_{tot}$	power dissipation per package				for temperature range: $-40$ to $+125$ $^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		500	mW	above $+70$ $^{\circ}\text{C}$ : derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above $+70$ $^{\circ}\text{C}$ : derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$



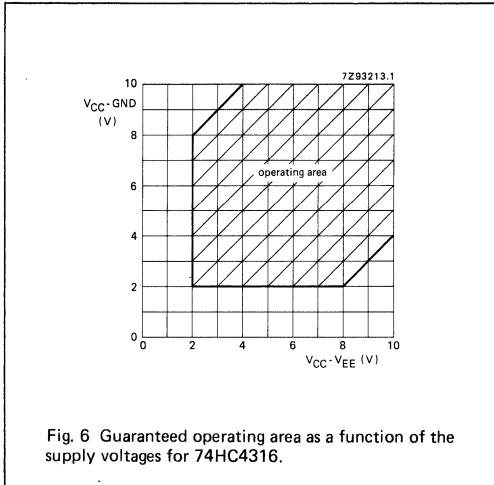


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4316.

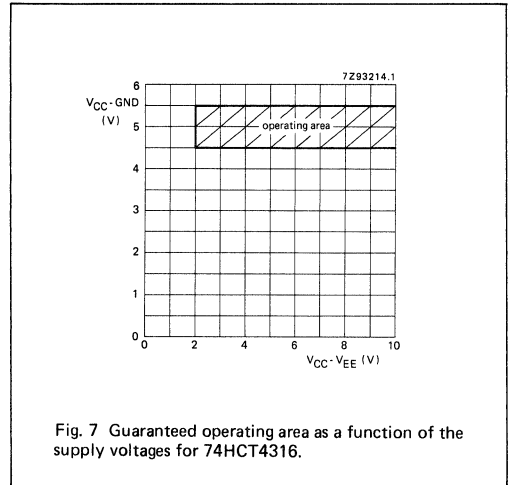


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4316.

**DC CHARACTERISTICS FOR 74HC/HCT**

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_S$ $\mu A$	$V_{is}$	$V_I$
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
$R_{ON}$	ON resistance	-	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		160	320	400	480	$\Omega$	4.5	0	1000				
		120	240	300	360	$\Omega$	6.0	0	1000				
$R_{ON}$	ON resistance	85	170	215	255	$\Omega$	4.5	-4.5	1000	$V_{EE}$	$V_{IH}$ or $V_{IL}$		
		160	-	-	-	$\Omega$	2.0	0	100				
		80	160	200	240	$\Omega$	4.5	0	1000				
$R_{ON}$	ON resistance	70	140	175	210	$\Omega$	6.0	0	1000	$V_{CC}$	$V_{IH}$ or $V_{IL}$		
		60	120	150	180	$\Omega$	4.5	-4.5	1000				
		170	-	-	-	$\Omega$	2.0	0	100				
$R_{ON}$	ON resistance	90	180	225	270	$\Omega$	4.5	0	1000	$V_{CC}$	$V_{IH}$ or $V_{IL}$		
		80	160	200	240	$\Omega$	6.0	0	1000				
		65	135	170	205	$\Omega$	4.5	-4.5	1000				
$\Delta R_{ON}$	maximum $\Delta R_{ON}$ resistance between any two channels	-	-	-	-	-	-	$\Omega$	2.0	0	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$	
		16	-	-	-	$\Omega$	4.5	0					
		9	-	-	-	$\Omega$	6.0	0					
		6	-	-	-	$\Omega$	4.5	-4.5					

**Notes to DC characteristics**

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS					
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER		
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.						max.	
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0				
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND		
±I <sub>S</sub>	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)	
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)	
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>	

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{os}$		61 22 18 19	205 41 35 37		255 51 43 47		310 62 53 56	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time nS to $V_{os}$		52 19 15 17	175 35 30 34		220 44 37 43		265 53 45 51	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{os}$		63 23 18 21	220 44 37 39		275 55 47 49		330 66 56 59	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time nS to $V_{os}$		52 19 15 18	175 35 30 36		220 44 37 45		265 53 45 54	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)

## DC CHARACTERISTICS FOR 74HCT

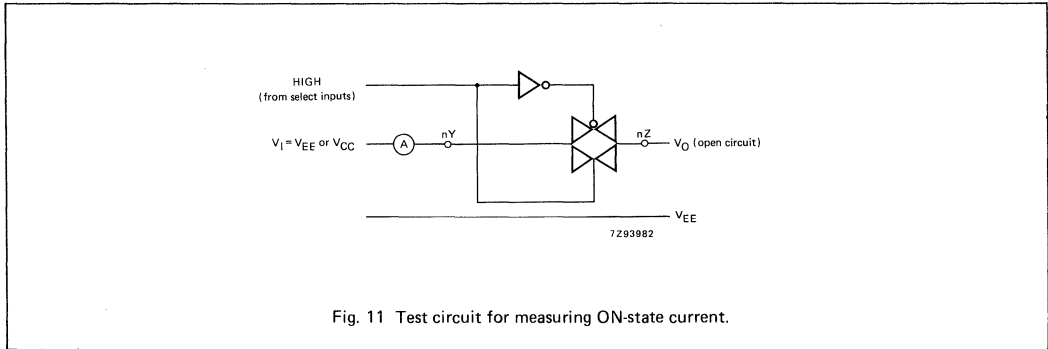
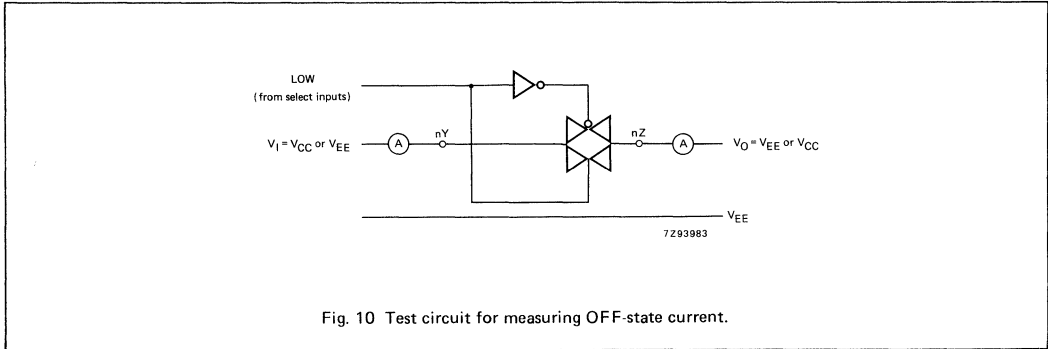
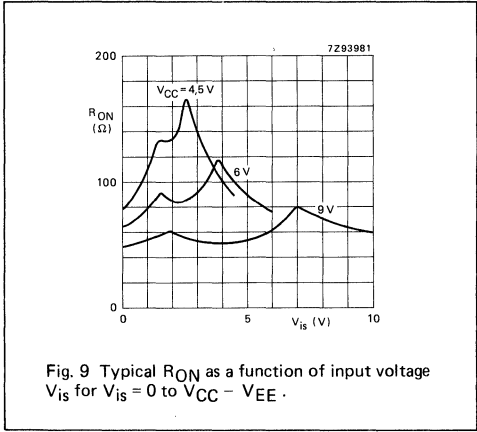
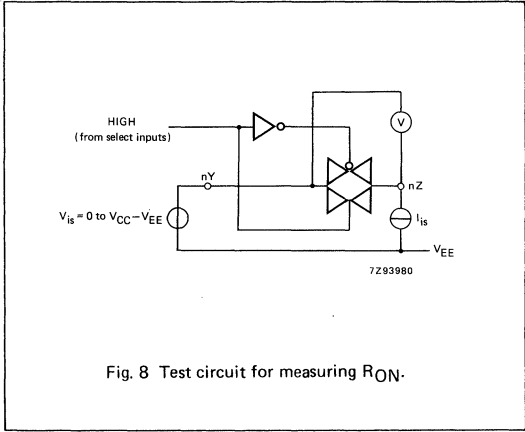
Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1V	other inputs at V <sub>CC</sub> or GND

## Note to HCT types

1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S <sub>n</sub>	0.50
E <sub>n</sub>	0.50



## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}$	turn "ON" time $\bar{E}$ to $V_{os}$		22 21	44 42		55 53		66 63	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PZL}$	turn "ON" time $\bar{E}$ to $V_{os}$		28 21	56 42		70 53		85 63	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PZH}$	turn "ON" time nS to $V_{os}$		20 17	40 34		53 43		60 51	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PZL}$	turn "ON" time nS to $V_{os}$		25 17	50 34		63 43		75 51	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}$ to $V_{os}$		25 23	50 46		53 58		75 69	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time nS to $V_{os}$		22 20	44 40		55 50		66 60	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Figs 19, 20 and 21)

## ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ 

SYMBOL	PARAMETER	typ.	UNIT	V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>is(p-p)</sub> V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF (see Figs 12 and 15)
	crosstalk between any two switches	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz; (see Fig. 16)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E or nS, square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig. 17)
f <sub>max</sub>	minimum frequency response (-3 dB)	150 160	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance	5	pF				

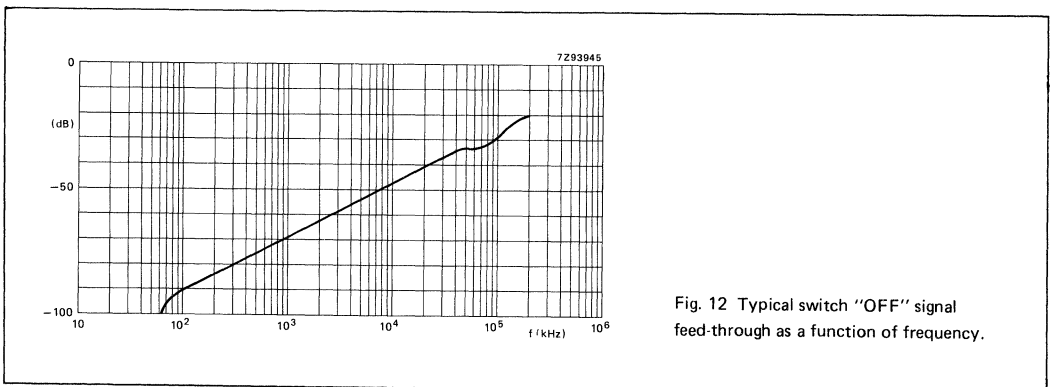
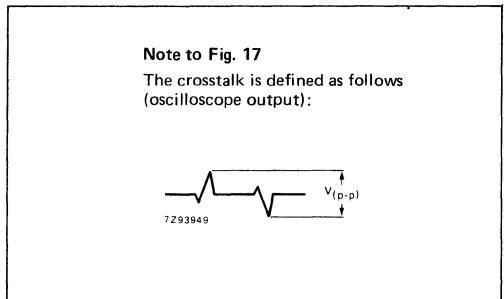
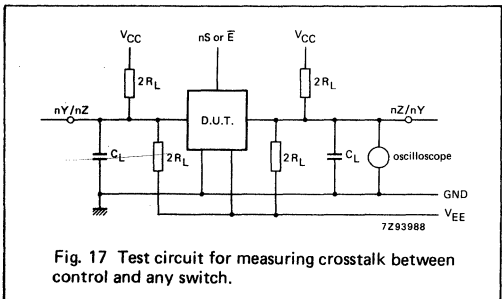
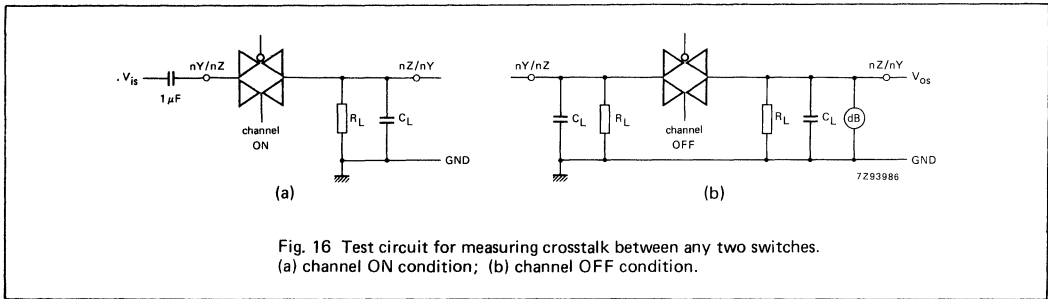
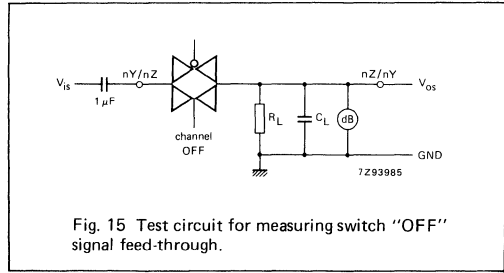
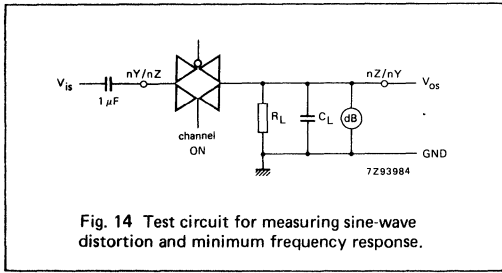
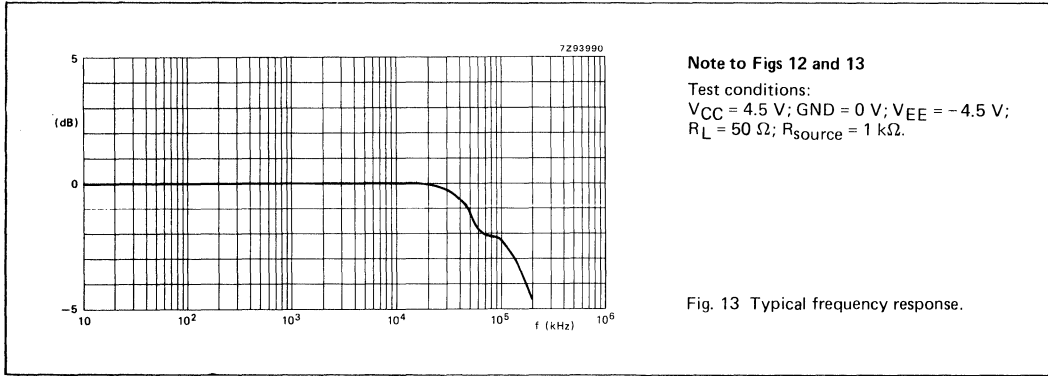
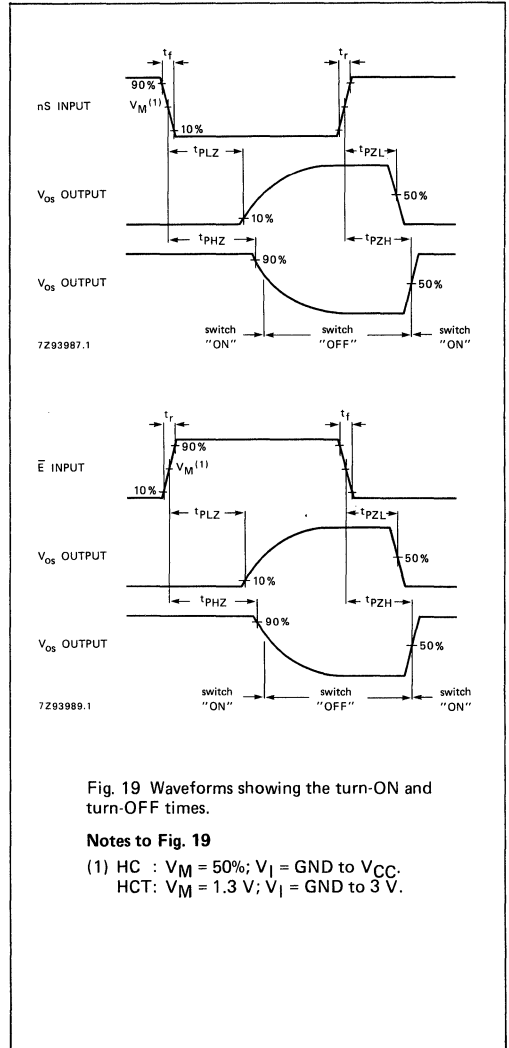
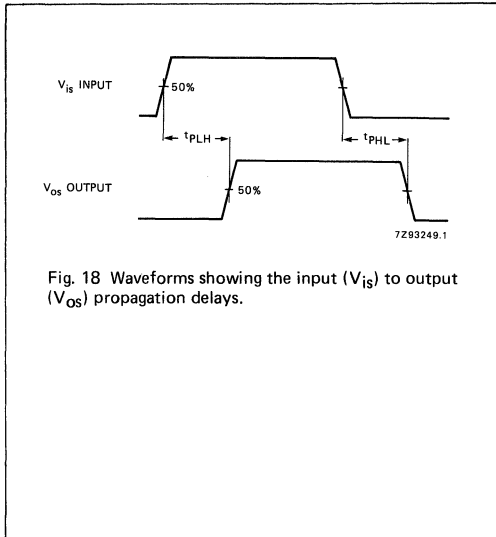


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.





AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

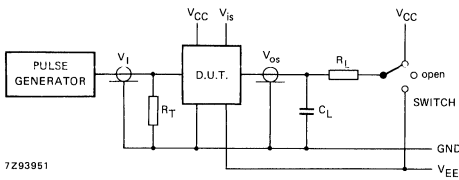


Fig. 20 Test circuit for measuring AC performance.

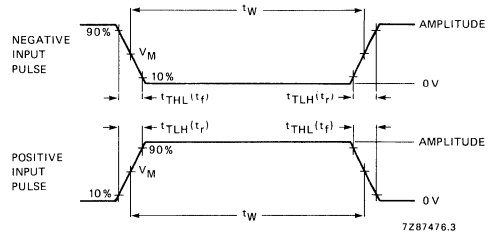


Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.

t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.



8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

FEATURES

- Wide analog input voltage range:  $\pm 5\text{ V}$
- Low "ON" resistance:  
 $80\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$   
 $70\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$   
 $60\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation:  
to enable 5 V logic to communicate with  $\pm 5\text{ V}$  analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4351 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4351 are 8-channel analog multiplexers/demultiplexers with three select inputs ( $S_0$  to  $S_2$ ), two enable inputs ( $E_1$  and  $E_2$ ), a latch enable input ( $\overline{LE}$ ), eight independent inputs/outputs ( $Y_0$  to  $Y_7$ ) and a common input/output ( $Z$ ).

With  $\overline{E}_1$  LOW and  $E_2$  is HIGH, one of the eight switches is selected (low impedance ON-state) by  $S_0$  to  $S_2$ . The data at the select inputs may be latched by using the active LOW latch enable input ( $\overline{LE}$ ). When  $\overline{LE}$  is HIGH the latch is transparent. When either of the two enable inputs,  $\overline{E}_1$  (active LOW) and  $E_2$  (active HIGH), is inactive, all 8 analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH}/t_{PZL}$	turn "ON" time $\overline{E}_1, E_2$ or $S_n$ to $V_{OS}$	$C_L = 15\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	27	35	ns
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\overline{E}_1, E_2$ or $S_n$ to $V_{OS}$		21	23	ns
$C_i$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	28	29	pF
$C_S$	max. switch capacitance independent common		5	5	pF
			25	25	pF

$V_{EE} = \text{GND} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

where:  
 $f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $C_S$  = max. switch capacitance in pF  
 $\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_1 = \text{GND}$  to  $V_{CC}$   
For HCT the condition is  $V_1 = \text{GND}$  to  $V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4351P: 20-lead DIL; plastic (SOT-146).  
PC74HC/HCT4351T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

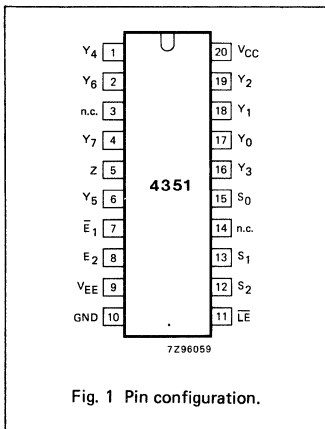


Fig. 1 Pin configuration.

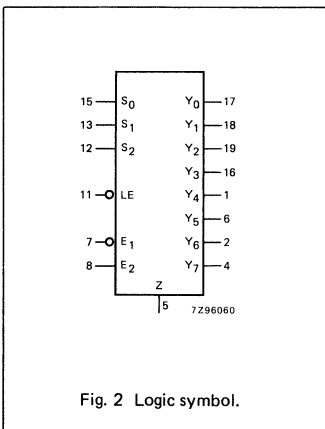


Fig. 2 Logic symbol.

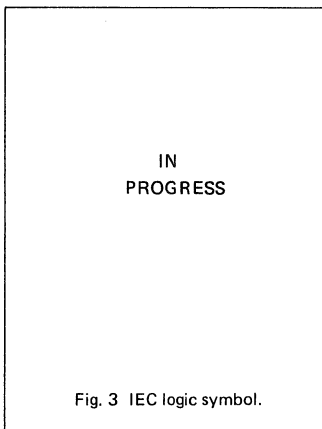


Fig. 3 IEC logic symbol.

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5	Z	common
3, 14	n.c.	not connected
7	$\bar{E}_1$	enable input (active LOW)
8	$E_2$	enable input (active HIGH)
9	$V_{EE}$	negative supply voltage
10	GND	ground (0 V)
11	$\bar{L}E$	latch enable input (active LOW)
15, 13, 12	$S_0$ to $S_2$	select inputs
17, 18, 19, 16, 1, 6, 2, 4	$Y_0$ to $Y_7$	independent inputs/outputs
20	$V_{CC}$	positive supply voltage

## GENERAL DESCRIPTION (Cont'd.)

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs ( $S_0$  to  $S_2$ ,  $\bar{L}E$ ,  $\bar{E}_1$  and  $E_2$ ). The  $V_{CC}$  to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs ( $Y_0$  to  $Y_7$ , and Z) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

## FUNCTION TABLE

INPUTS						CHANNEL ON
$\bar{E}_1$	$E_2$	$\bar{L}E$	$S_2$	$S_1$	$S_0$	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	$Y_0$
L	H	H	L	L	H	$Y_1$
L	H	H	L	H	L	$Y_2$
L	H	H	L	H	H	$Y_3$
L	H	H	H	L	L	$Y_4$
L	H	H	H	L	H	$Y_5$
L	H	H	H	H	L	$Y_6$
L	H	H	H	H	H	$Y_7$
L	H	L	X	X	X	*
X	X	↓	X	X	X	**

H = HIGH voltage level

L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW  $\bar{L}E$  transition

\* Last selected channel "ON".

\*\* Selected channels latched.

## APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

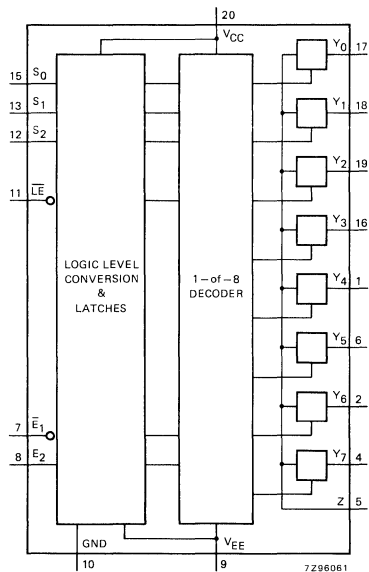


Fig. 4 Functional diagram.

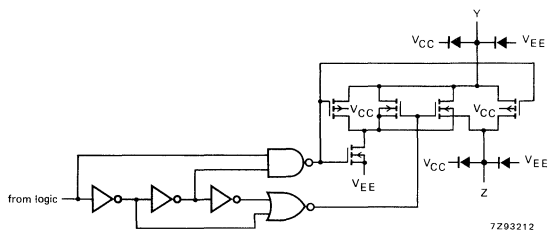


Fig. 5 Schematic diagram (one switch).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	$^{\circ}\text{C}$	
$P_{tot}$	power dissipation per package				for temperature range: $-40$ to $+125^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		500	mW	above $+70^{\circ}\text{C}$ : derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above $+70^{\circ}\text{C}$ : derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

## Note to ratings

To avoid drawing  $V_{CC}$  current out of terminal Z, when switch current flows in terminals  $Y_n$ , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{CC}$  current will flow out of terminals  $Y_n$ . In this case there is no limit for the voltage drop across the switch, but the voltages at  $Y_n$  and Z may not exceed  $V_{CC}$  or  $V_{EE}$ .

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}$ -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}$ - $V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

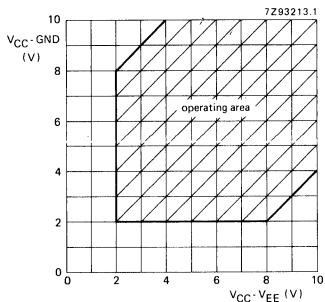


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4351.

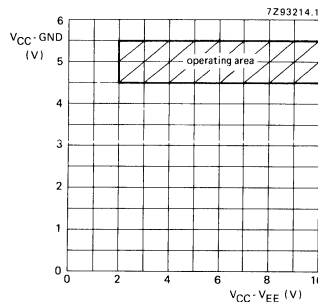


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4351.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_S$ $\mu A$	$V_{is}$	$V_i$
		+25		-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.		max.				
$R_{ON}$	ON resistance (peak)		—	—	—	—	—	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
			100	180	225	270		$\Omega$	4.5	0	1000		
			90	160	200	240		$\Omega$	6.0	0	1000		
			70	130	165	195		$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance		150	—	—	—	—	$\Omega$	2.0	0	100	$V_{EE}$	$V_{IH}$ or $V_{IL}$
			80	140	175	210		$\Omega$	4.5	0	1000		
			70	120	150	180		$\Omega$	6.0	0	1000		
			60	105	130	160		$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance		150	—	—	—	—	$\Omega$	2.0	0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$
			90	160	200	240		$\Omega$	4.5	0	1000		
			80	140	175	210		$\Omega$	6.0	0	1000		
			65	120	150	180		$\Omega$	4.5	-4.5	1000		
$\Delta R_{ON}$	maximum $\Delta ON$ resistance between any two channels		—					$\Omega$	2.0	0		$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
			9					$\Omega$	4.5	0			
			8					$\Omega$	6.0	0			
			6					$\Omega$	4.5	-4.5			

Notes to DC characteristics

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.



## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{Os}$		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 17)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{E}_1$ to $V_{Os}$		85 25 28	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $E_2$ to $V_{Os}$		85 31 25 25	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{L}E$ to $V_{Os}$		91 33 26 27	300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $S_n$ to $V_{Os}$		88 32 26 25	300 60 51 50		375 75 64 63		450 90 77 75	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}_1$ to $V_{Os}$		69 25 20 20	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $E_2$ to $V_{Os}$		72 26 21 19	250 50 43 40		315 63 54 50		375 75 64 60	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{L}E$ to $V_{Os}$		83 30 24 26	275 55 47 45		345 69 59 56		415 83 71 68	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $S_n$ to $V_{Os}$		80 29 23 24	275 55 47 48		345 69 59 60		415 83 71 71	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{su}$	set-up time $S_n$ to $\bar{L}E$		17 6 5 9	60 12 10 18		75 15 13 23		90 18 15 27	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_h$	hold time $S_n$ to $\bar{L}E$		-8 -3 -2 -4	5 5 5 5		5 5 5 5		5 5 5 5	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_W$	$\bar{L}E$ minimum pulse width HIGH		28 10 8 14	100 20 17 25		125 25 21 31		150 30 26 38	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)

## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS			
		74HCT									V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5				
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5				
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND		
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)	
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)	
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)	
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>	
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1V	other inputs at V <sub>CC</sub> or GND	

## Note to HCT types

1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E <sub>1</sub> , E <sub>2</sub>	0.50
S <sub>n</sub>	0.50
LE	1.5

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$	6 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 17)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{E}_1$ to $V_{os}$	40 31	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $E_2$ to $V_{os}$	35 26	70 50		88 63		105 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{LE}$ to $V_{os}$	42 37	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $S_n$ to $V_{os}$	39 30	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}_1$ to $V_{os}$	27 20	55 40		69 50		83 60	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $E_2$ to $V_{os}$	32 26	60 50		75 63		90 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{LE}$ to $V_{os}$	33 30	60 55		75 69		90 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $S_n$ to $V_{os}$	33 29	65 55		81 69		98 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 18)
$t_{su}$	set-up time $S_n$ to $\bar{LE}$	6 7	12 14		15 18		18 21	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_h$	hold time $S_n$ to $\bar{LE}$	-1 -2	5 5		5 5		5 5	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_w$	$\bar{LE}$ minimum pulse width HIGH	13 13	25 25		31 31		38 38	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)

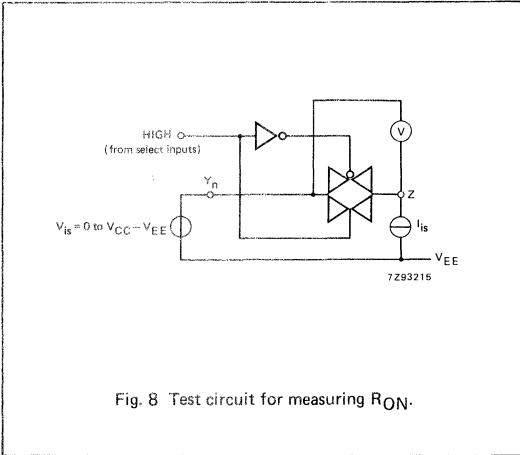


Fig. 8 Test circuit for measuring  $R_{ON}$ .

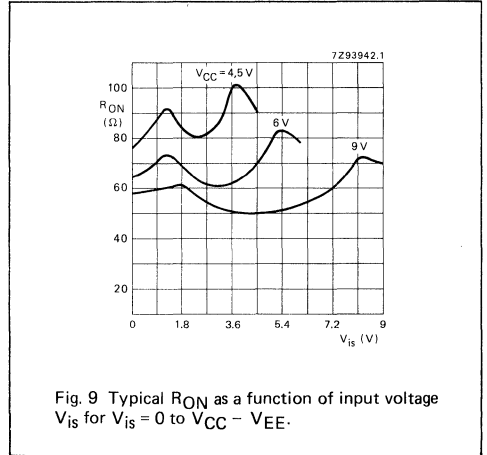


Fig. 9 Typical  $R_{ON}$  as a function of input voltage  $V_{is}$  for  $V_{is} = 0$  to  $V_{CC} - V_{EE}$ .

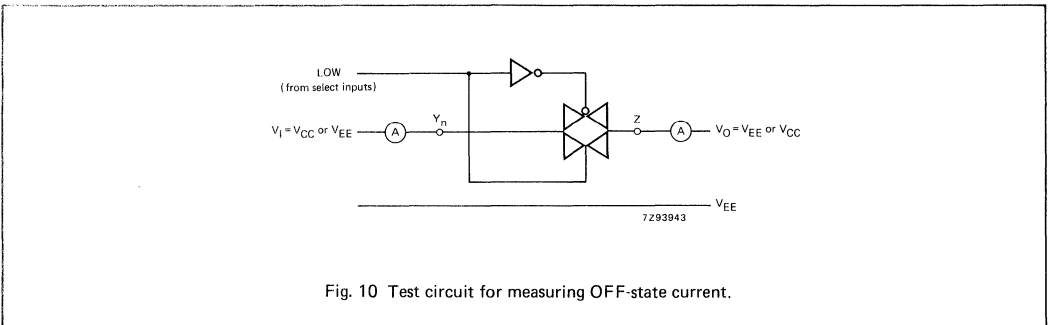


Fig. 10 Test circuit for measuring OFF-state current.

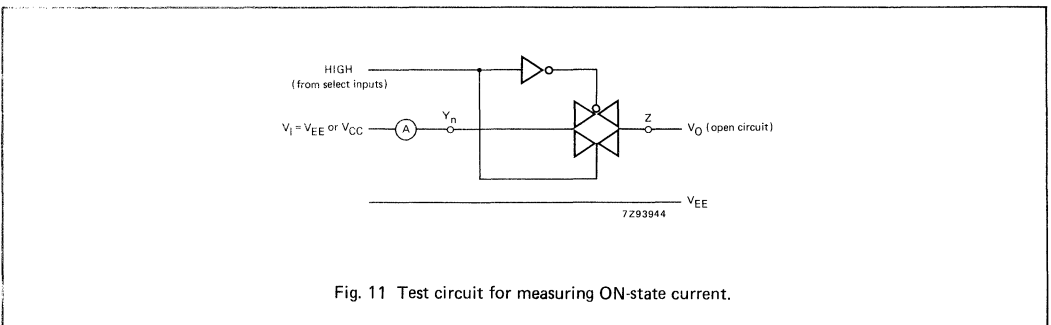


Fig. 11 Test circuit for measuring ON-state current.

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T<sub>amb</sub> = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>is(p-p)</sub> V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	%	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	%	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF (see Figs 12 and 15)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	120 220	mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E <sub>1</sub> , E <sub>2</sub> or S <sub>n</sub> , square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig. 16)
f <sub>max</sub>	minimum frequency response (-3dB)	160 170	MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance independent common	5 25	pF				

Notes to AC characteristics

General note

V<sub>is</sub> is the input voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an input.  
V<sub>os</sub> is the output voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V<sub>is</sub> to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V<sub>is</sub> to 0 dBm level at V<sub>os</sub> for 10 kHz (0 dBm = 1 mW into 50 Ω).

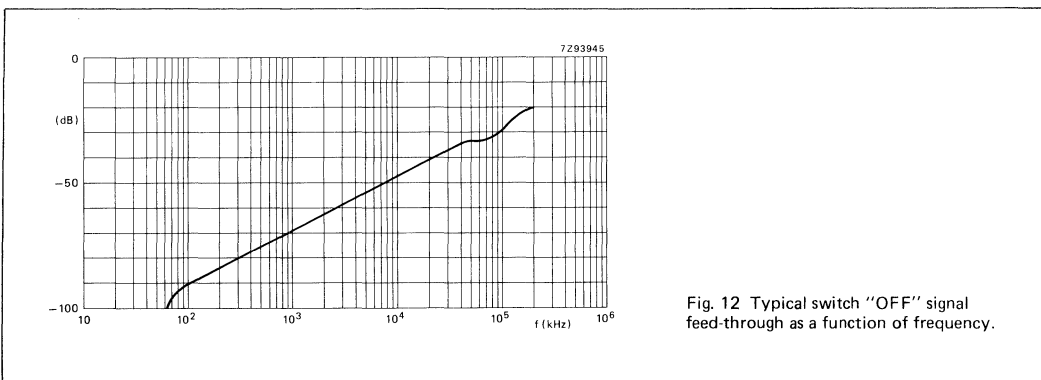
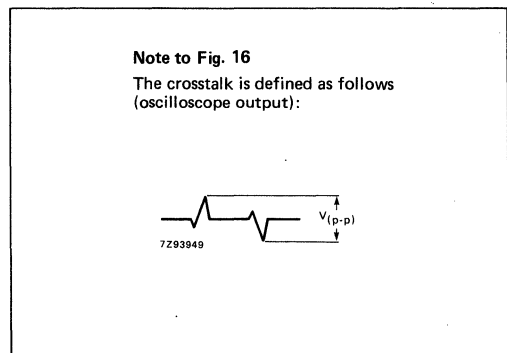
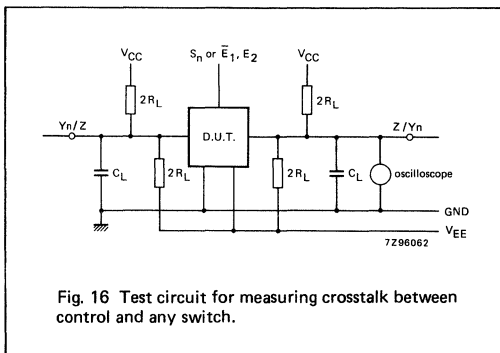
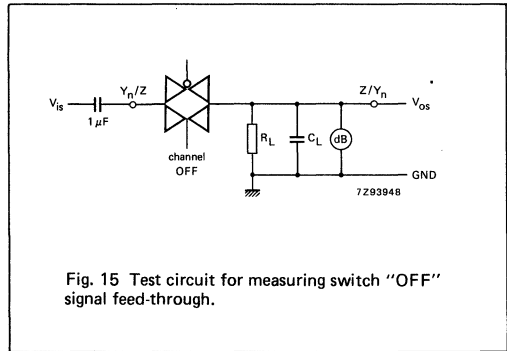
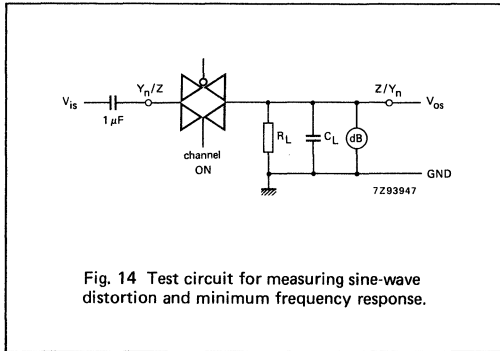
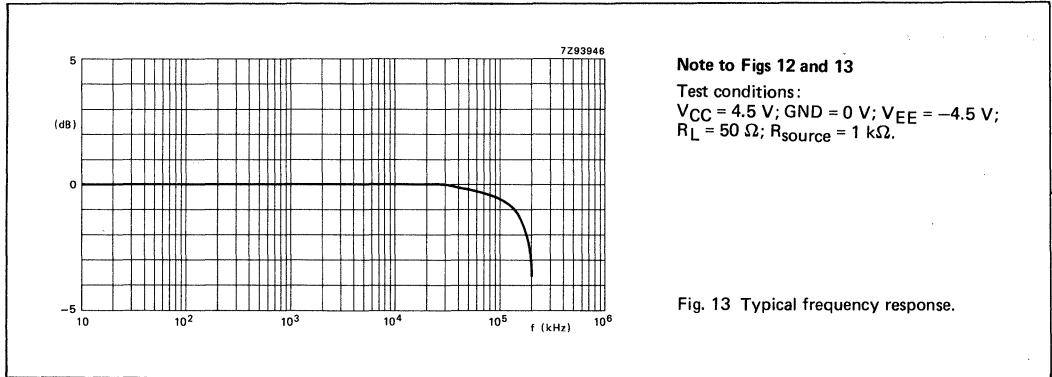


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



AC WAVEFORMS

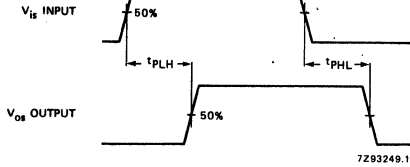


Fig. 17 Waveforms showing the input ( $V_{15}$ ) to output ( $V_{O5}$ ) propagation delays.

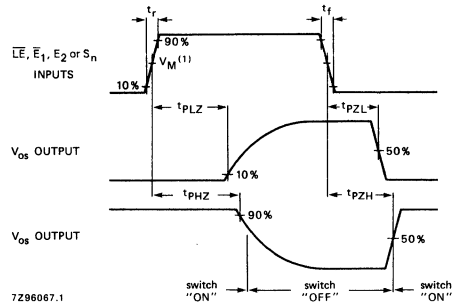


Fig. 18 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 18

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

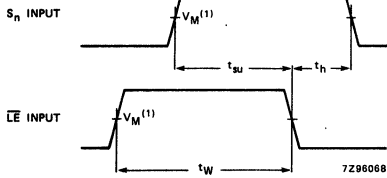


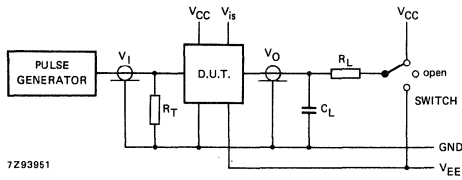
Fig. 19 Waveforms showing the set-up and hold times from  $S_n$  inputs to LE input, and minimum pulse width of LE.

Note to Fig. 19

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

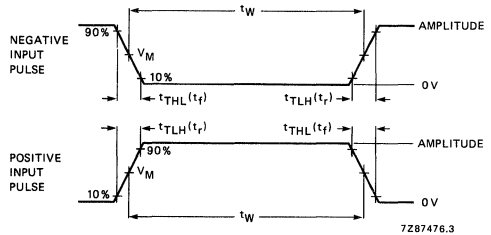


TEST CIRCUIT AND WAVEFORMS



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Fig. 20 Test circuit for measuring AC performance.



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Fig. 21 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>pZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>pZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>pHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>pLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	V <sub>ee</sub> pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 20 and 21:

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.

t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4352

MSI

## DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

### FEATURES

- **Wide analog input voltage range:**  $\pm 5\text{ V}$
- **Low "ON" resistance:**  
 $80\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$   
 $70\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$   
 $60\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- **Logic level translation:**  
to enable 5 V logic to communicate with  $\pm 5\text{ V}$  analog signals
- **Typical "break before make" built in**
- **Address latches provided**
- **Output capability: non-standard**
- **ICC category: MSI**

### GENERAL DESCRIPTION

The 74HC/HCT4352 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs ( $nY_0$  to  $nY_3$ ) and a common input/output ( $nZ$ ).

The common channel select logics include two select inputs ( $S_0$  and  $S_1$ ), an active LOW enable input ( $\bar{E}_1$ ), an active HIGH enable input ( $E_2$ ) and a latch enable input ( $\bar{LE}$ ).

With  $\bar{E}_1$  LOW and  $E_2$  HIGH, one of the four switches is selected (low impedance ON-state) by  $S_0$  and  $S_1$ . The data at the select inputs may be latched by using the active LOW latch enable input ( $\bar{LE}$ ).

When  $\bar{LE}$  is HIGH, the latch is transparent. When either of the two enable inputs,  $\bar{E}_1$  (active LOW) and  $E_2$  (active HIGH), is inactive, all analog switches are turned off.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}_1, E_2$ or $S_n$ to $V_{OS}$	$C_L = 15\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	35	40	ns
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}_1, E_2$ or $S_n$ to $V_{OS}$		21	25	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	—	—	pF
$C_S$	max. switch capacitance independent common		5 12	5 12	pF pF

$V_{EE} = \text{GND} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs

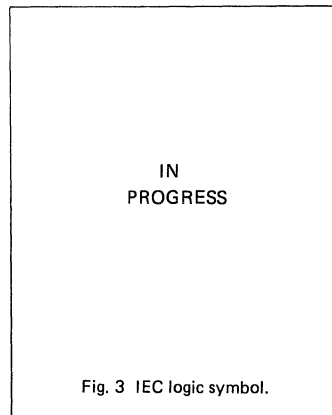
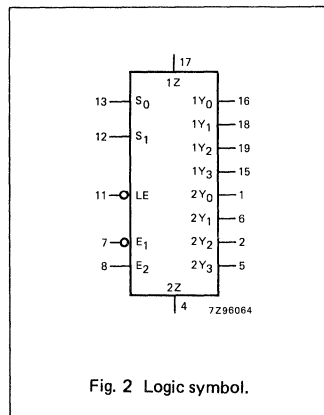
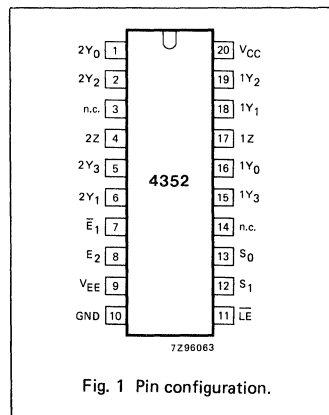
$C_L$  = output load capacitance in pF  
 $C_S$  = max. switch capacitance in pF  
 $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_1 = \text{GND}$  to  $V_{CC}$   
For HCT the condition is  $V_1 = \text{GND}$  to  $V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4352P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT4352T: 20-lead mini-pack; plastic (SO-20; SOT-163A).



## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 6, 2, 5 3, 14	2Y <sub>0</sub> to 2Y <sub>3</sub> n.c.	independent inputs/outputs not connected
7	$\bar{E}_1$	enable input (active LOW)
8	E <sub>2</sub>	enable input (active HIGH)
9	V <sub>EE</sub>	negative supply voltage
10	GND	ground (0 V)
11	$\bar{L}\bar{E}$	latch enable input (active LOW)
13, 12	S <sub>0</sub> , S <sub>1</sub>	select inputs
16, 18, 19, 15	1Y <sub>0</sub> to 1Y <sub>3</sub>	independent inputs/outputs
17, 4	1Z, 2Z	common inputs/outputs
20	V <sub>CC</sub>	positive supply voltage

## GENERAL DESCRIPTION (Cont'd.)

V<sub>CC</sub> and GND are the supply voltage pins for the digital control inputs (S<sub>0</sub>, S<sub>1</sub>,  $\bar{L}\bar{E}$ ,  $\bar{E}_1$  and E<sub>2</sub>). The V<sub>CC</sub> to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY<sub>0</sub> to nY<sub>3</sub>, and nZ) can swing between V<sub>CC</sub> as a positive limit and V<sub>EE</sub> as a negative limit. V<sub>CC</sub> - V<sub>EE</sub> may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V<sub>EE</sub> is connected to GND (typically ground).

## FUNCTION TABLE

INPUTS					CHANNEL ON
$\bar{E}_1$	E <sub>2</sub>	$\bar{L}\bar{E}$	S <sub>1</sub>	S <sub>0</sub>	
H	X	X	X	X	none
X	L	X	X	X	none
L	H	H	L	L	nY <sub>0</sub> - nZ
L	H	H	L	H	nY <sub>1</sub> - nZ
L	H	H	H	L	nY <sub>2</sub> - nZ
L	H	H	H	H	nY <sub>3</sub> - nZ
L	H	L	X	X	*
X	X	↓	X	X	**

H = HIGH voltage level

L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW  $\bar{L}\bar{E}$  transition

\* Last selected channel "ON".

\*\* Selected channels latched.

## APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

DEVELOPMENT DATA

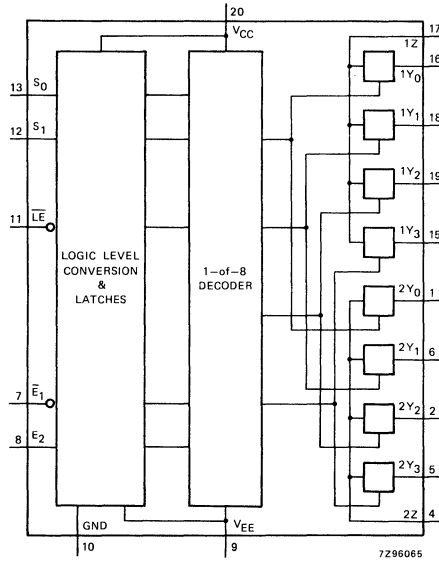


Fig. 4 Functional diagram.

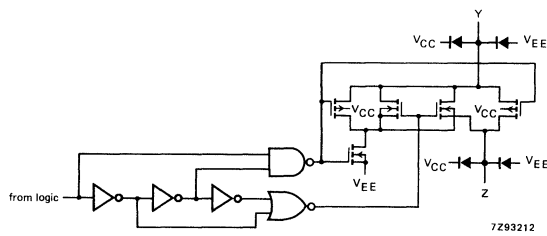


Fig. 5 Schematic diagram (one switch).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

## Note to ratings

To avoid drawing  $V_{CC}$  current out of terminals nZ, when switch current flows in terminals nY<sub>n</sub>, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no  $V_{CC}$  current will flow out of terminals nY<sub>n</sub>. In this case there is no limit for the voltage drop across the switch, but the voltages at nY<sub>n</sub> and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

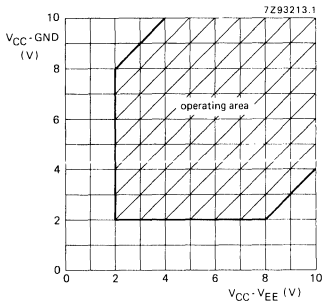


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4352.

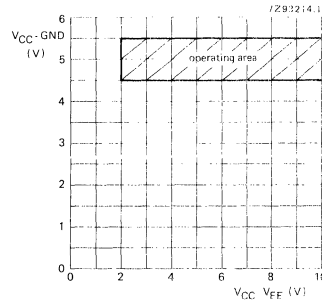


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4352.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V  
 For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

DEVELOPMENT DATA

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_S$ $\mu A$	$V_{is}$	$V_I$
		+25		-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.		max.				
$R_{ON}$	ON resistance (peak)	—	—	—	—	—	—	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		100	180	—	225	—	270	$\Omega$	4.5	0	1000		
		90	160	—	200	—	240	$\Omega$	6.0	0	1000		
$R_{ON}$	ON resistance	70	130	—	165	—	195	$\Omega$	4.5	-4.5	1000	$V_{EE}$	$V_{IH}$ or $V_{IL}$
		150	—	—	—	—	—	$\Omega$	2.0	0	100		
		80	140	—	175	—	210	$\Omega$	4.5	0	1000		
$R_{ON}$	ON resistance	70	120	—	150	—	180	$\Omega$	6.0	0	1000	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		60	105	—	130	—	160	$\Omega$	4.5	-4.5	1000		
		150	—	—	—	—	—	$\Omega$	2.0	0	100		
$R_{ON}$	ON resistance	90	160	—	200	—	240	$\Omega$	4.5	0	1000	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		80	140	—	175	—	210	$\Omega$	6.0	0	1000		
		65	120	—	150	—	180	$\Omega$	4.5	-4.5	1000		
$\Delta R_{ON}$	maximum $\Delta R_{ON}$ resistance between any two channels	—	—	—	—	—	—	$\Omega$	2.0	0	—	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		9	—	—	—	—	—	$\Omega$	4.5	0	—		
		8	—	—	—	—	—	$\Omega$	6.0	0	—		
		6	—	—	—	—	—	$\Omega$	4.5	-4.5	—		

Notes to DC characteristics

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.				
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3	V	2.0 4.5 6.0 9.0				
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>			60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF (see Fig. 18)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time E <sub>1</sub> ; E <sub>2</sub> to V <sub>os</sub> LE to V <sub>os</sub>			350 70 60 60		440 88 75 75		525 105 89 90	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 19)
t <sub>PZH</sub> / t <sub>PZL</sub>	turn "ON" time S <sub>n</sub> to V <sub>os</sub>			375 75 64 55		470 94 80 69		565 113 96 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 19)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time E <sub>1</sub> ; E <sub>2</sub> to V <sub>os</sub> LE to V <sub>os</sub>			275 55 47 50		345 69 59 63		415 83 71 75	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 19)
t <sub>PHZ</sub> / t <sub>PLZ</sub>	turn "OFF" time S <sub>n</sub> to V <sub>os</sub>			300 60 51 50		375 75 64 63		450 90 77 75	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 19)
t <sub>su</sub>	set-up time S <sub>n</sub> to LE			80 16 14 22		100 20 17 28		120 24 20 33	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 20)
t <sub>h</sub>	hold time S <sub>n</sub> to LE			5 5 5 5		5 5 5 5		5 5 5 5	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 20)
t <sub>w</sub>	LE minimum pulse width HIGH			100 20 17 25		125 25 21 31		150 30 26 38	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig. 20)

DEVELOPMENT DATA



## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS			
		74HCT									V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5				
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5				
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND		
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)	
±I <sub>S</sub>	analog switch OFF-state current all channels			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)	
±I <sub>S</sub>	analog switch ON-state current			0.2		2.0		2.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)	
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>	
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1V	other inputs at V <sub>CC</sub> or GND	

## Note to HCT types

1. The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

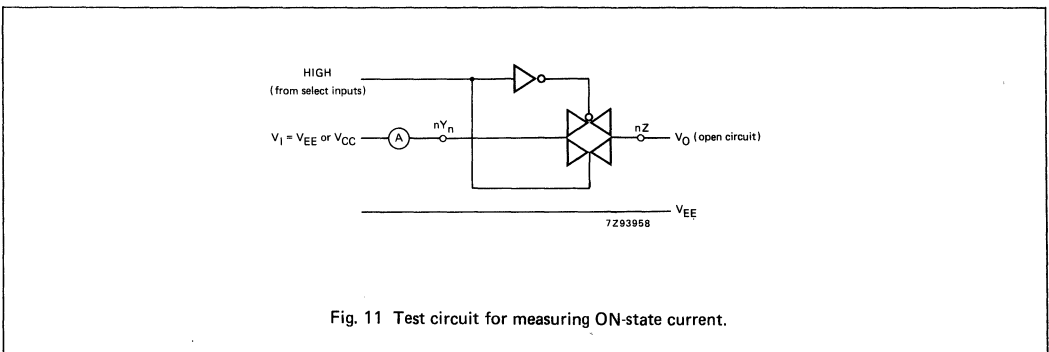
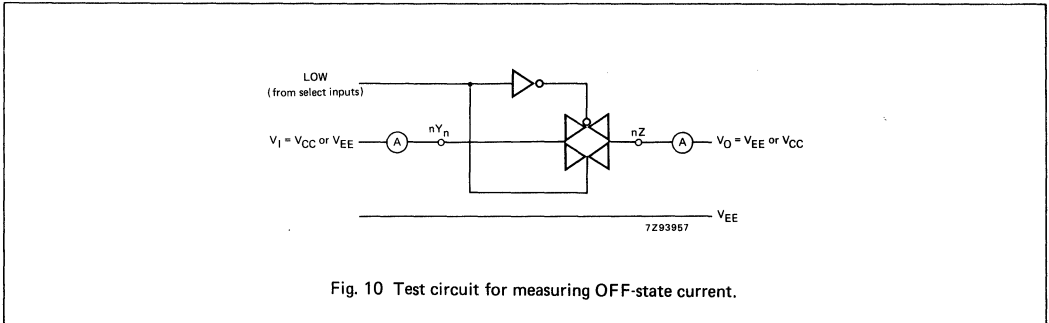
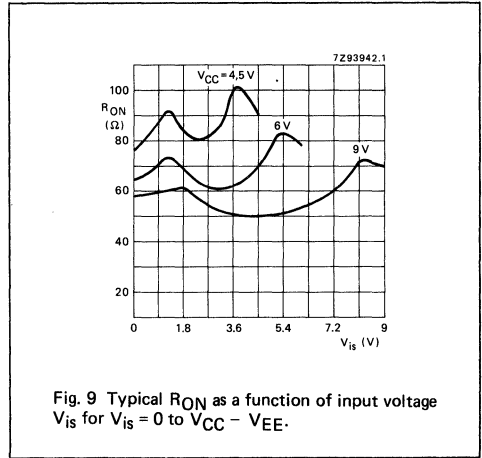
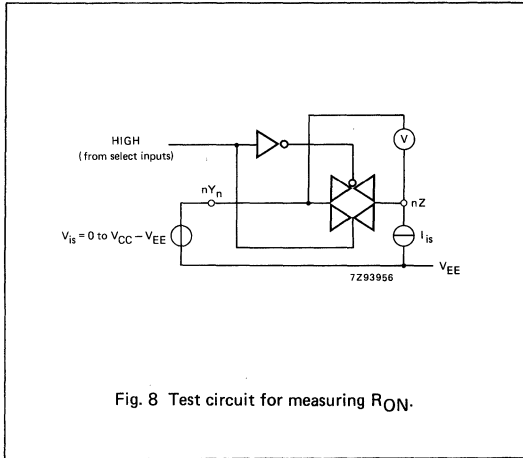
INPUT	UNIT LOAD COEFFICIENT
E <sub>1</sub> , E <sub>2</sub>	0.50
S <sub>n</sub>	0.50
LE	1.5

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$			12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\overline{E}_1$ ; $E_2$ to $V_{os}$ $\overline{LE}$ to $V_{os}$			80 65		100 81		120 98	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $S_n$ to $V_{os}$			80 65		100 81		120 98	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\overline{E}_1$ ; $E_2$ to $V_{os}$ $\overline{LE}$ to $V_{os}$			60 50		75 63		90 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $S_n$ to $V_{os}$			60 50		75 63		90 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{su}$	set-up time $S_n$ to $\overline{LE}$			16 22		20 28		24 33	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_h$	hold time $S_n$ to $\overline{LE}$			5 5		5 5		5 5	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_w$	$\overline{LE}$ minimum pulse width HIGH			20 25		25 31		30 38	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)

DEVELOPMENT DATA



## ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

## Recommended conditions and typical values

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

SYMBOL	PARAMETER	typ.	UNIT	$V_{CC}$ V	$V_{EE}$ V	$V_{is(p-p)}$ V	CONDITIONS
	sine-wave distortion $f = 1\text{ kHz}$	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$ ; $C_L = 50\text{ pF}$ (see Fig. 14)
	sine-wave distortion $f = 10\text{ kHz}$	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10\text{ k}\Omega$ ; $C_L = 50\text{ pF}$ (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ $f = 1\text{ MHz}$ (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600\text{ }\Omega$ ; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ( $E_1$ , $E_2$ or $S_n$ ; square-wave between $V_{CC}$ and GND, $t_r = t_f = 6\text{ ns}$ ) (see Fig. 17)
$f_{max}$	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50\text{ }\Omega$ ; $C_L = 10\text{ pF}$ (see Figs 13 and 14)
$C_S$	maximum switch capacitance independent common	5 12	pF pF				

DEVELOPMENT DATA

## Notes to AC characteristics

## General note

$V_{is}$  is the input voltage at an  $nY_n$  or  $nZ$  terminal, whichever is assigned as an input.  
 $V_{os}$  is the output voltage at an  $nY_n$  or  $nZ$  terminal, whichever is assigned as an output.

## Notes

1. Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).
2. Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for 10 kHz (0 dBm = 1 mW into 50  $\Omega$ ).

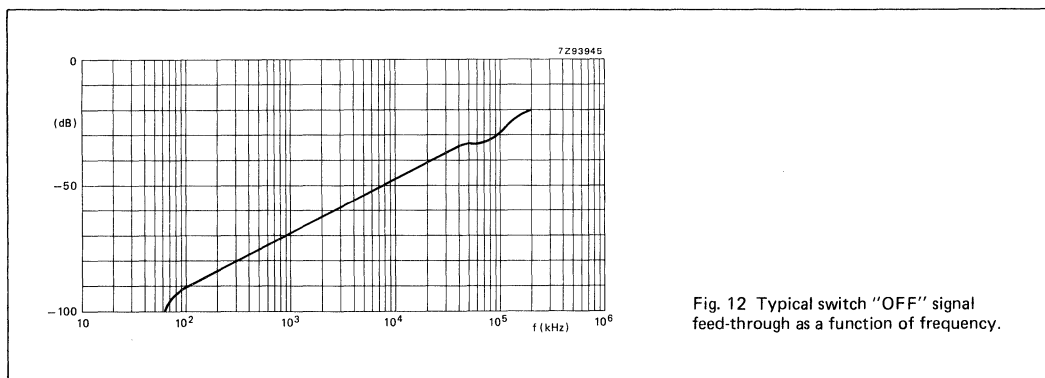
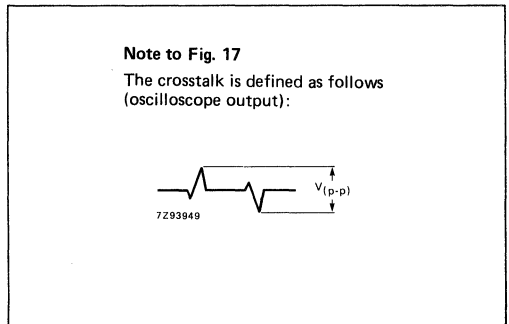
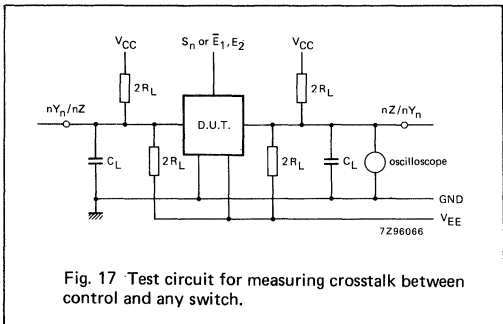
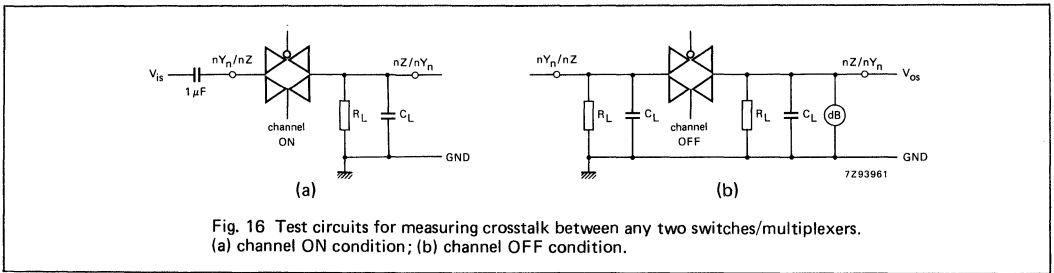
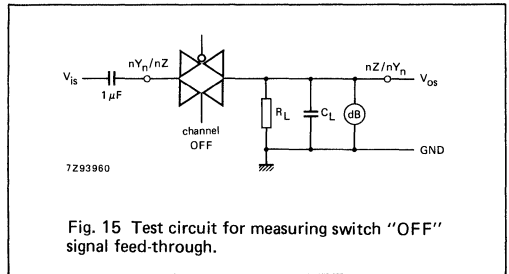
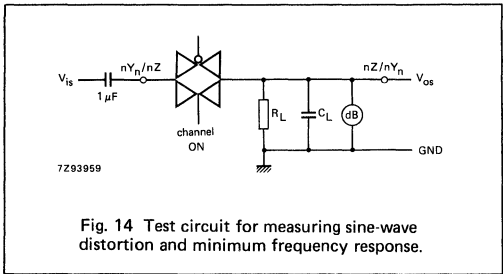
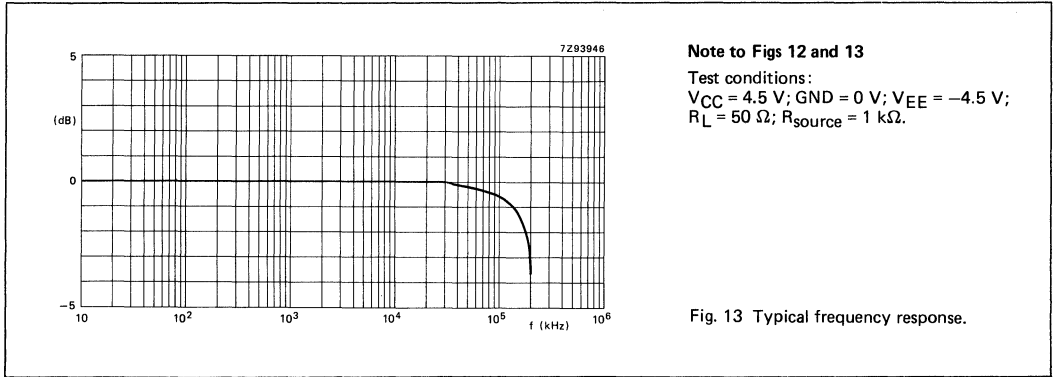


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



AC WAVEFORMS

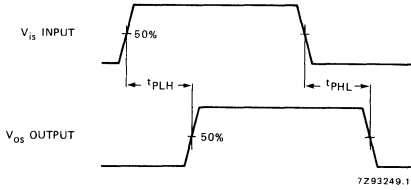


Fig. 18 Waveforms showing the input ( $V_{is}$ ) to output ( $V_{os}$ ) propagation delays.

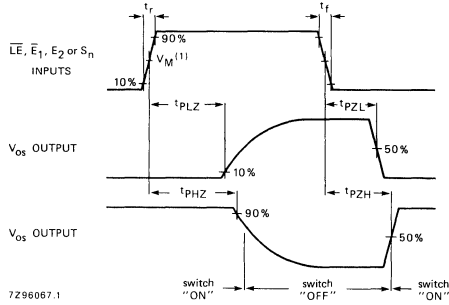


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DEVELOPMENT DATA

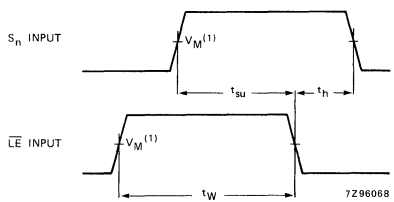


Fig. 20 Waveforms showing the set-up and hold times from  $S_n$  inputs to  $\overline{LE}$  input, and minimum pulse width of  $\overline{LE}$ .

Note to Fig. 20

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS

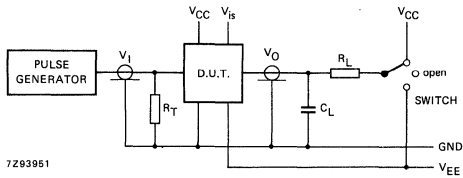


Fig. 21 Test circuit for measuring AC performance.

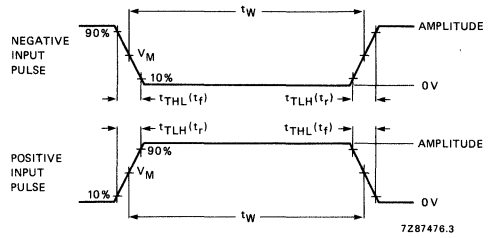


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>iss</sub>
tpZH	VEE	VCC
tpZL	VCC	VEE
tPHZ	VEE	VCC
tPLZ	VCC	VEE
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	VCC	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.

t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4353

MSI

## TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH LATCH

### FEATURES

- Wide analog input voltage range:  $\pm 5\text{ V}$
- Low "ON" resistance:
  - $80\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$
  - $70\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$
  - $60\ \Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation: to enable  $5\text{ V}$  logic to communicate with  $\pm 5\text{ V}$  analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4353 are high-speed Si-gate CMOS devices.

They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4353 are triple 2-channel analog multiplexers/demultiplexers with two common enable inputs ( $\bar{E}_1$  and  $E_2$ ) and a latch enable input (LE). Each multiplexer has two independent inputs/outputs ( $nY_0$  and  $nY_1$ ), a common input/output ( $nZ$ ) and select inputs ( $S_0$  to  $S_2$ ).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}_1, E_2$ or $S_n$ to $V_{Os}$	$C_L = 50\text{ pF}$ $R_L = 1\text{ k}\Omega$ $V_{CC} = 5\text{ V}$	21	23	ns
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}_1, E_2$ or $S_n$ to $V_{Os}$		19	21	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	—	—	pF
$C_S$	max. switch capacitance independent common		5 8	5 8	pF pF

$V_{EE} = \text{GND} = 0\text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\Sigma \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$  = sum of outputs

$C_L$  = output load capacitance in pF

$C_S$  = max. switch capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND}$  to  $V_{CC}$   
For HCT the condition is  $V_I = \text{GND}$  to  $V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4353P: 20-lead DIL; plastic (SOT-146).

PC74HC/HCT4353T: 20-lead mini-pack; plastic (SO-20; SOT-163A).

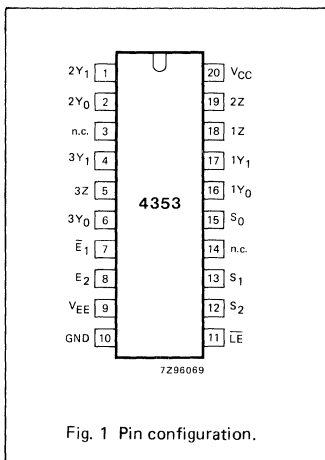


Fig. 1 Pin configuration.

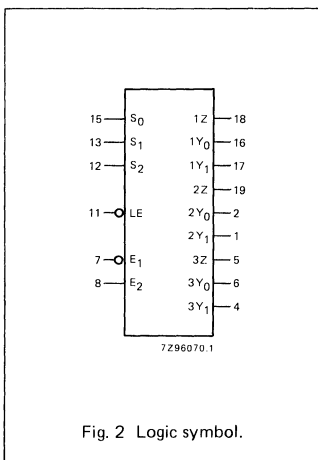


Fig. 2 Logic symbol.

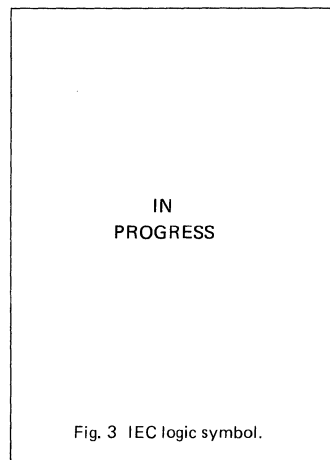


Fig. 3 IEC logic symbol.



## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	2Y <sub>0</sub> , 2Y <sub>1</sub>	independent inputs/outputs
5	3Z	common input/output
6, 4	3Y <sub>0</sub> , 3Y <sub>1</sub>	independent inputs/outputs
3, 14	n.c.	not connected
7	$\bar{E}_1$	enable input (active LOW)
8	E <sub>2</sub>	enable input (active HIGH)
9	V <sub>EE</sub>	negative supply voltage
10	GND	ground (0 V)
11	$\bar{L}\bar{E}$	latch enable input (active LOW)
15, 13, 12	S <sub>0</sub> to S <sub>2</sub>	select inputs
16, 17	1Y <sub>0</sub> , 1Y <sub>1</sub>	independent inputs/outputs
18	1Z	common input/output
19	2Z	common input/output
20	V <sub>CC</sub>	positive supply voltage

## FUNCTION TABLE

INPUTS				CHANNEL ON
$\bar{E}_1$	E <sub>2</sub>	$\bar{L}\bar{E}$	S <sub>n</sub>	
H	X	X	X	none
X	L	X	X	none
L	H	H	L	nY <sub>0</sub> - nZ
L	H	H	H	nY <sub>1</sub> - nZ
L	H	L	X	*
X	X	↓	X	**

H = HIGH voltage level

L = LOW voltage level

X = don't care

↓ = HIGH-to-LOW  $\bar{L}\bar{E}$  transition

\* Last selected channel "ON".

\*\* Selected channels latched.

## APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

## GENERAL DESCRIPTION (Cont'd.)

Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY<sub>0</sub> and nY<sub>1</sub>) and the other side connected to a common input/output (nZ).

With  $\bar{E}_1$  LOW and E<sub>2</sub> HIGH, one of the two switches is selected (low impedance ON-state) by S<sub>0</sub> to S<sub>2</sub>.

The data at the select inputs may be latched by using the active LOW latch enable input ( $\bar{L}\bar{E}$ ). When  $\bar{L}\bar{E}$  is HIGH, the latch is transparent. When either of the two enable inputs,  $\bar{E}_1$  (active LOW) and E<sub>2</sub> (active HIGH), is inactive, all analog switches are turned off.

V<sub>CC</sub> and GND are the supply voltage pins for the digital control inputs (S<sub>0</sub> to S<sub>2</sub>,  $\bar{L}\bar{E}$ ,  $\bar{E}_1$  and E<sub>2</sub>). The V<sub>CC</sub> to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY<sub>0</sub> and nY<sub>1</sub>, and nZ) can swing between V<sub>CC</sub> as a positive limit and V<sub>EE</sub> as a negative limit. V<sub>CC</sub> - V<sub>EE</sub> may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V<sub>EE</sub> is connected to GND (typically ground).

DEVELOPMENT DATA

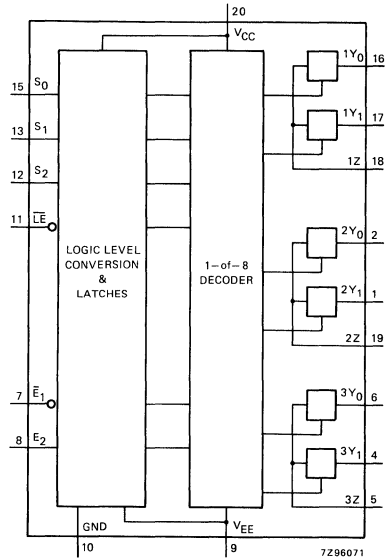


Fig. 4 Functional diagram.

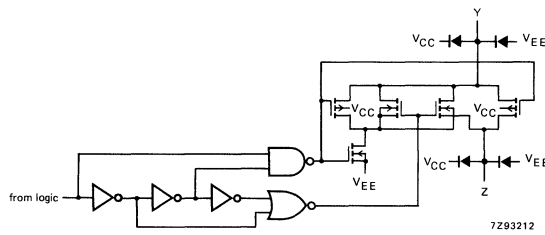


Fig. 5 Schematic diagram (one switch).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	$^{\circ}\text{C}$	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 $^{\circ}\text{C}$ 74HC/HCT
	plastic DIL		500	mW	above +70 $^{\circ}\text{C}$ : derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 $^{\circ}\text{C}$ : derate linearly with 6 mW/K
$P_S$	power dissipation per switch		100	mW	

## Note to ratings

To avoid drawing  $V_{CC}$  current out of terminals nZ, when switch current flows in terminals nY<sub>n</sub>, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no  $V_{CC}$  current will flow out of terminals nY<sub>n</sub>. In this case there is no limit for the voltage drop across the switch, but the voltages at nY<sub>n</sub> and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	$^{\circ}\text{C}$	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	$^{\circ}\text{C}$	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

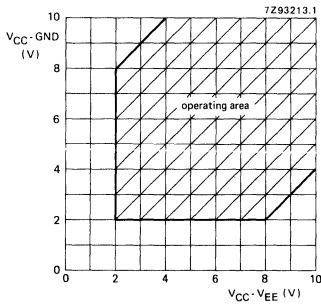


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4353.

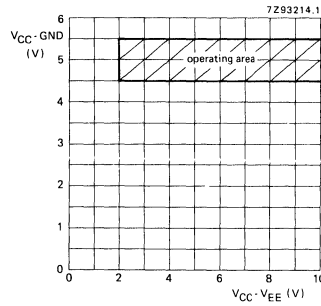


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4353.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V  
 For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

DEVELOPMENT DATA

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HC/HCT							$V_{CC}$ V	$V_{EE}$ V	$I_s$ $\mu A$	$V_{is}$	$V_i$
		+25		-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.		max.				
$R_{ON}$	ON resistance (peak)	-	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		100	180	225	270	240	195	$\Omega$	4.5	0	1000		
		90	160	200	240	180	160	$\Omega$	6.0	0	1000		
		70	130	165	195	160	160	$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance	150	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{EE}$	$V_{IH}$ or $V_{IL}$
		80	140	175	210	180	160	$\Omega$	4.5	0	1000		
		70	120	150	180	160	160	$\Omega$	6.0	0	1000		
		60	105	130	160	160	160	$\Omega$	4.5	-4.5	1000		
$R_{ON}$	ON resistance	150	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$
		90	160	200	240	180	160	$\Omega$	4.5	0	1000		
		80	140	175	210	180	160	$\Omega$	6.0	0	1000		
		65	120	150	180	160	160	$\Omega$	4.5	-4.5	1000		
$\Delta R_{ON}$	maximum $\Delta$ ON resistance between any two channels	-	-	-	-	-	-	$\Omega$	2.0	0	-	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$
		9	-	-	-	-	-	$\Omega$	4.5	0	-		
		8	-	-	-	-	-	$\Omega$	6.0	0	-		
		6	-	-	-	-	-	$\Omega$	4.5	-4.5	-		

Notes to DC characteristics

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig. 8.

## DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HC							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0			
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0			
±I <sub>I</sub>	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25		-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.		max.			
$t_{pHL}/$ $t_{pLH}$	propagation delay $V_{is}$ to $V_{os}$			60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{pZH}/$ $t_{pZL}$	turn "ON" time $\bar{E}_1$ ; $E_2$ to $V_{os}$ $\bar{L}E$ to $V_{os}$			300 60 51 55		375 75 64 69		450 90 77 83	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{pZH}/$ $t_{pZL}$	turn "ON" time $S_n$ to $V_{os}$			300 60 58 50		375 75 69 63		450 90 77 75	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{pHZ}/$ $t_{pLZ}$	turn "OFF" time $\bar{E}_1$ ; $E_2$ to $V_{os}$ $\bar{L}E$ to $V_{os}$			275 55 47 45		345 69 59 56		415 83 71 68	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{pHZ}/$ $t_{pLZ}$	turn "OFF" time $S_n$ to $V_{os}$			275 55 47 45		345 69 59 56		415 83 71 68	ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{su}$	set-up time $S_n$ to $\bar{L}E$	60 12 10 18			75 15 13 23		90 18 15 27		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_h$	hold time $S_n$ to $\bar{L}E$	5 5 5 5			5 5 5 5		5 5 5 5		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_w$	$\bar{L}E$ minimum pulse width HIGH	100 20 17 25			125 25 21 31		150 30 26 38		ns	2.0 4.5 6.0 4.5	0 0 0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)

DEVELOPMENT DATA

## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 10)
±I <sub>S</sub>	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>   = V <sub>CC</sub> - V <sub>EE</sub> (see Fig. 11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND

## Note to HCT types

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.  
To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E <sub>1</sub> , E <sub>2</sub>	0.50
S <sub>n</sub>	0.50
LE	1.5

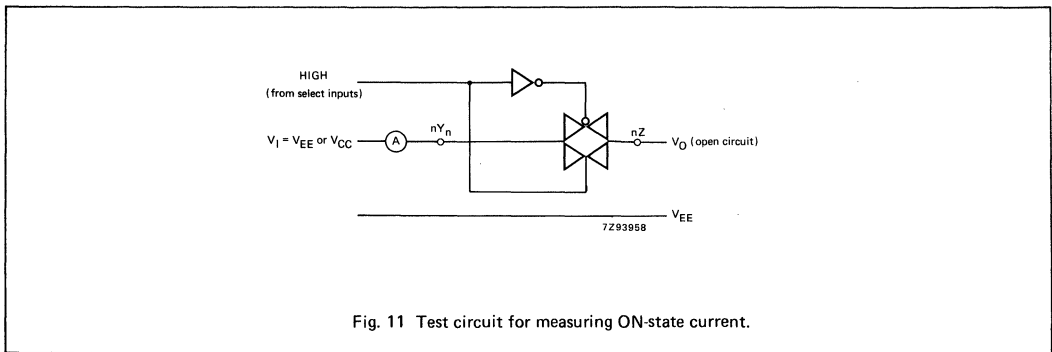
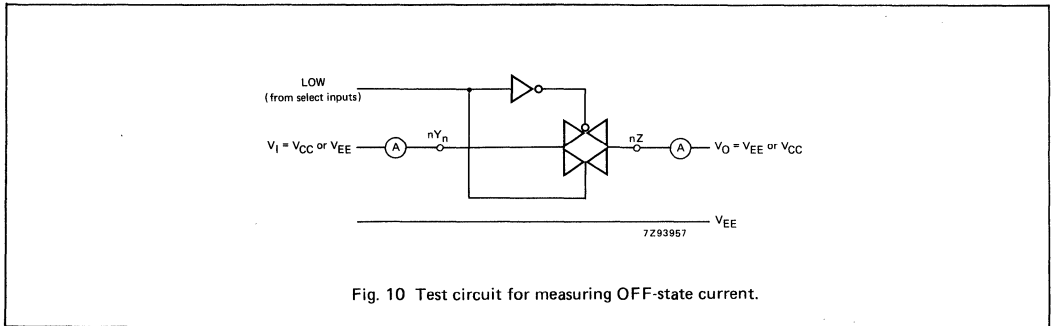
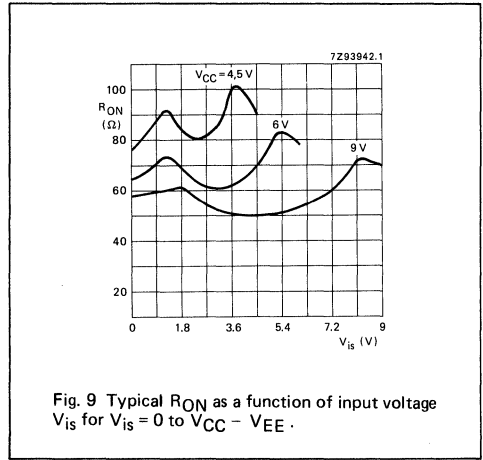
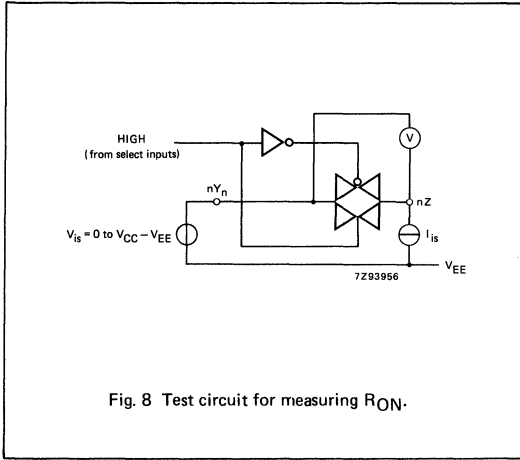
## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ V	$V_{EE}$ V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
$t_{PHL}/$ $t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$			12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig. 18)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $\bar{E}_1$ ; $E_2$ to $V_{os}$ $\bar{LE}$ to $V_{os}$			75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PZH}/$ $t_{PZL}$	turn "ON" time $S_n$ to $V_{os}$			75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $\bar{E}_1$ ; $E_2$ to $V_{os}$ $\bar{LE}$ to $V_{os}$			60 55		75 69		90 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{PHZ}/$ $t_{PLZ}$	turn "OFF" time $S_n$ to $V_{os}$			65 55		81 69		98 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 19)
$t_{su}$	set-up time $S_n$ to $\bar{LE}$	12 14			15 18			18 21	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_h$	hold time $S_n$ to $\bar{LE}$	5 5			5 5			5 5	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)
$t_w$	$\bar{LE}$ minimum pulse width HIGH	25 25			31 31			38 38	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig. 20)

DEVELOPMENT DATA





**ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT**

Recommended conditions and typical values

GND = 0 V; T<sub>amb</sub> = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V <sub>CC</sub> V	V <sub>EE</sub> V	V <sub>is(p-p)</sub> V	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF f = 1 MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (see Fig. 16)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E <sub>1</sub> , E <sub>2</sub> or S <sub>n</sub> , square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig. 17)
f <sub>max</sub>	minimum frequency response (-3dB)	170 180	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance independent common	5 8	pF pF				

DEVELOPMENT DATA

**Notes to AC characteristics**

**General note**

V<sub>is</sub> is the input voltage at an nY<sub>n</sub> or nZ terminal, whichever is assigned as an input.  
V<sub>os</sub> is the output voltage at an nY<sub>n</sub> or nZ terminal, whichever is assigned as an output.

**Notes**

1. Adjust input voltage V<sub>is</sub> to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V<sub>is</sub> to 0 dBm level at V<sub>os</sub> for 10 kHz (0 dBm = 1 mW into 50 Ω).

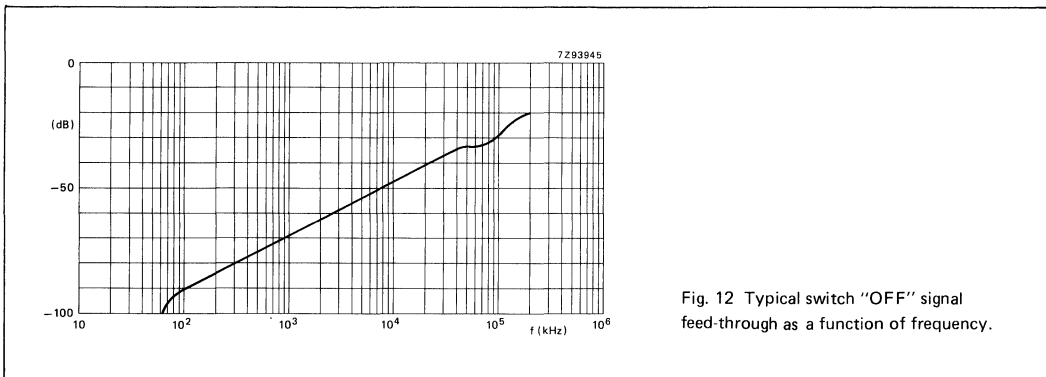
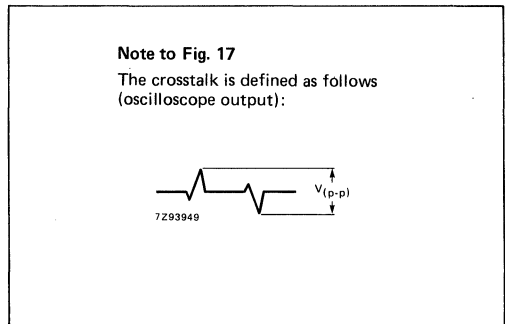
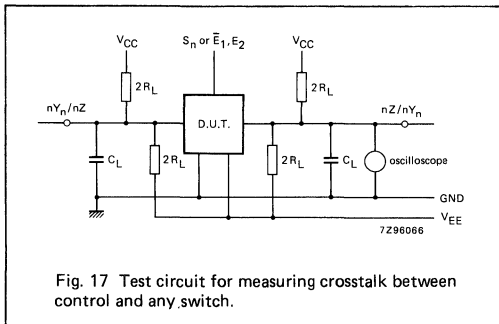
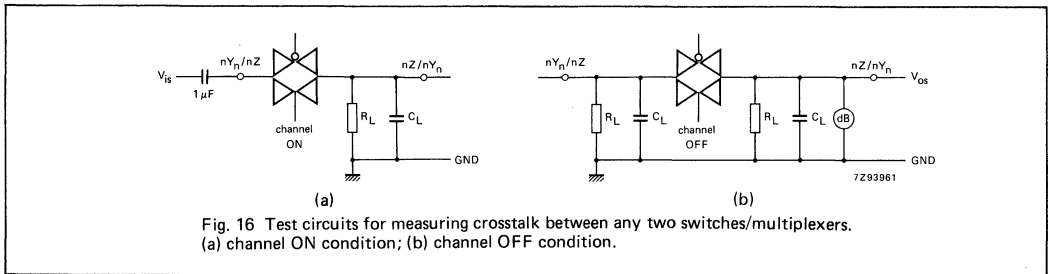
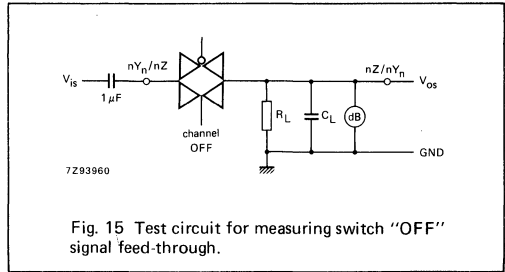
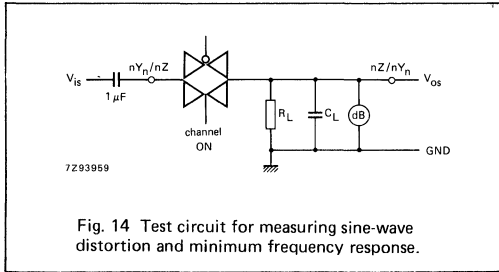
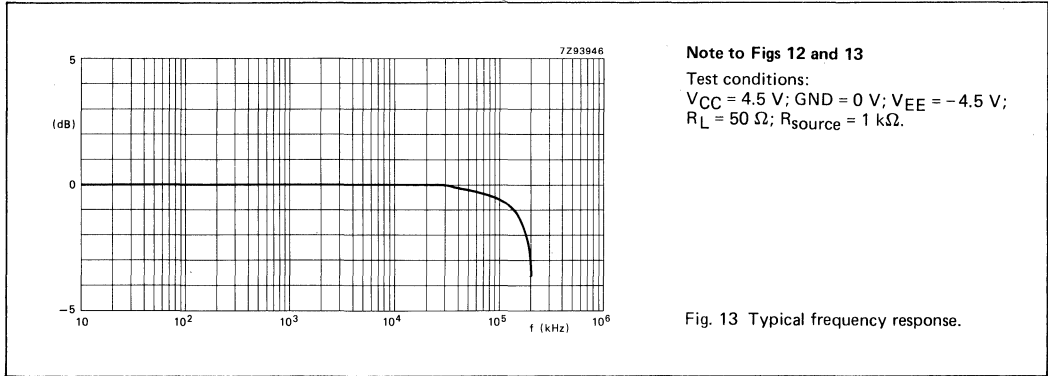


Fig. 12 Typical switch "OFF" signal feed-through as a function of frequency.



AC WAVEFORMS

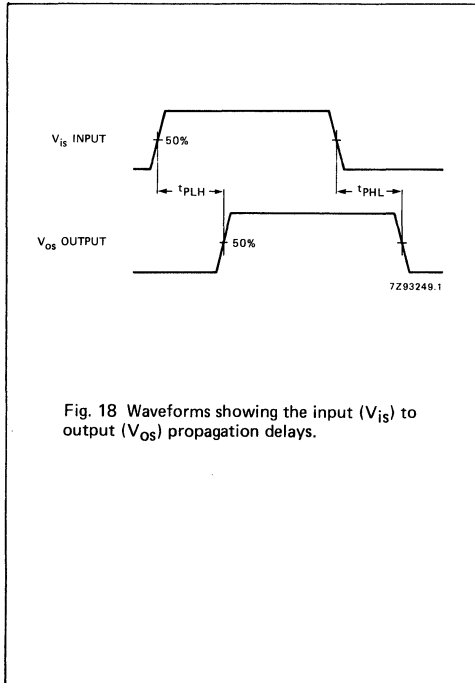


Fig. 18 Waveforms showing the input ( $V_{1S}$ ) to output ( $V_{Os}$ ) propagation delays.

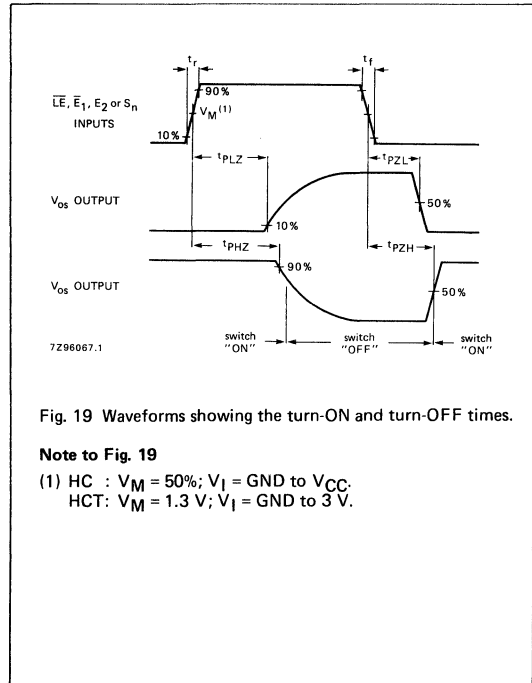


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

DEVELOPMENT DATA

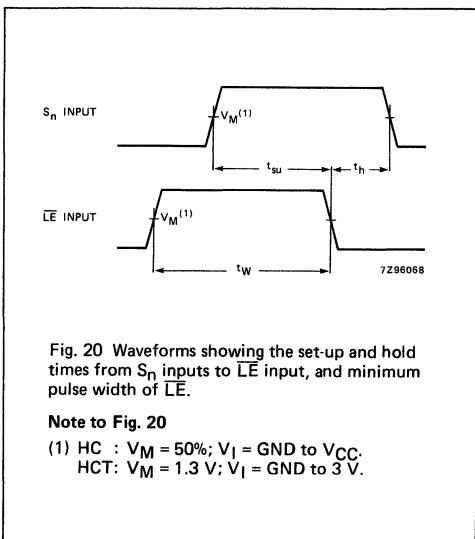


Fig. 20 Waveforms showing the set-up and hold times from  $S_n$  inputs to  $\overline{LE}$  input, and minimum pulse width of  $\overline{LE}$ .

Note to Fig. 20

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

TEST CIRCUIT AND WAVEFORMS

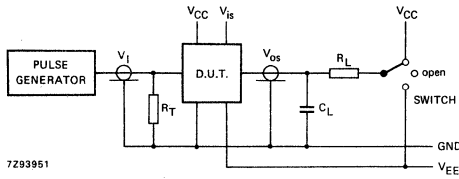


Fig. 21 Test circuit for measuring AC performance.

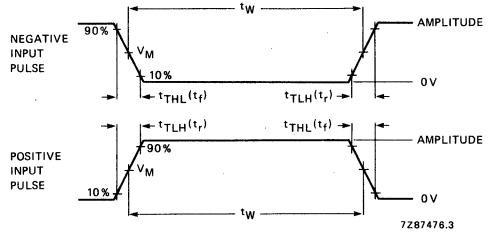


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> , t <sub>f</sub>	
			f <sub>max</sub> , PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

- C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.
- t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4510

MSI

## BCD UP/DOWN COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4510 are high-speed Si-gate CMOS devices and are pin compatible with the "4510" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4510 are edge-triggered synchronous up/down BCD counters with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input (CE), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D<sub>0</sub> to D<sub>3</sub>), four parallel outputs (Q<sub>0</sub> to Q<sub>3</sub>), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on D<sub>0</sub> to D<sub>3</sub> is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW-to-HIGH transition of CP if CE is LOW. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when Q<sub>0</sub> and Q<sub>3</sub> are HIGH and CE is LOW. When counting down, TC is LOW when Q<sub>0</sub> to Q<sub>3</sub> and CE are LOW. A HIGH on MR resets the counter (Q<sub>0</sub> to Q<sub>3</sub> = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$TC = \overline{CE} \cdot \{ (UP/DN) \cdot Q_0 \cdot Q_3 + (UP/DN) \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \}$$

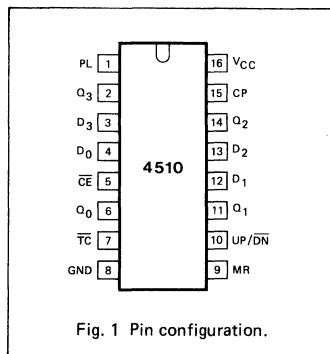


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	19	ns
f <sub>max</sub>	maximum clock frequency		45	45	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4510P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT4510T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D <sub>0</sub> to D <sub>3</sub>	parallel inputs
5	CE	count enable input (active LOW)
6, 11, 14, 2	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
7	TC	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/DN	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage

### FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition



**BCD TO 7-SEGMENT LATCH/DECODER/DRIVER**

**FEATURES**

- Latch storage of BCD inputs
- Blanking input
- Lamp test input
- Driving common cathode LED displays
- Guaranteed 10 mA drive capability per output
- Output capability, non-standard
- **ICC** category: MSI

**GENERAL DESCRIPTION**

The 74HC/HCT4511 are high-speed Si-gate CMOS devices and are pin compatible with "4511" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4511 are BCD to 7-segment latch/decoder/drivers with four address inputs (D<sub>1</sub> to D<sub>4</sub>), an active LOW latch enable input (LE), an active LOW ripple blanking input (BI), an active LOW lamp test input (LT), and seven active HIGH segment outputs (Q<sub>a</sub> to Q<sub>g</sub>).

When LE is LOW, the state of the segment outputs (Q<sub>a</sub> to Q<sub>g</sub>) is determined by the data on D<sub>1</sub> to D<sub>4</sub>.

When LE goes HIGH, the last data present on D<sub>1</sub> to D<sub>4</sub> are stored in the latches and the segment outputs remain stable.

When LT is LOW, all the segment outputs are HIGH independent of all other input conditions. With LT HIGH, a LOW on BI forces all segment outputs LOW. The inputs LT and BI do not affect the latch circuit.

**APPLICATIONS**

- Driving LED displays
- Driving incandescent displays
- Driving fluorescent displays
- Driving LCD displays
- Driving gas discharge displays

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	24	24	ns
	D <sub>n</sub> to Q <sub>n</sub>		23	2A	ns
	LE to Q <sub>n</sub>		19	20	ns
	BI to Q <sub>n</sub>		12	13	ns
C <sub>I</sub>	input capacitance		3.5	0.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	64	64	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

**Notes**

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

**ORDERING INFORMATION/PACKAGE OUTLINES**

PC74HC/HCT4511P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT4511T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
3	LT	lamp test input (active LOW)
4	BI	ripple blanking input (active LOW)
5	LE	latch enable input (active LOW)
7, 1, 2, 6	D <sub>1</sub> to D <sub>4</sub>	BCD address inputs
8	GND	ground (0 V)
13, 12, 11, 10, 9, 15, 14	Q <sub>a</sub> to Q <sub>g</sub>	segments outputs
16	V <sub>CC</sub>	positive supply voltage

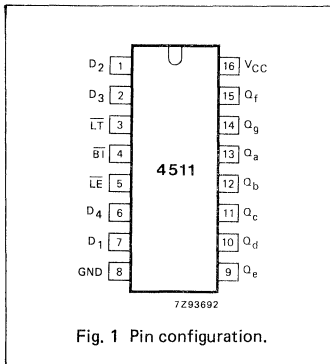


Fig. 1 Pin configuration.

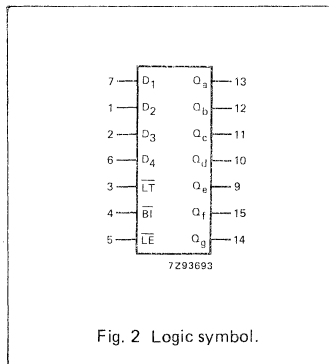


Fig. 2 Logic symbol.

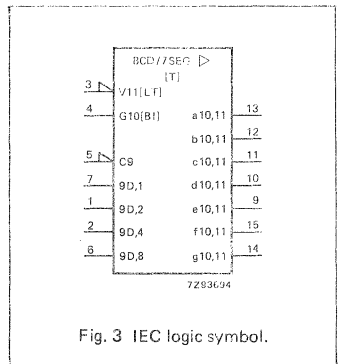


Fig. 3 IEC logic symbol.



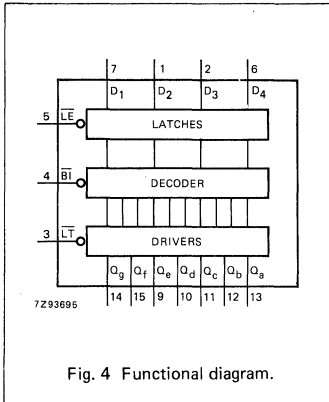


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	Q <sub>a</sub>	Q <sub>b</sub>	Q <sub>c</sub>	Q <sub>d</sub>	Q <sub>e</sub>	Q <sub>f</sub>	Q <sub>g</sub>	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	L	L	0
L	H	H	L	L	L	H	L	H	L	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	L	L	L	H	H	9
L	H	H	H	L	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	*							*

\* Depends upon the BCD-code applied during the LOW-to-HIGH transition of  $\overline{LE}$ .

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

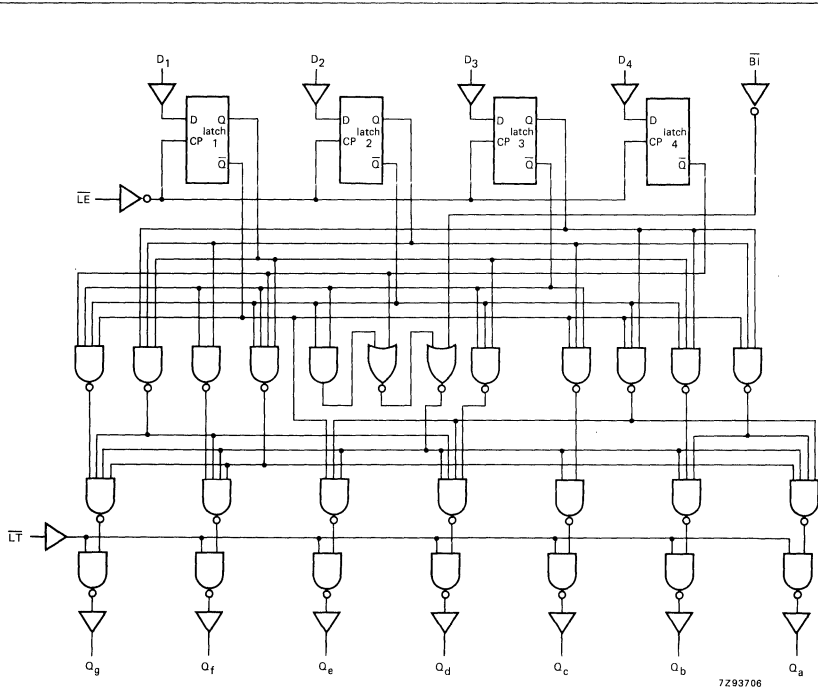


Fig. 5 Logic diagram.

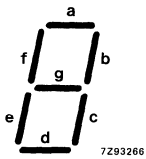


Fig. 6 Segment designation.



Fig. 7 Display.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting  $V_{CH}$  which is given below

$I_{CC}$  category: MSI

## Non-standard DC characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HC							$V_{CC}$ V	$V_I$	$-I_O$ mA	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
$V_{OH}$	HIGH level output voltage	3.98			3.84		3.70	V	4.5	$V_{IH}$ or $V_{IL}$	7.5 10.0	
$V_{OH}$	HIGH level output voltage	5.60			5.45		5.35	V	6.0	$V_{IH}$ or $V_{IL}$	7.5 10.0 15.0	
		3.60			3.35		3.10					
		5.48			5.34		5.20					
		4.80			4.50		4.20					

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay $D_n$ to $Q_n$		77 28 22	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 8
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{LE}$ to $Q_n$		74 27 22	270 54 46		330 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 9
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{BI}$ to $Q_n$		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{LT}$ to $Q_n$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8, 9 and 10
$t_W$	latch enable pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20	ns	2.0 4.5 6.0		Fig. 9
$t_{su}$	set-up time $D_n$ to $\overline{LE}$	60 12 10	14 5 4		75 15 13		90 18 15	ns	2.0 4.5 6.0		Fig. 11
$t_h$	hold time $D_n$ to $\overline{LE}$	0 0 0	-11 -4 -3		0 0 0		0 0 0	ns	2.0 4.5 6.0		Fig. 11

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard, excepting  $V_{OH}$  which is given below

$I_{CC}$  category: MSI

**Non-standard DC characteristics for 74HCT**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS				
		74HCT							$V_{CC}$ V	$V_I$	- $I_O$ mA		
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.					max.	
$V_{OH}$	HIGH level output voltage	3.98 3.60			3.84 3.35			3.70 3.10		V	4.5	$V_{IH}$ or $V_{IL}$	7.5 10.0

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

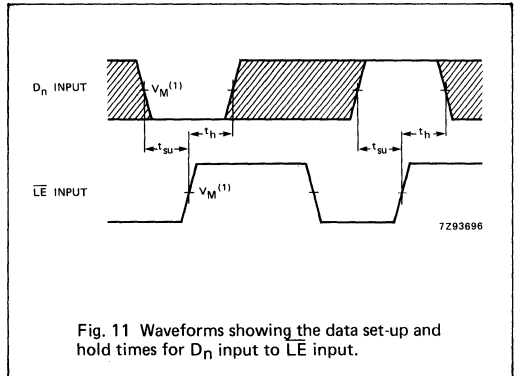
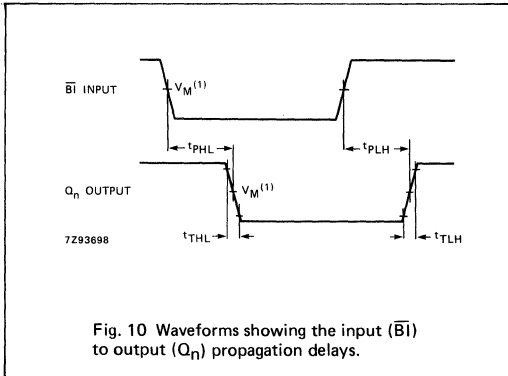
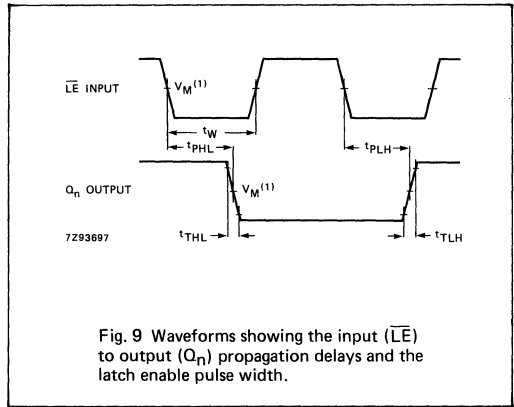
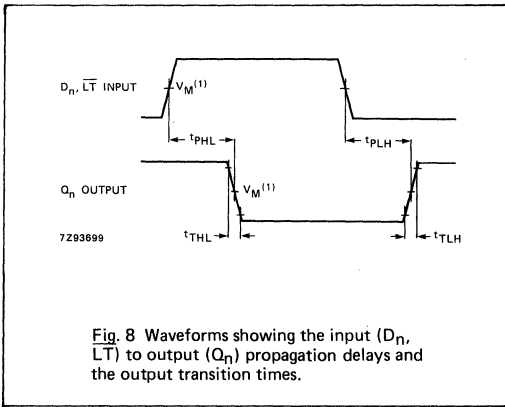
INPUT	UNIT LOAD COEFFICIENT
$\overline{LT}$ , $\overline{LE}$	1.50
$B_I$ , $D_n$	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$		28	60		75		90	ns	4.5	Fig. 8
$t_{PHL}/t_{PLH}$	propagation delay $\overline{LE}$ to $Q_n$		27	54		68		81	ns	4.5	Fig. 9
$t_{PHL}/t_{PLH}$	propagation delay $B_I$ to $Q_n$		23	44		55		66	ns	4.5	Fig. 10
$t_{PHL}/t_{PLH}$	propagation delay $\overline{LT}$ to $Q_n$		16	30		38		45	ns	4.5	Fig. 8
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Figs 8, 9 and 10
$t_W$	latch enable pulse width LOW	16	5		20		24		ns	4.5	Fig. 9
$t_{su}$	set-up time $D_n$ to $\overline{LE}$	12	5		15		18		ns	4.5	Fig. 11
$t_h$	hold time $D_n$ to $\overline{LE}$	0	-4		0		0		ns	4.5	Fig. 11

AC WAVEFORMS



Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Fig. 11

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION DIAGRAMS

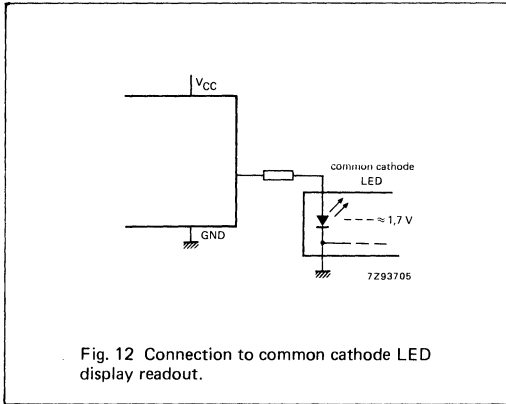


Fig. 12 Connection to common cathode LED display readout.

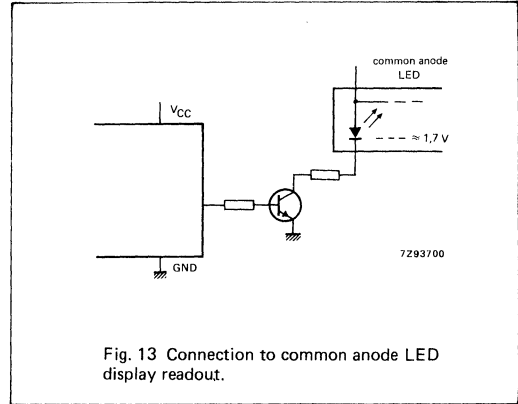
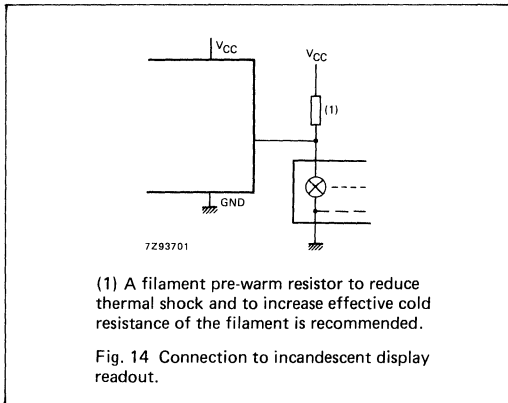


Fig. 13 Connection to common anode LED display readout.



(1) A filament pre-warm resistor to reduce thermal shock and to increase effective cold resistance of the filament is recommended.

Fig. 14 Connection to incandescent display readout.

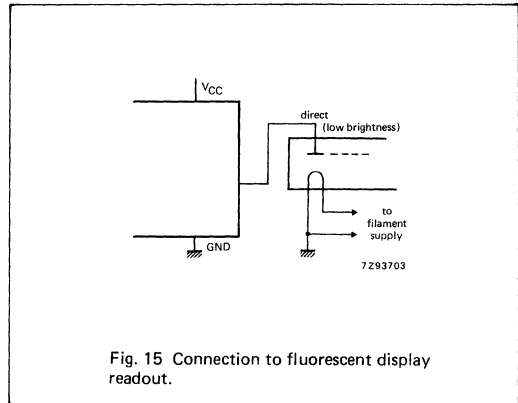


Fig. 15 Connection to fluorescent display readout.

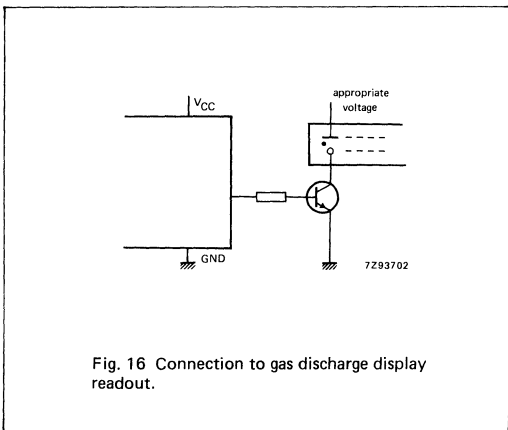


Fig. 16 Connection to gas discharge display readout.

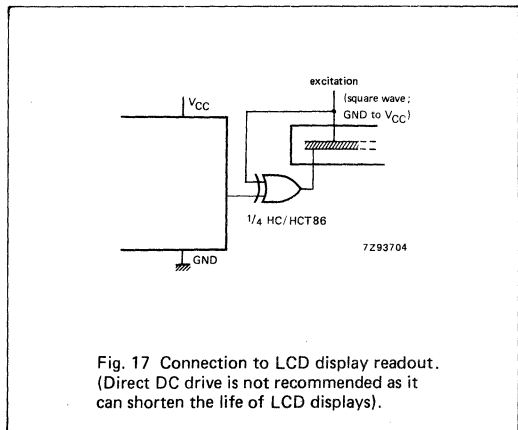


Fig. 17 Connection to LCD display readout. (Direct DC drive is not recommended as it can shorten the life of LCD displays).







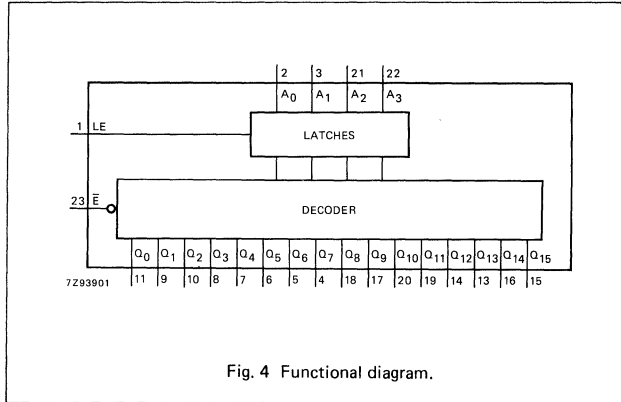


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs ( $A_0$  to  $A_3$ ), with latches, a latch enable input (LE), and an active LOW enable input ( $\bar{E}$ ). The 16 outputs ( $Q_0$  to  $Q_{15}$ ) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on  $A_n$ . When LE goes LOW, the last data present at  $A_n$  are stored in the latches and the outputs remain stable. When  $\bar{E}$  is LOW, the selected output, determined by the contents of the latch, is HIGH. At  $\bar{E}$  HIGH, all outputs are LOW. The enable input ( $\bar{E}$ ) does not affect the state of the latch.

When the "4514" is used as a demultiplexer,  $\bar{E}$  is the data input and  $A_0$  to  $A_3$  are the address inputs.

**APPLICATIONS**

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

**FUNCTION TABLE**

INPUTS					OUTPUTS																
$\bar{E}$	$A_0$	$A_1$	$A_2$	$A_3$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	$Q_7$	$Q_8$	$Q_9$	$Q_{10}$	$Q_{11}$	$Q_{12}$	$Q_{13}$	$Q_{14}$	$Q_{15}$	
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L

LE = HIGH  
H = HIGH voltage level  
L = LOW voltage level  
X = don't care

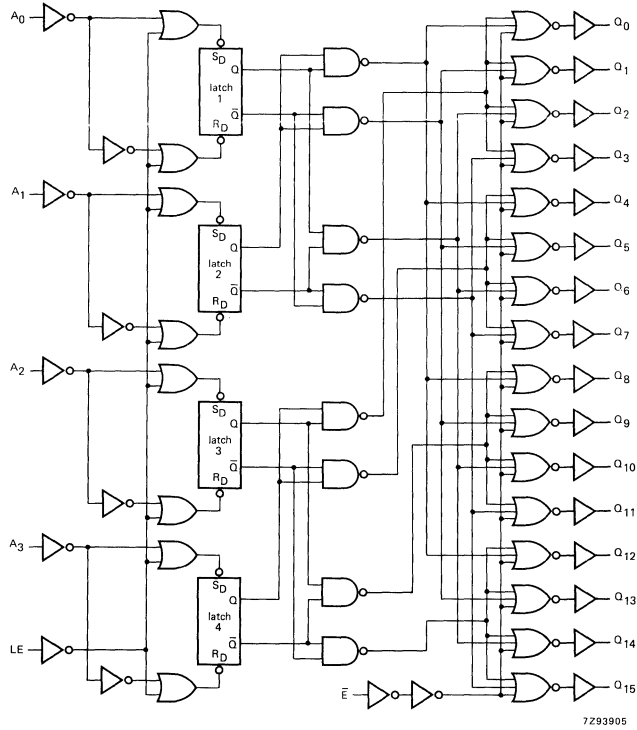


Fig. 5 Logic diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay E to Q <sub>n</sub>		41 15 12	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>w</sub>	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	90 18 15	25 9 7		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> to LE	1 1 1	-11 -4 -3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	0.65
LE	1.40
$\bar{E}$	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>		30	55		69		83	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		29	50		63		75	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to Q <sub>n</sub>		17	40		50		60	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	latch enable pulse width HIGH	16	4		20		24		ns	4.5	Fig. 7
t <sub>SU</sub>	set-up time A <sub>n</sub> to LE	18	9		23		27		ns	4.5	Fig. 7
t <sub>H</sub>	hold time A <sub>n</sub> to LE	3	-3		3		3		ns	4.5	Fig. 7

AC WAVEFORMS

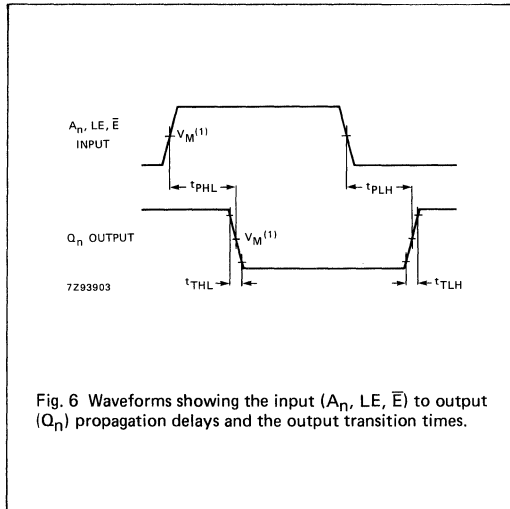


Fig. 6 Waveforms showing the input ( $A_n$ , LE,  $\bar{E}$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

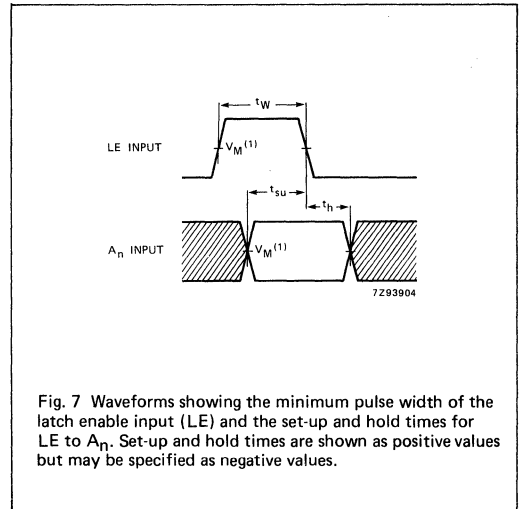


Fig. 7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to  $A_n$ . Set-up and hold times are shown as positive values but may be specified as negative values.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

4-TO-16 LINE DECODER/DEMULTIPLEXER WITH INPUT LATCHES

FEATURES

- Inverting outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	25	26	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	44	46	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f<sub>i</sub> = input frequency in MHz
- f<sub>o</sub> = output frequency in MHz
- Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
- C<sub>L</sub> = output load capacitance in pF
- V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4515P: 24-lead DIL; plastic (SOT-101A).

PC74HC/HCT4515T: 24-lead mini-pack; plastic (SO-24; SOT-137A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A <sub>0</sub> to A <sub>3</sub>	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	Q̄ <sub>0</sub> to Q̄ <sub>15</sub>	multiplexer outputs (active LOW)
12	GND	ground (0 V)
23	E	enable input (active LOW)
24	V <sub>CC</sub>	positive supply voltage

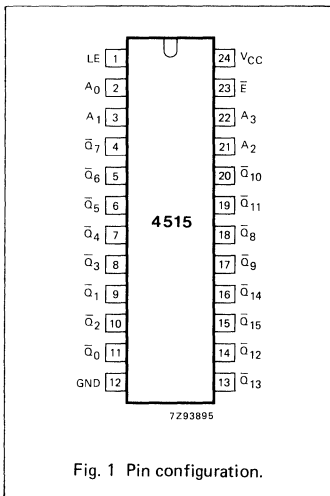


Fig. 1 Pin configuration.

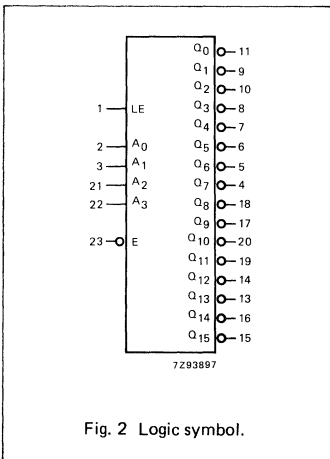


Fig. 2 Logic symbol.

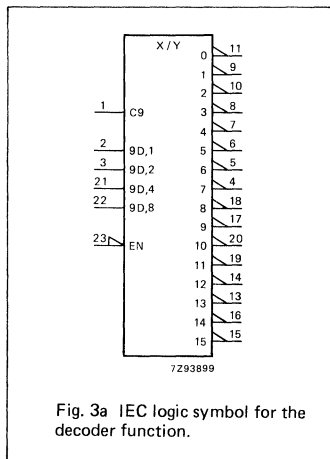


Fig. 3a IEC logic symbol for the decoder function.

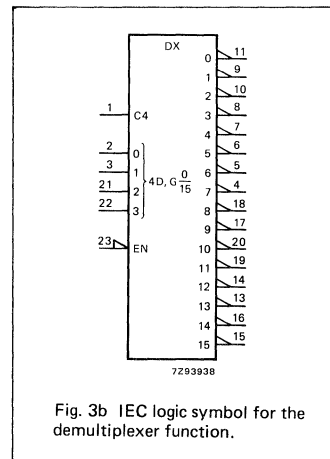


Fig. 3b IEC logic symbol for the demultiplexer function.

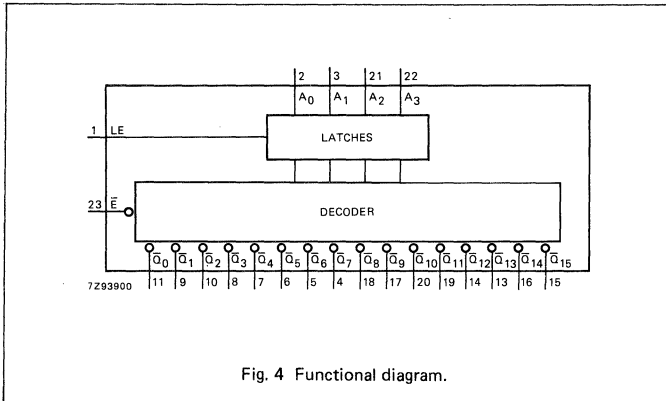


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs ( $A_0$  to  $A_3$ ) with latches, a latch enable input (LE), and an active LOW enable input ( $\bar{E}$ ). The 16 inverting outputs ( $\bar{Q}_0$  to  $\bar{Q}_{15}$ ) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on  $A_n$ . When LE goes LOW, the last data present at  $A_n$  are stored in the latches and the outputs remain stable. When  $\bar{E}$  is LOW, the selected output, determined by the contents of the latch, is LOW. At  $\bar{E}$  is HIGH, all outputs are HIGH. The enable input ( $\bar{E}$ ) does not affect the state of the latch.

When the "4515" is used as a demultiplexer,  $\bar{E}$  is the data input and  $A_0$  to  $A_3$  are the address inputs.

**APPLICATIONS**

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

**FUNCTION TABLE**

INPUTS					OUTPUTS																
$\bar{E}$	$A_0$	$A_1$	$A_2$	$A_3$	$\bar{Q}_0$	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	$\bar{Q}_6$	$\bar{Q}_7$	$\bar{Q}_8$	$\bar{Q}_9$	$\bar{Q}_{10}$	$\bar{Q}_{11}$	$\bar{Q}_{12}$	$\bar{Q}_{13}$	$\bar{Q}_{14}$	$\bar{Q}_{15}$	
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

LE = HIGH  
H = HIGH voltage level  
L = LOW voltage level  
X = don't care

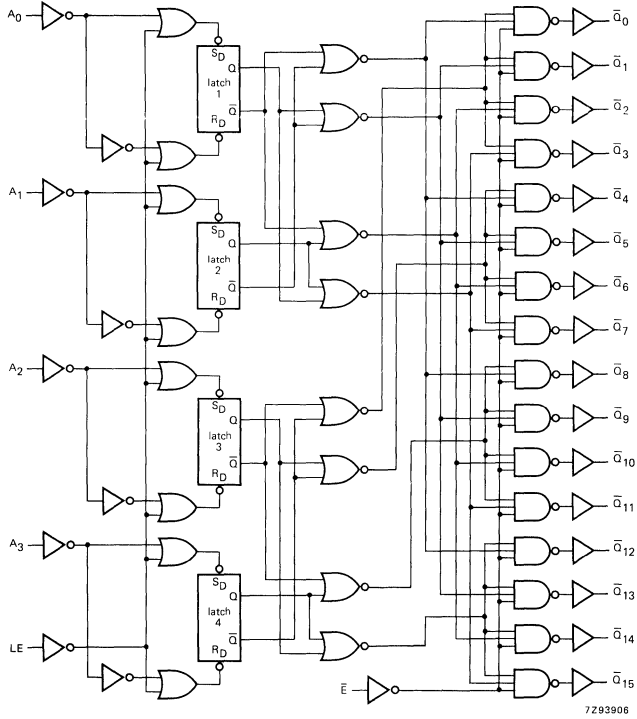


Fig. 5 Logic diagram.



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Q}_n$		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\bar{Q}_n$		66 24 19	225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to $\bar{Q}_n$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	latch enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	90 18 15	28 10 8		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> to LE	1 1 1	-11 -4 -3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 7

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

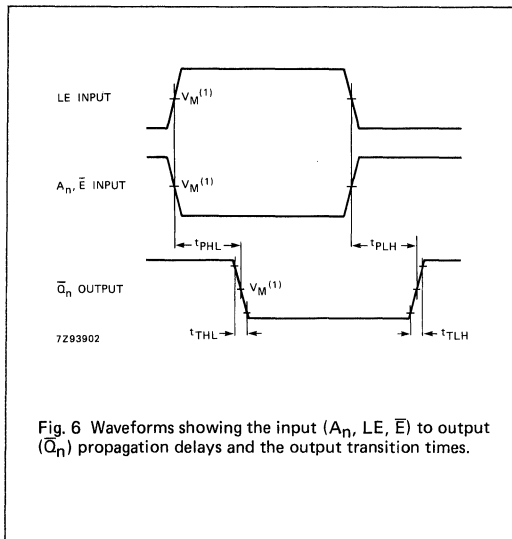
INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	0.65
LE	1.40
$\bar{E}$	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

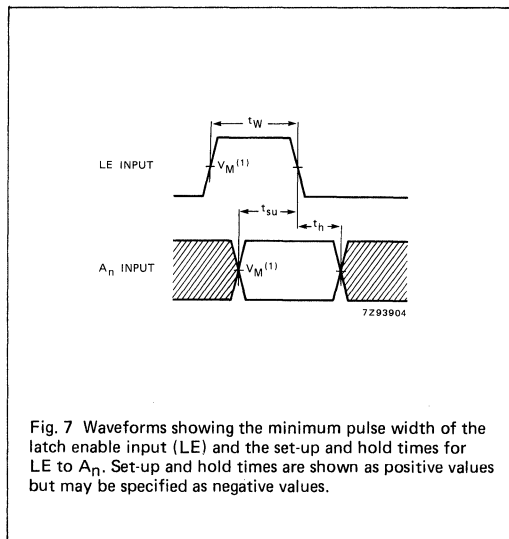
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Q}_n$		30	55		69		83	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\bar{Q}_n$		29	50		63		75	ns	4.5	Fig. 6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\bar{E}$ to $\bar{Q}_n$		18	40		50		60	ns	4.5	Fig. 6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 6
t <sub>W</sub>	latch enable pulse width HIGH	16	3		20		24		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time A <sub>n</sub> to LE	18	9		23		27		ns	4.5	Fig. 7
t <sub>h</sub>	hold time A <sub>n</sub> to LE	3	-2		3		3		ns	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .



Note to Fig. 7

The shaded areas indicate when the input is permitted to change for predictable output performance.

# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT4516

MSI

## BINARY UP/DOWN COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4516 are high-speed Si-gate CMOS devices and are pin compatible with the "4516" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4516 are edge-triggered synchronous up/down 4-bit binary counters with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input (CE), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D<sub>0</sub> to D<sub>3</sub>), four parallel outputs (Q<sub>0</sub> to Q<sub>3</sub>), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on D<sub>0</sub> to D<sub>3</sub> is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL and CE are LOW, the counter changes on the LOW-to-HIGH transition of CP. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when Q<sub>0</sub> to Q<sub>3</sub> are HIGH and CE is LOW. When counting down, TC is LOW when Q<sub>0</sub> to Q<sub>3</sub> and CE are LOW. A HIGH on MR resets the counter (Q<sub>0</sub> to Q<sub>3</sub> = LOW) independent of all other input conditions.

Logic equation for terminal count:

$$TC = \overline{CE} \cdot \{ (UP/\overline{DN}) \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 + (UP/\overline{DN}) \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \}$$

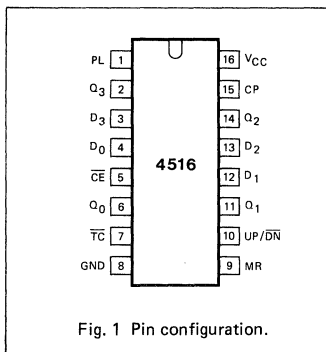


Fig. 1 Pin configuration.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	19	19	ns
f <sub>max</sub>	maximum clock frequency		45	45	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4516P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4516T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PL	parallel load input (active HIGH)
4, 12, 13, 3	D <sub>0</sub> to D <sub>3</sub>	parallel inputs
5	CE	count enable input (active LOW)
6, 11, 14, 2	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
7	TC	terminal count output (active LOW)
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
10	UP/DN	up/down control input
15	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage

### FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

H = HIGH voltage level

L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH clock transition

DUAL SYNCHRONOUS BCD COUNTER

FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4518 are high-speed Si-gate CMOS devices and are pin compatible with the "4518" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4518 are dual 4-bit internally synchronous BCD counters with an active HIGH clock input (nCP<sub>0</sub>) and an active LOW clock input (nCP<sub>1</sub>), buffered outputs from all four bit positions (nQ<sub>0</sub> to nQ<sub>3</sub>) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP<sub>0</sub> if nCP<sub>1</sub> is HIGH or the HIGH-to-LOW transition of nCP<sub>1</sub> if nCP<sub>0</sub> is LOW. Either nCP<sub>0</sub> or nCP<sub>1</sub> may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ<sub>0</sub> to nQ<sub>3</sub> = LOW) independent of nCP<sub>0</sub> and nCP<sub>1</sub>.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> , nCP <sub>1</sub> to nQ <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	22	24	ns
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		13	14	ns
f <sub>max</sub>	maximum clock frequency		67	55	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	27	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V  
Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4518P: 16-lead DIL; plastic (SOT-38Z).  
PC74HC/HCT4518T: 16-lead mini-pack, plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1CP <sub>0</sub> , 2CP <sub>0</sub>	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	1CP <sub>1</sub> , 2CP <sub>1</sub>	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	1Q <sub>0</sub> to 1Q <sub>3</sub>	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	2Q <sub>0</sub> to 2Q <sub>3</sub>	data outputs
16	V <sub>CC</sub>	positive supply voltage

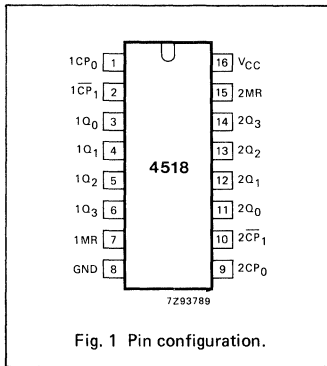


Fig. 1 Pin configuration.

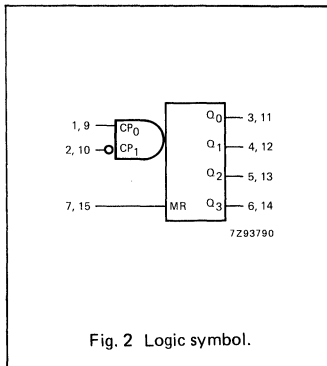


Fig. 2 Logic symbol.

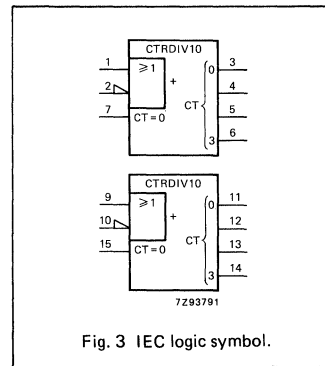


Fig. 3 IEC logic symbol.

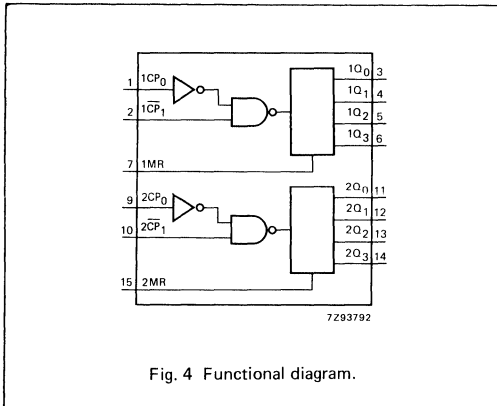


Fig. 4 Functional diagram.

FUNCTION TABLE

nCP <sub>0</sub>	nCP <sub>1</sub>	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q <sub>0</sub> to Q <sub>3</sub> = LOW

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition  
 ↓ = HIGH-to-LOW clock transition

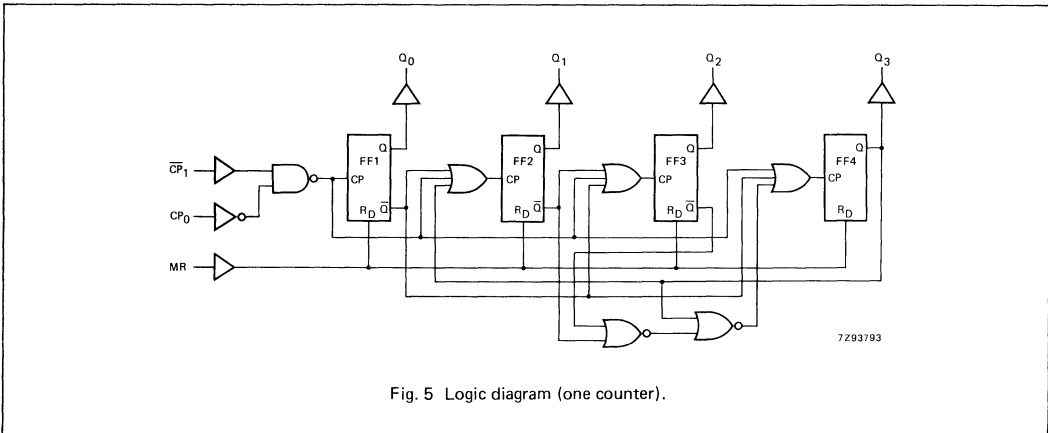


Fig. 5 Logic diagram (one counter).

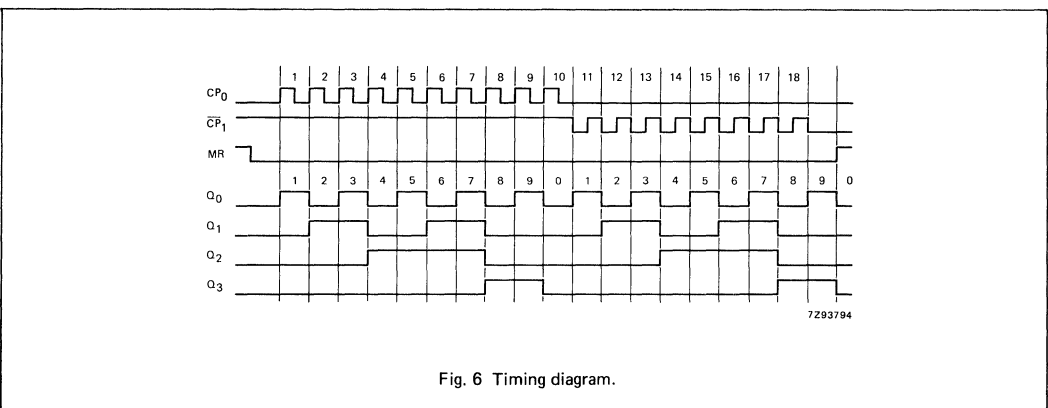


Fig. 6 Timing diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> , nCP <sub>1</sub> to nQ <sub>n</sub>		72	240		300		360	ns	2.0 4.5 6.0	Fig. 9
			26	48		60		72			
			21	41		51		61			
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		44	150		190		225	ns	2.0 4.5 6.0	Fig. 8
			16	30		38		45			
			13	26		33		38			
t <sub>THL</sub> / t <sub>TLLH</sub>	output transition time		19	75		95		110	ns	2.0 4.5 6.0	Fig. 9
			7	15		19		22			
			6	13		16		19			
t <sub>W</sub>	clock pulse width HIGH or LOW	80	25		100		120	ns	2.0 4.5 6.0	Fig. 8	
		16	9		20		24				
		14	7		17		20				
t <sub>W</sub>	master reset pulse width HIGH	120	39		150		180	ns	2.0 4.5 6.0	Fig. 8	
		24	14		30		36				
		20	11		26		31				
t <sub>rem</sub>	removal time nMR to nCP <sub>0</sub> , nCP <sub>1</sub>	0	-36		0		0	ns	2.0 4.5 6.0	Fig. 8	
		0	-13		0		0				
		0	-10		0		0				
t <sub>su</sub>	set-up time nCP <sub>1</sub> to nCP <sub>0</sub> ; nCP <sub>0</sub> to nCP <sub>1</sub>	80	17		100		120	ns	2.0 4.5 6.0	Fig. 7	
		16	6		20		24				
		14	5		17		20				
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	6.0	20		4.8		4.0	MHz	2.0 4.5 6.0	Fig. 8	
		30	61		24		20				
		35	73		28		24				

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP <sub>0</sub> , nCP <sub>1</sub>	0.30
nMR	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> , nCP <sub>1</sub> to nQ <sub>n</sub>		28	53		66		80	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		17	35		44		53	ns	4.5	Fig. 8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 9
t <sub>W</sub>	clock pulse width HIGH or LOW	20	11		25		30		ns	4.5	Fig. 8
t <sub>W</sub>	master reset pulse width HIGH	20	11		25		30		ns	4.5	Fig. 8
t <sub>rem</sub>	removal time nMR to nCP <sub>0</sub> , nCP <sub>1</sub>	0	-11		0		0		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time nCP <sub>1</sub> to nCP <sub>0</sub> ; nCP <sub>0</sub> to nCP <sub>1</sub>	16	5		20		24		ns	4.5	Fig. 7
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	25	50		20		17		MHz	4.5	Fig. 8



AC WAVEFORMS

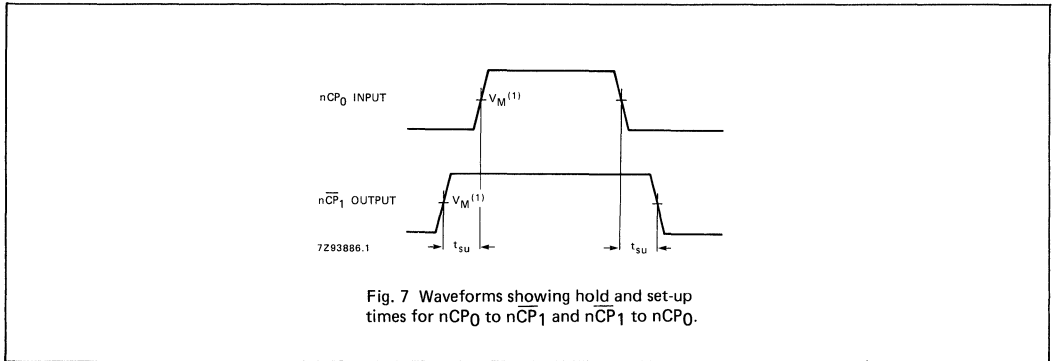


Fig. 7 Waveforms showing hold and set-up times for nCP<sub>0</sub> to nCP<sub>1</sub> and nCP<sub>1</sub> to nCP<sub>0</sub>.

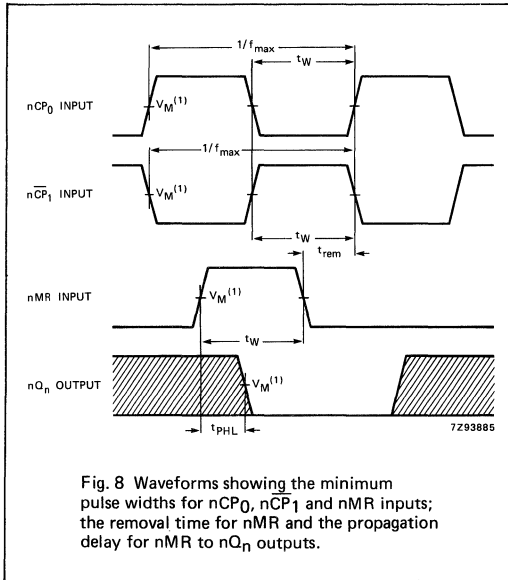


Fig. 8 Waveforms showing the minimum pulse widths for nCP<sub>0</sub>, nCP<sub>1</sub> and nMR inputs; the removal time for nMR and the propagation delay for nMR to nQ<sub>n</sub> outputs.

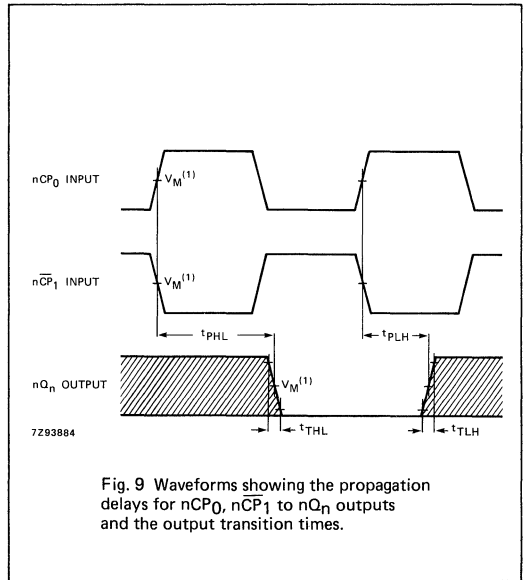


Fig. 9 Waveforms showing the propagation delays for nCP<sub>0</sub>, nCP<sub>1</sub> to nQ<sub>n</sub> outputs and the output transition times.

Note to Fig. 8 and Fig. 9

Conditions:

nCP<sub>1</sub> = HIGH while nCP<sub>0</sub> is triggered on a LOW-to-HIGH transition and nCP<sub>0</sub> = LOW, while nCP<sub>1</sub> is triggered on a HIGH-to-LOW transition.

Note to AC waveforms

(1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.  
HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

## DUAL 4-BIT SYNCHRONOUS BINARY COUNTER

### FEATURES

- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the "4520" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP<sub>0</sub>) and an active LOW clock input (nCP<sub>1</sub>), buffered outputs from all four bit positions (nQ<sub>0</sub> to nQ<sub>3</sub>) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP<sub>0</sub> if nCP<sub>1</sub> is HIGH or the HIGH-to-LOW transition of nCP<sub>1</sub> if nCP<sub>0</sub> is LOW. Either nCP<sub>0</sub> or nCP<sub>1</sub> may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ<sub>0</sub> to nQ<sub>3</sub> = LOW) independent of nCP<sub>0</sub> and nCP<sub>1</sub>.

### APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> , nCP <sub>1</sub> to nQ <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	24	28	ns
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		13	14	ns
f <sub>max</sub>	maximum clock frequency		66	64	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	29	29	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

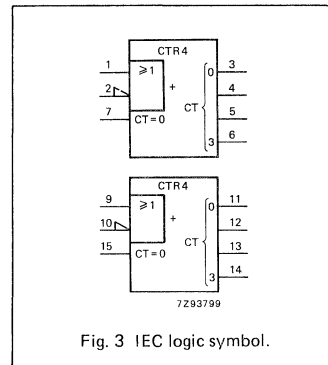
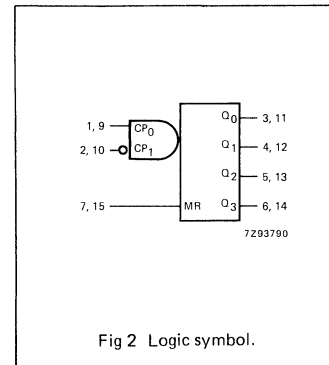
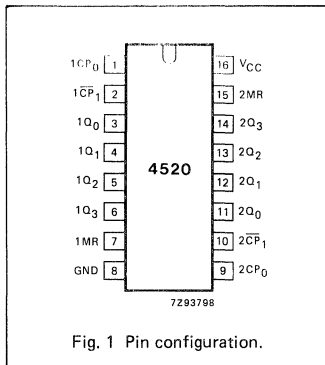
### ORDERING INFORMATION/PACKAGE OUTLINES

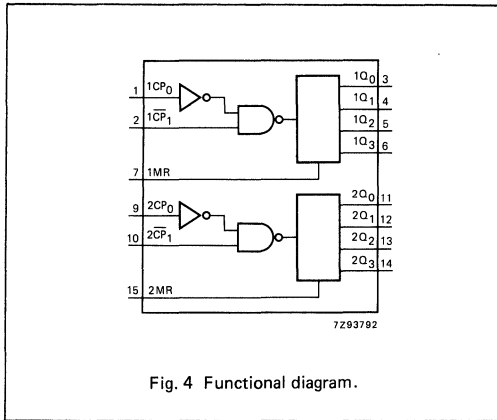
PC74HC/HCT4520P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4520T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1CP <sub>0</sub> , 2CP <sub>0</sub>	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	1CP <sub>1</sub> , 2CP <sub>1</sub>	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	1Q <sub>0</sub> to 1Q <sub>3</sub>	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	2Q <sub>0</sub> to 2Q <sub>3</sub>	data outputs
16	V <sub>CC</sub>	positive supply voltage

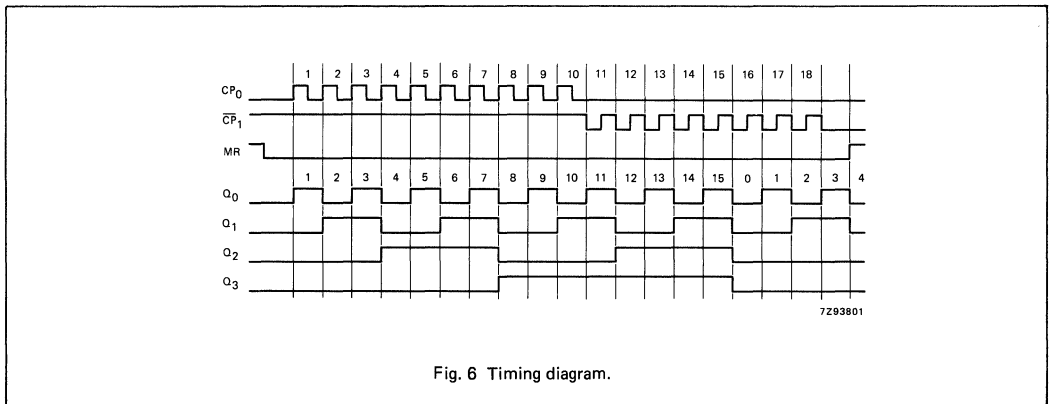
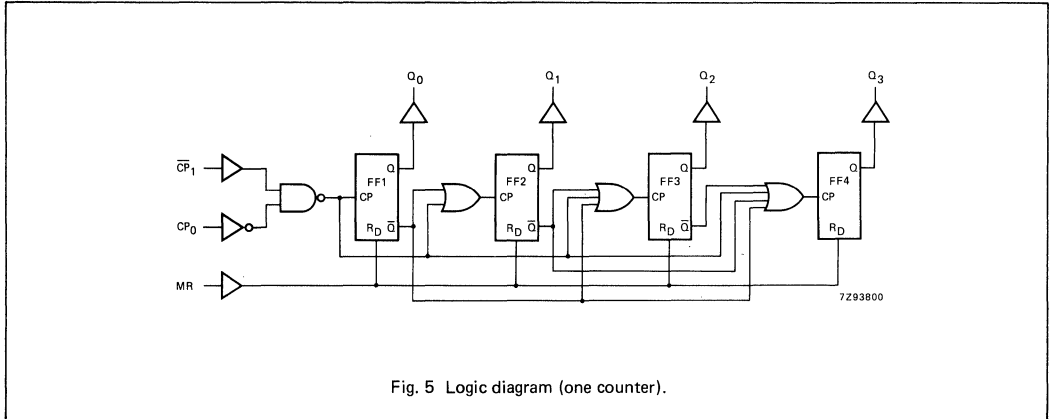




FUNCTION TABLE

nCP <sub>0</sub>	nCP <sub>1</sub>	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q <sub>0</sub> to Q <sub>3</sub> = LOW

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH clock transition  
↓ = HIGH-to-LOW clock transition



## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

IC<sub>C</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>n</sub>		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>n</sub>		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig. 8	
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8	
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
t <sub>W</sub>	master reset pulse width HIGH	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 7	
t <sub>rem</sub>	removal time nMR to nCP <sub>0</sub> , nCP <sub>1</sub>	0 0 0	-28 -10 -8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 7	
t <sub>su</sub>	set-up time nCP <sub>1</sub> to nCP <sub>0</sub> , nCP <sub>0</sub> to nCP <sub>1</sub>	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7	

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

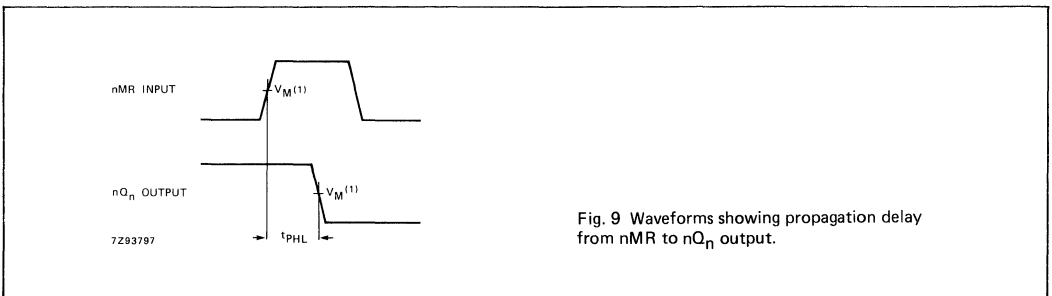
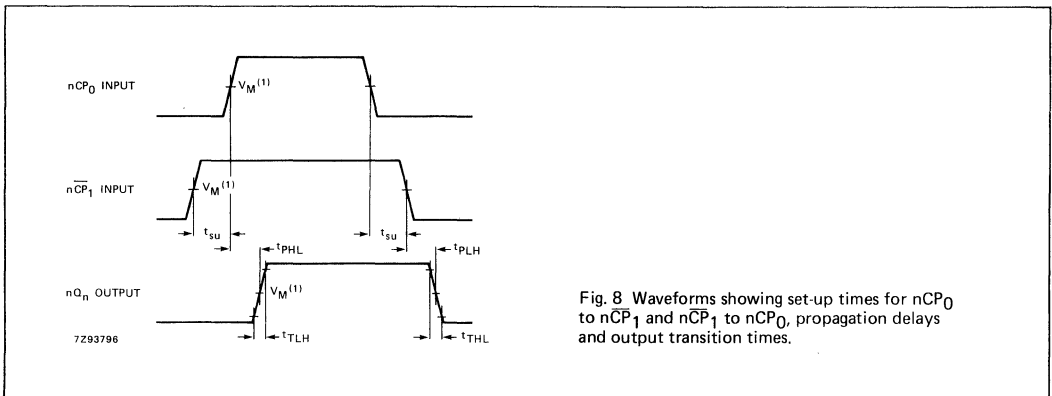
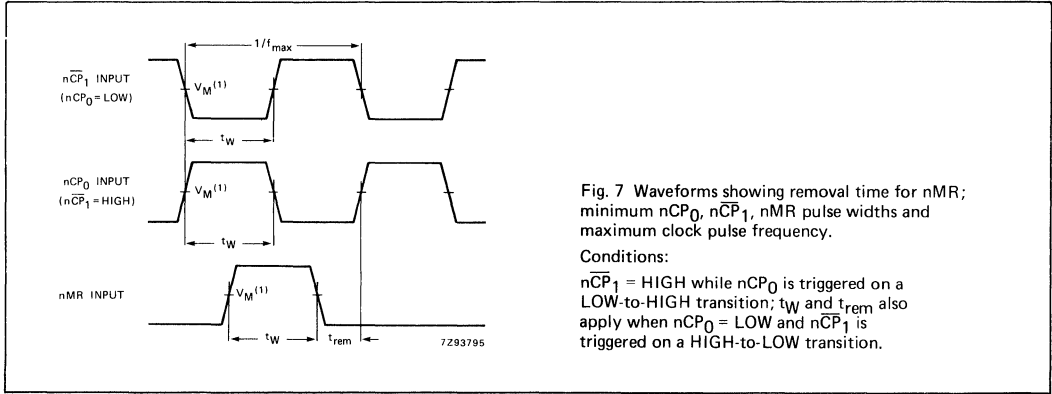
INPUT	UNIT LOAD COEFFICIENT
nCP <sub>0</sub> , nCP <sub>1</sub>	0.30
nMR	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>n</sub>		30	53		66		80	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>n</sub>		32	53		66		80	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		17	35		44		53	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>T LH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 8
t <sub>W</sub>	clock pulse width HIGH or LOW	20	13		25		30		ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width HIGH	20	12		25		30		ns	4.5	Fig. 7
t <sub>rem</sub>	removal time nMR to nCP <sub>0</sub> , nCP <sub>1</sub>	0	-9		0		0		ns	4.5	Fig. 7
t <sub>su</sub>	set-up time nCP <sub>1</sub> to nCP <sub>0</sub> , nCP <sub>0</sub> to nCP <sub>1</sub>	16	5		20		24		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	25	58		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ( $n\bar{A}_0$ ), an active HIGH trigger/retrigger input ( $nA_1$ ), an overriding active LOW direct reset input ( $n\bar{R}_D$ ), an output ( $nQ$ ) and its complement ( $n\bar{Q}$ ), and two pins ( $nC_{TC}$  and  $nRC_{TC}$ ) for connecting the external timing components  $C_T$  and  $R_T$ . Typical pulse width variation over temperature range is  $\pm 0.2\%$ .

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components  $C_T$  and  $R_T$ . The output pulse width (T) is equal to  $0.7 \times R_T \times C_T$ . The linear design techniques guarantee precise control of the output pulse width.

A LOW level at  $n\bar{R}_D$  terminates the output pulse immediately. The minimum reset pulse width depends on the value of the external timing capacitor  $C_T$ .

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $n\bar{A}_0, nA_1$ to $nQ, n\bar{Q}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	23	25	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per multivibrator	notes 1 and 2	—	—	pF

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- $f_i$  = input frequency in MHz
- $f_o$  = output frequency in MHz
- $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs
- $C_L$  = output load capacitance in pF
- $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4538P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4538T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}, 2C_{TC}$	external capacitor connections
2, 14	$1RC_{TC}, 2RC_{TC}$	external resistor/capacitor connections
3, 13	$1\bar{R}_D, 2\bar{R}_D$	direct reset inputs (active LOW)
4, 12	$1A_1, 2A_1$	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\bar{A}_0, 2\bar{A}_0$	trigger inputs (HIGH-to-LOW, edge-triggered)
6, 10	$1Q, 2Q$	pulse outputs
7, 9	$1\bar{Q}, 2\bar{Q}$	complementary pulse outputs
8	GND	ground (0 V)
16	$V_{CC}$	positive supply voltage

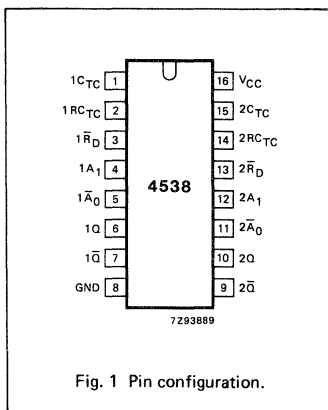


Fig. 1 Pin configuration.

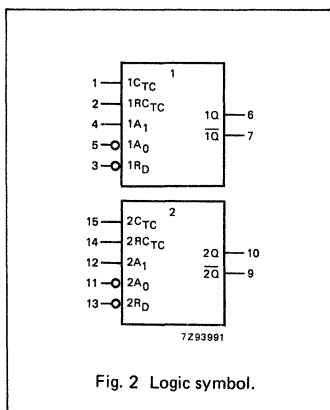


Fig. 2 Logic symbol.

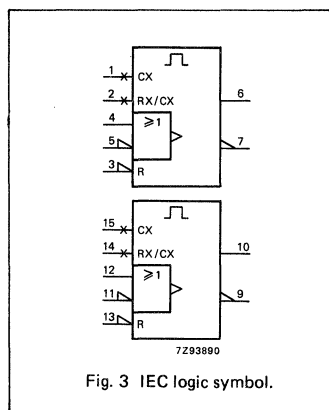


Fig. 3 IEC logic symbol.

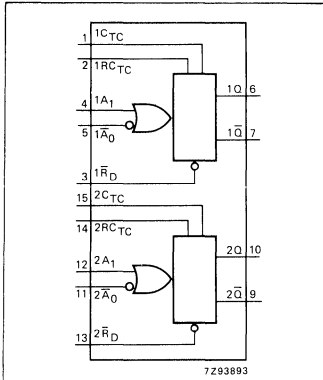
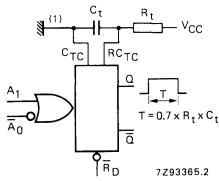


Fig. 4 Functional diagram.



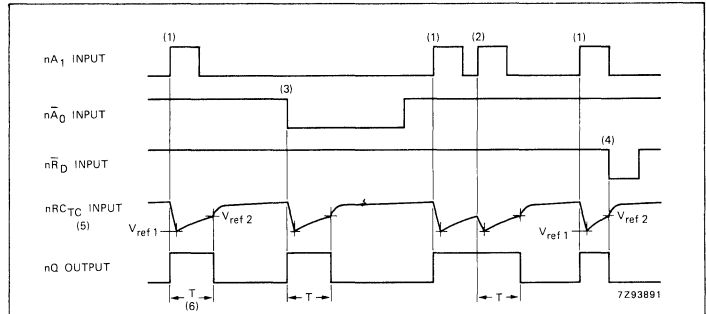
(1) Connect  $C_{TC}$  (pins 1 and 15) to GND (pin 8).

Fig. 5 Connection of the external timing components  $R_t$  and  $C_t$ .

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{A}_0$	$nA_1$	$n\bar{R}_D$	$nQ$	$n\bar{Q}$
↓	L	H	[Pulse]	[Pulse]
H	↑	H	[Pulse]	[Pulse]
X	X	L	L	H

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↓ = LOW-to-HIGH transition  
 ↑ = HIGH-to-LOW transition  
 = one HIGH level output pulse  
 = one LOW level output pulse



- (1) Positive edge triggering.
- (2) Positive edge retriggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5)  $V_{ref1}$  and  $V_{ref2}$  are internal reference voltages.
- (6)  $T = 0.7 \times R_t \times C_t$  (see also Fig. 5).

Fig. 6 Timing diagram.

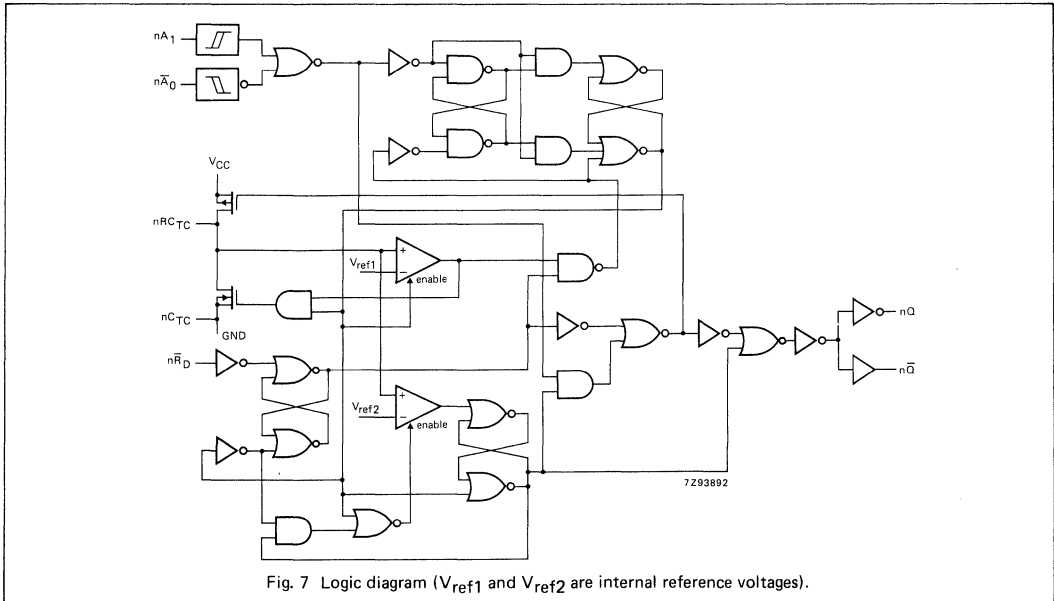


Fig. 7 Logic diagram ( $V_{ref1}$  and  $V_{ref2}$  are internal reference voltages).



**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PLH</sub>	propagation delay n $\bar{A}_0$ , nA <sub>1</sub> to nQ			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub>	propagation delay n $\bar{A}_0$ , nA <sub>1</sub> to n $\bar{Q}$			225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub>	propagation delay n $\bar{R}_D$ to nQ			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 8
t <sub>PLH</sub>	propagation delay n $\bar{R}_D$ to n $\bar{Q}$			250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 8
t <sub>THL</sub> / t <sub>TLLH</sub>	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	n $\bar{A}_0$ pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	nA <sub>1</sub> pulse width HIGH	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	n $\bar{R}_D$ pulse width LOW	80 16 14			100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>W</sub>	nQ, n $\bar{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ns	5.0	Fig. 8; R <sub>t</sub> = 10 k $\Omega$ ; C <sub>t</sub> = 0.1 $\mu$ F
t <sub>rem</sub>	removal time $\bar{R}_D$ to n $\bar{A}_0$ , nA <sub>1</sub>	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 8
t <sub>rt</sub>	retrigger time n $\bar{A}_0$ , nA <sub>1</sub>	- - -			- - -		- - -		ns	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$n\bar{A}_0, nA_1$	0.50
$n\bar{R}_D$	0.65

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

DEVELOPMENT DATA

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PLH}$	propagation delay $n\bar{A}_0, nA_1$ to nQ			60		75		90	ns	4.5	Fig. 8
$t_{PHL}$	propagation delay $n\bar{A}_0, nA_1$ to n $\bar{Q}$			55		69		83	ns	4.5	Fig. 8
$t_{PHL}$	propagation delay $n\bar{R}_D$ to nQ			40		50		60	ns	4.5	Fig. 8
$t_{PLH}$	propagation delay $n\bar{R}_D$ to n $\bar{Q}$			50		63		75	ns	4.5	Fig. 8
$t_{THL}/$ $t_{TLH}$	output transition time			15		19		21	ns	4.5	Fig. 8
$t_W$	$n\bar{A}_0, nA_1$ pulse width LOW	16			20		24		ns	4.5	Fig. 8
$t_W$	$n\bar{R}_D$ pulse width LOW	20			25		30		ns	4.5	Fig. 8
$t_W$	nQ, n $\bar{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ns	5.0	Fig. 8; $R_t = 10$ k $\Omega$ ; $C_t = 0.1$ $\mu$ F
$t_{rem}$	removal time $\bar{R}_D$ to $n\bar{A}_0, nA_1$	0			0		0		ns	4.5	Fig. 8
$t_{rt}$	retrigger time $n\bar{A}_0, nA_1$	-			-		-		ns	4.5	Fig. 8

AC WAVEFORMS

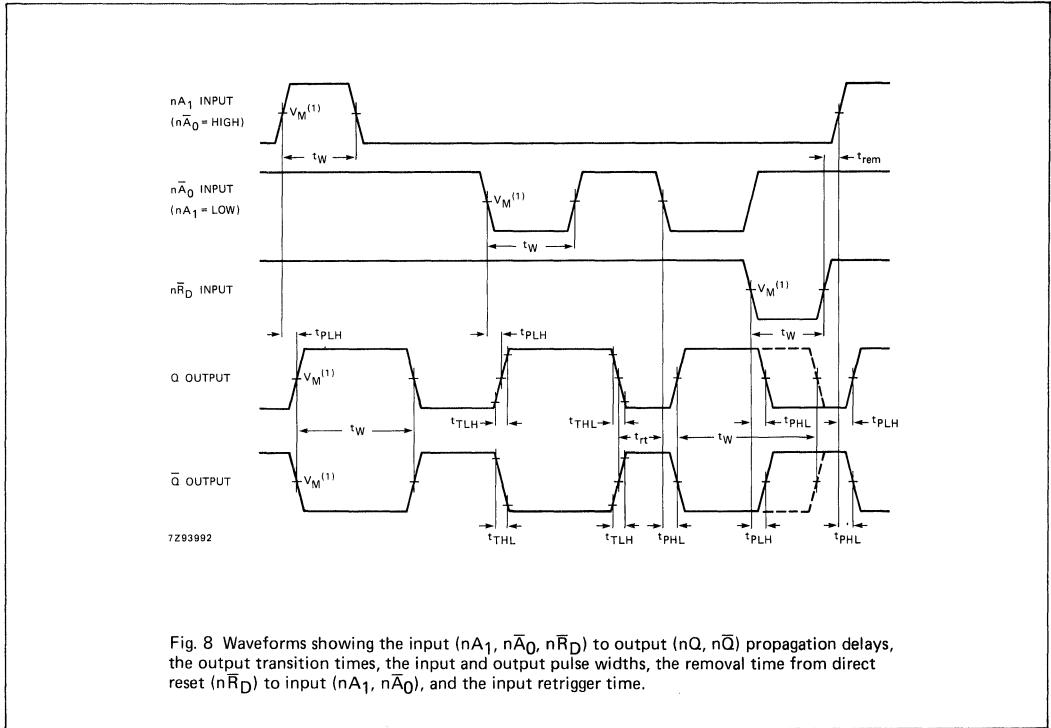


Fig. 8 Waveforms showing the input ( $nA_1$ ,  $n\bar{A}_0$ ,  $n\bar{R}_D$ ) to output ( $nQ$ ,  $n\bar{Q}$ ) propagation delays, the output transition times, the input and output pulse widths, the removal time from direct reset ( $n\bar{R}_D$ ) to input ( $nA_1$ ,  $n\bar{A}_0$ ), and the input retrigger time.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER FOR LCDs

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have four address inputs (D<sub>0</sub> to D<sub>3</sub>), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q<sub>a</sub> to Q<sub>g</sub>).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub> LD to Q <sub>n</sub> BI to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	29	33	ns
			32	31	ns
			20	28	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	42	42	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT4543P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT4543T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D <sub>0</sub> to D <sub>3</sub>	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12 13, 15, 14	Q <sub>a</sub> to Q <sub>g</sub>	segment outputs
16	V <sub>CC</sub>	positive supply voltage

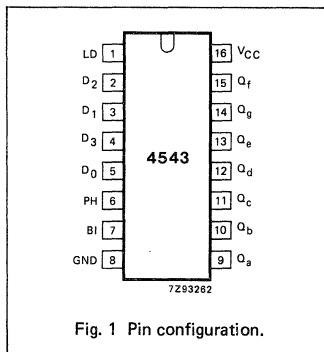


Fig. 1 Pin configuration.

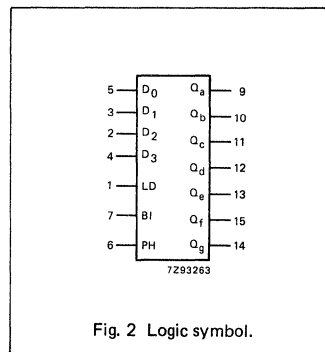


Fig. 2 Logic symbol.

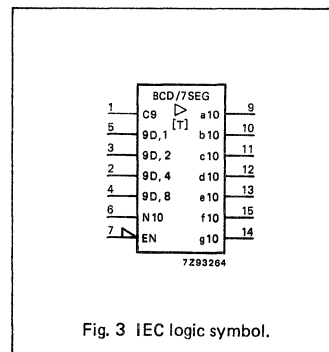


Fig. 3 IEC logic symbol.

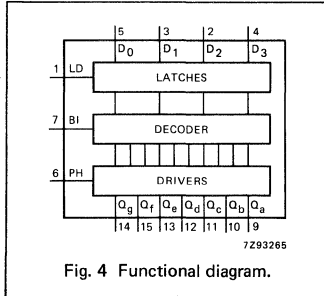


Fig. 4 Functional diagram.

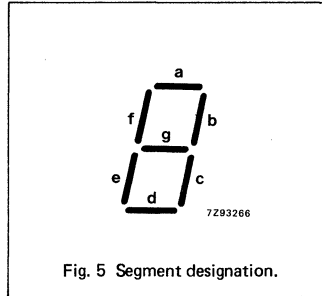


Fig. 5 Segment designation.

**APPLICATIONS**

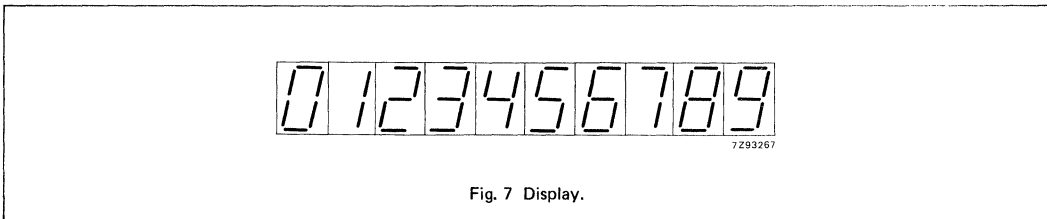
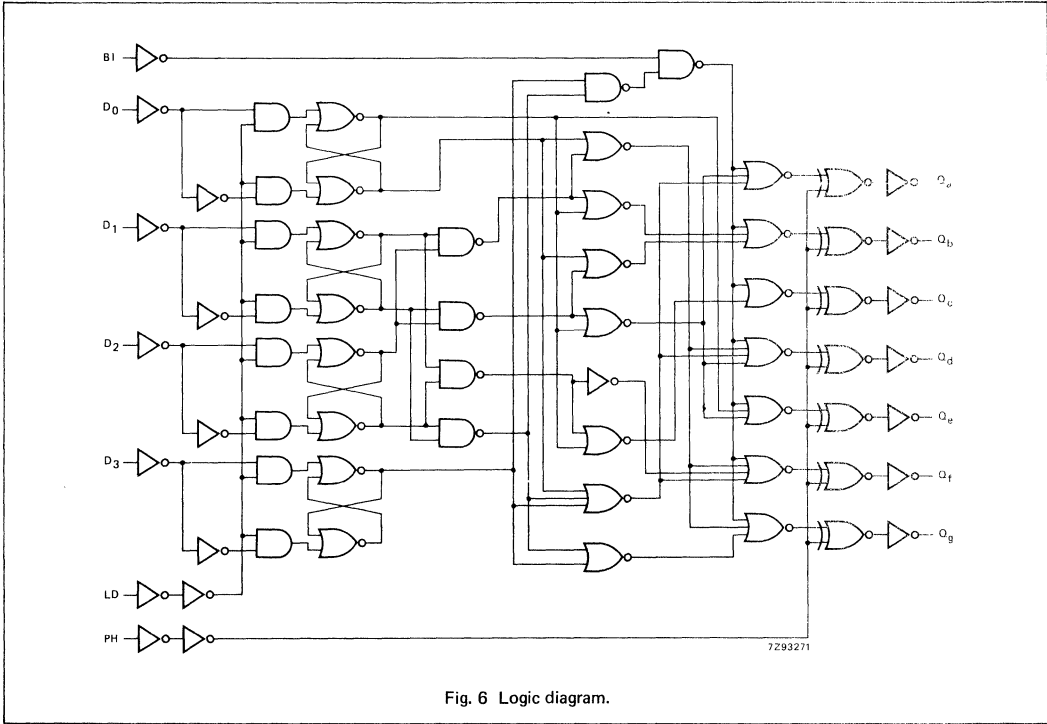
- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

**FUNCTION TABLE**

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH*	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Q <sub>a</sub>	Q <sub>b</sub>	Q <sub>c</sub>	Q <sub>d</sub>	Q <sub>e</sub>	Q <sub>f</sub>	Q <sub>g</sub>	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	H	H	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

\* For liquid crystal displays, apply a square-wave to PH.  
 \*\* Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134).  
For RATINGS see chapter "HCMOS family characteristics", section "Family specifications", standard outputs.

## DC CHARACTERISTICS FOR 74HC

Output capability: non-standard

I<sub>CC</sub> category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
VOH	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
VOH	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 1.0 mA -I <sub>O</sub> = 1.3 mA	
VOL	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
VOL	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 1.0 mA I <sub>O</sub> = 1.3 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current			8.0		80.0		160.0	μA	6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 0

## AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$		91 33 26	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 12
$t_{PHL}/t_{PLH}$	propagation delay LD to $Q_n$		102 37 30	370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig. 13
$t_{PHL}/t_{PLH}$	propagation delay BI to $Q_n$		66 24 19	265 53 45		330 66 56		495 99 84	ns	2.0 4.5 6.0	Fig. 14
$t_{PHL}/t_{PLH}$	propagation delay PH to $Q_n$		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	
$t_{THL}/t_{TLH}$	output transition time		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
$t_W$	LD pulse width HIGH or LOW	35 7 6	11 4 3		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 13
$t_{su}$	set-up time $D_n$ to LD	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 15
$t_h$	hold time $D_n$ to LD	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig. 15



**DC CHARACTERISTICS FOR 74HCT**

Output capability: non-standard  
I<sub>CC</sub> category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 1.0 mA
V <sub>OL</sub>	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 1.0 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	V <sub>CC</sub> or GND	
I <sub>CC</sub>	quiescent supply current			8.0		80.0		160.0	μA	5.5	V <sub>CC</sub> or GND	I <sub>O</sub> = 0
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V <sub>CC</sub> - 2.1 V	other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0

**Note to HCT types**

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here.  
To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

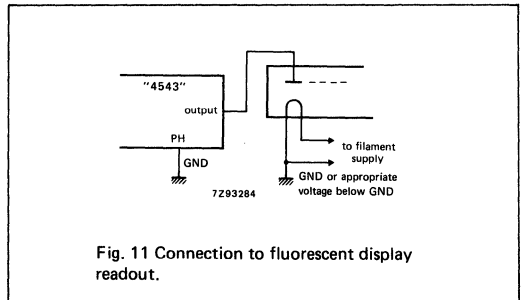
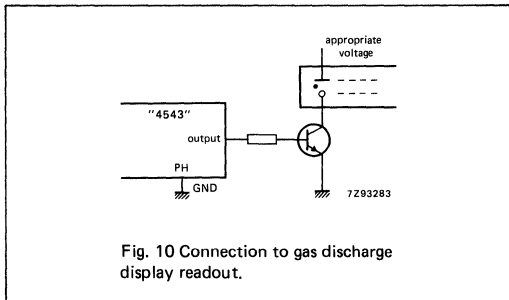
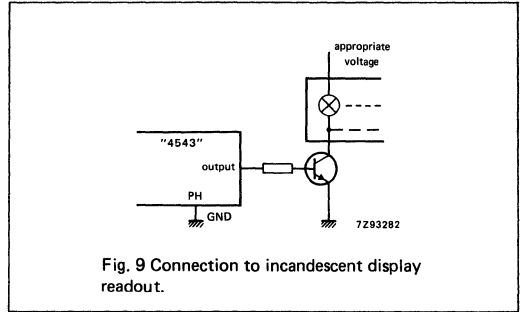
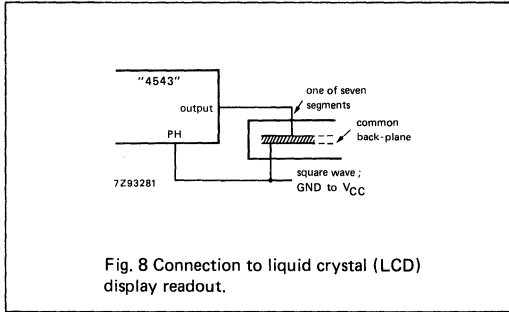
INPUT	UNIT LOAD COEFFICIENT
D <sub>0</sub> , D <sub>1</sub> , D <sub>2</sub>	1.00
D <sub>3</sub>	0.50
B <sub>I</sub>	0.50
L <sub>D</sub>	1.50
P <sub>H</sub>	1.25

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $D_n$ to $Q_n$		38	80		100		120	ns	4.5	Fig. 12
$t_{PHL}/t_{PLH}$	propagation delay LD to $Q_n$		36	68		85		102	ns	4.5	Fig. 13
$t_{PHL}/t_{PLH}$	propagation delay BI to $Q_n$		32	66		83		125	ns	4.5	Fig. 14
$t_{PHL}/t_{PLH}$	propagation delay PH to $Q_n$		24	66		83		125	ns	4.5	
$t_{THL}/t_{TLH}$	output transition time		23	50		63		75	ns	4.5	Figs 12, 13 and 14
$t_W$	LD pulse width HIGH or LOW	10	5		13		15		ns	4.5	Fig. 13
$t_{su}$	set-up time $D_n$ to LD	12	4		15		18		ns	4.5	Fig. 15
$t_h$	hold time $D_n$ to LD	8	2		10		12		ns	4.5	Fig. 15

APPLICATION DIAGRAMS



AC WAVEFORMS

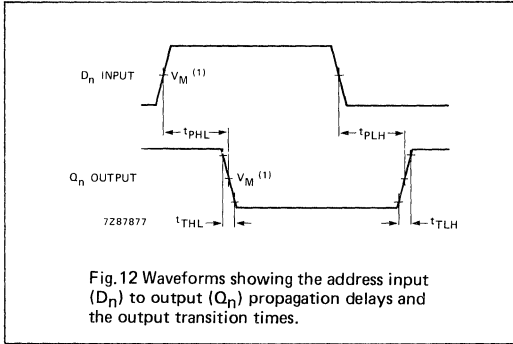


Fig. 12 Waveforms showing the address input ( $D_n$ ) to output ( $Q_n$ ) propagation delays and the output transition times.

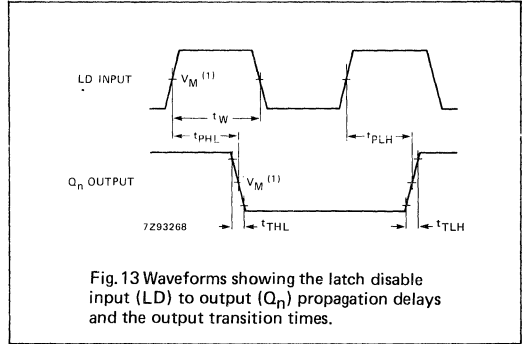


Fig. 13 Waveforms showing the latch disable input (LD) to output ( $Q_n$ ) propagation delays and the output transition times.

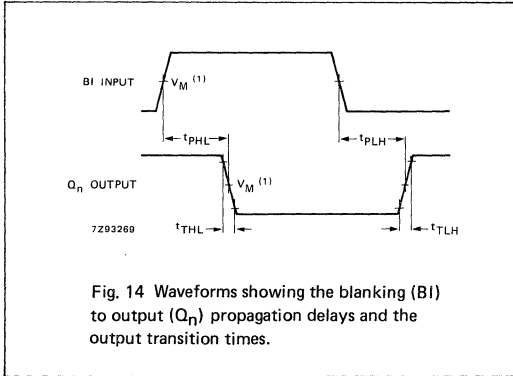


Fig. 14 Waveforms showing the blanking (BI) to output ( $Q_n$ ) propagation delays and the output transition times.

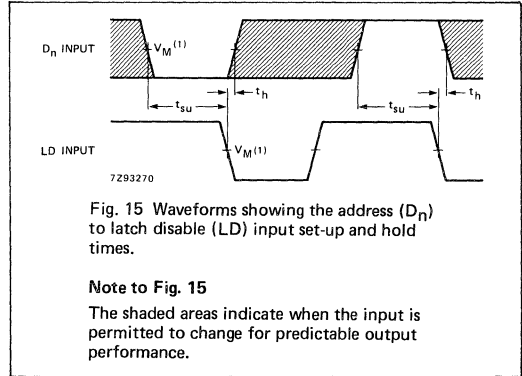


Fig. 15 Waveforms showing the address ( $D_n$ ) to latch disable (LD) input set-up and hold times.

Note to Fig. 15

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ ;
- HCT:  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND to } 3\text{ V}$ .



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT7030

MSI

## 9-BIT x 64-WORD FIFO REGISTER; 3-STATE

### FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- Master-reset input to clear data and control functions
- 25 MHz (typ.) shift-in, shift-out rates with flags
- 40 MHz (typ.) burst-in, burst-out rates without flags
- Cascadable to 25 MHz (typ.)
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: standard
- I<sup>2</sup>C category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT7030 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 25 MHz data-rate makes it ideal for high-speed applications. Burst data-rates of 40 MHz can be obtained in applications where the status flags are not used.

With separate controls for shift-in (SI) and shift-out (SO), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input (MR) and an output enable input (OE). Flags for data-in-ready (DIR) and data-out-ready (DOR) indicate the status of the device.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay SI, SO to DIR, DOR	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	14	16	ns
$f_{max}$	maximum clock frequency		40	40	MHz
$C_i$	input capacitance		3.5	3.5	pF

GND = 0 V;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

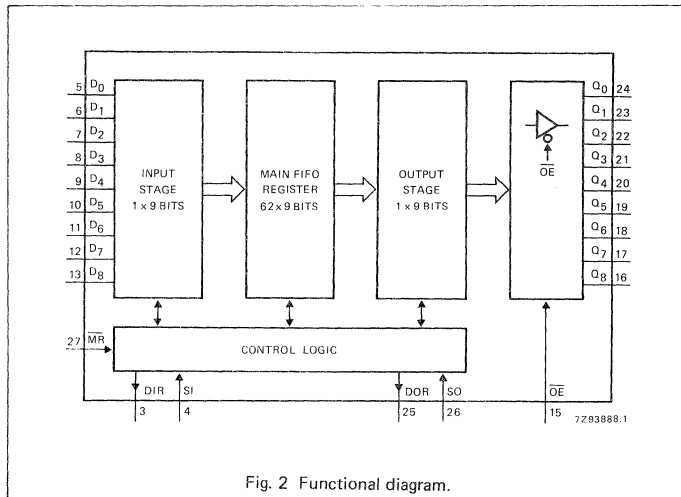
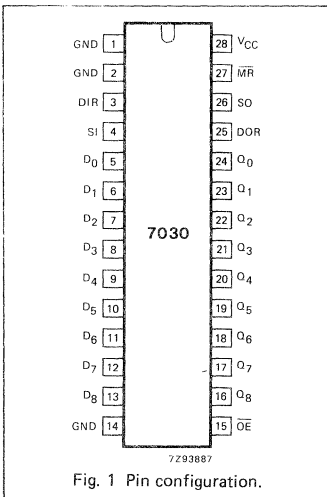
### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT7030P: 28-lead DIL; plastic (SOT-117D).

PC74HC/HCT7030T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 14	GND	ground (0 V) (all pins must be connected)
3	DIR	data-in-ready output
4	SI	shift-in input (active HIGH)
5, 6, 7, 8, 9, 10, 11, 12, 13	$D_0$ to $D_8$	parallel data inputs
15	$\overline{OE}$	output enable input (active LOW)
24, 23, 22, 21, 20, 19, 18, 17, 16	$Q_0$ to $Q_8$	3 state parallel data outputs
25	DOR	data-out-ready output
26	SO	shift-out input (active HIGH)
27	$\overline{MR}$	asynchronous master-reset input (active LOW)
28	$V_{CC}$	positive supply voltage



**GENERAL DESCRIPTION (continued)**

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

**INPUTS AND OUTPUTS****Data inputs (D<sub>0</sub> to D<sub>8</sub>)**

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration, i.e. 8 x 64, 7 x 64, down to 1 x 64, by tying unused data input pins to V<sub>CC</sub> or GND.

**Data outputs (Q<sub>0</sub> to Q<sub>8</sub>)**

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9 x 64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open.

**Master-reset ( $\overline{MR}$ )**

When  $\overline{MR}$  is LOW, all data and control functions within the FIFO are cleared, the data-in-ready (DIR) flag is set HIGH and the data-out-ready flag (DOR) is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

**Status flag outputs (DIR, DOR)**

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

DIR = HIGH indicates the input state is empty and ready to accept valid data;

DIR = LOW indicates that the FIFO is full or that a previous shift-in operation is not complete;

DOR = HIGH assures valid data is present at the outputs Q<sub>0</sub> to Q<sub>8</sub> (does not indicate that new data is awaiting transfer into the output stage);

DOR = LOW indicates the output stage is busy or there is no valid data.

**Shift-in control (SI)**

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process.

**Shift-out control (SO)**

A LOW-to-HIGH transition of SO causes the DOR flag to go LOW. A HIGH-to-

LOW transition of SO causes upstream data to move into the output stage, and empty locations to move towards the input stage.

**Output enable ( $\overline{OE}$ )**

The outputs Q<sub>0</sub> to Q<sub>8</sub> are enabled when  $\overline{OE}$  = LOW. When  $\overline{OE}$  = HIGH the outputs are in the high impedance OFF-state.

**FUNCTIONAL DESCRIPTION****Data input**

Following power-up, the master-reset ( $\overline{MR}$ ) input is pulsed LOW to clear the FIFO memory. The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D<sub>0</sub> to D<sub>8</sub> can be shifted-in using the SI control input. With SI = HIGH, data is shifted in to the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until SI is set to LOW. With SI = LOW the data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full.

With the FIFO full, SI can be held LOW until a shift-out (SO) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in (this remains at the first FIFO location until SI again goes LOW).

**Data transfer**

After data has been transferred from the input stage to the FIFO following SI = LOW, the data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as the data moves through the device.

**Data output**

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q<sub>0</sub> to Q<sub>8</sub>). The initial master-reset at power-on ( $\overline{MR}$  = LOW) sets DOR to LOW and clears the output stage. After  $\overline{MR}$  = HIGH, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH.

As the DOR flag goes HIGH, data can be shifted-out using the SO control input. With SO = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When SO is

held LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW. With the FIFO empty, the last word that was shifted-out is latched at the output Q<sub>0</sub> to Q<sub>8</sub>.

With the FIFO empty, the SO input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag going HIGH and a shift-out of data occurring. The SO control must be held LOW before additional data can be shifted out.

**High-speed burst mode**

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 40 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed.

**Expanded format**

The "7030" is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs themselves. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words x 9-bits.

**APPLICATIONS**

- High-speed disc or tape controller
- Video timebase correction
- A/D output buffers
- Voice synthesis
- Input/output formatter for digital filters and FFTs
- Bit-rate smoothing

## PHASE-LOCKED-LOOP WITH LOCK DETECTOR

## FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at  $V_{CC} = 4.5\text{ V}$
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C<sub>LD</sub>) and pin 8 (GND). For a frequency range of 100 kHz to 10 MHz the lock detector capacitor should be respectively 10 pF to 1000 pF.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$f_0$	VCO centre frequency	C1 = 40 pF R1 = 3 k $\Omega$ V <sub>CC</sub> = 5 V	18	18	MHz
C <sub>I</sub>	input capacitance (pin 5)		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	note 1	-	-	-

GND = 0 V; T<sub>amb</sub> = 25 °C

## Note 1

Applies to phase comparator section only (VCO disabled).  
For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.

## ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT7046AP: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT7046AT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

## APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

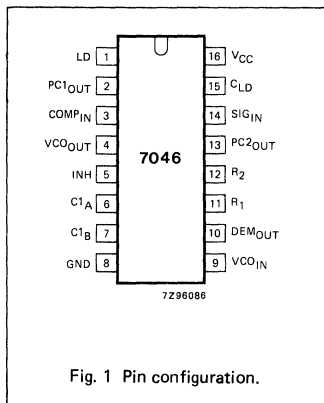


Fig. 1 Pin configuration.

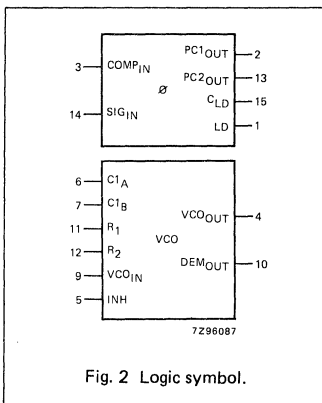


Fig. 2 Logic symbol.

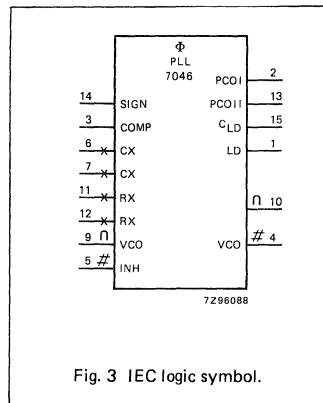


Fig. 3 IEC logic symbol.



**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	lock detector output (active HIGH)
2	PC1OUT	phase comparator 1 output
3	COMPIN	comparator input
4	VCOOUT	VCO output
5	INH	inhibit input
6	C1A	capacitor C1 connection A
7	C1B	capacitor C1 connection B
8	GND	ground (0 V)
9	VCOIN	VCO input
10	DEMOUT	demodulator output
11	R1	resistor R1 connection
12	R2	resistor R2 connection
13	PC2OUT	phase comparator 2 output
14	SIGIN	signal input
15	CLD	lock detector capacitor input
16	VCC	positive supply voltage

**GENERAL DESCRIPTION (Cont'd)**

**VCO**

The VCO requires one external capacitor C1 (between C1A and C1B) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEMOUT). In contrast to conventional techniques where the DEMOUT voltage is one threshold voltage lower than the VCO input voltage, here the DEMOUT voltage equals that of the VCO input. If DEMOUT is used, a load resistor (RS) should be connected from DEMOUT to GND; if unused, DEMOUT should be left open. The VCO output (VCOOUT) can be connected directly to the comparator input (COMPIN), or connected via a frequency-divider. The VCO output signal has a guaranteed duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

**Phase comparators**

The signal input (SIGIN) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

**Phase comparator 1 (PC1)**

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f1) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple (fr = 2f1) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{VCO}}{\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where VDEMOUT is the demodulator output at pin 10;

VDEMOUT = VPC1OUT (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (VDEMOUT), is the resultant of the phase differences of signals (SIGIN) and the comparator input (COMPIN) as shown in Fig. 6. The average of VDEMOUT is equal to 1/2 VCC when there is no signal

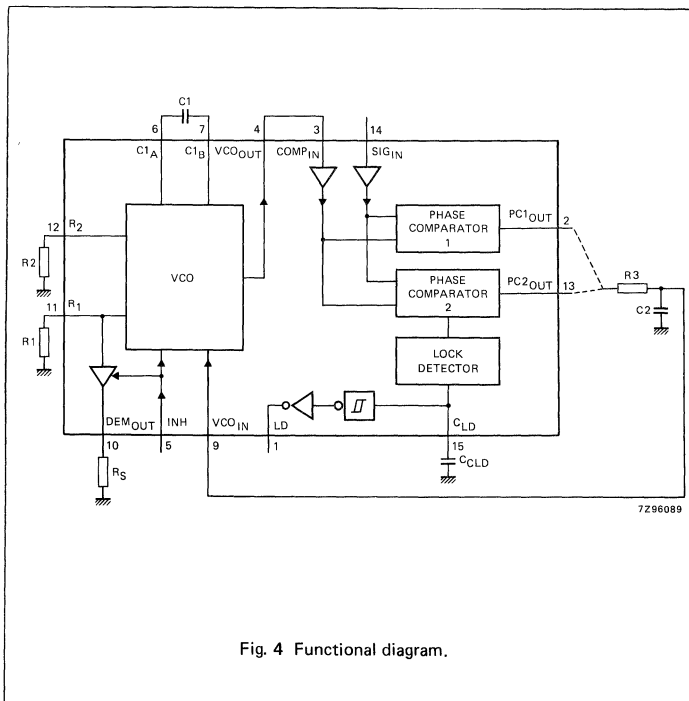


Fig. 4 Functional diagram.

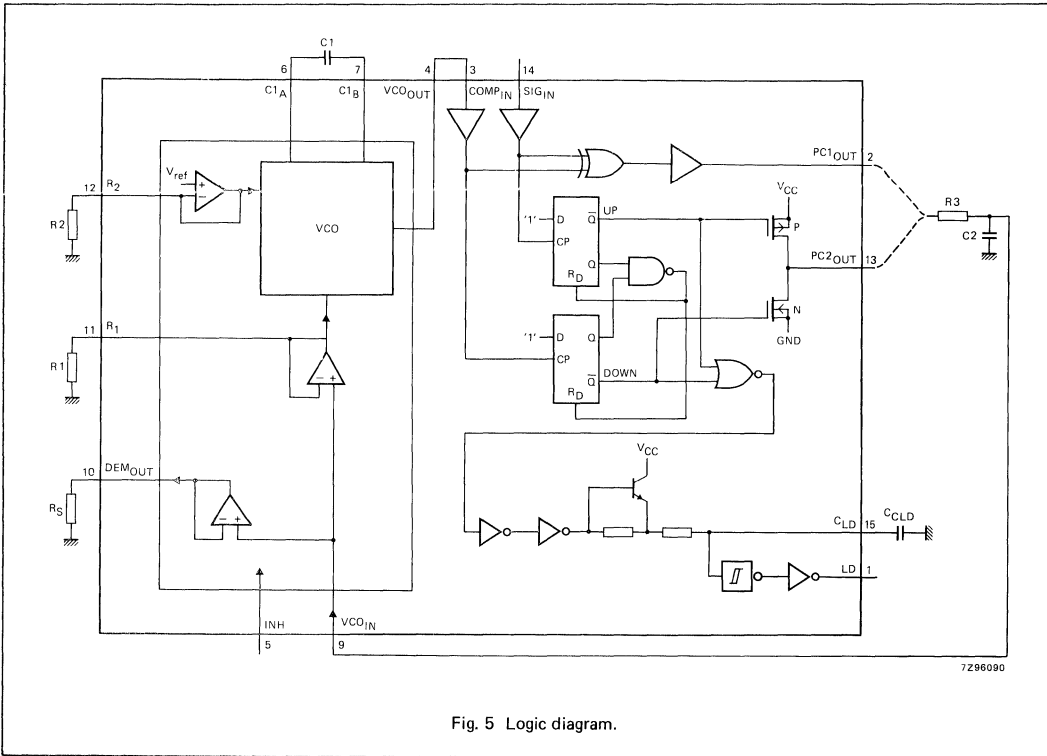


Fig. 5 Logic diagram.

or noise at SIG<sub>IN</sub> and with this input the VCO oscillates at the centre frequency (f<sub>0</sub>). Typical waveforms for the PC1 loop locked at f<sub>0</sub> are shown in Fig. 7.

The frequency capture range (2f<sub>c</sub>) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range (2f<sub>l</sub>) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

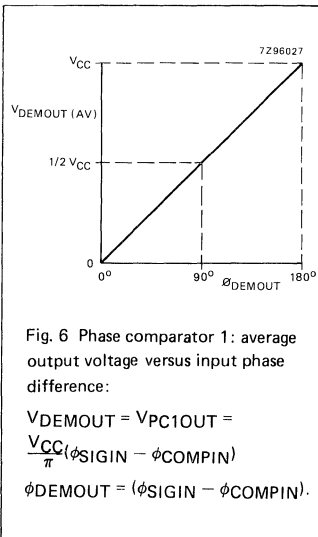


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

$$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$$

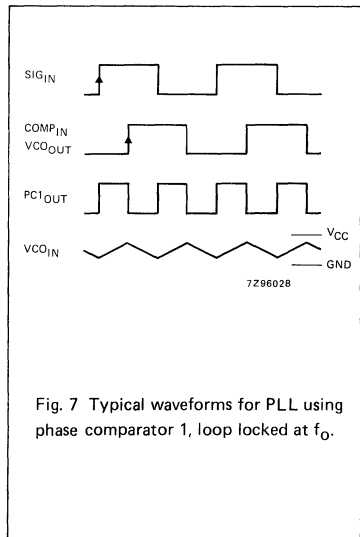


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f<sub>0</sub>.

**GENERAL DESCRIPTION (Cont'd)**

**Phase comparators (Cont'd)**

*Phase comparator 2 (PC2)*

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG<sub>IN</sub> and COMP<sub>IN</sub> are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG<sub>IN</sub> causes an up-count and COMP<sub>IN</sub> a down-count. The transfer function of PC2, assuming ripple ( $f_r = f_i$ ) is suppressed, is:

$$V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{4\pi}(\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where  $V_{\text{DEMOUT}}$  is the demodulator output at pin 10;  
 $V_{\text{DEMOUT}} = V_{\text{PC2OUT}}$  (via low-pass filter).

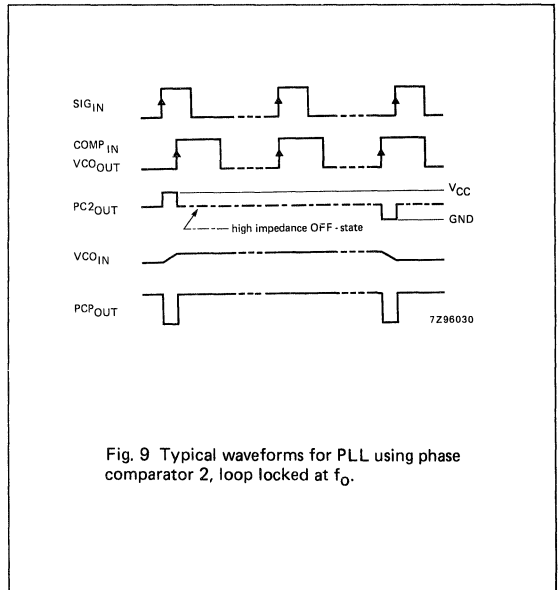
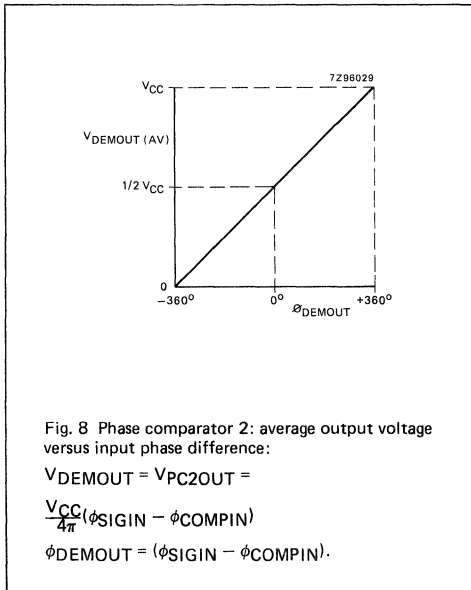
The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of SIG<sub>IN</sub> and COMP<sub>IN</sub> as shown in Fig. 8. Typical waveforms for the PC2 loop locked at  $f_0$  are shown in Fig. 9.

When the frequencies of SIG<sub>IN</sub> and COMP<sub>IN</sub> are equal but the phase of SIG<sub>IN</sub> leads that of COMP<sub>IN</sub>, the p-type output driver at PC2<sub>OUT</sub> is held "ON" for a time corresponding to the phase difference ( $\phi_{\text{DEMOUT}}$ ). When the phase of SIG<sub>IN</sub> lags that of COMP<sub>IN</sub>, the n-type driver is held "ON".

When the frequency of SIG<sub>IN</sub> is higher than that of COMP<sub>IN</sub>, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the SIG<sub>IN</sub> frequency is lower than the COMP<sub>IN</sub> frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the

voltage at the capacitor (C2) of the low-pass filter connected to PC2<sub>OUT</sub> varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP<sub>OUT</sub>) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG<sub>IN</sub> and COMP<sub>IN</sub> over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG<sub>IN</sub> the VCO adjusts, via PC2, to its lowest frequency.



## RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
$V_{CC}$	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
$V_I$	DC input voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$\pm I_{IK}$	DC input diode current except C1A, C1B		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{IK}$	DC input diode current C1A, C1B		10	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5$ V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C
	plastic DIL		500	mW	74HC/HCT above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

## DC CHARACTERISTICS FOR 74HC

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded

## Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8	0.5 1.35 1.8		V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>n</sub> OUT	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>n</sub> OUT	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>n</sub> OUT		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>n</sub> OUT		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0	5.0 11.0 27.0 45.0		μA	2.0 3.0 4.5 6.0	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current PC <sub>2</sub> OUT			0.5		5.0	10.0		μA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		800 250 150						kΩ	3.0 4.5 6.0		V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 10, 11 and 12

## VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40		0.47		0.54	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0		1.0	μA	5.5	V <sub>CC</sub> or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	0.9		3.2					V	4.5		over the range specified for R1; for linearity see Figs 18 and 19. Refer to note 2

## Notes

1. The parallel value of R1 and R2 should be more than 2.7 kΩ.
2. The maximum operating voltage can be as high as V<sub>CC</sub> - 0.9 V, however, this may result in an increased offset voltage.

DC CHARACTERISTICS FOR 74HC (Cont'd)

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
R <sub>S</sub>	resistor range	50		300				kΩ	4.5	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>	
V <sub>OFF</sub>	offset voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>		±20					mV	4.5	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig. 13	
R <sub>D</sub>	dynamic output resistance at DEM <sub>OUT</sub>		25					Ω	4.5	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>	

## AC CHARACTERISTICS FOR 74HC

## Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 14
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14
$t_{PZH}/$ $t_{PZL}$	3-state output enable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		83 30 24	280 56 48		350 70 60		420 84 71.4	ns	2.0 4.5 6.0	Fig. 15
$t_{PHZ}/$ $t_{PLZ}$	3-state output disable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 15
$V_I(p-p)$	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>		0.05 0.05 0.05 0.05						V	2.0 3.0 4.5 6.0	$f_i = 1$ MHz $C_L = 15$ pF

## VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.				max.
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2 V_{CC}$ ; $R1 = 100$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 100$ pF; see Fig. 16
$f_o$	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC}$ ; $R1 = 3$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 40$ pF; see Fig. 17
$\Delta f_{VCO}$	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	$R1 = 100$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 100$ pF; see Figs 18 and 19
$\delta_{VCO}$	duty factor at VCO <sub>OUT</sub>		50 50 50						%	3.0 4.5 6.0	



DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded

Note

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given above. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

## Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	3.15	2.4					V	4.5		
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		2.1	1.35				V	4.5		
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>n</sub> OUT	4.4	4.5		4.4		4.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>n</sub> OUT	3.98	4.32		3.84		3.7	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>n</sub> OUT		0	0.1		0.1	0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>n</sub> OUT		0.15	0.26		0.33	0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			30		38	45	μA	5.5	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current PC <sub>2</sub> OUT			0.5		5.0	10.0	μA	5.5	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		250					kΩ	4.5	V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 10, 11 and 12	

## DC CHARACTERISTICS FOR 74HCT (Cont'd)

## VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage INH	2.1 3.15 4.2	1.2 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2	V	3.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage INH		0.8 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8	0.9 1.35 1.8	V	3.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9	V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40 0.40		0.47 0.47	0.54 0.54	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0	1.0	μA	6.0	V <sub>CC</sub> or GND		
R1	resistor range	3.0 3.0 3.0		300 300 300				kΩ	3.0 4.5 6.0		note 1	
R2	resistor range	3.0 3.0 3.0		300 300 300				kΩ	3.0 4.5 6.0		note 1	
C1	capacitor range	40 40 40		no limit				pF	3.0 4.5 6.0			
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	0.9 0.9 0.9		1.9 3.2 4.6				V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 18 and 19. Refer to note 2	

## Notes

1. The parallel value of R1 and R2 should be more than 2.7 kΩ.
2. The maximum operating voltage can be as high as V<sub>CC</sub> - 0.9 V, however, this may result in an increased offset voltage.

## Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
R <sub>S</sub>	resistor range	50		300				kΩ	3.0 4.5 6.0	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>	
V <sub>OFF</sub>	offset voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>		±30 ±20 ±10					mV	3.0 4.5 6.0	V <sub>I</sub> = V <sub>COIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig. 13	
R <sub>D</sub>	dynamic output resistance at DEMOUT		25 25 25					Ω	3.0 4.5 6.0	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>	

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC1 <sub>OUT</sub>		26	45		56		68	ns	4.5	Fig. 14	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 14	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC2 <sub>OUT</sub>		35	60		75		90	ns	4.5	Fig. 15	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time SIG <sub>1IN</sub> , COMP <sub>1IN</sub> to PC2 <sub>OUT</sub>		40	70		88		105	ns	4.5	Fig. 15	
V <sub>I</sub> (p-p)	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>1IN</sub> or COMP <sub>1IN</sub>		0.05						V	4.5	f <sub>i</sub> = 1 MHz C <sub>L</sub> = 15 pF	

VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	typ.	max.	min.	max.				
Δf/T	frequency stability with temperature change				0.15				%/K	4.5	V <sub>I</sub> = V <sub>VCOIN</sub> within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 16b	
f <sub>o</sub>	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 17	
Δf <sub>VCO</sub>	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19	
δ <sub>VCO</sub>	duty factor at VCO <sub>OUT</sub>		50						%	4.5		

FIGURE REFERENCES FOR DC CHARACTERISTICS

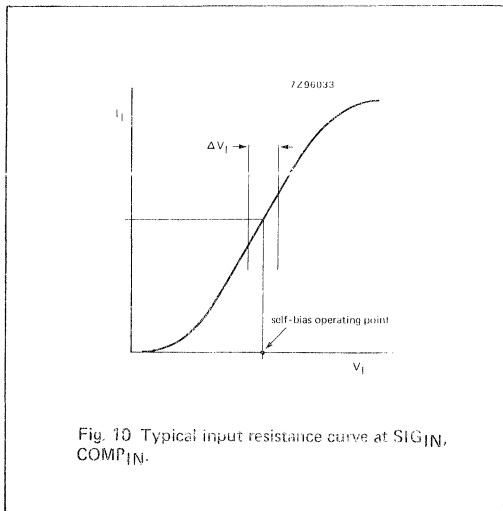


Fig. 10 Typical input resistance curve at SIG<sub>1N</sub>, COMP<sub>1N</sub>.

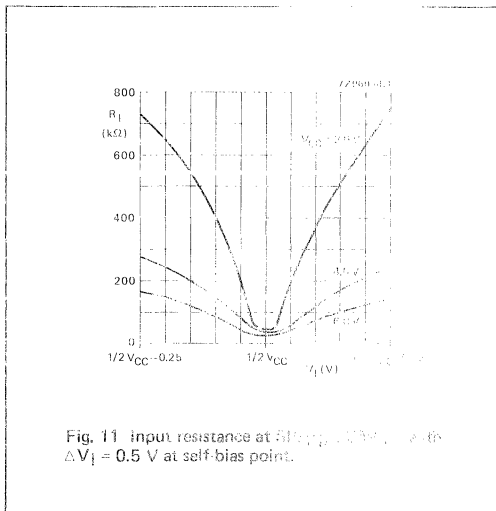


Fig. 11 Input resistance at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_i = 0.5$  V at self-bias point.

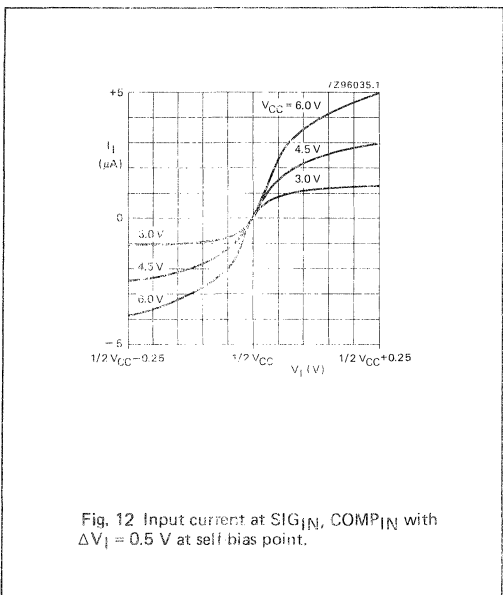


Fig. 12 Input current at SIG<sub>1N</sub>, COMP<sub>1N</sub> with  $\Delta V_i = 0.5$  V at self-bias point.

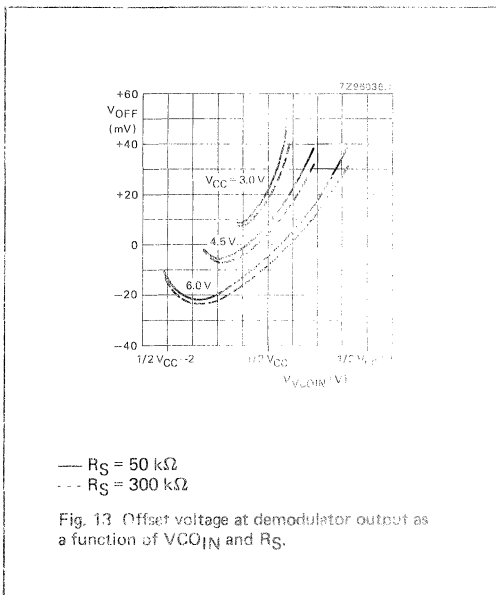
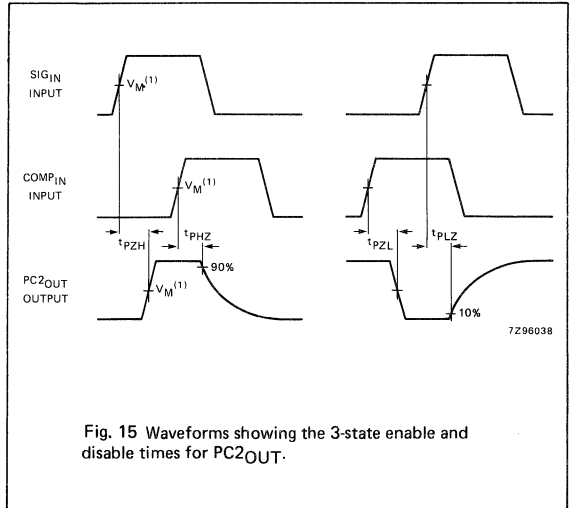
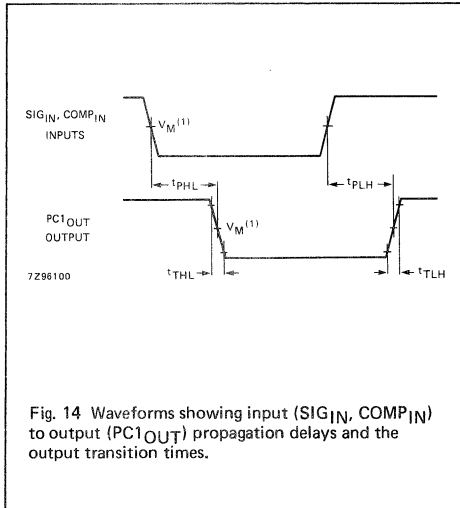


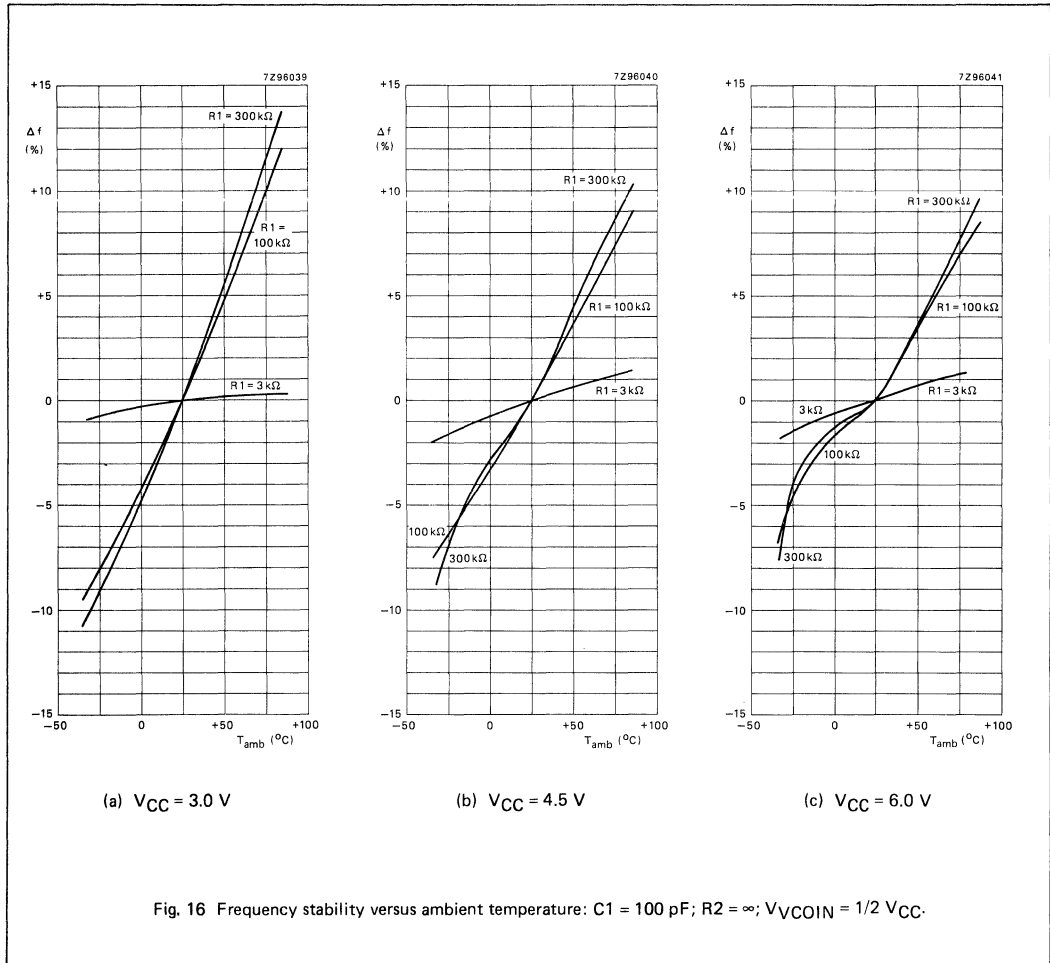
Fig. 13 Offset voltage at demodulator output as a function of VCO<sub>1N</sub> and  $R_S$ .

AC WAVEFORMS



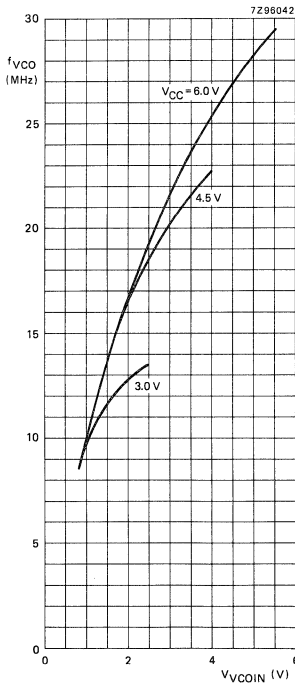
Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .
- HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

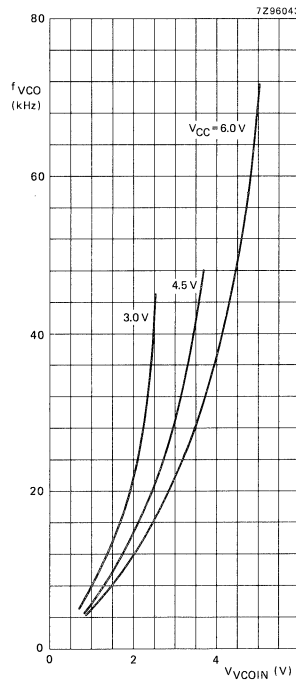




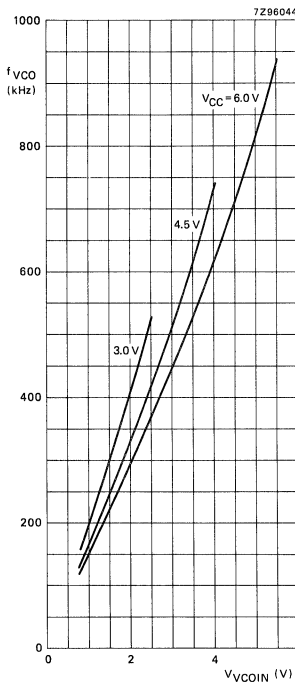
AC WAVEFORMS (Continued)



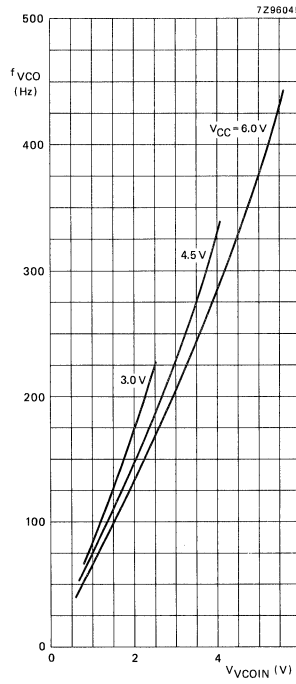
(a)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(b)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$



(c)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(d)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$

Fig. 17 Graphs showing VCO frequency ( $f_{VCO}$ ) as a function of the VCO input voltage ( $V_{VCOIN}$ ).

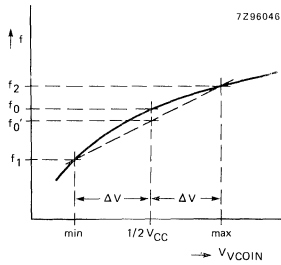


Fig. 18 Definition of VCO frequency linearity:

$\Delta V = 0.5 \text{ V}$  over the  $V_{CC}$  range:  
for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

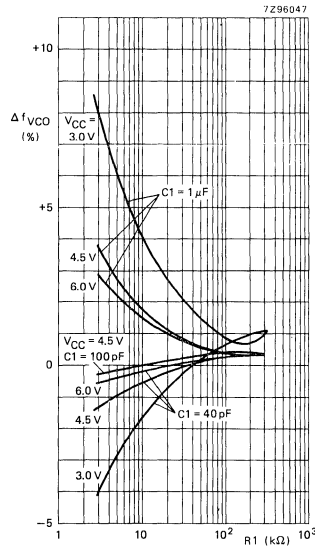
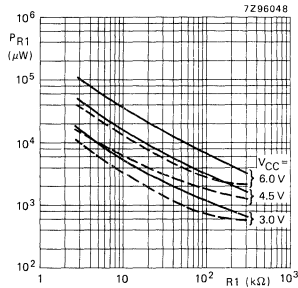
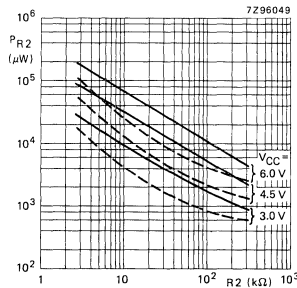


Fig. 19 Frequency linearity as a function of  $R_1$ ,  $C_1$  and  $V_{CC}$ :  $R_2 = \infty$  and  $\Delta V = 0.5 \text{ V}$ .



—  $C_1 = 40 \text{ pF}$   
- - -  $C_1 = 1 \mu\text{F}$

Fig. 20 Power dissipation versus the value of  $R_1$ :  $C_L = 50 \text{ pF}$ ;  $R_2 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ ;  $T_{\text{amb}} = 25^\circ\text{C}$ .



—  $C_1 = 40 \text{ pF}$   
- - -  $C_1 = 1 \mu\text{F}$

Fig. 21 Power dissipation versus the value of  $R_2$ :  $C_L = 50 \text{ pF}$ ;  $R_1 = \infty$ ;  $V_{VCOIN} = \text{GND} = 0 \text{ V}$ ;  $T_{\text{amb}} = 25^\circ\text{C}$ .

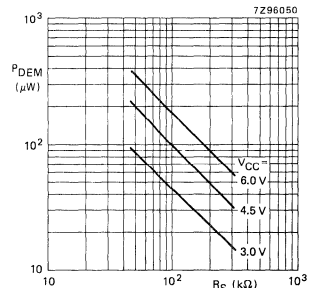


Fig. 22 Typical dc power dissipation of demodulator section as a function of  $R_S$ :  $R_1 = R_2 = \infty$ ;  $T_{\text{amb}} = 25^\circ\text{C}$ .

## APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046 in a phase-lock-loop system.

References should be made to Figs 27, 28 and 29 as indicated in the table.

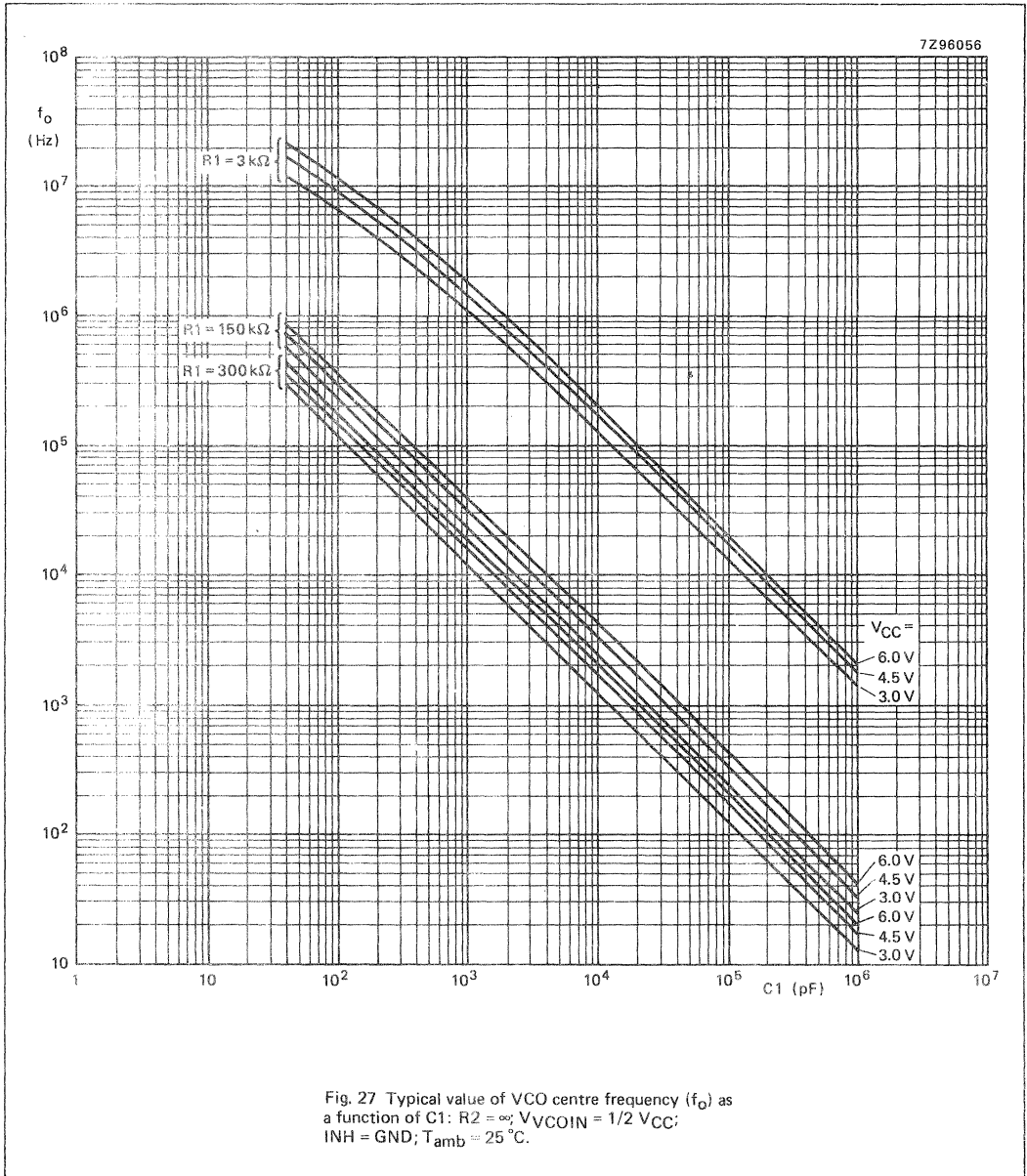
Values of the selected components should be within the following ranges:

- R1 between  $3\text{ k}\Omega$  and  $300\text{ k}\Omega$ ;  
 R2 between  $3\text{ k}\Omega$  and  $300\text{ k}\Omega$ ;  
 R1 + R2 parallel value  $> 2.7\text{ k}\Omega$ ;  
 C1 greater than  $40\text{ pF}$ .

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency without extra offset	PC1, PC2	<p><b>VCO frequency characteristic</b></p> <p>With <math>R2 = \infty</math> and R1 within the range <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 23.            (Due to R1, C1 time constant a small offset remains when <math>R2 = \infty</math>.)</p> <p>Fig. 23 Frequency characteristic of VCO operating without offset: <math>f_o</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	PC1	<p><b>Selection of R1 and C1</b></p> <p>Given <math>f_o</math>, determine the values of R1 and C1 using Fig. 27.</p>
	PC2	<p>Given <math>f_{max}</math> and <math>f_o</math>, determine the values of R1 and C1 using Fig. 27, use Fig. 29 to obtain <math>2f_L</math> and then use this to calculate <math>f_{min}</math>.</p>
VCO frequency with extra offset	PC1, PC2	<p><b>VCO frequency characteristic</b></p> <p>With R1 and R2 within the ranges <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, <math>3\text{ k}\Omega &lt; R2 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 24.</p> <p>Fig. 24 Frequency characteristic of VCO operating with offset: <math>f_o</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	PC1, PC2	<p><b>Selection of R1, R2 and C1</b></p> <p>Given <math>f_o</math> and <math>f_L</math>, determine the value of product <math>R1C1</math> by using Fig. 29.            Calculate <math>f_{off}</math> from the equation <math>f_{off} = f_o - 4.3f_L</math>.            Obtain the values of C1 and R2 by using Fig. 28.            Calculate the value of R1 from the value of C1 and the product <math>R1C1</math>.</p>

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG <sub>IN</sub> input	PC1	VCO adjusts to $f_o$ with $\phi_{\text{DEMOUT}} = 90^\circ$ and $V_{\text{VCOIN}} = 1/2 V_{\text{CC}}$ (see Fig. 6).
	PC2	VCO adjusts to $f_o$ with $\phi_{\text{DEMOUT}} = -360^\circ$ and $V_{\text{VCOIN}} = 0 \text{ V}$ (see Fig. 8).
PLL frequency capture range	PC1, PC2	<p><b>Loop filter component selection</b></p> <p>(a) <math>\tau = R3 \times C2</math>      (b) amplitude characteristic      (c) pole-zero diagram</p> <p>A small capture range (<math>2f_c</math>) is obtained if <math>\tau &gt; 2f_c \approx 1/\pi\sqrt{2\pi f_L/\tau}</math>.</p> <p>Fig. 25 Simple loop filter for PLL without offset.</p>
		<p>(a) <math>\tau_1 = R3 \times C2;</math> <math>\tau_2 = R4 \times C2;</math> <math>\tau_3 = (R3 + R4) \times C2</math>      (b) amplitude characteristic      (c) pole-zero diagram</p> <p>Fig. 26 Simple loop filter for PLL with offset.</p>
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$ , large ripple content at $\phi_{\text{DEMOUT}} = 90^\circ$
	PC2	$f_r = f_i$ , small ripple content at $\phi_{\text{DEMOUT}} = 0^\circ$

APPLICATION INFORMATION (Cont'd)



7Z96057

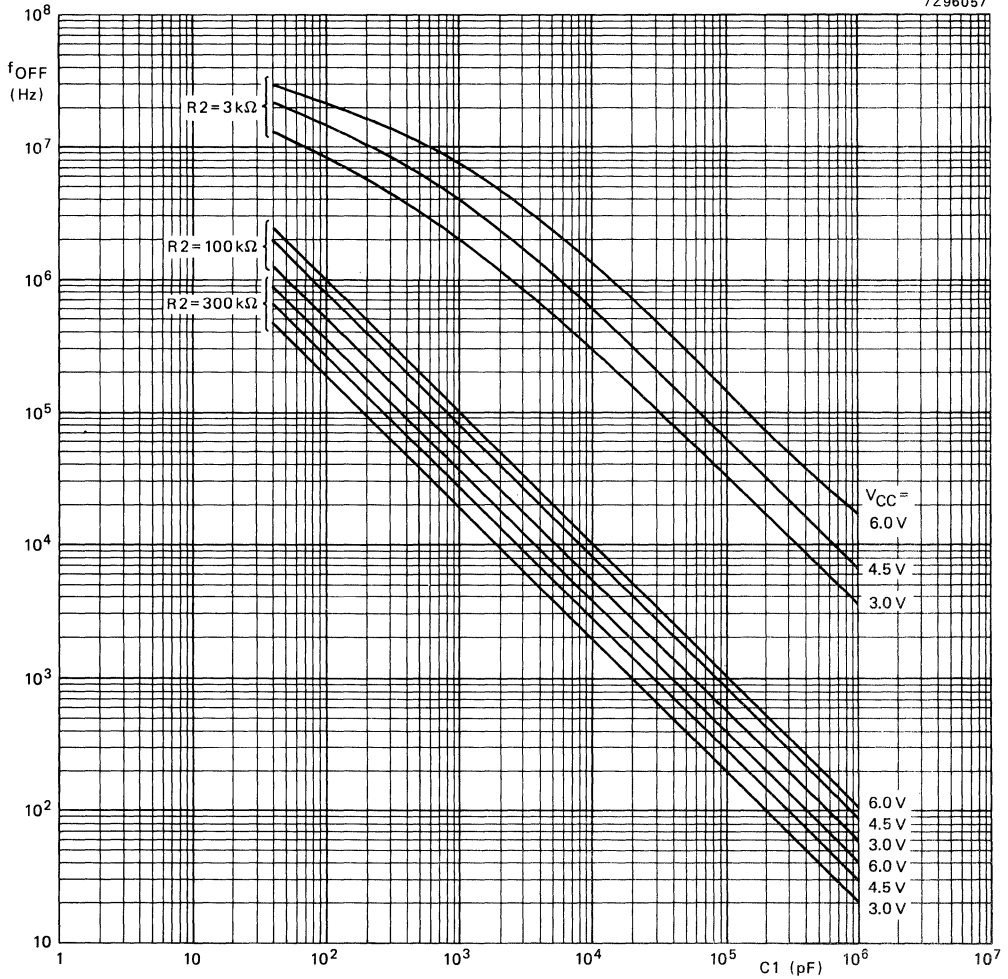
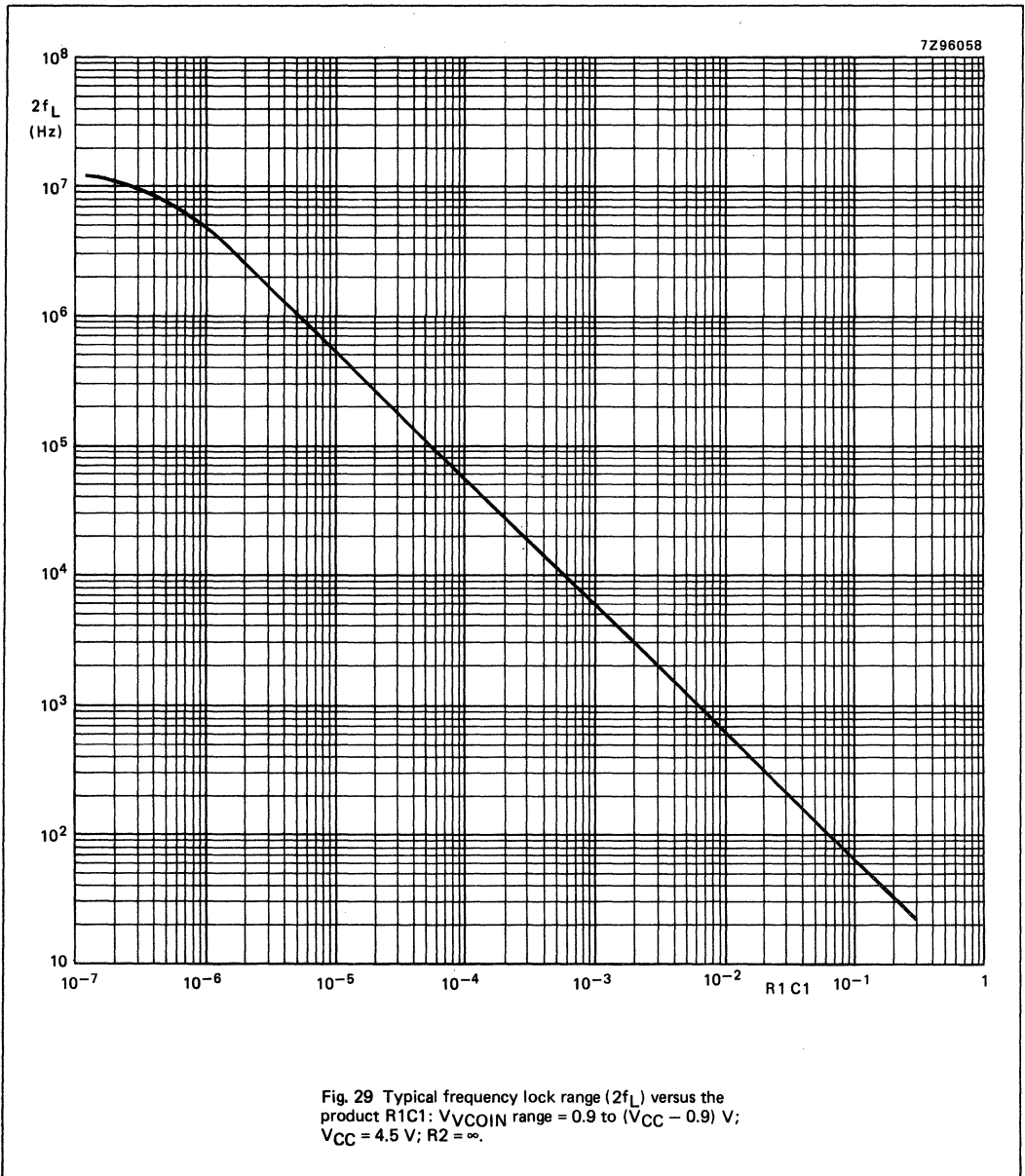


Fig. 28 Typical value of frequency offset as a function of  $C1$ :  $R1 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ ;  $INH = GND$ ;  $T_{amb} = 25^\circ\text{C}$ .

APPLICATION INFORMATION (Cont'd)



# DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

PC74HC/HCT40102

MSI

## 8-BIT SYNCHRONOUS BCD DOWN COUNTER

### FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- I<sup>2</sup>C category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT40102 are high-speed Si-gate CMOS devices and are pin compatible with the "40102" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT40102 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40102" is configured as two cascaded 4-bit BCD counters and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output (TC) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input (TE) is HIGH. The terminal count output (TC) goes LOW when the count reaches zero if TE is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input (PE) is LOW, data at the jam input (P<sub>0</sub> to P<sub>7</sub>) is clocked into the counter on the next positive-going clock transition regardless of the state of TE.

When the asynchronous preset enable input (PL) is LOW, data at the jam input (P<sub>0</sub> to P<sub>7</sub>) is asynchronously forced into the counter regardless of the state of PE, TE, or CP. The jam inputs (P<sub>0</sub> to P<sub>7</sub>) represent two 4-bit BCD words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			PL	PCD	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	24	26	ns
f <sub>max</sub>	maximum clock frequency		33	33	MHz
C <sub>i</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per counter	notes 1 and 2	25	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>i</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>i</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40102P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT40102T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	MR	asynchronous master reset input (active LOW)
3	TE	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P <sub>0</sub> to P <sub>7</sub>	jam inputs
8	GND	ground (0 V)
9	PL	asynchronous preset enable input (active LOW)
14	TC	terminal count output (active LOW)
15	PE	synchronous preset enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

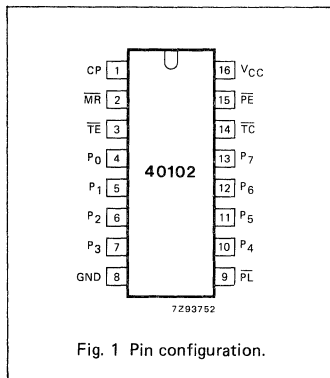


Fig. 1 Pin configuration.

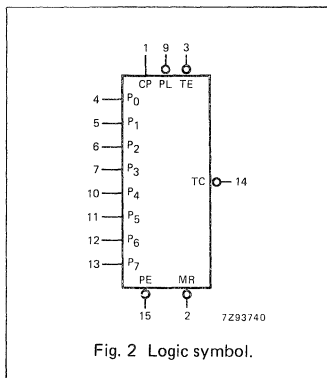


Fig. 2 Logic symbol.

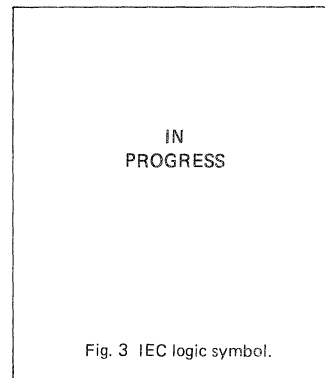


Fig. 3 IEC logic symbol.



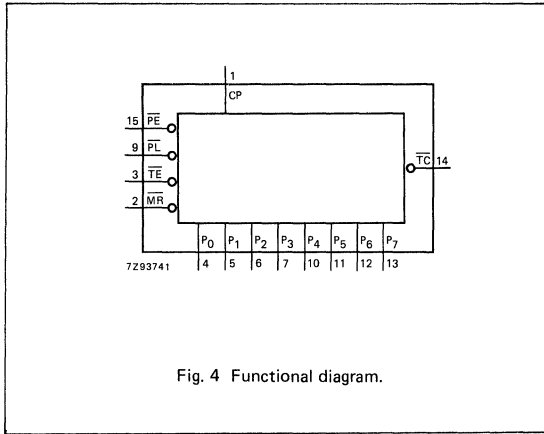


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

When the master reset input ( $\overline{MR}$ ) is LOW, the counter is asynchronously cleared to its maximum count (decimal 99) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except  $\overline{TE}$  are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 clock pulses long.

The "40102" may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either a synchronous or ripple mode.

**APPLICATIONS**

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

**FUNCTION TABLE**

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X	asynchronous	preset on next LOW-to-HIGH clock transition
H	L	X	X		preset asynchronously
L	X	X	X		clear to maximum count

**Notes to function table**

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P<sub>7</sub>, LSD = P<sub>0</sub>.

H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care

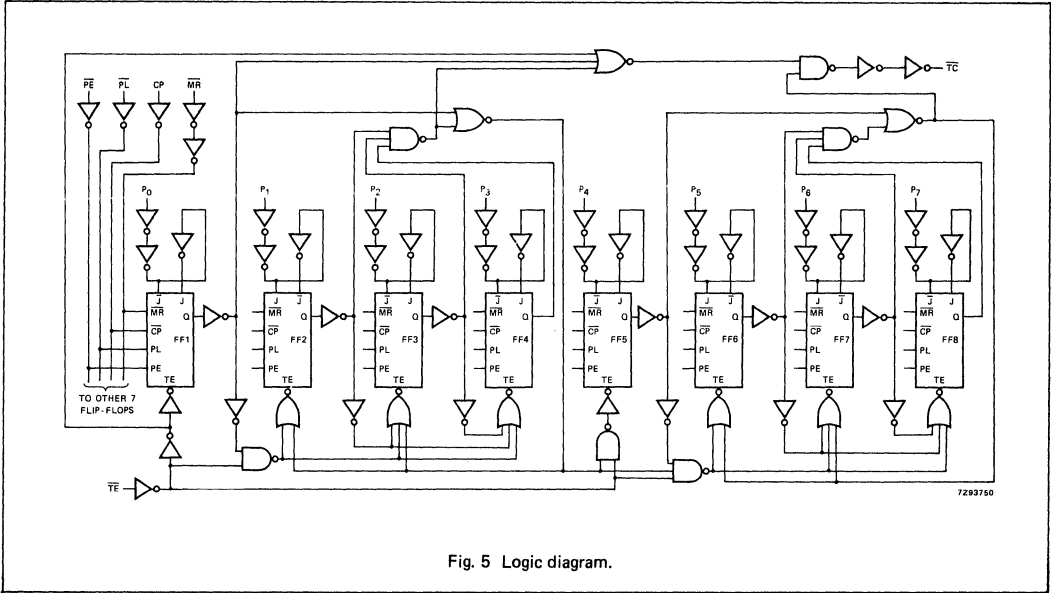


Fig. 5 Logic diagram.

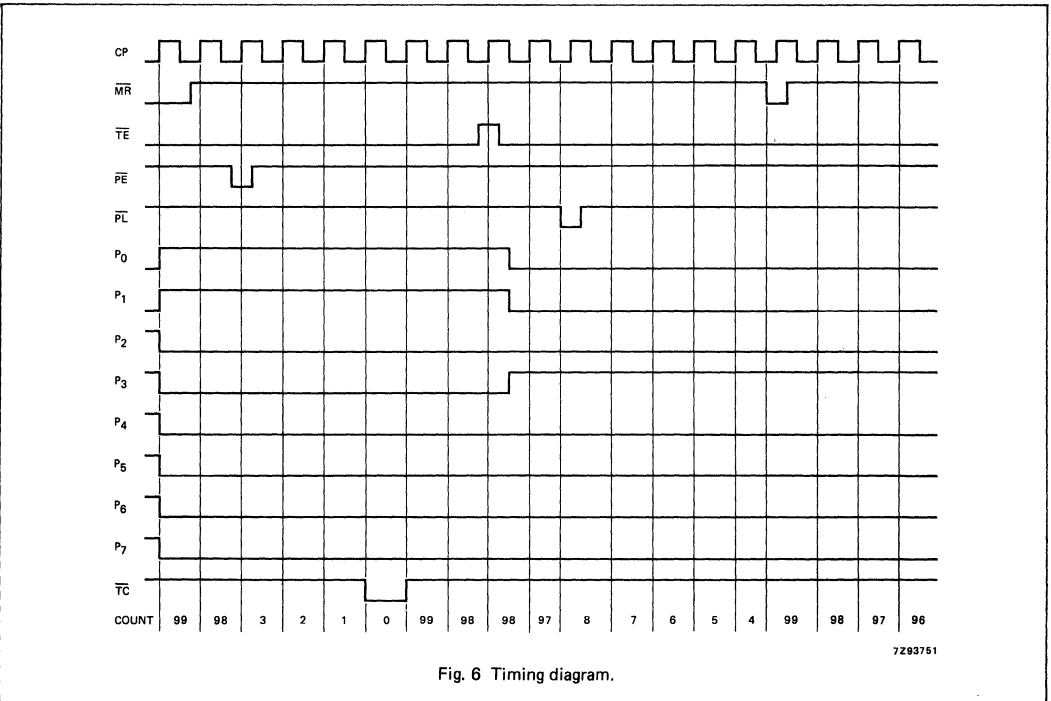


Fig. 6 Timing diagram.

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC			300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay TE to TC			200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to TC			275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC			275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time			75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs. 7 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW	165 33 28			205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	master reset pulse width LOW	150 30 26			190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	preset enable pulse width P <sub>L</sub> ; LOW	125 25 21			155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time MR to CP	50 10 9			65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time P <sub>E</sub> to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time TE to CP	175 35 30			220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time P <sub>n</sub> to CP	100 20 17			125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time P <sub>E</sub> to CP	0 0 0			0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

## AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HC									$V_{CC}$ V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_h$	hold time $\overline{TE}$ to CP	0			0			0		ns	2.0 4.5 6.0	Fig. 11
$t_h$	hold time $P_n$ to CP	5			5			5		ns	2.0 4.5 6.0	Fig. 12
$f_{max}$	maximum clock pulse frequency	3			2.4			2.0		MHz	2.0 4.5 6.0	Fig. 7
		15			12			10				
		18			14			12				

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 $I_{CC}$  category: MSI

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.  
To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP, $\overline{PE}$	1.50
$\overline{MR}$	1.00
TE	0.80
$P_n$	0.25

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

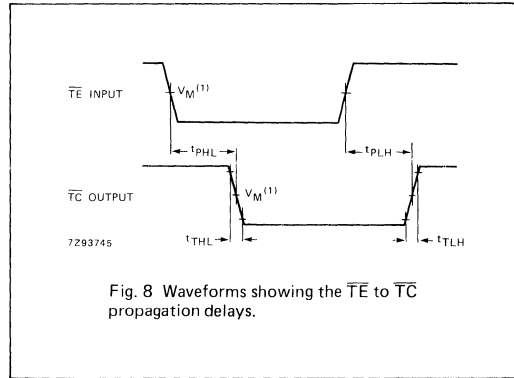
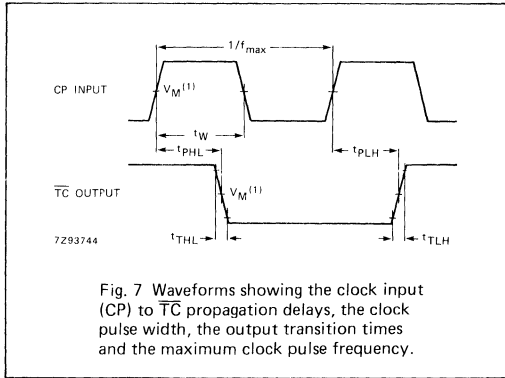
SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/$ $t_{PLH}$	propagation delay CP to TC			70		87		105		ns	4.5	Fig. 7
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{TE}$ to TC			50		63		75		ns	4.5	Fig. 8
$t_{PHL}/$ $t_{PLH}$	propagation delay $\overline{PL}$ to TC			60		75		90		ns	4.5	Fig. 9
$t_{PHL}$	propagation delay MR to TC			60		75		90		ns	4.5	Fig. 9
$t_{THL}/$ $t_{TLH}$	output transition time			15		19		22		ns	4.5	Figs. 7 and 8

## AC CHARACTERISTICS FOR 74 HCT (Cont'd)

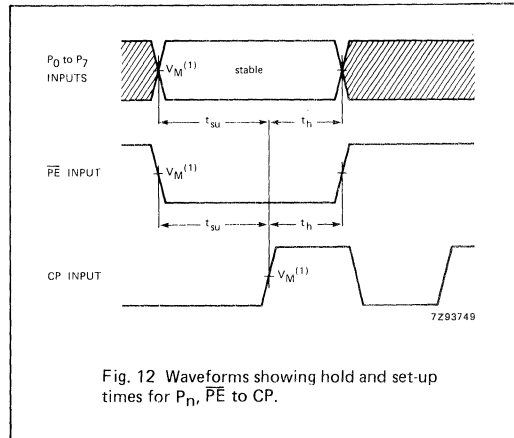
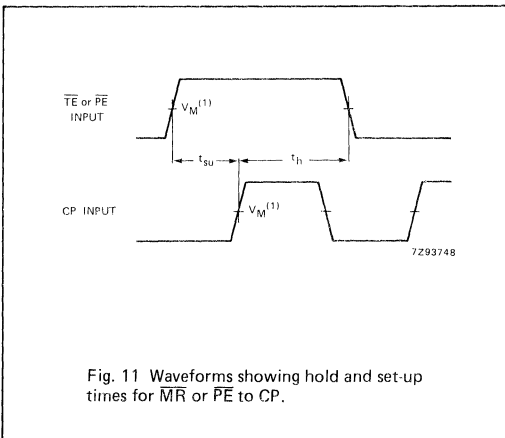
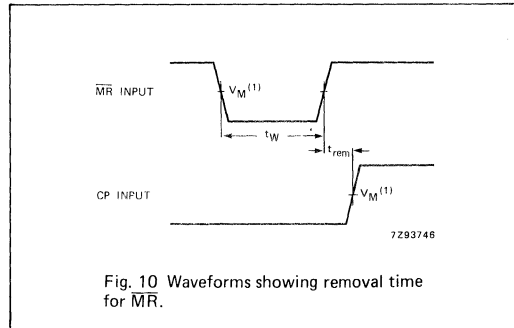
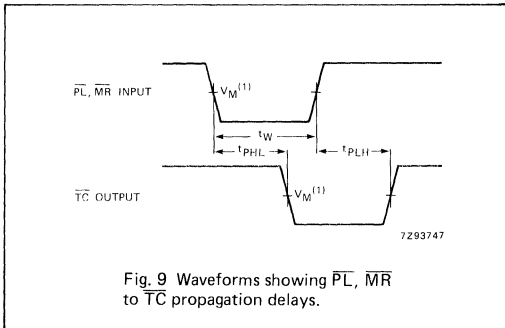
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_W$	clock pulse width HIGH or LOW	35			44		53		ns	4.5	Fig. 7
$t_W$	master reset pulse width LOW	40			50		60		ns	4.5	Fig. 9
$t_W$	preset enable pulse width PL; LOW	38			48		57		ns	4.5	Fig. 9
$t_{rem}$	removal time MR to CP	10			13		15		ns	4.5	Fig. 10
$t_{su}$	set-up time PE to CP	24			30		36		ns	4.5	Fig. 11
$t_{su}$	set-up time TE to CP	40			50		60		ns	4.5	Fig. 11
$t_{su}$	set-up time $P_n$ to CP	20			25		30		ns	4.5	Fig. 12
$t_h$	hold time PE to CP	0			0		0		ns	4.5	Fig. 11
$t_h$	hold time TE to CP	0			0		0		ns	4.5	Fig. 11
$t_h$	hold time $P_n$ to CP	5			5		5		ns	4.5	Fig. 12
$f_{max}$	maximum clock pulse frequency	14			11		9		MHz	4.5	Fig. 7

AC WAVEFORMS



DEVELOPMENT DATA



Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND}$  to  $V_{CC}$ .  
HCT :  $V_M = 1.3\text{ V}$ ;  $V_I = \text{GND}$  to  $3\text{ V}$ .

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.



## 8-BIT SYNCHRONOUS BINARY DOWN COUNTER

### FEATURES

- Cascadable
- Synchronous or asynchronous preset
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output (TC) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input (TE) is HIGH. The terminal count output (TC) goes LOW when the count reaches zero if TE is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input (PE) is LOW, data at the jam input (P<sub>0</sub> to P<sub>7</sub>) is clocked into the counter on the next positive-going clock transition regardless of the state of TE.

When the asynchronous preset enable input (PL) is LOW, data at the jam input (P<sub>0</sub> to P<sub>7</sub>) is asynchronously forced into the counter regardless of the state of PE, TE, or CP. The jam inputs (P<sub>0</sub> to P<sub>7</sub>) represent a single 8-bit binary word.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	29	30	ns
f <sub>max</sub>	maximum clock frequency		32	31	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per counter	notes 1 and 2	24	27	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

### Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz                    V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40103P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT40103T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	M $\bar{R}$	asynchronous master reset input (active LOW)
3	T $\bar{E}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P <sub>0</sub> to P <sub>7</sub>	jam inputs
8	GND	ground (0 V)
9	P $\bar{L}$	asynchronous preset enable input (active LOW)
14	T $\bar{C}$	terminal count output (active LOW)
15	P $\bar{E}$	synchronous preset enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage

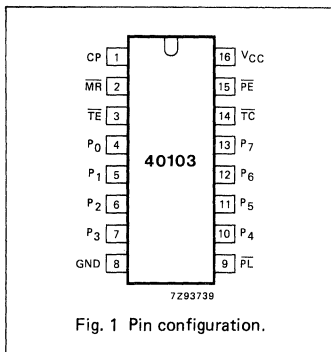


Fig. 1 Pin configuration.

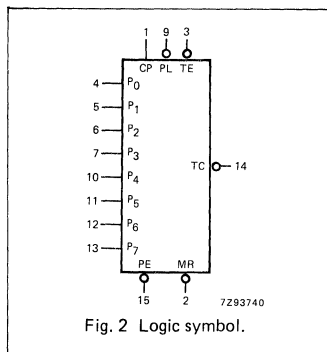


Fig. 2 Logic symbol.

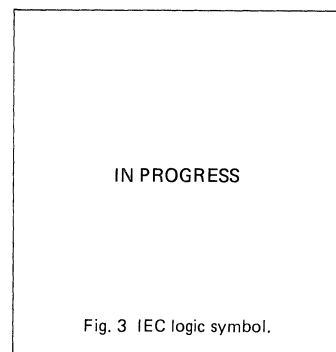


Fig. 3 IEC logic symbol.



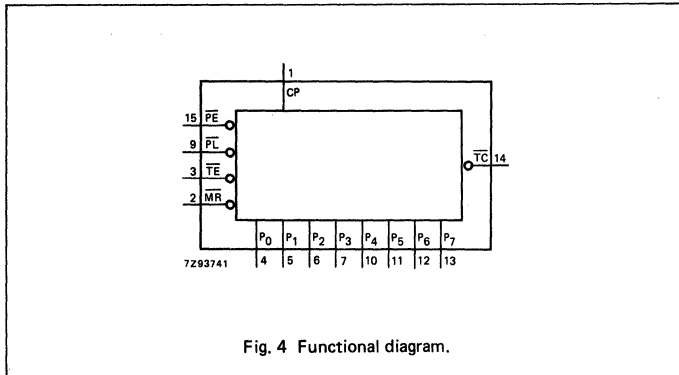


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

When the master reset input ( $\overline{MR}$ ) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except  $\overline{TE}$  are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

The "40103" may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either a synchronous or ripple mode.

**APPLICATIONS**

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters

**FUNCTION TABLE**

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to-HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

**Notes to function table**

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P7, LSD = P0.

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

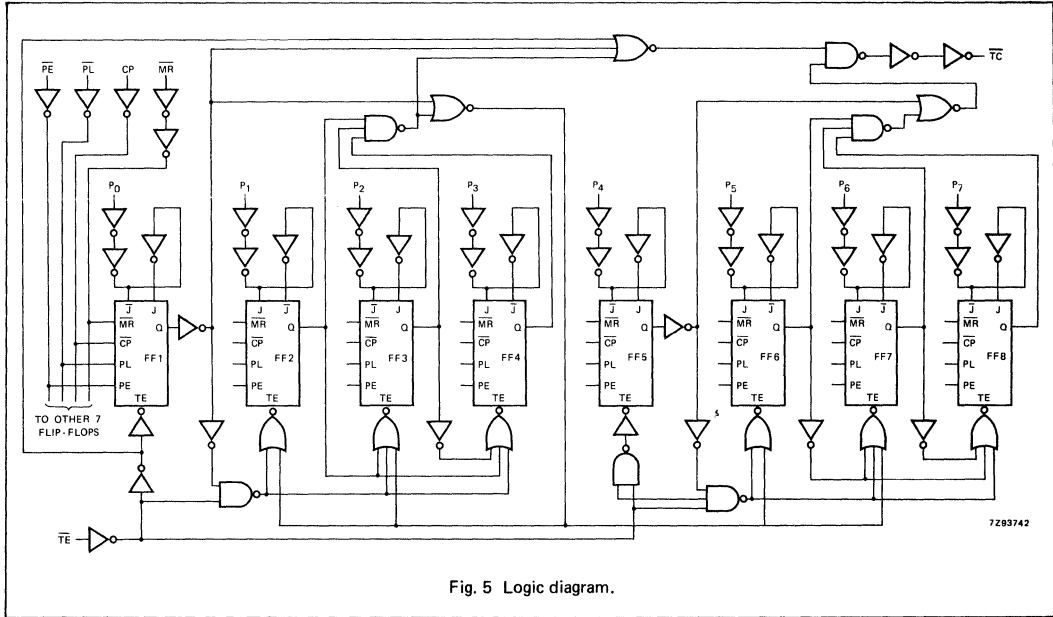


Fig. 5 Logic diagram.

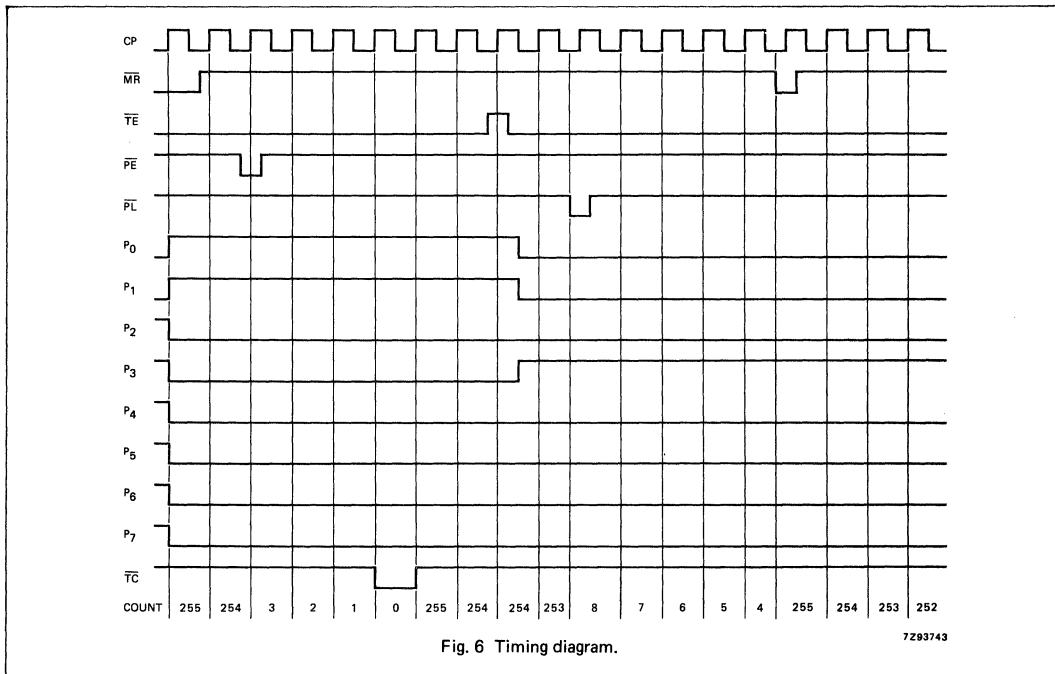


Fig. 6 Timing diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{TC}$		96 35 28	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{TE}$ to $\overline{TC}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{PL}$ to $\overline{TC}$		102 37 30	315 63 53		395 79 40		475 95 81	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay $\overline{MR}$ to $\overline{TC}$		83 30 24	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs. 7 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW	165 33 28	33 12 10		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t <sub>W</sub>	master reset pulse width LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	preset enable pulse width $\overline{PL}$ ; LOW	125 25 21	33 12 10		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t <sub>rem</sub>	removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time PE to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time $\overline{TE}$ to CP	150 30 26	44 16 13		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t <sub>su</sub>	set-up time P <sub>n</sub> to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time $\overline{PE}$ to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

## AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>h</sub>	hold time T <sub>E</sub> to CP	0	-30		0		0		ns	2.0 4.5 6.0	Fig. 11
t <sub>h</sub>	hold time P <sub>N</sub> to CP	0	-17		0		0		ns	2.0 4.5 6.0	Fig. 12
f <sub>max</sub>	maximum clock pulse frequency	3	10		2.4		2.0		MHz	2.0 4.5 6.0	Fig. 7
		15	29		12		10				
		18	35		14		12				

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP, $\overline{PE}$	1.50
MR	1.00
TE	0.80
P <sub>n</sub>	0.25

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		35	60		75		90	ns	4.5	Fig. 7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay TE to TC		23	40		50		60	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{PL}$ to TC		44	75		94		112	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay MR to TC		29	55		69		83	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Figs. 7 and 8
t <sub>W</sub>	clock pulse width HIGH or LOW	33	10		41		50		ns	4.5	Fig. 7
t <sub>W</sub>	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig. 9
t <sub>W</sub>	preset enable pulse width $\overline{PL}$ ; LOW	38	22		48		57		ns	4.5	Fig. 9
t <sub>rem</sub>	removal time MR to CP or $\overline{PL}$ to CP	10	1		13		15		ns	4.5	Fig. 10
t <sub>su</sub>	set-up time $\overline{PE}$ to CP	20	11		25		30		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time TE to CP	40	20		50		60		ns	4.5	Fig. 11
t <sub>su</sub>	set-up time P <sub>n</sub> to CP	20	11		25		30		ns	4.5	Fig. 12
t <sub>h</sub>	hold time $\overline{PE}$ to CP	2	-3		2		2		ns	4.5	Fig. 11

## AC CHARACTERISTICS FOR 74HCT (Cont'd)

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>h</sub>	hold time T <sub>E</sub> to CP	0	-10		0		0		ns	4.5	Fig. 11
t <sub>h</sub>	hold time P <sub>n</sub> to CP	0	-5		0		0		ns	4.5	Fig. 12
f <sub>max</sub>	maximum clock pulse frequency	15	28		12		10		MHz	4.5	Fig. 7

AC WAVEFORMS

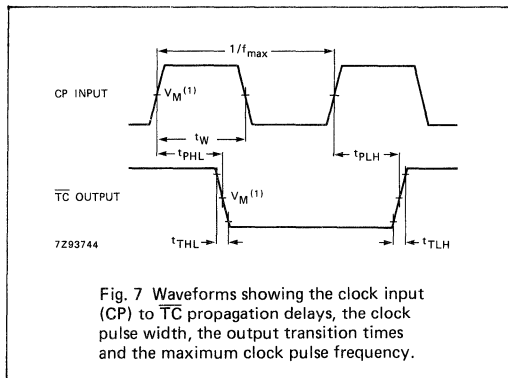


Fig. 7 Waveforms showing the clock input (CP) to TC propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

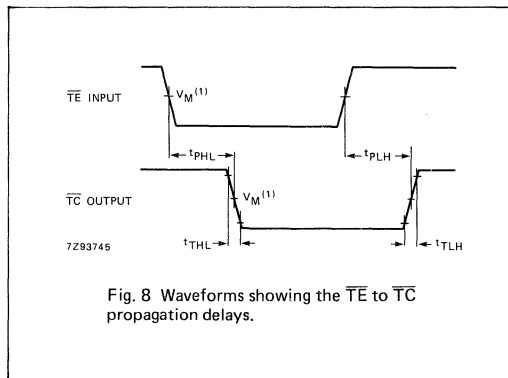


Fig. 8 Waveforms showing the TE to TC propagation delays.

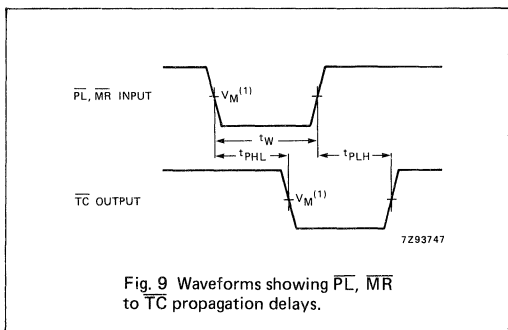


Fig. 9 Waveforms showing PL, MR to TC propagation delays.

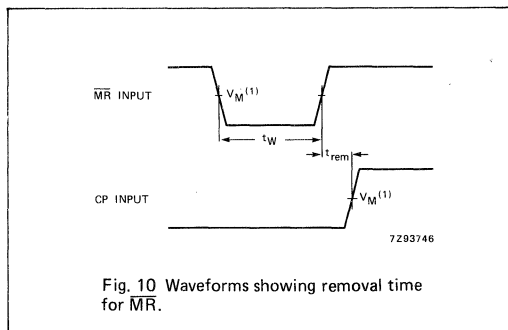


Fig. 10 Waveforms showing removal time for MR.

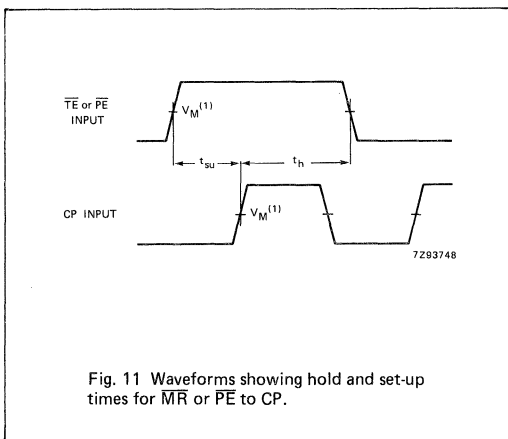


Fig. 11 Waveforms showing hold and set-up times for MR or PE to CP.

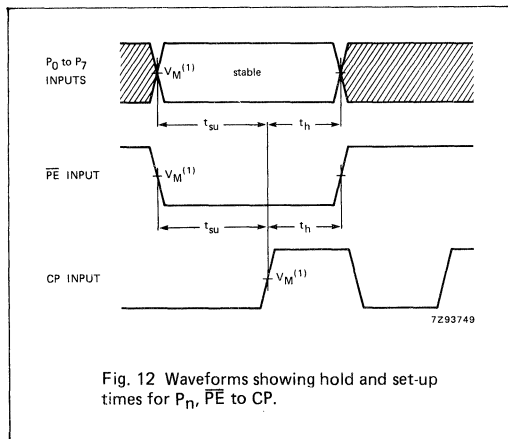


Fig. 12 Waveforms showing hold and set-up times for P<sub>0</sub>, PE to CP.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3V$ ;  $V_I = \text{GND to } 3V$ .

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

In the parallel-load mode (S<sub>0</sub> and S<sub>1</sub> are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D<sub>SR</sub>) and shift-left (D<sub>SL</sub>) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S<sub>0</sub> and S<sub>1</sub>) LOW and clocking the register.

When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

APPLICATIONS

- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	13	15	ns
f <sub>max</sub>	maximum clock frequency		61	51	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	75	75	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

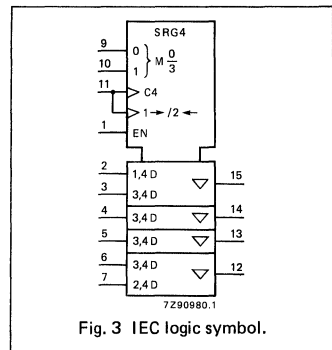
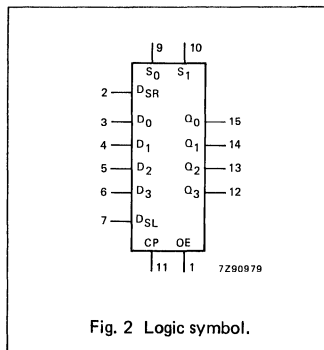
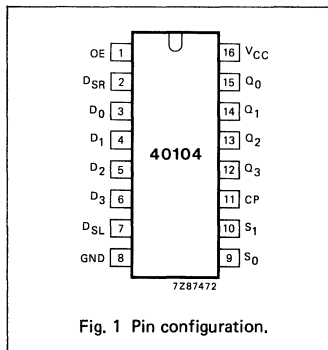
ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40104P: 16-lead DIL; plastic (SOT-38Z).

PC74HC/HCT40104T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D <sub>SR</sub>	serial data shift-right input
3, 4, 5, 6	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
7	D <sub>SL</sub>	serial data shift-left input
8	GND	ground (0 V)
9, 10	S <sub>0</sub> , S <sub>1</sub>	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q <sub>0</sub> to Q <sub>3</sub>	3-state parallel outputs
16	V <sub>CC</sub>	positive supply voltage







**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	2 2 2	-14 -3 -4		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	19 56 67		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

input	unit load coefficient
D <sub>0</sub> to D <sub>3</sub>	0.35
DSR, DSL	0.35
CP	0.35
S <sub>0</sub> , S <sub>1</sub>	0.70
OE	1.40

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	34		43		51	ns	4.5	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		12	30		38		45	ns	4.5	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		21	35		44		53	ns	4.5	Fig. 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig. 6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 6
t <sub>su</sub>	set-up time D <sub>n</sub> , DSR, DSL to CP	16	8		20		24		ns	4.5	Fig. 8
t <sub>su</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	20	9		25		30		ns	4.5	Fig. 8
t <sub>h</sub>	hold time D <sub>n</sub> , DSR, DSL to CP	2	-3		2		2		ns	4.5	Fig. 8
t <sub>h</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	2	-3		2		2		ns	4.5	Fig. 8
f <sub>max</sub>	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

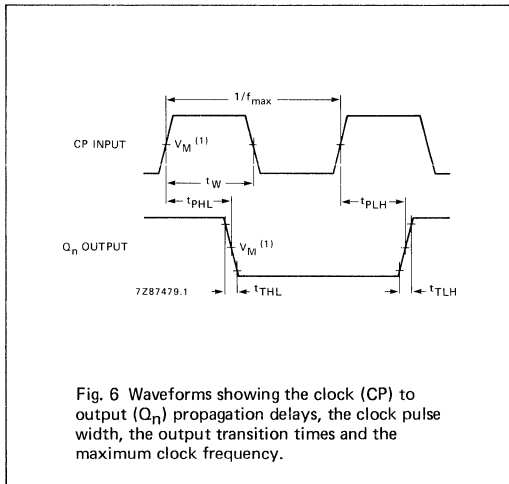


Fig. 6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

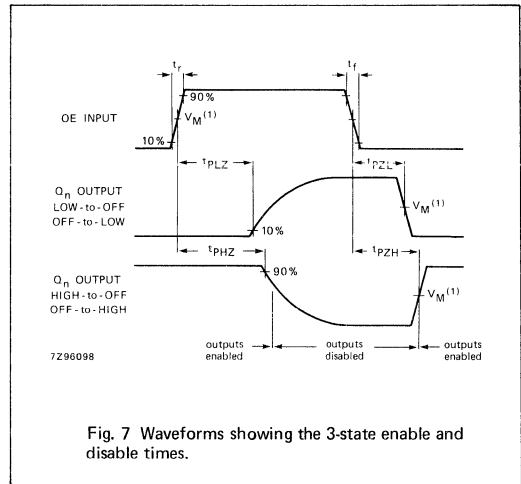


Fig. 7 Waveforms showing the 3-state enable and disable times.

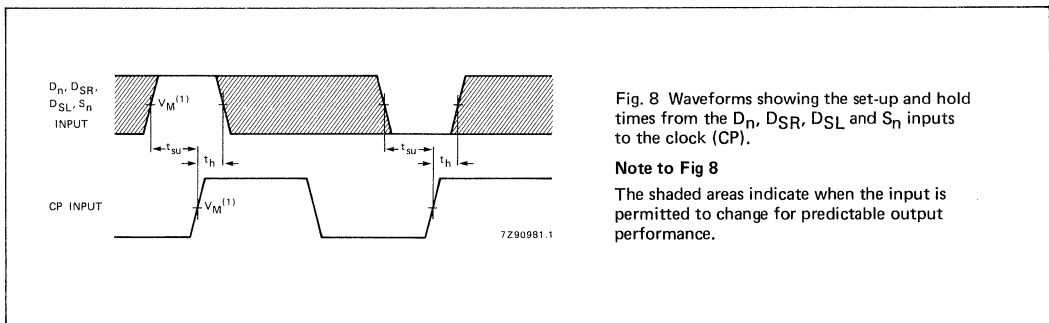


Fig. 8 Waveforms showing the set-up and hold times from the  $D_n, D_{SR}, D_{SL}$  and  $S_n$  inputs to the clock (CP).

Note to Fig 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .

HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .



### 4-BIT X 16-WORD FIFO REGISTER

#### FEATURES

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT40105 are high-speed Si-gate CMOS devices and are pin compatible with the "40105" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7. The 74HC/HCT40105 are first-in/first-out (FIFO) "elastic" storage registers that can store sixteen 4-bit words. The "40105" is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems. Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (data-in ready output - DIR) indicates if the FIFO is full, and the status of the last flip-flop (data-out ready output - DOR) indicates if the FIFO

*(continued on next page)*

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to DIR, DOR S $\bar{O}$ to Q <sub>n</sub>	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	16 37	15 35	ns ns
t <sub>PHL</sub>	propagation delay SI to DIR S $\bar{O}$ to DOR		16 17	18 18	ns ns
f <sub>max</sub>	maximum clock frequency		33	31	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	134	145	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

#### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
 f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

#### ORDERING INFORMATION/PACKAGE OUTLINES

PC74HC/HCT40105P: 16-lead DIL; plastic (SOT-38Z).  
 PC74HC/HCT40105T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	output enable input (active LOW)
2	DIR	data-in ready output
3	SI	shift in input (LOW to HIGH, edge-triggered)
4, 5, 6, 7	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
8	GND	ground (0 V)
9	MR	asynchronous master reset input (active HIGH)
13, 12, 11, 10	Q <sub>0</sub> to Q <sub>3</sub>	3-state data outputs
14	DOR	data-out ready output
15	S $\bar{O}$	shift-out input (HIGH to LOW, edge-triggered)
16	V <sub>CC</sub>	positive supply voltage

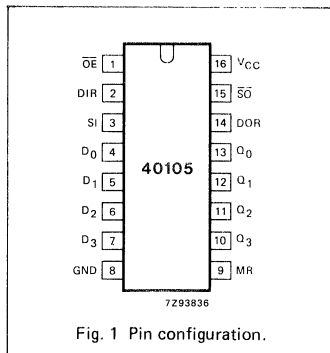


Fig. 1 Pin configuration.

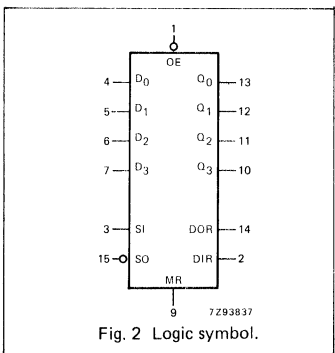


Fig. 2 Logic symbol.

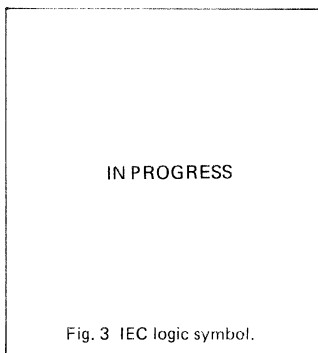


Fig. 3 IEC logic symbol.

**GENERAL DESCRIPTION (Cont'd)**

contains data. As the earliest data is removed from the bottom of the data stack (output end), all data entered later will automatically ripple toward the output.

**Loading data**

Data can be entered whenever the DIR flag is HIGH, by a LOW-to-HIGH transition on the shift-in input (SI). This input must go LOW momentarily before the next word is accepted by the FIFO. The DIR flag will go LOW momentarily, until the data has been transferred to the second location. The DIR flag remains LOW when all 16 word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes HIGH.

**Unloading data**

As soon as the first word has rippled to the output, the data out ready output (DOR) goes HIGH and data of the first word is available on the outputs.

Data of other words can be removed by a negative-going transition on the shift-out input (SO). This negative going transition causes the DOR signal to go LOW, while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go HIGH again signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH. If during unloading SI is HIGH, data on the data input of the FIFO is entered in the first location.

**Master reset**

A HIGH on the master reset input (MR) sets all the control logic marker bits to "0". DOR goes LOW and DIR goes HIGH. The contents of the data register are not changed but will be superseded when the first word is loaded. Thus MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D<sub>0</sub> to D<sub>3</sub>) is immediately moved into the first location upon completion of the reset process.

**3-state outputs**

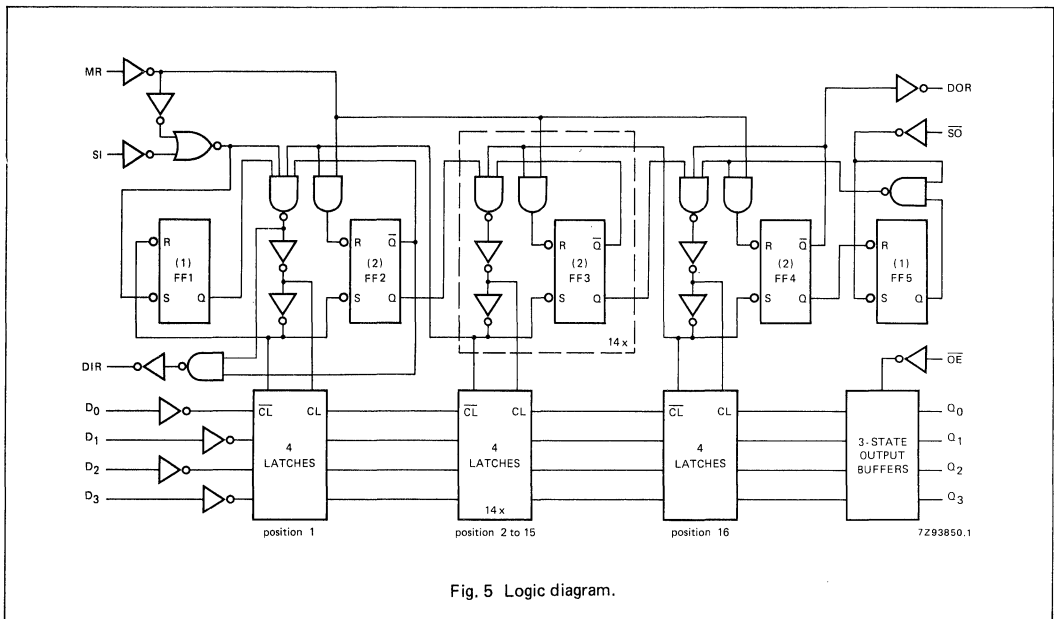
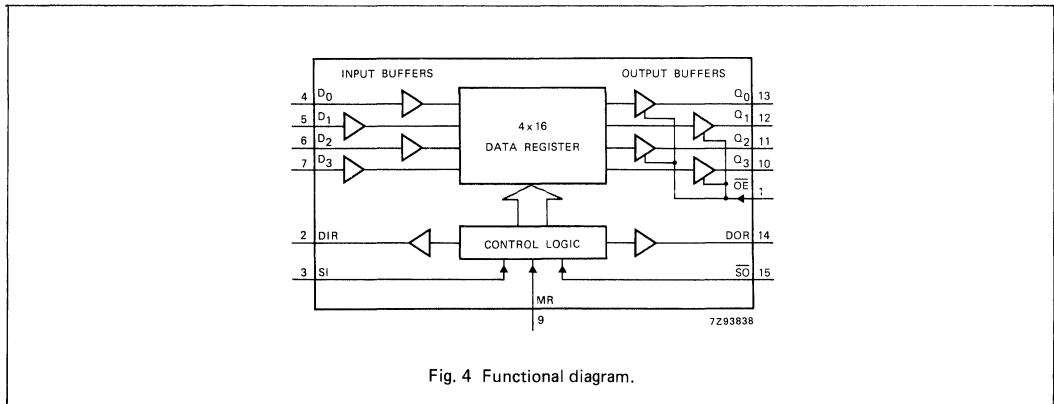
In order to facilitate data busing, 3-state outputs (Q<sub>0</sub> to Q<sub>3</sub>) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the 3-state control flag (output enable input - OE) forces the outputs into the high-impedance OFF-state mode.

**Cascading**

The "40105" can be cascaded to form longer registers simply by connecting the DIR outputs to the SO inputs and the DOR outputs to the SI inputs. In the cascading mode, a master reset pulse must be applied after the supply voltage is turned on. For words wider than 4 bits, the DIR and DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expansion occurs in both directions (see Figs. 6 and 7).

**APPLICATIONS**

- Bit-rate smoothing
- CPU/terminal buffering
- Data communications
- Peripheral buffering
- Line printer input buffers
- Auto-diallers
- CRT buffer memories
- Radar data acquisition

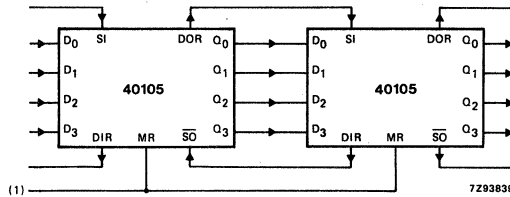


**Notes to Fig. 5**

(see control flip-flops)

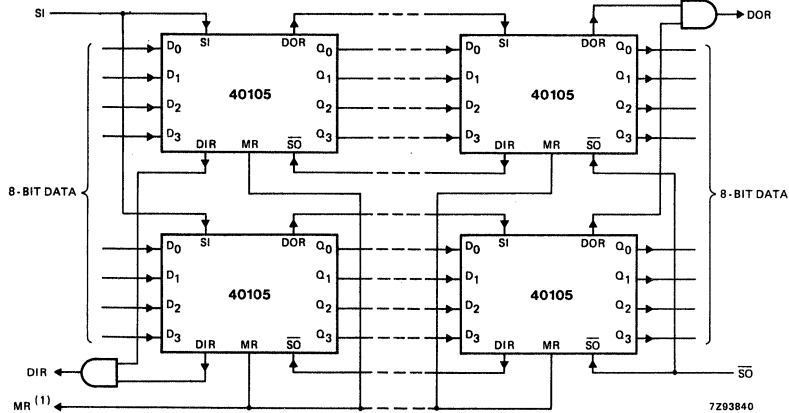
- (1) LOW on  $\bar{S}$  input of FF1 and FF5 will set Q output to HIGH independent of state on  $\bar{R}$  input.
- (2) LOW on  $\bar{R}$  input of FF2 and FF3 will set Q output to LOW independent of state on  $\bar{S}$  input.





(1) Master reset pulse must be applied when cascading by 16 n-bits.

Fig. 6 Expansion; 4-bits wide-by-16 n-bits long.



(1) Master reset pulse must be applied when cascading by 16 n-bits.

Fig. 7 Expansion; 8-bits wide-by-16 n-bits long.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to DIR, DOR		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub>	propagation delay SI to DIR		52 19 15	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 9
t <sub>PHL</sub>	propagation delay S <sub>O</sub> to DOR		55 20 16	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>O</sub> to Q <sub>N</sub>		116 42 34	400 80 68		500 100 85		600 120 102	ns	2.0 4.5 6.0	Fig. 11
t <sub>PLH</sub>	propagation delay/ripple through delay SI to DOR		564 205 165	2000 400 340		2500 500 425		3000 600 510	ns	2.0 4.5 6.0	Fig. 12
t <sub>PLH</sub>	propagation delay/ripple through delay S <sub>O</sub> to DIR		701 255 204	2500 500 425		3125 625 532		3750 750 638	ns	2.0 4.5 6.0	Fig. 13
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 11
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable OE to Q <sub>N</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 14
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>N</sub>		41 15 12	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 14
t <sub>W</sub>	SI pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9
t <sub>W</sub>	S <sub>O</sub> pulse width HIGH or LOW	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 10
t <sub>W</sub>	DIR pulse width HIGH or LOW	220 44 37	58 21 17		275 55 47		330 66 56		ns	2.0 4.5 6.0	Fig. 9

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS	
		74HC							$V_{CC}$ V	WAVEFORMS
		+25			-40 to +85		-40 to +125			
		min.	typ.	max.	min.	max.	min.		max.	
$t_W$	DOR pulse width HIGH or LOW	220 44 37	55 20 16		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 10
$t_W$	MR pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig. 8
$t_{rem}$	removal time MR to SI	50 10 9	14 5 4		65 13 11		75 15 13	ns	2.0 4.5 6.0	Fig. 15
$t_{su}$	set-up time $D_n$ to SI	-5 -5 -5	-39 -14 -11		-5 -5 -5		-5 -5 -5	ns	2.0 4.5 6.0	Fig. 16
$t_h$	hold time $D_n$ to SI	125 25 21	44 16 13		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 16
$f_{max}$	maximum pulse frequency SI, $\overline{SO}$	3.0 15 18	10 30 36		2.4 12 14		2.0 10 12	MHz	2.0 4.5 6.0	Figs 9 and 10

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
OE	0.75
SI	0.40
D <sub>n</sub>	0.30
MR	1.50
SO	0.40

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay MR to DIR, DOR		18	35		44		53	ns	4.5	Fig. 8
t <sub>PHL</sub>	propagation delay SI to DIR		21	42		53		63	ns	4.5	Fig. 9
t <sub>PHL</sub>	propagation delay SO to DOR		20	42		53		63	ns	4.5	Fig. 10
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SO to Q <sub>n</sub>		40	80		100		120	ns	4.5	Fig. 11
t <sub>PLH</sub>	propagation delay/ripple through delay SI to DOR		188	400		500		600	ns	4.5	Fig. 12
t <sub>PLH</sub>	propagation delay/ripple through delay SO to DIR		244	500		625		750	ns	4.5	Fig. 13
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig. 11
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		18	35		44		53	ns	4.5	Fig. 14
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		15	30		38		45	ns	4.5	Fig. 14
t <sub>W</sub>	SI pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig. 9
t <sub>W</sub>	SO pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 10

## AC CHARACTERISTICS FOR 74HCT (Cont'd)

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>W</sub>	DIR pulse width HIGH or LOW	40	20		50		60	ns	4.5	Fig. 9	
t <sub>W</sub>	DOR pulse width HIGH or LOW	40	19		50		60	ns	4.5	Fig. 10	
t <sub>W</sub>	MR pulse width HIGH	16	7		20		24	ns	4.5	Fig. 8	
t <sub>rem</sub>	removal time MR to SI	15	7		19		22	ns	4.5	Fig. 15	
t <sub>su</sub>	set-up time D <sub>n</sub> to SI	-5	-14		-5		-5	ns	4.5	Fig. 16	
t <sub>h</sub>	hold time D <sub>n</sub> to SI	25	16		31		38	ns	4.5	Fig. 16	
f <sub>max</sub>	maximum pulse frequency SI, $\overline{S0}$	15	28		12		10	MHz	4.5	Figs 9 and 10	

AC WAVEFORMS

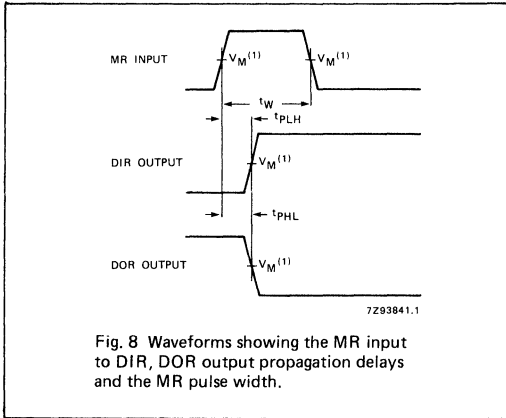


Fig. 8 Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

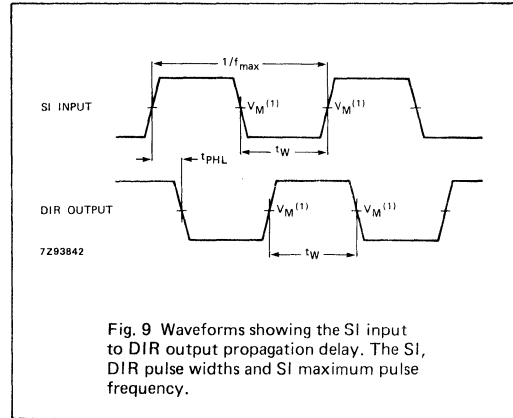


Fig. 9 Waveforms showing the SI input to DIR output propagation delay. The SI, DIR pulse widths and SI maximum pulse frequency.

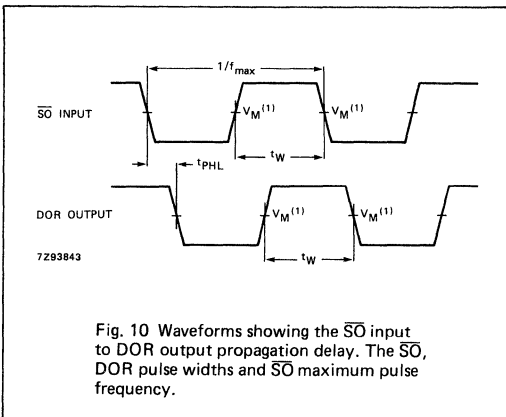


Fig. 10 Waveforms showing the  $\overline{S0}$  input to DOR output propagation delay. The  $\overline{S0}$ , DOR pulse widths and  $\overline{S0}$  maximum pulse frequency.

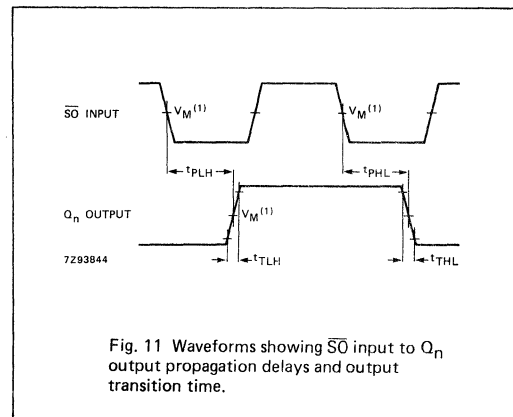


Fig. 11 Waveforms showing  $\overline{S0}$  input to  $Q_n$  output propagation delays and output transition time.

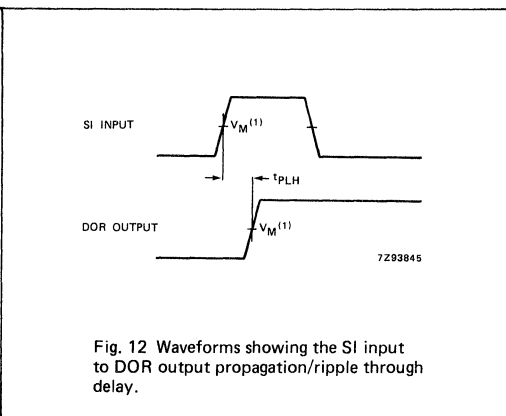


Fig. 12 Waveforms showing the SI input to DOR output propagation/ripple through delay.

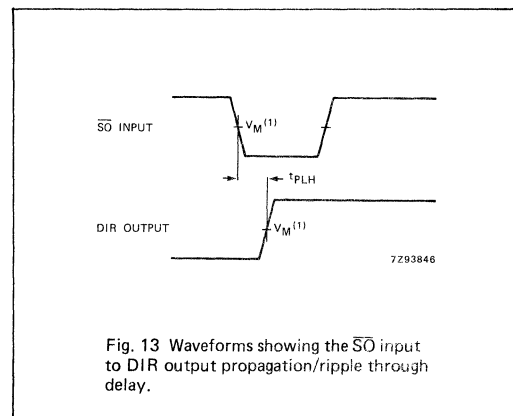


Fig. 13 Waveforms showing the  $\overline{S0}$  input to DIR output propagation/ripple through delay.

AC WAVEFORMS (Cont'd)

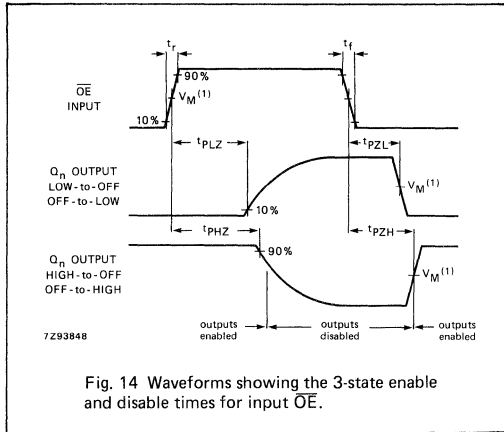


Fig. 14 Waveforms showing the 3-state enable and disable times for input  $\overline{OE}$ .

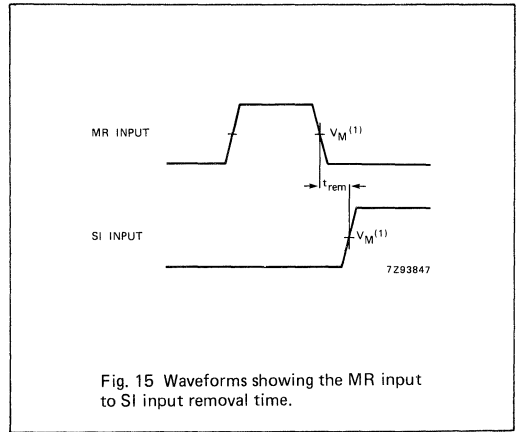


Fig. 15 Waveforms showing the MR input to SI input removal time.

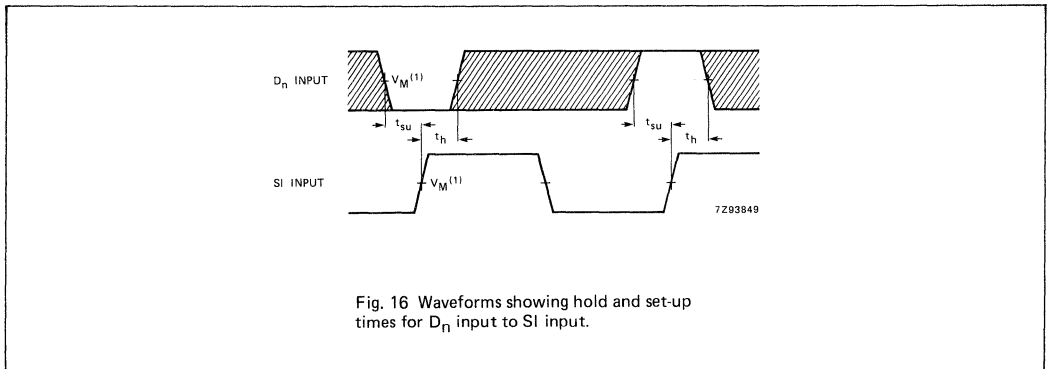


Fig. 16 Waveforms showing hold and set-up times for  $D_n$  input to SI input.

Note to Fig. 16

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

## APPLICATION NOTES

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## HANDLING PRECAUTIONS

### Electrostatic charges

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

### Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is  $1 \text{ k}\Omega$  to  $0,5 \text{ M}\Omega$  per  $\text{cm}^2$ . The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be earthed via a wrist strap and a resistor.
- All electrical equipment should be connected to the mains via an earth-leakage switch and the equipment cases should be earthed.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

### Receipt and storage

CMOS ICs are packed for despatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the task should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

## Assembly

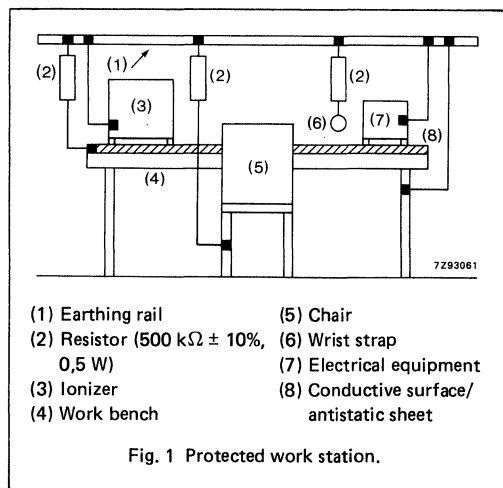
CMOS ICs must be removed from their protective packing with earthed component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.





## POWER SUPPLY LINE LAYOUT AND DECOUPLING RECOMMENDATIONS

Spikes due to output current switching and the charging and discharging of parasitic capacitance, are the two main sources of noise on the power lines of HCMOS logic systems. To minimize noise, the power supply should be decoupled. However, if switching speed is high, not only the voltage dips on the power lines must be considered but also the effects of  $di/dt$  radiation. Decoupling requirements are a balance between the precautions necessary to reduce the effects of these two phenomena.

The first requirement for minimizing noise is a well designed power distribution network. For instance, it is essential to have a good ground (GND) connection pattern on a pcb. Even the commonly used GND pattern shown in Fig.1 can cause problems. In Fig.1, an output from IC1 drives an input of IC2, and an output from IC3 drives an input of IC4. Since the signal paths between IC1 and IC2, and between IC3 and IC4 are not coupled, there should be no crosstalk between them. However, IC1 and IC3 share the hatched section of the GND comb, and when the output of IC1 switches, a spike could be generated on the GND of IC3. This could be transmitted to IC4 via the IC3-IC4 signal connection causing the output of IC4 to switch erroneously. If a double-sided board is used, it is therefore advisable to reduce the length of individual sections of the GND comb by installing links on the opposite side of the board as shown in Fig.2. This is especially important for boards on which high level currents are switched.

It is bad practice to use jumpers to connect GND/ $V_{CC}$  pins of ICs to pcb tracks (Fig.3). Jumpers are unlikely to be used on production boards, but they should not be used on prototype or one-off boards either because the inductance they introduce into the lines causes coupling between outputs. Printed connections should therefore be used to interconnect power tracks and IC pins. An even better solution is to use multi-layer boards so that individual layers can be used as a  $V_{CC}$  plane and a groundplane. The power supply can then be connected directly to the IC supply pins. Also, the inherent capacitance between the  $V_{CC}$  plane and the groundplane will reduce the amplitude of any high frequency noise on the power supply.

This inherent capacitance has the distinct advantage of being free from the inductance associated with discrete decoupling capacitors. A less expensive alternative to a multi-layer board is a multi-board which offers the same high frequency noise characteristics. With double-sided boards, it is not possible to dedicate a layer to a  $V_{CC}$  plane and a groundplane. Nevertheless, if at all possible, it is still best to have the  $V_{CC}$  and ground tracks on opposite sides of the board.

Connectors on any type of pcb should each have at least five ground pins to obtain good distribution of ground current.

The precautions outlined for ground tracks on the pcb are equally applicable to the power ( $V_{CC}$ ) lines.

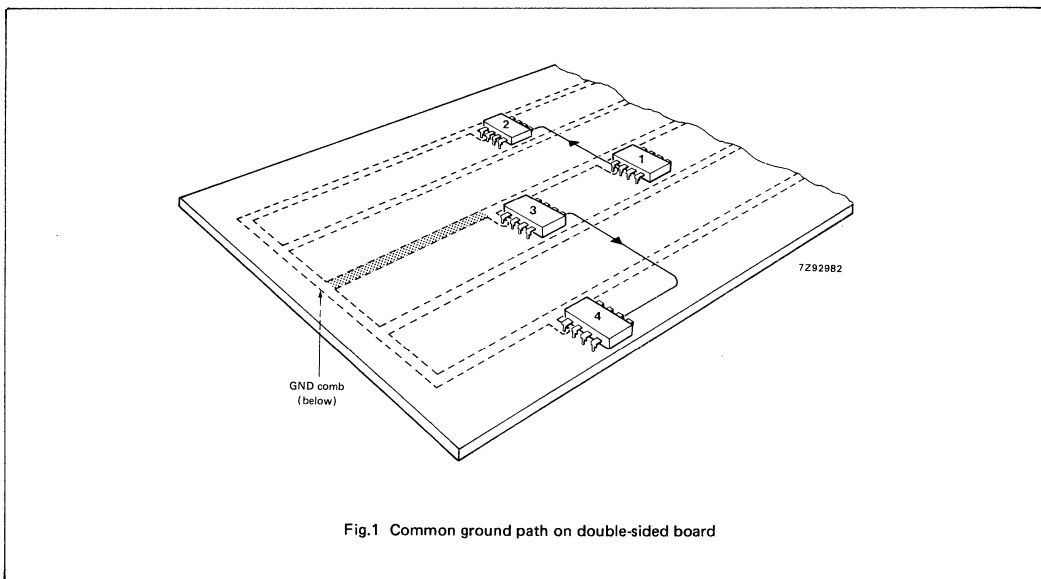


Fig.1 Common ground path on double-sided board

The wide HCMOS power supply range of 2 V to 6 V may suggest that voltage regulation is not necessary, but it must be remembered that supply voltage level variations will influence switching speed, noise immunity and power consumption. Supply voltage differences between ICs must also be avoided because a difference of as little as 0,5 V between power lines can cause unwanted effects. To isolate noise sources and avoid the use of a large voltage stabilizer with its heavy gauge (low impedance) wiring to each board, it is better to have a separate stabilizer for each board. However, care must be taken because a fault on a stabilizer for one board may be transmitted via the HCMOS input structure to other boards, possibly causing damage.

No matter how good the  $V_{CC}$  and GND connections are, all line inductance cannot be eliminated. This is where decoupling plays its part.

Ceramic capacitors are best for decoupling because they have very low series inductance. The advantage of using them will, however, be lost if they are connected too far from the IC. The inductance of the long tracks in conjunction with the capacitor will then form a very high-Q LC tuned-circuit, and the oscillations produced will have a worse effect than not having any decoupling at all. If it is impossible to make connections between decoupling capacitors and ICs shorter than 20 mm, then use several tracks connected in parallel and separated by at least one track-width (Fig.4). Some ceramic capacitors have preformed leads as shown in Fig.5(a). These leads introduce

unwanted inductance. It is better to use capacitors with straight leads mounted as shown in Fig.5(b).

In general, the minimum requirements for good decoupling are:

- one 47  $\mu\text{F}$  bulk capacitor per Eurocard
- one 1  $\mu\text{F}$  tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal IC and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per 4 packages of SSI logic

An example showing how to determine the value of decoupling capacitor follows. Assume a buffer output sees a  $100\ \Omega$  dynamic load and the output LOW-to-HIGH transition is 5 V; the current demand is therefore 50 mA per output. For an octal buffer, the current demand would be 0,4 A for 6 ns.

The instantaneous current in the capacitor is:

$$i = \frac{\Delta Q}{\Delta t}$$

$$\text{And } i = \frac{C\Delta V}{\Delta t} \quad (\text{from } Q = CV)$$

$$\text{Therefore, } C = \frac{i\Delta t}{\Delta V}$$

For an octal buffer and a change in  $V_{CC}$  of 0,4 V say,

$$C = \frac{0,4\ \text{A} \times 6 \times 10^{-9}\ \text{ns}}{0,4\ \text{V}} = 6\ \text{nF}.$$

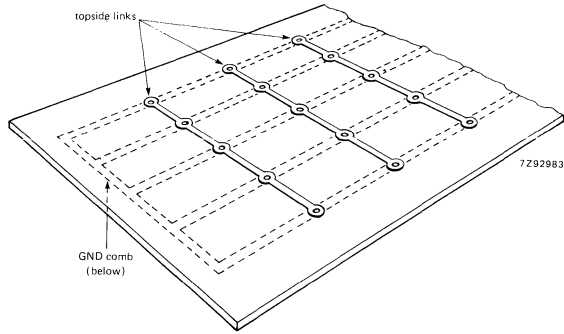


Fig.2 Reducing the length of common ground paths on double-sided board

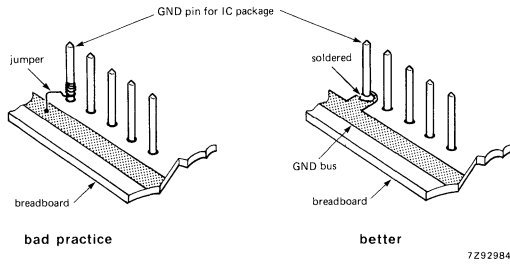


Fig.3 Methods of making ground connections

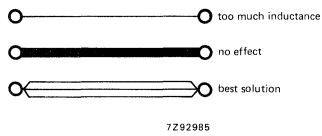


Fig.4 Power supply tracks

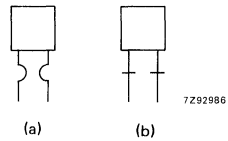


Fig.5 Leads of decoupling capacitors:  
(a)unsuitable; (b) preferred



## POWER DISSIPATION CONSIDERATIONS

For LSTTL logic ICs operating below 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With HCMOS logic ICs however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it is practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one and two orders of magnitude lower than the system clock frequency and the ICs therefore only draw quiescent current for most of the time. This means that replacing LSTTL ICs with equivalent 74HCT ICs, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

However, total system power dissipation, is the sum of both the quiescent and the dynamic power dissipation of all the ICs and must be determined and minimized during system design. For LSTTL, where the quiescent power dissipation is the most significant contributor to the total power dissipation, the total power dissipation can be simply derived from the product of  $V_{CC}$  and  $I_{CC}$  given in the data sheets. For HCMOS circuits however, the dynamic power dissipation which is the most significant part of the total power dissipation is influenced by circuit design. It cannot be read direct from the data sheets but must be calculated from the supply voltage, average switching frequency, load capacitance, internal capacitances of the IC, and transient switching currents.

This article explains how our method of specifying HCMOS ICs in the data sheets makes it very simple to calculate their quiescent, dynamic and total power dissipation.

## QUIESCENT POWER DISSIPATION

Quiescent power is dissipated by an IC when it is not switching and  $V_I = V_{CC}$  or GND. Figure 1(a) will be used to illustrate this power dissipation in HCMOS ICs. In the quiescent state, either the PMOS or the NMOS transistor is fully off and, in theory, no direct MOS transistor channel path exists between  $V_{CC}$  and GND. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between  $V_{CC}$  and GND. This quiescent supply current ( $I_{CC}$ ) is specified in the published data.

Three factors influence the value of  $I_{CC}$ , and therefore the quiescent power dissipation, for a particular IC. They are:

- Temperature: increasing temperature causes  $I_{CC}$  to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated.
- Device Complexity: MSI circuits dissipate more power than SSI circuits because they have a proportionally greater reverse-biased diode junction area.
- Supply voltage: the number of minority charge-carriers is linearly related to reverse junction voltage.

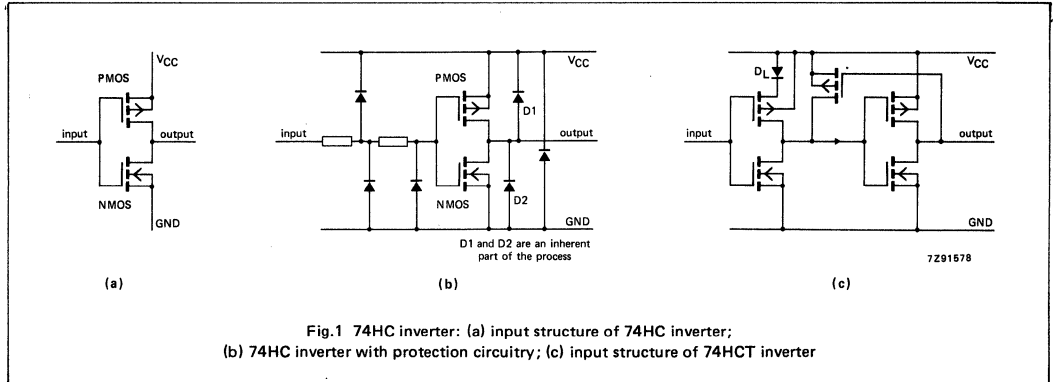
Table 1 shows the JEDEC industry standard for the worst-case  $I_{CC}$  in HCMOS ICs. It shows the effect of temperature and circuit complexity on  $I_{CC}$  at the maximum recommended supply voltage  $V_{CC}$ .  $I_{CC}$  can be linearly derated for other supply voltages and would be approximately one-third of the value in Table 1 for a 74HC IC with  $V_{CC} = 2$  V. Typical  $I_{CC}$  values are well below the maximum specified values.

TABLE 1  
JEDEC industry standard for d.c. characteristics of HCMOS ICs  
DC characteristics for 74HC/HCT

symbol	parameter	$T_{amb}$ (°C)						test conditions			
		74HC/HCT						unit	$V_{CC}$ V *	$V_I$	other
		+25		-40 to +85		-40 to +125					
min.	typ.	max.	min.	max.	min.	max.					
quiescent supply current											
$I_{CC}$	SSI	—	—	2,0	20,0	—	40,0	$\mu$ A	5,5	$V_{CC}$	$I_O = 0$
$I_{CC}$	flip-flops	—	—	4,0	40,0	—	80,0	$\mu$ A	5,5	or	$I_O = 0$
$I_{CC}$	MSI	—	—	8,0	80,0	—	160,0	$\mu$ A	5,5	GND	$I_O = 0$

\* for HC,  $V_{CC} = 6$  V.



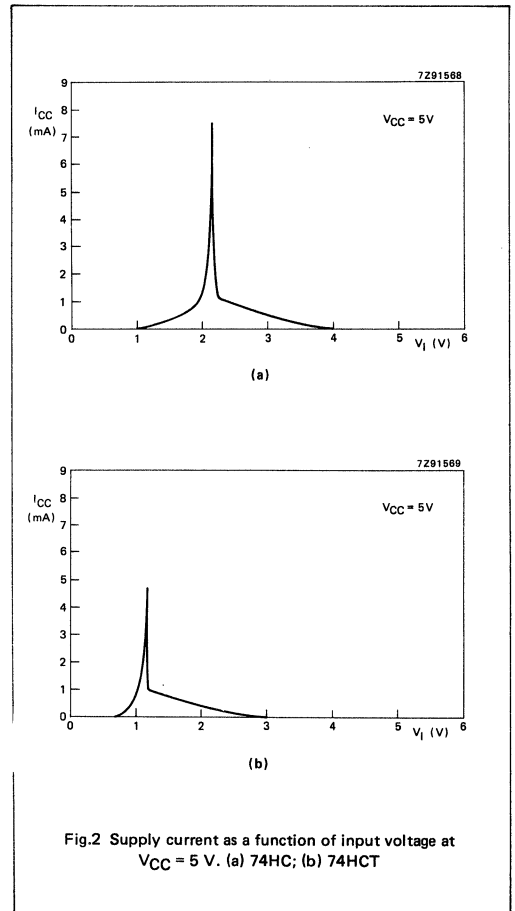


Another factor which influences quiescent power dissipation is the steady-state input voltage level which may slightly turn-on one of the input transistors shown in Fig.1(a) and yet not fully turn-off the other. This causes a small additional quiescent supply current ( $\Delta I_{CC}$ ) to flow between  $V_{CC}$  and GND. The level of  $\Delta I_{CC}$  depends on the size of the input transistors and is different for each device.

In a system consisting entirely of 74HC ICs, the additional quiescent supply current  $\Delta I_{CC}$  is so small that it can be omitted from practical power dissipation calculations. This is because 74HC outputs swing from GND to  $V_{CC}$ . The worst-case output levels with  $|I_O| = 20 \mu A$  are  $V_{OL} = 0,1 V$  max. and  $V_{OH} = V_{CC} - 0,1 V$  min., very close to GND and  $V_{CC}$  respectively. Figure 2(a) shows that  $\Delta I_{CC}$  is negligible when these levels are applied to 74HC inputs because they always turn one of the input transistors fully off.

However, if 74HC input levels are held close to the switching threshold (typically  $V_{CC}/2$ ), Fig.2 shows that the additional quiescent supply current ( $\Delta I_{CC}$ ) becomes much greater than quiescent supply current  $I_{CC}$ . This occurs if the mistake is made of driving a 74HC input from a TTL output. With a minimum TTL  $V_{OH}$  of 2,4 V driving a 74HC input, not only will a logic "1" probably not be recognized, but several milliamps of ( $\Delta I_{CC}$ ) will flow. To overcome this problem, an external pull-up resistor could be used as shown in Fig.3 but the resistor would dissipate significant power because its value would have to be low to maintain switching speed. 74HCT ICs have TTL input switching levels and should therefore be used instead of 74HC ICs whenever it is necessary to interface HCMOS with TTL logic.

Unlike 74HC ICs, 74HCT ICs can be substituted for LSTTL ICs and/or mixed with LSTTL, ALSTTL, ASTTL or FAST-TTL family ICs in the same system. Under some conditions, they may dissipate somewhat more quiescent power than 74HC ICs. For example, Fig.2(b) shows that a worst-case TTL  $V_{OL}$  of 0,5 V max. is close enough to GND



to turn the input NMOS transistor fully off so that  $\Delta I_{CC}$  is close to zero. However, a worst-case TTL  $V_{OH}$  of 2,4 V min. causes some  $\Delta I_{CC}$  to flow. For this reason, 74HCT data sheets specify  $I_{CC}$  at the worst-case input voltage of  $V_{CC} - 2,1$  V for  $V_{CC}$  ranging from 4,5 V to 5,5 V. It is further specified on a per input pin basis to allow more accurate power dissipation calculations if all the functions within an IC are not being used, or are being driven by different input voltage levels.

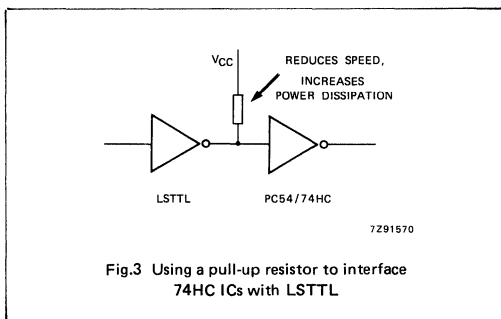


Fig.3 Using a pull-up resistor to interface 74HC ICs with LSTTL

Our proprietary 74HCT input structure shown in Fig.1(c) considerably reduces the additional quiescent supply current  $\Delta I_{CC}$ . The structure is identical to that for 74HC circuits except for a level-shifting diode between the PMOS transistor and  $V_{CC}$ , and the connection of the substrate of the CMOS transistor to  $V_{CC}$ . The effect is to reduce the input level switching threshold to 28% $V_{CC}$  instead of 50% $V_{CC}$  as is the case with 74HC ICs. This therefore reduces the additional quiescent current  $\Delta I_{CC}$  when a TTL minimum HIGH level of 2,4 V is applied to a 74HCT input by ensuring that the PMOS transistor is fully turned off. Figure 2(b) shows that  $\Delta I_{CC}$  is negligible when a 74HCT input is held at a typical TTL HIGH output level (3,4 V) or LOW output level (0,25 V).

### Calculating 74HC quiescent power dissipation

For power-critical applications such as battery-powered equipment, it may be necessary to calculate 74HC quiescent power dissipation as a standby value of battery drain. It is given by:

$$P_{QHC} = V_{CC} I_{CC} \quad (1)$$

$V_{CC}$  is dependent upon the particular application, we recommend that a  $\pm 10\%$  variation be allowed.  $I_{CC}$  at  $V_{CCmax}$  is obtained from the data sheet for the particular IC. For critical battery-powered applications, the value of  $I_{CC}$  can be linearly derated for any desired  $V_{CC}$ ; for example, at  $V_{CC} = 2$  V, use one-third of the limits shown in Table 1 for 74HC ICs.

### Calculating 74HCT quiescent power dissipation

Assume that an LSTTL IC with an output duty factor of 0,5 is switching one gate input in a 74HCT11 (triple 3-input AND gate) with a 5 V supply and an ambient temperature of 25 °C. Quiescent power dissipation is calculated from:

$$P_{QHCT} = V_{CC}(I_{CC} + \delta \Delta I_{CC}) \quad (2)$$

where  $\delta$  = switching duty factor.

$\Delta I_{CCmax}$  is calculated on a unit-load basis from the part of the data sheet reproduced in Table 2:

$$\Delta I_{CCmax} = 360 \mu A \text{ per input pin} \times 1 \text{ pin} \times 0,5 \text{ unit-load coefficient} = 180 \mu A.$$

Inserting this current and the values for  $V_{CC}$  (5,5 V),  $I_{CC} = 2 \mu A$  from Table 2, and  $\delta$  (0,5) into equation (2) gives:

$$P_{QHCT} = 5,5 \text{ V} [2 \mu A + (0,5 \times 180 \mu A)] = 506 \mu W.$$

This is only 2% of the 25,5 mW maximum quiescent power that would be dissipated by the equivalent LSTTL IC. Furthermore, as previously stated, the  $\Delta I_{CC}$  of 360  $\mu A$  per input pin quoted in Table 2 for the 74HCT11 IC is based on a worst-case HIGH input level of  $V_{CC} - 2,1$  V. In a typical application, the TTL HIGH input level driving the IC would be much higher than this, resulting in a reduction of  $\Delta I_{CC}$  by an order of magnitude.

If all the inputs of a 74HCT IC are driven by 74HC or equivalent CMOS outputs, the input levels are such that the additional quiescent supply current  $\Delta I_{CC}$  is so small that it can be omitted from 74HCT power dissipation calculations. 74HC quiescent power dissipation equation (1) can then be used to calculate 74HCT quiescent power dissipation.

### DYNAMIC POWER DISSIPATION

Unlike quiescent power dissipation, dynamic power dissipation is calculated in the same manner for both 74HC and 74HCT ICs. All equations presented here for dynamic power dissipation are therefore applicable to both 74HC and 74HCT ICs.

Three factors influence the dynamic power dissipation of HCMOS ICs. They are load capacitance, internal capacitance and switching transient currents (through-currents of transistor pairs when both transistors momentarily conduct during logic level transitions).

**TABLE 2**  
Specification of  $I_{CC}$ ,  $\Delta I_{CC}$  and unit load coefficient for 74HCT11 triple 3-input AND gate

symbol	parameter	$T_{amb}$ (°C)						unit	test conditions		
		74HCT							$V_{CC}$ V	$V_I$	other
		+25		-40 to +85		-40 to +125					
min.	typ.	max.	min.	max.	min.	max.					
$I_{CC}$	quiescent supply current		2,0		20,0		40,0	$\mu A$	5,5	$V_{CC}$ or GND	$I_O = 0$
$\Delta I_{CC}$	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)	100	360		450		490	$\mu A$	4,5 to 5,5	$V_{CC}$ -2,1 V	other inputs at $V_{CC}$ or GND: $I_O = 0$

**Note:**

- The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given here. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in table below.

input	unit load coefficient
nA, nB, nC	0,5

**Load capacitance**

The first contribution to dynamic power dissipation is caused by the charging and discharging of external capacitive loads. Figure 4 illustrates an HCMOS inverter with a capacitive load and, together with the following equations, will help to illustrate how load capacitance consumes power. The energy dissipated (joules) in charging and discharging the capacitive load is:

$$P_{CLt} = C_L V_{CC}^2 \quad (3)$$

where  $t = 1/f_O$  and  $C_L =$  total external load capacitance due to interconnections, driven inputs and any sockets that are used.

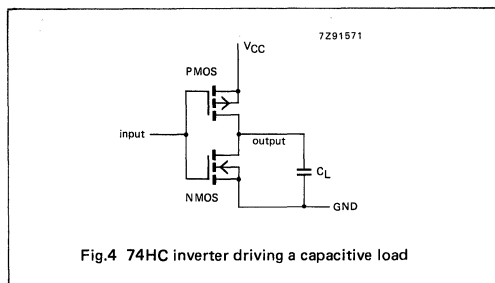


Fig.4 74HC inverter driving a capacitive load

The dynamic power dissipation due to capacitive loads is therefore:

$$P_{CL} = C_L V_{CC}^2 f_O \quad (4)$$

Equation (4) is only applicable if all the outputs are switching the same load. If they are not, the equation becomes:

$$P_{CL} = \Sigma(C_L V_{CC}^2 f_{O_i}) \quad (5)$$

For multiple output ICs, it is important to calculate with the appropriate output frequency. For example, at either output from a flip-flop,  $f_O = f_i/2$ ; for a 7-stage binary ripple counter (type 74HC/HCT4024),  $f_O$  is halved for each successive output stage so that  $f_O = f_i/64$  for the final output stage.

**Internal capacitance**

All MOS logic ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminium and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the circuit.

HCMOS ICs are manufactured with a self-aligned polysilicon gate process (3 $\mu m$  gate length) and local oxidation to reduce internal capacitance by minimising gate-to-source

and gate-to-drain capacitances. The junction capacitances, which are proportional to junction area, are smaller than those in HE4000B CMOS ICs because the diffusions are shallower. Figure 5 shows the location of the capacitances in a 74HC inverter.

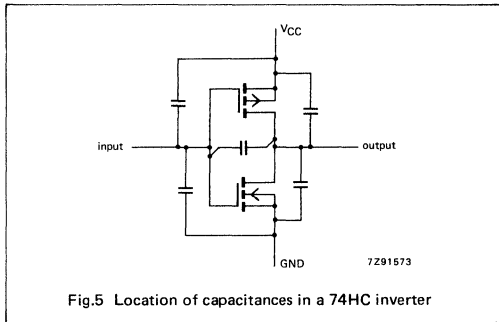


Fig.5 Location of capacitances in a 74HC inverter

For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance  $C_{pD}$ . It is defined in the data sheet for each HCMOS IC on a 'per function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within an IC. This allows more accurate power dissipation calculations to be made if logic functions within the same IC are operating at different frequencies.

The published figure for  $C_{pD}$  is valid for the worst-case operating mode under typical operating conditions. For example, in the case of a NAND gate, the state of the inputs is assumed to be such that the output is changing state; for a shift register or D-type flip-flop, it is assumed that alternately HIGH/LOW data is being clocked in. The specified value for  $C_{pD}$  however is a typical one; nevertheless, some protection will already be built-in to dynamic power dissipation calculations because the assumed worst-case operating modes don't always occur. Although we're not yet prepared to officially publish a maximum value for  $C_{pD}$ , a rough guide would be to increase the published figure by 50% for worst-case calculations. The method of measuring  $C_{pD}$  is explained in the chapter "User Guide".

**Switching transient currents**

The final factor that contributes to the dynamic power dissipation of HCMOS is internal switching transient currents. When the output of a basic HCMOS inverter as shown in Fig.6(a) changes state, either from a logic "1" to a logic "0" or vice-versa, there is a brief period during which both transistors conduct. This creates a temporary low-resistance path between  $V_{CC}$  and GND as shown in

Fig.6(b). In this transitory state, additional supply current ( $\Delta I_{CC}$ ) flows and power is dissipated, so input rise and fall times should be kept short. The average value of this transient current increases linearly with increasing switching frequency. In other words, power dissipation due to switching (like power dissipation due to internal capacitance) increases linearly with increasing switching frequency. However, since it is small compared to the power dissipation due to internal capacitance, its effect is included in the published value of power dissipation capacitance ( $C_{pD}$ ) which has discussed under the previous heading.

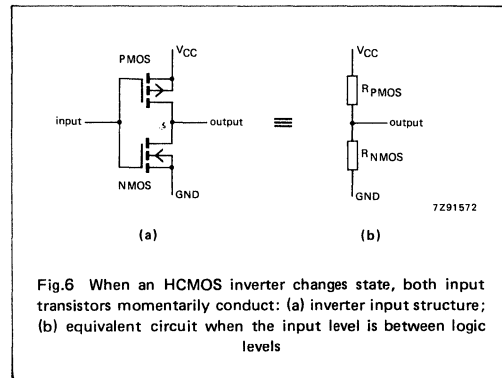


Fig.6 When an HCMOS inverter changes state, both input transistors momentarily conduct: (a) inverter input structure; (b) equivalent circuit when the input level is between logic levels

**Total dynamic power dissipation**

Since  $C_{pD}$  represents the load imposed by both internal capacitance and switching transient currents, the total dynamic power dissipation due to these factors is:

$$P_{DYN} = C_{pD} V_{CC}^2 f_i \tag{6}$$

The total dynamic power dissipation of HCMOS ICs is obtained by adding equation (6) to the power dissipation due to the total external capacitive load (equation 5) and is given by:

$$P_D = C_{pD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \tag{7}$$

**CALCULATING TOTAL POWER DISSIPATION FOR 74HC AND 74HCT ICs**

Total HCMOS power dissipation is a summation of the appropriate quiescent and dynamic power dissipation formulae previously described.

For 74HC/HCT ICs driven by CMOS levels:

$$P_{tot} = V_{CC} I_{CC} + C_{pD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \tag{8}$$

For 74HCT ICs driven by TTL:

$$P_{tot} = V_{CC} (I_{CC} + \delta I_{CC}) + C_{pD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) \tag{9}$$

**POWER DISSIPATION IN OSCILLATORS AND ONE-SHOTS**

The information presented so far is only valid for ICs switching rapidly between logic levels. Additional quiescent supply current  $\Delta I_{CC}$  is greater for one-shots, oscillators and gates arranged as oscillators because, in these applications, the input slowly passes through the switching threshold (typically 50% $V_{CC}$  for 74HC ICs and 28% $V_{CC}$  for 74HCT ICs) causing flow-through current as shown in Fig.2.

**POWER DISSIPATION COMPARISON BETWEEN HCMOS, LSTTL AND ALSTTL**

In any IC, there is a balance between speed and power dissipation. LSTTL logic is relatively fast but the quiescent power dissipated by its bipolar circuitry is considerable. ALSTTL improves upon LSTTL by using advanced wafer fabrication techniques and smaller geometries. These improvements increase speed and approximately halve the quiescent power dissipation.

CMOS ICs dissipate negligible quiescent power compared with all bipolar TTL logic ICs but, until the development of the HCMOS family, CMOS ICs were relatively slow. Use of advanced wafer fabrication techniques and smaller geometries has now made it possible for HCMOS to match the speed of LSTTL and yet retain the substantial power savings afforded by CMOS. Figure 7 shows the speed-power products for today's most popular logic IC technologies.

Figures 8 and 9 compare the dynamic power dissipation of SSI and MSI for 74HC, and LSTTL ICs. These graphs show that 74HC ICs maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL ICs is caused by the many bipolar transistors that continuously conduct.

Figures 8 and 9 also show that, as device complexity increases, the frequency at which HCMOS ICs dissipate the same amount of power as LSTTL ICs also increases. This is because, as LSTTL complexity increases, there are more resistive paths between  $V_{CC}$  and GND which carry more quiescent bias current and thus cause more quiescent power dissipation. HCMOS ICs also dissipate more quiescent power as their complexity increases, but the leakage currents which cause it are so small that it can be ignored.

The power dissipation of the different logic IC technologies is translated into total system power as a function of frequency in Fig.10 which is for a small system consisting of one gate and two flip-flops. The graph shows that HCMOS also dissipates substantially less power than LSTTL at the system level.

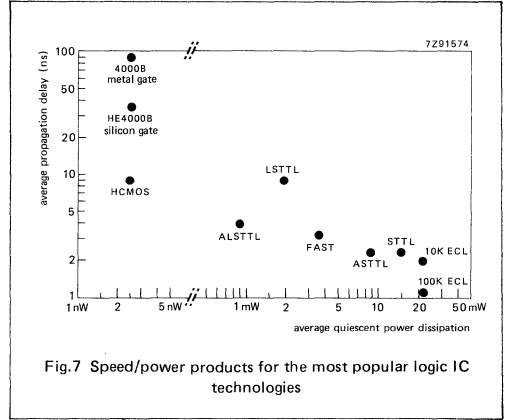


Fig.7 Speed/power products for the most popular logic IC technologies

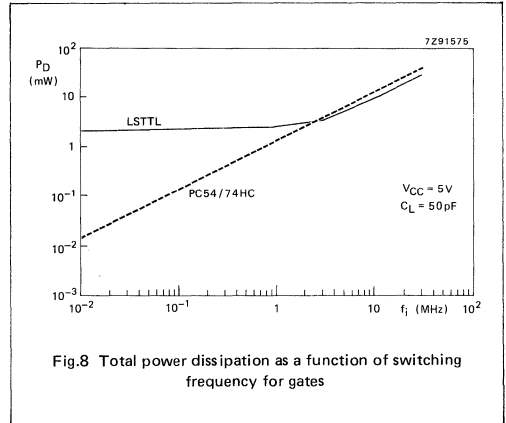


Fig.8 Total power dissipation as a function of switching frequency for gates

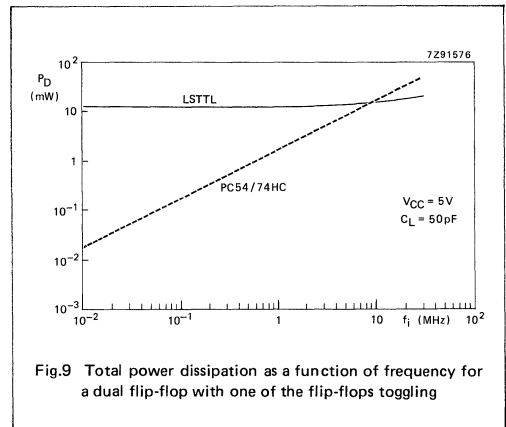


Fig.9 Total power dissipation as a function of frequency for a dual flip-flop with one of the flip-flops toggling

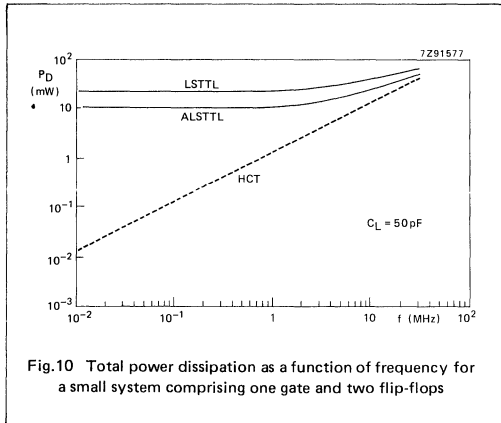


Fig.10 Total power dissipation as a function of frequency for a small system comprising one gate and two flip-flops

### INFLUENCE OF HCMOS ICs ON APPLICATIONS

The significantly lower power dissipation in an HCMOS logic system, compared with its LSTTL or ALSTTL equivalent, is *the* primary reason why HCMOS ICs should be used for new system designs and to replace LSTTL or ALSTTL ICs in many existing designs where power consumption and/or dissipation is a problem.

For new designs, HCMOS is the only suitable family of logic ICs for battery-powered portable personal computers. The use of HCMOS is *the* major trend in personal computers using all CMOS microprocessors, RAMs, ROMs, and peripherals. All CMOS designs can be powered-down to 2 V standby to extend battery life.

For non-portable equipment, the use of HCMOS logic and CMOS LSI is also preferred because it not only reduces power dissipation, but also significantly reduces, in order of priority, cost, size, and weight. Cost reductions stem from major reductions of power supply current and regulation, cooling fans, heatsinks, and copper buses.

An equally powerful motivating force for using HCMOS logic ICs with their lower power dissipation is the inherent and proven increase of component and equipment reliability. Equipment life is considerably extended because IC junction temperatures are much reduced and other components are exposed to lower ambient temperatures.



## PACKAGE OUTLINES

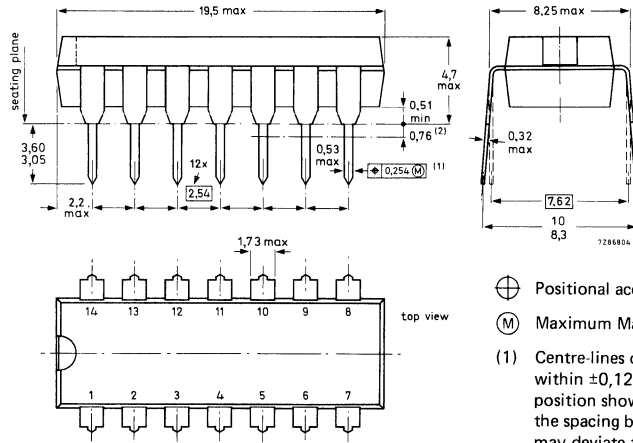
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**Outline drawings . . . . . 1001**





**14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)**



⊕ Positional accuracy.

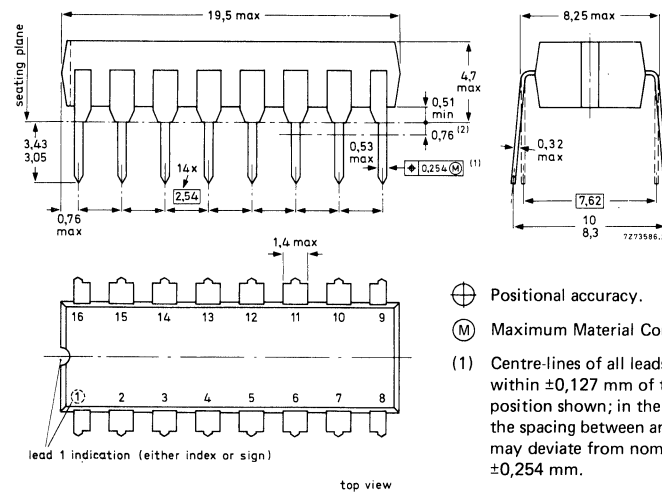
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

**16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)**



⊕ Positional accuracy.

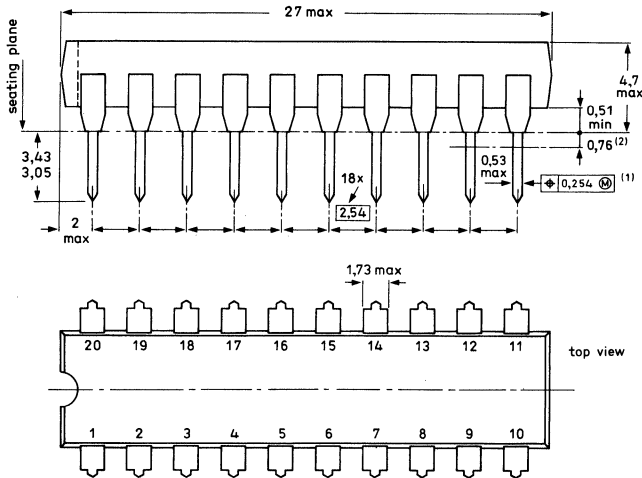
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.

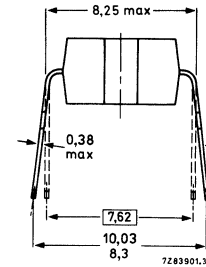
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)



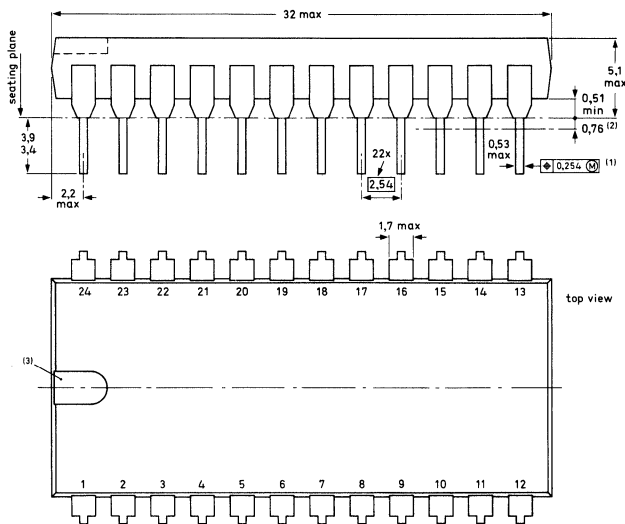
Dimensions in mm



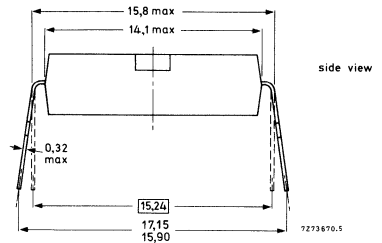
- ⊕ Positional accuracy.
- (M) Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL-IN-LINE; PLASTIC (SOT-101A)



Dimensions in mm



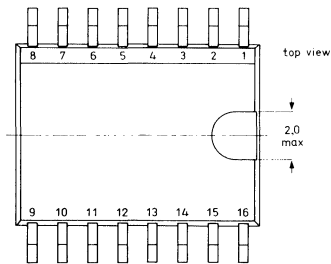
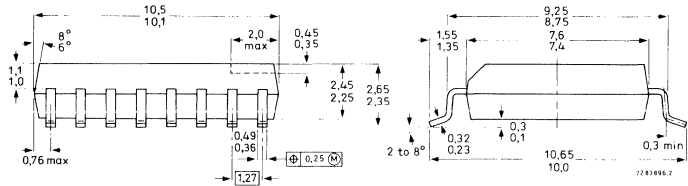
- ⊕ Positional accuracy.
- (M) Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.





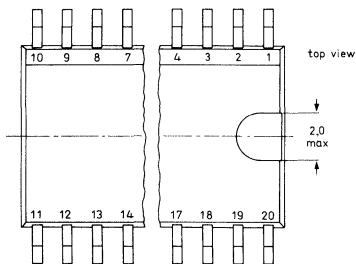
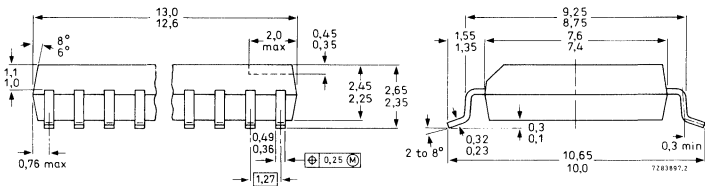
16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

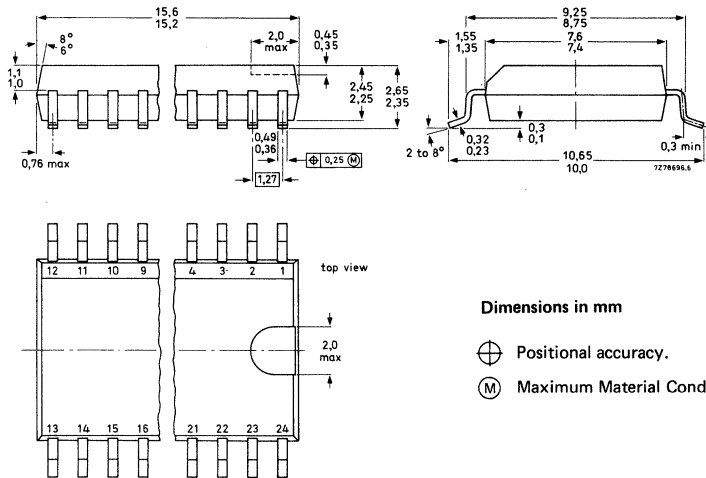
20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)



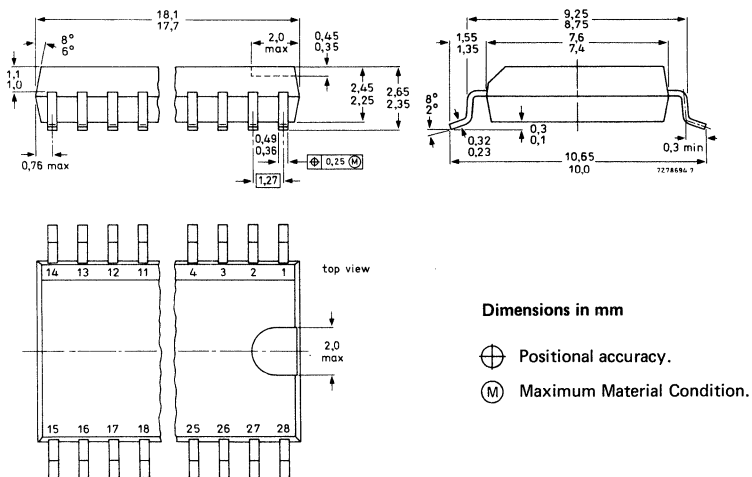
Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)



NOTES



NOTES

## FAMILY SPECIFICATIONS

### GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

### INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage ( $5\text{ V} \pm 10\%$ ) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

### HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

### RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
$V_I$	DC input voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHAR. per device
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$

### Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

### RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
$V_{CC}$	DC supply voltage	2.0	5.0	6.0	V	
$V_I$	DC input voltage range	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	°C	see DC and AC CHAR. per device
$T_{amb}$	operating ambient temperature range	-40		+125	°C	



## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OH</sub>	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 6.0 mA
V <sub>OL</sub>	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 6.0 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0
I <sub>CC</sub>	quiescent supply current SSI flip-flops MSI			2.0 4.0 8.0		20.0 40.0 80.0		40.0 80.0 160.0	μA μA μA	5.5 5.5 5.5	V <sub>CC</sub> or GND	I <sub>O</sub> = 0 I <sub>O</sub> = 0 I <sub>O</sub> = 0
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0

### Note

- The additional quiescent supply current per input is determined by the ΔI<sub>CC</sub> unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V<sub>I</sub> = 2.4 V; V<sub>CC</sub> = 5.5 V) specification is: ΔI<sub>CC</sub> = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs		25 35	mA mA	for $-0.5$ V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: – standard outputs – bus driver outputs		50 70	mA mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT/HCU
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

### Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.



## FAMILY SPECIFICATIONS

### GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

### INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage ( $5\text{ V} \pm 10\%$ ) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

### HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

### RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
$V_I$	DC input voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHAR. per device
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$

### Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

### RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
$V_{CC}$	DC supply voltage	2.0	5.0	6.0	V	
$V_I$	DC input voltage range	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	°C	see DC and AC CHAR. per device
$T_{amb}$	operating ambient temperature range	-40		+125	°C	





### DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OH</sub>	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 6.0 mA -I <sub>O</sub> = 7.8 mA	
V <sub>OL</sub>	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 6.0 mA I <sub>O</sub> = 7.8 mA
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
I <sub>CC</sub>	quiescent supply current SSI flip-flops MSI			2.0 4.0 8.0		20.0 40.0 80.0		40.0 80.0 160.0	μA μA μA	6.0 6.0 6.0	V <sub>CC</sub> or GND	I <sub>O</sub> = 0 I <sub>O</sub> = 0 I <sub>O</sub> = 0



## RATINGS

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$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs		25 35	mA mA	for $-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V
$\pm I_{CC}$ ; $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: – standard outputs – bus driver outputs		50 70	mA mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT/HCU
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