INTEGRATED CIRCUITS

DATA HANDBOOK

BOOK IC01a 1990

Radio, audio and associated systems
Bipolar, MOS
CA3089 to TDA1510A

Philips Components

PHILIPS

RADIO, AUDIO AND ASSOCIATED SYSTEMS
BIPOLAR, MOS

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PCA80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to +125 °C	209
PCA80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to +125 °C	213
PCA80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +125 °C	215
PCA80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to +125 °C	217
PCA83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to +125 oC	213
PCA83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2-pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +125 °C	215
PCA83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to +125 °C	217
PCA83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to +125 °C	219
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PCB80C31BH-3	microcontroller; 128 x 8 RAM; 1.2 to 16 MHz; 0 to +70 °C	209
PCB80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to +70 °C	209
PCB80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to +70 °C	209

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8051/80C51 family CMOS (continued)		
PCB80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to +70 °C	213
PCB80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; 0 to +70 °C	215
PCB80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to +70 °C	217
PCB80C851	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to +70 °C	221
PCB83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to +70 °C	213
PCB83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; 0 to +70 °C	215
PCB83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to +70 °C	217
PCB83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to +70 °C	219
PCB83C851	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to +70 °C	221
PCF80C31BH-3	microcontroller; 128 x 8 RAM; 1.2 to 12 MHz; −40 to +85 °C	209
PCF80C51BH-3	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; −40 to +85 °C	209
PCF80C552	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to +85 °C	213
PCF80C562	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +85 °C	215
PCF80C652	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; −40 to +85 °C	217
PCF80C851	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	221
PCF83C552	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; −40 to +85 °C	213

type no.	description	page
PCF83C562	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; −40 to +85 °C	215
PCF83C652	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^{2}C-bus; 1.2 to 12 MHz; −40 to + 85 °C	217
PCF83C654	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^{2}C-bus; 1.2 to 12 MHz; −40 to +85 °C	219
PCF83C851	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	221
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PCF84C21	microcontroller; 64 x 8 RAM; 2K x 8 ROM; plus 8-bit LED driver; I^{2}C-bus; −40 to +85 °C	283
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MAB8421	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^{2}C-bus; 1.0 to 6 MHz; 0 to +70 °C	79
MAB8422	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I^{2}C-bus; 1.0 to 6 MHz; 0 to +70 °C	81
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MAF84A22	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I^2C-bus; 1.0 to 5 MHz; –40 to +110 °C	81
MAF84A41	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 5 MHz; –40 to +110 °C	79
MAF84A42	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I^2C-bus; 1.0 to 5 MHz; –40 to +110 °C	81
MAF84A61	microcontroller; 128 x 8 RAM; 6K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 5 MHz; –40 to +110 °C	79
MAF8411	microcontroller; 64 x 8 RAM; 1K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to +85 °C	79
MAF8421	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to +85 °C	79
MAF8422	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I^2C-bus 1.0 to 6 MHz; –40 to +85 °C	81
MAF8441	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to +85 °C	79
MAF8442	microcontroller; 128 x 8 RAM; 4K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to +85 °C	81
MAF8461	microcontroller; 128 x 8 RAM; 6K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to +85 °C	79
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PCB80C39	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; 0 to +70 °C	211
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PCF80C39	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; –40 to +85 °C	211
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TDA7050	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1423
TDA7050T	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1427
TDA7052	1 W BTL mono audio amplifier for portable applications	1431
TDA7053	2 x 1 W BTL stereo audio power amplifier for portable applications	1437
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MAF8411P	microcontroller; 64 x 8 RAM; 1K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to + 85 °C	79
MAF8421P	microcontroller; 64 x 8 RAM; 2K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I^2C-bus; 1.0 to 6 MHz; –40 to + 85 °C	79
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PCA80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; –40 to + 110 °C	211

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PCA80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; –40 to + 125 °C	209
PCA80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	213
PCA80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; –40 to + 125 °C	215
PCA80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	217
PCA80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	217
PCA83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	213
PCA83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; –40 to + 125 °C	215
PCA83C652P	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	217
PCA83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 125 °C	217
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PCB80C31BH-3WP	microcontroller; 128 x 8 RAM; 1.2 to 16 MHz; 0 to + 70 °C	209
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PCB80C39WP	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; 0 to + 70 °C	211
PCB80C49P	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; 0 to + 70 °C	211
PCB80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; 0 to + 70 °C	211

type	description	page
PCB80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to + 70 °C	209
PCB80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 0.5 to 12 MHz; 0 to + 70 °C	209
PCB80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to + 70 °C	209
PCB80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 16 MHz; 0 to + 70 °C	209
PCB80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	213
PCB80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; 0 to + 70 °C	215
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PCB80C851WP	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
PCB80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	213
PCB83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; 0 to + 70 °C	215
PCB83C652P	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	217
PCB83C654P	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	219
PCB83C654WP	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; 0 to + 70 °C	219
PCB83C851P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to + 70 °C	221
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PCF80C31BH-3P	microcontroller; 128 x 8 RAM; 1.2 to 12 MHz; –40 to + 85 °C	209
PCF80C31BH-3WP	microcontroller; 128 x 8 RAM; 1.2 to 12 MHz; –40 to + 85 °C	209
PCF80C39P	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; –40 to + 85 °C	211
PCF80C39WP	microcontroller; 128 x 8 RAM; 1.0 to 15 MHz; –40 to + 85 °C	211
PCF80C49P	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; –40 to + 85 °C	211
PCF80C49WP	microcontroller; 128 x 8 RAM; 2K x 8 ROM; 1.0 to 15 MHz; –40 to + 85 °C	211
PCF80C51BH-3P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; –40 to + 85 °C	209
PCF80C51BH-3WP	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 1.2 to 12 MHz; –40 to + 85 °C	209
PCF80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	213
PCF80C562WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; –40 to + 85 °C	215
PCF80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	217
PCF80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	217
PCF80C851P	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; –40 to + 85 °C	221
PCF80C851WP	microcontroller; 128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; –40 to + 85 °C	221
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PCF83C552WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	213
PCF83C562WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; 2 pulse-width modulated signals; 8 multiplexed input lines; 1.2 to 12 MHz; –40 to + 85 °C	215

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PCF83C652WP	microcontroller; 256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	217
PCF83C654P	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	219
PCF83C654WP	microcontroller; 256 x 8 RAM; 16K x 8 ROM; serial I/O; UART; I^2C-bus; 1.2 to 12 MHz; –40 to + 85 °C	219
PCF83C851P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; –40 to + 85 °C	221
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PCF84C41T	microcontroller; 128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I^2C-bus; –40 to + 85 °C	283
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SA572D	programmable analogue compandor	103
SA572F	programmable analogue compandor	103
SA572N	programmable analogue compandor	103
SA5534N	dual and single low noise operational amplifier	135
SA5534AD	dual and single low noise operational amplifier	135
SA5534AN	dual and single low noise operational amplifier	135
SA602D	double balanced mixer and oscillator	143
SA602N	double balanced mixer and oscillator	143
SA602FE	double balanced mixer and oscillator	143
SA604AD	high performance low-power FM IF system	149
SA604AN	high performance low-power FM IF system	149
SA605D	low-power FM IF system	159
SA605F	low-power FM IF system	159
SA605N	low-power FM IF system	159
SA614AD	low-power FM IF system	169
SA614 AN	low-power FM IF system	169
SAA1057	radio tuning PLL frequency synthesizer (SYMO II)	545
SAA1064P	4-digit LED driver; I^2C-bus	555
SAA1099	stereo sound generator for sound effects and music synthesis (μC-controlled)	565
SAA1300	tuner switching circuit; I^2C-bus	581
SAA3004P	high performance transmitter (455 kHz) for infrared remote control; up to 448 commands	585
SAA3004T	high performance transmitter (455 kHz) for infrared remote control; up to 448 commands	585
SAA3006P	high performance transmitter (RC-5) for infrared remote control; up to 2048 commands	595
SAA3007P	high performance transmitter (455 kHz) for infrared remote control; up to 1280 commands; low voltage	609
SAA3007T	high performance transmitter (455 kHz) for infrared remote control; up to 1280 commands; low voltage	609
SAA3008P	high performance transmitter (38 kHz) for infrared remote control; low voltage	623
SAA3008T	high performance transmitter (38kHz) for infrared remote control; low voltage	623
SAA3009P	infrared remote control decoder; decodes 64 commands (RECS80/RC-5); up to 32 subaddresses; high current output capability for direct LED drive	637
SAA3010P	high performance transmitter (RC-5) for infrared remote control; low voltage	647
SAA3010T	high performance transmitter (RC-5) for infrared remote control; low voltage	647
SAA3028	high performance transcoder (RC-5) for infrared remote control; I^2C-bus	663
SAA3049P	infrared remote control decoder, low current version of SAA3009	637

type	description	page
SAA3049T	infrared remote control decoder, low current version of SAA3009	637
SAA7210	decoder for Compact Disc (second generation)	671
SAA722P	digital filter and interpolator for Compact Disc (second generation)	693
SAA7274P	audio digital input circuit (ADIC)	715
SAA7274T	audio digital input circuit (ADIC)	715
SAA7310P	decoder for Compact Disc (third generation)	727
SAA7310GP	decoder for Compact Disc (third generation)	727
SAA7320GP	stereo DAC for Compact Disc	757
SAD7630P	CCD delay line for error correction in video and sound carrier timebases (laservision players)	777
SAF1032P	receiver/decoder for infrared remote control	787
SAF1039P	transmitter for infrared remote control	787
SE5410F	10-bit high-speed multiplying DAC	119
SE5532FE	internally-compensated dual low noise operational amplifier	129
SE5532AFE	internally-compensated dual low noise operational amplifier	129
SE5534N	dual and single low noise operational amplifier	135
SE5534AN	dual and single low noise operational amplifier	135
SE5534FE	dual and single low noise operational amplifier	135
SE5534AFE	dual and single low noise operational amplifier	135
TDA1001B	interference and noise suppression circuit for FM receivers	801
TDA1001BT	interference and noise suppression circuit for FM receivers	801
TDA1010A	6 W audio power amplifier for in-car applications/10 W audio power amplifier for mains-fed applications	811
TDA1011	2 to 6 W audio power amplifier with preamplifier	829
TDA1013B	4 W audio power amplifier with DC volume control	841
TDA1015	1 to 4 W audio power amplifier with preamplifier	849
TDA1015T	0.5 W audio power amplifier with preamplifier	859
TDA1016	2 W recording/playback audio power amplifier with preamplifier, automatic level control, short circuit and thermal protection	865
TDA1020	12 W audio power amplifier with preamplifier for car radios	871
TDA1029	signal-sources switch (4 x two channels)	877
TDA1059B	motor speed regulator with thermal shut-down; multiplication coefficient = 9; drop-out voltage = 1.8 V	891
TDA1072A	AM receiver circuit for hi-fi and car radios	897
TDA1072AT	AM receiver circuit for hi-fi and car radios	913
TDA1074A	dual tandem electronic potentiometer circuit	931
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	941
TDA1510A	24 W BTL or 2 x 12 W stereo car radio power amplifier	941
TDA1512	12 to 20 W hi-fi audio power amplifier	983
TDA1512Q	12 to 20 W hi-fi audio power amplifier	983
TDA1514A	50 W hi-fi power amplifier for digital audio (e.g. Compact Disc)	989
TDA1515B	24 W or 2 x 12 W stereo car radio power amplifier	997
TDA1516Q	22 W BTL or 2 x 11 W stereo car radio power amplifier; closed loop voltage gain 26 dB	1003
TDA1517	2 x 6 W stereo car radio audio power amplifier (20 dB gain)	1011

type	description	page
TDA1518Q	22 W BTL or 2 x 11 W stereo car radio power amplifier; closed loop voltage gain 46 dB	1019
TDA1519	2 x 6 W stereo car radio audio power amplifier (40 dB gain)	1027
TDA1519A	22 W BTL or 2 x 11 W stereo car radio power amplifier	1035
TDA1519B	12 W BTL or 2 x 6 W stereo car radio power amplifier	1045
TDA1520B	20 W hi-fi audio power amplifier; complete SOAR protection	1055
TDA1520BQ	20 W hi-fi audio power amplifier; complete SOAR protection	1055
TDA1521	2 x 12 W hi-fi stereo audio power amplifier	1061
TDA1521A	2 x 6 W hi-fi stereo audio power amplifier	1071
TDA1521Q	2 x 12 W hi-fi stereo audio power amplifier	1061
TDA1522	stereo playback amplifier/equalizer with mute switch	1081
TDA1524A	stereo tone/volume control circuit	1091
TDA1525	stereo tone/volume control circuit	1103
TDA1534	14-bit ADC	1117
TDA1535	high-speed sample-and-hold amplifier	1125
TDA1541A	dual 16-bit DAC	1129
TDA1542	active element for post filtering (dual channel)	1137
TDA1543	dual 16-bit economy DAC (I^2S-bus format)	1145
TDA1572	AM receiver circuit for stereo hi-fi and car radios	1153
TDA1572T	AM receiver circuit for stereo hi-fi and car radios	1171
TDA1574	integrated FM tuner for radio receivers	1187
TDA1574T	integrated FM tuner for radio receivers	1195
TDA1576	FM/IF amplifier and detector	1205
TDA1578A	time multiplex PLL stereo decoder for hi-fi and car radios	1217
TDA1579	traffic warning decoder circuit (AM carriers); ARI system	1231
TDA1579T	traffic warning decoder circuit (AM carriers); ARI system	1231
TDA1589	traffic control message and warning tone circuit; ARI system	1241
TDA1596	FM/IF amplifier and detector	1249
TDA1596T	FM/IF amplifier and detector	1267
TDA1598	time multiplex PLL stereo decoder for hi-fi and car radios	1285
TDA1600	multi-function oscillator switch for audio cassette recorders	1293
TDA2611A	5 W audio power amplifier	1305
TDA2613	6 W hi-fi audio power amplifier	1315
TDA3047P	high performance receiver for infrared remote control; positive output voltage	1323
TDA3047T	high performance receiver for infrared remote control; positive output voltage	1323
TDA3048P	high performance receiver for infrared remote control; negative output voltage	1329
TDA3048T	high performance receiver for infrared remote control; negative output voltage	1329
TDA3810	spatial, stereo and pseudo-stereo sound circuit	1335
TDA5040T	DC motor drive circuit with magnetic-field detector	1339
TDA5708	photo diode signal processor for Compact Disc single-spot read-out systems	1347
TDA5709	radial error signal processor for Compact Disc	1367
TDA7000	FM radio circuit; mono (in plastic DIL18)	1381
TDA7010T	FM radio circuit; mono (in SO16 plastic mini-pack)	1389
TDA7021T	FM radio circuit; stereo/mono; for low voltage micro tuning system (MTS)	1397

type	description	page
TDA7030T	low voltage micro tuning system (MTS)	1407
TDA7040T	PLL stereo decoder; low voltage	1415
TDA7050	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1423
TDA7050T	150 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	1427
TDA7052	1 W BTL mono audio amplifier for portable applications	1431
TDA7053	2 x 1 W BTL stereo audio power amplifier for portable applications	1437
TDA8420	hi-fi stereo audio processor; I^2C-bus	1445
TDA8421	hi-fi stereo audio processor; I^2C-bus	1467
TDA8425	hi-fi stereo audio processor; I^2C-bus	1489
TDA8444	octuple 6-bit DAC; I^2C-bus	1511
TDA8808AT	photo diode signal processor for Compact Disc	1519
TDA8808T	photo diode signal processor for Compact Disc	1519
TDA8808	transfer functions	1539
TDA8809T	radial error signal processor for Compact Disc	1559
TDA8809	transfer functions	1571
TDB1080	IF limiting amplifier, FM detector and audio amplifier	1583
TDB1080T	IF limiting amplifier, FM detector and audio amplifier	1583
TDD1601	equalizer for audio cassette recorders	1589
TDD1742T	low power frequency synthesizer (LOPSY)	1605
TEA0651	Dolby B & C noise reduction circuit	1627
TEA0652	Dolby B & C noise reduction circuit	1627
TEA0653T	stereo or 2-channel Dolby B noise reduction circuit	1645
TEA0654	preamplifier and electronic switch for Dolby B & C noise reduction circuits	1627
TEA0657	dual Dolby B noise reduction circuit	1651
TEA0665	Dolby B & C processor with preamplifier and electronic switch	1659
TEA0665T	Dolby B & C processor with preamplifier and electronic switch	1659
TEA0666	Dolby B & C processor with preamplifier and electronic switch; changed frequency response in relation to TEA0665	1669
TEA0666T	Dolby B & C processor with preamplifier and electronic switch; changed frequency response in relation to TEA0665	1669
TEA0670T	Dolby B & C processor with preamplifier and electronic switch; low voltage	1679
TEA5551T	single-chip AM radio circuit, plus dual AF amplifier, for pocket receivers with headphones	1685
TEA5570	AM/FM radio receiver circuit	1697
TEA5580	PLL stereo decoder for medium-fi and car radios	1711
TEA5581	PLL stereo decoder with source selector switch for medium-fi and car radios	1721
TEA5581T	PLL stereo decoder with source selector switch for medium-fi and car radios	1721
TEA5591	AM/FM radio receiver circuit	1733

type	description	page
TEA6100	FM/IF system and microcomputer-based tuning interface; I^2C-bus	1751
TEA6200	AM upconversion radio receiver; 10.7 MHz IF	1775
TEA6300	car radio preamplifier and source selector with sound and fader controls; I^2C-bus	1787
TEA6300T	car radio preamplifier and source selector with sound and fader controls; I^2C-bus	1787
TEA6310T	sound fader control circuit; I^2C-bus	1803
TSA6057	radio tuning PLL frequency synthesizer; I^2C-bus	1821
TSA6057T	radio tuning PLL frequency synthesizer; I^2C-bus	1821
μA758N	FM stereo multiplex decoder; PLL	1831

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA1056P	PLL frequency synthesizer	successor type: SAA1057
SAA3027	infrared remote control transmitter (RC-5)	successor type: SAA3006
TCA730A	DC volume and balance stereo control circuit	
TCA740A	DC treble and bass stereo control circuit	
TDA1011A	2 to 6 W audio power amplifier	successor type: TDA1011
TDA1506	motor regulator and function controller for car cassette systems	
TDA1508	auto-reverse car radio cassette deck steering circuit	
TDA1533	PLL motor speed control circuit for hi-fi applications	
TDA7020T	low voltage FM stereo radio circuit	successor type: TDA7021T

GENERAL

Product status defenition for type numbers with prefixes CA, MC, NE, SA, SE and μA

Ordering information for type numbers with prefixes CA, MC, NE, SA, SE and μA

Type designation for type numbers with prefixes HEF, MAB, MAF, OM, PCA, PCB, PCF, PNA, SAA, SAD, SAF, TDA, TDB, TDD, TEA and TSA

Rating systems

Handling MOS devices

PRODUCT STATUS DEFINITION

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

For type numbers with prefixes CA, MC, NE, SA, SE and μA

Signetics' Linear integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order
$250 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that an SE prefix (−55°C to +125°C) indicates only the operating temperature range of a device and *not* its military qualification status. The military qualification status of any Linear product can be determined by either looking in the Military Data Manual and/or contacting your local sales office.

Table 1. Part Number Description

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
N E 5 5 3 7 N	LF398	LIN	Sample-and-Hold Amp

- Sample-and-Hold Amp → Description of Product Function
- LIN → Linear Product Family
- N (suffix) → Package Descriptions — See Table 2
- 5537 → Device Number
- NE → Device Family and Temperature Range Prefix — See Tables 3 & 4

Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer
   Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

CA3089
FM IF System

Product Specification

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram shows the CA3089 features, which include a three-stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8V to +18V.

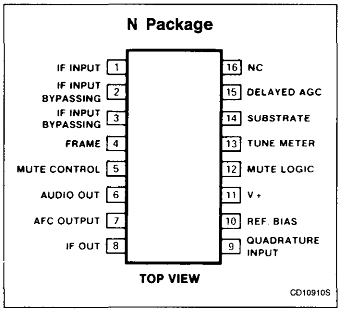
The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at -3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

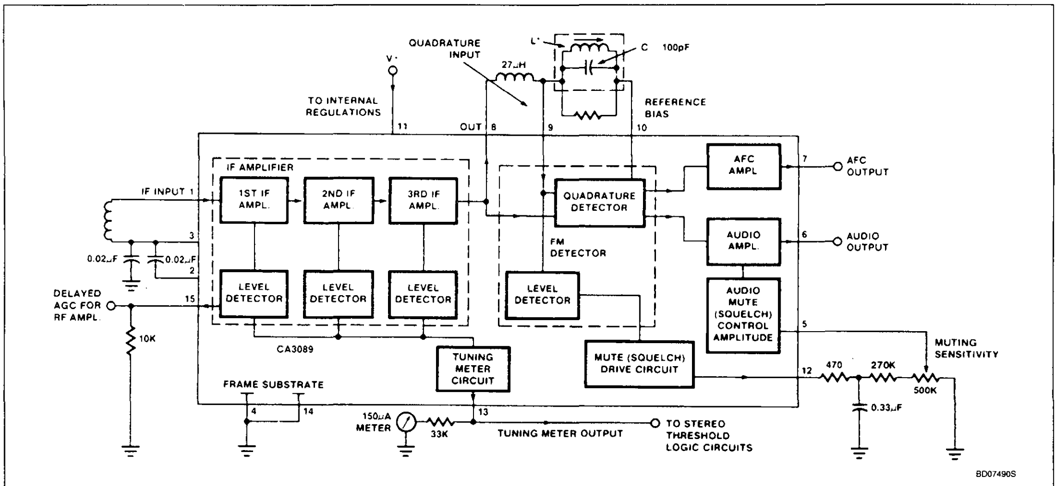
PIN CONFIGURATION



APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

BLOCK DIAGRAM

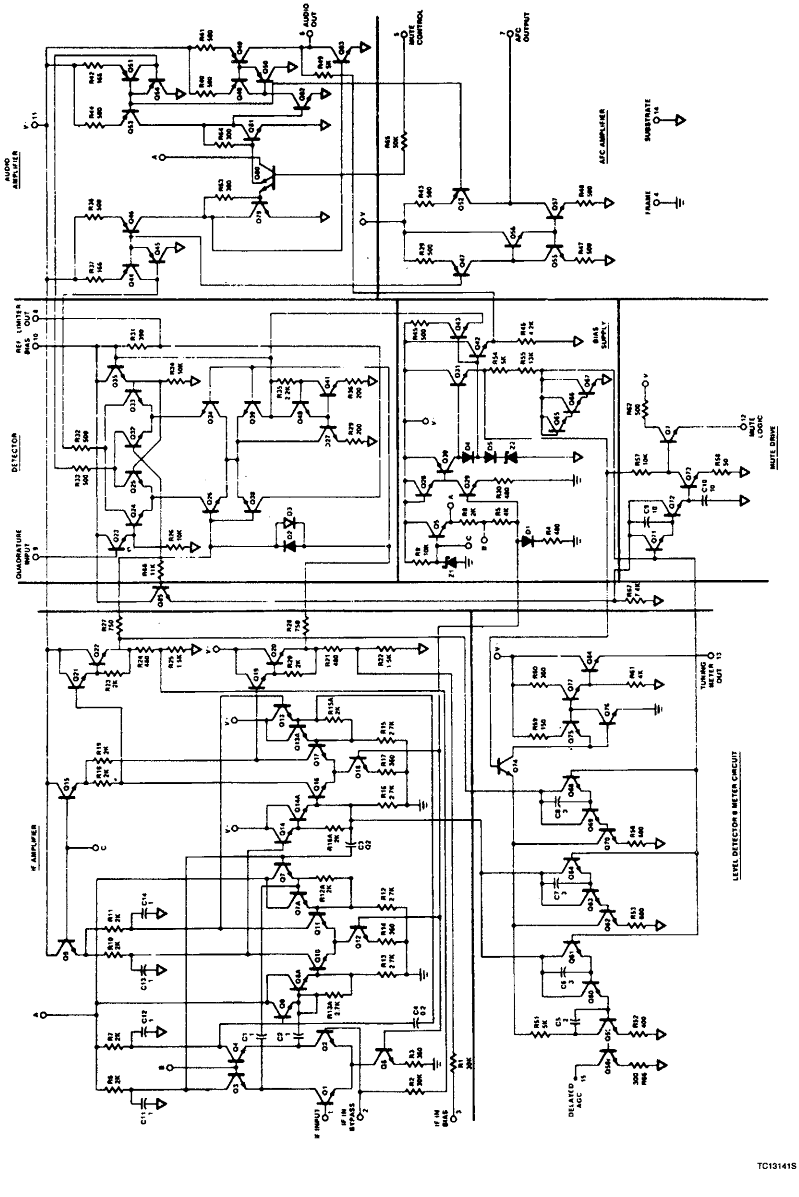


NOTES:
1. All resistor values are typical and in ohms. $Q_O \simeq 75$ (G.I. EX27825 or equivalent)
2. L tunes with 100pF (C) at 10.7MHz

FM IF System

CA3089

EQUIVALENT SCHEMATIC



TC13141S

NOTES:
1. All resistance values are typical and in ohms.
2. All capacitance values are in picofarads.

FM IF System

CA3089

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	−40°C to +85°C	CA3089N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	DC supply voltage: between terminals 11 and 4 between terminals 11 and 14	 18 18	 V V
	DC current (out of Terminal 15)	2	mA
P_D	Device dissipation: up to $T_A = 60°C$ above $T_A = 60°C$	 600 derate linearly 6.7	 mW mW/°C
T_A	Operating ambient temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

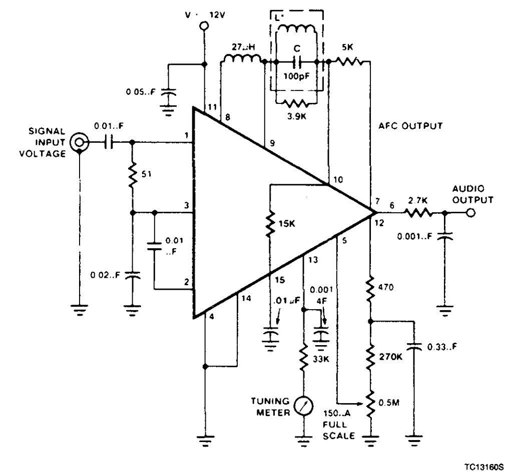
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Static (DC) Characteristics						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages[4]						
V_1	Terminal 1 (1F input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2 V_3	Terminal 2 (AC return to input) Terminal 3 (DC bias to input)	No signal input, non-muted No signal input, non-muted	1.2 1.2	1.9 1.9	2.4 2.4	V V
V_6 V_7 V_{10}	Terminal 6 (audio output) Terminal 7 (AFC) Terminal 10 (DC reference)	No signal input, non-muted No signal input, non-muted No signal input, non-muted	5.0 5.0 5.0	5.6 5.6 5.6	6.0 6.0 6.0	V V V
Dynamic Characteristics						
$V_{I(LIM)}$	Input limiting voltage (–3dB point)[3]			10	25	μV
	AMR AM rejection (Terminal 6)[4]	$V_{IN} = 0.1V$, $f_O = 10.7MHz$, $f_{MOD} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (Terminal 6)[3]		400	500	600	mV
 THD THD	Total harmonic distortion:[1] Single tuned (Terminal 6)[3] Double tuned (Terminal 6)[4]	 $f_{MOD} = 400Hz$, $V_{IN} = 0.1$		 0.5 0.1	 1.0	 % %
S + N/N MU_{IN}	Signal plus noise-to-noise ratio (Terminal 6)[3] Mute input (Terminal 5)	Deviation = ± 75kHz, $V_{IN} = 0.1V$ $V_5 = 2.5V$	60 50	70 70		dB dB
MU_{OUT}	Mute output (Terminal 12)	$V_{IN} = 50\mu V$ $V_{IN} = 0V$	 4.0		0.5	V V
MTR	Meter output (Terminal 13)	$V_{IN} = 0.1V$ $V_{IN} = 500\mu V$ $V_{IN} = 0V$	2.5 1.0	3.5 1.5	 0.7	V V V
AGC	Delay AGC (Terminal 15)	$V_{IN} = 0.01V$ $V_{IN} = 10\mu V$	 4.0	 5.0	0.5	V V
THD	Double tuned (Terminal 6)[4]	$f_{MOD} = 400Hz$ $V_{IN} = 0.1$		0.1		%

NOTES

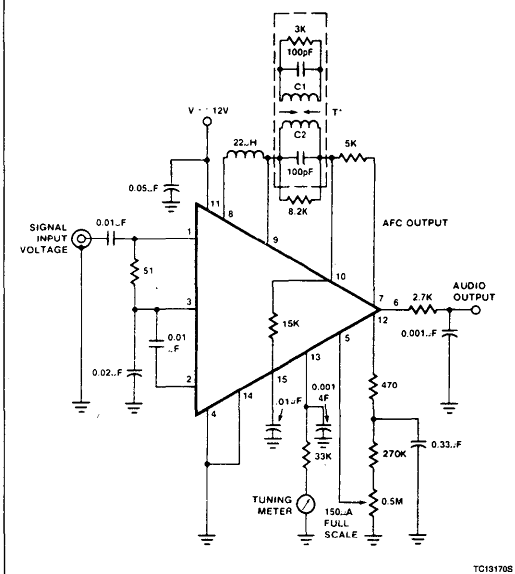
1. THD characteristics and audio level are essentially a function of the phase and Q characteristics of the network connected between Terminals 8, 9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS



NOTES:
1. L tunes with 100pF (C) at 10.7MHz.
2. All resistor values are typical and in ohms.
3. Q_O (unloaded) ≃ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 1. Test Circuit Using a Single-Tuned Detector Coil

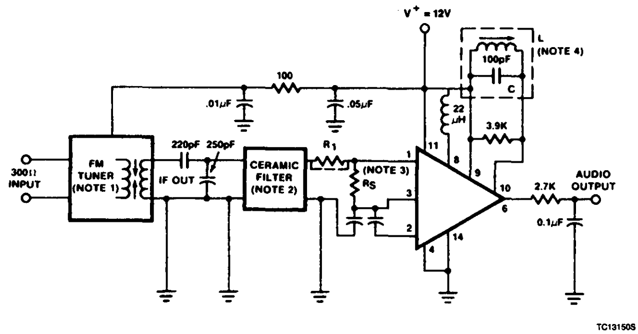


NOTES:
All resistor values are typical and in ohms.

T: Pri — Q_O (unloaded) ≃ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32' dia. form) Sec. – Q (unloaded) ≃ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32' dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C = 150mV)
Above values permit proper operation of mute (squelch) circuit 'E' type slugs, spacing 4mm

Figure 2. Test Circuit Using a Double-Tuned Detector Coil

TEST CIRCUITS



NOTES:
All resistor values are typical and in ohms.
1. Waller 4SN3FIC or equivalent.
2. Murate SFG 10.7mA or equivalent.
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330\Omega$.
4. L tunes with 100pF (C) at 10.7MHz Q_O unloaded ≃ 75 (G.I. EX27825 or equivalent).

Performance data at f_O = 98MHz, f_{MOD} = 400Hz, deviation = ± 74kHz.
± 74kHz.

−3dB limiting sensitivity	2µV (antenna level)
20dB quieting sensitivity	1µV (antenna level)
30dB quieting sensitivity	1.5µV (antenna level)

Figure 3. Typical FM Tuner With a Single-Tuned Detector Coil

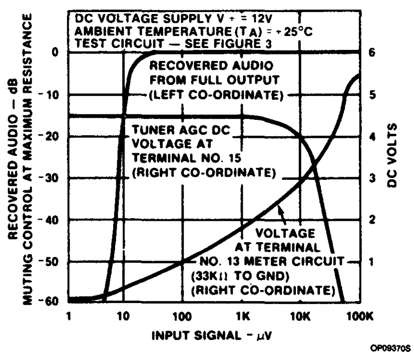
SYSTEM DESIGN CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good bypass capacitors would be ceramic disc with values in the range of 0.01 to 0.05µF.

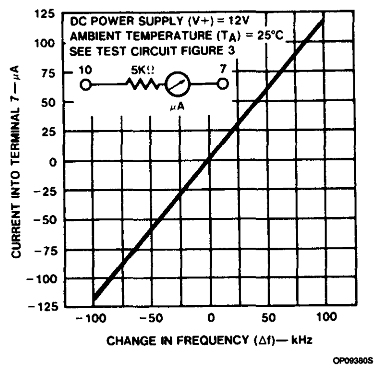
The input impedance of the CA3089 is approximately 10,000Ω. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50Ω and 100Ω is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

Muting Action, Tuner AGC
(Tuning meter output as a function of input signal voltage.)



AFC Characteristics
(Current at Terminal 7 as a function of change in frequency.)



FREQUENCY SYNTHESIZER

The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers, e.g. in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- High-performance phase comparator — low phase noise — low spurii.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
  - frequency offsets
  - ROM compatible
  - fractional channel capability.
- Programme range 6½ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

APPLICATION INFORMATION

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and navaids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to + 15	9,5 to 10,5 V

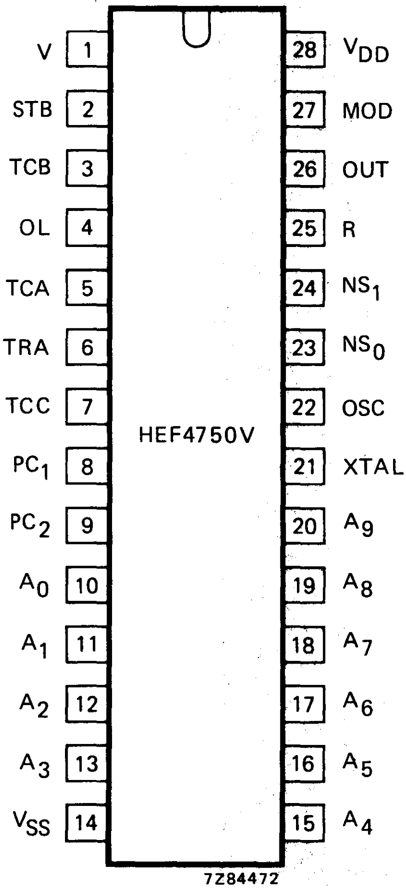


Fig. 1 Pinning diagram.

HEF4750VD: 28-lead DIL; ceramic (cerdip) (SOT135A).

PINNING

R	phase comparator input, reference
V	phase comparator input
STB	strobe input
TCA	timing capacitor C_A pin
TCB	timing capacitor C_B pin
TCC	timing capacitor C_C pin
TRA	biasing pin (resistor R_A)
PC_1	analogue phase comparator output
PC_2	digital phase comparator output
MOD	phase modulation input
OL	out-of-lock indication
OSC	reference oscillator/buffer input
XTAL	reference oscillator/buffer output
A_0 to A_9	programming inputs/programmable divider
NS_0, NS_1	programming inputs, prescaler
OUT	reference divider output

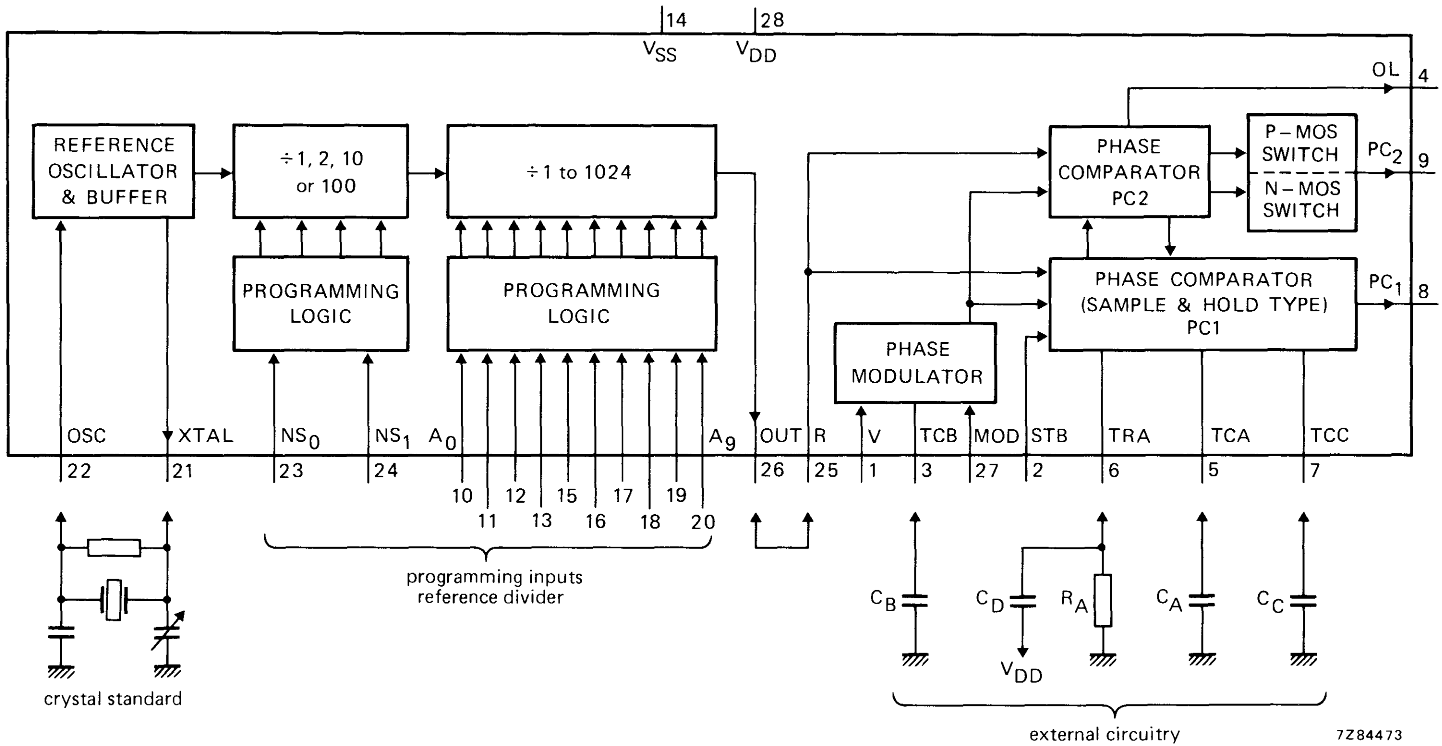


Fig. 2 Block diagram comprising five basic functions: phase comparator 1 (PC1), phase comparator 2 (PC2), phase modulator, reference oscillator and reference divider. These functions are described separately.

N.B. PC_1 = analogue output; PC_2 = 3-state output.

FUNCTIONAL DESCRIPTION

Phase comparator 1

Phase comparator 1 (PC1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V-input causes the hold capacitor (C_A) to be discharged and after a specified delay, caused by the Phase Modulator by means of an internal V′ pulse, it produces a positive-going ramp. A negative-going transition at the R-input terminates the ramp. Capacitor C_A holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to C_C and in turn buffered and made available at output PC_1.

If the ramp terminates before an R-input is present, an internal end of ramp (EOR) signal is produced.

These actions are illustrated in Fig. 3.

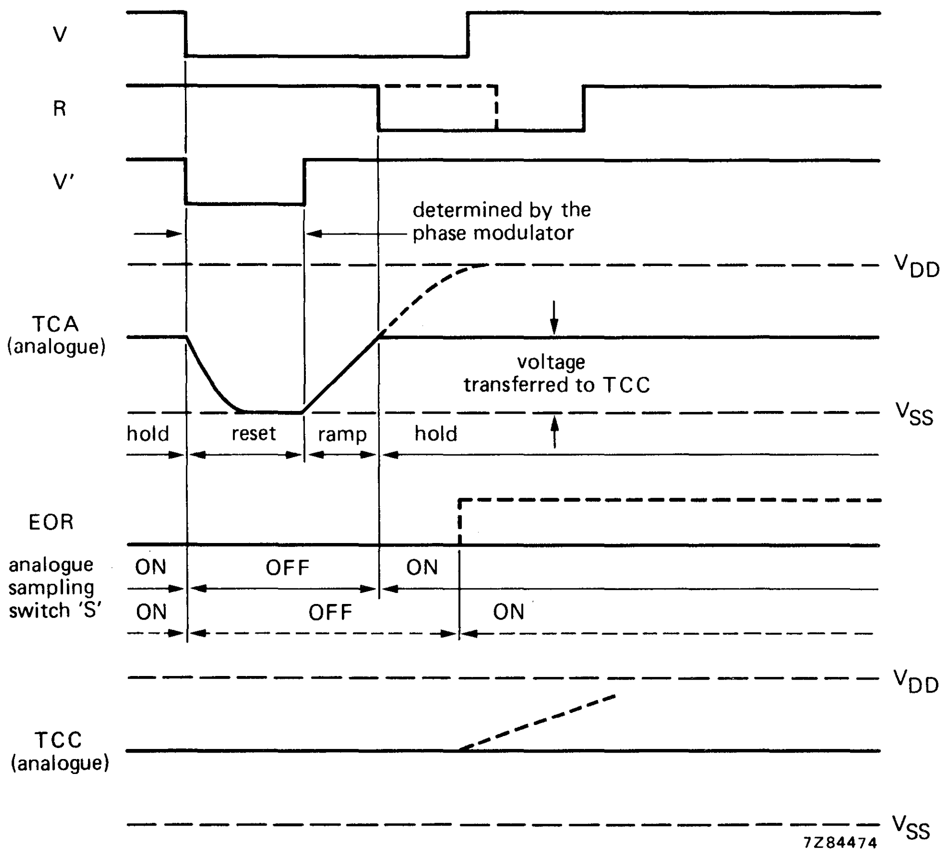


Fig. 3 Waveforms associated with PC1.

The resultant phase characteristic is shown in Fig. 4.

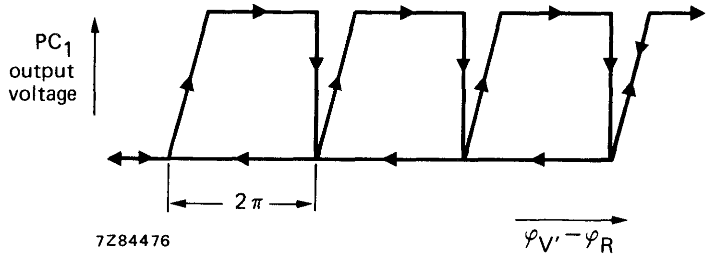


Fig. 4 Phase characteristic of PC_1.

PC1 is designed to have a high gain, typically 3200 V/cycle (at 12,5 kHz). This enables a low noise performance.

Phase comparator 2

Phase comparator 2 (PC2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible. It has a linear ± 360° phase range, which corresponds to a gain of typically 5 V/cycle. This digital phase comparator has three stable states:
— reset state,
— V' leads R state,
— R leads V' state.
Conversion from one state to another takes place according to the state diagram of Fig. 5.

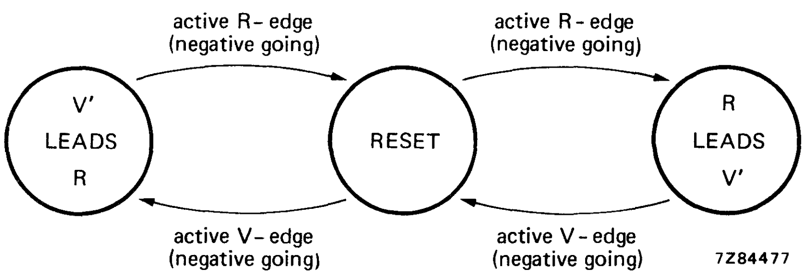


Fig. 5 State diagram of PC2.

Output PC_2 produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and V'. The average output voltage is a linear function of the phase difference. Output PC_2 remains in the high impedance OFF-state in the region in which PC1 operates. The resultant phase characteristic is shown in Fig. 6.

FUNCTIONAL DESCRIPTION (continued)

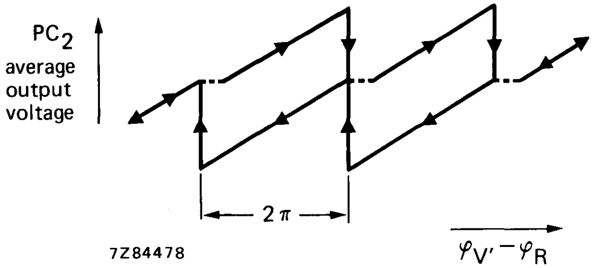


Fig. 6 Phase characteristic of PC_2.

Strobe function

The strobe function is intended for applications requiring extremely fast lock times. In normal operation the additional strobe input (STB) can be connected to the V-input and the circuit will function as described in the previous sections.

In single, phase-locked-loop type frequency synthesizers, the comparison frequency generally used is either the nominal channel spacing or a sub-multiple. PC2 runs at the higher frequency (a higher reference frequency must also be used), whilst strobing takes place on the lower frequency, thereby obtaining a decrease in lock time. In a system using the Universal Divider HEF4751V, the output OFS cycles on the lower frequency, the output OFF cycles on the higher frequency.

Out-of-lock function

There are a number of situations in which the system goes from the locked to the out-of-lock state (OL goes HIGH):

1. When V' leads R, however out of the range of PC1.
2. When R leads V'.
3. When an R-pulse is missing.
4. When a V-pulse is missing.
5. When two successive STB-commands occur, the first without corresponding V-signal.

Phase modulator

The phase modulator only uses one external capacitor, C_B at pin TCB. A negative-going transition at the V-input causes C_B to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MOD), the ramp terminates, C_B discharges and a start signal to the C_A-ramp at TCA is produced. A linear phase modulation is reached in this way.
If no modulation is required, the MOD-input must be connected to a fixed voltage of a certain positive value up to V_{DD}. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of PC1 (C_A) can be discharged during that time. Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.

Reference oscillator

The reference oscillator normally operates with an external crystal as shown in Fig. 2. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable division ratios of 1, 2, 10 and 100, according to the following tables:

- Binary divider

N (A_0 to A_9)	division ratio
0	1024
$0 \leqslant N \leqslant 1023$	N

- Prescaler

programming word (NS_0, NS_1)	division ratio
0	1
1	2
2	10
3	100

In this way suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a 'stand alone' programmable divider by connecting input TRA to V_{DD}, which causes all internal analogue currents to be switched off.

Biasing circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and V_{SS} pins. This circuitry supplies all analogue parts of the circuit. Consequently the analogue properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to V_{DD}, as shown in Fig. 7. The value of C_D has to be chosen such that the TRA input is 'clean', e.g. 10 nF at R_A = 68 kΩ.

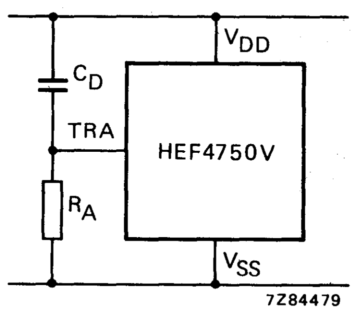


Fig. 7 Decoupling of input TRA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to + 15	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	± I	max. 10	mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max. 500	mW
Power dissipation per output for T_{amb} = 0 to 85 °C	P	max. 100	mW
Storage temperature	T_{stg}	−65 to + 150	°C
Operating ambient temperature	T_{amb}	−40 to + 85	°C

D.C. CHARACTERISTICS at V_{DD} = 10 V ± 5%; voltages are referenced to V_{SS} = 0 V, unless otherwise specified; for definitions see note 1.

parameter	symbol	T_{amb} (°C) −40 min.	typ.	max.	+ 25 min.	typ.	max.	+ 85 min.	typ.	max.	unit	notes
Quiescent device current	I_{DD}	−	−	100	−	−	100	−	−	750	μA	2
Input current; logic inputs, MOD	± I_{IN}	−	−	300	−	−	300	−	−	1000	nA	3
Output leakage current at ½ V_{DD}												3, 4
TCA, hold-state	± I_Z	−	−	20	−	0,05	20	−	−	60	nA	
TCC, analogue switch OFF	± I_Z	−	−	20	−	0,05	20	−	−	60	nA	
PC_2, high impedance OFF-state	± I_Z	−	−	50	−	−	50	−	−	500	nA	
Logic input voltage LOW	V_{IL}	max. 0,3 V_{DD}									V	
HIGH	V_{IH}	min. 0,7 V_{DD}									V	
Logic output voltage LOW; at $\lvert I_O \rvert < 1$ μA	V_{OL}	−	−	50	−	−	50	−	−	50	mV	3
HIGH	V_{OH}	min. V_{DD}−50 mV									mV	3
Logic output current LOW; at V_{OL} = 0,5 V												3
outputs OL, PC_2, OUT	I_{OL}	5,5	−	−	4,6	−	−	3,6	−	−	mA	
output XTAL	I_{OL}	2,8	−	−	2,4	−	−	1,9	−	−	mA	

parameter	symbol	T_{amb} (°C) -40 min.	typ.	max.	+25 min.	typ.	max.	+85 min.	typ.	max.	unit	notes
Logic output current HIGH; at $V_{OH} = V_{DD}-0,5$ V												3
outputs OL, PC_2, OUT	$-I_{OH}$	1,5	–	–	1,3	–	–	1,0	–	–	mA	
output XTAL	$-I_{OH}$	1,4	–	–	1,2	–	–	0,9	–	–	mA	
Output TCC sink current	I_O	–	–	–	–	2,1	–	–	–	–	mA	3,4,5
Output TCC source current	$-I_O$	–	–	–	–	1,9	–	–	–	–	mA	3,4,6
Internal resistance of TCC $\lvert$output swing$\rvert \leqslant 200$ mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	0,7	–	–	–	–	kΩ	3,4
Output TCC voltage with respect to TCA input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,7
Output PC_1 sink current	I_O	–	–	–	–	1,1	–	–	–	–	mA	3,4,8
Output PC_1 source current	$-I_O$	–	–	–	–	1,0	–	–	–	–	mA	3,4,9
Internal resistance of PC_1 $\lvert$output swing$\rvert \leqslant 200$ mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	1,4	–	–	–	–	kΩ	3,4
Output PC_1 voltage with respect to TCC input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,10
EOR generation $V_{EOR} = V_{DD}-V_{TCA}$	V_{EOR}	–	0,9	–	–	0,7	–	–	0,6	–	V	3,4,11
Source current; HIGH at $V_{OUT} = ½ V_{DD}$; output in ramp mode												3,4
TCA	I_O	–	–	–	–	13	–	–	–	–	mA	
TCB	I_O	–	–	–	–	2,5	–	–	–	–	mA	

A.C. CHARACTERISTICS

General note

The dynamic specifications are given for the circuit built-up with external components as given in Fig. 8, under the following conditions; for definitions see note 1; for definitions of times see Fig. 19; V_{DD} = 10 V ± 5%; T_{amb} = 25 °C; input transition times ≤ 20 ns; R_A = 68 kΩ ± 30% (see also note 4); C_A = 270 pF; C_B = 150 pF; C_C = 1 nF; C_D = 10 nF; unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions	notes
Slew rate							
TCA	S_{TCA}	–	52	–	V/µs	R_A = minimum	12
TCA	S_{TCA}	–	28	–	V/µs	R_A = maximum	12
TCB	S_{TCB}	–	20	–	V/µs	R_A = minimum	12
TCB	S_{TCB}	–	10	–	V/µs	R_A = maximum	12
Ramp linearity							
TCA	l_{TCA}	–	2	–	%		13
TCB	l_{TCB}	–	2	–	%		13
Start of TCA-ramp delay	t_{CBCA}	–	200	–	ns		
Delay of TCA-hold	t_{RCA}	–	40	–	ns		
Delay of TCA-discharge	t_{VCA}	–	60	–	ns		
Start of TCB-ramp delay	t_{VCB}	–	60	–	ns		
TCB-ramp duration	t_{rCB}	–	250	–	ns	V_{MOD} = 4 V	
	t_{rCB}	–	350	–	ns	V_{MOD} = 6 V	
	t_{rCB}	–	450	–	ns	V_{MOD} = 8 V	
Required TCB min. ramp duration	t_{rCB}	–	150	–	ns		14
Pulse width							
V : LOW	t_{PWVL}	–	20	–	ns		
V : HIGH	t_{PWVH}	–	20	–	ns		
R : LOW	t_{PWRL}	–	20	–	ns		
R : HIGH	t_{PWRH}	–	20	–	ns		
STB : LOW	t_{PWSL}	–	20	–	ns		
STB : HIGH	t_{PWSH}	–	20	–	ns		
Fall time							
TCA	t_{fCA}	–	50	–	ns		
TCB	t_{fCB}	–	50	–	ns		
Prescaler input frequency	f_{PR}	–	30	–	MHz	all division ratios	
Binary divider frequency	f_{DIV}	–	30	–	MHz	all division ratios	
Crystal oscillator frequency	f_{OSC}	–	10	–	MHz		
Average power supply current						locked state	
with speed-up 1 : 10	I_P	–	3,6	–	mA		15
without speed-up	I_P	–	3,2	–	mA		16

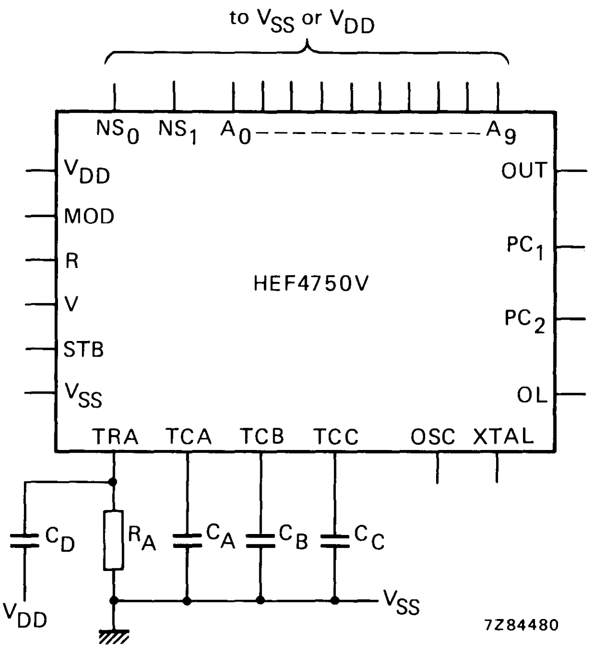


Fig. 8 Test circuit for measuring a.c. characteristics.

NOTES

1. Definitions:
   R_A = external biasing resistor between pins TRA and V_{SS}; 68 kΩ ± 30%.
   C_A = external timing capacitor for time/voltage converter, between pins TCA and V_{SS}.
   C_B = external timing capacitor for phase modulator, between pins TCB and V_{SS}.
   C_C = external hold capacitor between pins TCC and V_{SS}.
   C_D = decoupling capacitor between pins TRA and V_{DD}.
   Logic inputs: V, R, STB, A_0 to A_9, NS_0, NS_1, OSC.
   Logic outputs: OL, PC_2, XTAL, OUT.
   Analogue signals: TCA, TCB, TCC, TRA, PC_1, MOD.
2. TRA at V_{DD}; TCA, TCB, TCC and MOD at V_{SS}; logic inputs at V_{SS} or V_{DD}.
3. All logic inputs at V_{SS} or V_{DD}.
4. R_A connected; its value chosen such that I_{TRA} = 100 μA.
5. The analogue switch is in the ON position (see Fig. 9).

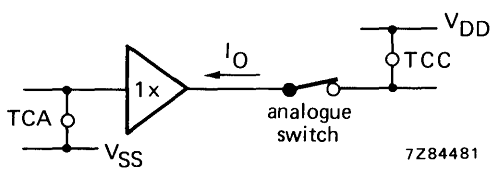


Fig. 9 Equivalent circuit for note 5.

NOTES (continued)

6. The analogue switch is in the ON position (see Fig. 10).

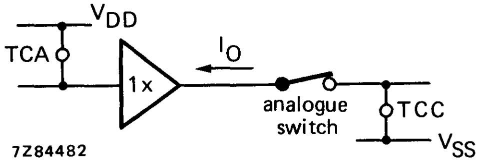


Fig. 10 Equivalent circuit for note 6.

7. This guarantees the d.c. voltage gain, combined with d.c.-offset.
   Input condition: 0,3 $V_{DD} \leqslant V_{TCA} \leqslant 0{,}7\ V_{DD}$.
   $\Delta V = V_{TCC} - V_{TCA}$.

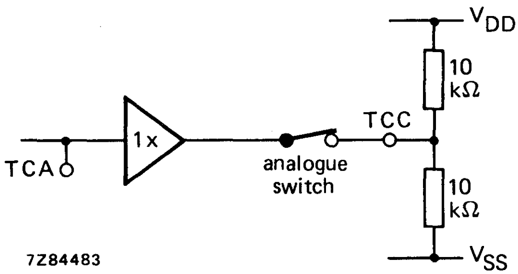


Fig. 11 Circuit for note 7.

8.

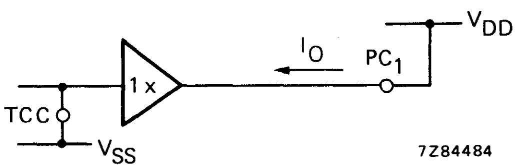


Fig. 12 Equivalent circuit for PC_1 sink current.

9.

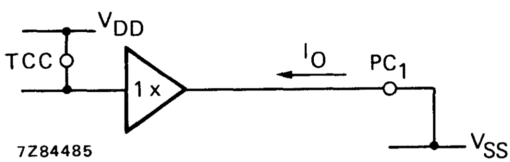


Fig. 13 Equivalent circuit for PC_1 source current.

10. This guarantees the d.c. voltage gain, combined with d.c.-offset.
    Input condition: 0,3 $V_{DD} \leqslant V_{TCC} \leqslant 0{,}7\ V_{DD}$.
    $\Delta V = V_{PC1} - V_{TCC}$.

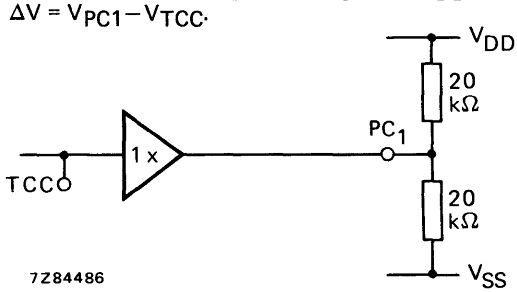


Fig. 14 Circuit for note 10.

11. Switching level at TCA, generating an EOR-signal, during increasing input voltage.
12.

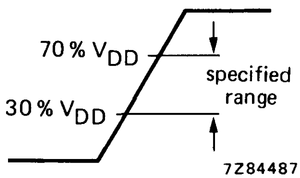


Fig. 15 Waveform at the output.

13. Definition of the ramp linearity at full swing.

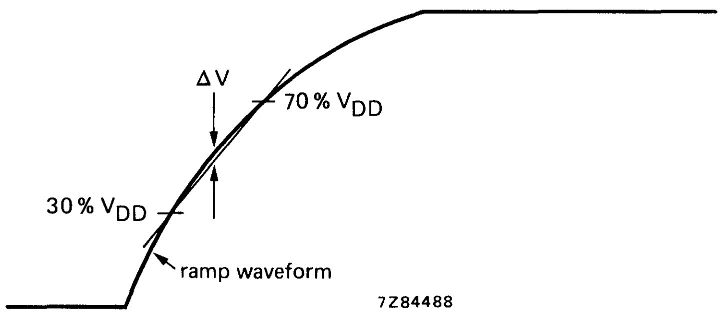


Fig. 16 ΔV is the maximum deviation of the ramp waveform to the straight line, which joins the 30% V_{DD} and 70% V_{DD} points.

$$\text{Linearity} = \frac{\Delta V}{\frac{1}{2} V_{DD}} \times 100\%.$$

14. The external components and modulation input voltage must be chosen such that this requirement will be fulfilled, to ensure that C_A is sufficiently discharged during that time.

NOTES (continued)

15. Circuit connections for power supply current specification, with speed-up 1 : 10. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
f_{OSC} = 5 MHz (external clock)
f_{STB} = 12,5 kHz
f_V = 125 kHz

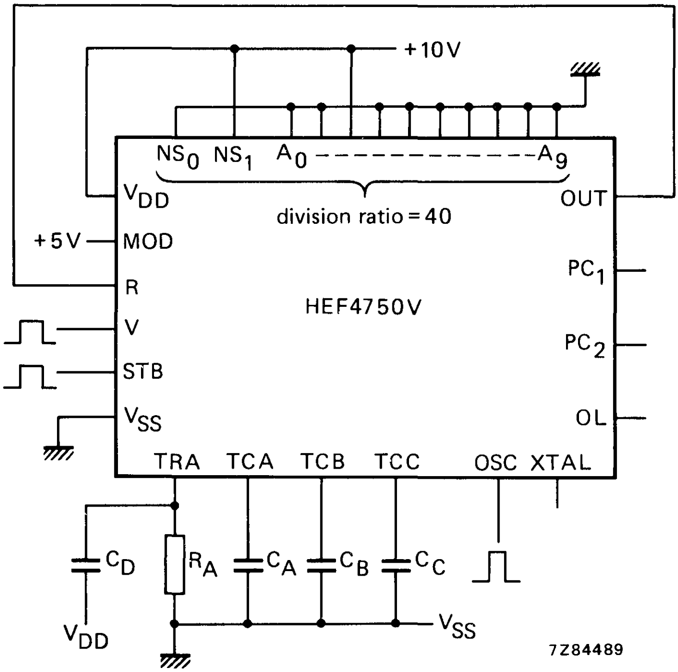


Fig. 17 Circuit for note 15.

16. Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
f_{OSC} = 5 MHz (external clock)
f_{STB} = 12,5 kHz
f_V = 12,5 kHz

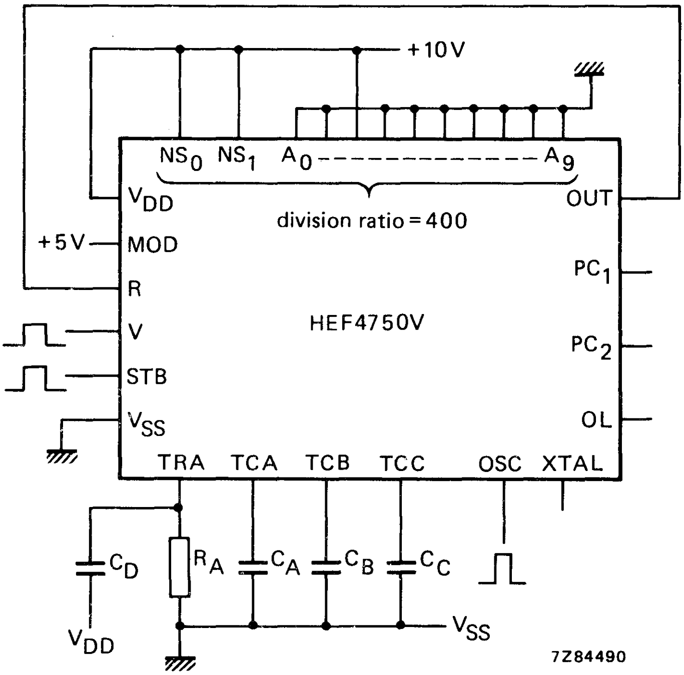
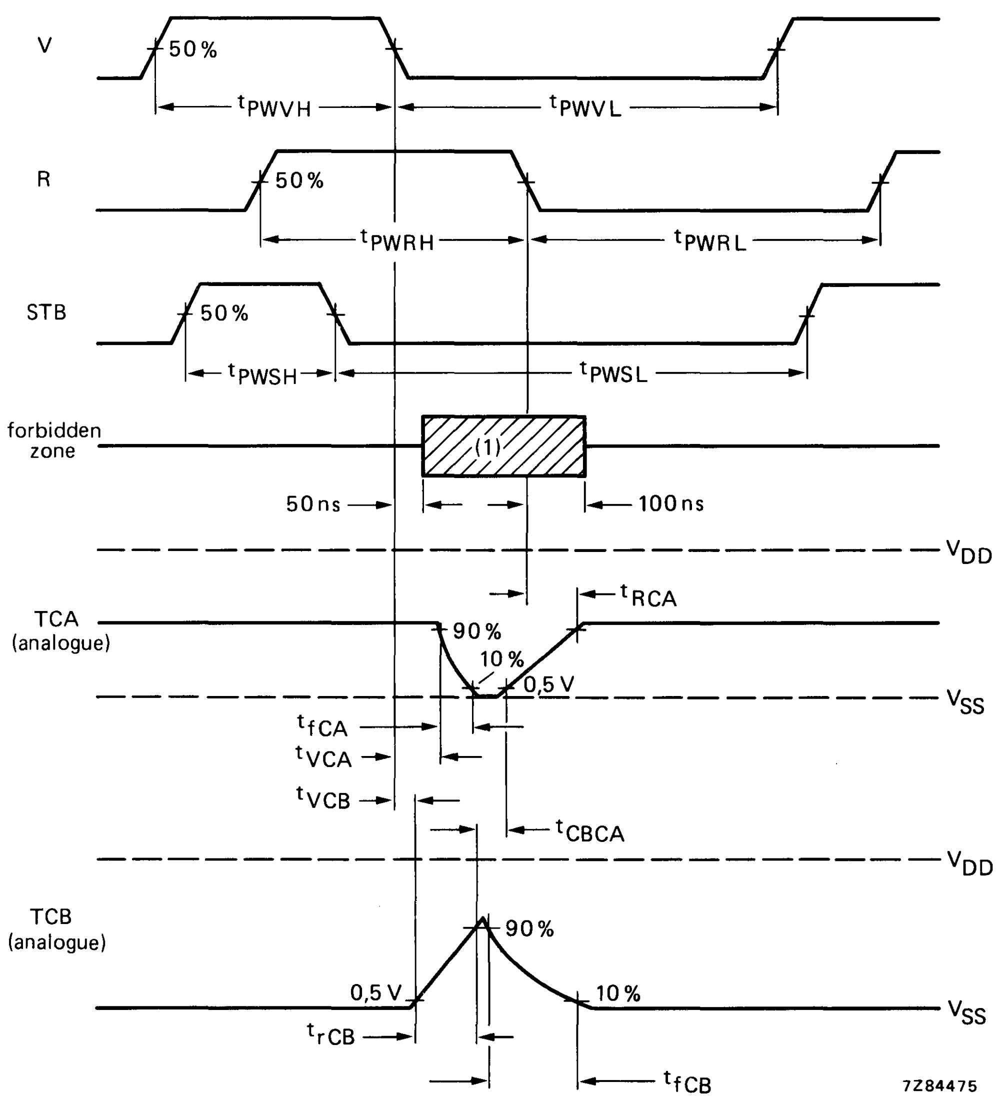


Fig. 18 Circuit for note 16.



(1) Forbidden zone in the *locked state* for the positive edge of V and R and both edges of STB.

Fig. 19 Waveforms showing times in the locked state.

UNIVERSAL DIVIDER

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷10/11 prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leqslant M \leqslant 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format.
To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.
The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D.
The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

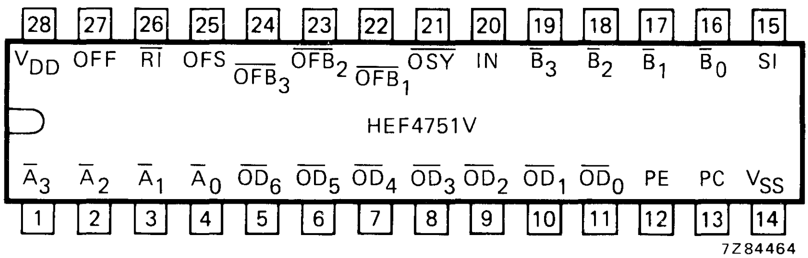


Fig. 1 Pinning diagram.

SUPPLY VOLTAGE

rating	recommended operating
−0,5 to +18	4,5 to 12,5 V

HEF4751VP : 28-lead DIL; plastic (SOT117).
HEF4751VD: 28-lead DIL; ceramic (cerdip) (SOT135A).
HEF4751VT : 28-lead mini-pack; plastic (SO28; SOT136A).

FAMILY DATA
I_{DD} LIMITS category LSI
} see Family Specifications

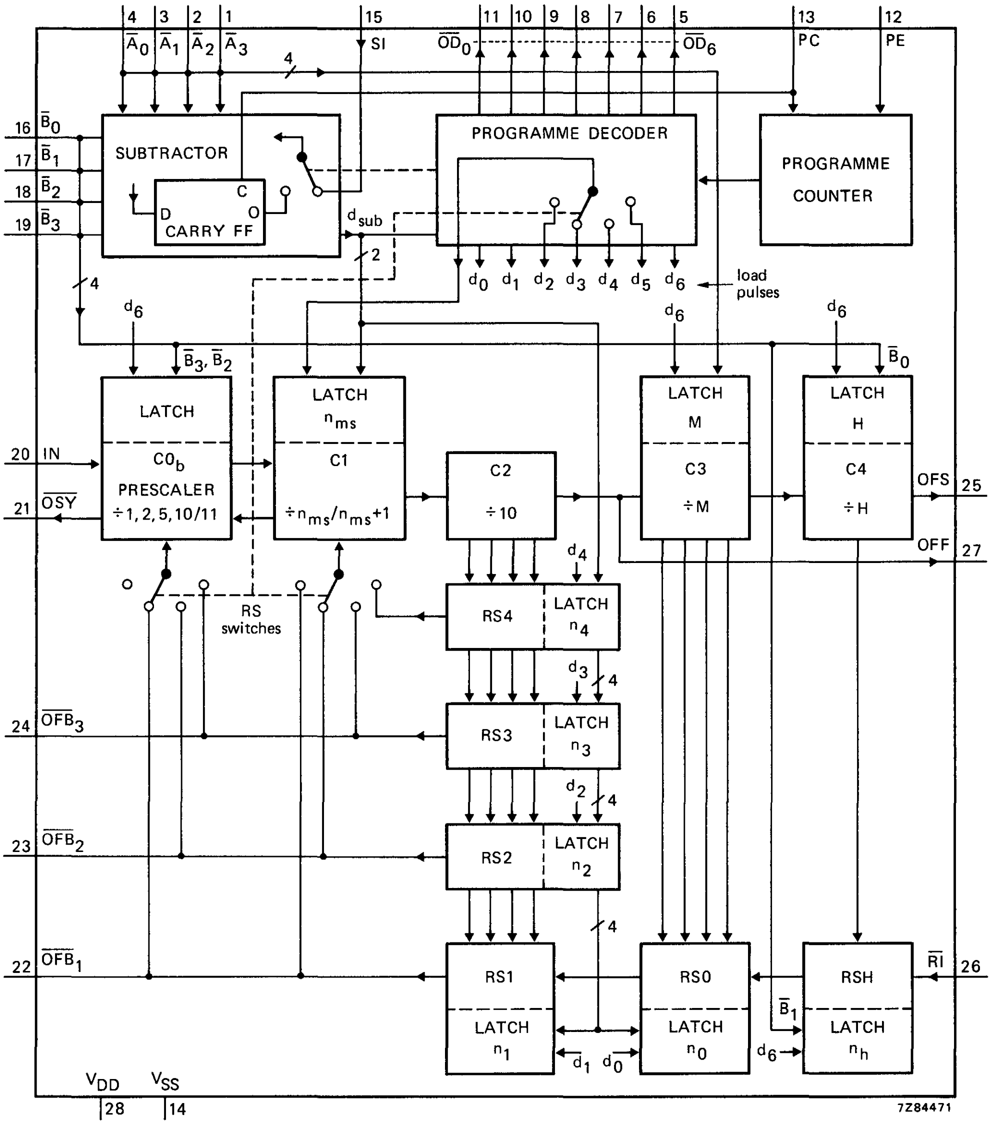


Fig. 2 Block diagram.

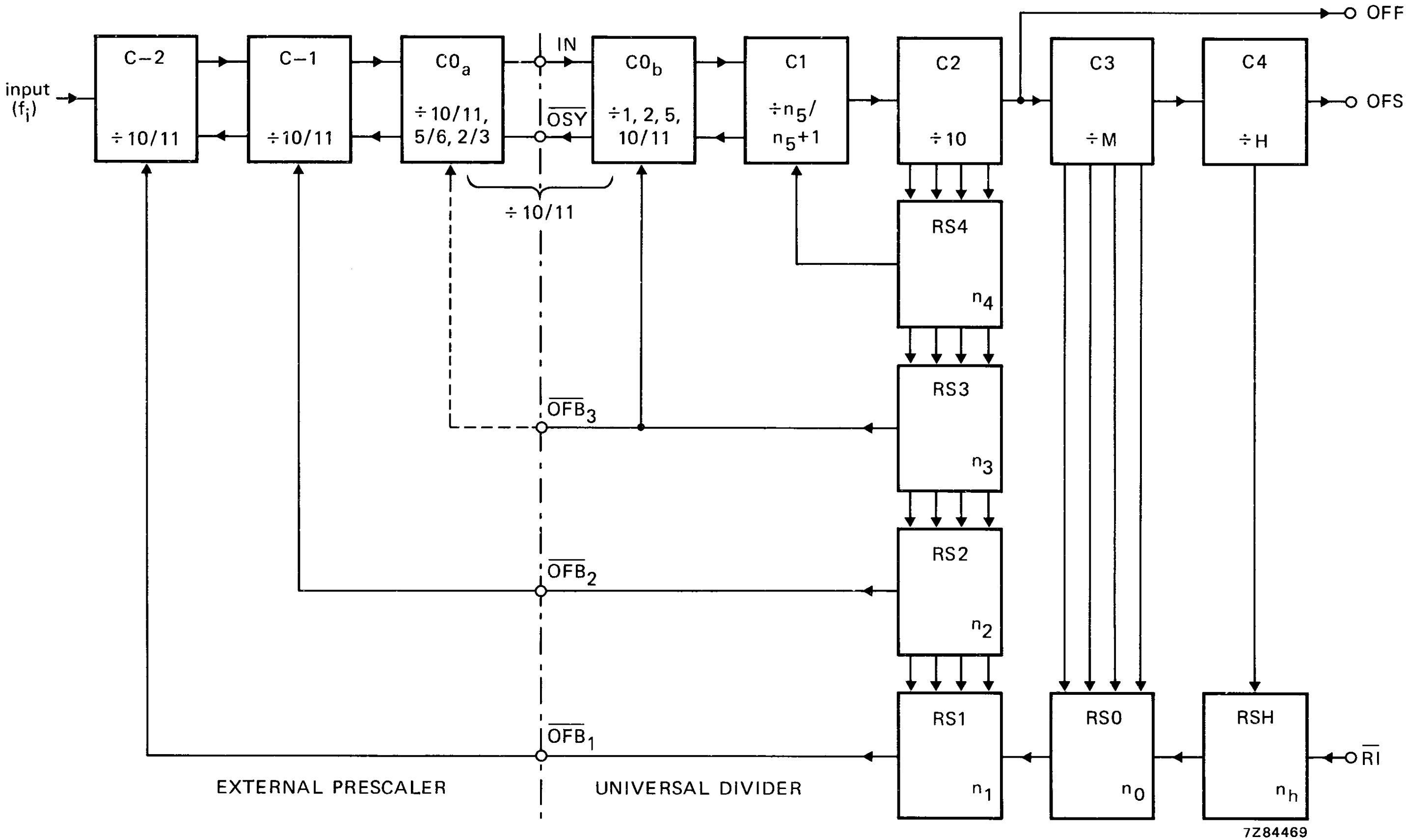


Fig. 3 The HEF4751V U.D. used in a system with 3 (fast) prescalers.
$1 \leqslant M \leqslant 16$; $1 \leqslant H \leqslant 2$; $n_5 > 0$; $f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1)\, M + n_0\}\, H + n_h$.

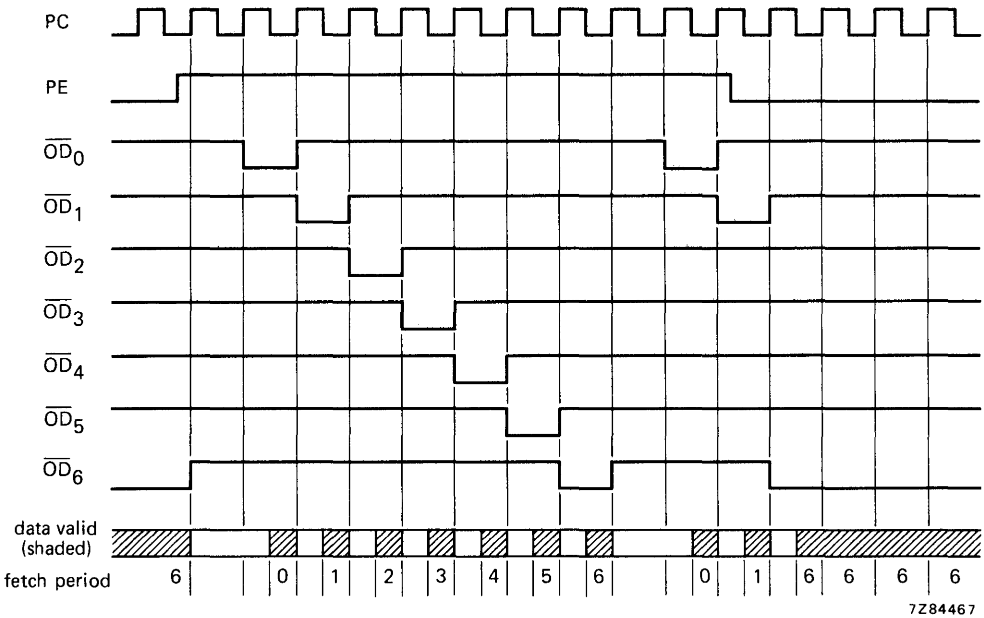


Fig. 4 Timing diagram showing programme data inputs.

Allocation of data input

fetch period	inputs $\overline{A}_3$ $\overline{A}_2$ $\overline{A}_1$ $\overline{A}_0$	$\overline{B}_3$ $\overline{B}_2$	$\overline{B}_1$ $\overline{B}_0$	SI
0	n_{0A}	n_{0B}		b_{in}
1	n_{1A}	n_{1B}		X
2	n_{2A}	n_{2B}		X
3	n_{3A}	n_{3B}		X
4	n_{4A}	n_{4B}		X
5	n_{5A}	n_{5B}		X
6	M	CO_b control	½ channel control	X

Allocation of data input $\overline{B}_3$ to $\overline{B}_0$ during fetch period 6

$\overline{B}_3$	$\overline{B}_2$	CO_b division ratio
L	L	1
L	H	2
H	L	5
H	H	10/11

$\overline{B}_1$	$\overline{B}_0$	½ channel configuration
L	L	H = 1
L	H	H = 2; n_h = 0
H	H	H = 2; n_h = 1
H	L	test state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PROGRAMME DATA INPUT (see also Figs 3 and 4)

The programming process is timed and controlled by input PC and PE. When the programme enable (PE) input is HIGH, the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs ($\overline{OD}_0$ to $\overline{OD}_6$). These data address signals may be used to address the external programme source. The data fetched from the programme source is applied to inputs $\overline{A}_0$ to $\overline{A}_3$ and $\overline{B}_0$ to $\overline{B}_3$. When PC is LOW in a fetch period an internal load pulse is generated, the data is valid during this time and has to be stable. When PE is LOW, the programming cyclus is interrupted on the first positive edge of PC. On the next negative edge at input PC fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the U.D. need programme input signals (see Fig. 2). Four of these (CO_b, C3, C4 and RSH) are concerned with the configuration of the U.D. and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5.

$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$

These digits are formed by a substractor from two external numbers A and B and a borrow-in (b_{in}).

$P = A - B - b_{in}$ or if this result is negative; $P = A - B - b_{in} + M \cdot 10^5$.

The numbers A and B, each consisting of six four bit digits n_{0A} to n_{5A} and n_{0B} to n_{5B}, are applied in fetch period 0 to 5 to the inputs $\overline{A}_0$ to $\overline{A}_3$ (data A) and $\overline{B}_0$ to $\overline{B}_3$ (data B) in binary coded negative logic.

$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}.$

$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}.$

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH: borrow, SI = LOW: no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{ms}) from the internal digits n_5 to n_2 of number P. The counter chain C − 2 to C1 (see Fig. 3) is fully programmable by the use of pulse rate feedback.

Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h respectively. In fetch period 6 the fractional counter C3, half channel counter C4 and CO_b are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: M = 16). The counter CO is a side steppable 10/11 counter composed of an internal part CO_b and an external part CO_a. CO_b is configured via $\overline{B}_3$ and $\overline{B}_2$ to a division ratio of 1 or 2 or 5 or 10/11; CO_a must have the complementary ratio 10/11 or 5/6 or 2/3 or 1 respectively. In the latter case CO_b comprises the whole CO counter with internal feedback, CO_a is then not required.

The half channel counter C4 is enabled with $\overline{B}_0$ = HIGH and disabled with $\overline{B}_0$ = LOW. With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1$ = HIGH, and no offset with $\overline{B}_1$ = LOW.

FEEDBACK TO PRESCALERS (see also Figs 5 and 6)

The counters C1, C0, C–1 and C–2 are side-steppable counters, i.e. its division ratio may be increased by one, by applying a pulse to a control terminal for the duration of one division cycle. Counter C2 has 10 states, which are accessible as timing signals for the rate selectors RS1 to RS4. A rate selector, programmed with n (n_1 to n_4 in the U.D.) generates n of 10 basic timing periods an active signal. Since $n \leqslant 9$, 1 of 10 periods is always non-active. In this period RS1 transfers the output of rate selector RS0, which is timed by counter C3 and programmed with n_0. Similarly, RS0 transfers RSH output during one period of C3. Rate selector RSH is timed by C4 and programmed with n_h. In one of the two states of C4, if enabled, or always, if C4 is disabled, RSH transfers the LOW active signal at input $\overline{RI}$ to RS0. If $\overline{RI}$ is not used it must be connected to HIGH. The feedback output signals of RS1, RS2 and RS3 are externally available as active LOW signals at outputs $\overline{OFB}_1$, $\overline{OFB}_2$ and $\overline{OFB}_3$.

Output $\overline{OFB}_1$ is intended for the prescaler at the highest frequency (if present), $\overline{OFB}_2$ for the next (if present) and $\overline{OFB}_3$ for the lowest frequency prescaler (if present). A prescaler needs a feedback signal, which is timed on one of its own division cycles in a basic timing period. The timing signal at $\overline{OSY}$ is LOW during the last U.D. input period of a basic timing period and is suitable for timing of the feedback for the last external prescaler. The synchronization signal for a preceding prescaler is the OR-function of the sync. input and sync. output of the following prescaler (all sync. signals active LOW).

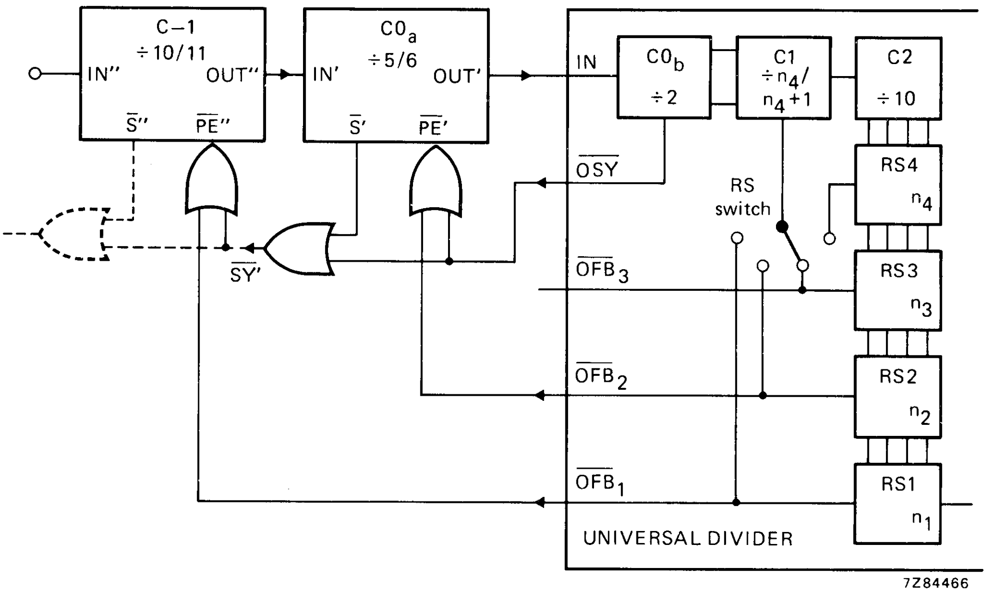


Fig. 5 Block diagram showing feedback to prescalers.

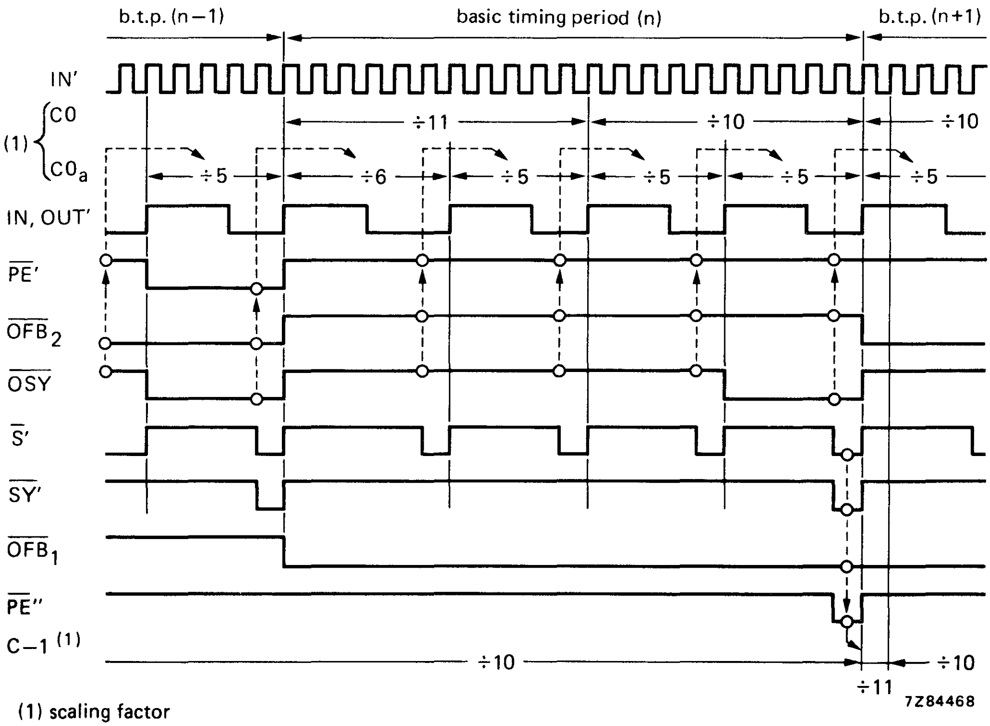


Fig. 6 Timing diagram showing signals occurring in Fig. 5.

CASCADING OF U.D.s (see also Fig. 8)

A U.D. is programmed into the 'slave' mode by the programme input data: $n_{2A} = 11$, $n_{2B} = 10$, $n_{3A} = n_{4A} = n_{3B} = n_{4B} = n_{5B} = 0$. A U.D. operating in the slave mode performs the function of two extra programmable stages C2' and C3' to a 'master' (not slave) mode operating U.D. More slave U.D.s may be used, every slave adding two lower significant digits to the system.

Output $\overline{OFB}_3$ is converted to the borrow output of the programme data subtractor, which is valid after fetch period 5. Input SI is the borrow input (both in master and in slave mode), which has to be valid in fetch period 0. Input SI has to be connected to output $\overline{OFB}_3$ of a following slave, if not present, to LOW. For proper transfer of the borrow from a lower to a higher significant U.D. subtractor, the U.D.s have to be programmed sequentially in order of significance or synchronously if the programme is repeated at least the number of U.D.s in the system.

Rate input $\overline{RI}$ and output OFS must be connected to rate output $\overline{OFB}_1$ and the input IN of the next slave U.D. The combination thus formed retains the full programmability and features of one U.D.

OUTPUT (see also Fig. 7)

The normal output of the U.D. is the slow output OFS, which consists of evenly spaced LOW pulses. This output is intended for accurate phase comparison. If a better frequency acquisition time is required, the fast output OFF can be used. The output frequency on OFF is a factor M • H higher than the frequency on OFS. However, phase jitter of maximum ±1 system input period occurs at OFF, since the division ratio of the counters preceding OFF are varied by slow feedback pulse trains from rate selectors following OFF.

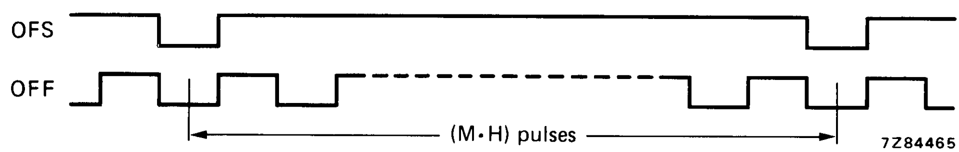


Fig. 7 Timing diagram showing output pulses.

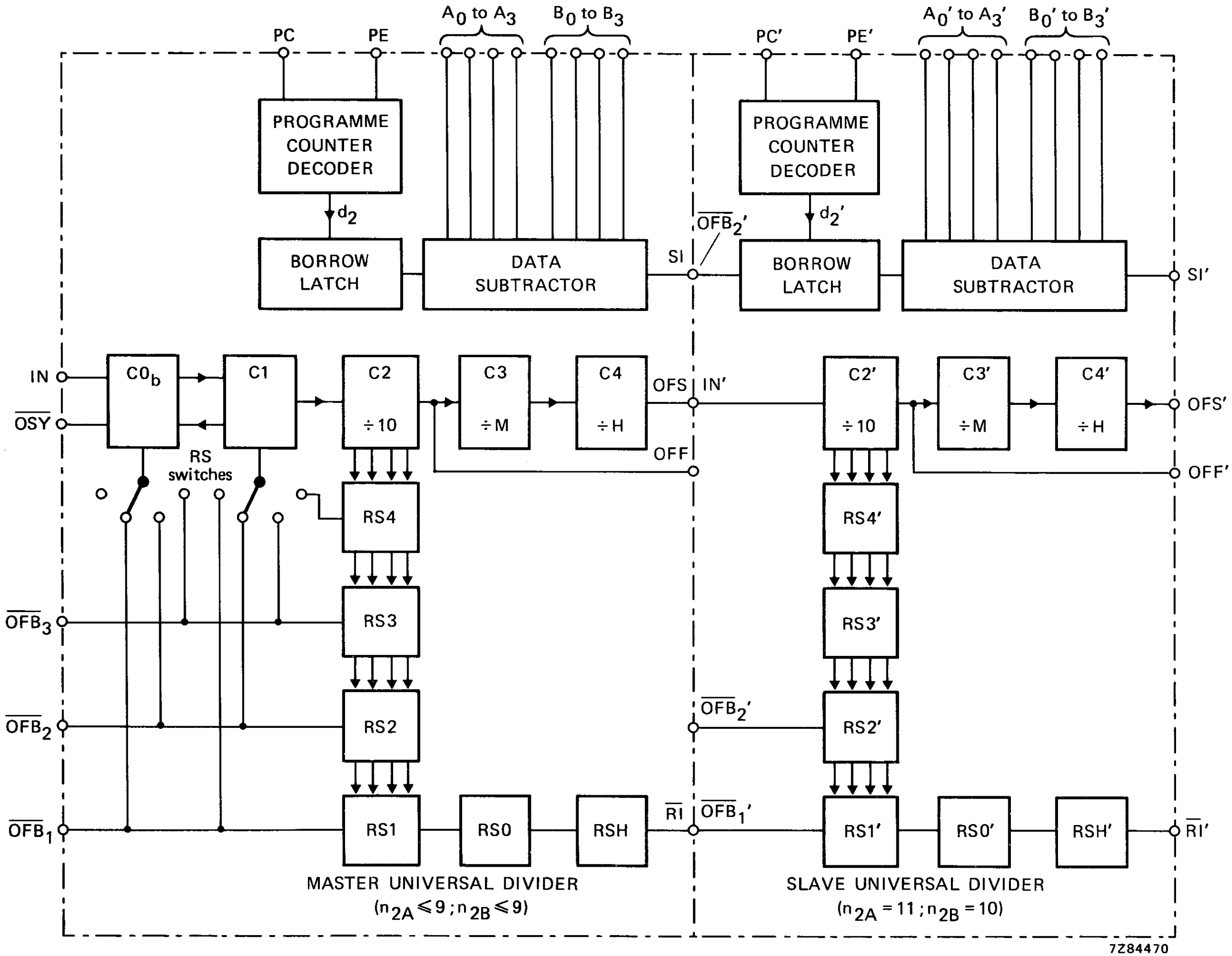


Fig. 8 Block diagram showing cascading of U.Ds.

D.C. CHARACTERISTICS $V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	max.	+25 min.	max.	+85 min.	max.
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6		1,4		1,1	mA
	5		0,4		1,7		1,5		1,2	mA
	10		0,5		2,9		2,7		2,2	mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	1,0		0,85		0,55	mA
	5	2,5			3,0		2,5		1,7	mA
	10	9,5			3,0		2,5		1,7	mA

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times $\leqslant 20$ ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit	
Propagation delay IN ⟶ $\overline{OSY}$ HIGH to LOW	5	t_{PHL}		135	270	ns	$C_L = 10$ pF
	10			45	90	ns	
Output transition times HIGH to LOW	5	t_{THL}		30	60	ns	$C_L = 50$ pF
	10			12	25	ns	
LOW to HIGH	5	t_{TLH}		45	90	ns	$C_L = 50$ pF
	10			20	40	ns	
Maximum input frequency; IN	5	f_{max}	4	8		MHz	$\delta = 50\%$
	10		12	24		MHz	CO_b ratio > 1
Maximum input frequency; IN	5	f_{max}	2	4		MHz	$\delta = 50\%$
	10		6	12		MHz	CO_b ratio = 1
Maximum input frequency; PC	5	f_{max}	0,15	0,3		MHz	
	10		0,5	1,0		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF)
	10	$5\,400\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	$\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)

FOR DETAILED INFORMATION SEE RELEVANT DATABOOK OR DATASHEET.

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84X1 family of microcontrollers is fabricated in NMOS. The family consists of 5 devices:

- MAB8401 – 128 bytes RAM, external program memory, with 8-bit LED-driver (10mA), emulation of MAB/F8422/42* possible
- MAB/MAF8411 – 1K byte ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8421 – 2K bytes ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8441 – 4K bytes ROM/128 bytes RAM plus 8-bit LED-driver
- MAB/MAF8461 – 6K bytes ROM/128 bytes RAM plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer/event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "8-bit Single-chip Microcontrollers user manual".

* See data sheet on MAB/F8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

0 to + 70 °C	MAB84X1 family
−40 to + 85 °C	MAF84X1 family only
−40 to + 110 °C	MAF84AX1 family only

PACKAGE OUTLINES

MAB8401B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8401WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT188).
MAB/MAF8411/21/41/61P: 28-lead DIL; plastic (SOT117).
MAF84A11/21/41/61P: 28-lead DIL; plastic (SOT117).
MAB8411/21/41/61T: 28-lead mini-pack; plastic (SO28; SOT163A).

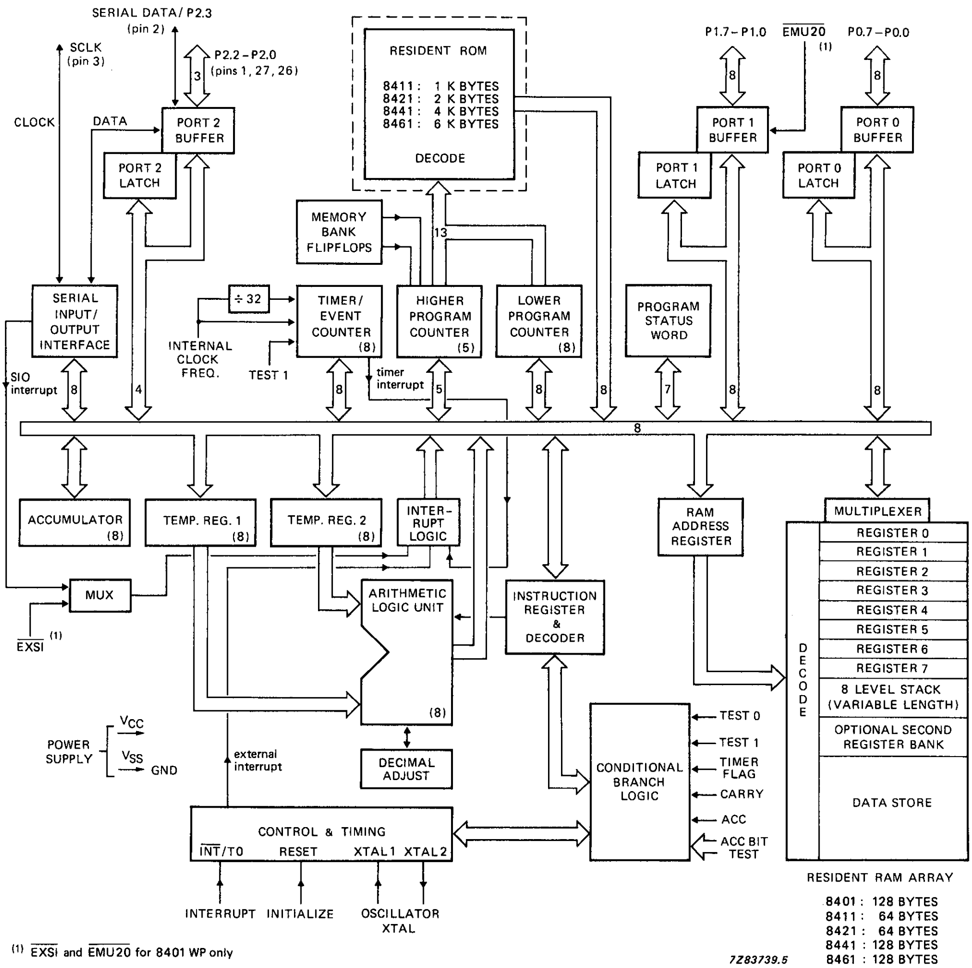
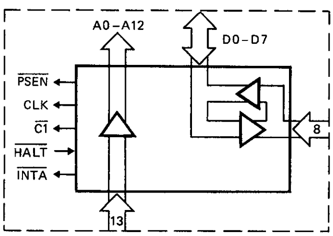


Fig. 4a Block diagram of the MAB84X1 family.



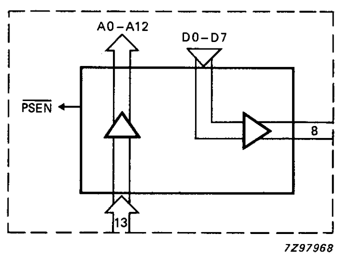


Fig. 4b Replacement for dotted part in Fig. 4a for the MAB8401WP bond-out version.

Fig. 4c Replacement of dotted part in Fig. 4a for the MAB8401B 'Piggy-back' version.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8421/8441 microcontrollers. The versions are:

- MAB8422 - 2K x 8 ROM/64 bytes RAM
- MAB8442 - 4K x 8 ROM/128 bytes RAM

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P1.0 and P1.1 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P2.0 - P2.2) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^{2}C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^{2}C-bus control is available upon request. For detailed information see the user manual 'Single-chip 8-bit microcontrollers'.

Features

- 8-bit: CPU, ROM, RAM and I/O
- 20 pin package
- MAB8422: 2K x 8 ROM/64 bytes RAM
- MAB8442: 4K x 8 ROM/128 bytes RAM
- 13 quasi-bidirectional I/O port lines
- Two testable inputs T1 and $\overline{INT}$/T0
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^{2}C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P1.0 and P1.1 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single power supply
- Operating temperature ranges: 0 to +70 °C (MAB84X2)
  –40 to +85 °C (MAF84X2)
  –40 to +110 °C (MAF84AX2)

PACKAGE OUTLINES

MAB/MAF84X2, MAF84AX2: 20-lead DIL; plastic (SOT146).

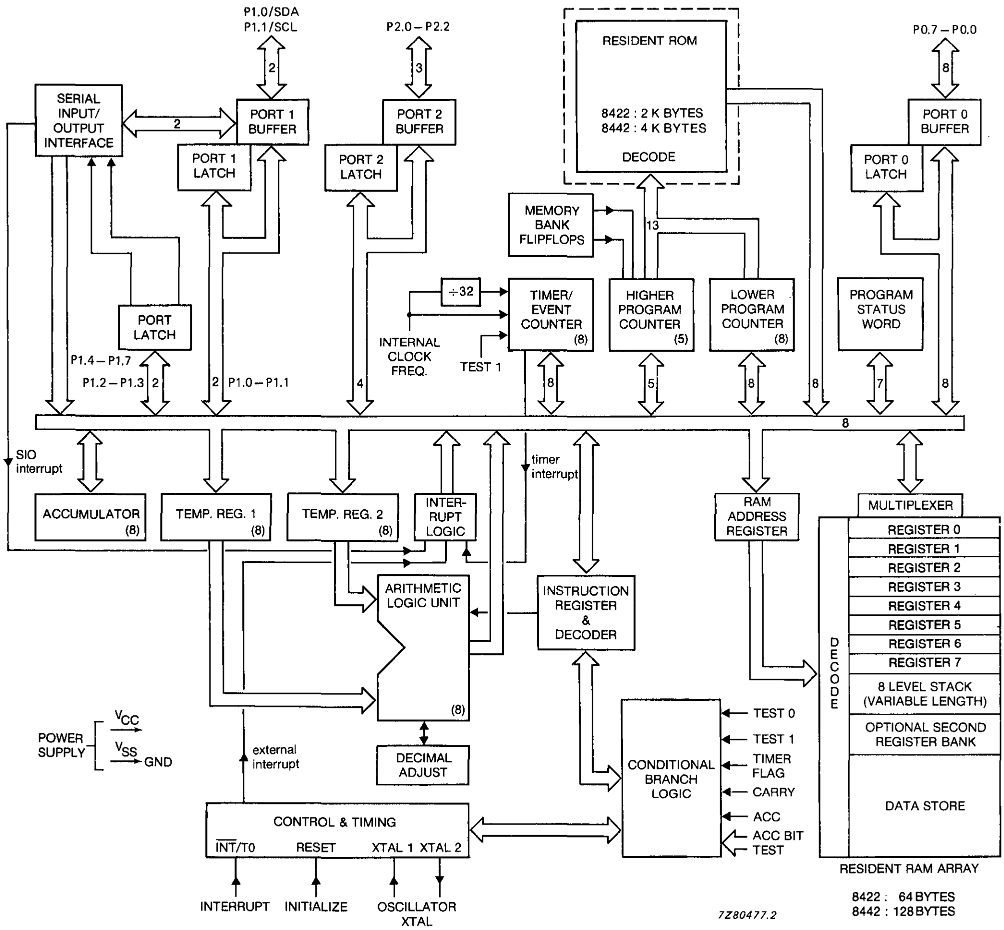


Fig. 1 Block diagram of the MAB8422/8442.

MC3410, MC3510, MC3410C
10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Signetics' design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

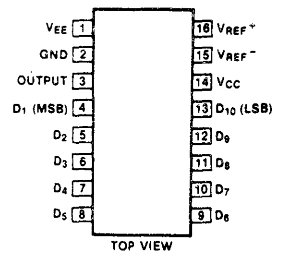
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed monotonicity over temperature**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **Wide output voltage compliance range**
- **High-speed multiplying input slew rate — 20mA/µs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

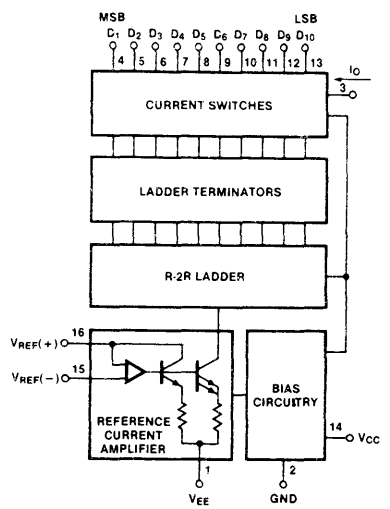
PIN CONFIGURATION

F Package



TOP VIEW

BLOCK DIAGRAM



10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	MC3410F
16-Pin Cerdip	0 to +70°C	MC3410CF
16-Pin Cerdip	−55°C to +125°C	MC3510F

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise noted

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} V_{EE}	Power supply	+7.0 −18	V_{DC} V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	0.5, −5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating ambient temperature range MC3510 MC3410, 3410C	 −55 to +125 0 to +70	 °C °C
T_J	Junction temperature, ceramic package	+150	°C
P_D	Maximum power dissipation, $T_A = 25°C$ (still-air)[1] F package	1190	mW

NOTE:
1. Derate above 25°C, at the following rates:
F package at 9.5mW/°C

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = + 5.0V_{DC}, V_{EE} = − 15$_{DC}$, $\frac{V_{REF}}{R16}$ = 2.0mA, all digital inputs at high logic level.

MC3510: T_A = −55°C to + 125°C, MC3410 Series: T_A = 0°C to + 70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3410, MC3510			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (error relative to full-scale I_O)	T_A = 25°C			±0.05			±0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (relative to full-scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_S	Settling time to within ± 1/2 LSB (all bits LOW-to-HIGH)	T_A = 25°C		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0"		2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) HIGH-level, V_{IH} = 5.5V LOW-level, V_{IL} = 0.8V			−0.05	+.04 −0.4		−0.05	+.04 −0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0		−1.0	−5.0	μA
I_{OR}	Output current range			4.0	5.0		4.0	5.0	mA
I_{OH}	Output current (all bits high)	V_{REF} = 2.000V, R_{16} = 1000Ω	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output current (all bits low)	T_A = 25°C		0	2.0		0	4.0	μA
V_O	Output voltage compliance	T_A = 25°C			−2.5 +0.2			−2.5 +0.2	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20			20		mA/μs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0			2.0		μs
PSRR(−)	Output current power supply sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output capacitance	V_O = 0		25			25		pF
C_I	Digital input capacitance (all bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			−11.4	+18 −20		−11.4	+18 −20	mA
V_{CC} V_{EE}	Power supply voltage range	T_A = 25°C	+4.75 −14.25	+5.0 −15	+5.25 −15.75	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption (all bits low) (all bits high)			220 200	380		220 200	380	mW

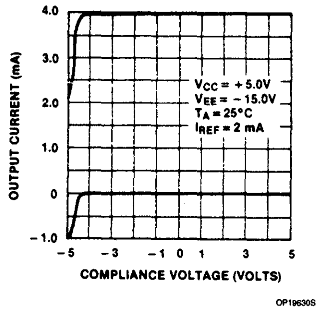


Figure 1. Output Current vs Output Compliance Voltage

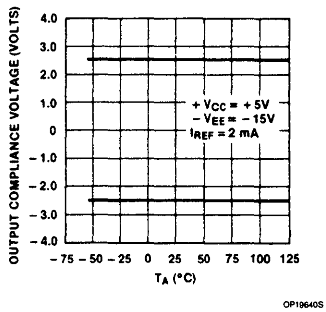


Figure 2. Maximum Output Compliance Voltage vs Temperature

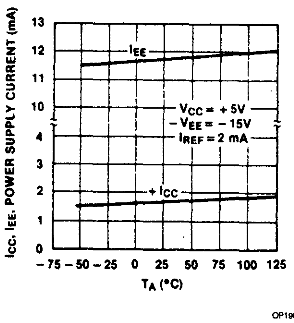


Figure 3. Power Supply Current vs Temperature

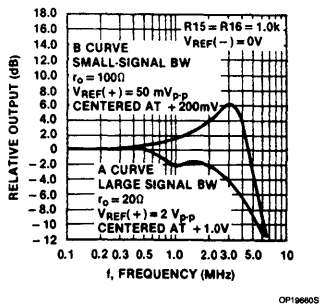


Figure 4. Reference Amplifier Frequency Response

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R_{16} (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R_{16} should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R_{16} to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R_{16} should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R_{16} and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R_{16} increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R_{16} = 1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

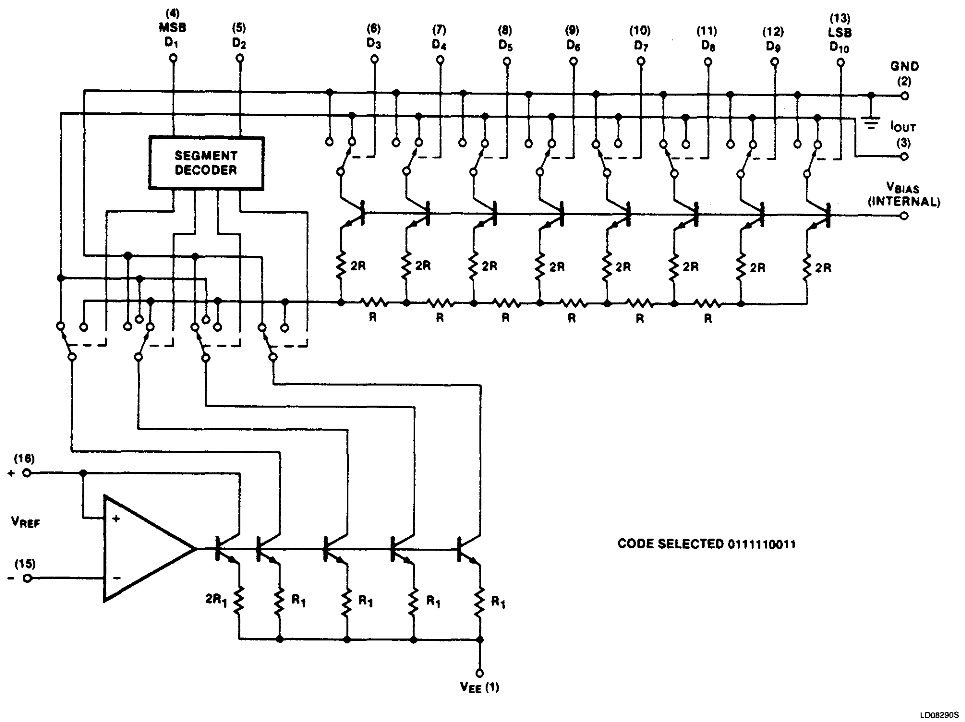
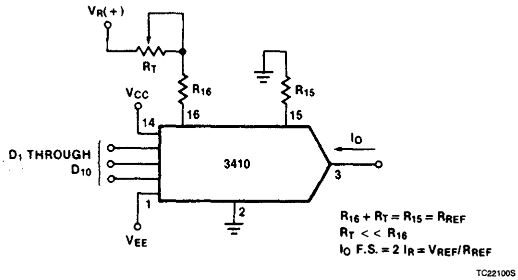


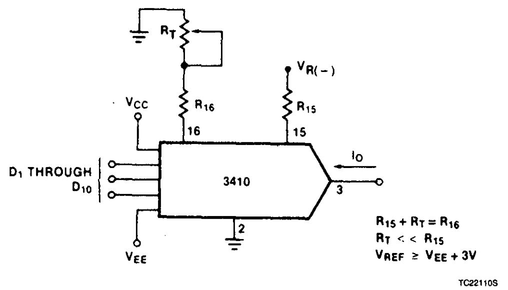
Figure 5. MC3410 Equivalent Circuit

10-Bit High-Speed Multiplying D/A Converter

MC3410, MC3510, MC3410C



a. Positive Reference Voltage



b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.

The MC3510 and the MC3410 are accurate to within ±0.05% at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The MC3410, MC3510 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

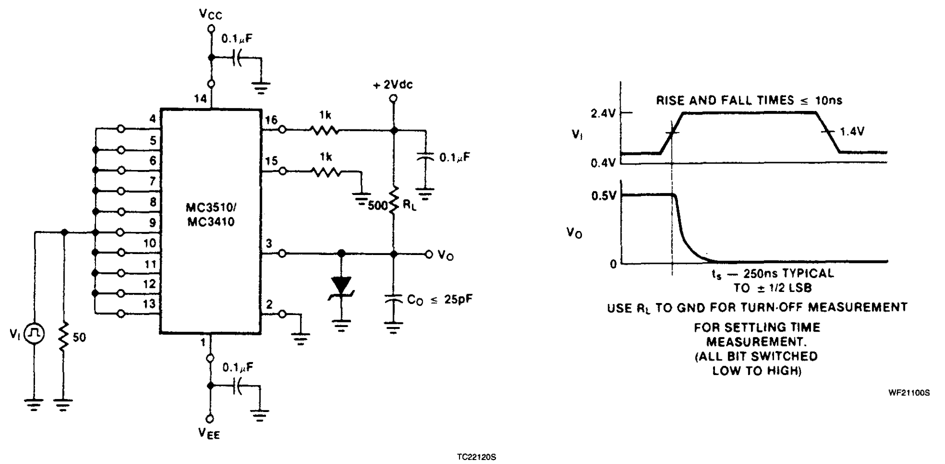


Figure 7. Settling Time

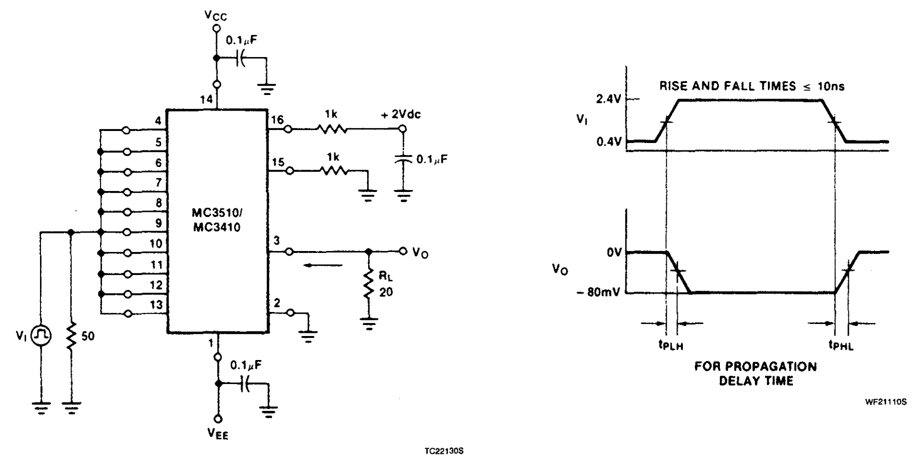


Figure 8. Propagation Delay Time

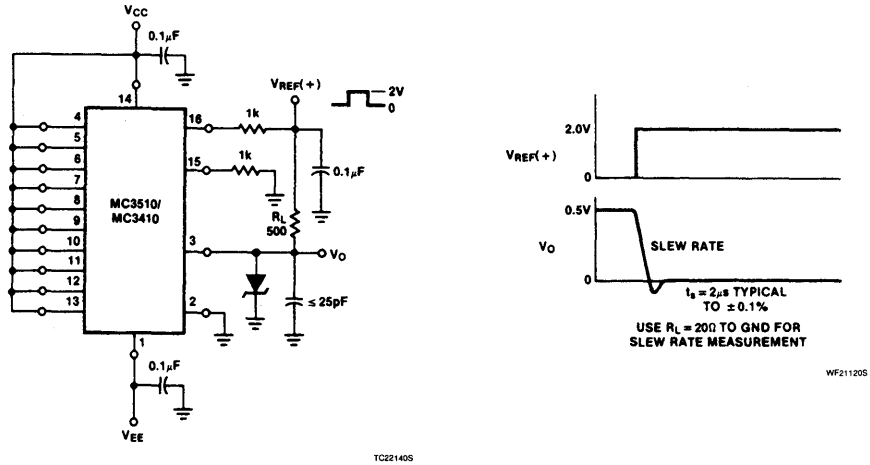
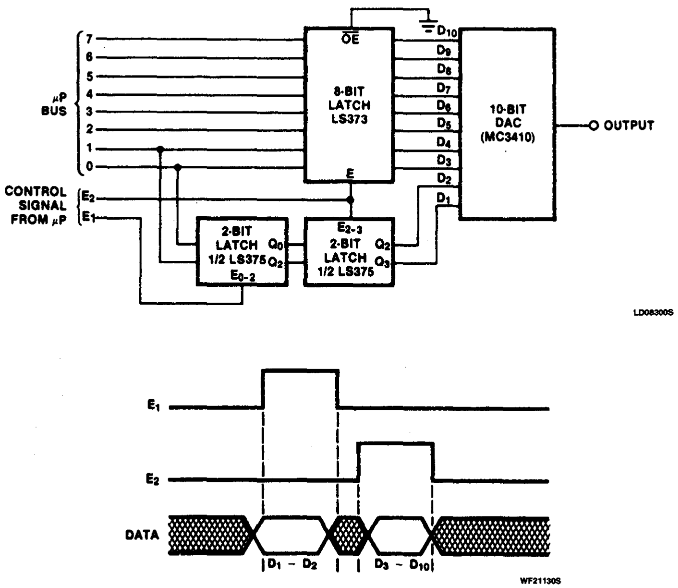


Figure 9. Reference Amplifier Settling Time and Slew Rate

TYPICAL APPLICATIONS



THE VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH E_2 PULSE.
TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 10. Interfacing 10-Bit DAC With 8-Bit Microprocessor

NE542
Dual Low-Noise Preamplifier

Product Specification

DESCRIPTION

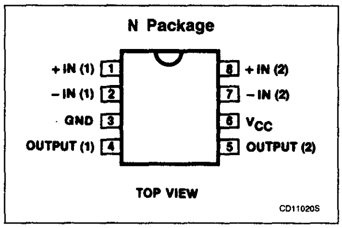
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ($V_{CC}-2V_{P-P}$), and internal compensation to 10dB. The NE542 operates from a single supply across a range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- **Low noise — 0.7μV total input noise**
- **High gain — 104dB open-loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing ($V_{CC}-2V_{P-P}$)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz ($15V_{P-P}$)**
- **Internally-compensated (stable at 10dB)**
- **Short-circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION



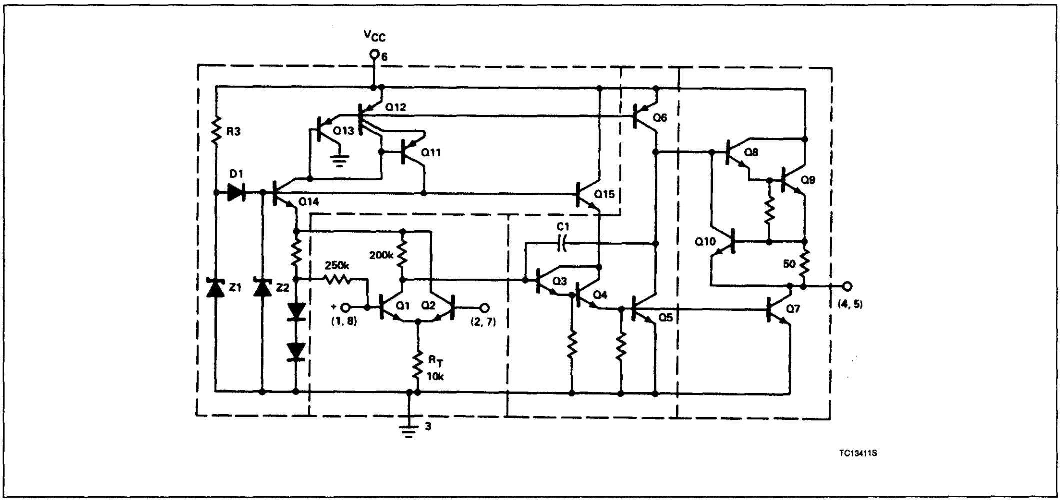
APPLICATIONS

- **Tape preamplifier**
- **Phono preamplifier**
- **Microphone preamplifier**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE542N

EQUIVALENT CIRCUIT



Dual Low-Noise Preamplifier NE542

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+24	V
P_D	Power dissipation	500	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	= dc

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

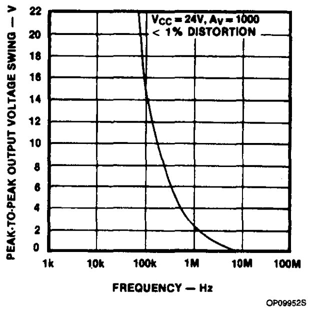
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		9		24	V
I_{CC}	Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
R_{IN}	Input resistance Positive input Negative input			 100 200		 kΩ kΩ
R_{OUT}	Output resistance	Open-loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 14V$, unless otherwise specified.

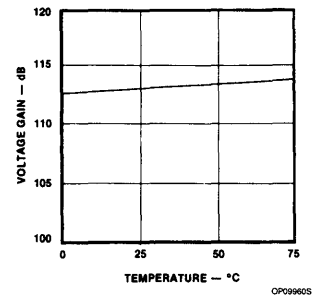
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
A_V	Voltage gain	Open-loop		160,000		V/V
I_{IN}	Negative Input current				0.5	
I_{OUT}	Output current	Source Sink (linear operation)	8 2	14 3		mA mA
V_{OUT}	Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
SR	Small signal bandwidth Slew rate			15 5		MHz V/μs
P_{BW}	Power bandwidth	$15V_{P-P}$		100		kHz
V_{IN}	Maximum input voltage	Linear operation, < 2.5% distortion			300	mV_{RMS}
PSRR	Power supply rejection ratio	f = 60, 120Hz f = 1kHz		100 110		dB dB
	Channel separation	f = 1kHz	40	70		dB
THD	Total harmonic distortion	40dB gain, f = 1kHz		0.1	0.3	%
	Total equivalent input noise	$R_S = 600\Omega$, 100 – 10,000Hz		0.7	1.2	μV_{RMS}
	Noise figure	$R_S = 50k\Omega$, 10 – 10,000Hz $R_S = 20k\Omega$, 10 – 10,000Hz $R_S = 10k\Omega$, 10 – 10,000Hz $R_S = 5k\Omega$, 10 – 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

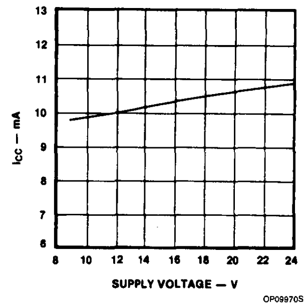
Large-Signal Frequency Response



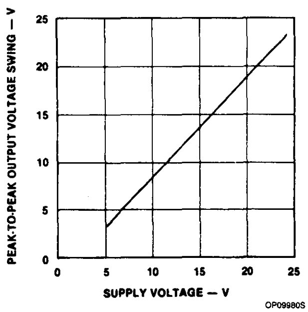
Gain vs Temperature



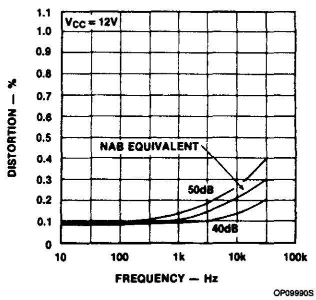
V_{CC} vs I_{CC}



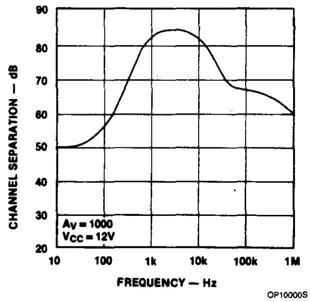
Peak-to-Peak Output Voltage Swing vs V_{CC}



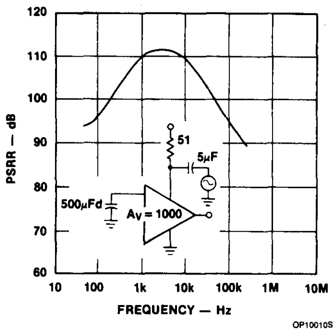
% Distortion



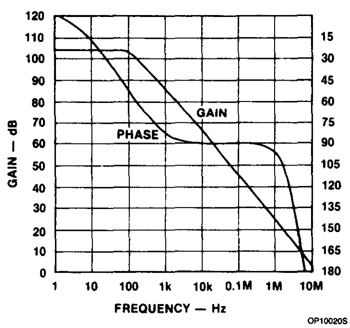
Channel Separation



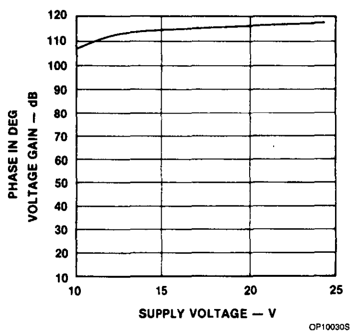
PSRR vs Frequency



Gain and Phase Response

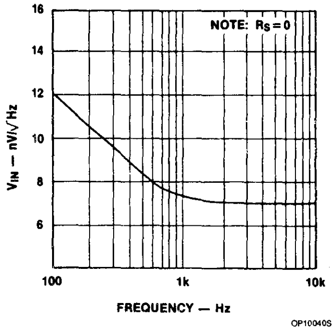


Voltage Gain vs Supply Voltage

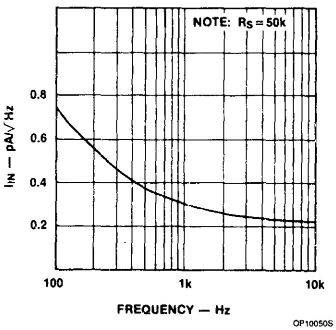


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

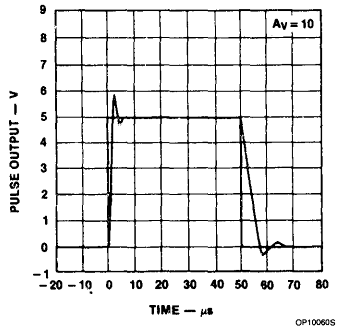
Noise Voltage vs Frequency



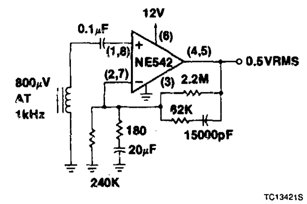
Noise Current vs Frequency



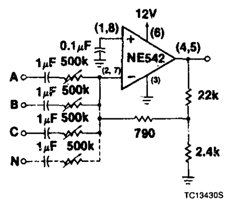
Pulse Response



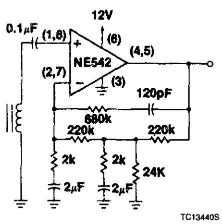
TYPICAL APPLICATIONS



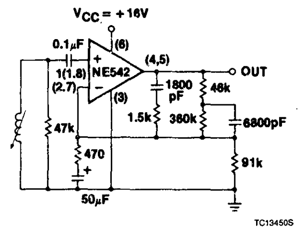
Typical Tape Playback Amplifier



Audio Mixer



Two-Pole Fast Turn-On NAB Tape Preamp



RIAA Magnetic Phono Preamp

NOTE:
All resistor values are typical and in ohms.

NE570/571/SA571
Compandor

Product Specification

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\,avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\,avg}{R_1}$$

FEATURES

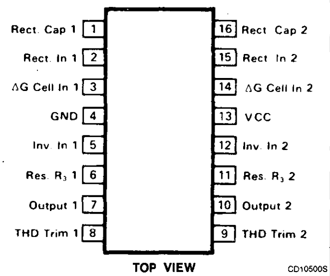
- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6V_{DC}**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

D, F, N Packages[1]

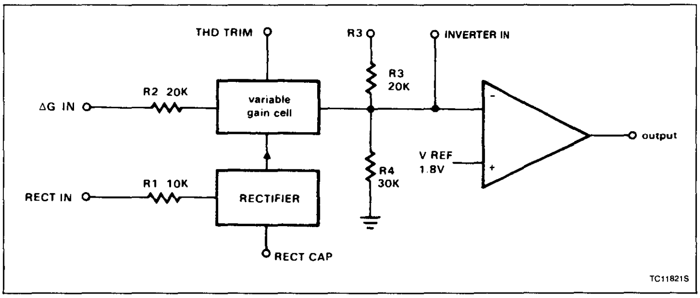


NOTE:
1. SOL - Released in Large SO Package Only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	-40°C to +85°C	SA571F
16-Pin Plastic DIP	-40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz – 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals [$V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = −30dBm, V_1 = 0dB		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

Compandor

NE570/571/SA571

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final};\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

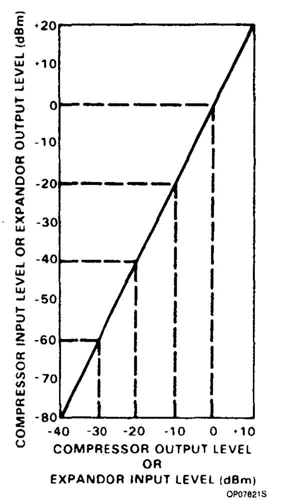
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

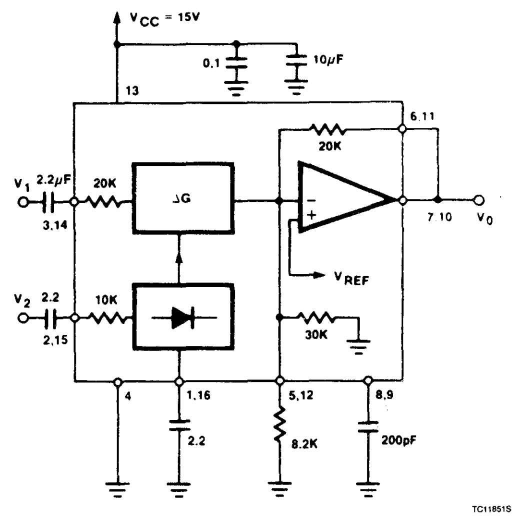
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

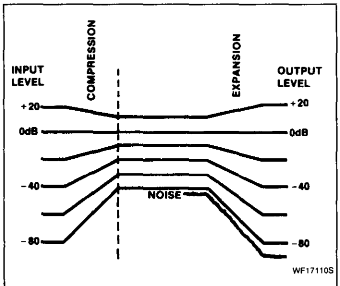


Figure 1. Restricted Dynamic Range Channel

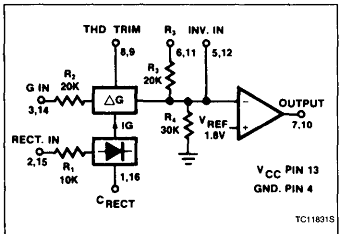


Figure 2. Chip Block Diagram (1 of 2 Channels)

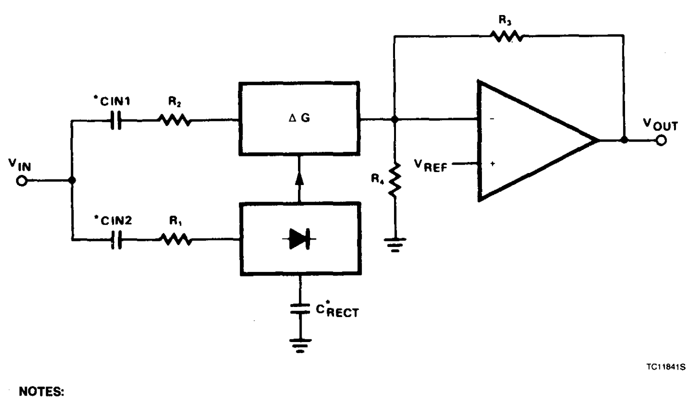
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k}\right) 1.8V$$



NOTES:

$$GAIN = \frac{2\ R_3\ V_{IN}\ (avg.)}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

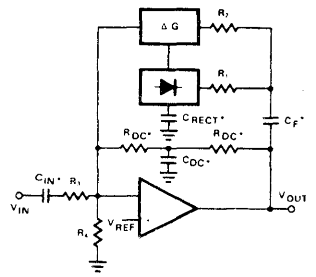
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4} V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)}\right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4. Basic Compressor

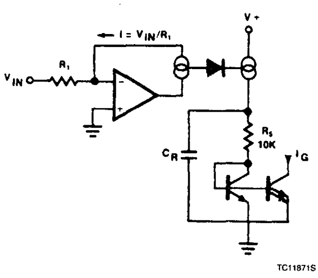
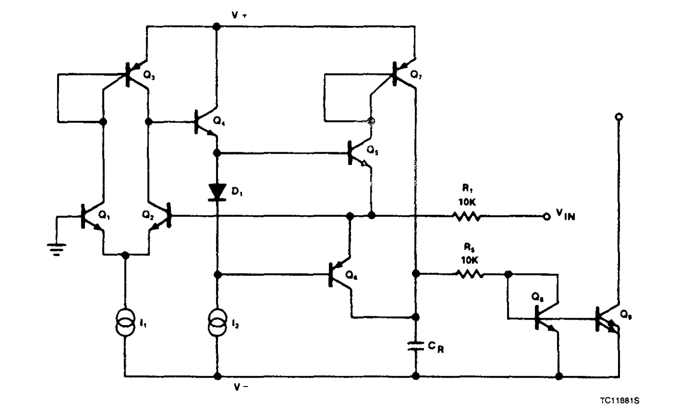


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$I_G = 2 \frac{V_{IN}\ avg}{R1}$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

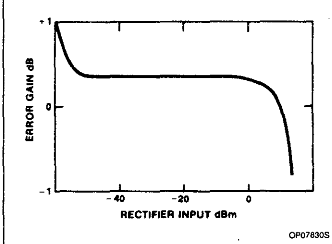


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, −20dBm, and −40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

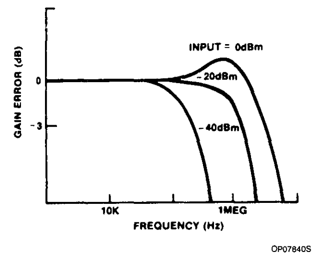


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

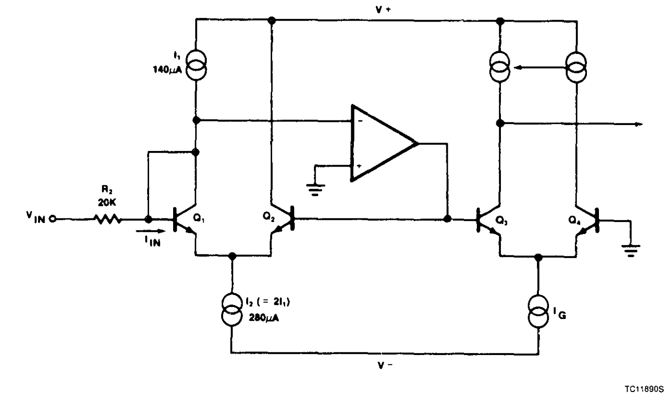
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2}\frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

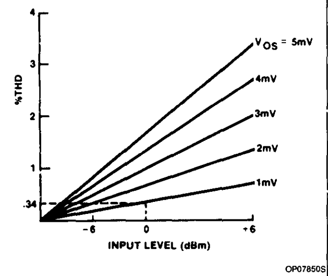


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

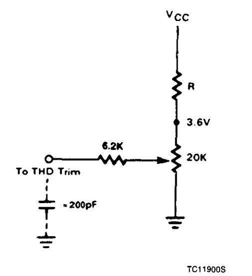


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

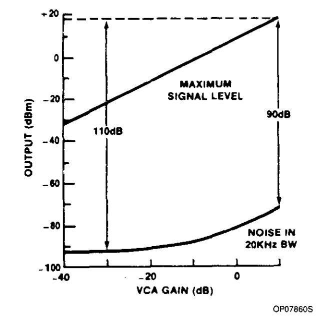


Figure 12. Dynamic Range of NE570

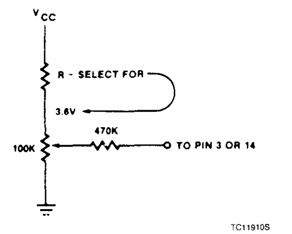


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implanted resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

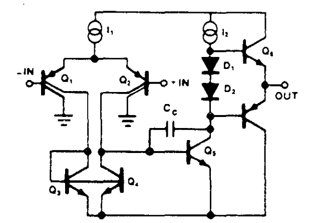


Figure 14. Operational Amplifier

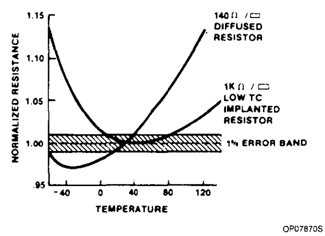


Figure 15. Resistance vs Temperature

NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

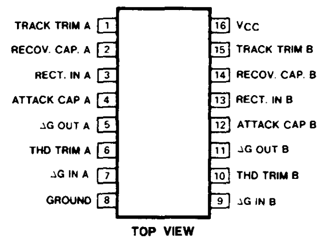
The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V - 22V**
- **System level adjustable with external components**

PIN CONFIGURATION

D, N, F Packages[1]



NOTE:
1. D package released in large SO (SOL) package only.

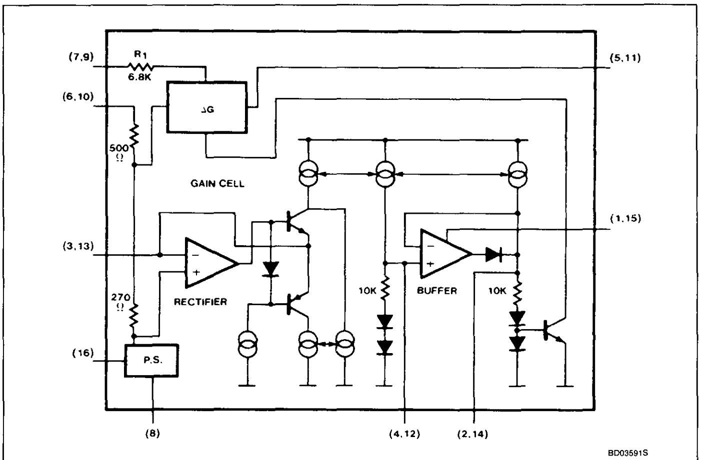
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	-40°C to +85°C	SA572D
16-Pin Cerdip	-40°C to +85°C	SA572F
16-Pin Plastic DIP	-40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

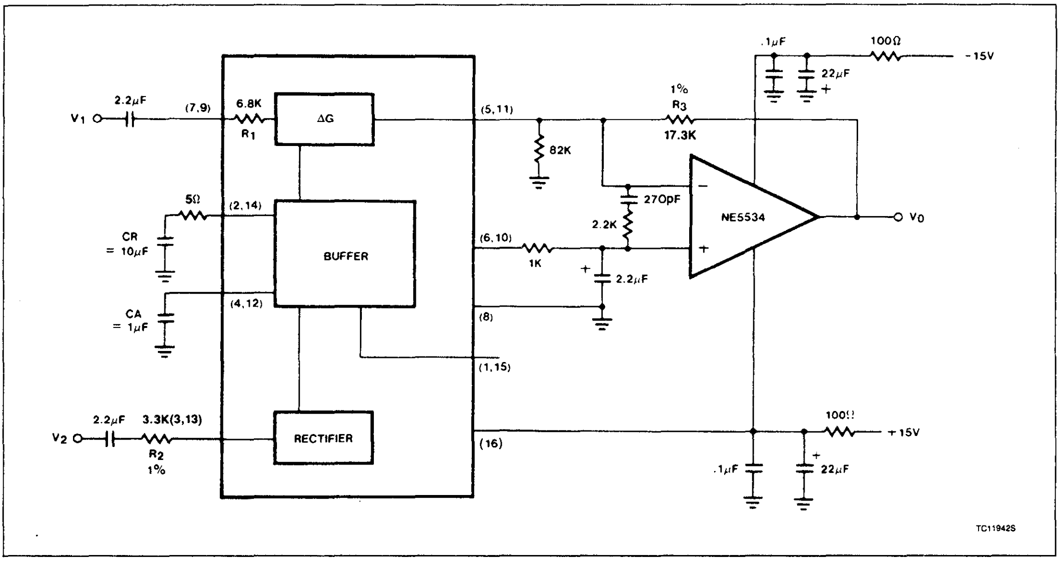
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 -40 to +85	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = $100mV_{RMS}$ at 1kHz; $V_1 = V_2$; $R_2 = 3.3k\Omega$; $R_3 = 17.3k\Omega$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz $C_A = 1.0\mu F$		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz $C_R = 10\mu F$		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 - 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to $100mV_{RMS}$		±20	±50		±20	±50	mV
	Unity gain level		-1	0	+1	-1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2 = 400mV$		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = $[V_O - V_O$ (unity gain)]dB $- V_2$dB	Rectifier input $V_2 = +6dB$ $V_1 = 0dB$ $V_2 = -30dB$ $V_1 = 0dB$		 ±0.2 ±0.5	 -1.5 +0.8		 ±0.2 ±0.5	 -2.5 +1.6	dB
	Channel crosstalk	$200mV_{RMS}$ into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3-Q4}} = \Delta_{BE_{Q1-Q2}}$$

$$(V_{BE} = V_T \; l_n \; IC/IS)$$

$$V_T \; l_n\left(\frac{\tfrac{1}{2}I_G + \tfrac{1}{2}I_O}{I_S}\right) - V_T \; l_n\left(\frac{\tfrac{1}{2}I_G - \tfrac{1}{2}I_O}{I_S}\right)$$

$$= V_T \; l_n\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \; l_n\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \dfrac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

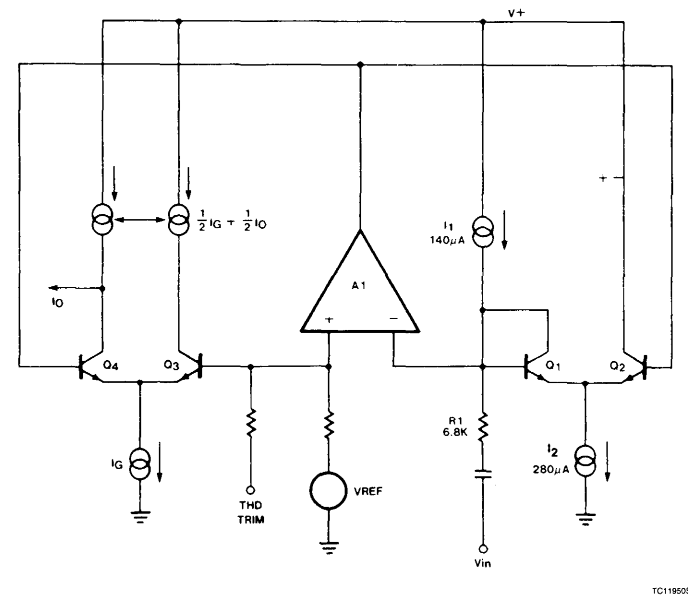


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$$

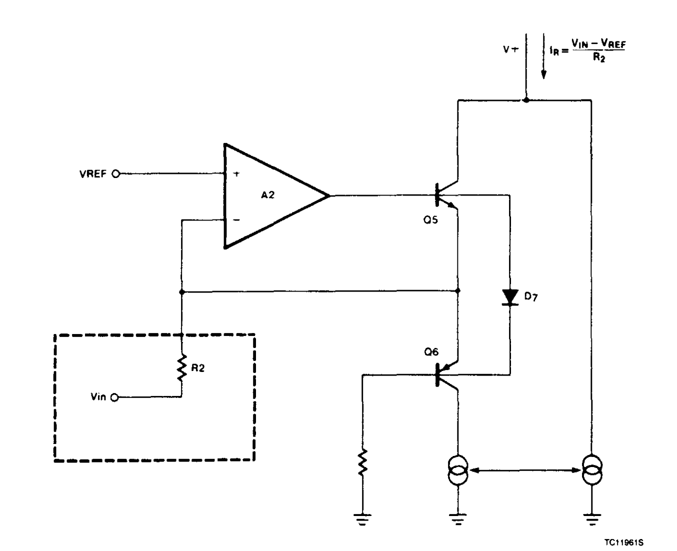


Figure 2. Simplified Rectifier Schematic

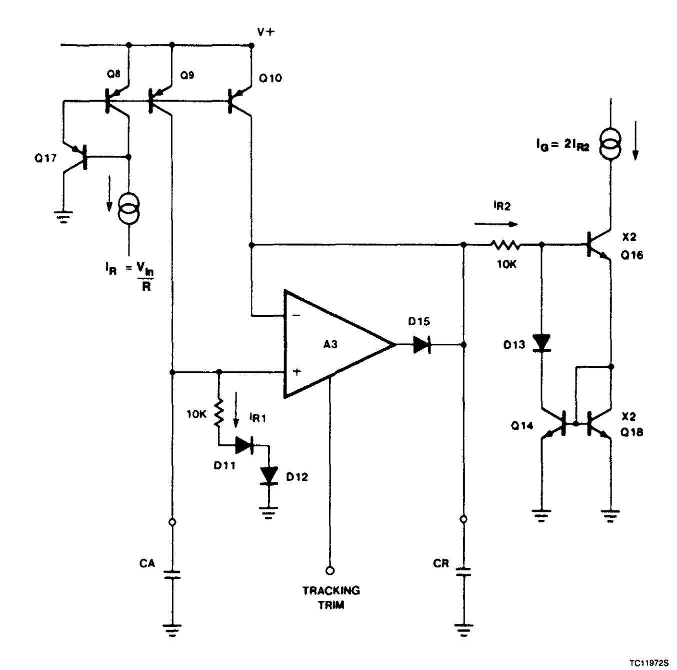


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a $\pm$1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR $\cdot$ R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of $\pm 3\mu$A.

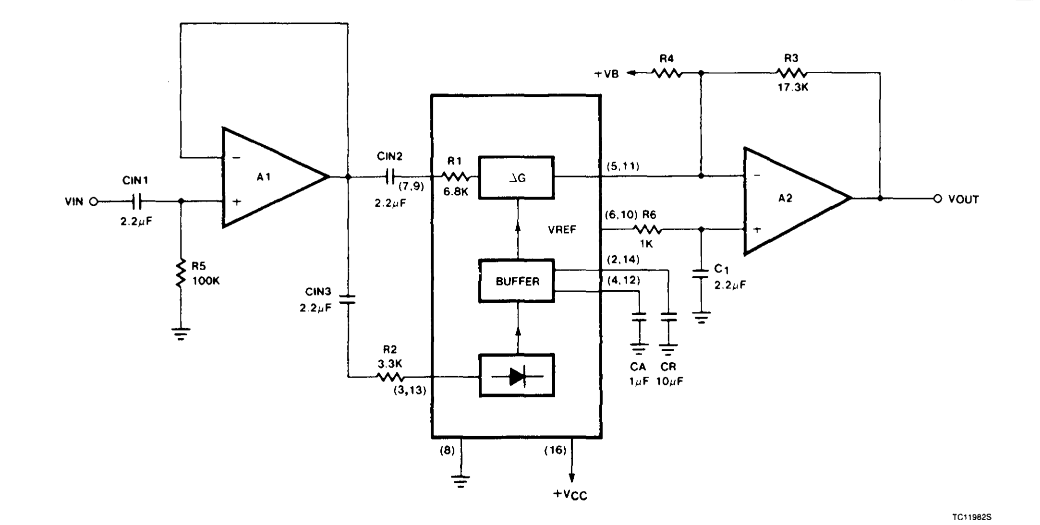


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

$(I_1 = 140\mu A)$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA · 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1+\frac{R_{DC1}+R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1}+R_{DC2}}{R_4}\right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

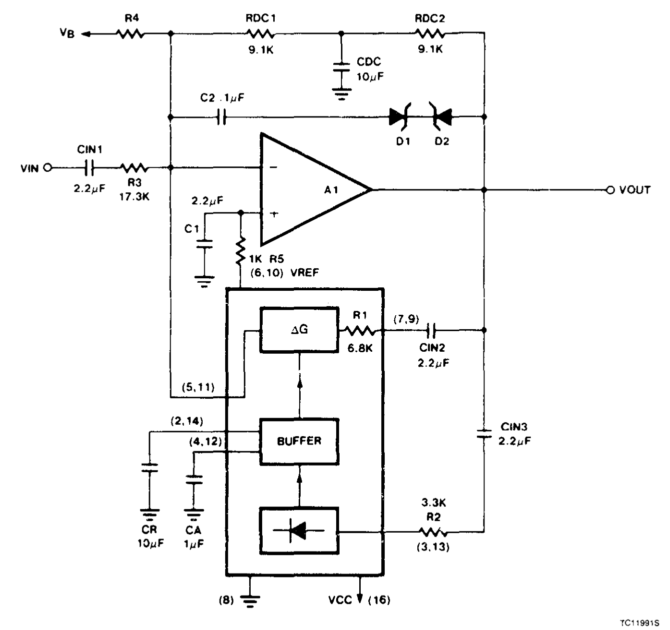


Figure 5. Basic Compressor Schematic

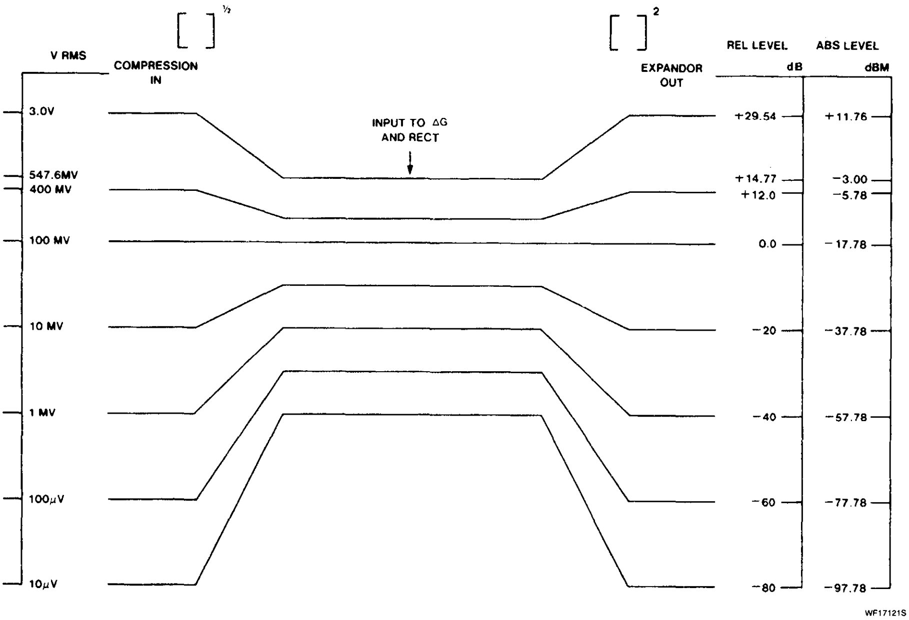


Figure 6. NE572 System Level

NE575
Low Voltage Compandor

Preliminary Specification

DESCRIPTION

The NE575 is a dual gain-control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

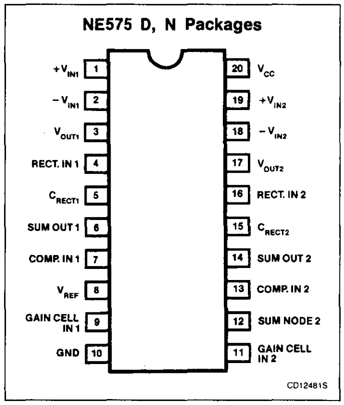
FEATURES

- **Operating voltage range from 3 to 7V**
- **Reference voltage of $100mV_{RMS}$ = 0dB**
- **One dedicated summing op amp per channel and two extra uncommitted op amps**
- **600Ω drive capability**
- **Single or split supply operation**
- **Wide input/output swing capability.**

APPLICATIONS

- **Portable communications**
- **Cellular radio**
- **Cordless telephone**
- **Consumer audio**
- **Portable broadcast mixers**
- **Wireless microphones**
- **Modems**
- **Electric organs**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SO	0 to +70°C	NE575D

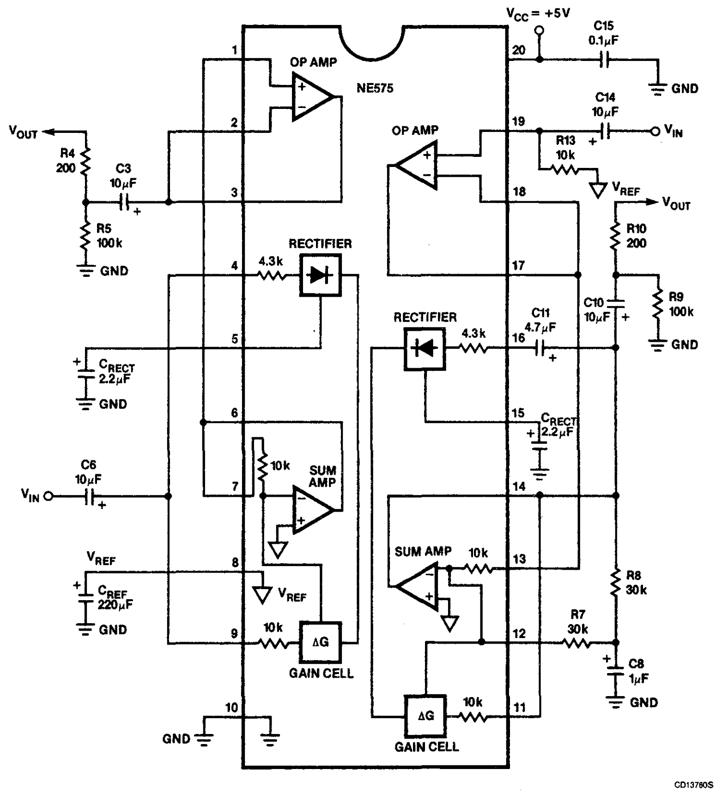
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	8	V
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, 0dB = 100mV, expander mode, $V_{CC} = 5V$, Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4	5.5	mA
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.13	1.0	%
eno	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20	μV
0dB	Unity gain level	1kHz	−1.0		1.0	dB
V_{OS}	Output voltage offset	no signal	−100		100	mV
	Output DC shift	no signal to 0dB	−50	10	50	mV
	Tracking error	1kHz, +6dB to −30dB	−0.5		+0.5	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220μF		−80	−65	dB
For operational amplifier						
V_O	Output swing	V_{P-P}, R_L = 10kΩ	V_{CC}−0.4	V_{CC}−0.2		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V − 4.5V	−0.3		0.3	μA
V_{OS}	Input offset voltage		−10	3	10	mV
A_{VOL}	Open-loop gain	R_L = 10kΩ	80	90		dB
SR	Slew rate	unity gain		1		V/μs
GBW	Bandwidth	unity gain		3		MHz
eni	Input voltage noise	BW = 20kHz		2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTE:
1. The IC remains functional down to 2V.



NOTE:
Left channel in expander mode; right channel in compressor mode.
For additional information, call the factory.

Figure 1. Typical Application

NE5240
Dolby Digital Audio Decoder

Preliminary Specification

DESCRIPTION

The NE5240 is a two channel decoder for the Dolby Digital Audio System. *The IC includes input latches to separate two channels of audio and control data, a precision internal voltage reference, and digital/analog signal processing circuitry for each channel. The IC design is implemented in a bipolar process to achieve low noise, low distortion, and wide dynamic range.

NOTE:
*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and applications information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

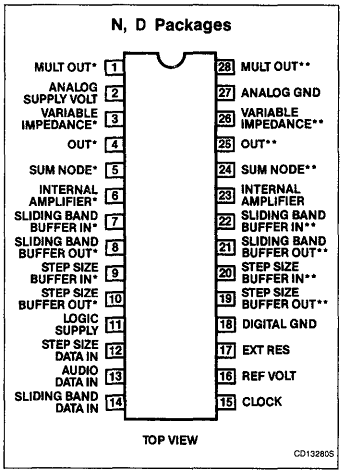
FEATURES

- **Wide dynamic range — 85dB**
- **Low distortion 0.05% @ 1kHz, -10dB**
- **TTL and CMOS compatible logic inputs**
- **Audio bandwidth — 30Hz to 15kHz**

APPLICATIONS

- **High quality digital transmission of audio data**
- **Satellite reception**
- **Cable TV**
- **Microwave distribution systems**

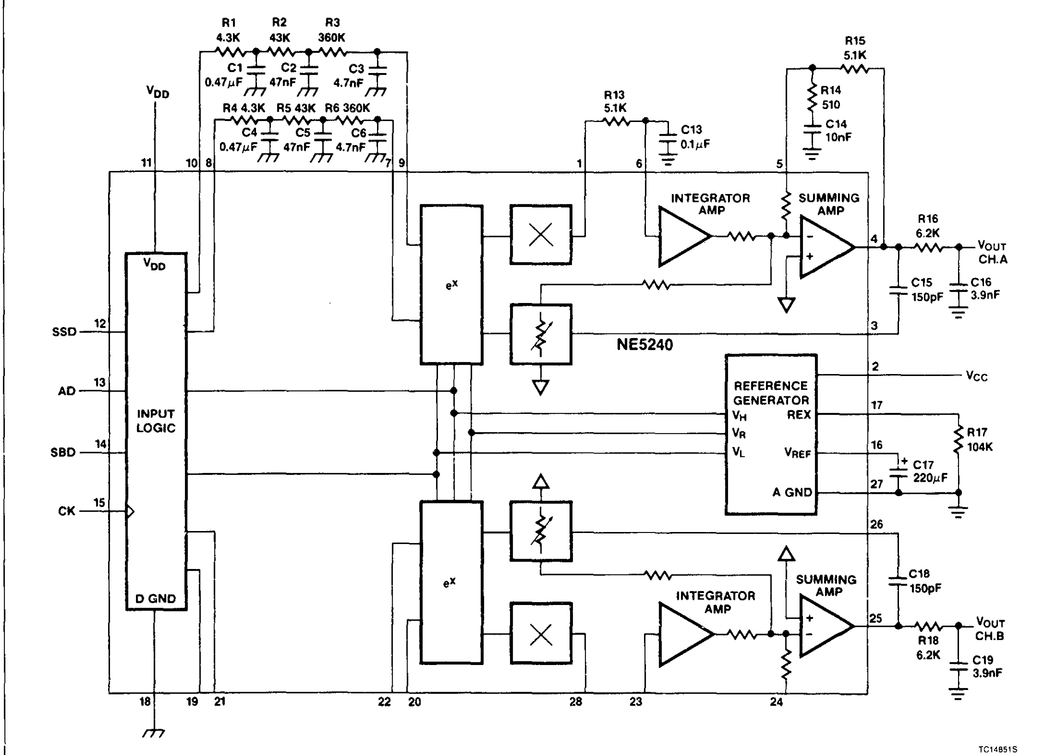
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin SO	0 to +70°C	NE5240D
28-Pin Plastic DIP	0 to +70°C	NE5240N

BLOCK DIAGRAM



NOTE:
One channel of the application shown with external components.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Analog supply voltage	+15	V
V_{DD}	Logic supply voltage	+7	V
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

All specifications are at $T_A = 25°C$, $V_{CC} = 12V$, $V_{DD} = 5V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Analog voltage supply range		10	12	14	V
V_{DD}	Logic voltage supply range		4.5	5	5.5	V
I_{CC}	Supply current	$V_{CC} = 12V$	10	24	35	mA
I_{DD}	Supply current	$V_{DD} = 5V$	5	12	18	mA
V_{IH}	Input voltage high		2		5	V
V_{IL}	Input voltage low		0		0.8	V
I_{IL}	Input current low	$V_{DD} = 4.5V$		10	100	μA
I_{IH}	Input current high			1	100	μA
t_S	Setup time		150			ns
t_H	Hold time		150			ns
I_B	Input buffers, Pins 7, 9, 20, 22	$V_{IN} = 2.0V$			100	nA
R_L	Summing amp output load		5			kΩ
V_{OS}	Output offset voltage			0.1	0.6	V
V_{OS}	Output offset change	10%-SBD-70%		±5	±20	mV
V_{REF}	Reference voltage		5.5	$0.5V_{CC}$	6.5	V

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			Min	Typ	Max	
V_O	Full-Scale output, 0dB	f = 100Hz		1.8		V_{RMS}
	Absolute output level	f = 1kHz, SSD = 40%	93	118	150	mV_{RMS}
	Channel balance	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 1kHz, 20%-SSD-70%	-1.5		1.5	dB
	Step-Size linearity	f = 100Hz, SSD = 90%	-2.5		1.0	dB
f_R	Frequency response	f = 2kHz, SBD = 10%	-1.0		1.0	dB
f_R	Frequency response	f = 5kHz, SBD = 20%	-1.0		1.0	dB
f_R	Frequency response	f = 7kHz, SBD = 30%	-1.0		1.0	dB
f_R	Frequency response	f = 8kHz, SBD = 40%	-1.0		1.0	dB
f_R	Frequency response	f = 10kHz, SBD = 50%	-1.0		1.0	dB
f_R	Frequency response (all WRT 100Hz)	f = 12kHz, SBD = 60% f = 14kHz, SBD = 70%	-1.0 -1.5		1.0 1.5	dB dB
S/N	Dynamic range	SSD = 70%, CCIR/ARM	80	85		dB
THD	Harmonic distortion	f = 1kHz, -3dB		0.1	0.5	%
THD	Harmonic distortion Channel separation	f = 1kHz, -10dB f = 1kHz, 0dB	 60	0.05 75	0.2	% dB
PSRR	Power supply rejection ratio[1]	f = 1kHz		60		dB

NOTES:
1. PSRR depends on value of capacitor on Pin 16.
2. The duty cycle of SSD and SBD control data is 10%, unless otherwise noted.

NE/SE5410
10-Bit High-Speed Multiplying D/A Converter

Product Specification

DESCRIPTION

The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

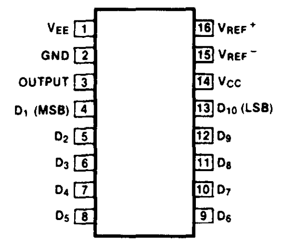
The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin- and function-compatible with MC3410**
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range — −2.5 to +2.5V**
- **Fast settling time — 250ns typical**
- **Digital inputs are TTL- and CMOS-compatible**
- **High-speed multiplying input slew rate — 20mA/μs**
- **Reference amplifier internally-compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION

F Package



TOP VIEW

CD11081S

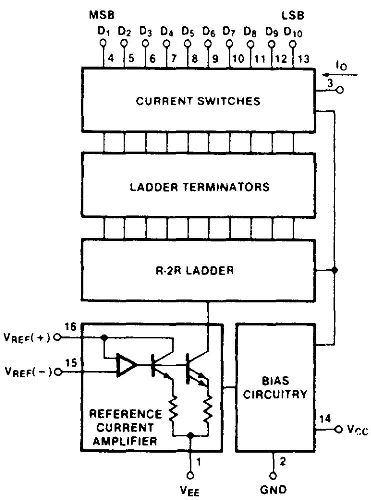
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5410F
16-Pin Cerdip	-55 to +125°C	SE5410F

BLOCK DIAGRAM



BD07540S

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		−18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	+4, −5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating temperature range SE5410 NE5410	 −55 to +125 0 to +70	 °C °C
T_J	Junction temperature Ceramic package	 +150	 °C
T_{STG}	Storage temperature	−65 to +150	°C
P_D	Maximum power dissipation $T_A = 25°C$ (still-air)[1]	1190	mW

NOTE:
1. Derate above 25°C at the following rate:
F package at 9.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $I_{REF} = 2.0mA$, all digital inputs at high logic level. SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ϵ_R	Relative accuracy (Error relative to full scale I_O)	Over temperature		±0.025	±0.05	%
				±¼	±½	LSB
	Differential non-linearity	Over temperature		±0.025	±0.05	%
				±¼	±½	LSB
t_S	Settling time to within ±½ LSB (all bits low to high)	$T_A = 25°C$		250		ns
t_{PLH} t_{PHL}	Propagation delay time	$T_A = 25°C$		35 20		ns
TCI_O	Output full-scale current drift			20	40	ppm/°C
V_{IH}	Digital input logic levels (all bits) High level, Logic "1" Low level, Logic "0"		 2.0 		 0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) High level, $V_{IH} = 5.5V$ Low level, $V_{IL} = 0.8V$				 20 −20	μA
$I_{REF(15)}$	Reference input bias current (Pin 15)			−1.0	−5.0	μA
I_{OH}	Output current (all bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000\Omega$	3.937	3.996	4.054	mA
I_{OL}	Output current (all bits low)	$T_A = 25°C$		0	0.4	μA
V_O	Output voltage compliance	$T_A = 25°C$ $\epsilon_R < 0.050\%$ relative to full-scale			−2.5 +2.5	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20		mA/μs

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $I_{REF} = 2.0mA$, all digital inputs at high logic level. SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0		μs
PSRR(−)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	$V_O = 0$		25		pF
C_I	Digital input capacitance (all bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power supply voltage range	$T_A = 25°C$ $V_O = 0$	+4.75 −14.25	+5.0 −15	+5.25 −15.75	V_{DC}
	Power consumption			190	300	mW

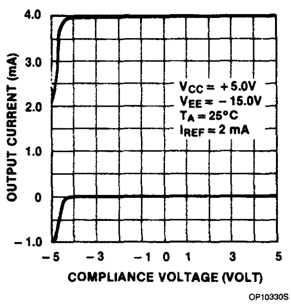


Figure 1. Output Current vs Output Compliance Voltage

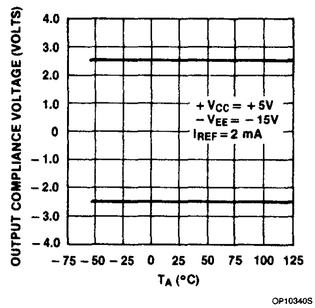


Figure 2. Maximum Output Compliance Voltage vs Temperature

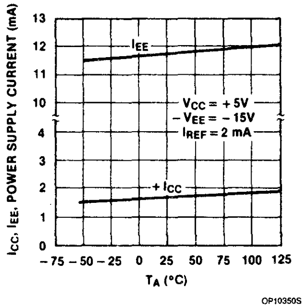


Figure 3. Power Supply Currents vs Temperature

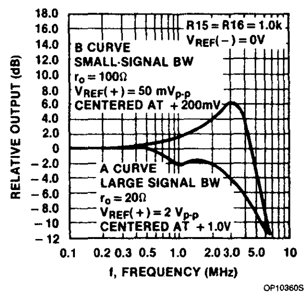


Figure 4. Reference Amplifier Frequency Response

10-Bit High-Speed Multiplying D/A Converter

NE/SE5410

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈10μs. The reference amplifier phase margin decreases as the current souce value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

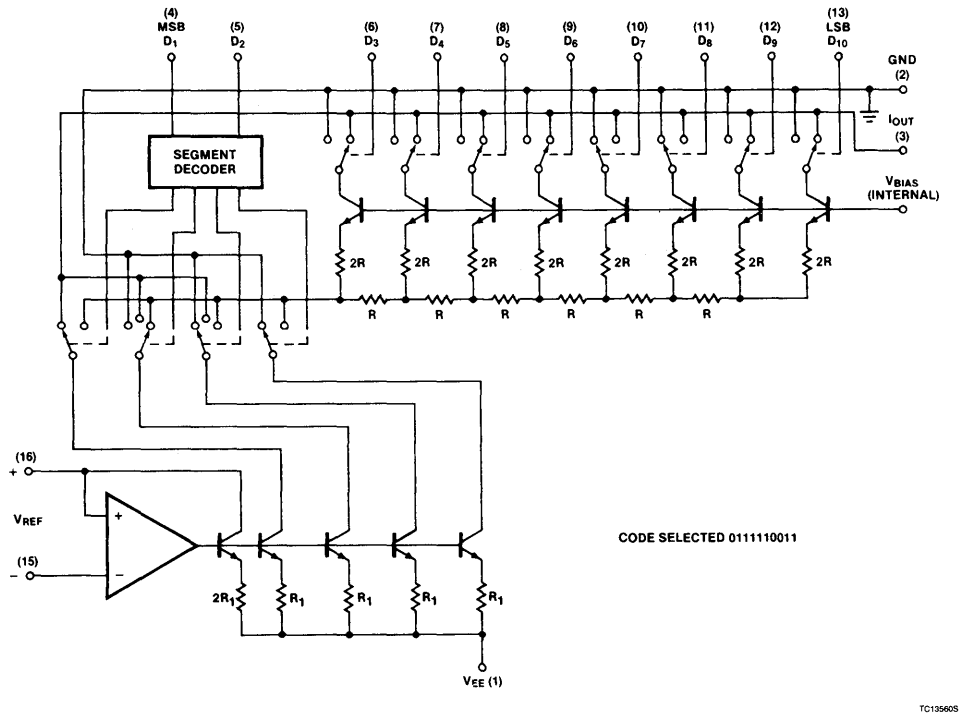
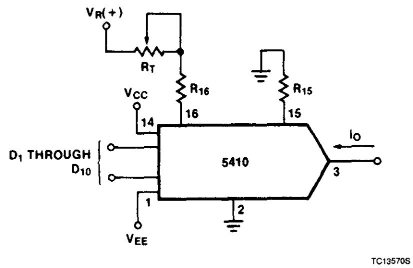
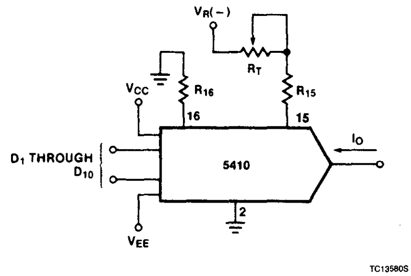


Figure 5. NE5410 Equivalent Circuit



NOTES:
$R_{16} + R_T = R_{15} = R_{REF}$
$R_T < < R_{16}$
I_O F.S. = 2 $I_R = V_{REF}/R_{REF}$

a. Positive Reference Voltabe



NOTES:
$R_{15} + R_T = R_{16}$
$R_T < < R_{15}$
$|V_{REF} \geqslant R_{VEE} + 3V$

b. Negative Reference Voltage

Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ±½ LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± ½ LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (< 0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to −2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

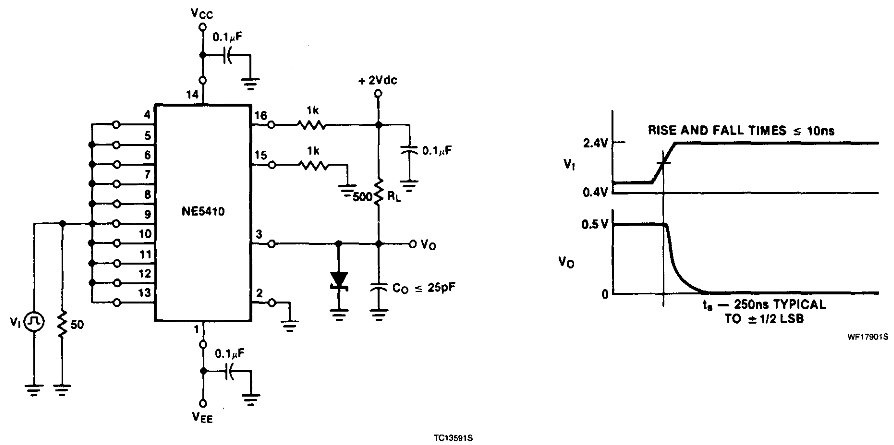


Figure 7. Settling Time

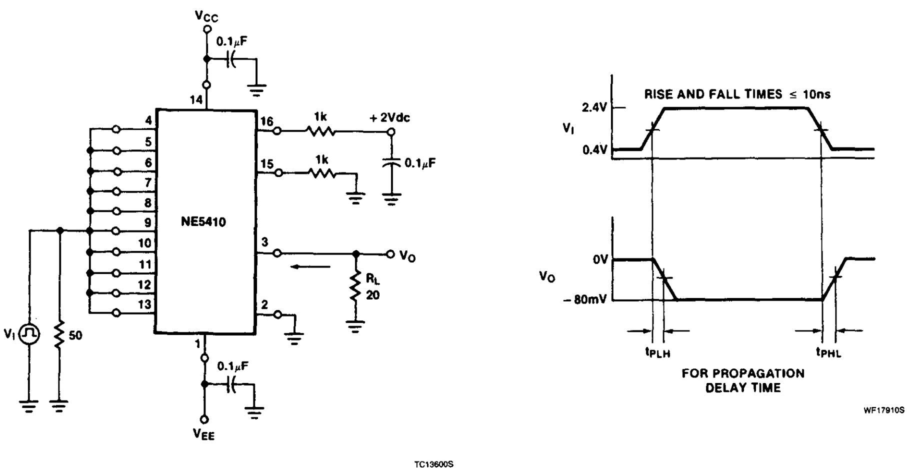
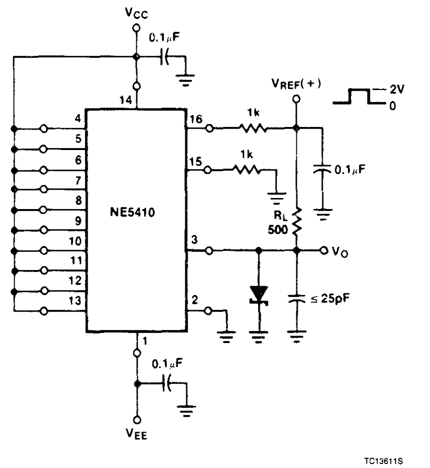
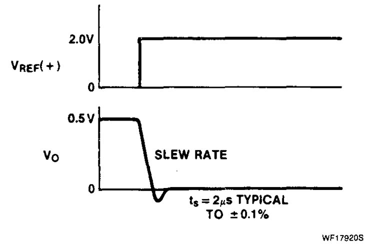


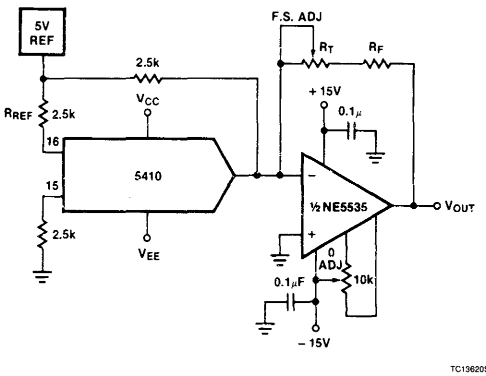
Figure 8. Propagation Delay Time



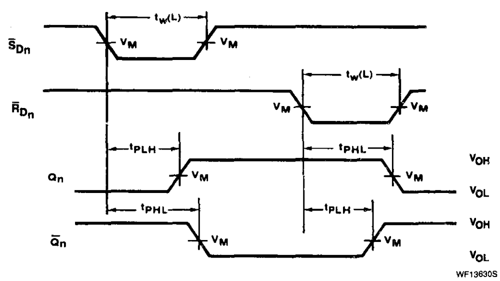


NOTE:
Use $R_L = 20\Omega$ to GND for slew rate measurement.

Figure 9. Reference Amplifier Settling Time and Slew Rate

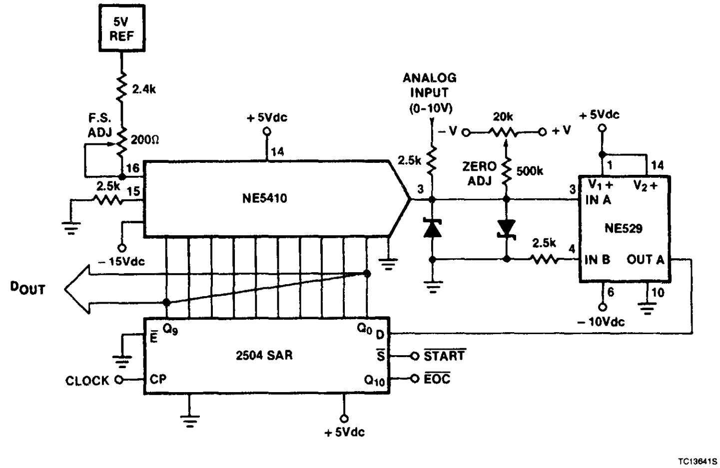


a. Bipolar Output (−10 to +10V)



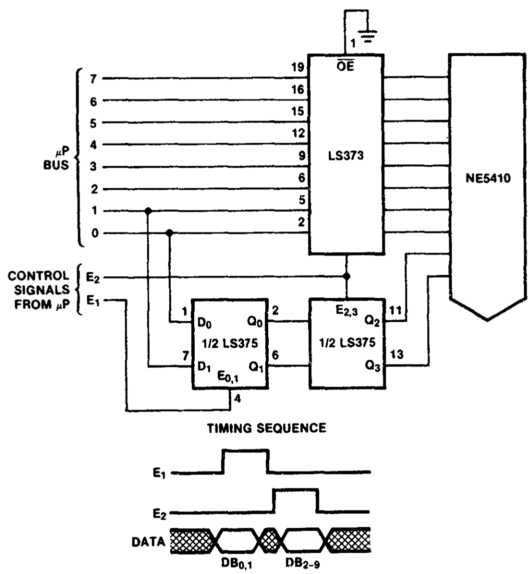
b. Unipolar Positive Output (0 − 10V)

Figure 10. Voltage Output Circuits



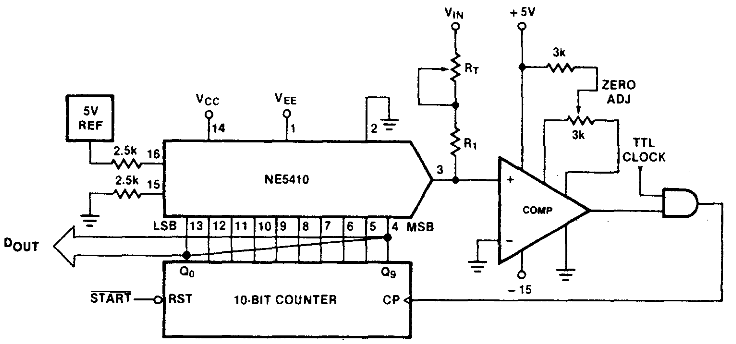
NOTES:
10-bit conversion time = 3.3μs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter



NOTE:
With this double latch technique, valid data will be latched to the DAC until updated with the E_2 pulse. Timing will depend on the processor used.

Figure 12. 8-Bit μP Bus Interface



NOTE:

V_{IN} FULL SCALE = 4mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

NE/SE5532/5532A
Internally-Compensated Dual Low Noise Operational Amplifier

Product Specification

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

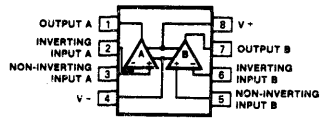
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used because it has guaranteed noise voltage specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$**
- **Input noise voltage: $5nV/\sqrt{Hz}$ (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **Compensated for unity gain**

PIN CONFIGURATIONS

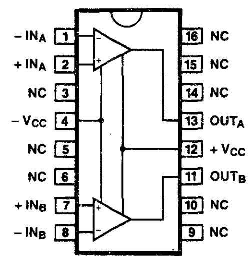
FE, N Packages



TOP VIEW

CD09880S

D Package[1]

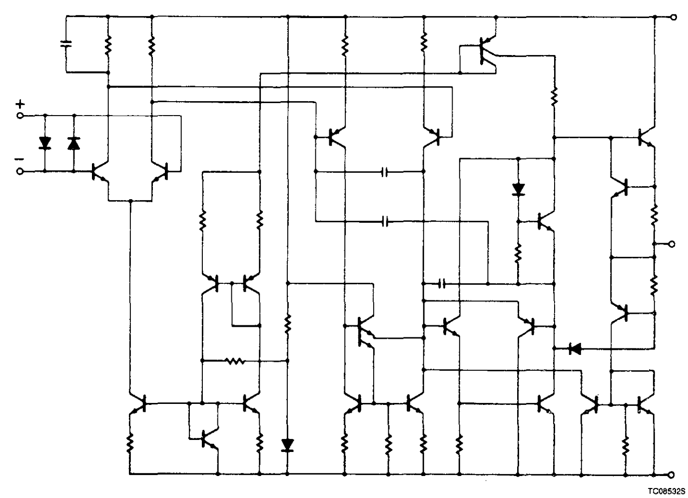


TOP VIEW

CD09891S

NOTE:
1. SOL and *non-standard* pinout.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE5532N
8-Pin Ceramic DIP	0 to 70°C	NE5532FE
8-Pin Plastic DIP	0 to 70°C	NE5532AN
8-Pin Ceramic DIP	0 to 70°C	NE5532AFE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532FE
8-Pin Ceramic DIP	−55°C to +125°C	SE5532AFE
16-Pin Plastic SOL	0 to 70°C	NE5532D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	$\pm V_{SUPPLY}$	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range NE5532/A SE5532/A	 0 to 70 -55 to +125	 °C °C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Maximum power dissipation, T_A = 25°C, (still-air)[2] N package F package D package	 1200 1000 1200	 mW mW mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistances of the above packages are as follows:
   N package at 100°C/W.
   F package at 135°C/W.
   D package at 105°C/W.

Internally-Compensated Dual Low Noise Operational Amplifier

NE/SE5532/5532A

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			8	10.5		8	16	mA
		Over temperature			13				mA
V_{CM}	Common-mode input range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	40	50		15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16		±15	±16		V
		Over temperature	±12	±14		±12	±14		V
		$R_L \geq 2k\Omega$	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±10	±12.5		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES:

1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the package thermal resistance.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

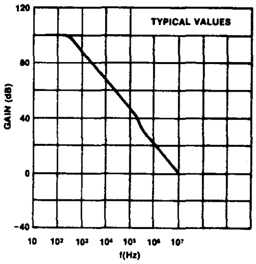
SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ Closed-loop $f = 10kHz$, $R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage-follower $V_{IN} = 100mV_{P-P}$ $C_L = 100pF$, $R_L = 600\Omega$		10		%
A_V	Gain	$f = 10kHz$		2.2		V/mV
GBW	Gain bandwidth product	$C_L = 100pF$, $R_L = 600\Omega$		10		MHz
SR	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$, $V_{CC} = \pm 18V$		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	$f_O = 30Hz$ $f_O = 1kHz$		8 5			8 5	12 6	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	$f_O = 30Hz$ $f_O = 1kHz$		2.7 0.7			2.7 0.7		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

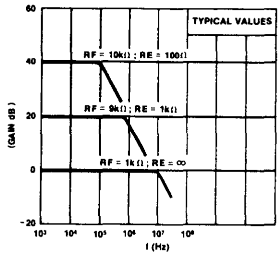
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Frequency Response



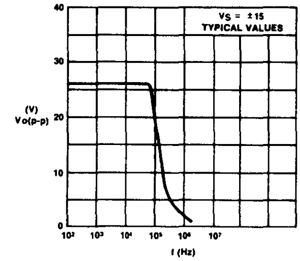
OP04870S

Closed-Loop Frequency Response



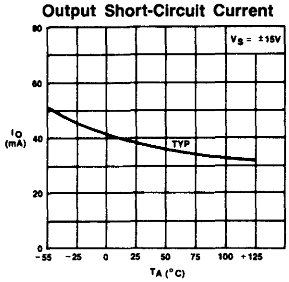
OPT4880S

Large-Signal Frequency Response



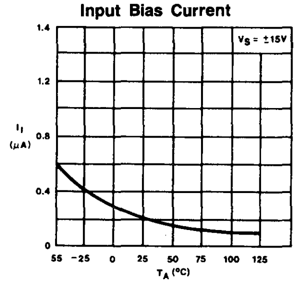
OPT4890S

Output Short-Circuit Current



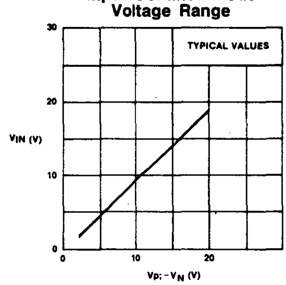
OP04900S

Input Bias Current



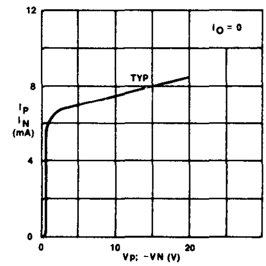
OP04910S

Input Common-Mode Voltage Range



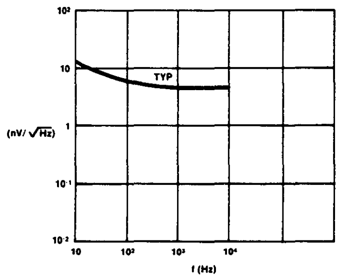
OP04920S

Supply Current



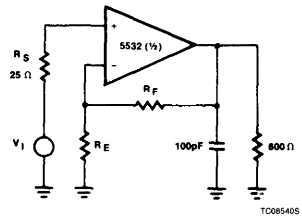
OP04930S

Input Noise Voltage Density

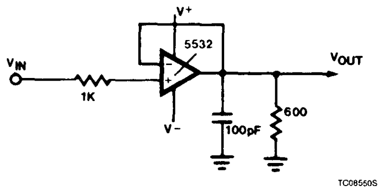


OP04940S

TEST CIRCUITS



Closed-Loop Frequency Response



Voltage-Follower

NE5533/5533A
NE/SA/SE5534/5534A
Dual and Single Low Noise Op Amp

Product Specification

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$ at $V_S = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwith: 200kHz**
- **Slew rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **5534 MIL-STD processing available**

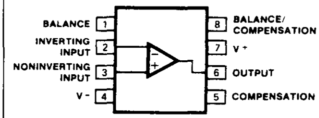
APPLICATIONS

- **Audio equipment**
- **Instrumentation and control circuits**
- **Telephone channel amplifiers**
- **Medical equipment**

PIN CONFIGURATIONS

NE/SA/SE5534/5534A

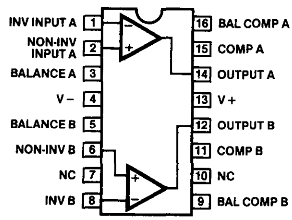
D, FE, N Packages



CD09900S

NE5533/5533A

N Package



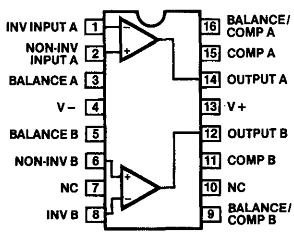
TOP VIEW

CD13740S

NE5533/5533A

D Package

D^2



TOP VIEW

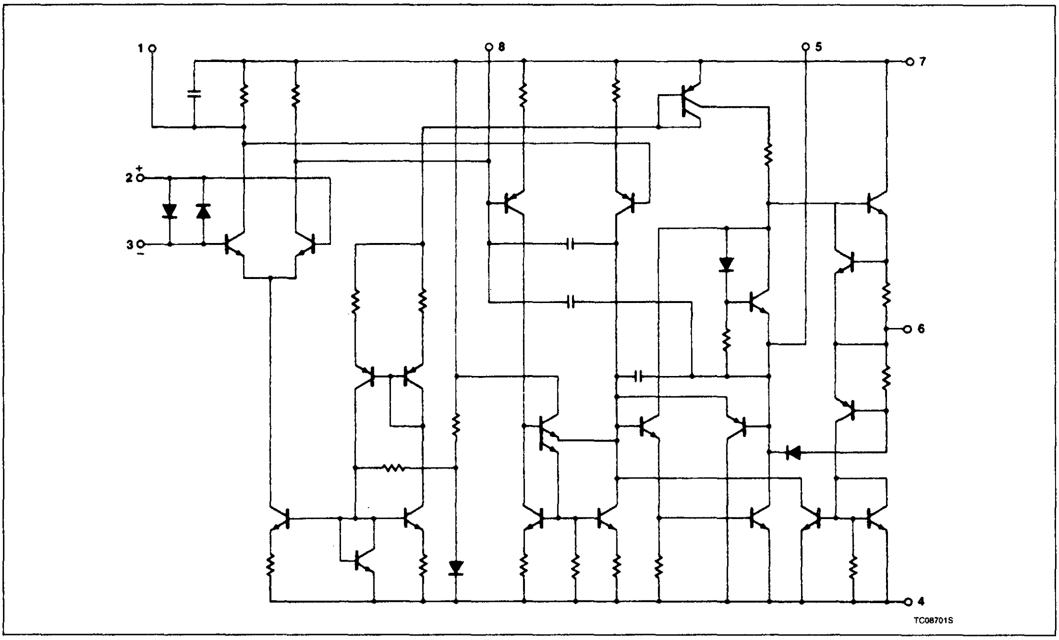
CD11390S

NOTE:
This device may not be symboled in standard format.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5533N
16-Pin Plastic SO package	0 to +70°C	NE5533AD
14-Pin Plastic DIP	0 to +70°C	NE5533AN
16-Pin Plastic SO package	0 to +70°C	NE5533D
8-Pin Plastic SO package	0 to +70°C	NE5534D
8-Pin Hermetic Cerdip	0 to +70°C	NE5534FE
8-Pin Plastic DIP	0 to +70°C	NE5534N
8-Pin Plastic SO package	0 to +70°C	NE5534AD
8-Pin Hermetic Cerdip	0 to +70°C	NE5534AFE
8-Pin Plastic DIP	0 to +70°C	NE5534AN
8-Pin Plastic DIP	-40°C to +85°C	SA5534N
8-Pin Plastic SO package	-40°C to +85°C	SA5534AD
8-Pin Plastic DIP	-40°C to +85°C	SA5534AN
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AFE
8-Pin Plastic DIP	-55°C to +125°C	SE5534N
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534FE
8-Pin Plastic DIP	-55°C to +125°C	SE5534AN

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	SE	-55 to +125	°C
	SA	-40 to +85	°C
	NE	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533D	1350	mW
	5533N	1500	mW
	5534D	750	mW
	5534FE	800	mW
	5534N	1150	mW
	Output short-circuit duration[3]	Indefinite	
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistance:
   8-pin ceramic DIP 150°C/W
   8-pin plastic DIP 105°C/W
   8-pin plastic SO 160°C/W
   14-pin plastic DIP 80°C/W
   16-pin plastic SO 90°C/W
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NE/SA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		μV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current per op amp			4	6.5		4	8	mA
		Over temperature			9			10	mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large-signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16		±15	±16		V
		$R_L \geq 2k\Omega$	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±12	±12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES:
1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$.
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$.
3. For SA5534/5534A, $T_{MIN} = -40°C$, $T_{MAX} = +125°C$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

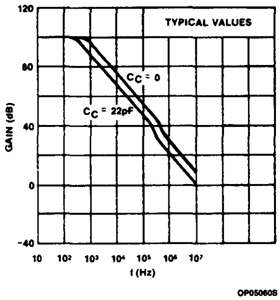
SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NESA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ closed-loop $f = 10kHz$, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
	Transient response	Voltage-follower, $V_{IN} = 50mV$ $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$							
t_R	Rise time			20			20		ns
	Overshoot			20			20		%
	Transient response	$V_{IN} = 50mV$, $R_L = 600\Omega$ $C_C = 47pF$, $C_L = 500pF$							
t_R	Rise time			50			50		ns
	Overshoot			35			35		%
A_V	Gain	$f = 10kHz$, $C_C = 0$ $f = 10kHz$, $C_C = 22pF$		6 2.2			6 2.2		V/mV V/mV
GBW	Gain bandwidth product	$C_C = 22pF$, $C_L = 100pF$		10			10		MHz
SR	Slew rate	$C_C = 0$ $C_C = 22pF$		13 6			13 6		V/μs V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$, $C_C = 0$ $V_{OUT} = \pm 10V$, $C_C = 22pF$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$ $C_C = 22pF$, $V_{CC} = \pm 18V$		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 15V$, unless otherwise specified.

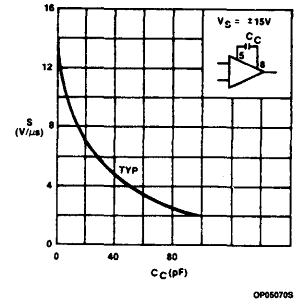
SYMBOL	PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	$f_O = 30Hz$ $f_O = 1kHz$		7 4			5.5 3.5	7 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
I_{NOISE}	Input noise current	$f_O = 30Hz$ $f_O = 1kHz$		2.5 0.6			1.5 0.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Broadband noise figure	$f = 10Hz - 20kHz$, $R_S = 5k\Omega$					0.9		dB
	Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

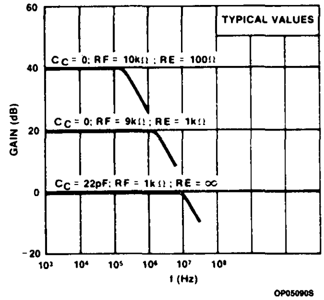
Open-Loop Frequency Response



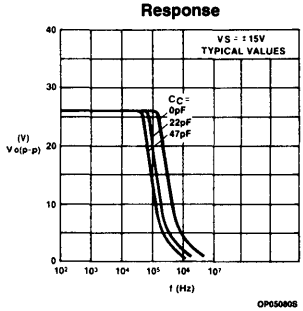
Slew Rate as a Function of Compensation Capacitance



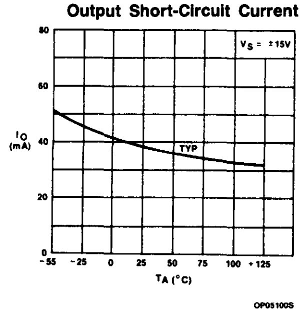
Closed-Loop Frequency Response



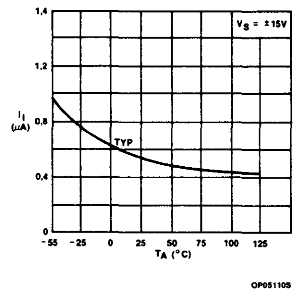
Large-Signal Frequency Response



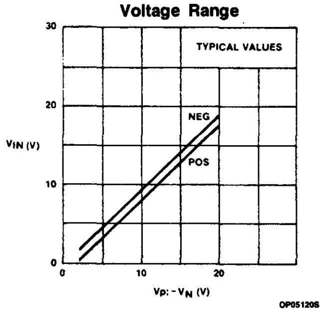
Output Short-Circuit Current



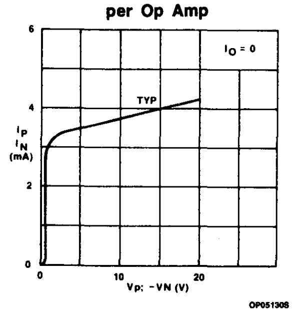
Input Bias Current



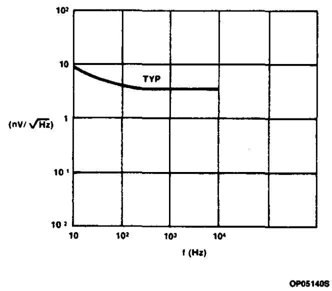
Input Common-Mode Voltage Range



Supply Current per Op Amp

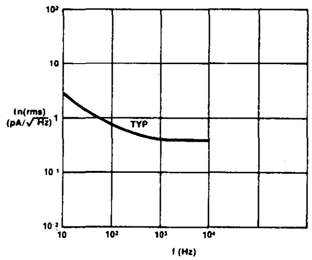


Input Noise Voltage Density

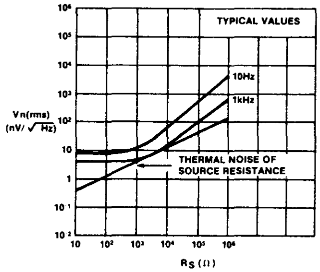


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

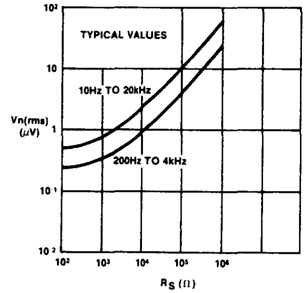
Input Noise Current Density



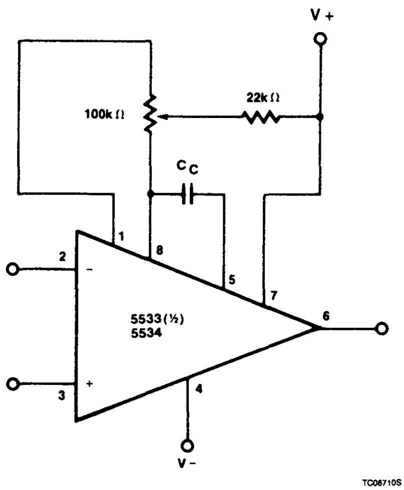
Total Input Noise Density



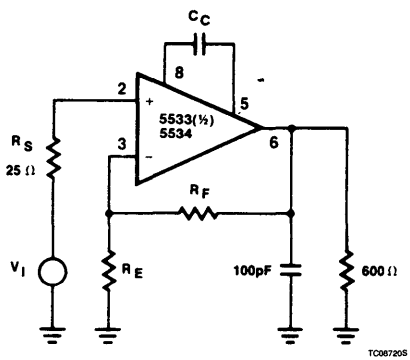
Broadband Input Noise Voltage



TEST LOAD CIRCUITS

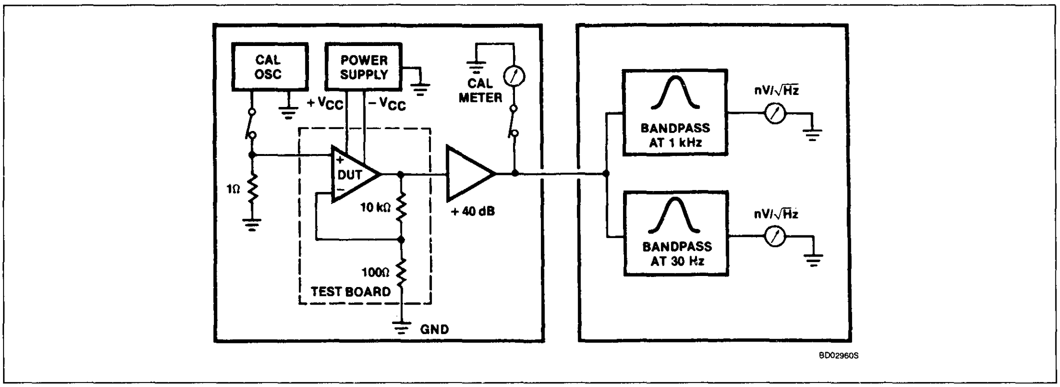


Frequency Compensation and Offset Voltage Adjustment Circuit



Closed-Loop Frequency Response

NOISE TEST BLOCK DIAGRAM



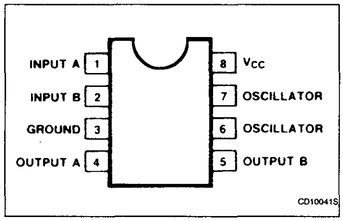
NE/SA602
Double-Balanced Mixer and Oscillator

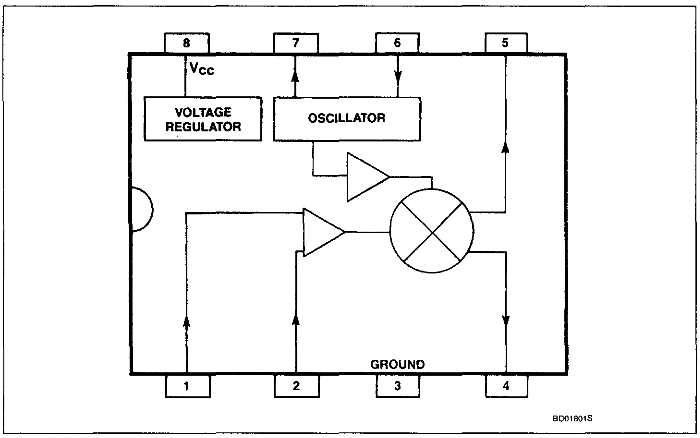
Product Specification

DESCRIPTION
The SA/NE602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES
- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

APPLICATIONS
- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

PIN CONFIGURATION


BLOCK DIAGRAM


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602N
8-Pin Plastic SO	0 to +70°C	NE602D
8-Pin Cerdip	0 to +70°C	NE602FE
8-Pin Plastic DIP	-40°C to +85°C	SA602N
8-Pin Plastic SO	-40°C to +85°C	SA602D
8-Pin Cerdip	-40°C to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE602 SA602	0 to +70 -40 to +85	°C °C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0	6.0	dB
	Third-order intercept point	$RF_{IN} = -45dBm$: $f_1 = 45.0$ $f_2 = 45.06$		−15	−17	dBm
	Conversion gain at 45MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

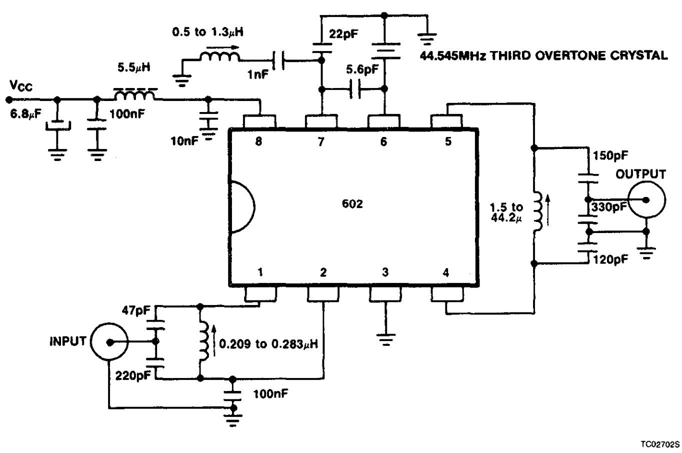


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE/SA602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least 200mV_{P-P}.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

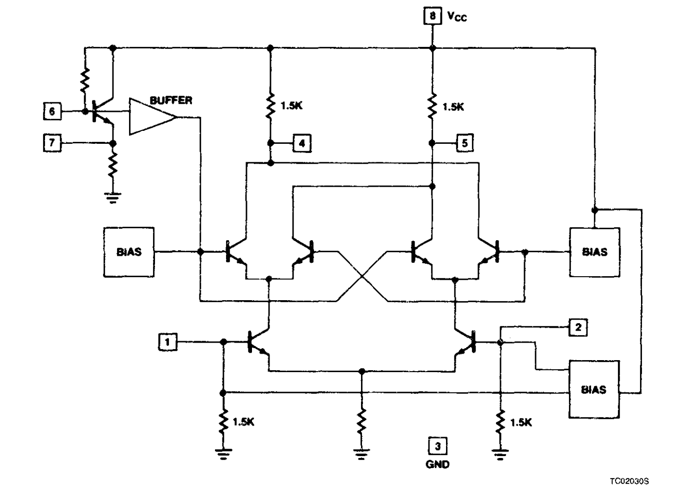
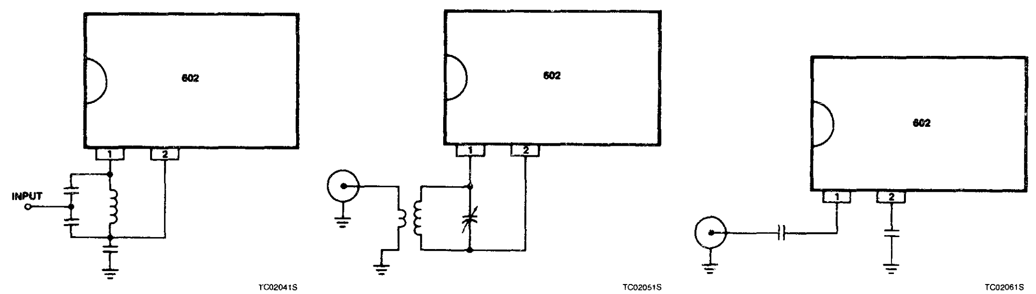


Figure 2. Equivalent Circuit

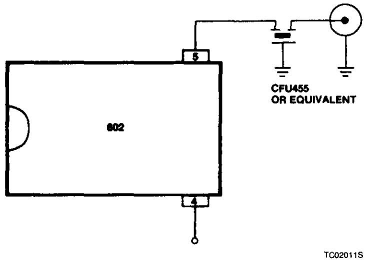


a. Single-Ended Tuned Input

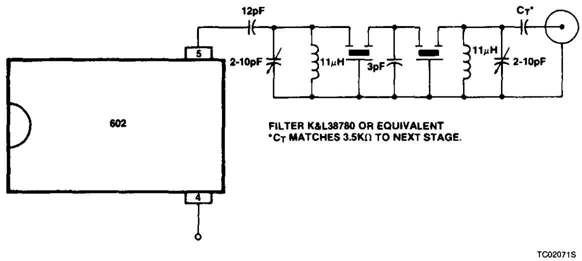
b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

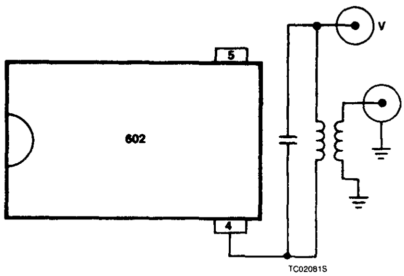
Figure 3. Input Configuration



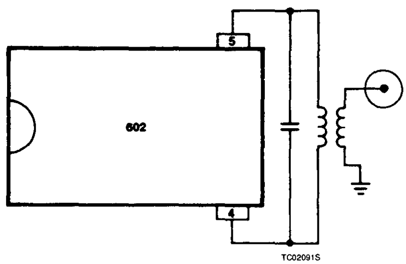
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

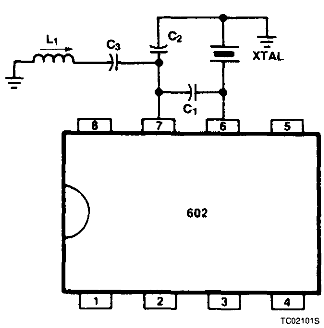


c. Single-Ended IFT

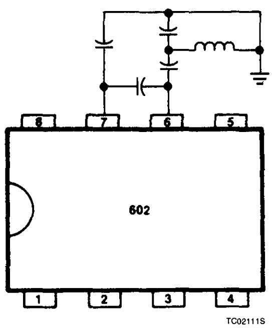


d. Balanced Output

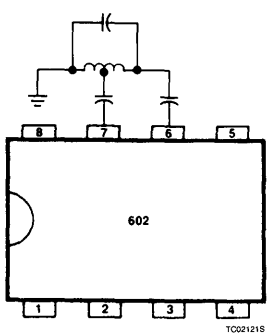
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

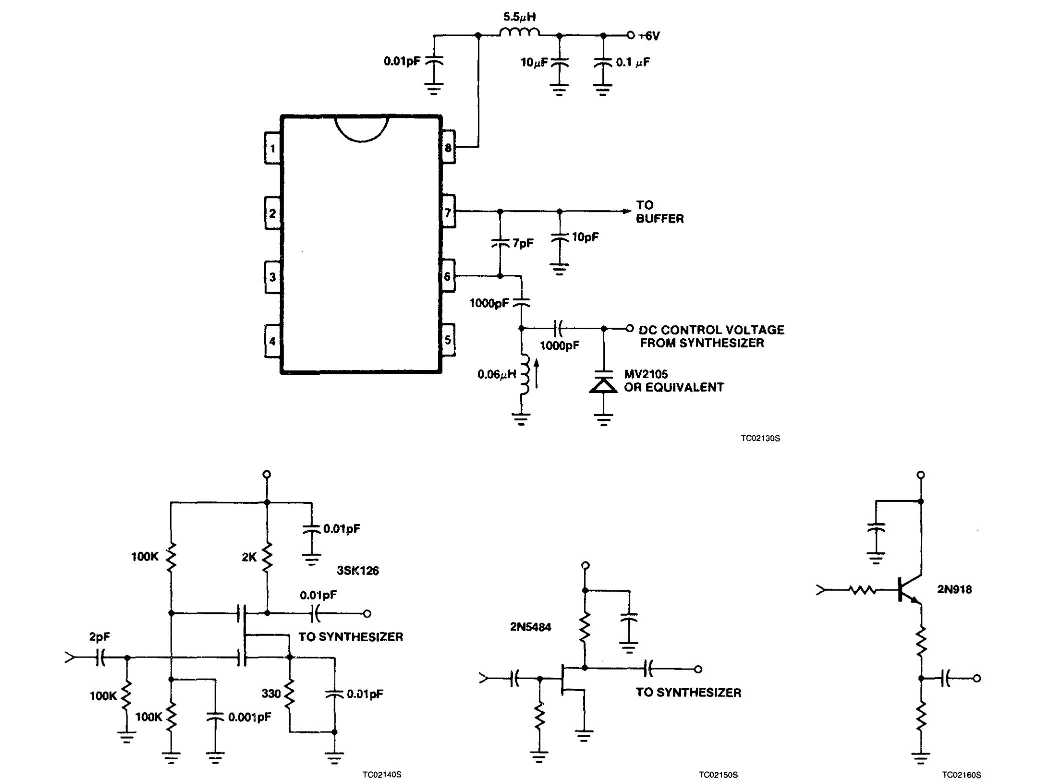


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

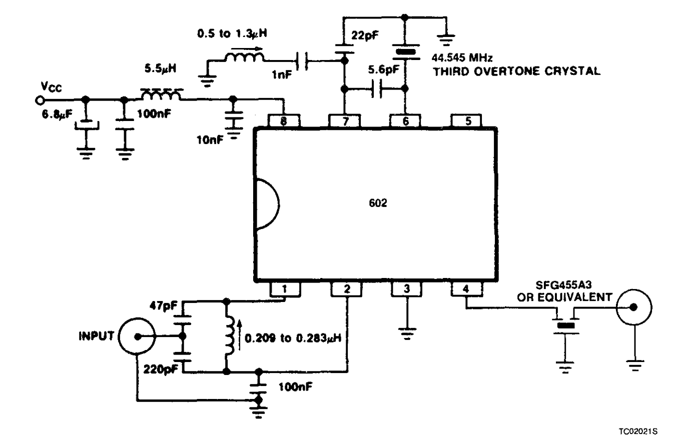


Figure 7. Typical Application for Cellular Radio

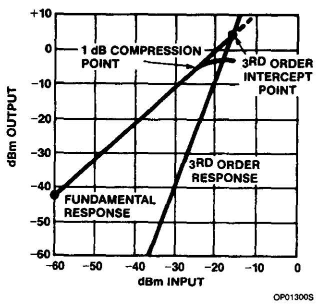


Figure 8. NE/SA602 Third-Order Intermod and 1dB Compression Point Performance

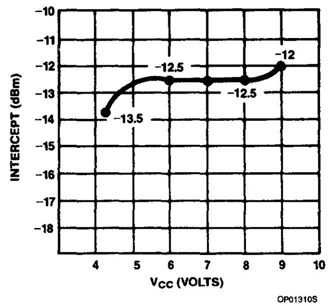


Figure 9. Input Third-Order Intercept Point vs V_{CC}

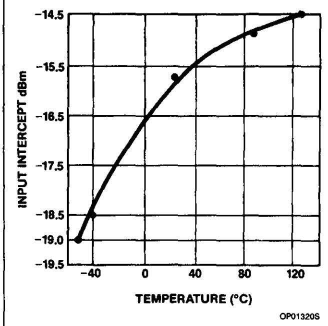


Figure 10. Third-Order Intercept Point vs Temperature

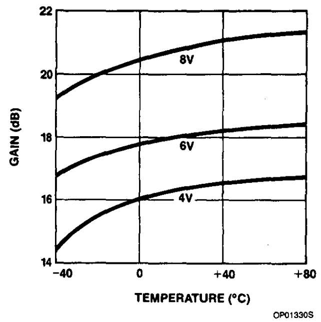


Figure 11

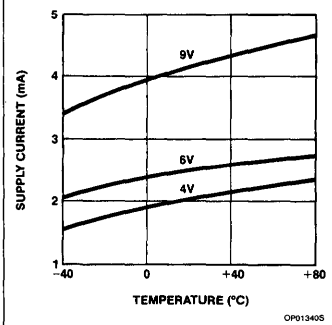


Figure 12

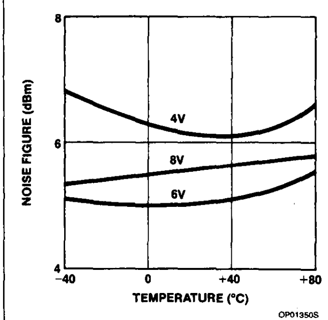


Figure 13

Signetics

NE/SA604A
High-Performance Low-Power FM IF System

Preliminary Specification

Linear Products

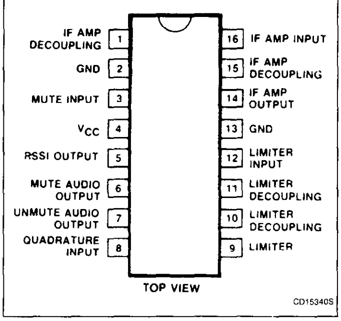
DESCRIPTION
The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature package).

FEATURES
- **Low-power consumption 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA604A meets cellular radio specifications**

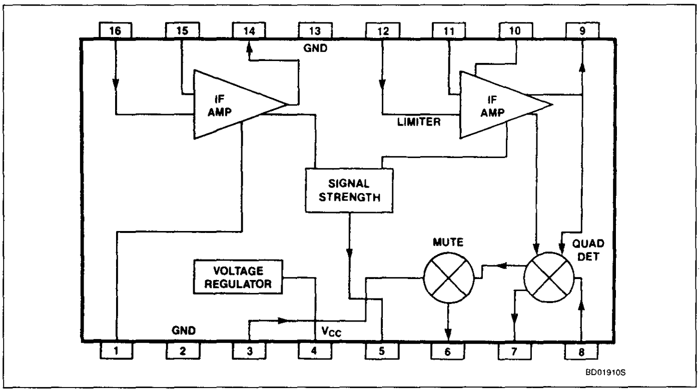
APPLICATIONS
- **Cellular Radio FM IF**
- **High performance communications receivers**
- **Intermediate freqency amplification and detection up to 21MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

PIN CONFIGURATION

D and N Packages



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604AN
16-Pin Plastic SO (Surface-mounted miniature package)	0 to +70°C	NE604AD
16-Pin Plastic DIP	−40 to +85°C	SA604AN
16-Pin Plastic SO (Surface-mounted miniature package)	−40 to +85°C	SA604AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating temperature NE604A SA604A	 0 to 70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Power supply voltage range		4.5		8.0	4.5		8.0	V
	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. IF frequency = 455kHz; IF level = −47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

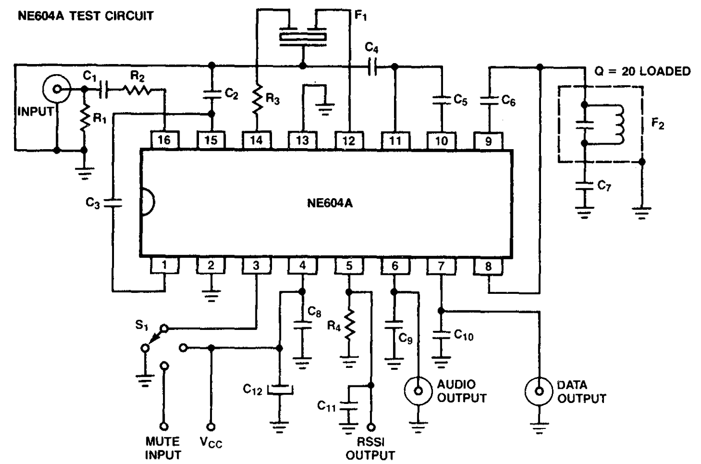
SYMBOL	PARAMETER	TEST CONDITIONS	NE604A			SA604A			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input limiting-3dB	Test at Pin 16		−92			−92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{rms}
	Recovered audio level	150pF de-emphasis		530			530		mV_{rms}
	SINAD sensitivity	RF level −97dBm		16			16		dB
	THD		−35	−42		−34	−42		dB
	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = −118dBm	0	160	550	0	160	650	mV
		RF level = −68dBm	2.0	2.65	3.0	1.09	2.65	3.1	V
		RF level = −18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k Pin 5		90			90		dB
	RSSI accuracy	R_4 = 100k Pin 5		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		Ω

NOTE:

1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

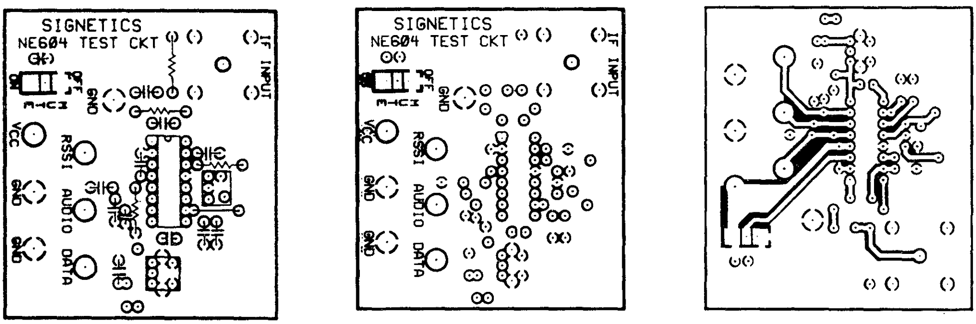
NE604(50)	NE604A (1.5k)/NE605 (1.5k)
−97dBm	−118dBm
−47dBm	−68dBm
+3 dBm	−18dBm

2. The NE605 and NE604A are both derived from the same basic die. The NE605 performance plot NE604A.



NOTES:

C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V
C3 100nF ± 10% 50V
C4 100nF ± 10% 50V
C5 100nF ± 10% 50V
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V
C8 100nF ± 10% 50V
C9 15nF ± 10% 50V
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% ¼W Metal Film
R2 1500Ω ± 1% ¼W Metal Film
R3 1500Ω ± 5% ⅛W Carbon Composition
R4 100kΩ ± 1% ¼W Metal Film



CD15410S CD15380S CD15390S

Figure 1. NE604A Test Circuit

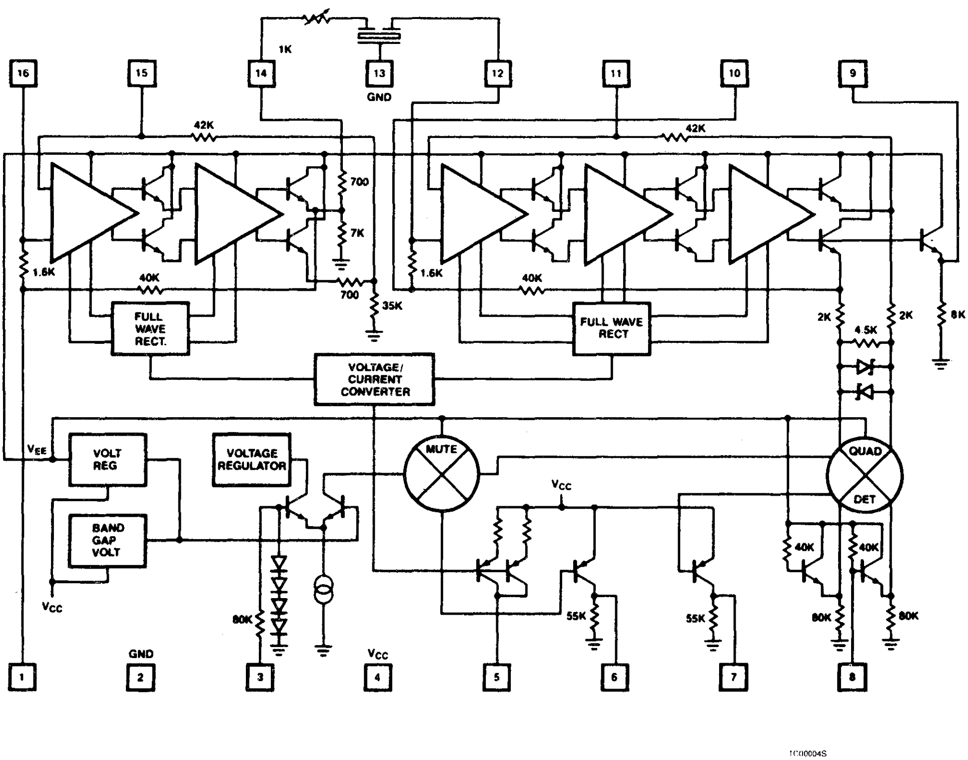


Figure 2. Equivalent Circuit

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A can not be evaluated independent of circuit, components, and board layout. A physicial layout which correlates to the electrical limits is shown in Figure 1. The configuration can be used as the basis for production layout.

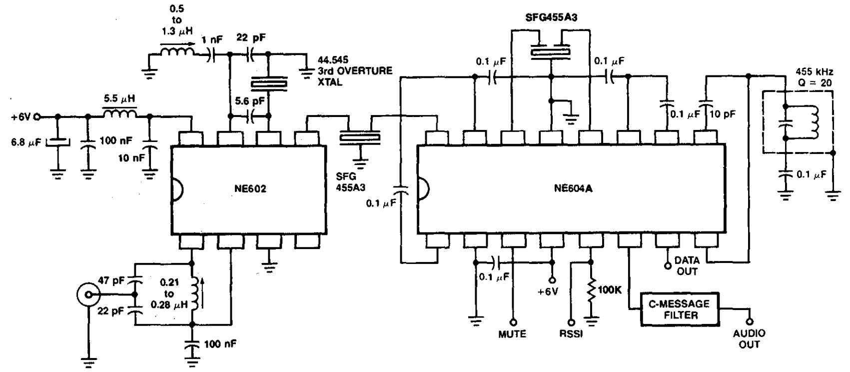
The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF AMPLIFIERS

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bankwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin



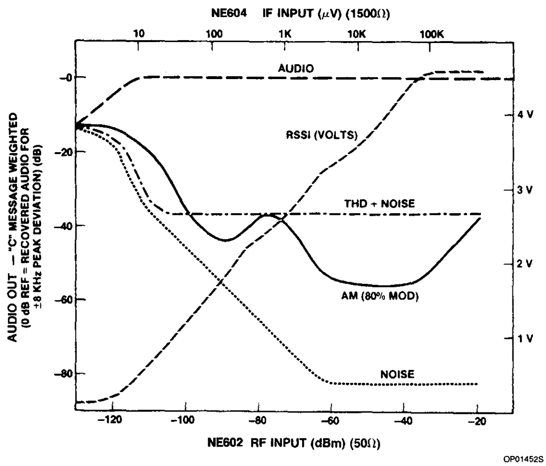


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

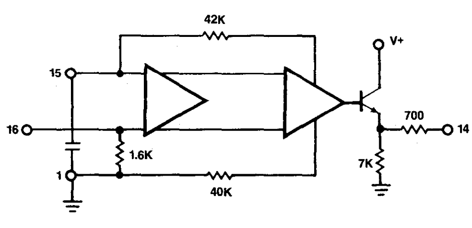


Figure 4. First Limiter Bias

to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduce gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

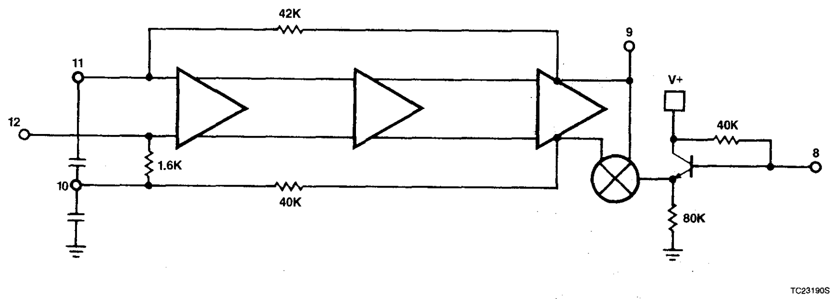


Figure 5. Second Limiter and Quadrature Detector

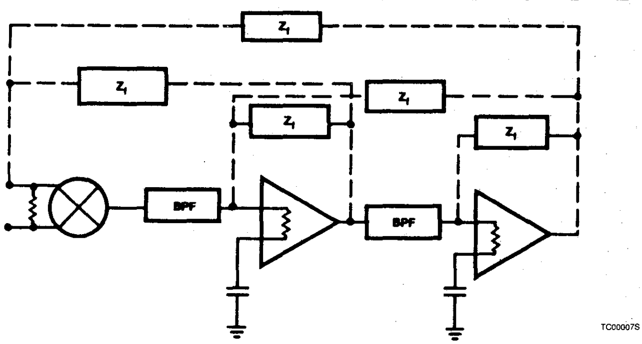


Figure 6. Feedback Paths

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and grounds, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptible with this layout. Every layout must be evaluated on its own merit, don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

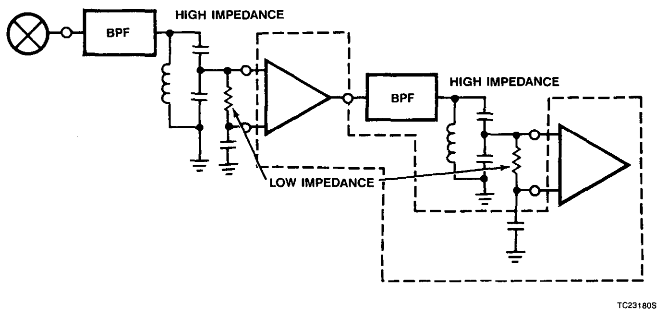
As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrow-band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean nonexistent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

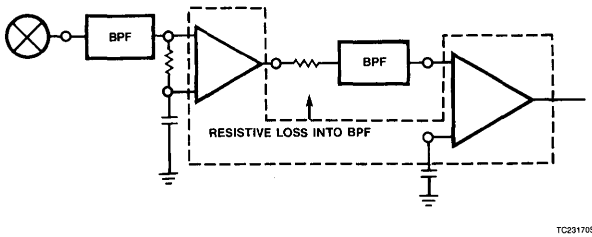
The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single ended to an external capacitor at Pin 9. There is a 90° phase shift across the phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multipler at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

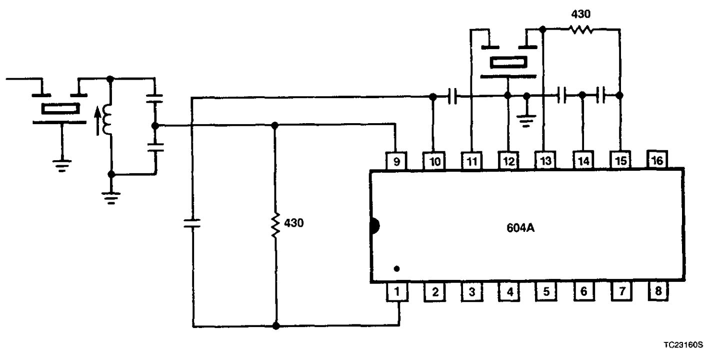


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

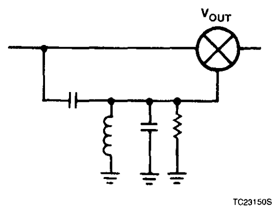


Figure 9.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

Frequency Discriminator Design Equations for NE604A

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_N \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_3 will be:

$$\phi = \angle V_O - \angle V_N = tg^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10. Is the plot of ϕ vs $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}.$$

The signal V_o would have a phase shift of $\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \quad (3)$$

$$\rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \quad (4)$$

after low pass filtering

$$\rightarrow V_{OUT} = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] = \frac{1}{2}A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega \quad (5)$$

$$V_{OUT} \propto 2Q_1\left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is the discriminated FM output.

NOTE: $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p.311. Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the ϕ vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discrimination FM signal. (Eq.6)

→Choose a Q = 20.

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S$ = 174pF and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH, should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be the logical output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10 MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1Ω resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an inband signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

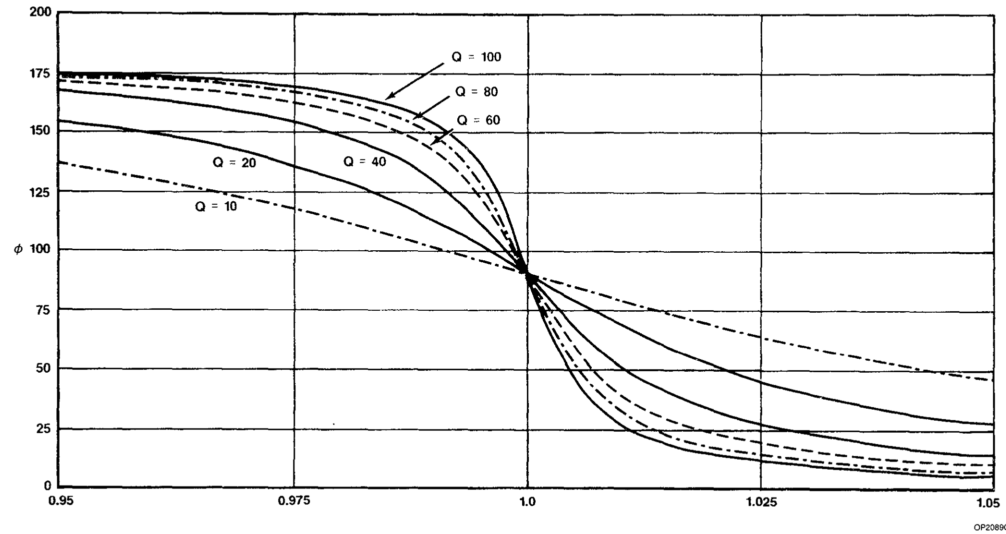


Figure 10. Phase vs. Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

NE/SA605
Low Power FM IF System

Objective Specification

DESCRIPTION

The NE/SA605 is a monolithic, low power FM IF system incorporating VHF monolithic, double-balanced mixer with input amplifier, on-board oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator.

It is intended for high performance, low power communication systems. The guaranteed parameters of the SA605 make this device particularly well-suited to cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 15dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low power, and noise characteristics make the NE/SA605 a superior choice for high-performance battery-operated equipment.

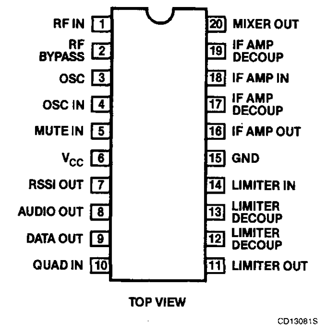
The NE/SA605 is available in 20-lead dual in-line plastic and Cerdip packages and 20-pin SO (surface-mounted miniature) packages.

FEATURES

- **Low power consumption: 5.3mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept, and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA605 meets cellular radio specifications**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB**
- **Separate data output**
- **Audio output with muting**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal-to-Noise and Distortion ratio) at 455kHz**

PIN CONFIGURATION

D, F, N Packages



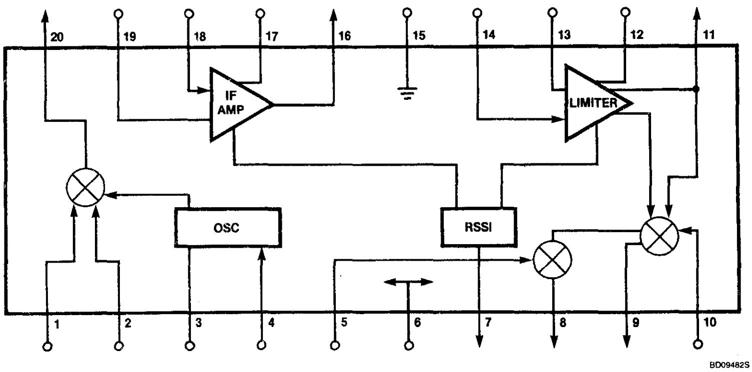
APPLICATIONS

- **Cellular radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE605N
20-Pin Plastic SO	0 to +70°C	NE605D
20-Pin Ceramic DIP	0 to +70°C	NE605F
20-Pin Plastic DIP	-40°C to +85°C	SA605N
20-Pin Plastic SO	-40°C to +85°C	SA605D
20-Pin Ceramic DIP	-40°C to +85°C	SA605F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range NE605 SA605	 0 to +70 -40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			5.3	6.0	mA
	Mute switch input threshold (on) (off)		 1.7		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz; IF frequency = 455MHz; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point	$RF_{IN} = -45dBm$: $f_1 = 45.0$ $f_2 = 45.06$		-15		dBm
	Conversion gain at 45MHz			15		dB
R_{IN}	RF input resistance	Single-ended input	1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 20)		1.5		kΩ
	Input limiting -3dB	Test at Pin 1		-117		dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level -117dBm	12	15		dB
THD	Total harmonic distortion		-35			dB
S/N	Signal-to-noise ratio	No modulation for noise	70	75		dB
	RSSI output	$R_{RSSI} = 100K$ RF level = -117dBm RF level = -67dBm RF level = -23dBm	 0 2.0 4.0		 400 2.6 5.0	 mV V V
	RSSI range	$R_{RSSI} = 100k$ Pin 7		90		dB
	RSSI accuracy	$R_{RSSI} = 100k$ Pin 7		±1.5		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance			50		kΩ
	Muted audio output impedance			50		kΩ

Circuit Description

The NE/SA605 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 500MHz. The bandwidth of the IF amplifiers is 25MHz. However, the gain distribution is optimized for 455kHz. The overall system is well-suited to battery operation as well as high-performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 15dB, and input third order intercept of −15dBm. The oscillator will operate well in excess of 200MHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The equivalent input impedance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network..

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 92dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability. Alternatively, if gain distribution permits, only the second limiting IF stage can be used. This stage has 57dB of gain.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

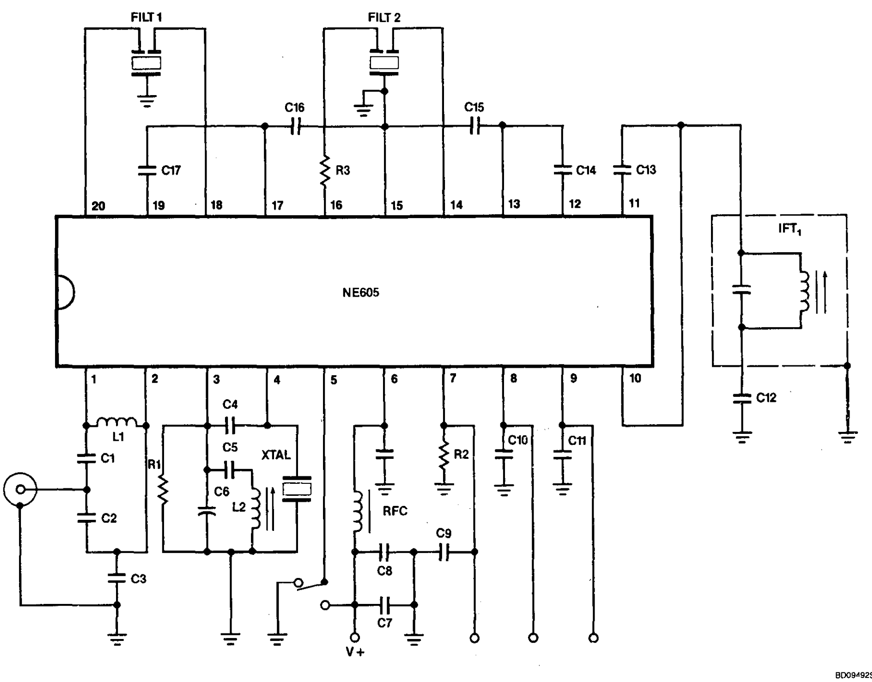


Figure 1. NE/SA605 45MHz Test and Application Circuit

NE612
Double-Balanced Mixer and Oscillator

Product Specification

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

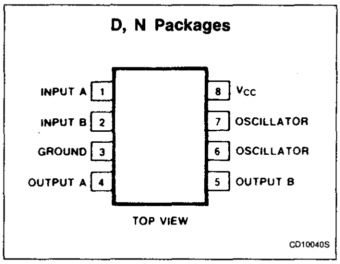
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

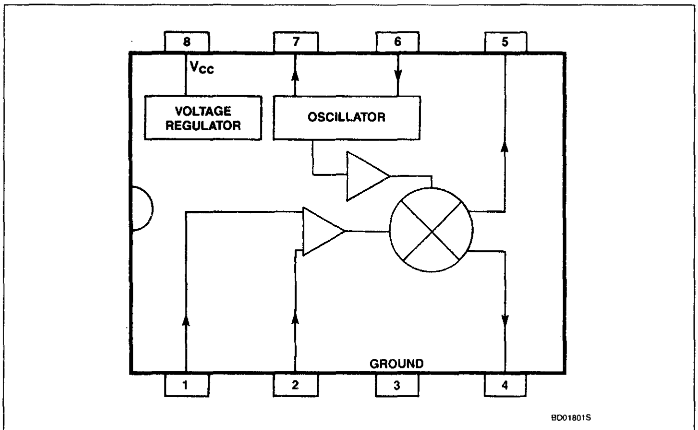
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



Double-Balanced Mixer and Oscillator

NE612

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	$RF_{IN} = -45dBm$		−15		dBm
	Conversion gain at 49MHz		14	18		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

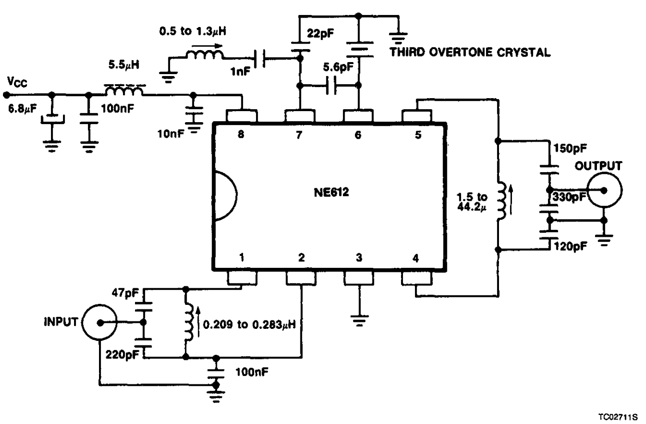


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be $200mV_{P-P}$ minimum to $300mV_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

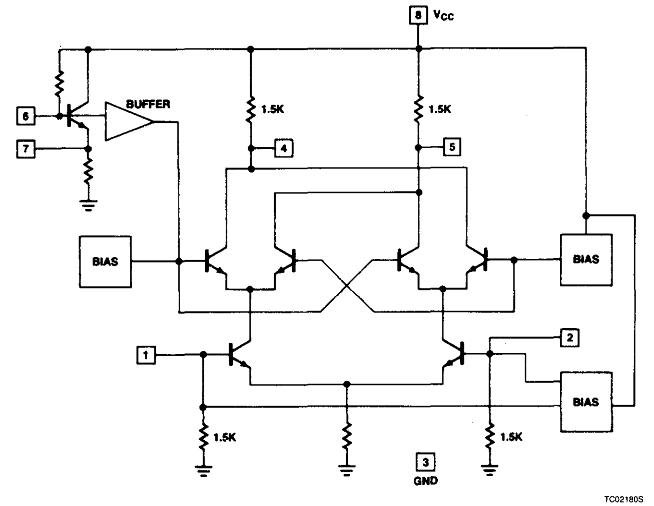
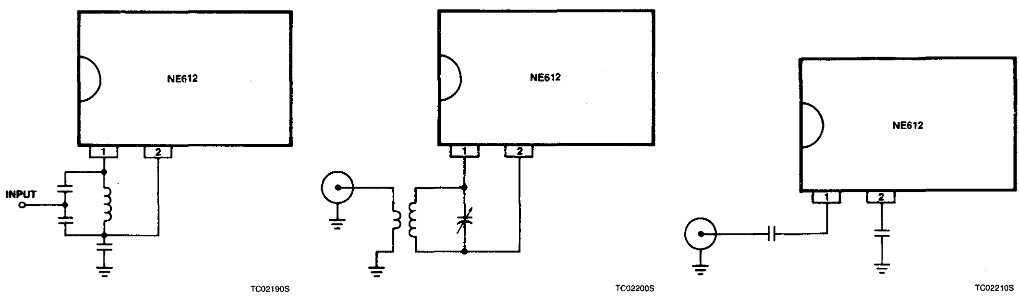
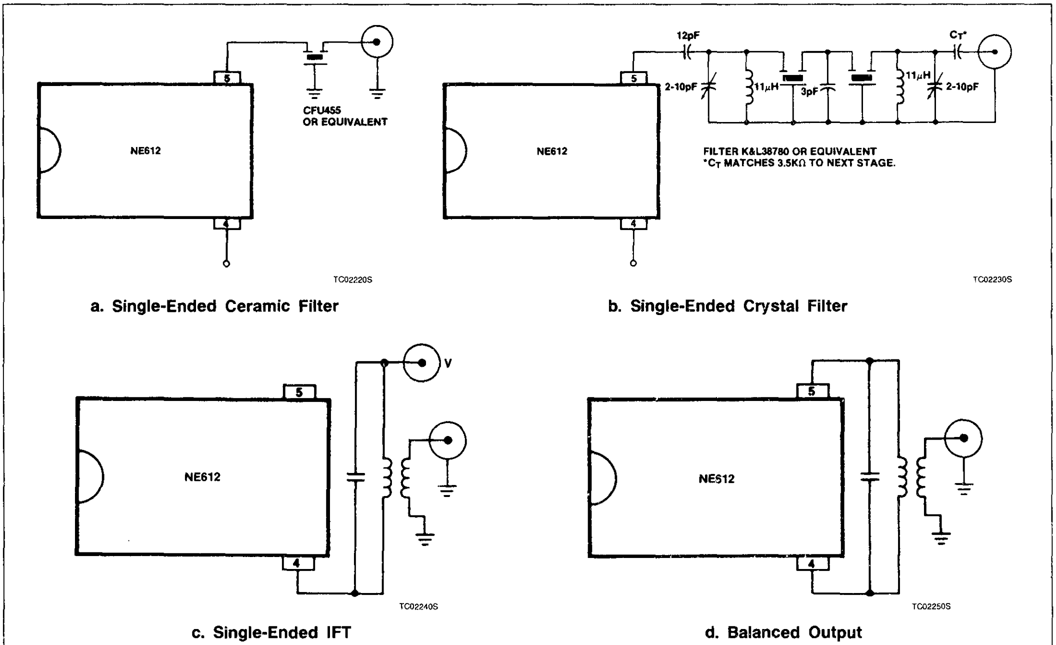


Figure 2. Equivalent Circuit



a. Single-Ended Tuned Input **b. Balanced Input (for Attenuation of Second Order Products)** **c. Single-Ended Untuned Input**

Figure 3. Input Configuration



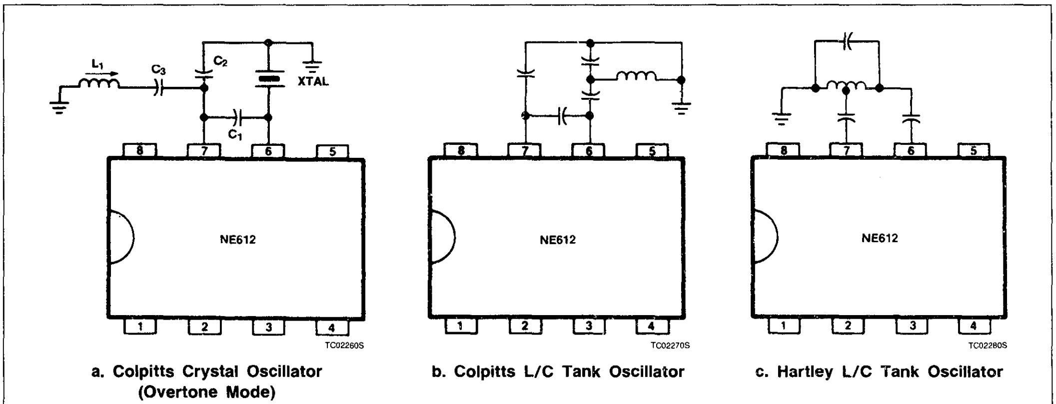
a. Single-Ended Ceramic Filter

b. Single-Ended Crystal Filter

c. Single-Ended IFT

d. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

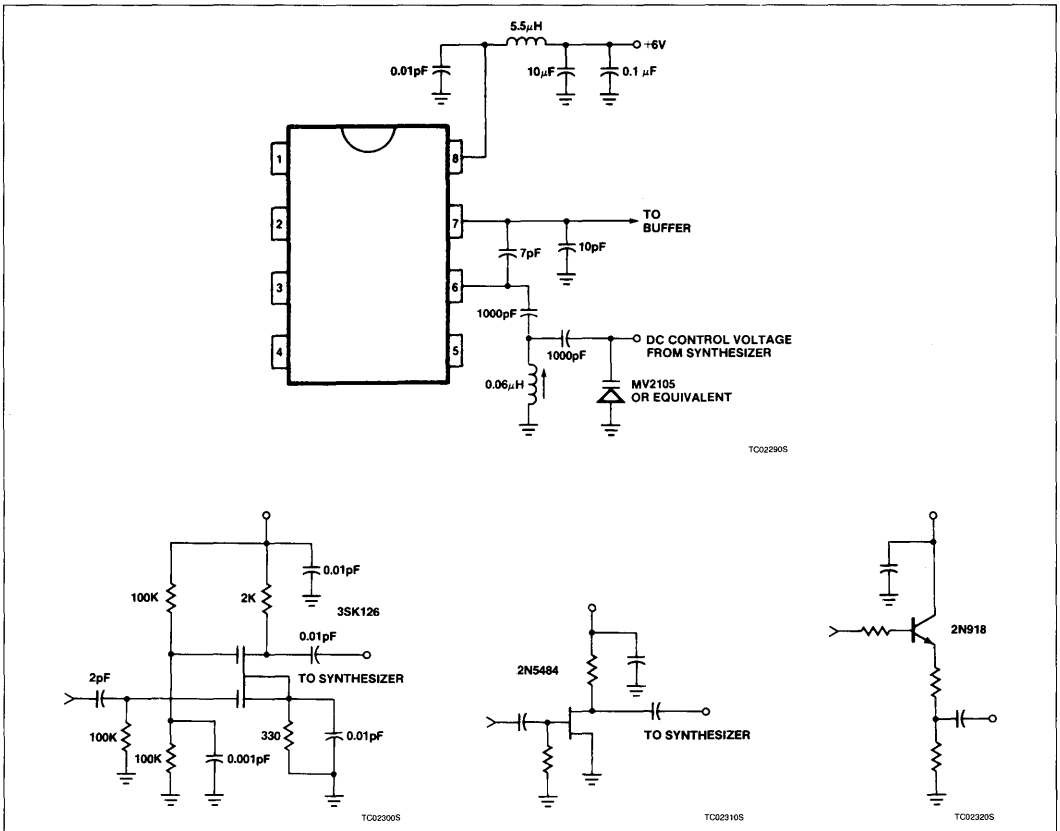


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

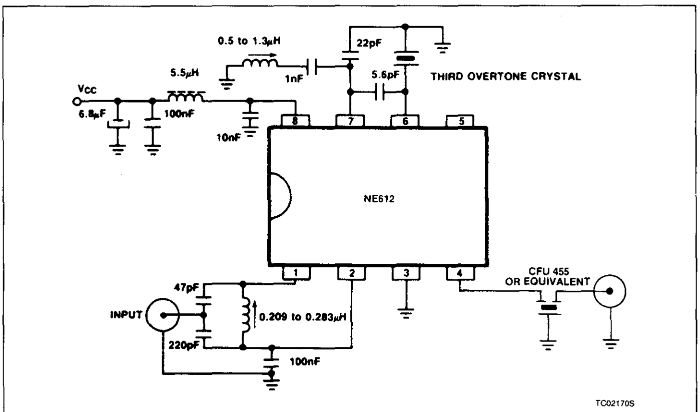


Figure 7. Typical Application for 46/49MHz Cordless Telephone

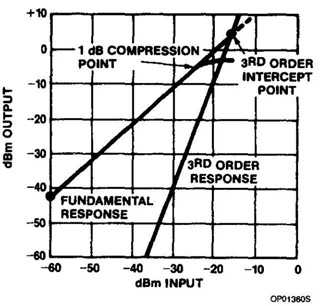


Figure 8. NE612 Third-Order Intermod and 1dB Compression Point Performance

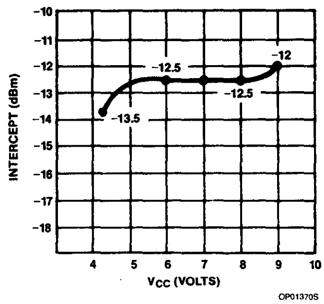


Figure 9. Input Third-Order Intercept Point vs V_{CC}

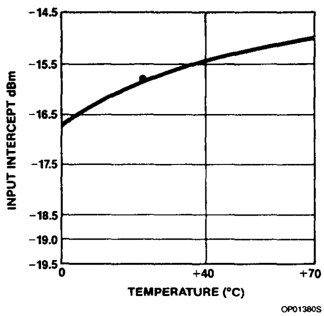


Figure 10. Third-Order Intercept Point vs Temperature

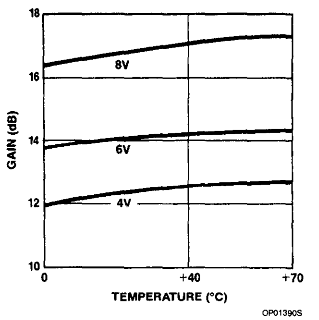


Figure 11

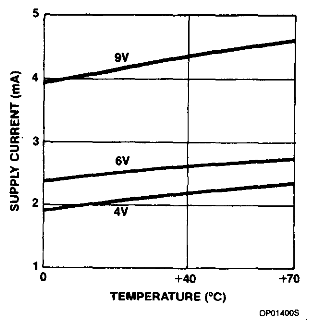


Figure 12

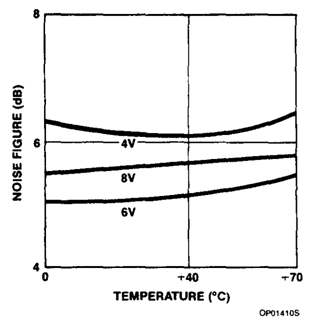


Figure 13

NE/SA614A
Low Power FM IF System

Preliminary Specification

DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature package).

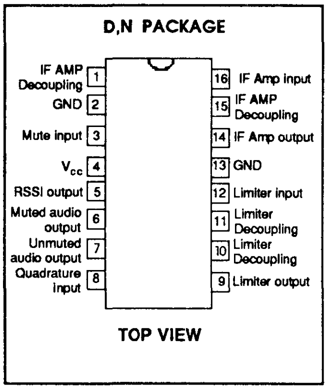
FEATURES

- **Low-power consumption 3.3mA typical**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs - muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**
- **SA614A meets consumer cellular radio specifications**

APPLICATIONS

- **Consumer cellular radio FM IF**
- **Consumer communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**

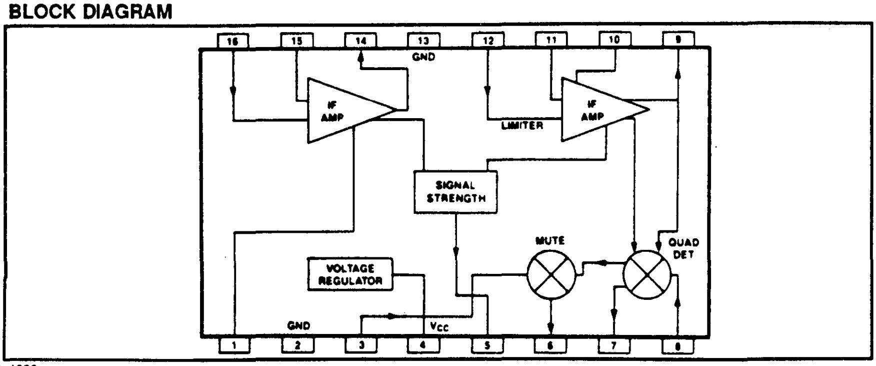
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614AN
16-Pin Plastic SO (Surface-mounted miniature package);	0 to +70°C	NE614AD
16-Pin Plastic DIP	-40 to +85°C	SA614AN
16-Pin Plastic SO (Surface-mounted miniature package);	-40 to +85°C	SA614AD

BLOCK DIAGRAM



September 13, 1988

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	-65 to +150	°C
Operating temperature		
NE614A	0 to 70	°C
SA614A	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated

PARAMETER	TEST CONDITIONS	NE614A			SA614A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power supply voltage range		4.5		8.0	4.5		8.0	V
DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
Mute switch input threshold (on)		1.7			1.7			V
(off)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS Typical reading at $T_A = 25°C$; $V_{CC} = +6V$ unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

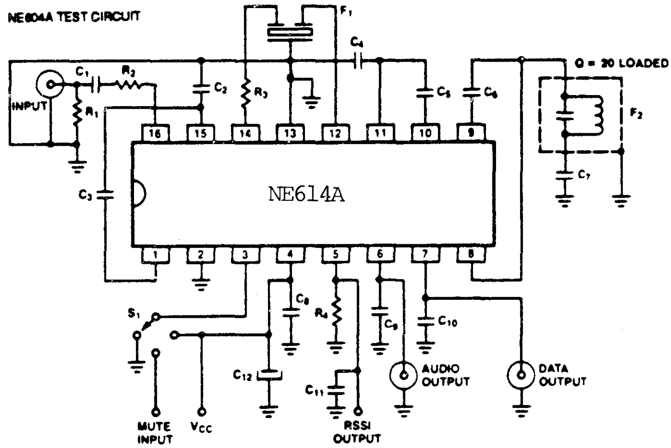
PARAMETER	TEST CONDITIONS	NE/SA614A			UNIT
		MIN	TYP	MAX	
Input limiting - 3dB	Test at Pin 16		-92		dBm/50Ω
AM rejection	80% AM 1kHz	25	33		dB
Recovered audio level	15nF de-emphasis	60	175	260	mV_{rms}
Recovered audio level	150pF de-emphasis		530		mV_{rms}
SINAD sensitivity	RF level -97dBm		12		dB
THD		-30	-42		dB
Signal-to-noise ratio	No modulation for noise		68		dB
RSSI output	RF level = -118dBm	0	160	800	mV
	RF level = -68dBm	1.7	2.50	3.3	V
	RF level = -18dBm	3.6	4.80	5.8	V
RSSI range	R_4 = 100k Pin 5		80		dB
RSSI accuracy	R_4 = 100k Pin 5		±2.0		dB
IF input impedance		1.4	1.6		kΩ
IF output impedance		0.85	1.0		kΩ
Limiter input impedance		1.4	1.6		kΩ
Unmuted audio output resistance			58		kΩ
Muted audio output resistance			58		kΩ

NOTE:

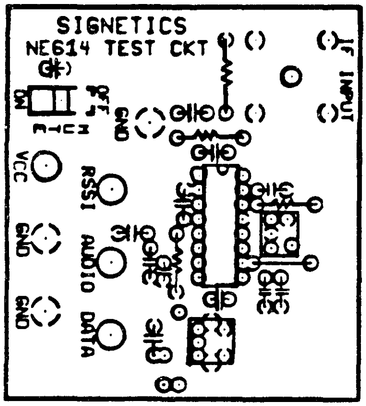
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

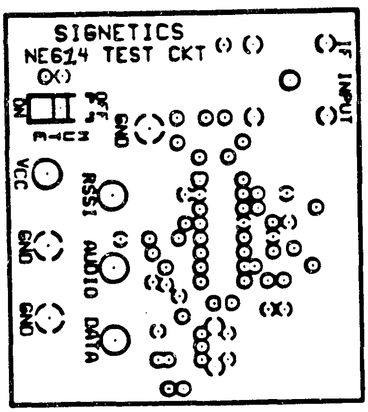
NE614A (50)	NE614A (1.5k)/NE615 (1.5k)
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V
C3 100nF ± 10% 50V
C4 100nF ± 10% 50V
C5 100nF ± 10% 50V
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V
C8 100nF ± 10% 50V
C9 15nF ± 10% 50V
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film





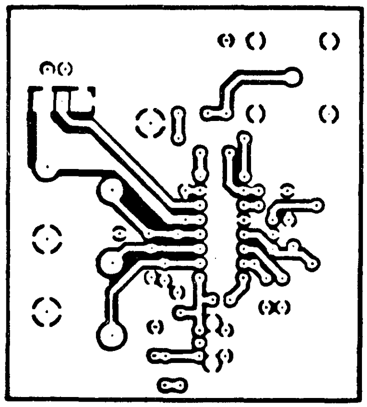


Figure 1. NE614A Test Circuit

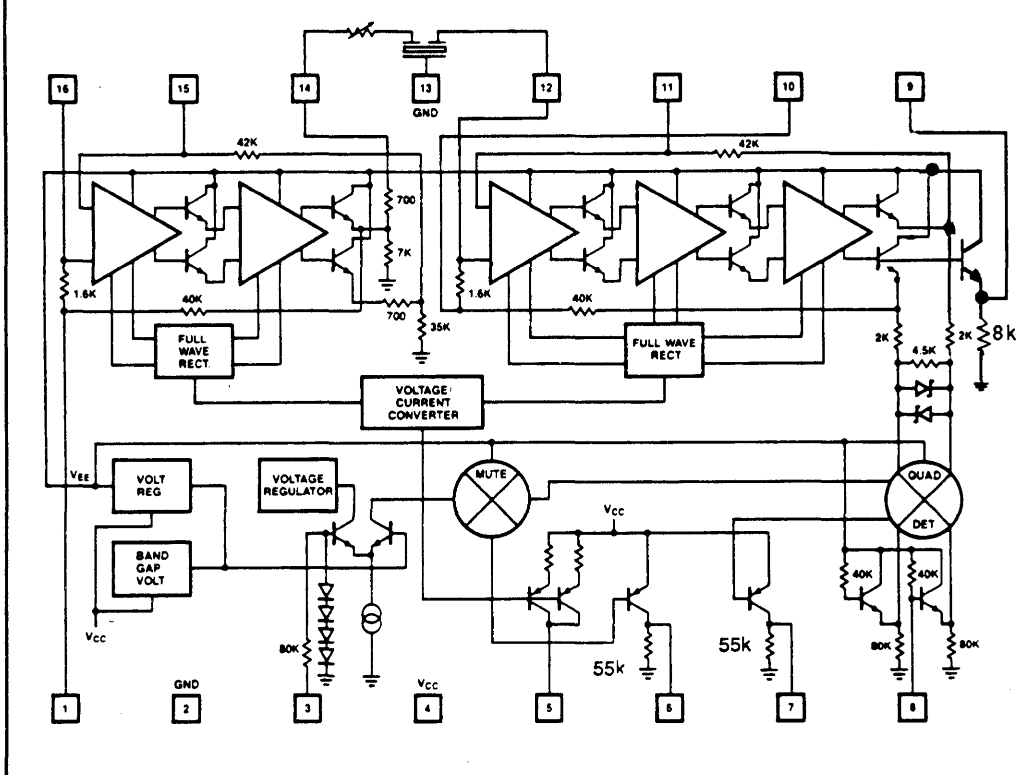


Figure 2. Equivalent Circuit

Circuit Description

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A can not be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feed-

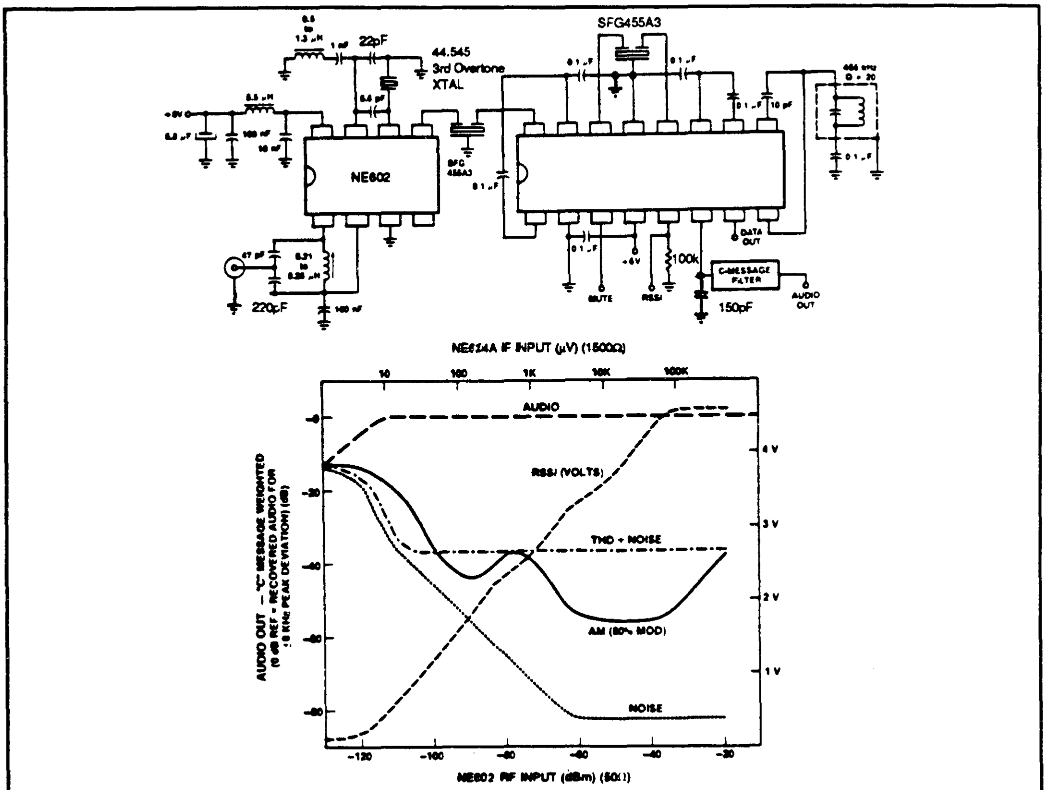


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

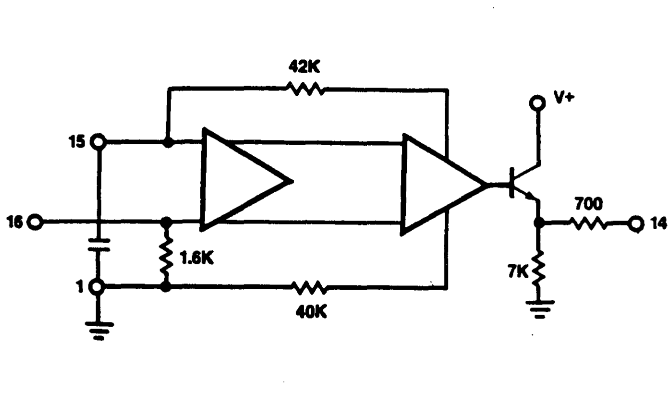


Figure 4. First Limiter Bias

back (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the

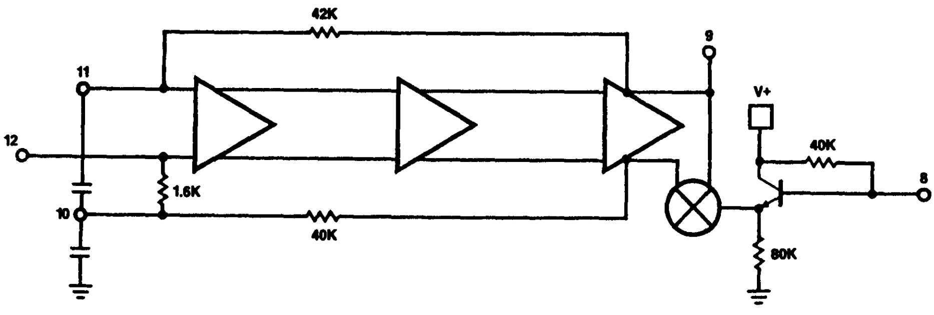


Figure 5. Second Limiter and Quadrature Detector

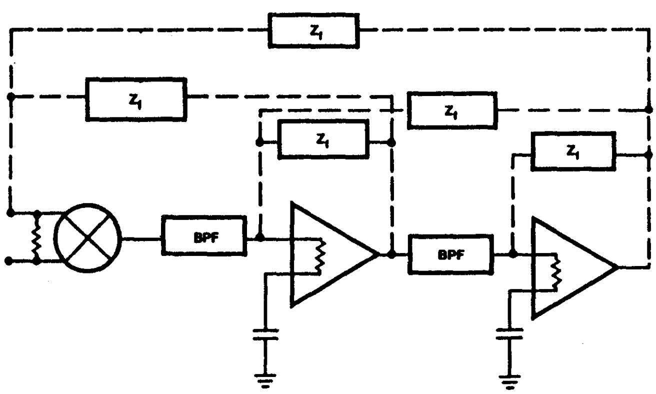


Figure 6. Feedback Paths

feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

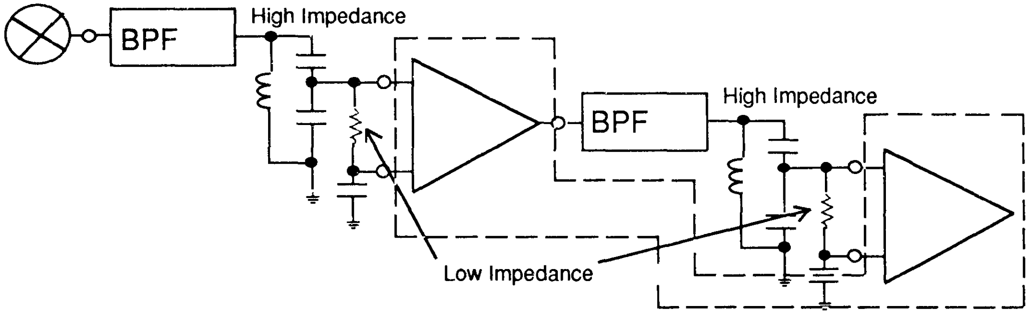
A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

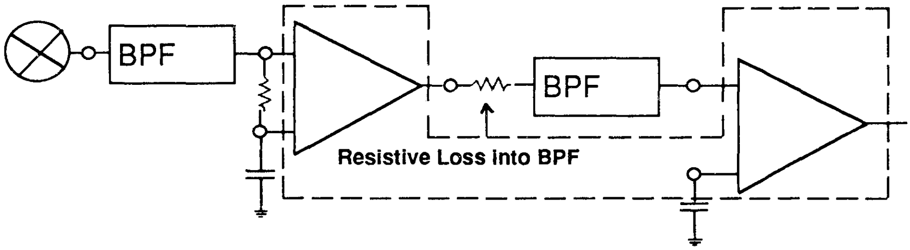
The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right at the V_{cc} pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1µF tantalum has proven acceptible with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

the filters. The input filter is a crystal type for narrow-band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

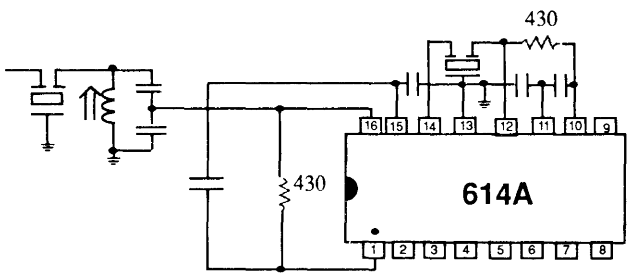


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

Frequency discriminator design equations for NE614A

$$V_O = \frac{C_S}{C_P + C_S} \cdot \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \cdot V_N \qquad (1a)$$

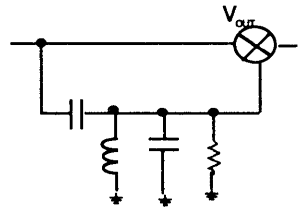


Figure 9.

$$\text{where} \quad \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_N = tg^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \qquad (2)$$

Figure 10. Is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \sin \omega t$

$$\Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \qquad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_N \cdot V_O = A^2 \sin \omega t \; \sin\left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \qquad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] \qquad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \qquad (6)$$

$$\text{For} \quad \frac{2Q_1\omega}{\omega_1} \ll \frac{\pi}{2}$$

Which is the discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.)

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p.311.

Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the ϕ vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$. The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq.6)

$\Rightarrow$ Choose a Q = 20.

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be the logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB . The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25µV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

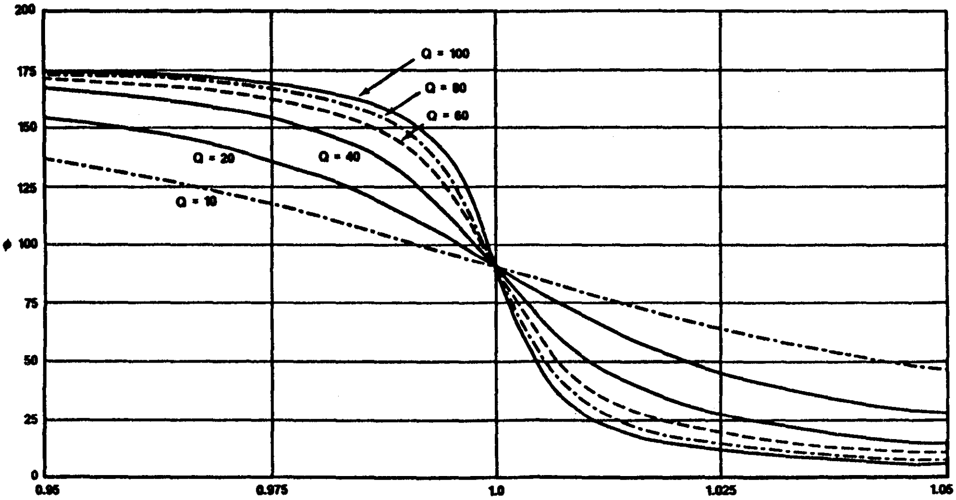


Figure 10. Phase vs. Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

NE645/646
Dolby Noise Reduction Circuit

Product Specification

DESCRIPTION

The NE645/646 is a monolithic audio noise reduction circuit designed as a direct replacement device for the NE645B/NE646B in Dolby* B-Type noise reduction systems. The NE645/646 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, California.

NOTE:
*T.M. Dolby Laboratories Licensing Corporation.

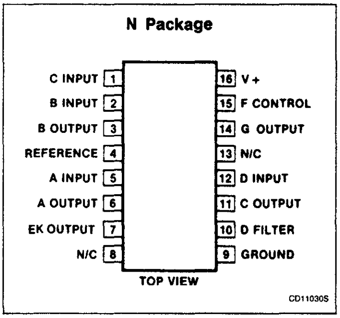
FEATURES

- **Accurate record mode frequency response**
- **Excellent frequency response tracking with temperature and V_{CC} ± 0.4 dB typical**
- **Excellent back-to-back dynamic response — DC shift less than 20mV typical**
- **Improved stability of all op amps**
- **High reliability packaging**

APPLICATIONS

- **Tape decks**
- **Dolby surround sound system**

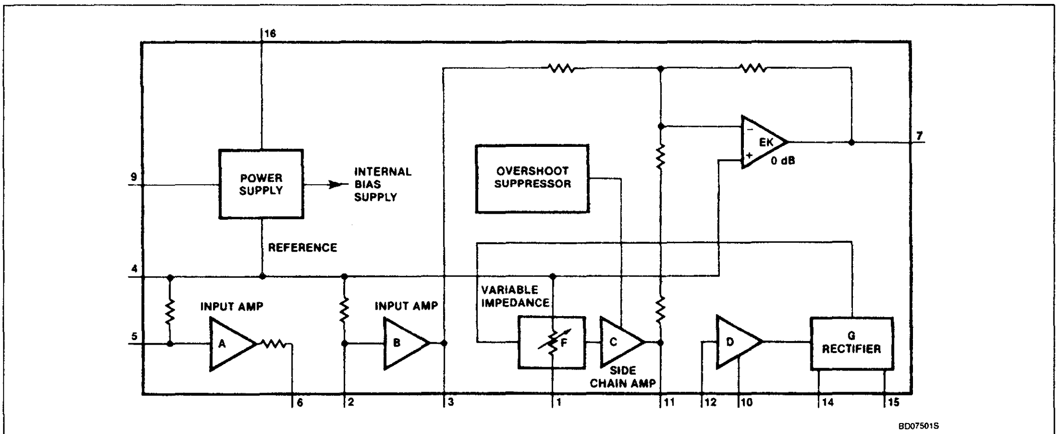
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE645N
16-Pin Plastic DIP	0 to +70°C	NE646N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	24	V
 T_A T_{STG}	Temperature range Operating ambient Storage	 0 to +70 -65 to +150	 °C °C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

DC ELECTRICAL CHARACTERISTICS

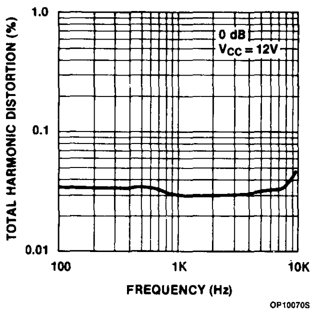
V_{CC} = 12V, f = 20Hz to 20kHz. All levels referenced to 580mV$_{RMS}$ (0dB) at Pin 3, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE645			NE646			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage Range		8		20	8		20	V
I_{CC}	Supply Current	V_{CC} = 12V		16	24		16	24	mA
A_V	Voltage gain (Pins 5-3)	f = 1kHz (Pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
A_V	Voltage gain (Pins 3-7)	f = 1kHz, 0 dB at Pin 3, noise reduction out	-0.5	0	+0.5	-0.5	0	+0.5	dB
	Distortion THD, 2nd and 3rd harmonic	f = 20Hz-10 kHz, 0dB f = 20Hz-10 kHz, +10dB		0.05 0.15	0.1 0.3		0.05 0.2	0.2 0.5	% %
	Signal handling[1] (V_{CC} = 12V)	1% dist at 1kHz	+12	+15		+12	+15		dB
S/N	Signal-to-noise ratio[2]	Record mode Playback mode	67 77	72 82		64 74	72 82		dB dB
	Record mode Frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	f = 1.4kHz 0dB -20dB -30dB	 -1 -16.6 -23.5	 0 -15.6 -22.5	 +1 -14.6 -21.5	 -1.5 -17.1 -24.0	 0 -15.6 -22.5	 +1.5 -14.1 -21.0	 dB dB dB
		f = 5kHz 0dB -20dB -30dB -40dB	 -0.7 -17.8 -22.8 -30.2	 +0.3 -16.8 -21.8 -29.7	 +1.3 -15.8 -20.8 -28.7	 -1.2 -18.3 -23.3 -30.2	 +0.3 -16.8 -21.8 -29.7	 +1.8 -15.3 -20.3 -28.2	 dB dB dB dB
		f = 20kHz 0dB -20dB -30dB	 -0.3 -18.3 -24.5	 +0.7 -17.3 -23.5	 +1.7 -16.3 -22.5	 -0.8 -18.8 -25.0	 +0.7 -17.3 -23.5	 +2.2 -15.8 -22.0	 dB dB dB
	Back-to-back frequency response	Using typical record mode .5 frequency response test points	-1	0	+1	-1.5	0	+1.5	dB
R_{IN}	Input resistance	Pin 5 Pin 2	35 3.1	50 4.2	65 5.3	35 3.1	50 4.2	65 5.3	kΩ kΩ
R_{OUT}	Output resistance	Pin 6 Pin 3 Pin 7	1.9	2.4 80 80	3.1 120 120	1.9	2.4 80 80	3.1 120 120	kΩ Ω Ω
	Back-to-back frequency response shift vs temperature vs supply voltage	 0°C to +70°C 8-20V		 ±0.4 ±0.4			 ±0.4 ±0.4		 dB dB

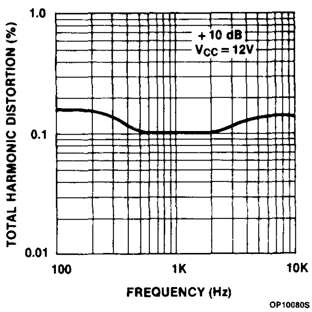
NOTES:
1. See maximum signal handling versus supply voltage characteristics.
2. All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

TYPICAL PERFORMANCE CHARACTERISTICS

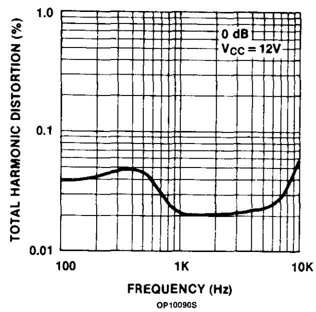
THD vs Frequency Record Mode



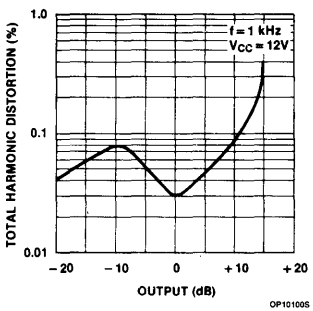
THD vs Frequency Record Mode



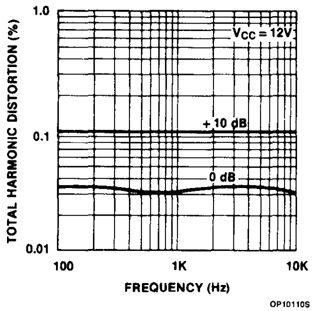
THD vs Frequency Play Mode



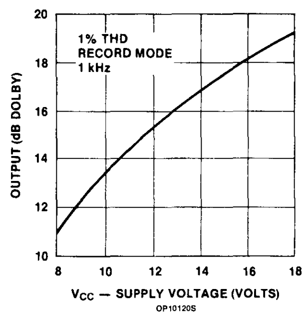
THD vs Output Record Mode



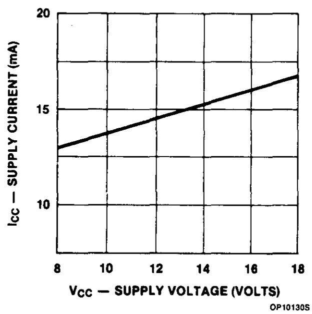
THD vs Frequency
Noise Reduction (NR) Off



Maximum Signal Handling
vs Supply Voltage



Supply Current vs
Supply Voltage



APPLICATION INFORMATION

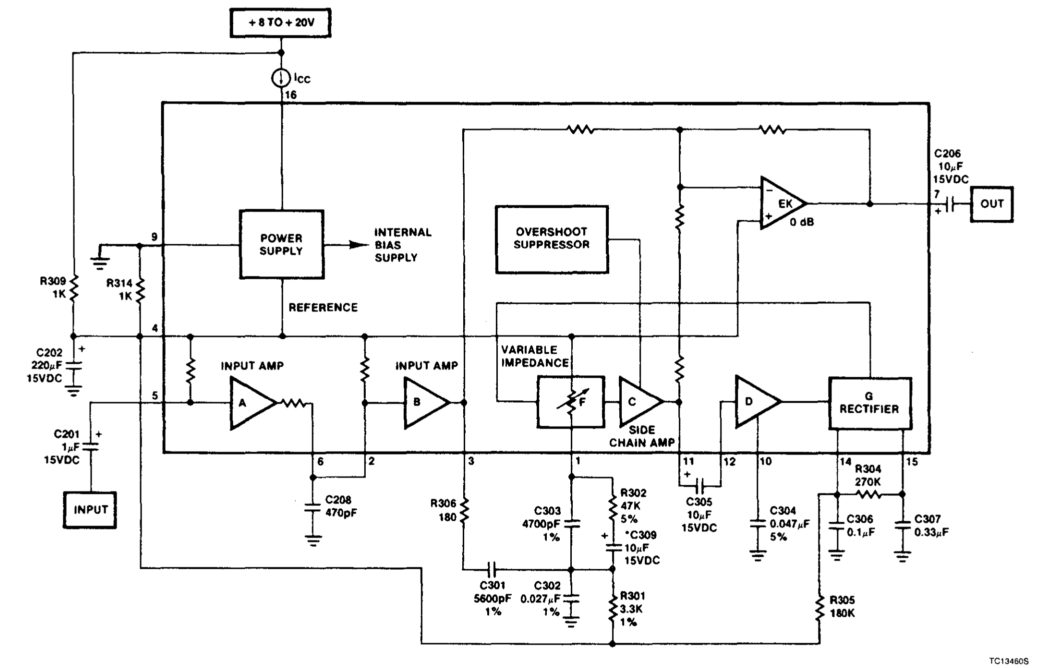
The NE645/646 is a direct replacement for the NE645B/646B. The NE645/646 incorporates improved design techniques to insure excellent performance required in Dolby B and C Type Audio Noise Reduction Systems. Critical component values are unchanged except for C309 on Pin 1 which is now an optional component in specific applications defined by Dolby Laboratories. All circuit parameters are guaranteed at 12V V_{CC}.

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT



NOTE:
All resistors standard and are measured in Ω. *Optional capacitor in specific applications defined by Dolby Laboratories.

Signetics

Linear Products

NE649
Low Voltage Dolby Noise Reduction Circuit

Product Specification

DESCRIPTION

The NE649 is an audio noise reduction circuit designed for use in low voltage entertainment systems. The circuit is used to reduce the level of background noise introduced during the recording and playback of audio signals on magnetic tape and improve the noise level in FM broadcast reception. The circuit is intended for use in automotive and portable cassette Dolby™ B-Type noise reduction systems. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

Dolby is a trademark of Dolby Laboratories Licensing Corporation

FEATURE

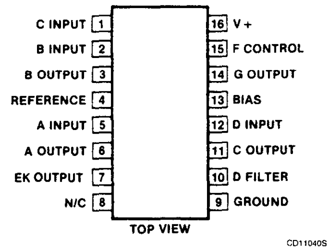
- **Low voltage operation**

APPLICATION

- **Tape decks**

PIN CONFIGURATION

N Package



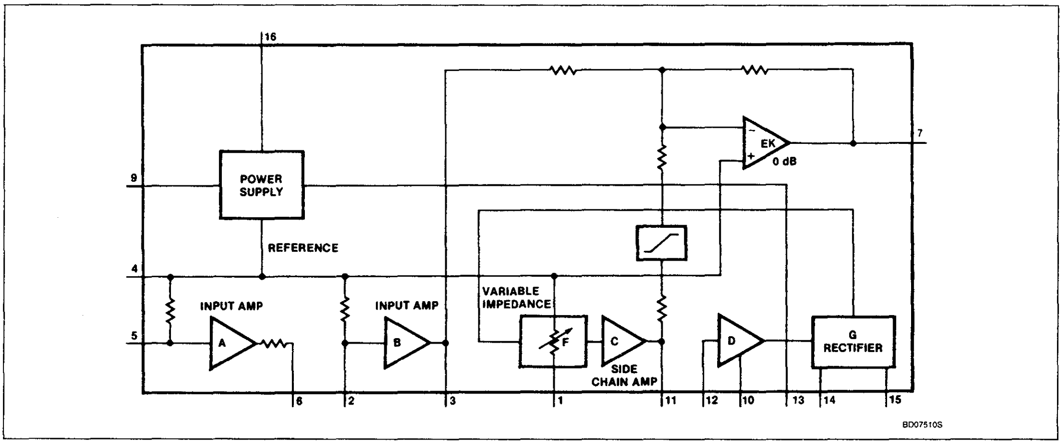
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE649N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	16	V
T_A	Operating temperature range	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	+300	°C

BLOCK DIAGRAM



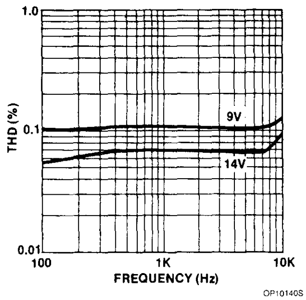
DC ELECTRICAL CHARACTERISTICS V_{CC} = 9V, f = 20Hz to 20kHz. All levels referenced to 580mV$_{RMS}$ (0dB) at Pin 3, T_A = +25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE649			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range[3]		6	9	14	V
	Minimum voltage supply for 8dB headroom 10dB headroom	 f = 1.4kHz THD < 1%	 6.5 7.5			 V V
I_{CC}	Supply Current			11	18	mA
I_{CC}	Supply Current[1]				20	mA
A_V	Voltage gain (Pins 5 - 3)	f = 1kHz (Pins 6 and 2 connected)	24.5	26	27.5	dB
A_V	Voltage gain (Pins 3 - 7)	f = 1kHz, 0dB at Pin 3, noise reduction out	-0.5	0	+0.5	dB
	Distortion	f = 20kHz to 10kHz, 0dB f = 20Hz to 10kHz, +10dB		0.05 0.2	0.2 0.5	% %
	Signal Handling (See Performance Characteristics)					
S/N	Signal-to-noise ratio[2]	Record (Pins 6 and 2 connected) Playback (Pins 6 and 2 connected)	64 74	72 82		dB dB
	Record mode frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	!f = 1.4kHz 0dB -20dB -30dB	 -1.5 -17.1 -24.0	 0 -15.6 -22.5	 +1.5 -14.1 -21.0	 dB dB dB
		f = 5kHz 0dB -20dB -30dB -40dB	 -1.2 -18.3 -23.3 -30.2	 +0.3 -16.8 -21.8 -29.7	 +1.8 -15.3 -20.3 -28.2	 dB dB dB dB
		f = 20kHz 0dB -20dB -30dB	 -0.8 -18.8 -25.0	 +0.7 -17.3 -23.5	 +2.2 -15.8 -22.0	 dB dB dB
	Back-to-back frequency response	Using typical record mode response		±1.5		db
R_{IN}	Input resistance	Pin 5 Pin 2	35 3.1	50 4.2	65 5.3	kΩ kΩ
R_{OUT}	Output resistance	Pin 6 Pin 3 Pin 7	1.9	2.4 80 80	3.1 120 120	kΩ Ω Ω
	Record mode frequency response shift vs temperature vs V_{CC}	 0 to 70°C -40 to 85°C 6 to 14V				 dB dB dB/V

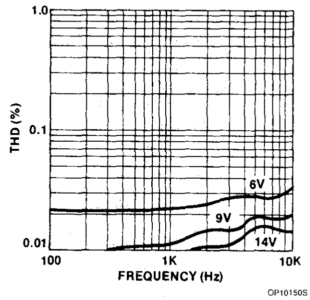
NOTES:
1. With electronic switching.
2. All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level. See Dolby Laboratories Bulletin 19.
3. The circuit will function as low as V_{CC} = 4.5V (i.e., output signal present). See graphs of I_{CC} and signal handling vs V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

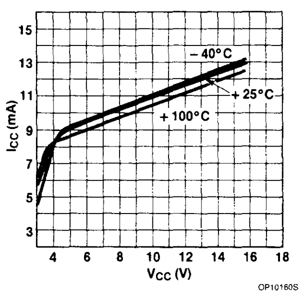
(+10dB) THD vs Frequency



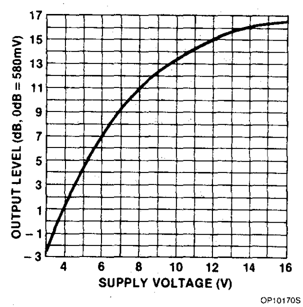
(0dB) THD vs Frequency



Current vs Supply Voltage



Maximum Signal Handling vs Supply Voltage for 1%THD (Record)



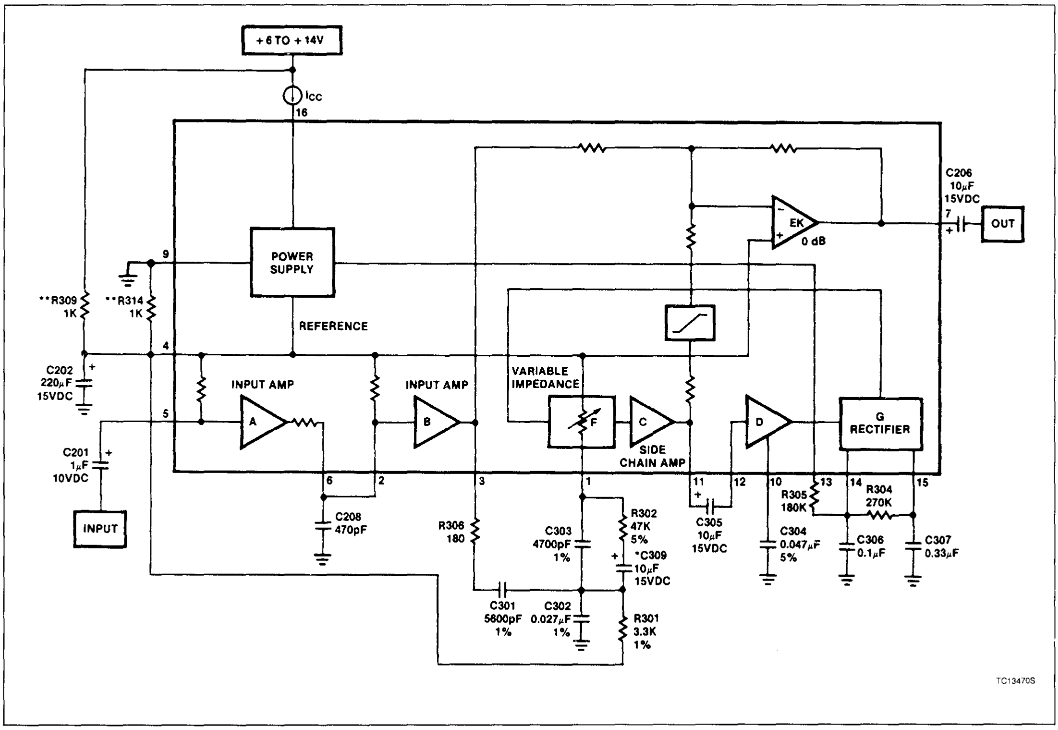
Low Voltage Dolby Noise Reduction Circuit NE649

DOLBY ENCODER Output for constant level input (single tone frequency response)

FREQUENCY (kHz)	INPUT LEVEL (dB) 0 (DOLBY LEVEL)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerance which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT



NE650
Dolby B-Type Noise Reduction Circuit

Product Specification

DESCRIPTION

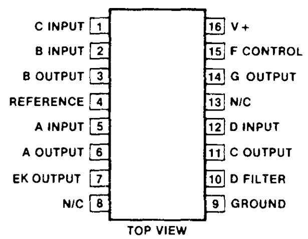
The NE650 is a monolithic audio noise reduction circuit designed for use in Dolby™ B-Type noise reduction systems. The NE650 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape.

The NE650 features excellent dynamic characteristics over a wide range of operating conditions and is pin-compatible with NE645/646. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

Dolby is a trademark of Dolby Laboratories Licensing Corporation.

PIN CONFIGURATION

N Package



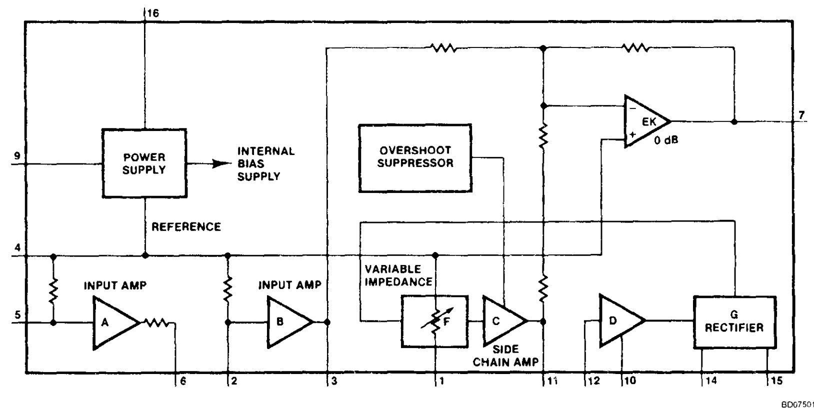
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE650N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	24	V
	Temperature range		
T_A	Operating ambient	0 to +70	°C
T_{STG}	Storage	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

BLOCK DIAGRAM



Dolby B-Type Noise Reduction Circuit

NE650

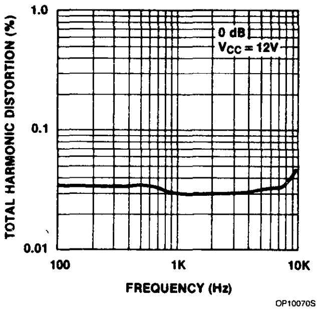
DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V, f = 20Hz to 20kHz. All levels referenced to 580mV$_{RMS}$(0db) at Pin 3, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	NE650			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		8		20	V
I_{CC}	Supply current	Electronic switching on		16	24	mA
A_V	Voltage gain (Pins 5 – 3)	f = 1kHz (Pins 6 and 2 connected)	25.5	26	26.5	dB
A_V	Voltage gain (Pins 3 – 7)	f = kHz, 0dB at Pin 3, noise reduction out	−0.5	0	+0.5	dB
A_V	Voltage gain (Pins 2 – 3)	f = 1kHz		13		dB
	Distortion THD: 2nd and 3rd harmonic	f=20Hz to 10kHz, 0dB f=20Hz to 10kHz, +10dB		0.05 0.15	0.1 0.3	% %
	Signal handling	1% distortion at 1kHz	+12	+15		dB
S/N	Signal-to-noise ratio*	Record mode Playback mode	68 78	72 82		dB dB
	Back-to-back frequency response	Using typical record mode response		±0.5		dB
	Record mode frequency response (at Pin 7) referenced to encode monitor point (Pin 3)	f = 1.4kHz 0dB −20dB −30dB	 −0.5 −16.1 −23.5	 0 −15.6 −22.5	 +0.5 −15.1 −21.5	 dB dB dB
		f = 5kHz 0dB −20dB −30dB −40dB	 −0.7 −17.3 −22.3 −30.2	 +0.3 −16.8 −21.8 −29.7	 +1.3 −16.3 −21.3 −29.2	 dB dB dB dB
		f = 20kHz 0dB −20dB −30dB	 −0.3 −18.3 −24.5	 +0.7 −17.3 −23.5	 +1.7 −16.3 −22.5	 dB dB dB
R_{IN}	Input resistance	Pin 5 Pin 2	35 3.1	50 4.2	65 5.3	kΩ kΩ
R_{OUT}	Output resistance	Pin 6 Pin 3 Pin 7	1.9	2.4 80 80	3.1 120 120	kΩ Ω Ω
	Back-to-back frequency response shift vs T_A vs V_{CC}	 0°C to −70°C 8 to 20V		 ±0.4 ±0.4		 dB dB

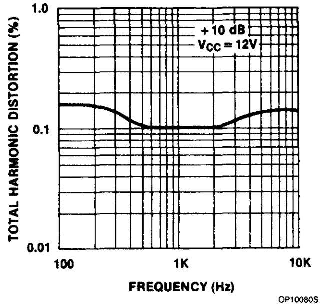
NOTE:
*All noise levels are measured CCIR/ARM weighted using a 10k source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

PERFORMANCE CHARACTERISTICS

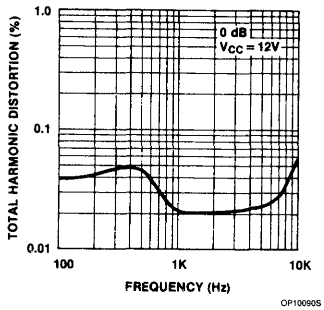
THD vs Frequency Record Mode



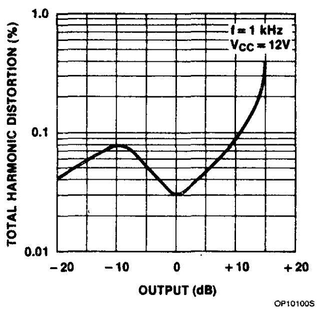
THD vs Frequency Record Mode



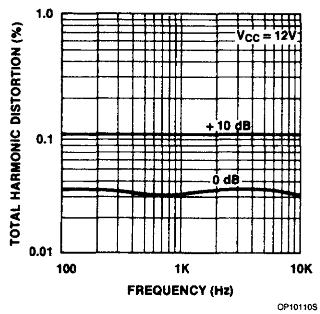
THD vs Frequency Play Mode



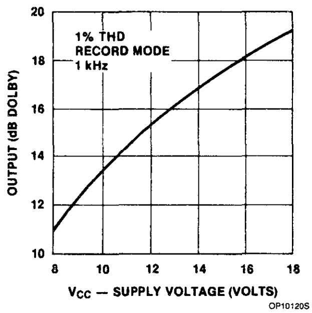
THD vs Output Record Mode



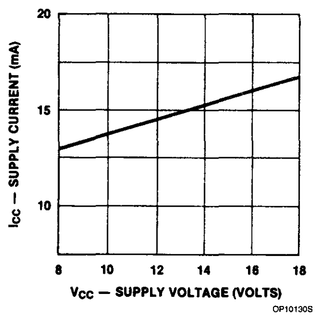
THD vs Frequency Noise Reduction (NR) Off



Maximum Signal Handling vs Supply Voltage



Supply Current vs Supply Voltage



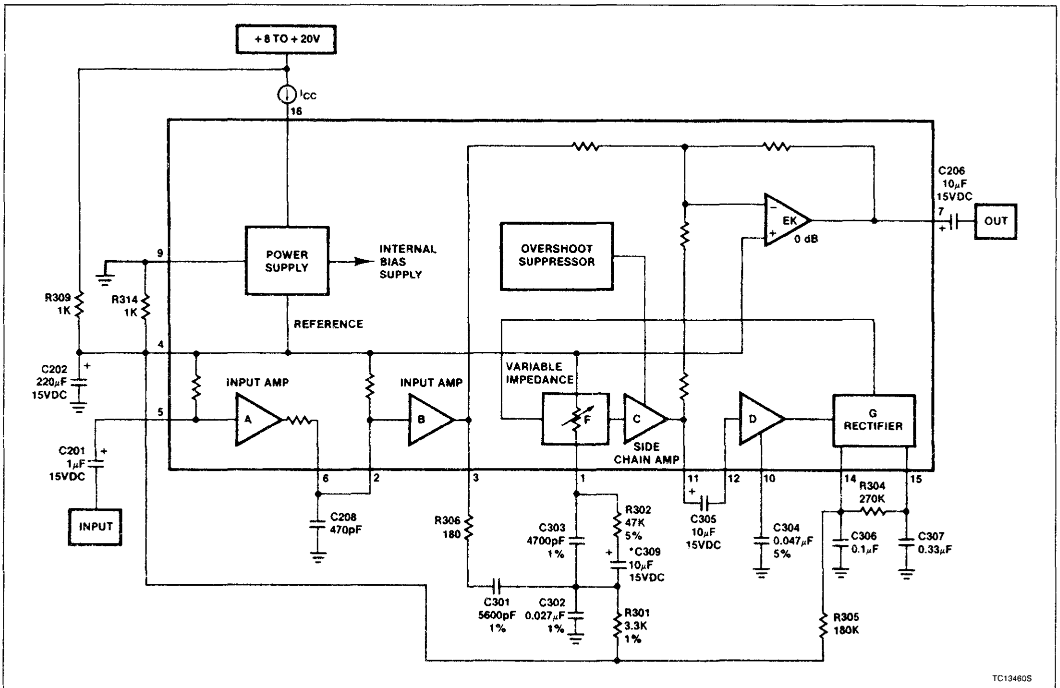
DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	−5	−10	−15	−20	−25	−30	−35	−40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE:
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerance which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

Dolby B-Type Noise Reduction Circuit NE650

TEST CIRCUIT



NOTES:
All resistors standard and are measured in Ω.
*Optional capacitor in specific applications defined by Dolby Laboratories.

LOW COST SPEECH DEMONSTRATION BOARD

GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single + 5 V supply
- Low cost

APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

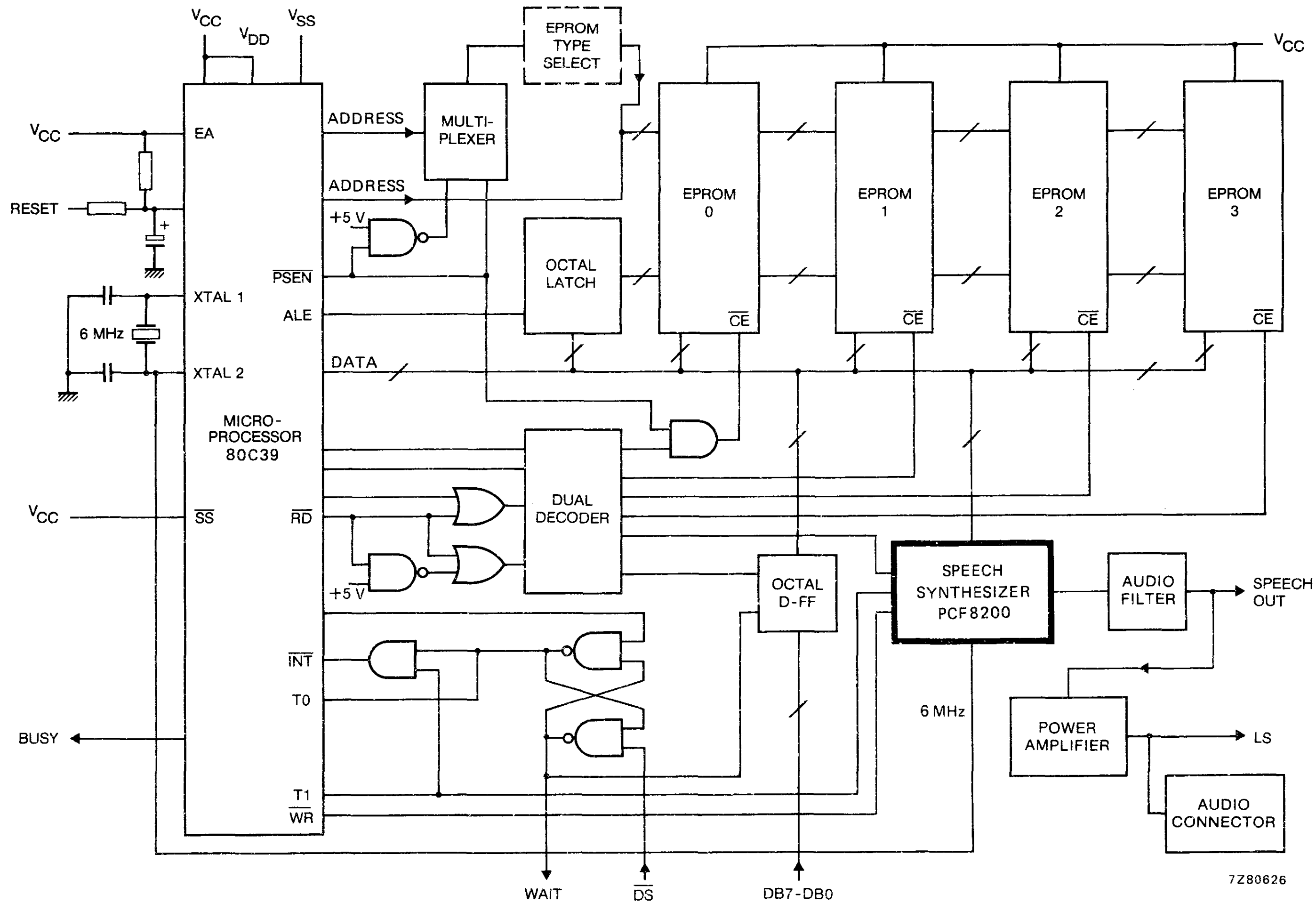


Fig. 1 Block diagram.

OPERATION

HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing. The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.

SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

– Male speech in several languages
– Female speech in several languages
– Programmable speaking speed

ORDERING INFORMATION

Product name: Low Cost Speech Demonstration Board

Type number: OM8200

Ordering code: 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

SPEECH DEMONSTRATION BOX

GENERAL DESCRIPTION

Speech demonstration box OM8201 is designed to be used in conjunction with the low cost speech demonstration board OM8200. The box contains all the necessary components to drive the board. The combination of these two components make an extremely attractive demonstration unit.

FEATURES

- Low cost
- Can use unmodified OM8200 board which allows access to all features of the OM8200
- Single + 9 V supply
  - Low power consumption therefore permits battery operation
  - External power supplies may also be used
  - Voltage is regulated and dropped to a standard + 5 V for the OM8200 board
- Simple mechanical construction
  - Allows easy access to the OM8200 for changing EPROMS
- Contains all peripherals needed to drive the OM8200

HARDWARE DESCRIPTION

The box contains a set of eight keypad switches which are connected to the data bus. Four switches can select which EPROM your speech data is derived from. Repeated pressing of an EPROM switch increments the expression number which will be uttered. To repeat the last expression, a separate switch must be activated.

It is possible in the PCF8200 to change the rate of speaking to 73%, 123% or 145% of the normal speed. A switch has been included on the box which will sequence through the speed options making the same utterance every time.

One of the two remaining switches is the master reset for the program and the other is for future enhancements of the box.

Included in the box are, the volume control for the amplifier, the loudspeaker, and a high impedance audio output.

The final piece of electronics is the power supply. This can be supplied from a + 9 V internal battery or from a + 9 V external supply. The + 9 V is regulated to a + 5 V supply which is then fed to other parts of the box and to the OM8200.

The box is of simple construction and allows easy access to the OM8200 for changing of EPROMS.

SOFTWARE DESCRIPTION

There is no software in the OM8201. The software of the OM8200 may be used in an unmodified form without any problems. However, if changes have been made to the control program of the OM8200 then different functions for the switches of the box can be achieved.

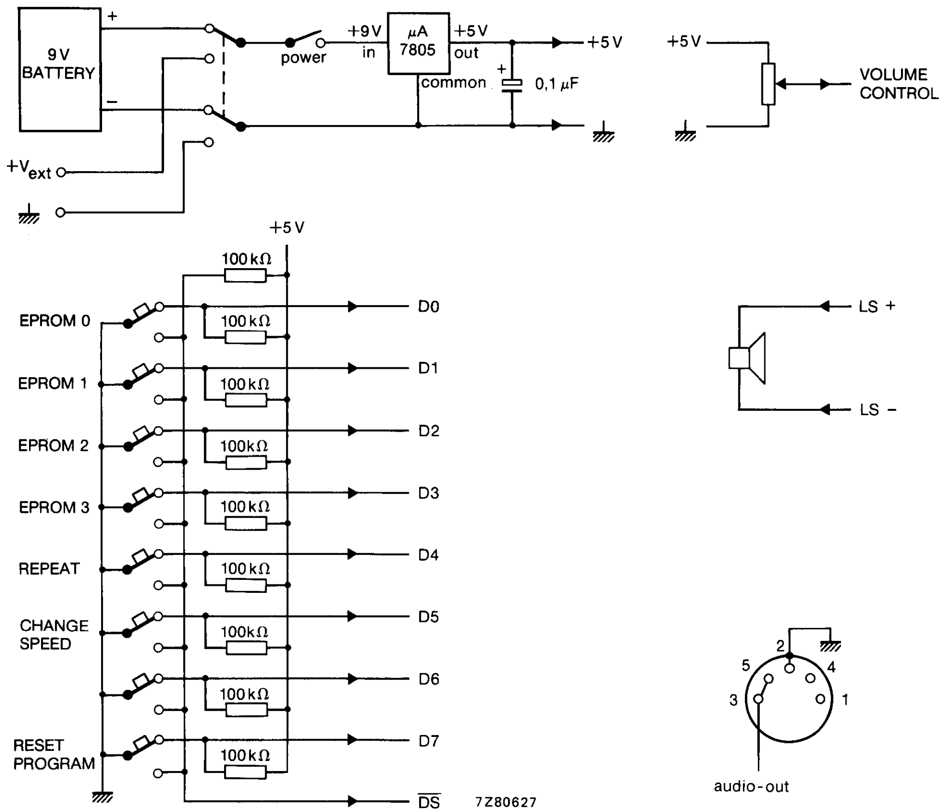


Fig. 1 Schematic diagram.

ORDERING INFORMATION

Product name: Speech Demonstration Box

Type number: OM8201

Ordering code: 9337 541 40000

N.B. OM8200 must be ordered as well if this box is to be used in demonstration mode.
The order number for the OM8200 is 9337 541 30000.

Orders should be placed with your local Philips/Signetics agent.

UPDATE PACKAGE FOR EXISTING OM8010 SPEECH EDITING SYSTEM

GENERAL DESCRIPTION

This package, OM8209, is an updating package which allows the users of our already existing editing system for the MEA8000 also to generate the parameters and codes necessary for our new CMOS voice synthesizer, PCF8200.

FEATURES

- Hardware updates for the synthesizer board to permit output via the PCF8200 and the MEA8000
- Software update to generate parameters and codes for the PCF8200
- Gives all the features of the OM8210 to those who have the OM8010 (used for generating first generation synthesizer codes)

Hardware

The only hardware changes are to the synthesizer card. This card is completely replaced by a new synthesizer card. This card contains the new PCF8200 voice synthesizer, the MEA8000 voice synthesizer and the necessary components required to interface the synthesizers to their environment.

Software

The software package is exactly the same as in the OM8210, for fuller information consult the data for that device.

ORDERING INFORMATION

Product name: Update package for existing OM8010 Speech Editing System using the HP9816S

Type number: OM8209

Ordering number: 9337 564 50000

Orders should be placed with your local Philips/Signetics agent.

SPEECH ANALYSIS/EDITING SYSTEM

GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses either the HP9816S or IBM-PC personal computer.
The OM8210 and the computer function together to produce speech coding for the PCF8200.
The system has many commands available, mostly single key operations, which gives it flexability.

FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

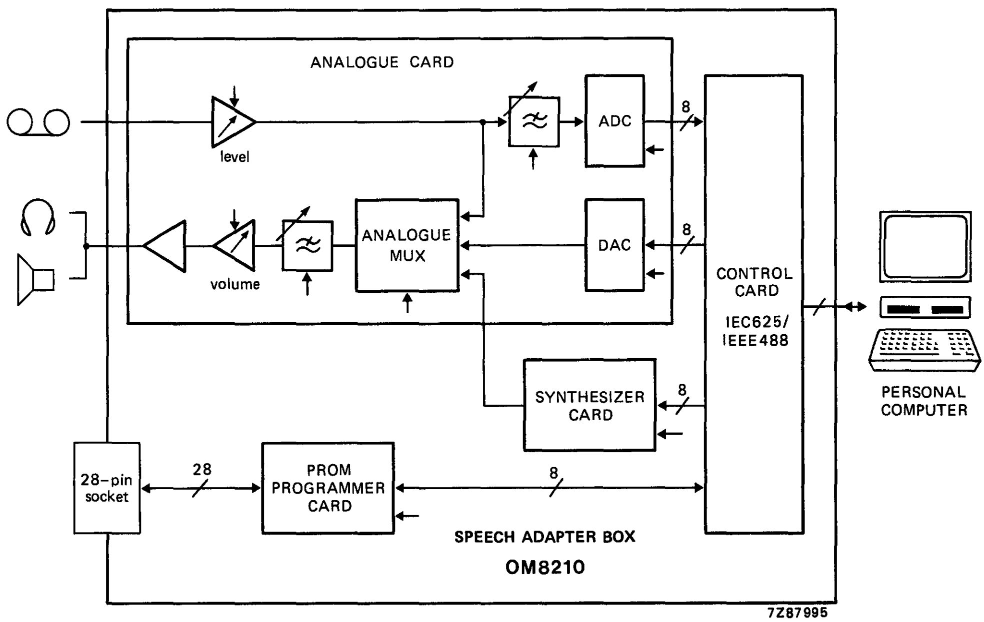


Fig. 1 Block diagram.

HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

Sample Mode	Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible.
Analysis Mode	Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters.
Parameter Edit Mode	Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration.
Code Mode	Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM.
EPROM Mode	Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands.
File Mode	Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library.
Media Mode	For diskette initialization and making back-up copies.
Option Mode	Allows the system configuration to be read or changed.

The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete Hewlett Packard based editing system:
- HP9816S-630 (optimum computer type) or HP9817
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 K bytes total required)

The following equipment is required to make a complete IBM based editing system:
- IBM-PC or PC-XT or Philips P3100
- Additional memory (512 K recommended)
- Display graphics card (Hercules monochrome)
- IEEE488 card (Tecmar Rev. D.)

ORDERING INFORMATION

Product name:	Speech Analysis/Editing System
Type number:	OM8210
Ordering code:	9337 561 50112

The computer system should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCB80C51 family of single-chip 8-bit microcontrollers is manufactured in an advanced CMOS process. The family consists of the following members:

- PCB80C51BH-3: 4 K bytes mask-programmable ROM, 128 bytes RAM
- PCB80C31BH-3: ROM-less version of the PCB80C51BH-3

In the following text, the generic term "PCB80C51BH-3" is used to refer to both family members.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 K bytes of program memory and/or up to 64 K bytes of data memory.

The PCB80C51BH-3 contains a non-volatile 4 K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/event counters; a five-source, two-priority level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB80C51BH-3 can be expanded using standard TTL compatible memories and logic.

The PCB80C51BH-3 has two software selectable modes of reduced activity for further power reduction - Idle and Power-down.

The Idle mode freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning.

The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

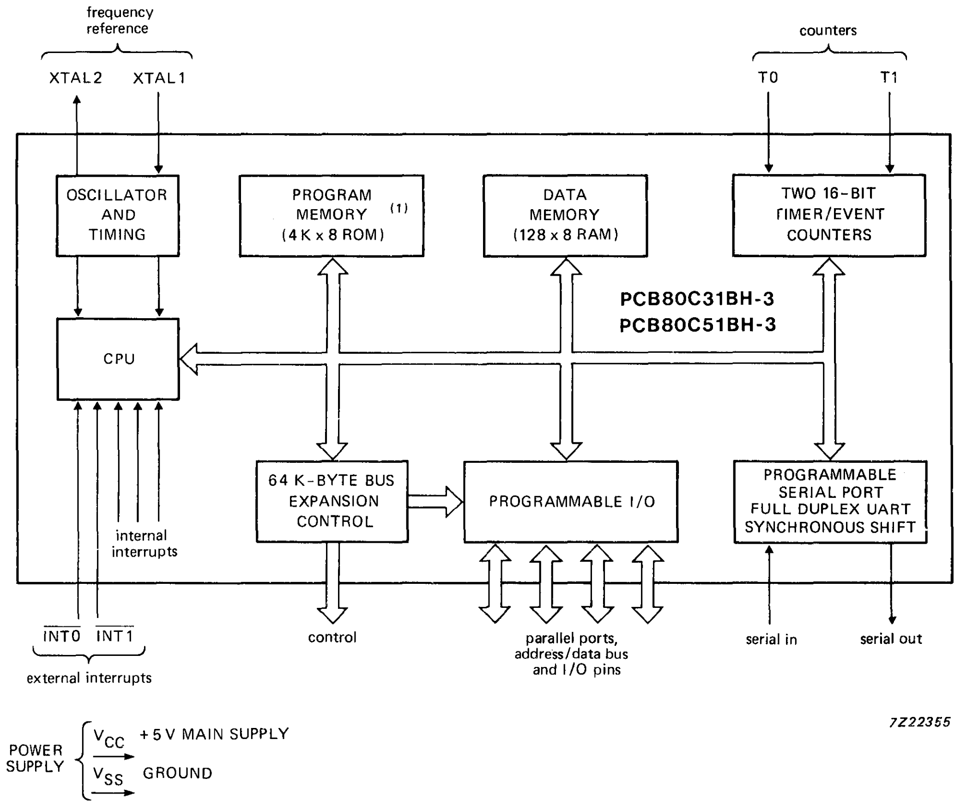
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs. Multiply, divide, subtract and compare are among the many instructions included in the instruction set.

Features

- 4 K x 8 ROM (80C51BH-3 only), 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- External memory expandable to 128 K, external ROM up to 64 K and/or external RAM up to 64 K
- Boolean processing
- 218 bit-addressable locations
- On-chip oscillator
- Five-source interrupt structure with two priority levels
- With a 12 MHz clock, 58% of the instructions execute in 1 μs; multiply and divide instructions execute in 4 μs; all other instructions execute in 2 μs
- Enhanced architecture with:
  non-page-oriented-instructions
  direct addressing
  four 8-byte + 1-byte register blanks
  stack depth up to 128-bytes
  multiply, divide, subtract and compare instructions
- PCB80C51/C31BH-3
  XTAL frequency range: 1,2 to 16 MHz
  temperature range: 0 °C to + 70 °C
  PCF80C51/C31BH-3
  XTAL frequency range: 1,2 to 12 MHz
  temperature range: –40 °C to + 85 °C
  PCA80C51/C31BH-3
  XTAL frequency range: 1,2 to 12 MHz
  temperature range: –40 °C to +125 °C

PACKAGE OUTLINES

PCB/PCF80C51/C31BH-3P, PCA80C51/C31BH-3P: 40 lead DIL; plastic (SOT129).
PCB/PCF80C51/C31BH-3WP, PCA80C51/C31BH-3WP: 44-lead PLCC; plastic leaded chip-carrier (SOT187 pedestal or SOT187AA pocket version depending on source, versions are interchangeable.



(1) PCB80C51BH-3 only.

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:
- The PCB80C49 with resident mask programmed 2 K x 8 ROM, 128 x 8 RAM.
- The PCB80C39 without resident program memory for use with external EPROM/ROM, 128 x 8 RAM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O, and to test individual individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.
An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power down mode is provided.
For further detailed information see users manual 'single-chip 8-bit microcontrollers'.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption
- Available with extended temperature ranges: (PCB version) 0 to + 70 ^{o}C
  (PCF version) −40 to + 85 ^{o}C
  (PCA version) −40 to + 110 ^{o}C
- Frequency range: 1 to 15 MHz for all temperature ranges

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB/F/A80C39/C49P: 40-lead DIL; plastic (SOT129).
PCB/F/A80C39/C49WP: 44-lead PLCC; plastic leaded chip carrier, 'pocket' version (SOT187AA); 'pedestal' version (SOT187). These versions are interchangeable.

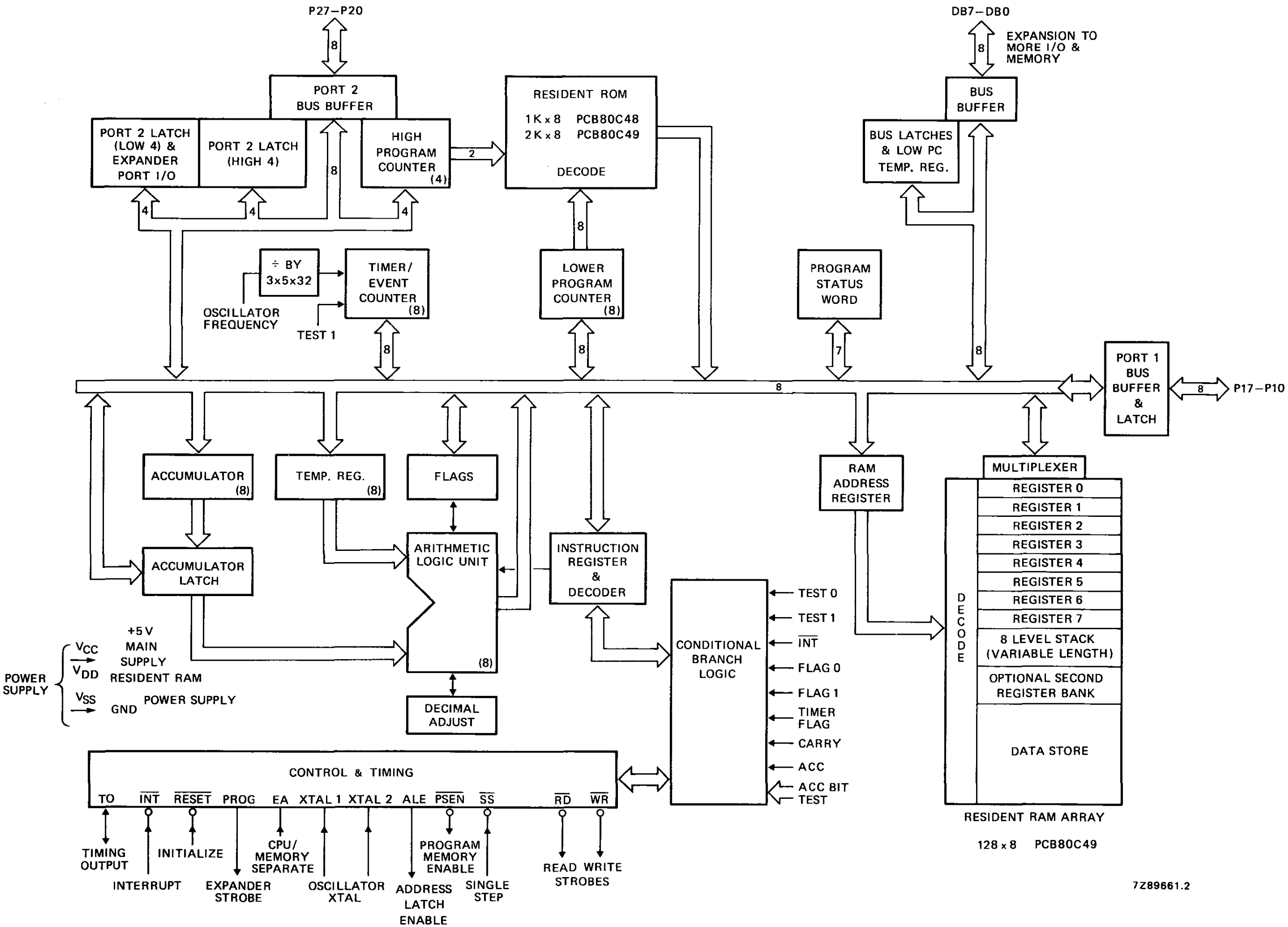


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552" is used to refer to both family members:

- PCB83C552: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C552: ROM-less version of the PCB83C552

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552 can be expanded using standard TTL compatible memories and logic.

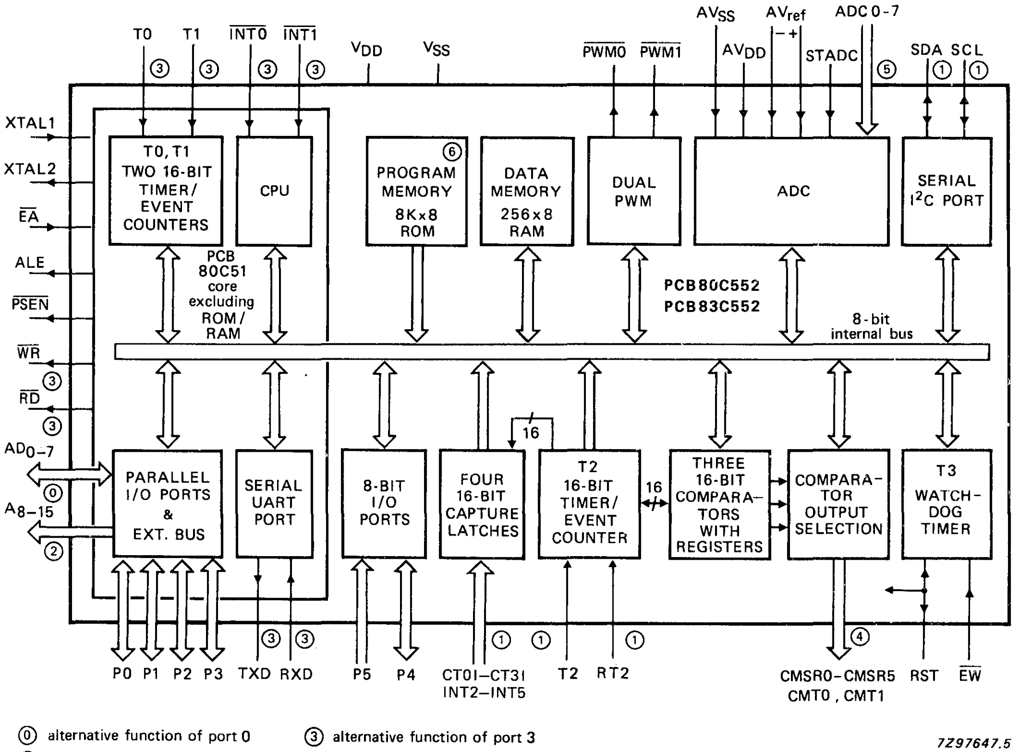
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analogue inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer
- PCB80C552/83C552
  XTAL frequency range: 1.2 to 12 MHz
  temperature range: 0 °C to +70 °C
  PCF80C552/83C552
  XTAL frequency range: 1.2 to 12 MHz
  temperature range: −40 °C to +85 °C
  PCA80C552/83C552
  XTAL frequency range: 1.2 to 12 MHz
  temperature range: −40 °C to +125 °C

PACKAGE OUTLINES

PCA/PCB/PCF/83C552/80C552WP
68-lead plastic leaded chip carrier (PLCC) 'pocket' version (SOT188AA)



(0) alternative function of port 0
(1) alternative functions of port 1
(2) alternative function of port 2
(3) alternative function of port 3
(4) alternative function of port 4
(5) alternative function of port 5
(6) not present in PCB80C552

POWER SUPPLY
- V_{DD} + 5 V MAIN SUPPLY
- V_{SS} GROUND

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATABOOK OR DATASHEET.

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C562 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. PCB83C562 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C562" is used to refer to both family members:

- PCB83C562: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C562: ROM-less version of the PCB83C562

The PCB83C562 contains a non-volatile 8 K x 8 read-only program memory (not ROM-less version), a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the PCB80C51), an additional 16-bit timer coupled to capture and compare latches; a fourteen source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC with pulse width modulated outputs, a UART serial interface, a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C562 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions; 44% one-byte, 41% two-byte and 15% three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

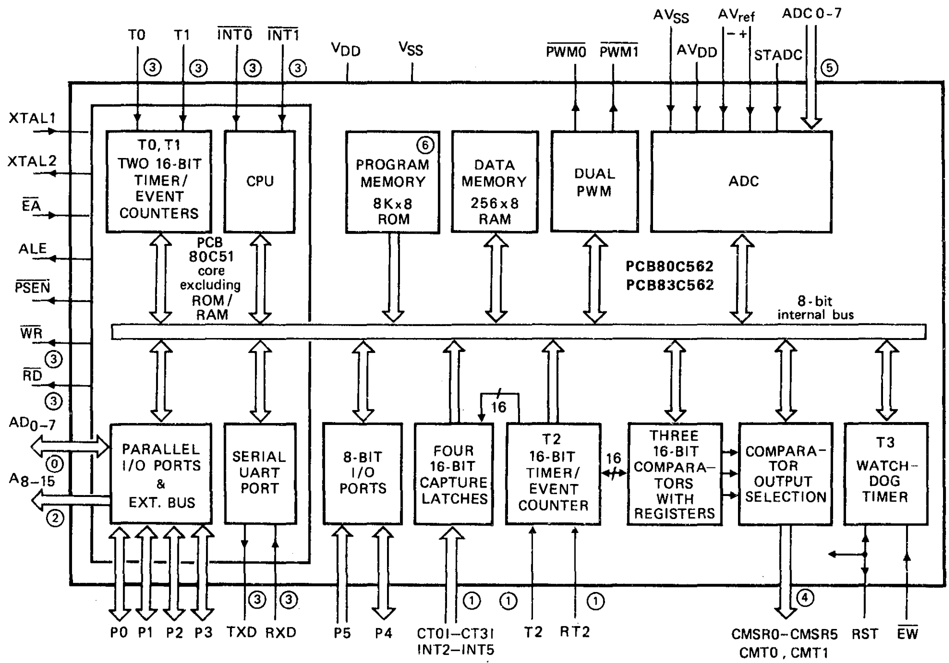
Features

- PCB80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K x 8 bytes
- 256 x 8 RAM, expandable externally to 64 K x 8 bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- An ADC with 8 multiplexed analogue inputs and 8-bit resolution
- Two 8-bit resolution, Pulse Width Modulated analogue outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer
- Operating ambient temperature range and XTAL frequency range:

  PCB83C562: 0 to + 70 °C; 1.2 MHz – 16 MHz
  PCF83C562: –40 to + 85 °C; 1.2 MHz – 12 MHz
  PCA83C562: –40 to + 125 °C; 1.2 MHz – 12 MHz

PACKAGE OUTLINE

PCB/PCF/PCA83C562: 68-lead PLCC; plastic 'pocket' version (SOT188AA).



(0) alternative function of port 0
(1) alternative functions of port 1
(2) alternative function of port 2
(3) alternative function of port 3
(4) alternative function of port 4
(5) alternative function of port 5
(6) not present in PCB80C552

POWER SUPPLY { V_{DD} + 5 V MAIN SUPPLY; V_{SS} GROUND }

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities
  Three temperature ranges available
  0 to + 70 °C; PCB83C652 versions
  –40 to + 85 °C; PCF83C652 versions
  –40 to + 125 °C; PCA83C652 versions
- Extended frequency range: 1.2 MHz to 12 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C652P; PCA/PCB/PCF80C652P: 40-lead DIL; plastic (SOT129).
PCA/PCB/PCF83C652WP; PCA/PCB/PCF80C652WP: 44-lead plastic leaded-chip-carrier (PLCC) (SOT187 pedestal or SOT187AA pocket versions, these are interchangeable).
PCA/PCB/PCF83C652H; PCA/PCB/PCF80C652H: 44-lead quad flat-pack (QFP). This is in preparation.

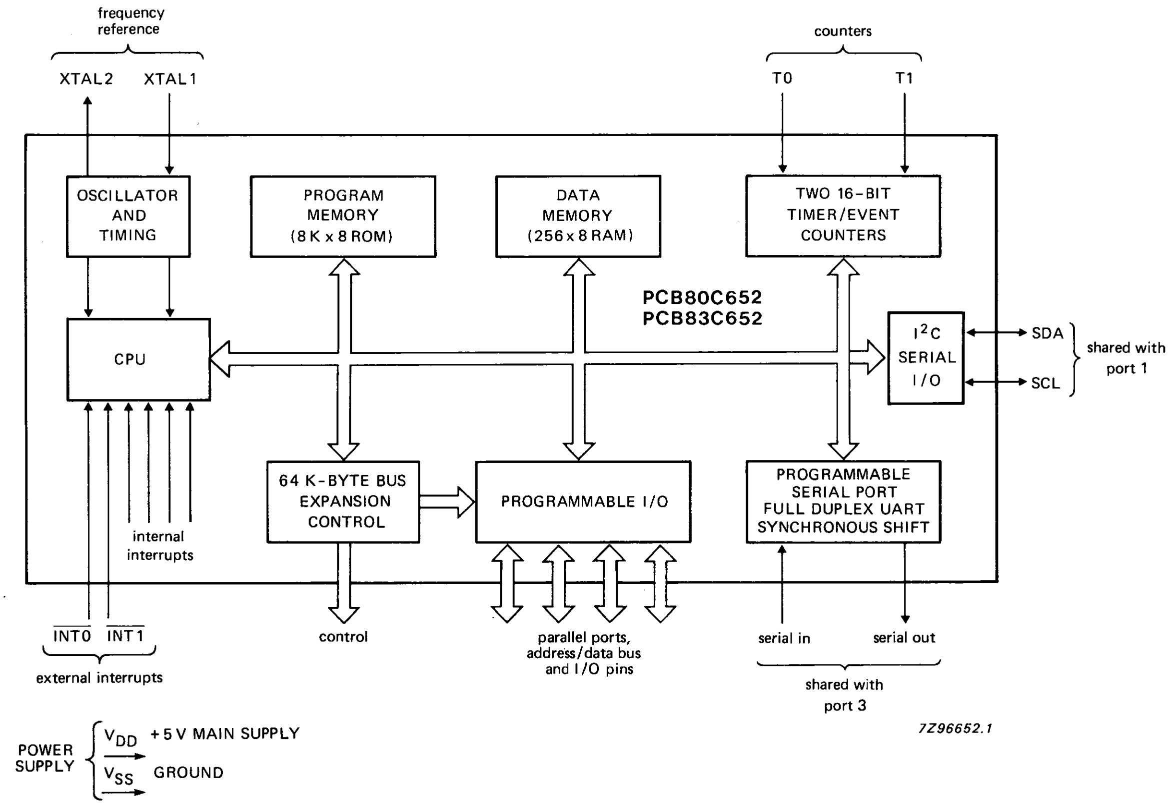


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C654 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C654 has the same instruction set as the PCB80C51. The ROM-less PCB80C652 should be used for development purposes.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C654 contains a non-volatile 16 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 16 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINES

PCB83C654P : 40-lead DIL; plastic (SOT129).
PCB83C654WP: 44-lead plastic leaded chip-carrier (PLCC); (SOT187 pedestal or SOT187AA pocket version depending on source, versions are interchangeable).
PCB83C654H : 44-lead quad flat-pack; plastic (SOT205A) in preparation.

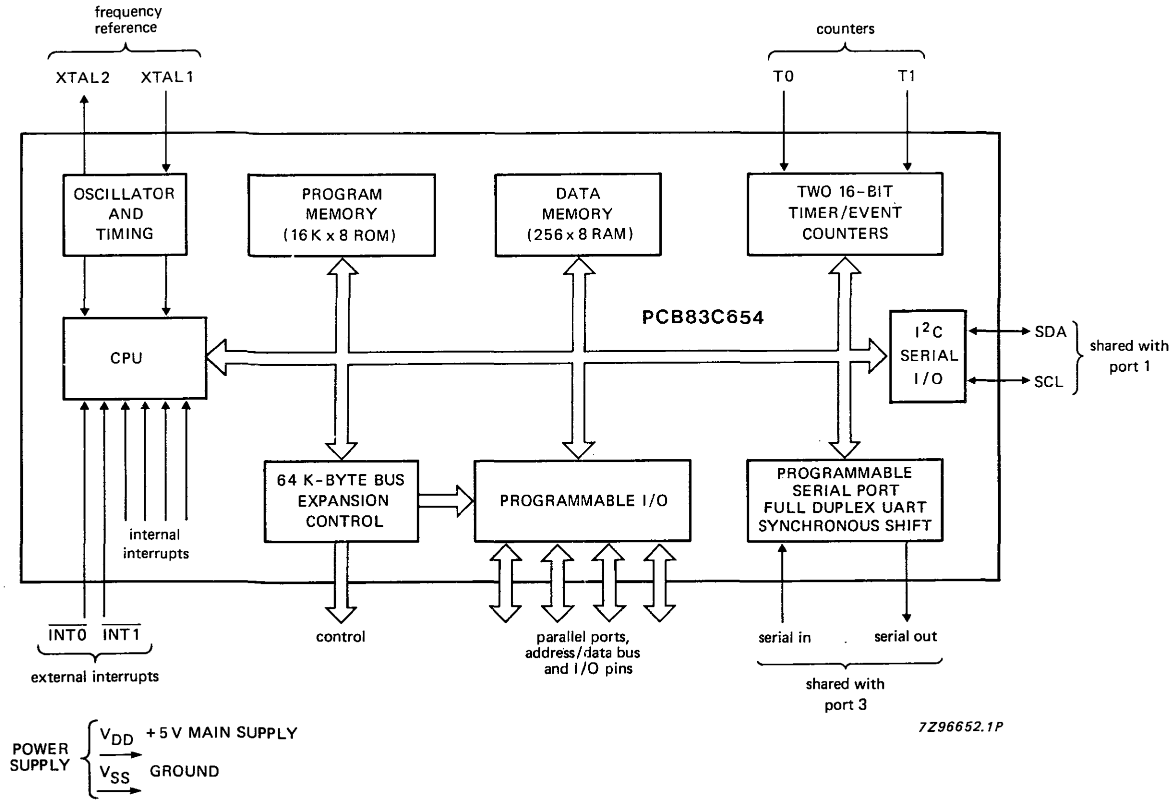


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATABOOK OR DATASHEET.

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C851 single chip microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C851 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term 'PCB83C851' is used to refer to both family members:

- PCB83C851: 4 K bytes mask-programmable ROM, 128 bytes RAM, 256 bytes EEPROM
- PCB80C851: ROM-less version of the PCB83C851

This device provides architectural enhancements that make it suitable for a variety of applications, specifically control systems.

The PCB83C851 contains a non-volatile 4 K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; a 256 byte electrically erasable programmable read only memory (EEPROM); 32 I/O lines; two 16-bit timer/event counters (identical to the timers of the PCB80C51); a seven source, five-vector, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART; and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C851 can be expanded using standard TTL compatible memories and logic.

The PCB83C851 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte and 16 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 µs and 40% in 2 µs. Multiply and divide instructions require 4 µs.

Features

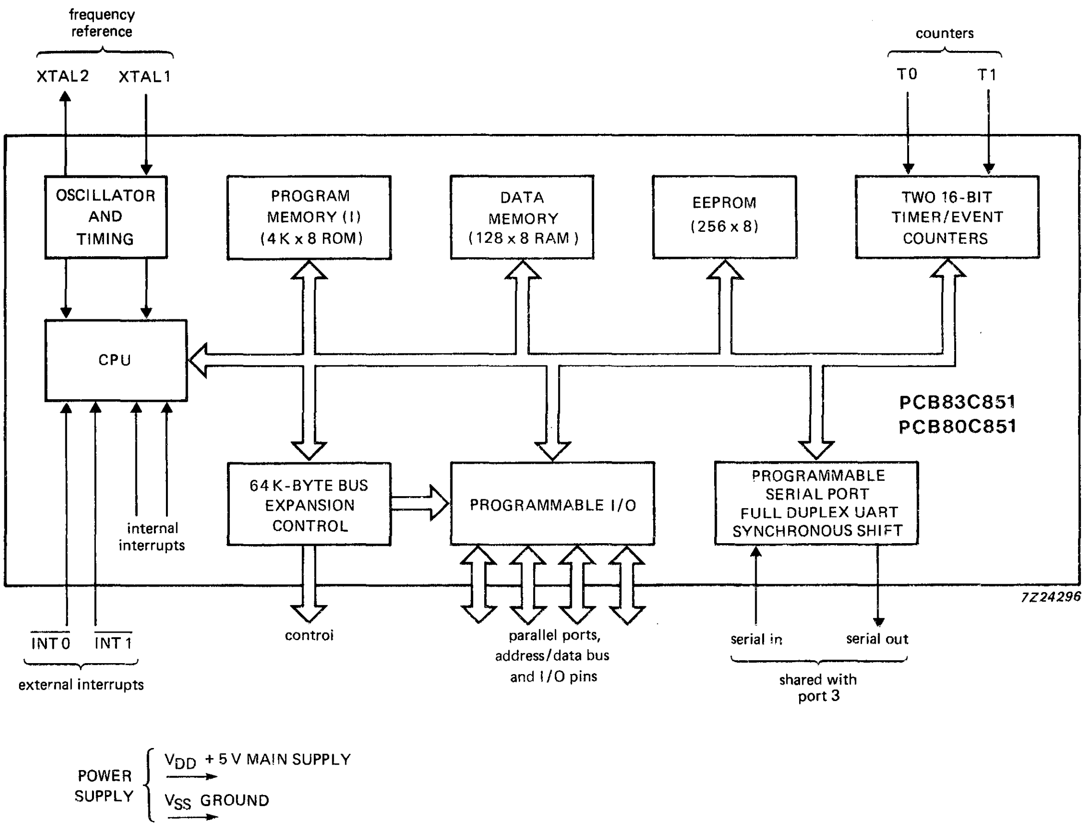
- PCB80C51 central processing unit
- 4 K x 8 ROM, expandable externally to 64 K bytes
- 128 x 8 RAM, expandable externally to 64 K bytes
- Four 8-bit I/O ports, 32 I/O lines
- Two 16-bit timer/event counters
- Full-duplex serial port
- Boolean processing
- On-chip oscillator
- Seven-source, five-vector interrupt structure with two priority levels
- 58% of the instructions are executed in 1 µs; multiply and divide in 4 µs; all others are executed in 2 µs (with a 12 MHz oscillator)
- Enhanced architecture with non-page-oriented-instructions, direct addressing, four 8-byte register banks, stack depth up to 128-bytes, multiply, divide, subtract and compare instructions
- ROM code protection (mask-programmable)
- Security mode, user dependent protection of the EEPROM contents
- Additional interrupt source (EEPROM) 'ORed' with serial interrupt

EEPROM:

- Non-volatile 256 x 8 bit EEPROM (electrically erasable programmable read only memory)
- On-chip voltage multiplier for erase/write
- 10000 erase/write cycles per byte
- 10 years non volatile data retention
- Infinite number of read cycles

PACKAGE OUTLINES

PCB/PCF83C851/80C851P: 40-lead DIL; plastic (SOT 129)
PCB/PCF83C851/80C851WP: 44-lead PLCC; plastic, leaded-chip-carrier (SOT187AA)



Note (1): PCB/PCF83C851 only

Fig. 1 Block diagram.

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_C) when in pointer or thermometer mode.

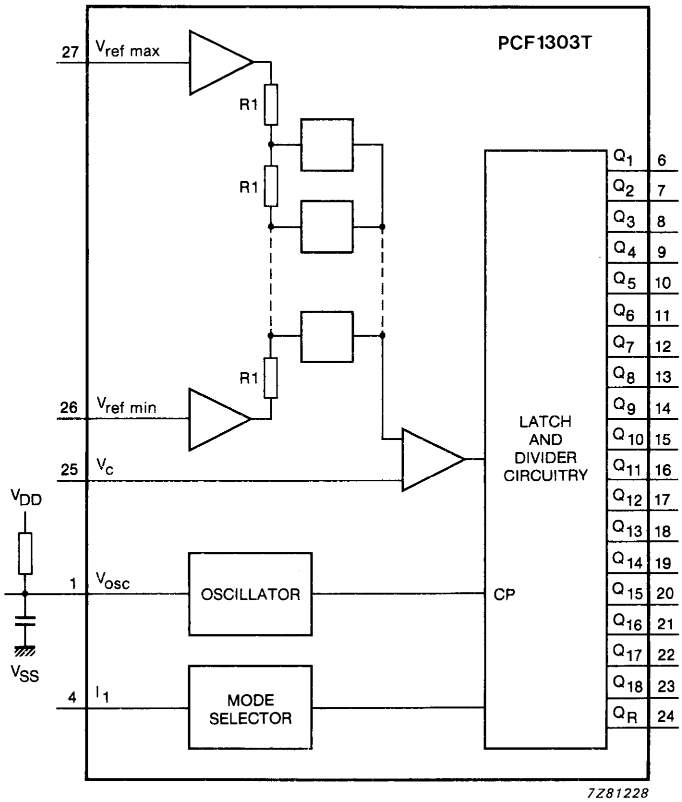
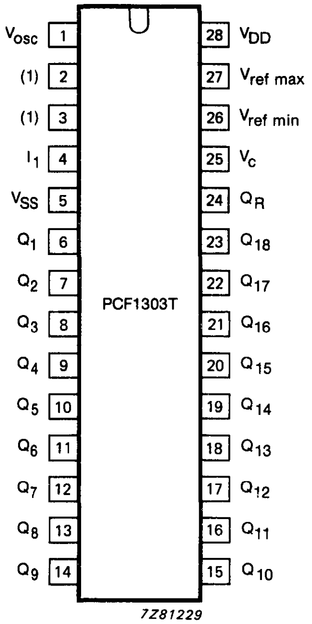


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).



(1) Pins 2 and 3 should be connected to V_{SS}.

Fig. 2 Pin configuration.

PIN DESCRIPTION

pin no.	symbol	name and function
1	V_{osc}	oscillator pin
4	I_1	mode select input
5	V_{SS}	ground (0 V)
6 to 23	Q_1 to Q_{18}	segment outputs
24	Q_R	back-plane output
25	V_c	control voltage
26 27	$V_{ref\ min}$ $V_{ref\ max}$	reference voltage inputs
28	V_{DD}	positive supply voltage

FUNCTION TABLE

I_1	mode
L	pointer
H	thermometer

H = HIGH voltage level
L = LOW voltage level

FUNCTIONAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to the control voltage when in pointer or thermometer mode.

The first segment will energize when the control voltage is less than the trigger voltage ($V_{T(bar)2}$ see equation [3]).

The circuit has analogue and digital sections.

The analogue section consists of a comparator with the inverting input coupled to the input control voltage. The non-inverting input of the comparator is connected via 17 analogue switches to the nodes of an 18-element resistor divider. The extremities of the resistor divider are coupled via high-input impedance amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The control input functions with Schmitt trigger action.

The digital section has one reference output (Q_R) to drive the back-plane and 18 outputs (Q_1 to Q_{18}) to drive the segments.

The segment outputs incorporate two latches and some gates.

The circuit is driven by an on-chip oscillator with external resistors and capacitors. The outputs are driven at typical 100 Hz.

LINEARITY

$$V_{step} = V_{step'} \pm \Delta V_{step} \qquad [1]$$

$V_{step'}$ is the voltage drop (internal) across the resistor-ladder network.
ΔV_{step} is the differential on V_{step}.

$$V_{step'} = \frac{(V_{ref\,max} \pm \Delta V_{2'}) - (V_{ref\,min} \pm \Delta V_2)}{18} \qquad [2]$$

ΔV_2 and $\Delta V_{2'}$ are the maximum offset voltage spread of the on-chip voltage followers.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_c pin is $V_{T(bar)n}$:

$$V_{T(bar)n} = (V_{ref\,min} \pm \Delta V_{2*}) + \{ (n-1)V_{step'} \pm \Delta V_R \} \pm \Delta V_1 \pm V_H \qquad [3]$$

n = number of segments; $2 \leqslant n \leqslant 18$.

ΔV_R is the voltage deviation at step n of the resistor-ladder network (for n = 2 or 18, $\Delta V_R = \Delta V_{step}$).

ΔV_1 is the offset voltage for the on-chip comparator.

V_H is the hysteresis voltage: 30% $V_{step} \geqslant V_H \geqslant$ 10% V_{step}.

* For ΔV_2 the same sign (+ or –) should be used as in equation [2].

RATINGS

Limiting values as in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	$-0{,}5$ to $+15$	V
Voltage on any input	V_I	$-0{,}5$ to $V_{DD} + 0{,}5$	V
D.C. current into any input or output	$\pm I_I$	max. 10	mA
Storage temperature range	T_{stg}	-25 to $+125$	^oC
Operating ambient temperature range	T_{amb}	-40 to $+85$	^oC

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

parameter	V_{DD} V	symbol	T_{amb} (^oC) −40 min.	−40 max.	+ 25 min.	+ 25 typ.	+ 25 max.	+ 85 min.	+ 85 max.	unit	notes
Quiescent device current	10,0	I_{DD}		1200			1200		1200	μA	1
Operating supply current	8,2	I_{DD}		2,0			2,0		2,0	mA	2
Input leakage current	6,0 8,2 10,0	$\pm I_I$ $\pm I_I$ $\pm I_I$		300 300 300			300 300 300		1000 1000 1000	nA nA nA	3
HIGH level input voltage select input I_1	6,0 8,2 10,0	V_{IH} V_{IH} V_{IH}	4,2 5,8 7,0		4,2 5,8 7,0			4,2 5,8 7,0		V V V	
LOW level input voltage select input I_1	6,0 8,2 10,0	V_{IL} V_{IL} V_{IL}		1,8 2,4 3,0	 2,4 		1,8 2,4 3,0		1,8 3,0	V V V	
HIGH level output voltage	6,0 8,2 10,0	V_{OH} V_{OH} V_{OH}	5,95 8,15 9,95		5,95 8,15 9,95			5,95 8,15 9,95		V V V	4
LOW level output voltage	6,0 8,2 10,0	V_{OL} V_{OL} V_{OL}		0,05 0,05 0,05			0,05 0,05 0,05		0,05 0,05 0,05	V V V	4
Output current HIGH	6,0 8,2 10,0	$-I_{OH}$ $-I_{OH}$ $-I_{OH}$	0,6 0,85 1,0		0,5 0,7 0,85			0,35 0,45 0,6		mA mA mA	5
Output current LOW	6,0 8,2 10,0	I_{OL} I_{OL} I_{OL}	0,65 1,0 1,3		0,5 0,8 1,0			0,4 0,6 0,8		mA mA mA	6

For notes see page 6.

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+ 25 min.	+ 25 typ.	+ 25 max.	+ 85 min.	+ 85 max.	unit	notes
Input voltage control input V_c	6,0 8,2 10,0	V_{IC} V_{IC} V_{IC}	0,0 0,0 0,0	6,0 8,2 10,0	0,0 0,0 0,0		6,0 8,2 10,0	0,0 0,0 0,0	6,0 8,2 10,0	V V V	
Input voltage $V_{ref\,max}$ input	6,0 8,2 10,0	$V_{IR\,max}$ $V_{IR\,max}$ $V_{IR\,max}$	3,6 3,6 3,6	5,5 7,7 9,5	3,6 3,6 3,6		5,5 7,7 9,5	3,6 3,6 3,6	5,5 7,7 9,5	V V V	
Input voltage $V_{ref\,min}$ input	6,0 8,2 10,0	$V_{IR\,min}$ $V_{IR\,min}$ $V_{IR\,min}$	0,5 0,5 0,5	1,0 4,5 6,0	0,5 0,5 0,5		1,0 4,5 6,0	0,5 0,5 0,5	1,0 4,5 6,0	V V V	
$V_{ref\,max}$ − $V_{ref\,min}$	6,0 8,2 10,0	ΔV_I ΔV_I ΔV_I	3,0 3,0 3,0		3,0 3,0 3,0			3,0 3,0 3,0		V V V	
DC component bar output to back-plane output	8,2	$\pm V_{BP}$		25		10	25		25	mV	7
Back-plane frequency	8,2	f_{BP}	90	110		100		90	110	Hz	8
Input offset voltage	8,2	$\pm V_{IO}$		120			120		120	mV	9
Step voltage variation	8,2	$\pm \Delta V_{step}$		50			50		50	mV	10
Input voltage slew rate V_c input	6,0 8,2 10,0	SR SR SR		50 50 50			50 50 50		50 50 50	V/s V/s V/s	11

For notes see next page.

Notes to D.C. characteristics

1. $V_{ref\,min} = 0,5$ V, $V_{ref\,max} = 9,5$ V, $V_c = V_{osc} = 0$ V, I_1 at V_{SS} or V_{DD}.
2. See Fig. 2.
3. Pin under test at V_{SS} or V_{DD}. All other inputs simultaneously at V_{SS} or V_{DD}.
4. $I_O = 0$, all inputs at V_{SS} or V_{DD}.
5. $V_{OH} = V_{DD} - 0,5$ V, all inputs at V_{SS} or V_{DD}.
6. $V_{OL} = 0,4$ V, all inputs at V_{SS} or V_{DD}.
7. $f_{BP} = 100$ Hz, load segment outputs to back-plane output.
   $C_1 - C_{18} \leqslant 0,01\ \mu F$, $C_{BP} = C_1 + C_2 + \ldots C_{18} \leqslant 0,05\ \mu F$, $R_1 - R_{18} \geqslant 2\ M\Omega$.
8. $R_{osc} = 0,1\ M\Omega$, $C_{osc} = 390$ pF.
9. Number of segments 2 or 18.
   For n = 2:
   $$V_{IO} = V_c - V_{ref\,min} - \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$
   For n = 18:
   $$V_{IO} = V_c - V_{ref\,max} + \frac{(V_{ref\,max}) - (V_{ref\,min})}{18} \pm V_H$$
10. See equation [1].
11. Condition applies with clock oscillator such that $f_{BP} = 100$ Hz.

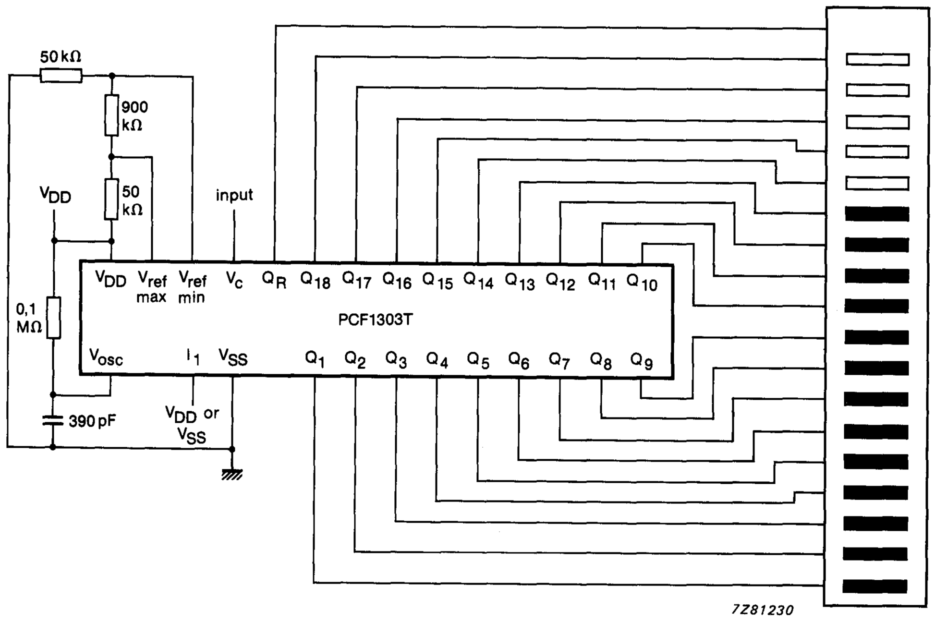


Fig. 3 Typical application.

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

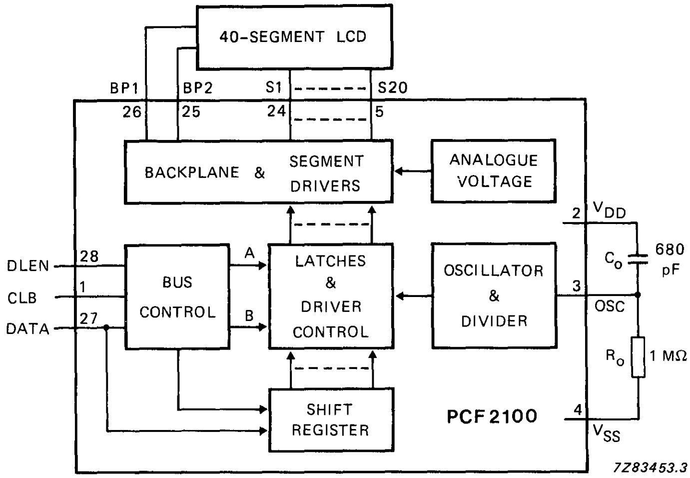


Fig. 1 Block diagram; PCF2100

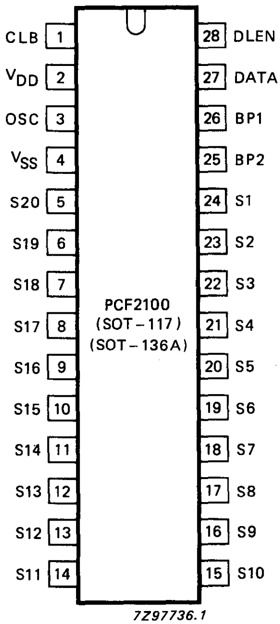


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply	
4	V_{SS}	negative supply	

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
27	DATA	data line	CBUS
28	DLEN	data line enable	CBUS

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

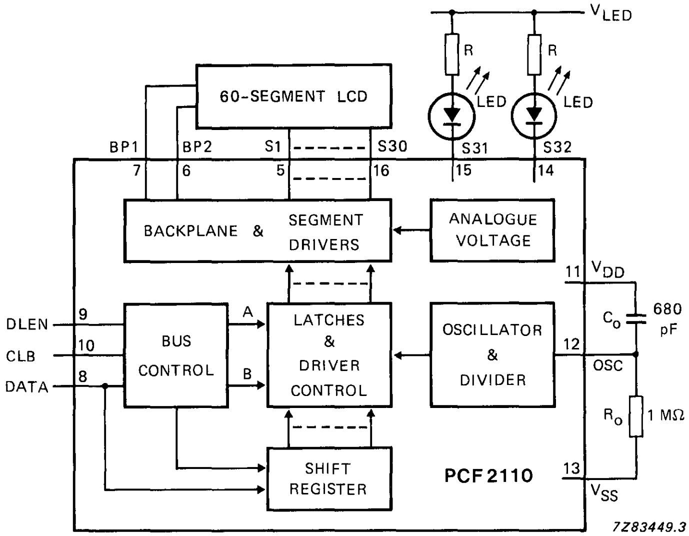


Fig. 3 Block diagram; PCF2110 (SOT-129).

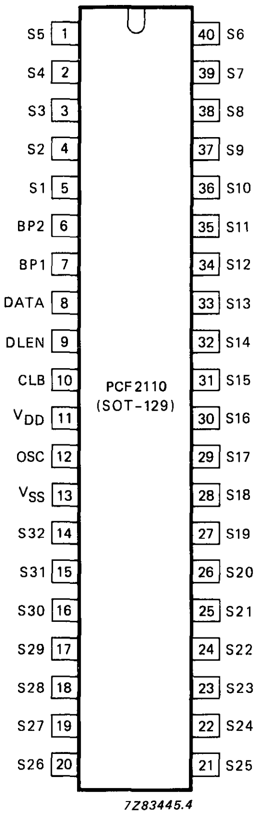


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply	
13	V_{SS}	negative supply	

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs	
6	BP2	backplane drivers (commons of LCD)	
7	BP1	backplane drivers (commons of LCD)	
14	S32	LED driver outputs	
15	S31	LED driver outputs	
16 to 40	S30 to S6	LCD driver outputs	

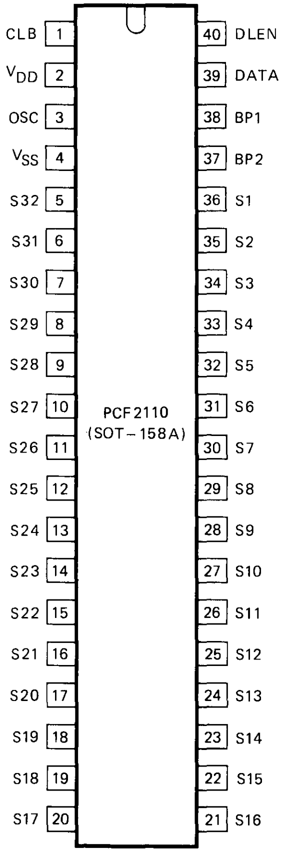


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Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

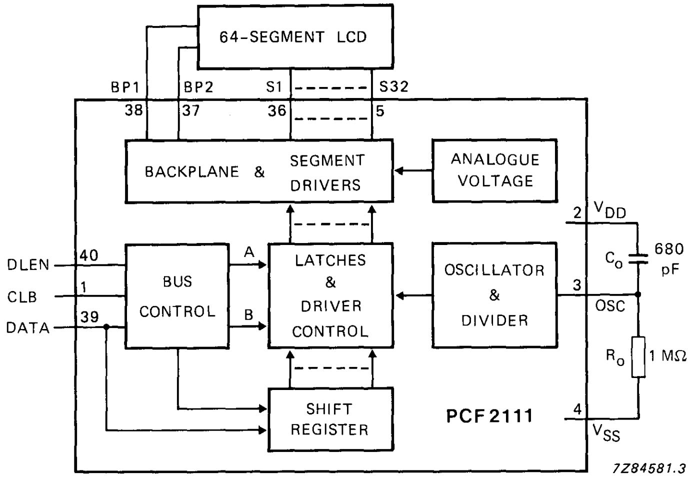


Fig. 6 Block diagram; PCF2111

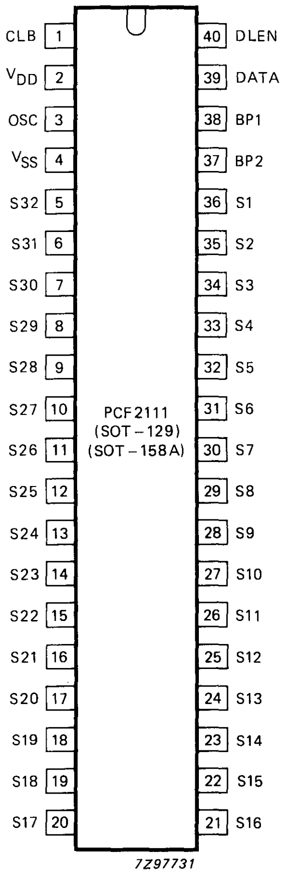


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

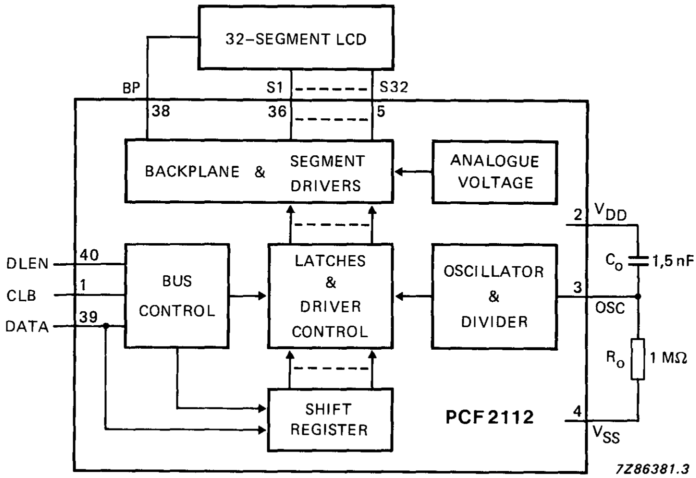


Fig. 8 Block diagram; PCF2112

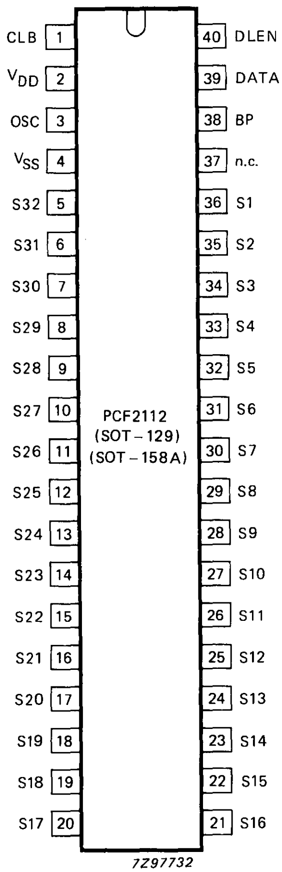


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

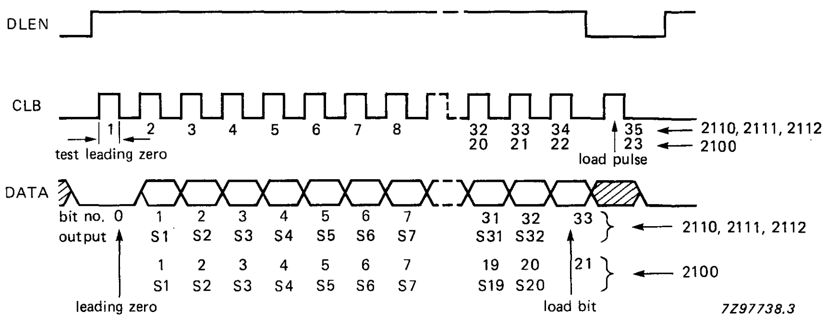


Fig. 10 CBUS data format.

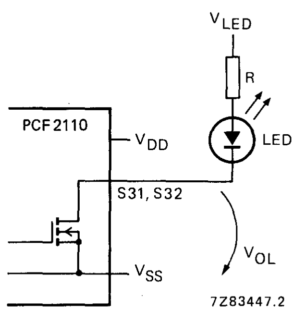


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

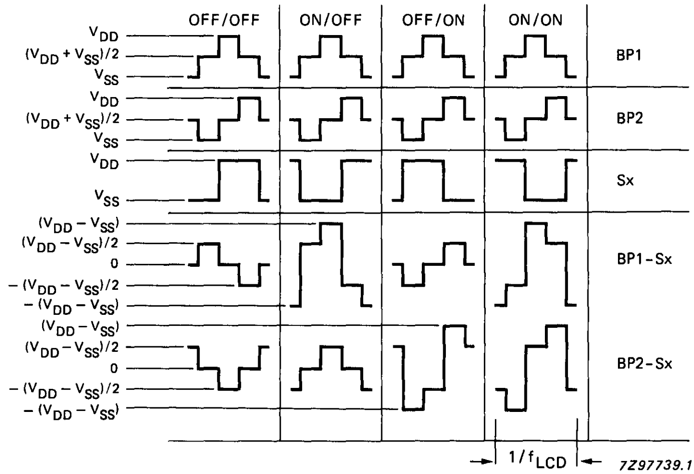


Fig. 12 Timing diagram (except PCF2112).

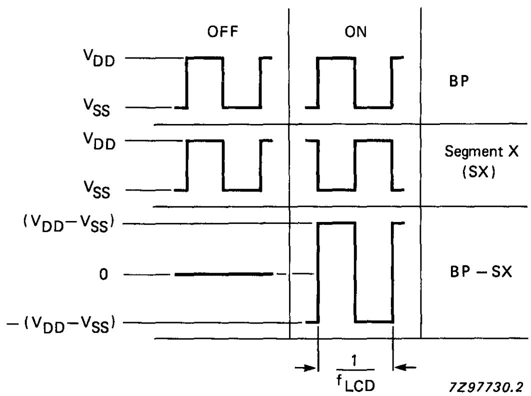


Fig. 13 Timing diagram for PCF2112.

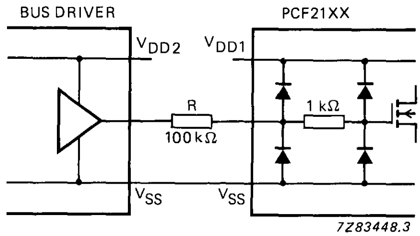
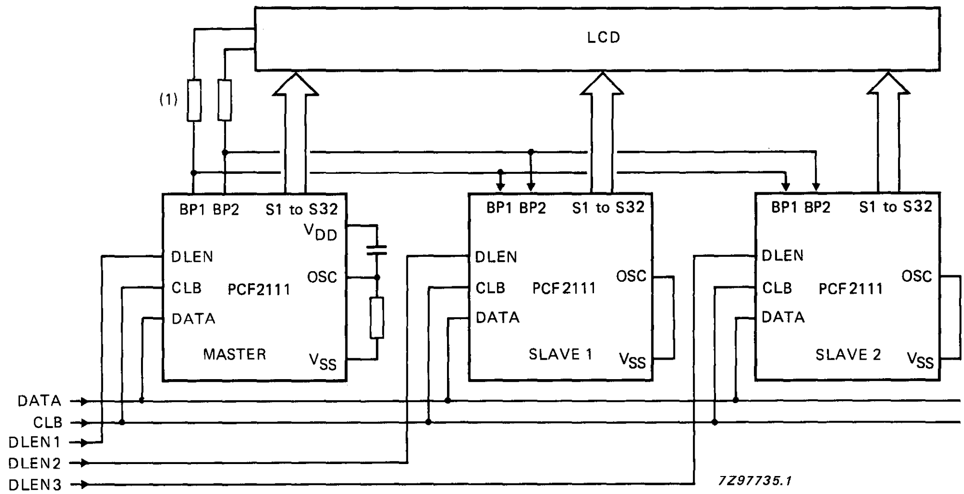


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu$A.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be > 2,7 kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}–0,5	V_{DD}+ 0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}–0,5	V_{DD}+ 0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	–	50	mA
DC input current		$\pm I_I$	–	20	mA
DC output current		$\pm I_O$	–	25	mA
Total power dissipation per package	note 1	P_{tot}	–	500	mW
Power dissipation per output		P_O	–	100	mW
Storage temperature range		T_{stg}	–65	+ 150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 2{,}25$ to $6{,}5$ V; $T_{amb} = -40$ to $+85$ °C; $R_O = 1$ MΩ; $C_O = 680$ pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	$C_O = 1{,}5$ nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	$V_{DD} = 5$ V	t_{BS}	–	20	100	μs
Driver delay with test loads	$V_{DD} = 5$ V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

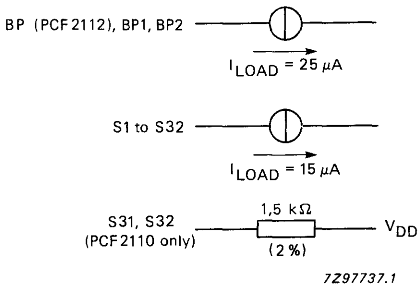
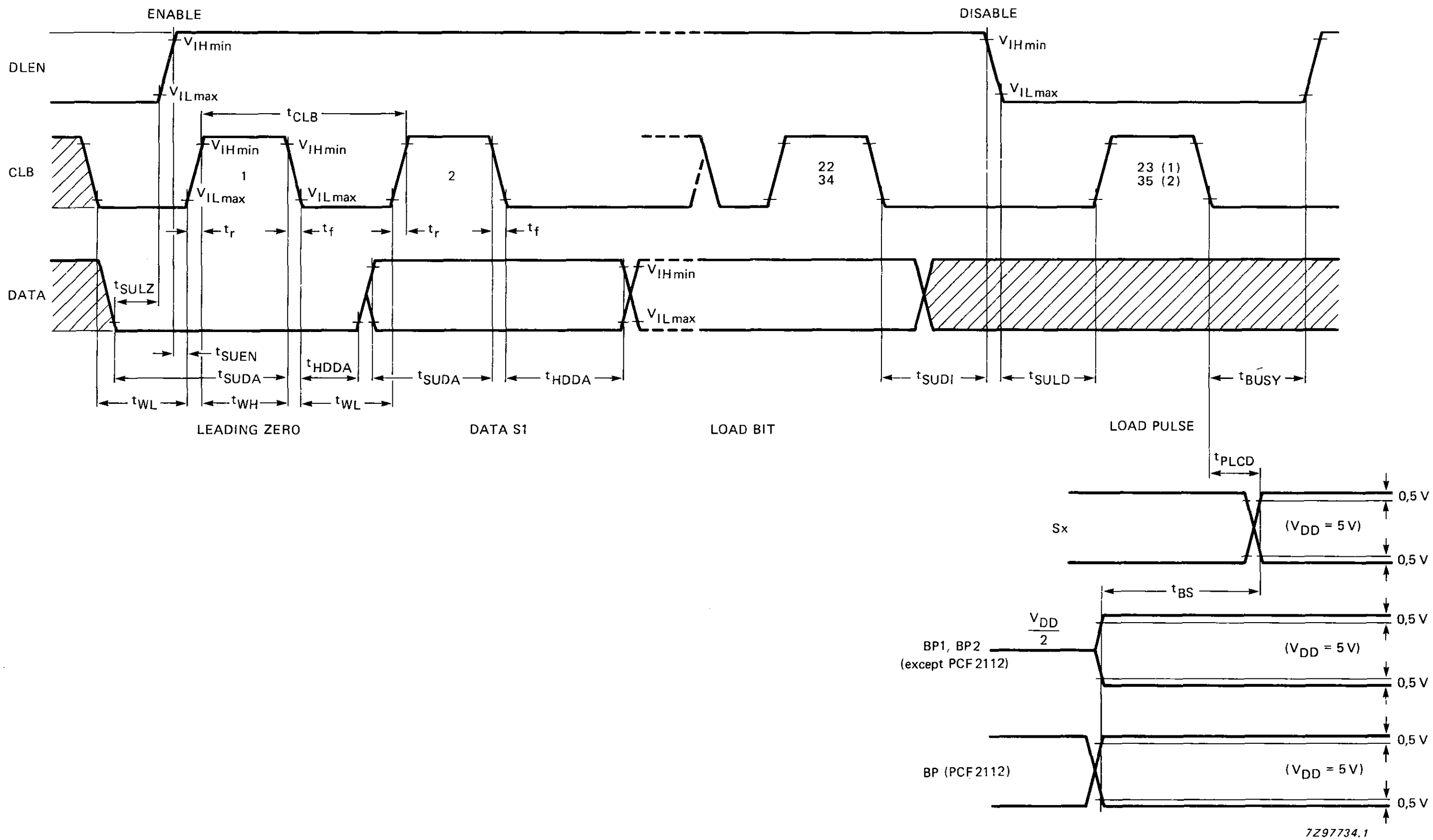


Fig. 16 Test loads.



(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

Fig. 17 CBUS timing.

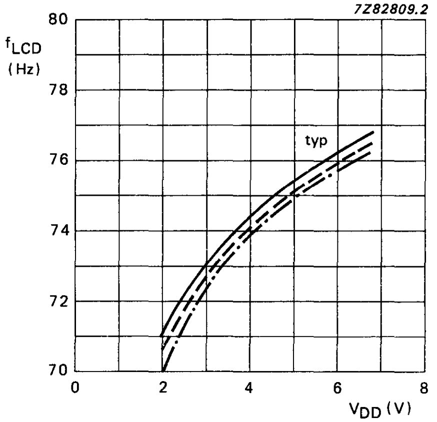


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
–. –. – T_{amb} = + 85 °C.

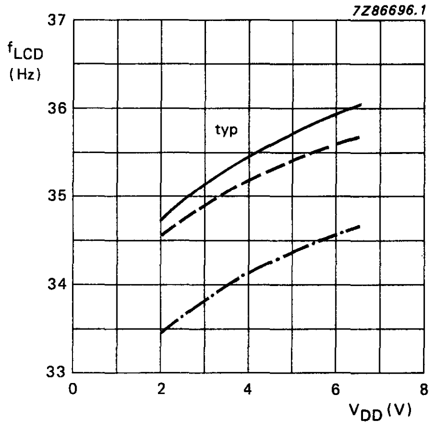


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
–. –. – T_{amb} = + 85 °C.

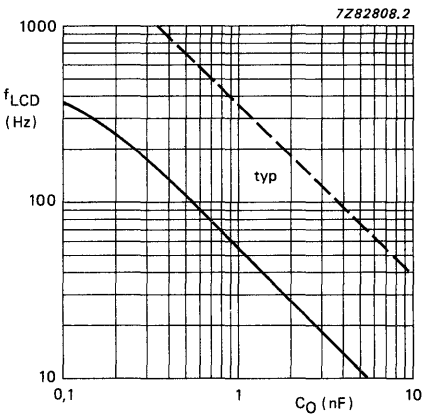


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

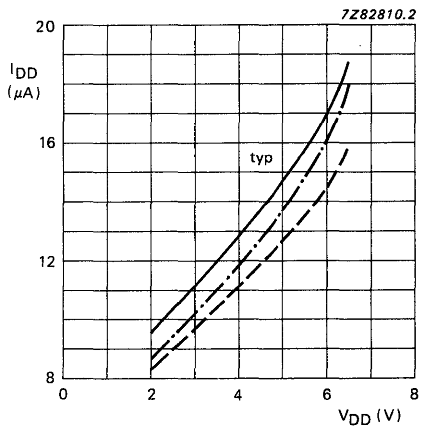


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
–. –. – T_{amb} = + 85 °C.

DEVELOPMENT DATA

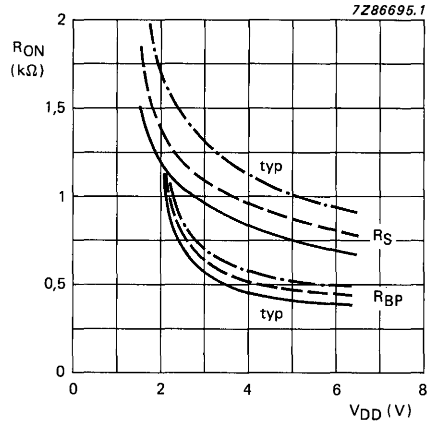


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

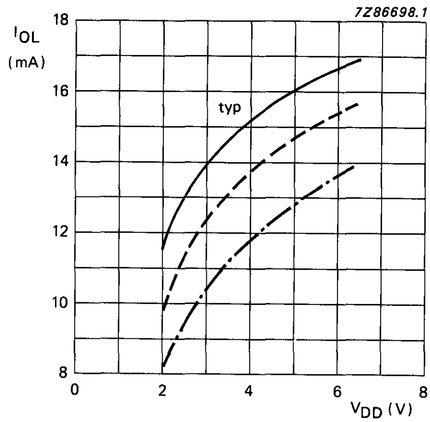


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding (TAB) module (SOT235)

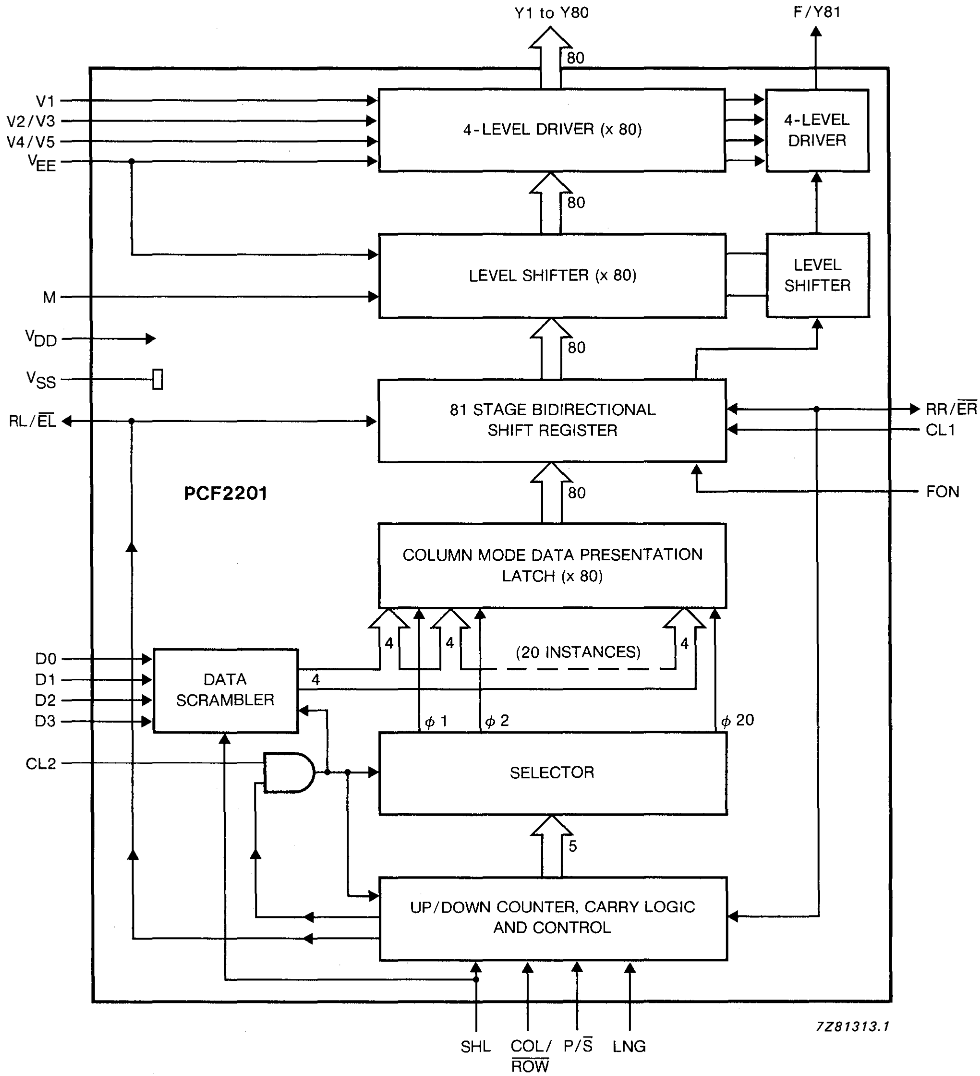


Fig. 1 Block diagram.

DEVELOPMENT DATA

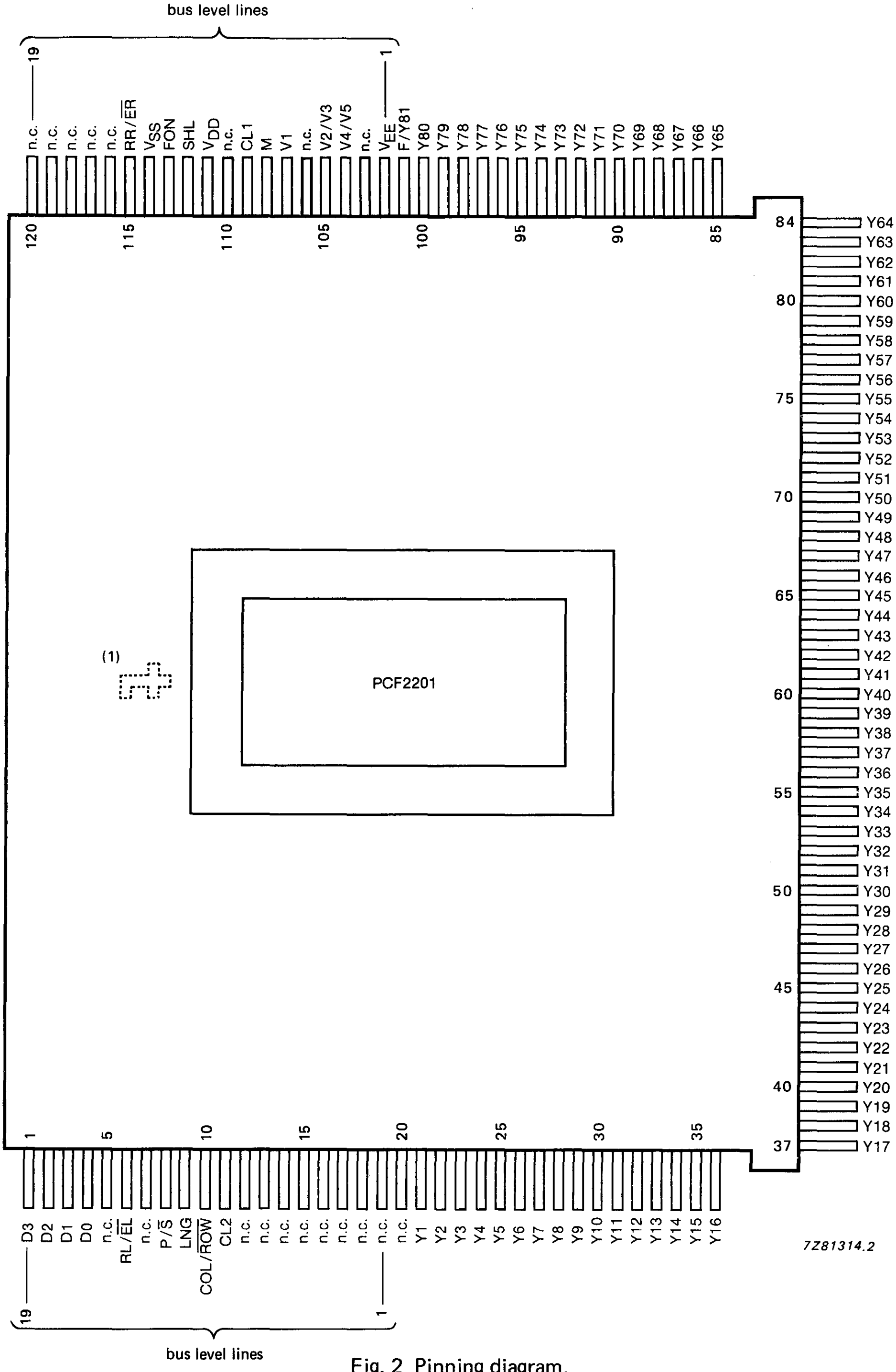


Fig. 2 Pinning diagram.

(1) mark orientation

PINNING FUNCTIONS

mnemonic	I/O	function
V_{DD}	P	Positive supply voltage (5 V)
V_{SS}	P	Logic ground (0 V)
V_1	P	Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
V_2/V_3	P	Upper non-selection level for row (V2) or column (V3) driver
V_4/V_5	P	Lower non-selection level for row (V5) or column (V4) driver
V_{EE}	P	Most negative LCD supply voltage (−20 V), selection level
Y1 to Y80	O	Liquid crystal driver outputs
CL1	I	Clock for 81 stage bidirectional shift register Loads parallel data from the data presentation latch and frame control in column driver mode Shifts data in row driver mode Negative edge triggered
CL2	I	Data transfer clock in column driver modes Data must be valid on the negative edge of CL2 Unused in row driver mode (may be left open)
COL/$\overline{\text{ROW}}$	I	Column/row driver mode select
P/$\overline{\text{S}}$	I	Parallel/serial mode select for column drivers Tie to V_{SS} in row driver mode
SHL	I	Shift direction select
D0 to D3	I	Data inputs in column driver modes Unused in row driver mode (may be left open) Filling order: (see table below) Also in the **serial** column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary

COL/$\overline{\text{ROW}}$	P/$\overline{\text{S}}$	SHL	D0	D1	D2	D3
H	L	L	Y1, Y2, Y3,.	unused	unused	unused
H	L	H	Y80, Y79,...	(may be left open)	(may be left open)	(may be left open)
H	H	L	Y1, Y5, Y9,.	Y2, Y6, Y10,.	Y3, Y7, Y11,.	Y4, Y8, Y12,..
H	H	H	Y80, Y76,...	Y79, Y75,....	Y78, Y74,....	Y77, Y73,.....

mnemonic	I/O	function
RL/$\overline{EL}$ RR/$\overline{ER}$	I/O	Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes

COL/$\overline{ROW}$	P/$\overline{S}$	SHL	RL/$\overline{EL}$	RR/$\overline{ER}$	comments
L	L	L	I	O	shift direction: RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)
L	L	H	O	I	shift direction: RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)
H	L	L	I	O	RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$
H	L	H	O	I	RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$
H	H	L	I	O	RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$
H	H	H	O	I	RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$

In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW

mnemonic	I/O	function
LNG	I	Length control

COL/$\overline{ROW}$	LNG	SHL	description	valid Yi	undefined Yi
L	L	L	65-bit row mode	Y1...Y65	Y66...Y80, F/Y81
L	L	H	operation	Y17...Y80, F/Y81	Y1...Y16
L	H	L	81-bit row mode	Y1...Y80, F/Y81	–
L	H	H	operation	Y1...Y80, F/Y81	–
H	L	L	64-bit column	Y1...Y64	Y65...Y80
H	L	H	mode operation	Y17...Y80	Y1...Y16
H	H	L	80-bit column	Y1...Y80	–
H	H	H	mode operation	Y1...Y80	–

In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>–</td><td>not connected</td></tr>
</table>

* Patent application pending.

FUNCTIONAL DESCRIPTION

4-level driver

One of the liquid crystal driver levels (V_1, V_2/V_3, V_4/V_5 and V_{EE}) is output onto lines Y1 to Y80 and F/Y81 depending on the state of the relevant level shifter.

Level shifter

The level shifter converts logic level driver information into LCD level selection signals. The LCD level selection signals are dependent on the contents of the 81 stage bidirectional shift register and the state of signals M and COL/$\overline{\text{ROW}}$.

81 stage bidirectional shift register

In row driver mode the bidirectional shift register is used for the row line scan. In column driver mode the bidirectional shift register is used to hold column data until the next line is assembled in the data presentation latch.

Column mode data presentation latch

The column mode data presentation latch provides temporary storage during transfer of column data required for the next row.

Data scrambler

In serial column data transfer, the data scrambler converts 1-bit data to parallel 4-bit nibbles. Data is rearranged by the data scrambler according to the orientation (left or right) of the chip, as defined by pin SHL.

Selector

The selector generates latch clocks $\phi1$ to $\phi20$ for the presentation latch. Selection is determined by the state of the up/down counter and the carry logic.

Up/down counter, carry logic and control

Incoming column data storage locations are determined by the up/down counter making use of enable lines (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$) and the length control select (LNG). The carry logic inhibits the data transfer clock (CL2) in inactive column drivers, thereby reducing power dissipation. When data transfer to one column driver is completed, the subsequent column driver is enabled by the carry logic. The control part co-ordinates the up/down counter and carry logic, depending upon the condition of the device (SHL, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, LNG, RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	V_{SS} −0,3 to V_{SS} + 7	V
LCD supply voltage range	V_{EE}	V_{DD} −30 to V_{DD}	V
V_1, V_2/V_3 voltage range (note 1)	V_U	$\frac{V_{DD} + V_{EE}}{2} - 1$ to V_{DD}	V
V_4/V_5 voltage range (note 1)	V_L	V_{EE} to $\frac{V_{DD} + V_{EE}}{2} - 1$	V
Input voltage range (CL1, CL2, COL/$\overline{\text{ROW}}$, P/$\overline{\text{S}}$, SHL, D0, D1, D2, D3, RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$, LNG, FON, M)	V_I	V_{SS} −0,3 to V_{DD} + 0,3	V
Output voltage range (RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$)	V_O	V_{SS} −0,3 to V_{DD} + 0,3	V
Driver output voltage range (F/Y81, Y1 to Y80)	V_Y	V_{EE} −0,3 to V_{DD} + 0,3	V
DC input current	$\pm I_I$	max. 20	mA
DC output current	$\pm I_O$	max. 25	mA
V_{DD}, V_{SS}, V_1, V_2/V_3, V_4/V_5 or V_{EE} current	$\pm I_{SUP}$	max. 20	mA
Power dissipation per package	P_{tot}	max. 400	mW
Power dissipation per output	P_o	max. 100	mW
Storage temperature range	T_{stg}	−65 to + 150	^oC

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

$V_{SS} = 0$ V; $V_{DD} = 4,5$ to 5,5 V;

$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$; $f_M = 100$ Hz

$T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	V_{DD}–25	–	V_{DD}–5	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD}	
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	V_{DD}–0,05	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DEVELOPMENT DATA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH $RL/\overline{EL}$ and $RR/\overline{ER}$	$V_{OH} = V_{DD} - 1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, $COL/\overline{ROW}$, $P/\overline{S}$, SHL, D0 to D3, $RL/\overline{EL}$, $RR/\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	µA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	µA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ µA; $V_{EE} = V_{DD} - 25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$;
$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	µs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . .Y80, F/Y81	$V_{EE} = V_{DD}$ –20 V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

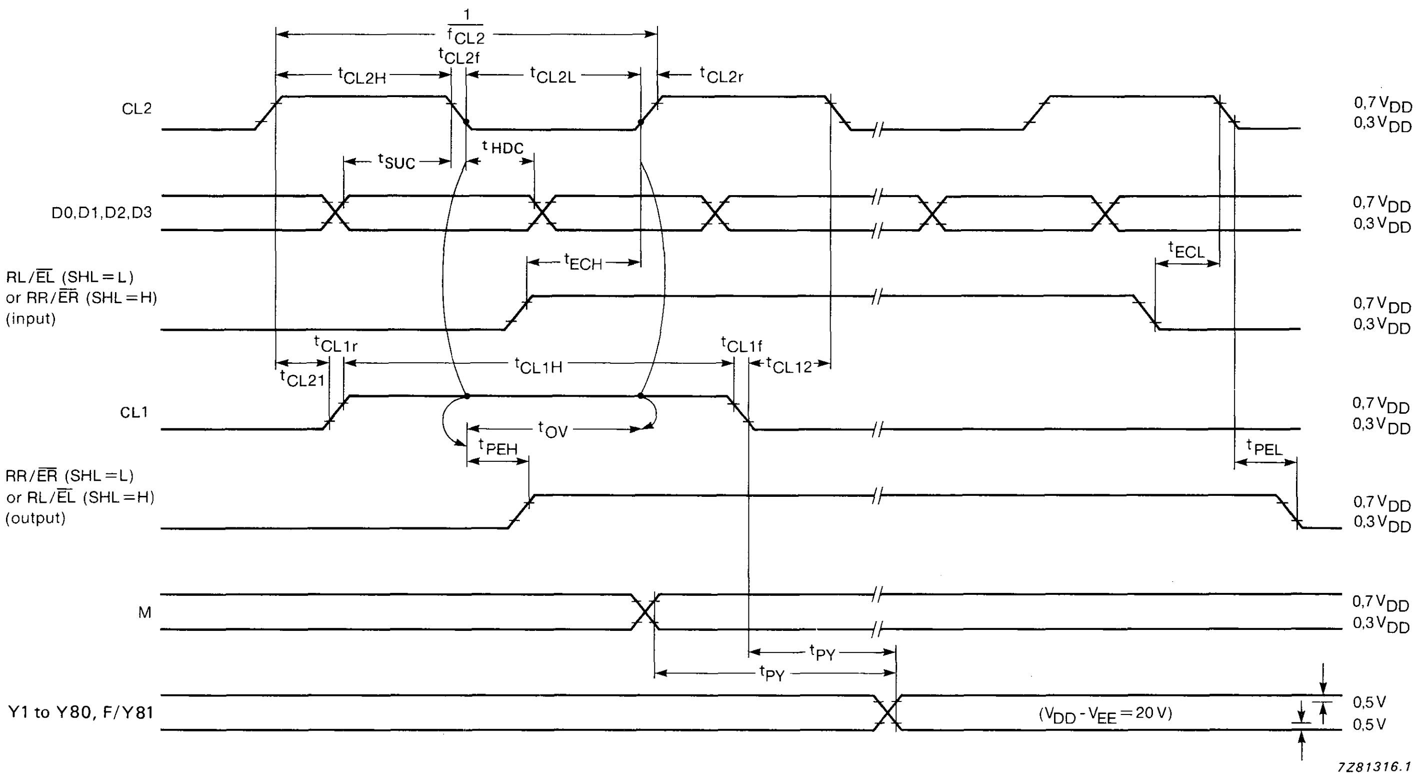


Fig. 4 Column driver timing waveforms.

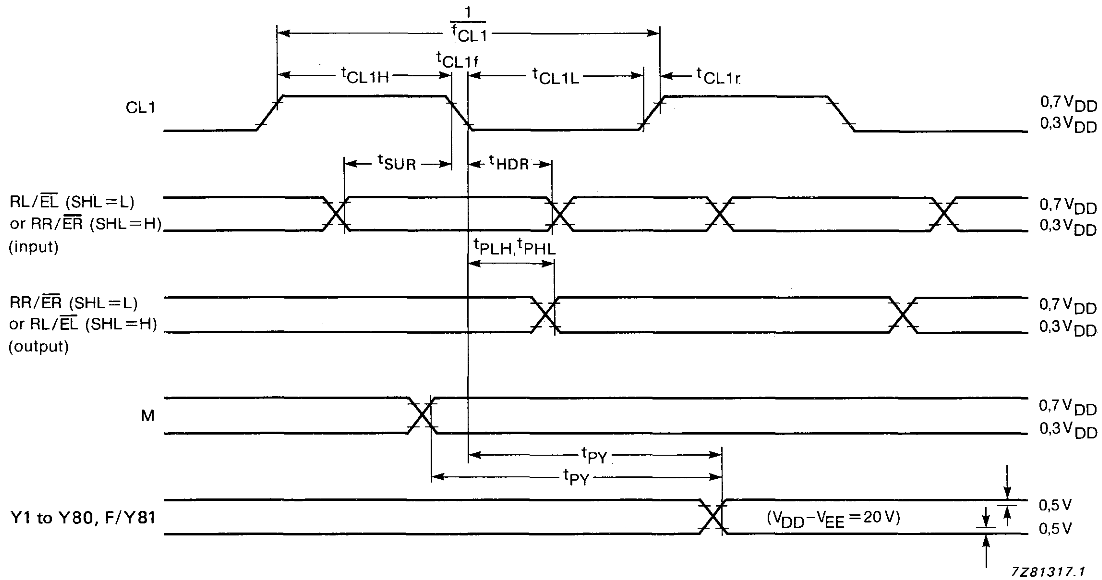


Fig. 5 Row driver timing waveforms.

APPLICATION INFORMATION

Generation of LCD bias levels

Optimum contrast for LCD flat-panels is achieved when the bias levels are selected using the formulae in Table 1. The multiplex rate is denoted by the variable n ($n \geqslant 9$). V_{th} is defined as the LCD threshold voltage, typically where the LCD exhibits approximately 10% contrast. The ratio of the 'ON' voltage to the 'OFF' voltage is discrimination (D) and is a measure of the flat-panel contrast at a given multiplex rate.

Table 1 LCD flat-panel bias levels for optimum contrast ($V_{op} = V1 - V_{EE}$)

$\frac{V_2}{V_{op}} = \frac{\sqrt{n}}{\sqrt{n}+1}$	$\frac{V_3}{V_{op}} = \frac{\sqrt{n}-1}{\sqrt{n}+1}$	$\frac{V_4}{V_{op}} = \frac{2}{\sqrt{n}+1}$	$\frac{V_5}{V_{op}} = \frac{1}{\sqrt{n}+1}$
$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$		$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$	
$D = \frac{V_{on(rms)}}{V_{off(rms)}} = \frac{\sqrt{n-1}}{\sqrt{n}-1}$		$\frac{V_{op}}{V_{th}} = \frac{\sqrt{n}+1}{\sqrt{2(1-1/\sqrt{n})}}$	

The intermediate bias levels are generated by a resistive divider (see Fig. 6). Capacitors (C) are used to smooth out switching transients. Considerable power consumption may result by using this arrangement when driving a large LCD flat-panel, because of the low impedance of the resistive divider.

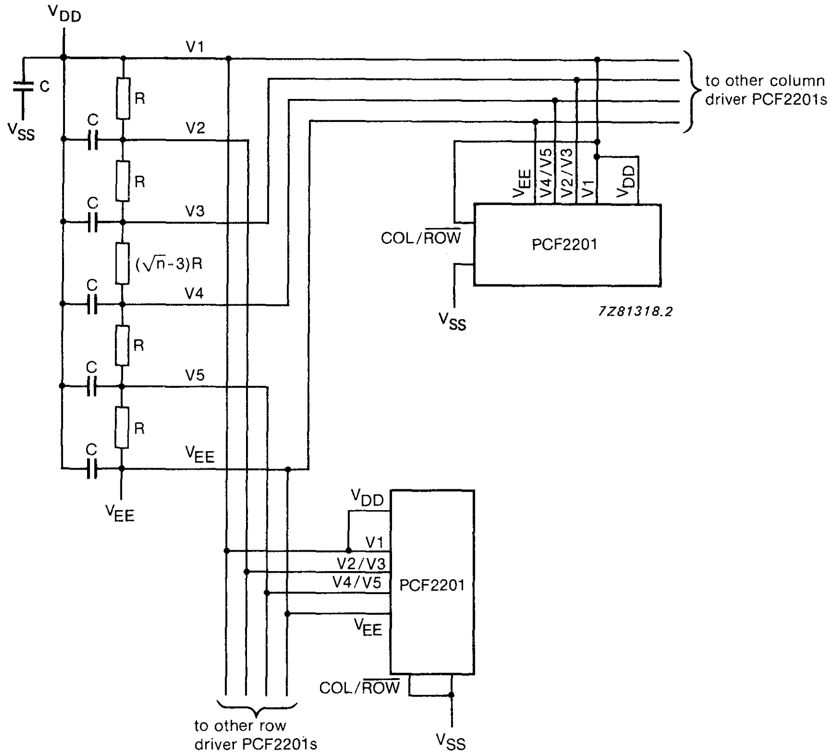


Fig. 6 Unbuffered LCD biasing level generation.

A better solution for LCD flat-panel biasing is presented in Fig. 7. The operational amplifiers provide low impedance biasing with a low power consumption. The fairly high impedance which can be implemented at the resistive divider, helps maintain low power consumption. One diode voltage drop seperates V1 from V_{DD} to compensate for the limited common mode voltage range (V+ −1,5 V) when the operational amplifiers are powered between V_{DD} and V_{EE}.

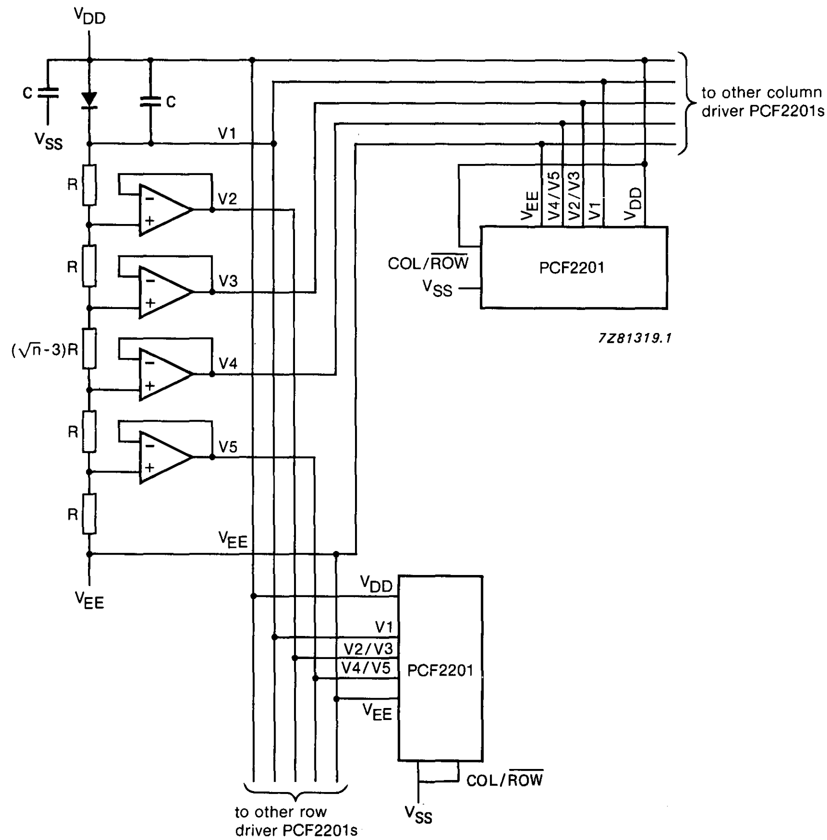


Fig. 7 Buffered LCD bias level generation.

Typical LCD flat-panel application

Alphanumeric/graphic computer terminals with LCD flat-panel screens using 200 x 640 dots are very popular. The format of 200 x 640 is compatible with the standard 25 lines by 80 characters at 8 x 8 dot character fonts. Fig. 8 gives a possible circuit using 19 PCF2201's, with upper and lower half screens used for good contrast. The use of half screens reduces the multiplex rate to 1:100 (Fig. 9 gives the timing information).

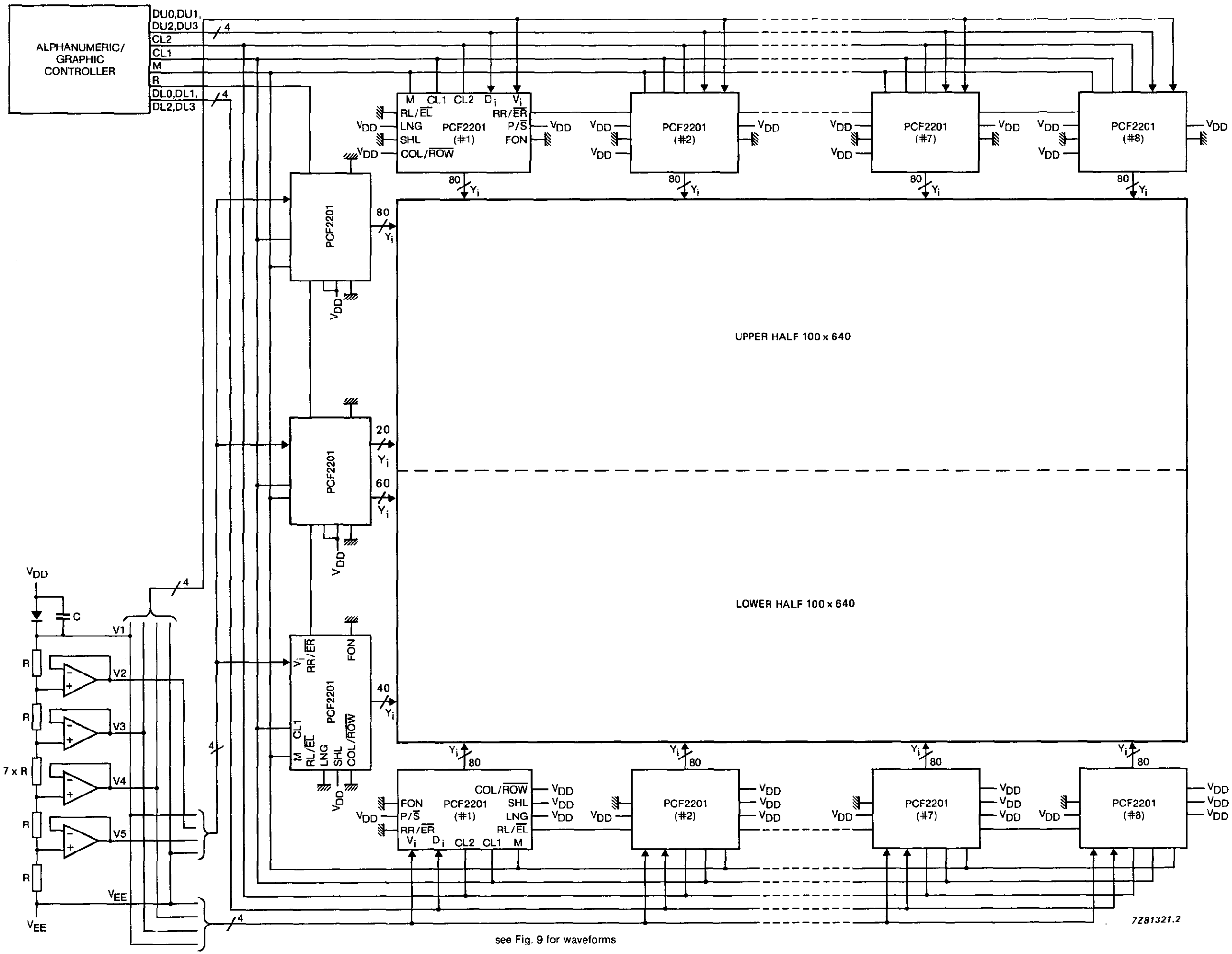


Fig. 8 LCD flat-panel with 1:100 multiplex rate in upper and lower half screens.

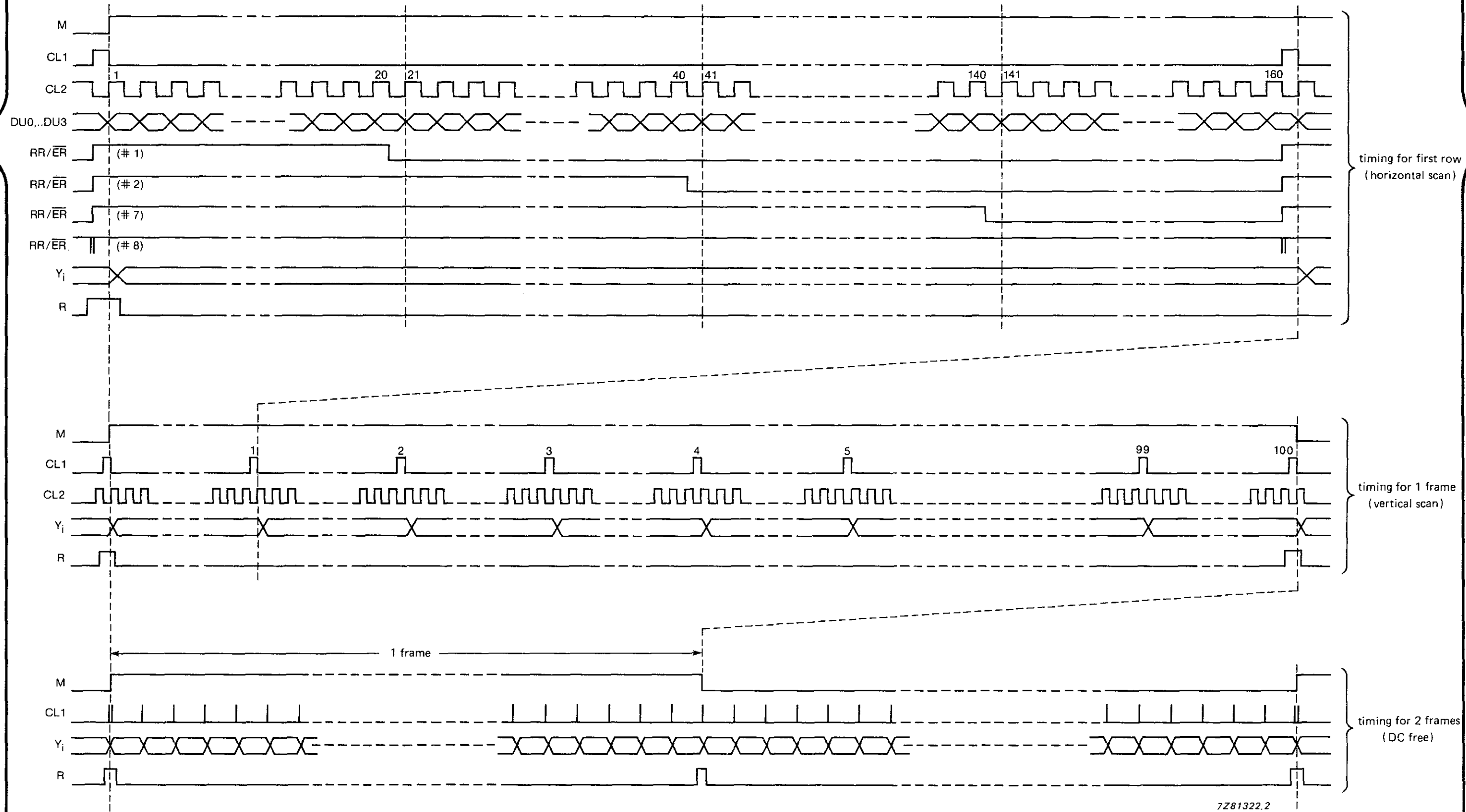
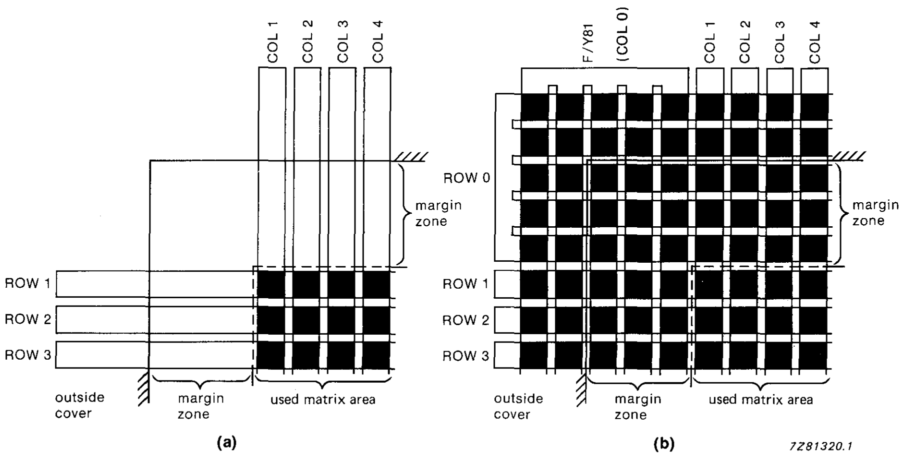


Fig. 9 Timing for the upper half screen of the LCD flat-panel (Fig. 8).
For the lower half screen, replace RR/$\overline{ER}$, DU0, DU1, DU2 and DU3 with RL/$\overline{EL}$, DL0, DL1, DL2, DL3.

Margin control

The used area of the flat-panel matrix is normally smaller than the LCD glass surface. Connection lines outside of the used area of the matrix carry row or column LCD signals (see Fig. 10A). This 'null' state differs slightly in colour from the 'OFF' state pixel for twisted nematic LCD. The structural change in the margin zone is noticeable.

When a high contrast Philips LCD flat-panel of the supertwisted birefringence effect (SBE) type is employed, the situation becomes critital. The colour of the 'OFF' state appears blue and the colour of the 'ON' state appears grey or white. Therefore inverted information is sent to the display, generating dark (blue) characters on a light (grey) background. The margin zone is treated as an extension of the used matrix area (see Fig. 10B), to avoid the margin zone appearing as a dark blue frame. This is extended out to a region where the LCD glass can be covered up. The additional row requires an increase in the multiplex rate from n to n + 1, the additional column is realized by the frame output of the furthest left and right column drivers of the flat-panel. This removes the requirement for additional column drivers packages to provide margin control.



(A) without margin control (B) with margin control

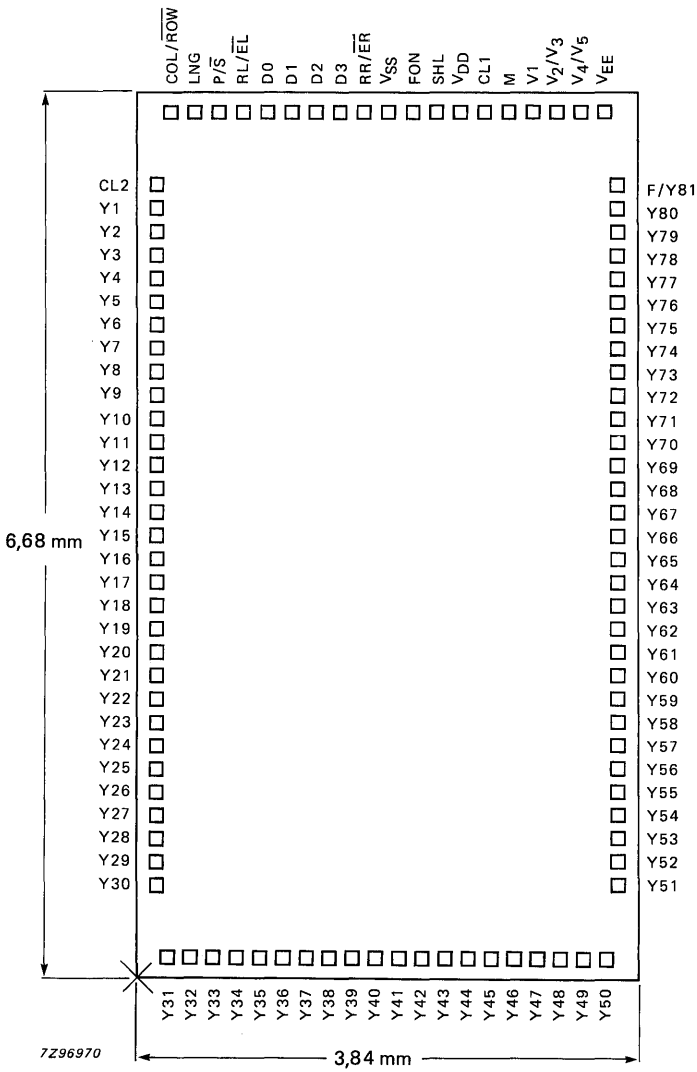
Fig. 10 Upper left corner of the LCD flat-panel.

Single plane wiring

The pinning of the PCF2201 tape-automated bonding package has been selected for ease of wiring. One side of this package contains no pins. The adjacent logic level lines are arranged so that they can be bussed in a single plane on the printed circuit board, which allows single sided substrates to be used.

For ease of wiring layout it is suggested to use the bus-level numbers (see Fig. 2) since most supply lines can be run through at the same level. On the actual package there are 120 pins, of which 19 pins are not internally connected. These extra pins are due to single plane wiring gaps and enhance stability in surface mounting.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

Table 2 Bonding pad centre locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
$RL/\overline{EL}$	820	6526	Y47	3068	154
$P/\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
$COL/\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	$RR/\overline{ER}$	1740	6526
Y42	2188	154			

DEVELOPMENT DATA

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	#	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

Value not yet available.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

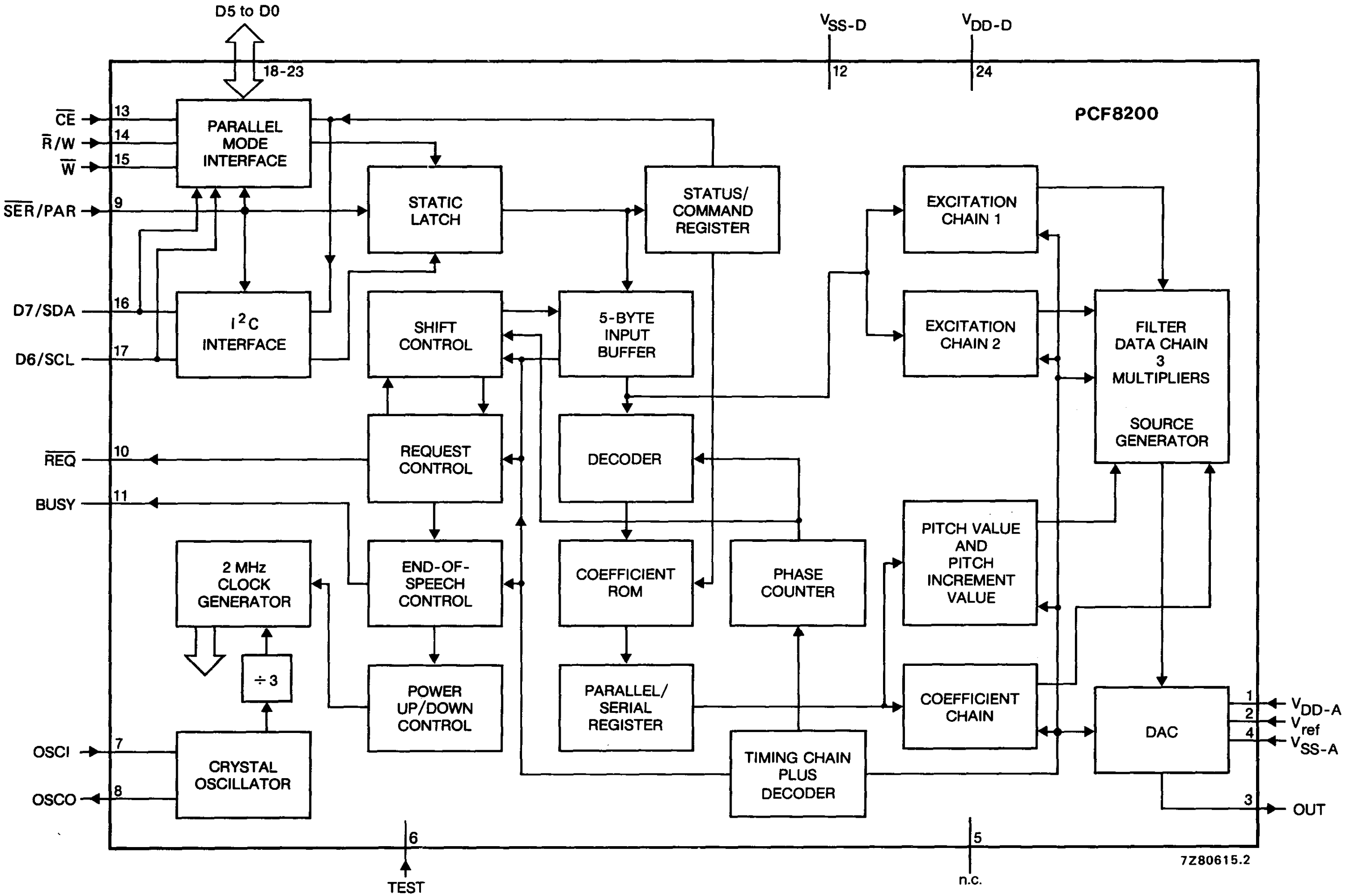


Fig. 1 Block diagram.

PINNING

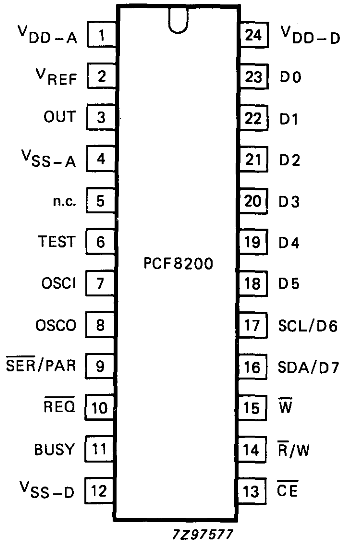


Fig. 2 Pinning diagram.

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	$\overline{R}$/W	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	parallel data input/outputs
20	D3	parallel data input/outputs
21	D2	parallel data input/outputs
22	D1	parallel data input/outputs
23	D0	parallel data input/outputs
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.

The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms
FD1, FD0					

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

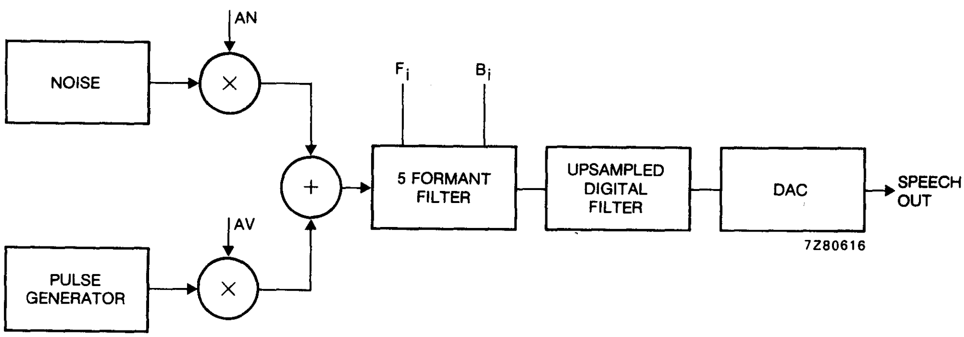


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.

<table>
<tr><th></th><th>D7</th><th></th><th></th><th></th><th></th><th></th><th></th><th>D0</th></tr>
<tr><td>byte 0</td><td colspan="3">B1</td><td colspan="5">F1</td></tr>
<tr><td>byte 1</td><td>F5</td><td colspan="2">B5</td><td colspan="5">PI</td></tr>
<tr><td>byte 2</td><td>FD1</td><td colspan="3">F3</td><td colspan="4">AM</td></tr>
<tr><td>byte 3</td><td>FD0</td><td colspan="2">B3</td><td colspan="5">F2</td></tr>
<tr><td>byte 4</td><td colspan="2">B4</td><td colspan="3">F4</td><td colspan="3">B2</td></tr>
</table>

7Z80617.2

It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

	D7							D0	
byte 0	0	0	0	0	0	0	0	0	"00"
byte 1	1	0	STOP	$\overline{M}$/F	0	0	FS1	FS0	

7Z80618.1

Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

D7							D0
$\overline{REQ}$	BUSY	STOP	x	x	x	x	x

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Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I^{2}C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I^{2}C ADDRESS

On chip there is a I^{2}C slave receiver/transmitter with the address:

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	–0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	–0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	–0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	–40	85	°C
Storage temperature range		T_{stg}	–55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, $\overline{R}$/W, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	# (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	#	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of –40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

Values not yet available.

DEVELOPMENT DATA

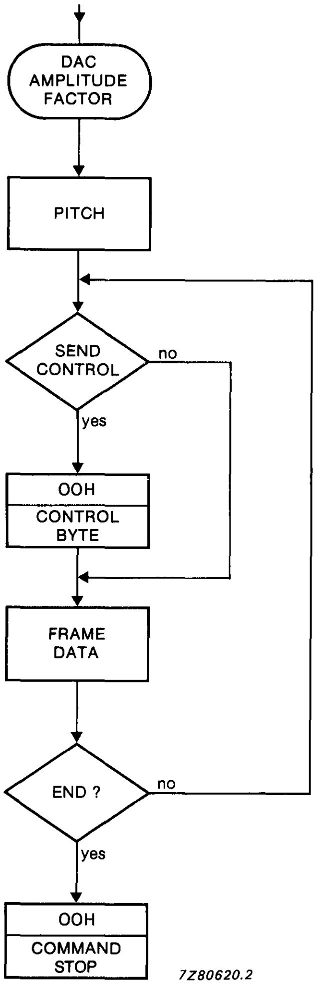
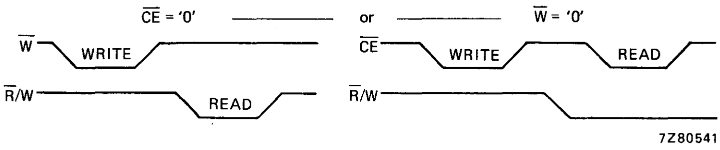


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}$/W and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}$/W and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

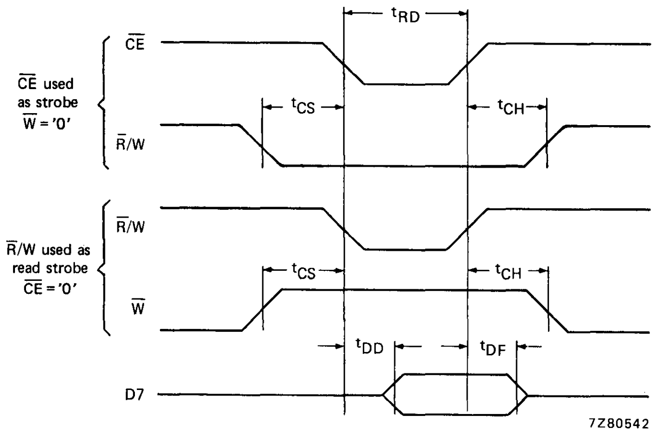


Fig. 8 Read timing.

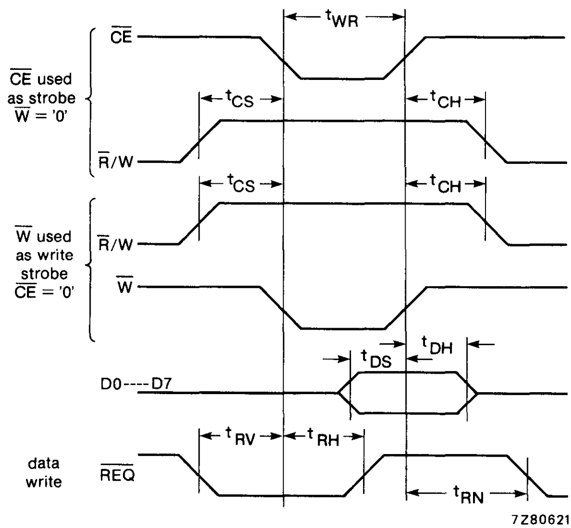


Fig. 9 Write timing.

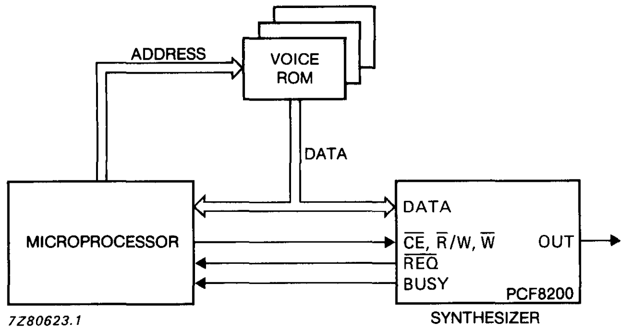


Fig. 10 Typical application configuration with parallel interface.

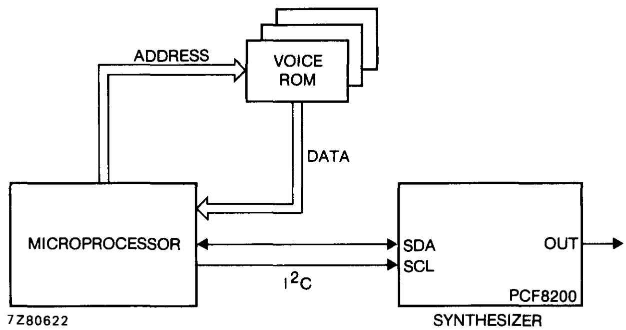


Fig. 11 Typical application configuration with series interface.

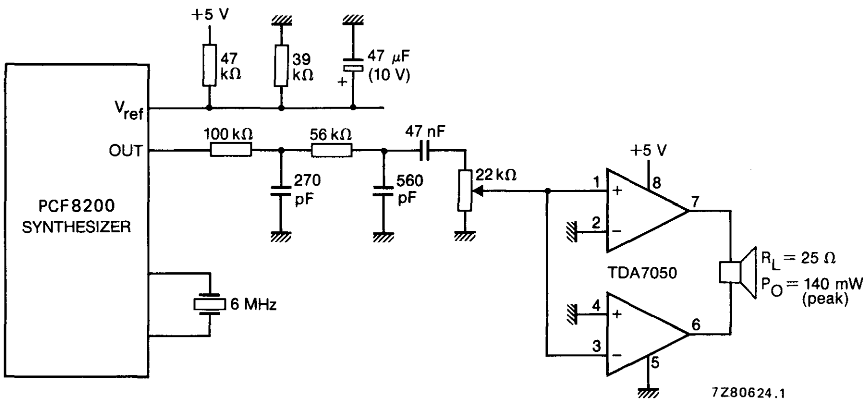


Fig. 12 An example of an output configuration.

DEVELOPMENT DATA

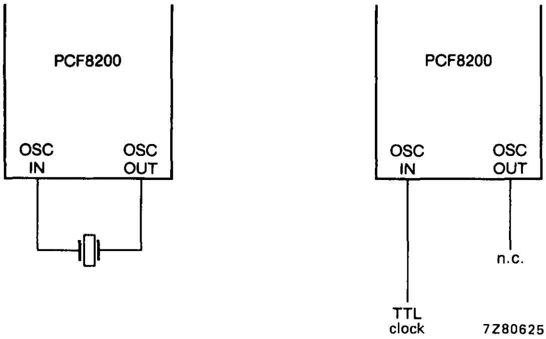


Fig. 13 Oscillator clock configurations.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER FAMILY

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84CXXX microcontroller family. The family consists of the following devices:

• PCF84C00	• PCF84C12	• PCF84C121	• PCF84C430
• PCF84C21	• PCF84C22	• PCF84C230	• PCF84C470
• PCF84C41	• PCF84C42	• PCF84C270	• PCF84C640
• PCF84C81	• PCF84C85	• PCF84C271	

This data sheet describes features of the PCF84CXXX microcontroller family which are common to several family members. For details on a particular device, consult the relevant data sheet.

All family members have quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048 and the PCF84CXXX family is very similar to the MAB8400 family.

Features common to all family members are listed below.

Features

- 8-bit CPU, ROM, RAM, I/O in a single DIL or SO package
- 1 K, 2 K, 4 K or 8 K x 8 ROM; there is also a ROM-less device
- 64, 128 or 256 x 8 RAM
- Quasi-bidirectional I/O port lines
- Two test inputs: one of which is also an external interrupt input
- Single-level vectored interrupt structure
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 V to 5,5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: –40 to + 85 °C

PACKAGE OUTLINES

Consult individual data sheets.

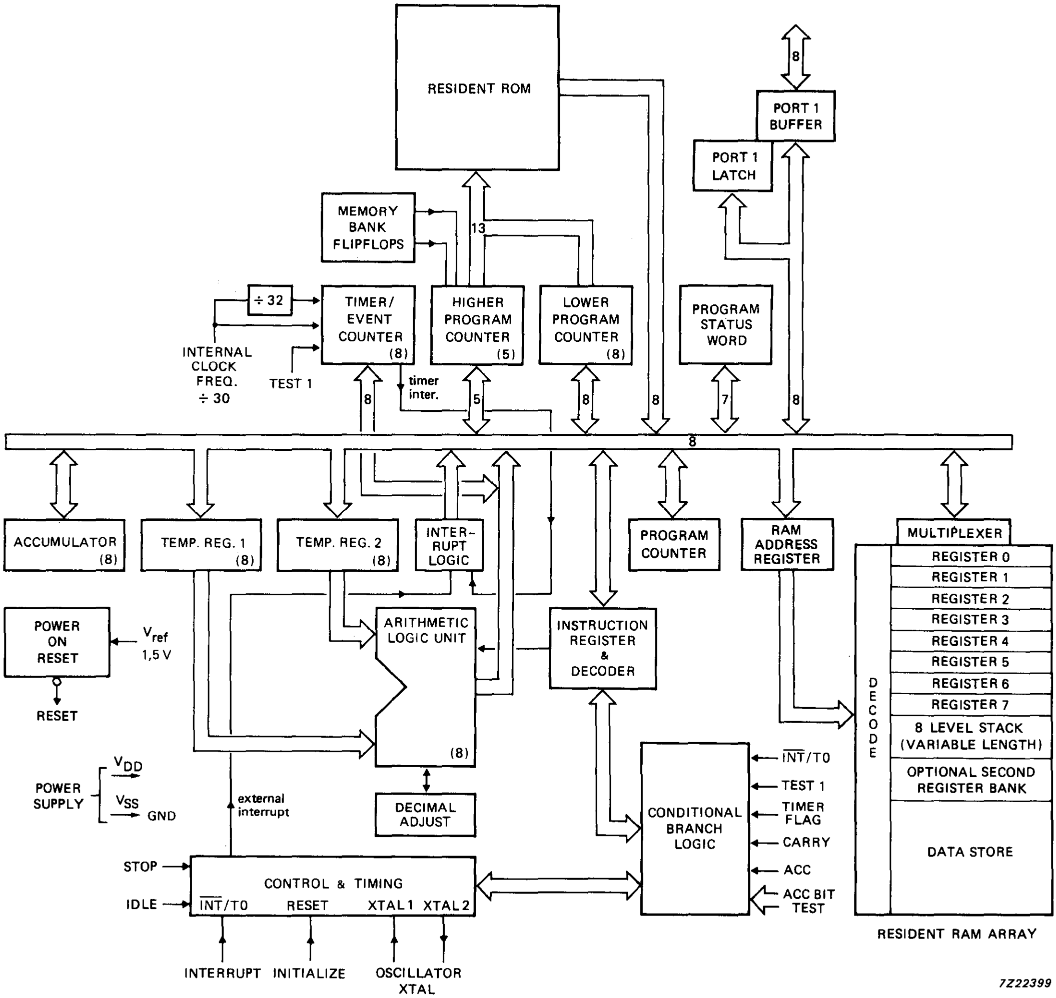


Fig. 1 PCF84CXXX block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the PCF84CXXX family. For detailed information, consult the PCF84CXXX data sheet.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: –40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see PCF84CXXX family data sheet

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word
Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

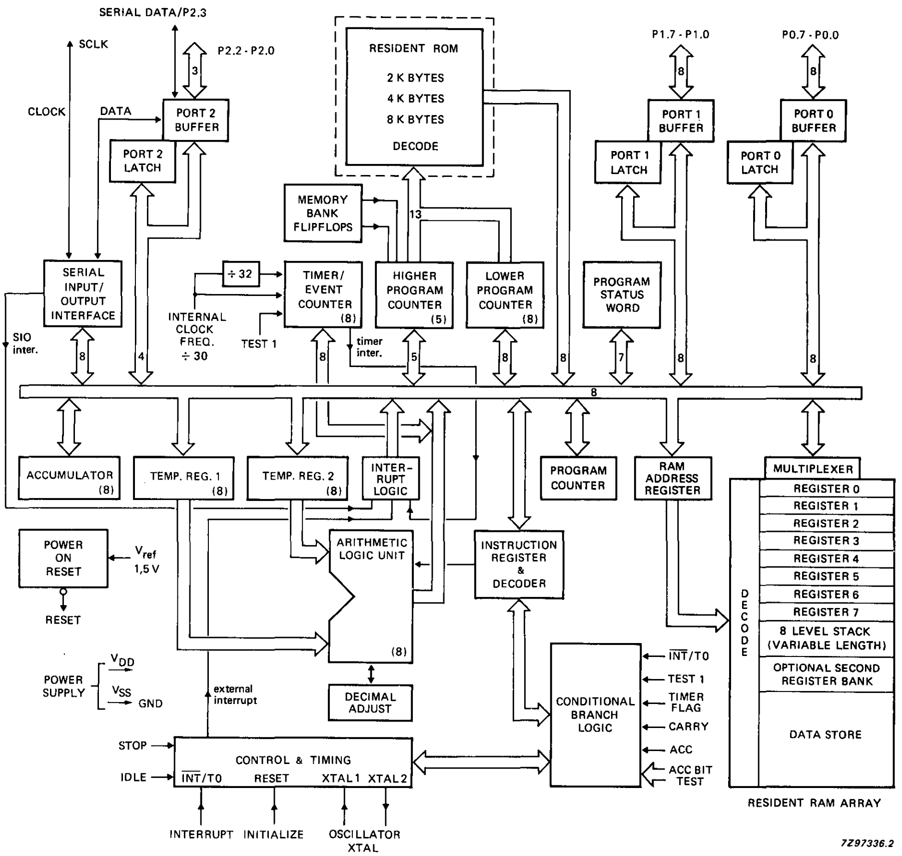
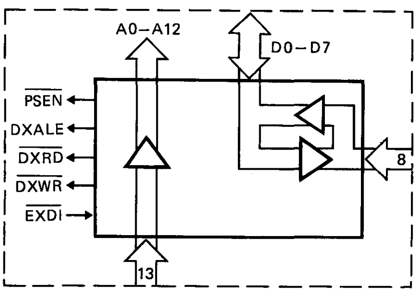


Fig. 1 Block diagram.



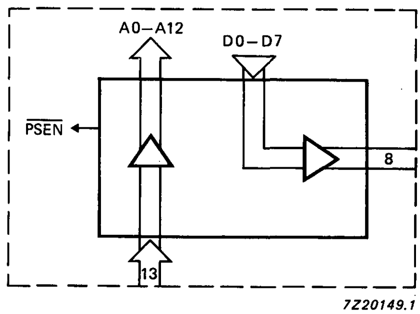


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C12, PCF84C22 and PCF84C42 microcontrollers. Each device has 13 quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C12 – 64 x 8 RAM, 1 K x 8 ROM
- PCF84C22 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C42 – 64 x 8 RAM, 4 K x 8 ROM

These efficient microcontrollers also perform well as arithmetic processors. The instruction set is similar to that of the MAB8048. They have bit handling abilities and facilities for both binary and BCD arithmetic.

These microcontrollers are members of the PCF84CXXX family. For detailed information, consult the PCF84CXXX data sheet.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K, 2 K or 4 K x 8 ROM
- 64 x 8 RAM
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level, vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 V to 5.5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: –40 to + 85 °C

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Interrupts
Oscillator
Timer/event counters
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1
Power-on-reset

PACKAGE OUTLINES

PCF84C12/22/42P: 20-lead DIL; plastic (SOT146).
PCF84C12/22/42T: 20-lead mini-pack; plastic (SO20, SOT163A).

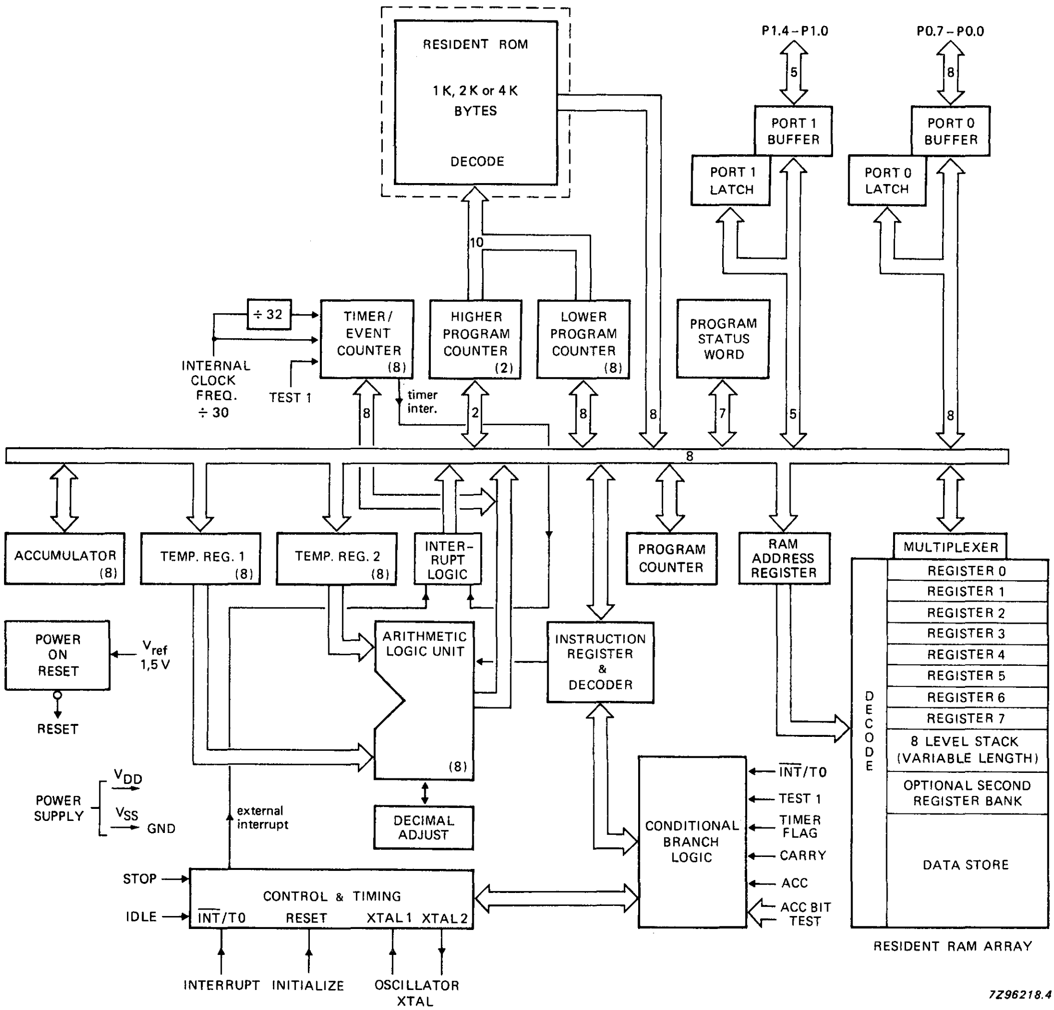


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE REVELANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information on the PCF84CXX see the "Single-chip 8-bit Microcontrollers" user manual.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158).

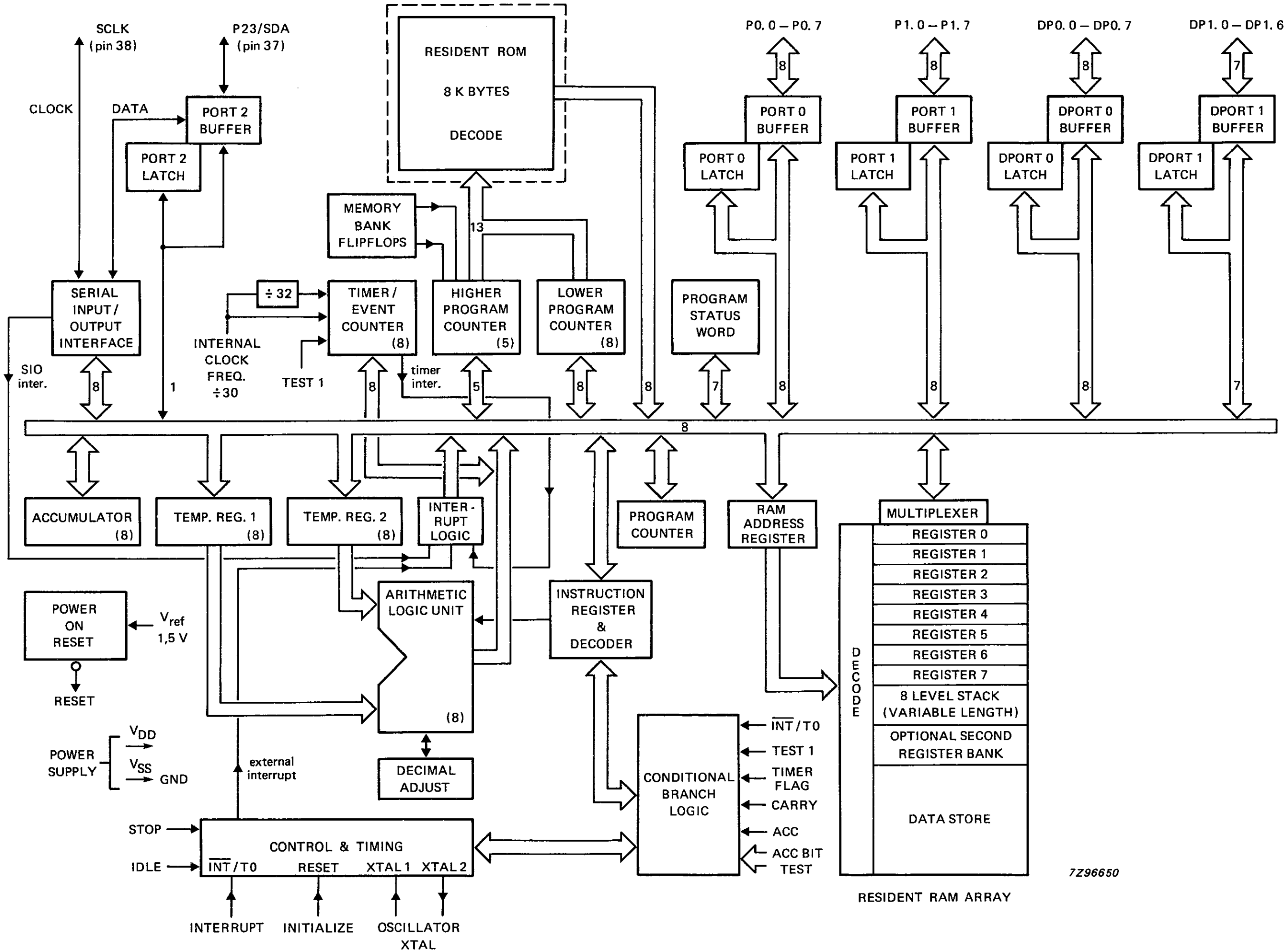


Fig. 1 Block diagram.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

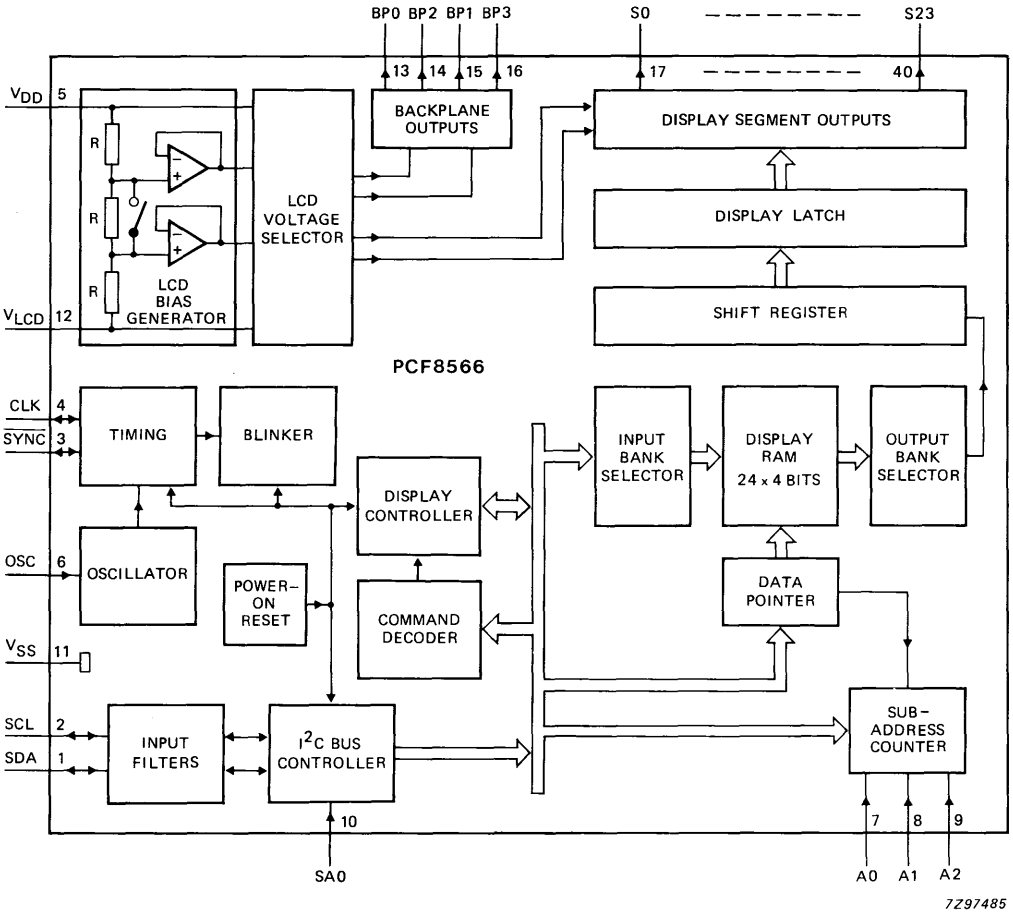


Fig. 1 Block diagram.

DEVELOPMENT DATA

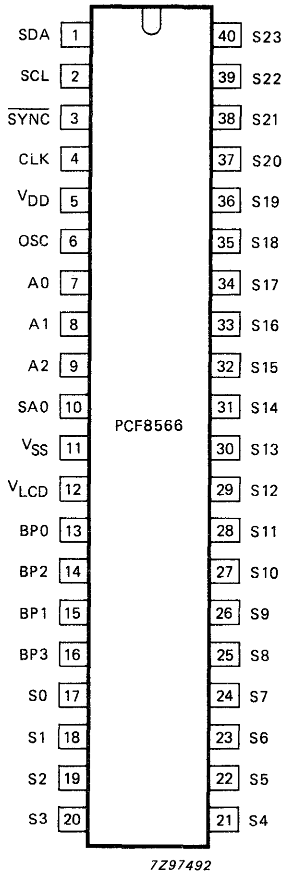


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7 8 9	A0 A1 A2	I^2C bus subaddress inputs
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13 14 15 16	BP0 BP2 BP1 BP3	LCD backplane outputs
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

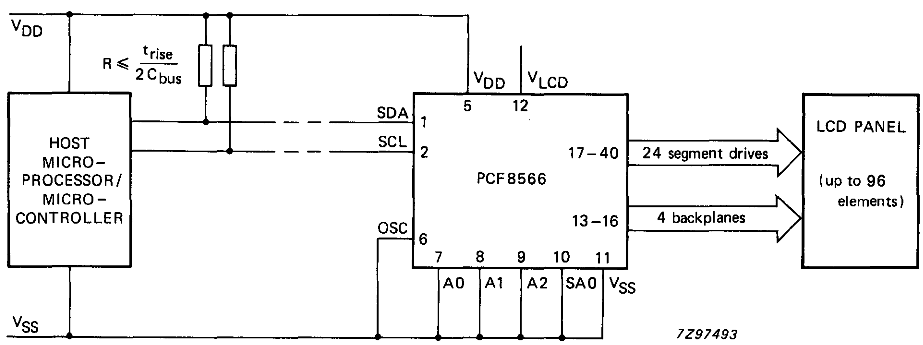


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

DEVELOPMENT DATA

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrsim 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1,732 for 1 : 3 multiplex or $\sqrt{21}/3$ = 1,528 for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\, V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

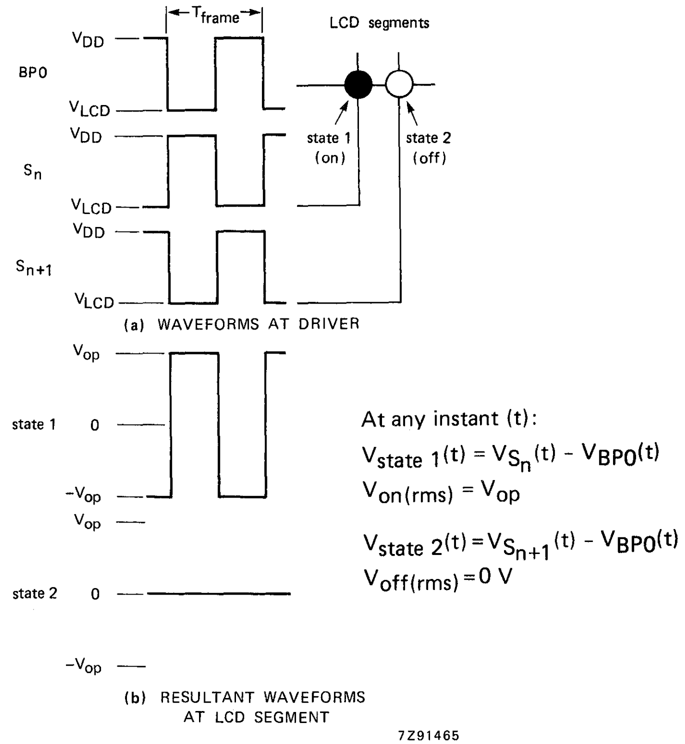


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

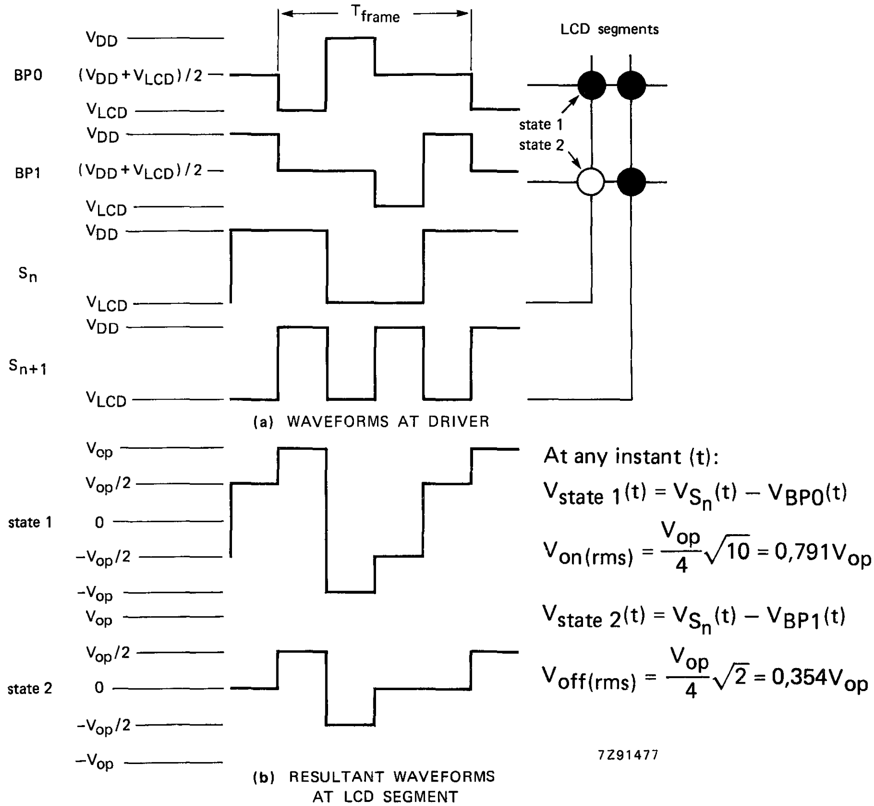
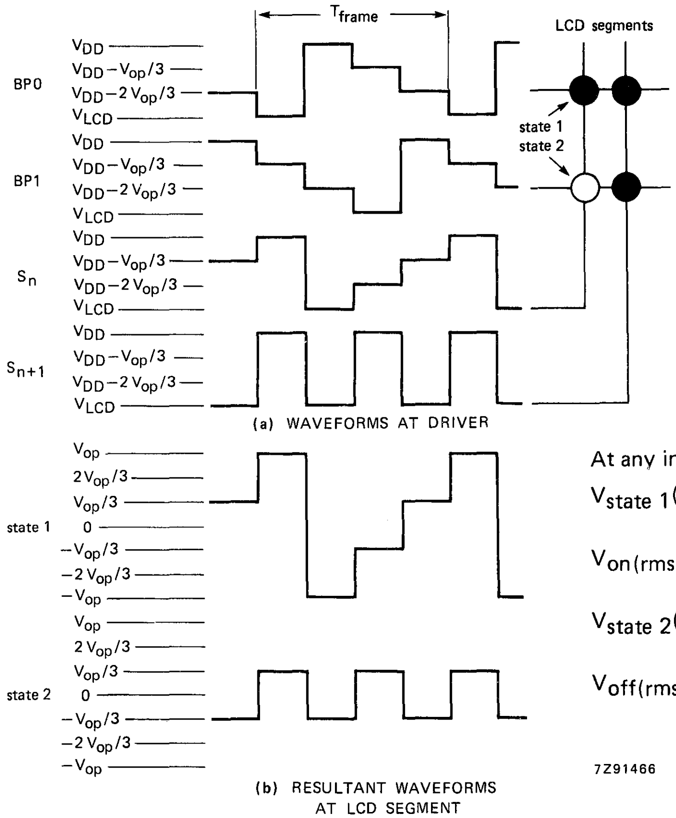


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = \frac{V_{op}}{3}\sqrt{5} = 0{,}745 V_{op}$

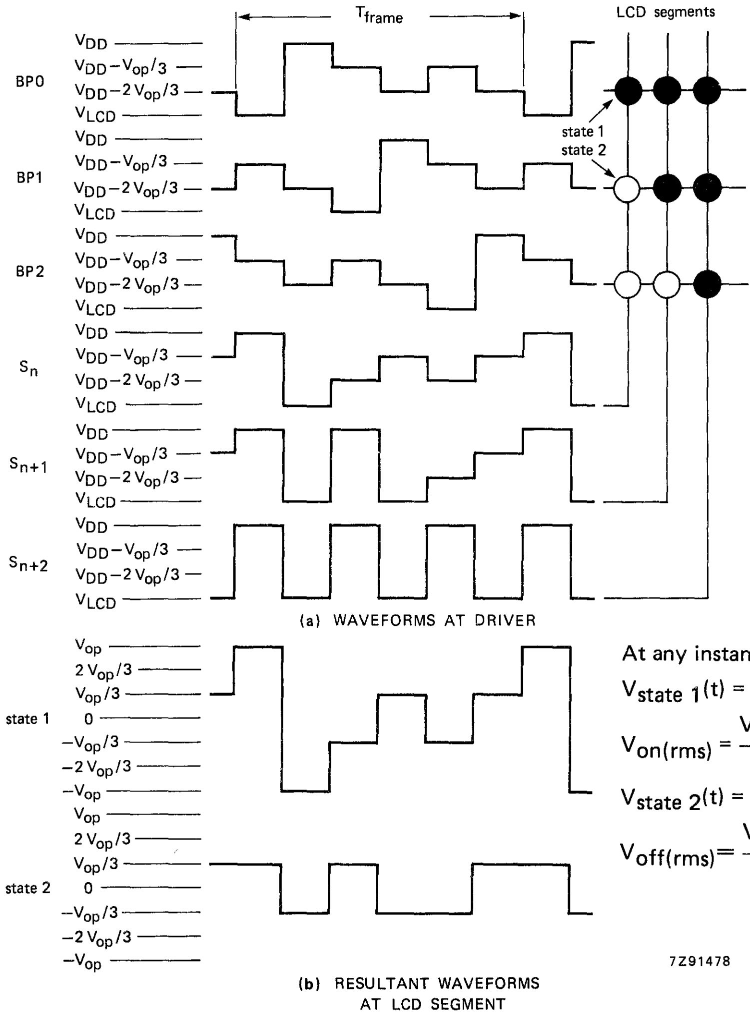
$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = \frac{V_{op}}{3} = 0{,}333 V_{op}$

7Z91466

Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.



At any instant (t):

$$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$$

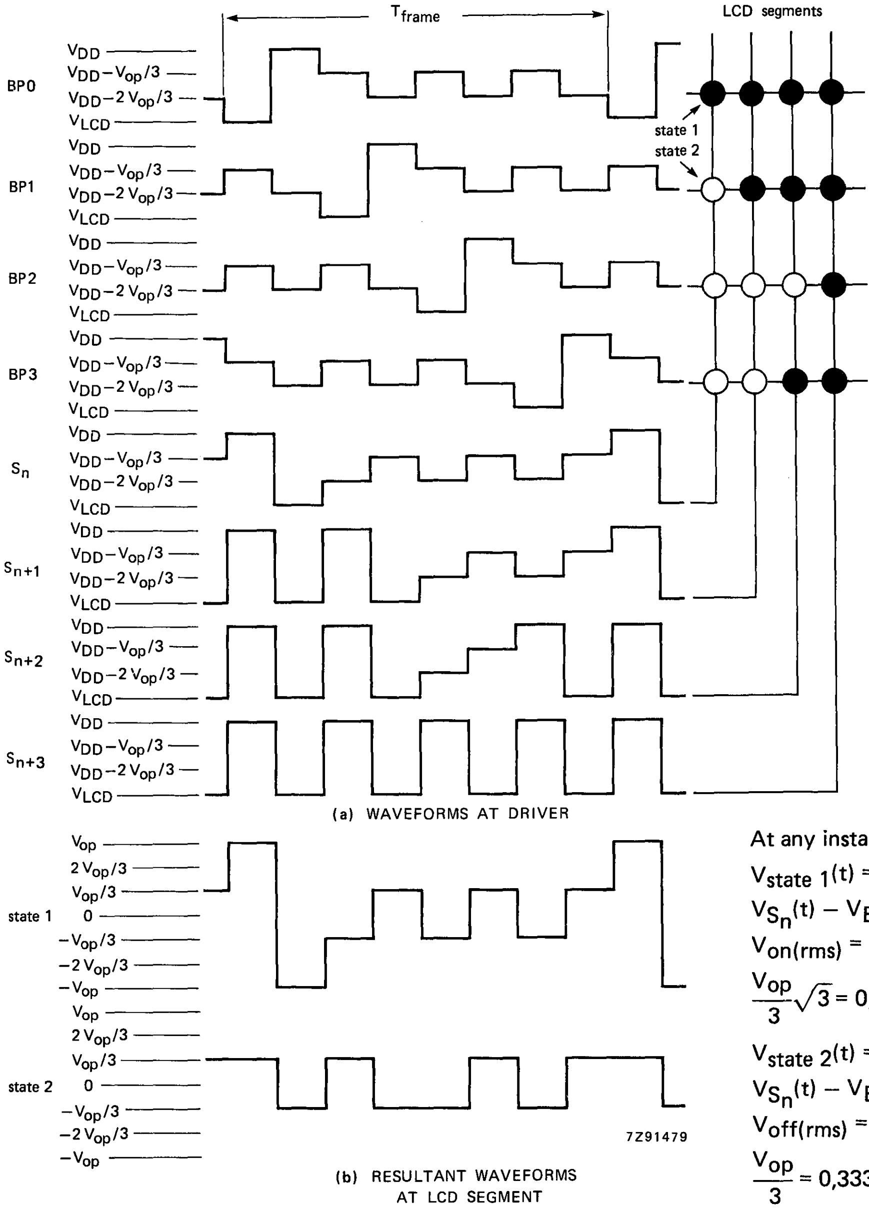
$$V_{on(rms)} = \frac{V_{op}}{9}\sqrt{33} = 0{,}638V_{op}$$

$$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$$

$$V_{off(rms)} = \frac{V_{op}}{3} = 0{,}333V_{op}$$

Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = \frac{V_{op}}{3}\sqrt{3} = 0{,}577V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = \frac{V_{op}}{3} = 0{,}333V_{op}$

Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

DEVELOPMENT DATA

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed back-plane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multi-plex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

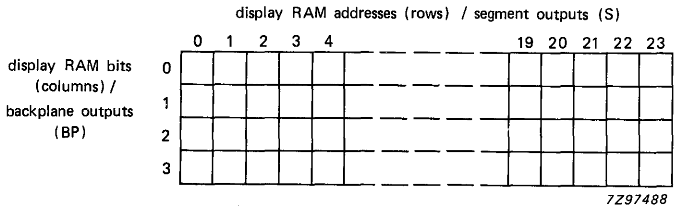


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

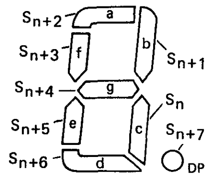
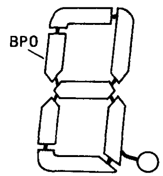
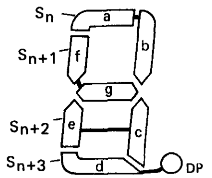
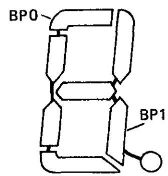
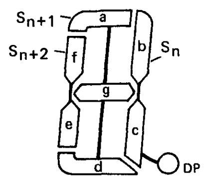
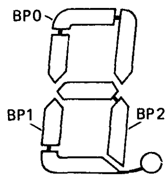
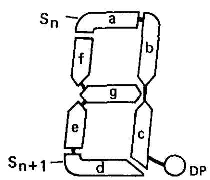
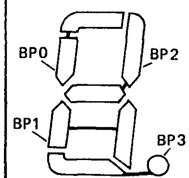
Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte (msb … lsb)
static			see table below	c b a f g e d DP
1 : 2 multiplex			see table below	a b f g e c d DP
1 : 3 multiplex			see table below	b DP c a d g f e
1 : 4 multiplex			see table below	a c b DP f e g d

Display RAM filling order — static:

bit/BP	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

Display RAM filling order — 1 : 2 multiplex:

bit/BP	n	n + 1	n + 2	n + 3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

Display RAM filling order — 1 : 3 multiplex:

bit/BP	n	n + 1	n + 2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

Display RAM filling order — 1 : 4 multiplex:

bit/BP	n	n + 1
0	a	f
1	c	e
2	b	g
3	DP	d

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

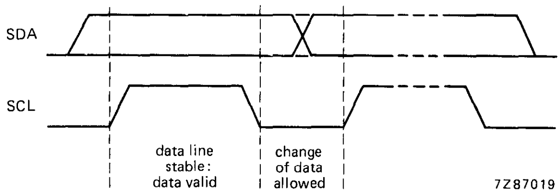


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

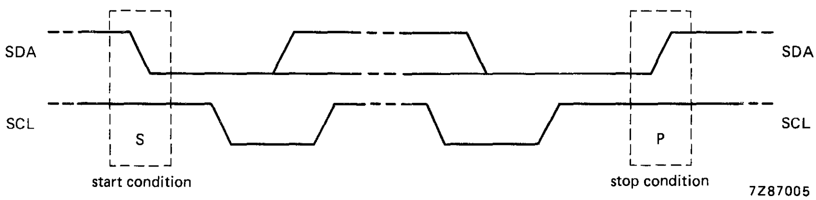


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

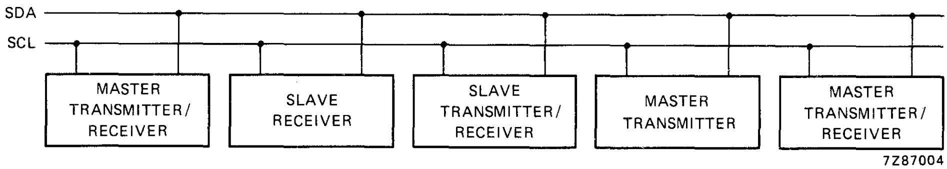


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

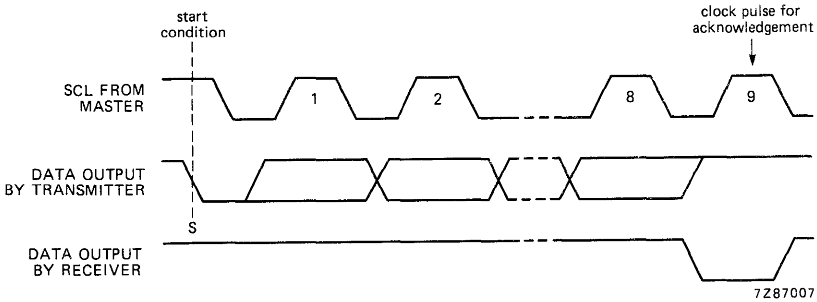


Fig. 14 Acknowledgement on the I²C bus.

PCF8566 I^2C bus controller

The PCF8566 acts as an I^2C slave receiver. It does not initiate I^2C bus transfers or transmit data to an I^2C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I^2C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I^2C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I^2C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I^2C bus protocol

Two I^2C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I^2C bus which allows:

(a) up to 16 PCF8566s on the same I^2C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I^2C bus.

The I^2C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I^2C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I^2C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I^2C bus master issues a stop condition (P).

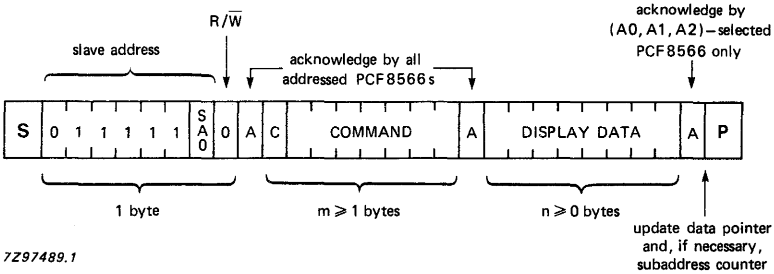


Fig. 15 I^2C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

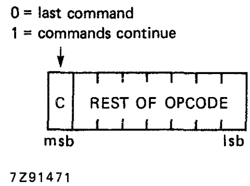


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options		description
MODE SET	LCD drive mode	bits M1 M0	Defines LCD drive mode
C 1 0 LP E B M1 M0	static (1 BP)	0 1	
	1 : 2 MUX (2 BP)	1 0	
	1 : 3 MUX (3 BP)	1 1	
	1 : 4 MUX (4 BP)	0 0	
	LCD bias	bit B	Defines LCD bias configuration
	1/3 bias	0	
	1/2 bias	1	
	display status	bit E	Defines display status The possibility to disable the display allows implementation of blinking under external control
	disabled (blank)	0	
	enabled	1	
	mode	bit LP	Defines power dissipation mode
	normal mode	0	
	power-saving mode	1	
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23		Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7		Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

command/opcode	options			description
BANK SELECT	static	1 : 2 MUX	bit I	Defines input bank selection (storage of arriving display data)
C 1 1 1 1 0 I O	RAM bit 0	RAM bits 0, 1	0	
	RAM bit 2	RAM bits 2, 3	1	
	static	1 : 2 MUX	bit O	Defines output bank selection (retrieval of LCD display data)
	RAM bit 0	RAM bits 0, 1	0	
	RAM bit 2	RAM bits 2, 3	1	
				The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK	blink frequency	bits BF1	BF0	Defines the blinking frequency
C 1 1 1 0 A BF1 BF0	off	0	0	
	2 Hz	0	1	
	1 Hz	1	0	
	0,5 Hz	1	1	
	blink mode		bit A	Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes
	normal blinking		0	
	alternation blinking		1	

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

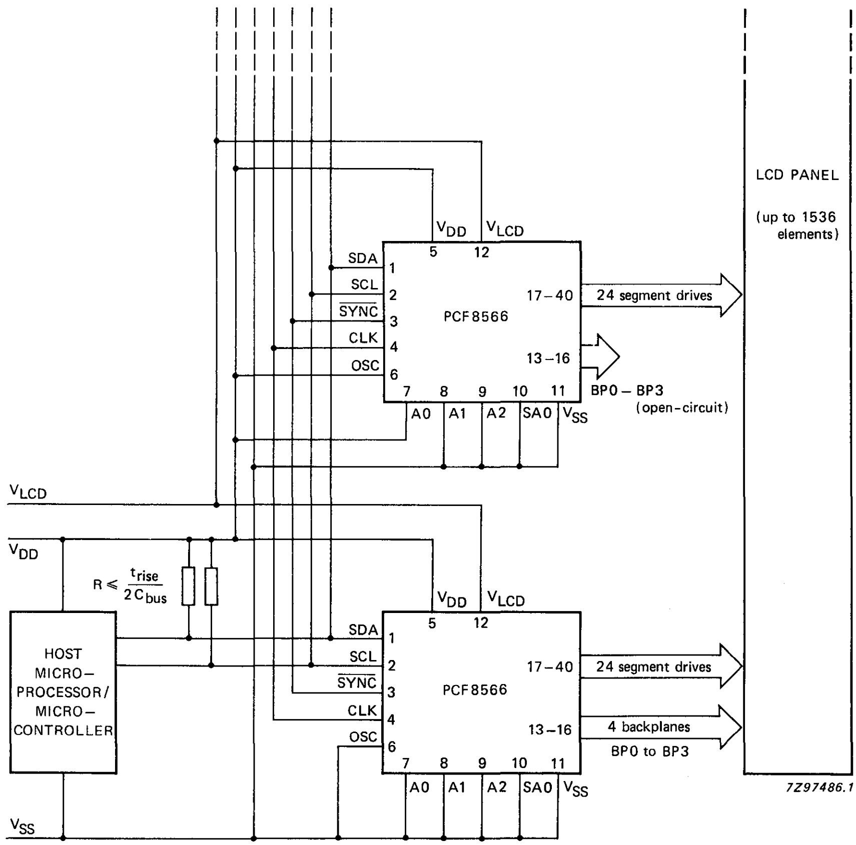


Fig. 17 Cascaded PCF8566 configuration.

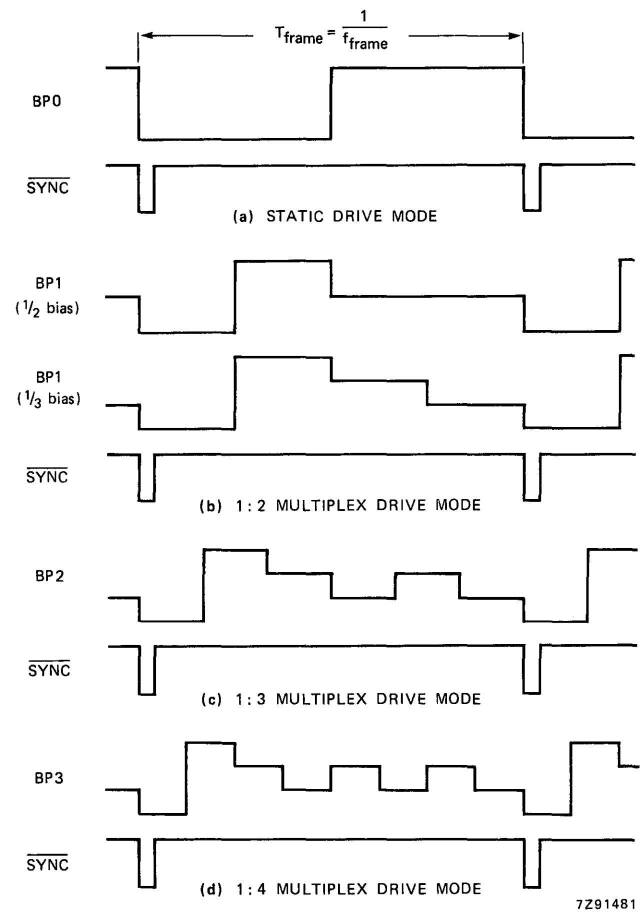


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		$-0,5$ to $+7$ V
LCD supply voltage range	V_{LCD}		$V_{DD}-7$ to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{\text{SYNC}}$; SA0)	V_I		$V_{SS}-0,5$ to $V_{DD}+0,5$ V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		$V_{LCD}-0,5$ to $V_{DD}+0,5$ V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		-65 to $+150$ ^oC

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

$V_{SS} = 0$ V; $V_{DD} = 2,5$ to 6 V; $V_{LCD} = V_{DD} -2,5$ to $V_{DD} -6$ V;
$T_{amb} = -40$ to $+85$ ^oC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	$V_{DD}-6$	–	$V_{DD}-2,5$	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} −0,05	–	–	V
Output current LOW (CLK, $\overline{\text{SYNC}}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at V_I = V_{SS} or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{\text{SYNC}}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at V_{LCD} = V_{DD} −5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at V_{LCD} = V_{DD} −5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{\text{SYNC}}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{\text{SYNC}}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I^2C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;\,STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;\,STA}$	4,7	–	–	μs
Data hold time	$t_{HD;\,DAT}$	0	–	–	μs
Data set-up time	$t_{SU;\,DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;\,STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I^2C bus maximum transmission speed is derated.

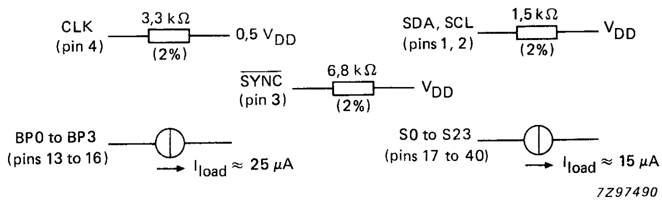


Fig. 19 Test loads.

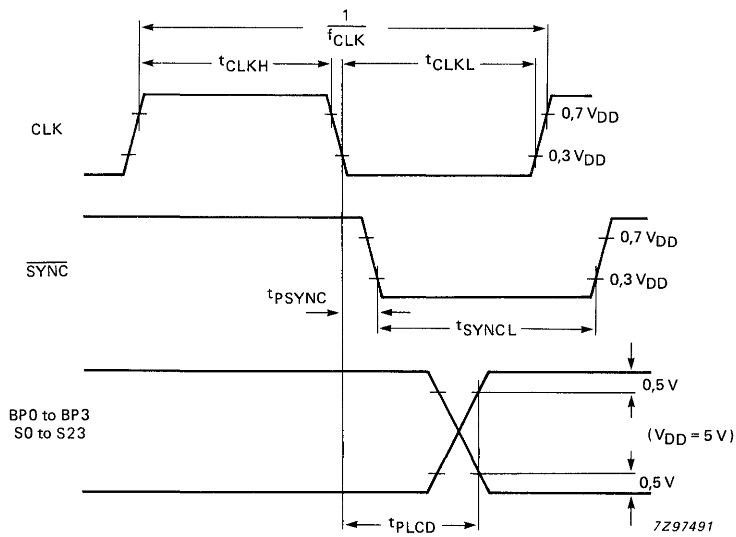


Fig. 20 Driver timing waveforms.

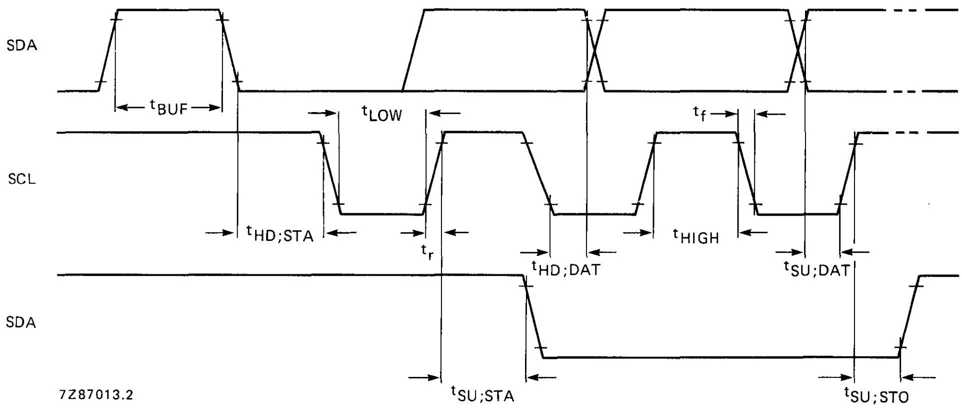
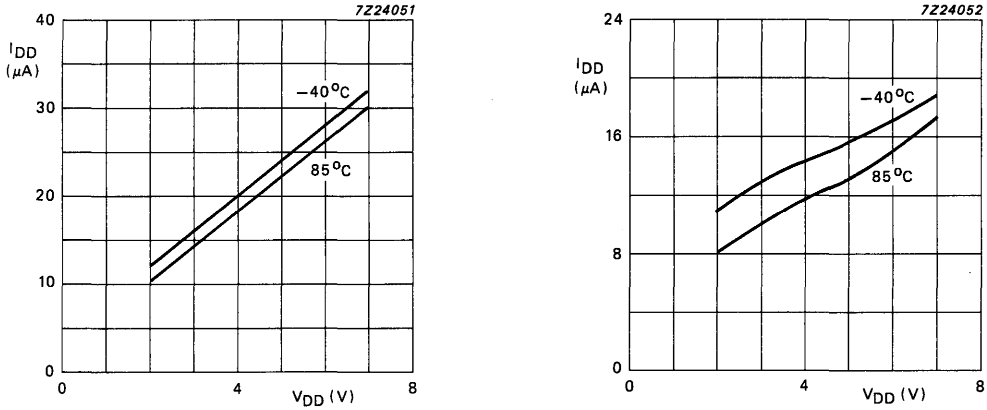


Fig. 21 I^2C bus timing waveforms.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

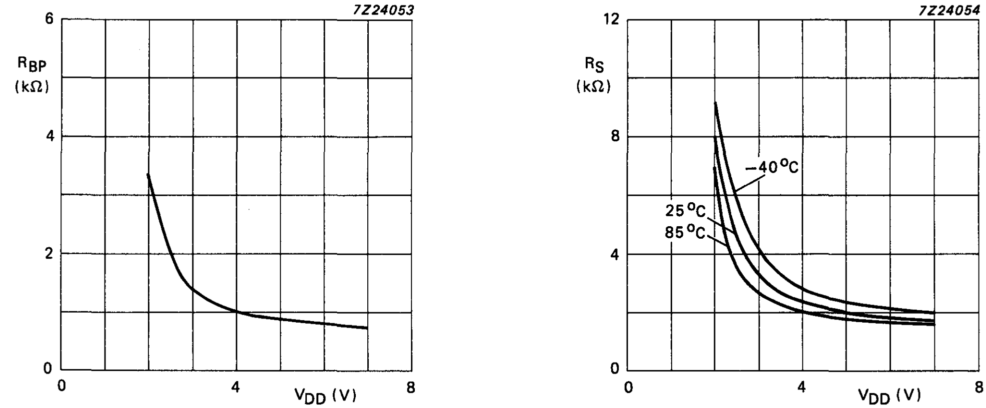


(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.

(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.

(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

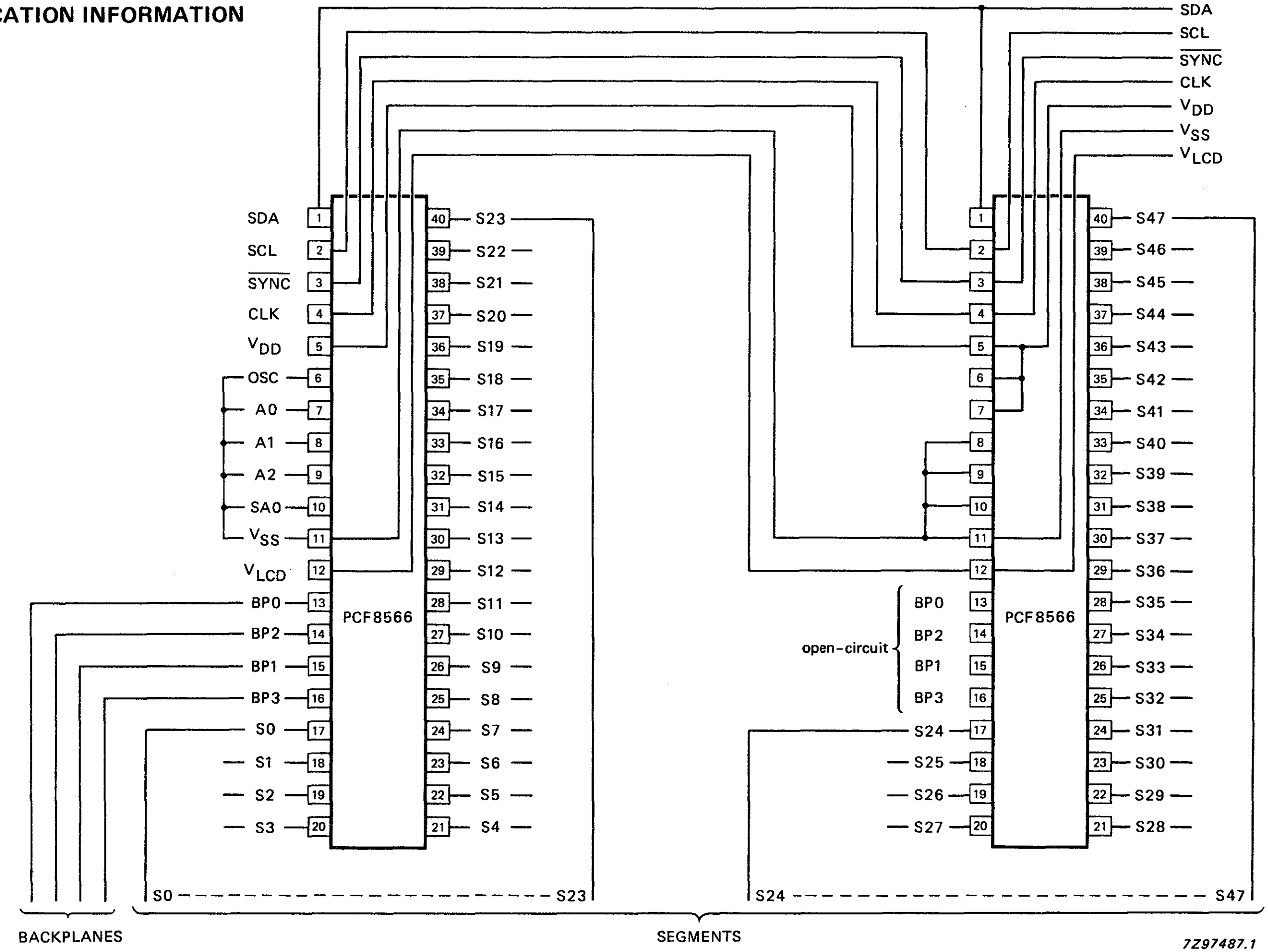


Fig. 24 Single plane wiring of packaged PCF8566s.

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data arė transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

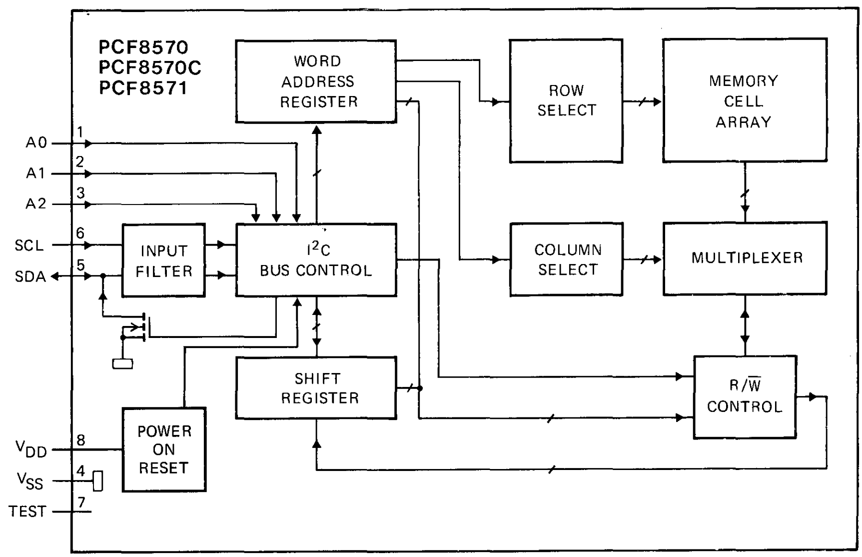


Fig.1 Block diagram.

7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C-bus
6	SCL	serial clock line } I^2C-bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

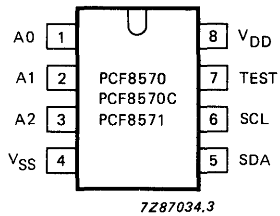


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	−	10	mA
DC output current	$\pm I_O$	−	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	50	mA
Total power dissipation	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	$V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby	f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
	T_{amb} = −25 to +70 °C	I_{DDO}	–	–	5	μA
Power-on reset level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs, input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	0.3 V_{DD}	V
Input voltage HIGH	note 2	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\lvert I_{LI} \rvert$	–	–	1	μA
Inputs A0 to A2; TEST						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	250	nA
Inputs SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current	V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	I_{DDR}	–	–	2	μA
Power saving mode	see Figs 12 and 13					
Supply current	TEST = V_{DD}; T_{amb} = 25 °C					
PCF8570/PCF8570C		I_{DDR}	–	50	400	nA
PCF8571		I_{DDR}	–	50	200	nA
Recovery time		t_{HD2}	–	50	–	μs

Notes to the characteristics

1. The power-on reset circuit resets the I^2C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0.5 mA.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

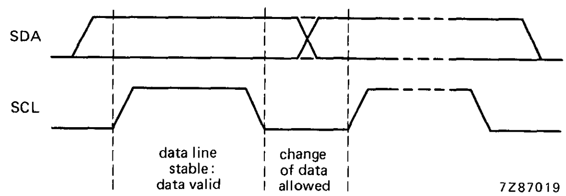


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

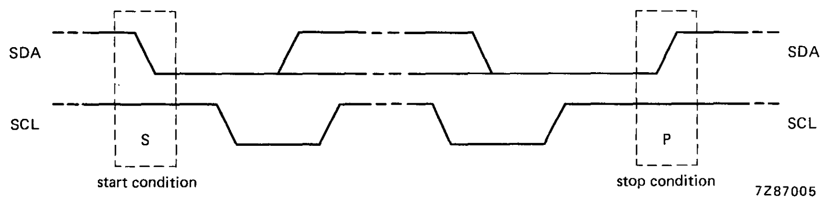


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

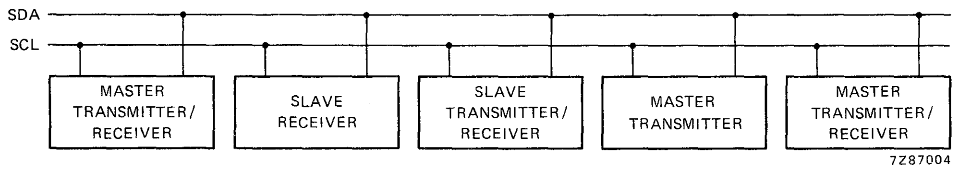


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

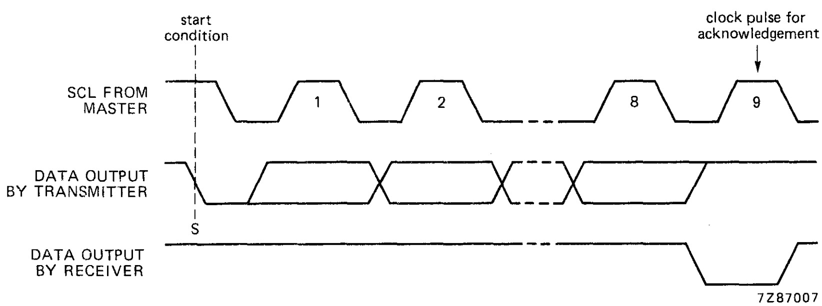


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

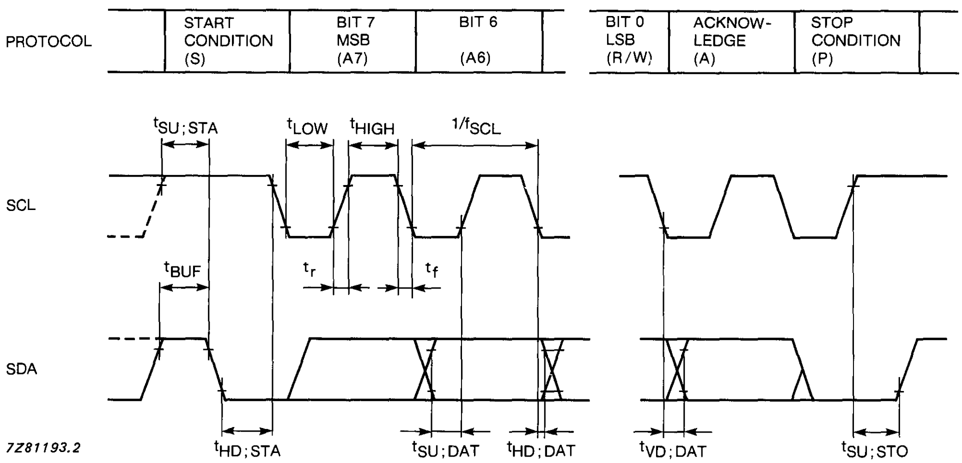


Fig.7 I^2C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig.8.

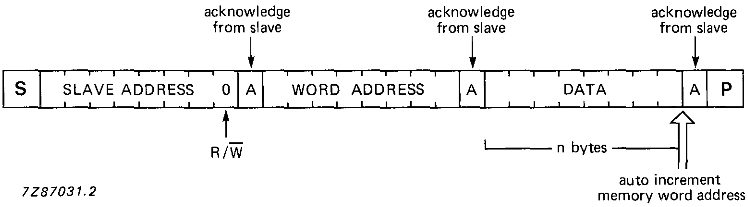


Fig.8(a) Master transmits to slave receiver (WRITE mode).

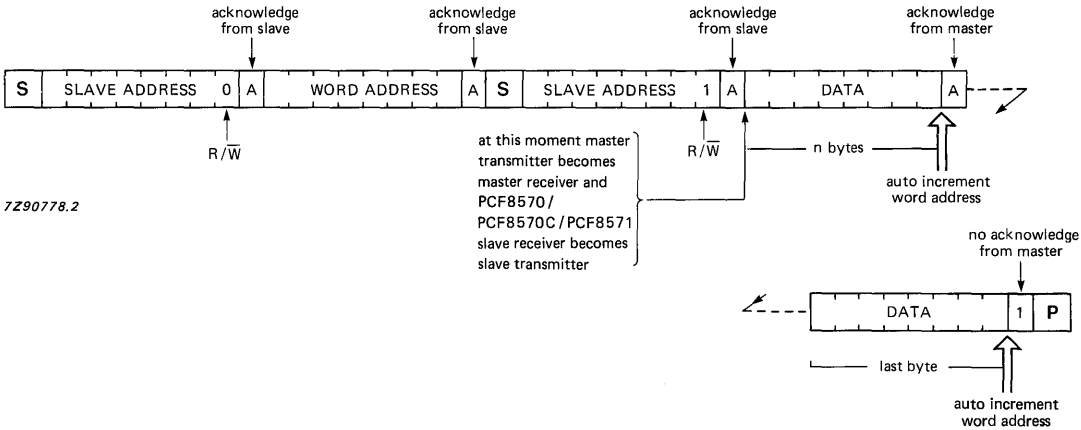


Fig.8(b) Master reads after setting word address (WRITE word address; READ data).

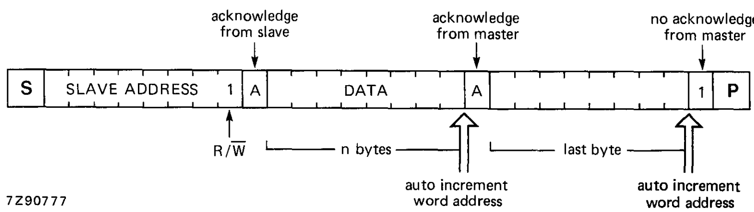


Fig.8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig.9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig.10).

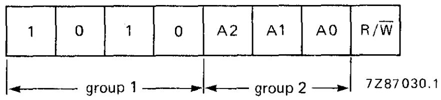


Fig.9 PCF8570 and PCF8571 address.

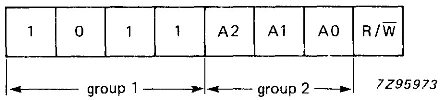
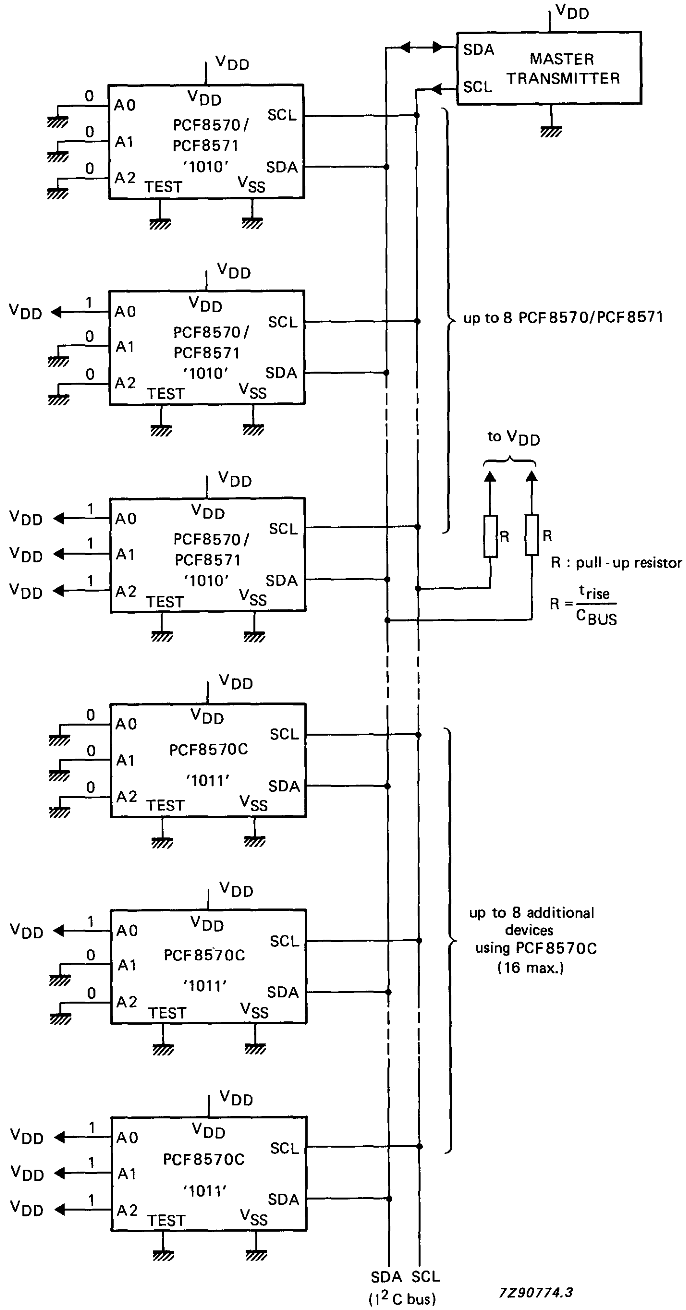


Fig.10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

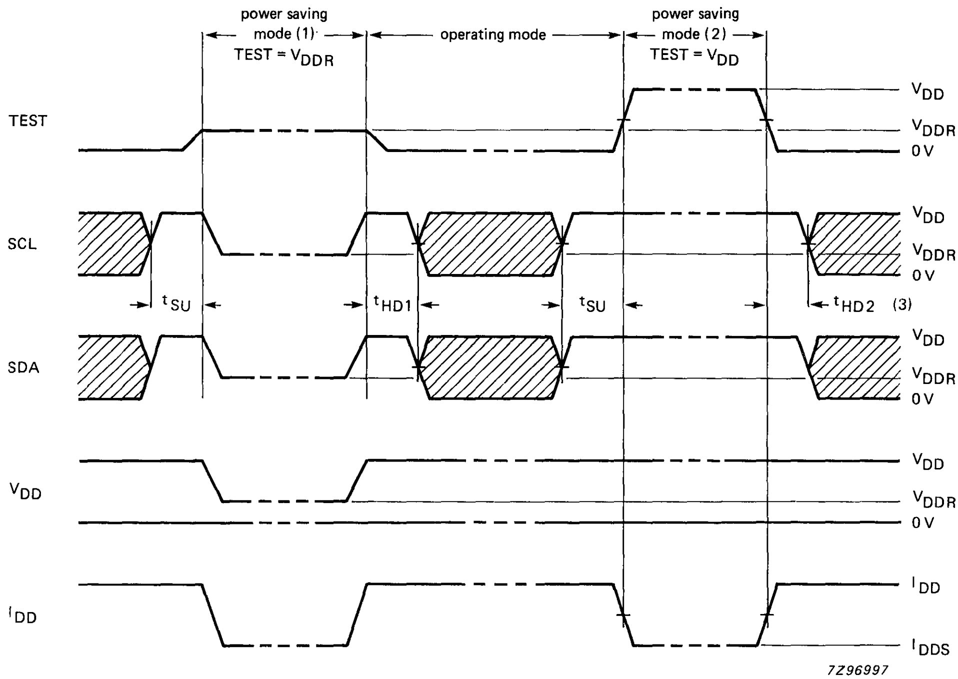


It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.11 Application diagram.

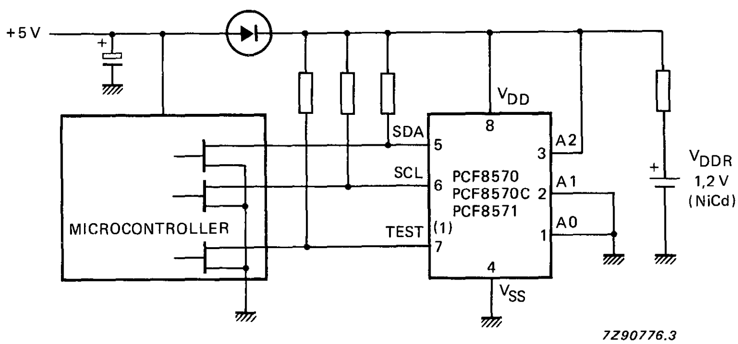
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4$ µs and $t_{HD2} \geqslant 50$ µs.

Fig.12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

It is recommended that a 4.7 µF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

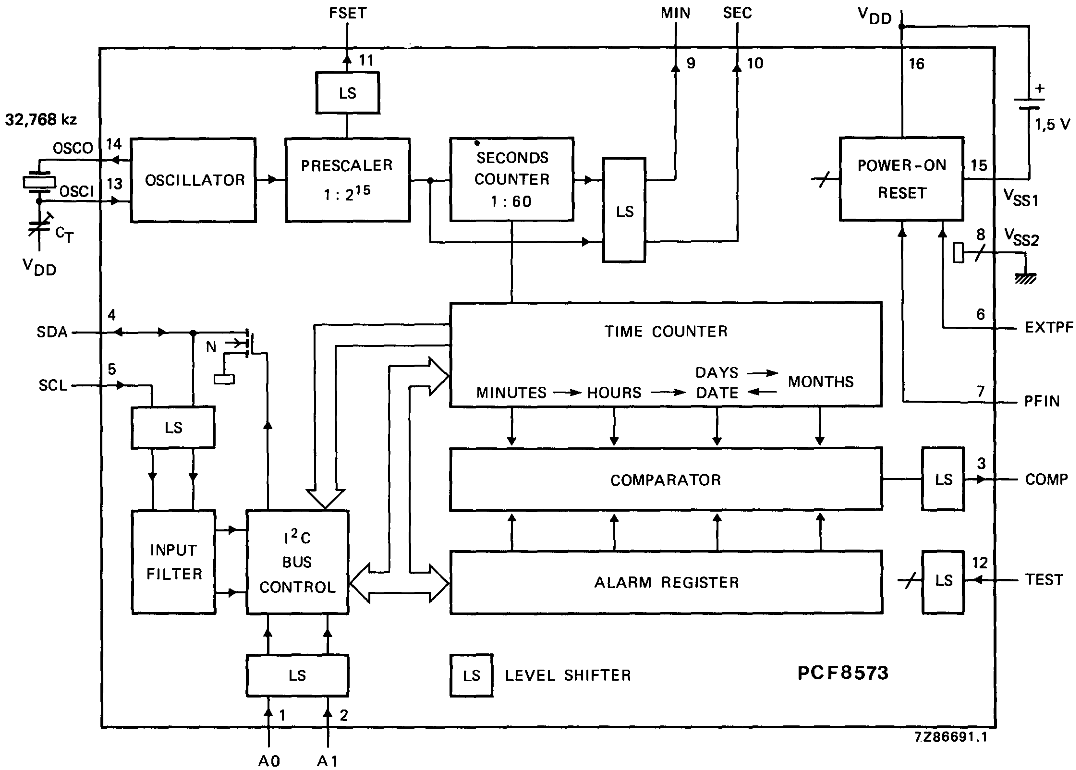


Fig.1 Block diagram.

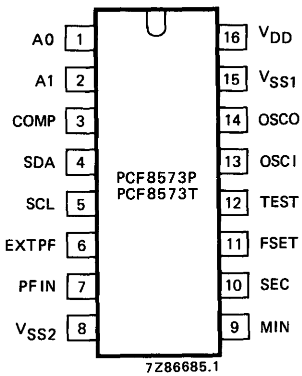


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line } I^2C-bus
5	SCL	serial clock line } I^2C-bus
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with $(V_{DD}-V_{SS1})$ greater than V_{TH1}, or by an externally generated power fail signal for application with $(V_{DD}-V_{SS1})$ less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage $(V_{DD}-V_{SS2})$ of the microcontroller to the internal supply voltage $(V_{DD}-V_{SS1})$ of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I^{2}C-BUS

The I^2 C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

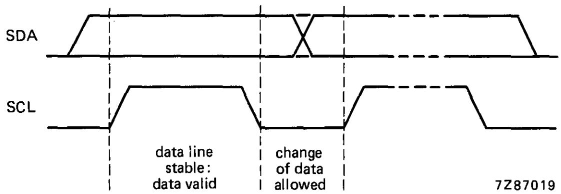


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

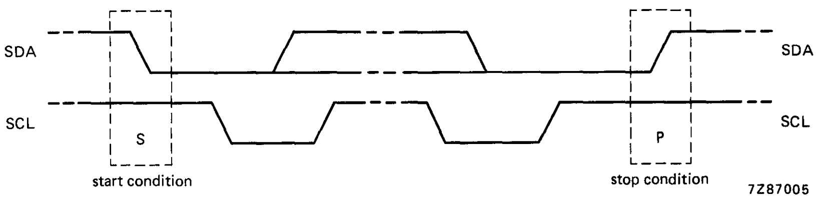


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

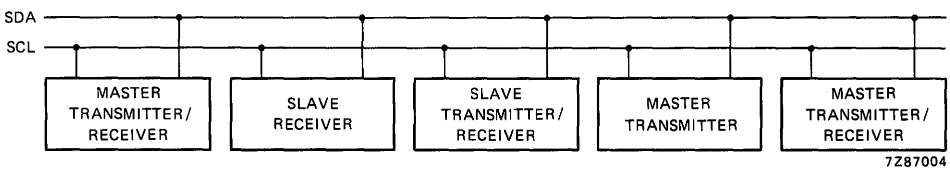


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

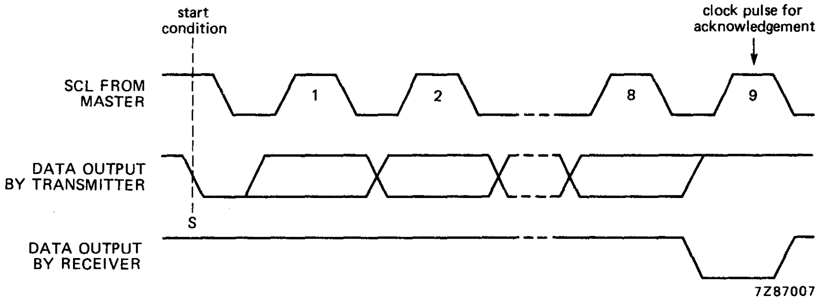


Fig.6 Acknowledgement on the I^2C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;\,STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;\,STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;\,DAT}$	250	–	–	ns
Data hold time	$t_{HD;\,DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;\,DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;\,STO}$	4.0	–	–	μs

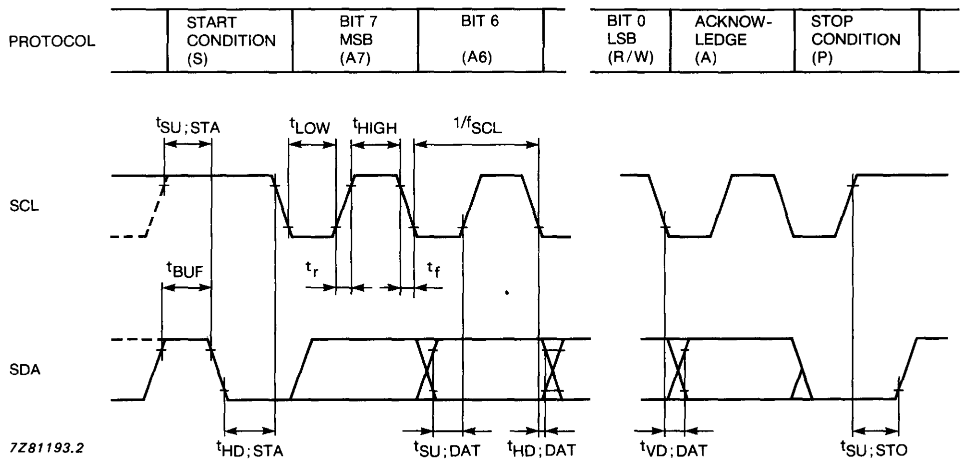


Fig.7 I²C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

MSB							LSB
1	1	0	1	0	A1	A0	R/$\overline{W}$

7Z86686

Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

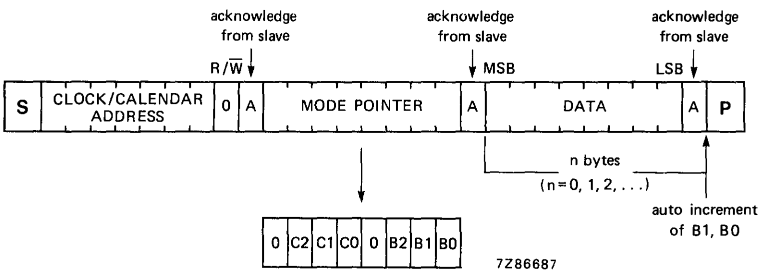


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB			DATA				LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

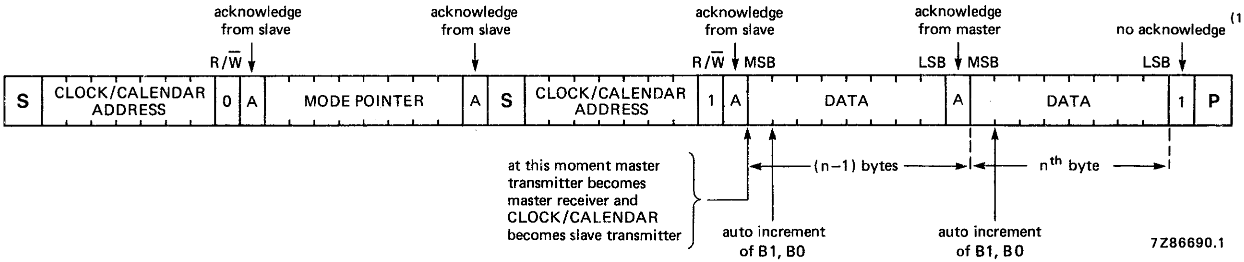
MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit

* = minutes

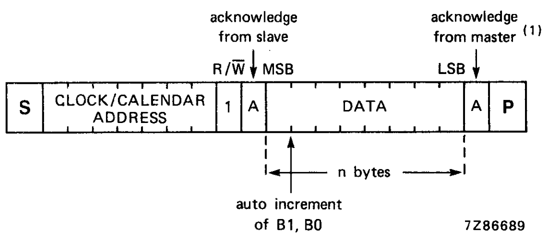
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	−	10	mA
Output current		I_O	−	10	mA
Power dissipation per output		P_O	−	100	mW
Total power dissipation		P_{tot}	−	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I^2C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geq$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_{LI}\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	1.0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	$I_O = 3$ mA; $V_{DD}-V_{SS2} = 2.5$ to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2} = 6$ V; $V_O = 6$ V	$\|I_L\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2} = 2.5$ V; $I_O = 0.3$ mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2} = 4$ to 6 V; $I_O = 1.6$ mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2} = 2.5$ V; $-I_O = 0.1$ mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2} = 4$ to 6 V; $-I_O = 0.5$ mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

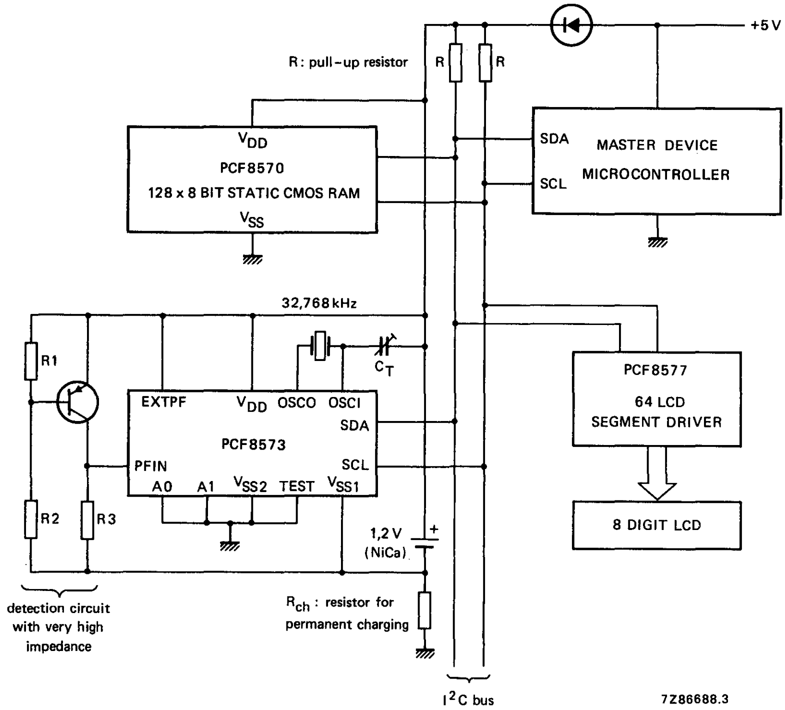


Fig.12 Application example of the PCF8573 clock/calendar.

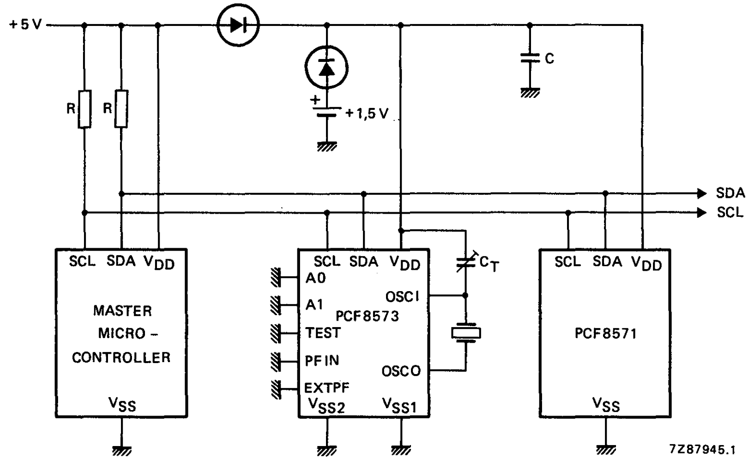


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

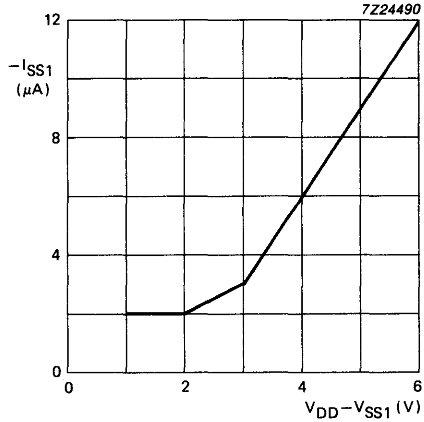


Fig.14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at T_{amb} = −40 to +85 °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

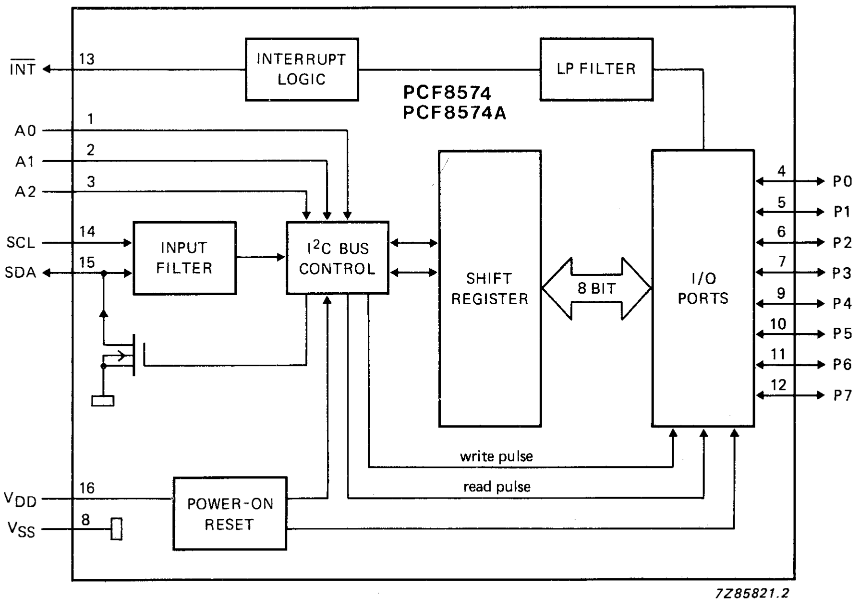


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

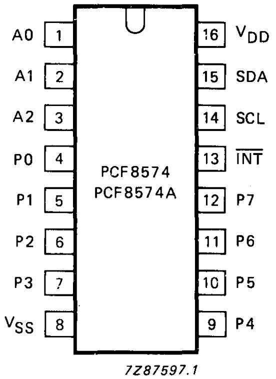


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7	P0 to P3	8-bit quasi-bidirectional I/O port
9 to 12	P4 to P7	
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

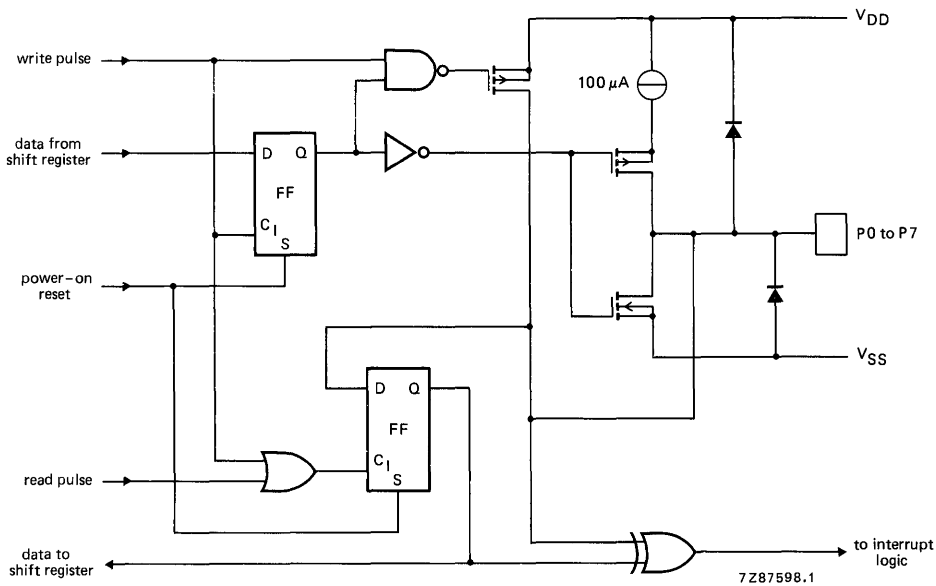


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I^2C-BUS

The I^2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

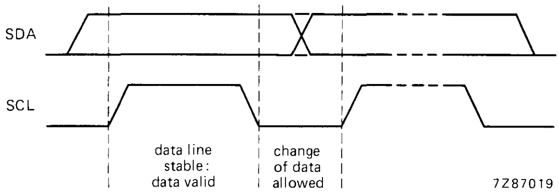


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

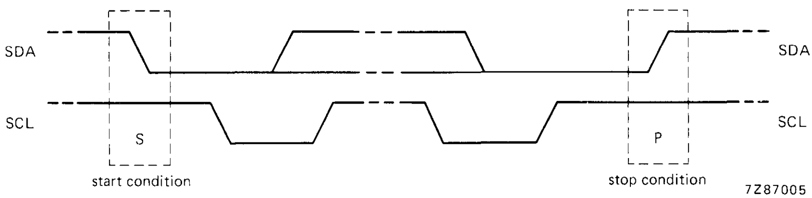


Fig.5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

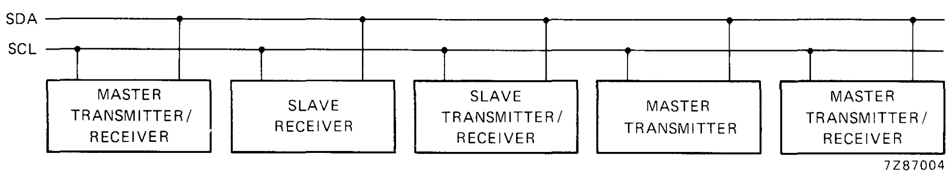


Fig.6 System configuration.

CHARACTERISTICS OF THE I²C-BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

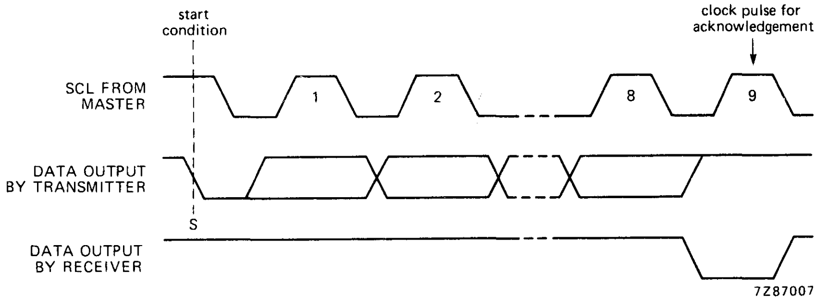


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

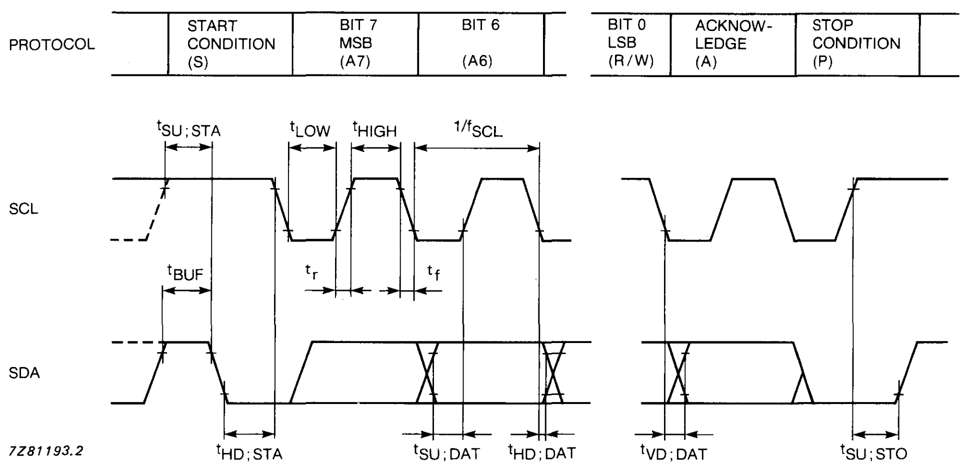
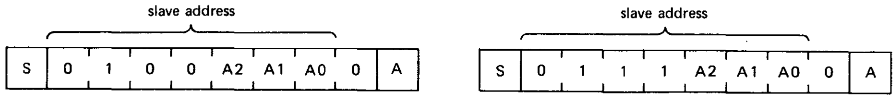


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574. (b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

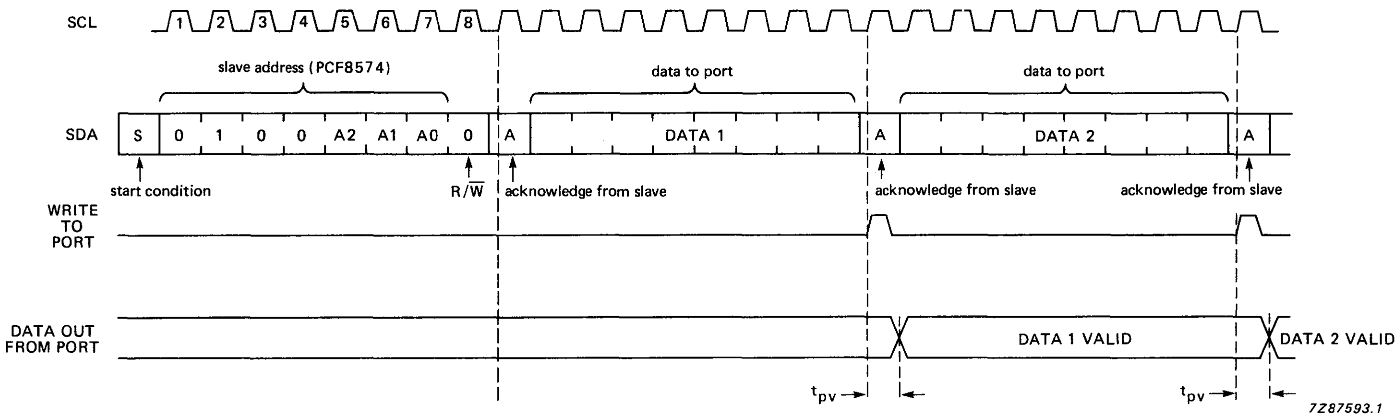


Fig.10 WRITE mode (output port).

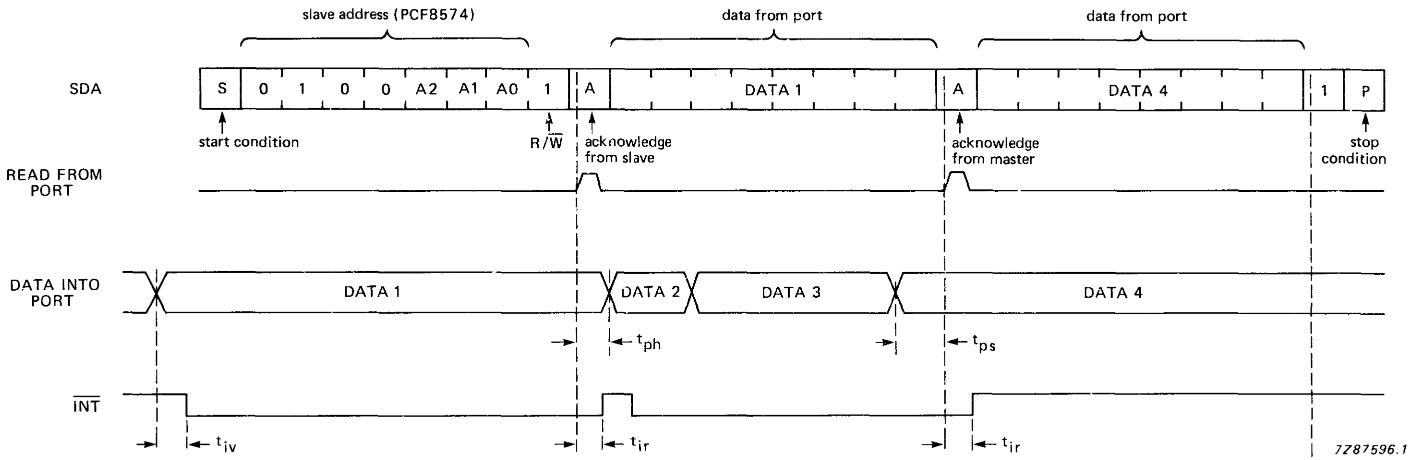


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

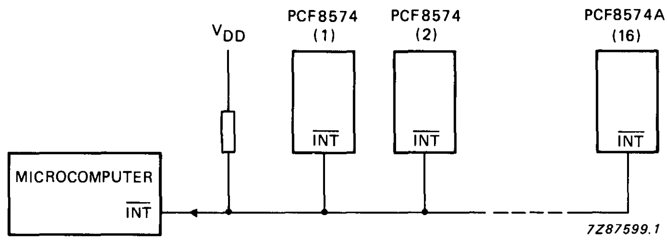


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

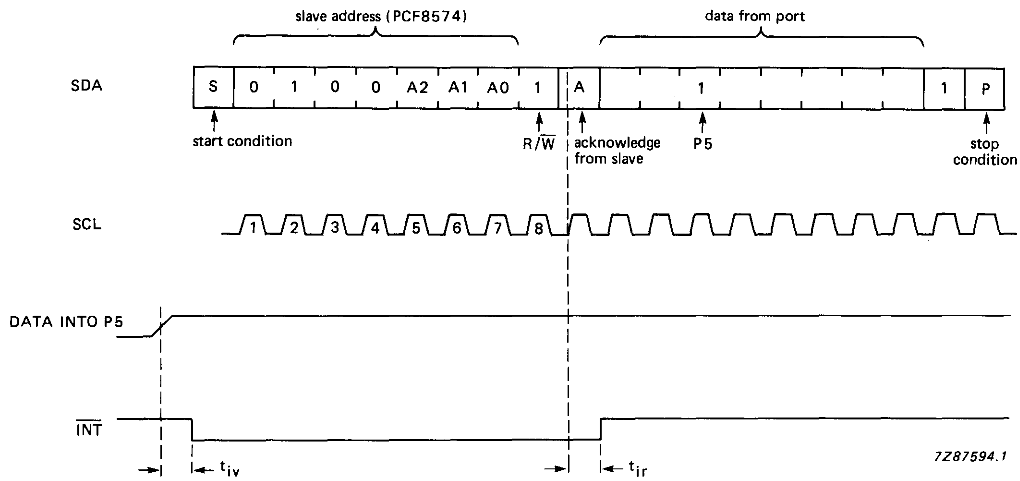


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

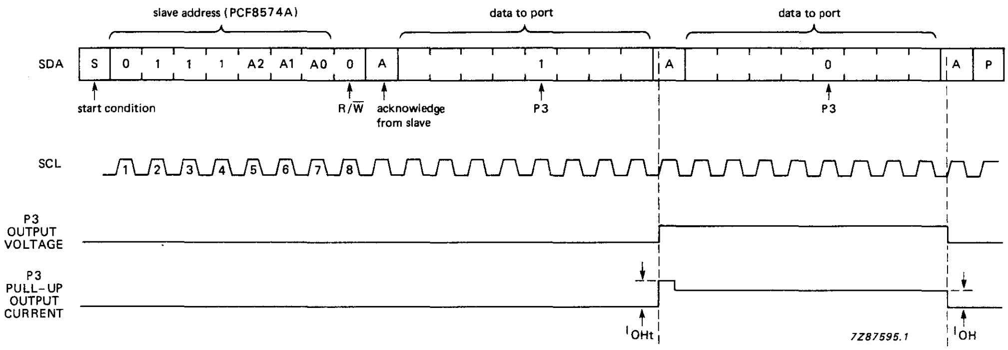


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	−	20	mA
DC output current	$\pm I_O$	−	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	100	mA
Total power dissipation	P_{tot}	−	400	mW
Power dissipation per output	P_O	−	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

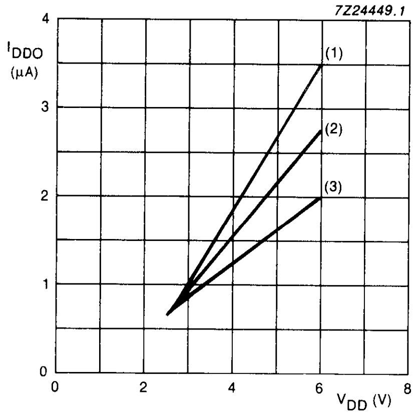
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\lvert I_{LI} \rvert$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L = \leqslant 100$ pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	$V_{OL} = 0.4$ V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L = \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	–0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_{LI}\|$	–	–	250	nA

Note to the characteristics

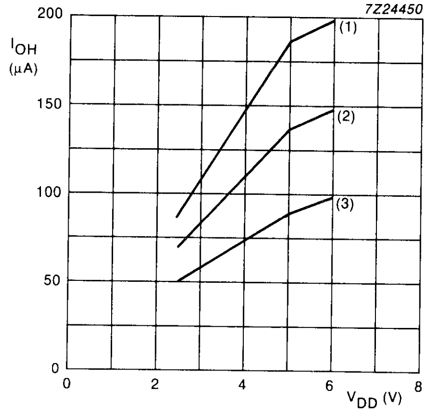
1. The power-on reset circuit resets the I^2C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.



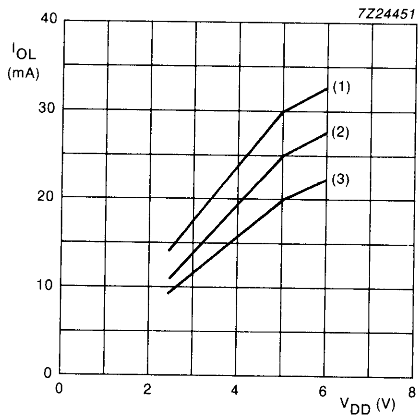
(1) T_{amb} = –40 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 85 °C

Fig.15 Typical standby current (I_{DDO}) as a function of supply voltage (V_{DD}).



(1) T_{amb} = –40 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 85 °C

Fig.16 Typical port output current HIGH (I_{OH}) as a function of supply voltage (V_{DD}); $V_{OH} = V_{SS}$.



(1) T_{amb} = –40 °C
(2) T_{amb} = + 25 °C
(3) T_{amb} = + 85 °C

Fig.17 Typical port output current LOW (I_{OL}) as a function of supply voltage (V_{DD}); V_{OL} = 1 V.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^{2}C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^{2}C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C-system provided the system conforms to the I^{2}C specifications defined by Philips.

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

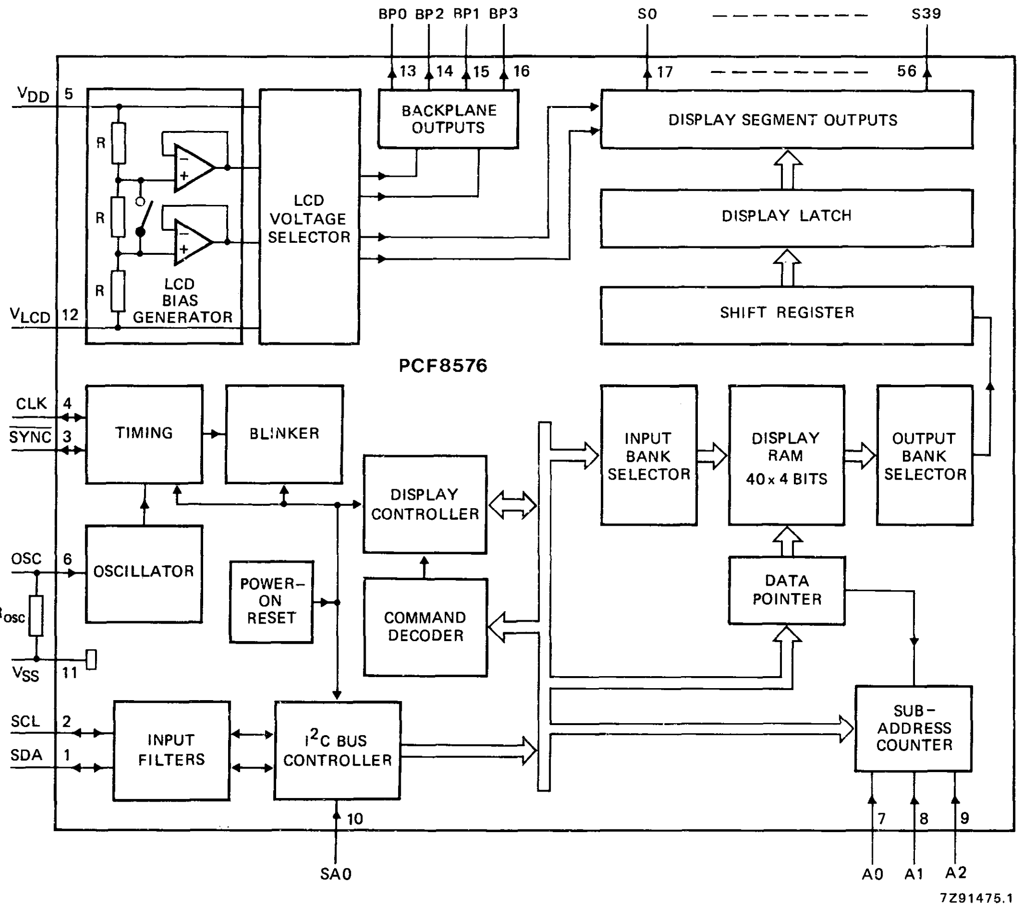


Fig. 1 Block diagram.

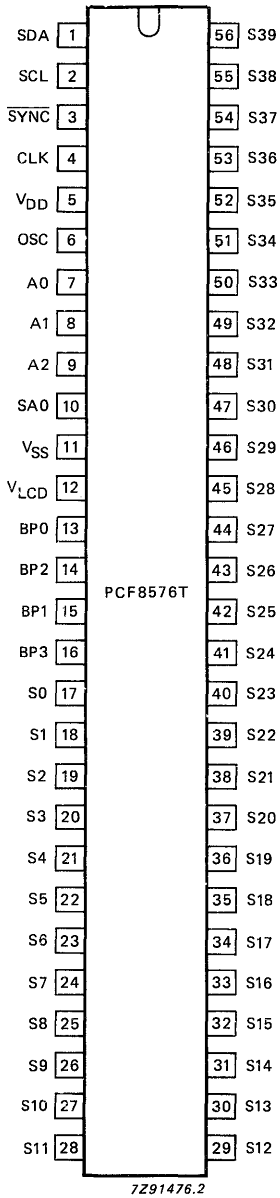


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C-bus data input/output
2	SCL	I^2C-bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C-bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C-bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.3. The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

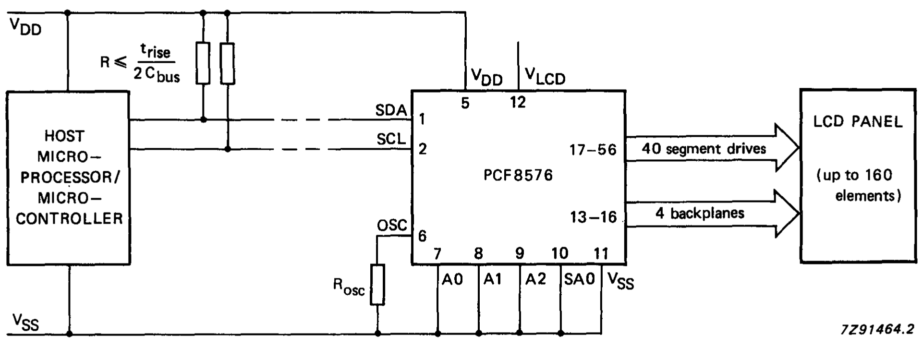


Fig.3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off\,(rms)}}{V_{op}}$	$\frac{V_{on\,(rms)}}{V_{op}}$	$D = \frac{V_{on\,(rms)}}{V_{off\,(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0.354$	$\sqrt{10}/4 = 0.791$	$\sqrt{5} = 2.236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	1/3 = 0.333	$\sqrt{5}/3 = 0.745$	$\sqrt{5} = 2.236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	1/3 = 0.333	$\sqrt{33}/9 = 0.638$	$\sqrt{33}/3 = 1.915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	1/3 = 0.333	$\sqrt{3}/3 = 0.577$	$\sqrt{3} = 1.732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off\,(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1.732 for 1: 3 multiplex or $\sqrt{21}/3$ = 1.528 for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

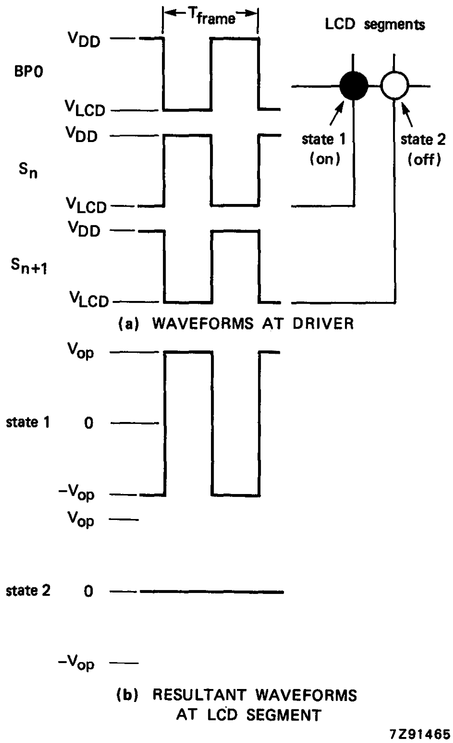
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off\,(rms)} = 2.449\ V_{off\,(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off\,(rms)} = 2.309\ V_{off\,(rms)}$

These compare with $V_{op} = 3\ V_{off\,(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

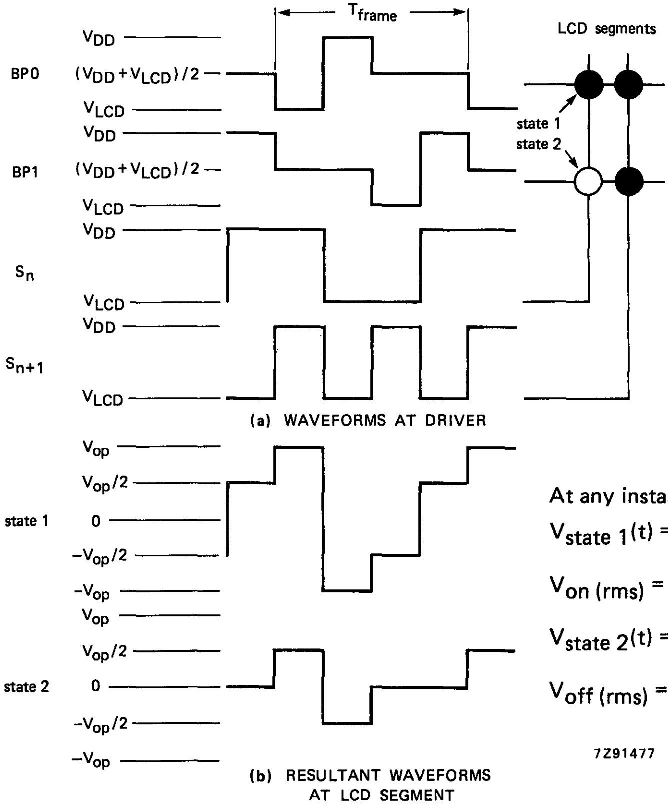
$V_{on\,(rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off\,(rms)} = 0\ V$

Fig.4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.



At any instant (t):

$$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$$

$$V_{on\ (rms)} = \frac{V_{op}}{4}\sqrt{10} = 0.791\ V_{op}$$

$$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$$

$$V_{off\ (rms)} = \frac{V_{op}}{4}\sqrt{2} = 0.354\ V_{op}$$

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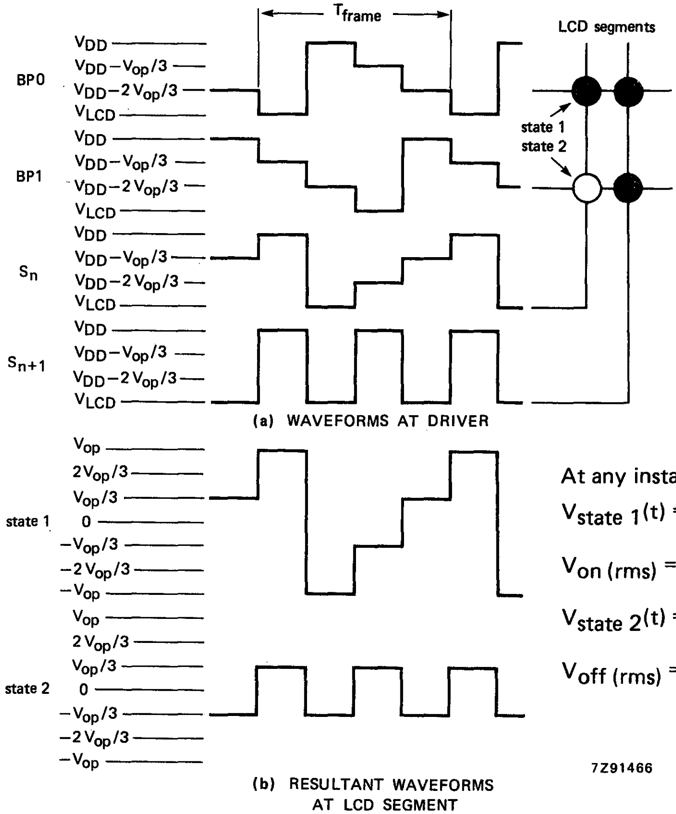
Fig.5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$$

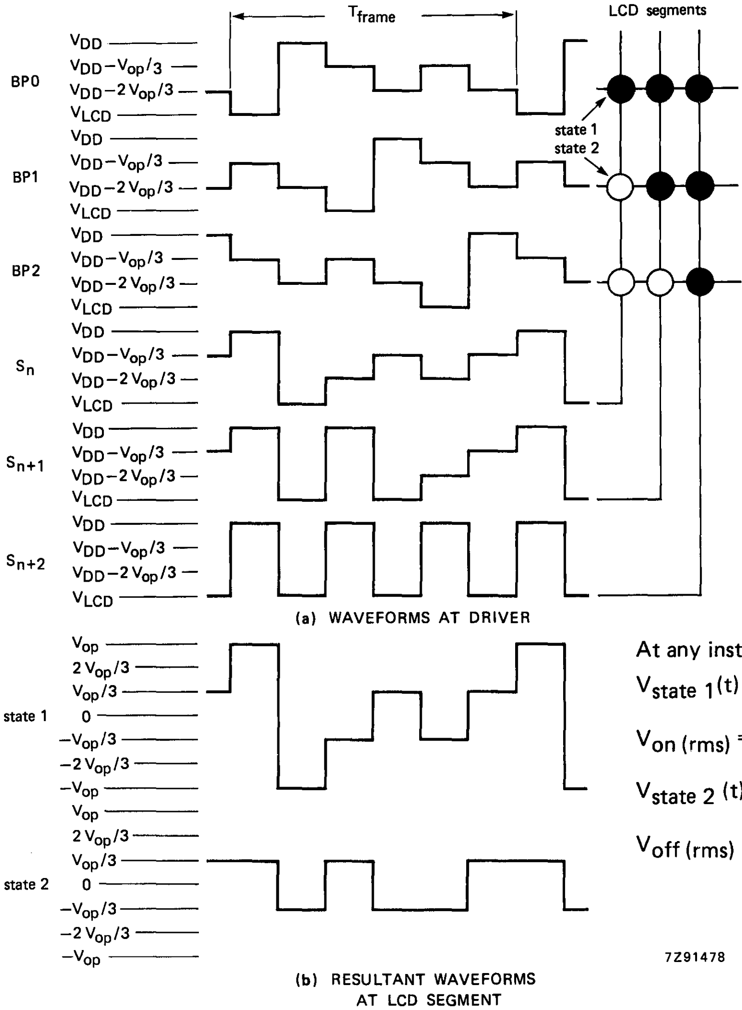
$$V_{on\ (rms)} = \frac{V_{op}}{3}\sqrt{5} = 0.745\ V_{op}$$

$$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$$

$$V_{off\ (rms)} = \frac{V_{op}}{3} = 0.333\ V_{op}$$

Fig.6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

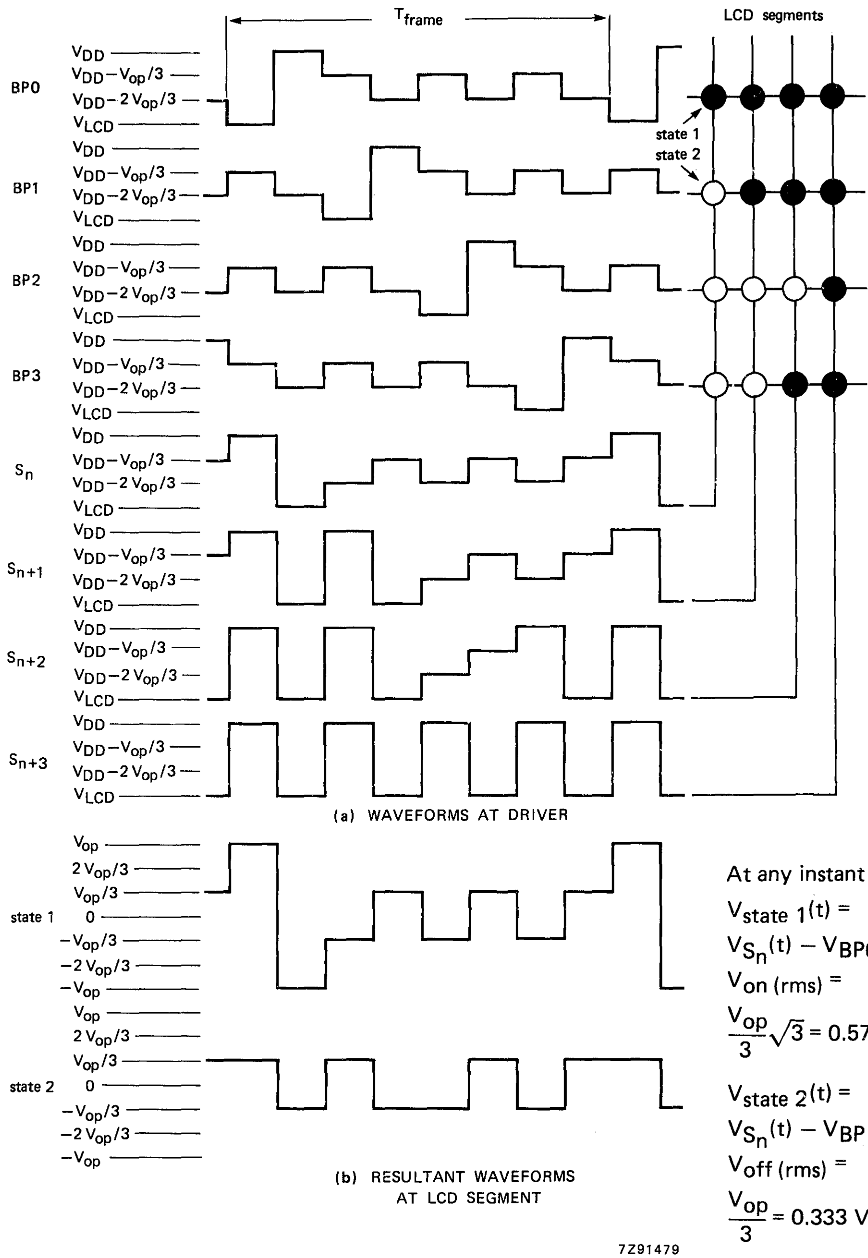
$V_{on\ (rms)} = \frac{V_{op}}{9}\sqrt{33} = 0.638\ V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off\ (rms)} = \frac{V_{op}}{3} = 0.333\ V_{op}$

Fig.7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on\ (rms)} = \frac{V_{op}}{3}\sqrt{3} = 0.577\ V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off\ (rms)} = \frac{V_{op}}{3} = 0.333\ V_{op}$

Fig.8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig.9. In this application, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

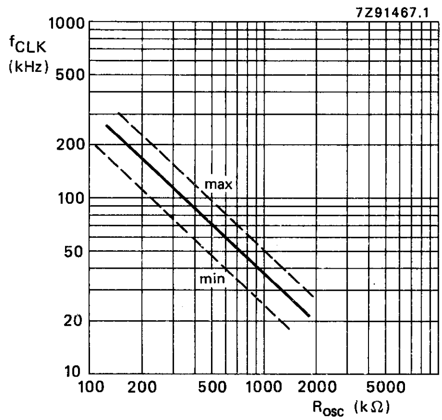


Fig.9 Oscillator frequency as a function of R_{OSC}: $f_{CLK} \approx (3.4 \times 10^7/R_{OSC})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C-bus. To allow I²C-bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{\text{SYNC}}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{OSC} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{OSC} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1.2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C-bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C-bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

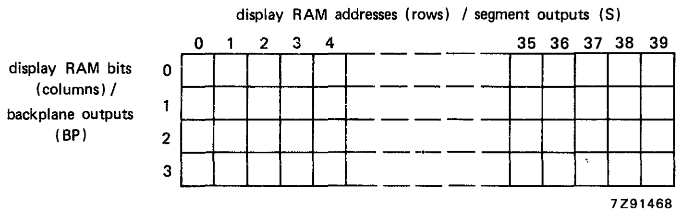


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

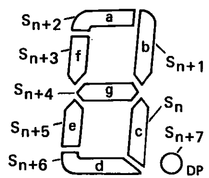
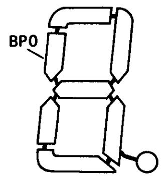
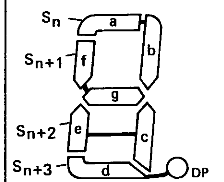
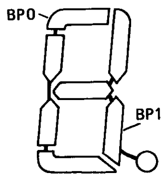
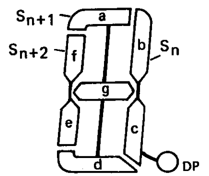
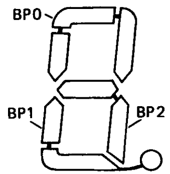
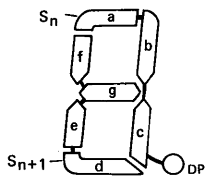
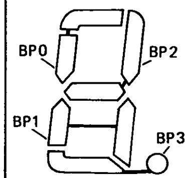
<table>
<tr><th>drive mode</th><th>LCD segments</th><th>LCD backplanes</th><th>display RAM filling order</th><th>transmitted display byte</th></tr>
<tr><td>static</td><td>
</td><td>
</td><td><table>
<tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th><th>n + 4</th><th>n + 5</th><th>n + 6</th><th>n + 7</th></tr>
<tr><td>bit/ 0</td><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr>
<tr><td>BP 1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
</table></td><td>msb lsb
<table><tr><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr></table></td></tr>
<tr><td>1 : 2
multiplex</td><td>
</td><td>
</td><td><table>
<tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th></tr>
<tr><td>bit/ 0</td><td>a</td><td>f</td><td>e</td><td>d</td></tr>
<tr><td>BP 1</td><td>b</td><td>g</td><td>c</td><td>DP</td></tr>
<tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
</table></td><td>msb lsb
<table><tr><td>a</td><td>b</td><td>f</td><td>g</td><td>e</td><td>c</td><td>d</td><td>DP</td></tr></table></td></tr>
<tr><td>1 : 3
multiplex</td><td>
</td><td>
</td><td><table>
<tr><th></th><th>n</th><th>n + 1</th><th>n + 2</th></tr>
<tr><td>bit/ 0</td><td>b</td><td>a</td><td>f</td></tr>
<tr><td>BP 1</td><td>DP</td><td>d</td><td>e</td></tr>
<tr><td>2</td><td>c</td><td>g</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td></tr>
</table></td><td>msb lsb
<table><tr><td>b</td><td>DP</td><td>c</td><td>a</td><td>d</td><td>g</td><td>f</td><td>e</td></tr></table></td></tr>
<tr><td>1 : 4
multiplex</td><td>
</td><td>
</td><td><table>
<tr><th></th><th>n</th><th>n + 1</th></tr>
<tr><td>bit/ 0</td><td>a</td><td>f</td></tr>
<tr><td>BP 1</td><td>c</td><td>e</td></tr>
<tr><td>2</td><td>b</td><td>g</td></tr>
<tr><td>3</td><td>DP</td><td>d</td></tr>
</table></td><td>msb lsb
<table><tr><td>a</td><td>c</td><td>b</td><td>DP</td><td>f</td><td>e</td><td>g</td><td>d</td></tr></table></td></tr>
</table>

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0.5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0.5

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

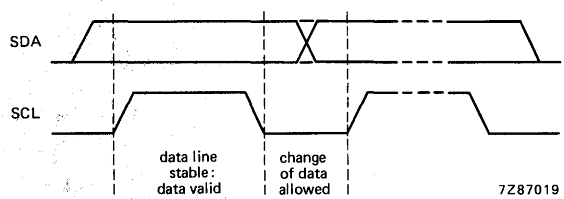


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

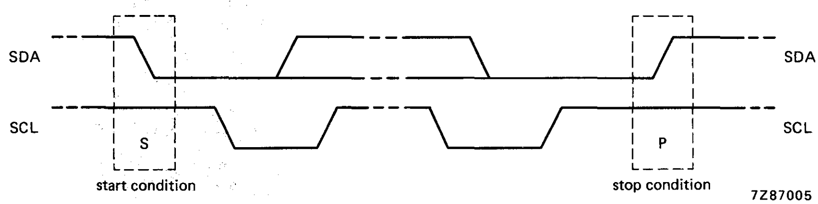


Fig.13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

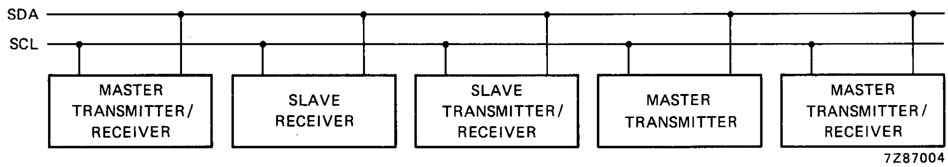


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

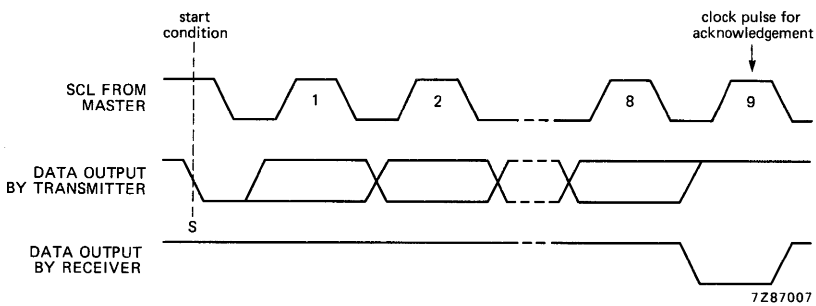


Fig.15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I^2C-bus controller

The PCF8576 acts as an I^2C slave receiver. It does not initiate I^2C-bus transfers or transmit data to an I^2C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I^2C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I^2C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I^2C-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I^2C-bus protocol

Two I^2C-bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I^2C-bus which allows:

(a) up to 16 PCF8576s on the same I^2C-bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I^2C-bus.

The I^2C-bus protocol is shown in Fig.16. The sequence is initiated with a start condition (S) from the I^2C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I^2C-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared mist significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I^2C-bus master issues a stop condition (P).

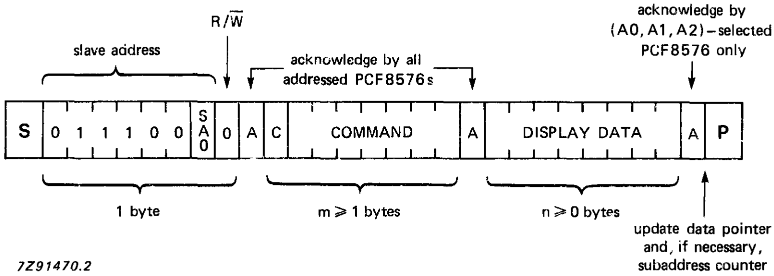


Fig.16 I^2C-bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. All available commands carry a continuation bit C in their most-significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

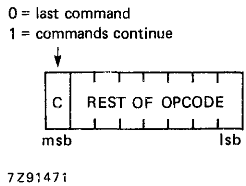


Fig.17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options			description
MODE SET C | 1 0 | LP | E | B | M1 | M0	LCD drive mode	bits M1	M0	Defines LCD drive mode
	static (1 BP)	0	1	
	1 : 2 MUX (2 BP)	1	0	
	1 : 3 MUX (3 BP)	1	1	
	1 : 4 MUX (4 BP)	0	0	
	LCD bias	bit B		Defines LCD bias configuration
	1/3 bias	0		
	1/2 bias	1		
	display status	bit E		Defines display status The possibility to disable the display allows implementation of blinking under external control
	disabled (blank)	0		
	enabled	1		
	mode	bit LP		Defines power dissipation mode
	normal mode	0		
	power-saving mode	1		
LOAD DATA POINTER C | 0 | P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39			Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C | 1 1 0 0 | A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7			Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th colspan="3">options</th><th>description</th></tr>
<tr><td rowspan="6">BANK SELECT
C 1 1 1 1 0 I O</td><td>static</td><td>1 : 2 MUX</td><td>bit I</td><td>Defines input bank selection (storage of arriving display data)</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td><td></td></tr>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td><td>Defines output bank selection (retrieval of LCD display data)</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td><td></td></tr>
<tr><td colspan="3"></td><td>The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td rowspan="4">BLINK
C 1 1 1 0 A BF1 BF0</td><td>blink frequency</td><td>bits BF1</td><td>BF0</td><td>Defines the blinking frequency</td></tr>
<tr><td>off
2 Hz
1 Hz
0.5 Hz</td><td>0
0
1
1</td><td>0
1
0
1</td><td></td></tr>
<tr><td colspan="2">blink mode</td><td>bit A</td><td rowspan="2">Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td colspan="2">normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I^2C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig.18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

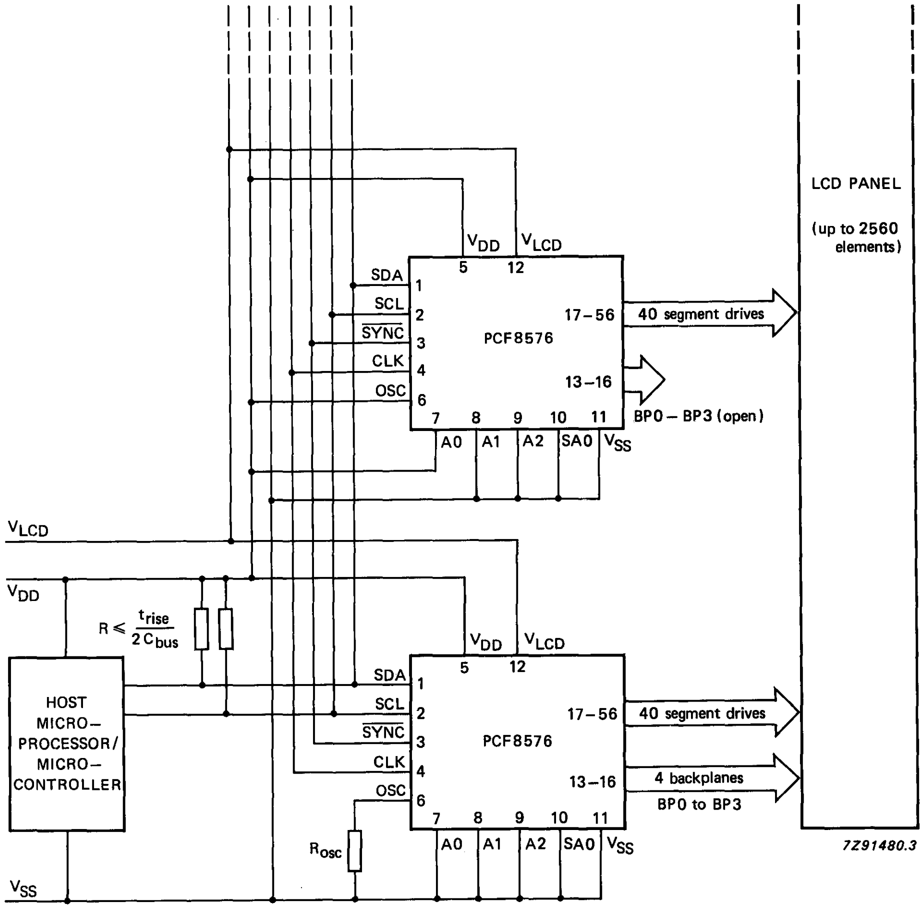
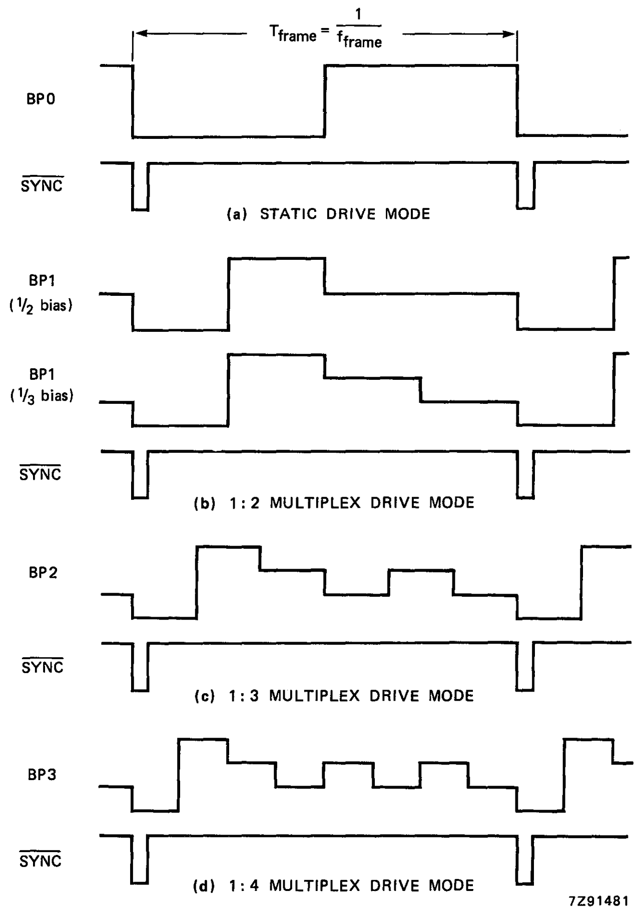


Fig.18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		–0,5 to + 11	V
LCD supply voltage range	V_{LCD}		V_{DD}–11 to V_{DD}	V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS}–0,5 to V_{DD} + 0,5	V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}–0,5 to V_{DD} + 0,5	V
D.C. input current	$\pm I_I$	max.	20	mA
D.C. output current	$\pm I_O$	max.	25	mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50	mA
Power dissipation per package	P_{tot}	max.	400	mW
Power dissipation per output	P_O	max.	100	mW
Storage temperature range	T_{stg}		–65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}–2 to V_{DD}–9 V;
T_{amb} = –40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}–9	–	V_{DD}–2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}–0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$–5 V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}$–5 V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}$–2 to V_{DD}–9 V;
T_{amb} = –40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}$–5 V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I^2C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I^2C bus maximum transmission speed is derated.

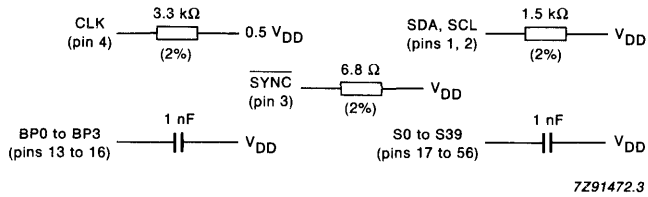


Fig. 20 Test loads.

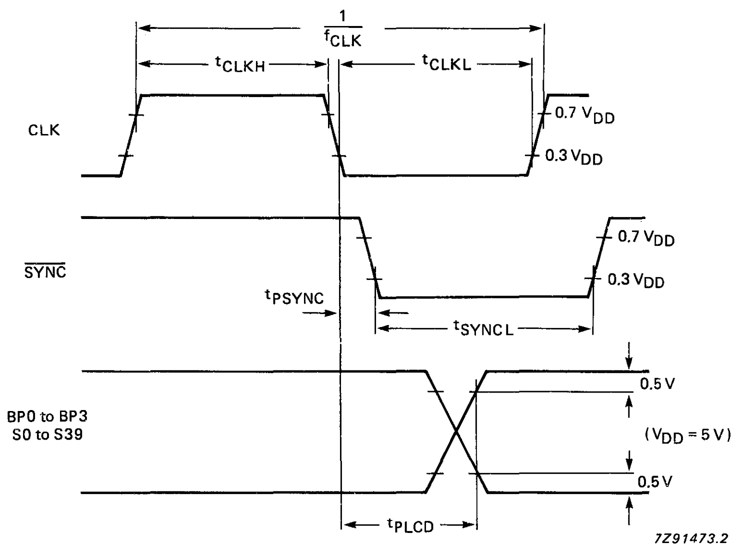


Fig. 21 Driver timing waveforms.

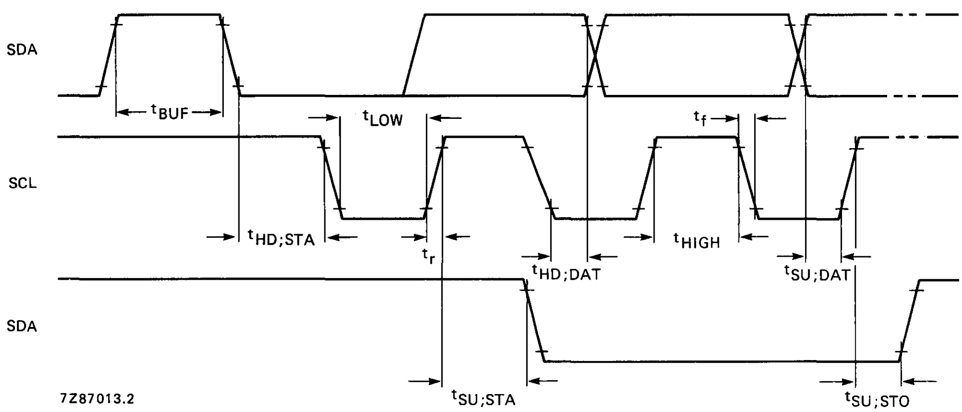
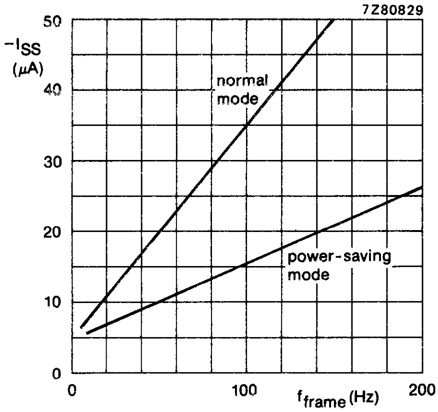
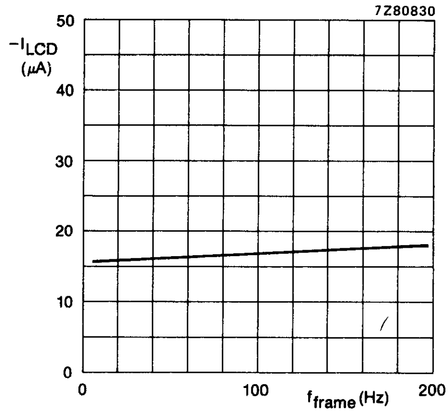


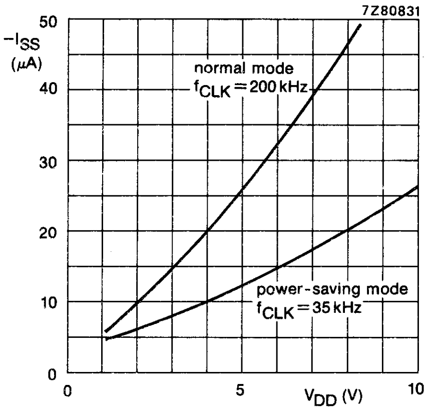
Fig. 22 I²C bus timing waveforms.



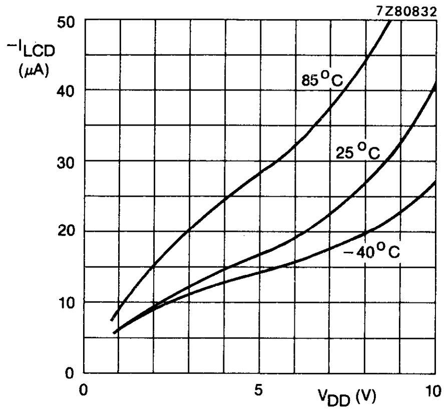
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

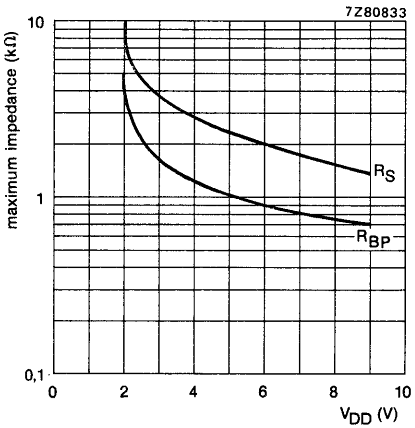


(c) V_{LCD} = 0 V; external clock;
T_{amb} = –40 to + 85 °C.

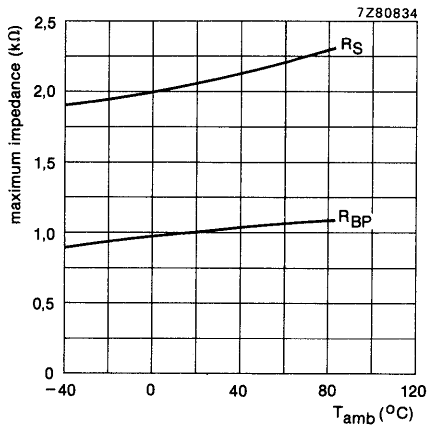


(d) V_{LCD} = 0 V; external clock;
f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

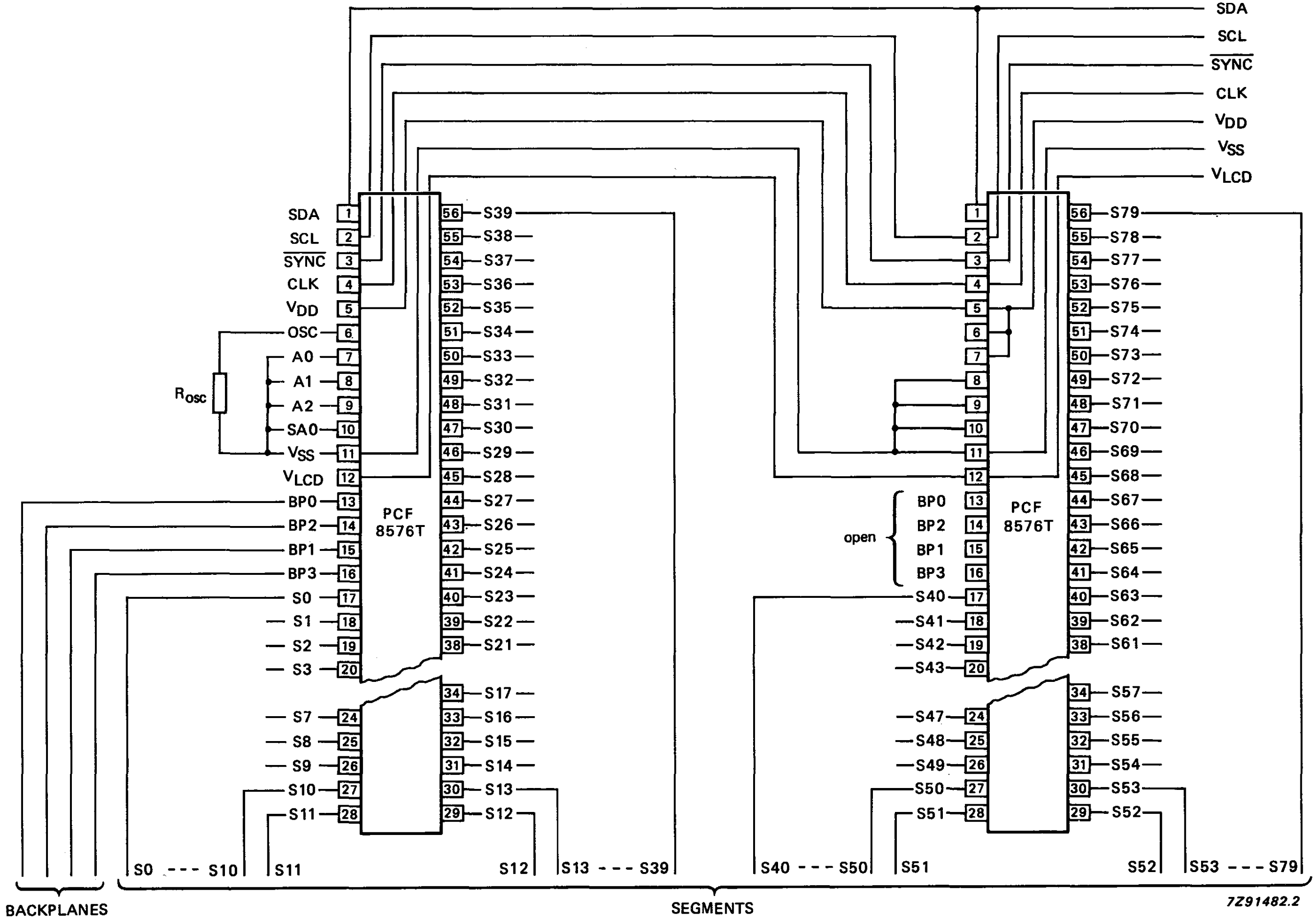


Fig. 25 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig.26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig.27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

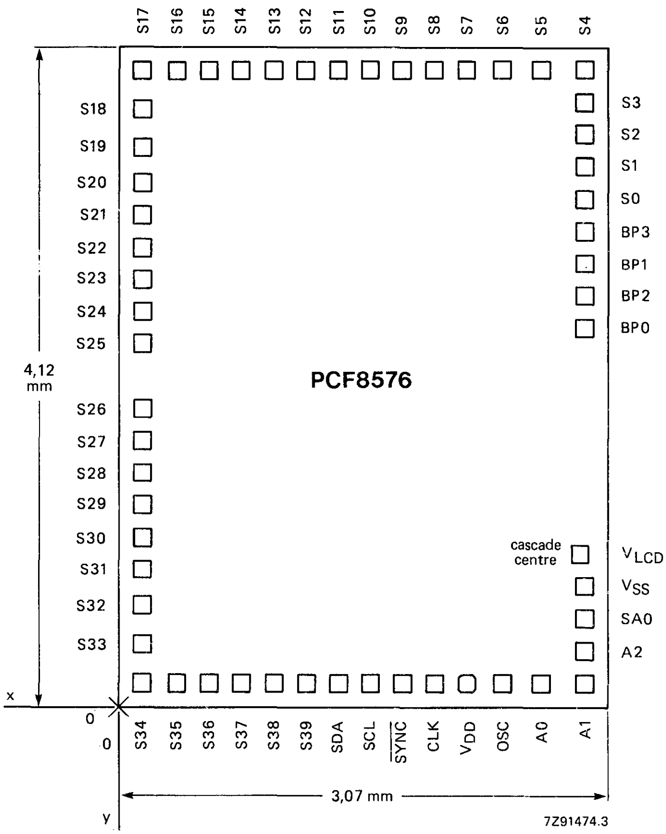


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380		
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380		
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32		640	
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0		560	
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

APPLICATION INFORMATION (continued)

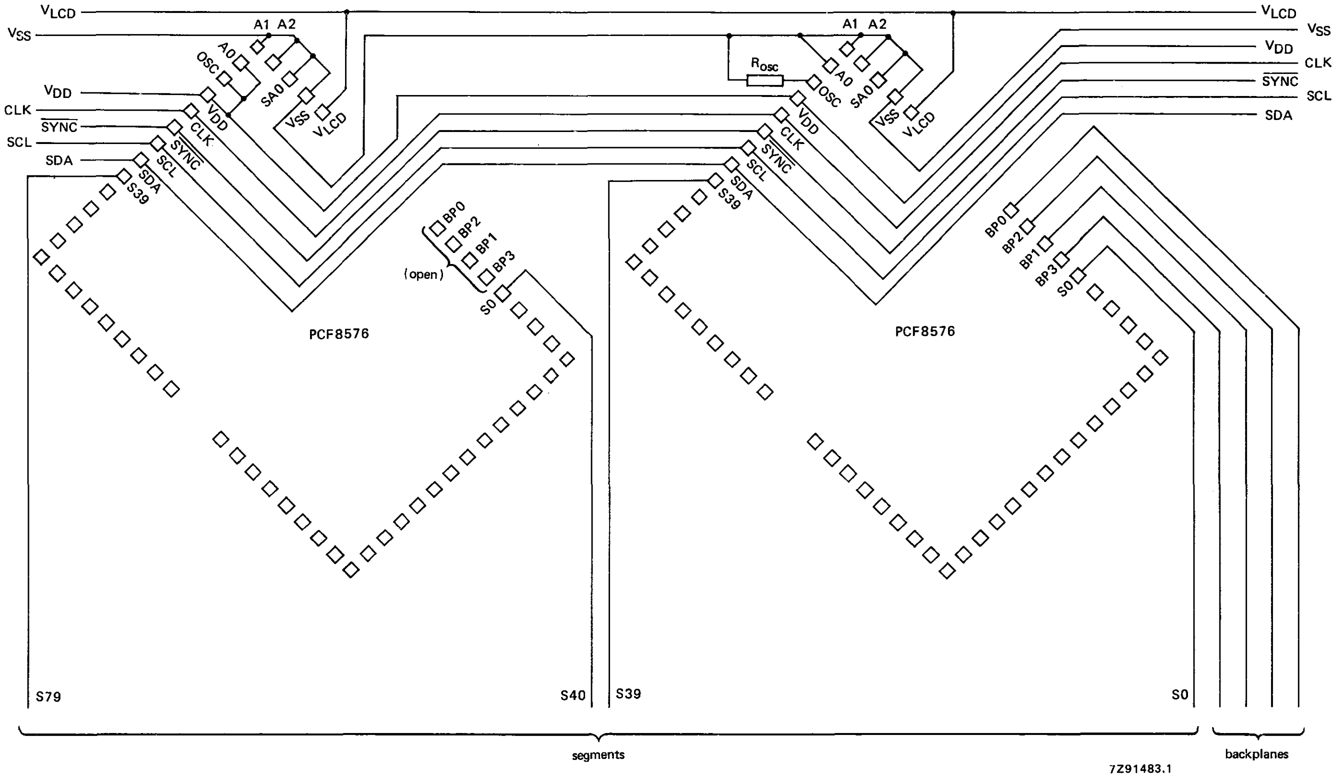


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave addresses.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 9 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset blanks display

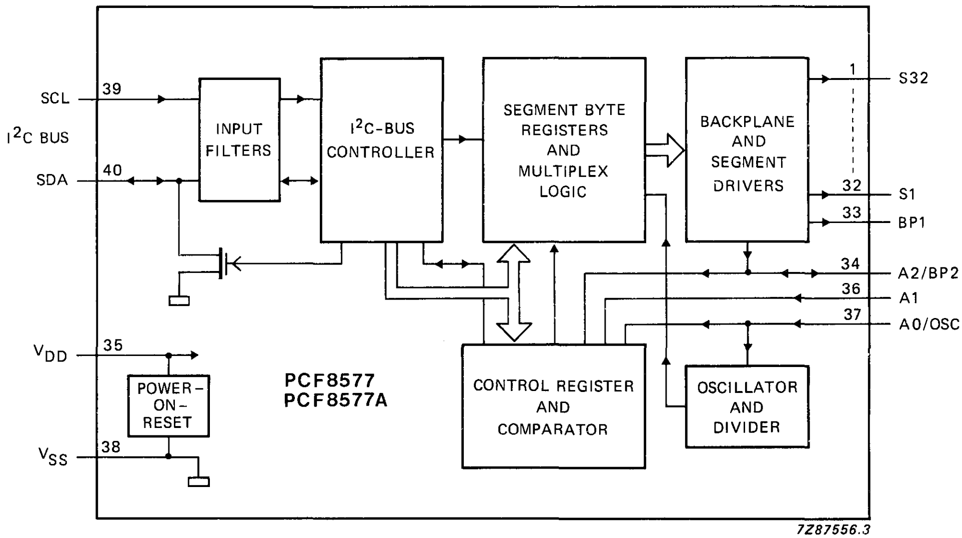


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT: in blister tape.
PCF8577U/5, PCF8577AU/5: wafer unsawn.
PCF8577U/10, PCF8577AU/10: chip-on-film frame carrier (FFC).

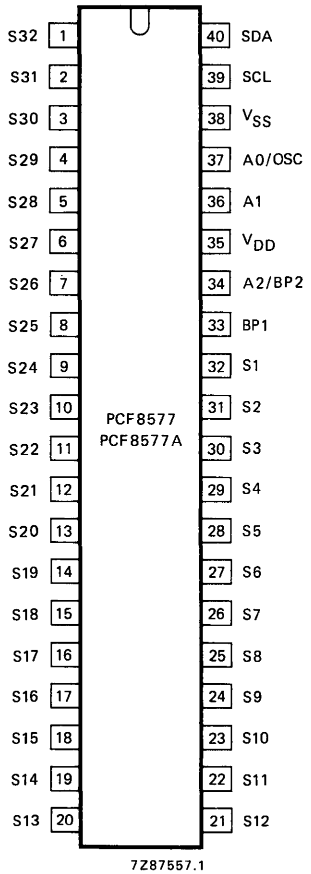


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

40	SDA	I^2C-bus data line
39	SCL	I^2C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I^2C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

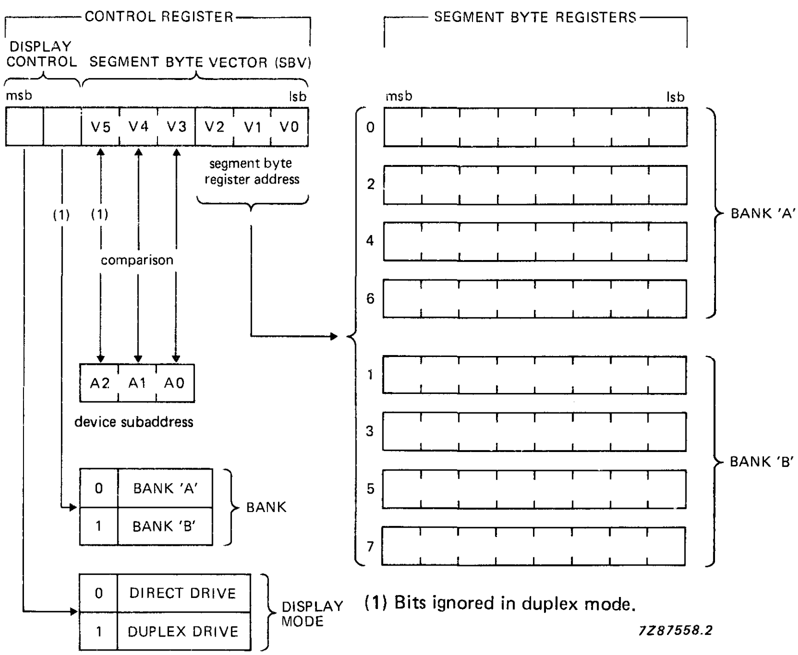


Fig.3 PCF8577 register organization.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

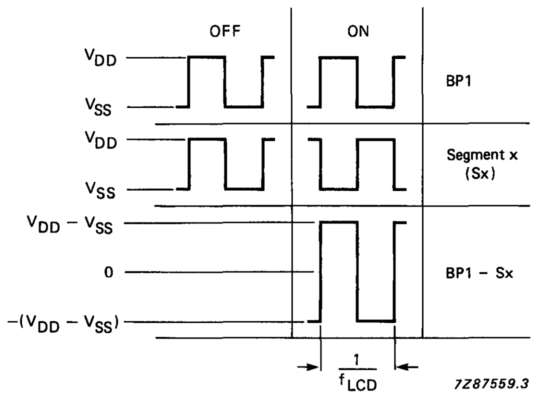
After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.



$V_{on(rms)} = V_{DD} - V_{SS}$
$V_{off(rms)} = 0$

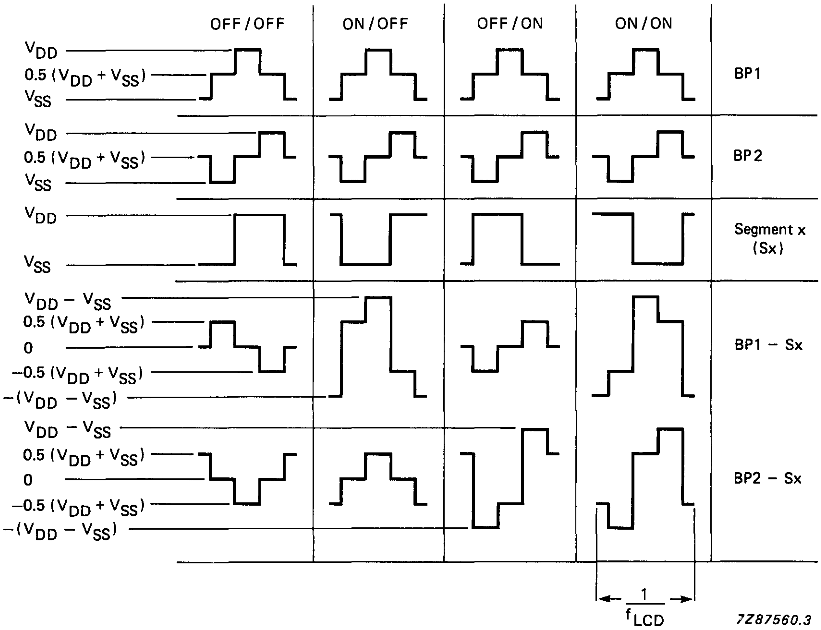
Fig.4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$$V_{on(rms)} = 0.791\,(V_{DD} - V_{SS})$$
$$V_{off(rms)} = 0.354\,(V_{DD} - V_{SS})$$
$$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$$

Fig.5 Duplex mode display output waveforms.

Power-on reset

At power-on reset the PCF8577 resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig.6.

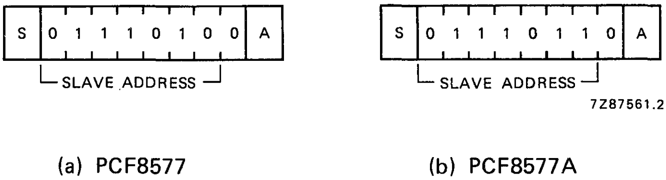


Fig.6 PCF8577 and PCF8577A slave addresses.

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

I^2C-bus protocol

The PCF8577 I^2C-bus protocol is shown in Fig.7.

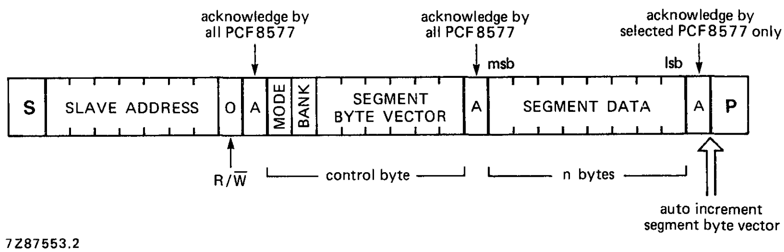


Fig.7 I^2C-bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig.6). All PCF8577s with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte-segment driver mapping in the direct drive mode

MODE	BANK	V2	V1	V0	segment register \ bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte; segment driver mapping in the duplex mode

MODE	BANK	V2	V1	V0	segment register \ bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

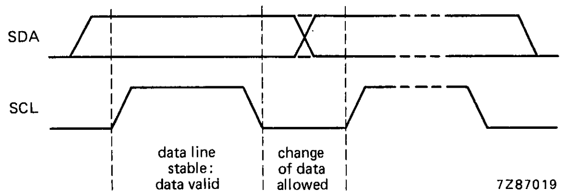


Fig.8 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

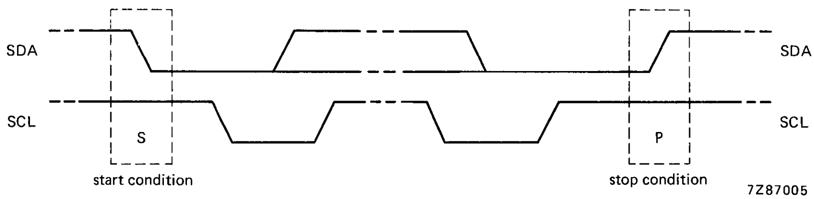


Fig.9 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

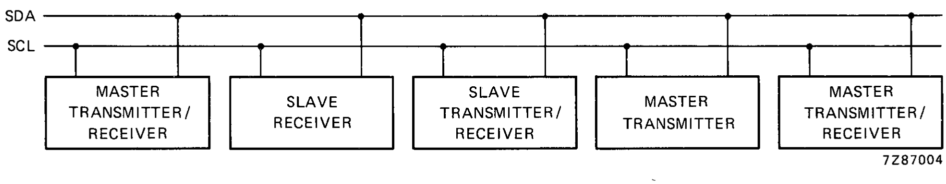


Fig.10 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

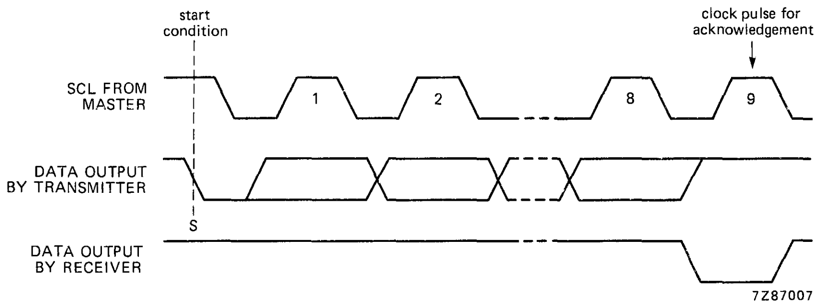


Fig.11 Acknowledgement on the I^2C-bus.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 11.0	V
Voltage on pin	V_I	−0.5	V_{DD} + 0.5	V
V_{DD} or V_{SS} current	I_{DD}; I_{SS}	−50	+ 50	mA
DC input current	I_I	−20	+ 20	mA
DC output current	I_O	−25	+ 25	mA
Power dissipation per package	P_{tot}	−	500*	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Derate 7.7 mW/K when $T_{amb} > 60$ °C.

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	9.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD1}	–	80	250	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD2}	–	25	150	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; A0/OSC = V_{DD} or V_{SS}	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}–0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}–0.10	–	V_{DD}	V
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.08	V
Input voltage HIGH		V_{IH4}	2.0	–	9.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	V_I = V_{DD} or V_{SS}	$+I_{L1}$	–	–	1	μA
A2; BP2						
Leakage current	V_I = V_{SS}	I_{L2}	–	–	1	μA
Pull-down current	V_I = V_{DD}	$-I_{L2}$	–	1.5	5	μA

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

parameter	conditions	symbol	min.	typ.*	max.	unit
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	$V_{OL} = 0.4$ V; $V_{DD} = 5$ V	I_{OL}	0.3	–	–	mA
	$V_{OH} = V_{DD} -0.4$ V; $V_{DD} = 5$ V	$-I_{OH}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}, V_{DD}, (V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

AC CHARACTERISTICS (note 2)

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	1.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.7	–	–	μs

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

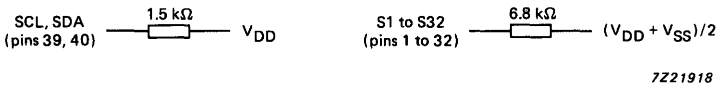


Fig.12 Test loads.

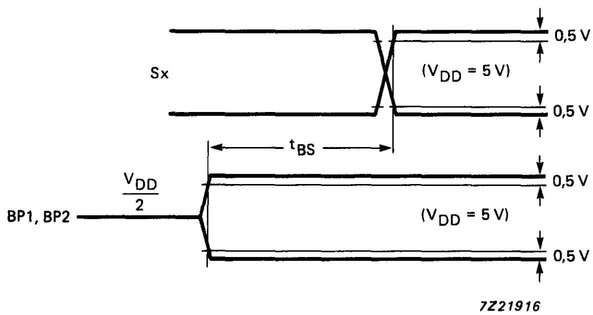


Fig.13 Driver timing waveforms.

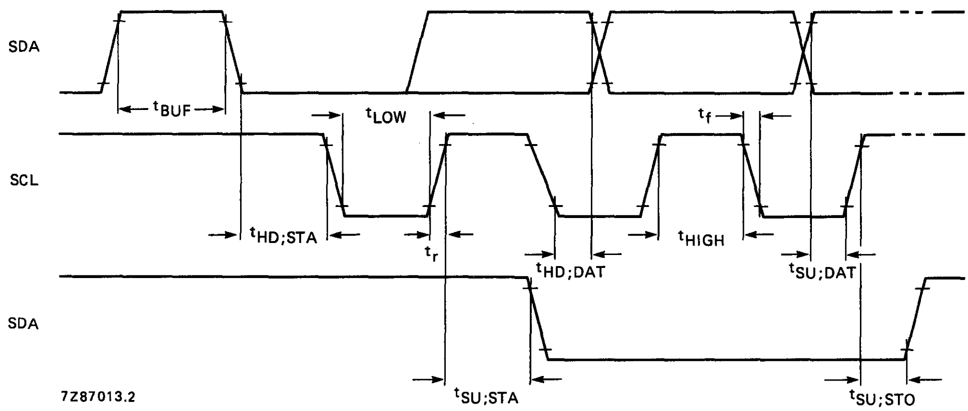


Fig.14 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

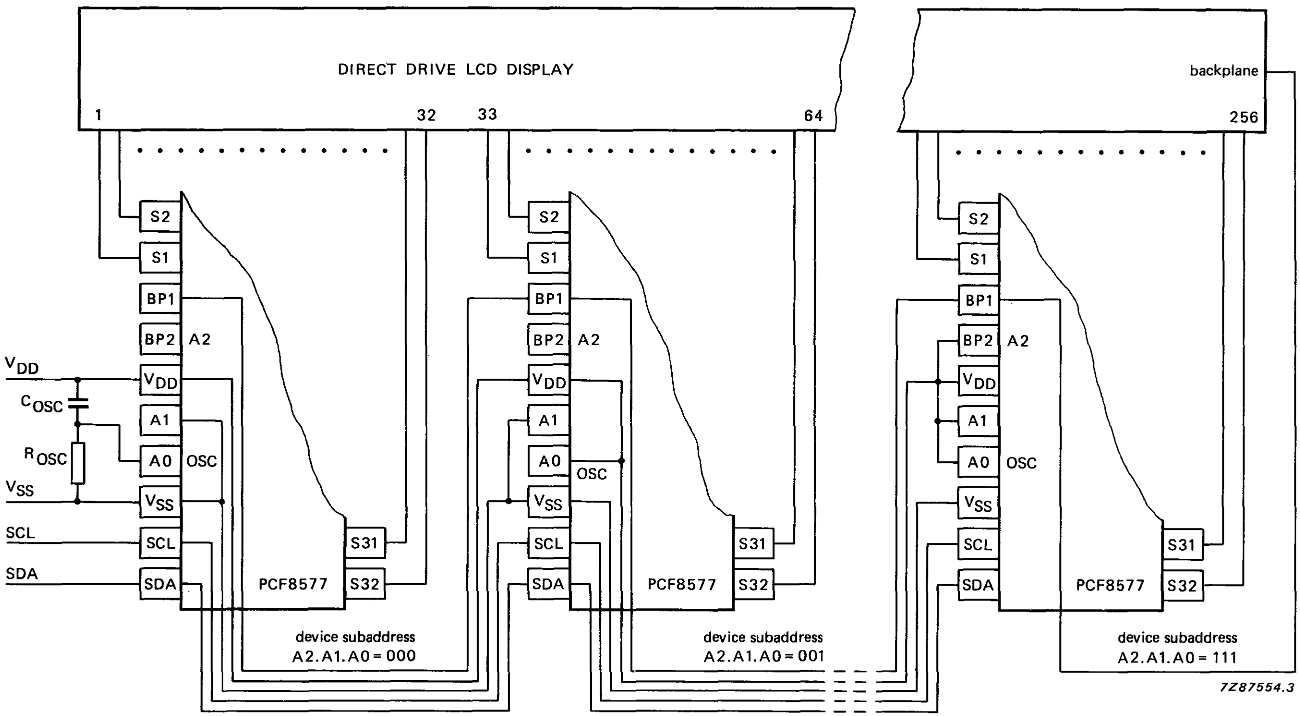


Fig.15 Direct drive display; expansion to 256 segments using eight PCF8577.

APPLICATION INFORMATION (continued)

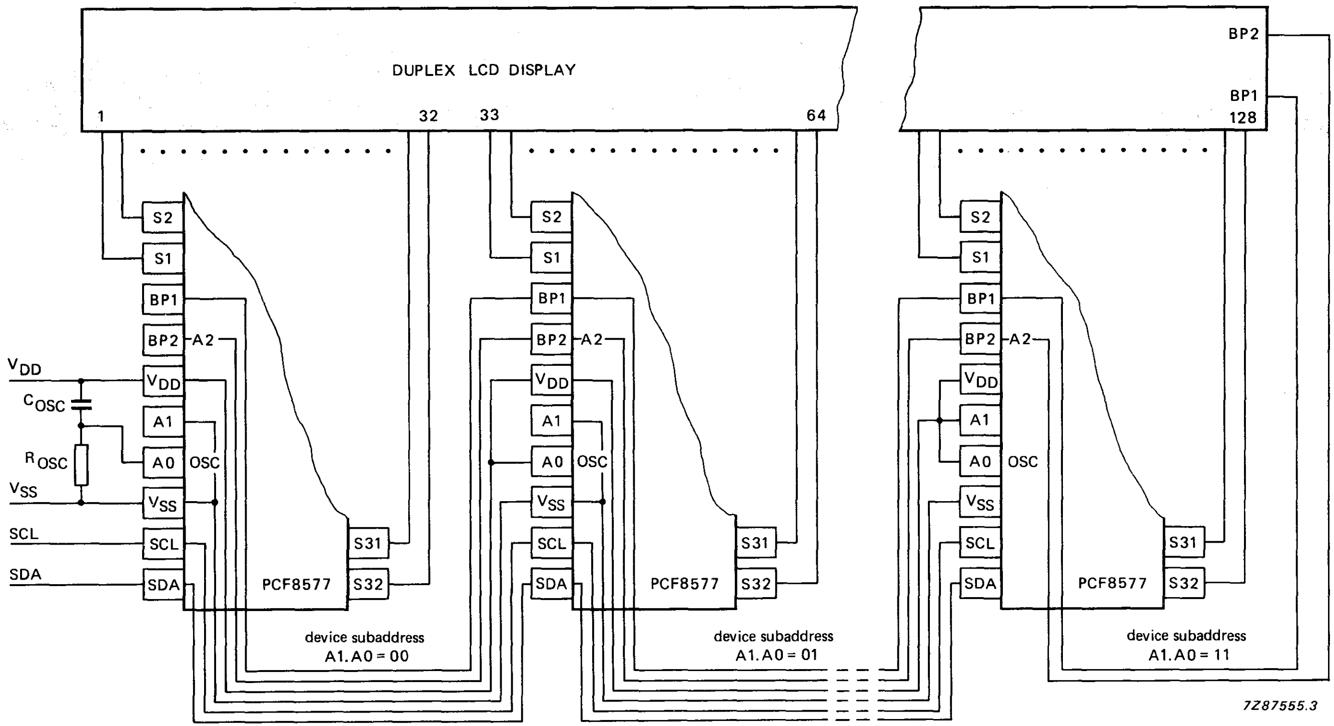
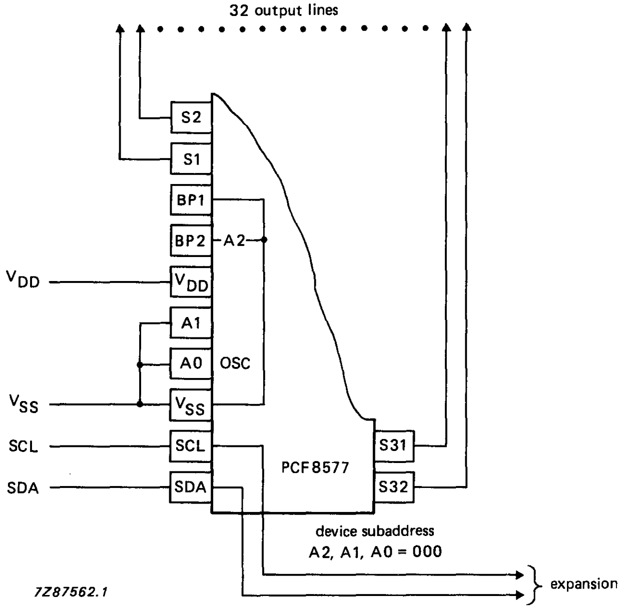


Fig.16 Duplex display; expansion to 2 x 128 segments using four PCF8577.

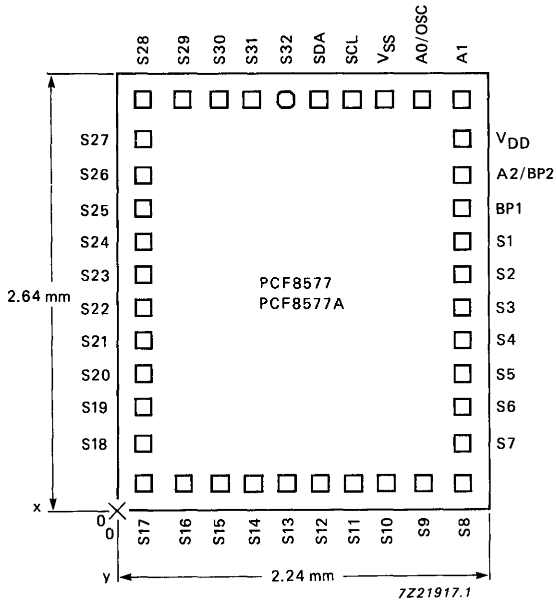


Notes

1. MODE bit must always be set to logic 0 (direct drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577 as 32-bit output expander in I²C-bus application.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.91 mm^2

Bonding pad dimensions: 120 μm x 120 μm

Fig.18 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to bottom corner, see Fig.18.

pad	X	Y	pad	X	Y
S32	1020	2480	S12	1220	160
S31	820	2480	S11	1420	160
S30	620	2480	S10	1620	160
S29	400	2480	S9	1840	160
S28	160	2480	S8	2080	160
S27	160	2240	S7	2080	400
S26	160	2020	S6	2080	620
S25	160	1820	S5	2080	820
S24	160	1620	S4	2080	1020
S23	160	1420	S3	2080	1220
S22	160	1220	S2	2080	1420
S21	160	1020	S1	2080	1620
S20	160	820	BP1	2080	1820
S19	160	620	A2/BP2	2080	2020
S18	160	400	V_{DD}	2080	2240
S17	160	160	A1	2080	2480
S16	400	160	A0/OSC	1840	2480
S15	620	160	V_{SS}	1620	2480
S14	820	160	SCL	1420	2480
S13	1020	160	SDA	1220	2480

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

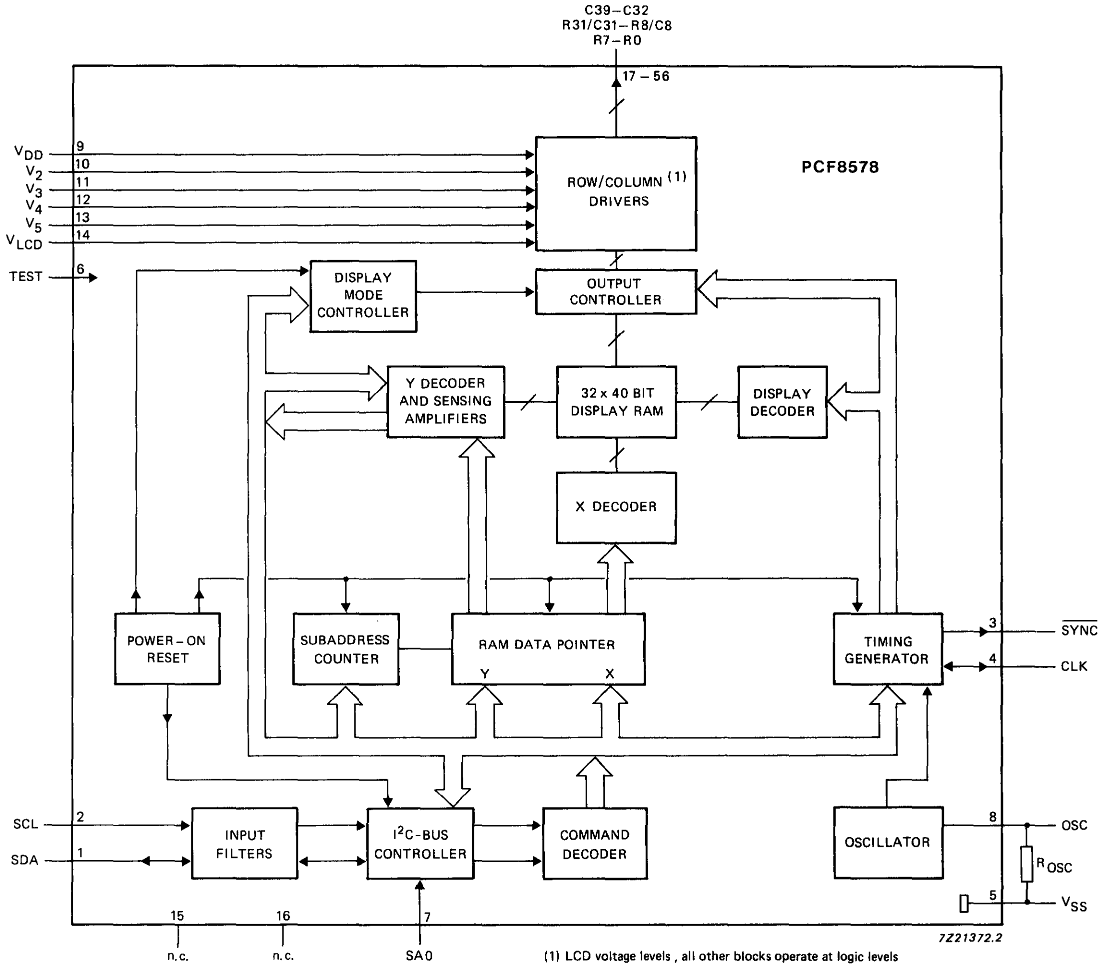


Fig.1 Block diagram.

PINNING

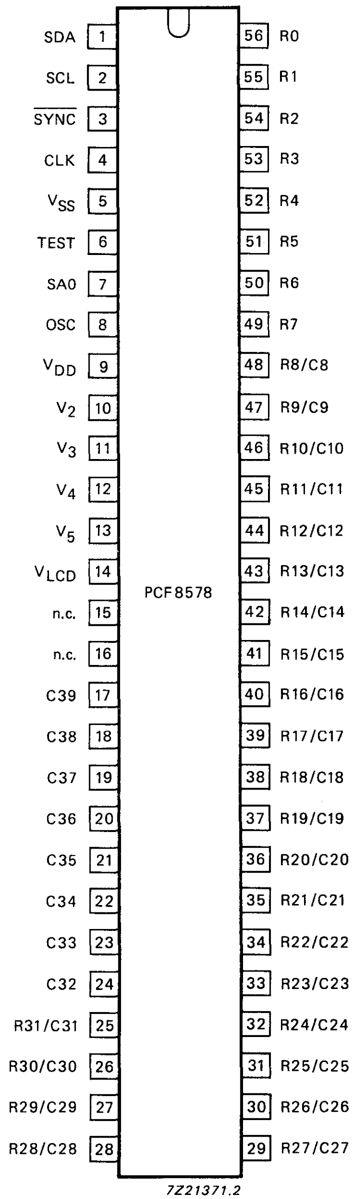
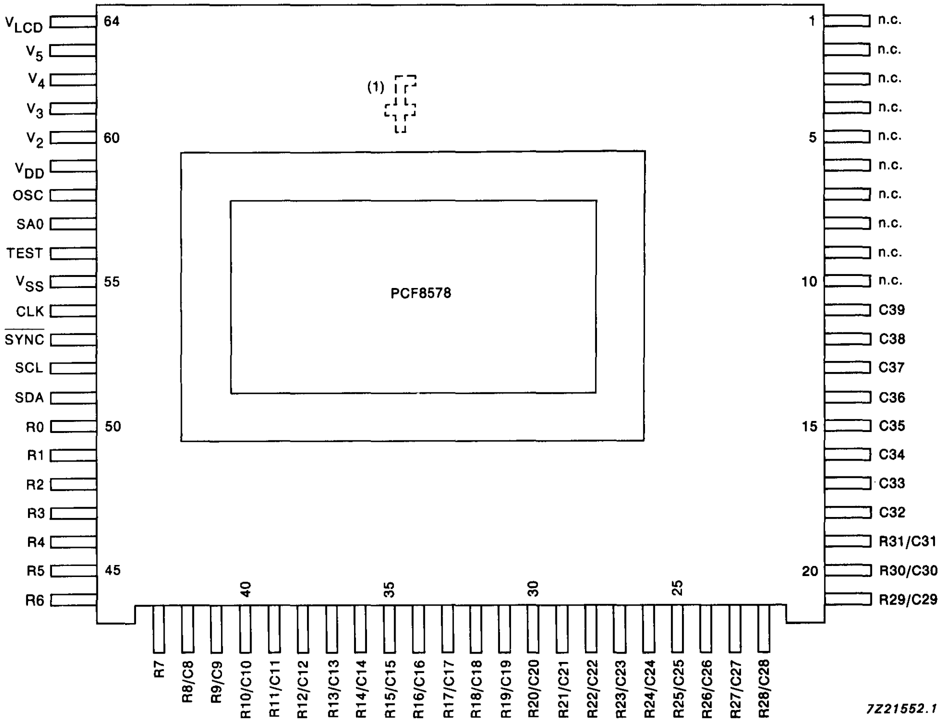


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram; SO121.

mnemonic	pin no.		description
	SOT190	SO121	
SDA	1	51	I^2C-bus serial data line
SCL	2	52	I^2C-bus serial clock line
$\overline{SYNC}$	3	53	cascade synchronization output
CLK	4	54	external clock input/output
V_{SS}	5	55	ground (logic)
TEST	6	56	test pin (connect to V_{SS})
SA0	7	57	I^2C-bus slave address input (bit 0)
OSC	8	58	oscillator input
V_{DD}	9	59	positive supply voltage
V_2 to V_5	10 - 13	60 - 63	LCD bias voltage inputs
V_{LCD}	14	64	LCD supply voltage
n.c.	15 - 16	1 - 10	not connected
C39 to C32	17 - 24	11 - 18	LCD column driver outputs
R31/C31 to R8/C8	25 - 48	19 - 42	LCD row/column driver outputs
R7 to R0	49 - 56	43 - 50	LCD row driver outputs

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See table 1 for common display configurations.

Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Possible display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1:8	8	32	–	–	small digital or alphanumeric displays
	1:16	16	24	–	–	
	1:24	24	16	–	–	
	1:32	32	8	–	–	
with PCF8579	1:8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1:16	16	624	16 x 2	640	
	1:24	24	616	24	640	
	1:32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microprocessor set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.3 (a stand-alone system would be identical but without the PCF8579s).

Multiplexed LCD bias generation

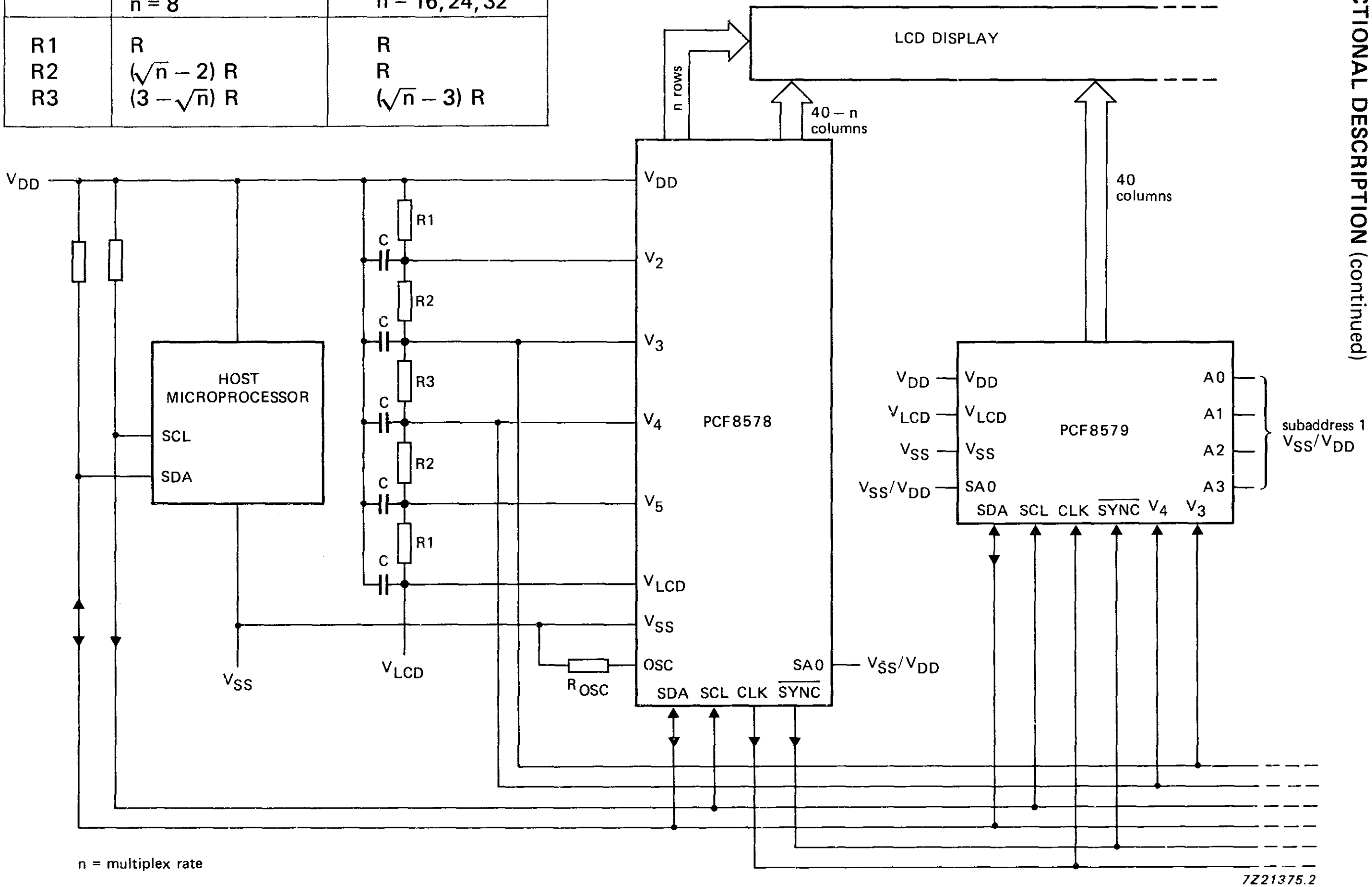
The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 2 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

DEVELOPMENT DATA

	multiplex rate (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n} - 2)$ R	R
R3	$(3 - \sqrt{n})$ R	$(\sqrt{n} - 3)$ R



n = multiplex rate

Fig.3 Typical mixed mode configuration.

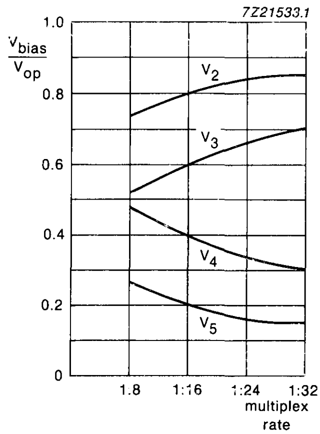


Fig.4 LCD bias voltages as a function of the multiplex rate.

DEVELOPMENT DATA

Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1:32 multiplex rate, row mode
3. Start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

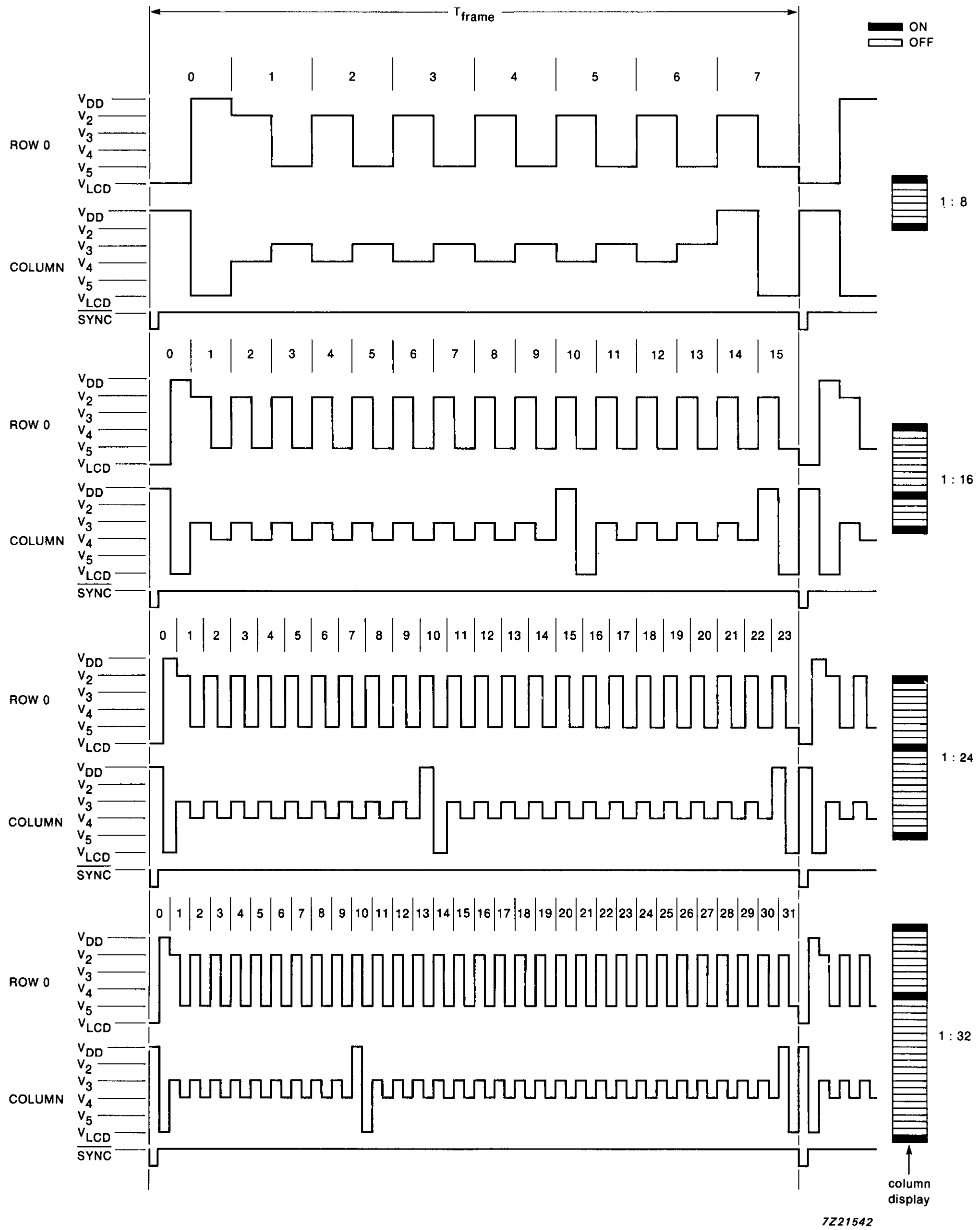
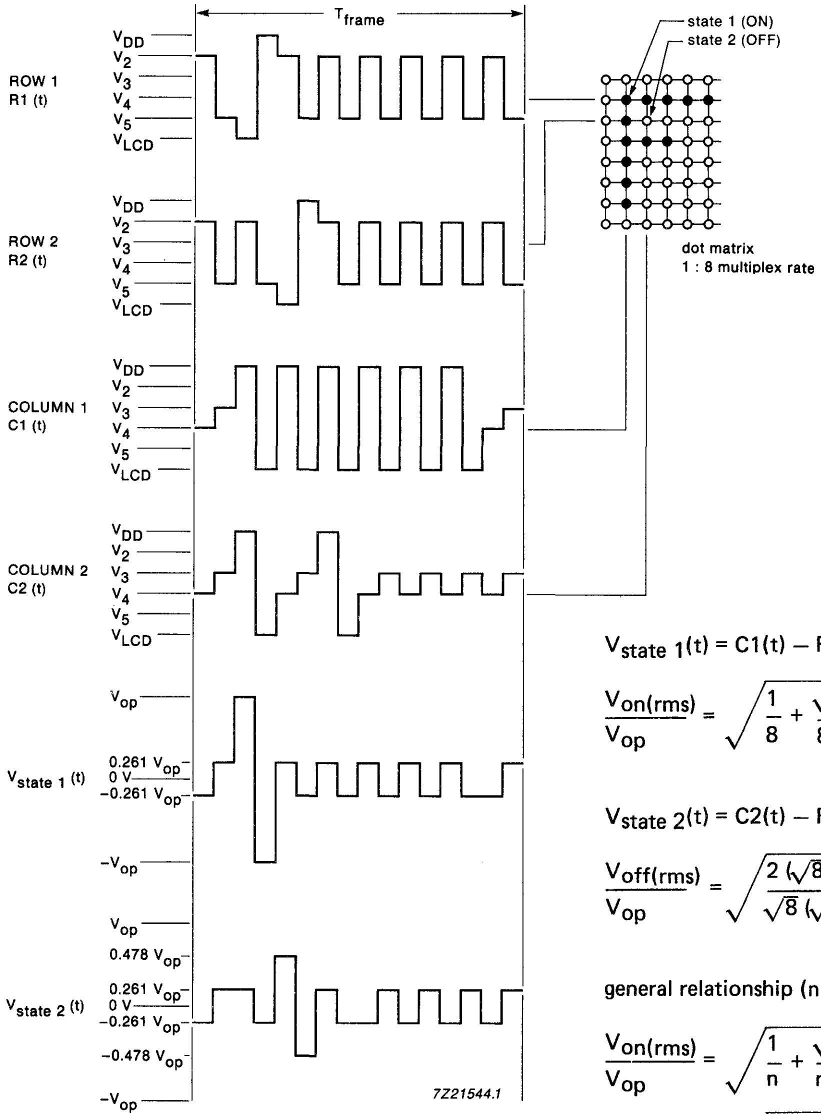


Fig.5 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8\,(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{8}-1)}{\sqrt{8}\,(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

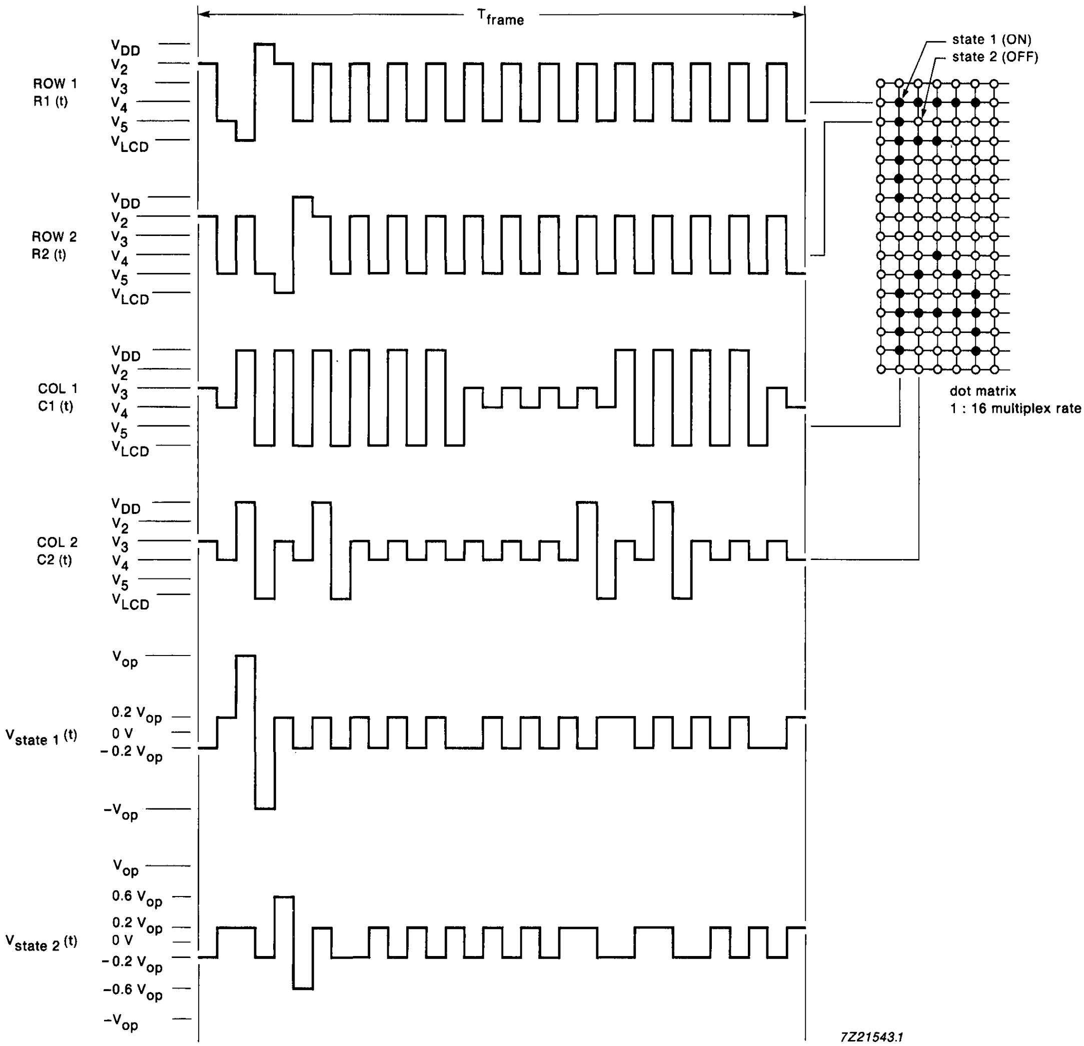
$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n\,(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n}-1)}{\sqrt{n}\,(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:8 multiplex rate.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1:16 multiplex rate.

DEVELOPMENT DATA

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.8. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency.

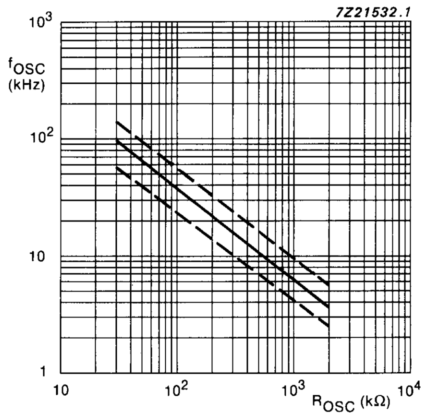


Fig.8 Oscillator frequency as a function of R_{OSC}.

Note

To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 3 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Table 3 Signal frequencies required for nominal 64 Hz frame frequency

oscillator frequency (R_{OSC} = 330 kΩ) f_{OSC} (Hz)	frame frequency $f_{\overline{SYNC}}$ (Hz)	multiplex rate n	division ratio	clock frequency f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

FUNCTIONAL DESCRIPTION (continued)

Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{\text{SYNC}}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit. Using a 1:16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations; i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1:8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit.

Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

Display RAM

The PCF8578 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

RAM operations are only possible when the PCF8578 is in mixed mode. In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.9).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.10):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.11. This feature is useful when scrolling in alphanumeric applications.

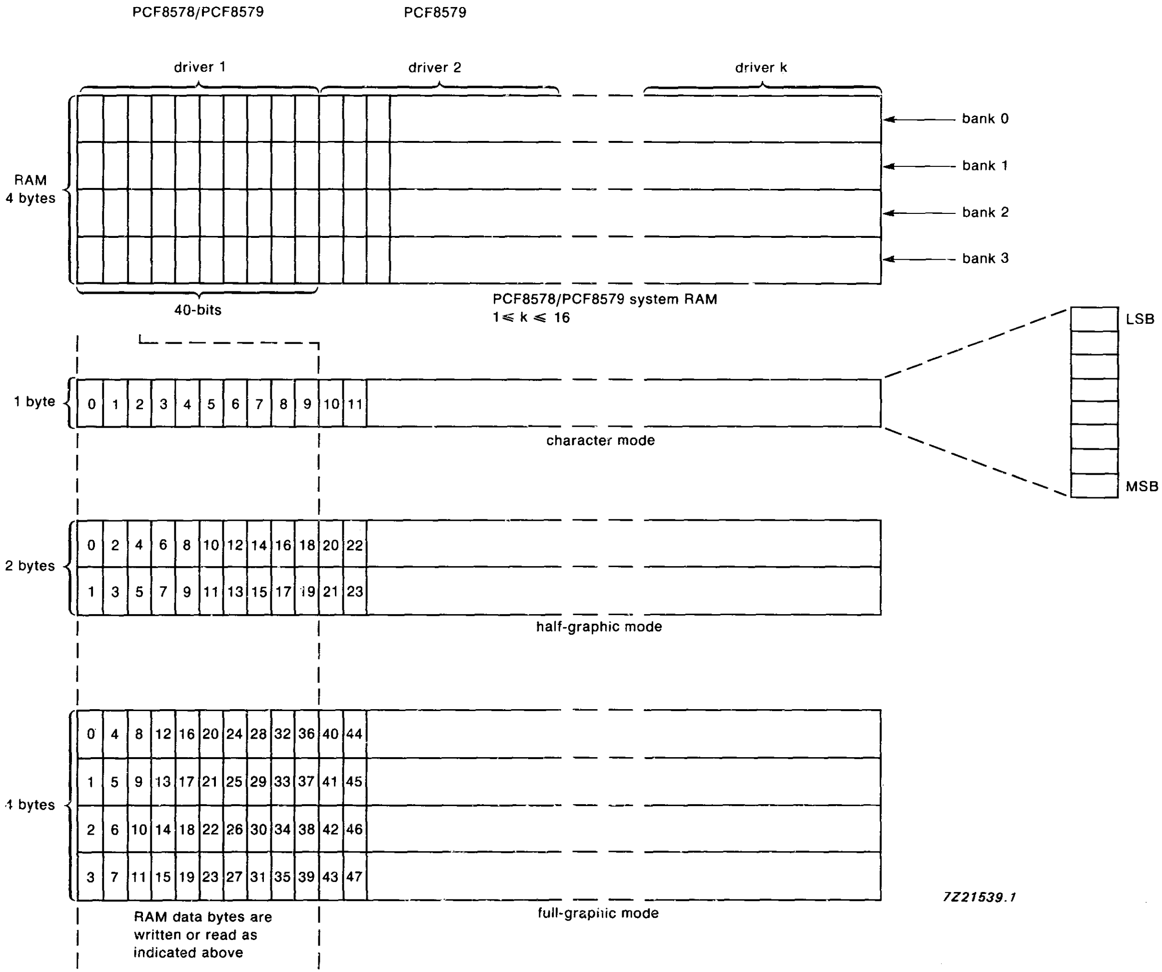


Fig.9 RAM access mode.

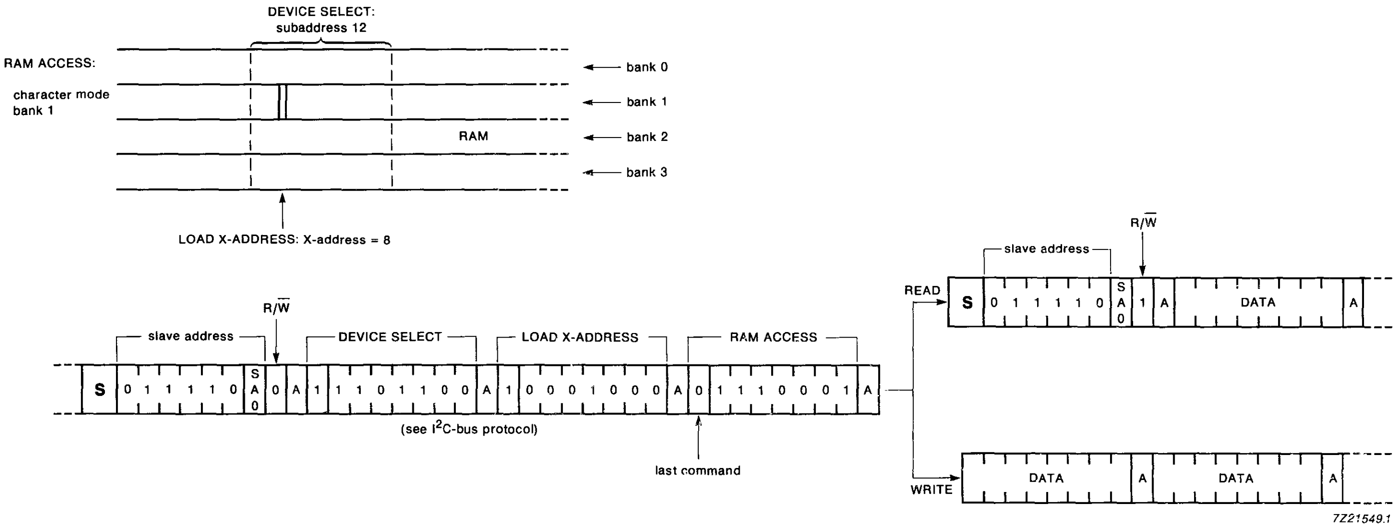


Fig.10 Example of commands specifying initial data byte RAM locations.

FUNCTIONAL DESCRIPTION (continued)

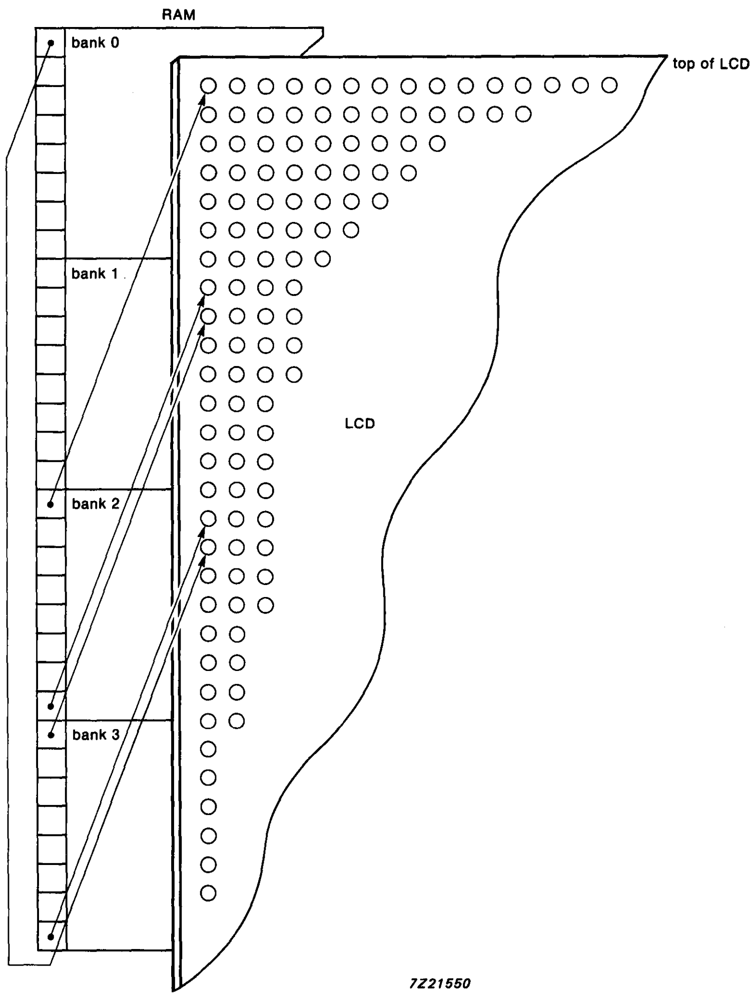


Fig.11 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I^2C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I^2C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I^2C-bus for very large applications
(b) the use of two types of LCD multiplex schemes on the same I^2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I^2C-bus protocol is shown in Fig. 12. All communications are initiated with a start condition (S) from the I^2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I^2C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A_0 to A_3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

DEVELOPMENT DATA

I²C-BUS PROTOCOL (continued)

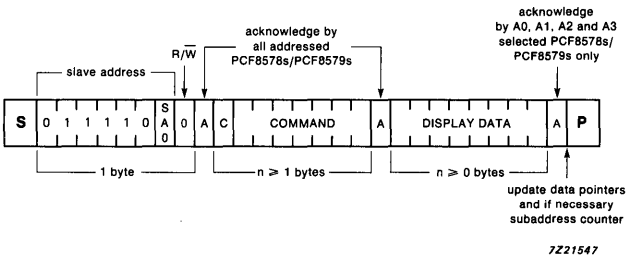


Fig.12(a) Master transmits to slave receiver (WRITE mode).

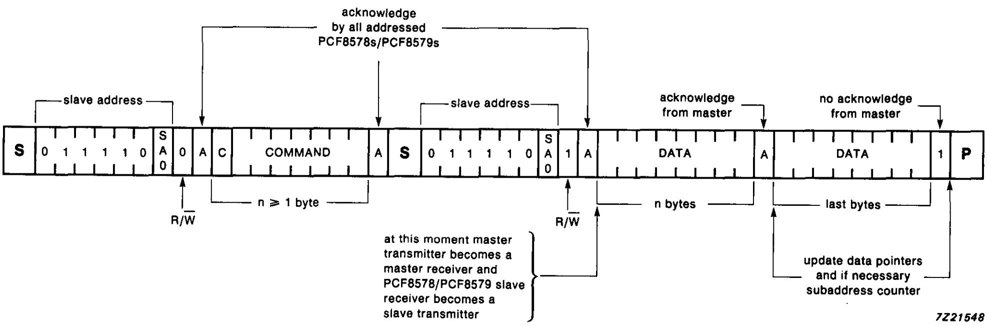


Fig.12(b) Master reads after sending command string (WRITE commands; READ data).

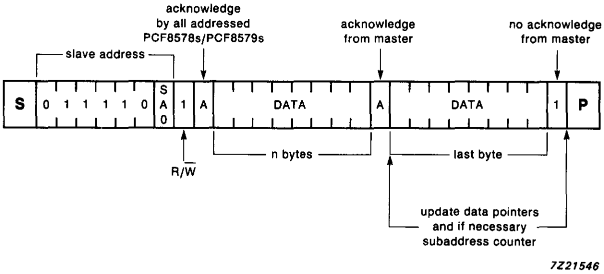
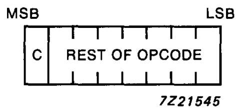


Fig.12(c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. The most-significant bit of a command is the continuation bit C (see Fig.13). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.13 General format of command byte.

The five commands available to the PCF8578 are defined in Tables 4 and 5.

Table 4 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic mode, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

I^2C-BUS PROTOCOL (continued)

Table 5 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C | 1 0 | T | E1 E0 | M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C | 1 1 1 1 1 | B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C | 1 1 0 | A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

command / opcode	options	description
RAM ACCESS C | 1 1 1 | G1 G0 | Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed * 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C | 0 | X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

DEVELOPMENT DATA

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

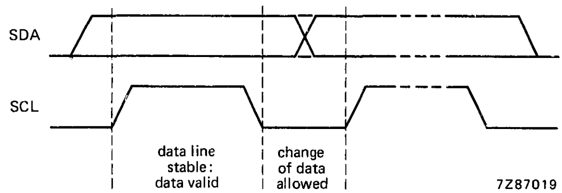


Fig.14 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

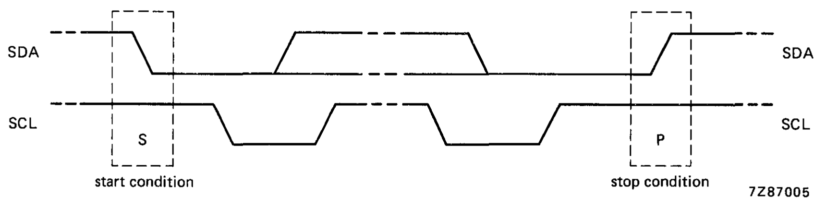


Fig.15 Definition of start and stop condition.

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

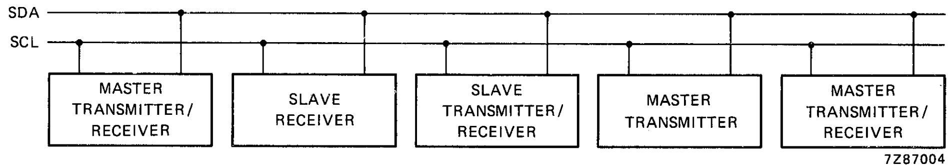


Fig.16 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

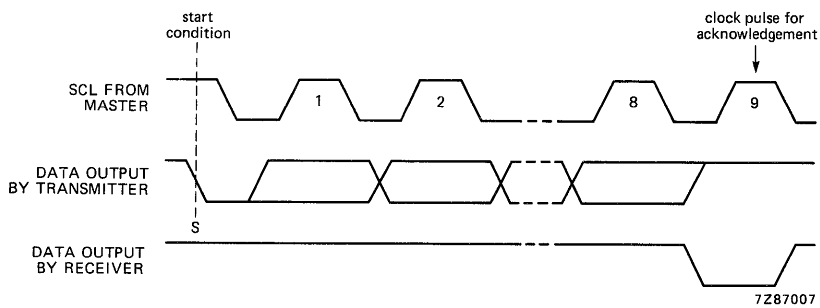


Fig.17 Acknowledgement on the I^2C-bus.

Note

The general characteristics and detailed specification of the I^2C-bus are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at SDA, SCL, CLK, TEST, SA0 and OSC	V_{I1}	V_{SS} −0.5	V_{DD} +0.5	V
V_2 to V_5	V_{I2}	V_{LCD} −0.5	V_{DD} +0.5	V
Output voltage range at $\overline{\text{SYNC}}$ and CLK	V_{O1}	V_{SS} −0.5	V_{DD} +0.5	V
R0 to R7, R8/C8 to R31/C31, and C32 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} +0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1;					
external clock	f_{CLK} = 2 kHz	I_{DD1}	–	6	15	μA
internal clock	R_{OSC} = 330 kΩ	I_{DD2}	–	20	50	μA
Power-on reset level	note 2	V_{POR}	0.8	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V; V_{DD} = 5 V	I_{OH1}	–	–	−1	mA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3.0	–	–	mA
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
Leakage current at OSC	V_I = V_{DD}	I_{L2}	−1	–	1	μA
Input capacitance at SCL and SDA	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	I_{L3}	−2	–	2	μA
DC component of LCD drivers R0 to R7, R8/C8 to R31/C31, and C32 to C39		± V_{DC}	–	20	–	mV
Output resistance at R0 to R7 and R8/C8 to R31/C31	note 4; row mode	R_{ROW}	–	1.5	3.0	kΩ
R8/C8 to R31/C31 and C32 to C39	column mode	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} –3.5 V to V_{DD} –9 V; T_{amb} = - 40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	f_{CLK1}	1.2	2.1	3.3	kHz
1:24		f_{CLK2}	0.9	1.6	2.5	kHz
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	500	ns
Driver delays	V_{DD} – V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	µs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	µs
Start condition set-up time	repeated start codes only	$t_{SU; STA}$	4.7	–	–	µs
Start condition hold time		$t_{HD; STA}$	4.0	–	–	µs
SCL LOW time		t_{LOW}	4.7	–	–	µs
SCL HIGH time		t_{HIGH}	4.0	–	–	µs
SCL and SDA rise time		t_r	–	–	1.0	µs
SCL and SDA fall time		t_f	–	–	0.3	µs
Data set-up time		$t_{SU; DAT}$	250	–	–	ns
Data hold time		$t_{HD; DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU; STO}$	4.0	–	–	µs

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor, (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   row mode, R0 to R7 and R8/C8 to R31/C31 (row mode):
   $V_2 - V_{LCD} \geqslant 6.65$ V; $V_5 - V_{LCD} \leqslant 2.35$ V; $I_{LOAD} = 150\ \mu A$

   column mode, R8/C8 to R31/C31 (column mode) and C32 to C39:
   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu A$.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

DEVELOPMENT DATA

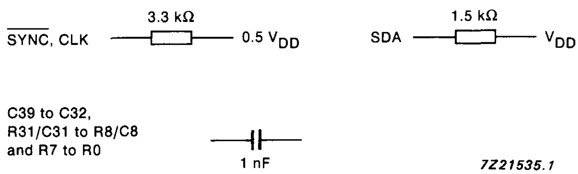


Fig.18 Test loads.

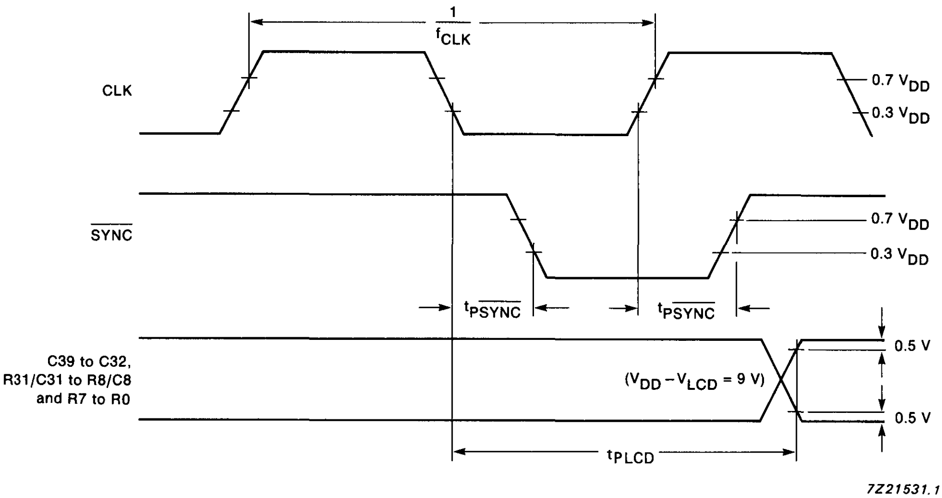


Fig.19 Driver timing waveforms.

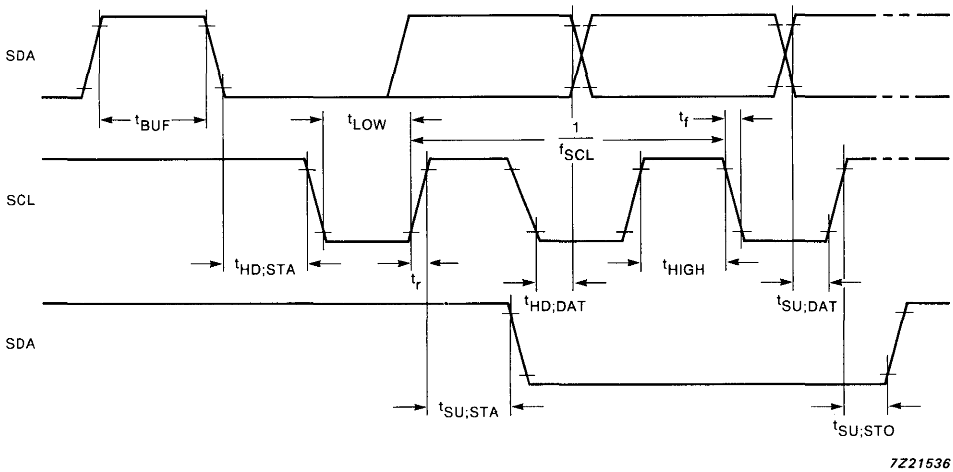


Fig.20 I^2C-bus timing waveforms.

APPLICATION INFORMATION

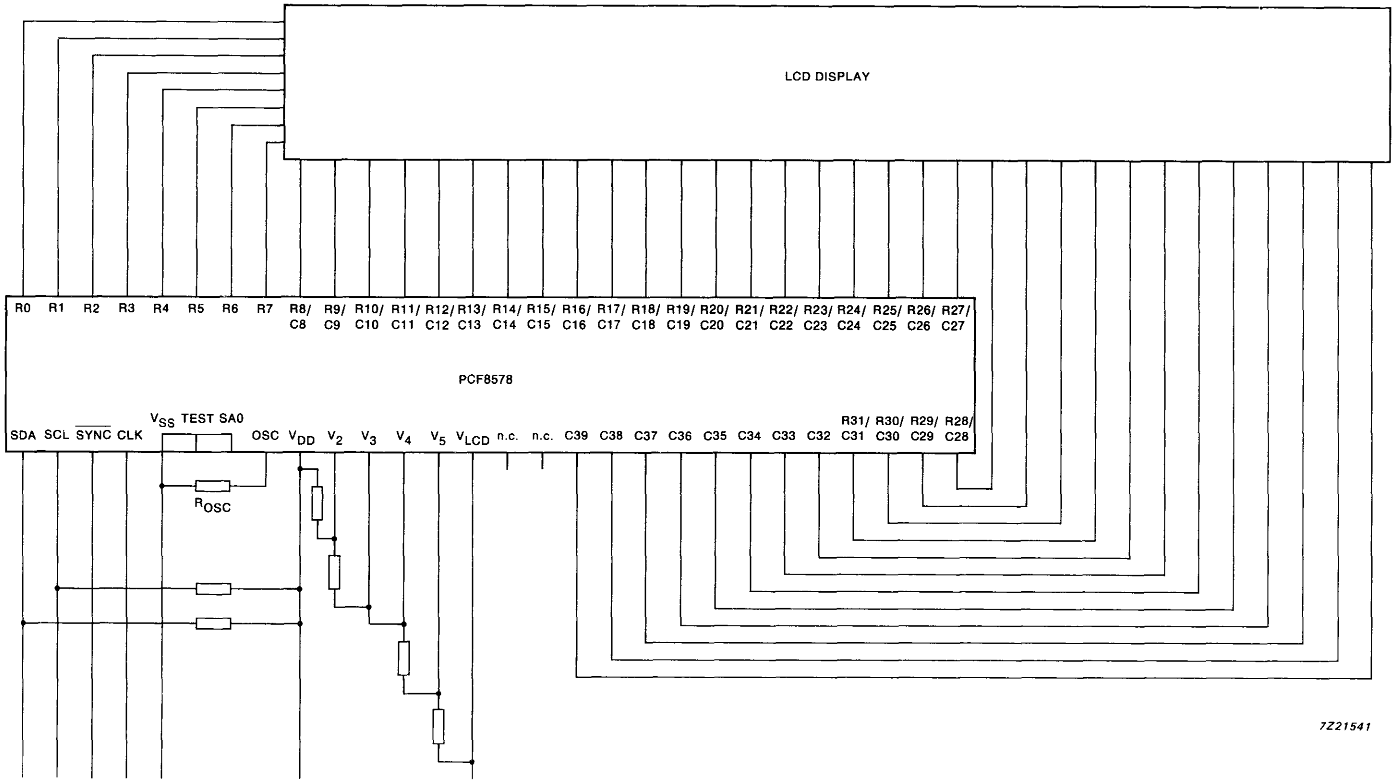


Fig.21 Stand-alone application using 8 rows and 32 columns.

APPLICATION INFORMATION (continued)

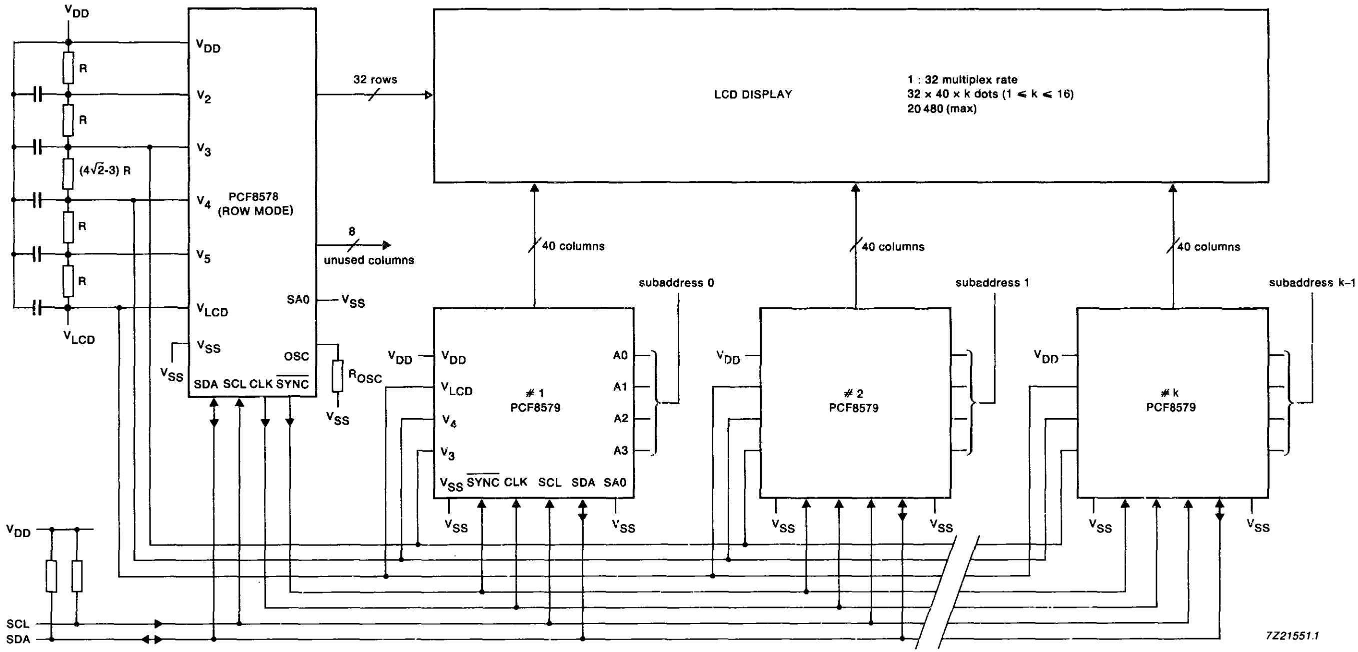


Fig.22 Typical LCD driver system with 1:32 multiplex rate.

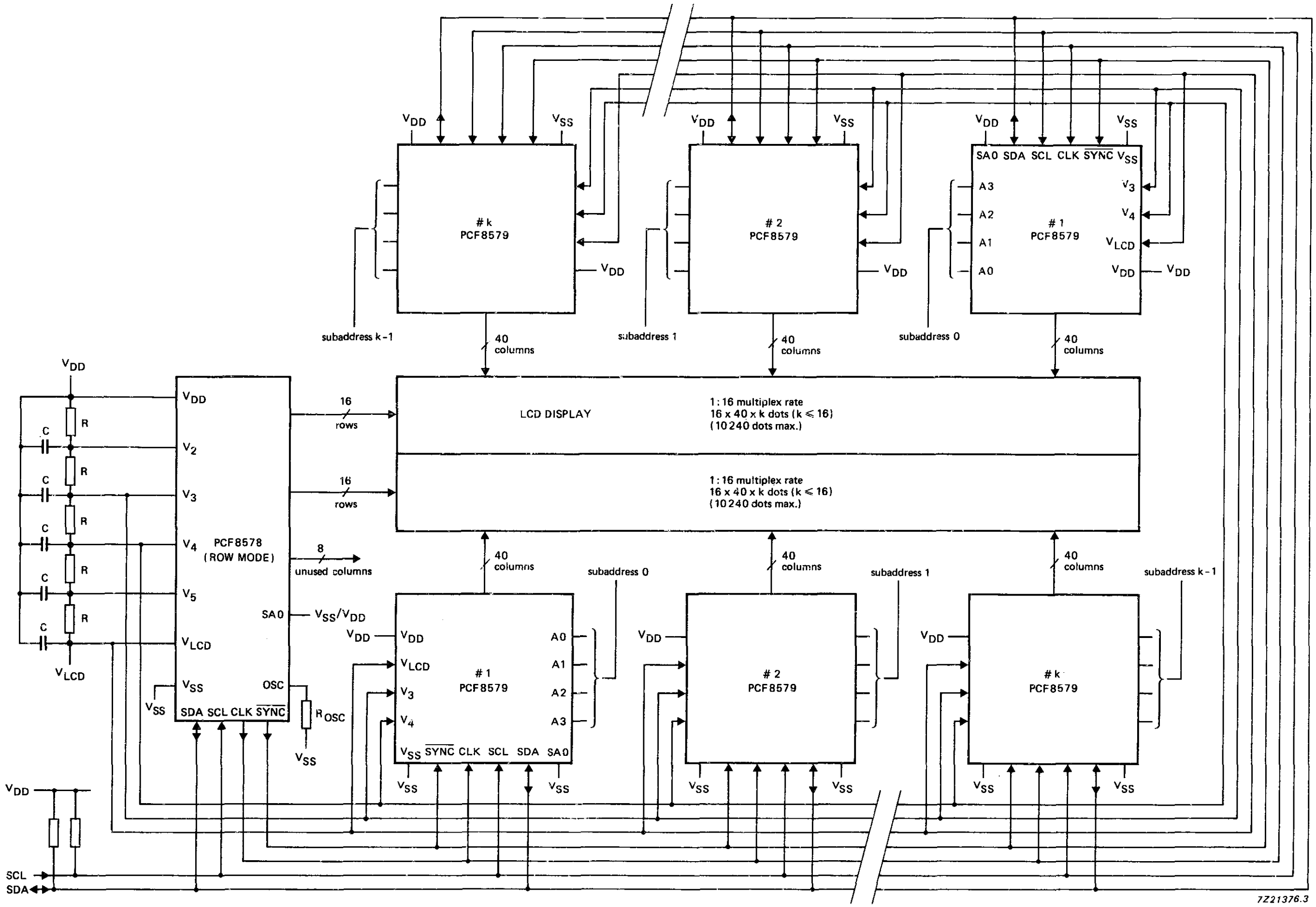


Fig.23 Split screen application with 1:16 multiplex rate for improved contrast.

APPLICATION INFORMATION (continued)

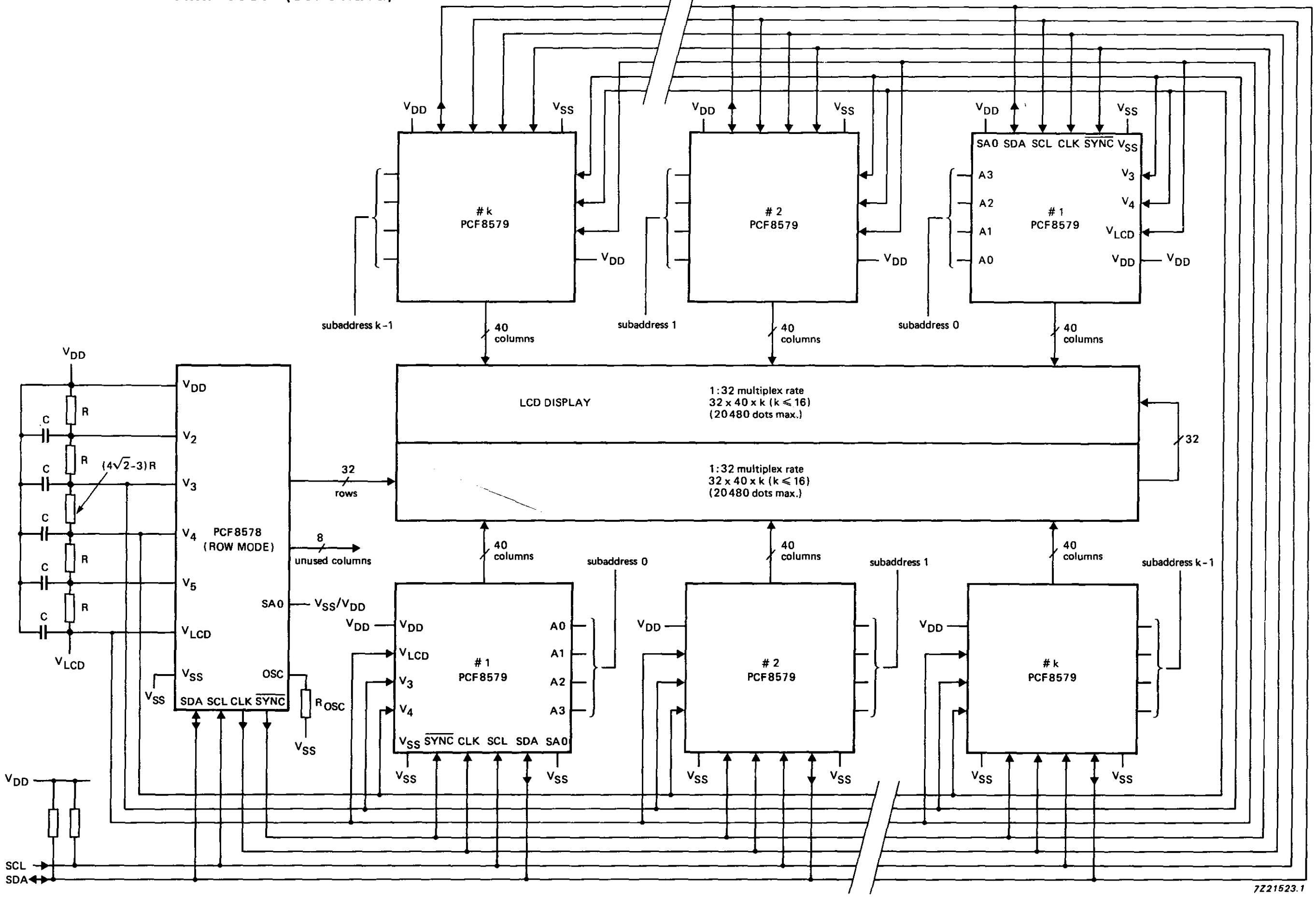


Fig.24 Split screen application with 1:32 multiplex rate.

DEVELOPMENT DATA

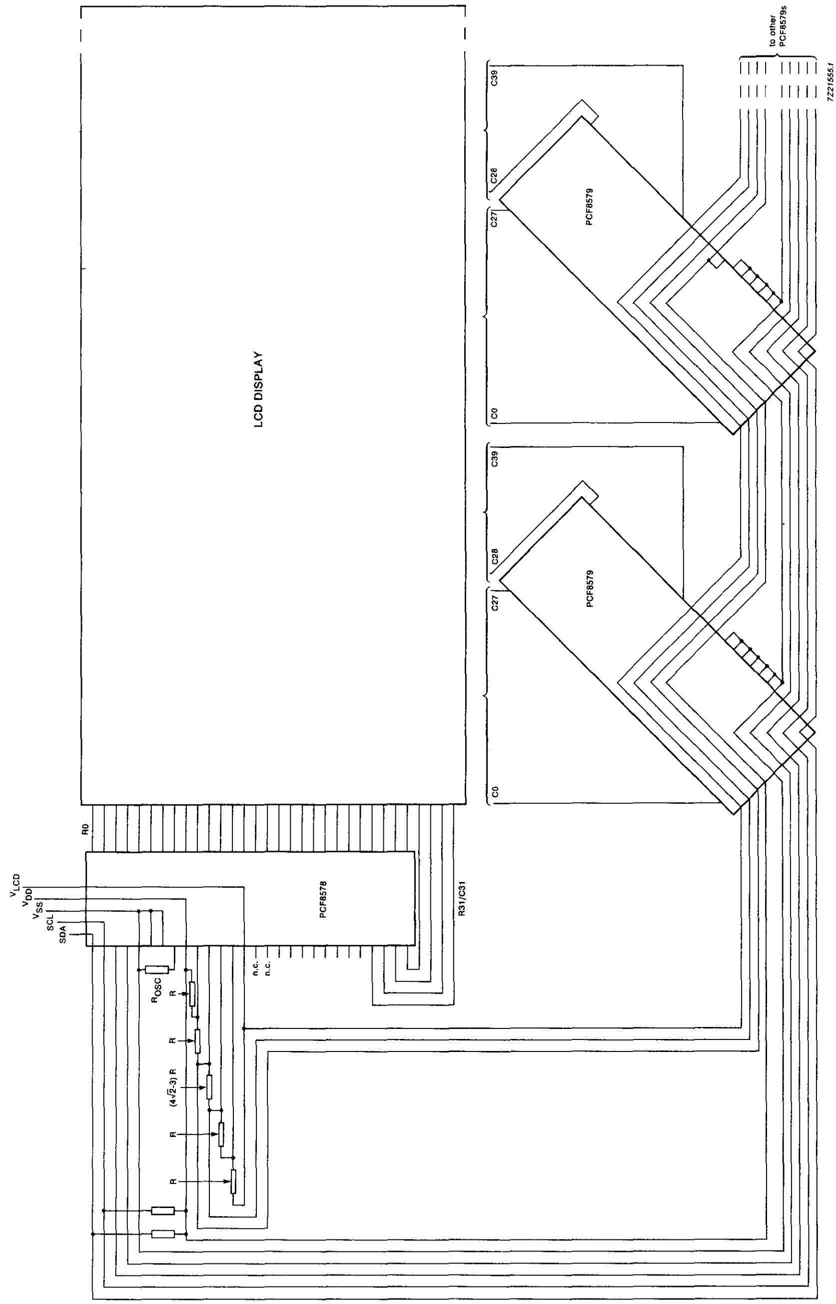
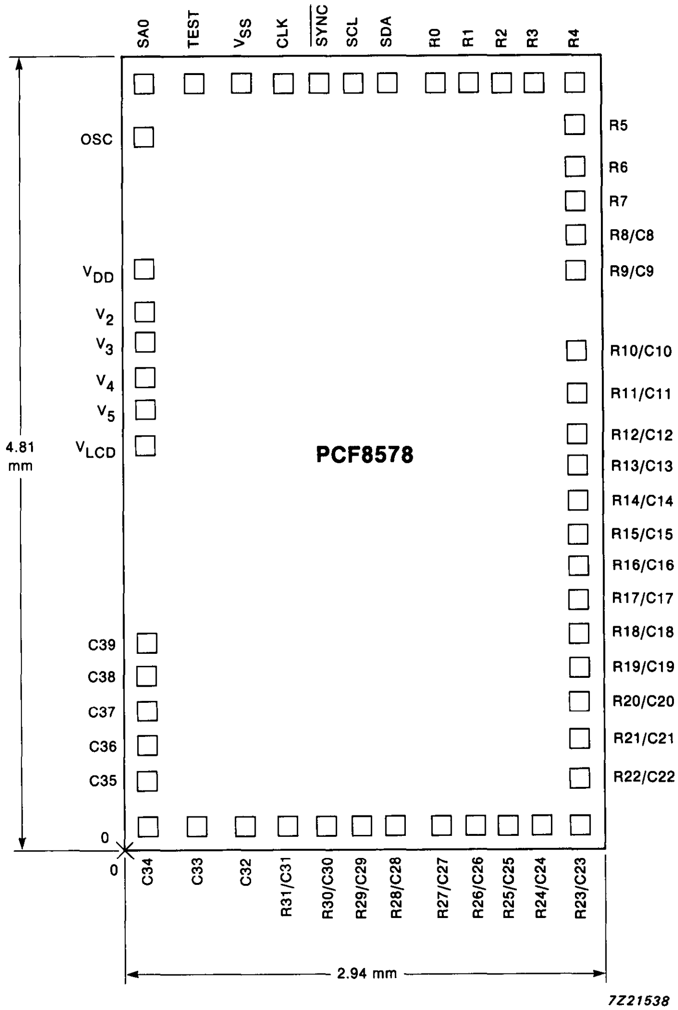


Fig.25 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.14 mm^2
Bonding pad dimensions: 120 μm x 120 μm.

Fig.26 Bonding pad locations.

Table 6 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.26.

pad	X	Y	pad	X	Y
SDA	1642	4642	R27/C27	1936	160
SCL	1438	4642	R26/C26	2140	160
$\overline{\text{SYNC}}$	1234	4642	R25/C25	2344	160
CLK	1000	4642	R24/C24	2548	160
V_{SS}	742	4642	R23/C23	2776	160
TEST	454	4642	R22/C22	2776	424
SA0	160	4642	R21/C21	2776	670
OSC	160	4318	R20/C20	2776	886
V_{DD}	160	3514	R19/C19	2776	1096
V_2	160	3274	R18/C18	2776	1300
V_3	160	3064	R17/C17	2776	1504
V_4	160	2860	R16/C16	2776	1708
V_5	160	2656	R15/C15	2776	1912
V_{LCD}	160	2452	R14/C14	2776	2116
n.c.	–	–	R13/C13	2776	2320
n.c.	–	–	R12/C12	2776	2524
C39	160	1252	R11/C11	2776	2752
C38	160	1048	R10/C10	2776	3004
C37	160	844	R9/C9	2776	3502
C36	160	628	R8/C8	2776	3706
C35	160	406	R7	2776	3916
C34	160	160	R6	2776	4132
C33	454	160	R5	2776	4378
C32	742	160	R4	2776	4642
R31/C31	1000	160	R3	2548	4642
R30/C30	1234	160	R2	2344	4642
R29/C29	1438	160	R1	2140	4642
R28/C28	1642	160	R0	1936	4642

CHIP-ON GLASS INFORMATION

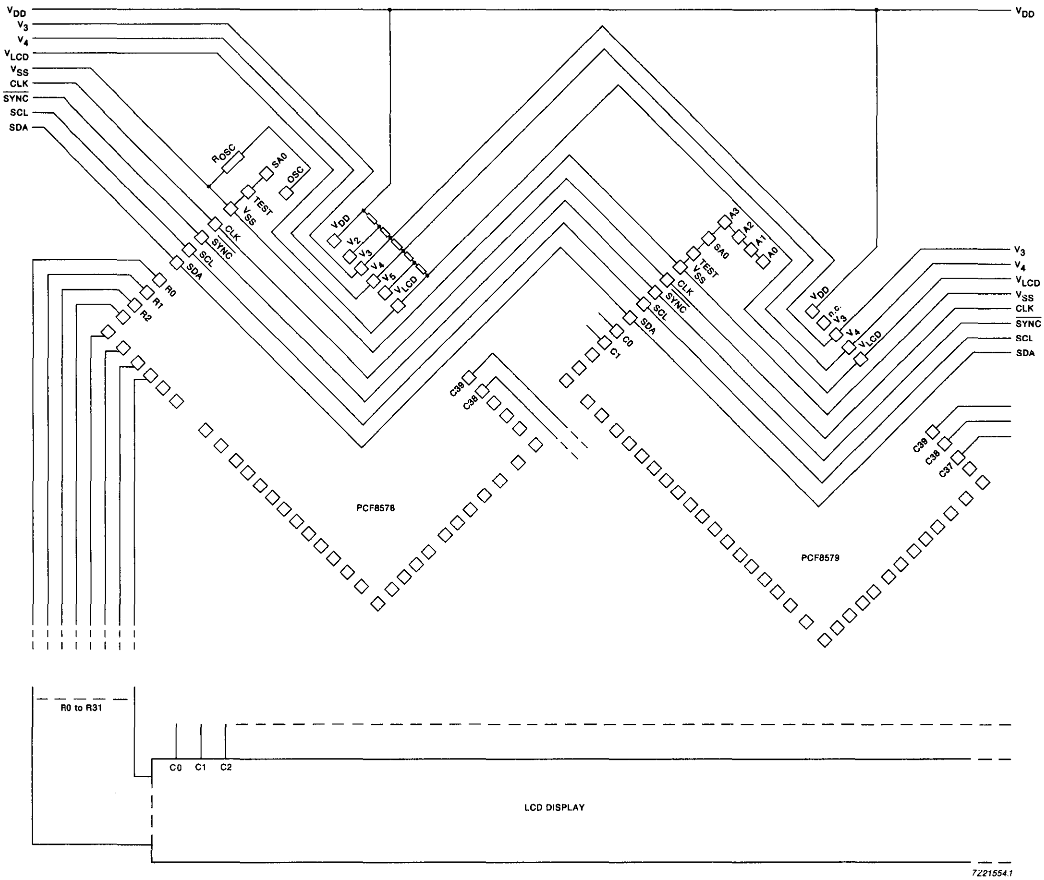


Fig.27 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.27

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

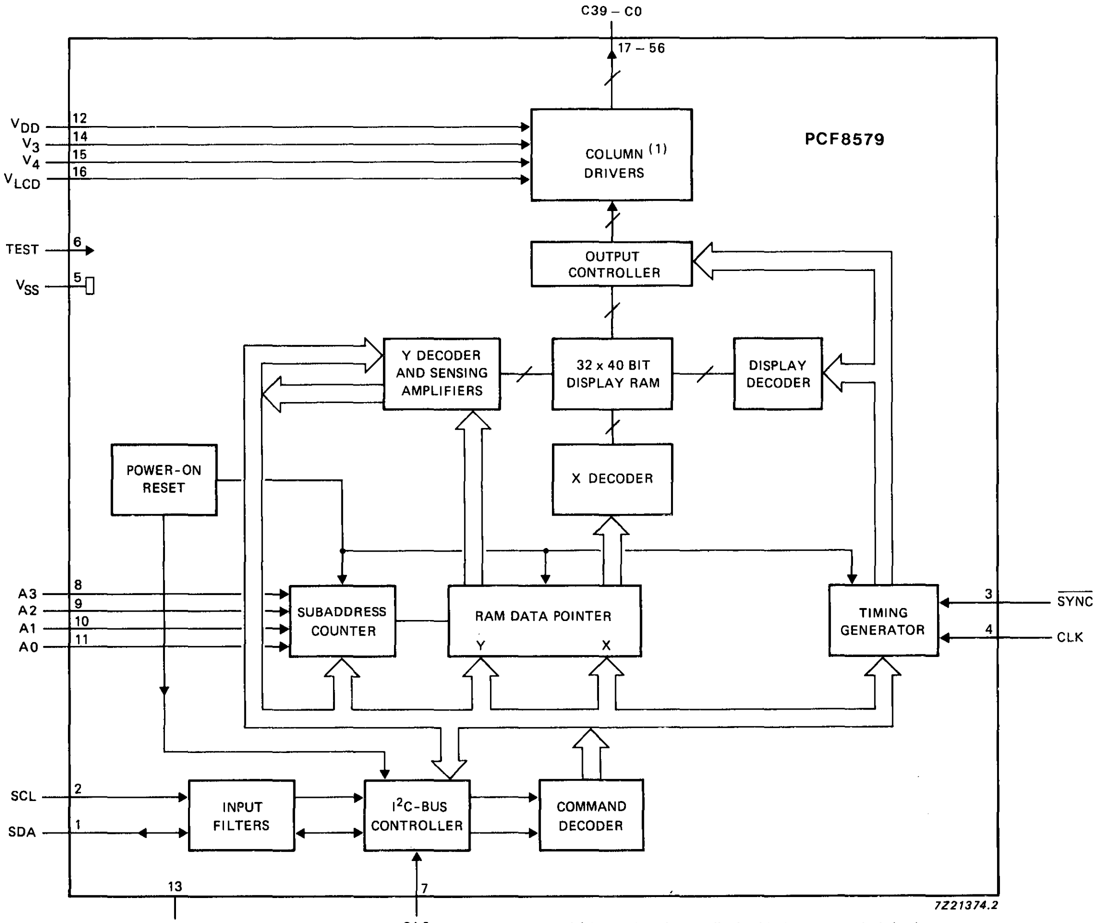
- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.



(1) LCD voltage levels, all other blocks operate at logic levels

Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

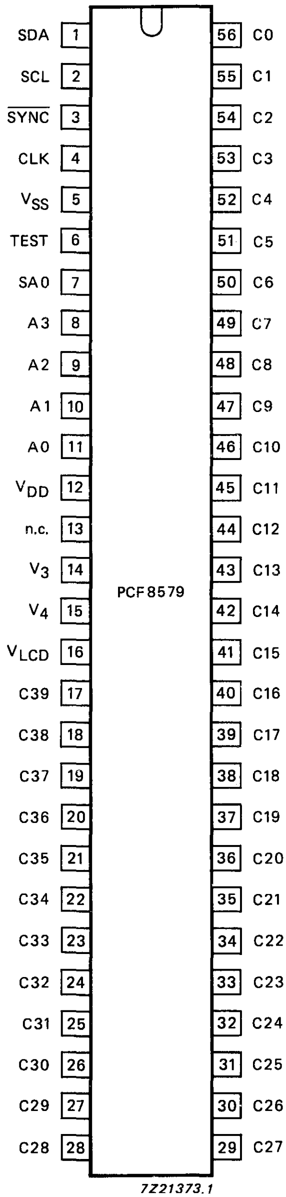
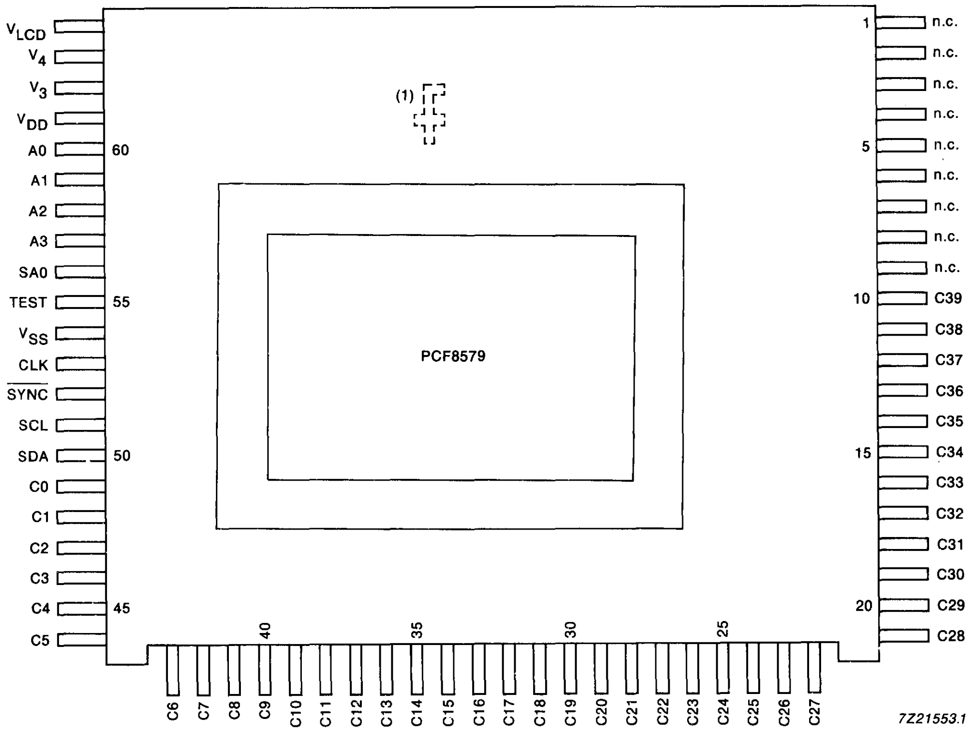


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SO122.

mnemonic	pin no.		description
	SOT190	SO122	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 - 11	57 - 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 - 15	62 - 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 - 56	10 - 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

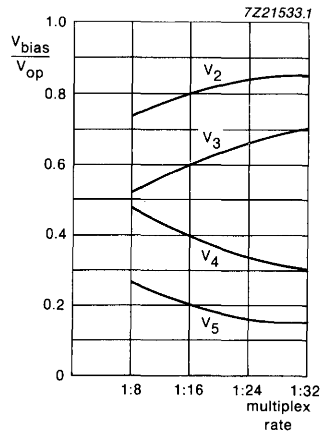


Fig.3 LCD bias voltage as a function of the multiplex rate.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578)
2. 1:32 multiplex rate
3. start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

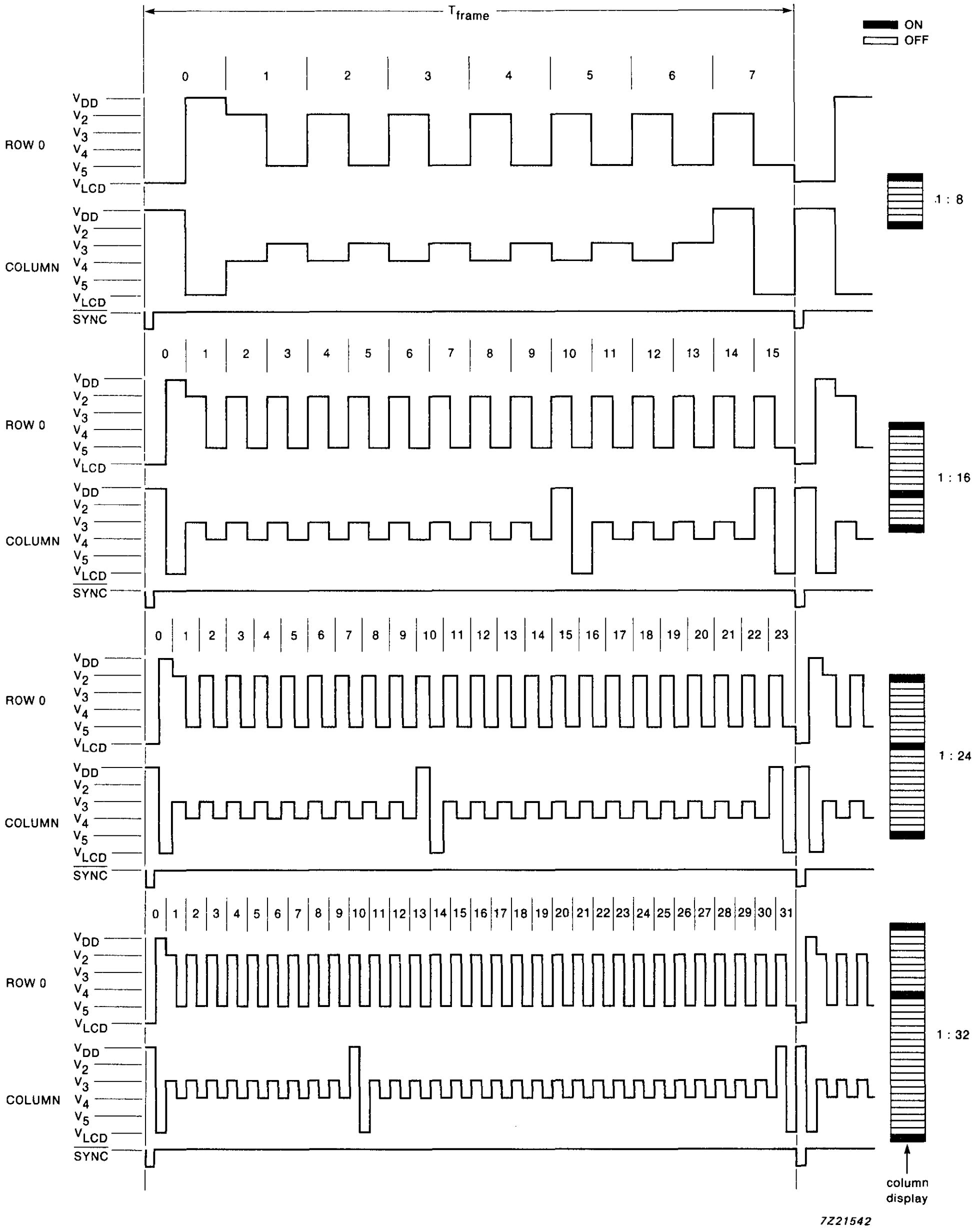
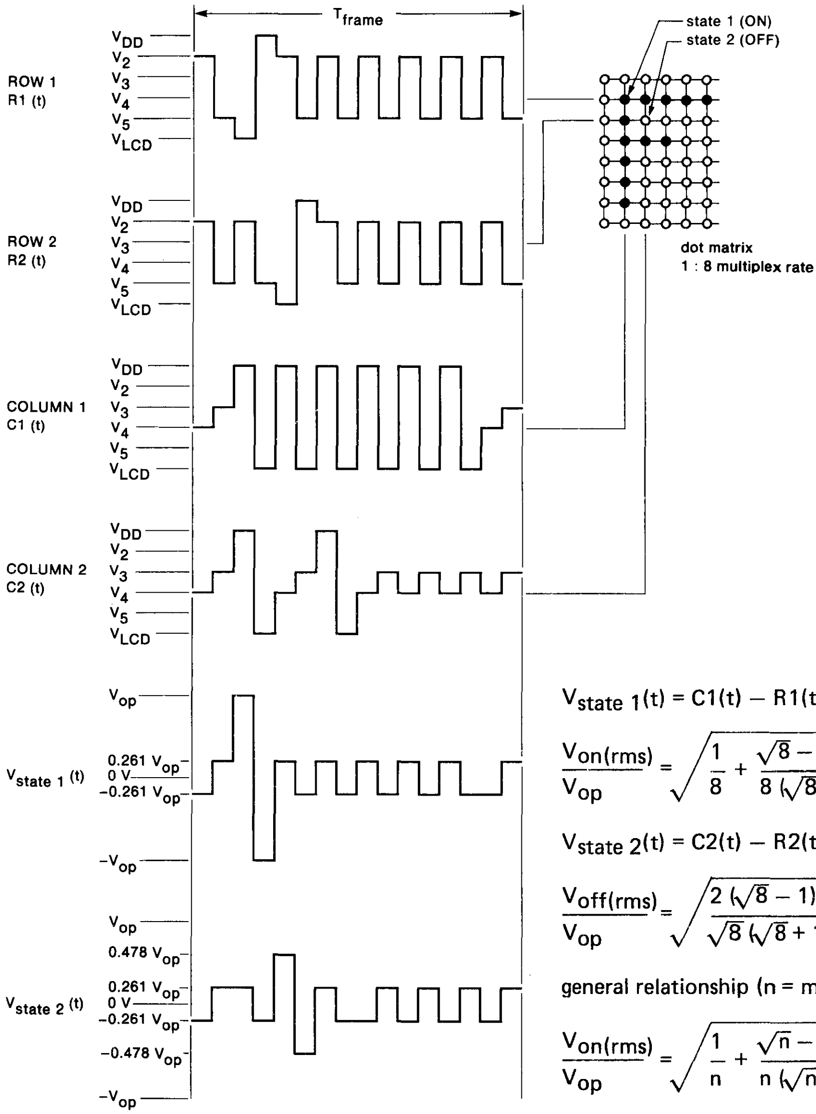


Fig.4 LCD row/column waveforms.

DEVELOPMENT DATA



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

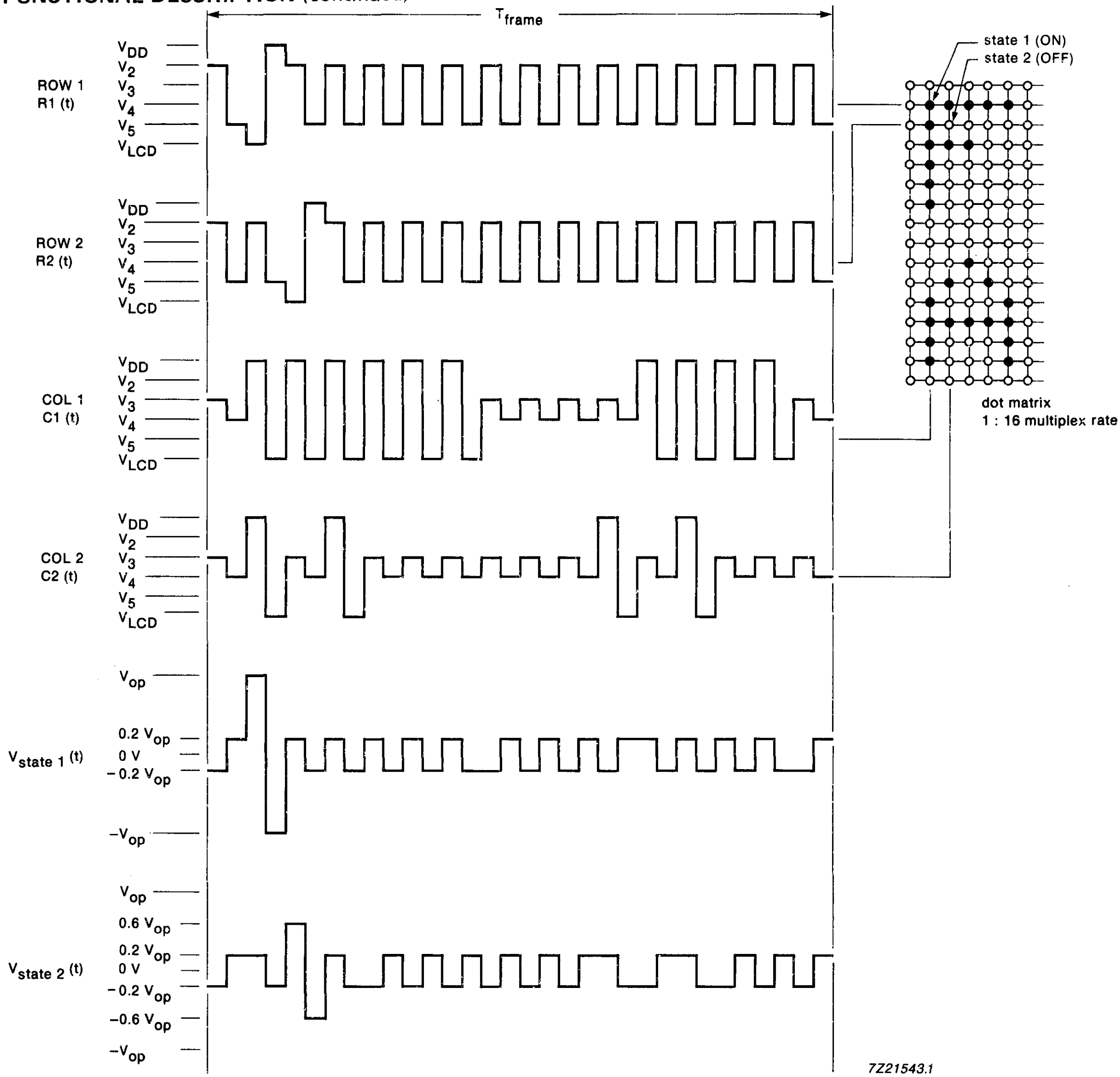
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.5 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{\text{SYNC}}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into or read from the display RAM, as specified by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrival take place, only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

FUNCTIONAL DESCRIPTION (continued)

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD, via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9. This feature is useful when scrolling in alphanumeric applications.

DEVELOPMENT DATA

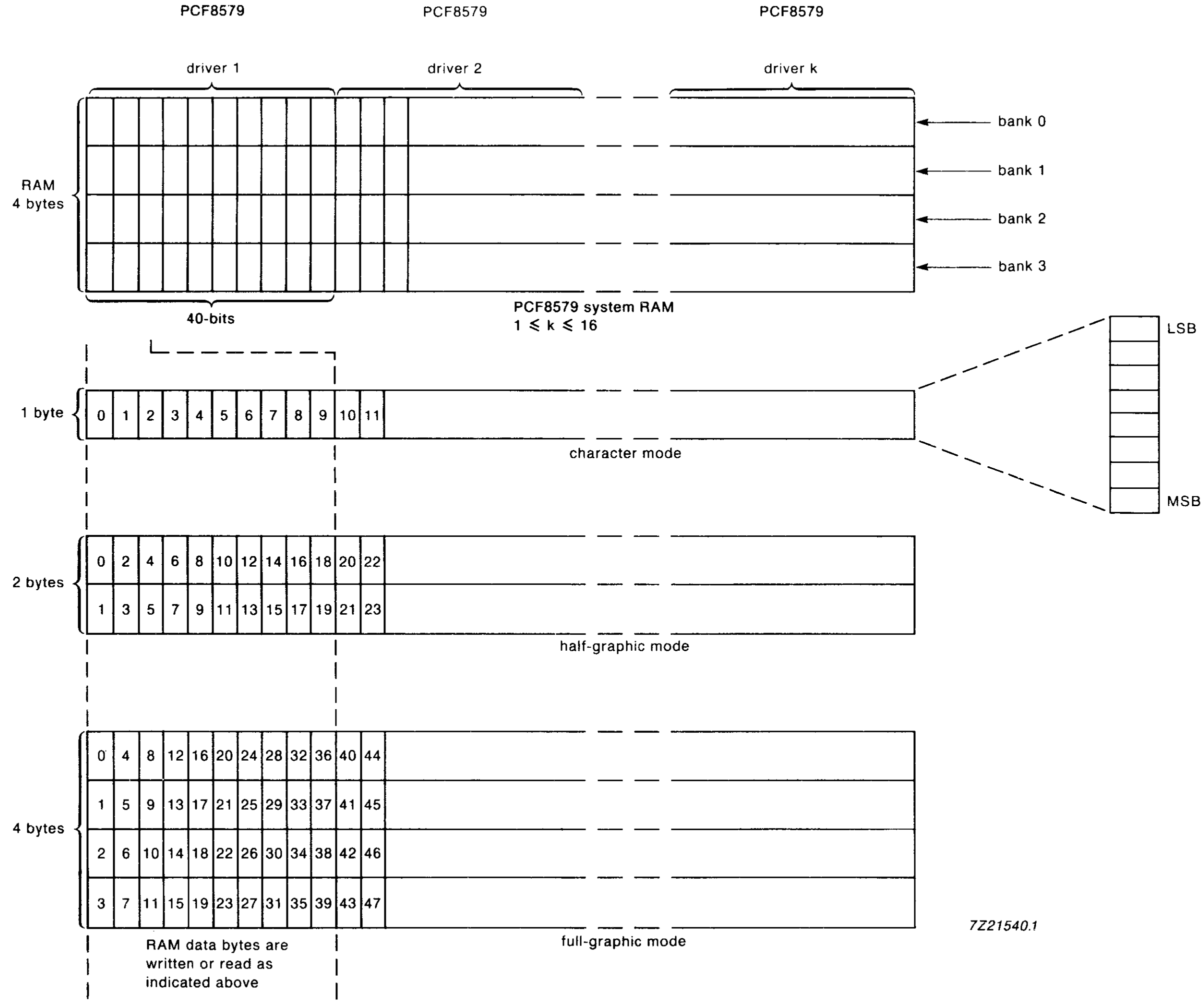


Fig.7 RAM ACCESS mode.

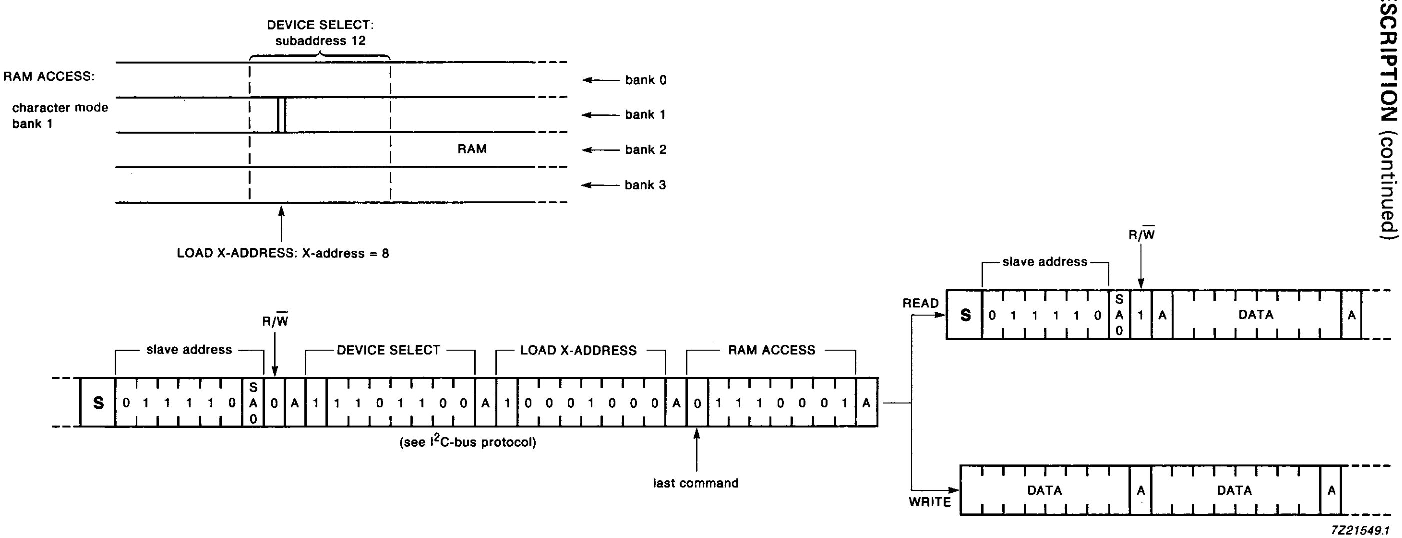


Fig.8 Example of commands specifying initial data byte RAM locations.

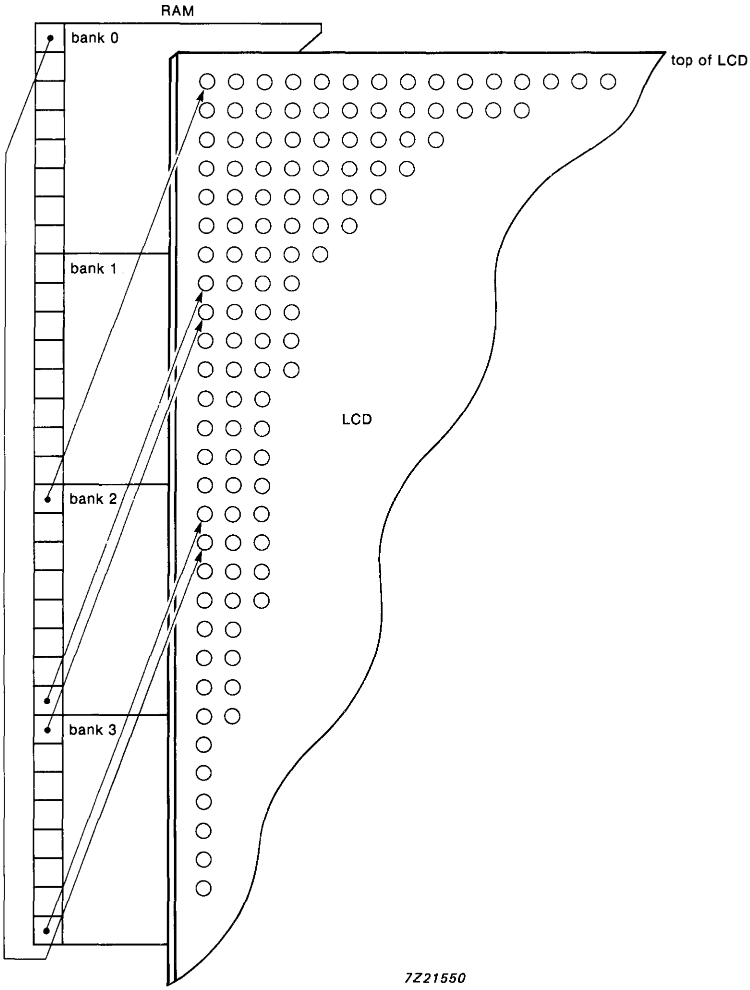


Fig.9 Relationship between display and SET START BANK;
1:32 multiplex rate and start bank = 2.

I^2C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I^2C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I^2C-bus for very large applications.
(b) the use of two types of LCD multiplex schemes on the same I^2C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I^2C-bus protocol is shown in Fig. 10. All communications are initiated with a start condition (S) from the I^2C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I^2C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0, A1, A2 and A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated with an unique hardware subaddress.

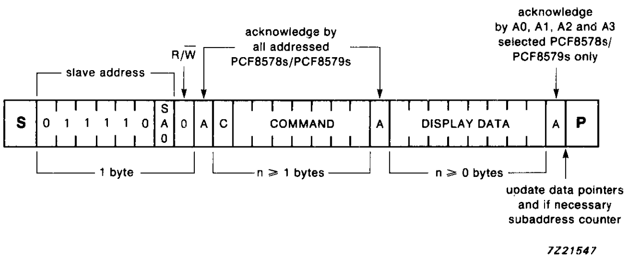


Fig.10(a) Master transmits to slave receiver (WRITE mode).

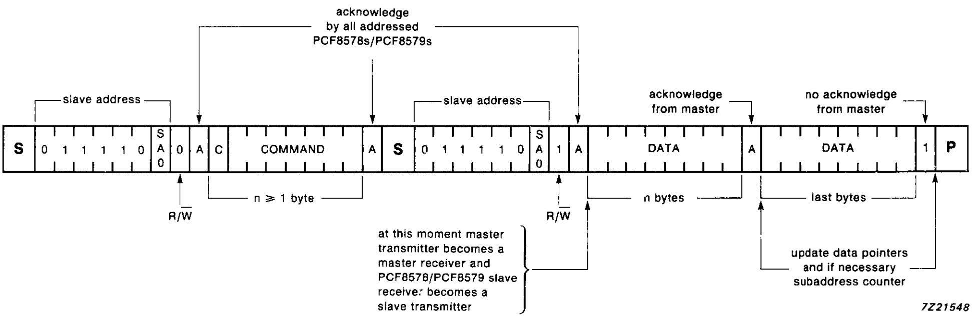


Fig.10(b) Master reads after sending command string (WRITE commands; READ data).

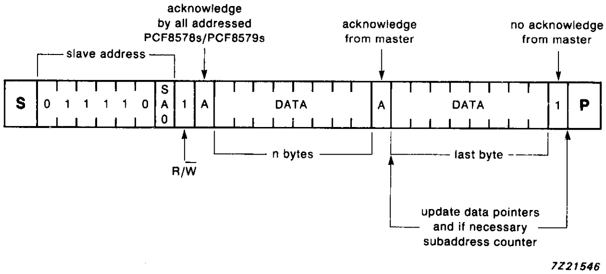
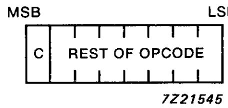


Fig.10(c) Master reads-slave immediately after sending slave address (READ mode).

I²C-BUS PROTOCOL (continued)

Command decoder

The command decoder indentifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.11 General format of command byte.

The five commands available to the PCF8579 are defined in Table 2.

Table 2 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic modes, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

Table 3 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C | 1 | 0 | T | E1 E0 | M1 M0	LCD drive mode — bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status — bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type — bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C | 1 1 1 1 1 | B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C | 1 1 0 | A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

I^2C BUS PROTOCOL (continued)

Table 3 (continued)

command / opcode	options	description
RAM ACCESS C | 1 1 1 | G1 G0 | Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed* 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C | 0 | X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

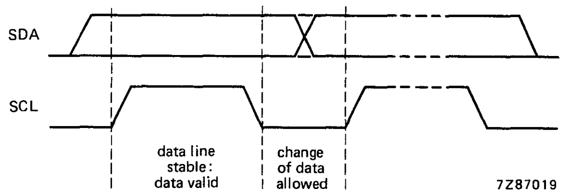


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

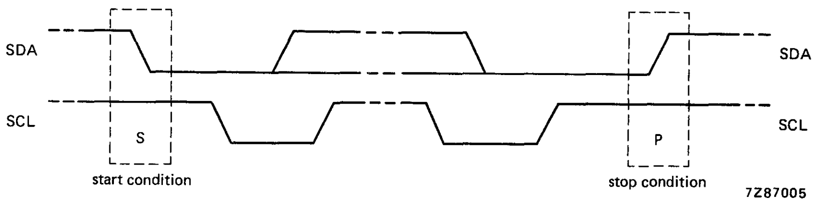


Fig.13 Definition of start and stop condition.

CHARACTERISTICS OF THE I^{2}C-BUS (continued)

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

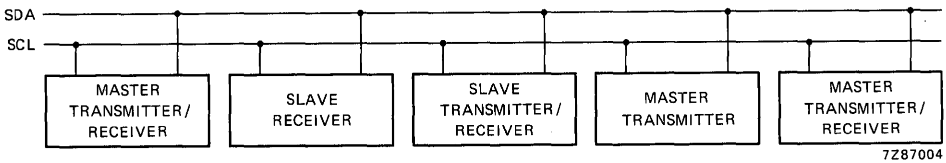


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

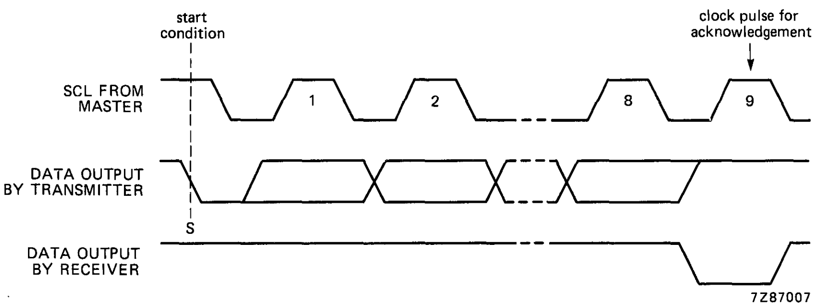


Fig.15 Acknowledgement on the I^{2}C-bus.

Note

The general characteristics and detailed specification of the I^{2}C-bus is available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{I1}	V_{SS} −0.5	V_{DD} + 0.5	V
V_3 to V_4	V_{I2}	V_{LCD} −0.5	V_{DD} + 0.5	V
Output voltage range at SDA	V_{O1}	V_{SS} −0.5	V_{DD} + 0.5	V
C0 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} + 0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{\text{SYNC}}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; $V_{LCD} = V_{DD}$ −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU; STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD; STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU; DAT}$	250	–	–	ns
Data hold time		$t_{HD; DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU; STO}$	4.0	–	–	μs

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty cycle.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu A$.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

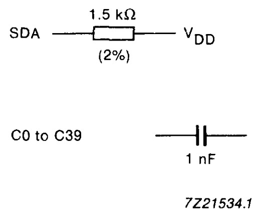


Fig.16 Test loads.

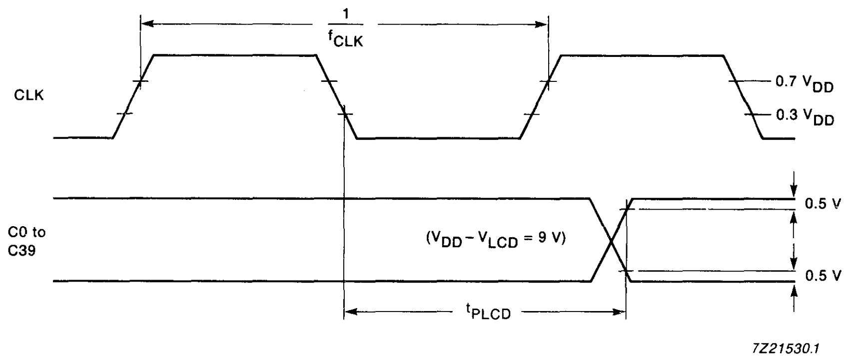


Fig.17 Driver timing waveforms.

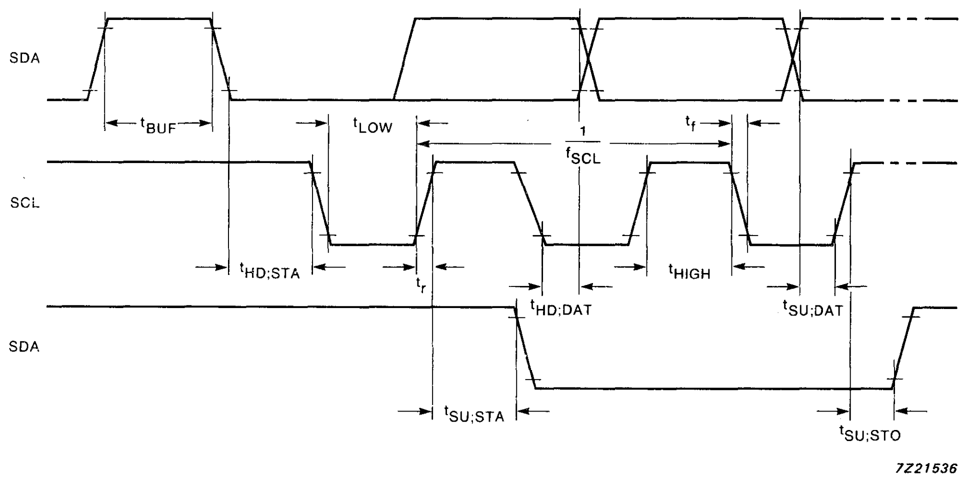


Fig.18 I^2C-bus timing waveforms.

DEVELOPMENT DATA

APPLICATION INFORMATION

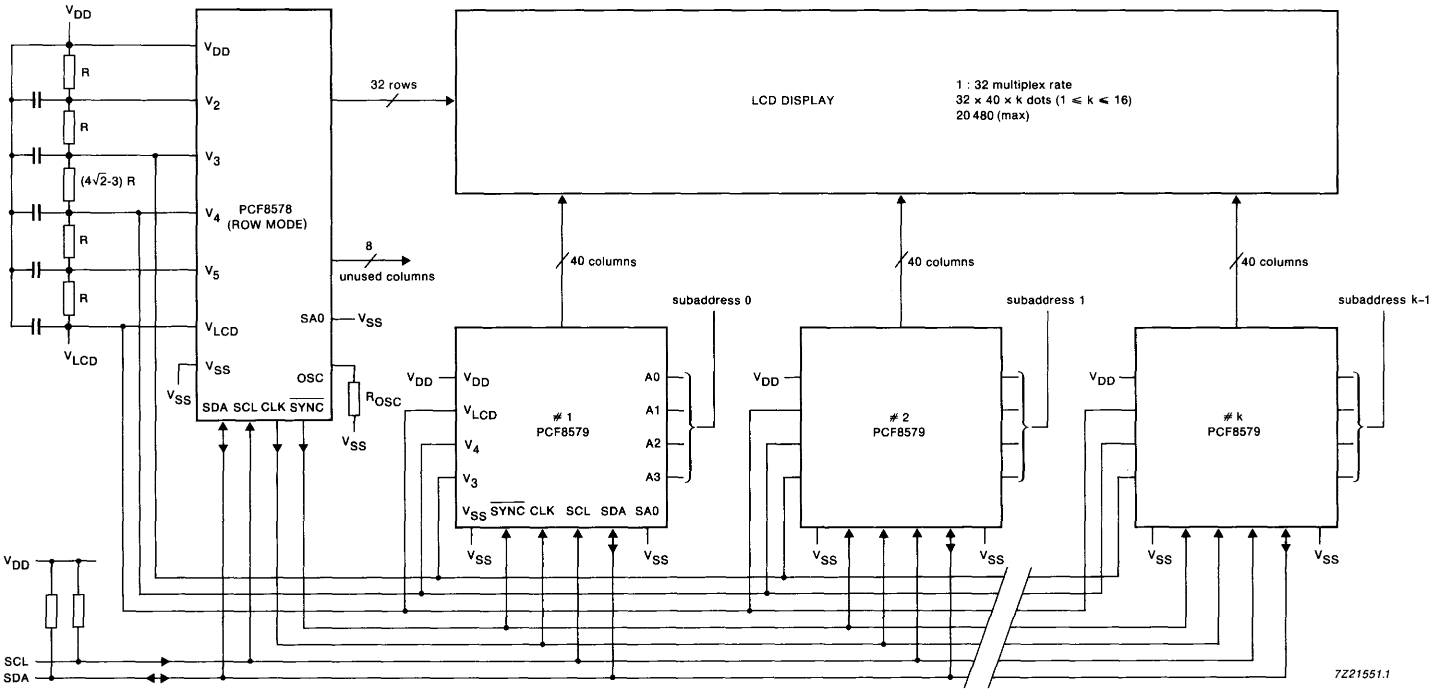


Fig.19 Typical LCD driver system with 1:32 multiplex rate.

DEVELOPMENT DATA

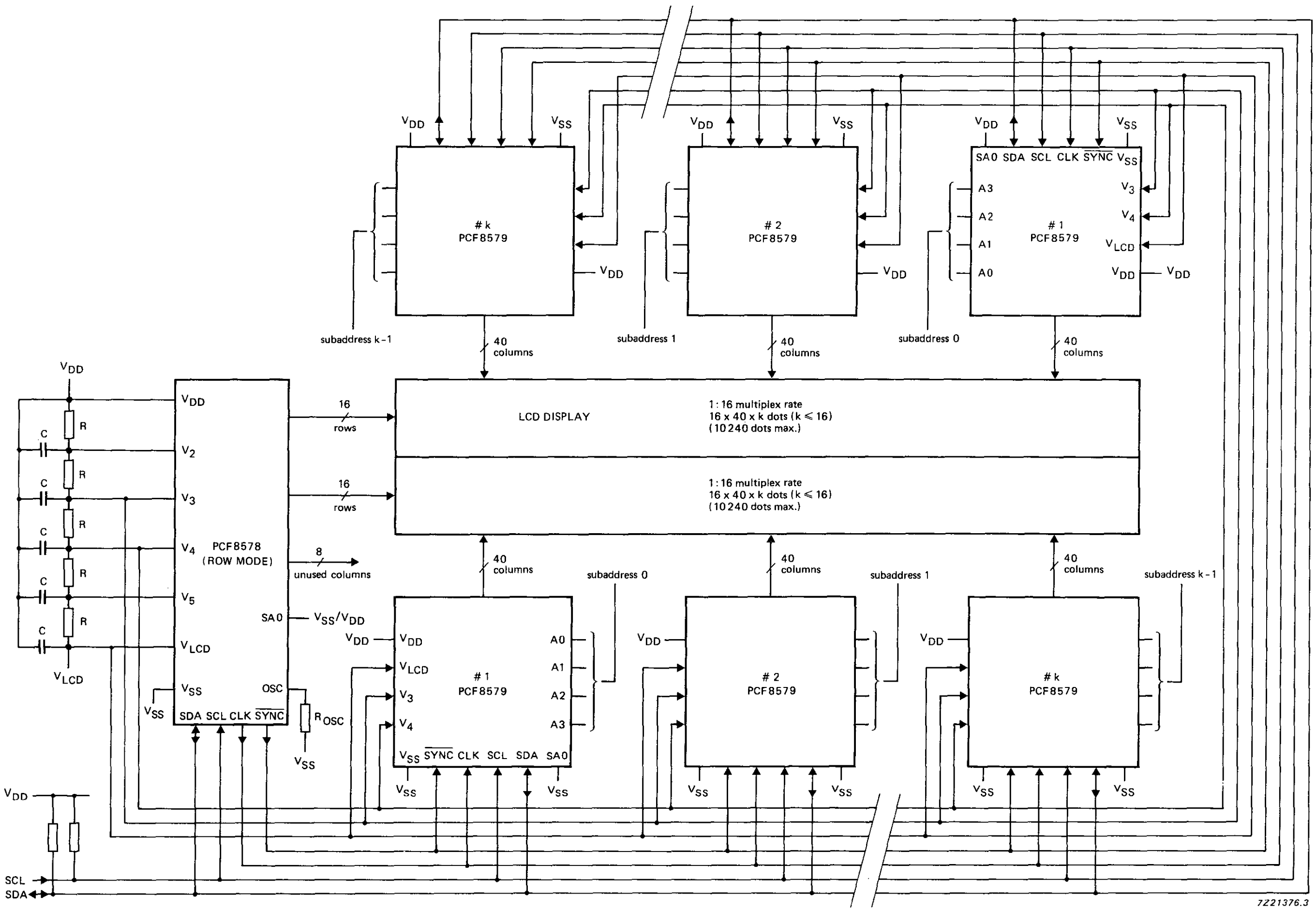


Fig.20 Split screen application with 1:16 multiplex rate for improved contrast.

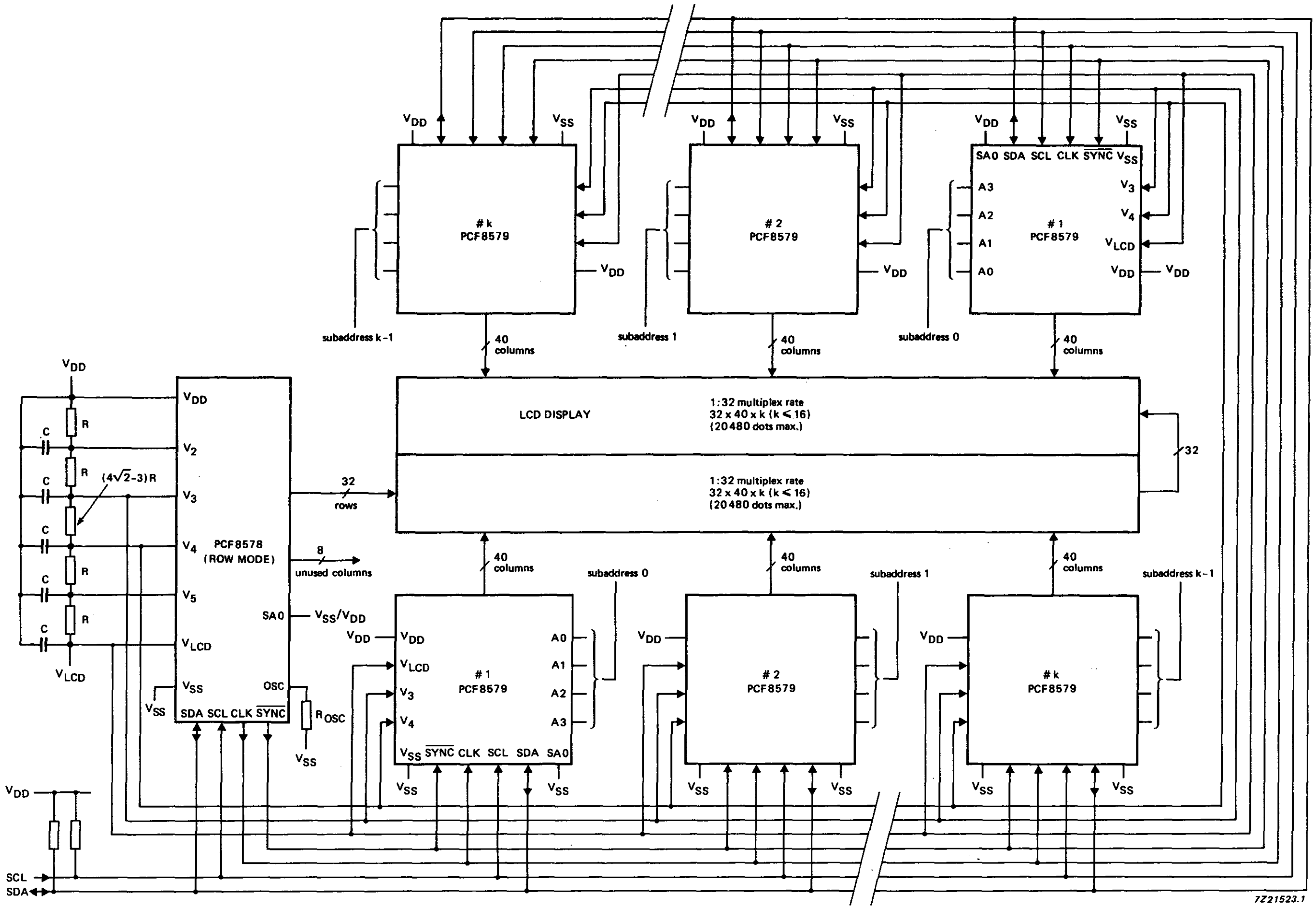


Fig.21 Split screen application using double screen with 1:32 multiplex rate.

DEVELOPMENT DATA

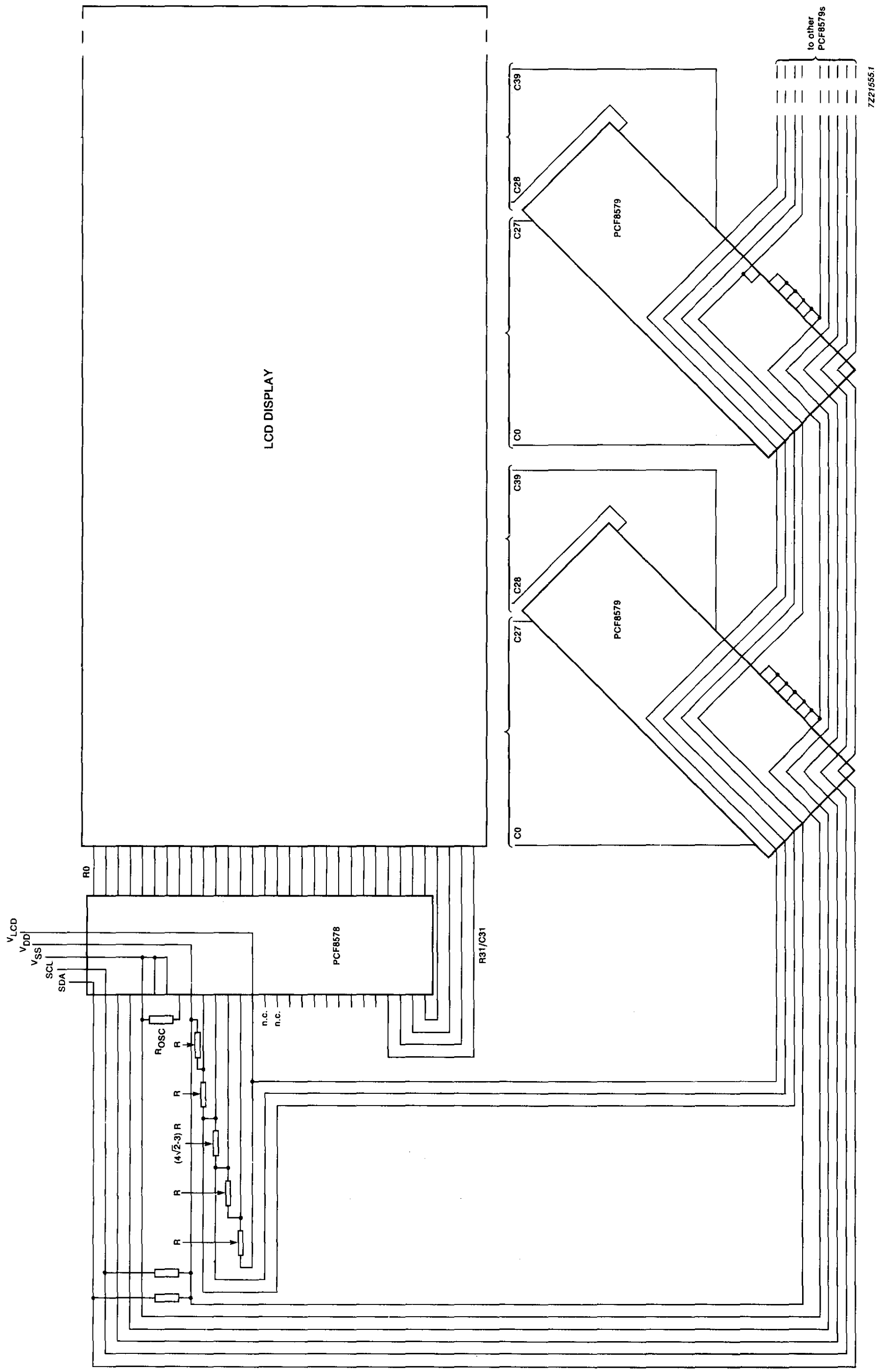
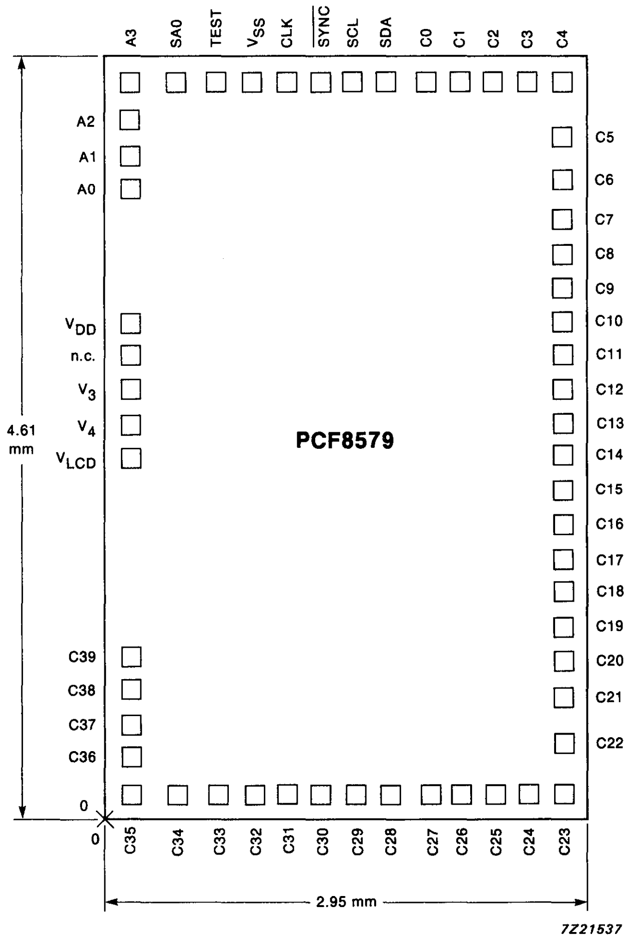


Fig.22 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 13.6 mm^2
Bonding pad dimensions: 120 μm x 120 μm

Fig.23 Bonding pad locations.

Table 4 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.23.

pad	X	Y	pad	X	Y
SDA	1726	4444	C27	1972	160
SCL	1522	4444	C26	2176	160
$\overline{\text{SYNC}}$	1318	4444	C25	2380	160
CLK	1114	4444	C24	2584	160
V_{SS}	910	4444	C23	2788	160
TEST	688	4444	C22	2788	472
SA0	442	4444	C21	2788	736
A3	160	4444	C20	2788	976
A2	160	4222	C19	2788	1180
A1	160	4018	C18	2788	1384
A0	160	3814	C17	2788	1588
V_{DD}	160	3010	C16	2788	1792
n.c.	160	2806	C15	2788	1996
V_2	160	2602	C14	2788	2200
V_3	160	2398	C13	2788	2404
V_{LCD}	160	2194	C12	2788	2608
C39	160	994	C11	2788	2812
C38	160	790	C10	2788	3016
C37	160	586	C9	2788	3220
C36	160	382	C8	2788	3424
C35	160	160	C7	2788	3628
C34	442	160	C6	2788	3868
C33	688	160	C5	2788	4132
C32	910	160	C4	2788	4444
C31	1114	160	C3	2584	4444
C30	1318	160	C2	2380	4444
C29	1522	160	C1	2176	4444
C28	1726	160	C0	1972	4444

DEVELOPMENT DATA

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHIP-ON GLASS INFORMATION

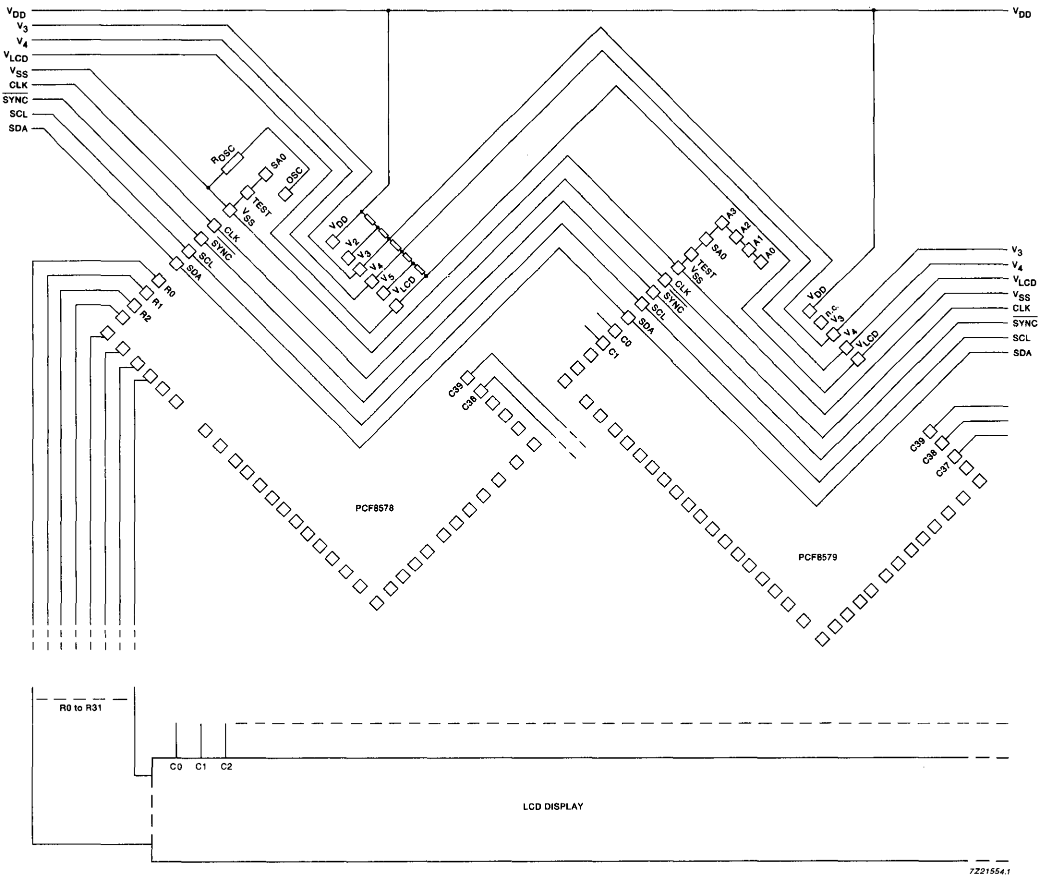


Fig.24 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.24

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

256 × 8-bit STATIC CMOS EEPROM WITH I^2C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I^2C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I^2C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator.
If the latter is used an RC time constant must be connected to pin 7 or 13.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

A version with automotive temperature range −40 to + 125 °C (PCF8582B) and a version with extended temperature range −40 to + 85 °C (PCF8582C) are in preparation.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

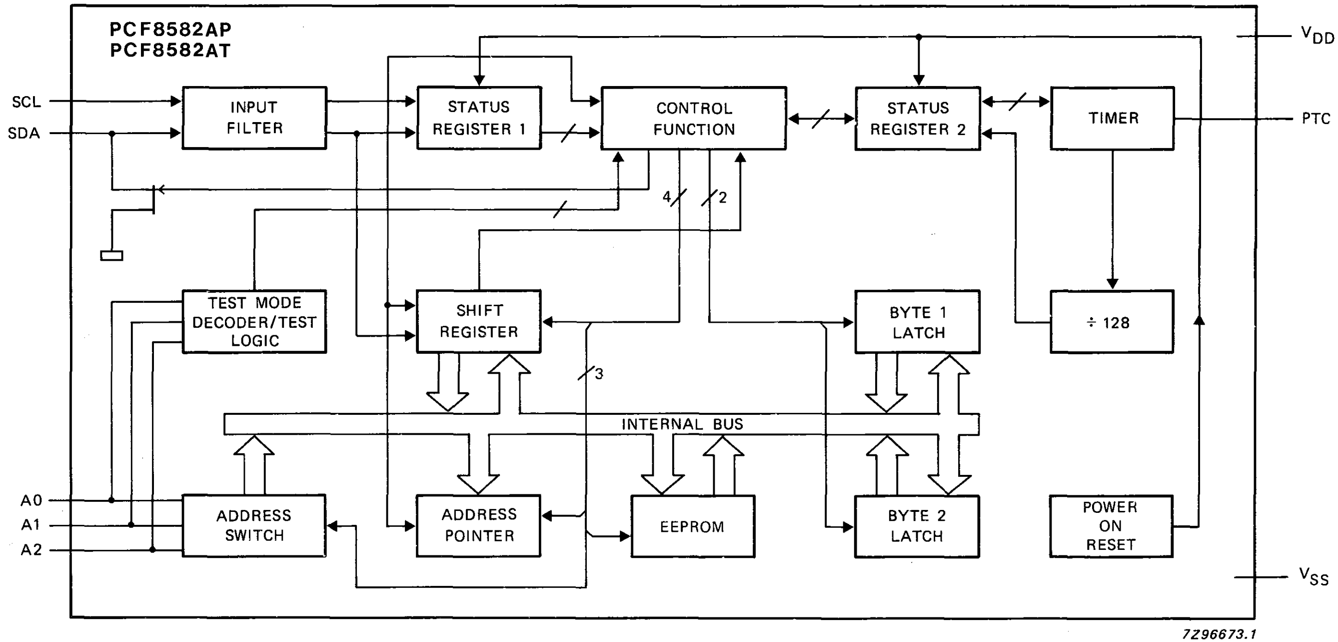
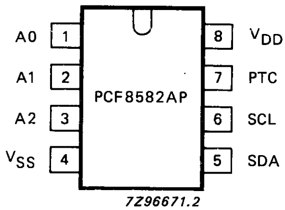
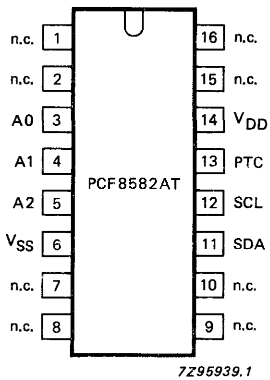


Fig. 1 Block diagram.



1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^{2}C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

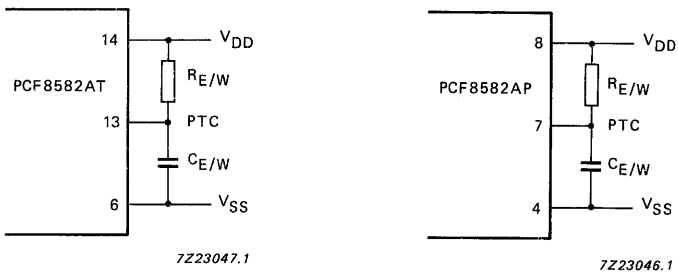
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^{2}C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.

DEVELOPMENT DATA



Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

FUNCTIONAL DESCRIPTION

Characteristics of the I^2C-bus

The I^2C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I^2C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

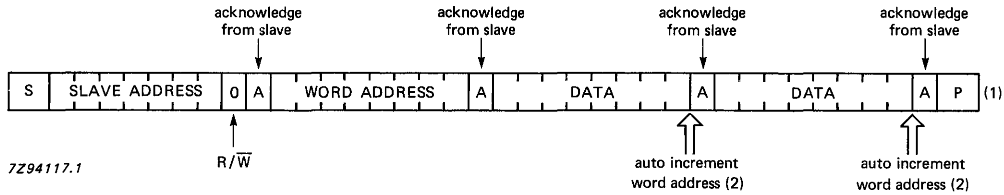
Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I^2C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

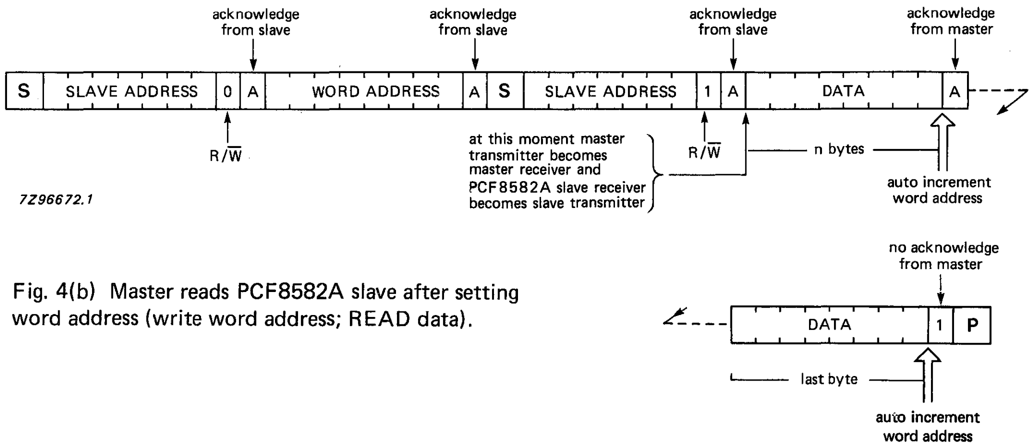


Fig. 4(b) Master reads PCF8582A slave after setting word address (write word address; READ data).

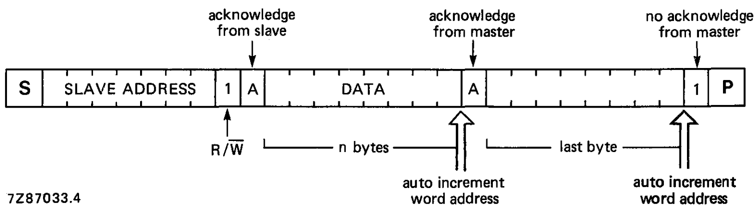


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).*

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W̄

* The device can be used as read only without the programming clock.

DEVELOPMENT DATA

I^2C-bus timing

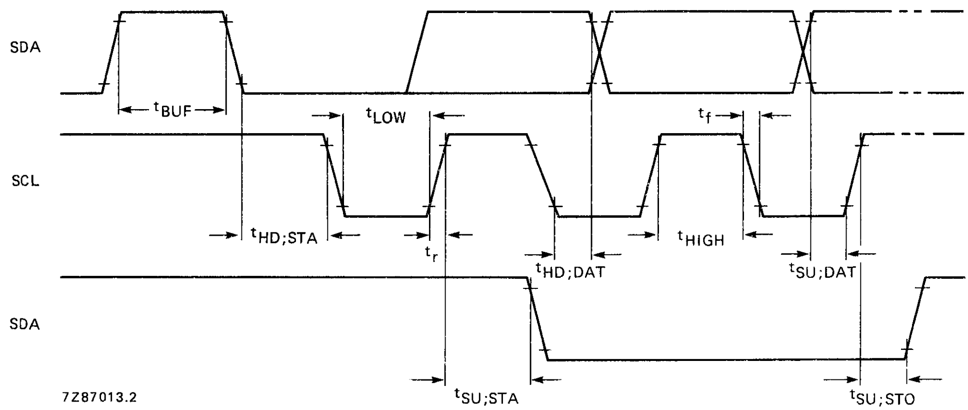
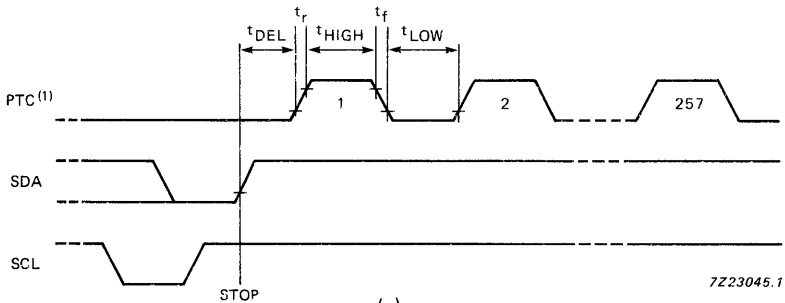
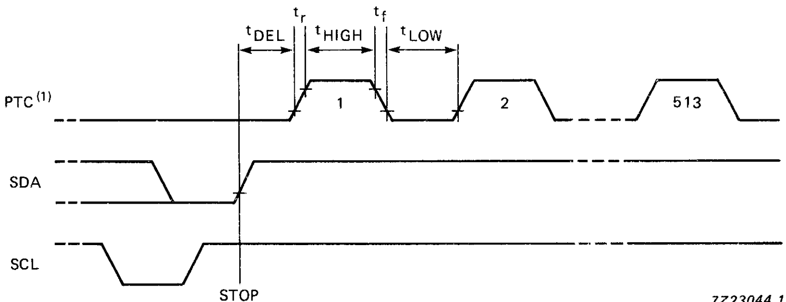


Fig. 5 I^2C-bus timing.



(a)



(b)

(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	−	1	mA
Output current	$\|I_O\|$	−	10	mA

DEVELOPMENT DATA

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	V_{OH} = V_{DD}	I_{LO}	–	–	1	μA
Input leakage current (SCL)	V_I = V_{DD} or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C-bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	5	–	40	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	10	–	50	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

CHARACTERISTICS (continued)

E/W programming time control

A. Using external resistor $R_{E/W}$ and capacitor $C_{E/W}$ (see Table 1)

Table 1 Recommended R, C combinations

$R_{E/W}$ (kΩ) note 1	$C_{E/W}$ (nF) note 2	$t_{E/W}$ (typ.) (ms) note 3
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5 (note 4)

Notes to Table 1

1. Maximum tolerance is 10%.
2. Maximum tolerance is 5%.
3. Actual E/W lines are mainly influenced by the tolerances in values of R and C.
4. Minimum allowed $t_{E/W}$ is 5 ms (see CHARACTERISTICS).

B. Using an external clock (see Table 2 and Fig.6)

Table 2 E/W programming time control using an external clock

parameters	symbol	min.	max.	unit
frequency	f_p	10.0	50.0	kHz
period LOW	t_{LOW}	10.0	—	s
period HIGH	t_{HIGH}	10.0	—	s
rise time	t_r	—	300	ns
fall time	t_f	—	300	ns
delay time	t_d	0	—	ns

CLOCK CALENDAR WITH 256 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1.0 V to 6 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

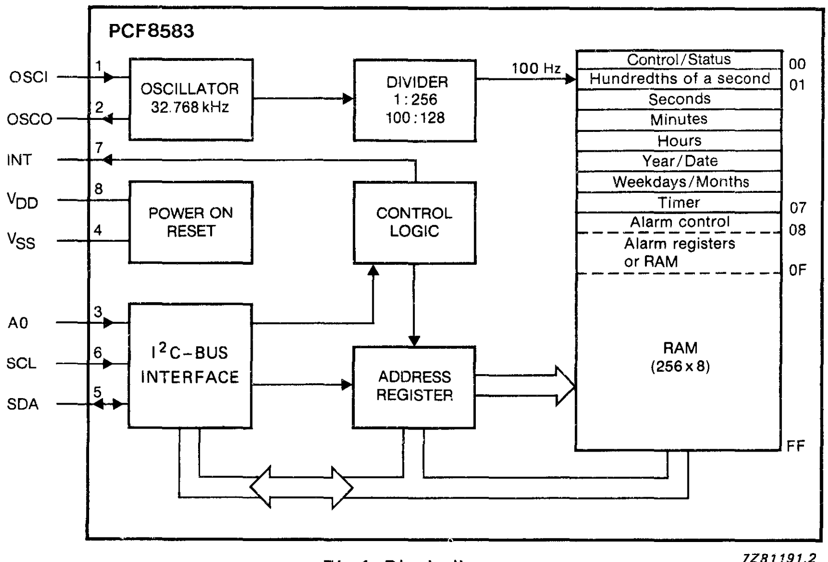


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176A).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input
2	OSCO	oscillator output
3	A0	address input
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C-bus
6	SCL	serial clock line } I^2C-bus
7	INT	open drain interrupt output (active low)
8	V_{DD}	positive supply

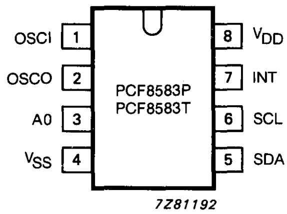


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	–0.8	+ 7.0	V
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	–	50	mA
Input voltage range	V_I	–0.8 to V_{DD}	+ 0.8	V
DC input current	I_I	–	10	mA
DC output current	I_O	–	10	mA
Power dissipation per package	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	–40	+ 85	°C
Storage temperature range	T_{stg}	–65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^{2}C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

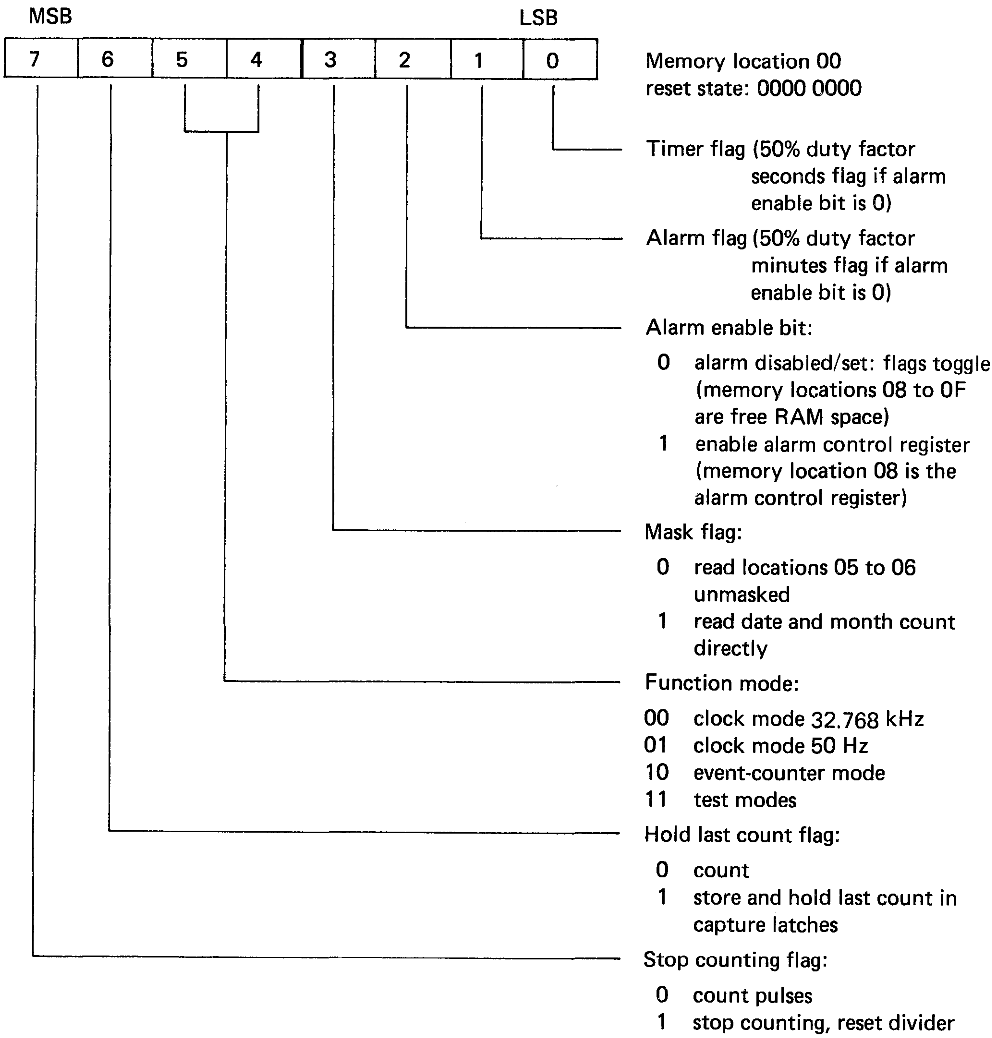


Fig.3 Control/status register.

DEVELOPMENT DATA

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

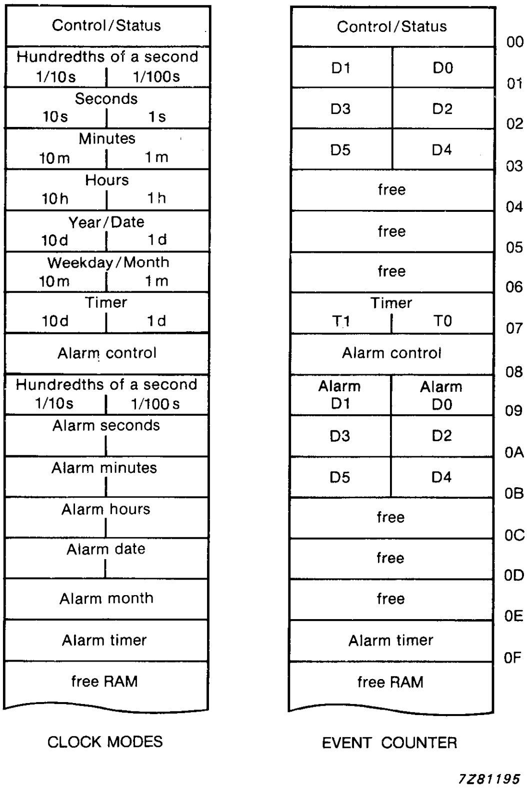


Fig.4 Register arrangement.

Counter registers (continued)

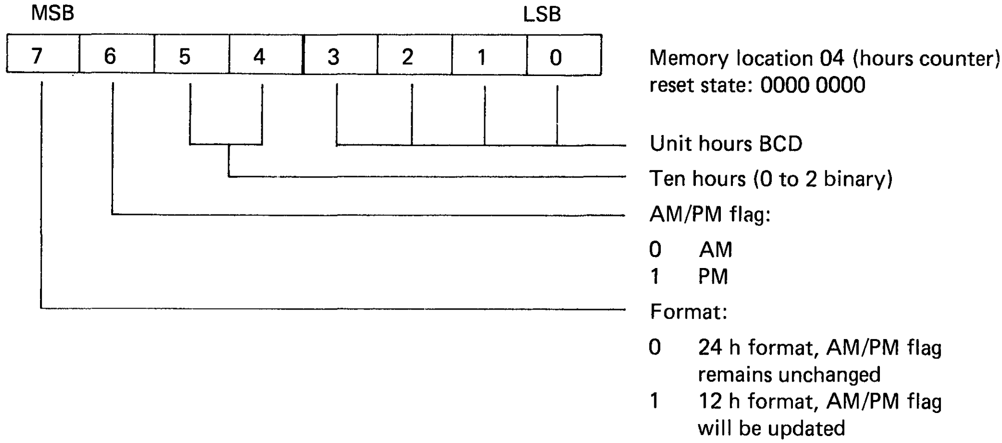


Fig.5 Format of the hours counter.

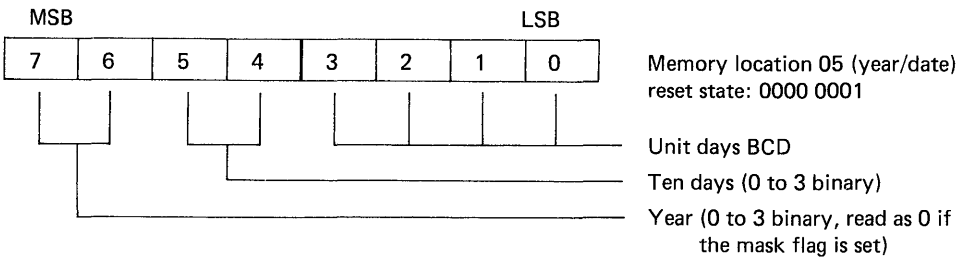


Fig.6 Format of the year/date counter.

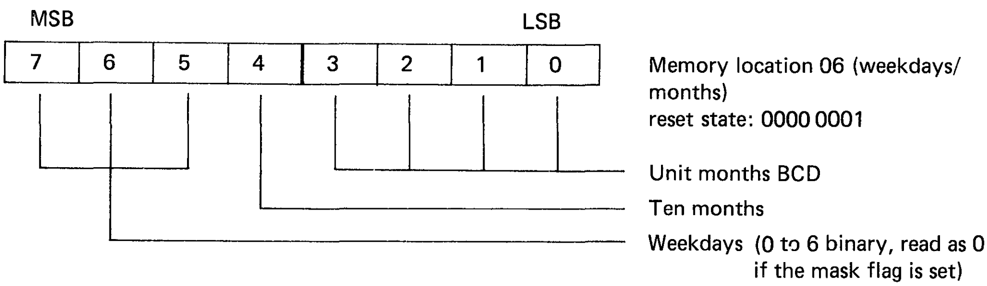


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

MSB LSB

7	6	5	4	3	2	1	0

Memory location 08
reset state: 0000 0000

Timer function:

000 no timer
001 hundredths of a second
010 seconds
011 minutes
100 hours
101 days
110 not used
111 test mode, all counters in parallel

Timer interrupt enable:

0 timer flag, no interrupt
1 timer flag, interrupt

Clock alarm function:

00 no clock alarm
01 daily alarm
10 weekday alarm
11 dated alarm

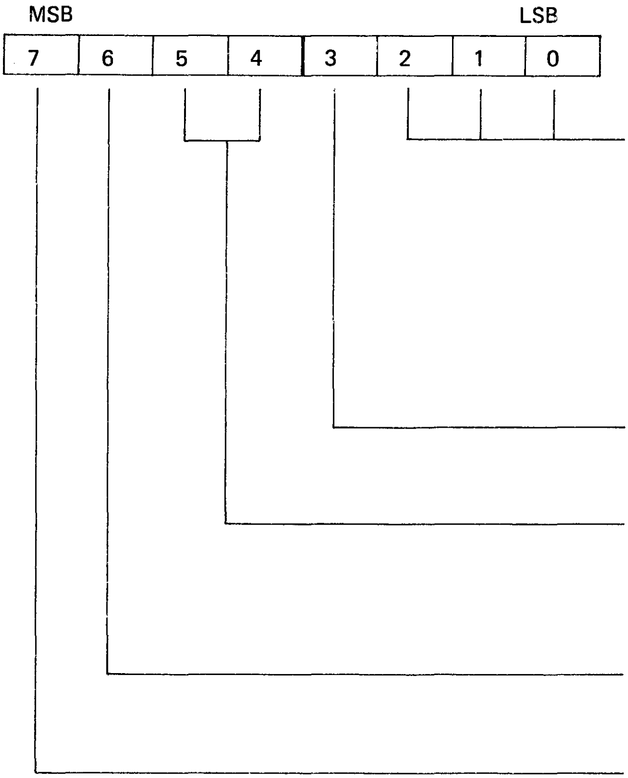
Timer alarm enable:

0 no timer alarm
1 timer alarm

Alarm interrupt enable:
(Valid only when "alarm enable" in control/status register is set)

0 alarm flag, no interrupt
1 alarm flag, interrupt

Fig.8a Alarm control register, clock modes.



Memory location 08
reset state: 0000 0000

Timer function:

000 no timer
001 units
010 100
011 10 000
100 1 000 000
101 not allowed
110 not allowed
111 test mode, all counters in parallel

Timer interrupt enable:

0 timer flag, no interrupt
1 timer flag, interrupt

Event alarm function:

00 no event alarm
01 event alarm
10 not allowed
11 not allowed

Timer alarm enable:

0 no timer alarm
1 timer alarm

Alarm interrupt enable:

0 alarm flag, no interrupt
1 alarm flag, interrupt

Fig.8b Alarm control register, event-counter mode.

DEVELOPMENT DATA

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Note: In the 12 h mode bits 6 and 7 of the alarm hours register must be the same as the hours counter.

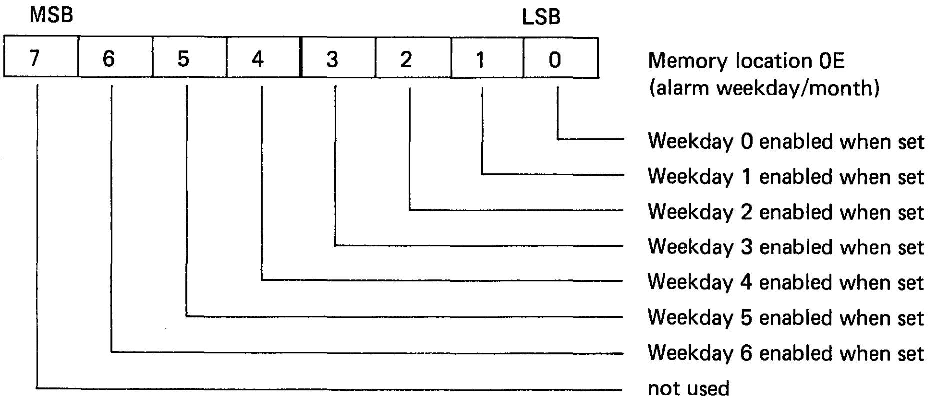


Fig.9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C-bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. 1 Hz is output at the interrupt (starts HIGH). This can be disabled by setting the alarm enable bit in the control/status register.

A second level-sensitive reset signal to the I^2C-bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERISTICS OF THE I^2C-BUS

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

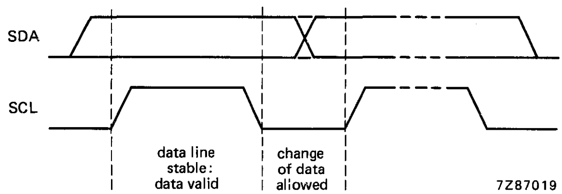


Fig.10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

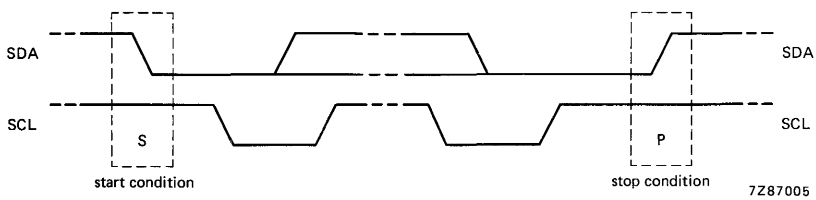


Fig.11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

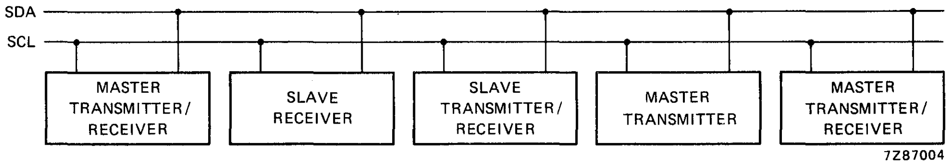


Fig.12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

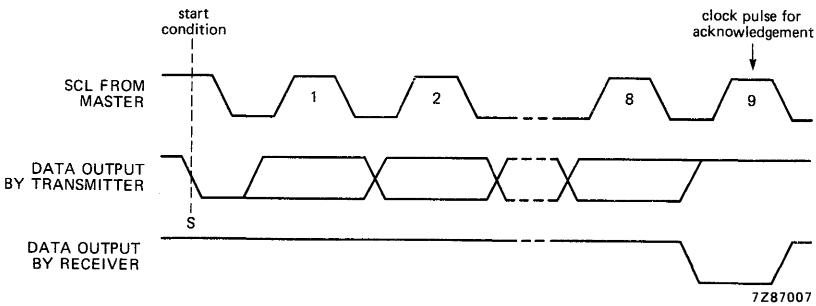


Fig.13 Acknowledgement on the I^2C-bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU; STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD; STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU; DAT}$	250	–	–	ns
Data hold time	$t_{HD; DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD; DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU; STO}$	4.0	–	–	μs

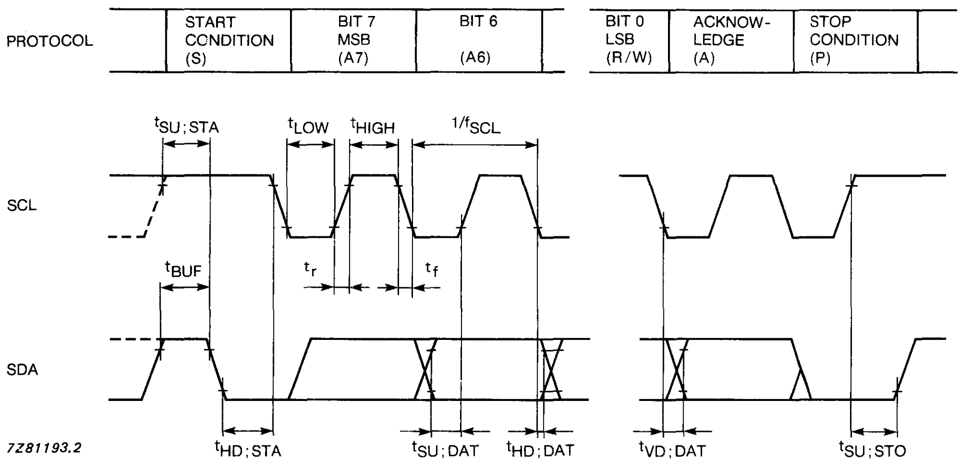


Fig. 14 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig.15.

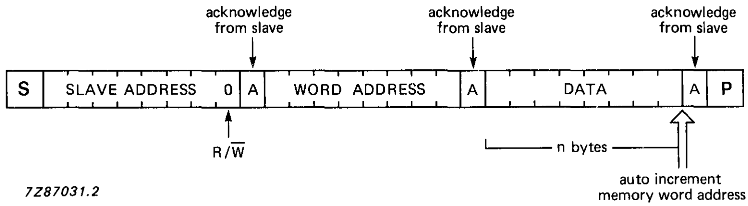


Fig.15a Master transmits to slave receiver (WRITE mode).

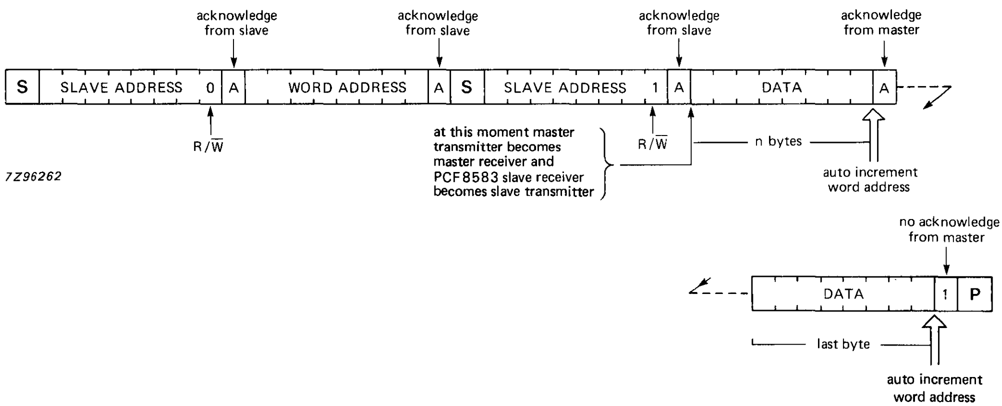


Fig.15b Master reads after setting word address (WRITE word address; READ data).

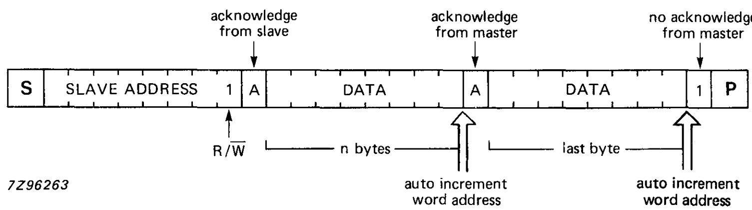


Fig.15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
operating		V_{DD}	2.5	–	6.0	V
clock	T_{amb} = 0 to + 70 °C	V_{DD}	1.0	–	6.0	V
Supply current						
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
clock	V_{DD} = 5 V	I_{DDO}	–	10	50	μA
clock	V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs; Input/output SDA						
Input voltage LOW	note 2	V_{IL}	–0.8	–	$0.3V_{DD}$	V
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
A0; OSCI						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	250	nA
SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
Output INT						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	note 3					
	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
	T_{amb} = –25 to + 70 °C; V_{DDR} = 1 V	I_{DDR}	–	–	2	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OSC}	–	40	–	pF
Oscillator stability for ΔV_{DD} = 100 mV	T_{amb} = 25 °C; V_{DD} = 1.5 V	f/fOSC	–	2 x 10^{-7}	–	
Input frequency	note 4	f_i	–	–	1	MHz
Quartz crystal parameters						
Frequency = 32.768 kHz						
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.
3. Event or 50 Hz mode only (no Quartz).
4. Event mode only.

APPLICATION INFORMATION

Quartz frequency adjustment

Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ± 5 x 10^{-6}). Average deviations of ± 5 minutes per year can be achieved.

Method 2: OSCI Trimmer

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

Power-on
Initialization (alarm function)

Routine:

Set clock to time T and set alarm to time T + dT.
At time T + dT (interrupt) repeat routine.

If time dT is approximately 10 ms a frequency of approximately 40 Hz is obtained.

APPLICATION INFORMATION (continued)

The PCF8583 slave address has a fixed combination 1010 as group 1.

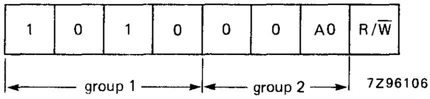
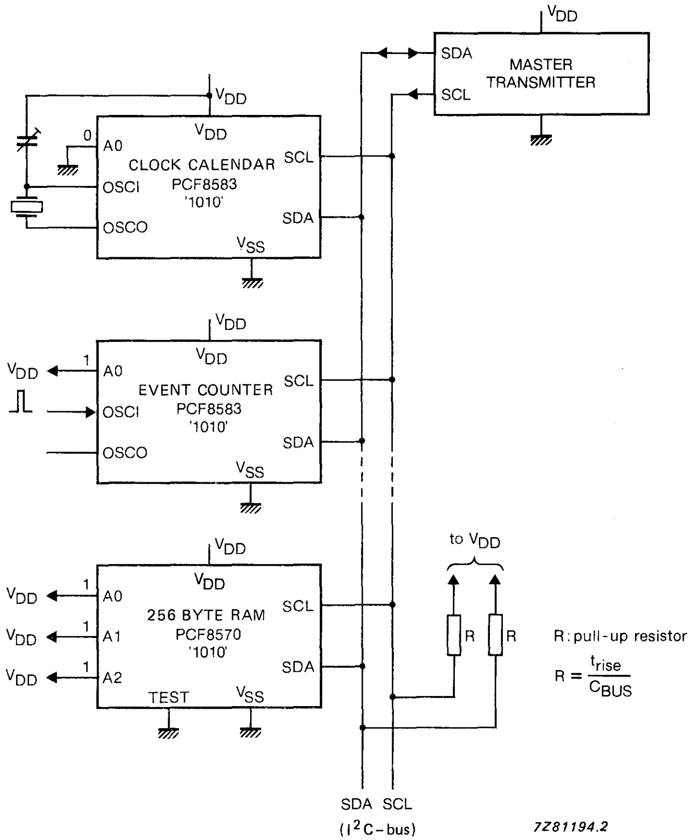


Fig.16 PCF8583 address.



Recommendation:
Connect a 4.7 μF 10 V solid aluminium (SAL) capacitor between V_{DD} and V_{SS}.

Fig.17 PCF8583 application diagram.

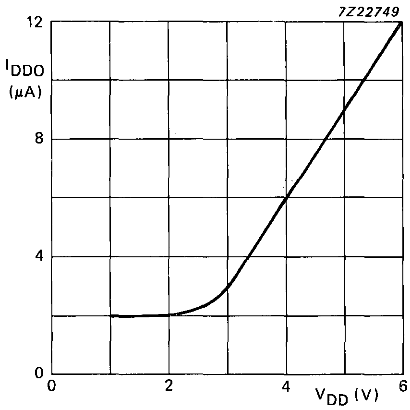


Fig.18 Typical supply current as a function of supply voltage (clock); T_{amb} = −40 to + 85 °C.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P: 16-lead DIL; plastic (SOT38).
PCF8591T: 16-lead mini-pack; plastic (SO16L; SOT162A).

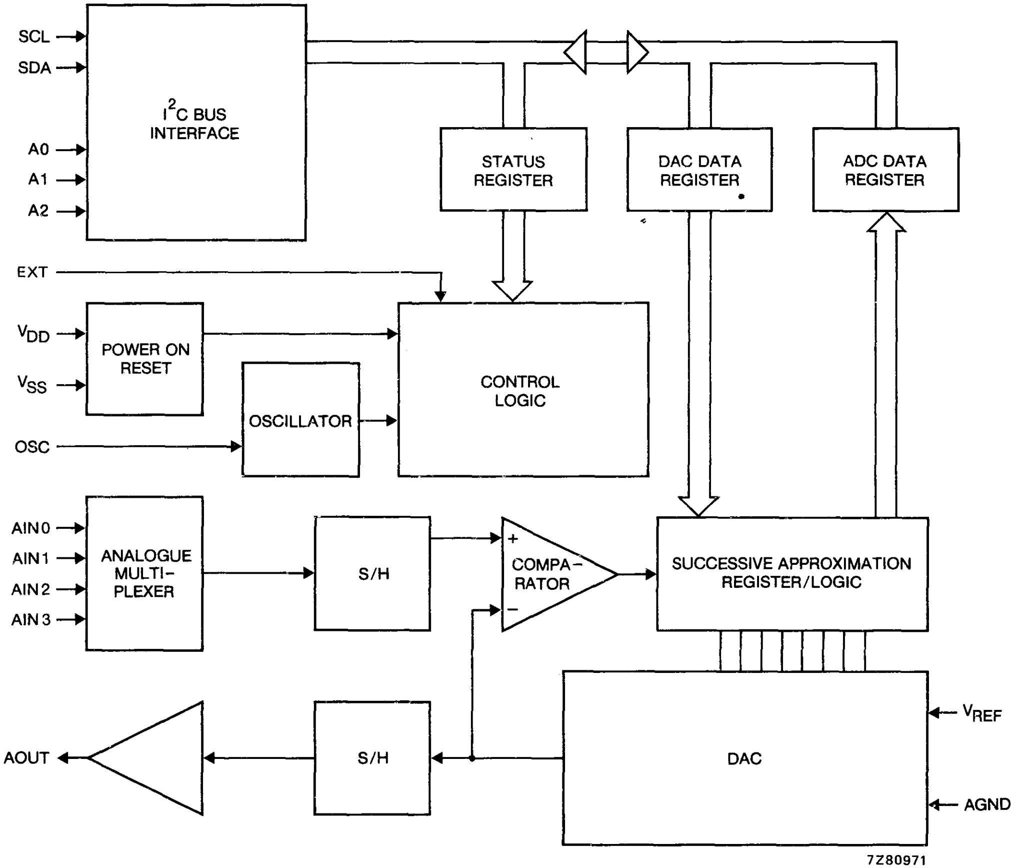


Fig. 1 Block diagram.

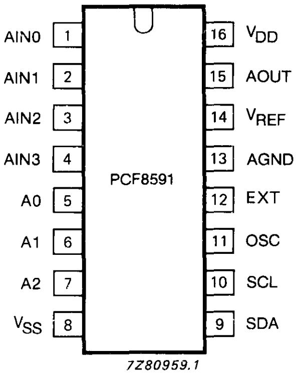


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

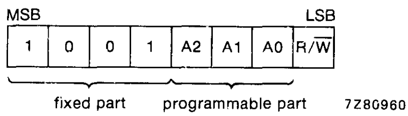


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

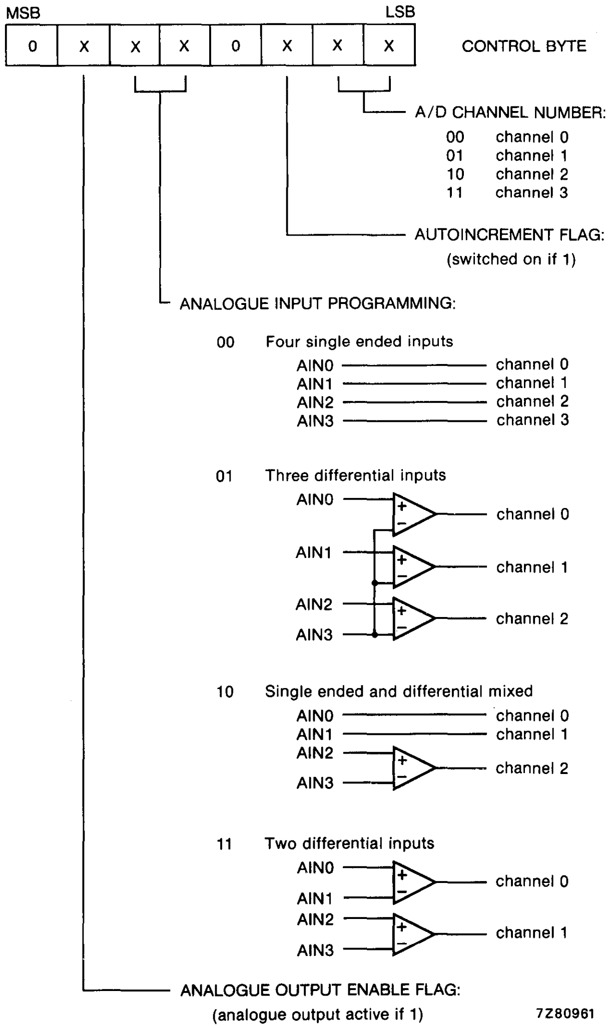


Fig. 4 Control byte.

...ent to a PCF8591 device is stored in the DAC data register and is converted to the ...ng analogue voltage using the on-chip D/A converter. This D/A converter consists of a ...divider chain connected to the external reference voltage with 256 taps and selection switches. ...cap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6.

The waveforms of a D/A conversion sequence are shown in Fig. 7.

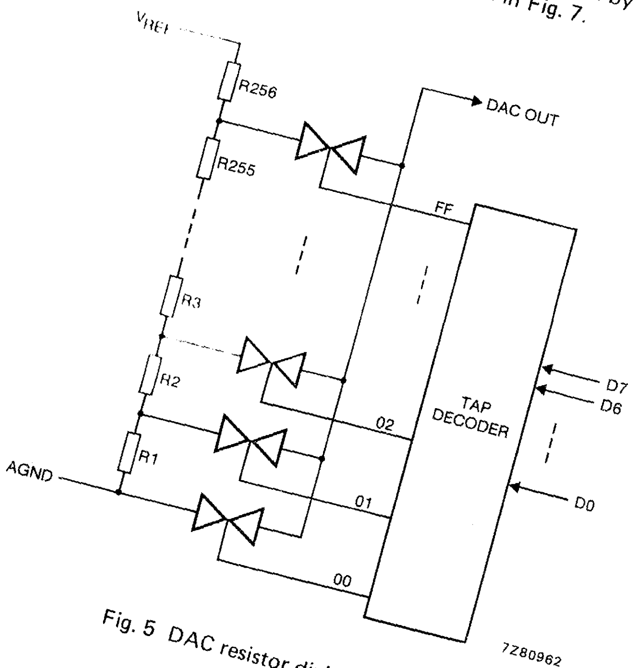


Fig. 5 DAC resistor divider chain.

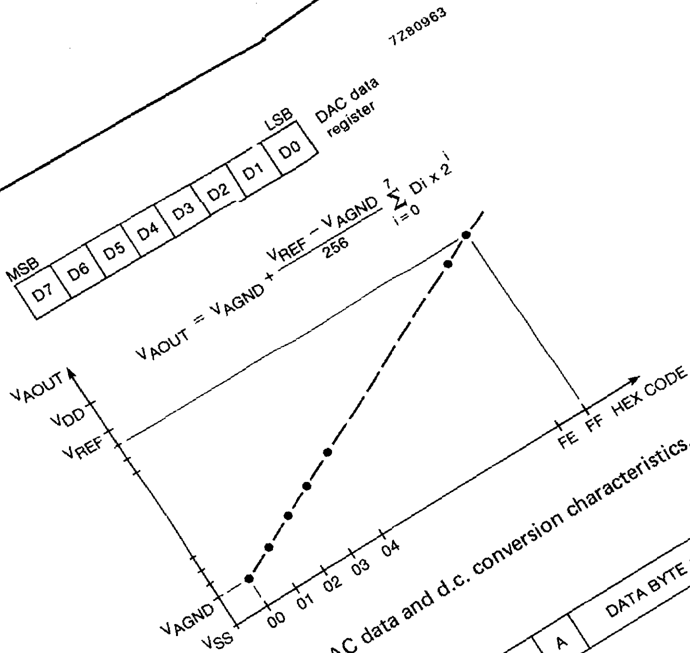


Fig. 6 DAC data and d.c. conversion characteristics.

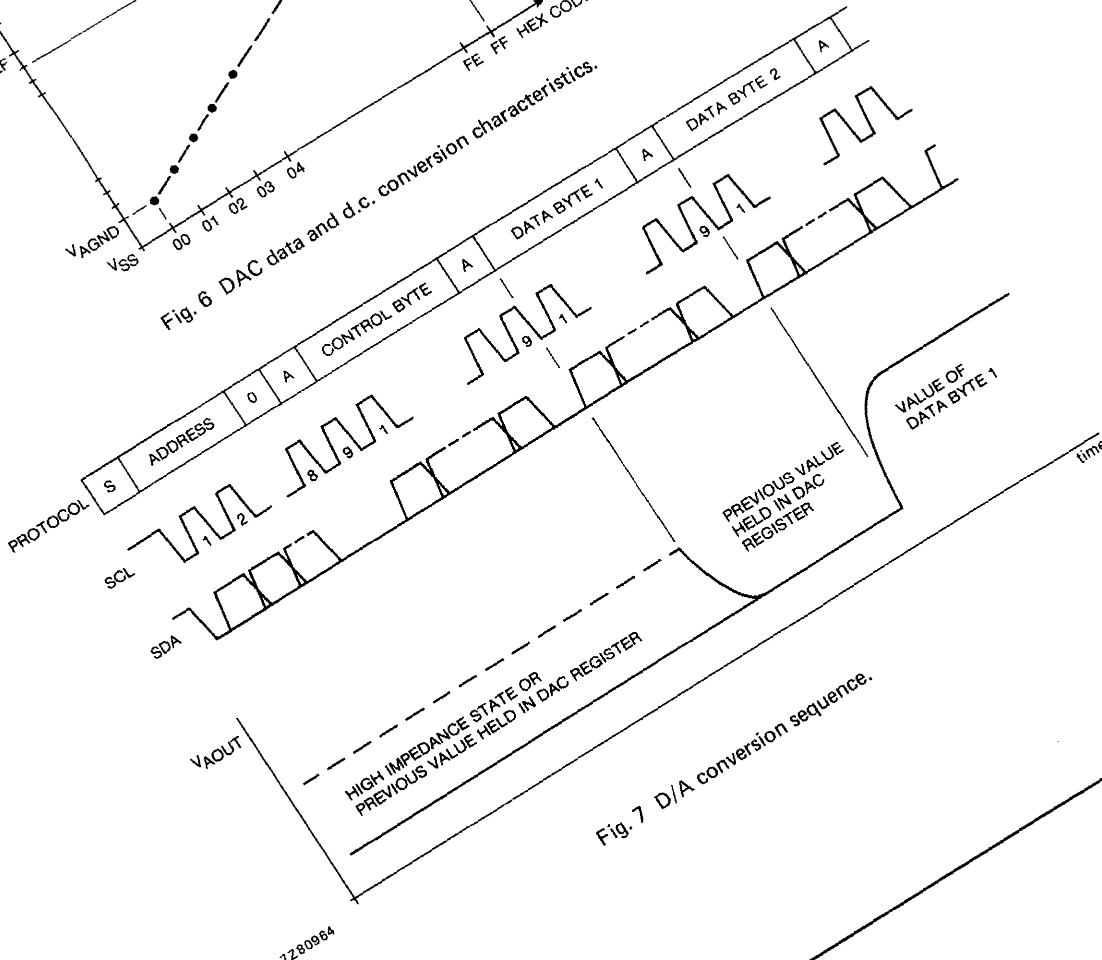


Fig. 7 D/A conversion sequence.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

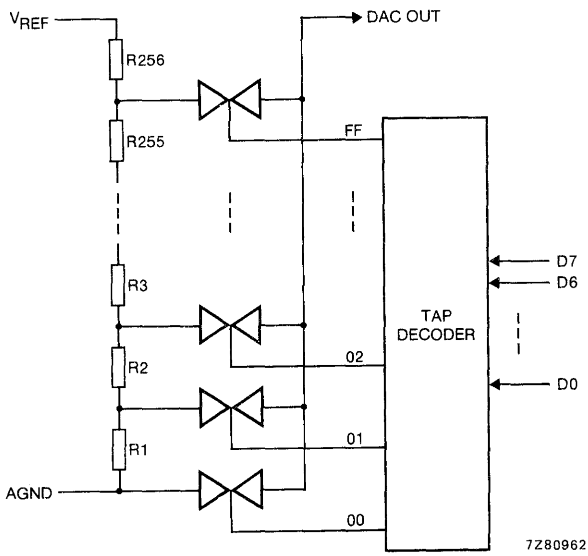


Fig. 5 DAC resistor divider chain.

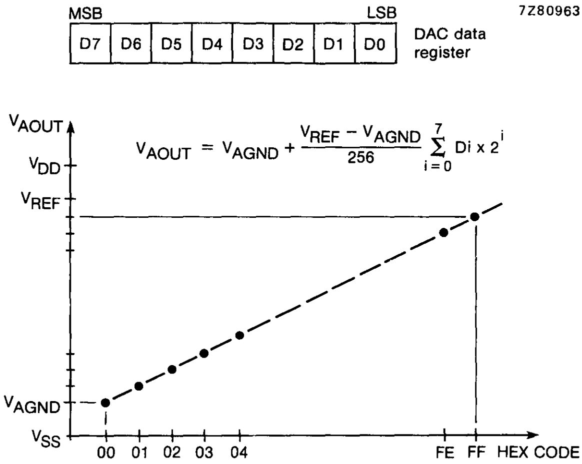


Fig. 6 DAC data and d.c. conversion characteristics.

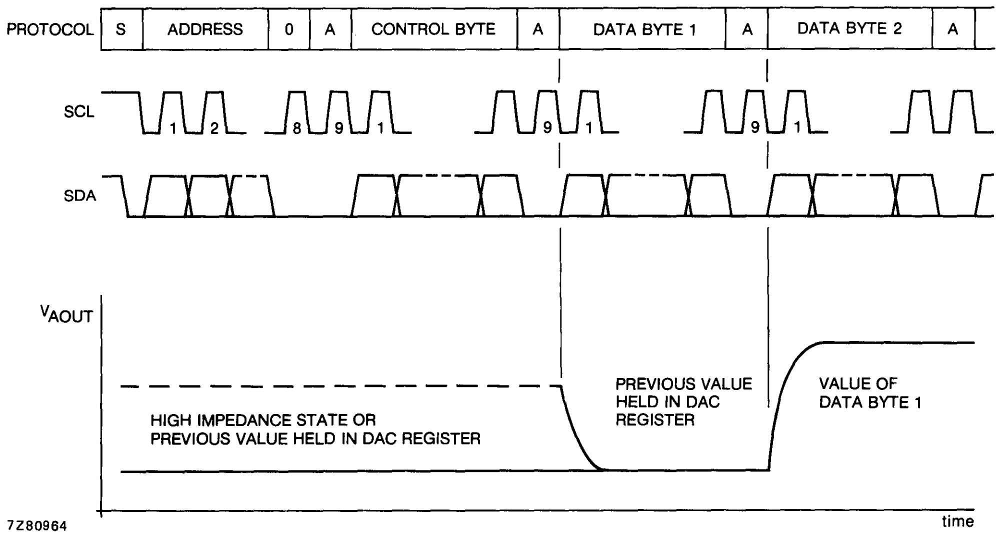


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

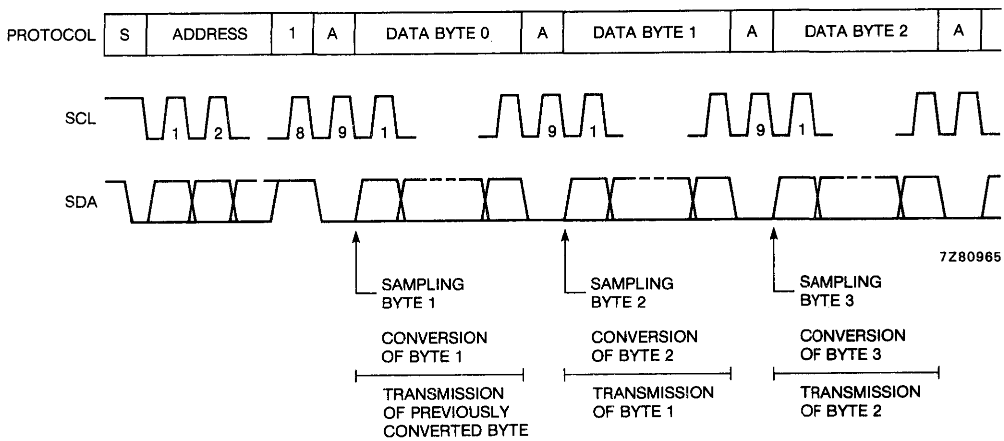


Fig. 8 A/D conversion sequence.

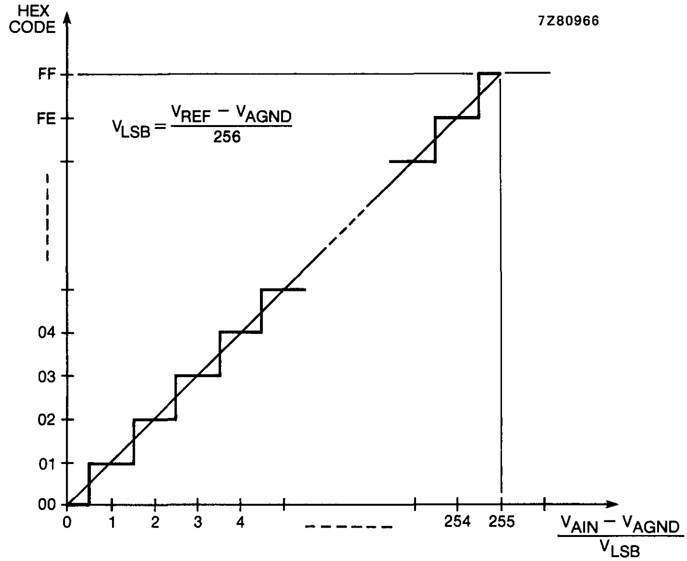


Fig. 9a A/D conversion characteristics of single-ended inputs.

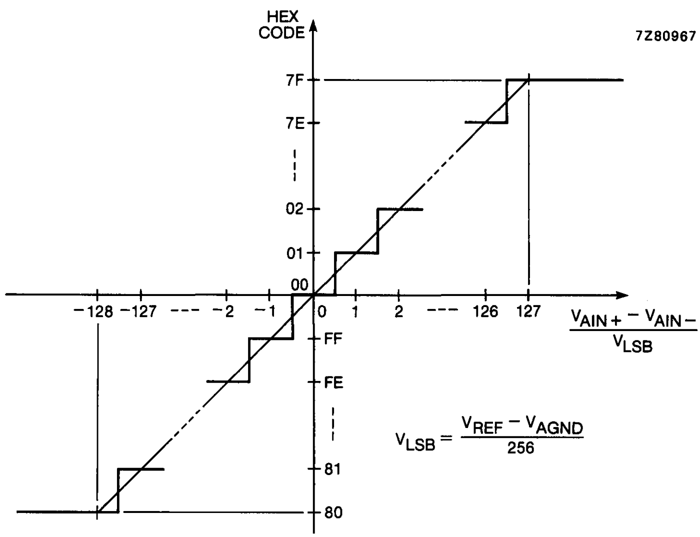


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

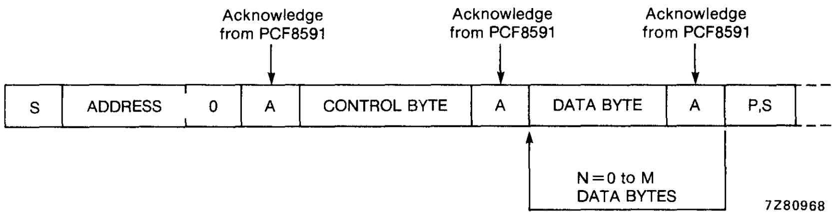


Fig. 10a Bus protocol for write mode, D/A conversion.

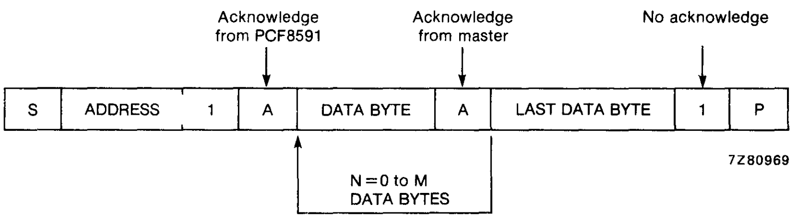


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I^{2}C BUS

The I^{2}C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

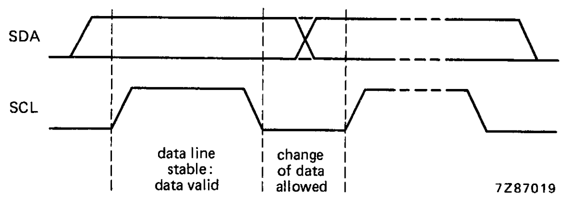


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

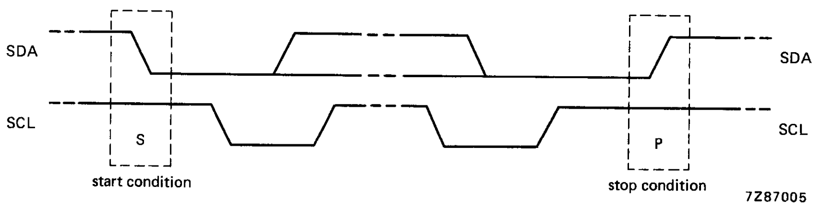


Fig. 12 Definition of start and stop condition.

DEVELOPMENT DATA

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

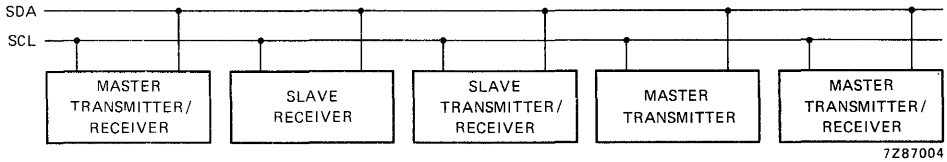


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

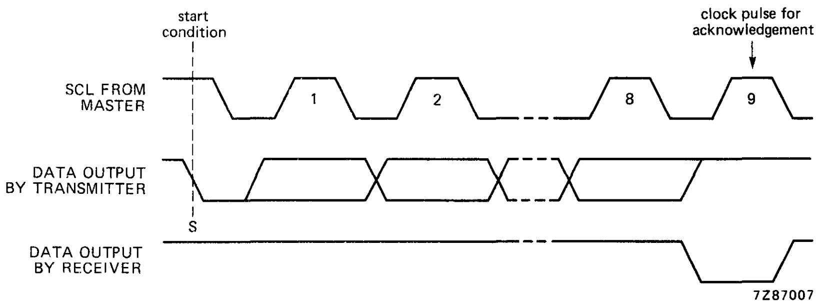


Fig. 14 Acknowledgement on the I^2C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

DEVELOPMENT DATA

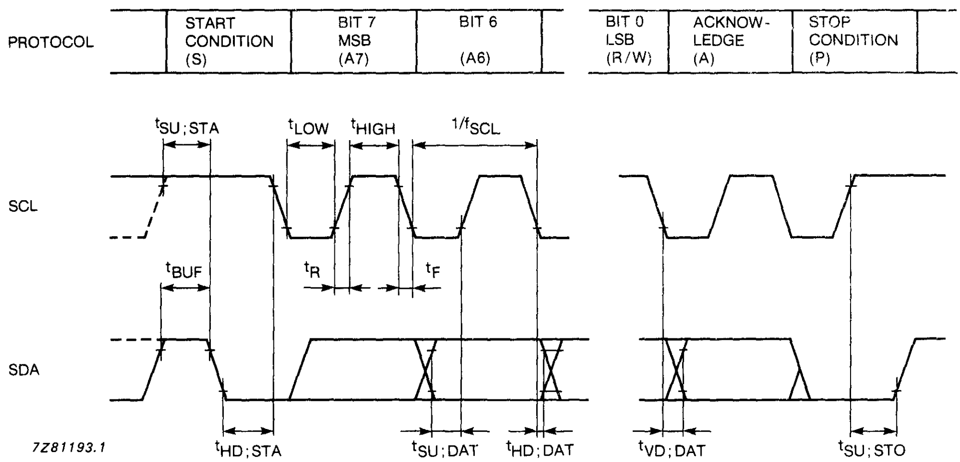


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = –40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0{,}9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

A/D CHARACTERISTICS

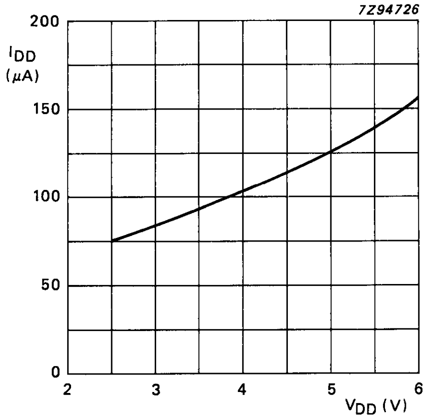
V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

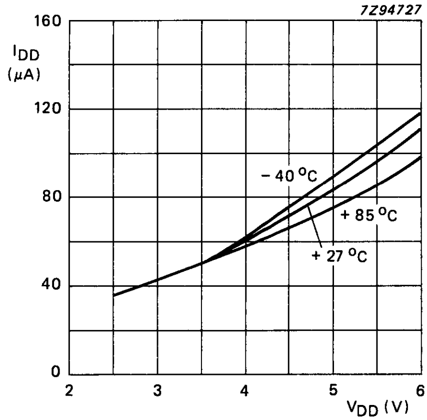
Note

1. The power on reset circuit resets the I²C bus logic when V_{DD} is less than V_{POR}.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

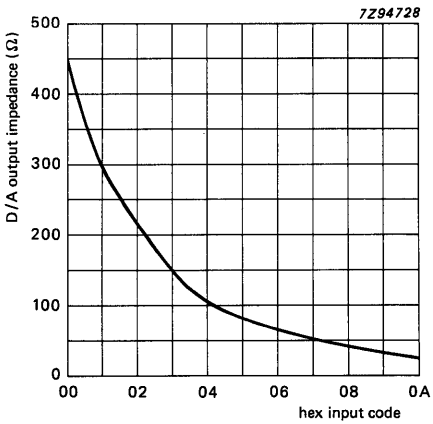


(a) internal oscillator; T_{amb} = + 27 ^{o}C.

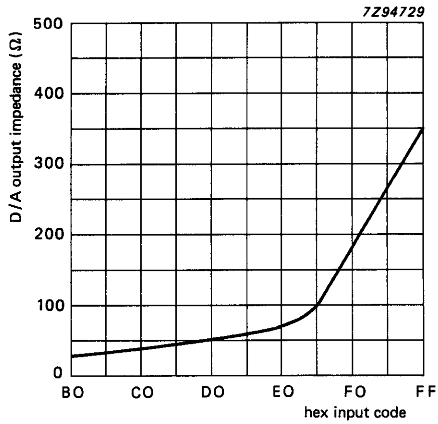


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 ^{o}C.



(b) output impedance near positive power rail; T_{amb} = + 27 ^{o}C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10 μF) are recommended for power supply and reference voltage inputs.

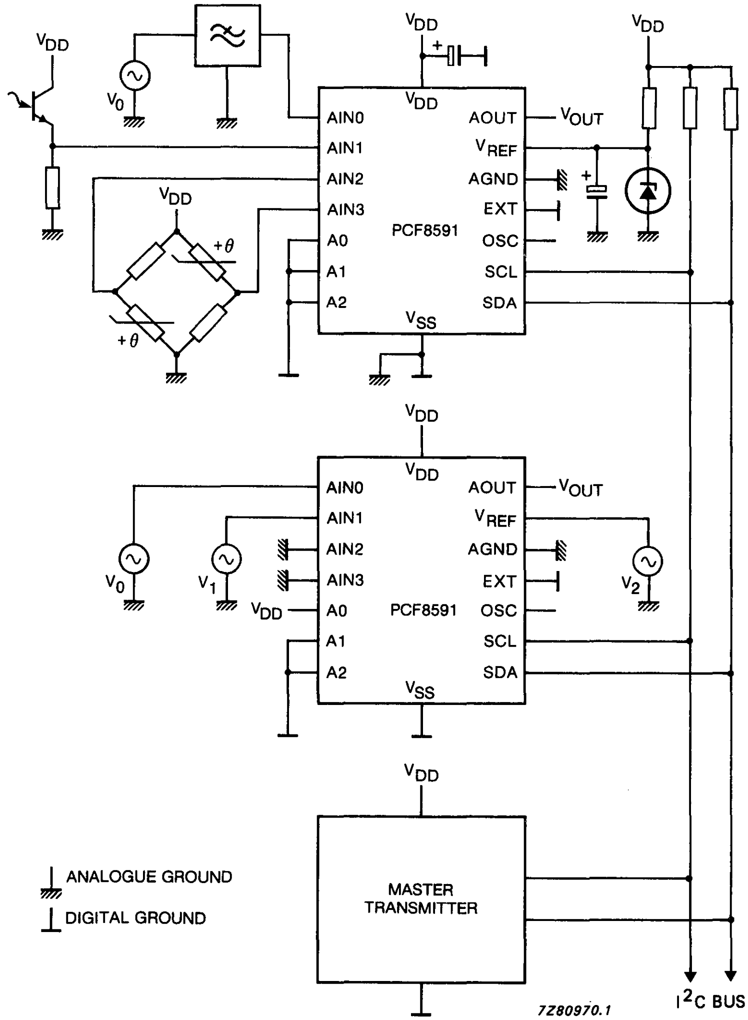


Fig. 18 Application diagram.

7-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC 7)

GENERAL DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

QUICK REFERENCE DATA

Measured over full voltage and temperature range unless otherwise specified

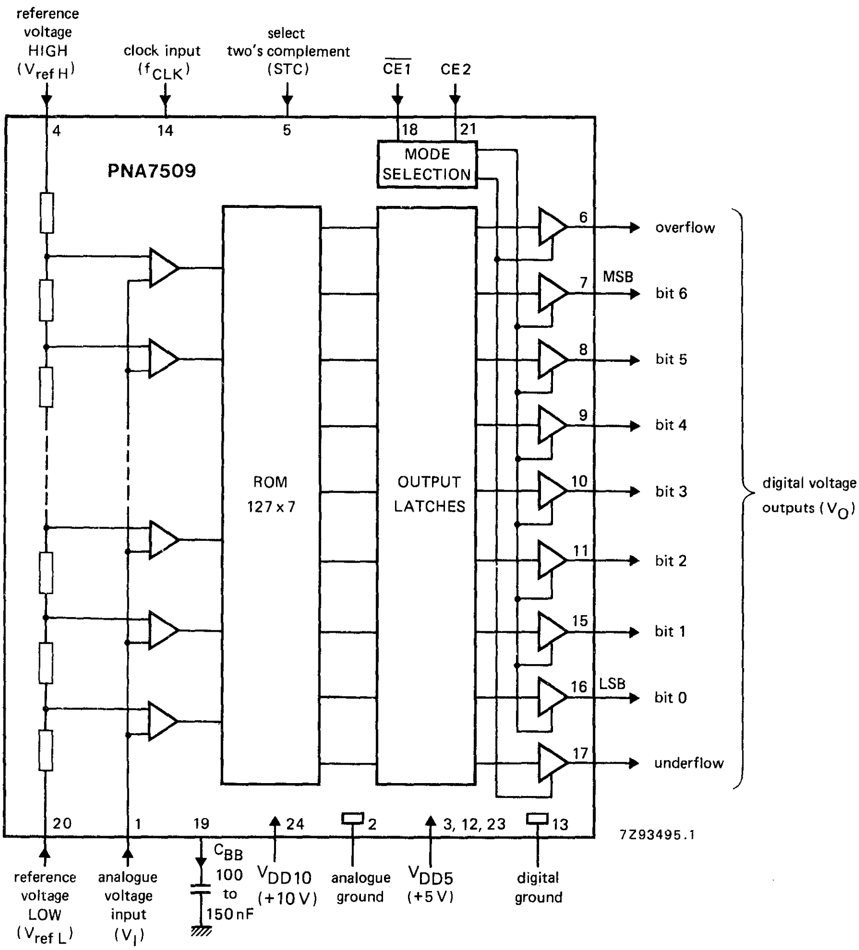
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pins 3, 12, 23)		V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)		V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	note 1	I_{DD5}	–	–	65	mA
Supply current (pin 24)	note 1	I_{DD10}	–	–	13	mA
Reference current (pins 4, 20)		I_{ref}	150	–	450	μA
Reference voltage LOW (pin 20)		V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)		V_{refH}	5,0	5,1	5,2	V
Non-linearity	f_i = 1,1 kHz					
integral		INL	–	–	± ½	LSB
differential		DNL	–	–	± ½	LSB
−3 dB Bandwidth		B	11	–	–	MHz
Clock frequency (pin 14)		f_{CLK}	1	–	22	MHz
Total power dissipation	note 1	P_{tot}	–	–	500	mW

Note to quick reference data

1. Measured under nominal conditions: V_{DD5} = 5 V; V_{DD10} = 10 V; T_{amb} = 22 °C.

PACKAGE OUTLINES

24-lead DIL; plastic (SOT101A).



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

DEVELOPMENT DATA

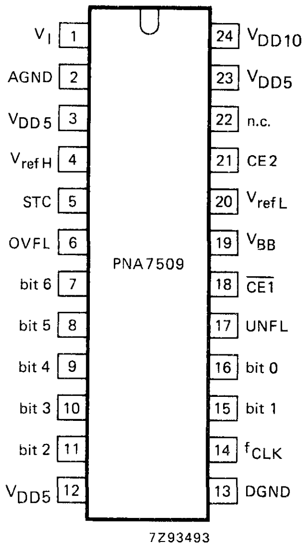


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD5}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD5}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	$\overline{CE\ 1}$	chip enable input 1
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	CE 2	chip enable input 2
22	n.c.	not connected
23	V_{DD5}	positive supply voltage (+ 5 V)
24	V_{DD10}	positive supply voltage (+ 10 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0,5 to + 7	V
Supply voltage range (pin 24)	V_{DD10}	−0,5 to + 12	V
Input voltage range	V_I	−0,5 to + 7	V
Output current	I_O	5	mA
Total power dissipation	P_{tot}	1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3,\ 12,\ 23\text{-}13} = 4{,}5$ to $5{,}5$ V; $V_{DD10} = V_{24\text{-}2} = 9{,}5$ to $10{,}5$ V; $C_{BB} = 100$ nF;
$T_{amb} = 0$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD5}	4,5	–	5,5	V
Supply voltage (pin 24)	V_{DD10}	9,5	–	10,5	V
Supply current (pins 3, 12, 23)	I_{DD5}	–	–	85	mA
Supply current (pin 24)	I_{DD10}	–	–	18	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	150	–	450	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input voltage HIGH (note 1)	V_{IH}	3,0	–	V_{DD5}	V
Digital input levels (pins 5,18,21; note 2)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15	–	70	μA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15	–	70	μA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	15	–	120	μA
Input leakage current (except pins 5, 18 and 21)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p\text{-}p)}$	–	2,6	–	V
Input capacitance (note 3)	$C_{1\text{-}2}$	–	–	30	pF

Notes to characteristics

1. Maximum input voltage must not exceed 5,0 V.
2. If pin 5 is LOW binary coding is selected.
   If pin 5 is HIGH two's complement is selected.
   If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
   For output coding see Table 1 and mode selection see Table 2.
3. Tested on sample base.

parameter	symbol	min.	max.	unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
Output voltage LOW at I_O = 2 mA	V_{OL}	0	+0,4	V
Output voltage HIGH at $-I_O$ = 0,5 mA	V_{OL}	2,4	V_{DD5}	V

Table 1 Output coding (V_{refL} = 2,50 V; V_{refH} = 5,08 V)

step	$V_{1\text{-}2}$ (1)	UNFL	OVFL	binary bit 6 — bit 0							two's complement bit 6 — bit 0							
underflow	< 2,51	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
0	2,51	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
1	2,53	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	steps
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2-125
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	
126	5,03	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	0	
127	5,05	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	
overflow	≥ 5,07	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	

Note to Table 1

1. Approximate values.

Table 2 Mode selection

$\overline{CE\ 1}$	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

DEVELOPMENT DATA

CHARACTERISTICS (continued)

$V_{DD5} = V_{3,\ 12,\ 23\text{-}13}$ = 4,5 V to 5,5 V; $V_{DD10} = V_{24\text{-}2}$ = 9,5 V to 10,5 V; V_{refL} = 2,5 V; V_{refH} = 5,1 V; f_{CLK} = 22 MHz; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C

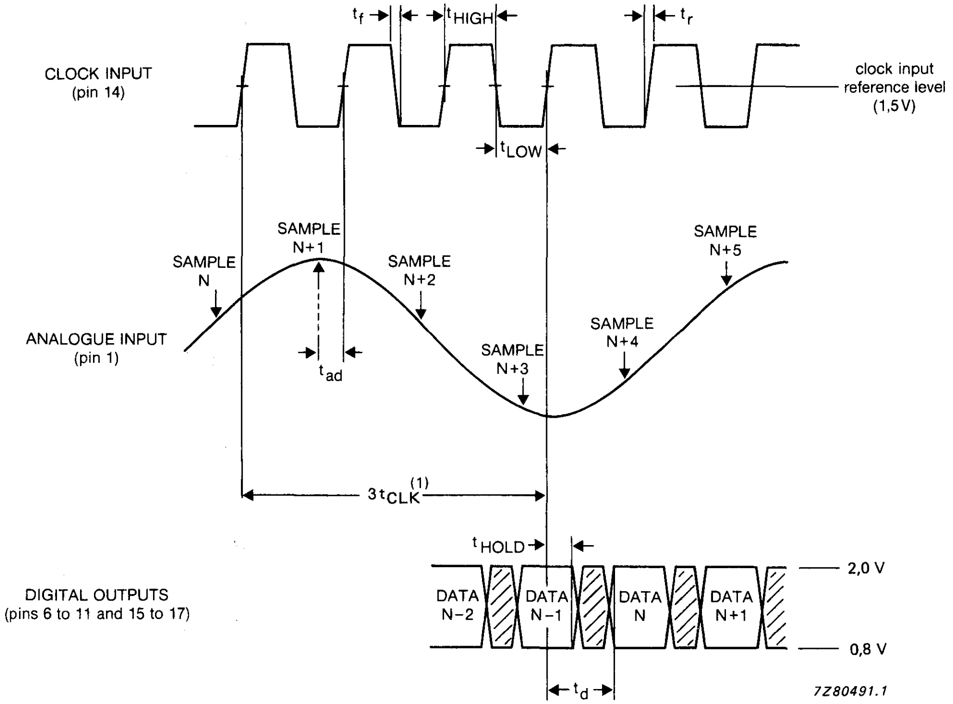
parameter	symbol	min.	max.	unit
Switching characteristics (see also Fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
Clock cycle time LOW	t_{LOW}	20	–	ns
Clock cycle time HIGH	t_{HIGH}	20	–	ns
Input rise and fall times (pin 1)				
rise time	t_r	–	3	ns
fall time	t_f	–	3	ns
Analogue input (note 1)				
Bandwidth (–3 dB)	B	11	–	MHz
Differential gain (note 2)	dG	–	± 5	%
Differential phase (note 2)	d_p	–	± 2,5	deg
Non-harmonic noise		–	–36	dB
Peak error (non-harmonic noise)(note 3)		–	3	LSB
Harmonics (full scale)				
fundamental (note 3)	f_0	–	0	dB
r.m.s. (2nd + 3rd harmonic)	$f_{2,3}$	–	–28	dB
r.m.s. (4th + 5th + 6th + 7th harmonic)	$f_{4\text{-}7}$	–	–35	dB

parameter	symbol	min.	max.	unit
Digital outputs (notes 1 and 4)				
Output hold time	t_{HOLD}	6	–	ns
Output delay time at C_L = 15 pF	t_d	–	38	ns
Output delay time at C_L = 50 pF	t_d	–	48	ns
3-state delay time	t_{dt}	–	25	ns
Capacitive output load	C_{OL}	0	15	pF
Transfer function				
Non-linearity at f_i = 1,1 kHz				
integral	INL	–	± ½	LSB
differential	DNL	–	± ½	LSB

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sinewave (peak-to-peak value of the analogue input voltage at $V_{I(p-p)}$ = 1,8 V) combined with a sinewave voltage ($V_{I(p-p)}$ = 0,7 V) at f_i = 5 MHz.
3. Analogue frequency $f_{i(A)}$ = 5 MHz
   Amplitude $V_{i(A)}$ = 2.42 V (peak-to-peak value).
4. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

DEVELOPMENT DATA



(1) There is a delay of 3 clock cycles between sampling of an analogue input signal and the corresponding digital output.

Fig. 3 Timing diagram.

APPLICATION NOTE

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V, T_{amb} = 22 °C.

parameter	symbol	typ.	unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	51	mA
Supply current (pin 24)	I_{DD10}	11	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (−3 dB)	B	20	MHz
Total power dissipation	P_{tot}	365	mW
Peak error (non-harmonic noise)		1,5	LSB
Suppression of harmonics sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± 1/4	LSB
differential	DNL	± 1/3	LSB
Differential gain	dG	± 3	%
Differential phase	dP	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB

Typical values are measured on sample base.

Application recommendation

Spikes at the 10 V supply input must be avoided (e. g. overshoots during switching). Even a spike duration of less than 1 μs can destroy the device.

APPLICATION NOTE (continued)

Test philosophy

Fig. 4 is a block diagram showing analogue-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test).
The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.
Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.
The successive processing completes the specific measurement (Fig. 5, 6, 7 and 8).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.
After low-pass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.
To calculate differential non-linearity a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation (Fig. 7).

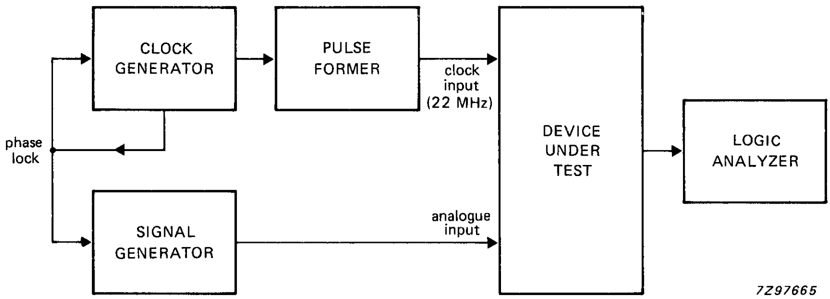
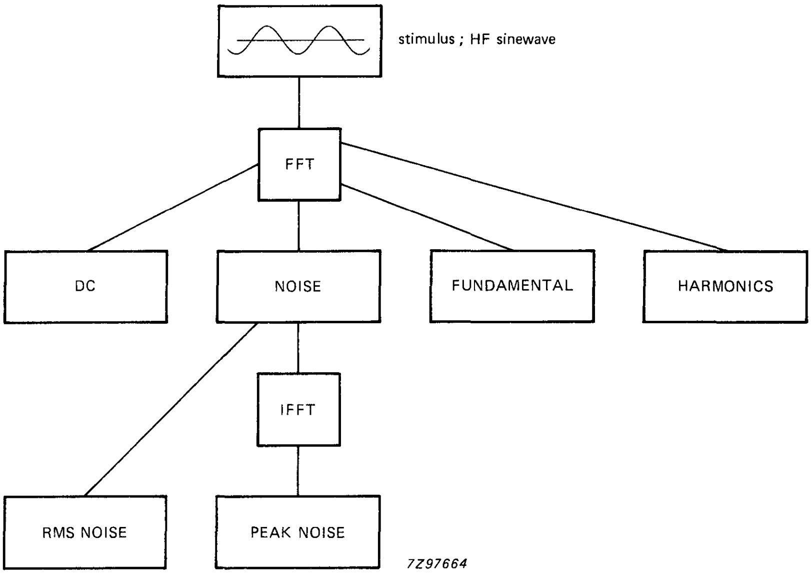


Fig. 4 Analogue-to-digital converter testing with locked signal source.



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Fig. 5 Sinewave test; non-harmonic noise and peak error.

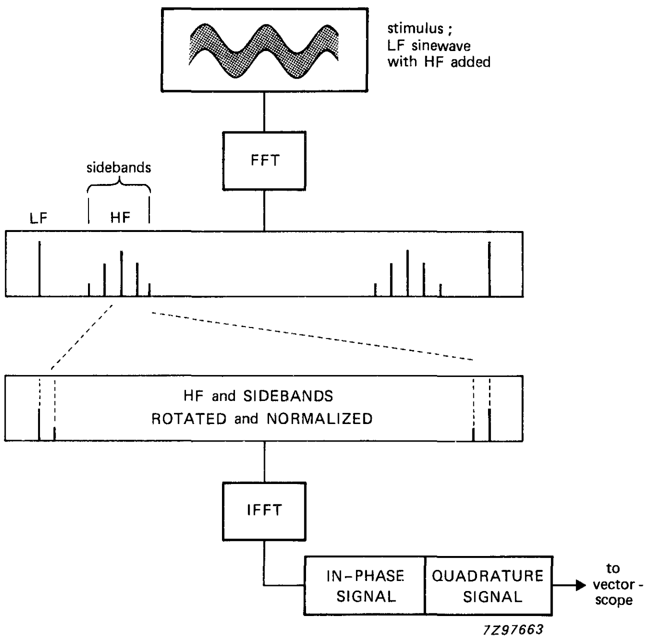
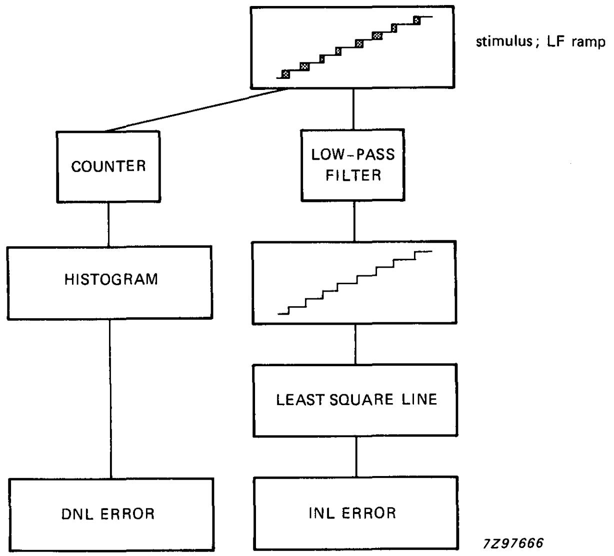


Fig. 6 Differential gain and phase.

DEVELOPMENT DATA

APPLICATION NOTE (continued)



Where: INL = Integral Non-Linearity.
DNL = Differential Non-Linearity.

Fig. 7 Low frequency ramp test; linearity.

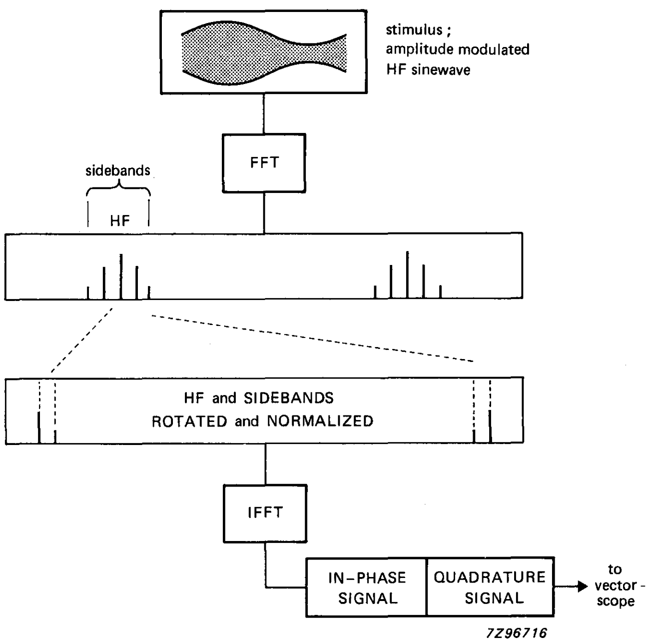


Fig. 8 Large signal phase error.

8-BIT MULTIPLYING DAC

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain. The multiplying capability is obtained by using the independent reference voltages.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the 75 Ω output impedance. Two's complement is selected when STC (pin 11) is HIGH or is not connected. STC inverts the most significant bit (MSB).

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB
- Multiplying capability
- 12 MHz bandwidth
- 8-bit resolution

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Reference voltage LOW		V_{refL}	0	–	2,0	V
Reference voltage HIGH		V_{refH}	0	–	2,0	V
Static non-linearity	note 1		–	–	± 0,5	LSB
Bandwidth at –3 dB	note 2	B	12	–	–	MHz
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Total power consumption		P	–	–	470	mW

For explanation of notes see "Notes to the characteristics".

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38D)

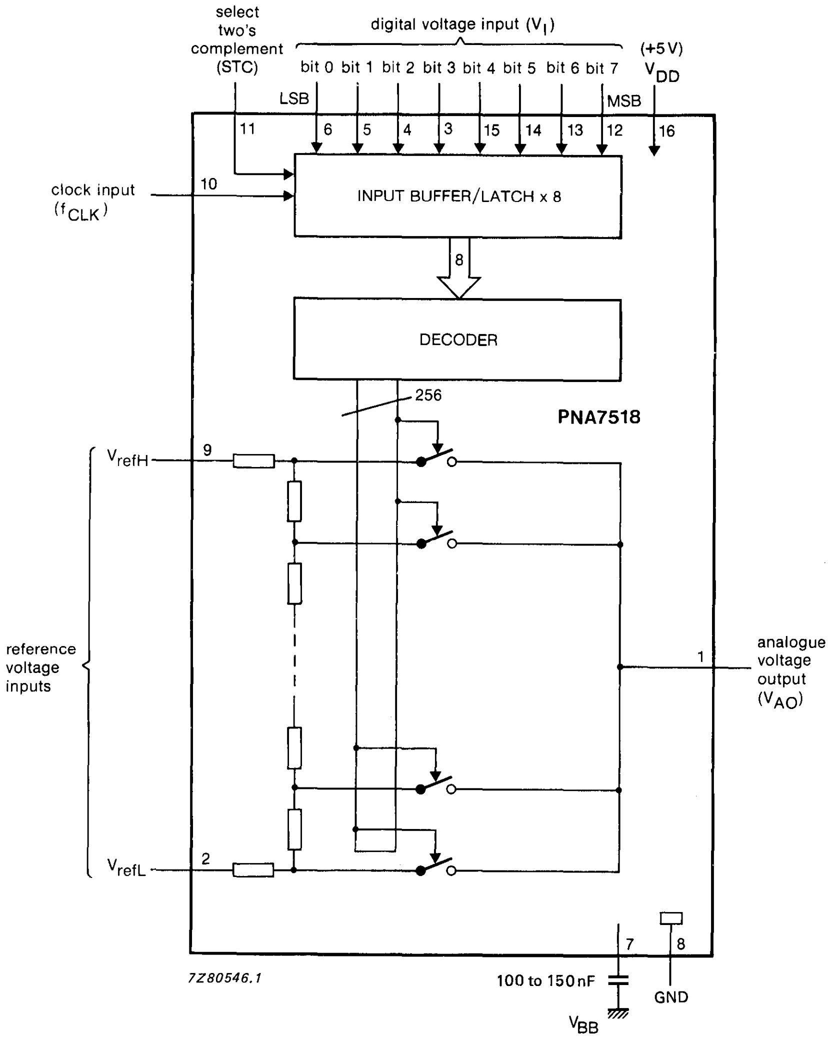


Fig. 1 Block diagram.

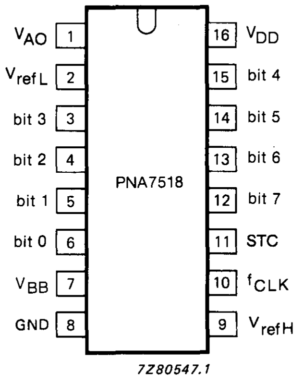


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	GND	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	–0,5	7,0	V
Input voltage B0 to B7 and STC	V_I	–0,5	7,0	V
Output voltage	V_{AO}	–0,5	7,0	V
Total power dissipation	P_{tot}	–	800	mW
Storage temperature range	T_{stg}	–65	+ 150	°C
Operating ambient temperature range	T_{amb}	0	+ 70	°C
Temperature range with back bias	T_{BB}	–10	+ 80	°C
Clock frequency	f_{CLK}	10	–	kHz

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	–	5,5	V
Supply current		I_{DD}	–	–	80	mA
Inputs B0 to B7, CLK, and STC						
Input voltage LOW		V_{IL}	0	–	0,8	V
Input voltage HIGH		V_{IH}	2	–	V_{DD}	V
Input leakage current (except STC)		I_{LI}	–	–	10	μA
STC input current		I_I	–	–	100	μA
Reference voltages						
Reference voltage LOW		V_{refL}	0	–	2	V
Reference voltage HIGH		V_{refH}	0	–	2	V
Reference ladder between V_{refL} and V_{refH}		R_{ref}	150	–	300	Ω
Linearity						
Static non-linearity	note 1		–	–	± 0,5	LSB
Clock input						
Clock frequency	T_{amb} = 25 °C; V_{DD} = 5 V	f_{CLK}	10	–	30	MHz
Bandwidth						
Bandwidth at –3 dB	note 2	B	12	–	–	MHz

Notes to the characteristics

1. Measured at R_{AO} = 200 kΩ; V_{refL} = 0 V; V_{refH} = 2 V and f_{CLK} = 28 MHz.
2. Measured at V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2 V; f_{CLK} = 30 MHz; duty cycle = 0,5; rise and fall time = 3 ns and a 6 pF load at the analogue output. The analogue output signal is scanned by an external sample and hold circuit.

APPLICATION INFORMATION

This section provides additional information to the characteristics. The values are measured on a sampling basis.

Table 1 Application characteristics

parameter	symbol	typ.	unit
Supply current	I_{DD}	50	mA
Power consumption	P	270	mW
Minimum clock frequency	f_{CLK}	10	kHz
Maximum clock frequency	f_{CLK}	45	MHz
Static non-linearity		± 0,25	LSB
Reference ladder	R_{ref}	210	Ω
Bandwidth	B	15	MHz
Set-up time	t_{SU}	3	ns
Input hold time	t_{HD}	4	ns
Propagation delay	t_{PD}	$1 \times t_{CLK} + 30$	ns

Where:

V_{DD} = 5 V; T_{amb} = 25 °C; V_{refL} = 0 V; V_{refH} = 2,0 V.

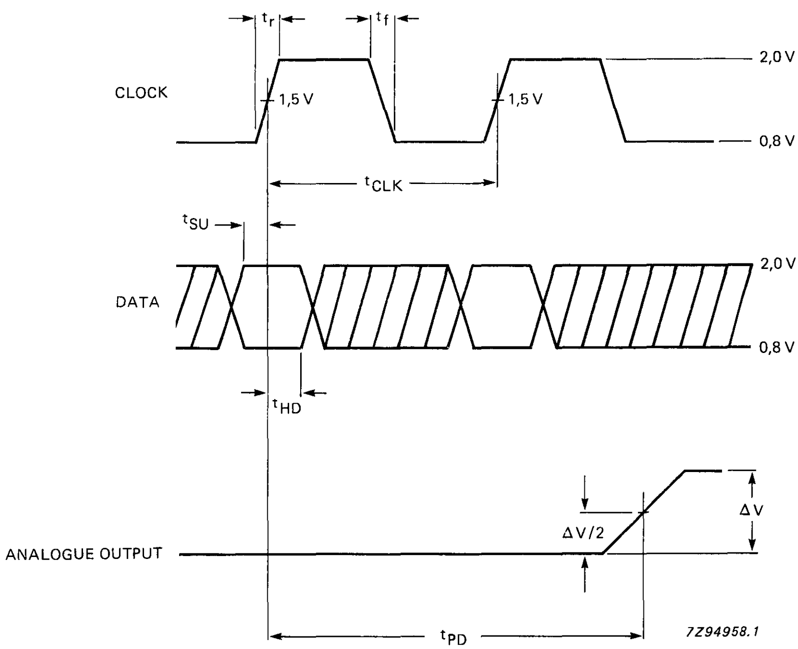


Fig. 3 Switching characteristics.

DEVELOPMENT DATA

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}		3,6 to 12	V
	V_{CC2}		3,6 to 12	V
	V_{CC3}		V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ.	18	mA
	I_{CC3}	typ.	0,8	mA
Input frequency ranges				
at pin FAM	f_{FAM}		512 kHz to 32	MHz
at pin FFM	f_{FFM}		70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	>	4	MHz
Operating ambient temperature range	T_{amb}		−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102H).

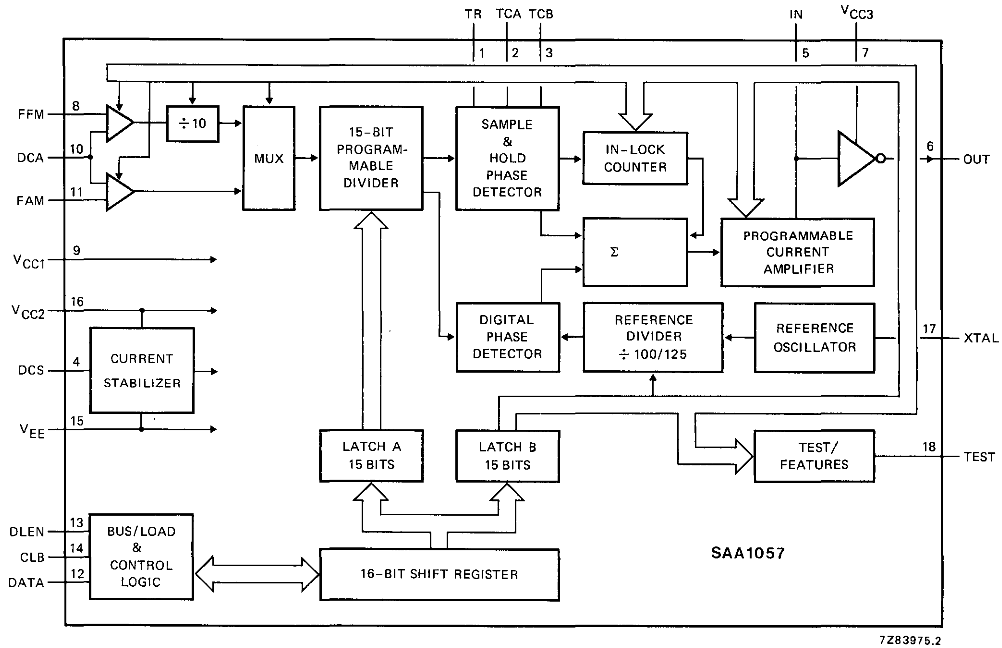


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM	FM/AM selection; '1' = FM, '0' = AM
REFH	reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)
CP3, CP2, CP1, CP0	control bits for the programmable current amplifier (see section Characteristics)
SB2	enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically
SLA	load mode of latch A; '1' = synchronous, '0' = asynchronous
PDM1, PDM0	phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM	bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on
T3	test bit; must be programmed always '0'
T2	test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin
T1	test bit; must be programmed always '0'
T0	test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

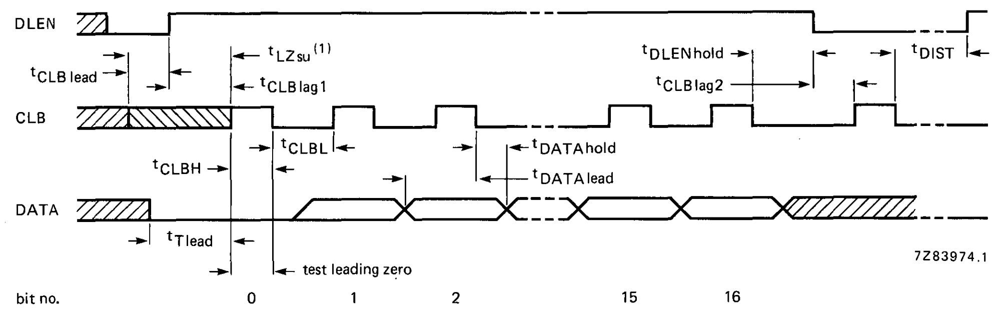


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^{2}C bus is used for other devices on the same data and clock lines.

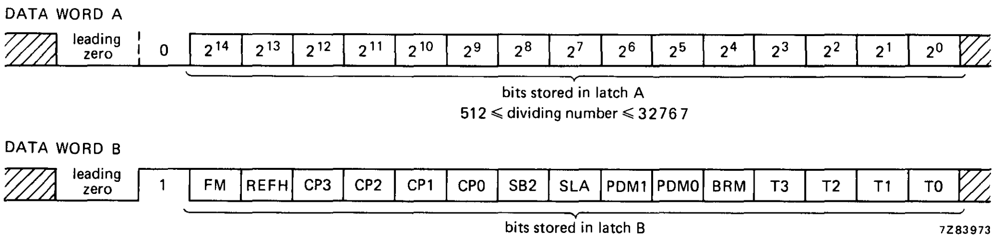


Fig. 3 Bit organization of data words A and B.

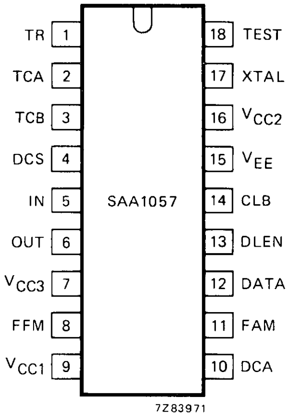


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	$I_{OUT} = 0$
Operating ambient temperature	T_{amb}	–25	–	+ 80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	–30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	$V_{IL} = 0,8$ V
Input current HIGH	I_{IH}	–	–	10	μA	$V_{IH} = 2,4$ V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	μs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	μs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	μs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	μs	
CLB pulse width LOW	t_{CLBL}	5	–	–	μs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	μs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	μs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	μs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	μs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	μs	next transmission after word 'B' to other device or
Busy time asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	$V_{CC2}-0,7$	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	μs	REFH = '1'
	t_{dis}	–	–	6,25	μs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT} = 1$ mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	$I_{OUT} = 1$ mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	$I_{OUT} = 0,1$ mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	$V_{OUT} = ½ V_{CC3}$
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at $f_{ripple} = 100$ Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

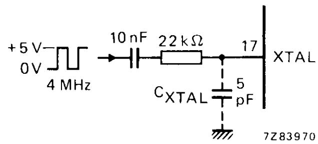


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

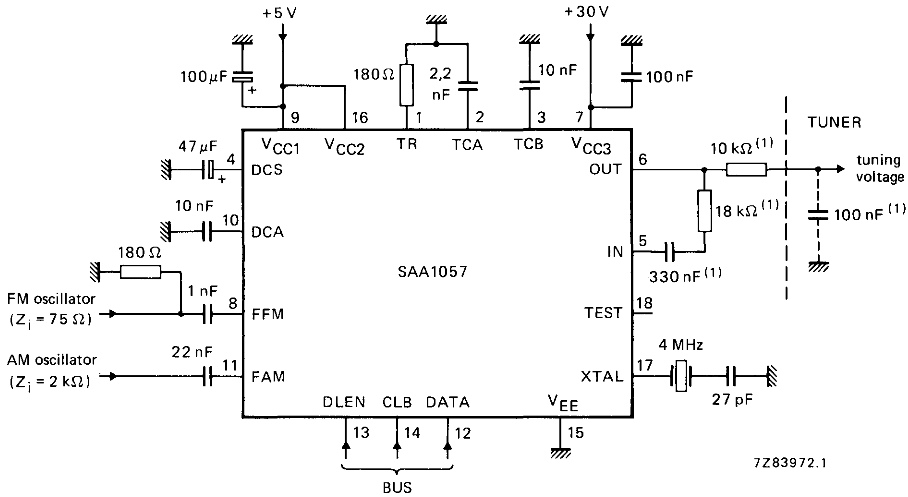
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

4-DIGIT LED-DRIVER WITH I^2C BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I^2L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I^2C bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	4,5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}	–	9,5	–	mA
Total power dissipation 24-lead DIL (SOT-101B)		P_{tot}	–	–	1000	mW
Operating ambient temperature range		T_{amb}	–20	–	+ 70	^oC

PACKAGE OUTLINE

SAA1064P: 24-lead DIL; plastic (with internal heat spreader) (SOT101B).

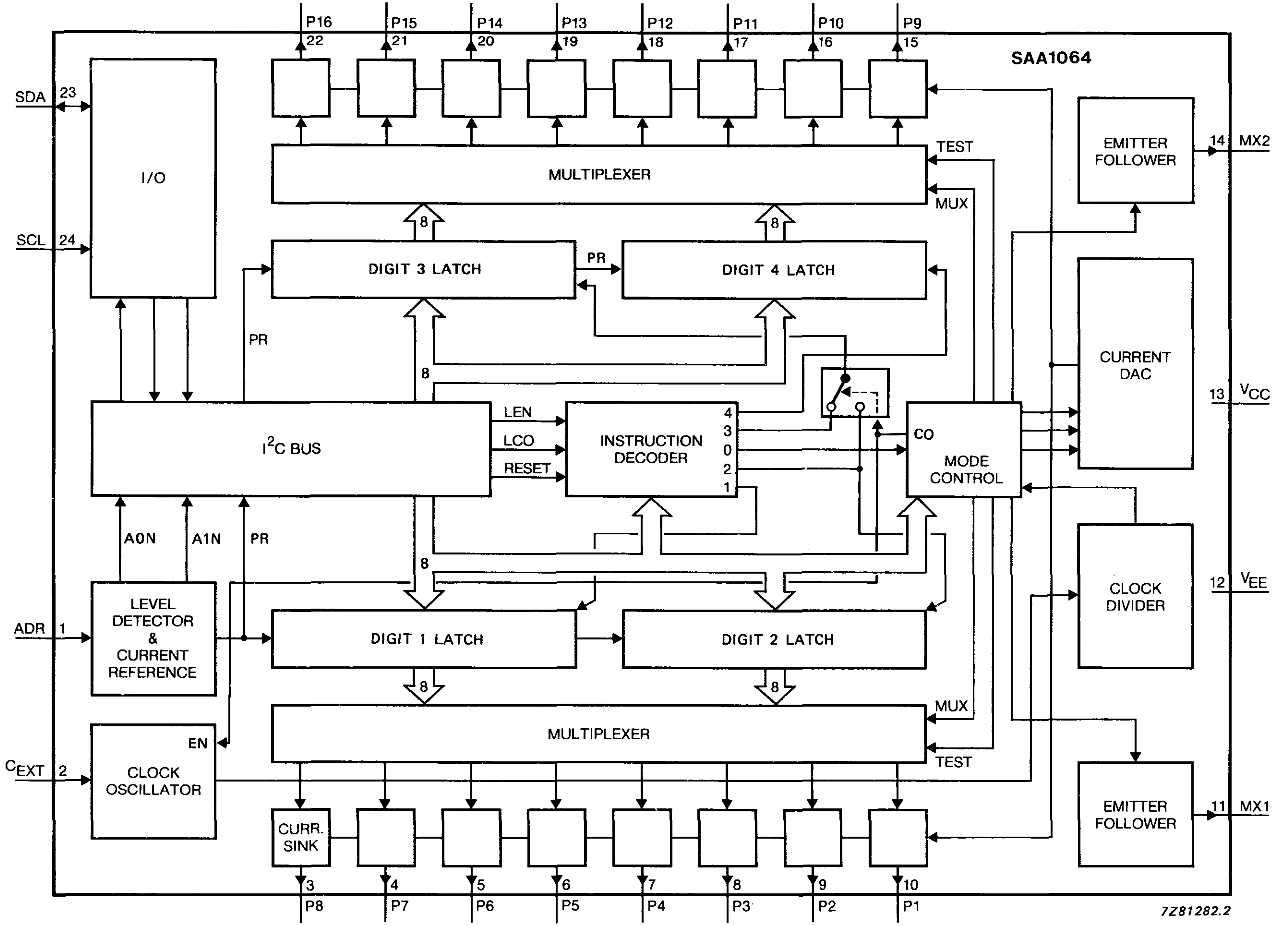


Fig. 1 Block diagram.

PINNING

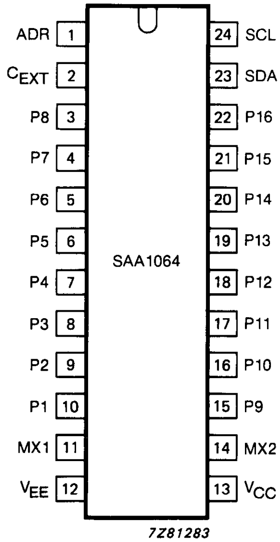


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

S	0 1 1 1 0 A1 A0 1	A	PR 0 0 0 0 0 0 0	1	P
	slave address		status byte		

Fig. 3a I²C bus format; READ mode.

S	0 1 1 1 0 A1 A0 0	A	0 0 0 0 0 SC SB SA	A	X C6 C5 C4 C3 C2 C1 C0	A
	slave address		instruction byte		control byte	

D17----------------D10	A	D27----------------D20	A	D37----------------D30	A	D47----------------D40	A	P
data digit 1		data digit 2		data digit 3		data digit 4		

Fig. 3b I²C bus format; WRITE mode.

S = start condition
P = stop condition
A = acknowledge
X = don't care

A1, A0 = programmable address bits
SC SB SA = subaddress bits
C6 to C0 = control bits
PR = POWER RESET flag

Address pin ADR

Four different slave addresses can be chosen by connecting ADR either to V_{EE}, 3/8 V_{CC}, 5/8 V_{CC} or V_{CC}. This results in the corresponding valid addresses HEX 70, 72, 74 and 76 for writing and 71, 73, 75 and 77 for reading. All other addresses cannot be acknowledged by the circuit.

Status byte

Only one bit is present in the status byte, the POWER RESET flag. A logic 1 indicates the occurence of a power failure since the last time it was read out. After completion of the READ action this flag will be set to logic 0.

Subaddressing

The bits SC, SB and SA form a pointer and determine to which register the data byte following the instruction byte will be written. All other bytes will then be stored in the registers with consecutive subaddresses. This feature is called Auto-Increment (AI) of the subaddress and enables a quick initialization by the master.
The subaddress pointer will wrap around from 7 to 0.
The subaddresses are given as follows:

SC	SB	SA	sub-address	function
0	0	0	00	control register
0	0	1	01	digit 1
0	1	0	02	digit 2
0	1	1	03	digit 3
1	0	0	04	digit 4
1	0	1	05	reserved, not used
1	1	0	06	
1	1	1	07	

Control bits (see Fig. 4)

The control bits C0 to C6 have the following meaning:

C0 = 0	static mode, i.e. continuous display of digits 1 and 2
C0 = 1	dynamic mode, i.e. alternating display of digit 1 + 3 and 2 + 4
C1 = 0/1	digits 1 + 3 are blanked/not blanked
C2 = 0/1	digits 2 + 4 are blanked/not blanked
C3 = 1	all segment outputs are switched-on for segment test*
C4 = 1	adds 3 mA to segment output current
C5 = 1	adds 6 mA to segment output current
C6 = 1	adds 12 mA to segment output current

Data

A segment is switched ON if the corresponding data bit is logic 1. Data bits D17 to D10 correspond with digit 1, D27 to D20 with digit 2, D37 to D30 with digit 3 and D47 to D40 with digit 4.
The MSBs correspond with outputs P8 and P16, the LSBs with P1 and P9. Digit numbers 1 to 4 are equal to their subaddresses (hex) 1 to 4.

* At a current determined by C4, C5 and C6.

SDA, SCL

The SDA and SCL I/O meet the I^2C bus specification. For protection against positive voltage pulses on these inputs voltage regulator diodes are connected to V_{EE}. This means that normal line voltage should not exceed 5,5 volt. Data will be latched on the positive-going edge of the acknowledge related clock pulse.

Power-on reset

The power-on reset signal is generated internally and sets all bits to zero, resulting in a completely blanked display. Only the POWER RESET flag is set.

External Control (C_{EXT})

With a capacitor connected to pin 2 the multiplex frequency can be set (see Fig. 5). When static this pin can be connected to V_{EE} or V_{CC} or left floating since the oscillator will be switched off.

Segment outputs

The segment outputs P1 to P16 are controllable current-sink sources. They are switched on by the corresponding data bits and their current is adjusted by control bits C4, C5 and C6.

Multiplex outputs

The multiplex outputs MX1 and MX2 are switched alternately in dynamic mode with a frequency derived from the clock-oscillator. In static mode MX1 is switched on. The outputs consist of an emitter-follower, which can be used to drive the common anodes of two displays directly provided that the total power dissipation of the circuit is not exceeded. If this occurs external transistors should be connected to pins 11 and 14 as shown in Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 13)		V_{CC}	–0,5	18	V
Supply current (pin 13)		I_{CC}	–50	200	mA
Total power dissipation					
SOT-101					
24-lead DIL		P_{tot}		1000	mW
SDA, SCL voltages		$V_{23, 24\text{-}12}$	–0,5	5,9	V
Voltages A0-MX1 and MX2-P16		$V_{1\text{-}11}$, $V_{14\text{-}22}$	–0,5	V_{CC} + 0,5	V
Input/output current all pins	outputs OFF	± I	–	10	mA
Operating ambient temperature range		T_{amb}	–20	+ 70	°C
Storage temperature range		T_{stg}	–65	+ 125	°C

THERMAL RESISTANCE

From crystal to ambient

24-lead DIL	$R_{th\ cr\text{-}a}$	35 K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; voltages are referenced to ground (V_{EE} = 0 V); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 13)		V_{CC}	4,5	5,0	15	V
Supply current	all outputs OFF V_{CC} = 5 V	I_{CC}	7,0	9,5	14,0	mA
Power dissipation	all outputs OFF	P_d	–	50	–	mW
SDA; SCL bus (pins 23 and 24)						
Input voltages		$V_{23,24}$	0	–	5,5	V
Logic input voltage LOW		$V_{IL(L)}$	–	–	1,5	V
Logic input voltage HIGH		$V_{IH(L)}$	3,0	–	–	V
Input current LOW	$V_{23,24} = V_{EE}$	I_{IL}	–	–	–10	µA
Input current HIGH	$V_{23,24} = V_{CC}$	I_{IH}	–	–	10	µA
SDA						
Logic output voltage LOW	I_O = 3 mA	$V_{OL(L)}$	–	–	0,4	V
Output sink current		I_O	3	–	–	mA
Address input (pin 1)						
Input voltage programmable address bits:						
A0 = 0; A1 = 0		V_1	V_{EE}	–	$3/16V_{CC}$	V
A0 = 1; A1 = 0		V_1	$5/16V_{CC}$	$3/8V_{CC}$	$7/16V_{CC}$	V
A0 = 0; A1 = 1		V_1	$9/16V_{CC}$	$5/8V_{CC}$	$11/16V_{CC}$	V
A0 = 1; A1 = 1		V_1	$13/16V_{CC}$	–	V_{CC}	V
Input current LOW	$V_1 = V_{EE}$	I_1	–	–	–10	µA
Input current HIGH	$V_1 = V_{CC}$	I_1	–	–	10	
External control (C_{EXT}) pin 2						
Switching level input						
Input voltage LOW		V_{IL}	–	–	V_{CC}–2,5	V
Input voltage HIGH		V_{IH}	V_{CC}–1,5	–	–	V
nput current	V_2 = 2 V	I_2	–140	–160	–180	µA
	V_2 = 4 V	I_2	140	160	180	µA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Segment outputs						
(P8 to P1; pins 3 to 10) (P9 to P16; pins 15 to 22)						
Output voltages	$I_O = 15$ mA	V_O	–	–	0,5	V
Output current HIGH	$V_O = V_{CC} = 15$ V	I_O	–	–	± 10	μA
Output current LOW control bits HIGH C4, C5 and C6	$V_O = 5$ V	I_O	17,85	21	25	mA
Contribution of:						
control bit C4		I_O	2,55	3,0	4,0	mA
control bit C5		I_O	5,1	6,0	7,0	mA
control bit C6		I_O	10,2	12,0	14,0	mA
Relative segment 1 output accuracy						
with respect to highest value when:						
I_3 to I_{10} and I_{15} to $I_{22} = 3$ mA		ΔI_O	–	–	5	%
I_3 to I_{10} and I_{15} to $I_{22} = 21$ mA		ΔI_O	–	–	7	%
Multiplex 1 and 2 (pins 11 and 14)						
Output voltage (when ON)	$I_O = 50$ mA	V_O	V_{CC} 1,5	–	–	V
Output current HIGH (when ON)	$V_O = 2$ V	$I_{11}; I_{14}$	50	–	*	mA
Output current LOW (when OFF)	$V_O = 2$ V	$-I_{11}; -I_{14}$	50	70	100	mA
Output period	$C_{2\text{-}12} = 2{,}7$ nF	T_{MPX}	5	–	10	ms
	$C_{2\text{-}12} = 820$ pF	T_{MPX}	–	1,25	–	ms
	$C_{2\text{-}12} = 390$ pF	T_{MPX}	–	666	–	μs
Output duty factor			48,4	–	–	%

* Value to be fixed.

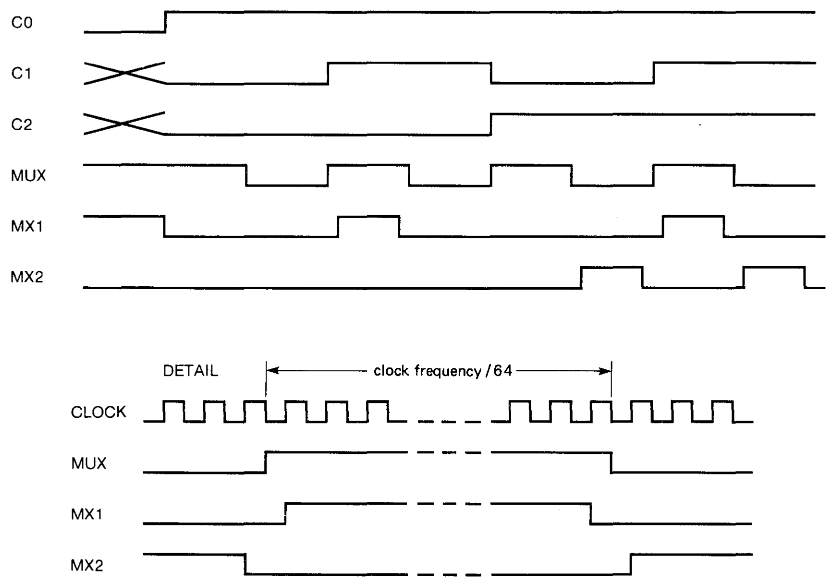


Fig. 4 Timing diagram.

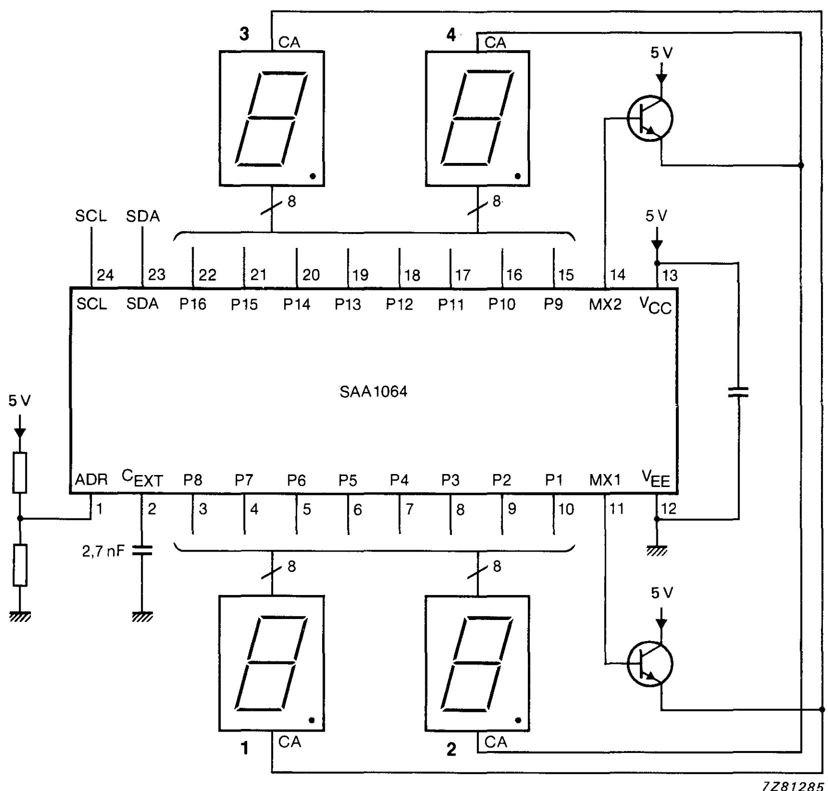


Fig. 5 Dynamic mode application diagram.

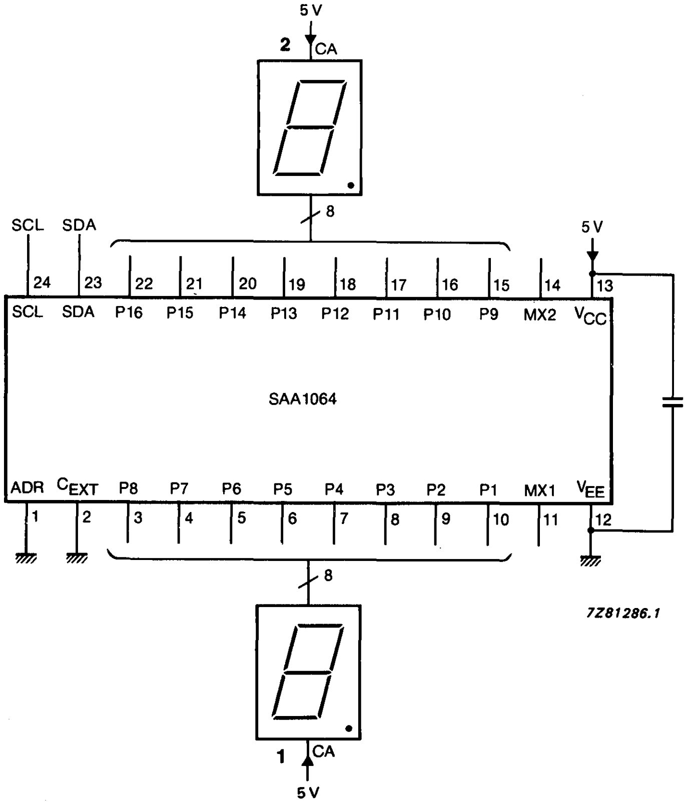


Fig. 6 Static mode application diagram.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

MICROPROCESSOR CONTROLLED STEREO SOUND GENERATOR FOR SOUND EFFECTS AND MUSIC SYNTHESIS

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5	V
Supply current (pin 18)	I_{DD}	typ.	70	mA
Reference current (pin 6)	I_{ref}	typ.	250	μA
Total power dissipation	P_{tot}		500	mW
Operating ambient temperature range	T_{amb}		0 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

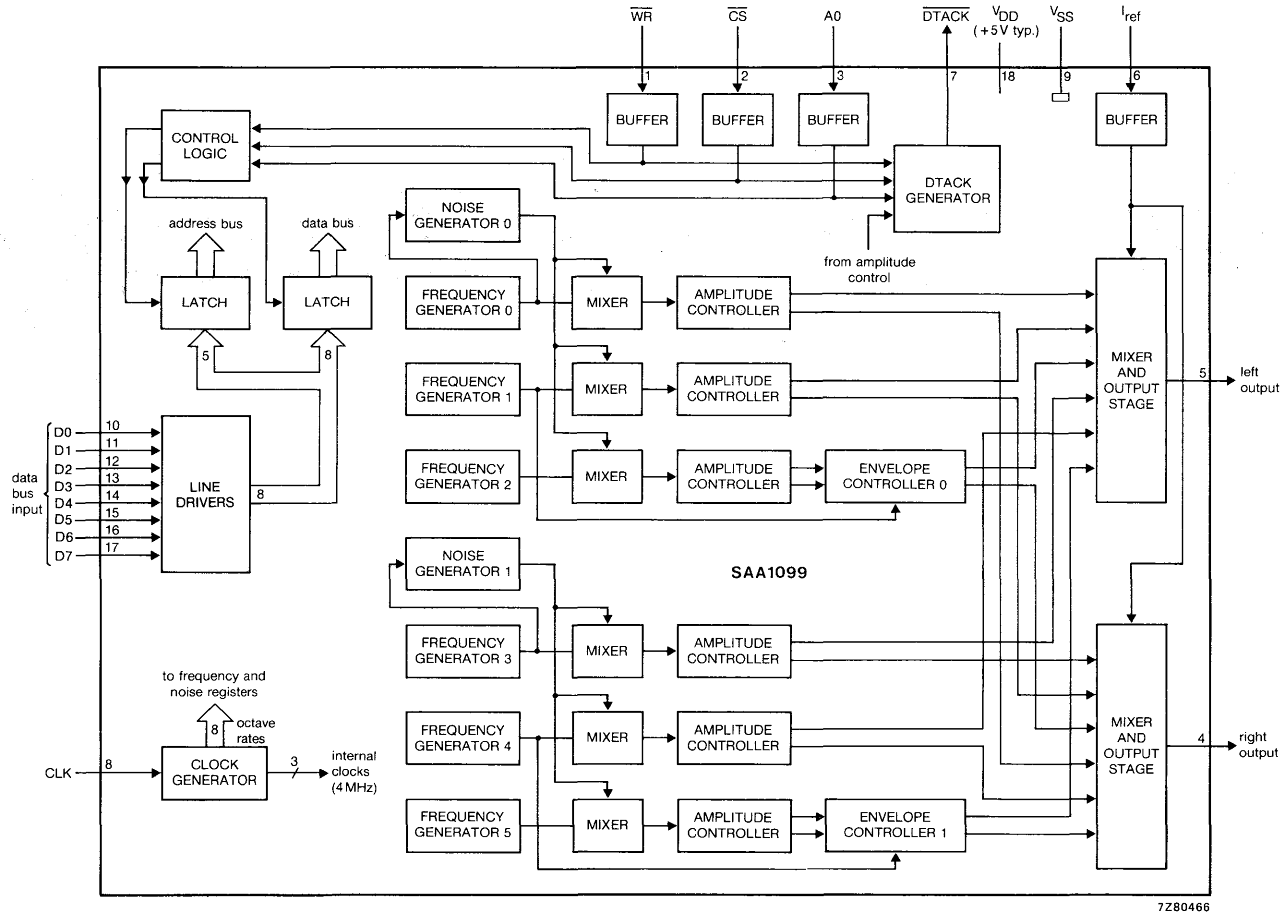


Fig. 1 Block diagram.

PINNING

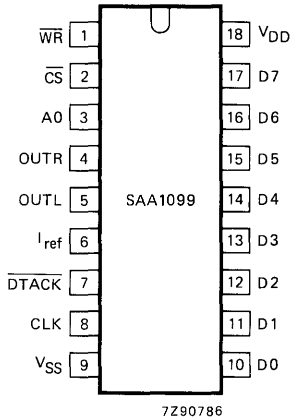


Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 31 Hz to 7,81 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone and to make it inaudible when required. The frequency generators may be synchronized using the frequency reset bit.

The frequency ranges per octave are:

Octave	Frequency range
0	31 Hz to 61 Hz
1	61 Hz to 122 Hz
2	122 Hz to 244 Hz
3	245 Hz to 488 Hz
4	489 Hz to 977 Hz
5	978 Hz to 1,95 kHz
6	1,96 kHz to 3,91 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.

In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

DEVELOPMENT DATA

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed.
To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded.
The contents of this register determines to which register the data is written in the next control-cycle.
If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}		−0,3 to +7,5	V
Maximum input voltage	V_I		−0,3 to +7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I		−0,5 to +7,5	V
Maximum output current	I_O	max.	10	mA
Total power dissipation	P_{tot}		500	mW
Storage temperature range	T_{stg}		−55 to +125	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C
Electrostatic handling*	V_{es}		−1000 to +1000	V

* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	70	100	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	–0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	$V_{7\text{-}9}$	–0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	120	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	110	%
With I_{ref} = 250 μA; R_L = 1,5 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	90	–	110	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	105	%
Output current one channel on	I_{01}	225	–	275	μA
Output current six channels on	I_{06}	1,3	–	1,6	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	150	–	350	μA
Output current six channels on	I_{06}	0,9	–	1,9	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	$4t_{CLK}$	–	–	
Bus cycle time (note 9)	t_{CY}	$16t_{CLK}$	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{LOW}	55	–	–	ns
Clock HIGH time	t_{HIGH}	55	–	–	ns

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E12 (5%) in all applications via:

$$R_L = 0{,}6\ [I_{ref}]^{-1} - 16\ [I_{ref}]^{-0{,}5} \pm 12\%$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 1,5 kΩ (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of four clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of 16 clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

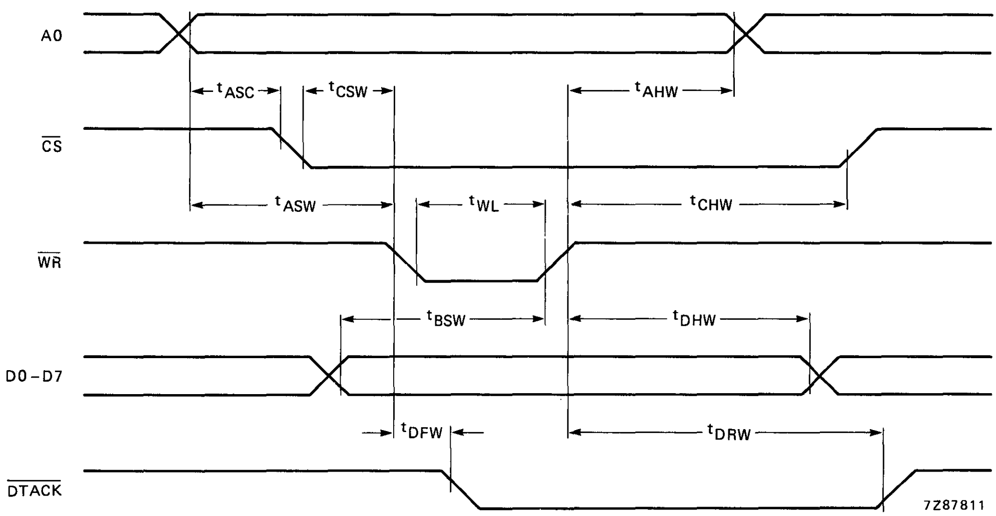


Fig. 3 Bus interface waveforms.

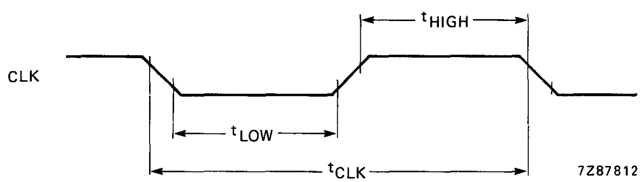


Fig. 4 Clock input waveform.

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,81 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map

register address	D7	D6	D5	D4	D3	D2	D1	D0	operations
	data bus inputs								
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	RST	SE	frequency reset (all channels) sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (31 Hz to 61 Hz) 0 0 1 (61 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (245 Hz to 488 Hz) 1 0 0 (489 Hz to 977 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,96 kHz to 3,91 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency 0 0 31,3 kHz 0 1 15,6 kHz 1 0 7,6 kHz 1 1 61 Hz to 15,6 kHz (frequency generator 0/3)

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 977 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled
RST	Reset signal to all frequency generators 0 all generators enabled 1 all generators reset and synchronized

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

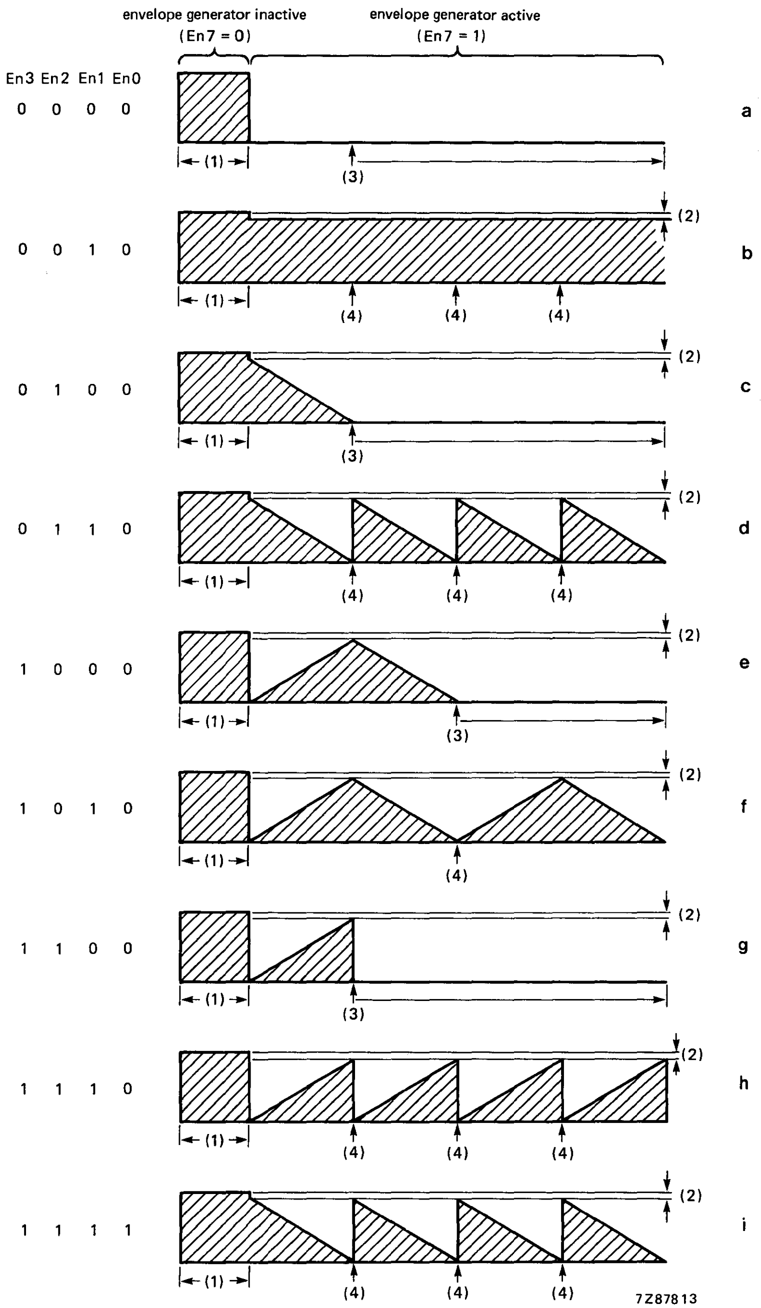


Fig. 5 Envelope waveforms.

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 7/8ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

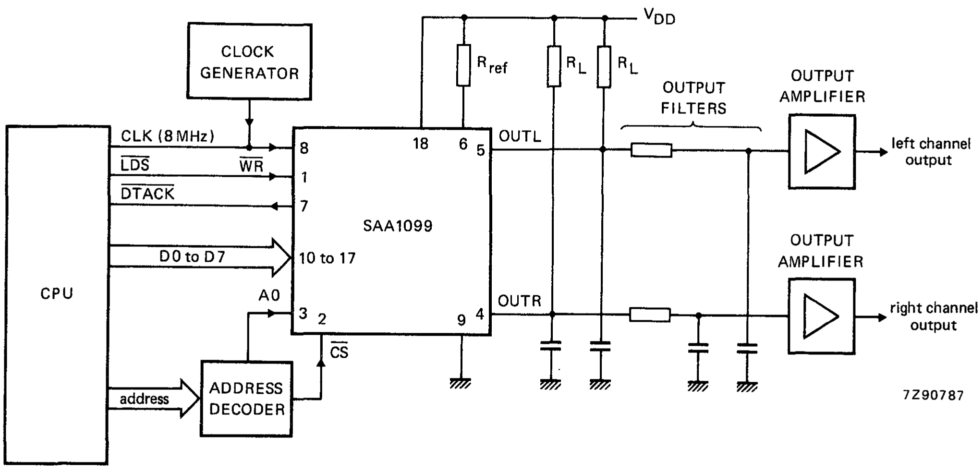


Fig. 6 Typical application circuit diagram.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

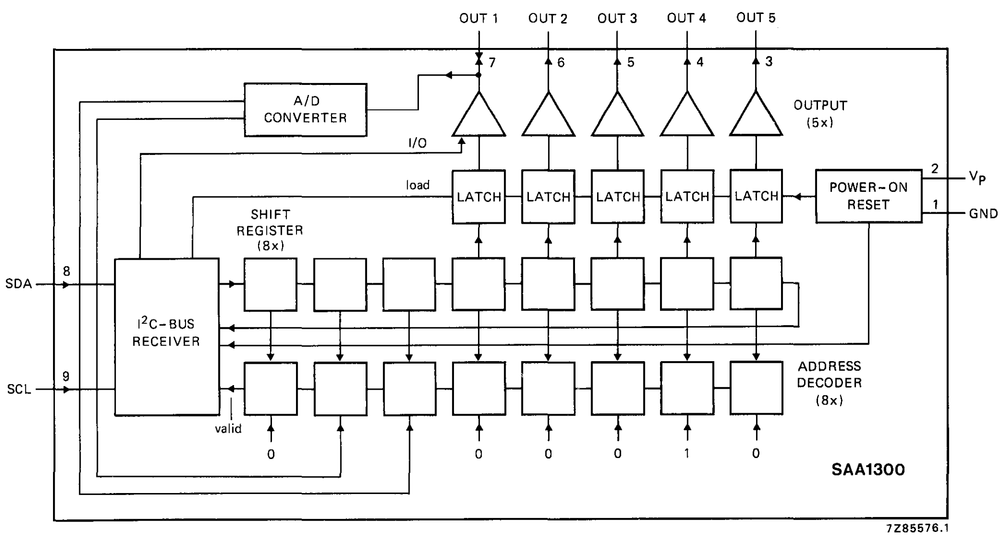


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	outputs
5	OUT 3	outputs
6	OUT 2	outputs
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 825	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF" condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

REMOTE CONTROL TRANSMITTER

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current (< 2 μA)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

SAA3004P: 20-lead DIL; plastic (SOT146).
SAA3004T: 20-lead mini-pack; plastic (SO20; SOT163A).

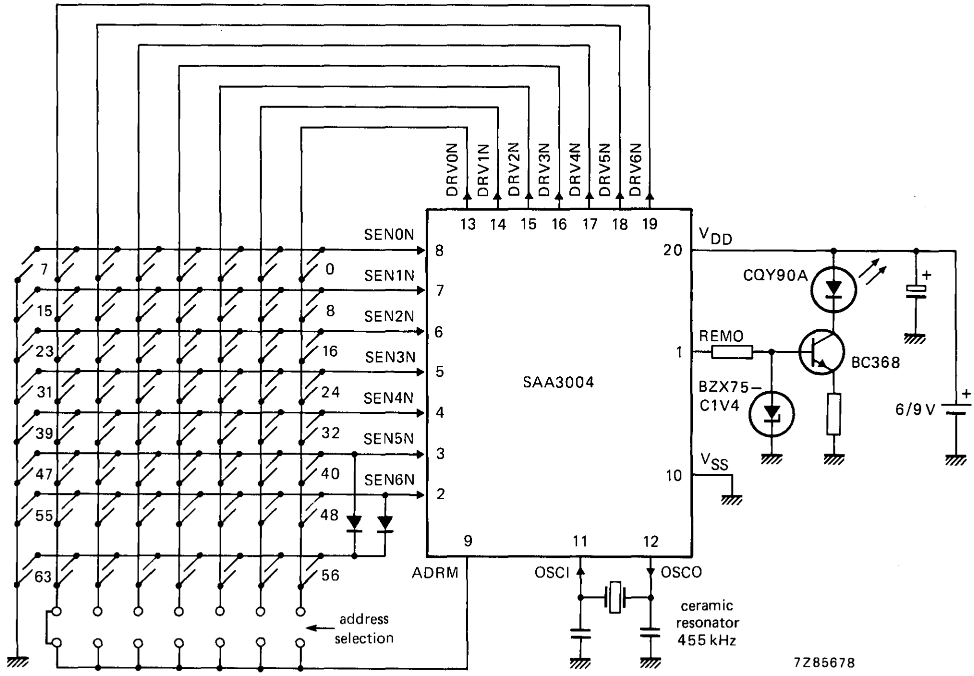


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

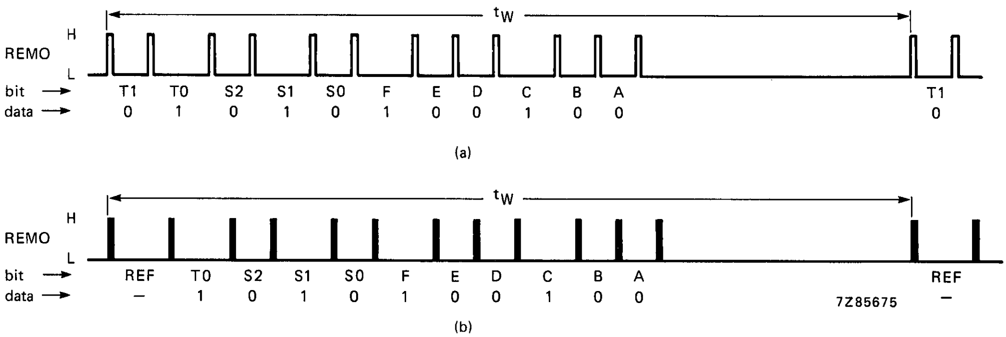
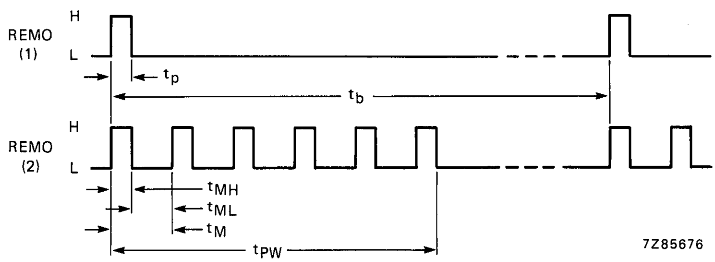


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

DEVELOPMENT DATA

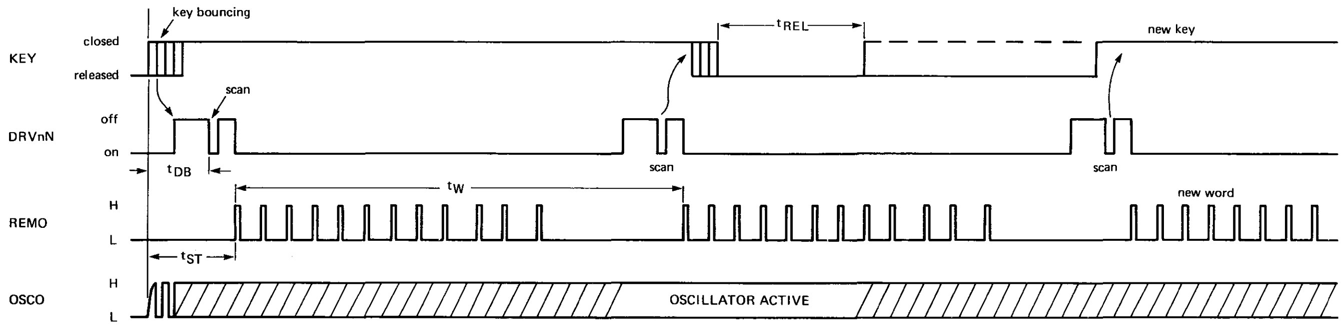


Fig. 4 Single key-stroke sequence.
Debounce time: t_{DB} = 4 to 9 x T_o.
Start time: t_{ST} = 5 to 10 x T_o.
Minimum release time: t_{REL} = T_o.
Word distance: t_W.

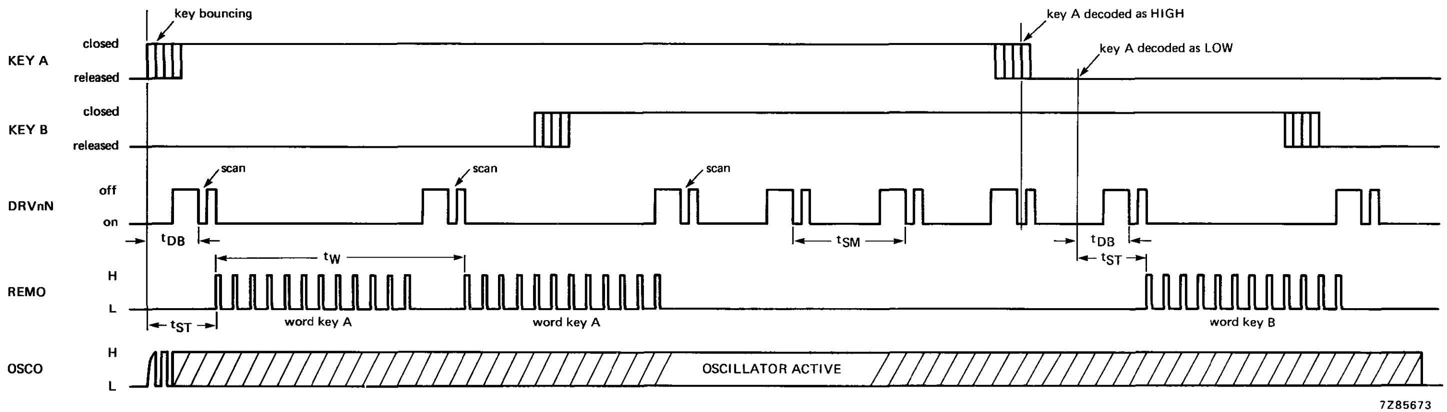


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: t_{SM} = 6 to 10 x T_o.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p µs	t_M µs	t_{ML} µs	t_{MH} µs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	t_{osc} = 2,2 µs
t_p	4 x t_{osc}	flashed pulse width
t_M	12 x t_{osc}	modulation period
t_{ML}	8 x t_{osc}	modulation period LOW
t_{MH}	4 x t_{osc}	modulation period HIGH
T_o	1152 x t_{osc}	basic unit of pulse distance
t_W	55 296 x t_{osc}	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	2 x T_o
logic "1"	3 x T_o
reference time	3 x T_o
toggle bit time	2 x T_o or 3 x T_o

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

DEVELOPMENT DATA

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

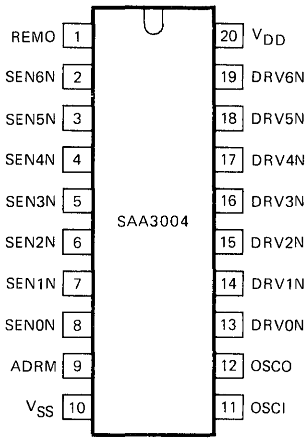


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Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	–0,5 to +15		V
Input voltage range	V_I	–0,5 to V_{DD} +0,5		V
Output voltage range	V_O	–0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = –20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	–55 to +150		°C
Operating ambient temperature range	T_{amb}	–20 to +70		°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	μA μA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	μA μA
Input leakage current $V_I = V_{DD}$	11	I_I	–	–	1	μA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	μA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	μA μA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	μA μA

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	V_{DD}–0,6	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

LOW VOLTAGE INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	2 to 7	V
Input voltage range	V_I	0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 9 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

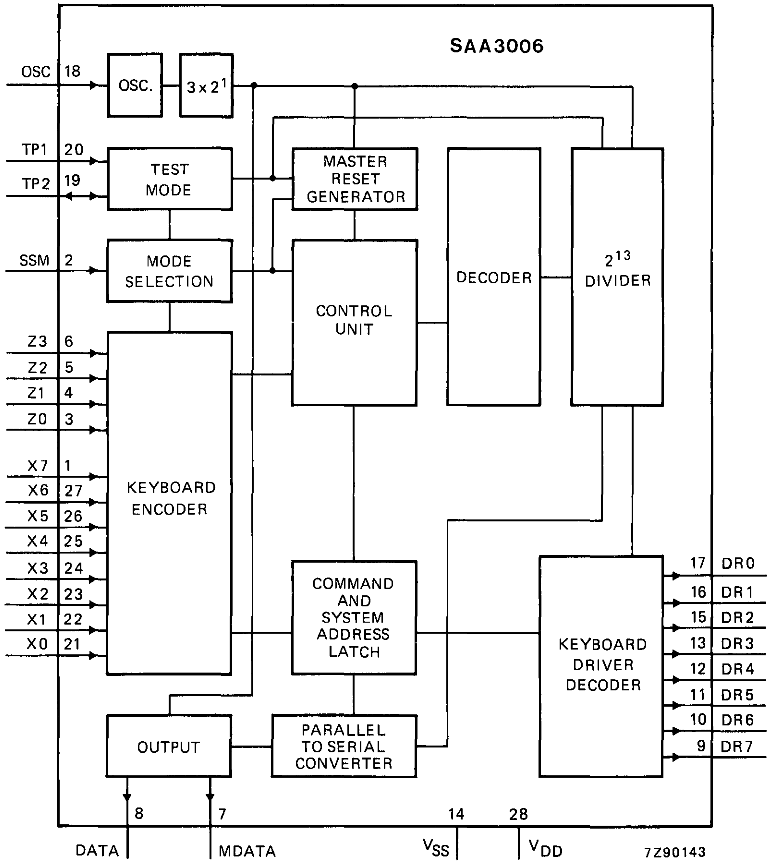


Fig. 1 Block diagram.

DEVELOPMENT DATA

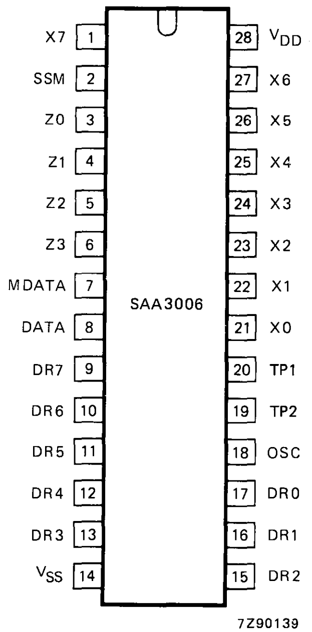
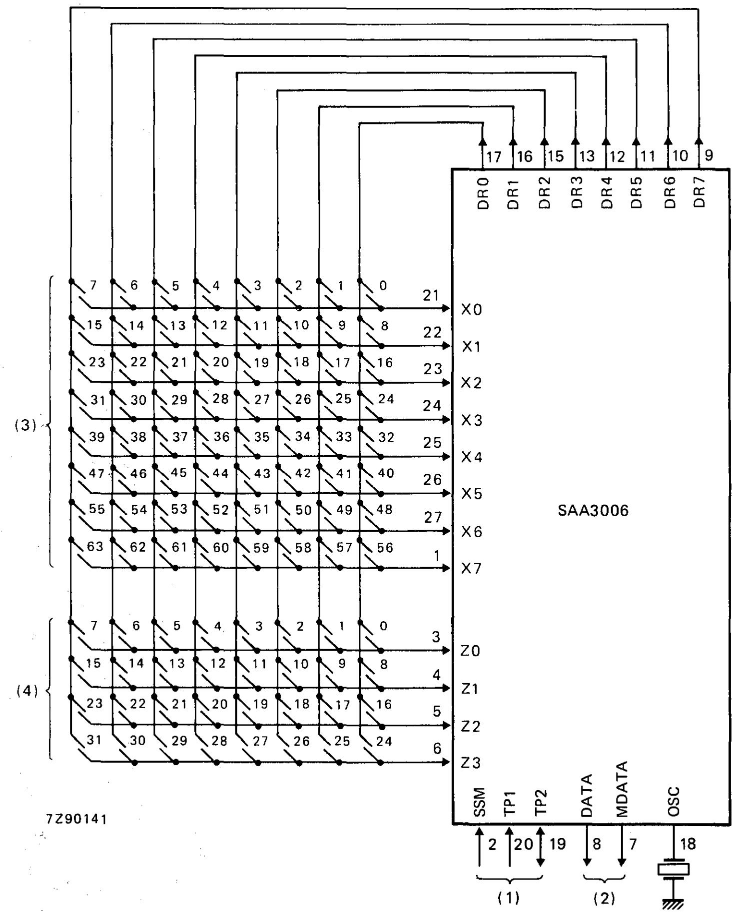


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	
22	X1	
23	X2	
24	X3	keyboard command inputs with
25	X4	P-channel pull-up transistors
26	X5	
27	X6	
1	X7	
3	Z0	
4	Z1	keyboard system inputs with
5	Z2	P-channel pull-up transistors
6	Z3	
2	SSM	system mode selection input
20	TP1	test input
19	TP2	test input/output
18	OSC	oscillator input
17	DR0	
16	DR1	
15	DR2	
13	DR3	scan driver output with open
12	DR4	drain N-channel transistors
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs
8	DATA	(3-state outputs)



(1) Control inputs for operating modes, test modes and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z- or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z- or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (catalogue number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5,25 V but it is necessary to fit a 10 kΩ resistor in series with the resonator when using supply voltages in the range 2,6 to 7 V.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of 1/12 of the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1 Test functions

TP1	TP2	Z2	Z3	function
LOW	LOW	matrix input	matrix input	normal
LOW	HIGH	matrix input	matrix input	scan + output frequency six times faster than normal
HIGH	output $f_{OSC}{}^{6}$	LOW	LOW	reset
HIGH	output $f_{OSC}{}^{6}$	HIGH	HIGH	output frequency 3×2^7 faster than normal

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7 kΩ.

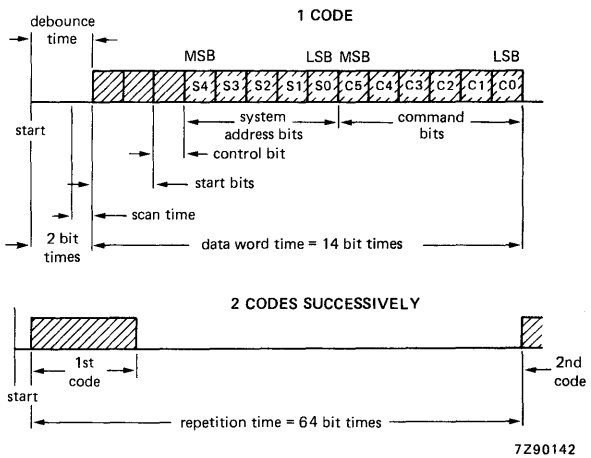


Fig. 4 DATA output format (RC-5).

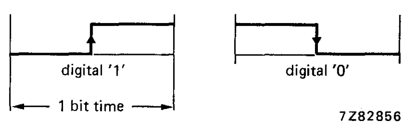


Fig. 5 Biphase transmission code; 1 bit time = $3 \times 2^8 \times T_{OSC}$ (typically 1,778 ms) where T_{OSC} is the oscillator period time.

Table 2 Command matrix X-DR

code no.	X-lines X. .								DR-lines DR. .								command bits C. .					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	•								•								0	0	0	0	0	0
1	•									•							0	0	0	0	0	1
2	•										•						0	0	0	0	1	0
3	•											•					0	0	0	0	1	1
4	•												•				0	0	0	1	0	0
5	•													•			0	0	0	1	0	1
6	•														•		0	0	0	1	1	0
7	•															•	0	0	0	1	1	1
8		•							•								0	0	1	0	0	0
9		•								•							0	0	1	0	0	1
10		•									•						0	0	1	0	1	0
11		•										•					0	0	1	0	1	1
12		•											•				0	0	1	1	0	0
13		•												•			0	0	1	1	0	1
14		•													•		0	0	1	1	1	0
15		•														•	0	0	1	1	1	1
16			•						•								0	1	0	0	0	0
17			•							•							0	1	0	0	0	1
18			•								•						0	1	0	0	1	0
19			•									•					0	1	0	0	1	1
20			•										•				0	1	0	1	0	0
21			•											•			0	1	0	1	0	1
22			•												•		0	1	0	1	1	0
23			•													•	0	1	0	1	1	1
24				•					•								0	1	1	0	0	0
25				•						•							0	1	1	0	0	1
26				•							•						0	1	1	0	1	0
27				•								•					0	1	1	0	1	1
28				•									•				0	1	1	1	0	0
29				•										•			0	1	1	1	0	1
30				•											•		0	1	1	1	1	0
31				•												•	0	1	1	1	1	1

DEVELOPMENT DATA

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

Table 3 System matrix Z-DR

system no.	Z-lines Z. .				DR-lines DR. .								system bits S. .				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5	to	8,5 V
Input voltage range	V_I	−0,5	to	$(V_{DD} + 0,5)$ V*
Input current	$+I_I$	max.		10 mA
Output voltage range	V_O	−0,5	to	$(V_{DD} + 0,5)$ V*
Output current	$+I_O$	max.		10 mA
Power dissipation output OSC	P_O	max.		50 mW
Power dissipation per output (all other outputs)	P_O	max.		100 mW
Total power dissipation per package	P_{tot}	max.		200 mW
Operating ambient temperature range	T_{amb}	−25	to	+85 °C
Storage temperature range	T_{stg}	−55	to	+150 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

* V_{DD} + 0,5 V not to exceed 9 V.

CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = -25$ to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	2	–	7	V
Supply current at $I_O = 0$ mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; $T_{amb} = 25$ °C	7	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at $V_I = 0$ V; TP = SSM = LOW	2 to 7	$-I_I$	10	–	600	μA
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at $T_{amb} = 25$ °C; TP = HIGH;						
$V_I = 7$ V		I_{IR}	–	–	1	μA
$V_I = 0$ V		$-I_{IR}$	–	–	1	μA
SSM, TP1 and TP2						
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at $T_{amb} = 25$ °C;						
$V_I = 7$ V		I_{IR}	–	–	1	μA
$V_I = 0$ V		$-I_{IR}$	–	–	1	μA
OSC						
Input leakage current at $T_{amb} = 25$ °C; $V_I = 0$ V; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7	$-I_I$	–	–	2	μA

DEVELOPMENT DATA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Outputs						
DATA and MDATA						
Output voltage HIGH at $-I_{OH}$ = 0,4 mA	2 to 7	V_{OH}	V_{DD} −0,3	–	–	V
Output voltage LOW at I_{OL} = 0,6 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at:						
V_O = 7 V		I_{OR}	–	–	10	µA
V_O = 0 V		$-I_{OR}$	–	–	20	µA
T_{amb} = 25 °C; V_O = 7 V		I_{OR}	–	–	1	µA
V_O = 0 V		$-I_{OR}$	–	–	2	µA
DR0 to DR7, TP2						
Output voltage LOW at I_{OL} = 0,3 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at V_O = 7 V	7	I_{OR}	–	–	10	µA
at V_O = 7 V T_{amb} = 25 °C		I_{OR}	–	–	1	µA
OSC						
Oscillator current at OSC = V_{DD}	7	I_{OSC}	4,5	–	30	µA
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	2	f_{OSC}	–	–	450	kHz
Free-running oscillator frequency at T_{amb} = 25 °C	2	f_{OSC}	10	–	120	kHz

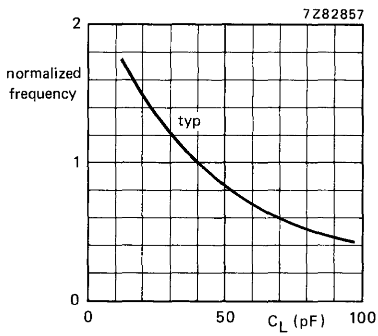


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

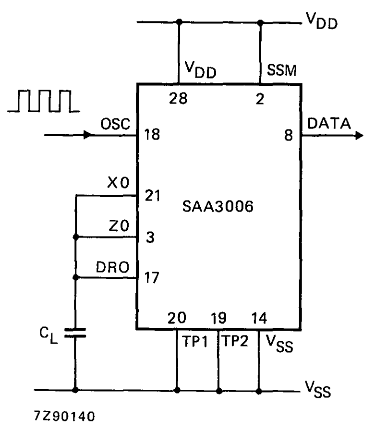


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

INFRARED REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3007 transmitter IC for infrared remote control systems has a capacity for 1280 commands arranged in 20 subsystem address groups of 64 commands each. The subsystem address may be selected by press-button or slider switches, or be hard-wired.

Commands are transmitted in patterns of pulses coded by the pulse spacing. The pulses can be infrared flashed (single pulse) or modulated. Flashed infrared transmissions require a wideband preamplifier at the receiver, but modulated transmissions allow a narrow band receiver to be used for improved noise rejection. The modulation frequency of the SAA3007 is 455 kHz which allows disturbance-free infrared operation in the presence of 10 - 100 kHz fluorescent lamps.

Features

- Flashed or modulated transmission modes
- Immune from fluorescent lamp disturbance in modulated mode
- Supply voltage range 2 V to 6,5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups } up to 1280 commands
- Up to 64 commands per subsystem address }
- Requires few additional components

PACKAGE OUTLINES

SAA3007P: 20-lead DIL; plastic (SOT146).
SAA3007T: 20-lead mini-pack; plastic (SO20; SOT163A).

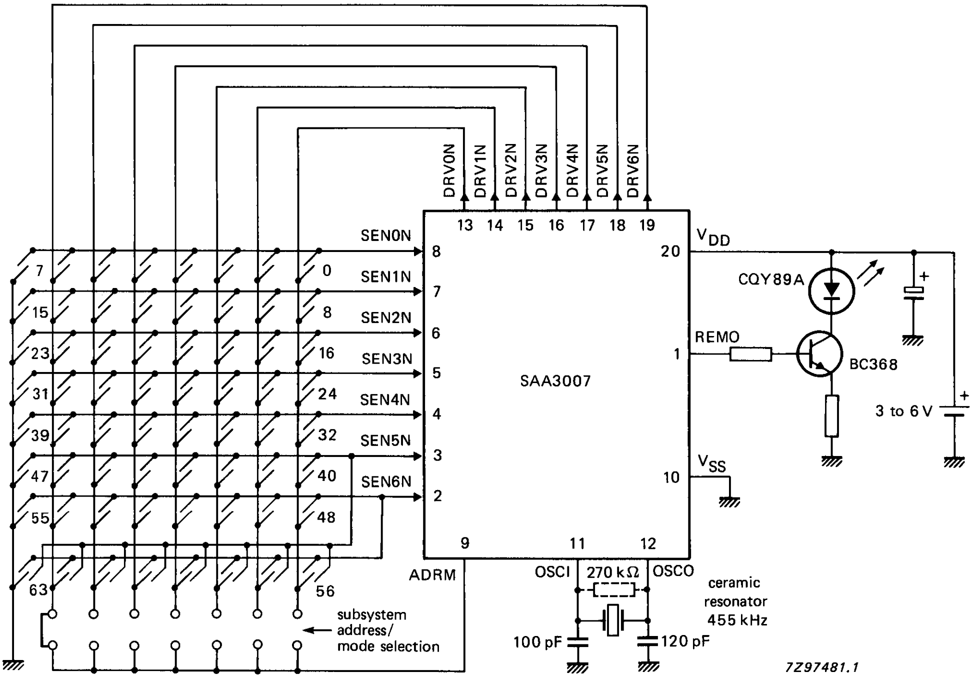


Fig. 1 SAA3007 application example.

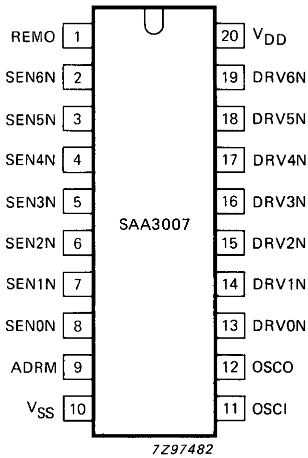


Fig. 2 Pinning diagram.

PINNING

1.	REMO	remote data output
2.	SEN6N	sense inputs from key matrix
3.	SEN5N	
4.	SEN4N	
5.	SEN3N	
6.	SEN2N	
7.	SEN1N	
8.	SEN0N	
9.	ADRM	address/mode control input
10.	V_{SS}	ground (0 V)
11.	OSCI	oscillator input
12.	OSCO	oscillator output
13.	DRV0N	drive outputs to key matrix
14.	DRV1N	
15.	DRV2N	
16.	DRV3N	
17.	DRV4N	
18.	DRV5N	
19.	DRV6N	
20.	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Key matrix (DRV0N - DRV6N and SEN0N - SEN6N)

The transmitter keyboard is arranged as a scanned matrix with seven driver lines (DRV0N to DRV6N) and seven sensing lines (SEN0N to SEN6N) as shown in Fig. 1. The matrix allows generation of 56 command codes per subsystem address, with triple contacts all 64 commands are addressable, giving a maximum possibility of 1280 commands.

Lines DRV0N to DRV6N are driven by open drain N-channel transistors (conductive in standby mode). The sense lines go to P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by key contact with a driver line. This key operation initiates a code transmission.

The maximum allowable value of contact series resistance for keyboard switches in the ON-state is 7 kΩ.

Address/mode input (ADRM)

Subsystem addresses are defined by connecting one or two of the key matrix driver lines (DRV0N to DRV6N) to the ADRM input. This allows up to 20 subsystem addresses to be generated for the REMO output (bits S3, S2, S1 and S0) as shown in Table 1 and Fig. 3.

The transmission mode is defined by the DRV6N to ADRM connection as follows:

Flashed mode	DRV6N not connected to ADRM
Modulated mode	DRV6N connected to ADRM

When more than one connection is made to ADRM then all connections should be decoupled using diodes.

The ADRM input has switched pull-up and pull-down loads. In the standby mode only 'pull-down' is active and ADRM is held LOW (this condition is independent of ADRM circuit configuration and minimizes power loss in the standby mode).
When a key is pressed the transmitter becomes active, 'pull-down' is switched off, 'pull-up' is switched on and the driver line signals are sensed for the subsystem address coding.

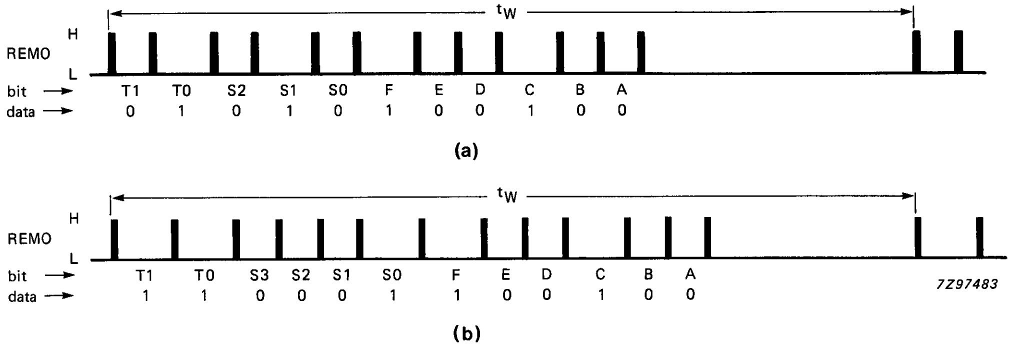
The subsystem address is sensed only within the first scan cycle, whereas the command code is sensed in every scan. The transmitted subsystem address remains unchanged if the subsystem address selection is changed while the command key is pressed. A change of the subsystem address does not start a transmission.

Remote control signal output (REMO)

The REMO output driver stage incorporates a bipolar emitter-follower which allows a high output current in the output active (HIGH) state. The format of the output pulse trains are shown in Fig. 3 and one cycle of the output waveform for flashed or modulated mode is shown in Fig. 4.

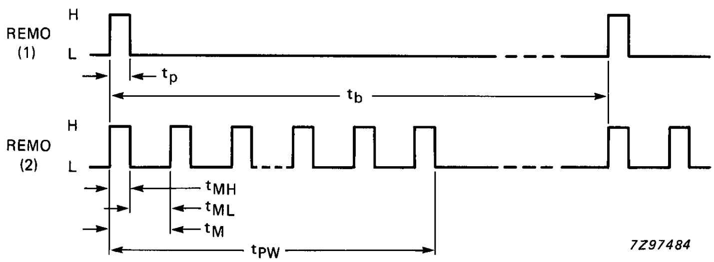
A data word starts with two toggle bits T0, T1 (Fig. 3) which indicate by changing state that the next instruction is a new command. The subsystem address is defined by the bits S3, S2, S1 and S0 (bit S3 is transmitted only for subsystem addresses 8 to 20). The selected command key is defined by bits F, E, D, C, B and A as shown in Table 2.

FUNCTIONAL DESCRIPTION (continued)



T1, T0	toggle bits
S3, S2, S1, S0	subsystem address
A to F	command bits
t_W	word length
binary values	determined by pulse spacing

Fig. 3 Data format of remote control signal (REMO); (a) subsystem addresses 1 to 7, (b) subsystem addresses 8 to 20.



(1) Flashed mode
(2) Modulated mode

Fig. 4 Waveform for one pulse period at REMO output; for timing values see Table 3.

All pulse timings are multiples of the oscillator period (t_{osc}) as given in Table 3. Information carried on the REMO output is defined as logic 1 or logic 0 by the time (t_b) between leading edges of the initial pulses of adjacent pulse periods.

Oscillator (OSCI, OSCO)

The external components for the oscillator circuit are connected to OSCI and OSCO. The oscillator operates with a ceramic resonator in the frequency range 350 kHz to 500 kHz, as defined by the resonator. With a supply voltage of less then 3 V a 270 KΩ resistor should be connected in parallel with the resonator (see Fig. 1).

Table 1 Definition of subsystem addresses

address number	driver line(s) connected to ADRM	subsystem address S3	S2	S1	S0
1	no connection	–	1	1	1
2	DRV0N	–	0	0	0
3	DRV1N	–	0	0	1
4	DRV2N	–	0	1	0
5	DRV3N	–	0	1	1
6	DRV4N	–	1	0	0
7	DRV5N	–	1	0	1
8	DRV0N and DRV2N	0	0	0	0
9	DRV0N and DRV3N	1	0	0	0
10	DRV0N and DRV4N	0	1	0	0
11	DRV0N and DRV5N	1	1	0	0
12	DRV1N and DRV2N	0	0	0	1
13	DRV1N and DRV3N	1	0	0	1
14	DRV1N and DRV4N	0	1	0	1
15	DRV1N and DRV5N	1	1	0	1
16	DRV2N and DRV3N	1	0	1	0
17	DRV2N and DRV4N	0	1	1	0
18	DRV2N and DRV5N	1	1	1	0
19	DRV3N and DRV4N	0	1	1	1
20	DRV3N and DRV5N	1	1	1	1

DEVELOPMENT DATA

Table 2 Definition of command codes

key pressed	drive-to-sense connection made	command code generated F	E	D	C	B	A
0	DRV0N to SEN0N	0	0	0	0	0	0
1	DRV1N to SEN0N	0	0	0	0	0	1
2	DRV2N to SEN0N	0	0	0	0	1	0
3	DRV3N to SEN0N	0	0	0	0	1	1
4	DRV4N to SEN0N	0	0	0	1	0	0
5	DRV5N to SEN0N	0	0	0	1	0	1
6	DRV6N to SEN0N	0	0	0	1	1	0
7	DRV7N to SEN0N	0	0	0	1	1	1
8	DRV0N to SEN1N	0	0	1	0	0	0
9	DRV1N to SEN1N	0	0	1	0	0	1
10	DRV2N to SEN1N	0	0	1	0	1	0
11	DRV3N to SEN1N	0	0	1	0	1	1
12	DRV4N to SEN1N	0	0	1	1	0	0
13	DRV5N to SEN1N	0	0	1	1	0	1
14	DRV6N to SEN1N	0	0	1	1	1	0
15	DRV7N to SEN1N	0	0	1	1	1	1

Table 2 Definition of command codes (continued)

key pressed	drive-to-sense connection made	command code generated F	E	D	C	B	A
16	DRV0N to SEN2N	0	1	0	0	0	0
17	DRV1N to SEN2N	0	1	0	0	0	1
18	DRV2N to SEN2N	0	1	0	0	1	0
19	DRV3N to SEN2N	0	1	0	0	1	1
20	DRV4N to SEN2N	0	1	0	1	0	0
21	DRV5N to SEN2N	0	1	0	1	0	1
22	DRV6N to SEN2N	0	1	0	1	1	0
23	DRV7N to SEN2N	0	1	0	1	1	1
24	DRV0N to SEN3N	0	1	1	0	0	0
25	DRV1N to SEN3N	0	1	1	0	0	1
26	DRV2N to SEN3N	0	1	1	0	1	0
27	DRV3N to SEN3N	0	1	1	0	1	1
28	DRV4N to SEN3N	0	1	1	1	0	0
29	DRV5N to SEN3N	0	1	1	1	0	1
30	DRV6N to SEN3N	0	1	1	1	1	0
31	DRV7N to SEN3N	0	1	1	1	1	1
32	DRV0N to SEN4N	1	0	0	0	0	0
33	DRV1N to SEN4N	1	0	0	0	0	1
34	DRV2N to SEN4N	1	0	0	0	1	0
35	DRV3N to SEN4N	1	0	0	0	1	1
36	DRV4N to SEN4N	1	0	0	1	0	0
37	DRV5N to SEN4N	1	0	0	1	0	1
38	DRV6N to SEN4N	1	0	0	1	1	0
39	DRV7N to SEN4N	1	0	0	1	1	1
40	DRV0N to SEN5N	1	0	1	0	0	0
41	DRV1N to SEN5N	1	0	1	0	0	1
42	DRV2N to SEN5N	1	0	1	0	1	0
43	DRV3N to SEN5N	1	0	1	0	1	1
44	DRV4N to SEN5N	1	0	1	1	0	0
45	DRV5N to SEN5N	1	0	1	1	0	1
46	DRV6N to SEN5N	1	0	1	1	1	0
47	DRV7N to SEN5N	1	0	1	1	1	1
48	DRV0N to SEN6N	1	1	0	0	0	0
49	DRV1N to SEN6N	1	1	0	0	0	1
50	DRV2N to SEN6N	1	1	0	0	1	0
51	DRV3N to SEN6N	1	1	0	0	1	1
52	DRV4N to SEN6N	1	1	0	1	0	0
53	DRV5N to SEN6N	1	1	0	1	0	1
54	DRV6N to SEN6N	1	1	0	1	1	0
55	DRV7N to SEN6N	1	1	0	1	1	1
56	DRV0N to SEN5N and SEN6N	1	1	1	0	0	0
57	DRV1N to SEN5N and SEN6N	1	1	1	0	0	1
58	DRV2N to SEN5N and SEN6N	1	1	1	0	1	0
59	DRV3N to SEN5N and SEN6N	1	1	1	0	1	1
60	DRV4N to SEN5N and SEN6N	1	1	1	1	0	0
61	DRV5N to SEN5N and SEN6N	1	1	1	1	0	1
62	DRV6N to SEN5N and SEN6N	1	1	1	1	1	0
63	DRV7N to SEN5N and SEN6N	1	1	1	1	1	1

Table 3 Pulse timing

parameter	symbol	duration	duration at f_{osc} = 455 kHz; t_{osc} = 2,2 μs
Flashed pulse width	t_p	4 x t_{osc}	8,8 μs
Modulation period	t_M	1 x t_{osc}	2,2 μs
Modulation LOW time	t_{ML}	0,5 x t_{osc}	1,1 μs
Modulation HIGH time	t_{MH}	0,5 x t_{osc}	1,1 μs
Modulation pulse width	t_{pw}	$7t_M + t_{MH}$	16,5 μs
Basic unit of pulse spacing	t_o	1152 x t_{osc}	2,53 ms
Word length for sub-system addresses			
1 to 7	t_W	55296 x t_{osc}	121 ms
8 to 20	t_W	59904 x t_{osc}	132 ms
Pulse spacing for			
logic 0	t_b	2 x t_o	5,06 ms
logic 1	t_b	3 x t_o	7,59 ms

DEVELOPMENT DATA

OPERATION

Keyboard

In the standby mode all drivers DRV0N - DRV6N are 'on' but are non-conducting due to their open drain configuration. When a key is pressed, a completed drain connection pulls down one or more of the sense lines to ground. Referring to Fig. 5, the power-up sequence for the IC commences as a key is pressed. The oscillator becomes active and then, following the debounce time (t_{DB}), the output drivers become active successively.

Within the first scan cycle the mode selection, subsystem address and the selected command are sensed and loaded into an internal data latch.

Multiple keystroke protection

In a multiple keystroke sequence the command selected is always that of the first key to be sensed and the scan rate increases to speed detection of a key-release (Fig. 6).

If more than one key is pressed at the same time, the output sequence is not changed.

There are two restrictions caused by the special structure of the keyboard matrix:

The keys switching directly to ground (codes 7, 15, 23, 31, 39, 47, 55, 63) are not completely covered by multiple keystroke protection. If one sense input is switched to ground, other keys on that sense line are ignored.

The sense lines SEN5N and SEN6N are not protected against multiple keystrokes on the same driver line because this has been used to define codes 56 to 63.

Output sequence

The output operation starts when the selected code has been detected. A burst of pulses, including the latched address and command codes, is generated at the output REMO for as long as the key is pressed. The format of the output pulse train is as shown in Figs 3 and 4. The operation is terminated by releasing the key, or by pressing more than one key at the same time. Once a sequence has been started, the transmitted words will always be completed after the key has been released.

The toggle bits T0, T1 are incremented if the key is released for a minimum time t_{REL} (Fig. 5). They remain unchanged in a multiple keystroke sequence.

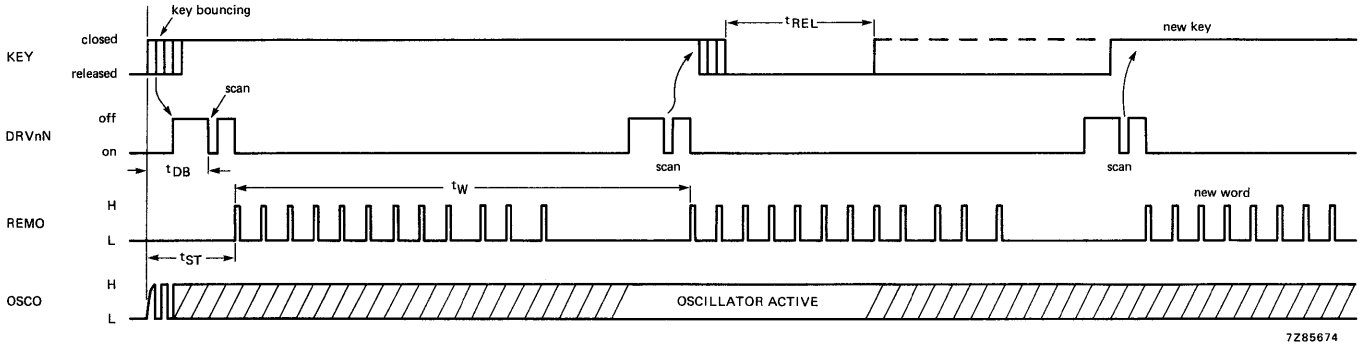


Fig. 5 Single keystroke sequence: t_{DB} = debounce time = 4 T_o to 9 T_o; t_{ST} = start time = 5 T_o to 10 T_o; t_{REL} = minimum release time = T_o; t_W = word length.

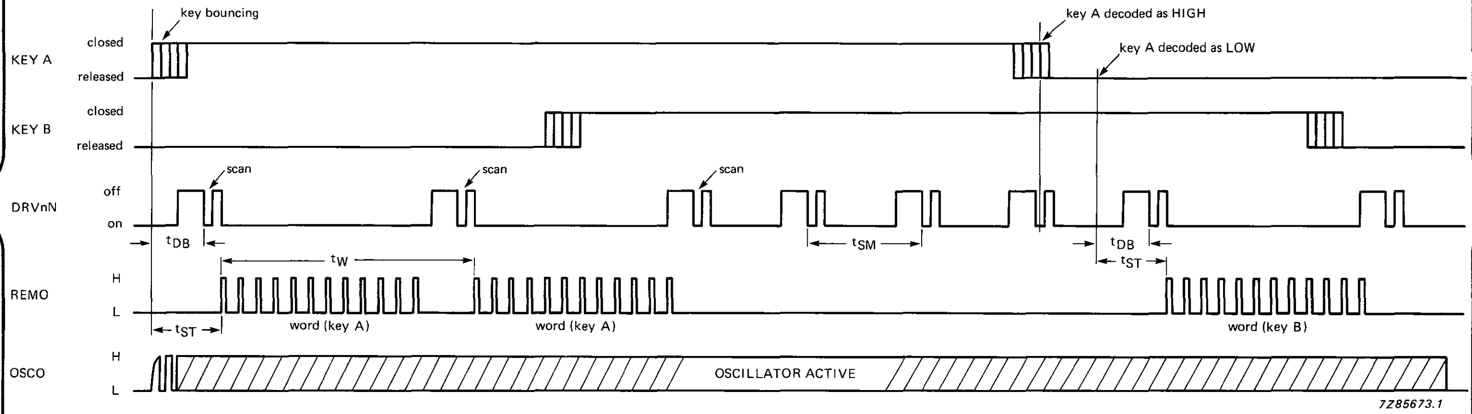


Fig. 6 Multiple keystroke sequence: t_{SM} = scan rate (multiple keystroke) = 6 T_o to 10 T_o; t_{DB}, t_{ST} and t_W are as per Fig. 5.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	$V_{DD} = V_{20\text{-}10}$	−0,3	+ 7	V
Input voltage range	V_I	−0,3	V_{DD} + 0,3	V
Output voltage range	V_O	−0,3	V_{DD} + 0,3	V
Total power dissipation				
DIL package (SOT-146C1)	P_{tot}	−	300	mW
mini-pack (SO-20; SOT-163A)	P_{tot}	−	200	mW
Power dissipation				
matrix outputs DRV0N to DRV6N	P_O	−	50	mW
remote data output REMO	P_O	−	200	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	^oC
Storage temperature range	T_{stg}	−20	+ 125	^oC

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 0 to +70 ^oC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 20	V_{DD}	2,0	−	6,5	V
Supply current						
active	f_{osc} = 455 kHz;					
	V_{DD} = 3,0 V	I_{DD}	−	0,25	−	mA
	V_{DD} = 4,5 V	I_{DD}	−	0,5	−	mA
	V_{DD} = 6,0 V	I_{DD}	−	1,0	−	mA
Supply current						
standby mode	T_{amb} = 25 ^oC;					
	V_{DD} = 6,0 V	I_{DD}	−	−	4	μA
Oscillator frequency						
(ceramic resonator)	V_{DD} = 2 to 6,5 V	f_{osc}	350	−	500	kHz

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs SEN0N to SEN6N						
Input voltage LOW	V_{DD} = 2 to 6,5 V	V_{IL}	–	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{DD} = 2 to 6,5 V	V_{IH}	0,7 x V_{DD}	–	–	V
Input current (P-channel pull-up)	V_{IL} = 0 V; V_{DD} = 2 V	$-I_I$	10	–	100	μA
	V_{IL} = 0 V; V_{DD} = 6,5 V	$-I_I$	100	–	600	μA
Outputs DRV0N to DRV6N (open drain)						
Output voltage "ON"	I_O = 0,25 mA; V_{DD} = 2 V	V_{OL}	–	–	0,3	V
	I_O = 2,5 mA; V_{DD} = 6,5 V	V_{OL}	–	–	0,6	V
Output current "OFF"	V_{DD} = 6,5 V	I_O	–	–	10	μA
Input ADRM						
Input voltage LOW		V_{IL}	–	–	0,4 x V_{DD}	V
Input voltage HIGH		V_{IH}	0,85 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up and pull-down)						
pull-up active	V_I = 0 V; V_{DD} = 2 V	$-I_{IL}$	10	–	100	μA
	V_I = 0 V; V_{DD} = 6,5 V	$-I_{IL}$	100	–	600	μA
pull-down active	V_I = V_{DD}; V_{DD} = 2 V	I_{IH}	10	–	100	μA
	V_I = 0 V; V_{DD} = 6,5 V	I_{IH}	100	–	600	μA
Output REMO						
Output voltage HIGH	$-I_{OH}$ = 40 mA; T_{amb} = 25 °C;					
	V_{DD} = 2 V	V_{OH}	0,8	–	–	V
	V_{DD} = 6,5 V	V_{OH}	5,0	–	–	V
	$-I_{OH}$ = 100 mA; T_{amb} = 25 °C;					
	V_{DD} = 4 V	V_{OH}	1,5	–	–	V
	V_{DD} = 6,5 V	V_{OH}	4,5	–	–	V
	$-I_{OH}$ = 0,5 mA; V_{DD} = 2 V	V_{OH}	0,8 x V_{DD}	–	–	V
Output voltage LOW	I_{OL} = 0,5 mA; V_{DD} = 2 V	V_{OL}	–	–	0,4	V
	I_{OL} = 2,0 mA; V_{DD} = 6,5 V	V_{OL}	–	–	0,4	V

parameter	conditions	symbol	min.	typ.	max.	unit
Input OSCI						
Input current HIGH	V_{DD} = 2 V	I_{IH}	–	–	5,0	μA
	V_{DD} = 6,5 V	I_{IH}	5,0	–	70	μA
Output OSCO						
Output voltage HIGH	$-I_{OH}$ = 100 μA; V_{DD} = 6,5 V	V_{OH}	V_{DD} –0,8	–	–	V
Output voltage LOW	I_{OL} = 100 μA; V_{DD} = 6,5 V	V_{OL}	–	–	0,7	V

INFRARED REMOTE CONTROL TRANSMITTER (RECS 80 LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3008 transmitter IC is designed for infrared remote control systems. It has a capacity for 1280 commands arranged in 20 sub-system address groups of 64 commands each. The subsystem address may be selected by press-button, slider switches or be hard-wired.

Commands are transmitted in patterns which are pulse distance coded. Modulated pulse transmissions allow a narrow-band receiver to be used for improved noise rejection. The modulation frequency of the SAA3008 is 38 kHz which is 1/12 of the oscillator frequency of 455 kHz (typical).

Features

- Modulated transmission
- Ceramic resonator controlled frequency
- Data-word-start with reference time of unique start pattern
- Supply voltage range 2 V to 6.5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups } up to 1280 commands
- Up to 64 commands per subsystem address }
- Requires few additional components

PACKAGE OUTLINES

SAA3008P: 20-lead DIL; plastic (SOT146).
SAA3008T: 20-lead mini-pack; plastic (SO20; SOT163A).

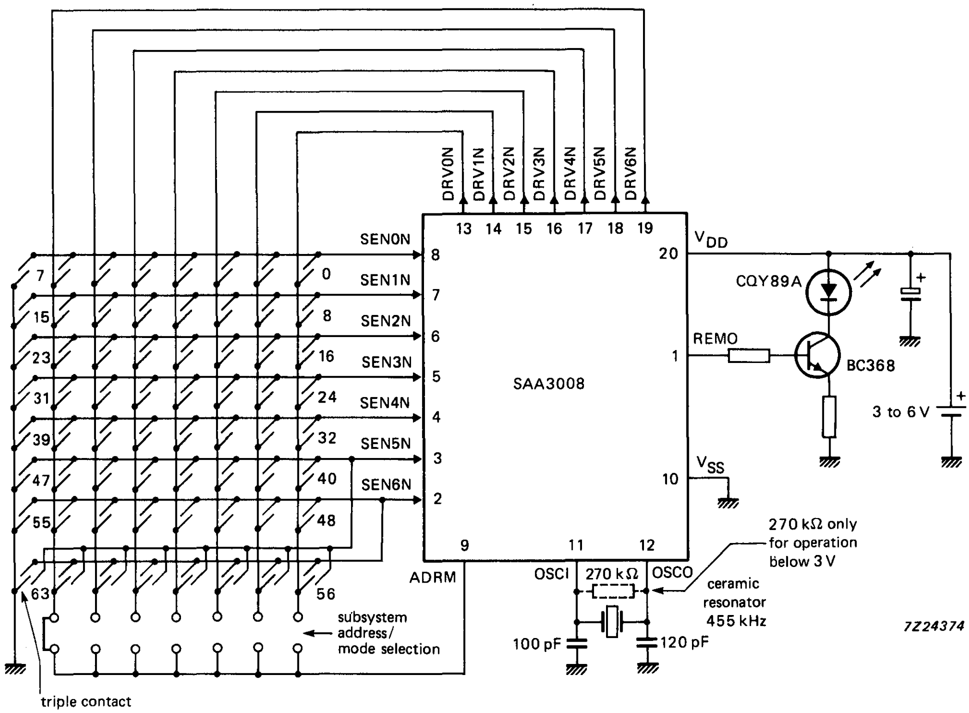


Fig.1 SAA3008 application example.

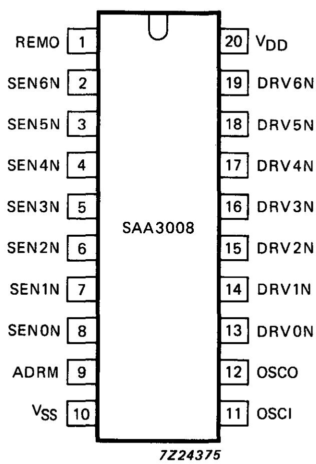


Fig.2 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	
3	SEN5N	
4	SEN4N	
5	SEN3N	sense inputs from key matrix
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address/mode control input
10	V_{SS}	ground (0 V)
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	
14	DRV1N	
15	DRV2N	
16	DRV3N	drive outputs to key matrix
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Key matrix (DRV0N - DRV6N and SEN0N - SEN6N)

The transmitter keyboard is arranged as a scanned matrix with seven driver outputs (DRV0N to DRV6N) and seven sensing inputs (SEN0N to SEN6N) as shown in Fig.1. The driver outputs are open-drain n-channel transistors which are conductive in the stand-by mode. The sensing inputs enable the generation of 56 command codes. With two external diodes connected (or triple contact), as in Fig.1, all 64 commands are addressable. The sense lines have p-channel pull-up transistors, so that they are HIGH until pulled LOW by connecting them to an output via a key depression to initiate a code transmission.
The maximum allowable value of contact series resistance for keyboard switches in the ON-state is 7 kΩ.

Address/mode input (ADRM)

Subsystem addresses are defined by connecting one or two of the key matrix driver lines (DRV0N to DRV6N) to the ADRM input. This allows up to 20 subsystem addresses to be generated for the REMO output (bits S3, S2, S1 and S0) as shown in Table 1 and Fig.3.

The transmission mode is defined by the DRV6N to ADRM connection as follows:

- Mode 1 DRV6N not connected to ADRM
- Mode 2 DRV6N connected to ADRM

In Mode 1 the reference time REF equals 3To, this may be used as a reference time for the decoding sequence. In Mode 2 an additional modulated pulse has been inserted into the middle of the reference time, therefore, these pulses are now separated by 1.5To. This unique start pattern START uses the detection of a beginning word (see Fig.3).
When more than one connection is made to ADRM then all connections should be decoupled using diodes.

The ADRM input has switched pull-up and pull-down loads. In the standby mode only pull-down load is active and ADRM input is held LOW (this condition is independent of the ADRM circuit configuration and minimizes power loss in the standby mode). When a key is pressed the transmitter becomes active (pull-down is switched OFF, pull-up is switched ON) and the driver line signals are sensed for the subsystem address coding.

The subsystem address is sensed only within the first scan cycle, whereas the command code is sensed in every scan. The transmitted subsystem address remains unchanged if the subsystem address selection is changed while the command key is pressed. A change of the subsystem address does not start a transmission.

In a multiple keystroke sequence (Fig.6) the second word B might be transmitted with subsystem address 18 or 19 instead of the preselected subsystem address (Table 1). This is only relevant for systems decoding subsystem address 18 or 19.

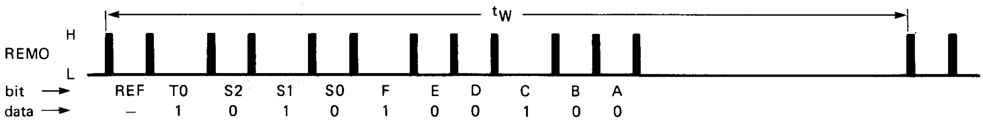
Remote control signal output (REMO)

The REMO output driver stage incorporates a bipolar emitter-follower which allows a high output current in the output active (HIGH) state (Fig.7).
The information is defined by the distance 't_b' between the leading edges of the modulated pulses (Fig.4). The distance t_b is a multiple of the basic unit T_o (Table 3) which equals 1152 periods of the oscillator frequency f_{osc} (Table 3). The pulses are modulated with 6 periods of 1/12 of the oscillator frequency (38 kHz).
The format of the output data is illustrated in Figs 3 and 4.
A data word starts with the reference time and toggle bit T0 and is followed by the definition bits for the subsystem address S3, S2, S1 and S0 (bit S3 is transmitted only for subsystem addresses 8 to 20). The selected command key is defined by bits F, E, D, C, B and A as shown in Table 2.

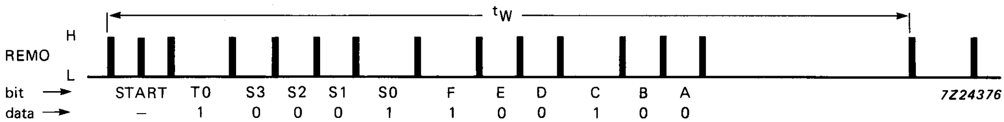
DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The toggle bit T0 acts as an indication for the decoder whether the next instruction should be considered as a new command or not. The codes for the subsystem address and the selected key are given in Table 3.



(a) Transmission with reference time and subsystem addresses 1 to 7.



(b) Transmission with start-pattern and subsystem addresses 8 to 20.

Where:

Reference time	
start pattern T0	toggle bit
S3, S2, S1, S0	subsystem address
A to F	command bits
t_W	word length
binary values	determined by pulse spacing

Fig.3 Data format of remote control signal (REMO).

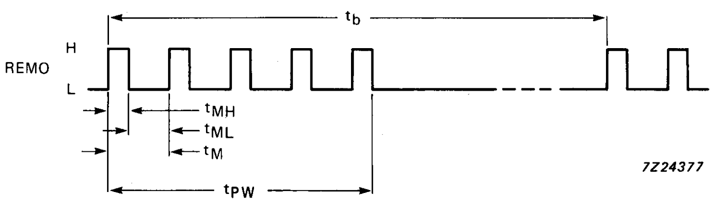


Fig.4 Waveform for one pulse period at REMO output; for timing values see Table 3.

Oscillator (OSCI, OSCO)

The external components for the oscillator circuit are connected to OSCI and OSCO. The oscillator operates with a ceramic resonator in the frequency range 350 kHz to 500 kHz, as defined by the resonator. When operating at a supply voltage of below 3 V a 270 kHz resistor should be connected in parallel with the resonator.

Table 1 Definition of subsystem addresses

address number	driver line(s) connected to ADRM	subsystem address S3	S2	S1	S0
1	no connection	–	1	1	1
2	DRV0N	–	0	0	0
3	DRV1N	–	0	0	1
4	DRV2N	–	0	1	0
5	DRV3N	–	0	1	1
6	DRV4N	–	1	0	0
7	DRV5N	–	1	0	1
8	DRV0N and DRV2N	0	0	0	0
9	DRV0N and DRV3N	1	0	0	0
10	DRV0N and DRV4N	0	1	0	0
11	DRV0N and DRV5N	1	1	0	0
12	DRV1N and DRV2N	0	0	0	1
13	DRV1N and DRV3N	1	0	0	1
14	DRV1N and DRV4N	0	1	0	1
15	DRV1N and DRV5N	1	1	0	1
16	DRV2N and DRV3N	1	0	1	0
17	DRV2N and DRV4N	0	1	1	0
18	DRV2N and DRV5N	1	1	1	0
19	DRV3N and DRV4N	0	1	1	1
20	DRV3N and DRV5N	1	1	1	1

DEVELOPMENT DATA

Table 2 Definition of command codes

key pressed	drive-to-sense connection made	command code generated F	EE	D	C	B	A
0	DRV0N to SEN0N	0	0	0	0	0	0
1	DRV1N to SEN0N	0	0	0	0	0	1
2	DRV2N to SEN0N	0	0	0	0	1	0
3	DRV3N to SEN0N	0	0	0	0	1	1
4	DRV4N to SEN0N	0	0	0	1	0	0
5	DRV5N to SEN0N	0	0	0	1	0	1
6	DRV6N to SEN0N	0	0	0	1	1	0
7	DRV7N to SEN0N	0	0	0	1	1	1
8	DRV0N to SEN1N	0	0	1	0	0	0
9	DRV1N to SEN1N	0	0	1	0	0	1
10	DRV2N to SEN1N	0	0	1	0	1	0
11	DRV3N to SEN1N	0	0	1	0	1	1
12	DRV4N to SEN1N	0	0	1	1	0	0
13	DRV5N to SEN1N	0	0	1	1	0	1
14	DRV6N to SEN1N	0	0	1	1	1	0
15	DRV7N to SEN1N	0	0	1	1	1	1
16	DRV0N to SEN2N	0	1	0	0	0	0
17	DRV1N to SEN2N	0	1	0	0	0	1
18	DRV2N to SEN2N	0	1	0	0	1	0
19	DRV3N to SEN2N	0	1	0	0	1	1
20	DRV4N to SEN2N	0	1	0	1	0	0

Table 2 Definition of command codes (continued)

key pressed	drive-to-sense connection made	command code generated F	E	D	C	B	A
21	DRV5N to SEN2N	0	1	0	1	0	1
22	DRV6N to SEN2N	0	1	0	1	1	0
23	DRV7N to SEN2N	0	1	0	1	1	1
24	DRV0N to SEN3N	0	1	1	0	0	0
25	DRV1N to SEN3N	0	1	1	0	0	1
26	DRV2N to SEN3N	0	1	1	0	1	0
27	DRV3N to SEN3N	0	1	1	0	1	1
28	DRV4N to SEN3N	0	1	1	1	0	0
29	DRV5N to SEN3N	0	1	1	1	0	1
30	DRV6N to SEN3N	0	1	1	1	1	0
31	DRV7N to SEN3N	0	1	1	1	1	1
32	DRV0N to SEN4N	1	0	0	0	0	0
33	DRV1N to SEN4N	1	0	0	0	0	1
34	DRV2N to SEN4N	1	0	0	0	1	0
35	DRV3N to SEN4N	1	0	0	0	1	1
36	DRV4N to SEN4N	1	0	0	1	0	0
37	DRV5N to SEN4N	1	0	0	1	0	1
38	DRV6N to SEN4N	1	0	0	1	1	0
39	DRV7N to SEN4N	1	0	0	1	1	1
40	DRV0N to SEN5N	1	0	1	0	0	0
41	DRV1N to SEN5N	1	0	1	0	0	1
42	DRV2N to SEN5N	1	0	1	0	1	0
43	DRV3N to SEN5N	1	0	1	0	1	1
44	DRV4N to SEN5N	1	0	1	1	0	0
45	DRV5N to SEN5N	1	0	1	1	0	1
46	DRV6N to SEN5N	1	0	1	1	1	0
47	DRV7N to SEN5N	1	0	1	1	1	1
48	DRV0N to SEN6N	1	1	0	0	0	0
49	DRV1N to SEN6N	1	1	0	0	0	1
50	DRV2N to SEN6N	1	1	0	0	1	0
51	DRV3N to SEN6N	1	1	0	0	1	1
52	DRV4N to SEN6N	1	1	0	1	0	0
53	DRV5N to SEN6N	1	1	0	1	0	1
54	DRV6N to SEN6N	1	1	0	1	1	0
55	DRV7N to SEN6N	1	1	0	1	1	1
56	DRV0N to SEN5N and SEN6N	1	1	1	0	0	0
57	DRV1N to SEN5N and SEN6N	1	1	1	0	0	1
58	DRV2N to SEN5N and SEN6N	1	1	1	0	1	0
59	DRV3N to SEN5N and SEN6N	1	1	1	0	1	1
60	DRV4N to SEN5N and SEN6N	1	1	1	1	0	0
61	DRV5N to SEN5N and SEN6N	1	1	1	1	0	1
62	DRV6N to SEN5N and SEN6N	1	1	1	1	1	0
63	DRV7N to SEN5N and SEN6N	1	1	1	1	1	1

Table 3 Pulse timing

parameter	symbol	duration	duration at f_{osc} = 455 kHz; t_{osc} = 2.2 μs
Modulation period	t_M	$12t_{osc}$	26.4 μs
Modulation LOW time	t_{ML}	$8t_{osc}$	17.6 μs
Modulation HIGH time	t_{MH}	$4t_{osc}$	8.8 μs
Modulation pulse width	t_{PW}	$5t_M + t_{MH}$	140.8 μs
Basic unit of pulse spacing	t_o	$1152t_{osc}$	2.53 ms
Word length for subsystem addresses			
0 to 7	t_W	$55296t_{osc}$	121.44 ms
8 to 20	t_W	$59904t_{osc}$	132.56 ms
Pulse separation for			
logic 0	t_b	$2t_o$	5.06 ms
logic 1	t_b	$3t_o$	7.59 ms
reference time	t_b	$3t_o$	7.59 ms
toggle bit	t_b	$2t_o$	5.06 ms
		$3t_o$	7.59 ms
Start pattern	t_b	2 x $1.5t_o$	2 x 3.79 ms

DEVELOPMENT DATA

OPERATION

Keyboard

In the standby mode all drivers DRV0N-DRV6N are ON but are non-conducting due to their open drain configuration. When a key is pressed, a completed drain connection pulls down one or more of the sense lines to ground. Referring to Fig.5, the power-up sequence for the IC commences as a key is pressed. The oscillator becomes active and then, following the debounce time (t_{DB}), the output drivers become active successively.

Within the first scan cycle the transmission mode, subsystem address and the selected command code are sensed and loaded into an internal data latch. In a multiple keystroke sequence (Fig.6) the command code is always altered according to the sensed key.

Multiple keystroke protection

The keyborad is protected against multiple keystrokes. If more than one key is pressed the circuit will not generate a new REMO sequence (Fig.6).
In a multiple keystroke sequence the scan repetition rate is increased to detect the release of the key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

- The keys switching directly to ground (codes 7, 15, 23, 31, 39, 47, 55, 63) are not completely covered by multiple keystroke protection. If one sense input is switched to ground, other keys on that sense line are ignored.
- The sense lines SEN5N and SEN6N are not protected against multiple keystrokes on the same driver line because this has been used to define codes 56 to 63.

OPERATION (continued)

Output sequence

The output operation starts when the code of the selected key has been loaded into the internal command register. A burst of pulses, including the latched address and command codes, is generated at the output REMO for as long as the key is pressed. The format of the output pulse train is as shown in Figs 3 and 4. The operation is terminated by releasing the key, or by pressing more than one key at the same time. Once a sequence has been started, the transmitted words will always be completed after the key has been released.
The toggle bit T0 is incremented if the key is released for a minimum time t_{REL} (Fig.5). In a multiple keystroke sequence the toggle bit remains unchanged.

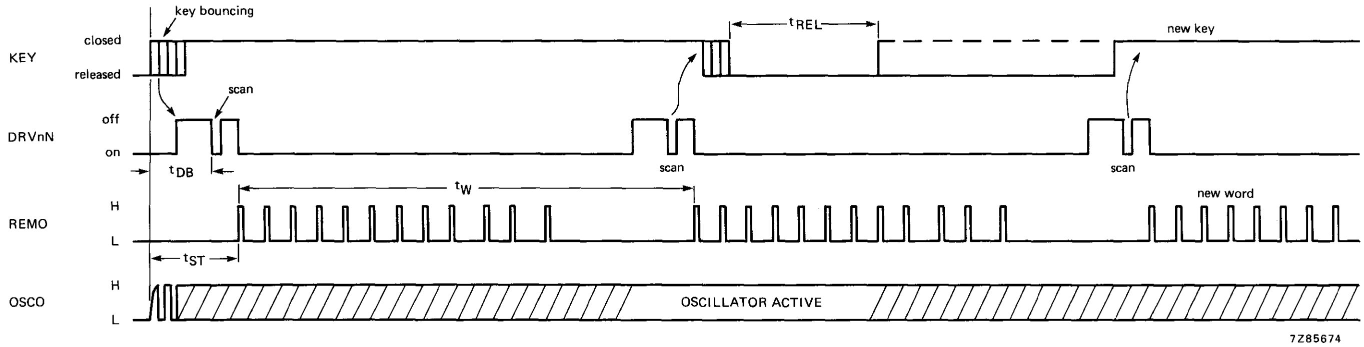


Fig.5 Single keystroke sequence; t_{DB} = debounce time = $4T_o$ to $9T_o$; t_{ST} = start time = $5T_o$ to $10T_o$; t_{REL} = minimum release time = T_o; t_W = word length.

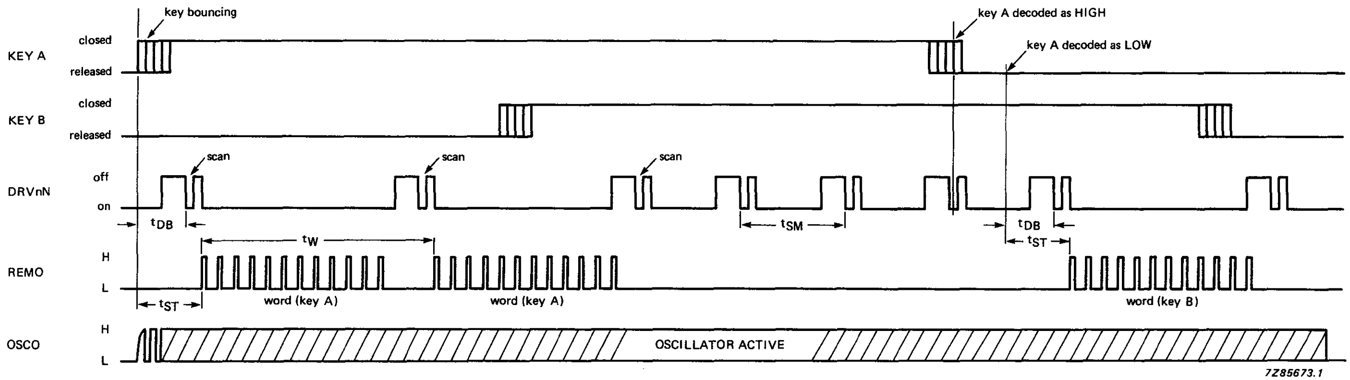


Fig.6 Scan rate multiple keystroke sequence: t_{SM} = scan rate (multiple keystroke) = $6T_o$ to $10T_o$; t_{DB}, t_{ST}, and t_W are as per Fig.5.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.3	+7	V
Input voltage range		V_I	−0.3	$V_{DD}+0.3$	V
Output voltage range		V_O	−0.3	$V_{DD}+0.3$	V
Total power dissipation					
DIL package (SOT146)		P_{tot}	–	300	mW
mini-pack (SO20; SOT163A)		P_{tot}	–	200	mW
Power dissipation					
matrix outputs DRV0N to DRV6N		P_O	–	50	mW
remote data output REMO		P_O	–	200	mW
Operating ambient temperature range		T_{amb}	−20	+70	^oC
Storage temperature range		T_{stg}	−20	+125	^oC

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 0$ to $+70$ ^oC; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	6.5	V
Supply current active	$f_{osc} = 455$ kHz;					
	$V_{DD} = 3$ V	I_{DD}	–	0.25	–	mA
	$V_{DD} = 4.5$ V	I_{DD}	–	0.5	–	mA
	$V_{DD} = 6$ V	I_{DD}	–	1	–	mA
Standby mode	$T_{amb} = 25$ ^oC;					
	$V_{DD} = 6$ V	I_{DD}	–	–	4	μA
Oscillator frequency (ceramic resonator)	$V_{DD} = 2$ to 6.5 V	f_{osc}	350	–	500	kHz
Inputs SEN0N to SEN6N						
Input voltage LOW	$V_{DD} = 2$ to 6.5 V	V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH	$V_{DD} = 2$ to 6.5 V	V_{IH}	0.7 V_{DD}	–	–	V
Input current (p-channel pull-up)	$V_{IL} = 0$ V					
	$V_{DD} = 2$ V	I_I	−10	–	−100	μA
	$V_{DD} = 6.5$ V	I_I	−100	–	−600	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs DRV0N to DRV6N (open drain 1)						
Output voltage ON	I_O = 0.25 mA; V_{DD} = 2 V	V_{OL}	–	–	0.3	V
	I_O = 2.5 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.6	V
Output current OFF	V_{DD} = 6.5 V	I_O	–	–	10	μA
Input ADRM						
Input voltage LOW		V_{IL}	–	–	0.4 V_{DD}	V
Input voltage HIGH		V_{IH}	0.85 V_{DD}	–	–	V
Input current (switched p and n channel pull-up and pull-down)						
pull-up active	V_I = 0 V					
	V_{DD} = 2 V	I_{IL}	–10	–	–100	μA
	V_{DD} = 6.5 V	I_{IL}	–100	–	–600	μA
pull-down active	V_I = V_{DD}					
	V_{DD} = 2 V	I_{IH}	10	–	100	μA
	V_{DD} = 6.5 V	I_{IH}	100	–	600	μA
Output REMO						
Output voltage HIGH	I_{OH} = –40 mA; T_{amb} = 25 °C					
	V_{DD} = 2 V	V_{OH}	0.8	–	–	V
	V_{DD} = 6.5 V	V_{OH}	5.0	–	–	V
	I_{OH} = 0.5 mA; V_{DD} = 2 V	V_{OH}	0.8 V_{DD}	–	–	V
Output voltage LOW	I_{OL} = 0.5 mA; V_{DD} = 2 V	V_{OL}	–	–	0.4	V
	I_{OL} = 2.0 mA; V_{DD} = 6.5 V	V_{OL}	–	–	0.4	V
Input OSCI						
Input current HIGH	V_{DD} = 6.5 V	I_{IH}	3.0	–	7.0	μA
Output OSCO						
Output voltage HIGH	I_{OH} = 100 μA; V_{DD} = 6.5 V	V_{OH}	V_{DD}–0.8	–	–	V
Output voltage LOW	I_{OL} = 100 μA; V_{DD} = 6.5 V	V_{OL}	–	–	0.7	V

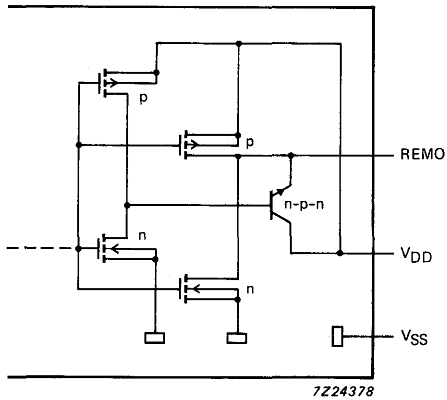


Fig.7 REMO output stage.

DEVELOPMENT DATA

INFRARED REMOTE CONTROL DECODERS

GENERAL DESCRIPTION

The main function of the SAA3009 and SAA3049 ICs is to check and convert the received coded data (RECS80/RC5) into latched binary outputs. The device address can be hard-wired for a particular address allowing several devices in one location. Alternatively, received data with any address can be accepted, the received data and address are then outputs.

Features

- Decodes 64 remote control commands with a maximum of 32 subaddresses
- Accepts RECS80 codes with pulse position modulation (SAA3004, SAA3007, SAA3008) or RC5 codes with biphase transmission (SAA3006, SAA3010)
- Available at SAA3009 with 8 high current (10 mA) open-drain outputs and internal pull-ups for direct LED drive via resistors or as SAA3049 for low supply current applications
- Adding circuitry for binary decoding allows a maximum of 2048 commands to be used, for example 1-of-16 decoder (HEF4515)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009	note 1	V_{CC}	4.5	5.0	5.5	V
SAA3049	note 2	V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009	note 1	I_{CC}	–	–	70	mA
SAA3049	note 2	I_{CC}	–	1.0	2.0	mA
Oscillator frequency		f_{osc}	–	4	–	MHz
Output sink current LOW (pins 1 to 8)						
SAA3009	note 3	I_{OL}	–	–	10	mA
SAA3049	note 4	I_{OL}	1.6	3.0	–	mA

Notes to the QUICK REFERENCE DATA

1. $T_{amb} = 0$ to $+ 70$ °C.
2. $T_{amb} = -40$ to $+ 85$ °C.
3. Open-drain with 20 to 50 kΩ internal pull-up resistor.
4. Open-drain without internal pull-up resistor at $V_{CC} = 5$ V ± 10%; $V_O = 0.4$ V.

PACKAGE OUTLINES

SAA3009P; SAA3049P: 20 lead DIL; plastic (SOT146).
SAA3049T: 20 lead mini-pack; plastic (SO20; SOT163A).

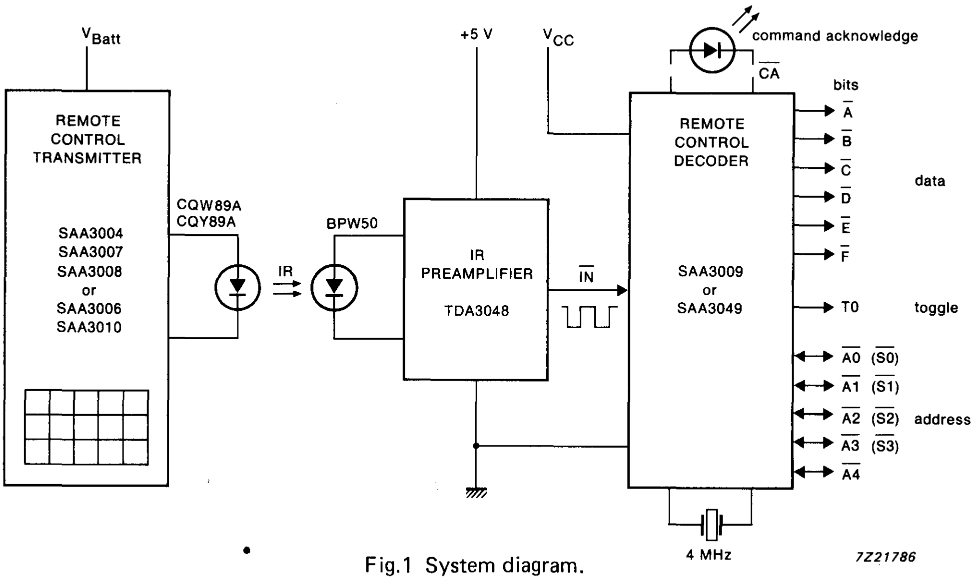


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004	V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)
SAA3007	V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)
SAA3008	V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)
SAA3006	V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)
SAA3010	V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	$V_{CC}+0.8$	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	−	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	−	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	−	10	mA
Total power dissipation				
SAA3009	P_{tot}	−	1	W
SAA3049	P_{tot}	−	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+ 70	°C
SAA3049	T_{amb}	−40	+ 85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+ 150	°C
SAA3049	T_{stg}	−65	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = –40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	–0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	–0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	I_{OH} = −50 μA	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	I_{OL} = 5 mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	V_{CC} = 5 V ± 10%; V_{OL} = 0.4 V	I_{OL}	1.6	3.0	–	mA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 ot SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

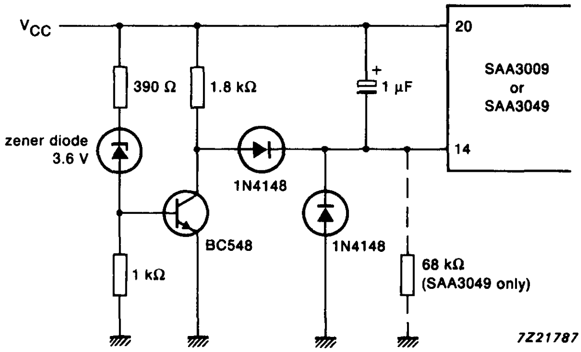


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

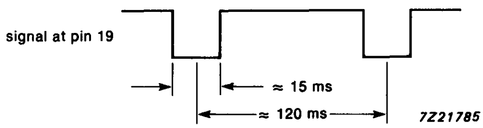
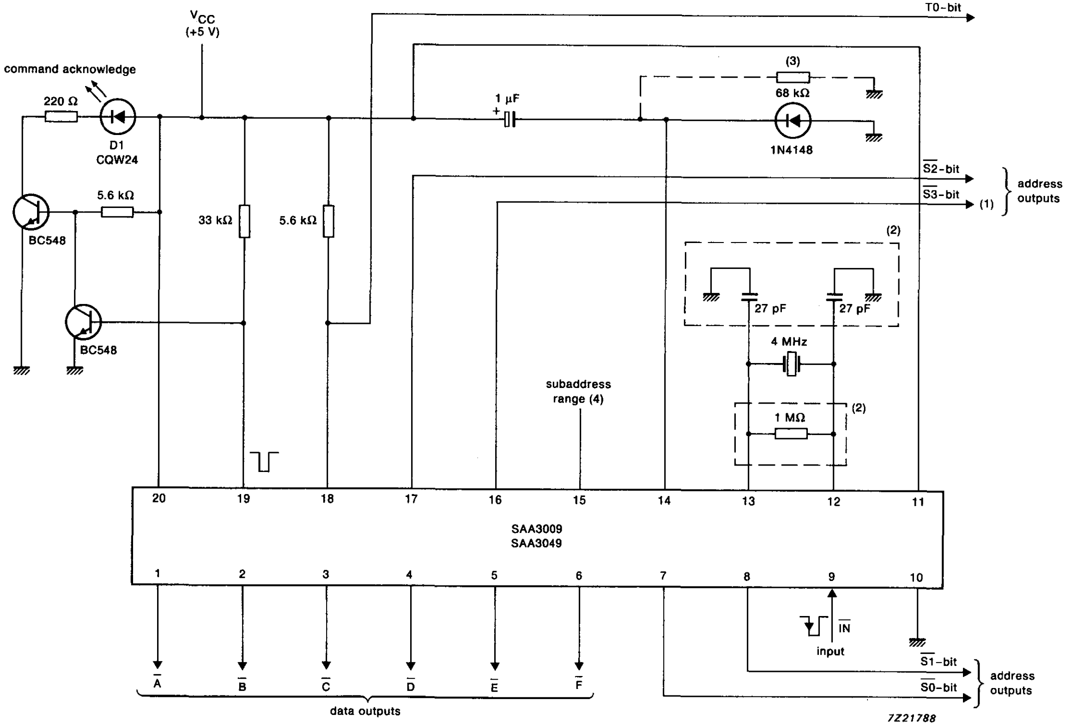


Fig.3 Output diagram of command acknowledge.

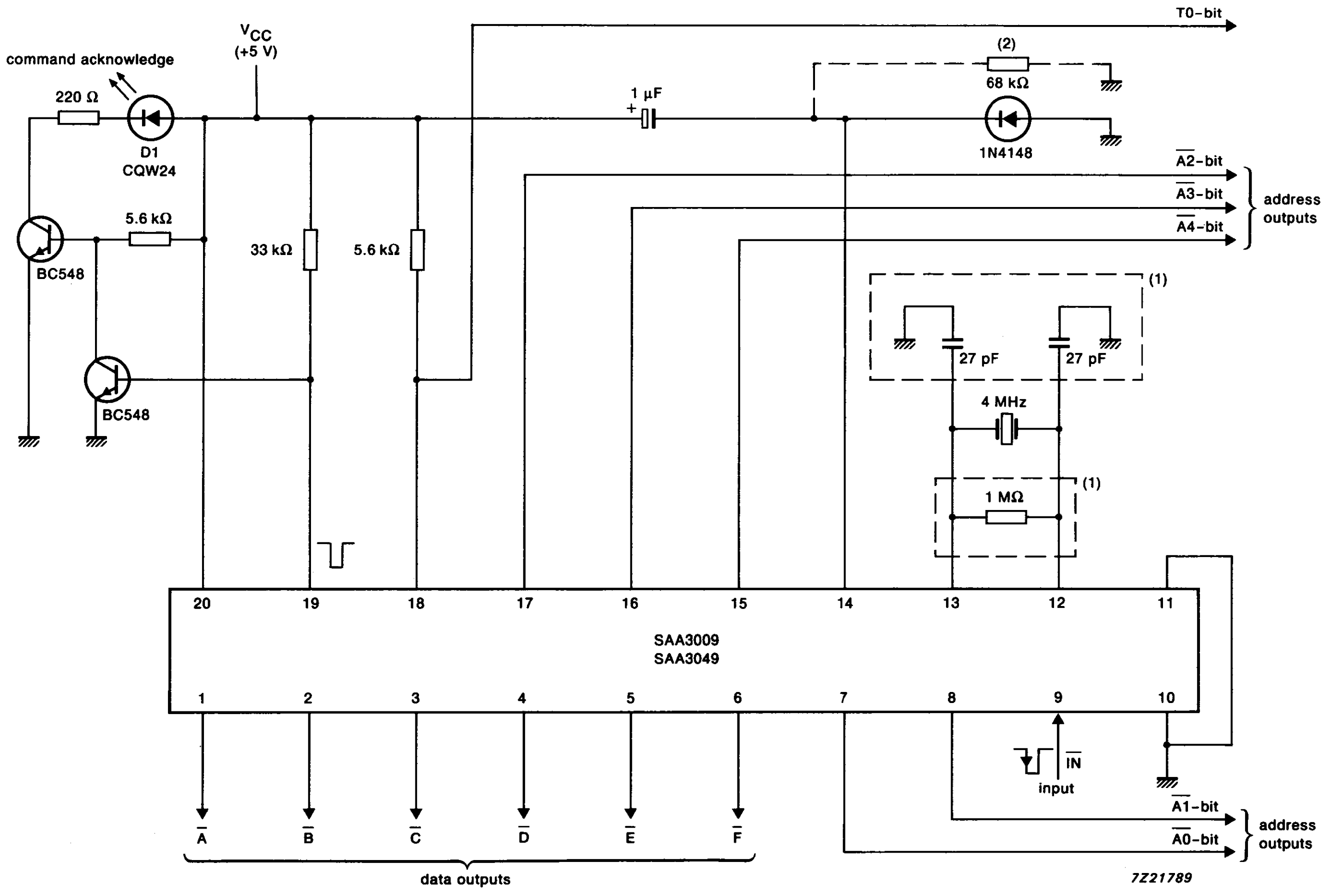
APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
   when LOW (subaddress 8 to 20) pin 15 is connected to ground
   when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
   when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

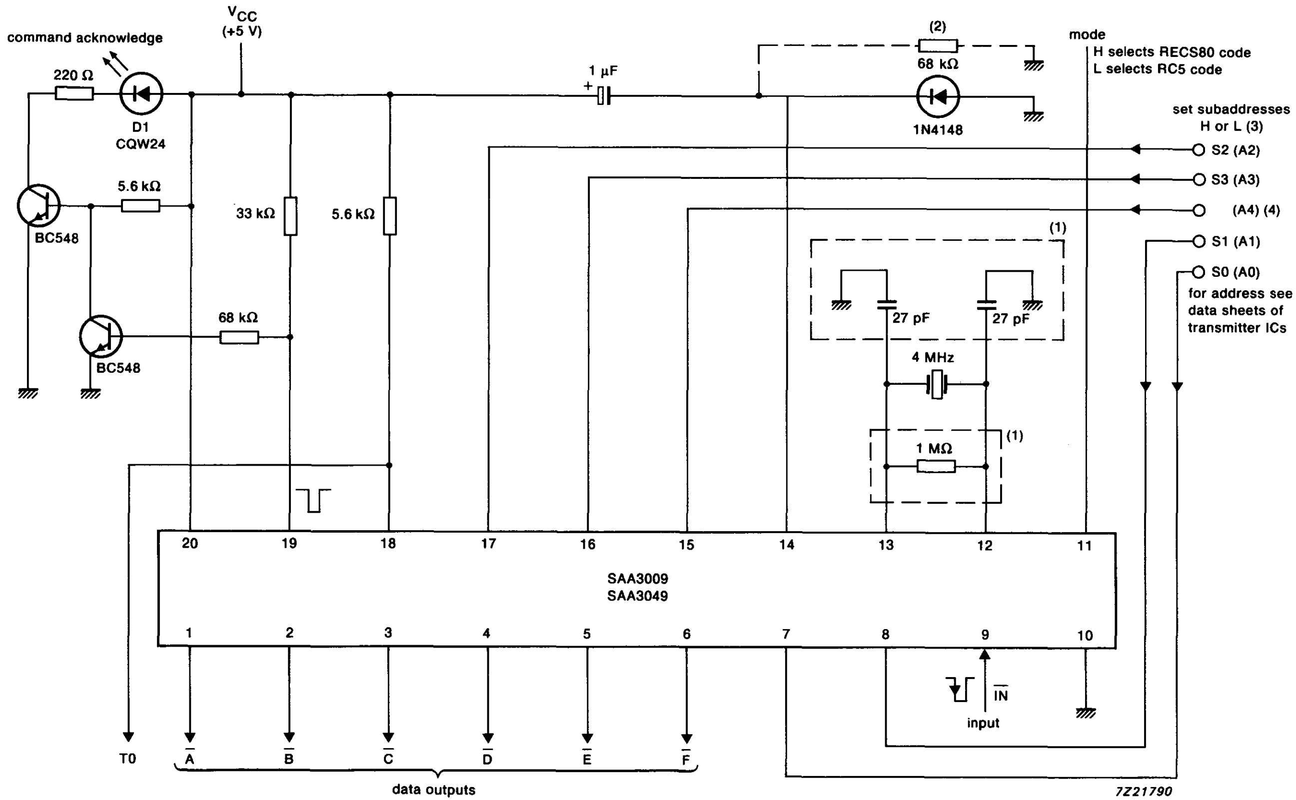
Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

APPLICATION INFORMATION (continued)



(1) only for SAA3009.
(2) only for SAA3049.

Fig.5 Remote control decoder with latched 12-bit parallel outputs (11 bits inverted) for use with transmitter types SAA3006 or SAA3010; pin 11 is LOW for RC5 code.



(1) only for SAA3009.
(2) only for SAA3049.
(3) address inputs:
when LOW address input pin is connected to ground
when HIGH address input pin is open (SAA3009)
when HIGH address input pin is connected via pull-up resistor to V_{CC} (SAA3049)
(4) subaddress range RECS80 code:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.6 Remote control decoder for up to 20 subaddresses with 6 + 1-bit parallel outputs (RECS80 code). Decoder is set for required subaddress by holding address pins HIGH or LOW. Pin 11 is HIGH for use with transmitter types SAA3004, SAA3007 or SAA3008 (RECS80 code). Pin 11 is LOW for use with transmitter types SAA3006 or SAA3010 (RC5 code). Remote control decoder for up to 32 subaddresses with 6 + 1-bit parallel outputs (RC5 code).

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	–0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	–0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	–25	–	85	^oC

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

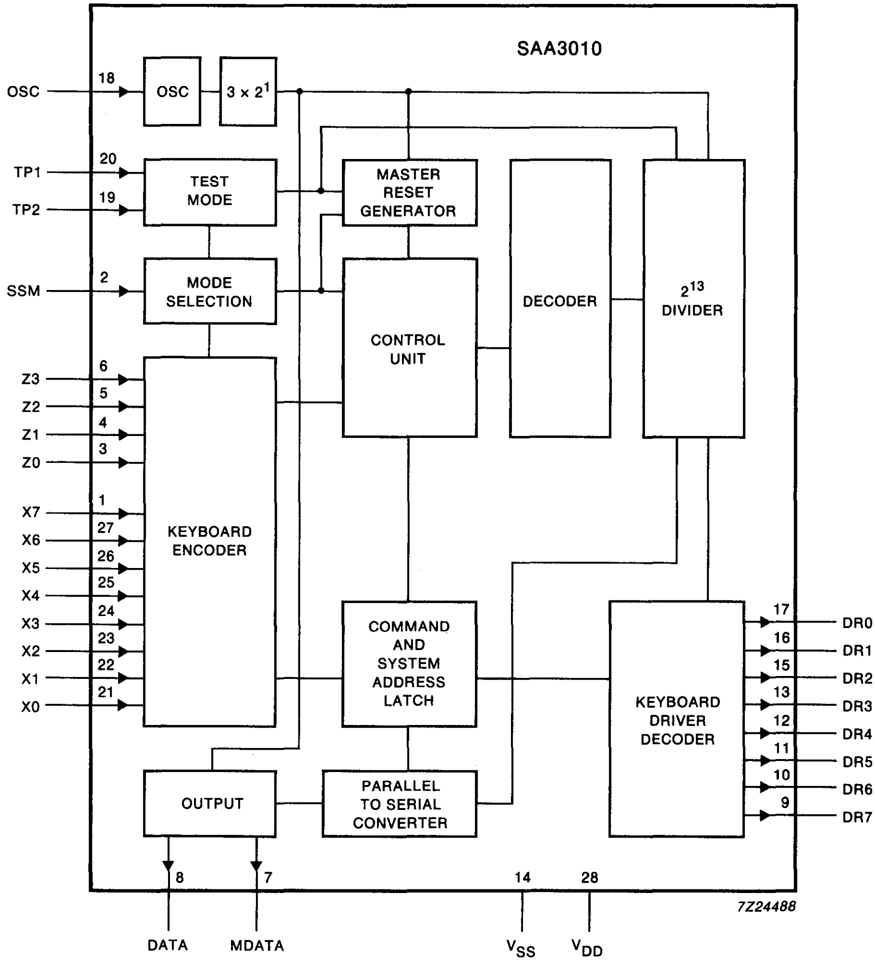


Fig.1 Block diagram.

PINNING

pin	mnemonic	function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	V_{SS}	ground (0 V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	V_{DD} (I)	voltage supply

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

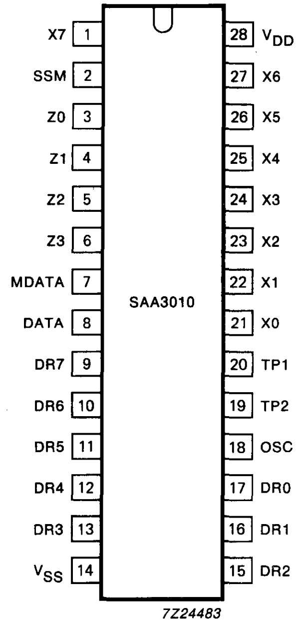


Fig.2 Pinning diagram.

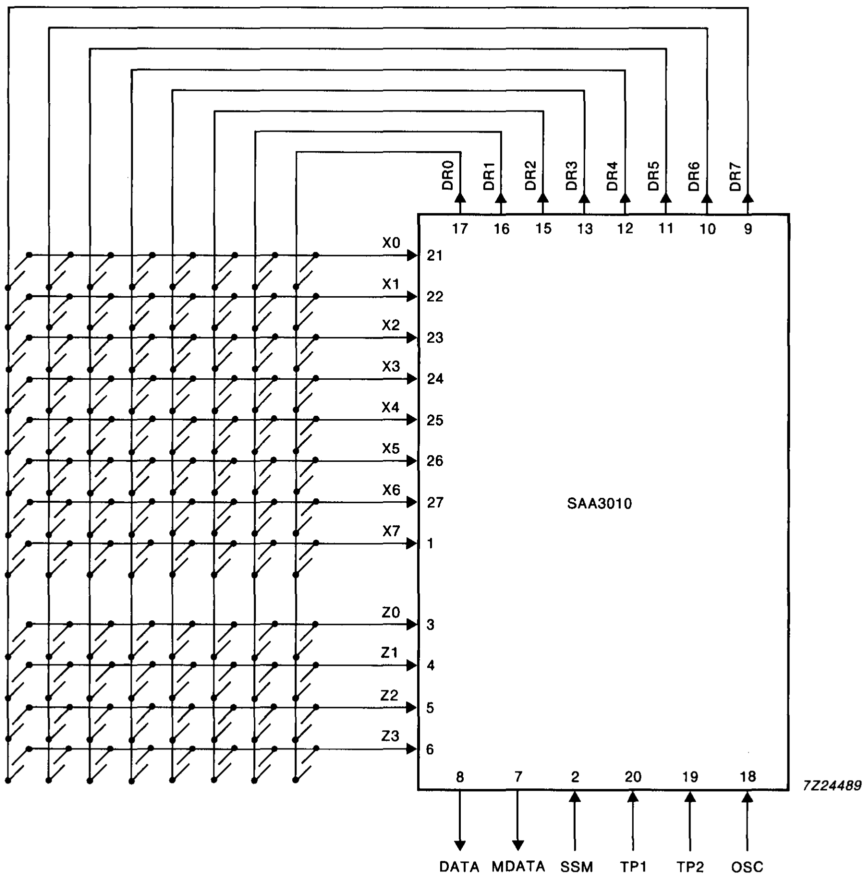


Fig.3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).

When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.

The maximum value of the contact series resistance of the switched keyboard is 7 kΩ.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.4 and Tables 1 and 2. The code is transmitted using a biphase technique as illustrated by Fig.5. The code consists of four parts:

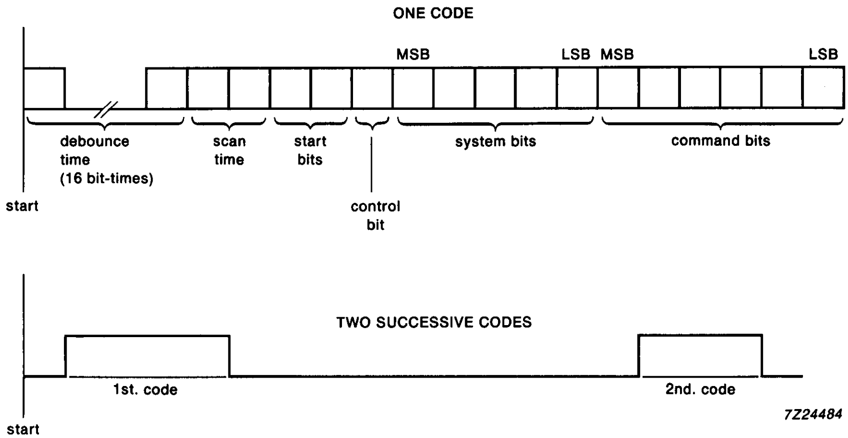
- Start part – 1.5 bits (2 x logic 1)
- Control part – 1 bit
- System part – 5 bits
- Command part – 6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50% duty factor.

In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).

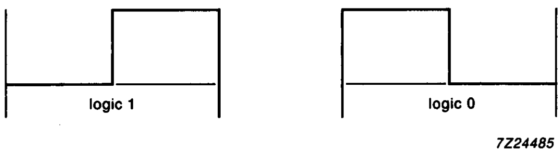
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

FUNCTIONAL DESCRIPTION (continued)



Where: debounce time + scan time = 18 bit-times
repetition time = 4 x 16 bit-times

Fig.4 Data output format.



Where: 1 bit-time = $3.2^8 \times T_{OSC}$ = 1.778 ms (typ.)

Fig.5 Biphase transmission technique.

Table 1 Command matrix (X-DR)

code no.	X-lines 0	1	2	3	4	5	6	7	DR-lines 0	1	2	3	4	5	6	7	command bits 5 4 3 2 1 0
0	●								●								0 0 0 0 0 0
1	●									●							0 0 0 0 0 1
2	●										●						0 0 0 0 1 0
3	●											●					0 0 0 0 1 1
4	●												●				0 0 0 1 0 0
5	●													●			0 0 0 1 0 1
6	●														●		0 0 0 1 1 0
7	●															●	0 0 0 1 1 1
8		●							●								0 0 1 0 0 0
9		●								●							0 0 1 0 0 1
10		●									●						0 0 1 0 1 0
11		●										●					0 0 1 0 1 1
12		●											●				0 0 1 1 0 0
13		●												●			0 0 1 1 0 1
14		●													●		0 0 1 1 1 0
15		●														●	0 0 1 1 1 1
16			●						●								0 1 0 0 0 0
17			●							●							0 1 0 0 0 1
18			●								●						0 1 0 0 1 0
19			●									●					0 1 0 0 1 1
20			●										●				0 1 0 1 0 0
21			●											●			0 1 0 1 0 1
22			●												●		0 1 0 1 1 0
23			●													●	0 1 0 1 1 1
24				●					●								0 1 1 0 0 0
25				●						●							0 1 1 0 0 1
26				●							●						0 1 1 0 1 0
27				●								●					0 1 1 0 1 1
28				●									●				0 1 1 1 0 0
29				●										●			0 1 1 1 0 1
30				●											●		0 1 1 1 1 0
31				●												●	0 1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Table 1 Command matrix (X-DR) (continued)

code no.	X-lines								DR-lines								command bits					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					•				•								1	0	0	0	0	0
33					•					•							1	0	0	0	0	1
34					•						•						1	0	0	0	1	0
35					•							•					1	0	0	0	1	1
36					•								•				1	0	0	1	0	0
37					•									•			1	0	0	1	0	1
38					•										•		1	0	0	1	1	0
39					•											•	1	0	0	1	1	1
40						•			•								1	0	1	0	0	0
41						•				•							1	0	1	0	0	1
42						•					•						1	0	1	0	1	0
43						•						•					1	0	1	0	1	1
44						•							•				1	0	1	1	0	0
45						•								•			1	0	1	1	0	1
46						•									•		1	0	1	1	1	0
47						•										•	1	0	1	1	1	1
48							•		•								1	1	0	0	0	0
49							•			•							1	1	0	0	0	1
50							•				•						1	1	0	0	1	0
51							•					•					1	1	0	0	1	1
52							•						•				1	1	0	1	0	0
53							•							•			1	1	0	1	0	1
54							•								•		1	1	0	1	1	0
55							•									•	1	1	0	1	1	1
56								•	•								1	1	1	0	0	0
57								•		•							1	1	1	0	0	1
58								•			•						1	1	1	0	1	0
59								•				•					1	1	1	0	1	1
60								•					•				1	1	1	1	0	0
61								•						•			1	1	1	1	0	1
62								•							•		1	1	1	1	1	0
63								•								•	1	1	1	1	1	1

Table 2 System matrix (Z-DR)

syst.	Z-lines								DR-lines								system bits
no.	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	4 3 2 1 0
0	●								●								0 0 0 0 0
1	●									●							0 0 0 0 1
2	●										●						0 0 0 1 0
3	●											●					0 0 0 1 1
4	●												●				0 0 1 0 0
5	●													●			0 0 1 0 1
6	●														●		0 0 1 1 0
7	●															●	0 0 1 1 1
8		●							●								0 1 0 0 0
9		●								●							0 1 0 0 1
10		●									●						0 1 0 1 0
11		●										●					0 1 0 1 1
12		●											●				0 1 1 0 0
13		●												●			0 1 1 0 1
14		●													●		0 1 1 1 0
15		●														●	0 1 1 1 1
16			●						●								1 0 0 0 0
17			●							●							1 0 0 0 1
18			●								●						1 0 0 1 0
19			●									●					1 0 0 1 1
20			●										●				1 0 1 0 0
21			●											●			1 0 1 0 1
22			●												●		1 0 1 1 0
23			●													●	1 0 1 1 1
24				●					●								1 1 0 0 0
25				●						●							1 1 0 0 1
26				●							●						1 1 0 1 0
27				●								●					1 1 0 1 1
28				●									●				1 1 1 0 0
29				●										●			1 1 1 0 1
30				●											●		1 1 1 1 0
31				●												●	1 1 1 1 1

FUNCTIONAL DESCRIPTION (continued)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with "take over" of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

- debounce time
- between two codes.

When a key is released during matrix scanning, a reset will occur if:

- a key is released while one of the driver outputs is in the low ohmic state (logic 0)
- a key is released before that key has been detected
- there is no wired connection in the Z-DR matrix when SSM is HIGH.

Oscillator

The OSC is the input/output for a 1-pin oscillator. The oscillator is formed by a ceramic resonator, TOKO CRK429,order code, 2422 540 98069 or equivalent. A resistor of 6.8 kΩ must be placed in series with the resonator. The resistor and resonator are grounded at one side.

Test

Initialization of the circuit is performed when TP1, TP2 and OSC are HIGH. All internal nodes are defined except for the LATCH. The latch is defined when a scan cycle is started by pulling down an X- or Z-input while the oscillator is running.

If the debounce cycle has been completed, the scan cycle can be completed 3×2^3 faster, by setting TP1 HIGH.

If the scan cycle has been completed, the contents of the latch can be read 3×2^7 faster by setting TP2 HIGH.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	8.5	V
Input voltage range *	V_I	−0.5	V_{DD}+0.5	V
Output voltage range *	V_O	−0.5	V_{DD}+0.5	V
Input current	I_I	−	±10	mA
Output current	I_O	−	±10	mA
Maximum power dissipation				
OSC output	P_O	−	50	mW
other outputs	P_O	−	100	mW
Total power dissipation	P_{tot}	−	200	mW
Operating ambient temperature range	T_{amb}	−25	+ 85	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

* V_{DD}+0.5 V must not exceed 9.0 V.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

T_{amb} = −25 °C to + 70 °C; V_{DD} = 2.0 to 7.0 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.0	–	7.0	V
Quiescent supply current	note 1 T_{amb} = 25 °C; I_O = 0 mA at all outputs. X0 to X7 and Z0 to Z3 at V_{DD} TP1, TP2, OSC at V_{SS} SSM at V_{SS} or V_{DD}	I_{DD}	–	–	10	μA
INPUTS						
Keyboard inputs X and Z with p-channel pull-up transistor						
Input current at each input	V_I = 0 V; TP1 = TP2 = SSM = LOW	$-I_I$	10	–	600	μA
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	note 2	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7 V; TP1 = TP2 = HIGH	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	1	μA
OSC						
Input leakage current	T_{amb} = 25 °C; V_I = 0 V; TP1 = TP2 = HIGH	$-I_{LI}$	–	–	2	μA
Input current	T_{amb} = 25 °C; V_I = V_{DD}	I_{OSC}	4.5	–	30	μA
SSM, TP1, TP2						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current	T_{amb} = 25 °C; V_I = 7.0 V	I_{LI}	–	–	1	μA
Input leakage current	T_{amb} = 25 °C; V_I = 0 V	$-I_{LI}$	–	–	1	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
OUTPUTS						
DATA, MDATA						
Output voltage HIGH	$I_{OH} = -0.4$ mA	V_{OH}	V_{DD}-0.3	–	–	V
Output voltage LOW	$I_{OL} = 0.6$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA
	$V_O = 0$ V	$-I_{LO}$	–	–	20	μA
	$V_O = 0$ V; $T_{amb} = 25$ °C	$-I_{LO}$	–	–	2	μA
DR0 to DR7						
Output voltage LOW	$I_{OL} = 0.3$ mA	V_{OL}	–	–	0.3	V
Output leakage current	$V_O = 7.0$ V	$+I_{LO}$	–	–	10	μA
	$V_O = 7.0$ V; $T_{amb} = 25$ °C	$+I_{LO}$	–	–	1	μA

Notes to the DC characteristics

1. Quiescent supply current measurement must be preceded by the initialization procedure described in the **TEST** section.
2. This DC test condition protects the AC performance of the output. The DC current requirements in the actual application are lower.

AC CHARACTERISTICS

T_{amb} = −25 to + 85 °C; V_{DD} = 2.0 to 7.0 V unless otherwise stated

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency	C_L = 160 pF; Figs 6 and 7					
operational		f_{OSC}	−	−	450	kHz
free-running		f_{OSC}	10	−	120	kHz

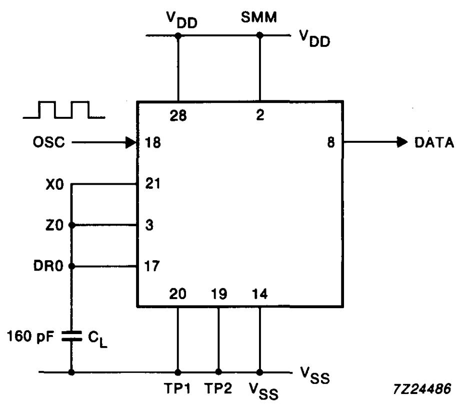


Fig.6 Test set-up for maximum f_{OSC} measurement.

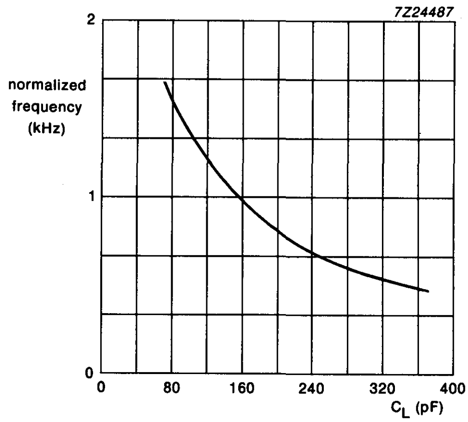


Fig.7 Typical normalized frequency as a function of keyboard load capacitance.

INFRARED REMOTE CONTROL TRANSCODER (RC-5)

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5	V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200	μA
Operating ambient temperature range	T_{amb}	−25 to	+85	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT 38Z).

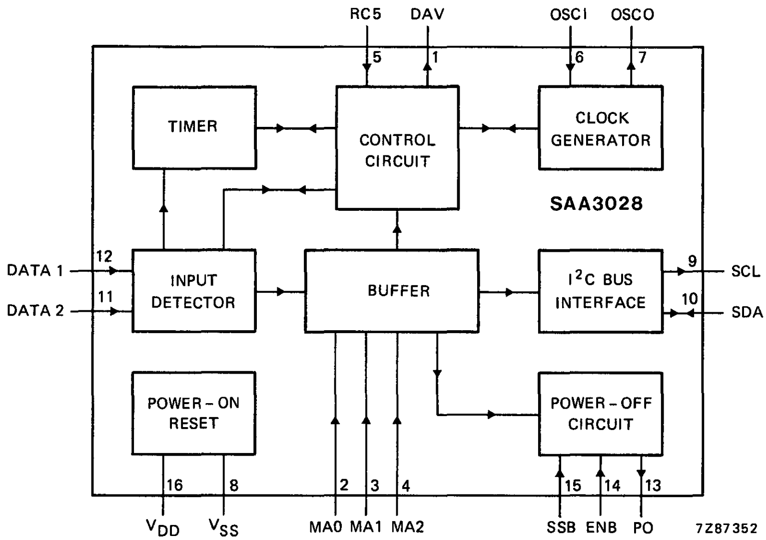


Fig. 1 Block diagram.

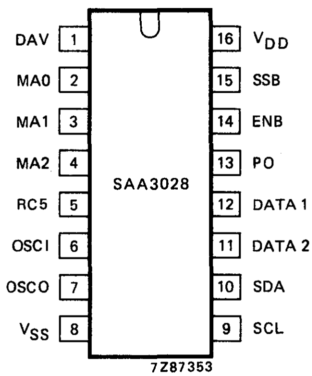


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor	
2	MA0	master address inputs	
3	MA1		
4	MA2		
5	RC5	data 2 input select	
6	OSCI	oscillator input	
7	OSCO	oscillator output	
8	V_{SS}	negative supply (ground)	
9	SCL	serial clock line	I^2C bus
10	SDA	serial data line	
11	DATA 2	data 2 input	
12	DATA 1	data 1 input	
13	PO	power-off signal output with open drain N-channel transistor	
14	ENB	enable input	
15	SSB	set standby input	
16	V_{DD}	positive supply (+5 V)	

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

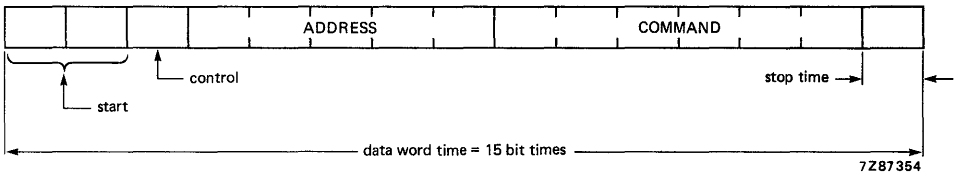


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

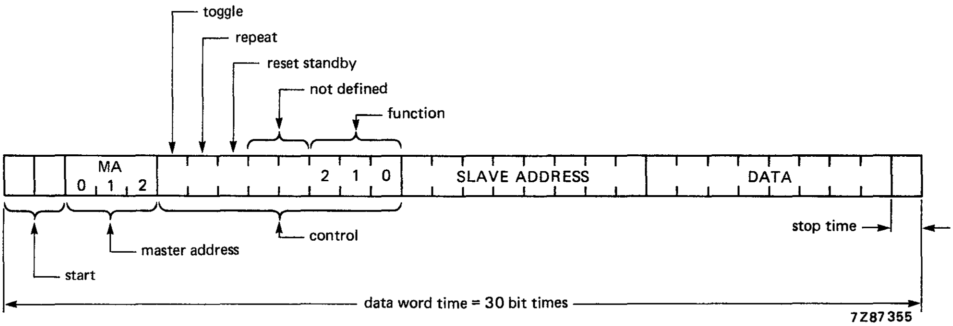


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

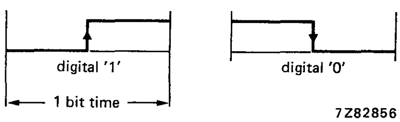


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH Enables the set standby input SSB.

SSB = LOW Causes power-off output PO to go HIGH.

PO = HIGH This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

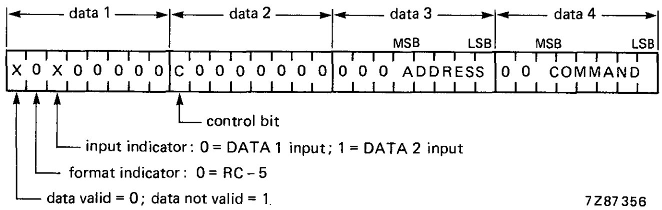


Fig. 6 RC-5 binary equivalent value format.

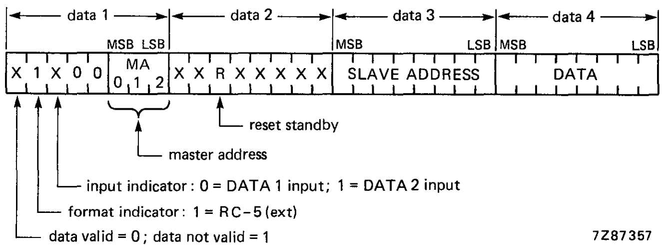


Fig. 7 RC-5(ext) binary equivalent value format.

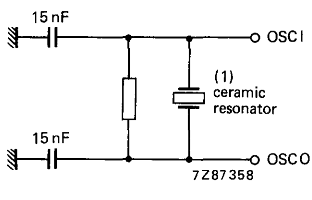
DEVELOPMENT DATA

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

FUNCTIONAL DESCRIPTION (continued)

I²C bus transmission

Formats for I²C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

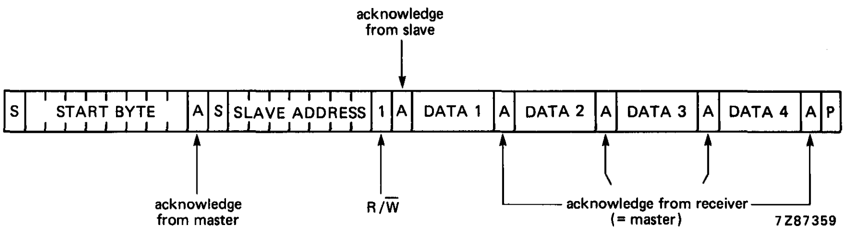


Fig. 9 Format for transmission in I²C low speed mode.

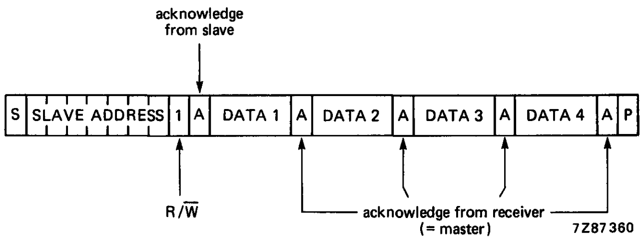


Fig. 10 Format for transmission in I²C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	–0,5 to	+15	V
Input voltage range	V_I	–0,5 to	$(V_{DD}+0,5)$	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	–0,5 to	$(V_{DD}+0,5)$	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	–25 to	+85	°C
Storage temperature range	T_{stg}	–55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	µA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	µA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	µA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	µA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} – 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C;						
V_O = 5,5 V	5,5	I_{OR}	–	–	1	µA
V_O = 0 V	5,5	I_{OR}	–	–	1	µA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	µA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

DECODER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7210 incorporates the functions of demodulator, subcoding processor, error corrector and concealment in one chip. The device accepts data from the disc and outputs serial data directly to a dual 16-bit digital-to-analogue converter TDA1541 (DAC) via the Inter IC signal bus (I^2S). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering. For descriptive purposes, the SAA7210 is referred to as the A-chip and the SAA7220 as the B-chip.

Features

- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Cross-Interleaved Reed-Solomon Code (CIRC) used for error correction system
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange between A-chip, B-chip and DAC
- Bidirectional data bus to external RAM (16 K x 4 bits)

QUICK REFERENCE DATA

Supply voltage (pin 40)	V_{DD}	typ.	5	V
Supply current (pin 40)	I_{DD}	typ.	200	mA
Data slicer input voltage range	$V_{I(p-p)}$		0,25 to 2,5	V
Oscillator operating frequency				
XTAL	f_{XTAL}	typ.	11,2896	MHz
VCO	f_{VCO}	typ.	8,6436	MHz
Maximum output current (each output)	I_O	max.	10	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

PACKAGE OUTLINE

40-lead DIL; plastic (SOT129).

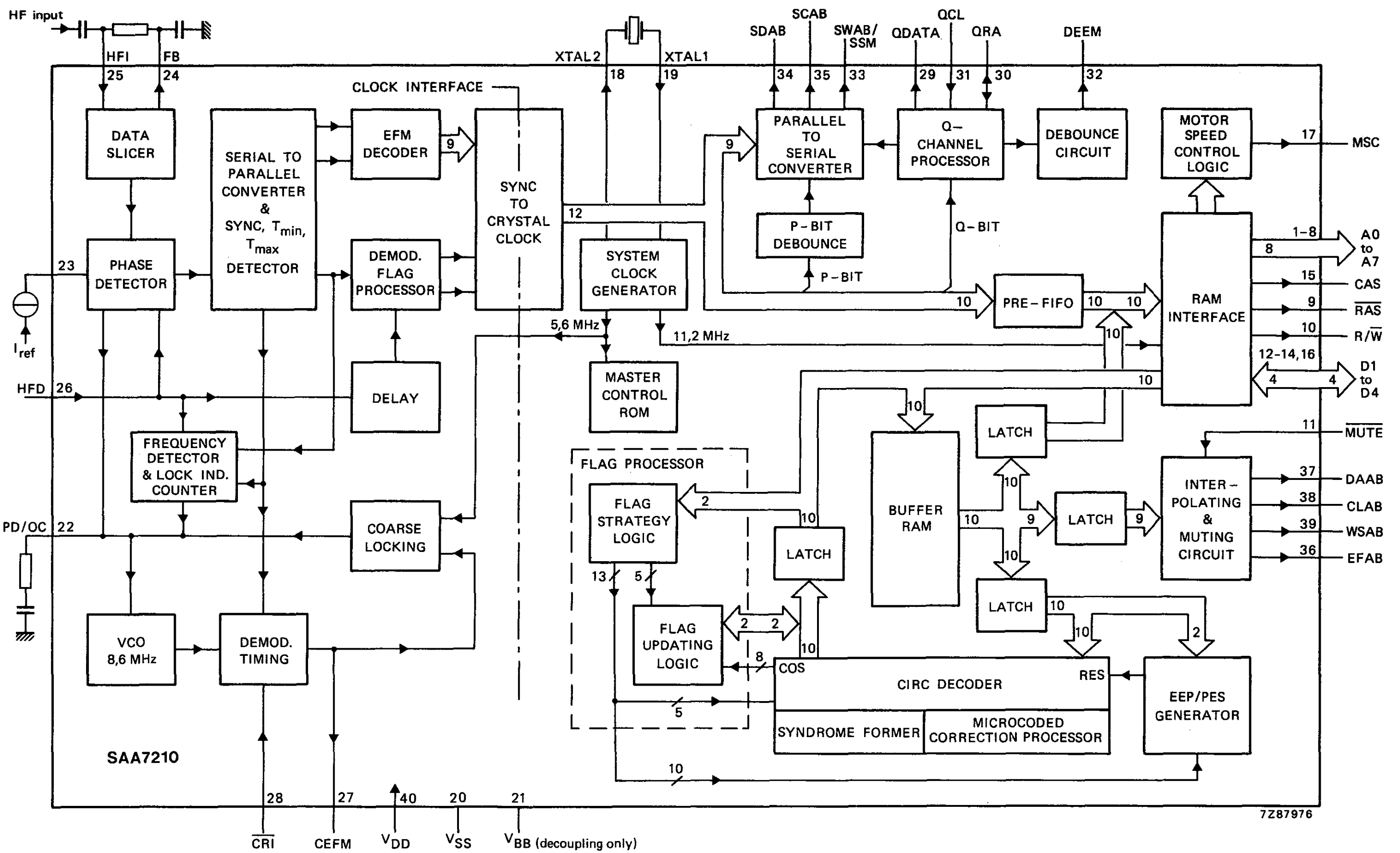


Fig. 1 Block diagram.

PINNING

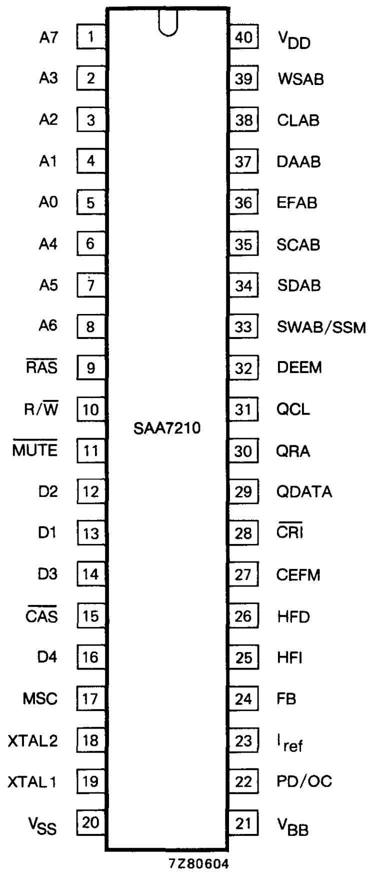


Fig. 2 Pinning diagram; for pin functions see next page.

DEVELOPMENT DATA

Pin functions

pin no.	mnemonic	description
1-8	A0-A7	**Address:** address outputs to external RAM.
9	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB (pin 37) is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first "good" value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12-14	D1-D3	**Data:** data inputs/outputs to external RAM.
15	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	D4	**Data:** data input/output to external RAM.
17	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continous 50% duty factor.
18	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	V_{SS}	**Ground:** circuit earth potential.
21	V_{BB}	**Back Bias supply voltage:** back bias output voltage (−2,5 V ±20%). The internal back bias generator can be decoupled at this pin.
22	PD/OC	**Phase Detector output/Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	I_{ref}	**Current reference:** external reference input to the phase detector. This input is required to minimize the spread in the charge pump output of the phase detector. An internal clamp prevents the voltage on this pin rising above 3,5 V.
24	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input at pin 25 (HFI) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD (pin 26) is LOW, this output goes to high impedance state.
25	HFI	**High-Frequency Input:** level detector input to the data slicer. A differential signal of between 0,25 and 2,5 V (peak-to-peak value) is required to drive the data slicer correctly. When a T_{max} violation is detected or when HFD is LOW, this input is biased directly to its threshold voltage.
26	HFD	**High-Frequency Detector:** when HIGH this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer. An internal voltage clamp of 3 V (typ.) requires the HFD input to be fed via a high impedance. This input has an internal pull-up of 50 kΩ (typ.).

pin no.	mnemonic	description
27	CEFM	**Clock Eight-to-Fourteen Modulation**: demodulator clock output 4,3218 MHz (typ.).
28	$\overline{CRI}$	**Counter Reset Inhibit:** when LOW this input signal allows the divide-by-588 master counter in the DEMOD timing to run-free. This input has an internal pull-up of 50 kΩ (typ.).
29	QDATA	**Q-channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol).
30	QRA	**Q-channel Request input/Acknowledge output:** the output has an internal pull-up of nominally 10 kΩ. (see subcoding microprocessor handshaking protocol).
31	QCL	**Q-channel Clock**: clock input generated by the micro-processor when it detects a QRA LOW signal.
32	DEEM	**De-emphasis:**signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit.
33	SWAB/SSM	**Subcoding Word clock output & Start/Stop Motor input:** open drain output which is sensed during each HIGH period and if externally forced LOW a motor-stop condition will be decoded and fed to the motor control logic circuit.
34	SDAB	**Subcoding Data**: a 10-bit burst of data, including flags and sync bits, is output serially to the B-chip once per frame clocked by burst clock output SCAB (see Fig. 4).
35	SCAB	**Subcoding Clock**: a 10-bit burst clock 2,8224 MHz (typ.) output which is used to synchronize the subcoding data.
36	EFAB	**Error Flag:** output from interpolation and mute circuit to B-chip indicating unreliable data.
37	DAAB	**Data**: this output which is fed to the B-chip or DAC, together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Fig. 5).
38	CLAB	**Clock**: output to B-chip or DAC.
39	WSAB	**Word Select:** output to B-chip or DAC.
40	V_{DD}	**Power Supply**: positive supply voltage(+ 5 V).

Note to the pin functions

The pin sequence of the address outputs (A0-A7) and the data outputs (D1-D4) has been selected to be compatible with various dynamic 16 K x 4-bit RAMs including the 4416.

FUNCTIONAL DESCRIPTION

Demodulation

Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at twice the input data rate (typically at 8,6436 MHz), its frequency being dependent on the voltage at pin 22 (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output is divided by two to provide the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (PD/OC), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source connected to pin 23 (I_{ref}).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input (pin 28) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.

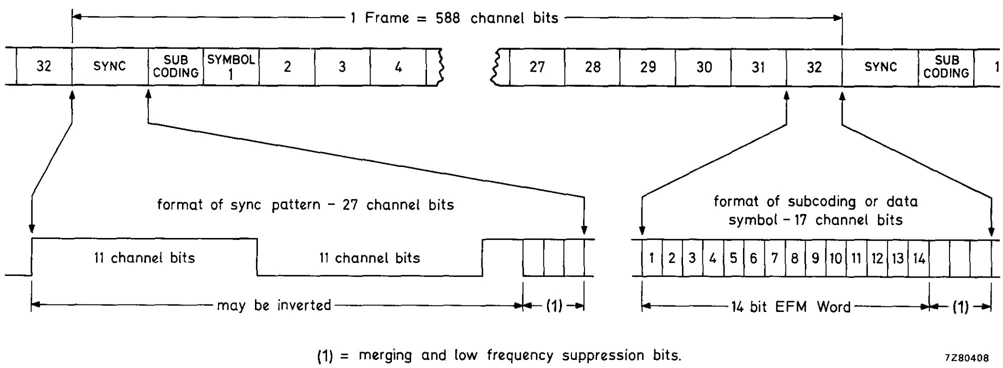


Fig. 3 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output to B-chip

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output (pin 32) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34. The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output to the B-chip consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally on the rising edge of SWAB at pin 33 (see Fig. 4).

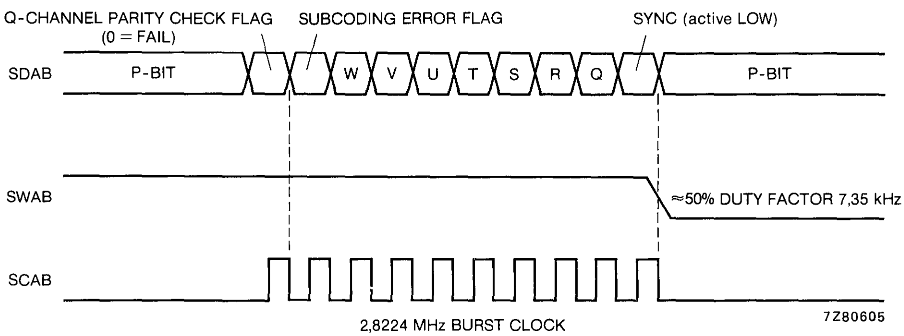


Fig. 4 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4 symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency (e.g. pitch control).

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 6) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address ($\overline{\text{RAS}}$ pin 9) is set up first and then three 4-bit nibbles are accessed using sequential column addresses ($\overline{\text{CAS}}$ pin 15). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good' data (flags = 00) and three levels of error can be indicated.
The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

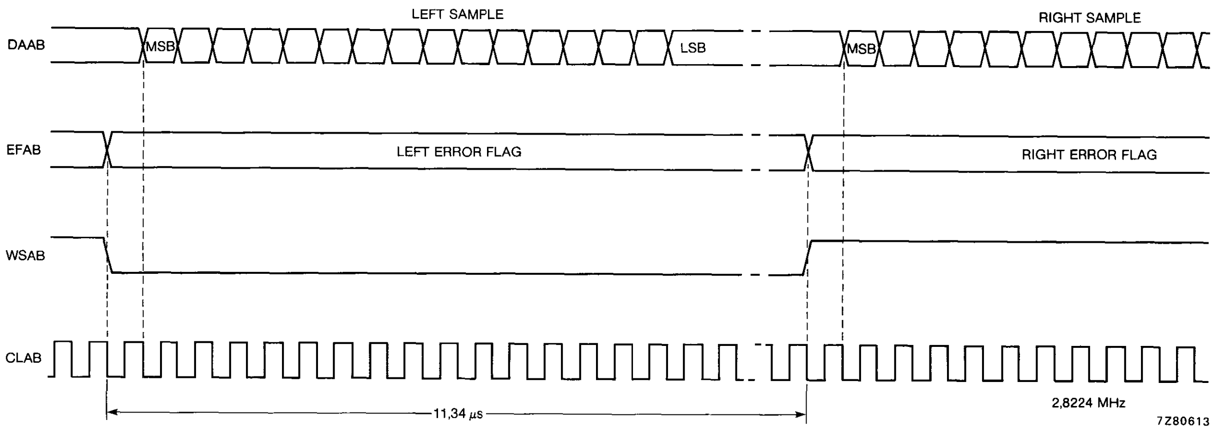


Fig. 5 Typical waveform outputs to B-chip or DAC.

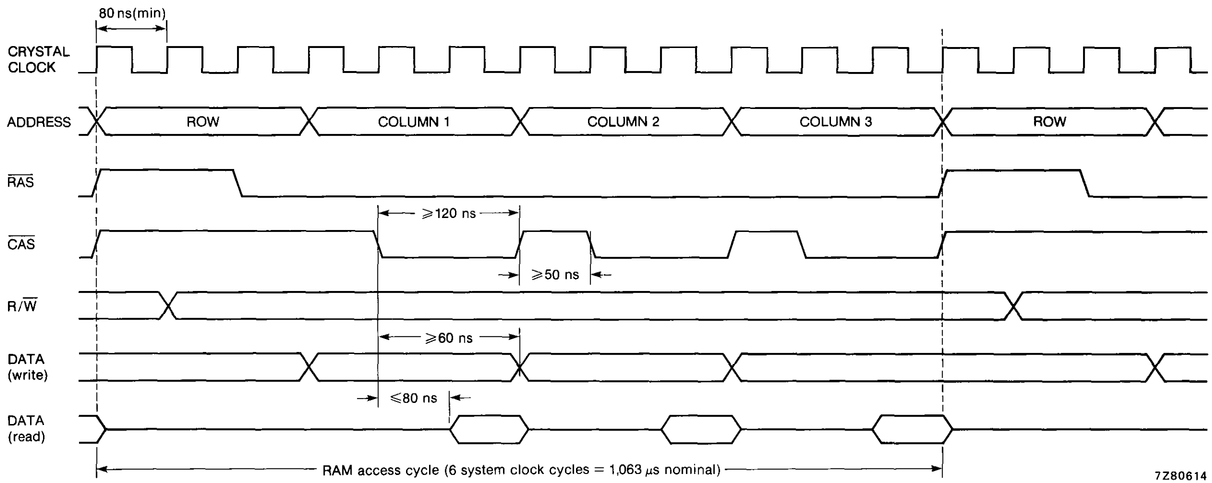


Fig. 6 RAM timing waveforms: timings based on RAM TMS4416; $\overline{G}$ input to RAM held LOW.

FUNCTIONAL DESCRIPTION (continued)

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the B-chip where it receives additional and more efficient concealment.

Motor speed control (see Fig. 7)

The motor speed control (MSC) output from pin 17 is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

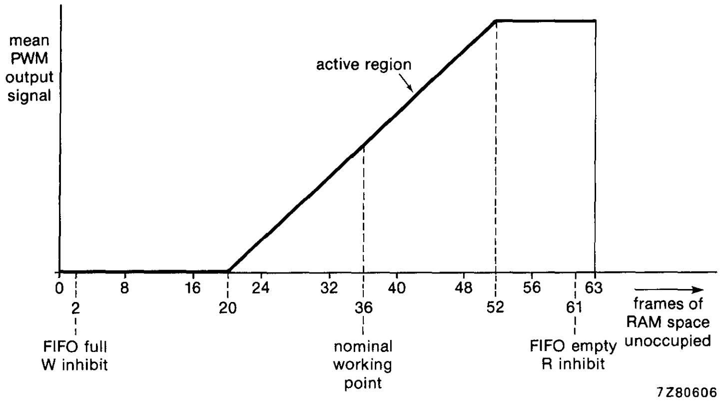


Fig. 7 Motor speed control.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}		−0,5 to +7,0	V
Maximum input voltage range	V_I		−0,5 to V_{DD} +0,5	V
Input current (pin 23)	I_I	max.	5	mA
Maximum output voltage range (pin 17, 33)	V_O		−0,5 to +7,0	V
Output current (each output)	I_O	max.	10	mA
Storage temperature range	T_{stg}		−55 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C
Electrostatic handling *	V_{es}		−1000 to +1000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = –2- to +70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 40)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 40)	I_{DD}	–	200	tbf	mA
Inputs					
D1-D4, QCL					
Input voltage LOW	V_{IL}	–0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
$\overline{\text{MUTE}}$, $\overline{\text{CRI}}$					
Input voltage LOW	V_{IL}	–0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance at V_I = 0 V	$\|Z_I\|$	tbf	50	tbf	kΩ
Input capacitance	C_I	–	–	7	pF
QRA, SWAB					
Input voltage LOW	V_{IL}	–0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance	C_I	–	–	7	pF
Internal pull-up impedance at V_I = 0 V	$\|Z_I\|$	5	10	–	kΩ
HFD					
Input voltage LOW	V_{IL}	–0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	clamped	V
Input clamping voltage at I_I = 100 μA	V_{CL}	–	3	–	V
Input source current	$\pm I_S$	–	–	100	μA
Input capacitance	C_I	–	–	7	pF
Internal pull-up impedance at V_I = 0 V	$\|Z_I\|$	–	50	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Outputs					
A1-A8, R/$\overline{W}$, D1-D4, $\overline{CAS}$, $\overline{RAS}$, CEFM, QDATA, DEEM, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
MSC (open drain)					
Output voltage LOW at $-I_{OL}$ = 1 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	50	pF
SWAB, QRA (open drain)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
Internal load resistance	R_L	5	–	–	kΩ
ANALOGUE CIRCUITS					
Data slicer					
Input HFI					
A.C. input voltage range (peak-to-peak value)	$V_{I(p-p)}$	0,25	–	2,5	V
Input impedance					
normal (HFD HIGH)	$\|Z_I\|$	tbf	–	tbf	kΩ
disabled (HFD LOW)	$\|Z_I\|$	tbf	–	tbf	kΩ
Input capacitance	C_I	–	–	7	pF
Output FB					
Output current at V_{FB} = 2 V	I_O	tbf	100	tbf	μA
Phase detector					
Output PD/OC					
Output impedance	$\|Z_O\|$	–	tbf	–	kΩ
Control range (note 1)	α	±2,1	–	–	rad
Gain factor	G	–	tbf	–	mA/rad
Input I_{ref}					
Input reference current	I_{ref}	–	500	tbf	μA

CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Fine frequency detector					
Output PD/OC					
Output impedance	$\|Z_O\|$	–	2	–	kΩ
Coarse frequency detector					
Output PD/OC (note 2)					
Output impedance	$\|Z_O\|$	–	1	–	kΩ
Voltage controlled oscillator					
Input PD/OC					
Oscillator constant	K_{osc}	–	tbf	–	MHz/V
Crystal oscillator					
Input XTAL1					
Output XTAL2					
Mutual conductance at 100 kHz	G_m	1,5	–	–	mS
Small signal voltage gain ($G_V = G_m \times R_O$)	G_V	3,5	–	–	V/V
Input capacitance	C_I	–	–	10	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Output capacitance	C_O	–	–	10	pF
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Slave clock mode					
Input voltage (peak-to-peak value)	$V_{I(p\text{-}p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW	V_{IL}	–0,3	–	0,8	V
Input voltage HIGH	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 3)	t_r	–	–	20	ns
Input fall time (note 3)	t_f	–	–	20	ns
Input HIGH time at 1,2 V (relative to clock period)	t_{HIGH}	35	–	65	%

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)					
coarse frequency detector inactive	f_{VCO1}	$f_{XTAL}/2$	8,6436	f_{XTAL}	MHz
no input pin 25 (HFI)	f_{VCO2}	4	–	15	MHz
Outputs (see Figs. 8 and 9)					
CEFM (note 4)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Output HIGH time	t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (note 4) (data to B-chip; 1^2S format)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB					
Data set-up time	$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB					
Data hold time	$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (note 4) (subcoding outputs)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
SDAB to SCAB					
Subcoding data set-up time	$t_{SU;SDAT}$	100	–	–	ns
SCAB to SDAB					
Subcoding data hold time	$t_{HD;SDAT}$	100	–	–	ns
SWAB (note 4)					
Output rise time	t_r	–	–	1	μs
Output fall time	t_f	–	–	100	ns
Output duty factor		–	50	–	%

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Q-channel I/O (see Figs. 12 and 13)					
QRA, QCL, QDATA					
Access time (note 5)					
normal mode	$t_{ACC;\,N}$	0	–	13,3 + n x 13,3	ms
refresh mode	$t_{ACC;\,F}$	13,3	–	n x 13,3	ms
QCL to QRA acknowledge delay	t_{DACK}	–	–	500	ns
QCL to QRA request hold time	$t_{HD;\,R}$	500	–	–	ns
QCL clock input LOW time	$t_{CK;\,LOW}$	500	–	–	ns
QCL clock input HIGH time	$t_{CK;\,HIGH}$	500	–	–	ns
QCL to QDATA delay time	t_{DD}	–	–	500	ns
Data hold time before new frame is accessed	$t_{HD;\,ACC}$	2,3	–	–	ms
Acknowledge time	t_{ACK}	–	–	10,8	ms

Notes to the characteristics

1. 1 rad = $\frac{180^{o}}{(3,14)}$.
2. Coarse frequency detector output PD/OC active for VCO frequencies $> f_{XTAL}$ and $< \frac{f_{XTAL}}{2}$.
3. Reference levels = 1 V and 2,4 V.
4. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
5. Q-channel access times dependent on cyclic redundancy check (CRC).

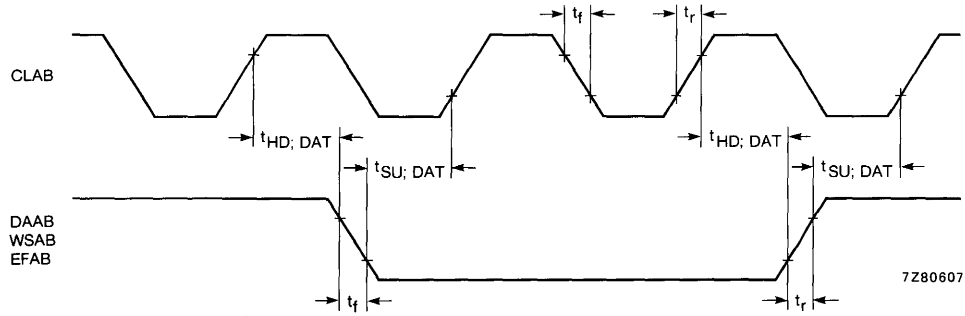


Fig. 8 Typical data output waveforms to B-chip or DAC: reference levels = 0,8 V and 2,0 V.

DEVELOPMENT DATA

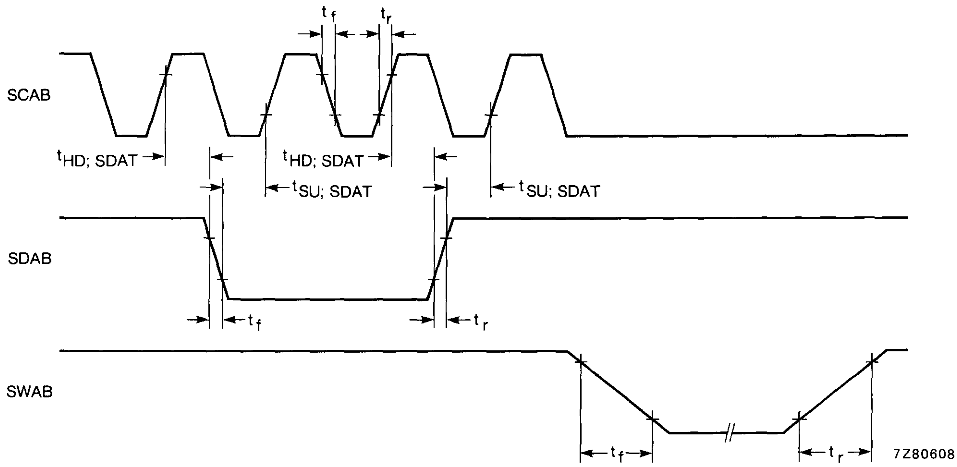


Fig. 9 Typical subcoding data output waveforms: reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a d.c. free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the d.c. content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 10).

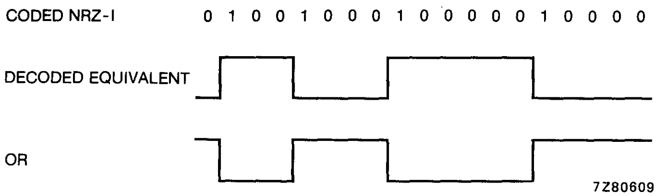


Fig. 10 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

Table 2 EFM code conversion

No.	DNZ data symbol	equivalent code word	No.	DNZ data symbol	equivalent code word
	D1 D8	C1 C14		D1 D8	C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11 to 119			139 to 247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

APPLICATION INFORMATION (continued)

Subcoding microprocessor handshaking protocol (see Figs. 11, 12 and 13)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7210.

The SAA7210 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7210 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7210 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowledge signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7210 now disables the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7210 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7210 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

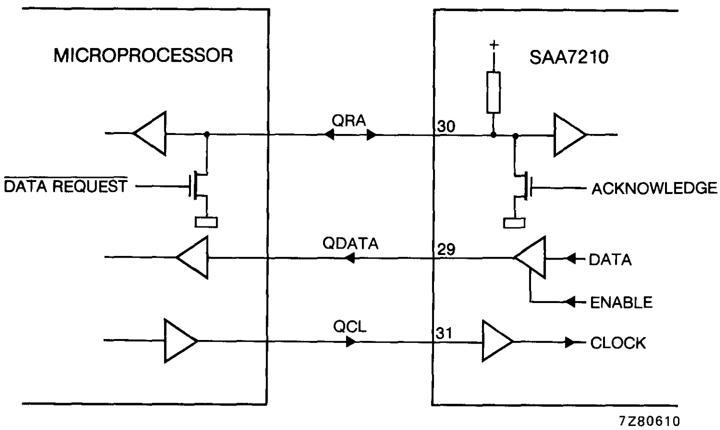


Fig. 11 Microprocessor handshaking protocol.

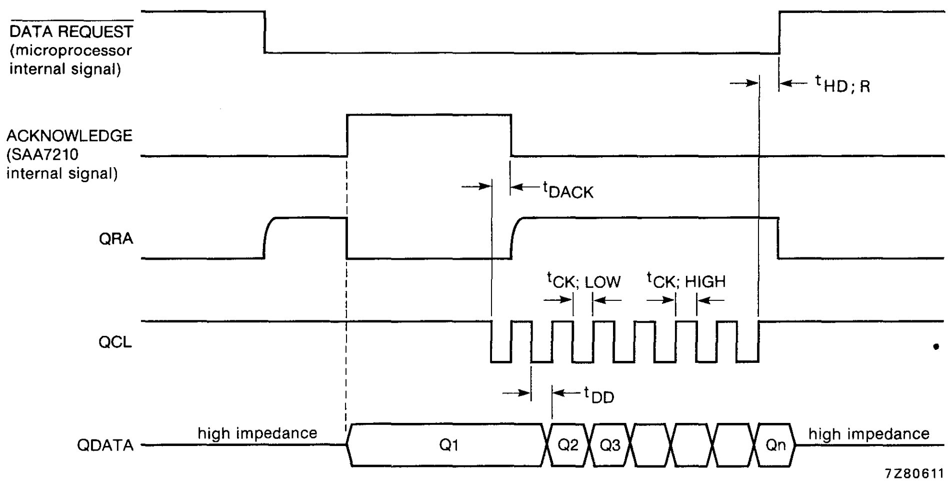


Fig. 12 Q-channel timing waveforms (normal mode).

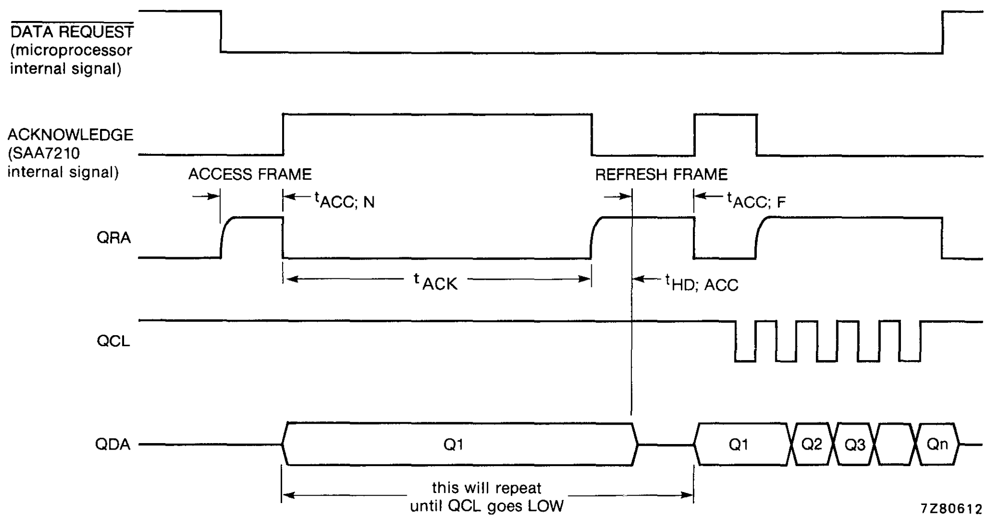


Fig. 13 Q-channel timing waveforms (refresh mode).

DIGITAL FILTER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7220 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. For descriptive purposes, the SAA7220 is referred to as the B-chip and the SAA7210 as the A-chip.

Features

- 16-bit serial data input (two's complement)
- Interpolated data replaces erroneous data samples
- −12 dB attenuation via the active LOW attenuation input control (ATSB)
- Smoothed transitions before and after muting
- Two identical finite impulse response transversal filters each with a sampling rate of four times that of the normal digital audio data
- Digital audio output of 32-bit words transmitted in biphase-mark code
- I²S data transfer between SAA7210, SAA7220 and 16-bit dual DAC (TDA1541)

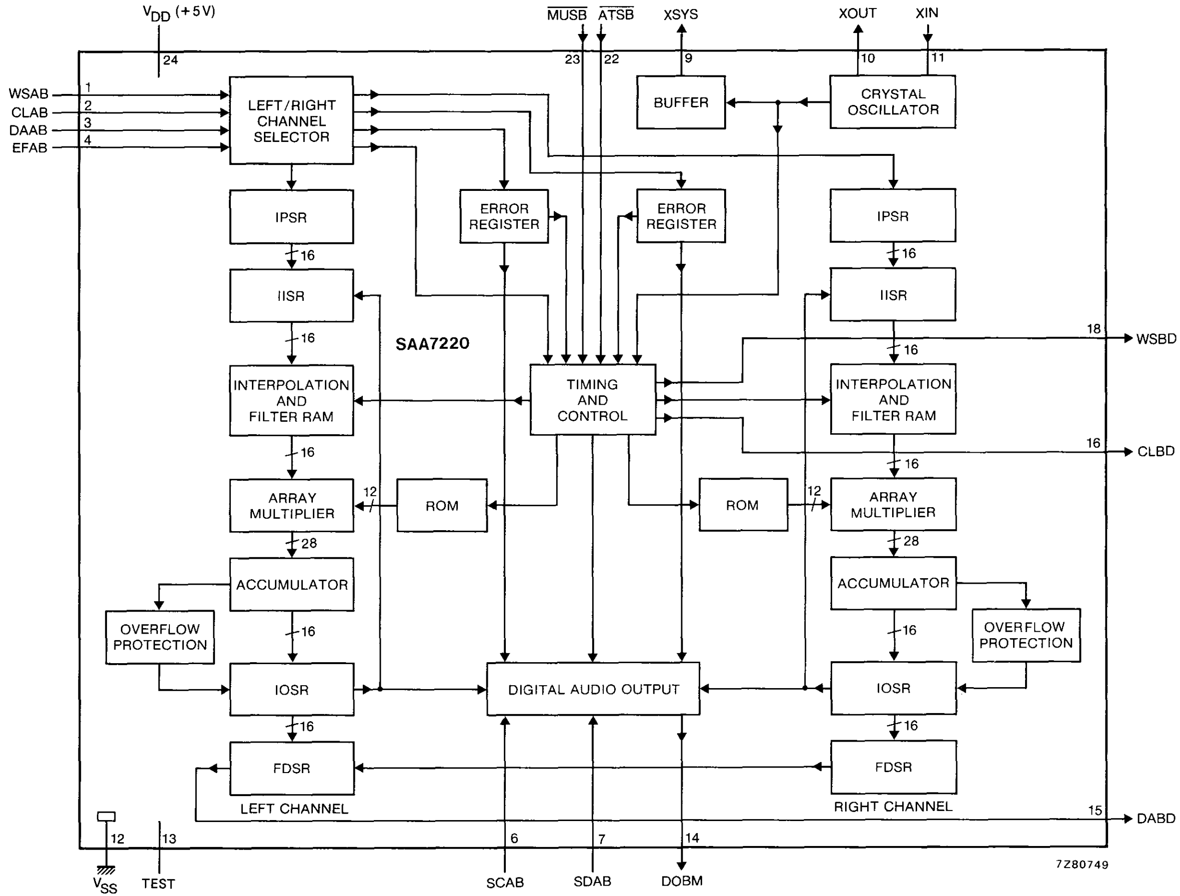
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 24)		V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)		I_{DD}	100	180	285	mA
Input voltage ranges						
WSAB, DAAB, EFAB, SDAB	note 2					
CLAB, SCAB, $\overline{\text{ATSB}}$, $\overline{\text{MUSB}}$	note 3					
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Output voltage ranges						
DABD, CLBD, WSBD						
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
DOBM						
Voltage across a 75 Ω load via attenuator (peak-to-peak value)	see Fig. 10	$V_{L(p-p)}$	0,4	–	0,6	V
Operating frequency XTAL		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

For explanation of notes see "Notes to the characteristics".

PACKAGE OUTLINE

SAA7220P/A: 24-lead DIL; plastic (with internal heat spreader) (SOT101A).



Where:

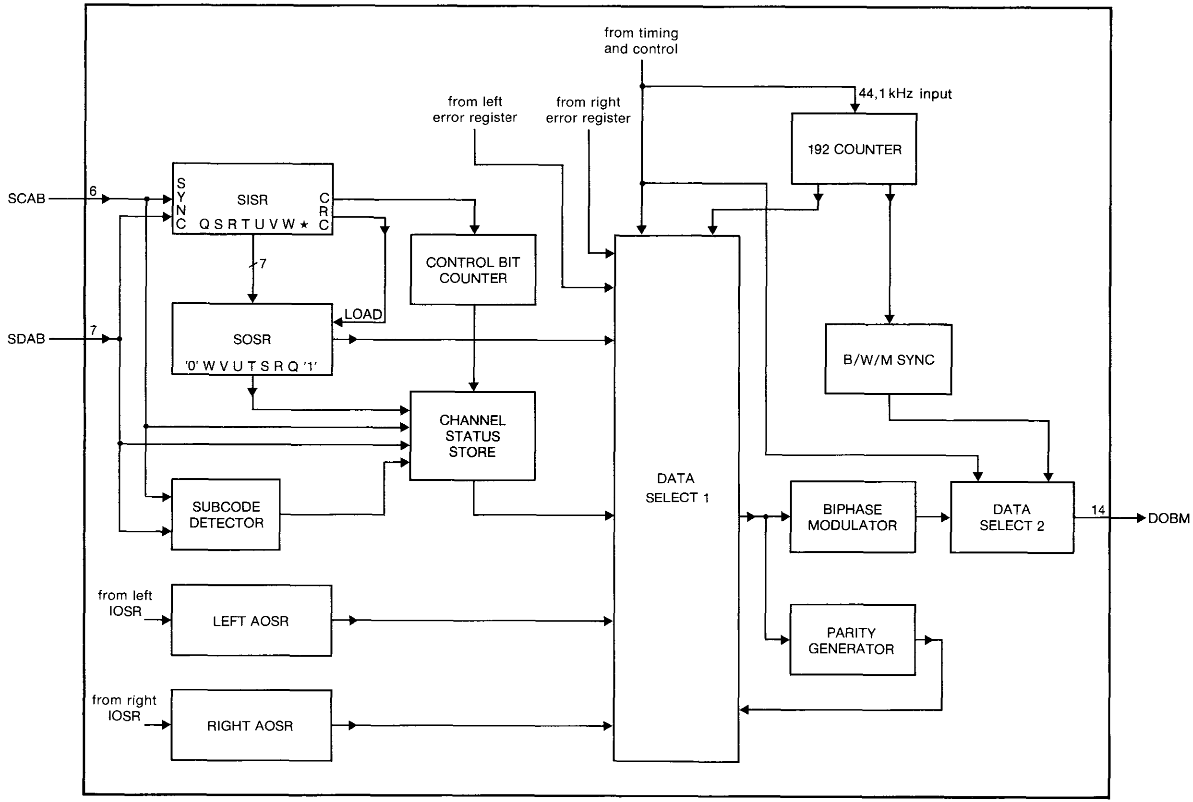
IPSR = Input Shift Register

IISR = Intermediate Input Shift Register

IOSR = Intermediate Output Shift Register

FDSR = Filter Data Shift Register

Fig. 1 Digital filter block diagram.



Where:

SISR	= Subcode Input Shift Register	IOSR	= Intermediate Output Shift Register
SOSR	= Subcode Output Shift Register	AOSR	= Audio Output Shift Register
		*	= Subcode word error flag

Fig. 2 Digital audio output block diagram.

PINNING

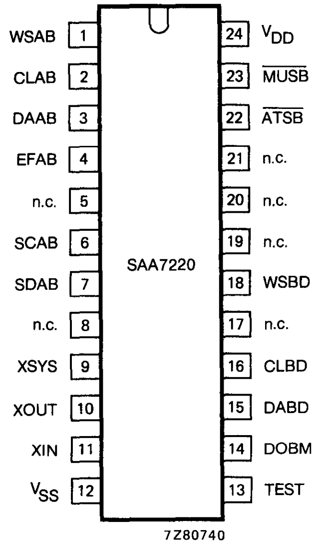


Fig. 3 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	WSAB	**Word Select:** input from A-chip.
2	CLAB	**Clock:** input from A-chip; has an internal pull-up.
3	DAAB	**Data:** input from A-chip.
4	EFAB	**Error Flag:** active HIGH input from A-chip indicating unreliable data. This input has an internal pull-down.
5	n.c.	not connected.
6	SCAB	**Subcode Clock:** a 10-bit burst clock 2,8224 MHz (typ.) input which synchronizes the subcode data. This input has an internal pull-up.
7	SDAB	**Subcode Data:** a 10-bit burst of data, including flags and sync bits serially input from the A-chip once per frame clocked by burst clock input SCAB (see Fig. 8). This input has an internal pull-down.
8	n.c.	not connected.
9	XSYS	**System clock output:** 11,2896 MHz (typ.) output to DAC and to A-chip as slave clock input.
10	XOUT	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
11	XIN	**Crystal oscillator input:** input from crystal oscillator or slave clock.

pin no.	mnemonic	description
12	V_{SS}	**Ground:** circuit earth potentional.
13	TEST	**Test input:** this input has an internal pull-down. In normal operation pin 13 should be open-circuit or connected to V_{SS}.
14	DOBM	**Digital audio output:** this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data. Transmission is by biphase-mark code.
15	DABD	**Data:** this output which is fed to the DAC, together with its clock (CLBD) and word select (WSBD) outputs, conforms to the I^2S format (see Fig. 7).
16	CLBD	**Clock:** output to DAC.
17	n.c.	not connected.
18	WSBD	**Word Select:** output to DAC.
19	n.c.	not connected.
20	n.c.	not connected.
21	n.c.	not connected.
22	$\overline{\text{ATSB}}$	**Attenuation:** when active LOW this control input provides −12 dB attenuation. This input has an internal pull-up.
23	$\overline{\text{MUSB}}$	**Mute:** active LOW control input with internal pull-up.
24	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).

FUNCTIONAL DESCRIPTION

General

The SAA7220 incorporates the following functions:

- Interpolation of data in error
- Attenuation
- Muting
- Finite impulse response transversal filtering with a four times increased sampling rate
- A digital audio output

Serial data formatted in two's complement (DAAB; pin 3) is clocked in by its bit clock (CLAB; pin 2) together with word select (WSAB; pin 1) and error flag (EFAB; pin 4) as shown in Fig. 1. After resynchronization with the internal clocks the data is separated into left and right channels and fed to two identical Input Shift Registers (IPSR). Internal timing and control loads the data into the interpolation RAM via the Intermediate Input Shift Register (IISR).

After interpolation, attenuation and muting the data is fed serially from the Intermediate Output Shift Register (IOSR) to the Audio Output Shift Register (AOSR) and to the IISR. From the IISR it is loaded into the filter RAM.

After filtering the data is passed to the Filter Data Shift Register (FDSR). From the FDSR it is transmitted serially to the data output (DABD; pin 15) together with the appropriate word select (WSBD; pin 18) and bit clock (CLBD; pin 16), in accordance with the I^2S bus specification. Data is again formatted in two's complement. Outputs DABD, WSBD and CLBD are strobed to maintain the correct timing relationship with the system clock output (XSYS) at pin 9 (see Fig. 13).

FUNCTIONAL DESCRIPTION (continued)

The subcode data (SDAB; pin 7) and 10-bit burst clock (SCAB; pin 6) are resynchronized to the internal clocks within the digital audio output block. SCAB clocks the data into the Subcode Input Shift Register (SISR; Fig. 2). Data is transferred to the Subcode Output Shift Register (SOSR) on receipt of all of the 10-bit burst clocks. The subcode data is then mixed with the data from the AOSR and the error flag to provide the output DOBM at pin 14. SISR is reset when no clocks are detected on the SCAB input.

Interpolation

When, for either left or right channel, unreliable samples are flagged between two correct samples, linear interpolation is used to replace the erroneous samples (up to a maximum of 8 consecutive errors).
When the error flag is set, the sample is replaced by a value calculated by the following formula:

$$S(n) = \frac{x}{x+1} \cdot S(n-1) + \frac{1}{x+1} \cdot S(n+x)$$

Where: $S(n)$ = new sample value
x = number of successive erroneous samples following $S(n-1)$
$S(n-1)$ = the preceding sample
$S(n+x)$ = the first following correct sample

The value of x is detected (1 to 8) to determine the coefficients for the multiplications. Eight coefficient pairs are stored in the ROM. If $x = 0$ or $\geqslant 9$ then $S(n)$ will remain unchanged.

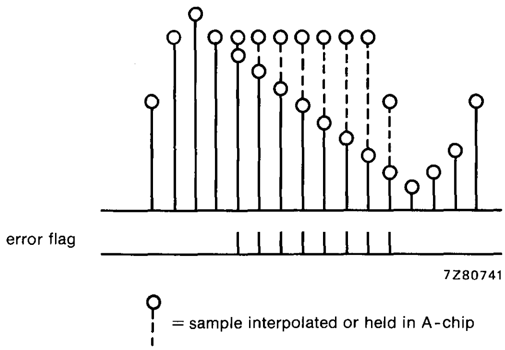


Fig. 4 Example of an eight sample linear interpolation.

Attenuation

Attenuation is controlled by the ATSB input at pin 22. When the input is active LOW the sample is multiplied by a coefficient that provides −12 dB attenuation. If the input is HIGH the multiplication factor is 1.

Mute

Mute is controlled by the MUSB input at pin 23. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. 32 coefficients are used to step down the value of the data, each one being used 31 times before stepping onto the next. When MUSB is released (pin 23 HIGH) the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order.

Filtering

The SAA7220 incorporates two identical finite impulse response transversal filters with the equivalent of 120 taps, one filter for each stereo channel. The corresponding 120 coefficients are structured as 4 sections of 30 coefficients.
(Each ROM contains only 60 filter coefficients, the same 60 being used a second time, but in the reverse order, to make a total of 120.) Plots of the filter characteristics are shown in Fig. 16.

Data is stored in a 480-bit RAM (30 words x 16 bits). The 30 words are sequentially addressed 4 times to generate the 4 output samples.

When a new word is moved from the interpolation RAM to the filter RAM, the oldest word is discarded and all other words moved one position with respect to the ROM coefficients. The data storage effectively forms a 30 sample wide moving window on the input data. The samples move within this window at 5,6448 MHz and the window moves one sample every 22,6 μs.

An output word is formed by multiplying 30 samples from the filter RAM with 30 coefficients from the ROM using a 16 x 12 array multiplier. The result is added in an accumulator. At the end of the 30 multiplications the 16 MSB's are passed from the accumulator via the IOSR to the FDSR, and the accumulator is reset. Overflow protection is incorporated so that the output always limits cleanly in the event of accumulator overflow. Also, to simplify the design of the digital-to-analogue converter a d.c. offset of + 5% is added to the accumulator.

The filtered data is output in the I^2S format at a 5,6448 MHz bit rate and a sample rate of 176,4 kHz.

Digital audio output

Audio 16-bit samples and subcode data are formatted according to the Philips/Sony proposal; "Digital audio interface for domestic use" (Reference Philips 'Red Book' CD-DA standard specification).
The digital audio output (DOBM; pin 14) consists of 32-bit words transmitted in biphase-mark code. That is, two transitions for a logic 1 and one transition for a logic 0. The 32-bit words are transmitted in blocks of 384 words. Table 1 shows the information contained in each word.
The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns (B, M and W) indicate the following situations:

- Sync B; start of a block of 384 words, contains left sample (11101000)
- Sync M; word contains left sample, but is not a block start (11100010)
- Sync W; word contains right sample (11100100)

In the SAA7220 sync words are always preceded by 0. A typical biphase-mark code output is shown in Fig. 11.

Left and right samples are transmitted alternately.
Audio samples are available for digital audio output after interpolation, attenuation and muting, but before filtering.
Data held in the Subcode Output Shift Register (SOSR) is transmitted via the user data bit and is asynchronous with the block rate.

Digital audio output (continued)

Table 1 Composition of the 32-bit digital audio output word

bit number	description	information
1 to 4	sync	–
5 to 8	auxiliary	not used (always zero)
9 to 28	audio sample	bits 9 to 12 not used (always zero). bits 13 (LSB) to 28 (MSB) two's complement
29	audio valid	copy of the error flag
30	user data	used for subcode data
31	channel status	indication of control bits and category code
32	parity bit	even parity for all word bits excluding sync pattern

Channel status

The channel status bit is the same for both left and right words. Therefore a block of 384 words contains 192 channel status bits as shown in Table 2.

When there is no subcode the channel status will switch over to the general format. ' No subcode' is identified by the subcode detector when SCAB is a continuous HIGH or LOW.

Table 2 Channel status bit assignment

bit number	description	subcode provided	no subcode provided
1 to 4	control	copy of Q channel	bits 1 and 2 zero bit 3 image of SCAB bit 4 image of SDAB
5 to 8	reserved	always zero	always zero
9 to 16	category code	CD category bit 9 logic 1	general category all bits zero
17 to 192		always zero	always zero

If a subcode clock is provided but there is no subcode data (SDAB is a continuous HIGH or LOW) the control bits will be zero and the category code will be CD.

The SYNC bit and the cyclic redundancy check bit (CRC) in the subcode data from the A-chip to the B-chip have the format shown by Fig. 5. Typical subcode data input waveforms are shown by Fig. 8.

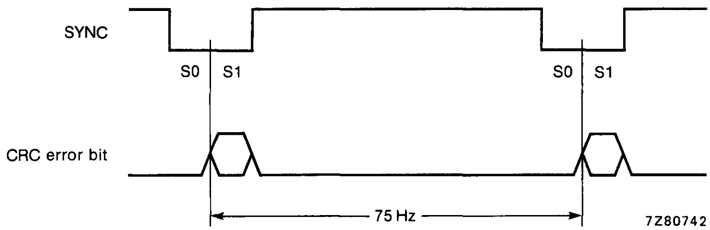


Fig. 5 Subcode data format for SYNC and CRC bits.

SYNC is active LOW and indicates the start of a subcode block, which contains 98 words including 2 sync words, S0 and S1.
CRC is always LOW except during SYNC S1 when:

- CRC = logic 1; previous Q block was true
- CRC = logic 0; previous Q block was false

Two 32-bit words are transmitted at the sample frequency of 44,1 kHz (2 x 32 x 44,1 kHz = 2,8224 Mbits/s data rate). An internal 5,6448 MHz clock (XSYS/2) is used in the biphase modulator.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 24)	V_{DD}	–0,5	–	+ 7,0	V
Maximum input voltage range	V_I	–0,5	–	V_{DD}+ 0,5	V
Storage temperature range	T_{stg}	–55	–	+ 125	°C
Operating temperature range	T_{amb}	–20	–	+ 70	°C
Electrostatic handling*	V_{es}	–1000	–	+ 1000	V

Ensure no electrical connections are made to the underside or ends of the package as there is the possibility of making accidental connection to the lead frame and/or internal heat spreader of the device.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 24)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)	I_{DD}	100	180	285	mA
Inputs					
WSAB, DAAB					
Input voltage LOW (note 1)	V_{IL}	−0,3	−	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	−	V_{DD} + 0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	−	−	μA
at V_I = V_{DD}	I_{LI}	−	−	+ 10	μA
Input capacitance	C_I	−	−	7	pF
EFAB, SDAB (note 2)					
Input voltage LOW (note 1)	V_{IL}	−0,3	−	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	−	V_{DD} + 0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	−	−	μA
at V_I = V_{DD}	I_{LI}	−	−	+ 50	μA
Input capacitance	C_I	−	−	7	pF
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$ (note 3)					
Input voltage LOW (note 1)	V_{IL}	−0,3	−	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	−	V_{DD} + 0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−30	−	−	μA
at V_I = V_{DD}	I_{LI}	−	−	+ 10	μA
Input capacitance	C_I	−	−	7	pF
Crystal oscillator (see Fig. 9)					
Input XIN					
Output XOUT (note 4)					
Mutual conductance at 100 kHz	G_m	1,5	−	−	mA/V
Small signal voltage gain ($A_v = G_m \times R_O$)	A_v	3,5	−	−	V/V
Input capacitance	C_I	−	−	10	pF
Feedback capacitance	C_{FB}	−	−	5	pF
Output capacitance	C_O	−	−	10	pF
Input leakage current					
at V_I = 0 V	I_{LI}	−10	−	−	μA
at V_I = V_{DD}	I_{LI}	−	−	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
Slave clock mode					
Input voltage (note 5) (peak-to-peak value)	$V_{I(p-p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW (note 6)	V_{IL}	0	–	1	V
Input voltage HIGH (note 6)	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 7)	t_r	–	–	20	ns
Input fall time (note 7)	t_f	–	–	20	ns
Input HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%
Outputs (note 4)					
DABD, CLBD, WSBD					
Output voltage LOW at I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
XSYS (note 8)					
Output voltage LOW	V_{OL}	0	–	0,4	V
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
DOBM					
Voltage across a 75 Ω load via attenuator; see Fig. 10 (peak-to-peak value)	$V_{L(p-p)}$	0,4	–	0,6	V
D.C. offset voltage	V_{LDC}	–0,05	–	+ 0,05	V
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Inputs (see Fig. 12)					
SCAB, CLAB (note 9)					
SCAB clock frequency (burst clock)	f_{SCAB}	–	2,8224	–	MHz
CLAB clock frequency	f_{CLAB}	–	2,8224	–	MHz
or (note 10)	f_{CLAB}	–	1,4112	–	MHz
Clock LOW time	t_{CKL}	110	–	–	ns
Clock HIGH time	t_{CKH}	110	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAAB, WSAB, EFAB (note 11)					
Data set-up time	$t_{SU; DAT}$	40	–	–	ns
Data hold time	$t_{HD; DAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
SDAB (note 12)					
Subcode data set-up time	$t_{SU; SDAT}$	40	–	–	ns
Subcode data hold time	$t_{HD; SDAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
Outputs (see Figs 13 and 14)					
WSBD (notes 9 and 13)					
Word select set-up time	$t_{SU; WS}$	40	–	–	ns
Word select hold time	$t_{HD; WS}$	0	–	–	ns
WSBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 13)					
Data set-up time	$t_{SU; DATD}$	40	–	–	ns
Data hold time	$t_{HD; DATD}$	0	–	–	ns
DABD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
CLBD (notes 9 and 13)					
Clock period	t_{CK}	161	177	197	ns
Clock LOW time	t_{CKL}	65	–	–	ns
Clock HIGH time	t_{CKH}	65	–	–	ns
Clock set-up time	$t_{SU; CLD}$	40	–	–	ns
Clock hold time	$t_{HD; CLD}$	0	–	–	ns
CLBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 14)					
Data set-up time	$t_{SU; DATBD}$	40	–	–	ns
Data hold time	$t_{HD; DATBD}$	60	–	–	ns

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
WSBD (notes 9 and 14)					
Word select set-up time	$t_{SU;\,DATWSD}$	40	–	–	ns
Word select hold time	$t_{HD;\,DATWSD}$	60	–	–	ns
DOBM (note 15)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Data bit 0 (note 16)					
pulse width HIGH	$t_{HIGH(0)}$	336	354	372	ns
pulse width LOW	$t_{LOW(0)}$	336	354	372	ns
Data bit 1 (note 17)					
pulse width HIGH	$t_{HIGH(1)}$	172	177	182	ns
pulse width LOW	$t_{LOW(1)}$	172	177	182	ns
XSYS					
Output rise time (note 9)	t_r	–	–	20	ns
Output fall time (note 9)	t_f	–	–	20	ns
Output HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%

INTER·IC I²S SOUND

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

A Philips publication "I²S bus specification" is available on request.

Notes to the characteristics

1. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
2. Inputs EFAB and SDAB both have internal pull-downs.
3. Inputs CLAB, SCAB, $\overline{ATSB}$ and $\overline{MUSB}$ have internal pull-ups.
4. All outputs are short-circuit protected except crystal oscillator output.
5. If used in a.c. coupled mode.
6. $V_{IH} - V_{IL} \geqslant 1{,}6$ V.
7. Reference levels = 10% and 90%.
8. The output current conditions are dependent on the drive conditions.
   When a crystal oscillator is being used the output current capability is I_{OL} = + 0,8 mA; I_{OH} = −0,2 mA. But if a slave input is being used the output currents are reduced to I_{OL} = + 0,2 mA; I_{OH} = −0,2 mA.
9. Reference levels = 0,8 V and 2,0 V.
10. The signal CLAB can run at either 2,8 MHz (1/4 system clock) or 1,4 MHz (1/8 system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being 1/4 or 1/8 of the system clock frequency.
11. Input set-up and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0,8 V and 2,0 V.
12. Input set-up and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0,8 V and 2,0 V.
13. Output set-up and hold times measured with respect to system clock output (XSYS).
14. Output set-up and hold times measured with respect to clock output (CLBD).
15. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.
16. Data bit 0 pulse width times are typically system clock period ($1/f_{XTAL}$) x 4. Maximum and minimum values are ± 5% of this time. Values shown are for f_{XTAL} = 11,2896 MHz, but these will change accordingly if f_{XTAL} changes.
17. Data bit 1 pulse width times are typically system clock period ($1/f_{XTAL}$) x 2. Maximum and minimum values are ± 2,5% of this time. Values shown are for f_{XTAL} = 11,2896 MHz, but these will change accordingly if f_{XTAL} changes.

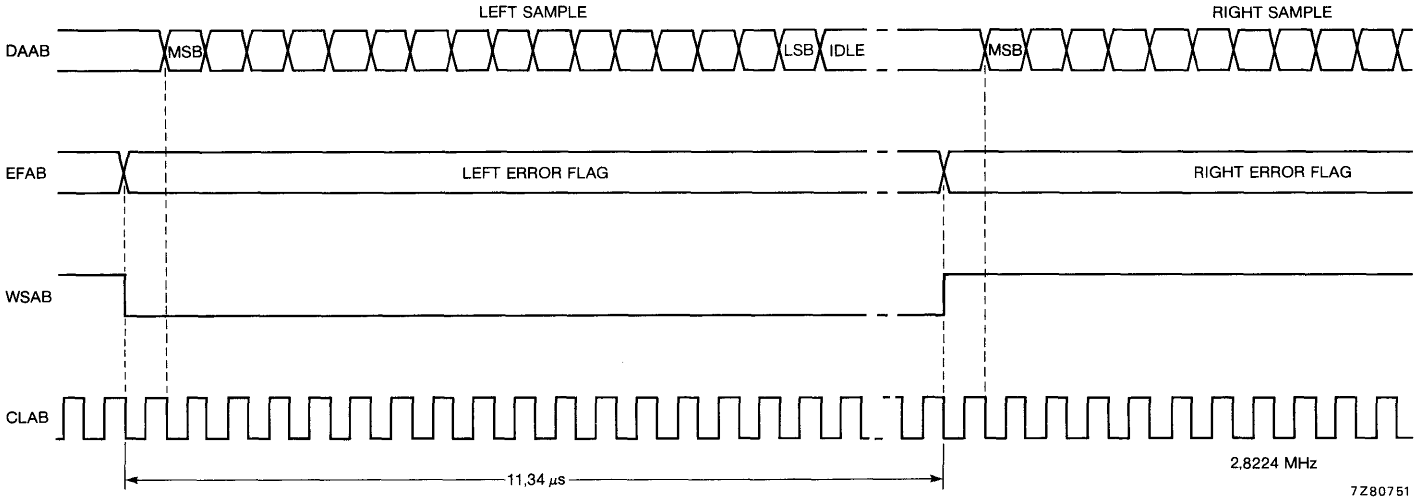


Fig. 6(a) Typical sample data input waveforms from A-chip at 2,8 MHz.

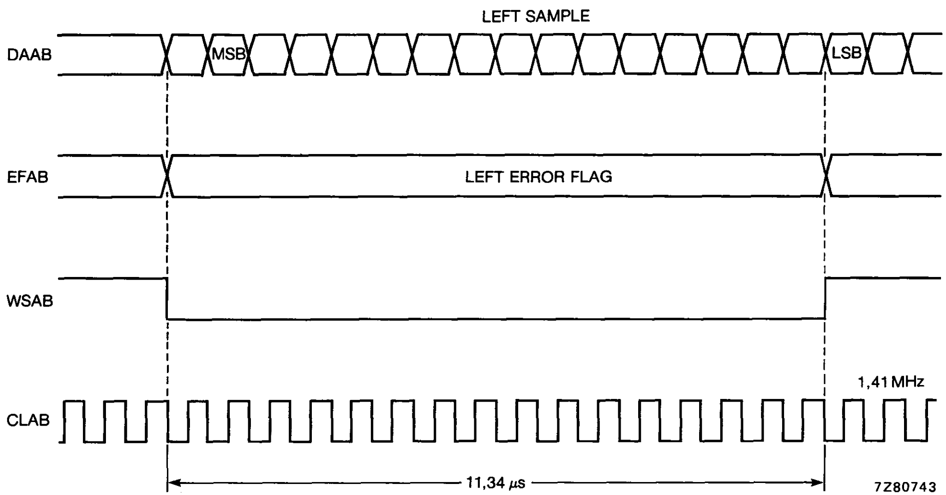


Fig. 6(b) Typical sample data input waveforms at 1,4 MHz.

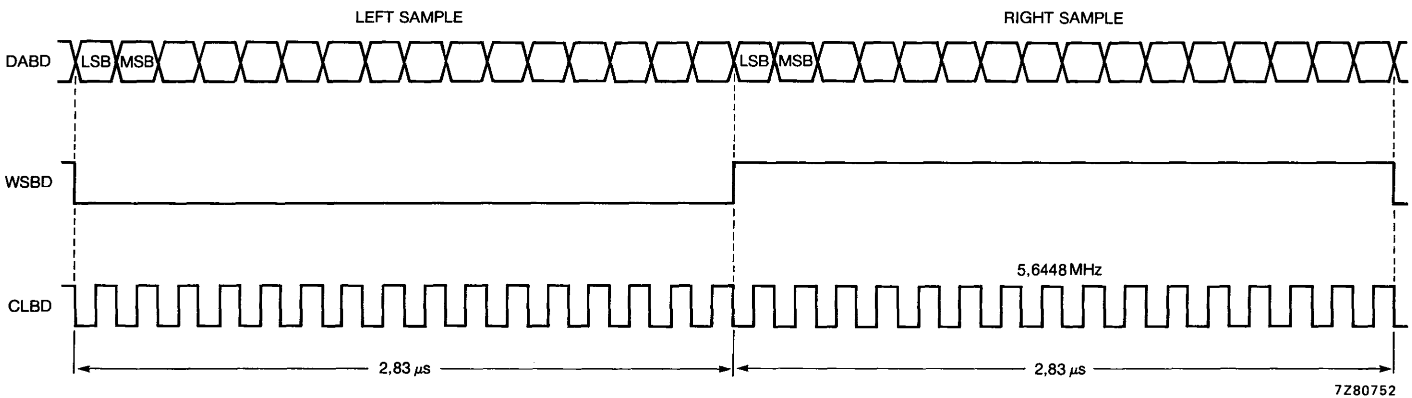
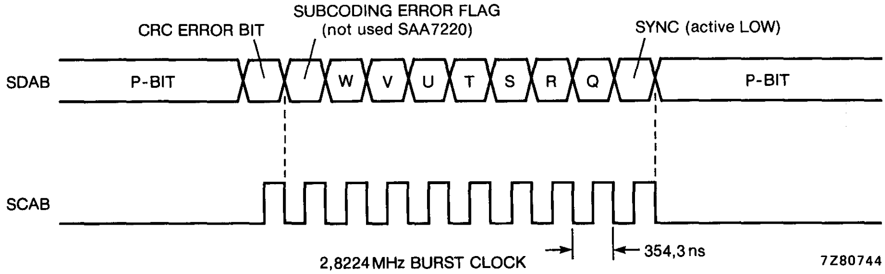
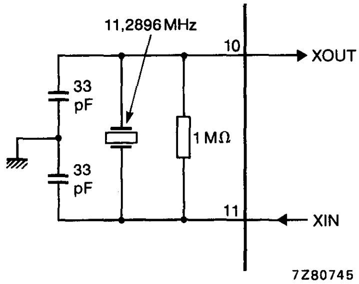


Fig. 7 Typical sample data output waveforms to DAC.



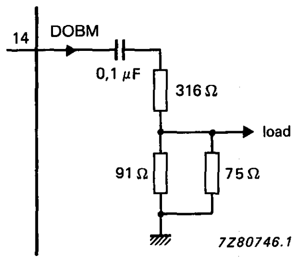
Subcode word frequency = 7,35 kHz.

Fig. 8 Typical subcode data input waveforms.



Oscillator catalogue no. 4322 143 05031

Fig. 9 Crystal oscillator circuit.



Tolerance of resistors = 1 %

Fig. 10 Digital audio output load.

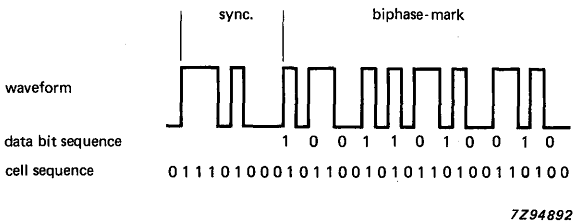


Fig. 11 Biphase-mark code.

TIMING

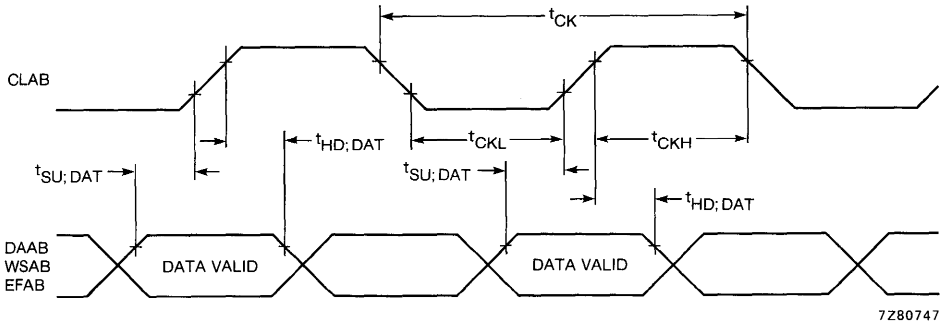


Fig. 12 Data input timings; reference levels = 0,8 V and 2,0 V.
(also applicable to subcode data input ($t_{SU;\,SDAT}$ and $t_{HD;\,SDAT}$).

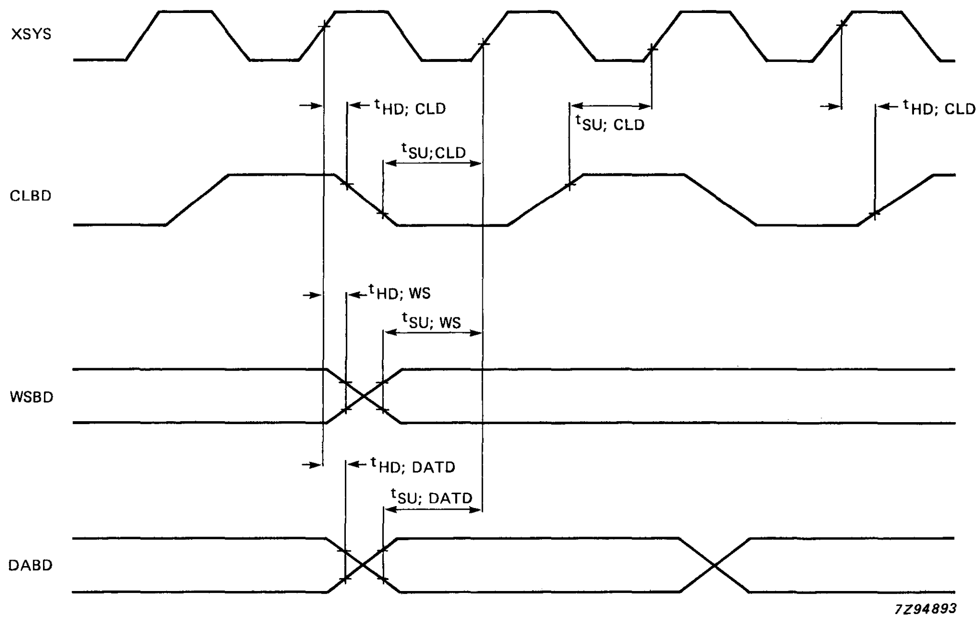


Fig. 13 Data output timings with respect to system clock output (XSYS); reference levels = 0,8 V and 2,0 V.

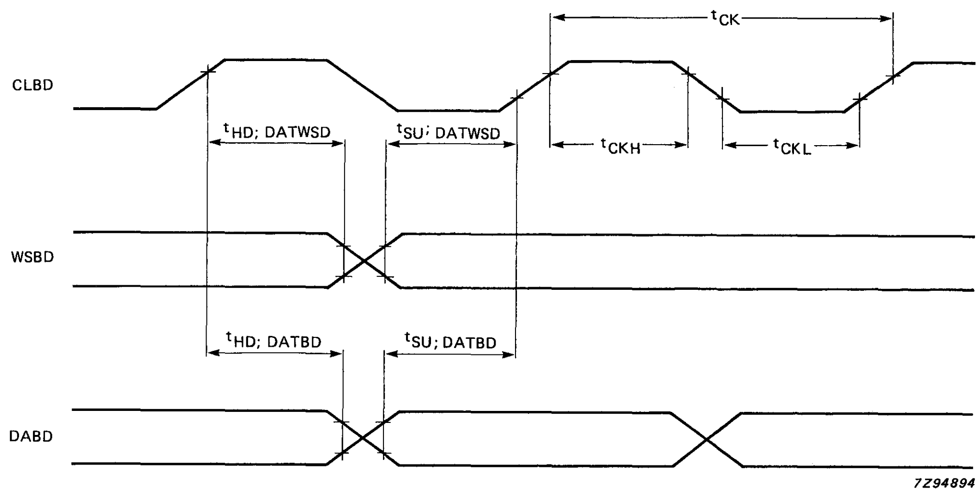


Fig. 14 Data output timings with respect to clock output (CLBD); reference levels = 0,8 V and 2,0 V.

APPLICATION INFORMATION

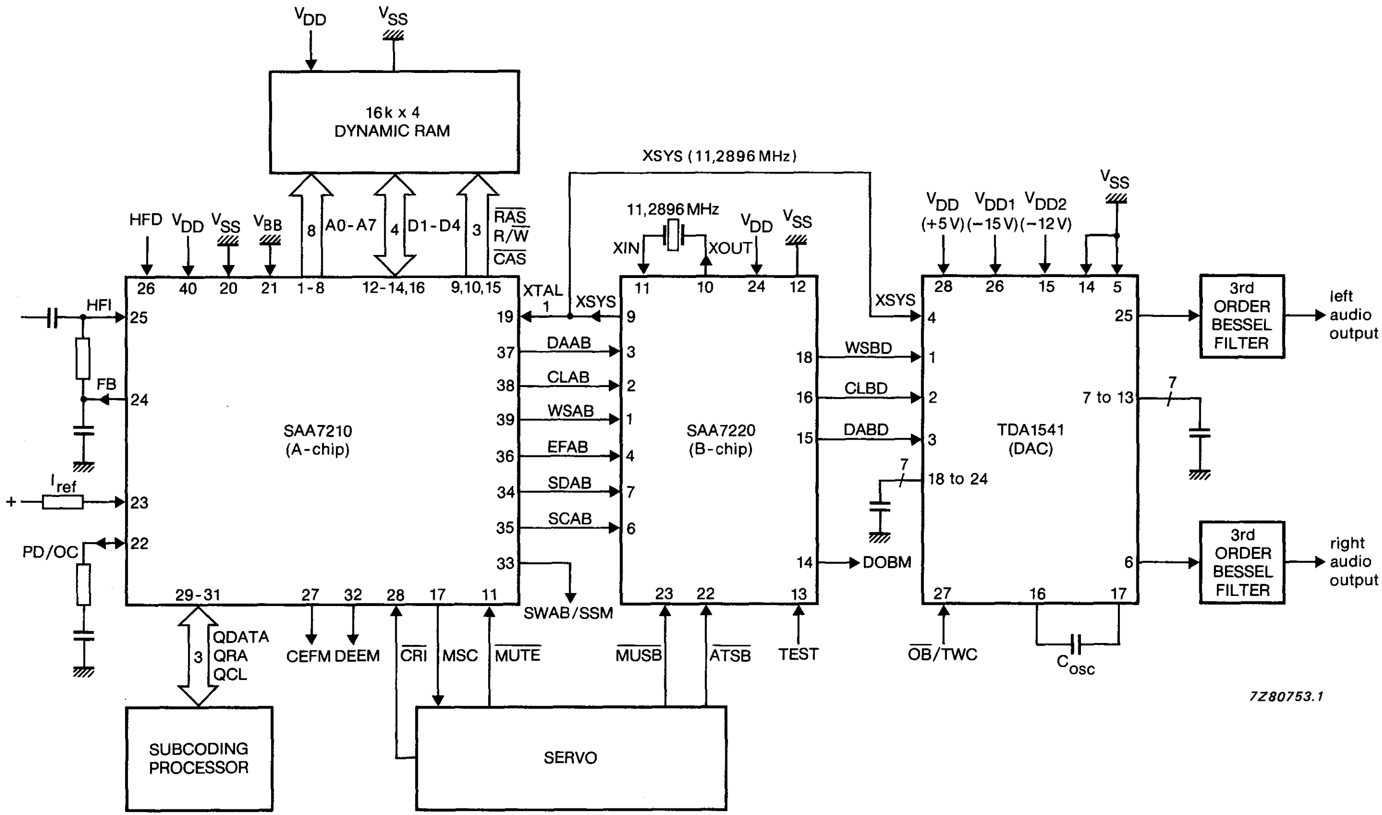


Fig. 15 System application diagram.

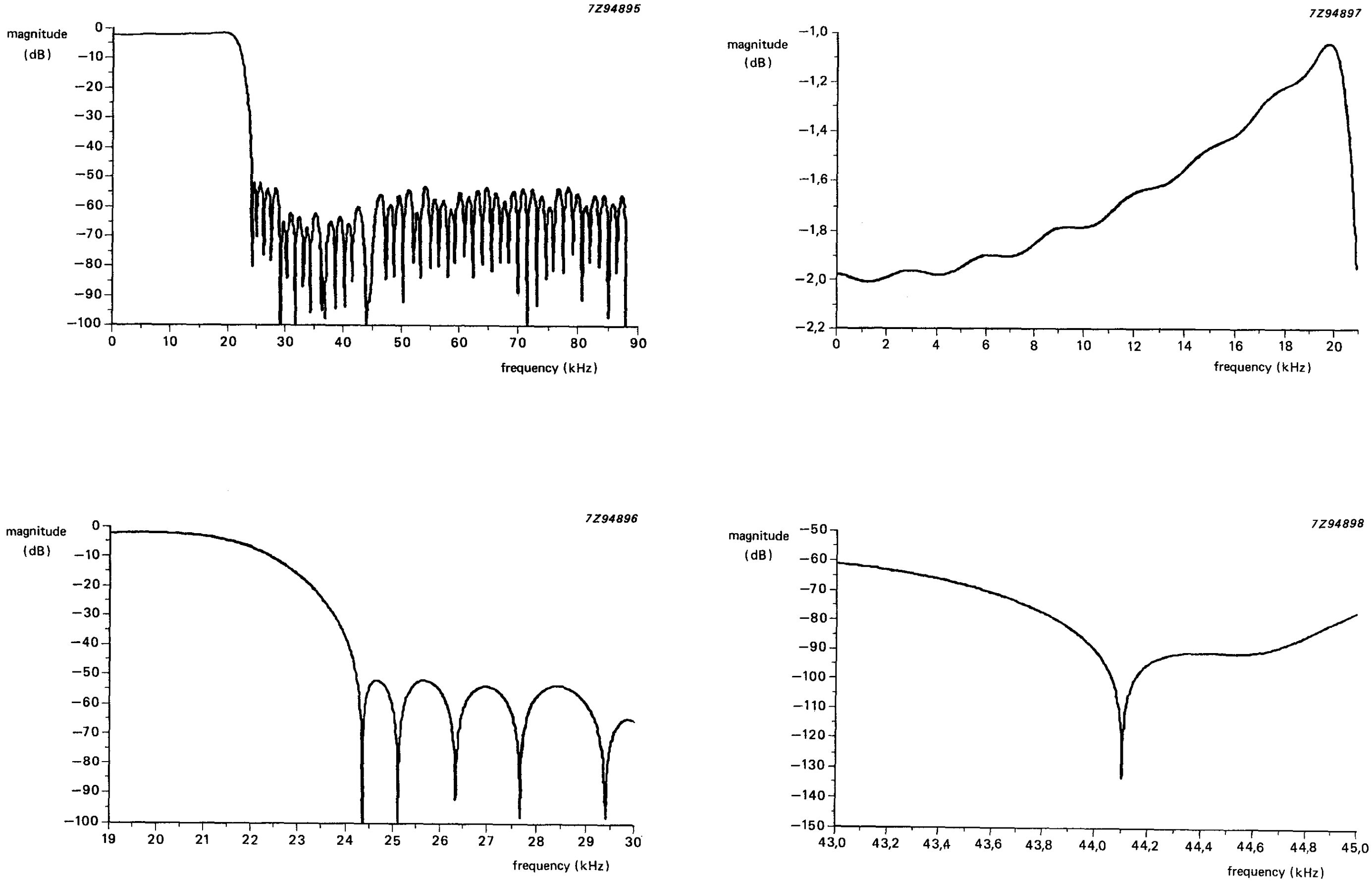


Fig. 16 Digital filter characteristics; magnitude as a function of frequency.

AUDIO DIGITAL INPUT CIRCUIT (ADIC)

GENERAL DESCRIPTION

The SAA7274 is an Audio Digital Input Circuit (ADIC) which converts a 2-channel stereo digital audio signal conforming to the Philips/Sony format into an equivalent binary value of data and control bits. The output function of this device is to convert the equivalent binary value of the data bits (for each channel) into a serial digital audio signal conforming to the I^2S format.

Features

- I^2S bus output
- Biphase audio signal (Philips/Sony format) operating at TTL levels

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	–	5.5	V
Inputs	except IBIFA					
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current	$V_I = 0$ V	$-I_I$	–	–	1	µA
	$V_I = 5.5$ V	I_I	–	–	1	µA
Input capacitance		C_I	–	–	7.5	pF
Outputs	except OSCL					
Output voltage HIGH	$-I_{OH} = 2$ mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	$I_{OL} = 2$ mA	V_{OL}	–	–	0.4	V
Operating ambient temperature range		T_{amb}	–40	–	+70	°C

PACKAGE OUTLINES

SAA7274P: 24-lead DIL; plastic (SOT101A).
SAA7274T: 24-lead mini-pack; plastic (SO24; SOT137A).

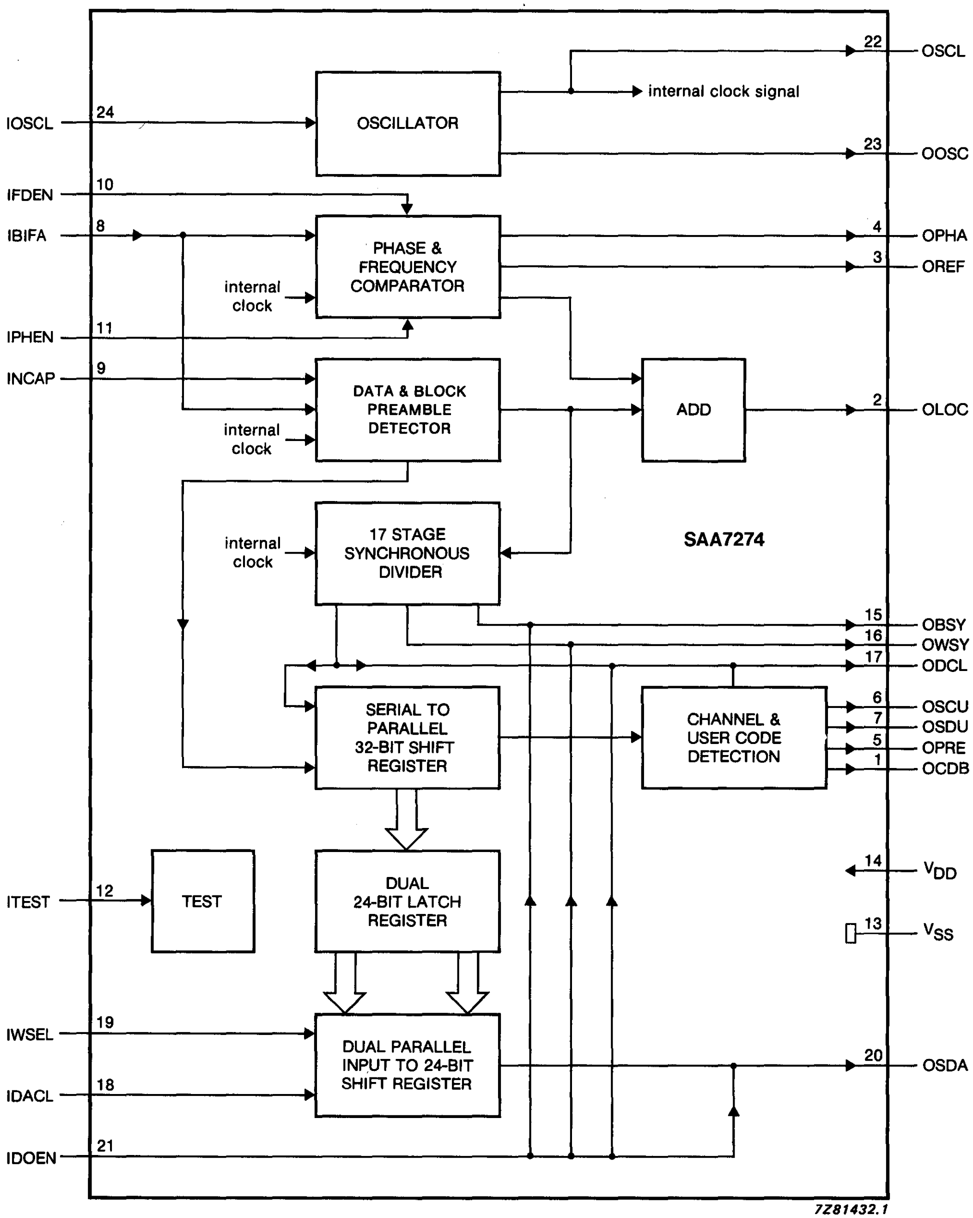


Fig.1 Block diagram.

PINNING

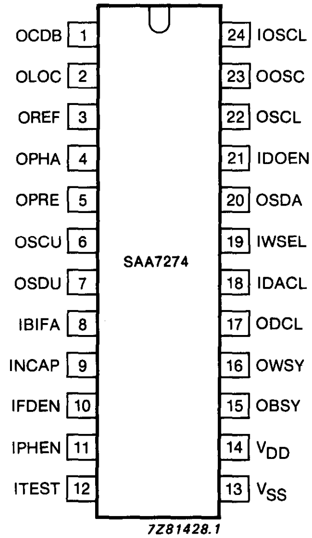


Fig.2 Pinning diagram.

DEVELOPMENT DATA

Power supply

V_{DD}	positive supply voltage (5 V)
V_{SS}	ground (0 V)

Input (capacitive/CMOS with protection)

IBIFA	biphase input signal (min. 1 MHz; max. 3.1 MHz)

Inputs (CMOS protection)

INCAP	capacitive input enable
IFDEN	frequency detector enable
IPHEN	phase-locked loop edge selector
ITEST	test input enable
IDACL	data clock input signal (max. 5 MHz)
IWSEL	word select input signal (max. 50 kHz)
IDOEN	output enable
IOSCL	clock oscillator input (min. 8 MHz; max. 12.5 MHz)

Outputs (CMOS push-pull)

OCDB	control data bits (max. 400 kHz)
OLOC	out-of-lock signal
OREF	phase reference signal (max. 6.2 MHz)
OPHA	phase output signal (max. 6.2 MHz)
OPRE	pre-emphasis level
OSCU	user clock/copy-bit signal (max. 3.1 MHz)
OSDU	user data/pre-emphasis (max. 3.1 MHz)
OSCL	system clock buffer (min. 8 MHz; max. 12.5 MHz)
OOSC	clock oscillator output (min. 8 MHz; max. 12.5 MHz)

Outputs (3-state push-pull)

OBSY	block synchronization output signal (1/49152 system clock)
OWSY	word clock output signal (1/256 system clock)
ODCL	data clock output signal (1/4 system clock)
OSDA	data output signal (max. 2.5 MHz)

FUNCTIONAL DESCRIPTION

Main function

The biphase input signal must conform to the Philips/Sony format, as well as satisfying the following conditions:

- number of channels: 2
- transmission code: biphase mark
- synchronization method: biphase violation
- number of data bits: 24, starting with the LSB
- number of control bits: 4
- preamble values:

preceding cell	0	1
block preamble	11101000	00010111

The main function performs the following tasts:

- Provides the output function with the equivalent binary value of the data bits separately for each of the two channels. These values are available until new information is received.
- To select the biphase input signal (IBIFA) with standard LOCMOS levels when capacitive input enable (INCAP) is LOW.
  To select the biphase input signal capacitively coupled via an internal amplifier to the circuit logic when INCAP is HIGH.
- Generates an out-of-lock output signal (OLOC) which is HIGH when the frequency of the biphase input signal is equal to 1/4 of the system clock frequency and when the block preambles are detected in the biphase input signal.
- If the biphase input signal is not present after 32 clock pulses, then the output OSCU is forced HIGH and outputs OSDU, OPRE, OLOC, OCDB and OSDA are forced LOW.
- Generates a data clock output signal (ODCL) with a frequency of 1/4 of the system clock. When a block preamble is detected in the biphase input signal ODCL is synchronized to a LOW value.
- Generates a word clock output signal (OWSY) with a frequency of 1/256 of the system clock. When a block preamble is detected in the biphase input signal OWSY is synchronized to a LOW value.
- Generates a block synchronization output signal (OBSY). This signal is HIGH during 4 system clock periods and has a frequency of 1/49152 of the system clock. The signal is synchronized with the block preambles of the biphase input signal.
- Generates a phase output signal (OPHA) and a phase reference signal (OREF). If the frequency of the biphase input signal (IBIFA) equals 1/4 of the system clock frequency ($f_{IOSCL}/4$) then the IC generates OPHA and OREF as shown in Fig.3.
  If the frequency of the biphase input signal (IBIFA) is greater or less than 1/4 of the system clock frequency then the IC generates OPHA and OREF as shown in Fig.4.

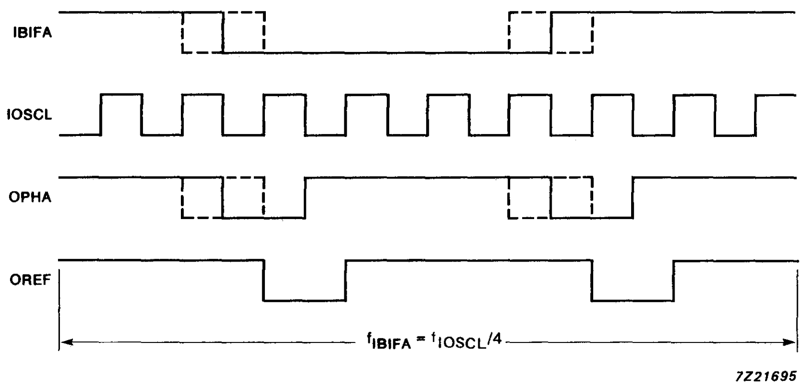


Fig.3 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

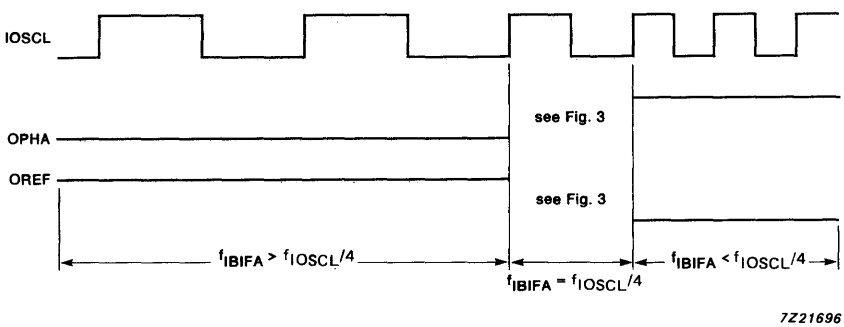


Fig.4 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} \neq f_{IOSCL}/4$.

FUNCTIONAL DESCRIPTION (continued)

Output function

The output function performs the following tasks:

- Provides the data output (OSDA) with the data bits from each channel in the following order:

MSB . . . . LSB 0 0 0 0 0 0 0 0

- Outputs the data of the right and left channel. When word select input signal (IWSEL) is HIGH the data of the right channel is output and when LOW the data of the left channel is output.
- Delivers serial data to the OSDA output, if IDOEN = HIGH. This occurs on each negative transition of the data clock input signal (IDACL). Following a status change at the word select input (IWSEL), the data (MSB first) is output on the first negative transition of IDACL.
  If the number of clock pulses in a word exceeds 24, then the following bits will be internally set to zero.
- Generates the following subcodes:

series 1,	0	0	U1	T1	S1	R1	Q1	1	0	0	
series 2,	CRC	0	V1	U1	T1	S1	R1	Q1	1	0	
series 3,	0	0	W1	V1	U1	T1	S1	R1	Q1	1	

  and after receiving the next user byte:

series 4,	0	0	W2	V2	U2	T2	S2	R2	Q2	1	etc.

- If the value of the category bits, bits 9 to 16 of the input signal, = 10000000 (compact disc format) and the value of the mode bits, bits 7 and 8, = 00, the user data output (OSDU) will deliver the bits of the subcode following the specified lay-out (above). The subcode starts only after receipt of at least 16 zero bits. Simultaneously a user clock signal (OSCU) consisting of 10 clock pulses is present. The output signal starts when a subcode is completed and is clocked on the negative transition of OSCU. The first data word of each subcode frame is output 3 times in succession with the data pattern shifted each time as outlined for series 1 through series 3 in the layout given above. The CRC performs a check on the 96 Q bits of the preceding subcode. If CRC is correct then the CRC bit = 1.
- Channel status:

  copy permitted (bit 3)
  pre-emphasis (bit 4)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	. . .
control		.	.	res	.	mode		category								

  If the value of the category bits **do not** equal 10000000 (compact disc format) and the value of the mode bits equals 00 (mode 0), then:

  output OSDU indicates the status of bit 4 (pre-emphasis) of the channel status and output OSCU indicates the status of bit 3 (copy permitted) of the channel status provided the control bits conform to the 2-channel audio signal format.

- Uses the output pre-emphasis (OPRE) to indicate the status of bit 4 of the channel status for a 2-channel audio signal.
- Outputs the 4 control bits of the biphase input signal (IBIFA) represented by V, U, C and P at OCDB. The output delivers the bits in the same sequence during the next word, each bit continues for 32 clock pulses.

Additional input and output signals

The following input and output signals are available from this circuit:

- Phase output signal (OPHA) and phase reference signal (OREF) for use in a phase-locked loop (PLL). The OPHA signal is a result of the difference between the frequency and phase of the biphase input signal and the system clock. OREF signal provides the reference signal for the PLL.
- Input signal IFDEN enables the frequency detector. The frequency detection as present in the 2 signals OPHA and OREF can be enabled by taking this signal LOW.
- Data clock output signal (ODCL), which has a frequency of 1/4 of the system clock frequency.
- Word clock output signal (OWSY), which has a frequency of 1/256 of the system clock frequency.
- Block synchronization output signal (OBSY), which has a frequency of 1/49152 of the system clock.
- ODCL, OWSY and OBSY will be synchronized to the block preambles in the biphase input signal IBIFA.
- Outputs ODCL, OWSY, OBSY and OSDA are enabled via a 3-state mode by input IDOEN.
- IPHEN input selects dual or single edge detection of the input signal IBIFA in the phase detector. A low level selects the single-edge detection mode.
- Out-of-lock signal (OLOC). This output is LOW if the PLL is out-of-lock, or no block preambles are present in the biphase input signal IBIFA.
- User data/pre-emphasis output signal (OSDU). After receiving a category code of mode 0 from a non-compact disc source this signal outputs the pre-emphasis bit of the channel status bits in the biphase input signal. If the category code of mode 0 is from a compact disc source then the user data bits from the subcode channel including the CRC check on the 96 preceding Q bits are output.
- User clock/copy bit output signal (OSCU). After receiving a category code of mode 0 from a non-compact disc source then the copy bit of the channel status bits in the biphase input signal is output. If the category code of mode 0 is from a compact disc source then 10 clock pulses for the 'user data' are output.
- Pre-emphasis level output signal (OPRE), which indicates the value of the pre-emphasis bit of the channel status bits after receiving the two-channel audio fromat in the biphase input signal (IBIFA).
- Control data bits output signal (OCDB), which contains the 4 control bits of each word of the biphase input signal.
- Input ITEST is used for device tests at the factory only, for normal operation it has to be connected to V_{SS}.

Clock oscillator

The clock oscillator of the circuit can be formed by connecting either LC components or a crystal or a ceramic resonator between the oscillator input and output pins.

The circuit can also be driven by an external signal source applied to the oscillator input. The oscillator output is buffered and available at pin OSCL. The internal circuitry is driven via an inverter, which is connected to the buffered output. This allows all the output signals (especially ODCL, OWSY and OBSY) to change their state after a pulse from OSCL, independent of the capacitive load of the OSCL pin. All output signals of the circuit are triggered on the positive transition of the buffered OSCL signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	–0.5	7.0	V
Input voltage	note 1	V_I	–0.5	V_{DD}+0.5	V
Maximum input current		I_{IM}	–	±10	mA
Maximum output current		I_{OM}	–	±10	mA
Maximum supply current in V_{SS}		I_{SS}	–	–40	mA
Maximum supply current in V_{DD}		I_{DD}	–	+40	mA
Maximum power dissipation per output		P	–	50	mW
Total power dissipation		P_{tot}	–	280	mW
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–40	+70	°C

Note

1. Input voltage should not exceed 7 V unless otherwise specified.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

INTER·IC I^2S SOUND

Purchase of Philips' I^2S components conveys a license under the Philips' I^2S patent to use the components in the I^2S-system provided the system conforms to the I^2S specification defined by Philips.

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to +70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current	note 1	I_{DD}	–	–	100	μA
	note 2	I_{DD}	–	*	–	mA
Inputs						
IBIFA						
Input voltage (peak-to-peak value)	note 3	$V_{I(p-p)}$	30	–	300	mV
Input voltage (non-active)	INCAP = V_{DD}	V_I	–	–	5	mV
All other inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current	V_I = 0 V	$-I_I$	–	–	1	μA
	V_I = 5.5 V	I_I	–	–	1	μA
Input capacitance		C_I	–	–	7.5	pF
Outputs						
OSCL						
Output voltage HIGH	$-I_{OL}$ = 8 mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	I_{OL} = 10 mA	V_{OL}	–	–	0.4	V
All other outputs						
Output voltage HIGH	$-I_{OL}$ = 2 mA	V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
OSDA, ODCL, OWSY, OBSY						
Output leakage current	3-state	I_{LO}	–	–	10	μA
OWSY, ODCL and OBSY						
Load capacitance		C_L	20	–	50	pF
OSCL						
Load capacitance		C_L	–	–	80	pF
All other outputs						
Load capacitance		C_L	–	–	50	pF

Notes to the DC characteristics

1. V_O = V_{DD}, I_O = 0 mA on all outputs and V_I = V_{SS} on all inputs, except INCAP which must be at V_{SS}.
2. f_{OSCL} = 11.3 MHz.
3. INCAP = V_{DD}, f_{min} = 1 MHz, t_r and t_f = 10%.

* Value to be fixed.

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = –40 to +70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency						
IOSCL		f_{IOSCL}	–	–	12.5	MHz
Timing pulse LOW		t_{PL}	37	–	–	ns
Rise and fall time		t_r, t_f	–	–	10	ns
Set-up and hold times						
IWSEL to IDACL	see Fig.5					
Data set-up time		t_{SU}	1	–	–	*
Data hold time		t_{HD}	–	–	1	*
Proagation delays						
IOSCL to OSCL		t_p	–	–	10	ns
IDACL to OSDA		t_p	–	–	50	ns
OSCL to OWSY and ODCL						
HIGH-to-LOW		t_{PHL}	10	–	50	ns
LOW-to-HIGH		t_{PLH}	10	–	50	ns
Rise and fall times						
OSCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	5	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	15	ns
OWSY and ODCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	10	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	40	ns

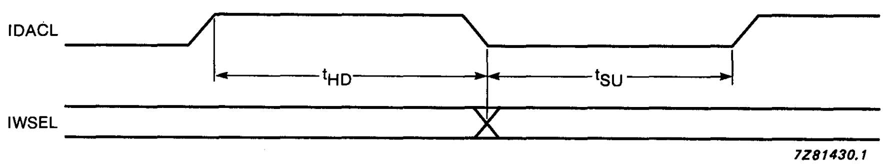
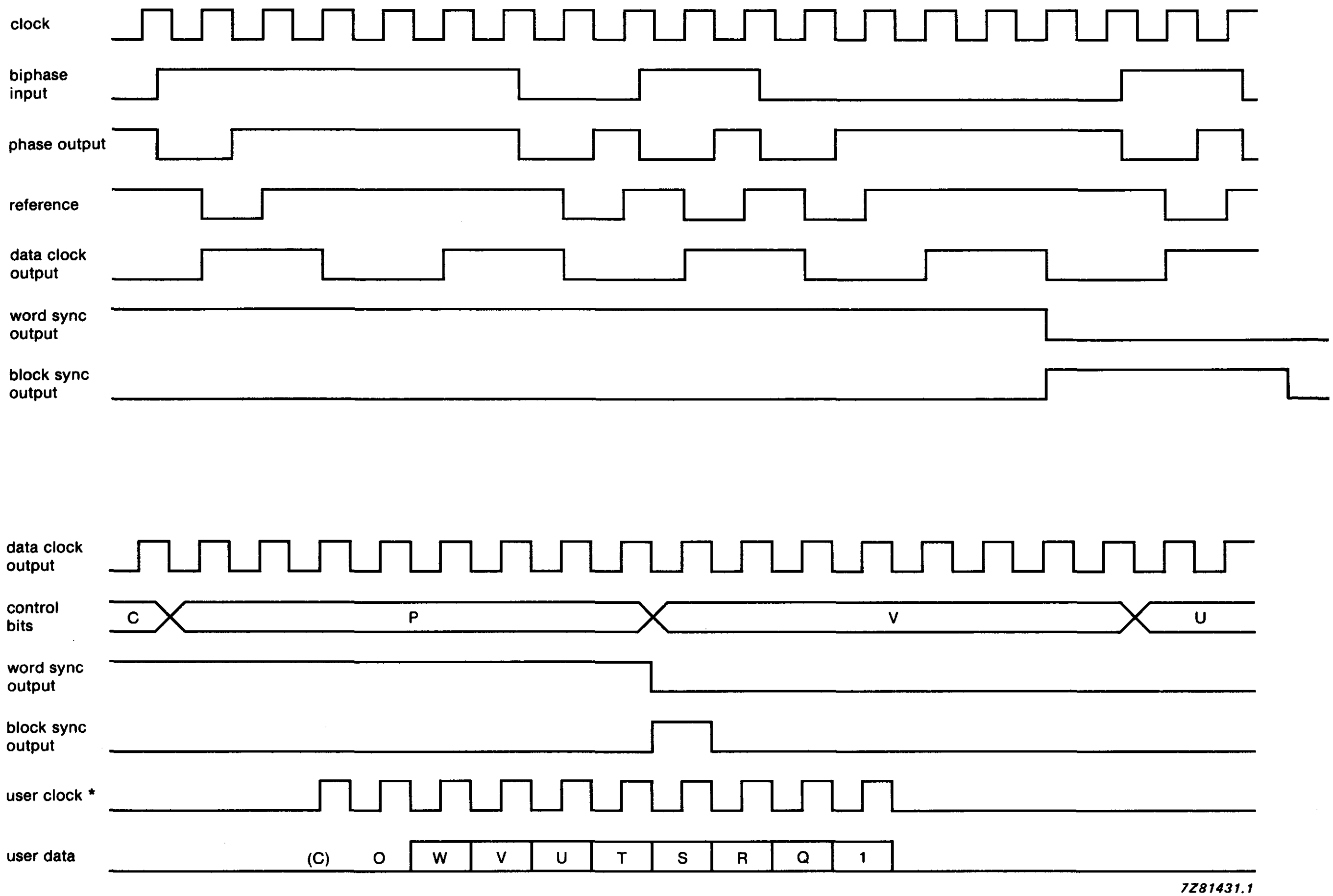


Fig.5 Set-up and hold time diagram.

* Clock periods of OSCL.

DEVELOPMENT DATA



* user clock pattern is not necessarily synchronous with the block sync signal.

Fig.6 Timing diagram.

CMOS DECODER FOR COMPACT DISC SYSTEMS

GENERAL DESCRIPTION

The SAA7310 (CD3A) incorporates the functions of demodulator, subcoding processor, motor speed control, error corrector and concealment in one CMOS chip. The device accepts data from the disc and outputs serial data via the Inter IC signal bus (I^2S) directly to a digital-to-analogue converter (such as the stereo CMOS dual DAC; SAA7320). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering.
The SAA7310 is available in both 40-pin DIL and 44-pin QFP packages.

Features

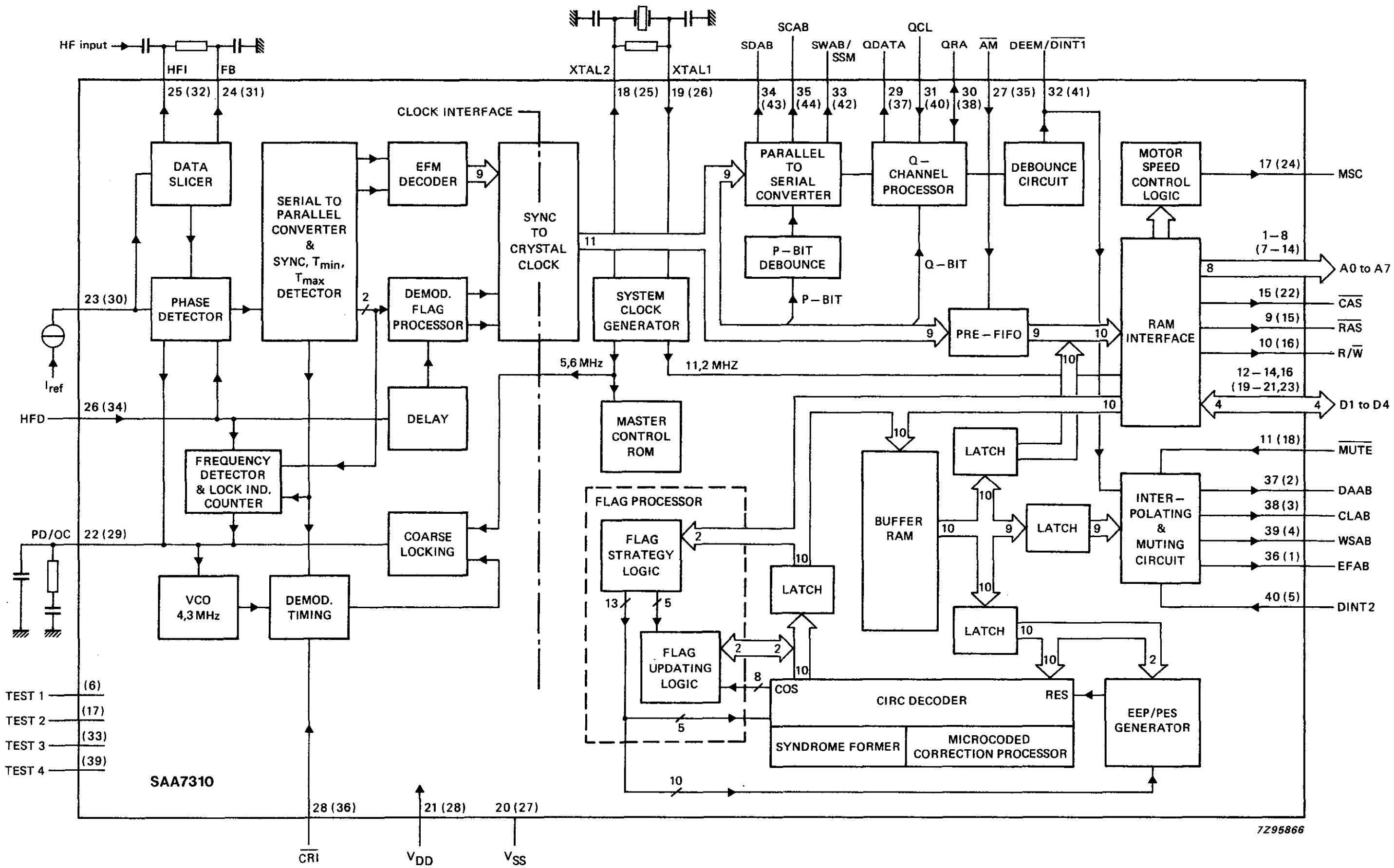
- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Adaptive CIRC error correction enabling 4 erroneous symbols per frame (32 symbols) to be corrected
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange
- Bidirectional data bus to external RAM (16 K x 4 bits) with 64-frame FIFO capacity
- Demodulator PLL requiring virtually no peripheral components
- Replacement for the CD2A
- Low power consumption (typ. 175 mW)
- Track loss correction by additional muting
- Non-digital audio interface application (such as CD-ROM or CD-I)
- 2-package option
- −40 to +85 °C operating temperature range

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	35	50	mA
Data slicer input voltage (peak-to-peak value)	$V_{I(p-p)}$	0,5	–	2,5	V
Oscillator operating frequency					
XTAL	f_{XTAL}	10,16	11,2896	12,42	MHz
VCO (PLL locked on to data)	f_{VCO1}	2,54	4,3218	6,21	MHz
Output current (each output)	I_O	−10	–	+ 10	mA
Operating ambient temperature	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINES

SAA7310P : 40-lead DIL; plastic (SOT129).
SAA7310GP : 44-lead QFP; plastic (SOT205A).



Pins in parenthesis relate to 44-pin QFP package.

Fig. 1 Block diagram.

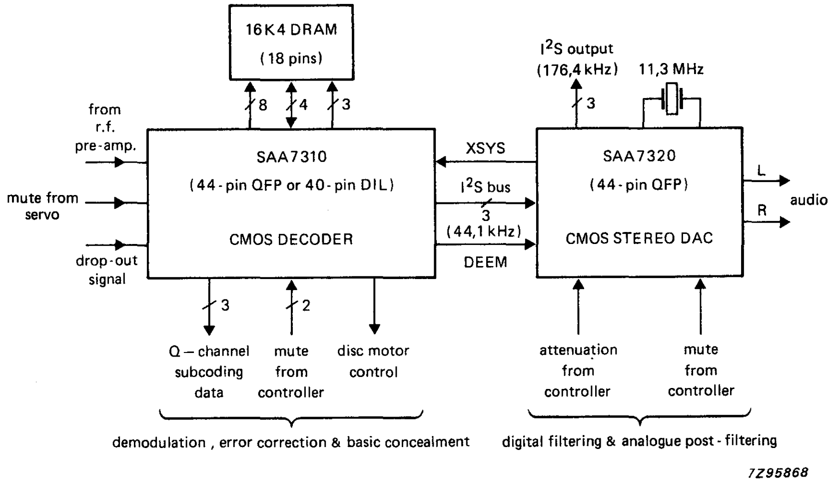


Fig. 2 (a) Block diagram of SAA7310 as used with SAA7320.

DEVELOPMENT DATA

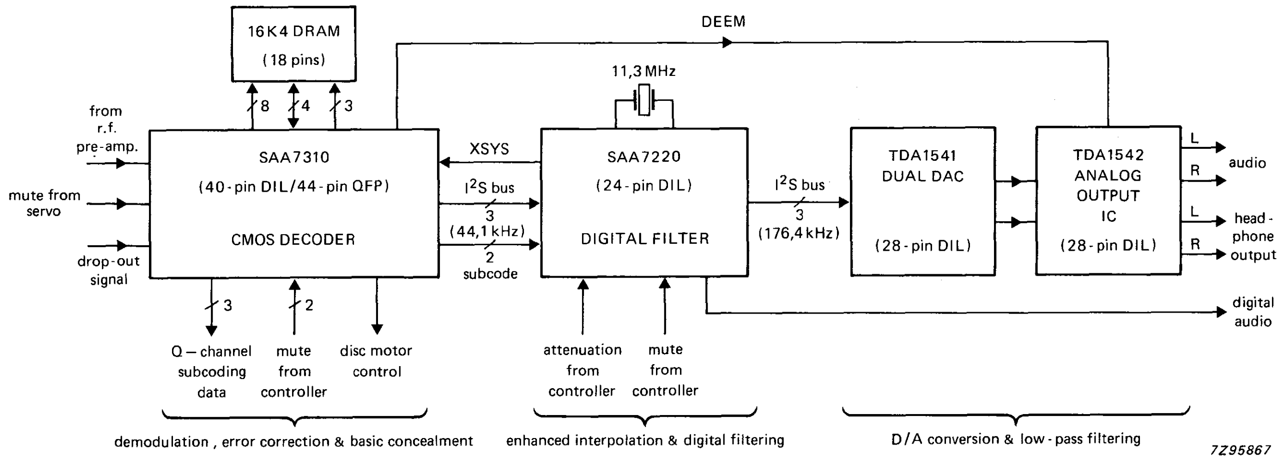


Fig. 2 (b) Block diagram of SAA7310 as used with SAA7220.

PINNING

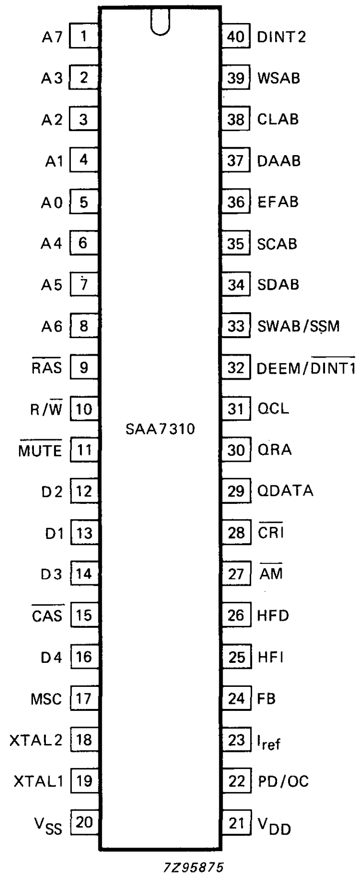


Fig. 3 Pinning diagram; for 40-lead DIL package.

PINNING (continued)

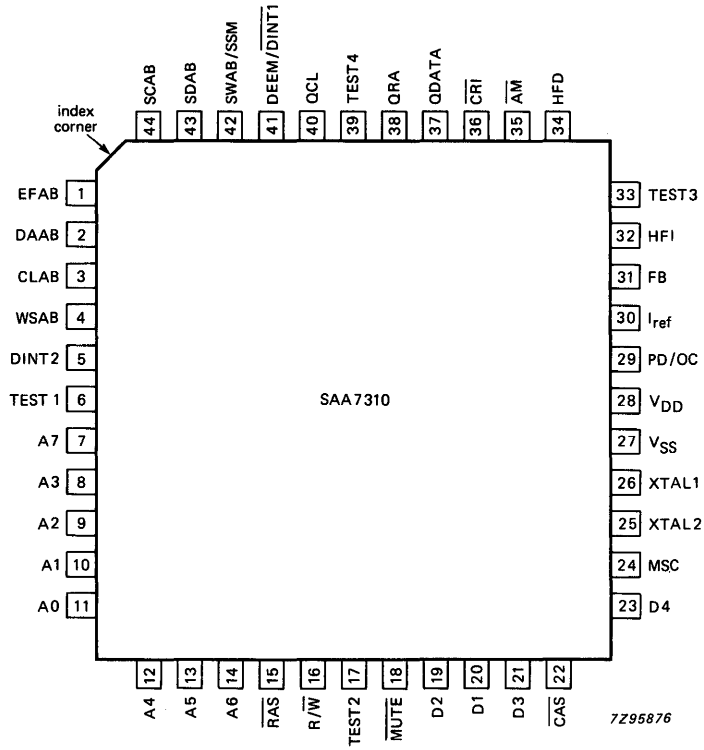


Fig. 4 Pinning diagram; for 44-lead QFP package.

DEVELOPMENT DATA

Pin functions

pin no. DIL	QFP	mneumonic	description
1 - 8	7 - 14	A0 - A7	**Address:** address outputs to external RAM.
9	15	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	16	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	18	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB, pin 37 (2), is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first 'good' value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12 - 14	19 - 21	D1 - D3	**Data:** data inputs/outputs to external RAM.
15	22	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	23	D4	**Data:** data input/output to external RAM.
17	24	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (42) (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continuous 50% duty factor.
18	25	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	26	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	27	V_{SS}	**Ground:** circuit earth potential.
21	28	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).
22	29	PD/OC	**Phase Detector output/ Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	30	I_{ref}	**Current reference:** external reference input to the phase detector and data slicer. This input is required to minimize the spread in the charge pump output of the phase detector and data slicer.
24	31	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input HFI at pin 25 (32) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD at pin 26 (34) is LOW, this output goes to a high impedance state.

Pin functions (continued)

pin no.		mneumonic	description
DIL	QFP		
25	32	HFI	**High-Frequency Input:** level detector input to the data slicer. A differential signal of between 0,5 and 2,5 V (peak-to-peak value) is required to drive the data slicer correctly. When a T_{max} violation is detected or when HFD is LOW, this input is biassed directly to its threshold voltage
26	34	HFD	**High-Frequency Detector:** when HIGH this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer. An internal voltage clamp of 3 V (typ.) requires the HFD input to be fed via a high impedance. This input has an internal pull-up of 50 kΩ (typ.).
27	35	$\overline{\text{AM}}$	**Additional Mute:** This pin is normally held HIGH. Should track loss occur the pin should be taken LOW and then the data is forced LOW at the pre-FIFO stage. The muted data will then be corrected after de-interleaving. **Note** With DINT2, DEEM/$\overline{\text{DINT1}}$, FB set to logic 0 and SDAB, SCAB set to logic 1, this pin becomes the demodulator clock output (CEFM) of the SAA7210 (CD2A).
28	36	$\overline{\text{CRI}}$	**Counter Reset Inhibit:** when LOW this input signal allows the divide-by-588 master counter in the DEMOD timing to run-free. This input has an internal pull-up of 50 kΩ (typ.).
29	37	QDATA	**Q-channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol).
30	38	QRA	**Q-channel Request input/Acknowledge output:** the output has an internal pull-up of nominally 10 kΩ. (see subcoding microprocessor handshaking protocol).
31	40	QCL	**Q-channel Clock:** clock input generated by the microprocessor when it detects a QRA LOW signal.
32	41	DEEM/$\overline{\text{DINT1}}$	**De-emphasis output and data interpolated input:** signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit in DEEM mode. When using the CD3A in a non-digital audio application this pin should be set HIGH (with DINT2 set LOW) to prevent data being interpolated. **Note** This pin should **only** be used in its input mode when DINT2 is LOW.
33	42	SWAB/SSM	**Subcoding Word clock output and Start/Stop Motor input:** open drain output which is sensed during each HIGH period and if externally forced LOW a motor-stop condition will be decoded and fed to the motor control logic circuit. When allowed to return HIGH, the motor will start. This open-drain output has an internal pull-up of 10 kΩ (typ.).

Pin functions

pin no. DIL	QFP	mneumonic	description
34	43	SDAB	**Subcoding Data:** a 10-bit burst of data, including flags and sync bits, is output serially once per frame clocked by burst clock output SCAB (see Fig. 6).
35	44	SCAB	**Subcoding Clock:** a 10-bit burst clock 2,8224 MHz (typ.) output which is used to synchronize the subcoding data.
36	1	EFAB	**Error Flag:** output from interpolation and mute circuit indicating unreliable data.
37	2	DAAB	**Data:** this output together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Fig. 7).
38	3	CLAB	**Clock:** I^2S output.
39	4	WSAB	**Word Select:** I^2S output.
40	5	DINT2	**Data interpolated input:** this pin should normally be set HIGH. When using the CD3A in a non-digital audio application this pin should be set LOW (with DEEM/$\overline{\text{DINT1}}$ set HIGH) to prevent data being interpolated.

The following pins apply to the 44-pin QFP package only:

–	6	TEST1	**Test output 1**
–	17	TEST2	**Test output 2**
–	33	TEST3	**Test output 3**
–	39	TEST4	**Test output 4**

Note to the pin functions

The pin sequence of the address outputs (A0 - A7) and the data outputs (D1 - D4) has been selected to be compatible with various dynamic 16 K x 4-bit RAMs including the 4416.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

All references to pin numbers show the 40-lead DIL pin first followed by the 40-lead QFP pin in parenthesis.

Demodulation

Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at the input data rate (typically at 4,3218 MHz), its frequency being dependent on the voltage at pin 22 (29) (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output provides the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (29), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source I_{ref} connected to pin 23 (30).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input at pin 28 (36) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.

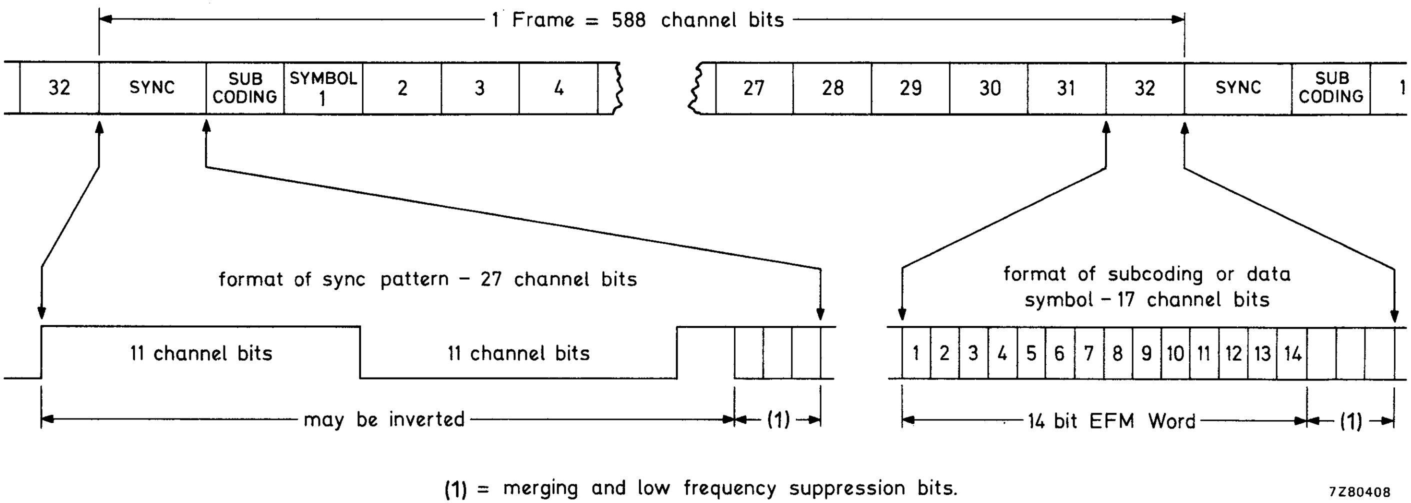


Fig. 5 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output pin 32 (41) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34 (43). The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally in the rising edge of SWAB at pin 33 (42); see Fig. 6.

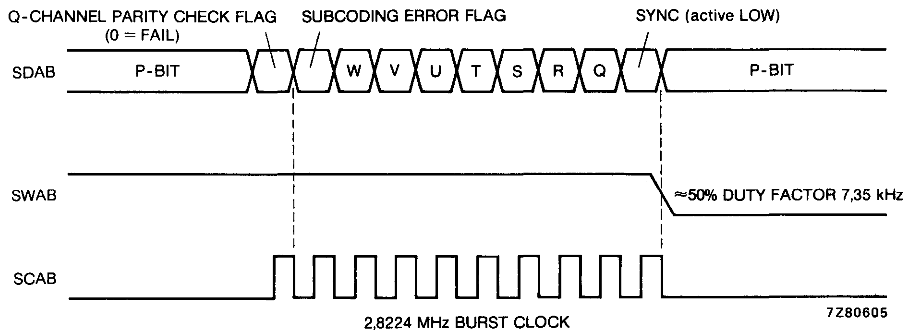


Fig. 6 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4-symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency.

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 8) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address $\overline{RAS}$ pin 9 (15) is set up first and then three 4-bit nibbles are accessed using sequential column addresses $\overline{CAS}$ pin 15 (22). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good' data (flags = 00) and three levels of error can be indicated.

The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

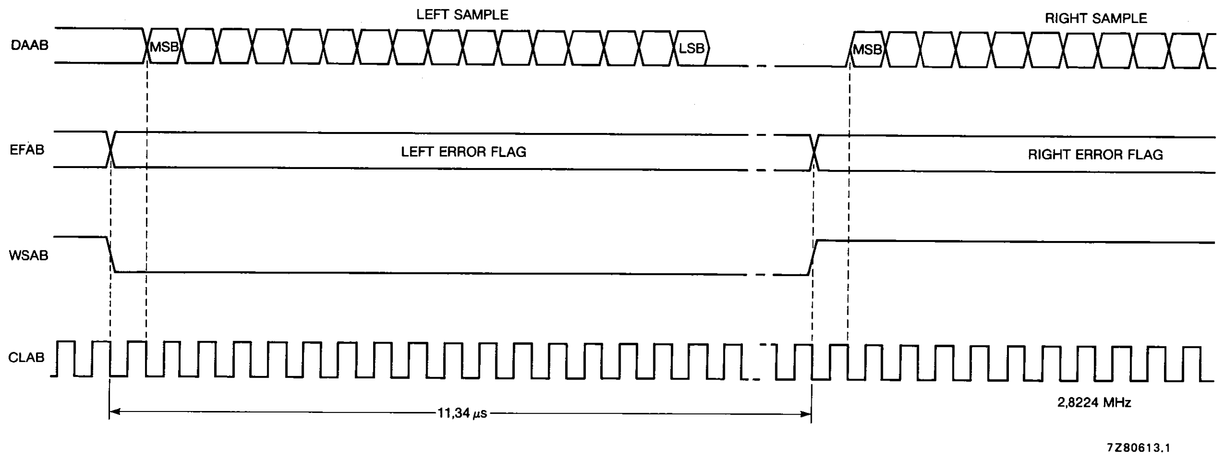


Fig. 7 Typical I²S waveform outputs to SAA7220 or SAA7320.

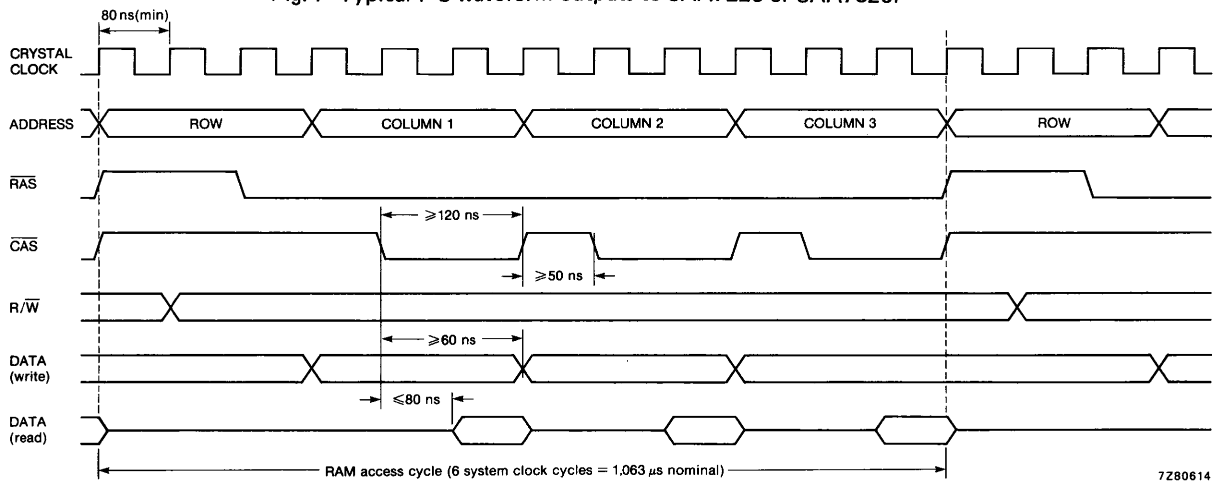


Fig. 8 RAM timing waveforms: timings based on RAM TMS4416; $\overline{G}$ input to RAM held LOW.

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

When using the CD3A in a non-digital audio application, pins DINT2 and DEEM/$\overline{\text{DINT1}}$ should be set to logic 0 and logic 1 respectively. The URD flag will then be disabled to prevent data being interpolated.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the SAA7220 where it receives additional and more efficient concealment (see Fig. 9).

FUNCTIONAL DESCRIPTION (continued)

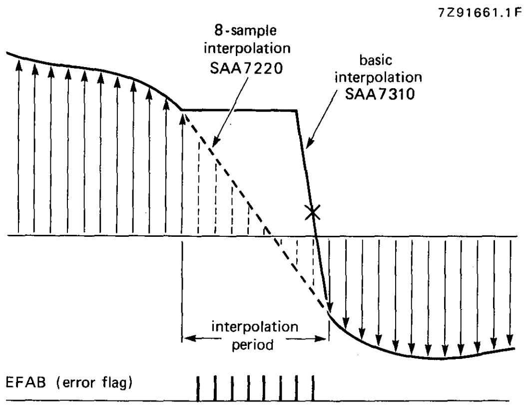


Fig. 9 The SAA7220 can make an 8-sample linear interpolation, the SAA7310 a hold and single-sample interpolation. When interpolating more than 8 samples, a hold function operates in the SAA7220 before the interpolation.

Non-digital audio applications

The CD3A contains a special mode for non-digital applications such as CD-ROM and CD-I. In this mode the concealment section is not allowed to operate. The flagged output words of the error correction circuit are passed to the output DAAB without being affected by the interpolation circuit. The EFAB output signal indicates unreliable output words on a sample basis when one or both bytes in a sample are unreliable. This is necessary as the CD-ROM/CD-I player performs its own error correction strategy on the data. The level of data integrity has to be much higher to ensure no errors occur in text or numerical information.

Specifications of CD-ROM and CD-I modes are available on request.

Motor speed control (see Fig. 10)

The motor speed control (MSC) output from pin 17 (24) is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

Track loss correction

The CD3A also incorporates a function to provide extra correction during track loss. Should track loss occur, the additional mute pin ($\overline{AM}$) should be taken LOW, which forces the data LOW at the pre-FIFO stage. This muted data is then corrected after de-interleaving. This function is particularly useful for applications where mechanical shock is likely to occur.

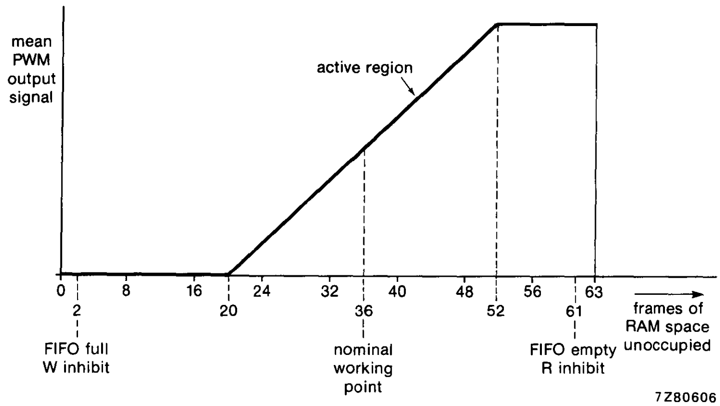


Fig. 10 Motor speed control.

CD2A replacement

The CD3A can become a direct replacement for the CD2A by externally connecting pin 21 to V_{DD} and modifying the PLL peripheral components (see Fig. 12).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage, pin 21 (28)	V_{DD}	–0,5	+ 6,5	V
Maximum input voltage	V_I	–0,5	V_{DD} + 0,5	V
Input current, pin 23 (30)	I_I	–	5	mA
Maximum output voltage MSC, QRA, SWAB/SSM	V_O	–0,5	+ 6,5	V
Output current (each output)	I_O	–	± 10	mA
DC V_{SS} or V_{DD} current	I_{DD} or I_{SS}	–	± 100	mA
DC input diode current	I_{IK}	–	± 20	mA
DC output diode current	I_{OK}	–	± 20	mA
Storage temperature range	T_{stg}	–55	+ 150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C
Electrostatic handling*	V_{es}	–1000	+ 1000	V

INTER·IC I²S SOUND

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

Detailed information on the I²S bus specification is available on request.

Supply of this Compact Disc IC does not convey an implied licence under any patent right to use this IC in any Compact Disc application.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage, pin 21 (28)		V_{DD}	4,5	5,0	5,5	V
Supply current, pin 21 (28)		I_{DD}	–	35	50	mA
Inputs						
D1 – D4, QCL, $\overline{AM}$, DEEM/$\overline{DINT1}$, DINT2						
Input voltage LOW	note 1	V_{IL}	–0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	note 2	I_{LI}	–10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
$\overline{MUTE}$, $\overline{CRI}$						
Input voltage LOW	note 1	V_{IL}	–0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance	V_I = 0 V	$\|Z_I\|$	18	50	110	kΩ
Input capacitance		C_I	–	–	10	pF
QRA, SWAB/SSM						
Input voltage LOW	note 1	V_{IL}	–0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance		C_I	–	–	10	pF
Internal pull-up impedance	V_I = 0 V	$\|Z_I\|$	3,9	10	18	kΩ
HFD						
Input voltage LOW		V_{IL}	–0,3	–	+ 0,8	V
Input voltage HIGH		V_{IH}	2,0	–	clamped	V
Input clamping voltage	I_I = 100 μA	V_{CL}	2,0	3,0	4,5	V
Input source current		I_S	–100	–	100	μA
Input capacitance		C_I	–	–	10	pF
Internall pull-up impedance	V_I = 0 V	$\|Z_I\|$	18	50	110	kΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs						
A0–A7, R/$\overline{W}$, D1–D4, $\overline{CAS}$, $\overline{RAS}$, QDATA, DEEM/$\overline{DINT1}$, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB, TEST1, TEST2, TEST3, TEST4						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD}	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	–10	–	+ 10	μA
MSC (open drain)						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	0	–	0,35	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	–10	–	+ 10	μA
SWAB/SSM, QRA (open drain)						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance		C_L	–	–	50	pF
Internal load resistance		R_L	3,9	10	18	kΩ
ANALOGUE CIRCUITS						
Data slicer (see Fig. 11)						
Input HFI						
AC input voltage range (peak-to-peak value)		$V_{I(p-p)}$	0,5	–	2,5	V
Input impedance						
normal (HFD HIGH)		$\|Z_I\|$	500	–	–	kΩ
disabled (HFD LOW)		$\|Z_I\|$	50	100	200	kΩ
Input capacitance		C_I	–	–	10	pF
Output FB						
Output current	V_{FB} = 2 V	I_O	$I_{ref}/5$ –20%	$I_{ref}/5$	$I_{ref}/5$ +20%	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase detector						
Output PD/OC	see Fig. 12					
Output current	PD/OC = 1 to 3 V	I_O	$\pm I_{ref}$–20%	$\pm I_{ref}$	$\pm I_{ref}$+20%	μA
Control range	note 3	α	±2,1	–	–	rad
Input I_{ref}	see Fig. 13					
Input reference current		I_{ref}	–	500	*	μA
Fine frequency detector						
Output PD/OC						
Output impedance		$\|Z_O\|$	2	4,1	5,6	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Coarse frequency detector						
Output PD/OC	note 4					
Output impedance		$\|Z_O\|$	1	2,3	3,2	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Voltage controlled oscillator						
Input PD/OC						
Oscillator constant		K_{osc}	–	3,5	–	MHz/V
Crystal oscillator	see Fig. 14					
Input XTAL1						
Output XTAL2						
Mutual conductance	100 kHz	G_m	1,5	–	–	ms
Small signal voltage gain	$G_v = G_m \times R_o$	G_v	3,5	–	–	V/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
Output capacitance		C_O	–	–	10	pF
Input leakage current	note 2	I_{LI}	–10	–	+ 10	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Slave clock mode	see Fig. 15					
Input voltage (peak-to-peak value)		$V_{I(p\text{-}p)}$	3,0	–	$V_{DD}+0,5$	V
Input voltage LOW	note 1	V_{IL}	–0,3	–	0,8	V
Input voltage HIGH	note 1	V_{IH}	2,4	–	$V_{DD}+0,5$	V
Input rise time	note 5	t_r	–	–	20	ns
Input fall time	note 5	t_f	–	–	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	–	55	%
TIMING						
Operating frequency (XTAL)		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)	PLL locked on to data	f_{VCO1}	2,54	4,3218	6,21	MHz
Operating frequency (VCO)	VCO absolute limits; PLL not locked on to data	f_{VCO2}	2	–	7,5	MHz
Outputs	Figs. 16 and 17					
CEFM	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
Output HIGH time		t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (I^2S format)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB						
Data set-up time		$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB						
Data hold time		$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (subcoding outputs)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
SDAB to SCAB						
Subcoding data set-up time		$t_{SU;SDAT}$	100	–	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
SCAB to SDAB						
Subcoding data hold time		$t_{HD; SDAT}$	100	–	–	ns
SWAB/SSM	note 6					
Output rise time		t_r	–	–	1	ns
Output fall time		t_f	–	–	100	ns
Output duty factor			–	50	–	%
Q-channel I/O	Figs 18 and 19					
QRA, QCL, QDATA						
Access time	note 7					
normal mode		$t_{ACC; N}$	0	–	13,3 + n x 13,3	ms
refresh mode		$t_{ACC; F}$	13,3	–	n x 13,3	ms
QCL to QRA						
acknowledge delay		t_{DACK}	–	–	500	ns
request hold time		$t_{HD; R}$	750	–	–	ns
QCL clock input LOW time		$t_{CK; LOW}$	750	–	–	ns
QCL clock input HIGH time		$t_{CK; HIGH}$	750	–	–	ns
QCL to QDATA delay time		t_{DD}	–	–	750	ns
Data hold time before new frame is accessed		$t_{HD; ACC}$	2,3	–	–	ms
Acknowledge time		t_{ACK}	–	–	10,8	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{LI(min)}$ and $I_{LO(min)}$ measured at $V_I = 0$ V; $I_{LI(max)}$ and $I_{LO(max)}$ measured at $V_I = V_{DD}$.
3. 1 rad = $\frac{180^o}{(3,14)}$.
4. Coarse frequency detector output PD/OC active for VCO frequencies $> \frac{f_{XTAL}}{2}$ and $< \frac{f_{XTAL}}{4}$.
5. Reference levels = 0,5 V and 2,5 V.
6. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
7. Q-channel access times dependent on cyclic redundancy check (CRC); n = number of cycles until CRC is 'good'.

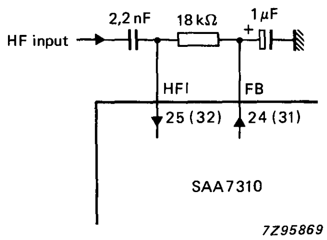


Fig. 11 Data slicer HFI input.

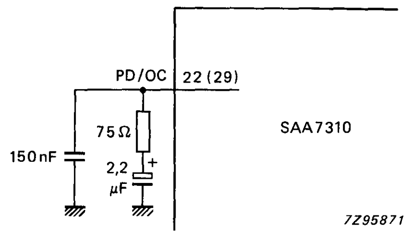


Fig. 12 PLL circuit.

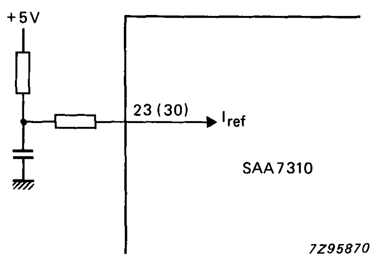


Fig. 13 I_{ref} circuit.

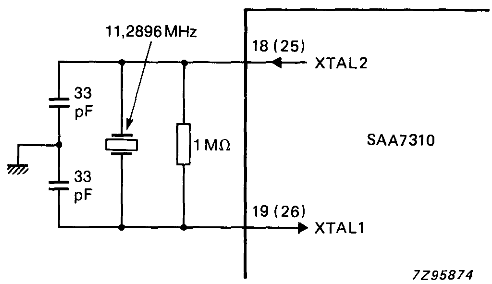


Fig. 14 Crystal oscillator circuit; using crystal type: 4322 143 05031.

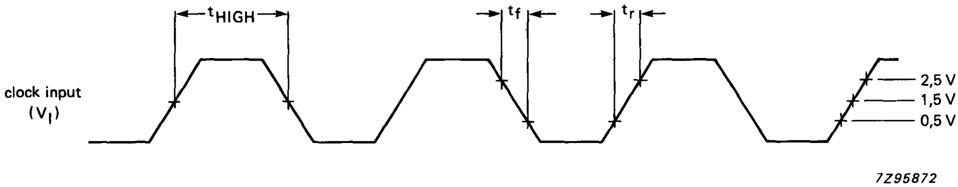


Fig. 15 Input clock timing diagram; reference levels 0,5 V, 1,5 V and 2,5 V.

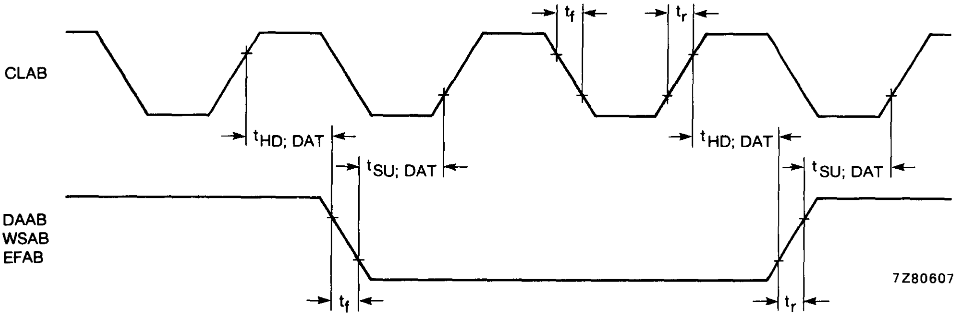


Fig. 16 Typical I²S data output waveforms; reference levels = 0,8 V and 2,0 V.

DEVELOPMENT DATA

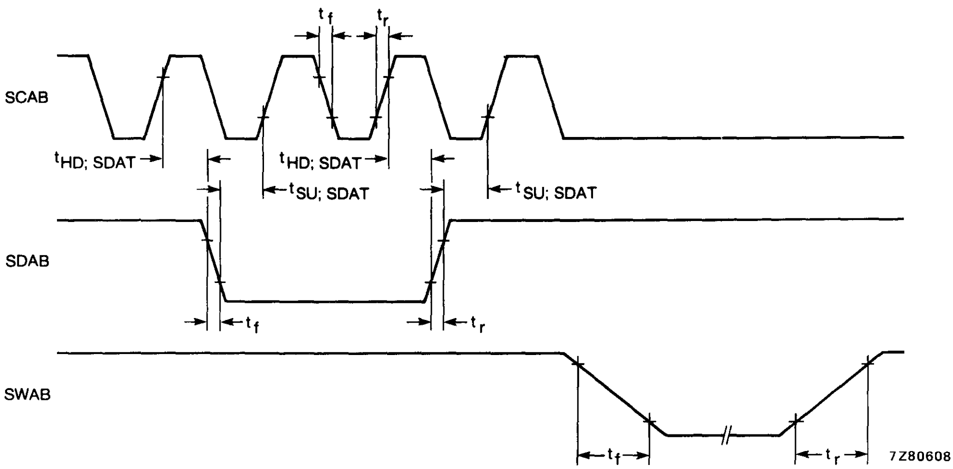


Fig. 17 Typical subcoding data output waveforms; reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

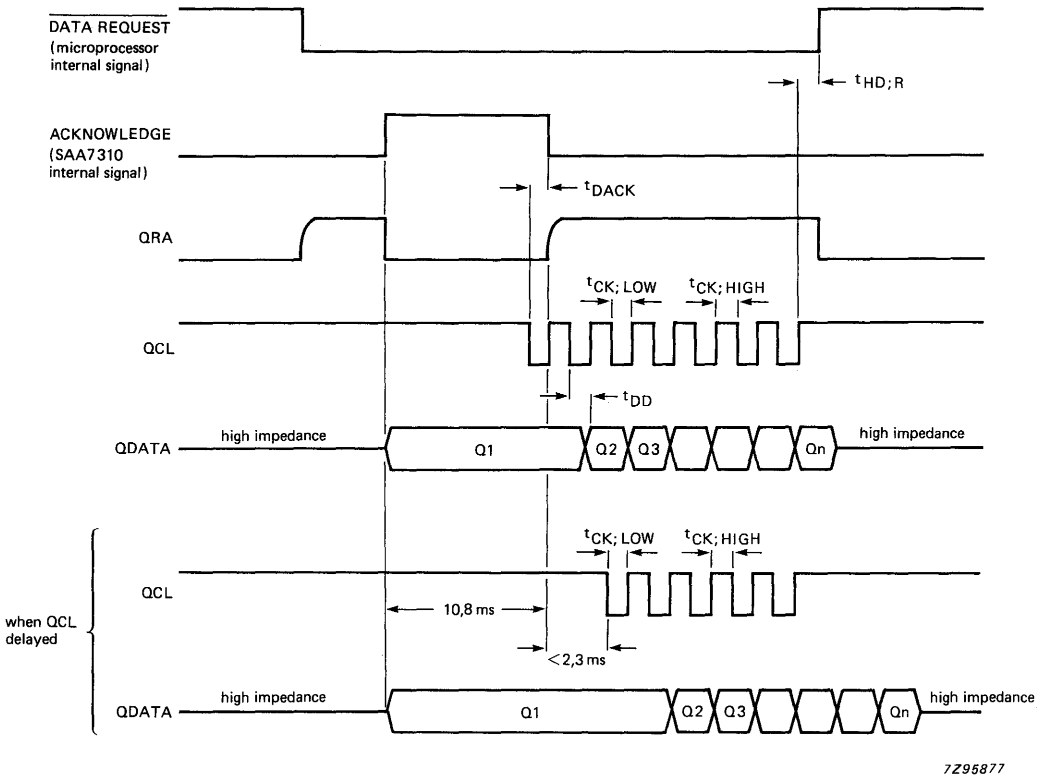


Fig. 18 Q-channel timing waveforms (normal mode).

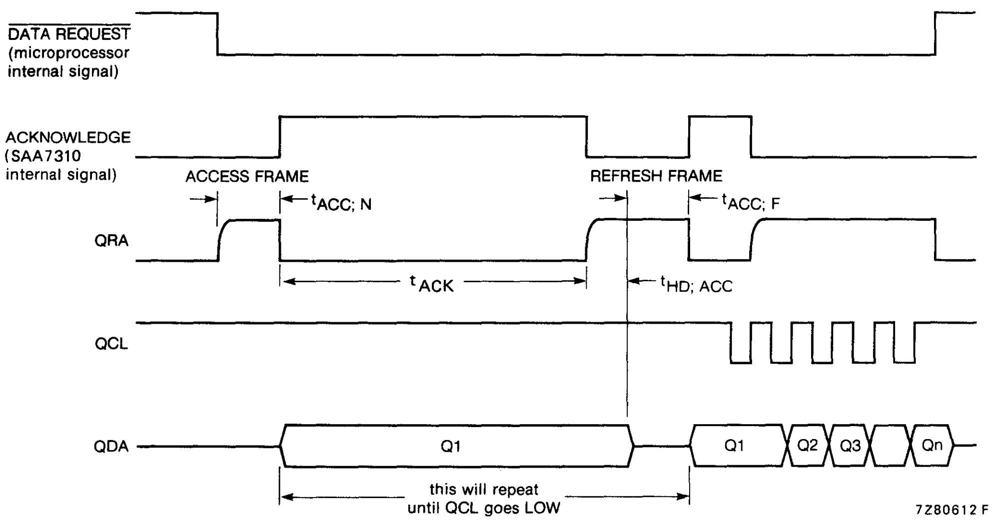


Fig. 19 Q-channel timing waveforms (refresh mode).

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a DC free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the DC content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 20).

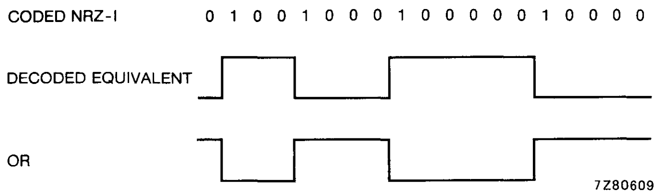


Fig. 20 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

APPLICATION INFORMATION (continued)

Table 2 EFM code conversion

No.	DNZ data symbol	equivalent code word	No.	DNZ data symbol	equivalent code word
	D1 D8	C1 C14		D1 D8	C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11			139		
to			to		
119			247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

Subcoding microprocessor handshaking protocol (see Figs. 18, 19 and 21)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7310.

The SAA7310 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7310 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7310 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowlegde signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7310 now disabled the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7310 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7310 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

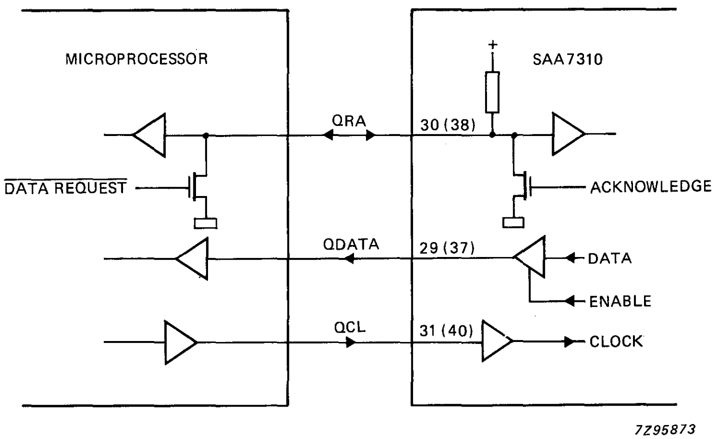


Fig. 21 Microprocessor handshaking protocol.

STEREO CMOS DAC FOR COMPACT DISC DIGITAL AUDIO SYSTEMS

GENERAL DESCRIPTION

The SAA7320 (DAC3) is a complete monolithic stereo CMOS 16-bit input digital-to-analogue converter designed for application in low/mid-cost portable compact disc systems.

Features

- I^2S data input
- 3-stage digital filter incorporating F.I.R. filter, linear interpolator and sample and hold
- 2nd order noise shaper to provide a signal-to-noise ratio of > 90 dB
- 16-bit resolution from a 1-bit converter, using switched capacitor integrator
- 3rd order low-pass filter to reduce out-of-band noise
- −12 dB attenuation, de-emphasis and mute control
- Low power consumption (typ. 300 mW)
- Single supply operation (+ 5 V)
- −40 to + 85 °C operating temperature range

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (analogue)		V_{DDA}	4,5	5,0	5,5	V
Supply current (analogue)		I_{DDA}	–	20	*	mA
Supply voltage (digital)		V_{DD}	4,5	5,0	5,5	V
Supply current (digital)		I_{DD}	–	40	*	mA
Signal-to-noise ratio at the analogue outputs	0 dB input	S/N	–	90	–	dB
Input voltage ranges WSI, CLI, DAI, DEC, $\overline{ATT}$						
Input voltage LOW	note 6	V_{IL}	0	–	+ 0,8	V
Input voltage HIGH	note 6	V_{IH}	2,0	–	V_{DD}+ 0,5	V
Output voltage ranges WSO, CLO, DAO, XSYS,						
Output voltage LOW	note 6	V_{OL}	0	–	+ 0,4	V
Output voltage HIGH	note 6	V_{OH}	2,4	–	V_{DD}+ 0,5	V
Operating frequency XTAL		f_{XTAL}	8,0	11,2896	12,3	MHz
Operating ambient temperature range		T_{amb}	−40	–	+ 85	°C

* Value to be fixed.

For explanation of notes see "Notes to the characteristics".

PACKAGE OUTLINE

SAA7320GP: 44-lead QFP; plastic (SOT205A).

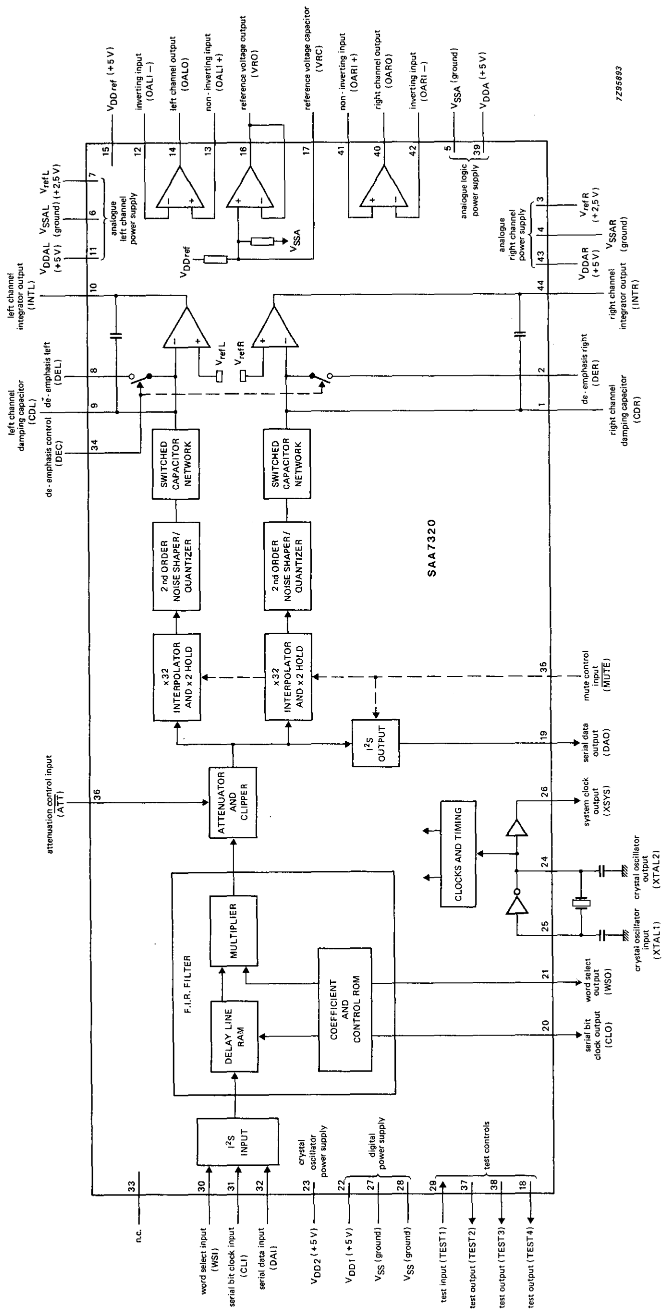


Fig. 1 Block diagram.

PINNING

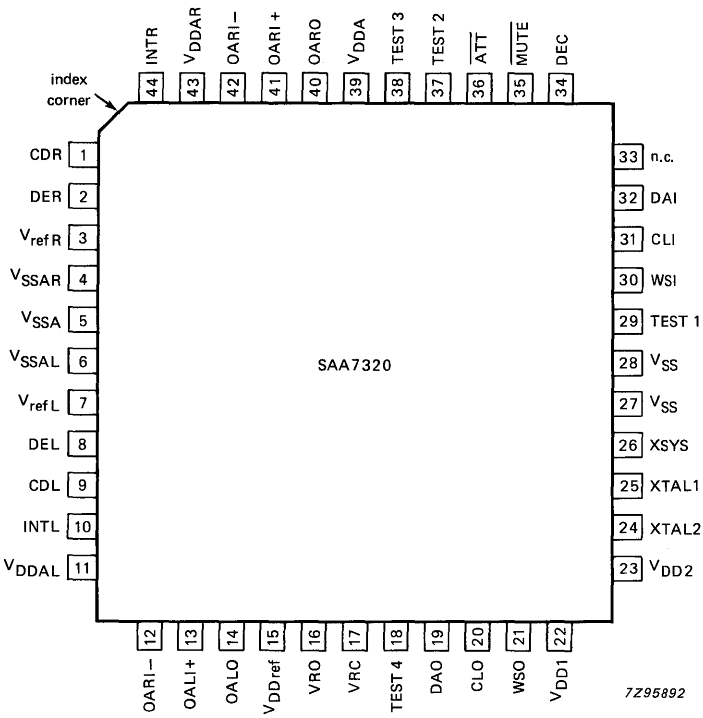


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Pin functions

pin no.	mnemonic	description
1	CDR	**Capacitor Damping Right**: damping capacitor for the right channel switched-capacitor integrator.
2	DER	**De-emphasis Right:** connection to the de-emphasis switch in the feedback of the right channel integrator.
3	V_{refR}	**Reference voltage Right:** reference voltage input for the analogue right channel ground (+ 2,5 V typ.).
4	V_{SSAR}	**Ground**: ground connection for the analogue right channel.
5	V_{SSA}	**Ground**: ground connection for logic in the analogue section.
6	V_{SSAL}	**Ground**: ground connection for the analogue left channel.
7	V_{refL}	**Reference voltage Left:** reference voltage input for the analogue left channel ground (+ 2,5 V typ.).
8	DEL	**De-emphasis Left:** connection to the de-emphasis switch in the feedback of the left channel integrator.
9	CDL	**Capacitor Damping Left:** damping capacitor for the left channel switched-capacitor integrator.
10	INTL	**Integrator Left**: output from the left channel switched-capacitor integrator.
11	V_{DDAL}	**Power Supply:** + 5 V supply voltage for the analogue left channel.
12	OALI−	**Operational Amplifier Left Input −**: inverting input to the left channel low-pass filter operational amplifier.
13	OALI+	**Operational Amplifier Left Input** +: non-inverting input to the left channel low-pass filter operational amplifier.
14	OALO	**Operational Amplifier Left Output:** output from the left channel operational amplifier.
15	V_{DDref}	**Power Supply:** +5 V supply voltage for the reference voltage generator.
16	VRO	**Reference Voltage Output**: internal reference voltage output (+ 2,5 V typ.).
17	VRC	**Reference Voltage Capacitor**: internal reference voltage high impedance node requiring an external smoothing capacitor.
18	TEST4	**Test output 4:** pin should be left open-circuit.
19	DAO	**I^2S Serial Data Output**: is a 16-bit linear two's-complement PCM signal at a data rate of 176,4 kHz (typ.) formatted in accordance with I^2S. After 4 x upsampling by the digital filter this signal is output so that an external DAC could be used; combined with CLO and WSO it can be considered as a master transmitter.
20	CLO	**I^2S Serial bit Clock Output:** f_{CLO} = 5,6448 MHz typ.
21	WSO	**I^2S Word Select Output**: 176,4 kHz typ.
22	V_{DD1}	**Power supply**: + 5 V supply voltage for the digital section.
23	V_{DD2}	**Power Supply**: + 5 V supply voltage for the crystal oscillator.
24	XTAL2	**Crystal oscillator output:** drive output to clock crystal.
25	XTAL1	**Crystal oscillator input:** input from crystal oscillator or external clock input (11,2896 MHz typ.).
26	XSYS	**System clock output**: buffered output from crystal oscillator
27, 28	V_{SS}	**Ground**: ground connection for the digital section.

pin no.	mnemonic	description
29	TEST1	**Test input 1:** pin should be connected to ground.
30	WSI	**I^2S Word Select Input:** 44,1 kHz typ. WSI together with CLI, is used to clock the I^2S serial data input (DAI) and synchronize the main timing chain.
31	CLI	**I^2S Serial bit Clock Input:** f_{CLI} = 2,8224 MHz typ.
32	DAI	**I^2S Serial Data Input:** is a 16-bit linear two's-complement PCM signal formatted in accordance with I^2S. If more than 16 bits are supplied then the least significant bits (LSBs) will be truncated.
33	n.c.	**not connected.**
34	DEC	**De-emphasis Control:** this input switches an extra external capacitor network into both the analogue left and right channel integrator feedback.
35	$\overline{\text{MUTE}}$	**Mute:** when active LOW this Schmitt trigger control input will force the interpolator data input to zero. It will also force the I^2S data output (DAO) to zero.
36	$\overline{\text{ATT}}$	**Attenuation:** when active LOW this control input provides −12 dB attenuation to the analogue output amplitude.
37	TEST2	**Test output 2:** pin should be left open-circuit.
38	TEST 3	**Test output 3:** pin should be left open-circuit.
39	V_{DDA}	**Power Supply:** + 5 V supply voltage for logic in the analogue section.
40	OARO	**Operational Amplifier Right Output:** output from the right channel operational amplifier.
41	OARI+	**Operational Amplifier Right Input +:** non-inverting input to the right channel low-pass filter operational amplifier.
42	OARI−	**Operational Amplifier Right Input −:** inverting input to the right channel low-pass filter operational amplifier.
43	V_{DDAR}	**Power Supply:** + 5 V supply voltage for the analogue right channel.
44	INTR	**Integrator Right:** output from the right channel switched-capacitor integrator.

FUNCTIONAL DESCRIPTION

General

The SAA7320 CMOS DAC heavily oversamples to several MHz (256 x the sampling frequency, fs), so that the band-limiting filters required for waveform smoothing and out-of-band noise reduction are mainly digital. In addition to the digital filters the circuit contains active components for analogue post filtering. In most applications very few external components are required. An output after the 4 x upsampling filter allows the circuit to be used as an interface between the decoder and external DAC in high-performance compact disc systems. The SAA7320 requires only one + 5 V supply; the required reference voltage is generated internally.
Separate supply pins for each of the 1-bit DACs achieves high performance signal-to-noise ratio and channel separation.
There is no phase delay between the two analogue outputs despite the fact that the upsampling filter structure is multiplexed between the two data channels.

Oversampling digital filter

This is a 3-stage digital filter.

- The first stage provides 4 x oversampling to 176,4 kHz using a 128-tap F.I.R. low pass filter. Data is stored in a cyclic RAM, the filter coefficients in a ROM and the convolutions are performed using an array multiplier.
- The second stage is a 32 x oversampling linear interpolator.
- The third stage provides 2 x upsampling using a sample and hold, giving a total of 256 x upsampling (11,2896 MHz).

The first stage oversamples to 176,4 kHz with a band-pass ripple of ± 0,035 dB and a stop-band attenuation of –60 dB above 24,2 kHz. It also contains frequency response compensation for the interpolator/analogue post-filtering roll-off and coefficient scaling to prevent overflow in the noise shaper.

The characteristics of the F.I.R. filter are shown in Fig. 8.

Switched-capacitor DAC

The digital-to-analogue conversion is achieved with a 1-bit DAC oversampled to 256 fs with second-order noise shaping performed digitally to give a 1-bit Pulse Density Modulated (PDM) code with a signal-to-noise ratio of > 90 dB. Integral with the actual 1-bit converter is a first-order low-pass filtering action which reduces the total HF noise power.

A switched capacitor technique is used for the 1-bit DAC which converts the PDM stream to an analogue signal with a signal-to-noise ratio of > 90 dB. A fixed charge is either added or substracted from the virtual earth node of a first-order filter. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure. The output slew rate of this filter is chosen so that the operational amplifier always remains within its high gain linear region.

An internally generated out-of-band dither signal is used to suppress audible idling patterns in the noise shaper at low signal levels. This signal is injected digitally into the x 32 upsampling interpolator at a frequency 352 kHz and a level of –20 dB.

FUNCTIONAL DESCRIPTION (continued)

Attenuation

Attenuation is controlled by the $\overline{ATT}$ input at pin 36. This input will allow an attenuation of the analogue output amplitude by −12 dB during track search.

De-emphasis and low-pass filter

Extra on-chip analogue circuitry provides post filtering:

- Input DEC (pin 34) switches an extra external capacitor network into both the left and right channel analogue integrator feedback to control roll-off.
  Output from the right channel switched-capacitor integrator (INTR) is available at pin 44. Output from the left channel switched-capacitor integrator (INTL) is available at pin 10.
- A low-pass filter, for further attenuation of out-of-band noise, can be constructed using the internal CMOS operational amplifiers. The digital filter contains compensation for a third-order Butterworth filter with a −3 dB cut-off at 60 kHz.

I^2S serial interface

The SAA7230 has two I^2S ports incorporated; DAI (pin 32) and DAO (pin 19).

- DAI receives data from the Compact Disc decoder IC (or any 16-bit 44,1 kHz I^2S source).
- DAO transmits the 4 x oversampled data to an external DAC.

The 'slave' receiver requires a serial bit clock input (CLI; pin 31) and a word select input (WSI; pin 30). To ensure that the filter is 'in-phase' with the input, the main timing chain is automatically synchronized to the incoming word select signal. The frequency of the data must also be synchronized to the filter by:

- the source supplying the 11,2896 MHz system clock via crystal oscillator input (XTAL1; pin 25).

or

- SAA7320 supplying the system clock to the source via XSYS (pin 26).

The SAA7320 will use only the 16 most significant bits of input data even though the I^2S format allows a variable word length (see Fig. 4).

The 'master' transmitter supplies bit clock, word select and data signals at twice the frequency of the receiver to allow for the 4 x upsampling. Therefore all 16 bit positions are used.

Conversion path

The SAA7320 data conversion path is shown in Fig. 3. As both paths are identical only one path is shown. The data flow is in a serial format up to the linear interpolator stage and then separated into two channels.

CD3A application

A system application diagram of the CD3A with the DAC3 is shown in Fig. 9.

Detailed information on the I^2C bus specification is available on request.

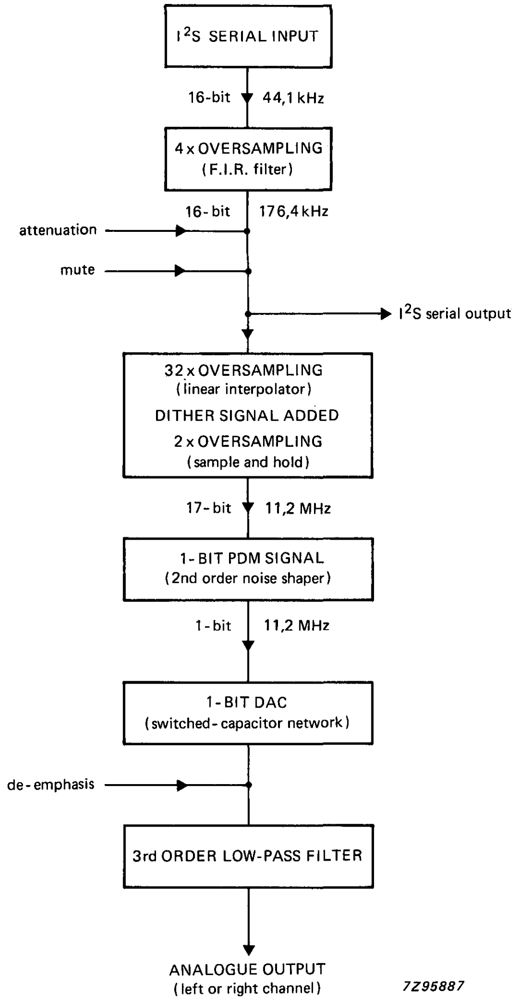


Fig. 3 Flow diagram of SAA7320 data conversion path (one channel).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage*	V_{DDA}	–0,5	+ 6,5	V
DC input voltage	V_I	–0,5	V_{DD}+ 0,5	V
DC input diode current	I_{IK}	–	± 20	mA
DC output voltage	V_O	–0,5	V_{DD}+ 0,5	V
DC output source or sink current	I_O	–	± 25	mA
DC V_{DD} or V_{SS} current (total)	I_{DD} or I_{SS}	–	± 0,5	A
Storage temperature range	T_{stg}	–65	+ 150	°C
Operating ambient temperature range	T_{amb}	–40	+ 85	°C
Electrostatic handling**	V_{es}	–1000	+ 1000	V

DEVELOPMENT DATA

* All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.

** Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (analogue)		V_{DDA}	4,5	5,0	5,5	V
Supply current (analogue)		I_{DDA}	–	20	*	mA
Supply voltage (digital)		V_{DD}	4,5	5,0	5,5	V
Supply current (digital)		I_{DD}	–	40	*	mA
ANALOGUE PART						
Reference voltage source						
VRO; VRC						
High impedance reference voltage level		V_{refC}	$0,45V_{DD}$	$0,5V_{DD}$	$0,55V_{DD}$	V
Output reference voltage relative to VRC		ΔV_{refO}	–10	0	+ 10	mV
Reference voltage output impedance		$\|Z_{refO}\|$	–	2	4	Ω
Reference voltage inputs						
V_{refL}; V_{refR}	note 1					
Reference input voltage		V_{ref}	$0,45V_{DD}$	$0,5V_{DD}$	$0,55V_{DD}$	V
Outputs						
INTL; INTR						
Output level (RMS value)	note 2; fs = 44,1 kHz	$V_{AO(rms)}$	–	–	1,0	V
Output dynamic impedance		Z_{AO}	–	100	200	Ω
Output load resistance	to V_{ref}	R_L	10	–	–	kΩ
Output load capacitance	to V_{ref}	C_L	–	–	+ 20	pF
Output DC level	to V_{ref}	V_{AODC}	–20	–	+ 20	mV

* Value to be fixed.

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Filter characteristics	note 3					
Signal spectrum (0 dB = F.S.D. input)						
$<$ 20 kHz		SS	−0,035	—	+ 0,035	dB
$>$ 24,1 kHz		SS	−60	—	—	dB
Signal-to-noise ratio						
0 dB input		S/N	90	—	—	dB
−10 dB input		S/N	83	—	—	dB
Total harmonic distortion	at 0 dB/1 kHz	THD	—	—	−90	dB
Digital silence	Mute LOW		*	−96	—	dB
Channel separation	at 1 kHz	α	*	80	—	dB
Power supply rejection ratio to V_{DD}		PSRR	*	60	—	dB
Operational amplifiers						
Open loop gain		G_{ol}	*	85	*	dB
Output impedance		$\|Z_O\|$	—	100	150	Ω
Input offset voltage		V_{Ios}	−10	—	+ 10	mV
Signal-to-noise ratio (20 Hz to 20 kHz)	note 4	S/N	+ 95	—	—	dB
Total harmonic distortion (20 Hz to 20 kHz)	note 5	THD	—	—	−94	dB
Unity gain bandwidth		G_{BW}	5	10	—	MHz
Output load to V_{ref}						
capacitive		C_L	—	—	200	pF
resistive		R_L	3	—	—	kΩ
DIGITAL PART						
Inputs						
WSI, CLI, DAI, DEC, $\overline{ATT}$						
Input voltage LOW	note 6	V_{IL}	−0,5	—	+ 0,8	V
Input voltage HIGH	note 6	V_{IH}	2,0	—	V_{DD}+0,5	V
Input leakage current	note 7	I_{LI}	−10	0	+ 10	μA
Input capacitance		C_I	—	—	10	pF

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{MUTE}}$ (Schmitt trigger)						
Switching voltage threshold						
rising		V_{thr}	$0{,}54V_{DD}$	$0{,}6V_{DD}$	$0{,}66V_{DD}$	V
falling		V_{thf}	$0{,}36V_{DD}$	$0{,}4V_{DD}$	$0{,}44V_{DD}$	V
Input leakage current	note 7	I_{LI}	−10	0	+ 10	μA
Input capacitance		C_I	–	–	10	pF
Crystal oscillator input						
External clock only XTAL1						
Input voltage LOW	note 6	V_{IL}	−0,5	–	1,5	V
Input voltage HIGH	note 6	V_{IH}	3,5	–	V_{DD} to 5 V	V
Input leakage current	note 7	I_{LI}	−10	0	+ 10	μA
Input capacitance		C_I	–	–	10	pF
Outputs						
DAO, CLO, WSO, XSYS						
Output voltage LOW	note 6; $-I_{OL} = 400\ \mu A$	V_{OL}	−0,5	–	+ 0,4	V
Output voltage HIGH	note 6; $I_{OH} = 20\ \mu A$	V_{OH}	2,4	–	V_{DD}+ 0,5	V
Load capacitance		C_L	–	–	35	pF
Crystal oscillator	see Fig. 7					
Input XTAL1						
Output XTAL2						
Operating frequency XTAL		f_{XTAL}	8,0	11,2896	12,3	MHz
Mutual conductance	100 kHz	G_m	1,5	–	–	mA/V
Small signal voltage gain	$G_v = G_m \times R_O$	G_v	3,5	–	–	V/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
Output capacitance		C_O	–	–	10	pF
Input leakage current	note 7	I_{LI}	−10	–	+ 10	μA

parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
External clock input						
XTAL1						
Input frequency (fs x 256)		f_C	8,0	11,2896	12,3	MHz
Input rise time	note 8	t_r	–	–	20	ns
Input fall time	note 8	t_f	–	–	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	–	55	%
System clock output						
XSYS	note 9					
Output rise time	note 8	t_r	–	–	20	ns
Output fall time	note 8	t_f	–	–	20	ns
Output HIGH time (relative to clock period)	at 1,5 V note 10	t_{HIGH}	45	–	55	%
I^2S TIMING						
Receiver	see Fig. 5					
Clock input CLI						
Input clock period		t_{CK}	320	354	1000	ns
Input HIGH time		t_{CKH}	112	–	–	ns
Input LOW time		t_{CKL}	112	–	–	ns
Data inputs WSI, DAI						
Data set-up time		$t_{SU; DAT}$	40	–	–	ns
Data hold time		$t_{HD; DAT}$	0	–	–	ns

DEVELOPMENT DATA

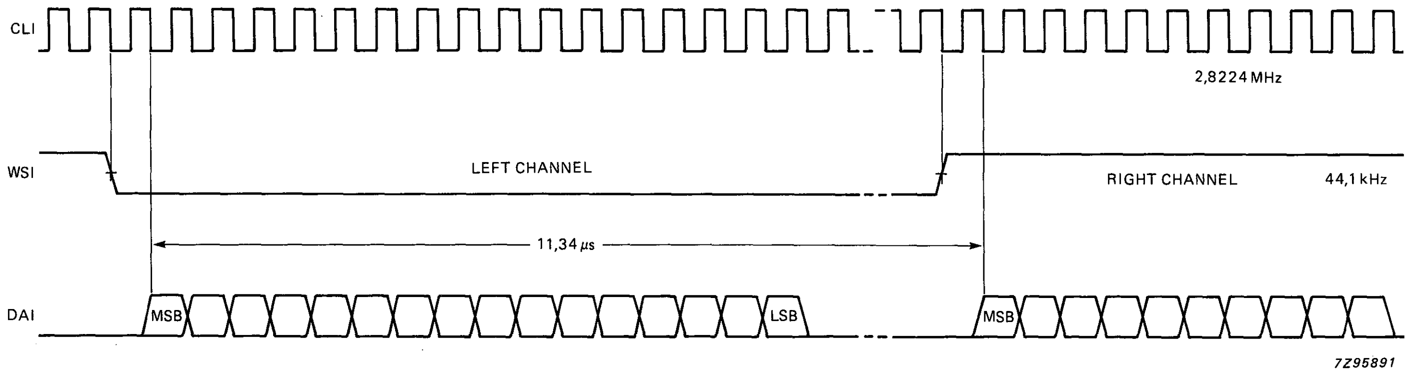
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Transmitter	see Fig. 6					
Clock output CLO						
Output clock period		t_{CK}	–	$2/f_C$	–	ns
Output HIGH time		t_{CKH}	60	–	–	ns
Output LOW time		t_{CKL}	60	–	–	ns
Data WSO						
Data set-up time		$t_{SU;\,DATWS}$	40	–	–	ns
Data hold time		$t_{HD;\,DATWS}$	40	–	–	ns
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
Data output DAO						
Data set-up time		$t_{SU;\,DATD}$	40	–	–	ns
Data hold time		$t_{HD;\,DATD}$	40	–	–	ns
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns

Notes to the characteristics

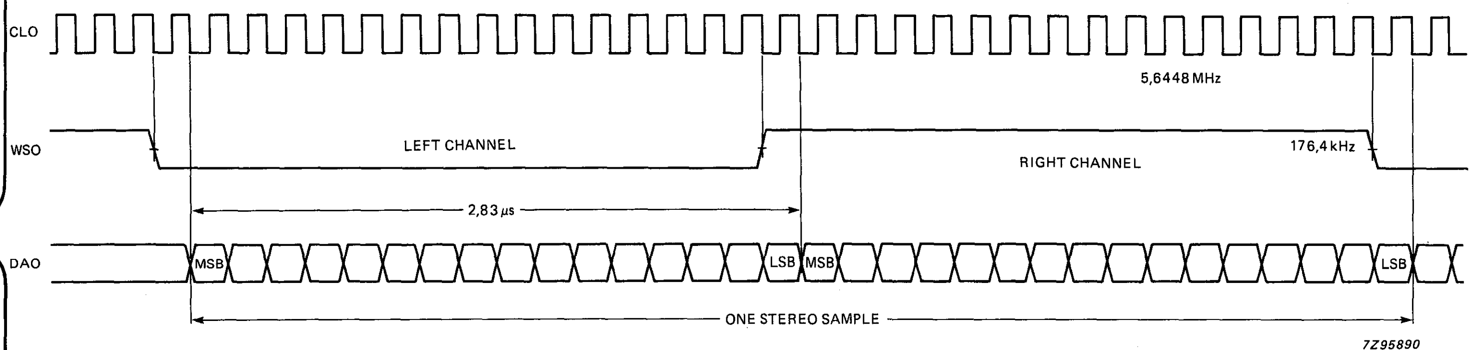
1. Any noise at these inputs is transferred directly to the analogue outputs.
2. Output levels depend on integrator components. Value shown is for maximum digital code.
3. The filter characteristics apply to the complete system at a sampling rate (fs) of 44,1 kHz.
4. Value relative to 1 $V_{(rms)}$, with unity gain.
5. Unity gain output = 1 $V_{(rms)}$.
6. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
7. $I_{LI(min)}$ and $I_{LO(min)}$ measured at V_I = 0 V; $I_{LI(max)}$ and $I_{LO(max)}$ measured at $V_I = V_{DD}$.
8. Reference levels = 0,8 V and 2,0 V.
9. Output times are measured with a capacitive load of 35 pF.
10. t_{HIGH} valid only when used with XTAL.

DEVELOPMENT DATA



(a)

Fig. 4(a) Typical I^{2}S data input waveforms at 2,8 MHz.



(b)

Fig. 4(b) Typical I^{2}S data output waveforms at 5,6 MHz.

TIMING

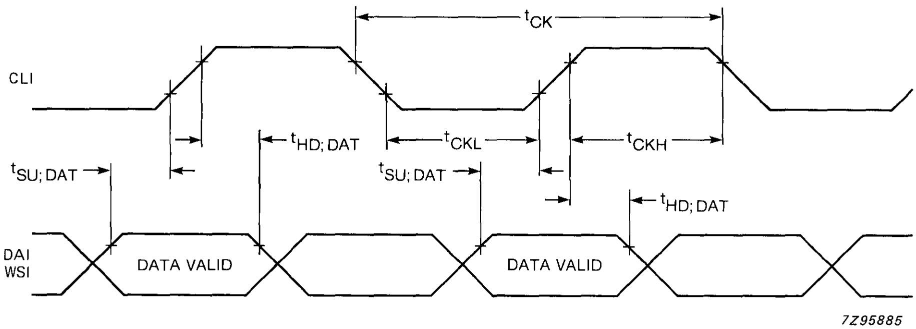


Fig. 5 Data input timing with respect to I^2S serial bit clock input (CLI); reference levels = 0,8 V and 2,0 V.

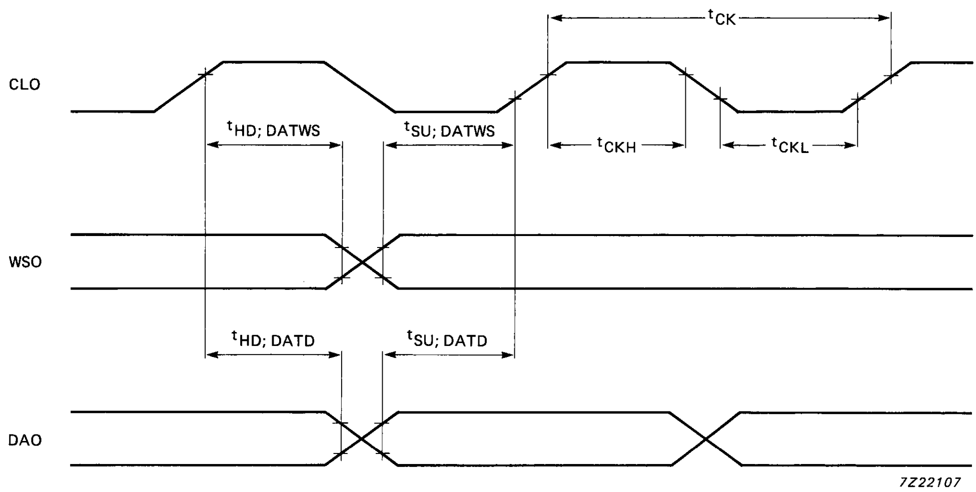


Fig. 6 Data output timing with respect to clock output (CLO); reference levels = 0,8 V and 2,0 V.

DEVELOPMENT DATA

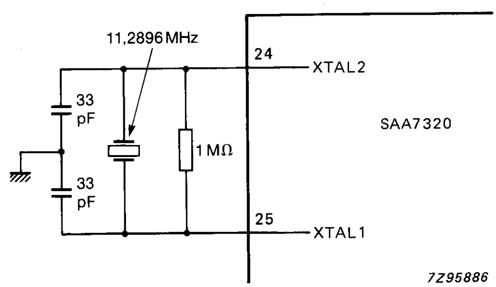


Fig. 7 Crystal oscillator circuit using crystal type: 4322 143 05031.

APPLICATION INFORMATION

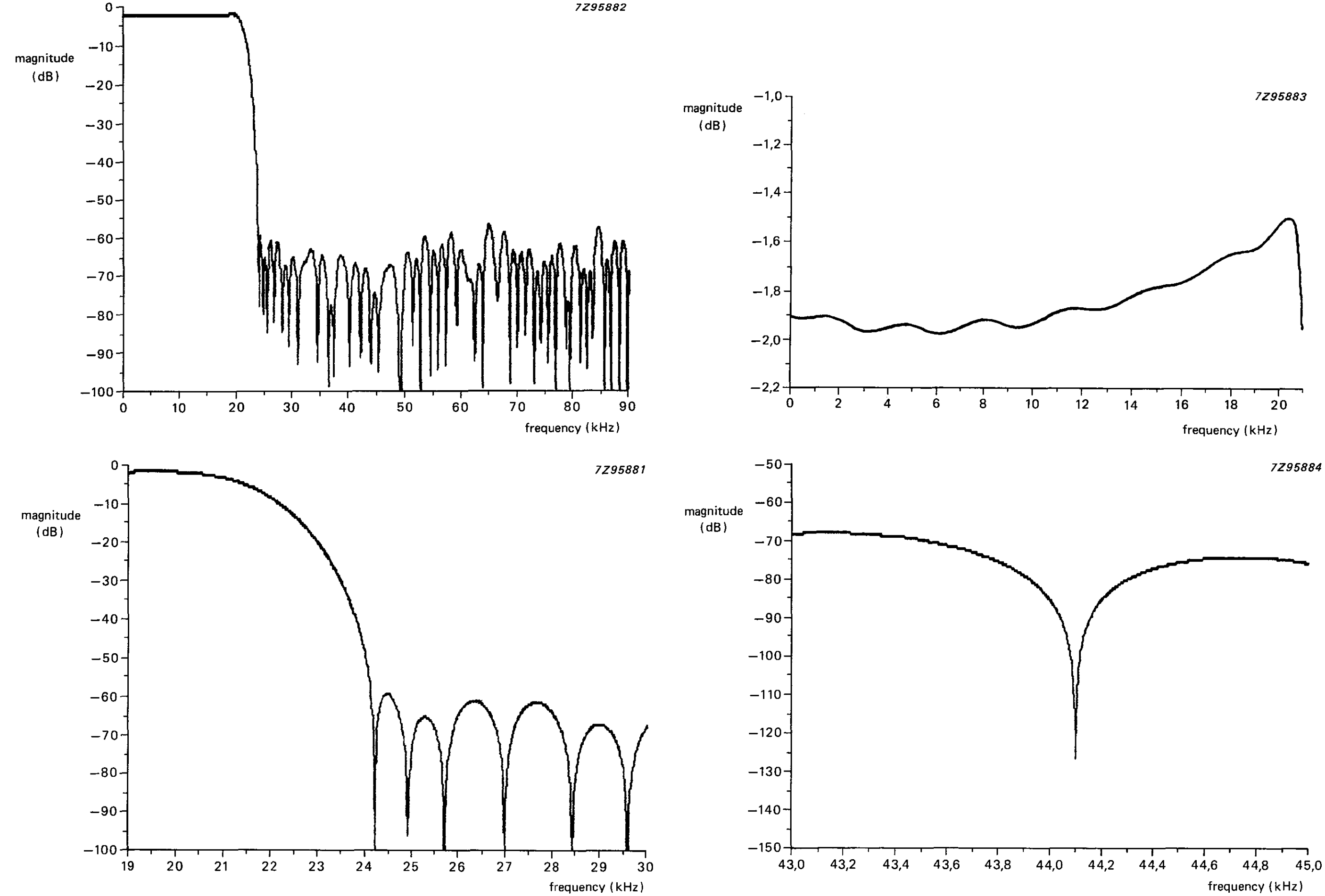
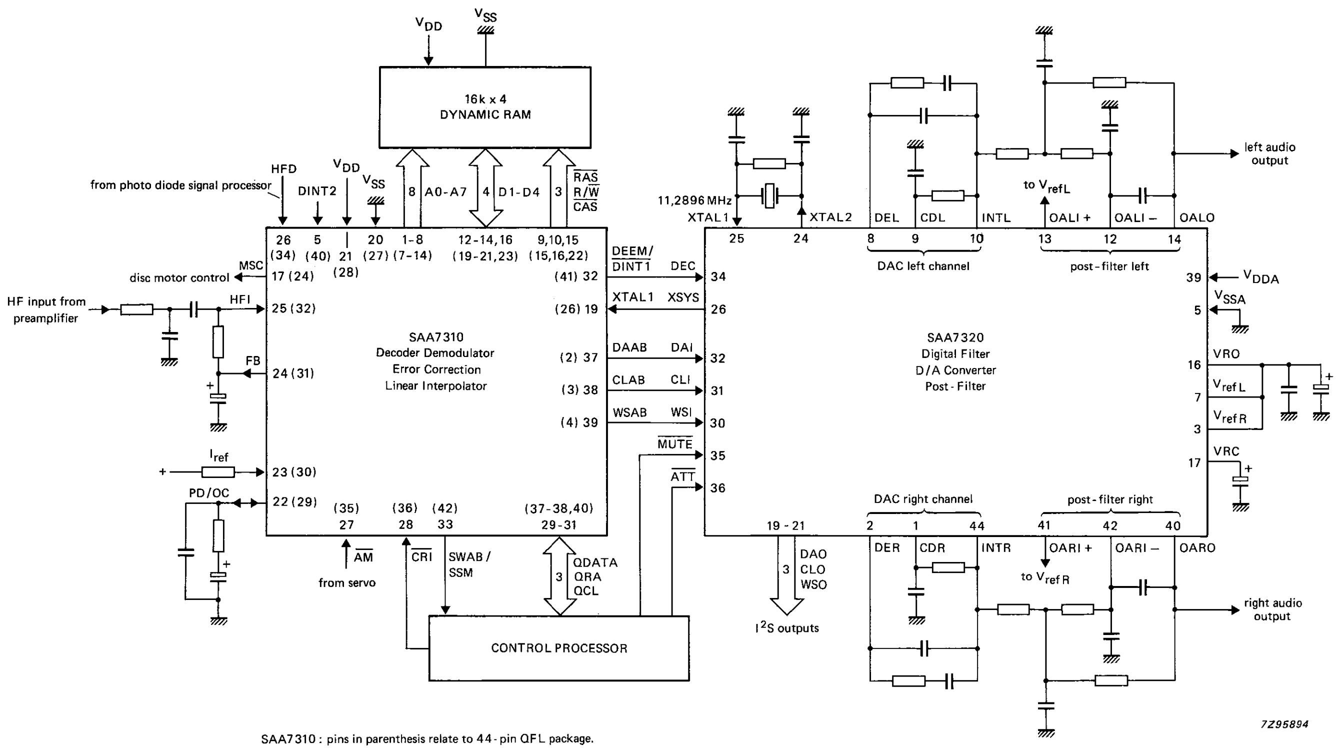


Fig. 8 Digital filter characteristics; magnitude as a function of frequency.



SAA7310 : pins in parenthesis relate to 44-pin QFL package.

Fig. 9 System application diagram; CD3A with the DAC3.

TIME BASE CORRECTION DELAY LINE (TBC)

GENERAL DESCRIPTION

The SAD7630 is a charge-coupled device (CCD) dual variable delay line. It is designed for fault correction of composite video signals in compact disc video (CDV) applications. One line can be used to correct the time error of the composite video signal and the other line to correct the time error of the analogue audio carriers.

Features

- Variable clock frequency range of 13 to 24 MHz
- Separate power supply (V_{DDA} and V_{DDD}) to prevent interference between digital and analogue circuits
- Applicable for either PAL or NTSC players

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
analogue		V_{DDA}	4.75	5.0	5.5	V
digital		V_{DDD}	4.75	5.0	5.5	V
substrate bias		$-V_{SB}$	3.5	3.0	2.5	V
Supply current range	$I_I = 0$ mA; $f_{CLK} = 16.6$ MHz					
analogue		I_{DDA}	1	2	4	mA
digital		I_{DDD}	8	12	16	mA
substrate bias		$\|I_{SB}\|$	–	–	100	μA
Inputs						
V_{ref1}; V_{ref2}						
DC input voltage		V_{ref}	0	–	1.5	V
Input current level		I_{ref}	–	–	10	μA
V_{I1}; V_{I2}						
Signal amplitude	$V_I = V_{ref}$	V_I	0	1	1.6	V
Outputs						
V_{O1}; V_{O2}	R_{FZ} to $V_{SB} = 47$ kΩ					
DC output voltage	V_I to $V_{ref} = 0$ V	V_O	0.25	0.5	0.75	V
Operating ambient temperature range		T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38D).

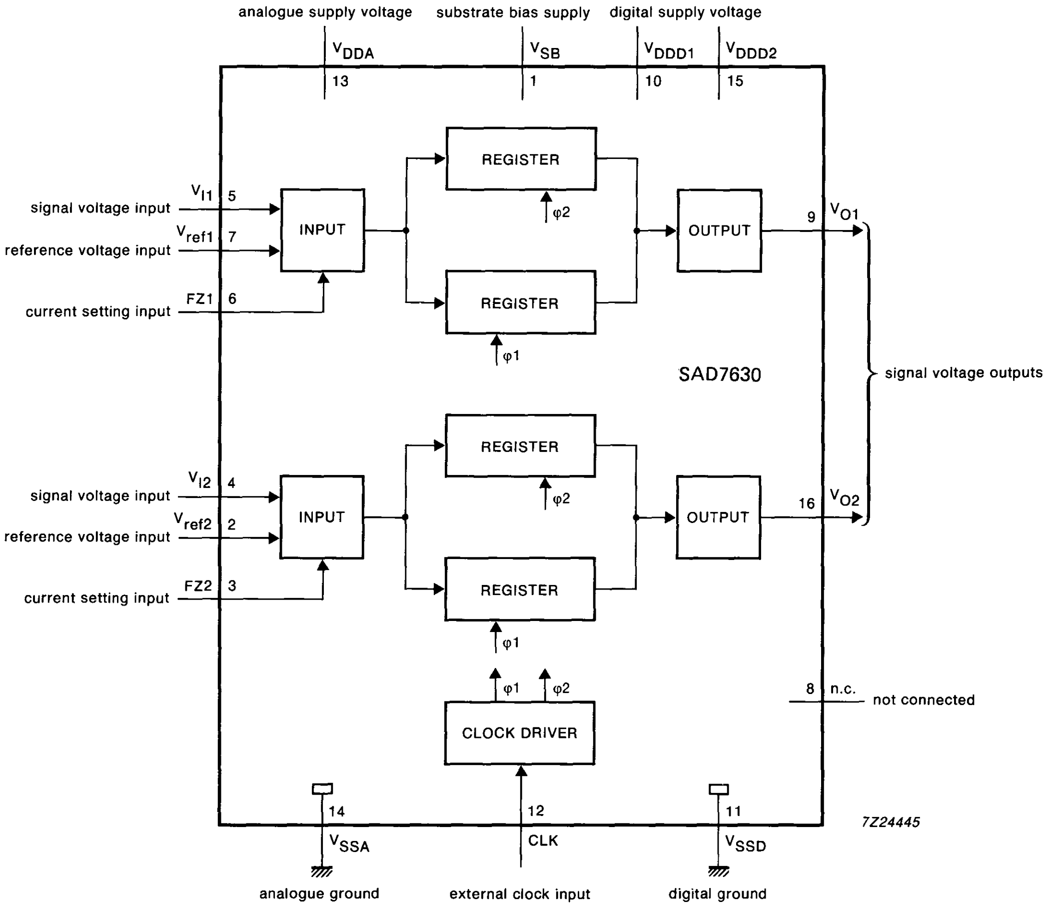


Fig.1 Block diagram.

PINNING

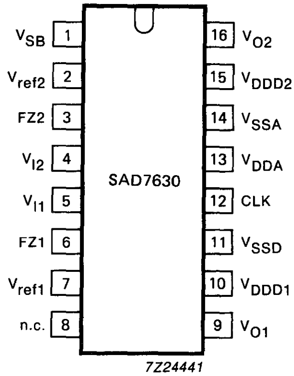


Fig.2 Pinning diagram.

Power supply

V_{DDA}	analogue supply voltage
V_{SSA}	analogue ground
V_{DDD1}, V_{DDD2}	digital supply voltage
V_{SSD}	digital ground
V_{SB}	substrate bias supply

Input

CLK	external clock input

Inputs (analogue)

V_{ref1}, V_{ref2}	reference voltage inputs
V_{I1}, V_{I2}	signal voltage inputs
FZ1, FZ2	input stage current setting inputs

Outputs (analogue)

V_{O1}, V_{O2}	signal voltage outputs

FUNCTIONAL DESCRIPTION

Principle of variable delay

The input signal is sampled by clock pulses. At each pulse the samples are shifted one step in a 526 stage register. Two parallel multiplexed registers form one delay line. Each register is clocked by two clock pulses $\varphi1$ and $\varphi2$ which have a phase difference of 180°.

Effectively the two parallel multiplexed registers operate as a 1052 stage single line at the double clock frequency. This provides sufficient video bandwidth and delay range for CDV applications.

The delay time is inversely proportional to the clock frequency. Thus for a frequency range of 13 to 24 MHz the following values apply:

- Maximum delay time $1052 \div 13.10^6 = 80.92\ \mu s$
- Minimum delay time $1052 \div 24.10^6 = 43.83\ \mu s$
- Delay range $80.92 - 43.83 = 37.09\ \mu s$

Video input circuit

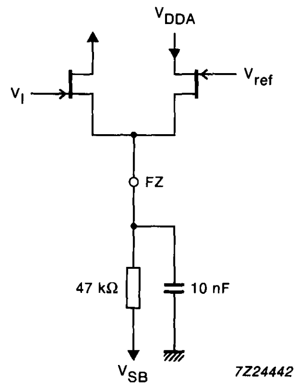


Fig.3 Video input circuit.

Each line has two inputs V_I and V_{ref}. The input signal amplitude is defined as $V_I - V_{ref}$.

Within the specified limits V_{ref} can be used to set the required DC input range for V_I. The FZ input can be used to set the current in the input stage.

In the nominal situation FZ is connected to V_{SB} (−3 V typ.) via a 47 kΩ resistor.

DEVELOPMENT DATA

Video input signal

PAL

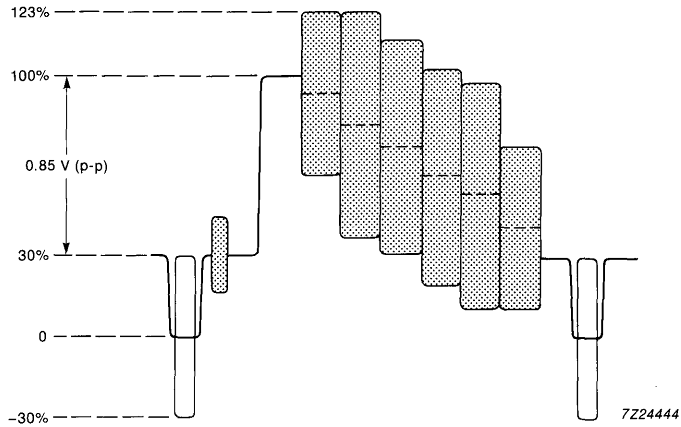


Fig.4 Video input signal for PAL.

The PAL line waveform of 100% saturated colour bars with special burst.
Tip sync to top-white = 100% ≙ 0.85 V (p-p).
Thus the maximum signal amplitude can become 150% x 0.85 V (p-p) = 1.3 V (p-p).

NTSC

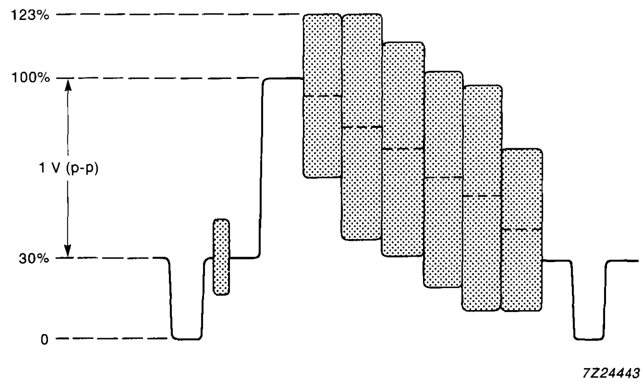


Fig.5 Video input signal for NTSC.

The NTSC line waveform of 100% saturated colour bars.
Tip sync to top-white = 100% ≙ 1.0 V (p-p).
Thus the maximum signal amplitude can become 123% x 1.0 V (p-p) = 1.23 V (p-p).

FUNCTIONAL DESCRIPTION (continued)

Supplies

Separate supply voltages (V_{DDA} and V_{DDD} are provided to prevent interference between analogue and digital circuits. However, it is still necessary to connect decoupling capacitors as near as possible to the respective ground pins. At decreasing V_{DDD} the transfer loss for high input frequencies at maximum f_{CLK} is increasing, therefore care must be taken not to exceed the specification limits of V_{DDD} (4.75 V to 5.5 V).

Clock circuit

The externally applied clock signal is internally converted to a squarewave. Flipflops generate two antiphase signals ($\varphi 1$ and $\varphi 2$) at half the clock frequency which operate the registers.

Output circuit

The output signals of the two multiplexed registers are demultiplexed and stored in a hold capacitor. A buffer stage following the hold capacitor is non-inverting and has a low output impedance (100 Ω typ.).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range					
analogue		V_{DDA}	−0.5	+7.0	V
digital		V_{DDD}	−0.5	+7.0	V
Input voltage	note 1	V_I	−0.5	$V_{DD}+0.5$	V
Output voltage	note 1	V_O	−0.5	$V_{DD}+0.5$	V
Maximum input current		I_{IM}	−	± 10	mA
Maximum output current		I_{OM}	−	± 10	mA
Maximum supply current in V_{SSA}; V_{SSD}		I_{SS}	−	−30	mA
Maximum supply current in V_{DDA}; V_{DDD}		I_{DD}	−	+30	mA
Total power dissipation		P_{tot}	−	500	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−25	+70	°C

Note to the Ratings

1. Input voltage should not exceed 7 V unless otherwise specified.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

T_{amb} = −25 to + 70 °C, unless otherwise specified; all parameters measured with the test circuit of Fig.6.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
analogue		V_{DDA}	4.75	5.0	5.5	V
digital		V_{DDD}	4.75	5.0	5.5	V
substrate bias		$-V_{SB}$	3.5	3.0	2.5	V
Supply current range	$I_I = 0$ mA; $f_{CLK} = 16.6$ MHz					
analogue		I_{DDA}	1	2	4	mA
digital		I_{DDD}	8	12	16	mA
substrate bias		$\|I_{SB}\|$	–	–	100	μA
Inputs						
V_{ref1}; V_{ref2}						
DC input voltage		V_{ref}	0	–	1.5	V
Input current level		I_{ref}	–	–	10	μA
V_{I1}; V_{I2}						
Signal amplitude	$V_I = V_{ref}$	V_I	0	1	1.6	V
Input impedance		R_I	1	–	–	MΩ
		C_I	–	–	10	pF
CLK						
Input voltage amplitude (peak-to-peak value)		$V_{AC(p-p)}$	0.30	0.60	0.90	V
DC output voltage		V_{DC}	1.5	–	3.5	V
Input current		I_{DC}	–	–	150	μA
Input frequency		f_{CLK}	13	–	24	MHz
FZ1; FZ2						
DC input voltage	w.r.t. V_{ref}	$-V_{DC}$	1.5	–	0.5	V
Outputs						
V_{O1}; V_{O2}	R_{FZ} to V_{SB} = 47 kΩ					
DC output voltage	V_I to V_{ref} = 0 V	V_O	0.25	0.5	0.75	V
	V_I to V_{ref} = 1.6 V	V_O	2.0	2.5	3.0	V
DC output current		$\|I_O\|$	–	–	1	mA
Output impedance		R_O	–	–	250	Ω
Maximum load impedance		R_L	–	–	10	kΩ
		C_L	–	–	10	pF

AC CHARACTERISTICS

V_{DDD} = 4.75 to 5.5 V; T_{amb} = −25 to +70 °C, unless otherwise specified; all parameters measured with the test circuit of Fig.6.

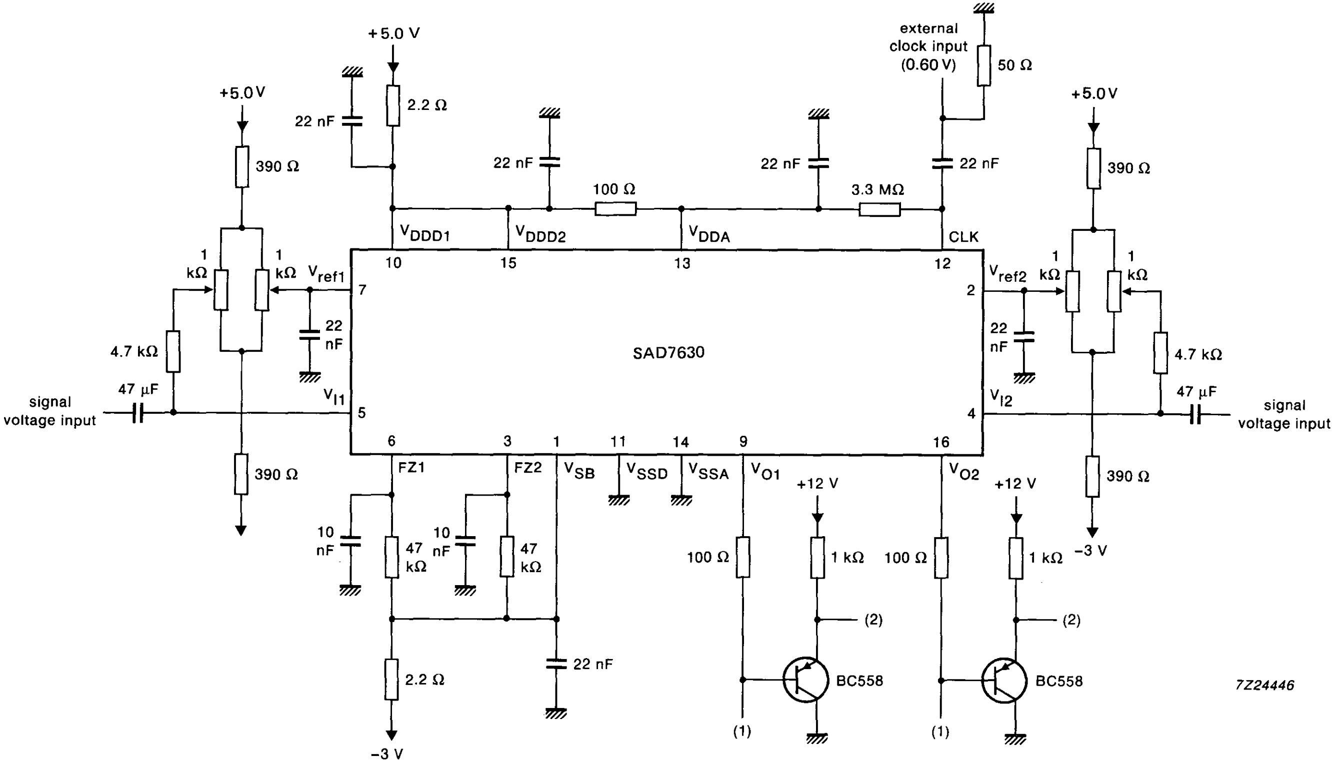
parameter	conditions	symbol	min.	typ.	max.	unit
Voltage gain	note 1	G_v	2	3	4	dB
Transfer loss at 5 MHz (w.r.t. 1 kHz)	f_{CLK} = 13 and 24 MHz	H_d	1.0	2.5	4.5	dB
Linearity error	note 2	L_e	−	−	6	%
Differential gain	note 2	G_d	−	−	5	%
Differential phase	note 2	α_d	−	−	5	deg.
DC output voltage		V_O	−	30	70	mV
Clock leakage voltage (RMS value)	f_{CLK} = 13 to 24 MHz					
6.5 MHz		V_{LCLK}	−	−	8	mV
13 MHz		V_{LCLK}	−	−	20	mV
19.5 MHz		V_{LCLK}	−	−	20	mV
Noise output voltage (RMS value)	B = 5 MHz (unweighted)	$V_{on(rms)}$	−	−	*	mV
Crosstalk attenuation between lines	note 3	a_x	−	−	*	dB
Distortion	note 4	d	−	−	10	%

DEVELOPMENT DATA

Notes to the AC characteristics

1. V_I to V_{ref} = 1 V(p-p); f_i = 1 kHz; f_{CLK} = 16.6 MHz.
2. V_I to V_{ref} = 1 V(p-p); f_{CLK} = 16.6 MHz.
3. V_I to V_{ref} = 1 V(p-p); f_i = 2 MHz; f_{CLK} = 16.6 MHz.
4. V_I to V_{ref} = 1.6 V(p-p); f_i = 1 kHz; f_{CLK} = 16.6 MHz.

* Value to be fixed.



(1) DC measurements.
(2) AC measurements.

Fig.6 Measuring circuit.

REMOTE CONTROL SYSTEM FOR INFRARED OPERATION

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.

Features:

SAF1032P receiver/decoder:

- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:

- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

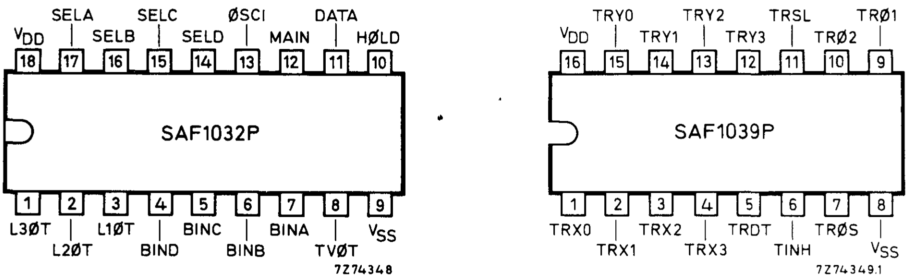


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT102).
SAF1039P: 16-lead DIL; plastic (SOT38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

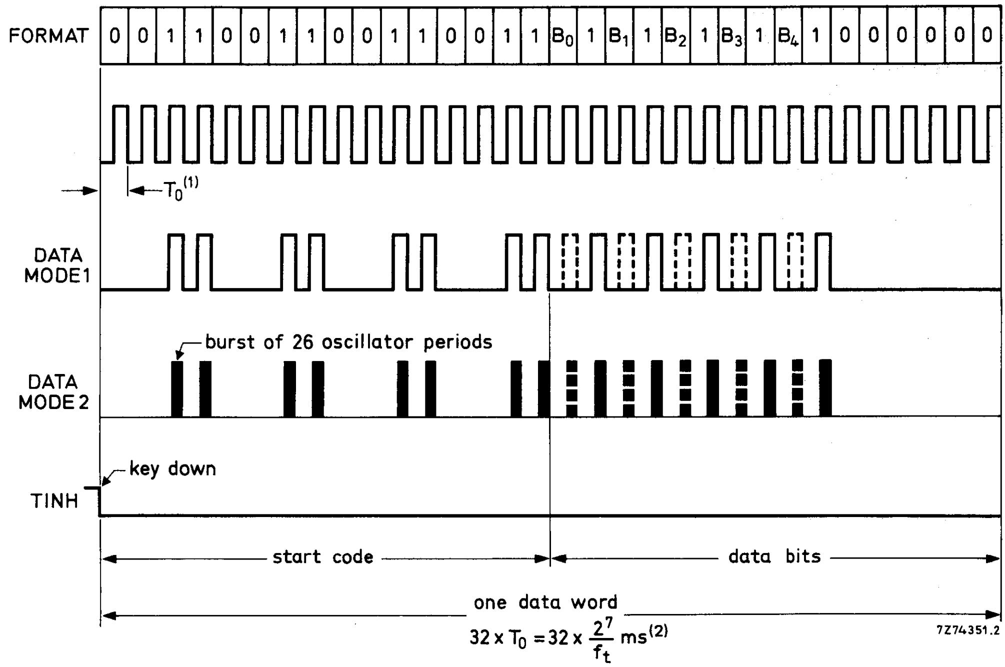
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	TRSL	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

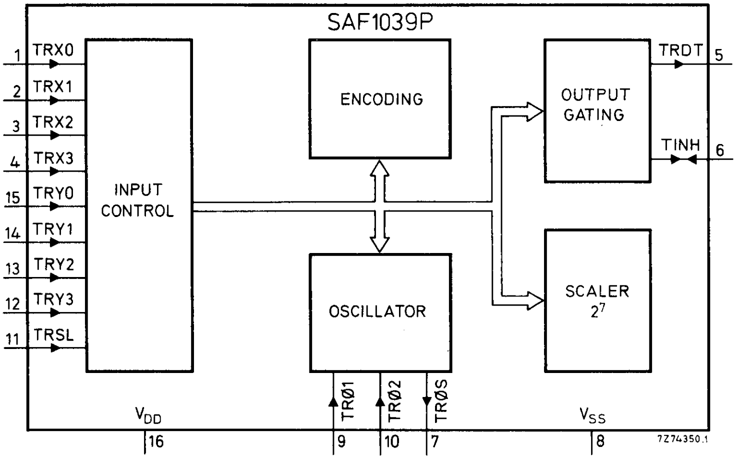


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on the previous page, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

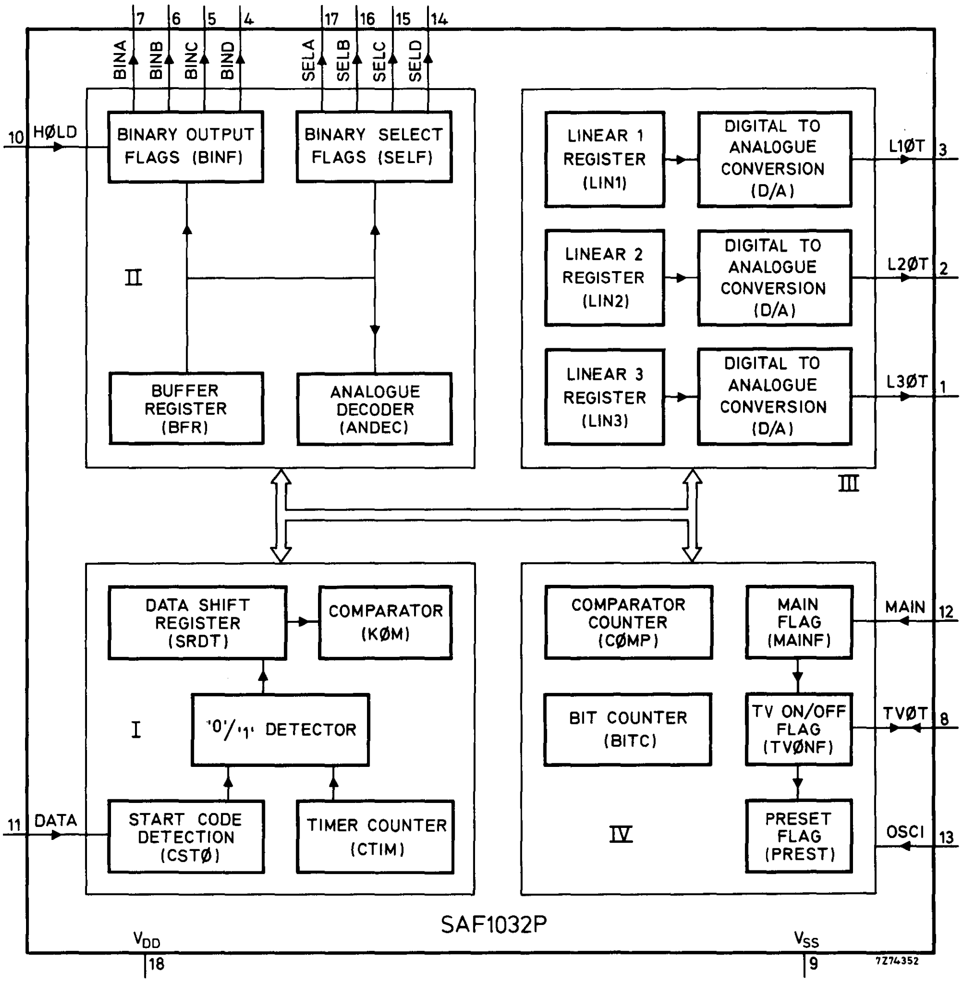


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see operating output code table).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geq$ 100 μs.

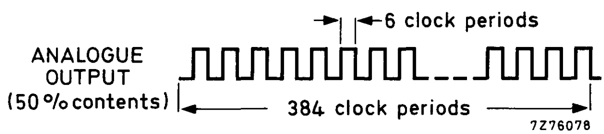


Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	programme
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	select + ON
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	programme
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	select + ON
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN3) − 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN2) − 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	reg. (LIN1) − 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	spare functions
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(L.ØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON — 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON — 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}	−0,5 to 11	V
Input voltage	V_I	max. 11	V
Current into any terminal	$\pm I_I$	max. 10	mA
Power dissipation (per output)	P_o	max. 50	mW
Power dissipation (per package)	P_{tot}	max. 200	mW
Operating ambient temperature	T_{amb}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1,7	mA	10	all
		–	0,8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0{,}8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0{,}2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0{,}5$ V	$-I_{OH}$	0,4	–	–	mA	7	all
output current LOW at V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0,4 V	I_{OL}	0,4	–	–	mA	7	all
Oscillator							
maximum oscillator frequency	f_{osc}	120	–	–	kHz		
frequency variation with supply voltage, temperature and spread of IC properties at f_{nom} = 36 kHz (note 3)	Δf	–	–	$0{,}15f_{nom}$		7 to 10	all
oscillator current drain at f_{nom} = 36 kHz	I_{osc}	–	1,3	2,5	mA	10	25

Notes follow characteristics.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	$0{,}2V_{DD}$	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	$0{,}4V_{DD}$	–	$0{,}9V_{DD}$	V	5 to 10	all
input voltage decreasing	V_{td}	$0{,}1V_{DD}$	–	$0{,}6V_{DD}$	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA	8	all
output leakage current at V_O = V_{SS} to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see next page.

Notes to characteristics

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

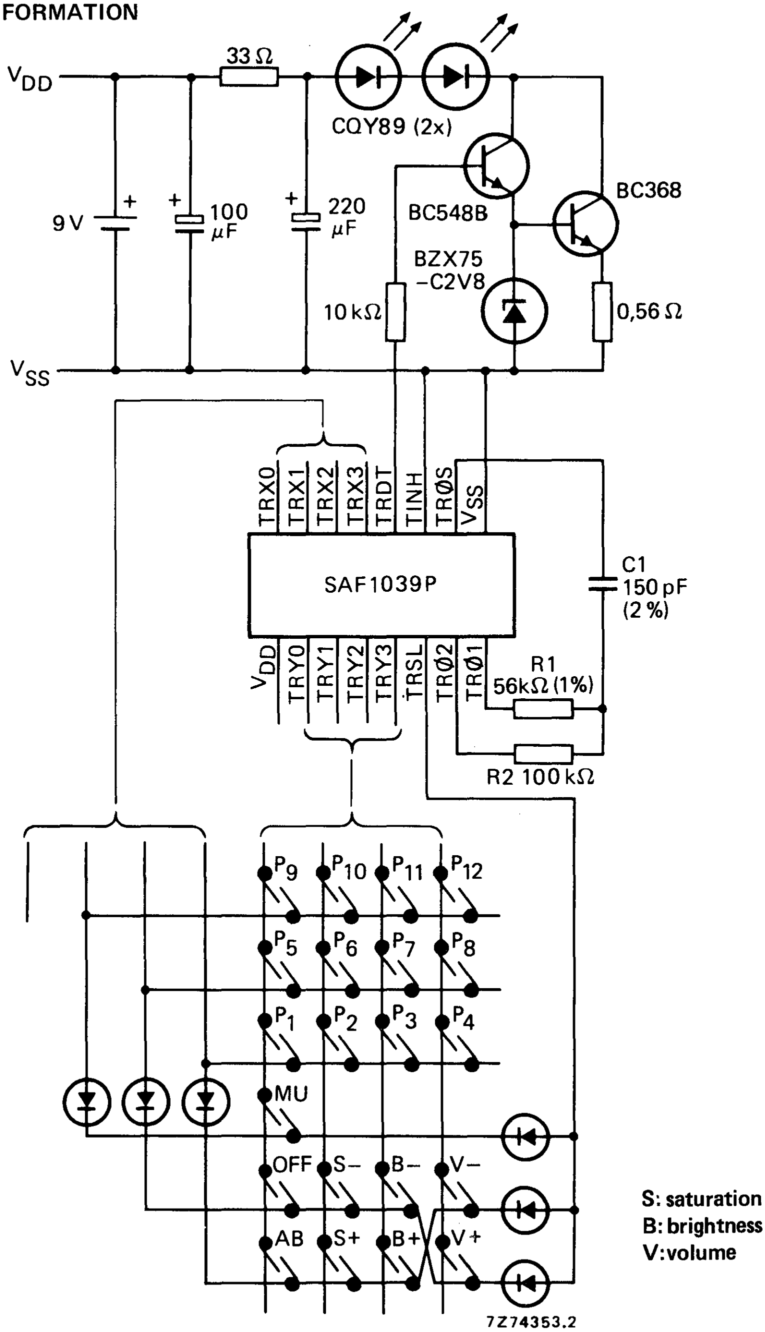


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

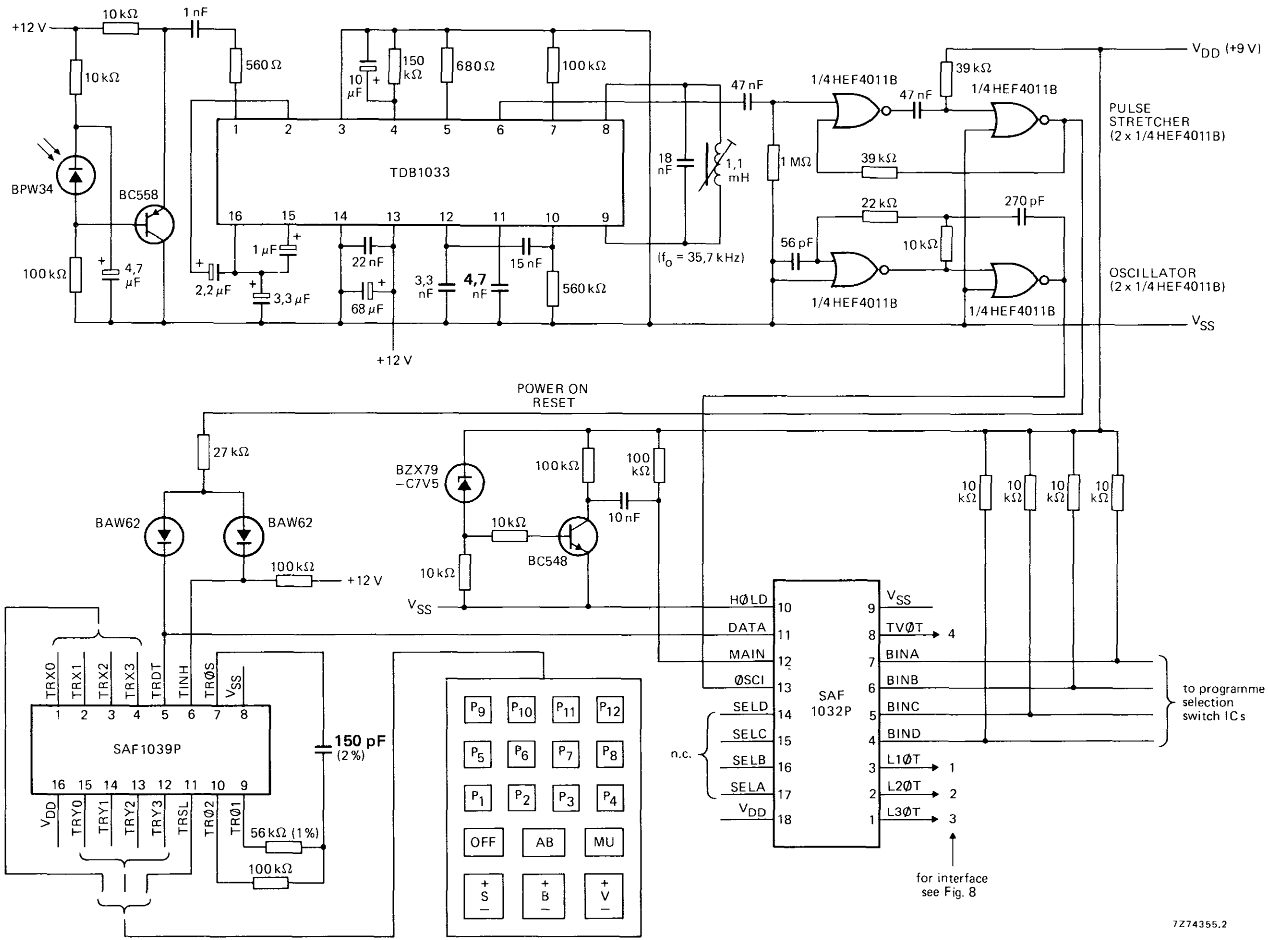


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

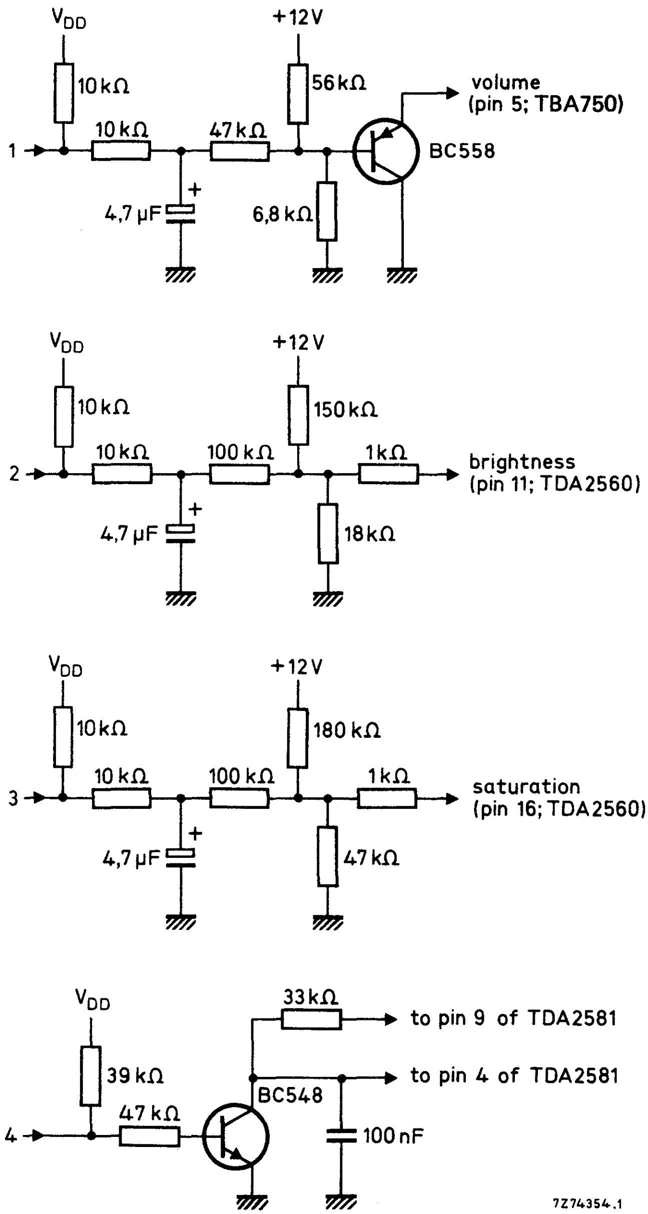


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12	V
Supply current (pin 9)	I_P	typ.	14	mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1	V
Input resistance (pin 1)	R_i	min.	35	kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5	dB
Total harmonic distortion	THD	typ.	0,25	%
Bandwidth	B	typ.	70	kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19	mV
Suppression pulse duration	t_s	typ.	27	μs
Supply voltage range (pin 9)	V_P		7,5 to 16	V
Operating ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT38).
TDA1001BT: 16-lead mini-pack; plastic (SO16; SOT109A).

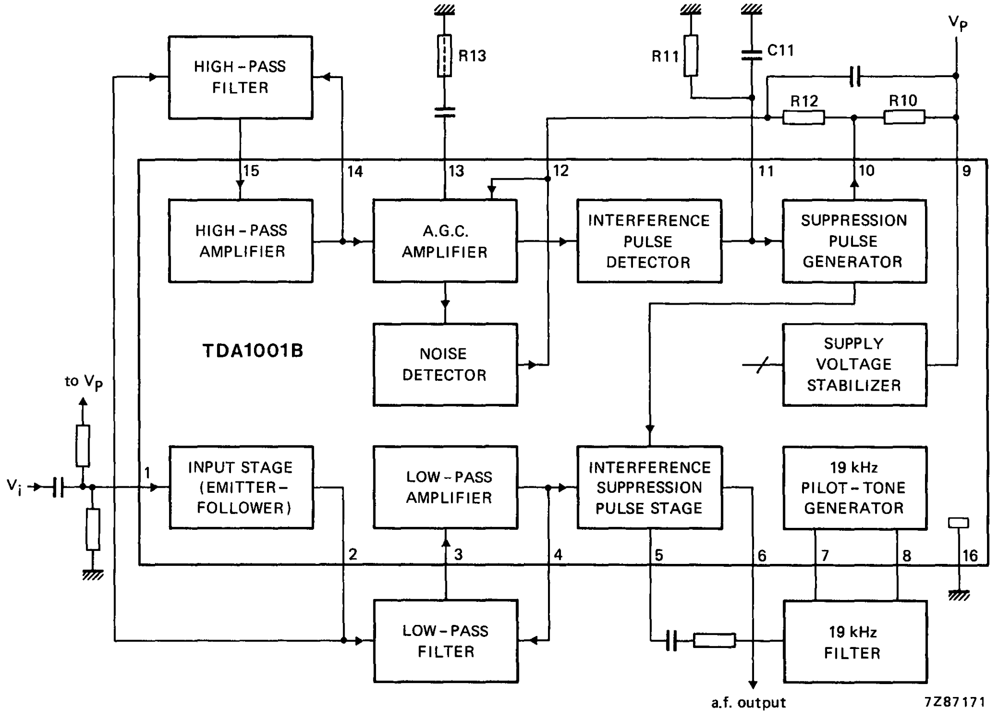


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18	V
Input voltage (pin 1)	$V_{1\text{-}16}$	max.	V_P	V
Output current (pin 6)	I_6	max.	1	mA
	$-I_6$	max.	15	mA
Total power dissipation	see derating curves Fig. 2			
Storage temperature range	T_{stg}	−65 to +150		^oC
Operating ambient temperature range	T_{amb}	−30 to +80		^oC

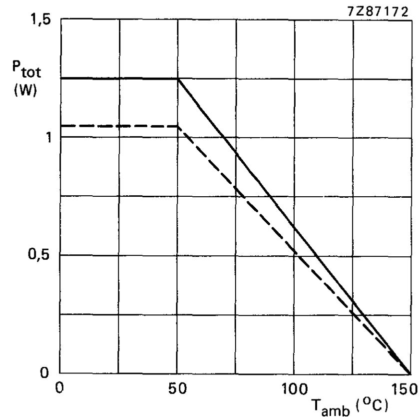


Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\lvert Z_{i1} \rvert$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$	–	6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\lvert Z_{i8} \rvert$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\lvert Z_{o7} \rvert$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\,m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\,m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
$(V_{i(tr)O} + 3\text{ dB})$	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11) 1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\|Z_{i1}\|$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4)					
$V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a de-emphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

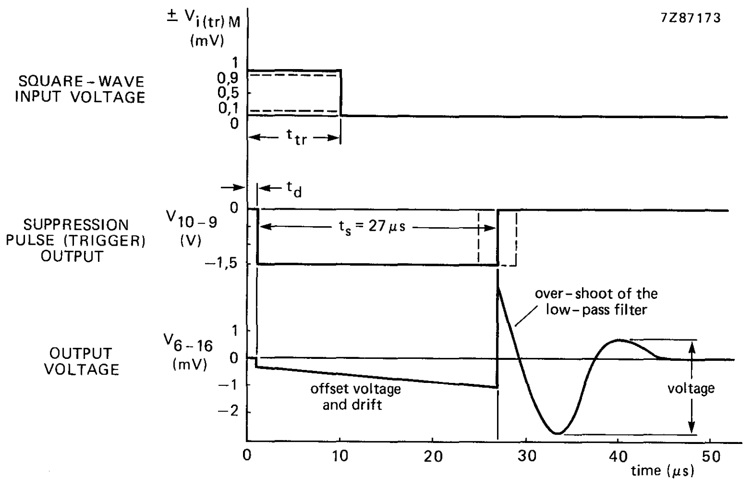


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

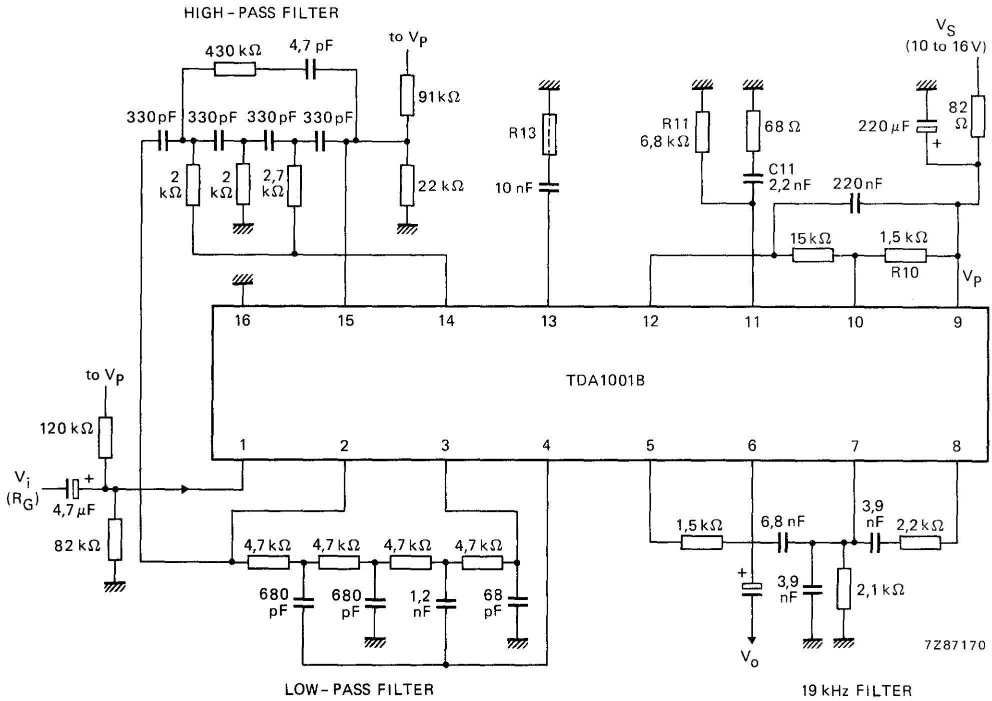


Fig. 4 Application circuit diagram.

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

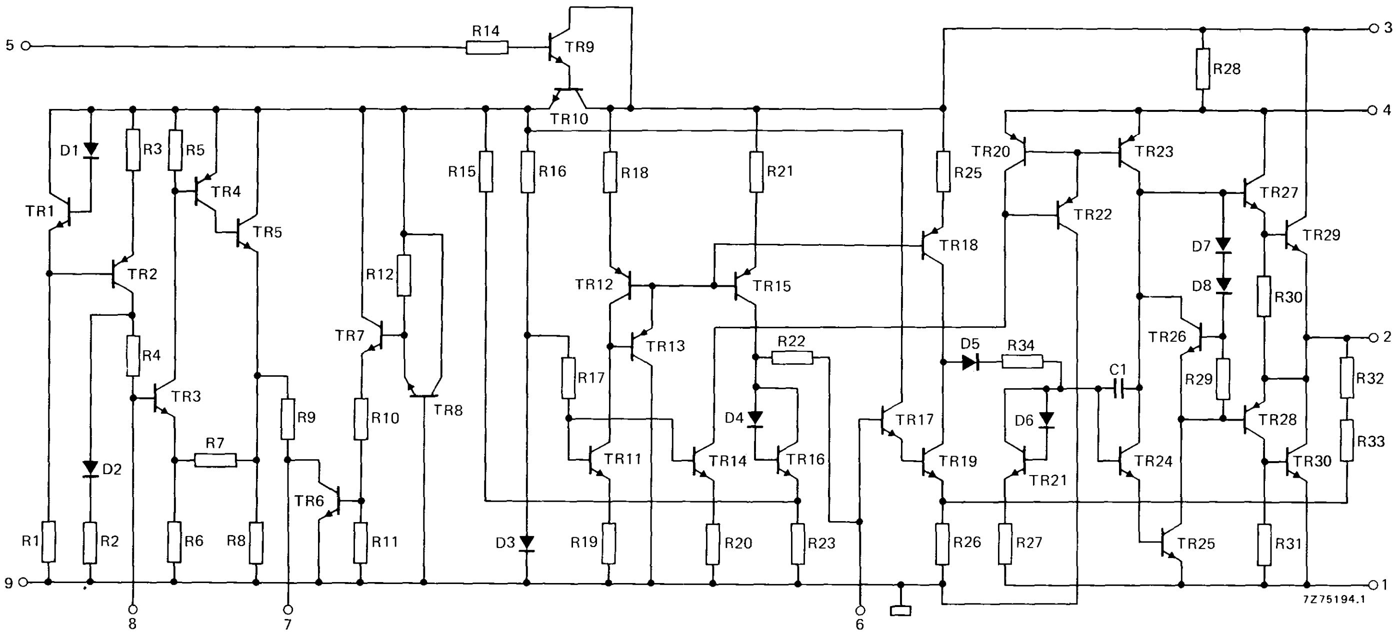


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	5	A
Repetitive peak output current	I_{ORM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		^oC
Operating ambient temperature	T_{amb}	−25 to + 150		^oC
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100	hours

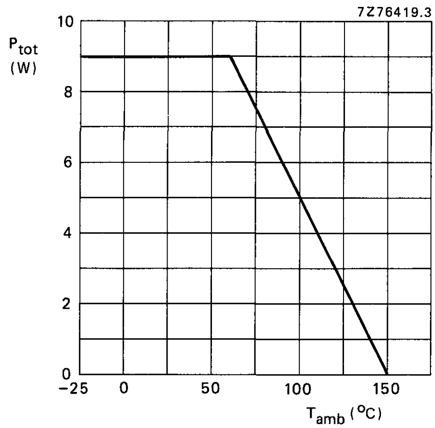


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 ^oC maximum; thermal shut-down starts at T_j = 150 ^oC. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$$R_{th\ h\text{-}a} = 23 - (10 + 1) = 12\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	<	3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap				
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	>	5,9	W
		typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ.	5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Voltage gain				
preamplifier (note 3)	G_{v1}	typ.	24	dB
			21 to 27	dB
power amplifier	G_{v2}	typ.	30	dB
			27 to 33	dB
total amplifier	$G_{v\,tot}$	typ.	54	dB
			51 to 57	dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ.	0,2	%
Efficiency at P_o = 6 W	η	typ.	75	%
Frequency response (−3 dB)	B		80 Hz to 15	kHz
Input impedance				
preamplifier (note 4)	$\lvert Z_i \rvert$	typ.	30	kΩ
			20 to 40	kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,7	mV
		<	1,4	mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	>	42	dB
at f = 100 Hz; C2 = 1 μF	RR	>	37	dB
Sensitivity for P_o = 5,8 W	V_i	typ.	10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

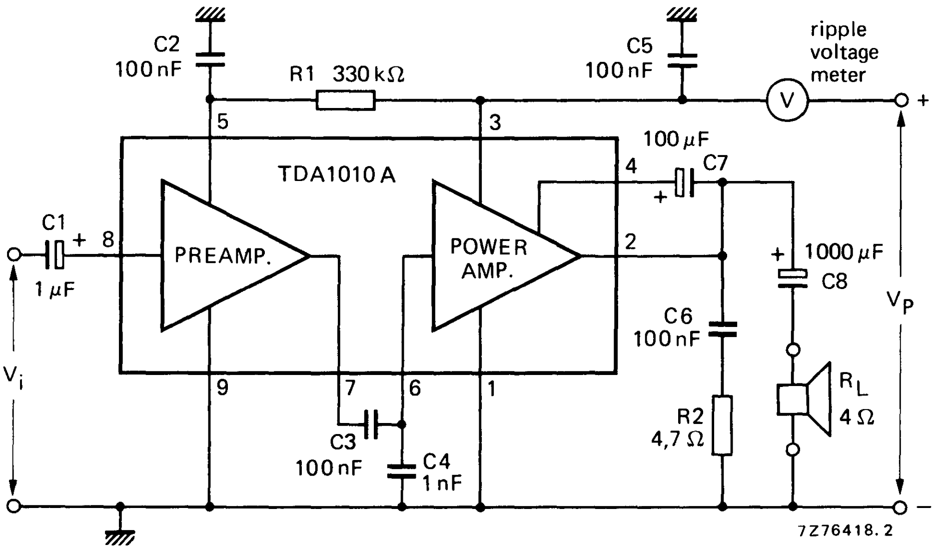


Fig. 3 Test circuit.

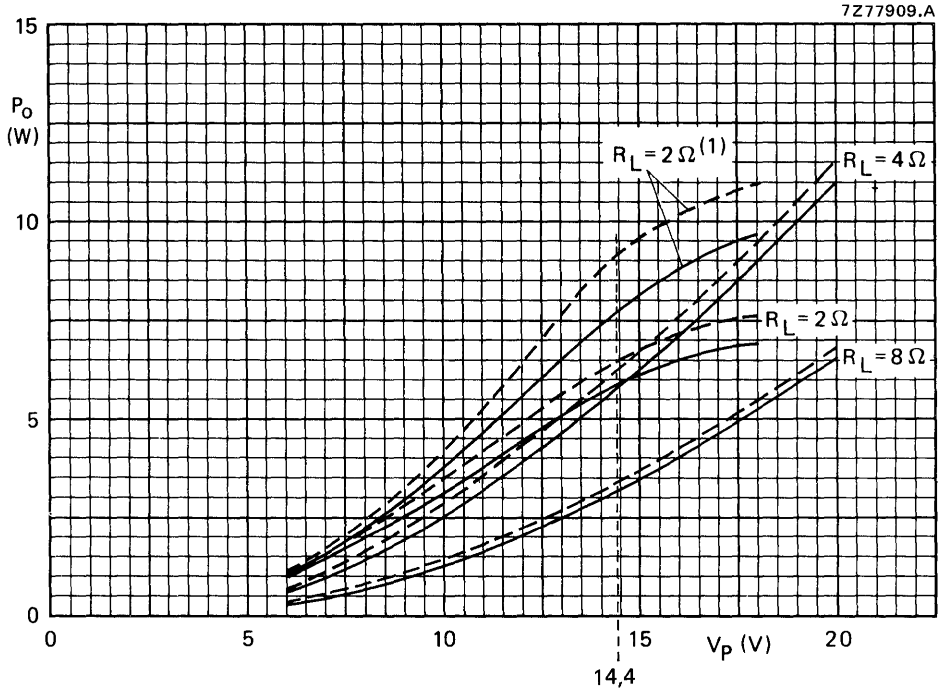


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

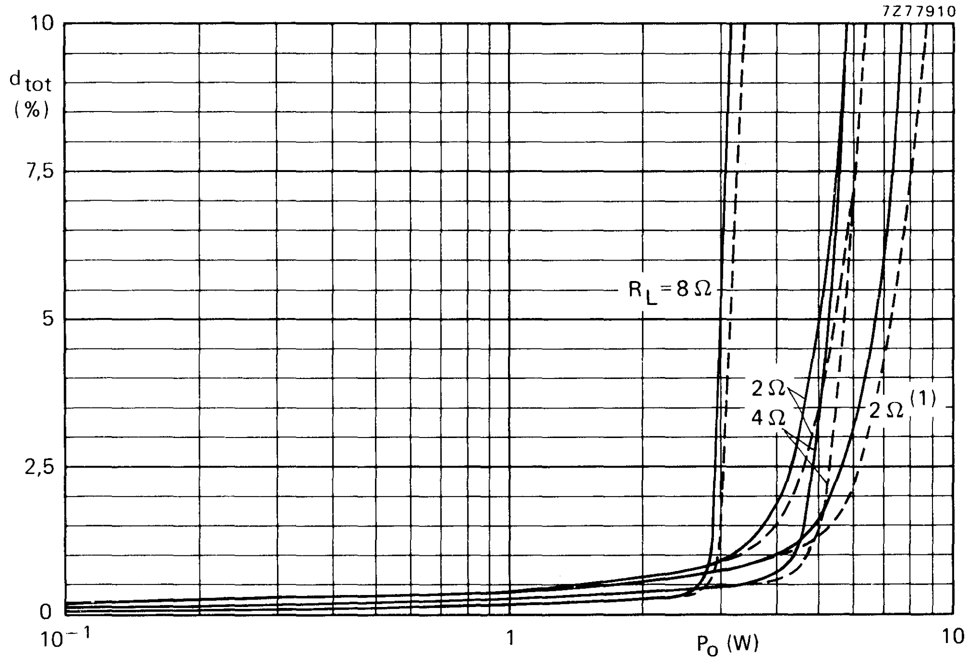


Fig. 5 For caption see preceding page.

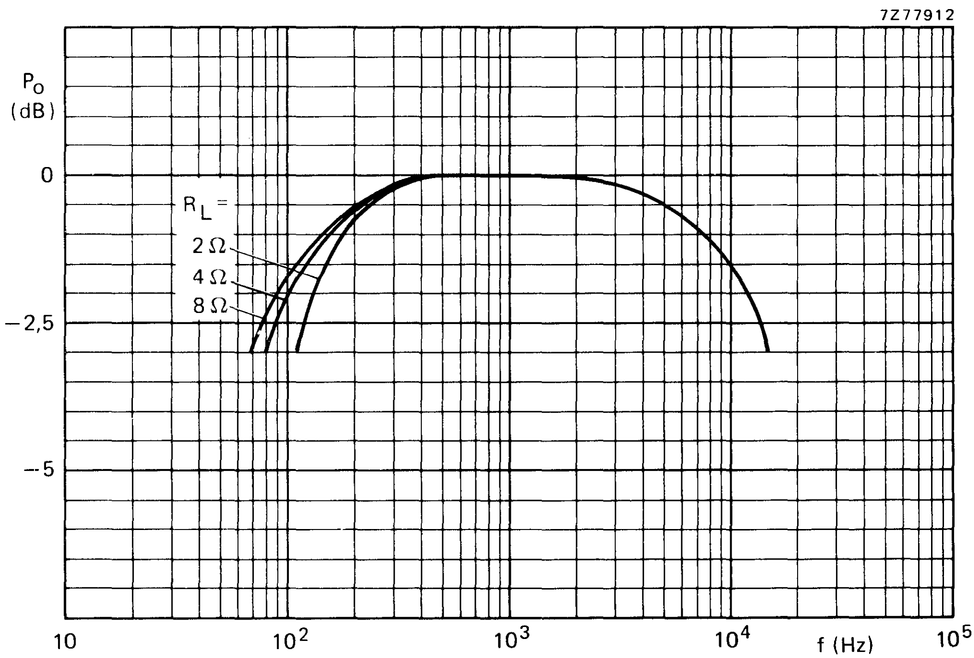


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

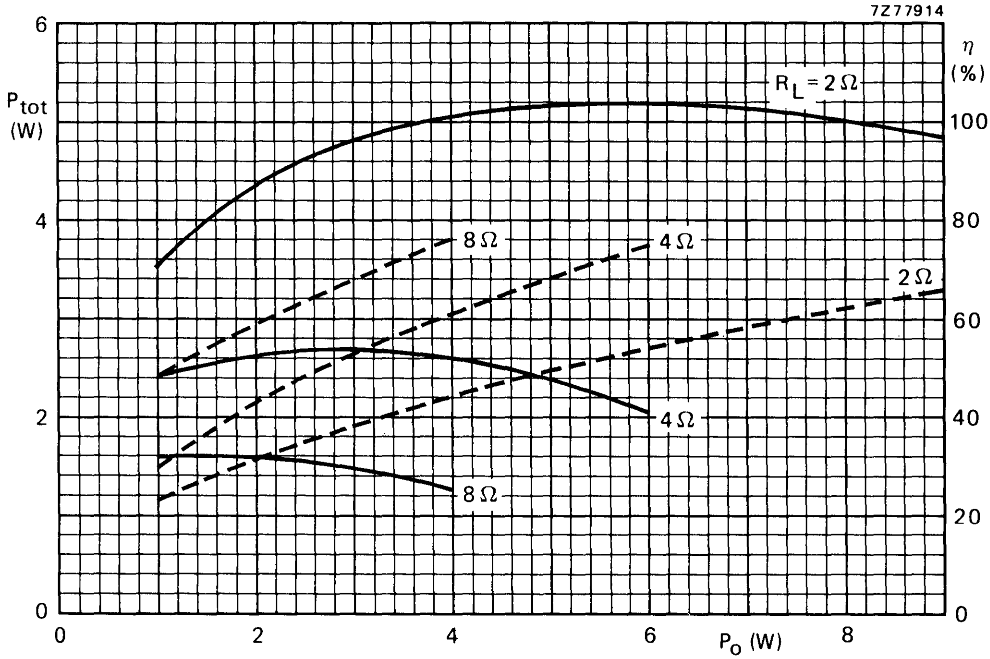


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\ \Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

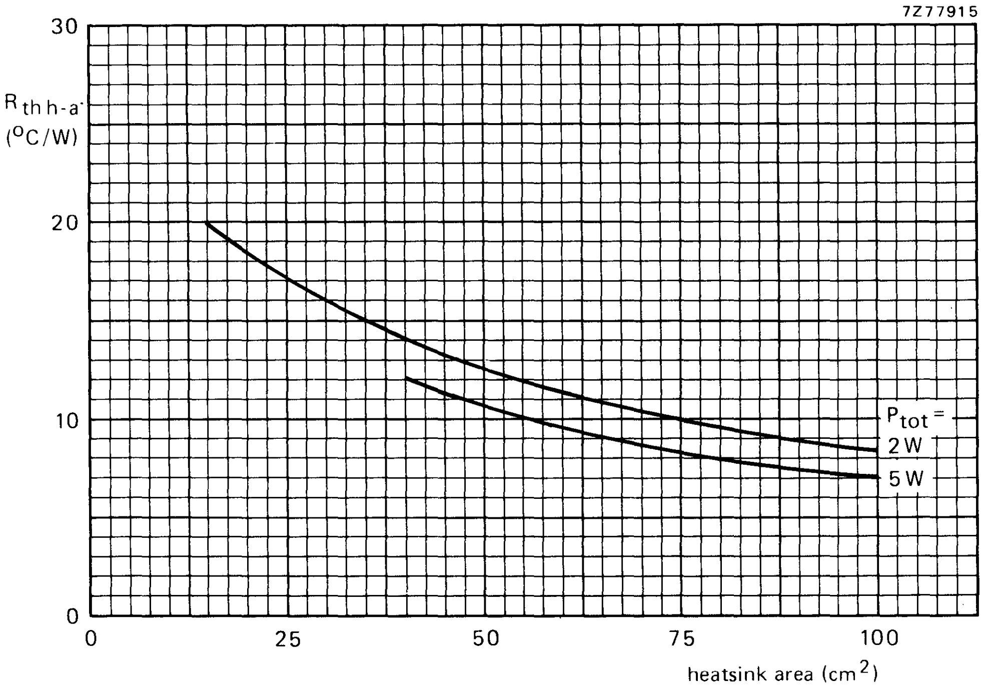


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

APPLICATION INFORMATION

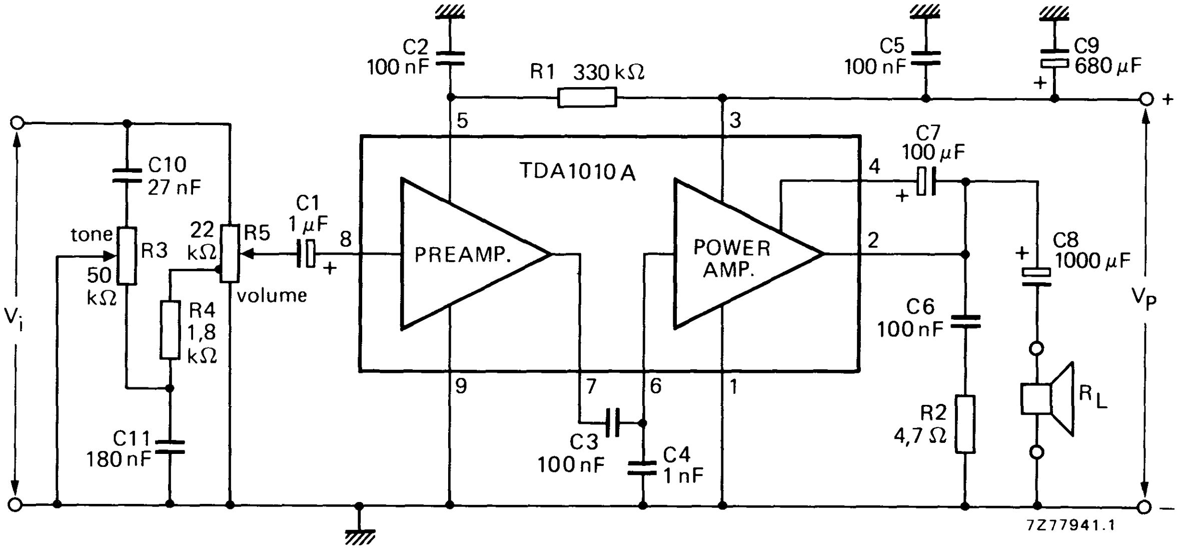


Fig. 9 Complete mono audio amplifier of a car radio.

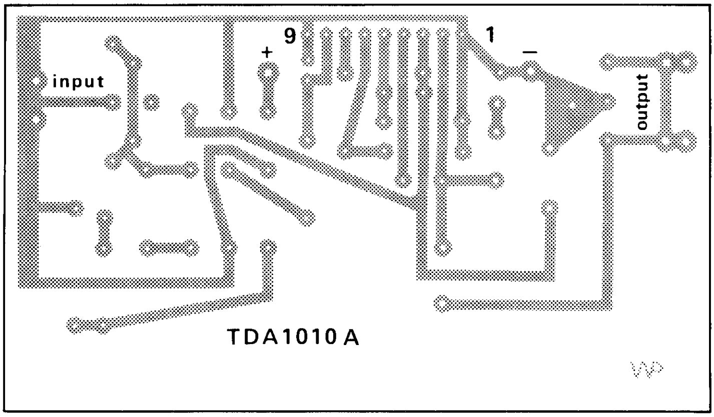


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Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

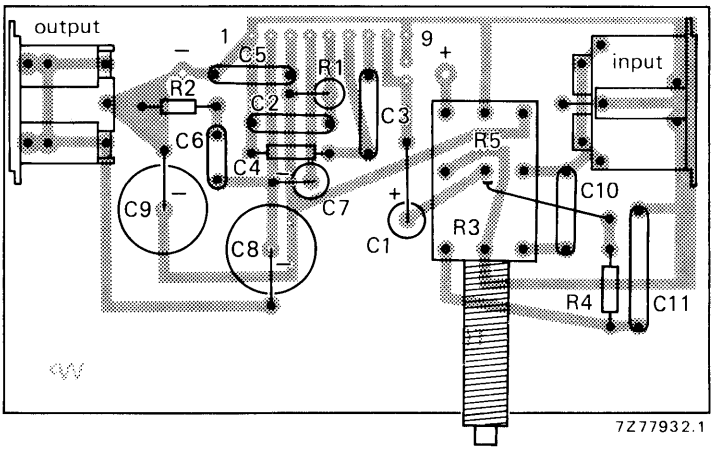

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Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

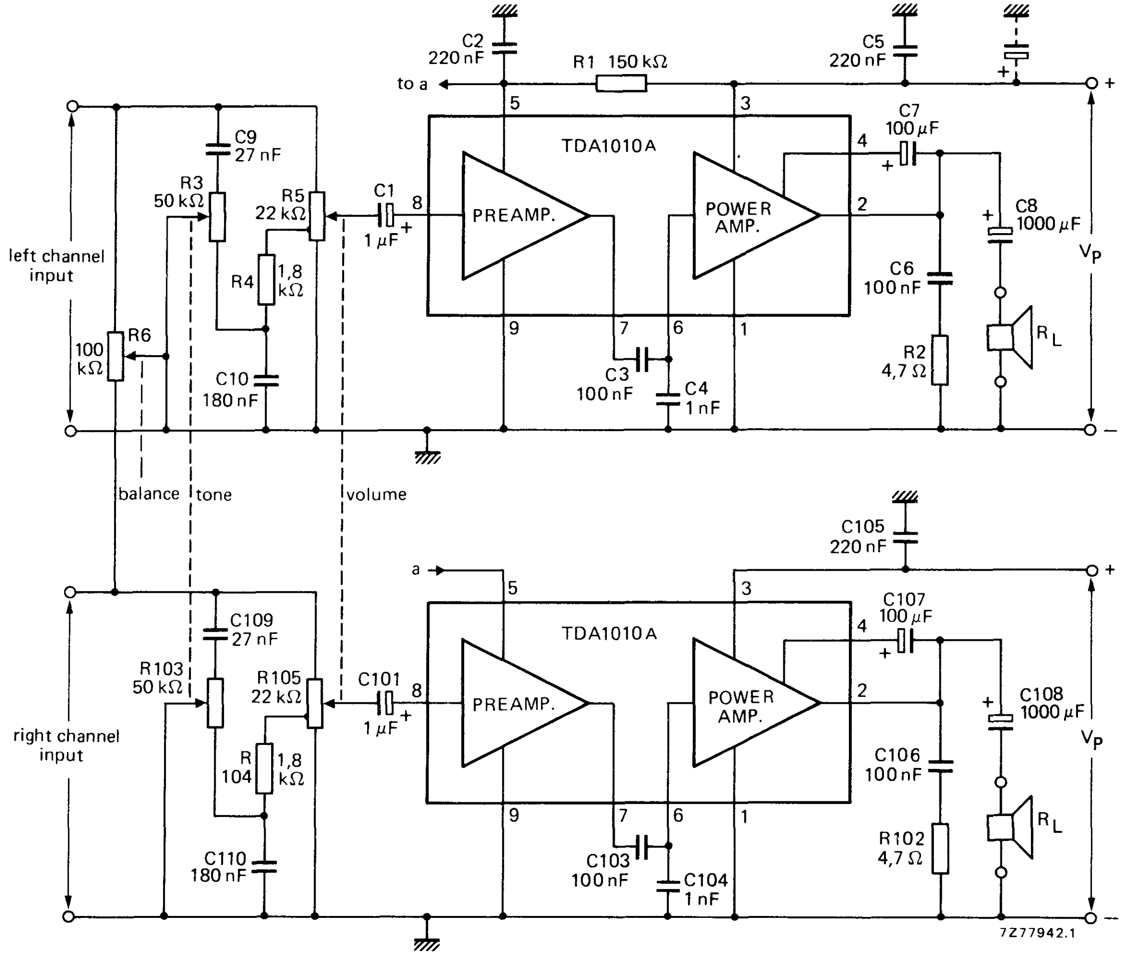

Fig. 12 Complete stereo car radio amplifier.

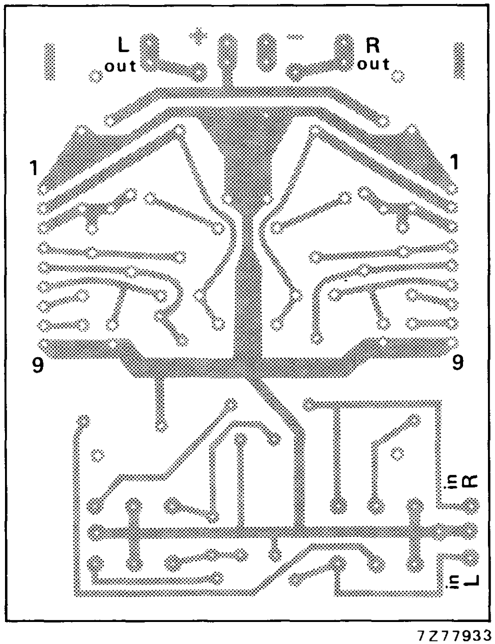

Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

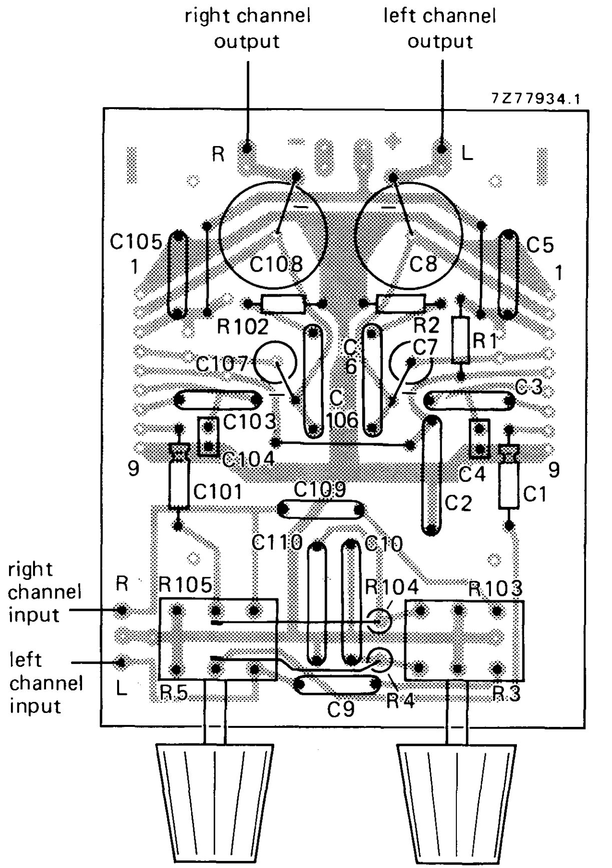

Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

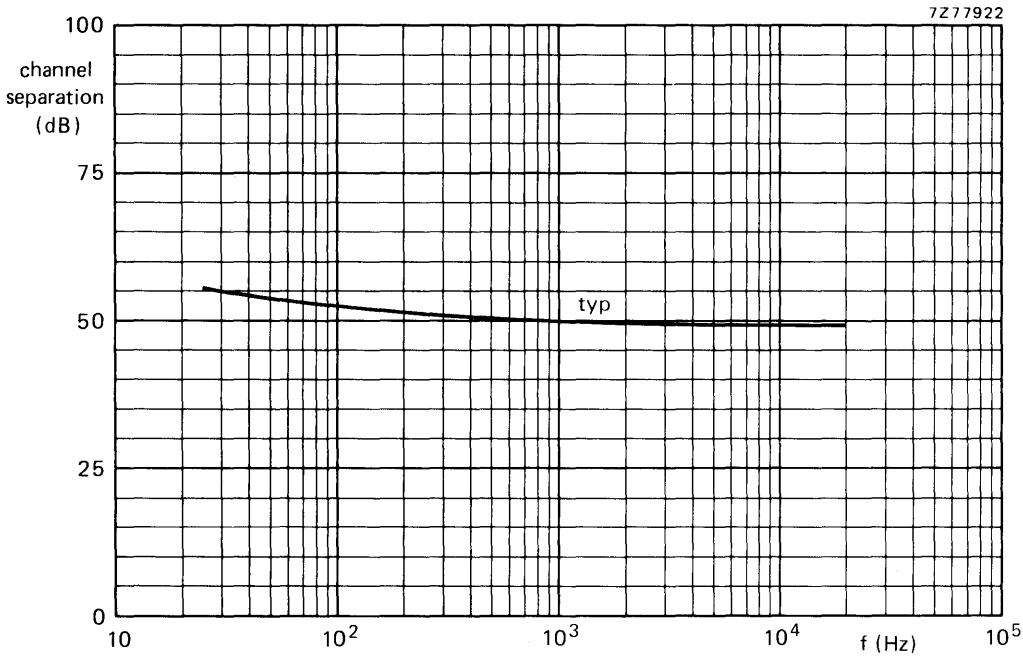

Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

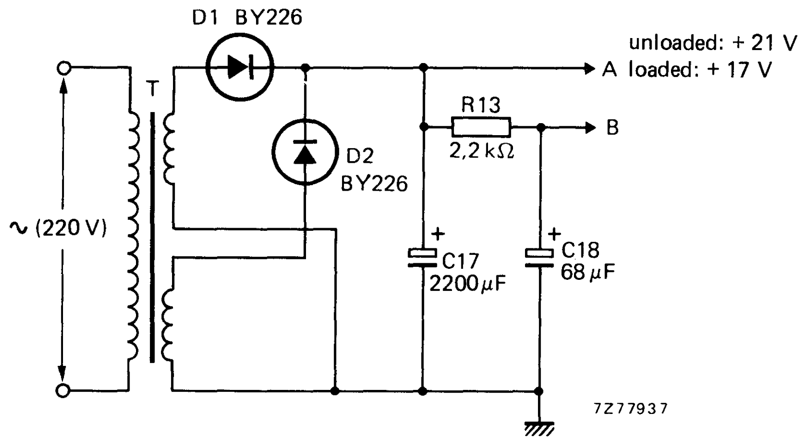

Fig. 16 Power supply of circuit of Fig. 17.

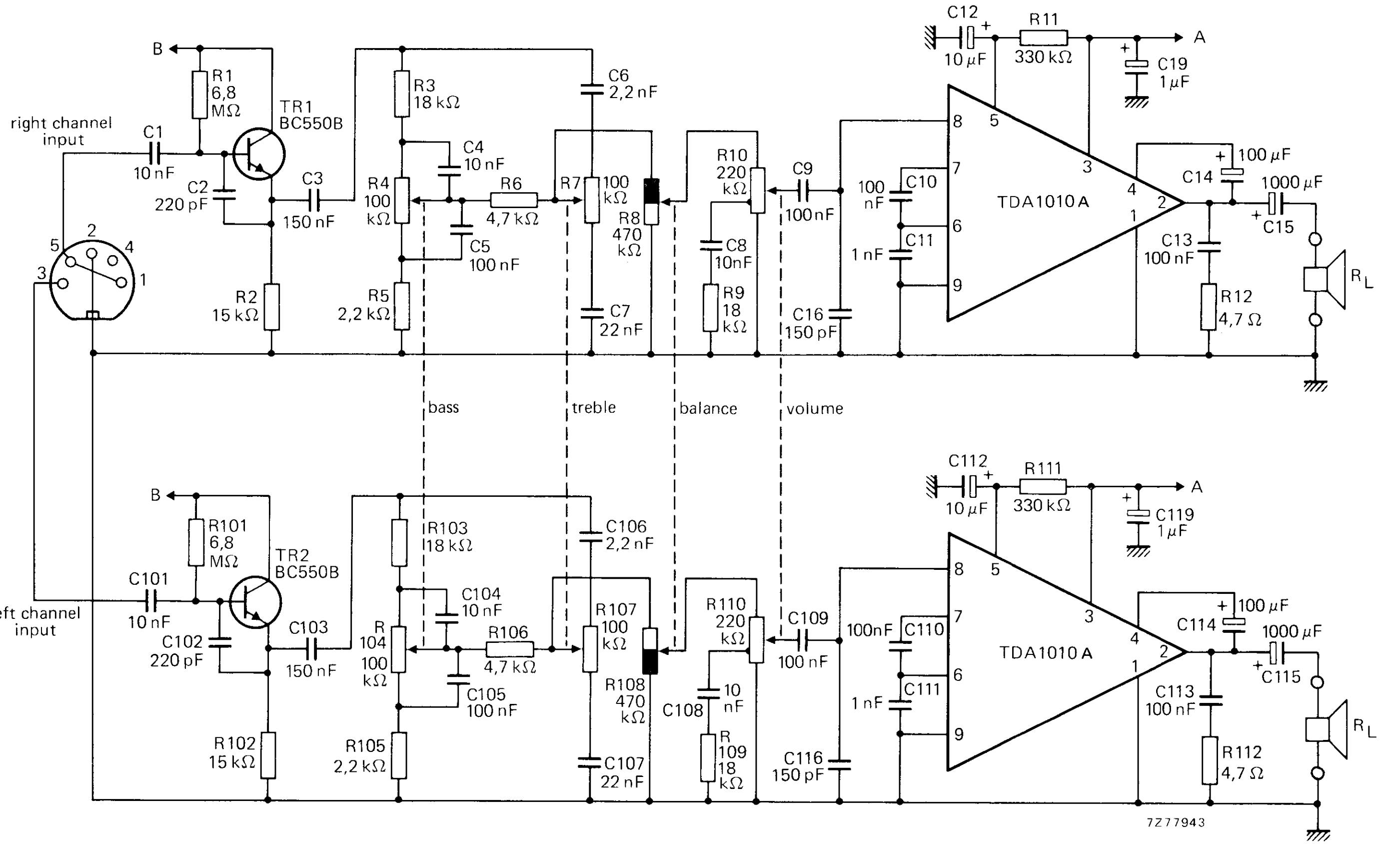

Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

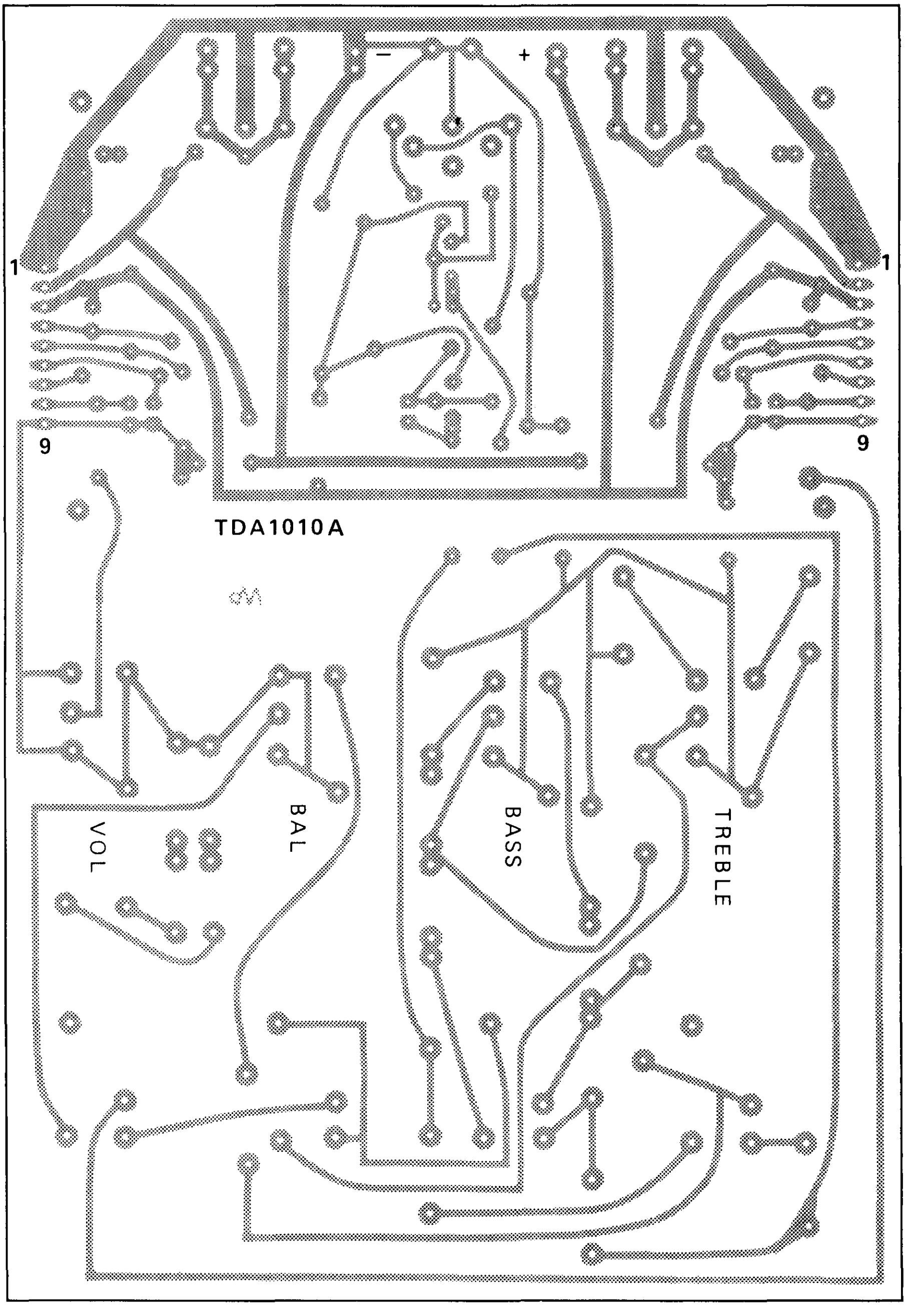

Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

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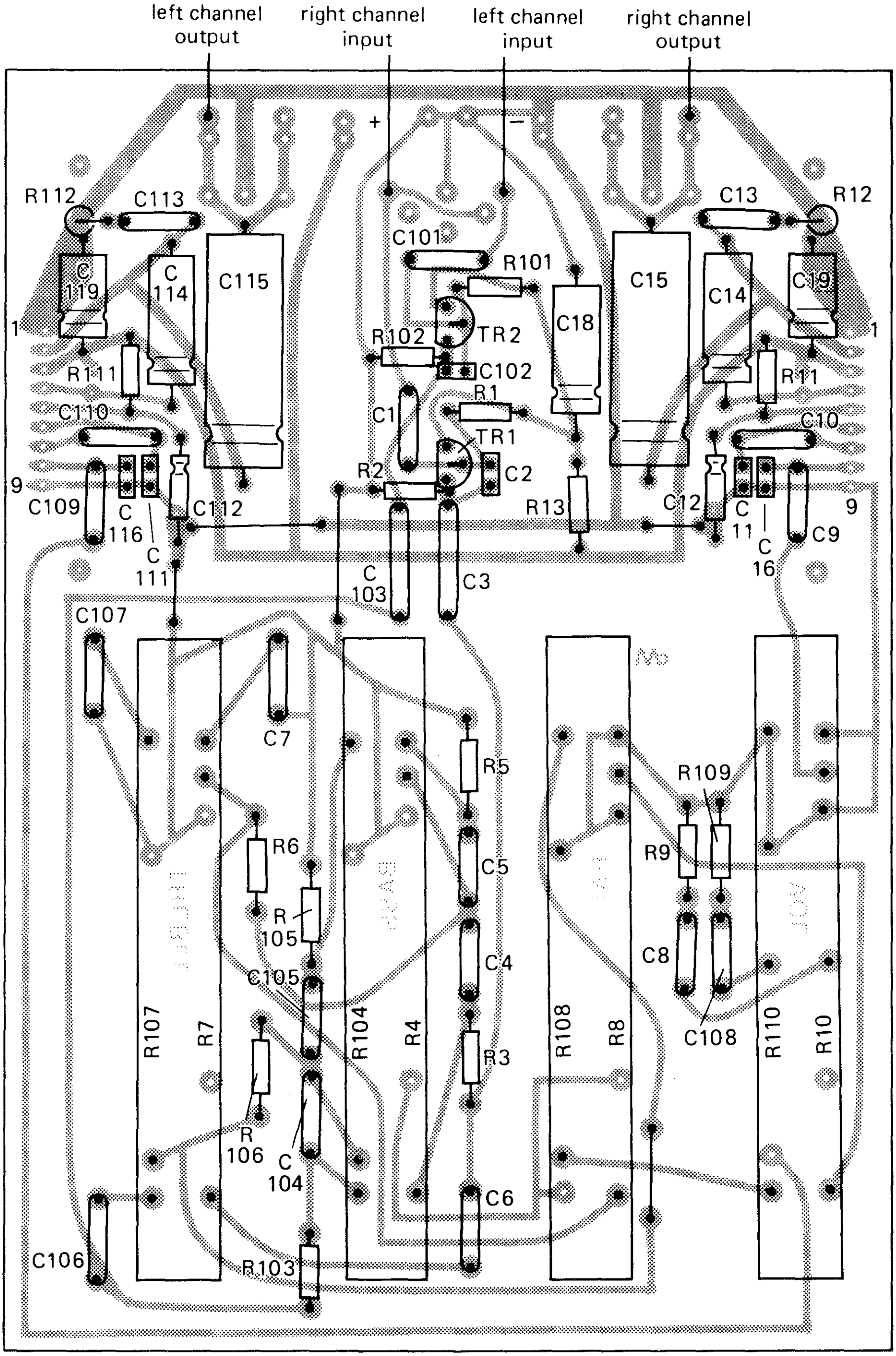


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

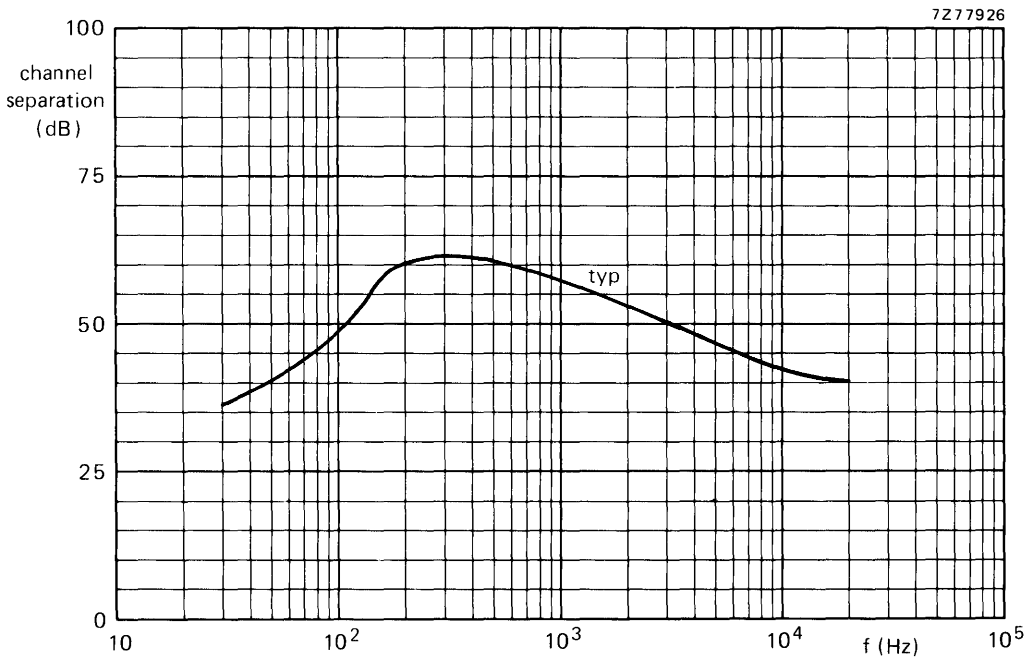


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

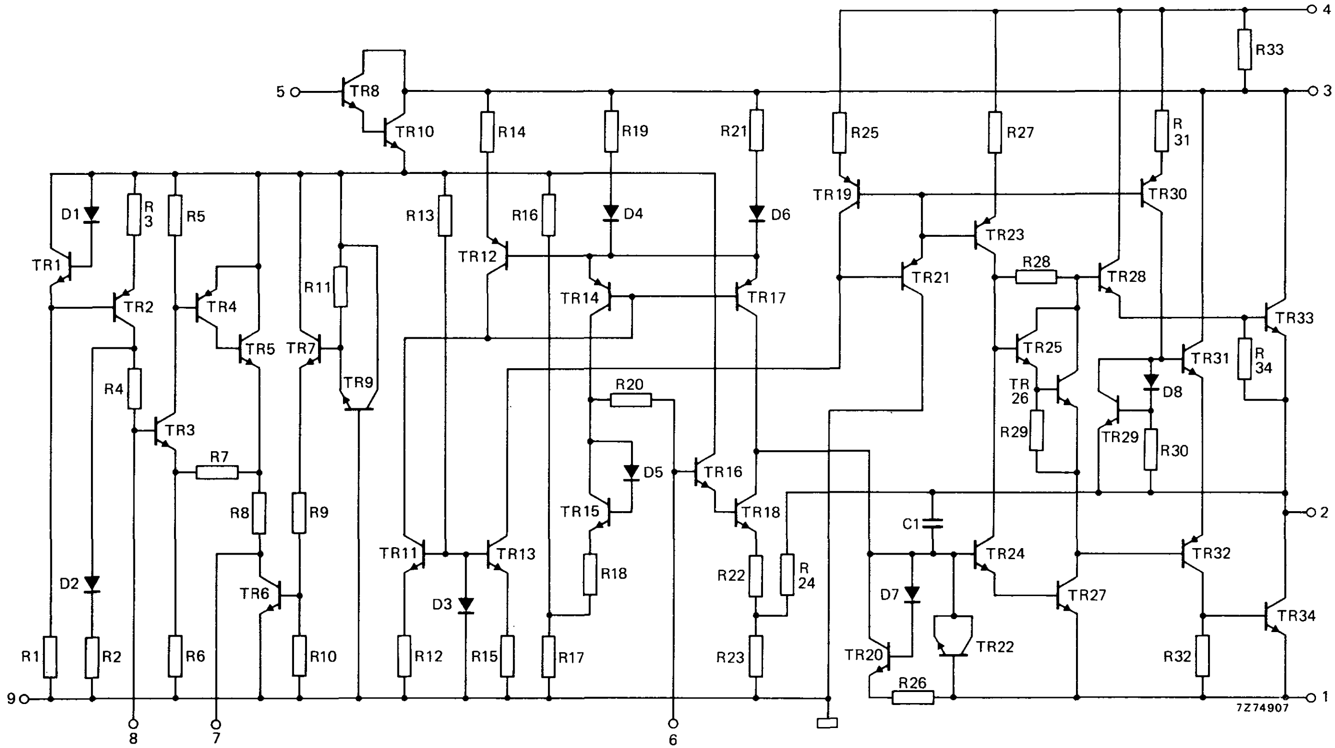


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

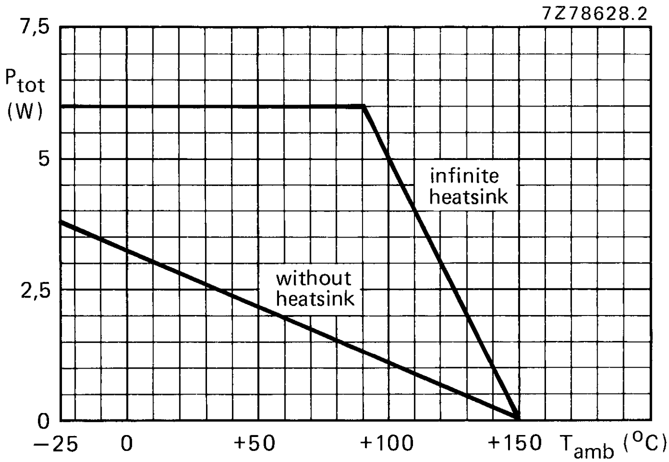


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-60}{1,8} = 50\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab}$ = 10 K/W and $R_{th\,tab\text{-}h}$ = 1 K/W, $R_{th\,h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 20	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	>	3,6	W
		typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier	G_{v2}	typ.	29	dB
			27 to 31	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			50 to 54	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; –3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ.	20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,6	mV
		<	1,4	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

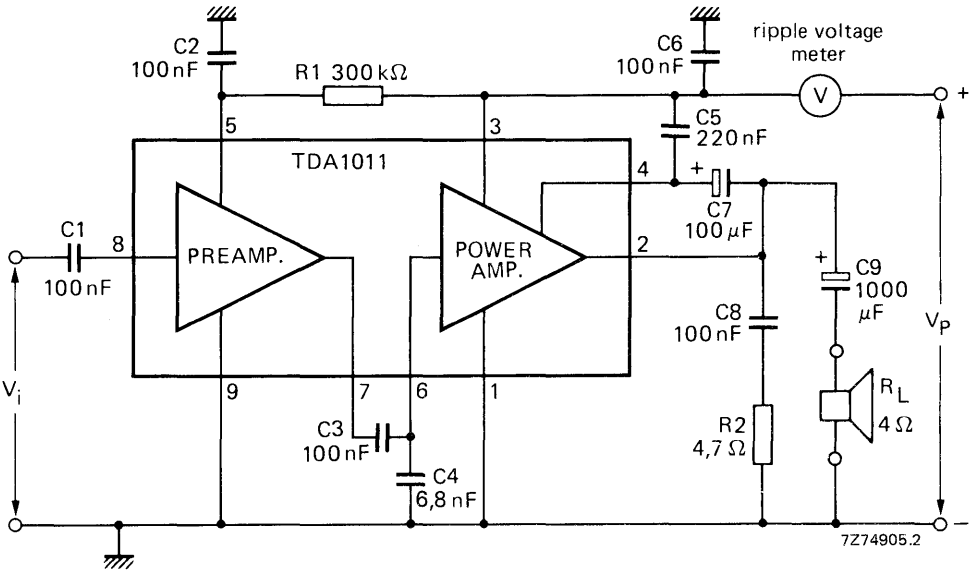


Fig. 3 Test circuit.

APPLICATION INFORMATION

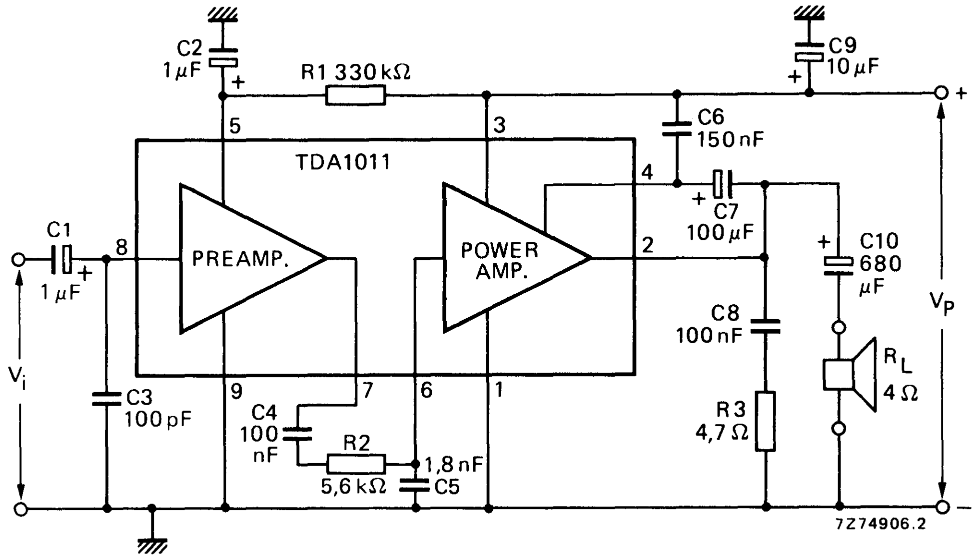


Fig. 4 Circuit diagram of a 4 W amplifier.

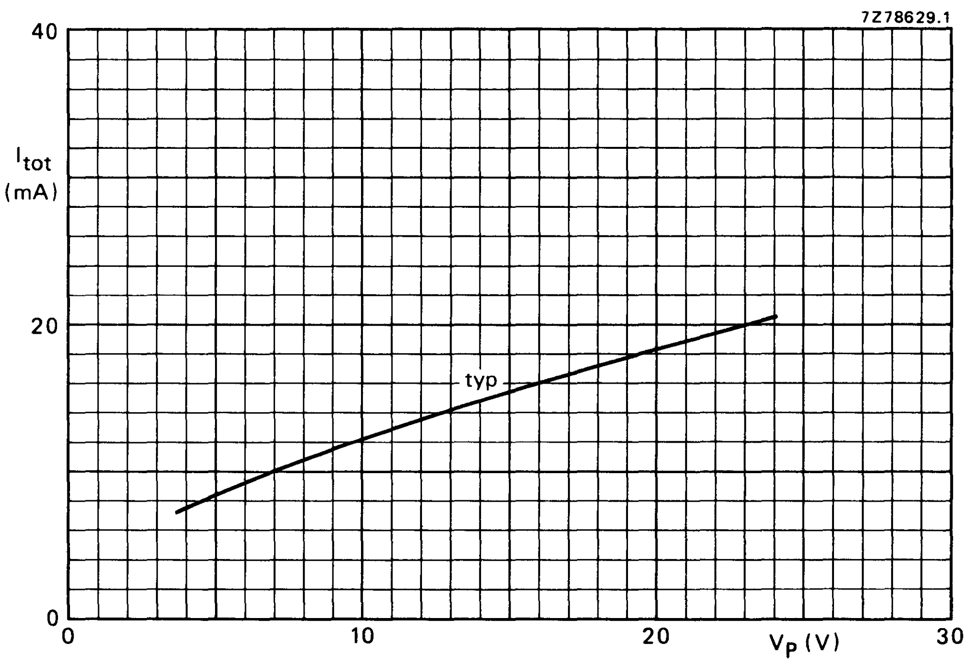


Fig. 5 Total quiescent current as a function of supply voltage.

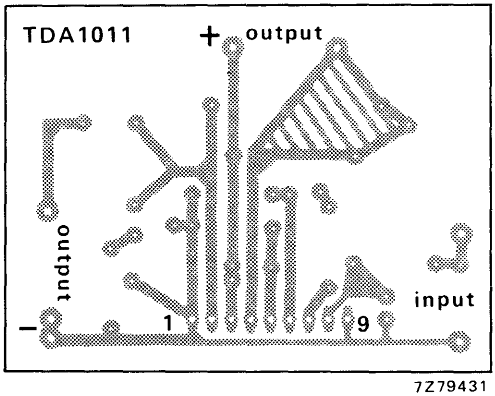


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

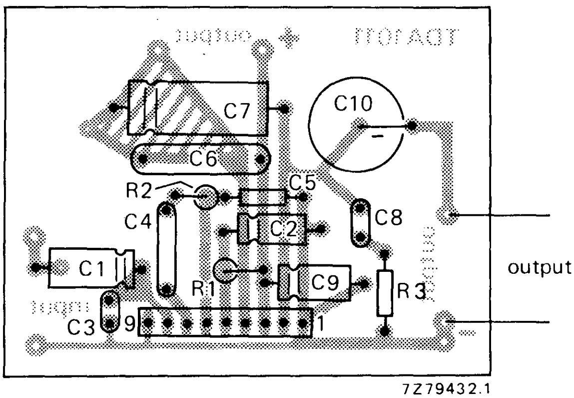


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

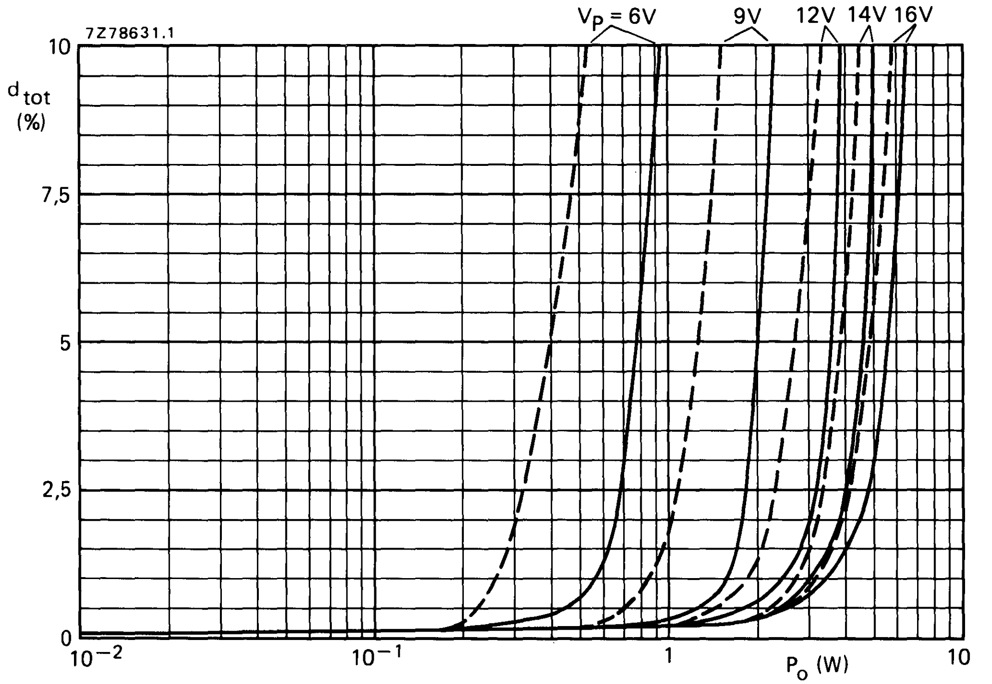


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; — — — without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

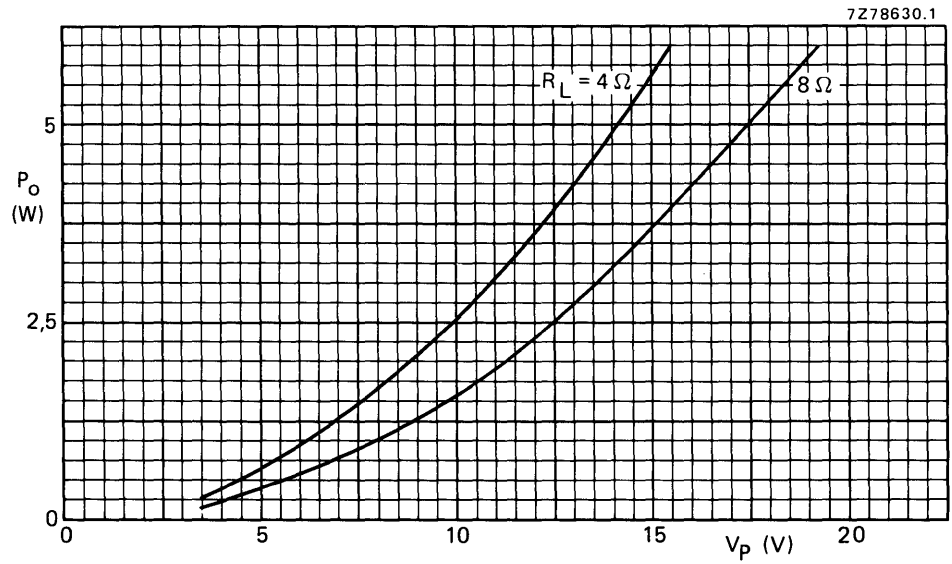


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

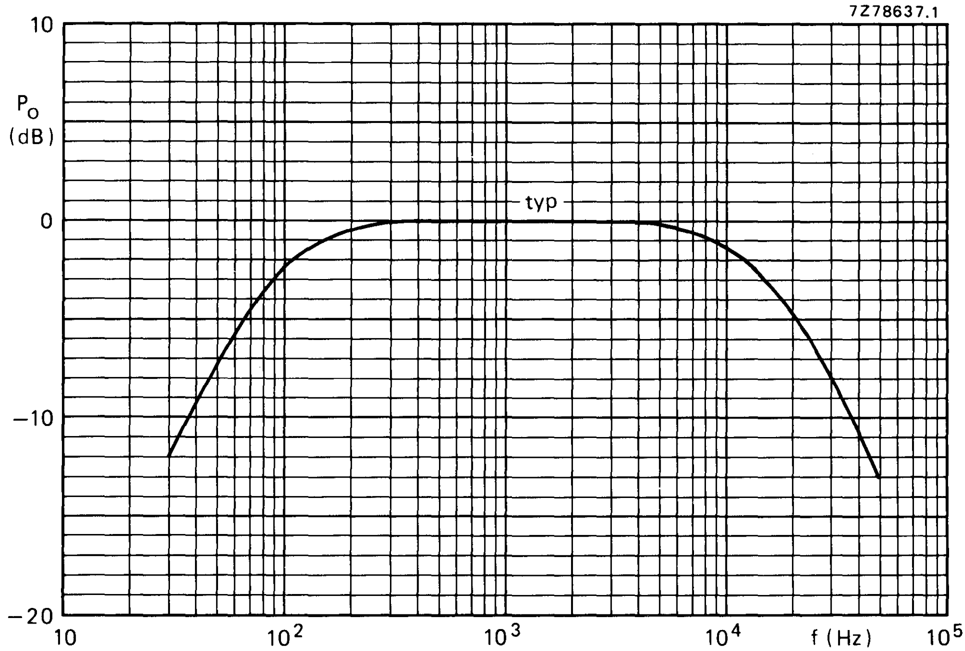


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

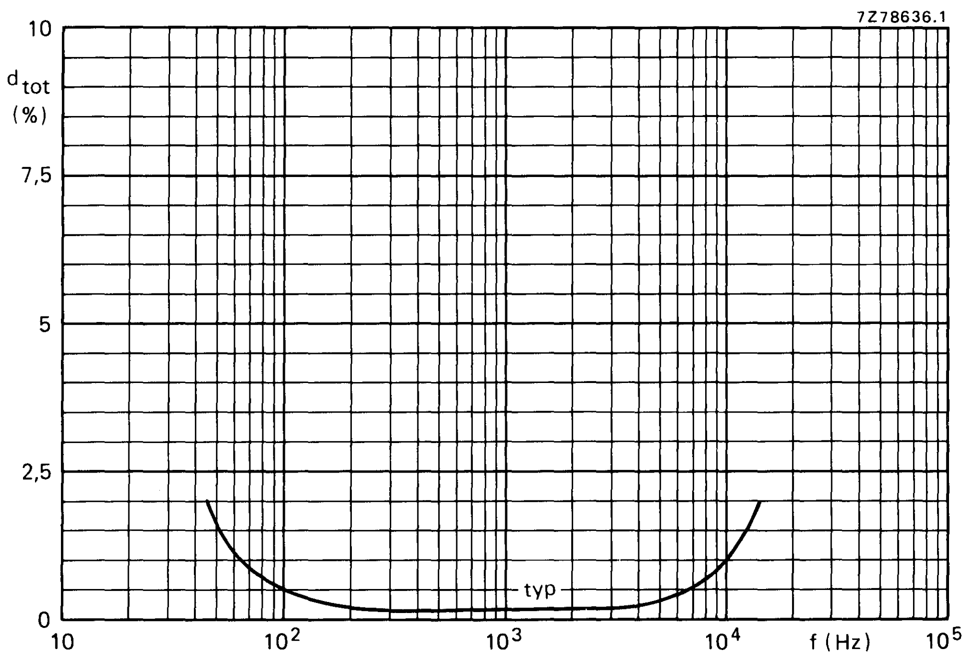


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

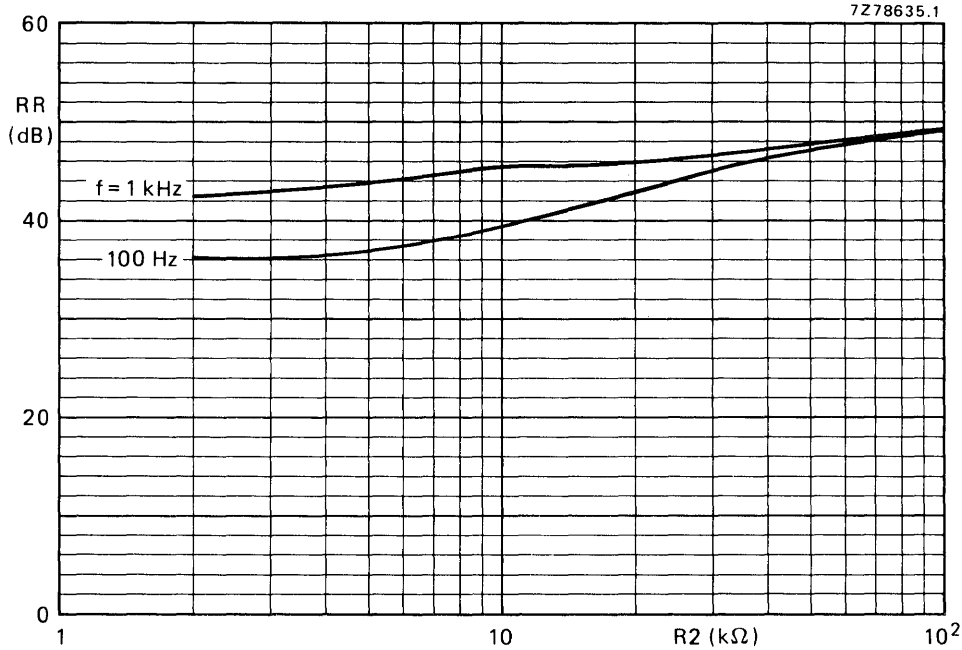


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

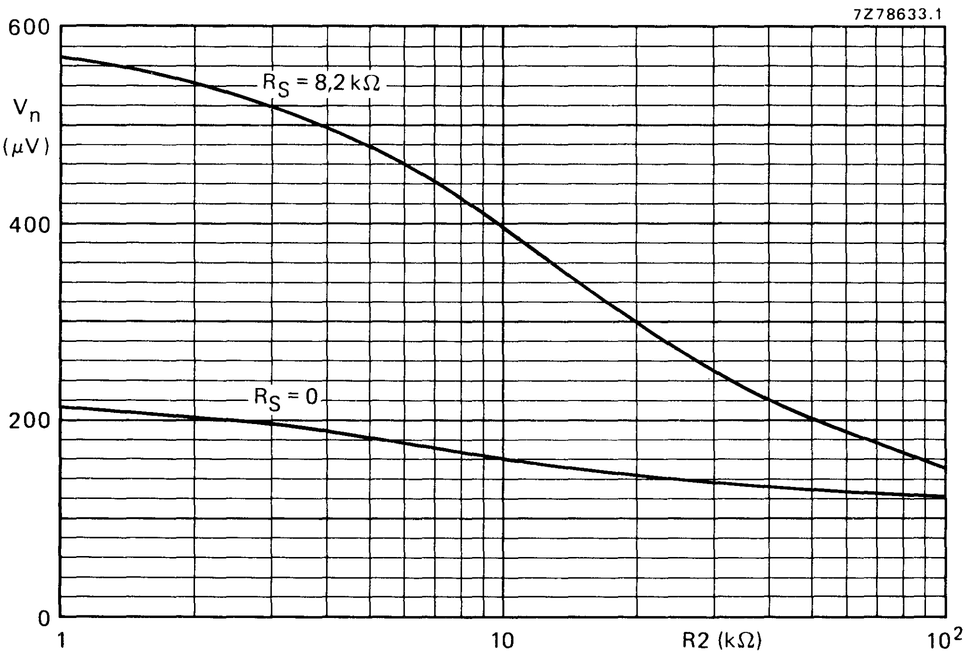


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

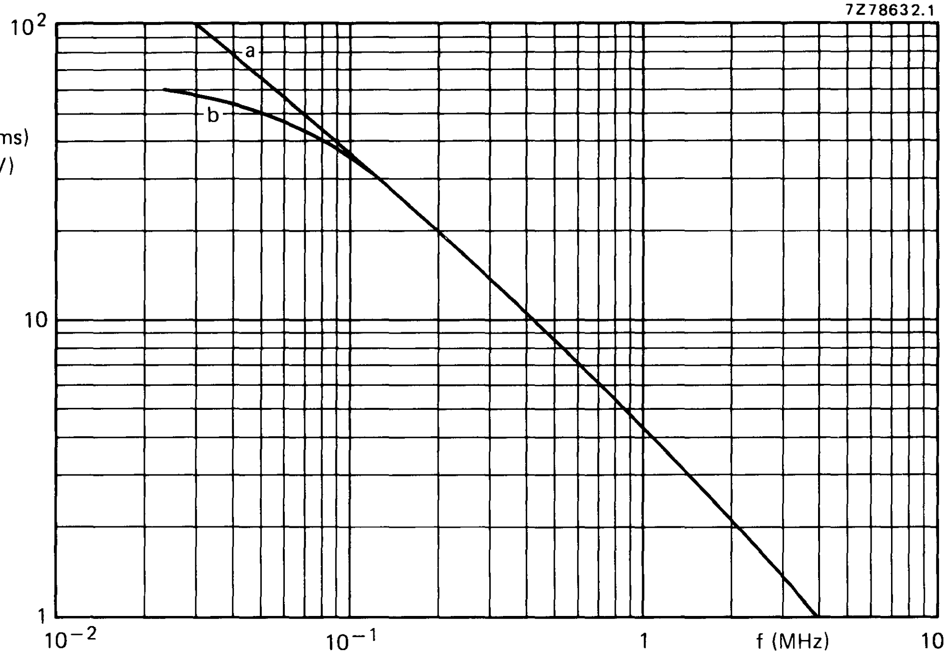


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

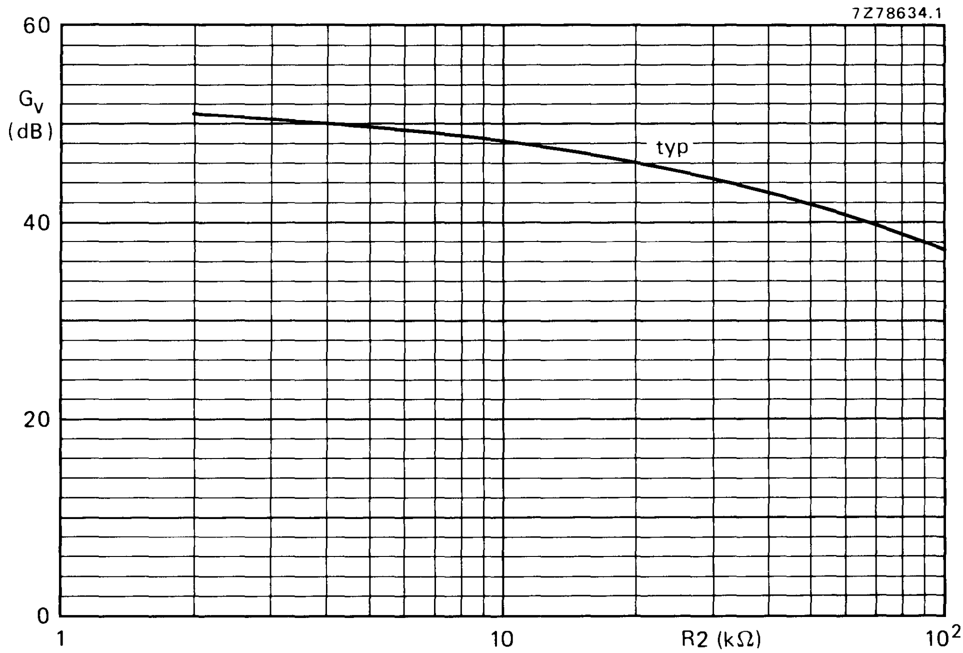


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_v\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

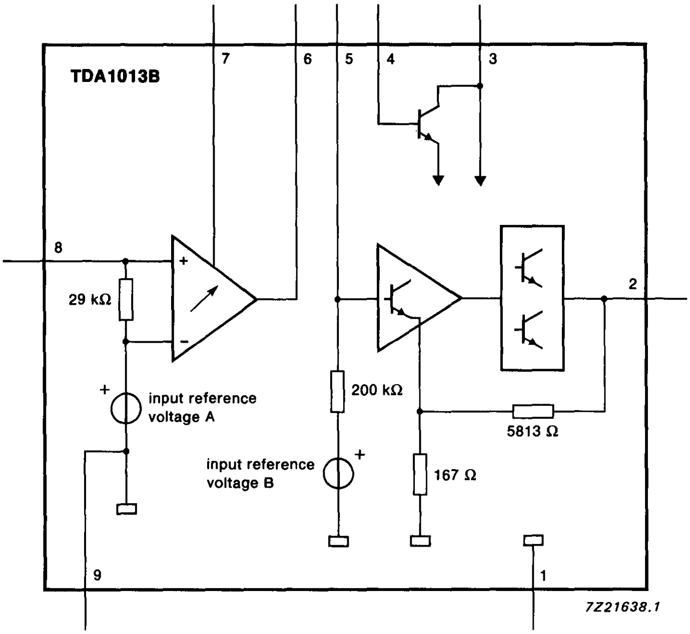


Fig.1 Block diagram.

PINNING

1 signal ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 power ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–65	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

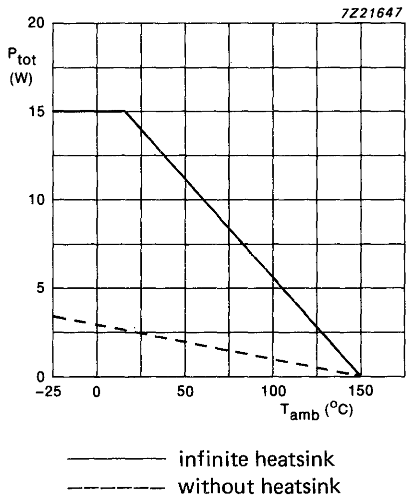


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ \text{K/W}$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

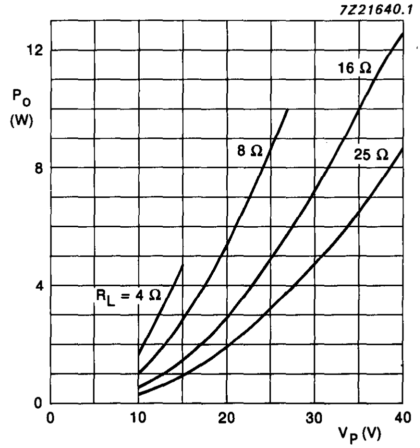


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

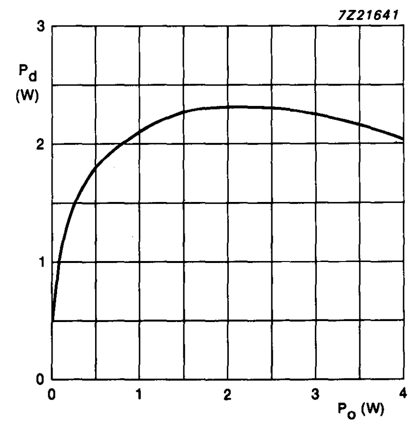


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

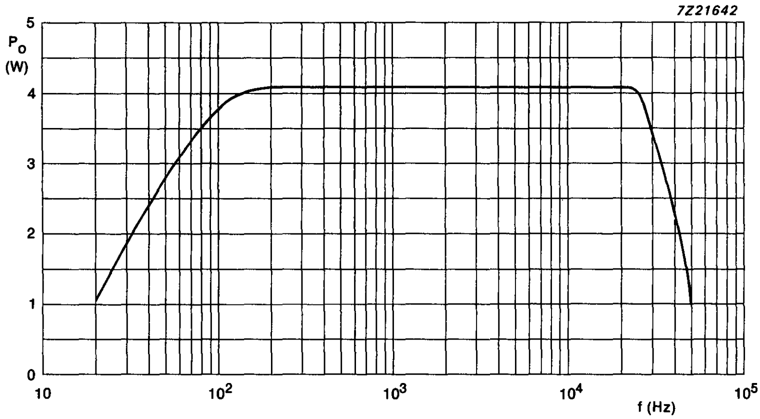


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω;
THD = 10% and control voltage (V_7) = 6.5 V.

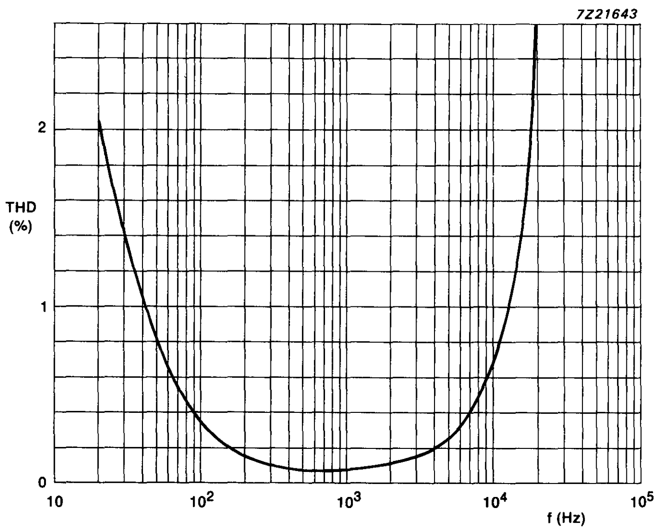


Fig.6 Total harmonic distortion as a function of frequency;
V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

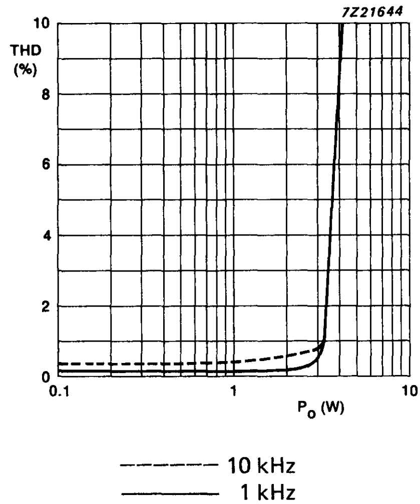


Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

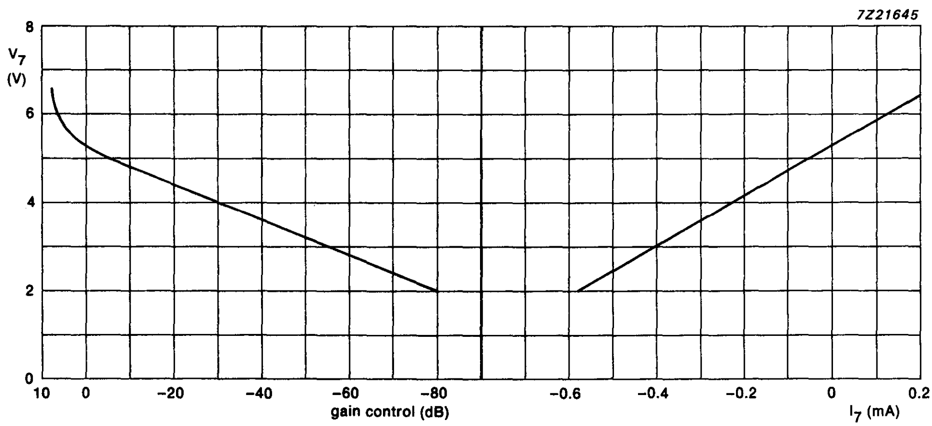


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

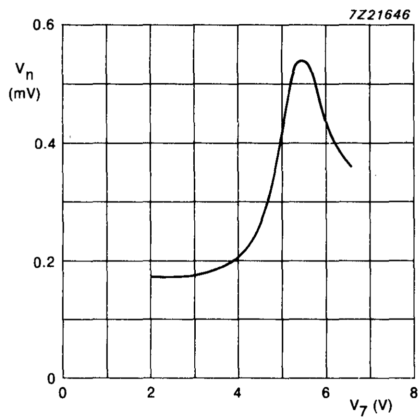
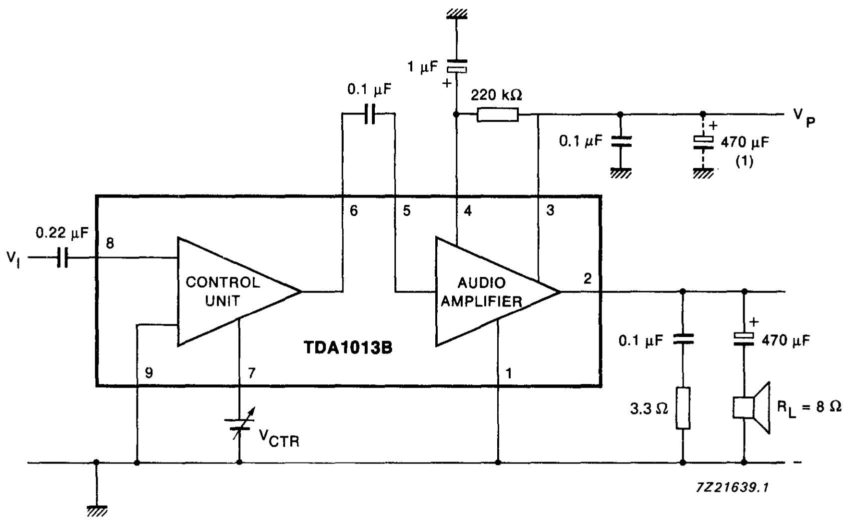


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

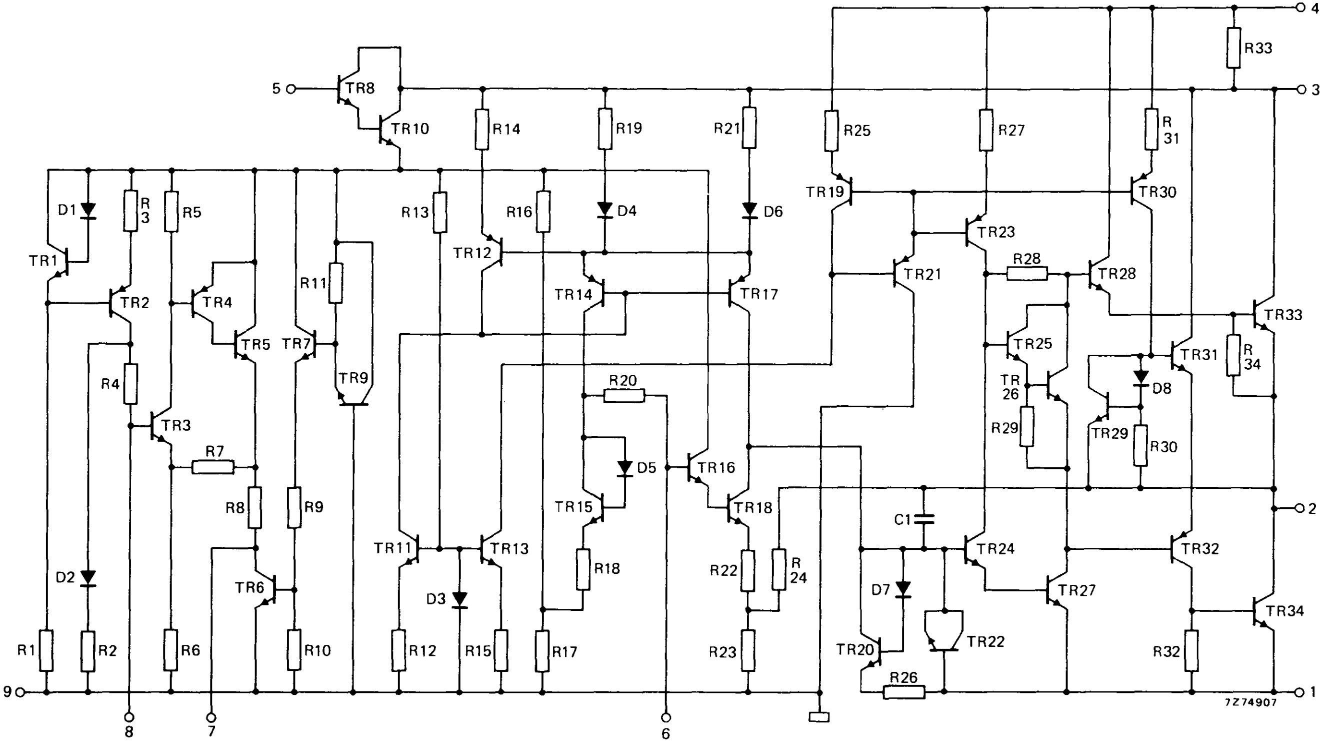


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	^oC
Operating ambient temperature	T_{amb}		−25 to + 150	^oC
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

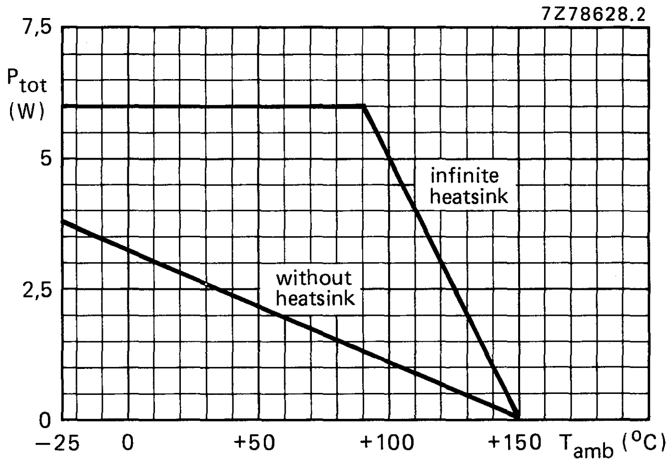


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 ^oC maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-45}{1,8} = 58 \text{ K/W.}$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 18	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	25	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
power amplifier	G_{v2}	typ.	29	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			49 to 55	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1,0	%
Frequency response; −3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ.	20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ.	0,8	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 100 Hz	RR	typ.	38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

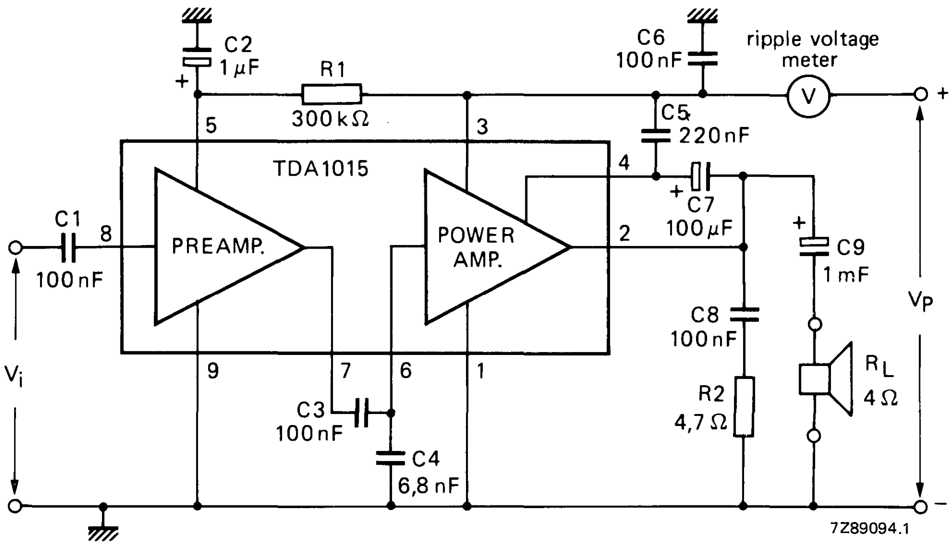


Fig. 3 Test circuit.

APPLICATION INFORMATION

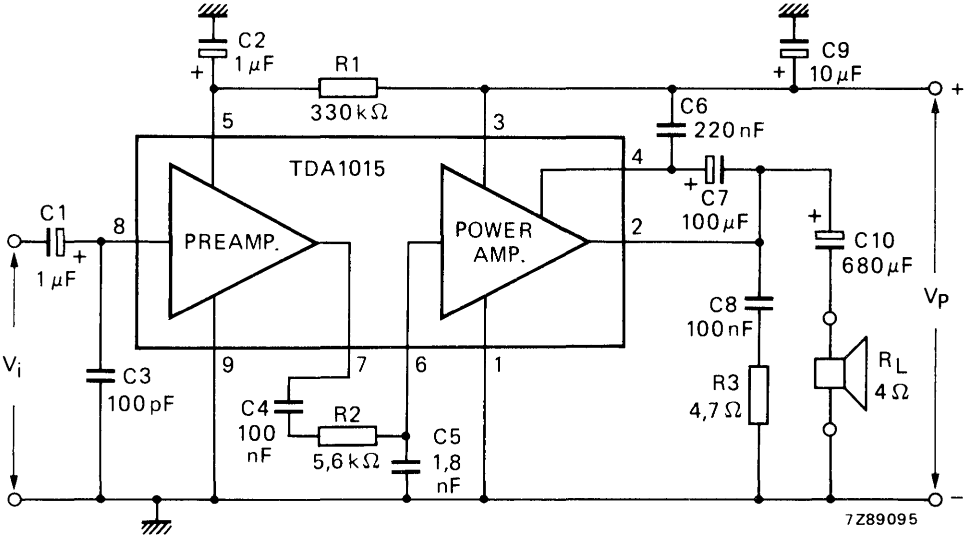


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

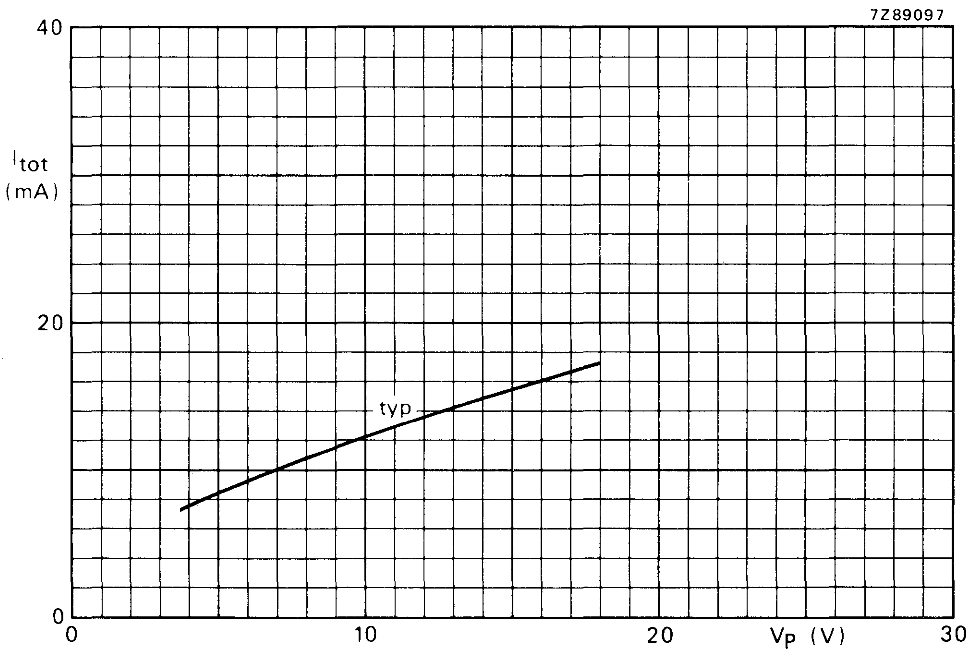


Fig. 5 Total quiescent current as a function of supply voltage.

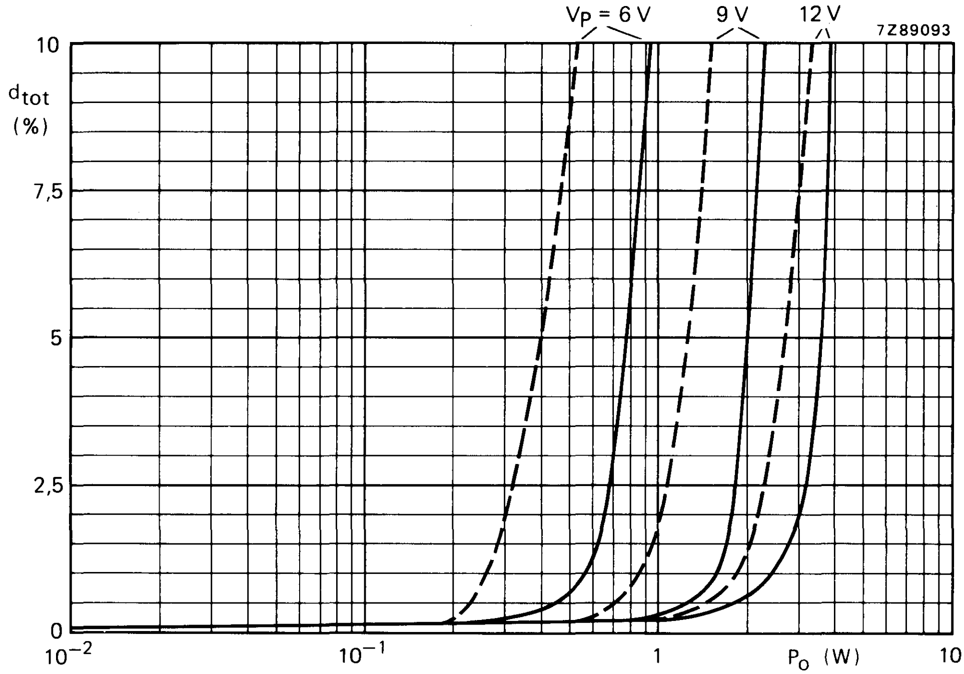


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

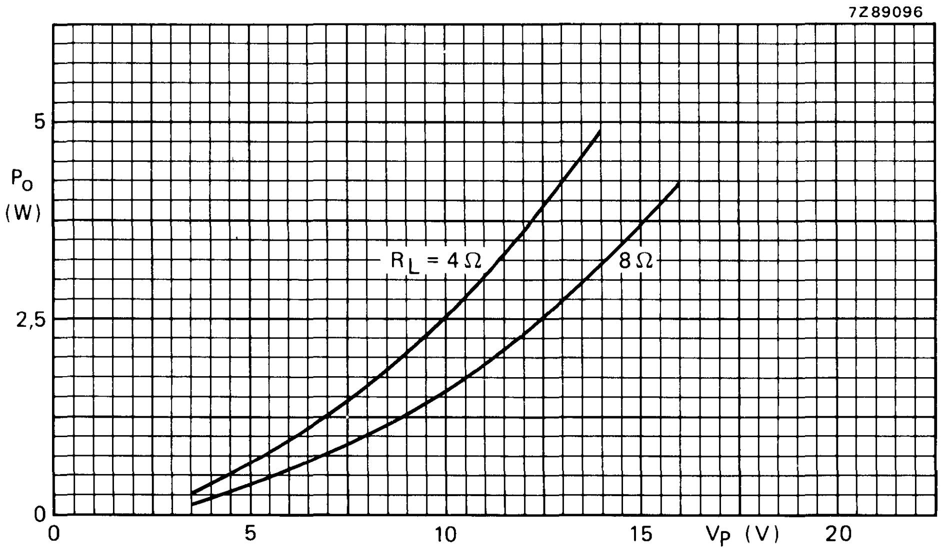


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

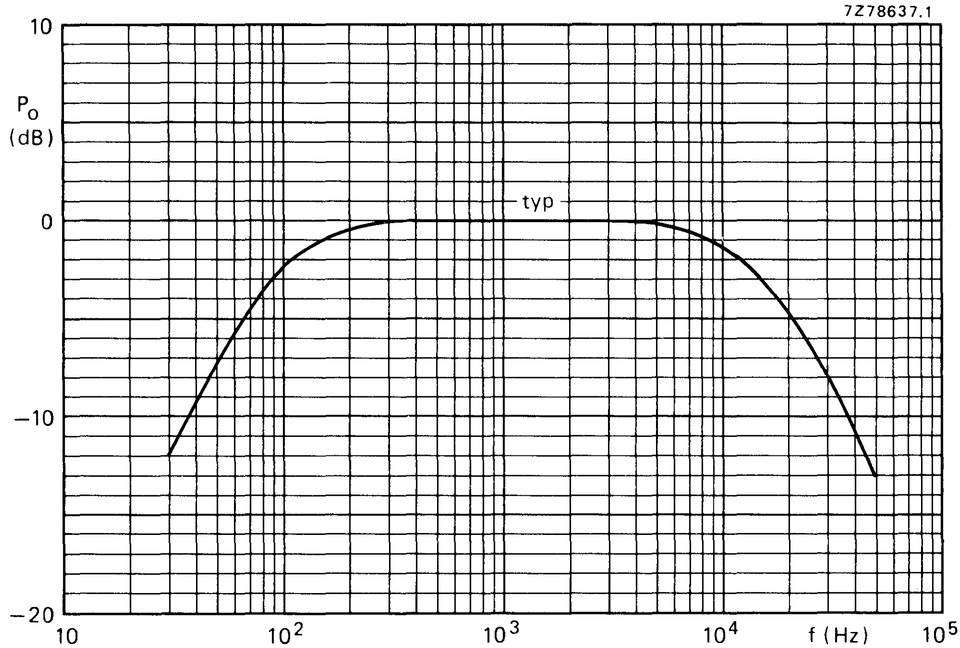


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

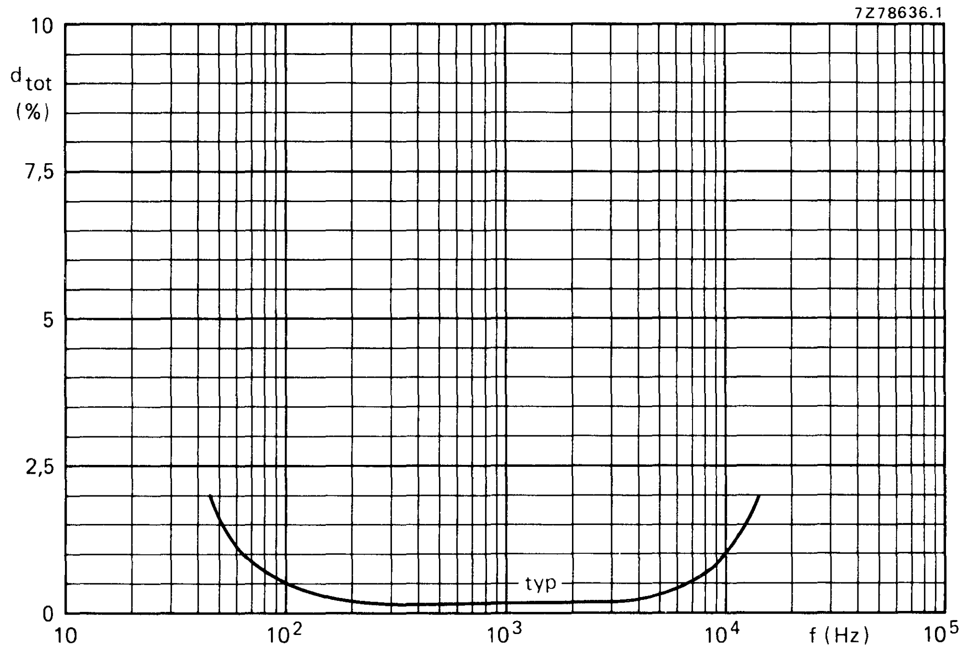


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

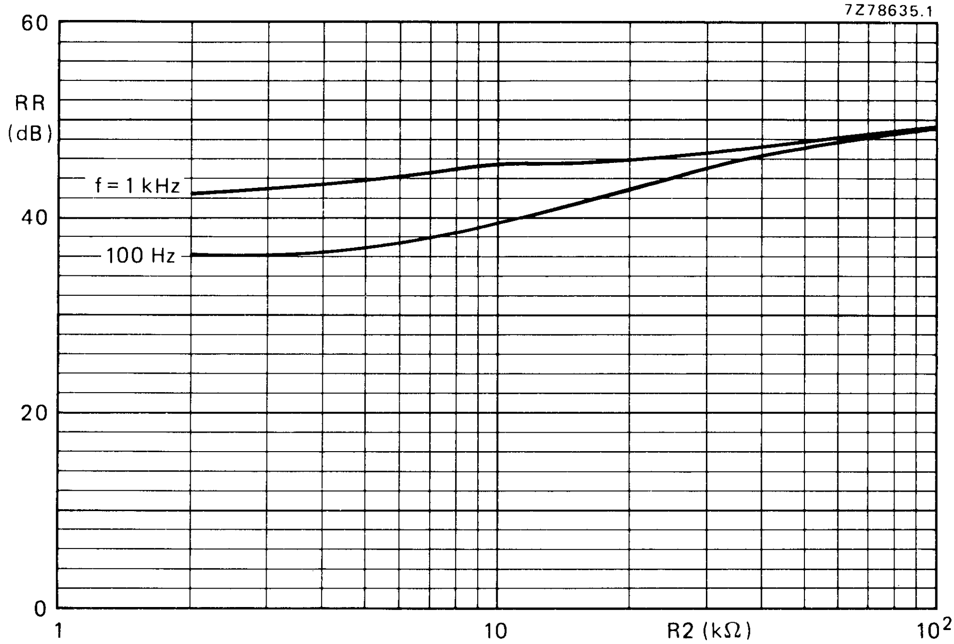


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

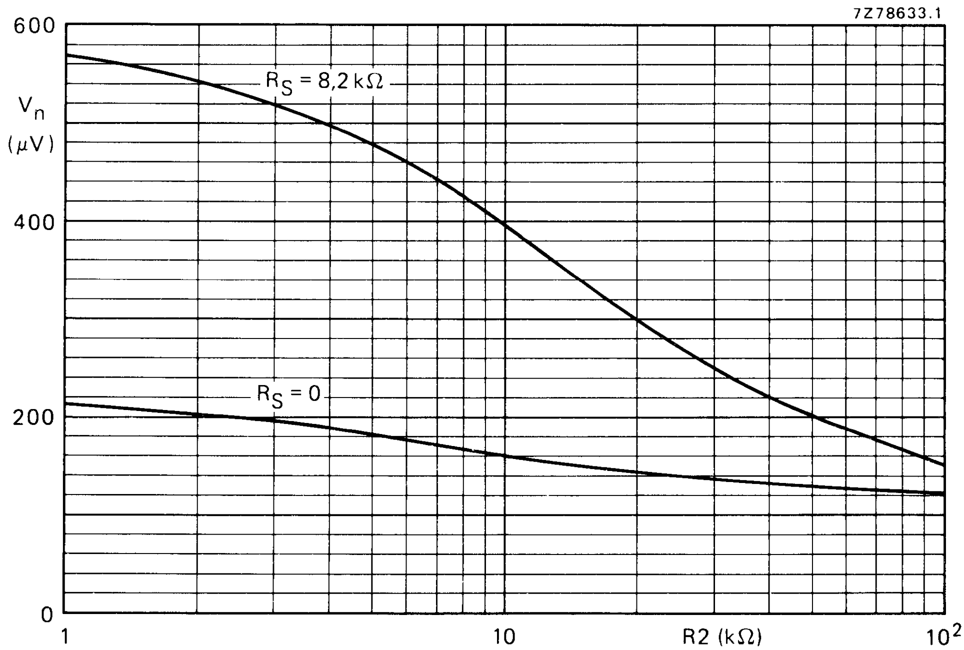


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

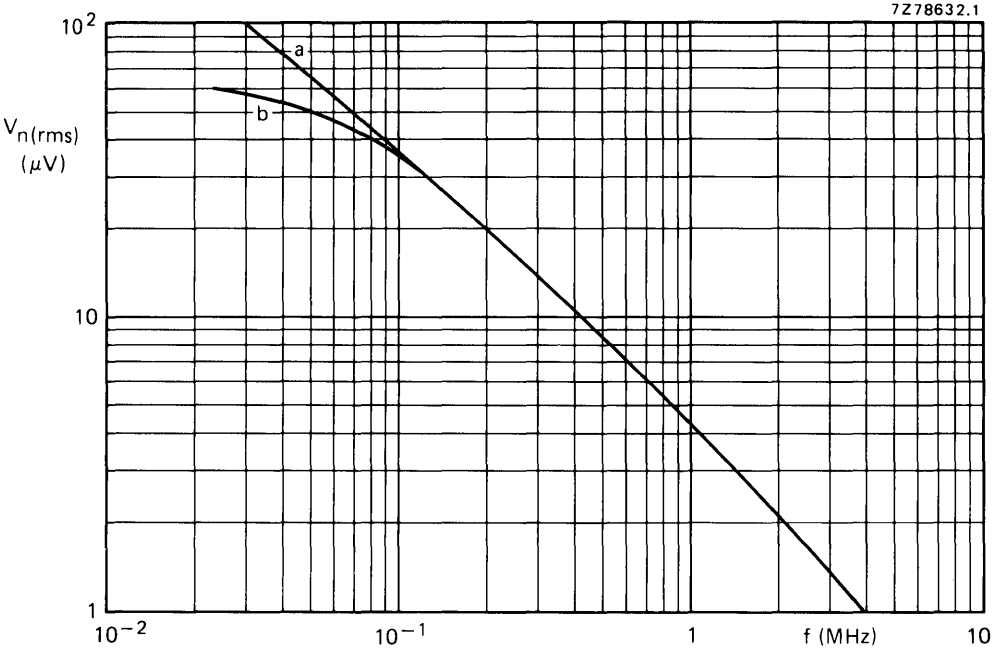


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

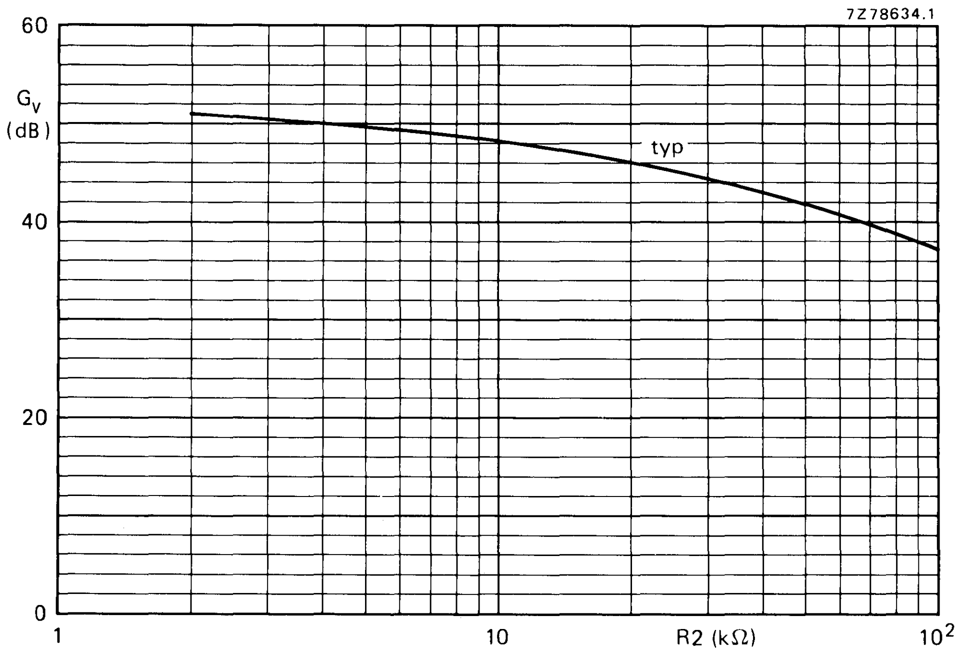


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	^oC
Storage temperature range	T_{stg}		−55 to +150	^oC

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

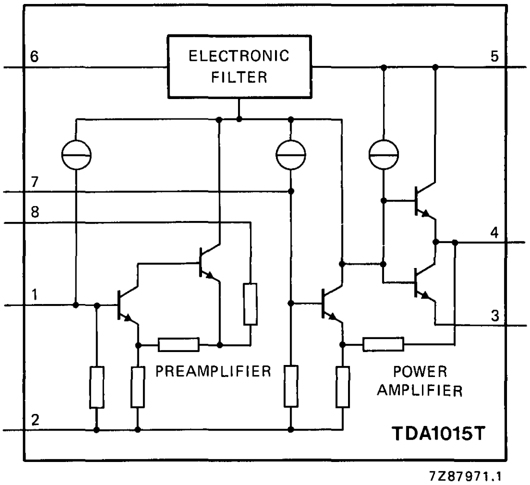


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12	V
Peak output current	I_{OM}	max.	1	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature range			−55 to +150	°C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1	hour

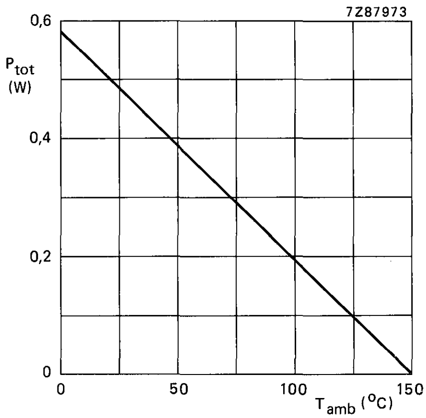


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at –3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

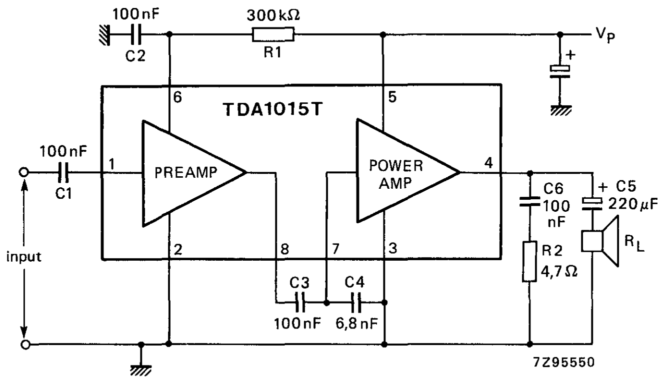


Fig. 3 Test circuit.

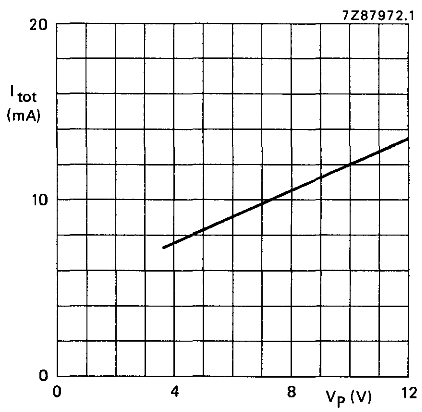


Fig. 4 Total quiescent current as a function of supply voltage.

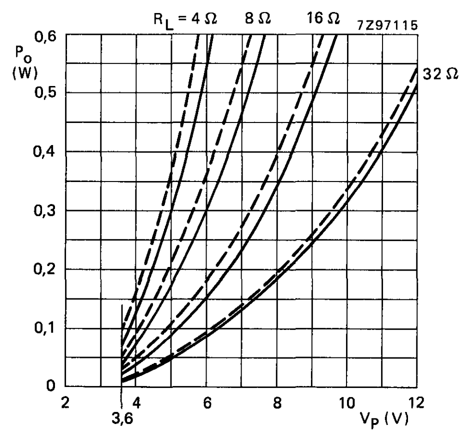


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

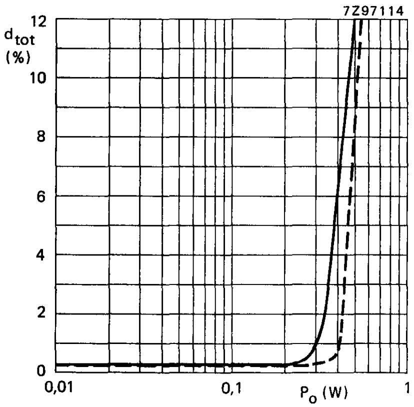


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

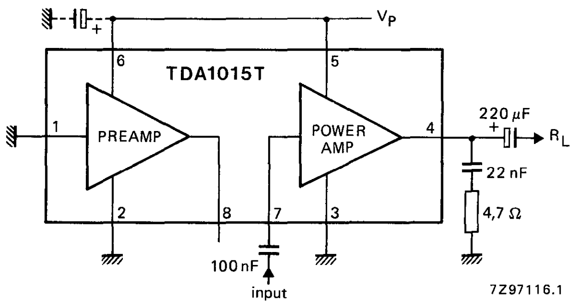


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

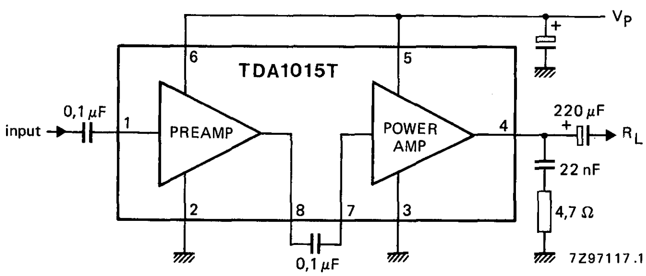


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\ tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

Features

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	typ.	10	mA
Operating ambient temperature range	T_{amb}		−25 to 150	°C
Power amplifier				
Output power at d_{tot} = 10%				
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2	W
Closed loop gain	G_c	typ.	36	dB
Preamplifier				
Open loop gain	G_o	min.	70	dB
Minimum closed loop voltage gain	$G_{c\,min}$	min.	35	dB
Output voltage at d_{tot} = 1%	V_o	min.	1	V
Automatic Level Control (A.L.C.)				
Gain variation for ΔV_i = 40 dB	ΔG_v	typ.	2	dB
Stabilized supply voltage				
Output voltage	$V_{5\text{-}16}$	typ.	2,6	V

PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT38).

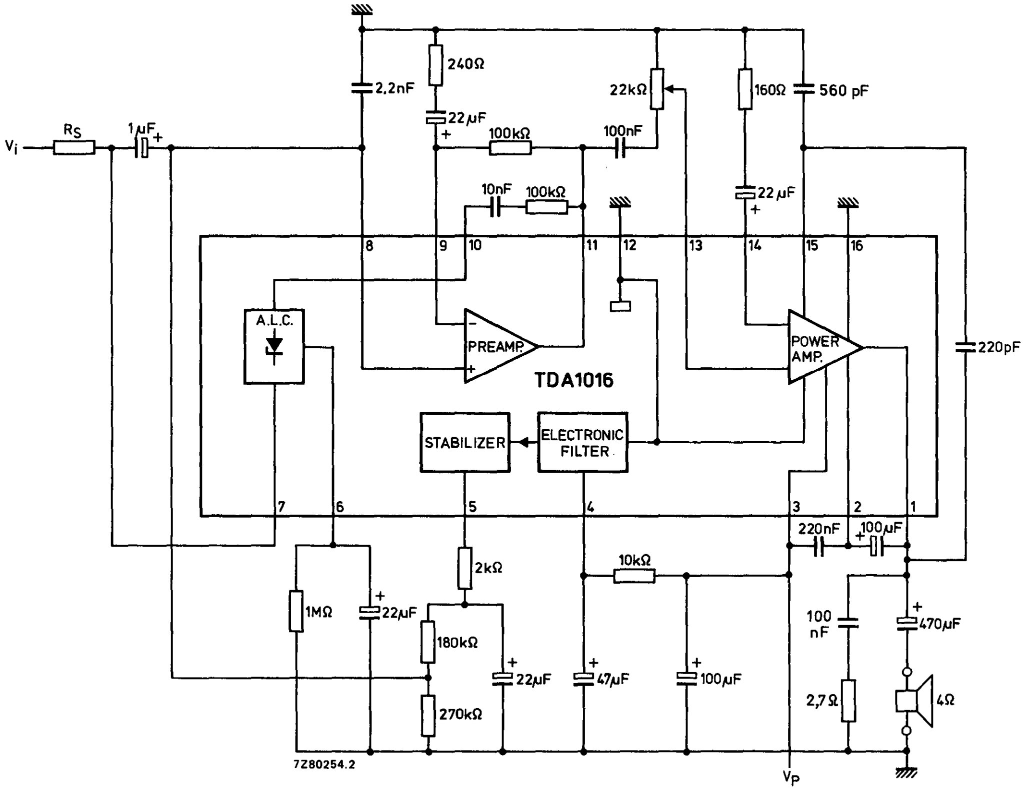


Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	V_P	max.	18	V
Repetitive peak output current	I_{ORM}	max.	1	A
Non-repetitive peak output current (pin 1)	I_{OSM}	max.	2	A
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sinewave drive; $V_P = 12$ V	t_{sc}	max.	100	hours
Crystal temperature	T_c	max.	150	°C
Storage temperature range	T_{stg}	–55 to + 150		°C
Operating ambient temperature range	T_{amb}	–25 to + 150		°C

THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient	$R_{th\ j\text{-}a}$	=	55	K/W

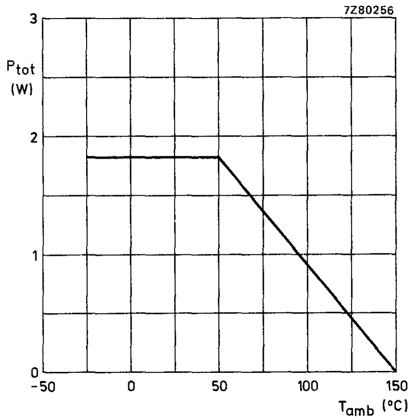


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = 6$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	V_P	3,6	6	15	V
Supply current; total quiescent at $V_P = 6$ V	I_{tot}	–	10	–	mA
Power amplifier					
Output power at $d_{tot} = 10\%$*					
$V_P = 6$ V	P_o	–	1	–	W
$V_P = 9$ V	P_o	–	2	–	W
Closed loop voltage gain	G_c	–	36	–	dB
Total harmonic distortion at $P_o = 0,5$ W	d_{tot}	–	–	1	%
Input impedance	$\lvert Z_i \rvert$	0,5	–	–	MΩ
Ripple rejection at f = 100 Hz ($R_S = 0\ \Omega$)	RR	40	50	–	dB
Noise output voltage (r.m.s. value) $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz	$V_{n(rms)}$	–	90	200	μV
Noise output voltage at 500 kHz $R_S = 0\ \Omega$; B = 5 kHz	V_n	–	8	–	μV
Preamplifier					
Open loop voltage gain at f = 10 kHz	G_o	70	78	–	dB
Closed loop voltage gain	G_c	–	52	–	dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\ min}$	35	–	–	dB
Output voltage at $d_{tot} = 1\%$	V_o	1	–	–	V
Output voltage with A.L.C. $V_i = 2$ mV	V_o	0,45	0,5	0,55	V
Total harmonic distortion with A.L.C.					
$V_i = 2$ mV	d_{tot}	–	–	1	%
$V_i = 360$ mV	d_{tot}	–	–	3	%
Signal-to-noise ratio related to $V_i = 1,2$ mV; $R_S = 1\ k\Omega$; B = 60 Hz to 15 kHz	S/N	–	60	–	dB
Input impedance	$\lvert Z_i \rvert$	100	–	–	kΩ
Ripple rejection at f = 100 Hz; $R_S = 0\ \Omega$	RR	50	54	–	dB
Output impedance **	$\lvert Z_o \rvert$	–	–	50	Ω

* Measured with an ideal coupling capacitor connected to the speaker load.
** I_P (effective value) must not exceed 1 mA.

parameter	symbol	min.	typ.	max.	unit
Automatic Level Control (A.L.C.) (see Fig. 3)**					
Gain variation for ΔV_i = 45 dB	ΔG_v	–	2	3	dB
Limiting time*	t_l	–	–	50	ms
Level setting time*	t_s	–	–	50	ms
Recovery time* ▲	t_r	–	100	–	s
Voltage stabilizer					
Output voltage	$V_{11\text{-}15}$	–	2,6	–	V
Load current	I_{11}	–	–	1,5	mA
Ripple rejection at f = 100 Hz	RR	40	–	–	dB

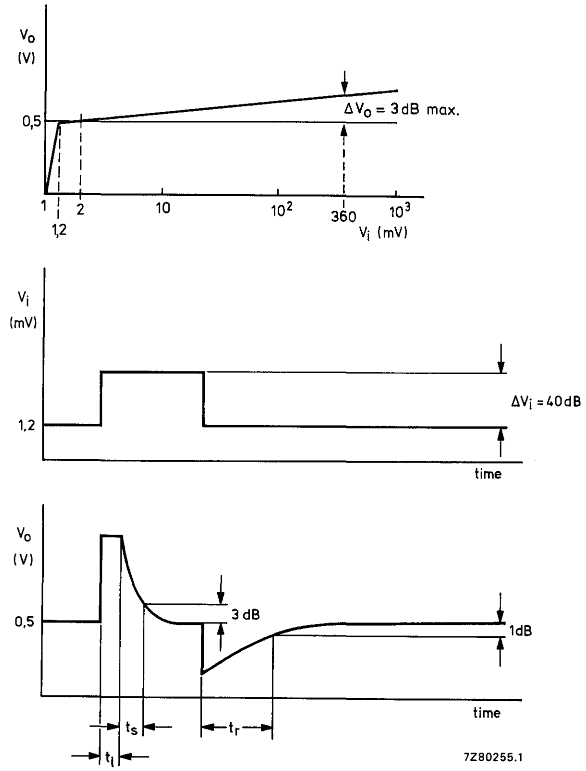


Fig. 3 Typical A.L.C. curve with R_S = 10 kΩ.

* At ΔV_i = 40 dB with respect to V_i = 1,2 mV.

** The A.L.C. tracking in stereo has a typical spread of 1 dB if pins 6 of both ICs are connected to the same RC network.

▲ Without a shunt resistor across A.L.C.
With 1 MΩ or 2,2 MΩ across A.L.C. recovery time becomes 22 or 50 seconds.

12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Output power at d_{tot} = 10% (with bootstrap)				
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10	W
		typ.	12	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5	W
Output power at d_{tot} = 10% (without bootstrap)				
V_P = 14,4 V; R_L = 4 Ω	P_o	>	4,5	W
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	typ.	40	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	40	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	30	mA
Stand-by current	I_{sb}	<	1	mA
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

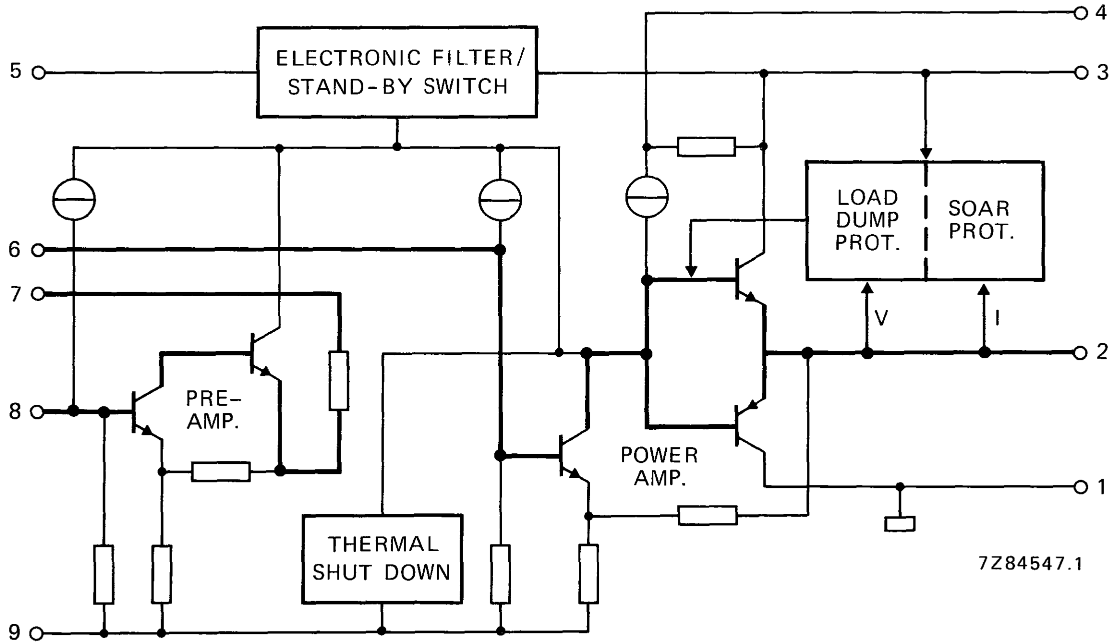


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18	V
Supply voltage; non-operating	V_P	max.	28	V
Supply voltage; load dump	V_P	max.	45	V
Non-repetitive peak output current	I_{OSM}	max.	6	A
Total power dissipation	see derating curves Fig. 2			
Storage temperature range	T_{stg}	−55 to + 150		°C
Crystal temperature	T_c	max.	150	°C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100	hours

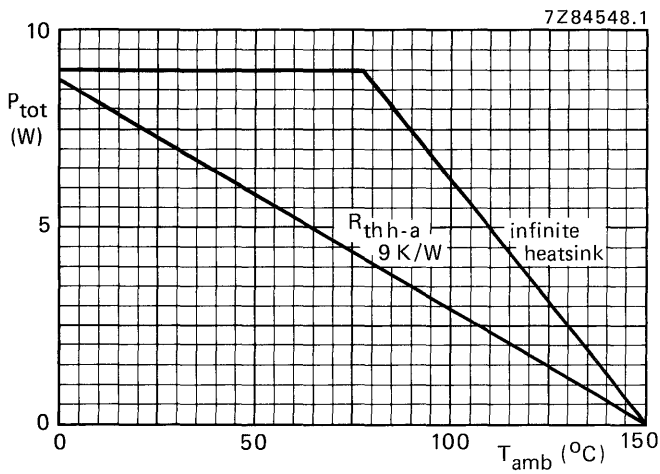


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-60}{5,2} = 17,3\ \text{K/W}$$

Since $R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} = 8$ K/W, $R_{th\,h\text{-}a} = 17,3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Total quiescent current				
at V_P = 14,4 V	I_{tot}	typ.	30	mA
at V_P = 18 V	I_{tot}	typ.	40	mA

A.C. CHARACTERISTICS

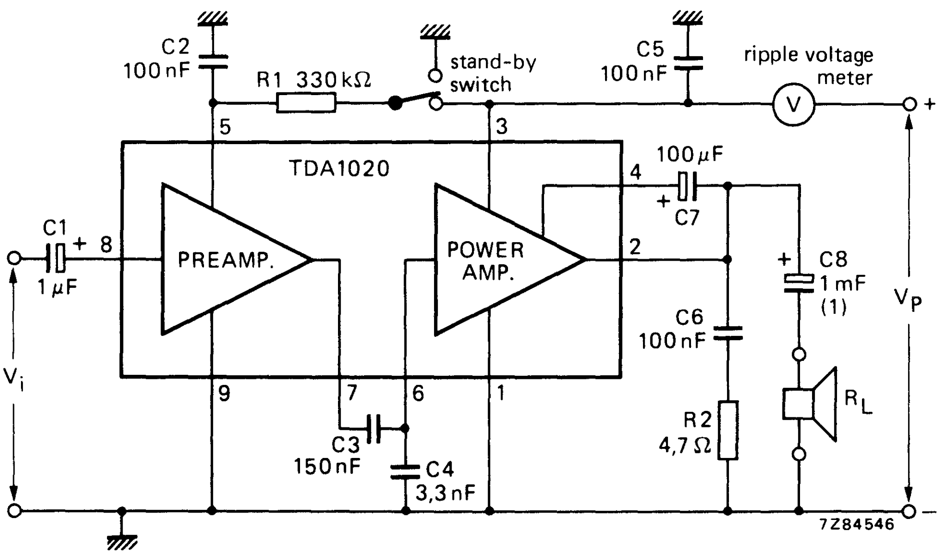
T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

Output power at d_{tot} = 10%; with bootstrap (note 1)				
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10	W
		typ.	12	W
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6	W
		typ.	7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5	W
Output power at d_{tot} = 1%; with bootstrap (note 1)				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,5	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3	W
Output voltage (r.m.s. value)				
R_L = 1 kΩ; d_{tot} = 0,5%	$V_{o(rms)}$	typ.	5	V
Output power at d_{tot} = 10%; without bootstrap	P_o	>	4,5	W
Voltage gain				
preamplifier (note 2)	G_{v1}	typ.	17,7	dB
			16,7 to 18,7	dB
power amplifier	G_{v2}	typ.	29,5	dB
			28,5 to 30,5	dB
total amplifier	$G_{v\,tot}$	typ.	47	dB
			46,2 to 48,2	dB
Input impedance				
preamplifier	$\lvert Z_i \rvert$	typ.	40	kΩ
			28 to 52	kΩ
power amplifier	$\lvert Z_i \rvert$	typ.	40	kΩ
			28 to 52	kΩ
Output impedance				
preamplifier	$\lvert Z_o \rvert$	typ.	2,0	kΩ
			1,4 to 2,6	kΩ
power amplifier	$\lvert Z_o \rvert$	typ.	50	mΩ
Output voltage (r.m.s. value) at d_{tot} = 1%				
preamplifier (note 2)	$V_{o(rms)}$	>	1	V
		typ.	1,5	V
Frequency response	B		50 Hz to 25	kHz
Noise output voltage (r.m.s. value; note 3)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3	mV
		<	0,5	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,5	mV
		<	1,0	mV

Ripple rejection (note 4)			
at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	>	48 dB
		typ.	54 dB
Bootstrap current at onset of clipping (pin 4)			
R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

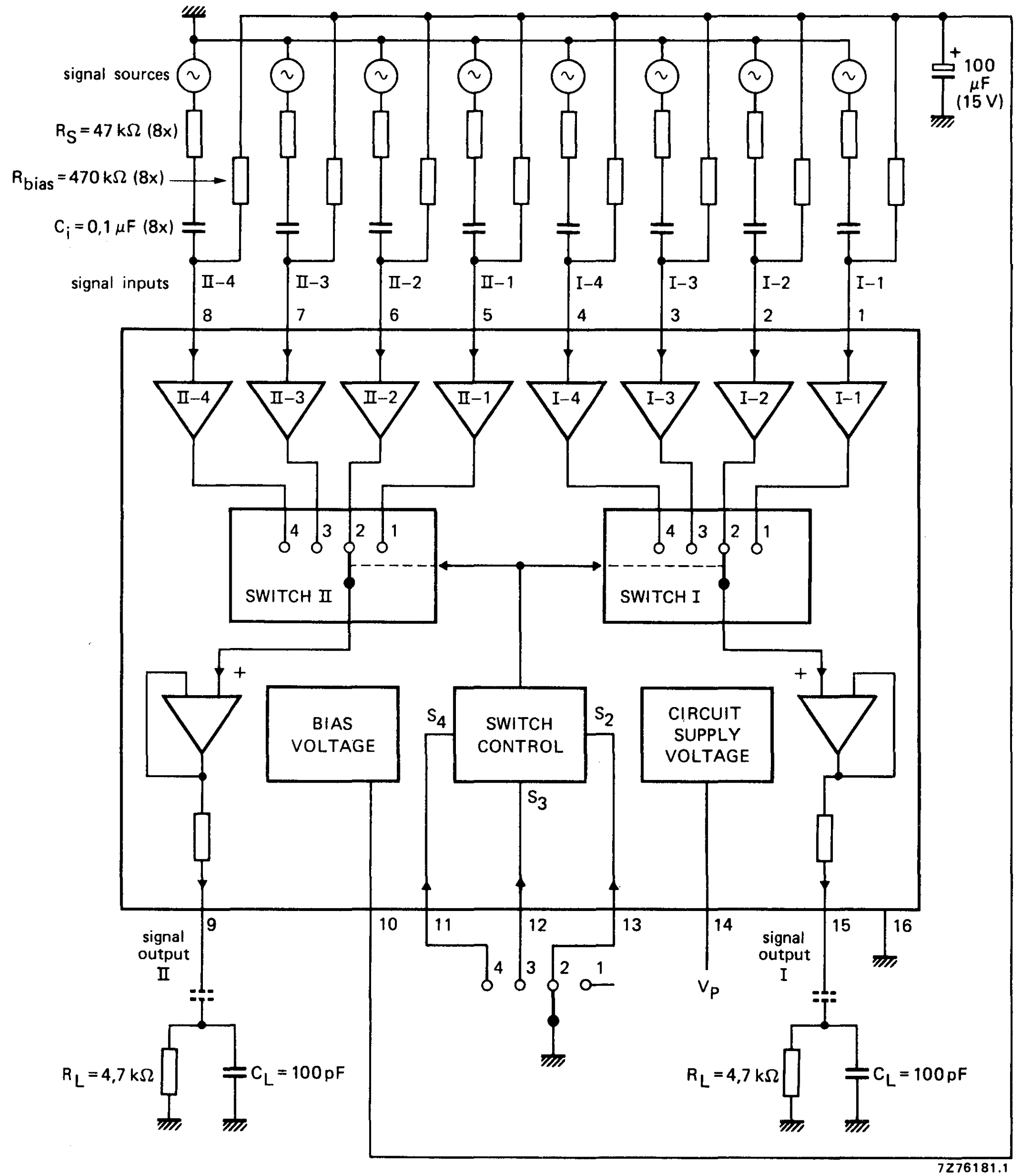


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V

Signal inputs

Input offset voltage of switched-on inputs $R_S \leqslant 1\ k\Omega$	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10\ k\Omega$	SVRR	typ.	100	µV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	µV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1\ k\Omega$; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)} = 1$ V; $R_S = 1$ kΩ; $R_L = 10$ MΩ; $C_L = 10$ pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ $R_L = 10$ MΩ; $C_L = 10$ pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	V_{10-16}	typ.	11 V *
			10,2 to 11,8 V
Output resistance	R_{10-16}	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		V_{11-16}	V_{12-16}	V_{13-16}
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1,5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* V_{10-16} is typically $0,5 \cdot V_{14-16} + 1,5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ.	10	mV
		<	100	mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	>	5,0	V
		typ.	5,3	V
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

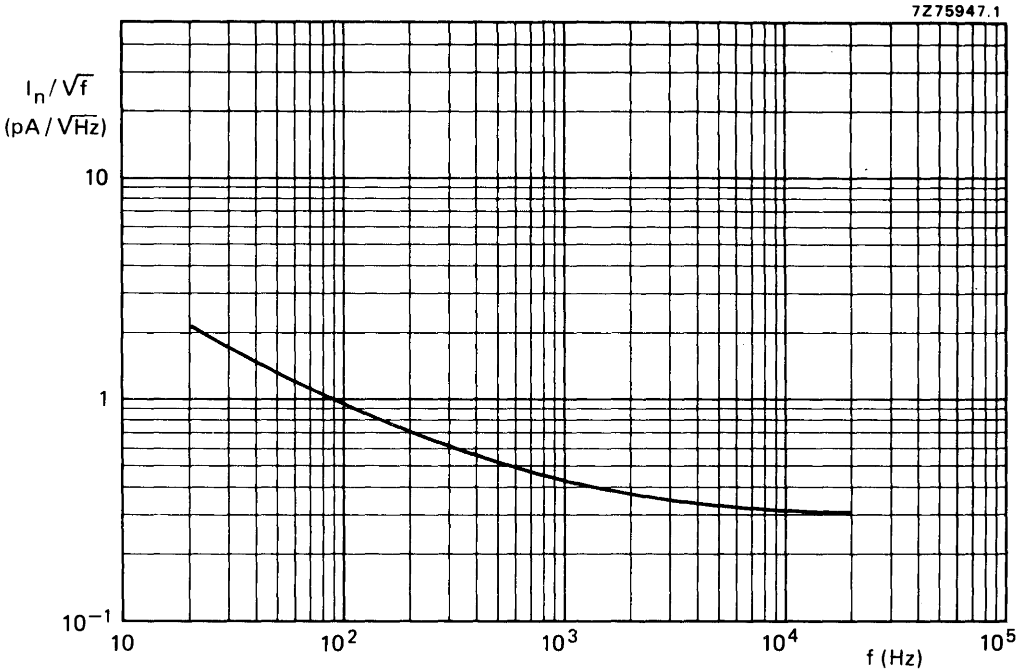


Fig. 2 Equivalent input noise current.

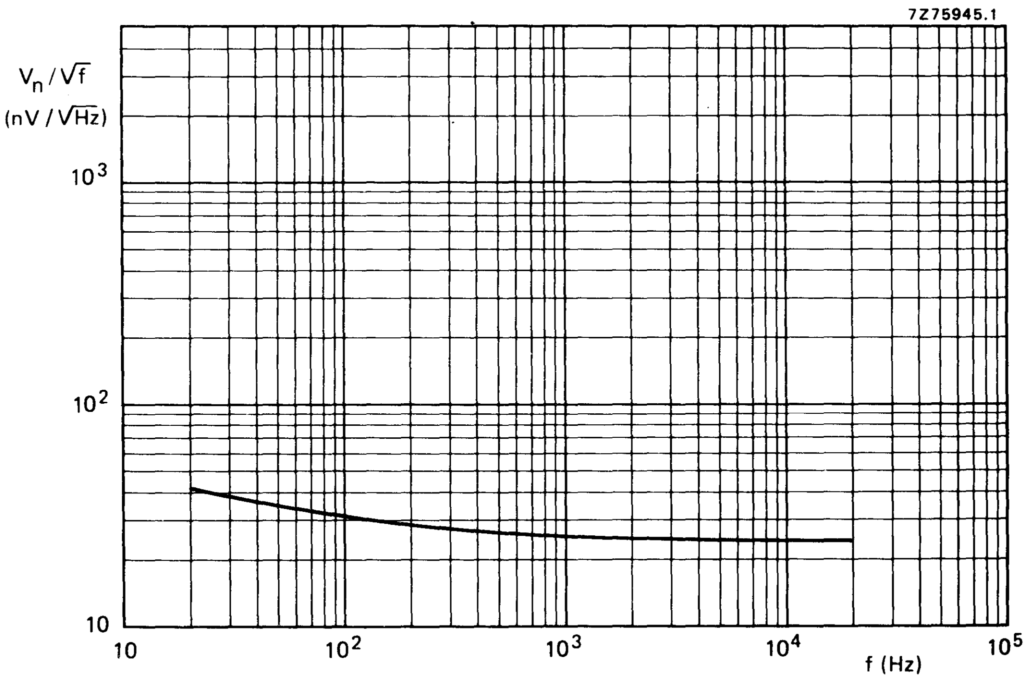


Fig. 3 Equivalent input noise voltage.

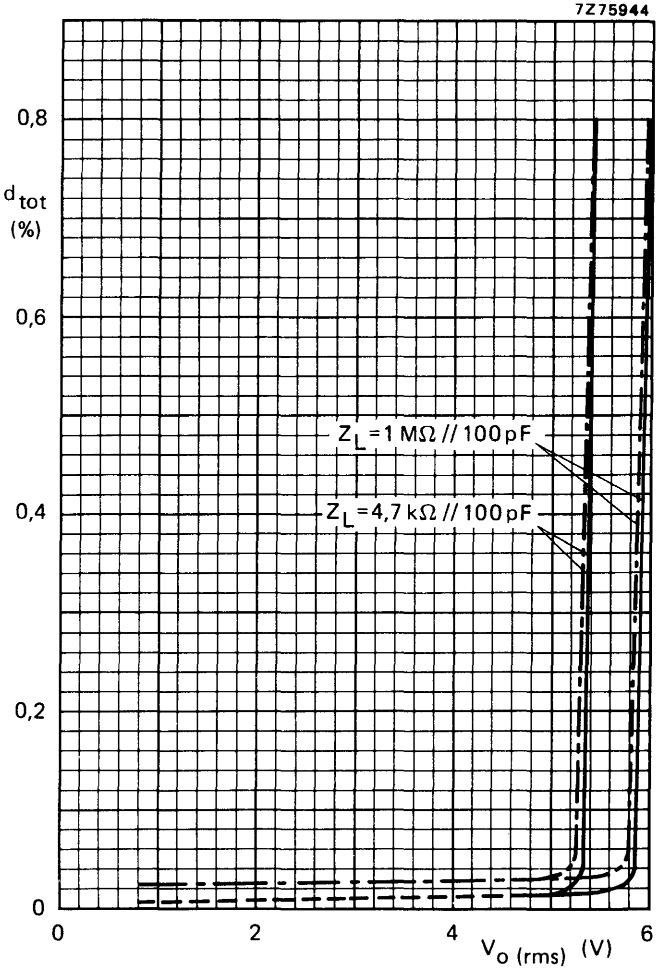


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

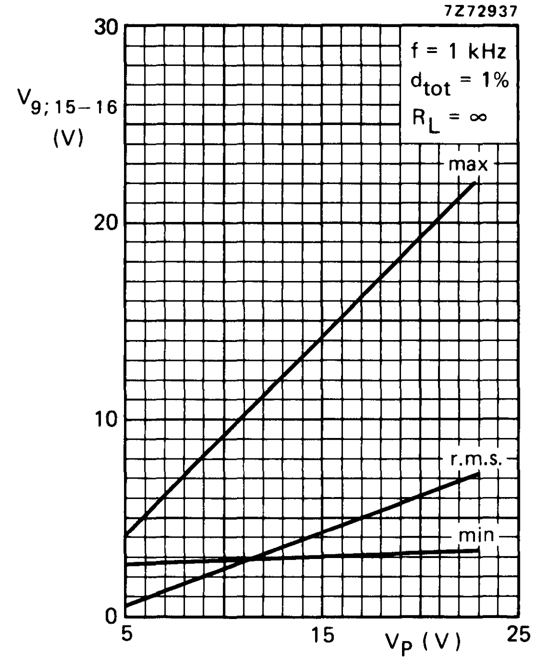


Fig. 5 Output voltage as a function of supply voltage.

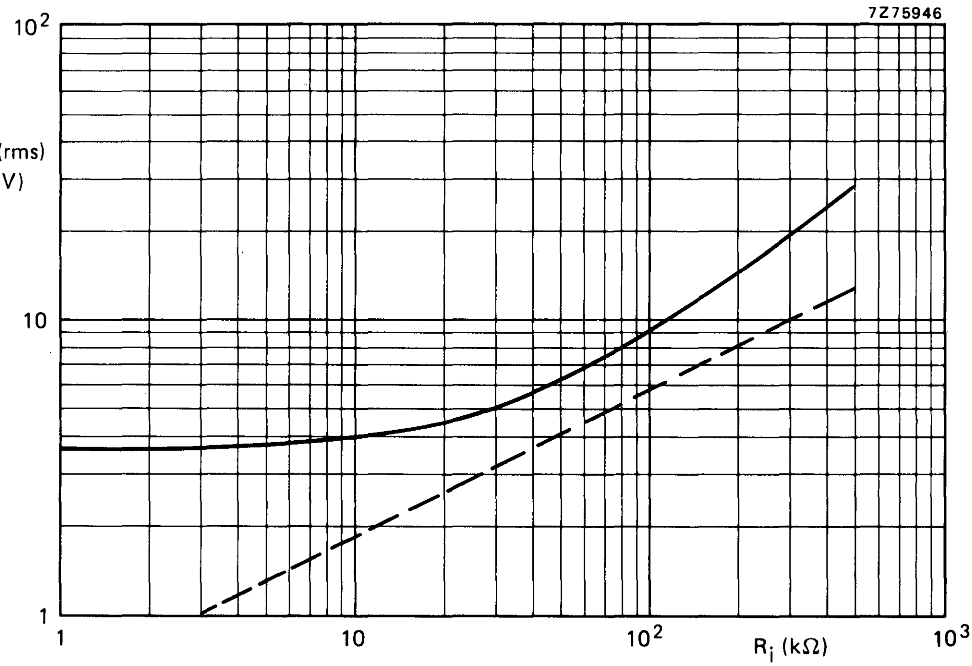


Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

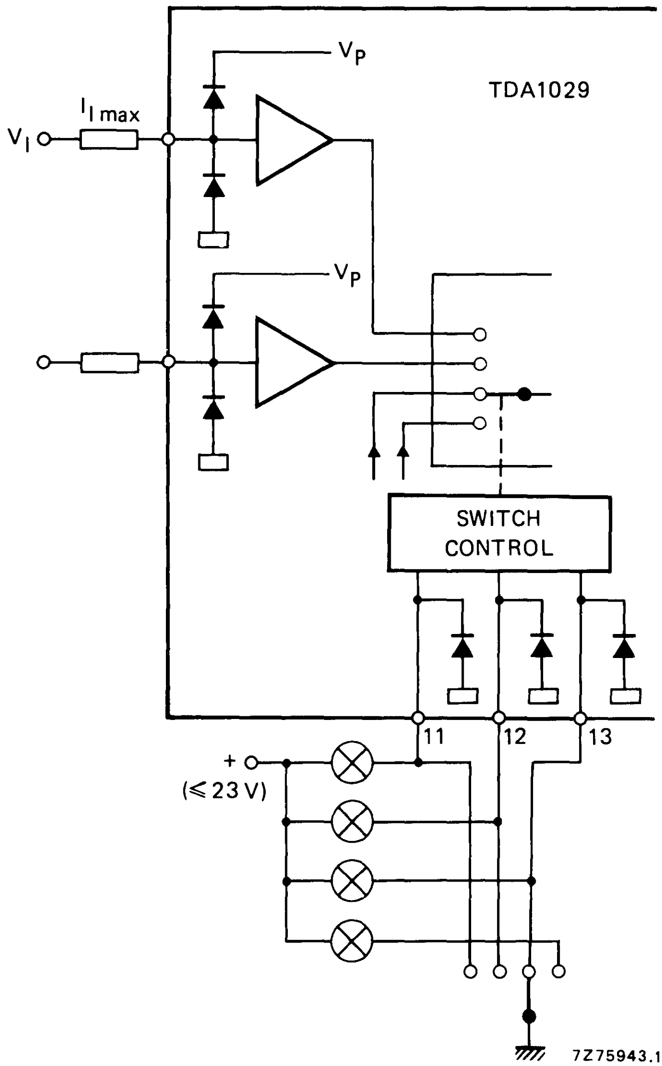


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

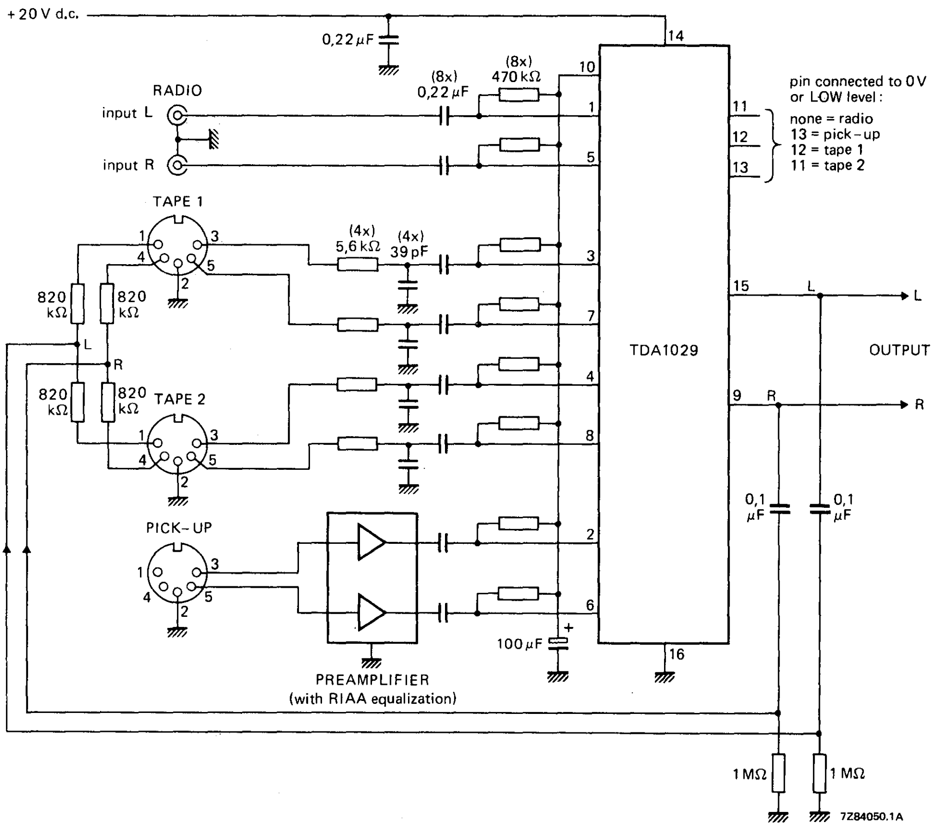


Fig. 8 TDA1029 connected as a four input stereo source selector.

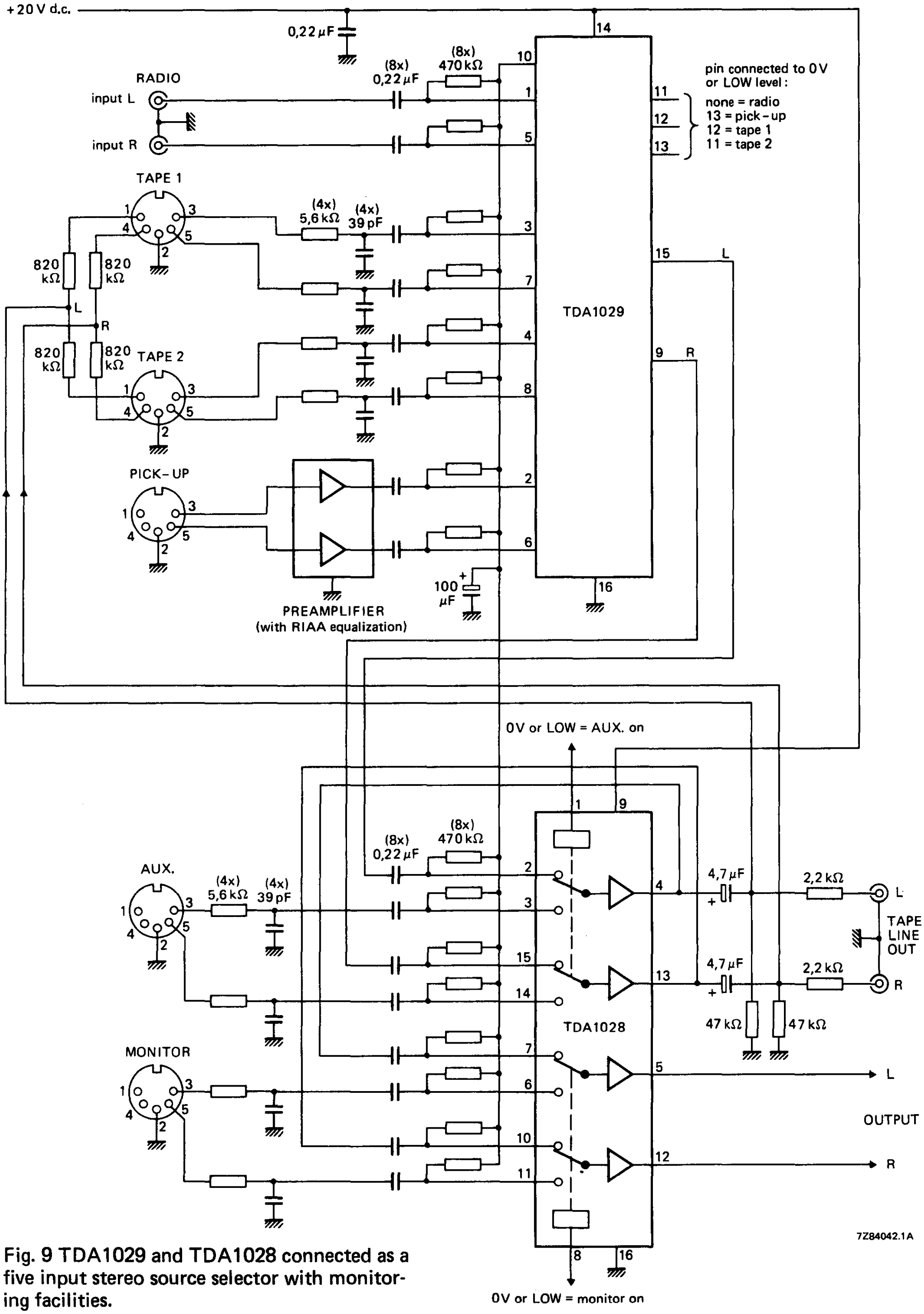


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

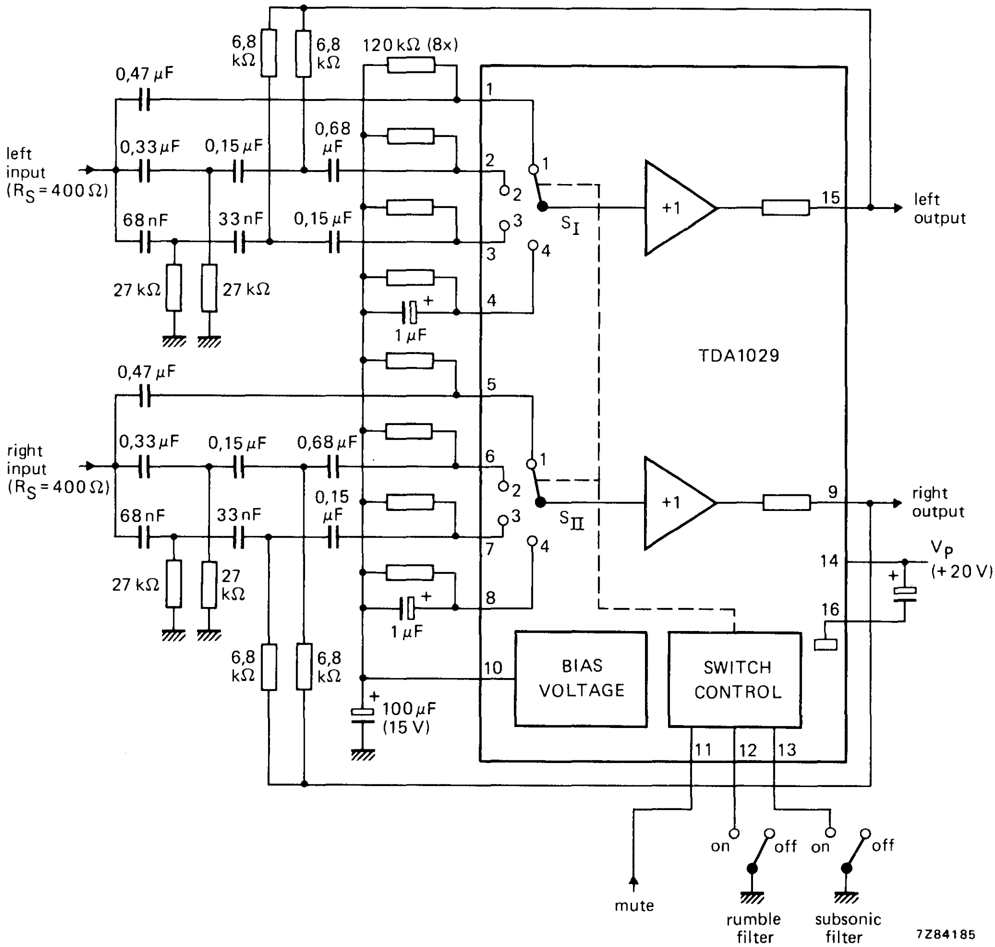


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

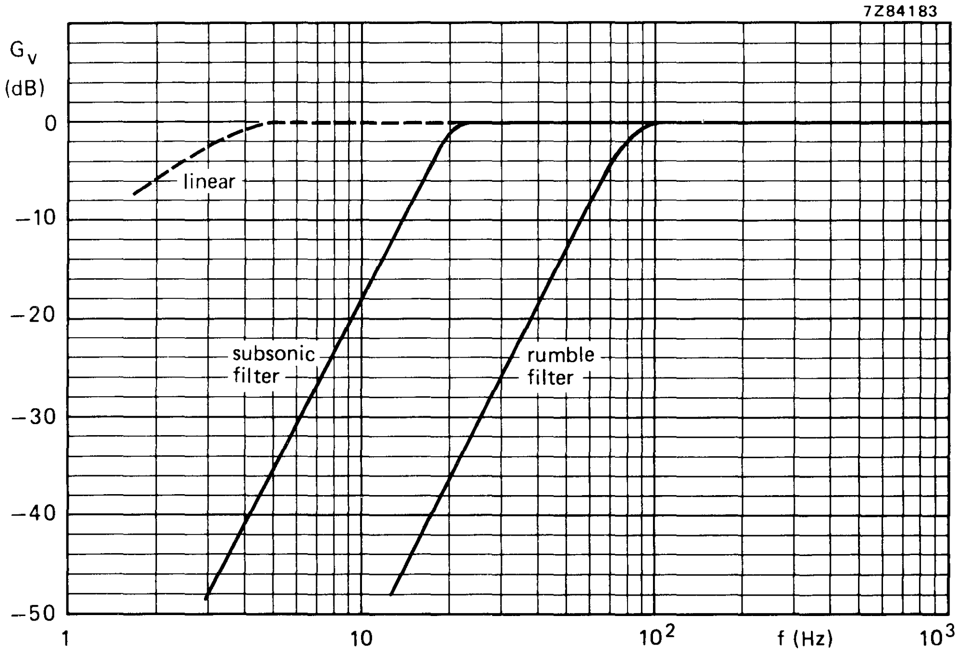


Fig. 11 Frequency response curves for the circuit of Fig. 10.

MOTOR SPEED REGULATOR WITH THERMAL SHUT-DOWN

The TDA1059B is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

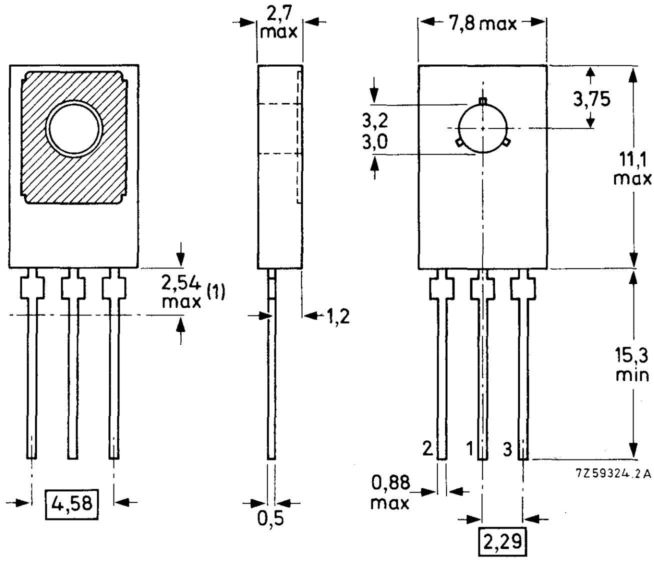
QUICK REFERENCE DATA

Supply voltage	$V_P = V_{2-1}$	typ.	9	V
			3,3 to 16	V
Internal reference voltage	V_{ref}	typ.	1,3	V
Drop-out voltage	V_{3-1}	typ.	1,8	V
Limited output current	I_{3lim}	typ.	0,6	A
Multiplication coefficient	k	typ.	9	

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

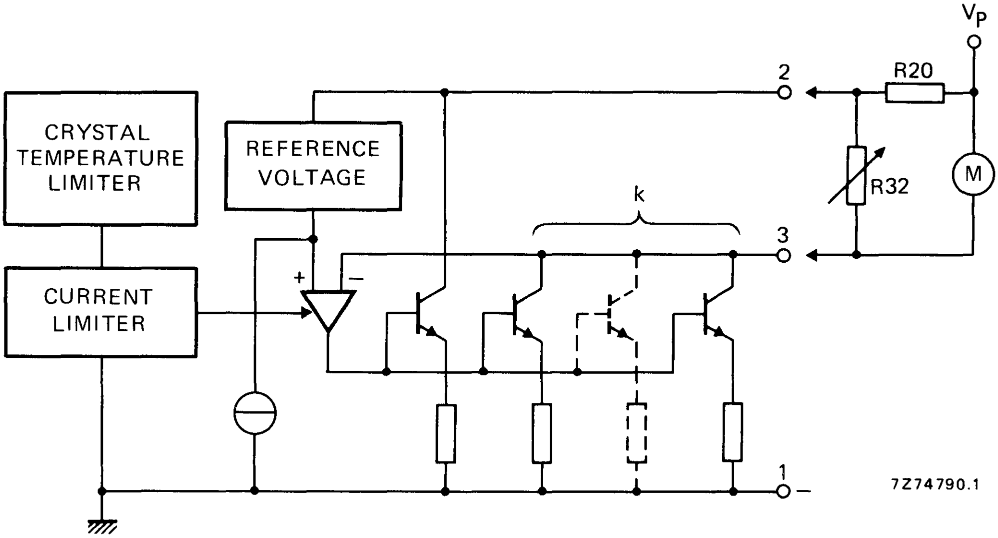


Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2\text{-}1}$	max.	16 V
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature (see Fig. 3 and note)	T_{amb}	−25 to + 130	°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

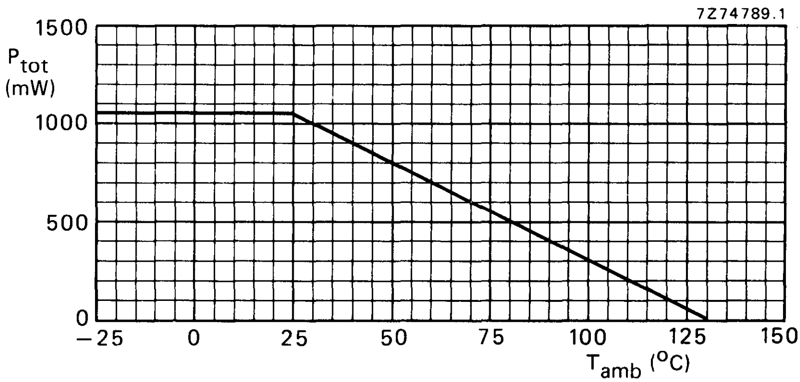


Fig. 3 Power derating curve.

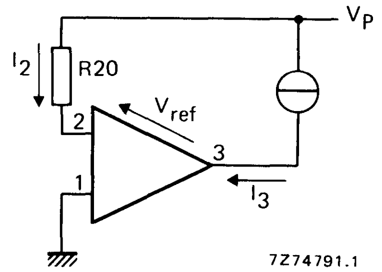
Note
At ambient temperatures above 130 °C, the crystal temperature limiter decreases the internal power consumption.

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; R20 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4.

		min.	typ.	max.	
Supply voltage	$V_P = V_{2\text{-}1}$	3,3	9	16	V
Internal reference voltage V_P = 3,3 V; I_3 = 80 mA	V_{ref}	1,24	1,3	1,36	V
Drop-out voltage I_3 = 80 mA; ΔV_{ref} = 5%	$V_{3\text{-}1}$	–	1,8	2,06	V
Quiescent current; I_3 = 0	I_q	1,8	2,3	2,8	mA
Limited output current*	I_{3lim}	0,3	0,6	1	A
Multiplication coefficient I_3 = 50 mA ± 10 mA	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5	
Line regulation V_P = 3,3 to 16 V at I_3 = 50 mA					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_P$	–0,115	0	+ 0,115	%/V
multiplication coefficient variation I_3 = 50 ± 10 mA	$\frac{\Delta k}{k} / \Delta V_P$	–	0,86	–	%/V
input current variation; I_3 = 50 mA	$\frac{\Delta I_2}{\Delta V_P}$	–15	0	+ 20	μA/V
Load regulation					
reference voltage variation I_3 = 20 to 80 mA	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_3$	0	19	38,5	%/A
multiplication coefficient variation I_3 = 30 ± 10 to 70 ± 10 mA	$\frac{\Delta k}{k} / \Delta I_3$	–0,075	0	+ 0,075	%/mA
Temperature coefficient I_3 = 50 mA; T_{amb} = –15 to + 65 °C					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	–0,03	0	+ 0,03	%/K
multiplication coefficient variation ΔI_3 = ± 10 mA	$\frac{\Delta k}{k} / \Delta T_{amb}$	–	0,008	–	%/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	–2	0	+ 2	μA/K

* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059B will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

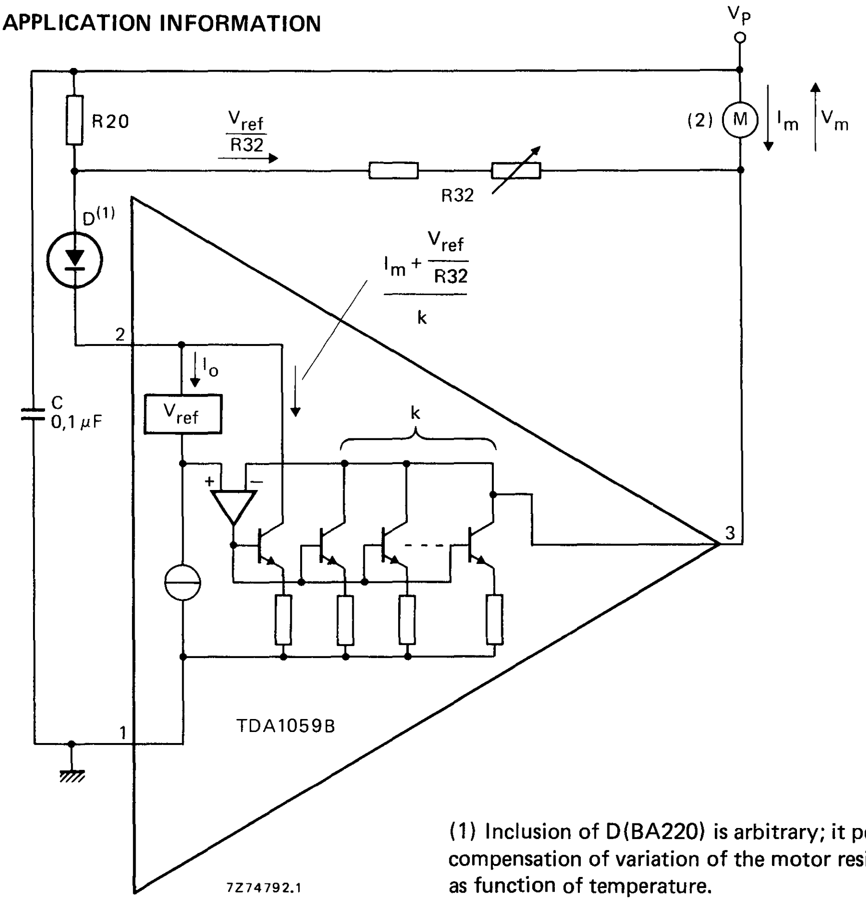


Note

For start operation: V_{ref} must start with final V_P = 6,7 V and a time constant of 3 τ = 100 ms in which τ = R.C; R = source impedance, C = by-pass capacitor.

Fig. 4 Test circuit.

APPLICATION INFORMATION



(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 100 Ω + 100 Ω (variable).

Fig. 5 Example of using the TDA1059B in a d.c. motor speed regulation circuit.

Motor equations

$E_m = \alpha_1 n$ where: α_1, α_2 = motor constant

$I_m = \alpha_2 r$ n = number of revolutions

$V_m = E_m + R_m I_m$ r = motor torque

E_m = back electromotive force

R_m = motor resistance

The back electromotive force (E_m) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m \right) I_m + V_{ref} \left\{ 1 + \frac{R20}{R32} \left(1 + \frac{1}{k} \right) \right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m \right) I_m + \left(V_{ref} + V_D \right) \left\{ 1 + \frac{R20}{R32} \left(1 + \frac{1}{k} \right) \right\} + R20.I_o$$

Speed regulation is constant when E_m is independent of I_m variations; this will be obtained when $R20 = kR_m$.

E_m, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

Features

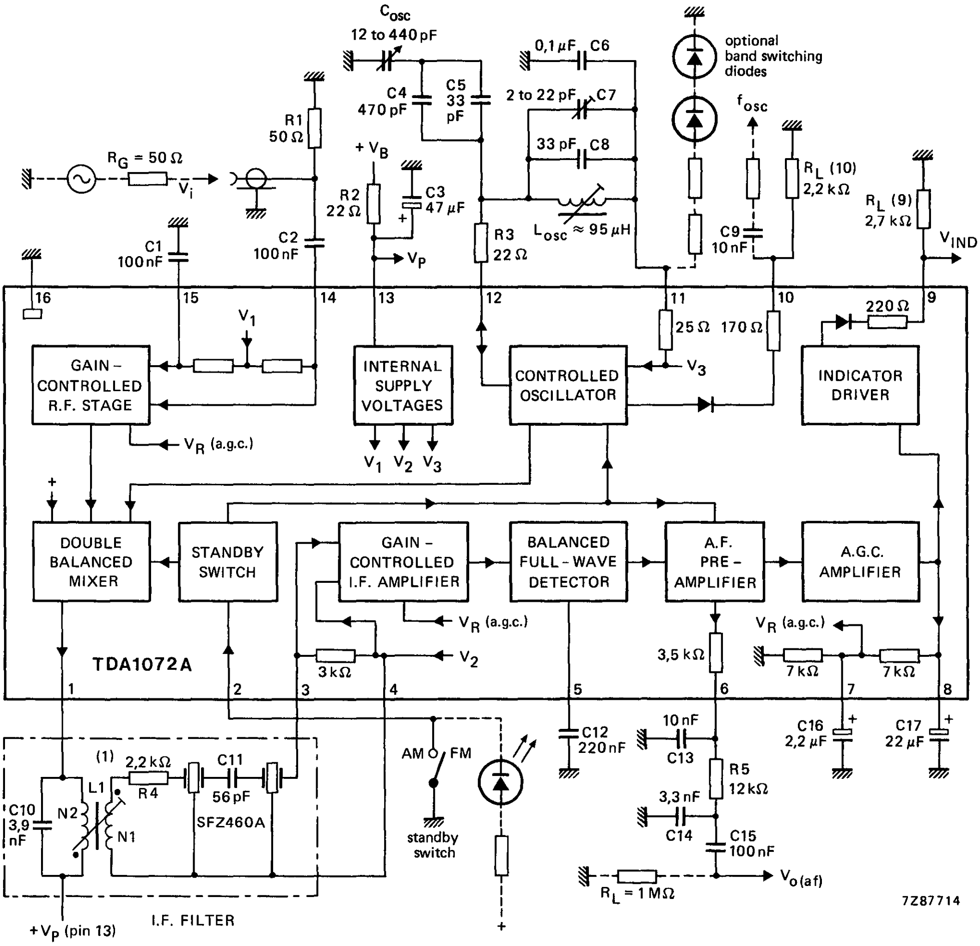
- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

QUICK REFERENCE DATA

Supply voltage range	V_P		7,5 to 18	V
Supply current range	I_P		15 to 30	mA
R.F. input voltage for S + N/N = 6 dB at m = 30%	V_i	typ.	1,5	μV
R.F. input voltage for 3% total harmonic distortion (THD) at m = 80%	V_i	typ.	500	mV
A.F. output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30% and f_m = 400 Hz	$V_{o(af)}$	typ.	310	mV
A.G.C. range: change of V_i for 1 dB change of $V_{o(af)}$		typ.	86	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	V_{IND}	typ.	2,8	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; $Q_O = 65$; $Q_B = 57$.
Filter data: $Z_F = 700\ \Omega$ at $R_{3\text{-}4} = 3\ k\Omega$; $Z_I = 4,8\ k\Omega$.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage	$V_P = V_{13\text{-}16}$	max.	20 V
Total power dissipation	P_{tot}	max.	875 mW
Input voltage	$\lvert V_{14\text{-}15} \rvert$	max.	12 V
	$-V_{14\text{-}16}, -V_{15\text{-}16}$	max.	0,6 V
	$V_{14\text{-}16}, V_{15\text{-}16}$	max.	V_P V
Input current	$\lvert I_{14} \rvert, \lvert I_{15} \rvert$	max.	200 mA
Operating ambient temperature range	T_{amb}	−40 to	+ 80 °C
Storage temperature range	T_{stg}	−55 to	+ 150 °C
Junction temperature	T_j	max.	+ 125 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	80 K/W

DEVICE CHARACTERISTICS

$V_P = V_{13\text{-}16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_{13\text{-}16}$	7,5	8,5	18	V
Supply current	$I_P = I_{13}$	15	23	30	mA
R.F. stage and mixer					
Input voltage (d.c. value)	$V_{14\text{-}16}, V_{15\text{-}16}$	–	$V_P/2$	–	V
R.F. input impedance at $V_i < 300\ \mu V$	$R_{14\text{-}16}, R_{15\text{-}16}$	–	5,5	–	kΩ
	$C_{14\text{-}16}, C_{15\text{-}16}$	–	25	–	pF
R.F. input impedance at $V_i > 10$ mV	$R_{14\text{-}16}, R_{15\text{-}16}$	–	8	–	kΩ
	$C_{14\text{-}16}, C_{15\text{-}16}$	–	22	–	pF
I.F. output impedance	$R_{1\text{-}16}$	500	–	–	kΩ
	$C_{1\text{-}16}$	–	6	–	pF
Conversion transconductance before start of a.g.c.	I_1/V_i	–	6,5	–	mA/V
Maximum i.f. output voltage, inductive coupling to pin 1	$V_{1\text{-}13(p\text{-}p)}$	–	5	–	V
D.C. value of output current (pin 1) at $V_i = 0$ V	I_1	–	1,2	–	mA
A.G.C. range of input stage		–	30	–	dB
R.F. signal handling capability: input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,6	–	60	MHz
Oscillator amplitude (pins 11 to 12)	$V_{11\text{-}12}$	–	130	150	mV
External load impedance	$R_{12\text{-}11(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation	$R_{12\text{-}11(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_{13\text{-}16}/V_{11\text{-}16}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE})	$V_{11\text{-}16}$	–	4,2	–	V
D.C. output current (for switching diodes)	$-I_{11}$	0	–	20	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)	$\Delta V_{11\text{-}16}$	–	0,5	–	V
Buffered oscillator output					
D.C. output voltage	$V_{10\text{-}16}$	–	0,7	–	V
Output signal amplitude	$V_{10\text{-}16(p\text{-}p)}$	–	320	–	mV
Output impedance	R_{10}	–	170	–	Ω
Output current	$-I_{10(peak)}$	–	–	3	mA
I.F., a.g.c. and a.f. stages					
D.C. input voltage	$V_{3\text{-}16}$, $V_{4\text{-}16}$	–	2,0	–	V
I.F. input impedance	$R_{3\text{-}4}$	2,4	3	3,9	kΩ
	$C_{3\text{-}4}$	–	7	–	pF
I.F. input voltage for THD = 3% at m = 80%	$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of a.g.c.	$V_{3\text{-}4}/V_{6\text{-}16}$	–	68	–	dB
A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV	$\Delta V_{3\text{-}4}$	–	55	–	dB
A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV	$V_{o(af)}$	–	310	–	mV
A.F. output impedance (pin 6)	$\|Z_o\|$	–	3,5	–	kΩ
Indicator driver					
Output voltage at V_i = 0 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	–	20	150	mV
Output voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	2,5	2,8	3,1	V
Load resistance	$R_{L(9)}$	1,5	–	–	kΩ

DEVICE CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Standby switch					
Switching threshold at V_P = 7,5 to 18 V; T_{amb} = −40 to + 80 °C					
on-voltage	$V_{2\text{-}16}$	0	–	2,0	V
off-voltage	$V_{2\text{-}16}$	3,5	–	20	V
on-current at $V_{2\text{-}16}$ = 0 V	$-I_2$	–	–	200	μA
off-current at $V_{2\text{-}16}$ = 20 V	$\|I_2\|$	–	–	10	μA

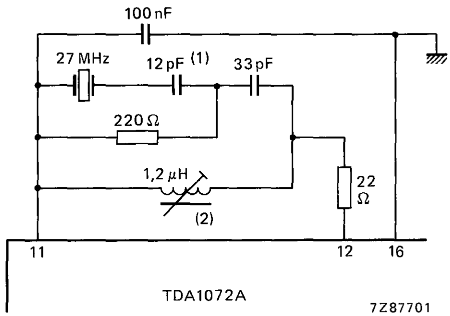
OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity					
R.F. input required for S + N/N = 6 dB	V_i	–	1,5	–	μV
R.F. input required for S + N/N = 26 dB	V_i	–	15	–	μV
R.F. input required for S + N/N = 46 dB	V_i	–	150	–	μV
R.F. input at start of a.g.c.	V_i	–	30	–	μV
R.F. large signal handling					
R.F. input at THD = 3%; m = 80%	V_i	–	500	–	mV
R.F. input at THD = 3%; m = 30%	V_i	–	700	–	mV
R.F. input at THD = 10%; m = 30%	V_i	–	900	–	mV
A.G.C. range					
Change of V_i for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
A.F. output voltage at V_i = 4 μV; m = 80%	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at V_i = 1 mV	$V_{o(af)}$	240	310	390	mV
THD at V_i = 1 mV; m = 80%	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV; m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio at V_i = 100 mV	(S + N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_P/V_{o(af)}]$)	RR	–	38	–	dB

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of i.f. whistles at V_i = 15 μV; m = 0% related to a.f. signal of m = 30%					
at $f_i \approx 2 \times f_{if}$	$\alpha_{2\,if}$	–	37	–	dB
at $f_i \approx 3 \times f_{if}$	$\alpha_{3\,if}$	–	44	–	dB
I.F. suppression at r.f. input					
for symmetrical input	α_{if}	–	40	–	dB
for asymmetrical input	α_{if}	–	40	–	dB
Residual oscillator signal at mixer output					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

APPLICATION INFORMATION (continued)

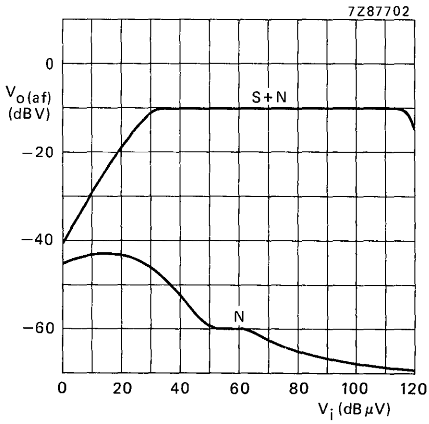


Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

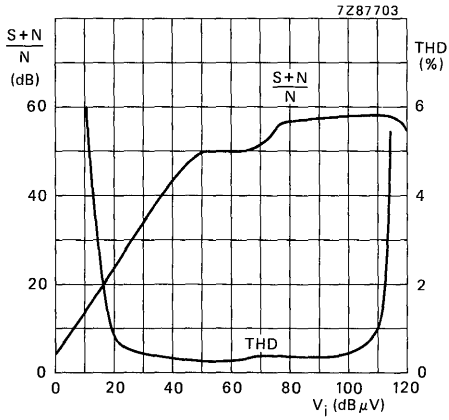


Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

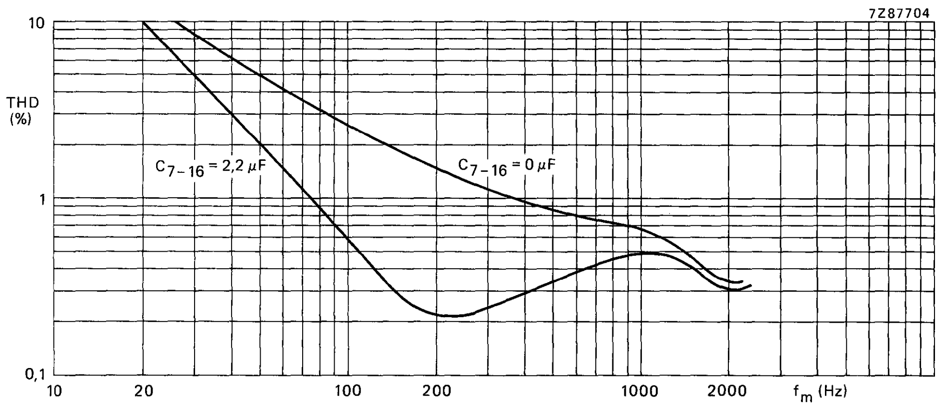


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2,2 μF.

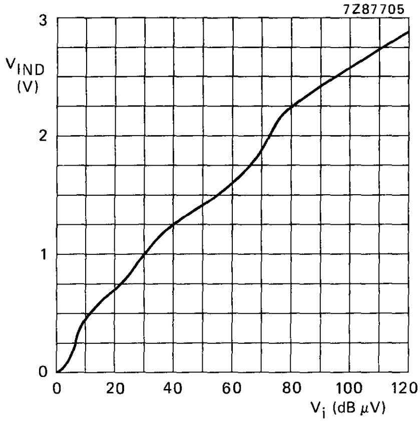


Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

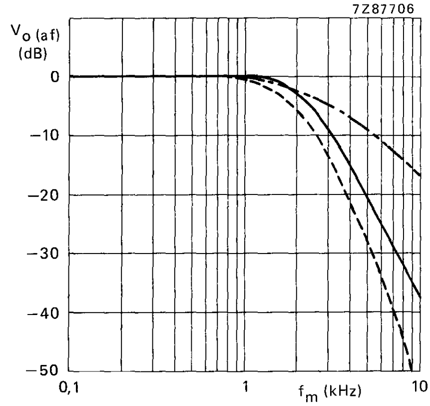


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:

——————— with i.f. filter;

—·—·—·—· with a.f. filter;

— — — — — — with i.f. and a.f. filters.

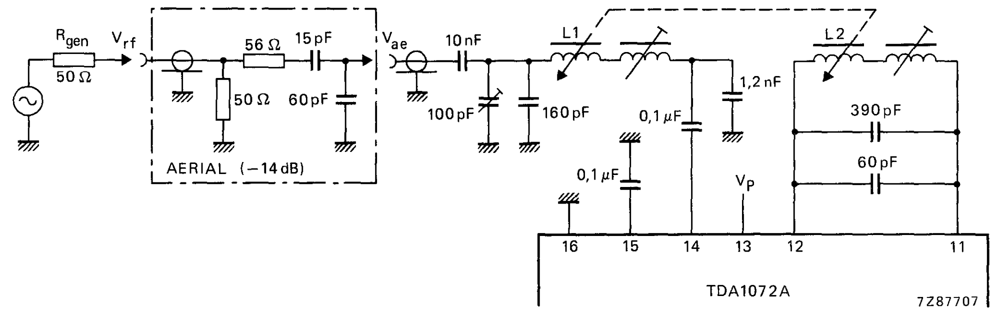


Fig. 8 Car radio application with inductive tuning.

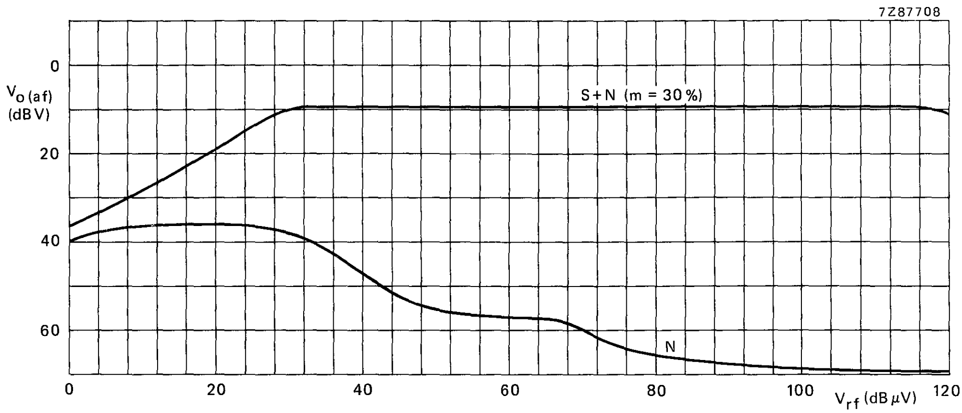


Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

APPLICATION INFORMATION (continued)

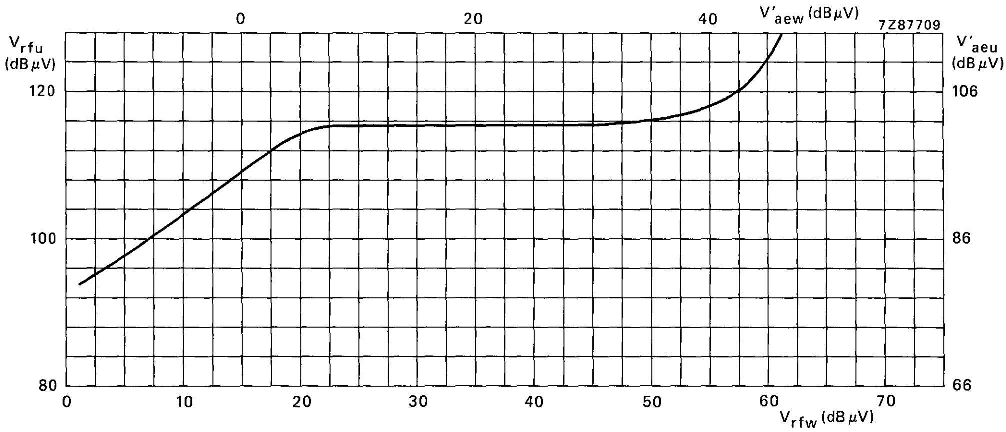


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

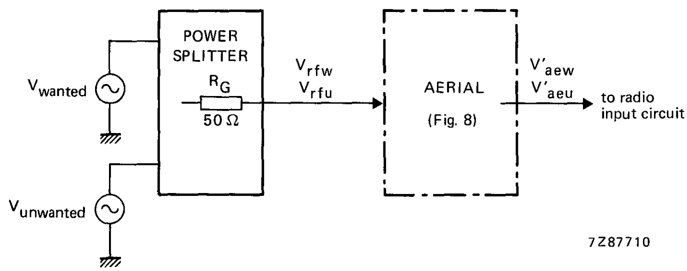


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

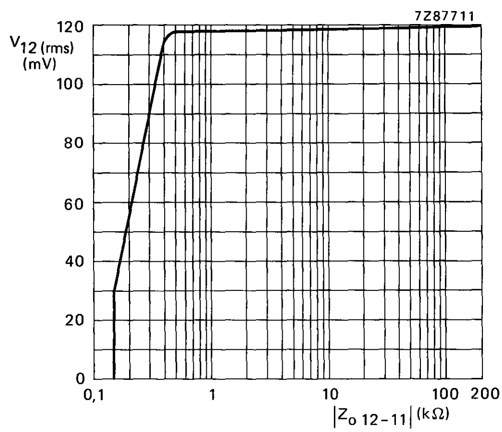


Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

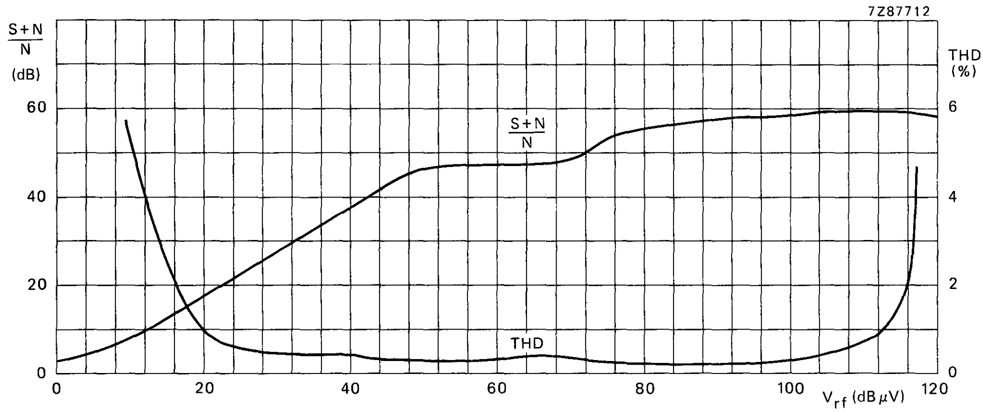


Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

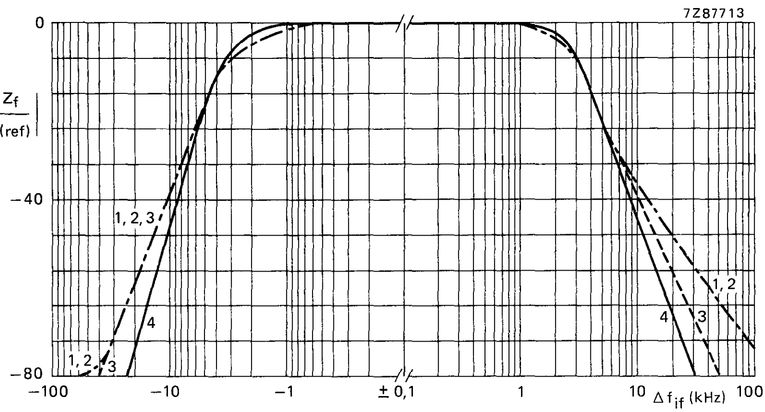


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

APPLICATION INFORMATION (continued)

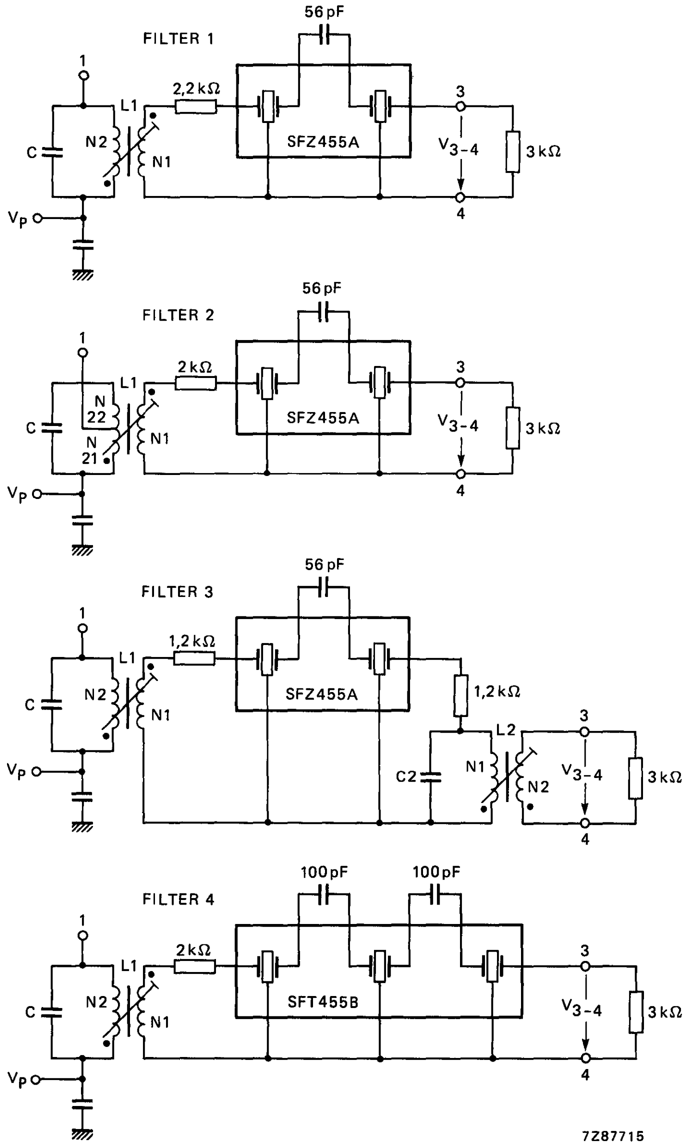


Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

Table 1 Data for I.F. filters shown in Fig. 15. Criterium for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings	12 32	13 66 33	15 31	29 29 (N1) (N2)	13 31	
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (–3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (–3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

APPLICATION INFORMATION (continued)

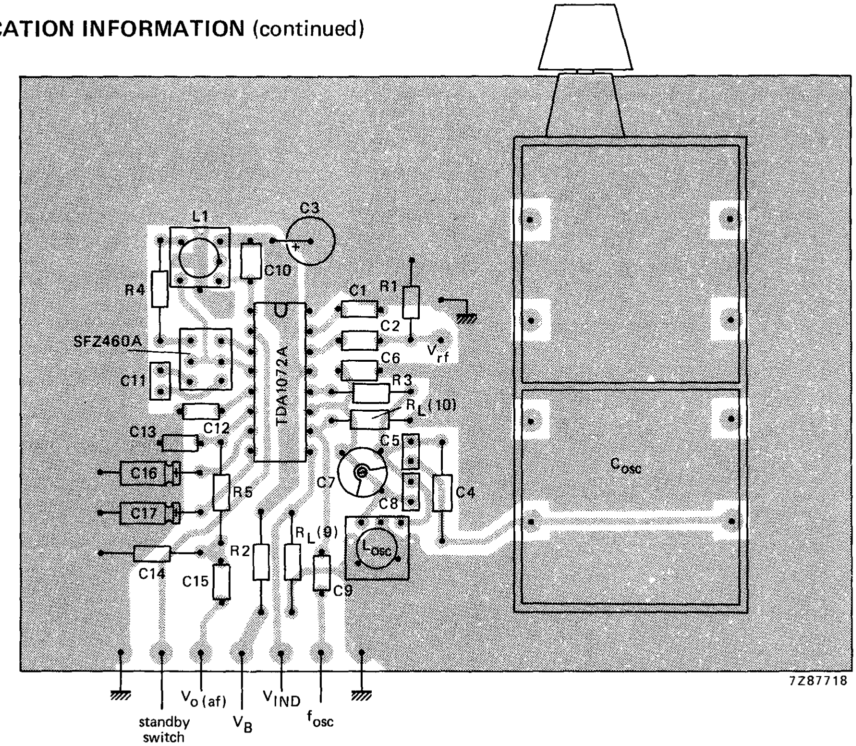


Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

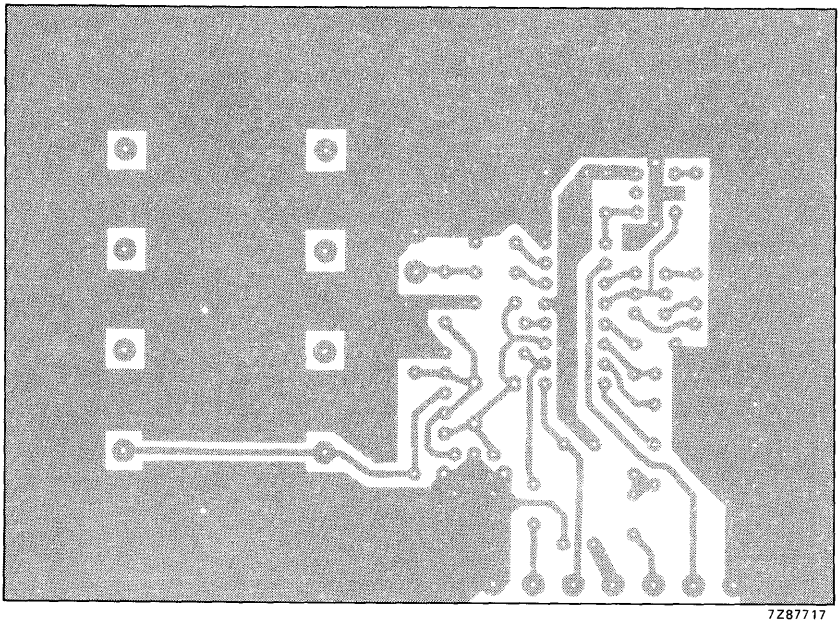
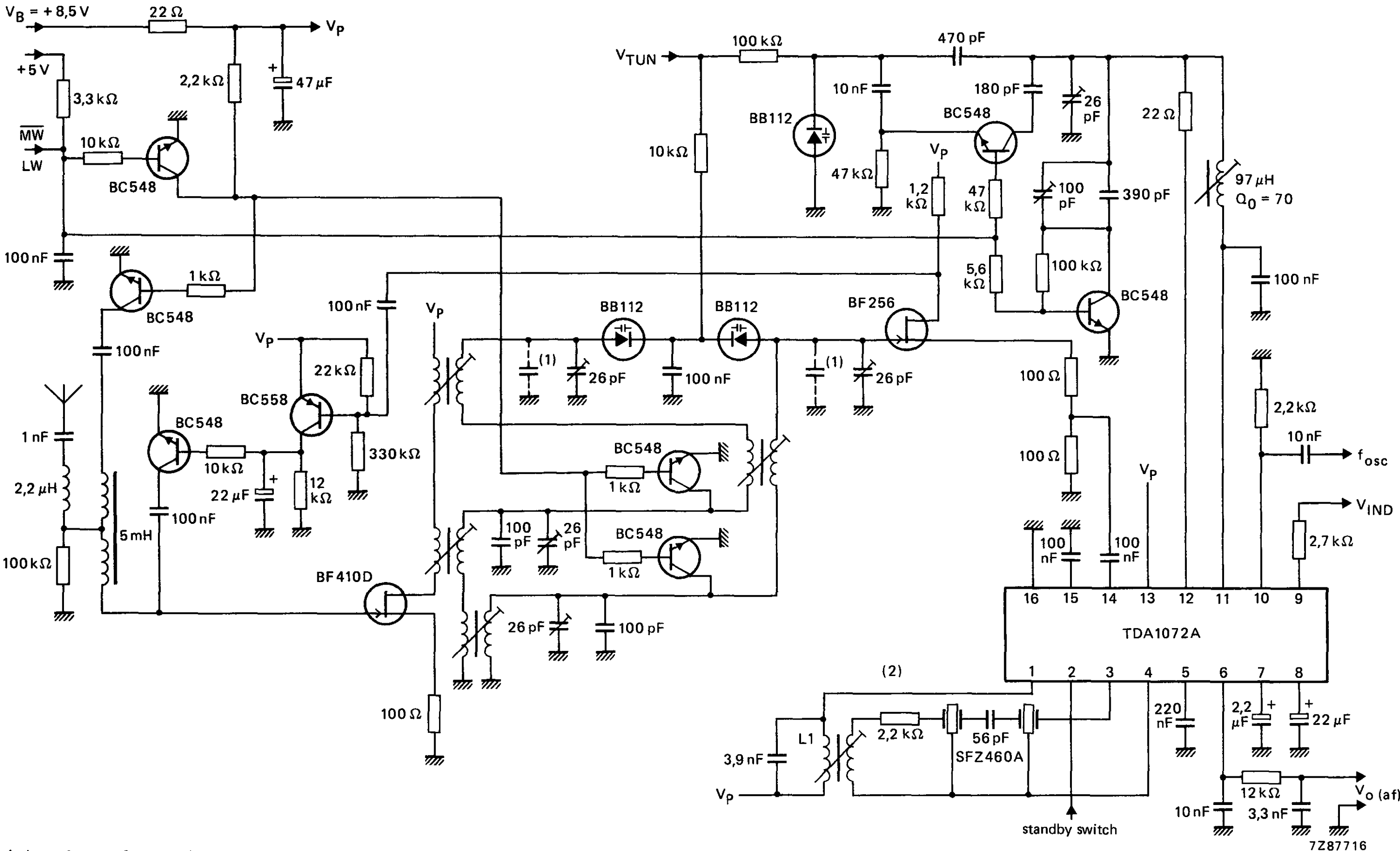


Fig. 17 Printed-circuit board showing track side.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA 1072AT integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV. RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

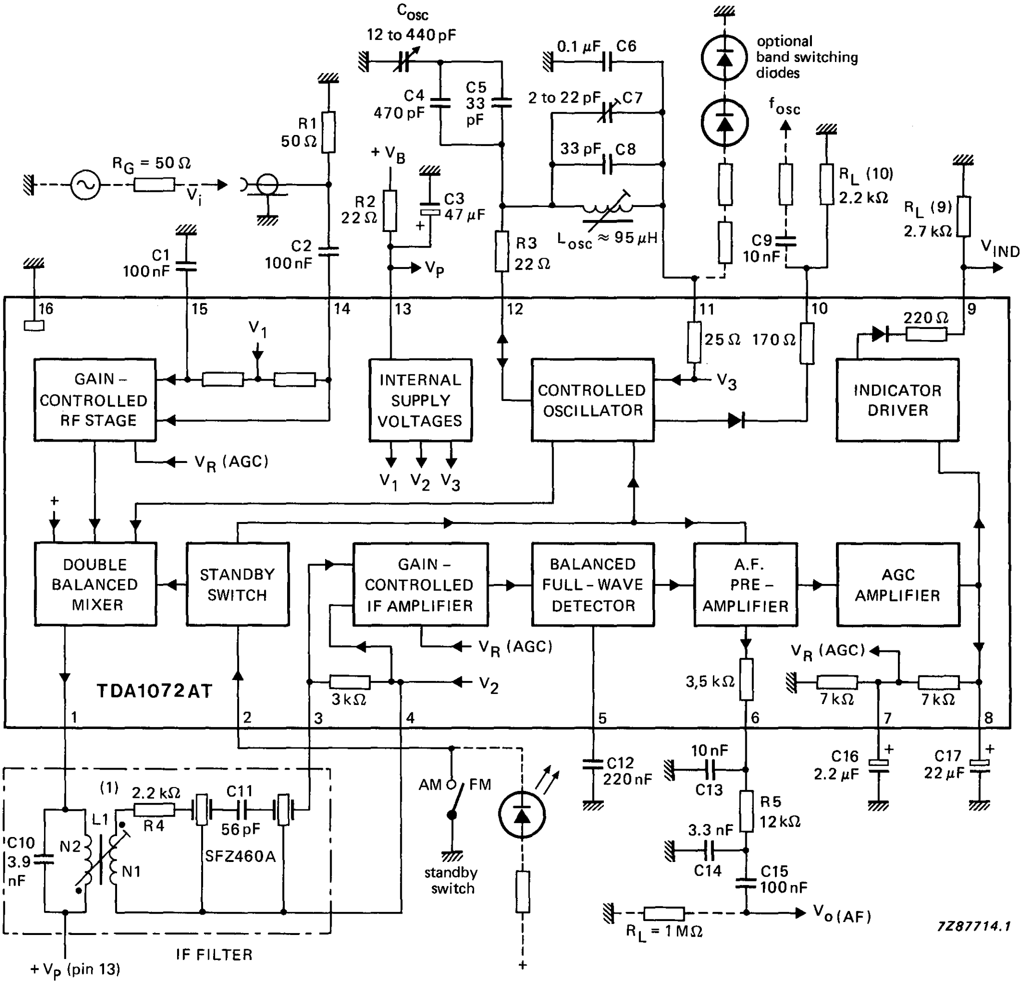
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	–	10	V
Supply current range		I_P	15	–	26	mA
RF input voltage for S+N/N = 6 dB at m = 30%		V_I	–	1.5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%		V_I	–	500	–	mV
AF output voltage with V_I = 2 mV; f_I = 1 MHz; m = 30% and f_m = 400 Hz		$V_{O(AF)}$	–	310	–	mV
AGC range: change of V_I for 1 dB change of $V_{O(AF)}$			–	86	–	dB
Field strength indicator voltage at V_I = 500 mV; $R_{L(9)}$ = 2.7 kΩ		V_{IND}	–	2.8	–	V

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1: N1/N2 = 12/32; Q_O = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at $R_{3\text{-}4}$ = 3 kΩ; Z_1 = 4.8 kΩ.

Fig.1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is also improved. Low noise working is achieved in the differential amplifier by using transistors with a low base resistance.

A double balanced mixer provides the IF output to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network.

DEVELOPMENT DATA

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. The residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output. The amplifier output stage uses an emitter follower with a series resistor which, together with an external capacitor, provides the required low-pass filtering for AF signals.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives a fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter. The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If field strength information is not needed, $R_{L(9)}$ can be omitted.

FUNCTIONAL DESCRIPTION (continued)

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and demodulator are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	$V_P = V_{13\text{-}16}$	V_{13}	–	12	V
Input voltage					
pins 14-15		$V_{14\text{-}15}$	–	10	V
pins 14-16		$V_{14\text{-}16}$	–	V_P	V
pins 15-16		$V_{15\text{-}16}$	–	V_P	V
pins 14-16		$V_{14\text{-}16}$	–	–0.6	V
pins 15-16		$V_{15\text{-}16}$	–	–0.6	V
Input current (pins 14 and 15)		$I_{14\text{-}15}$	–	200	mA
Total power dissipation*		P_{tot}	–	300	mW
Operating ambient temperature range		T_{amb}	–40	+ 80	°C
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\,j\text{-}a}$ 300 K/W; 160 K/W*

* Mounted on epoxiprint

CHARACTERISTICS

$V_P = V_{13\text{-}16} = 8.5$ V; $T_{amb} = 25\ ^oC$; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig.1; all measurements are with respect to ground (pin 16); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_{13}	7.5	8.5	10	V
Supply current (pin 13)		I_{13}	15	23	27	mA
RF stage and mixer						
Input voltage (DC value)		$V_{14\text{-}15}$	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$		$R_{14\text{-}15}$	–	5.5	–	kΩ
		$C_{14\text{-}15}$	–	25	–	pF
RF input impedance at $V_I > 10$ mV		$R_{14\text{-}15}$	–	8	–	kΩ
		$C_{14\text{-}15}$	–	22	–	pF
IF output impedance		R_1	500	0	0	kΩ
		C_1	–	6	–	pF
Conversion transconductance before start of AGC		I_1/V_I	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1, (peak-to-peak value)		$V_{1(p\text{-}p)}$	–	5	–	V
DC value of output current (pin 1) at $V_I = 0$ V		I_1	–	1.2	–	mA
AGC range of input stage			–	30	–	dB
RF signal handling capability: input voltage for THD = 3% at m = 80% (RMS value)		$V_{I(rms)}$	–	500	–	mV
Oscillator						
Frequency range		Δf	0.6	–	60	MHz
Oscillator amplitude (pins 11 to 12) (peak-to-peak value)		$V_{11\text{-}12(p\text{-}p)}$	–	130	150	mV
External load impedance		$R_{11\text{-}12(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation		$R_{11\text{-}12(ext)}$	–	–	60	Ω

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection at V_P = 100 mV (RMS value); f_p = 100 Hz ($RR = 20 \log [V_{13}/V_{11}]$)						
Source voltage for switching diodes (6 x V_{BE})		V_{11}	–	4.2	–	V
DC output current (for switching diodes)	$V_P = V_{13} \leqslant 9$ V	I_{11}	0	–	5	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)		ΔV_{11}	–	0.5	–	V
Buffered oscillator output						
DC output voltage		V_{10}	–	0.7	–	V
Output signal amplitude (peak-to-peak value)		$V_{10(p\text{-}p)}$	–	320	–	mV
Output impedance		R_{10}	–	170	–	Ω
Output current		$I_{10(peak)}$	–	–	–3	mA
IF, AGC and AF stages						
DC input voltage		$V_{3\text{-}4}$	–	2	–	V
IF input impedance		$R_{3\text{-}4}$	2.4	3.0	3.9	kΩ
		$C_{3\text{-}4}$	–	7	–	pF
IF input voltage for THD = 3% at m = 80%		$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of AGC		$V_{3\text{-}4}/V_6$	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{O(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV		$\Delta V_{3\text{-}4}$	–	55	–	dB
AF output voltage at $V_{3\text{-}4(IF)}$ = 50 μV		$V_{O(AF)}$	–	130	–	mV
AF output voltage at $V_{3\text{-}4(IF)}$ = 1 mV		$V_{O(AF)}$	–	310	–	mV
AF output impedance (pin 6)		$\|Z_O\|$	–	3.5	–	kΩ

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator driver						
Output voltage at $V_I = 0$ mV	$R_{L(9)} = 2.7$ kΩ	V_9	–	20	150	mV
Output voltage at $V_I = 500$ mV	$R_{L(9)} = 2.7$ kΩ	V_9	2.5	2.8	3.1	V
Load resistance		$R_{L(9)}$	2.7	–	–	kΩ
Standby switch						
Switching threshold at $V_P = 7.5$ to 18 V; $T_{amb} = -40$ to $+80$ °C						
ON-voltage		V_2	0	–	2	V
OFF-voltage		V_2	3.5	–	20	V
ON-current	$V_2 = 0$ V	I_2	–	–	–200	μA
OFF-current	$V_2 = 20$ V	I_2	–	–	10	μA

OPERATING CHARACTERISTICS

$V_P = 8.5$ V; $f_I = 1$ MHz; m = 30%; $f_m = 400$ Hz; $T_{amb} = 25$ °C; measured in Fig.1; unless otherwise specified

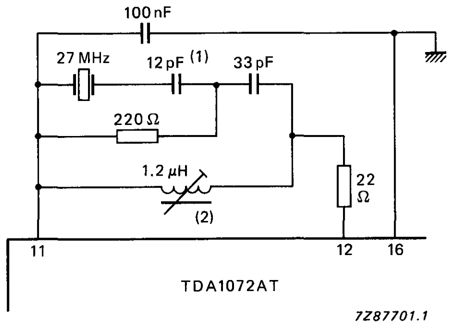
parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input required for						
S+N/N = 6 dB		V_I	–	1.5	–	μV
S+N/N = 26 dB		V_I	–	15	–	μV
S+N/N = 46 dB		V_I	–	150	–	μV
RF input at start of AGC		V_I	–	30	–	μV
RF large signal handling						
RF input at						
THD = 3%; m = 80%		V_I	–	500	–	mV
THD = 3%; m = 30%		V_I	–	700	–	mV
THD = 10%; m = 30%		V_I	–	900	–	mV

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AGC range						
Change of V_I for						
1 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	86	–	dB
6 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	91	–	dB
Output signal						
AF output voltage at						
V_I = 4 μV	m = 80%	$V_{O(AF)}$	–	130	–	mV
V_I = 1 mV		$V_{O(AF)}$	240	310	390	mV
Total harmonic distortion at						
V_I = 1 mV	m = 80%	d_{tot}	–	0.5	–	%
V_I = 500 mV	m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio	V_I = 100 mV	S+N/N	–	58	–	dB
Ripple rejection at						
V_I = 2 mV						
V_P = 100 mV (RMS value)						
f_p = 100 Hz						
(RR = 20 log [$V_P/V_{O(AF)}$])		RR	–	38	–	dB
Unwanted signals						
Suppression of IF whistles						
at V_I = 15 μV; m = 0%						
related to AF signal of						
m = 30%						
at $f_I \approx 2 \times f_{IF}$		α_{2IF}	–	37	–	dB
at $f_I \approx 3 \times f_{IF}$		α_{3IF}	–	44	–	dB
IF suppression at RF input						
for symmetrical input		α_{IF}	–	40	–	dB
for asymmetrical input		α_{IF}	–	40	–	dB
Residual oscillator signal						
at mixer output						
at f_{osc}		$I_{(osc)}$	–	1	–	μA
at 2 x f_{osc}		$I_{(2osc)}$	–	1.1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0.1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig.2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

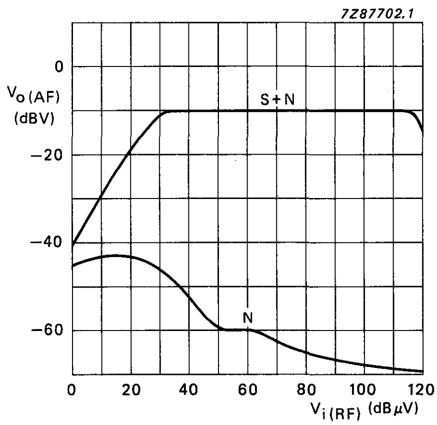


Fig.3 AF output as a function of RF input in the circuit of Fig.1; f_I = 1 MHz; f_m = 400 Hz; m = 30%.

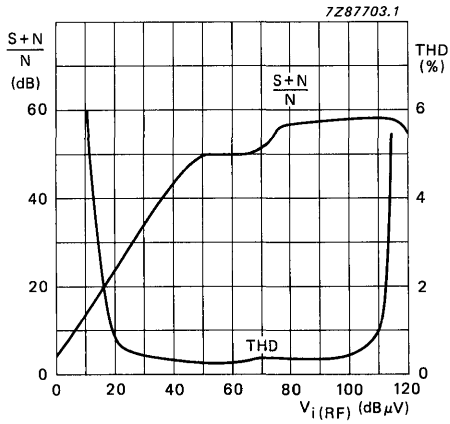


Fig.4 Total harmonic distortion and S+N/N as functions of RF input in the circuit of Fig.1; m = 30% for (S+N)/N curve and m = 80% for THD curve.

APPLICATION INFORMATION (continued)

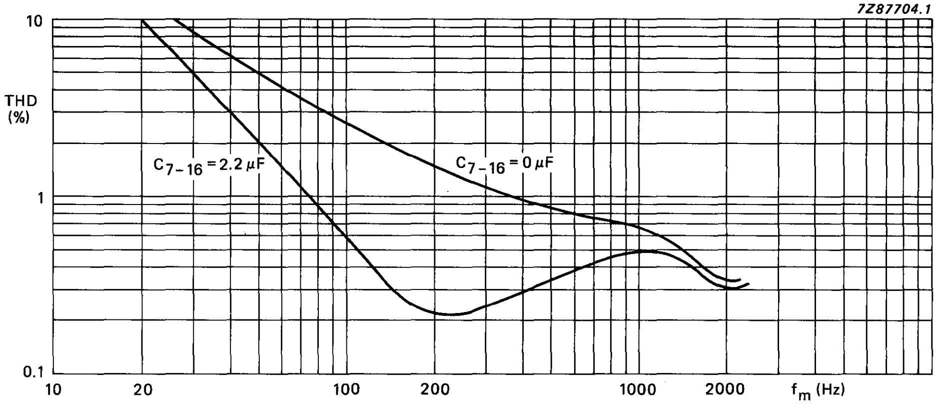


Fig.5 Total harmonic distortion as a function of modulation frequency at V_I = 5 mV; m = 80%; measured in the circuit of Fig.1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2.2 μF.

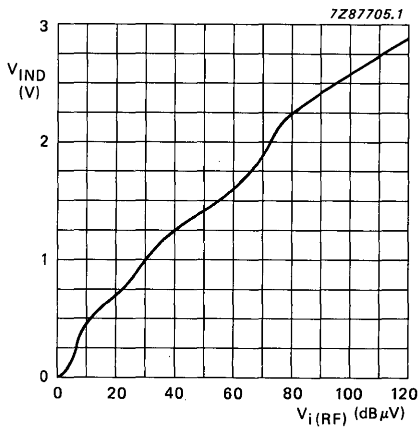
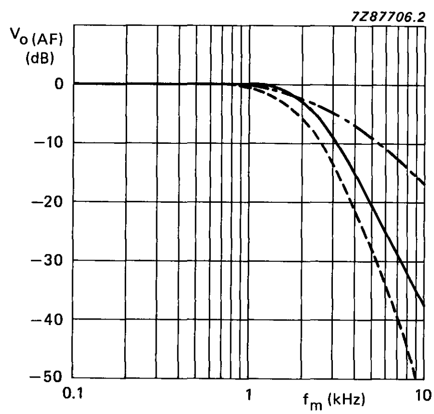


Fig.6 Indicator driver voltage as a function of RF input in the circuit of Fig.1.



—— with IF filter

—.—. with AF filter

------- with IF and AF filter

Fig.7 Typical frequency response curves from Fig.1 showing the effects of filtering.

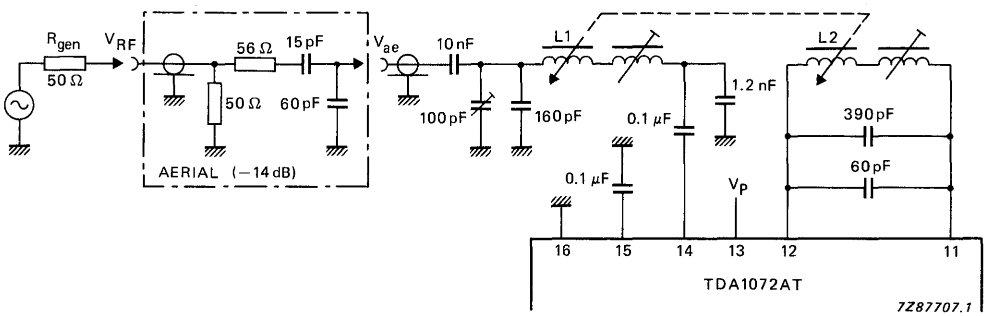


Fig.8 Car radio application with inductive tuning.

DEVELOPMENT DATA

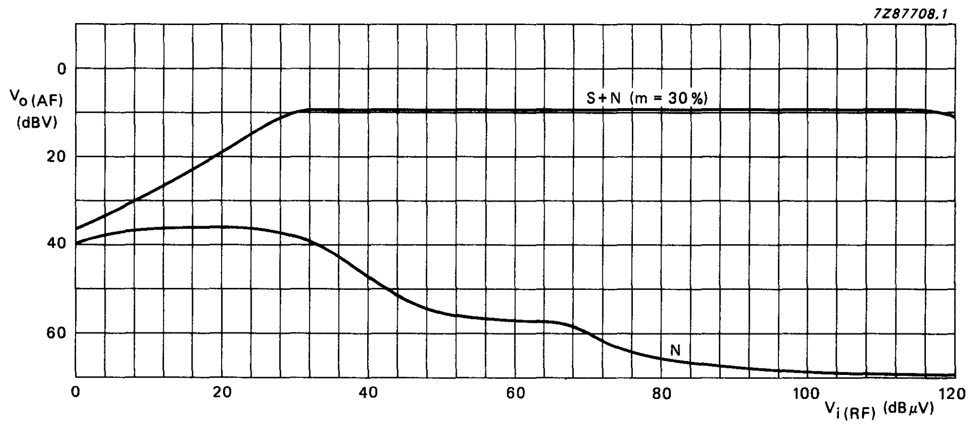


Fig.9 AF output as a function of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

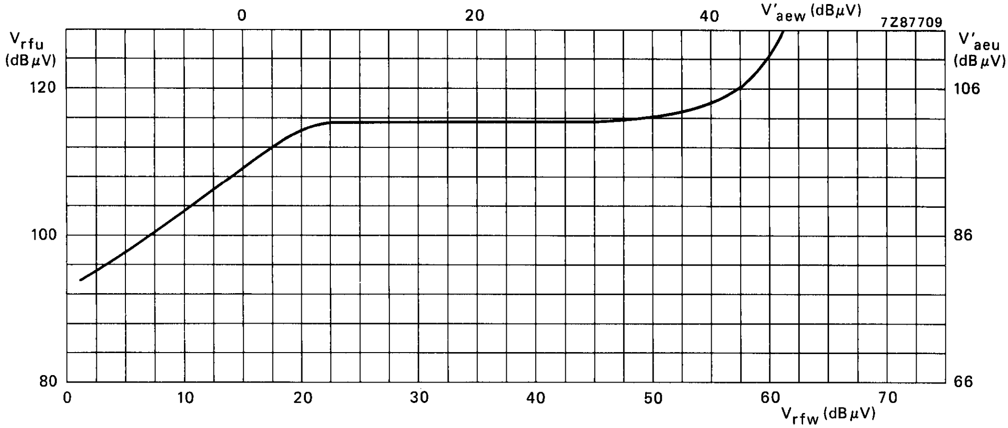


Fig.10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig.8 with the input circuit as shown in Fig.11. Curve is for wanted $V_{O(AF)}$/unwanted $V_{O(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

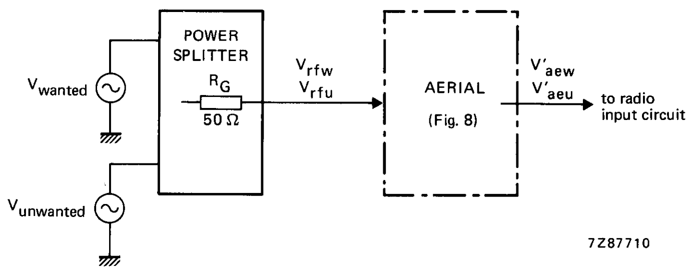


Fig.11 Input circuit to show cross-modulation suppression (see Fig.10).

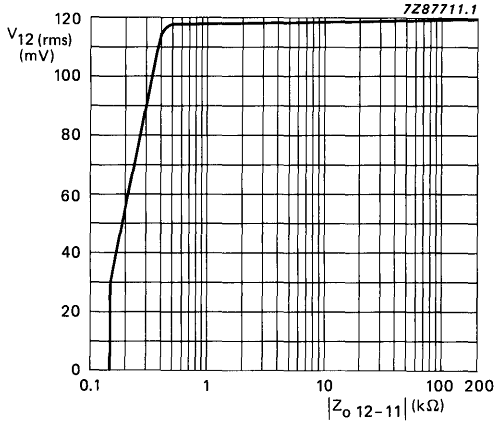


Fig.12 Oscillator amplitude as a function of the impedance at pins 11 and 12 in the circuit of Fig.8.

DEVELOPMENT DATA

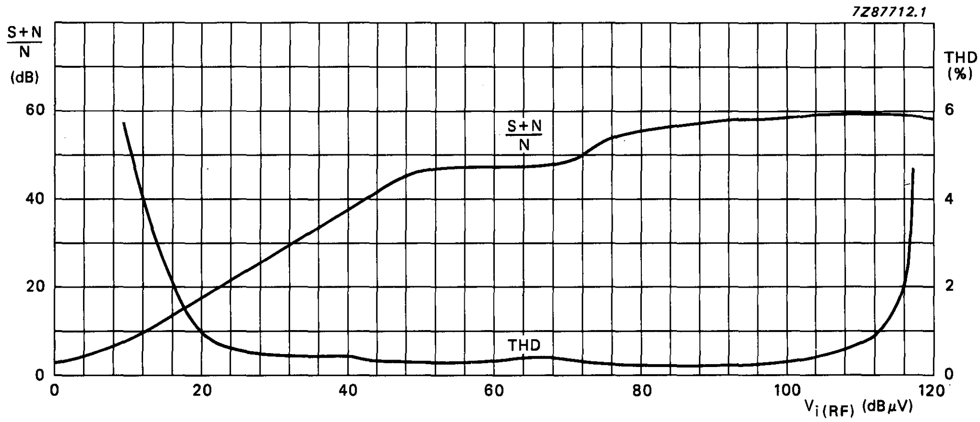


Fig.13 Total harmonic distortion and (S+N)/N as functions of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

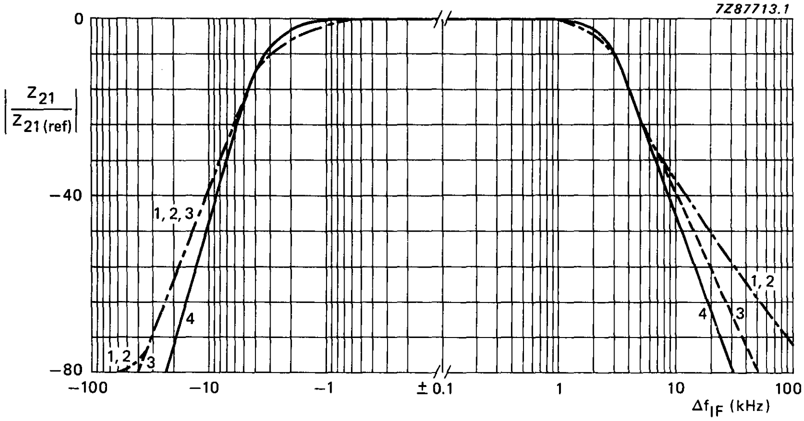


Fig.14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.14; centre frequency = 455 kHz.

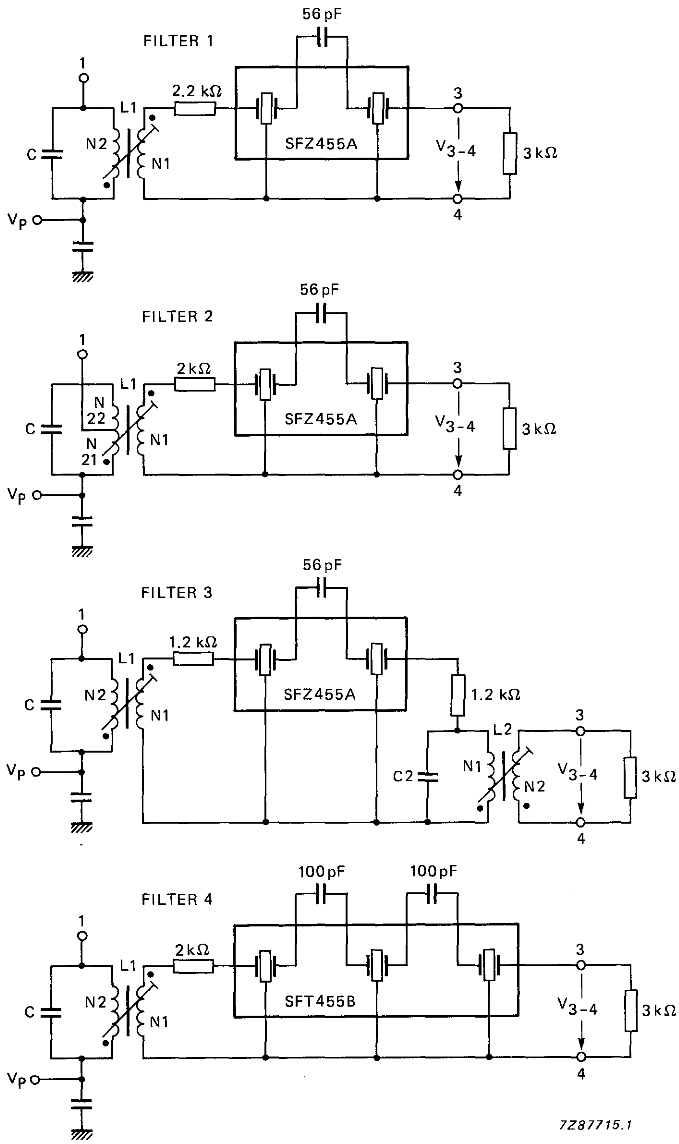


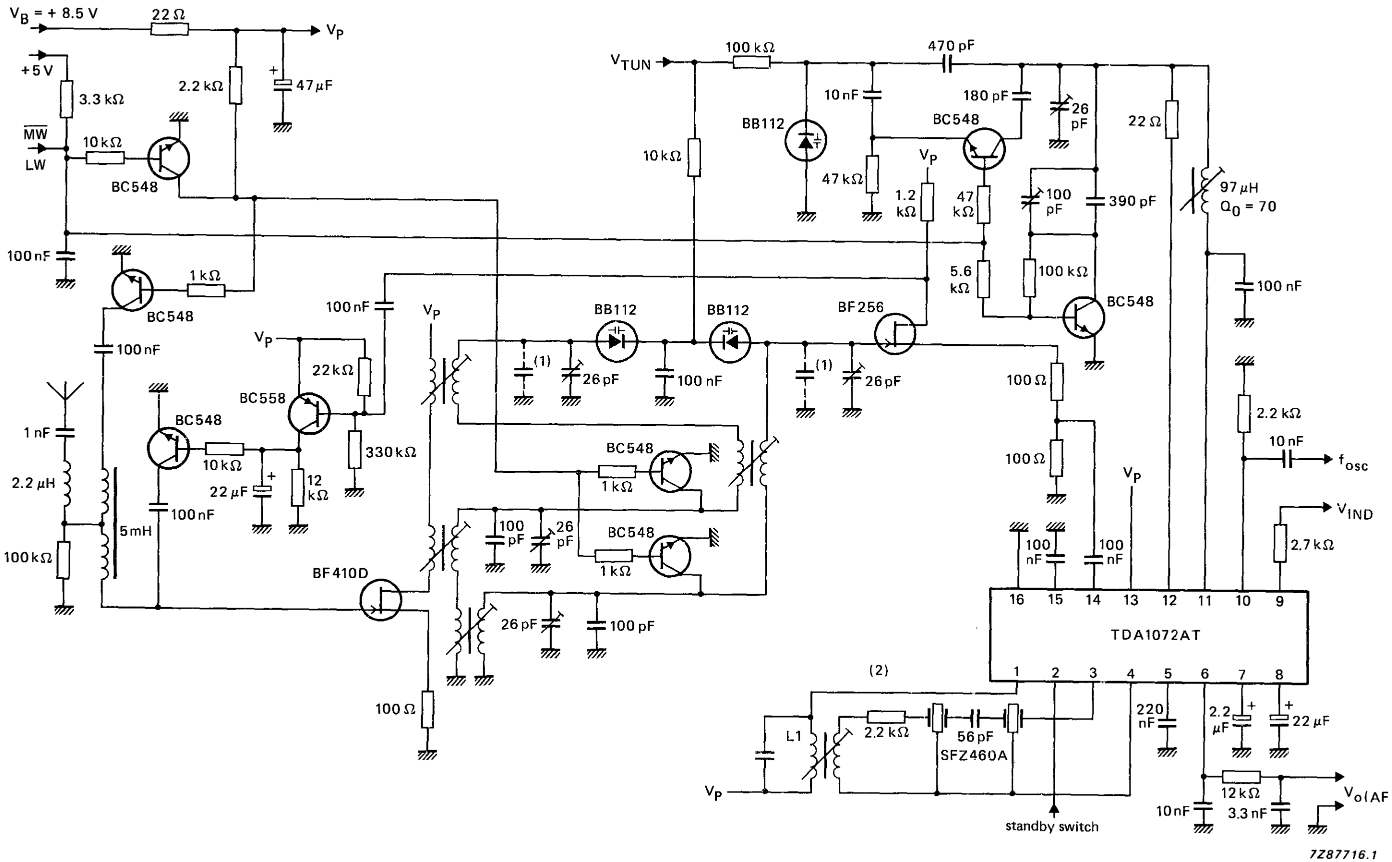
Fig.15 IF filter variants applied to the circuit of Fig.1; for filter data refer to Table 1.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0.09	0.08	0.09	0.08	0.09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings	● ● 12 ● 32 ● ●	● ● 13 ● 33 = ● ●	● ● 15 ● 31 ● ●	● ● 29 29 ● ● ● (N1) (N2)	● ● 13 ● 31 ● ●	
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4.8	3.8	4.2		4.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0.70	0.67	0.68		0.68	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding. N2 the outer winding.

Table 1 Data for IF filters shown in Fig.15. Criterium for adjustment is Z_F = maximum (optional selectivity curve at centre frequency f_o = 455 kHz).
See also Fig.14.

DEVELOPMENT DATA



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.

(2) For IF filter and coil data refer to Fig.1.

Fig.18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage AGC optimised for good large-signal handling.

DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20	V
Supply current (pin 11)	I_P	typ.	22	mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6	V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6	V
Total harmonic distortion	THD	typ.	0,05	%
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50	μV
Control range	$\Delta\alpha$	typ.	110	dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80	dB
Ripple rejection (100 Hz)	α_{100}	typ.	46	dB
Tracking of ganged potentiometers	ΔG_v	typ.	0,5	dB
Supply voltage range	V_P		7,5 to 23	V
Operating ambient temperature range	T_{amb}		−30 to + 80	^oC

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

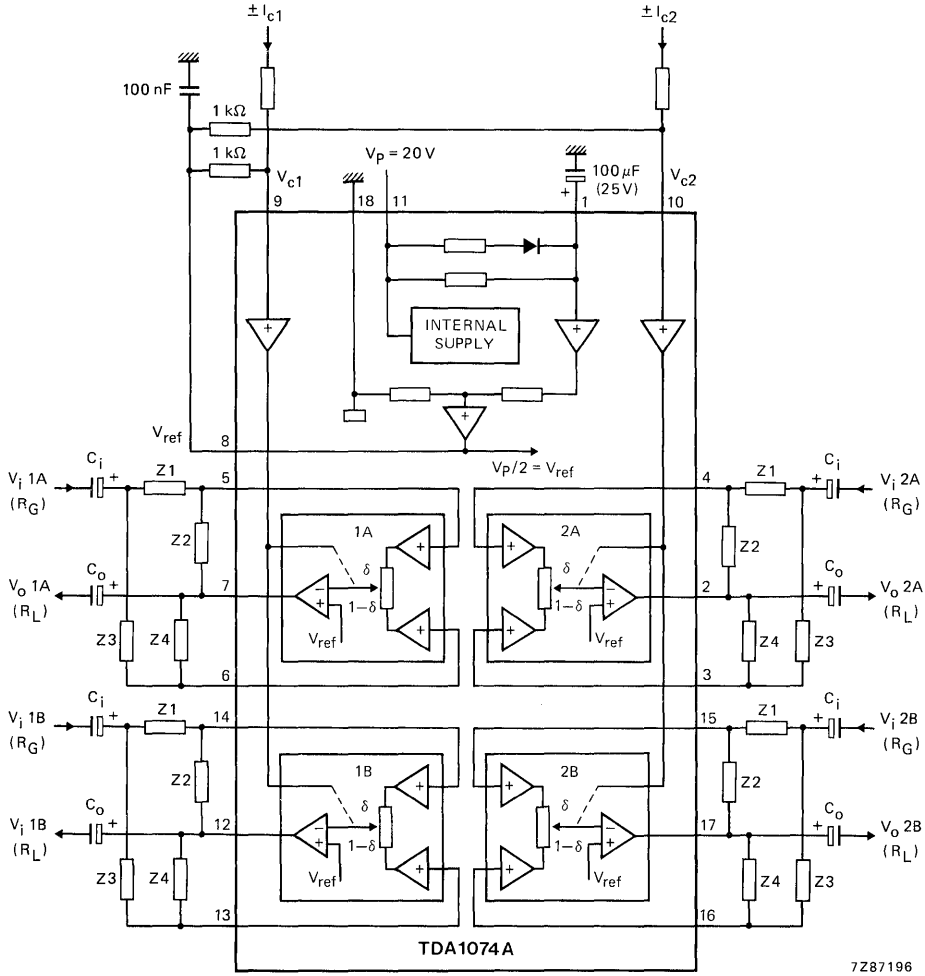


Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance R_G = 60 Ω; the output load resistance R_L = 4,7 kΩ; the coupling capacitors at the inputs and outputs are C_i = 2,2 µF and C_o = 10 µF respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23	V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1	V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i		0 to V_P	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

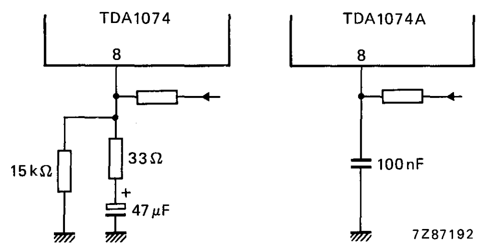


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; R_L > 4,7 kΩ; C_L < 30 pF; f = 1 kHz; with a linear frequency response (V_{c1} = V_{c2} = 0 V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) $V_{c1} = V_{c2} = 0$ V	f	10	–	20 000	Hz
Voltage gain at linear frequency response ($V_{c1} = V_{c2} = 0$ V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at $\pm V_{c1} = \pm V_{c2}$ = 120 mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) V_{c2} = 120 mV		–	17,5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2}$ = 120 mV		–	17,5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) V_{c1} = 120 mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1}$ = 120 mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)}$ = 300 mV f = 1 kHz (measured selectively)	THD	–	0,002	–	%
f = 20 Hz to 20 kHz	THD	–	0,005	–	%
at $V_{o(rms)}$ = 5 V f = 1 kHz	THD	–	0,015	0,1	%
f = 20 Hz to 20 kHz	THD	–	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i;\,o(rms)}$	5,5	6,2	–	V
Power bandwidth at reference level $V_{o(rms)}$ = 5 V (−3 dB); THD = 0,1%	B	–	40	–	kHz
Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	–	86	–	dB
f = 20 Hz to 20 kHz	α_{ct}	–	80	–	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	–	20	–	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	–	46	–	dB

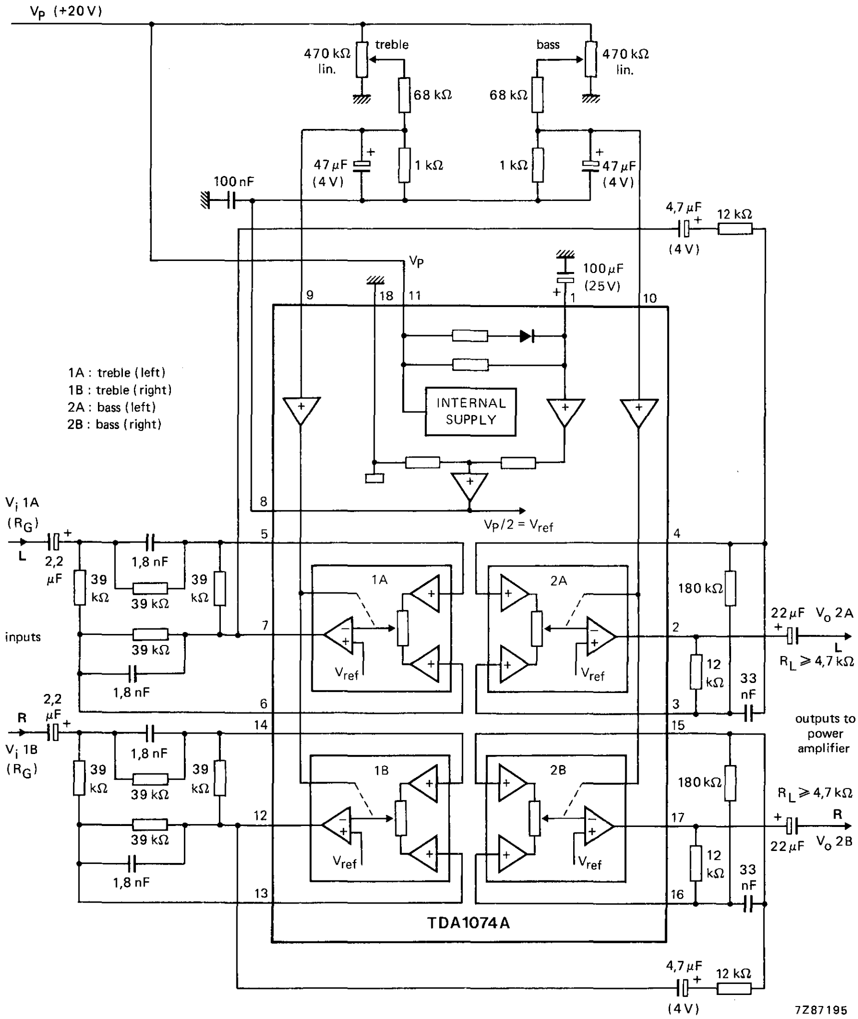


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

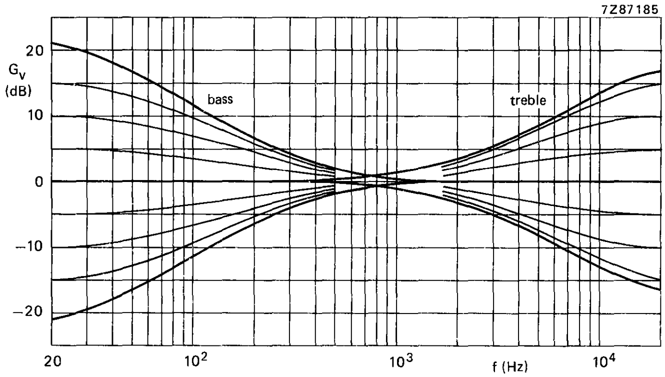


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

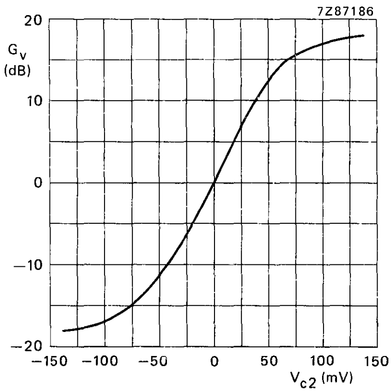


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

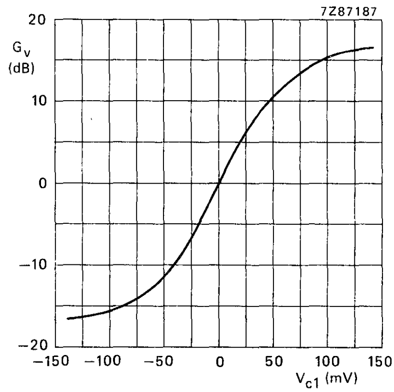
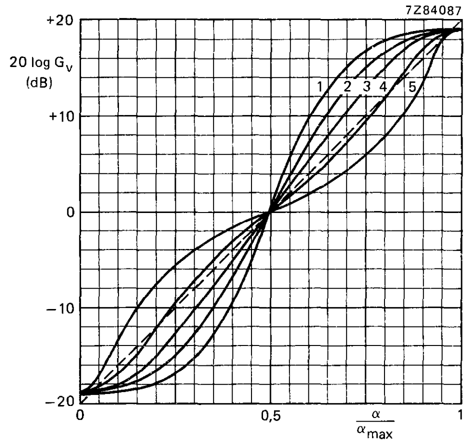


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

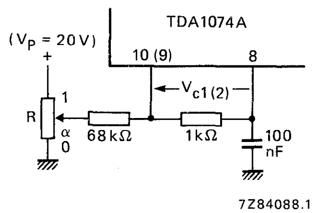


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

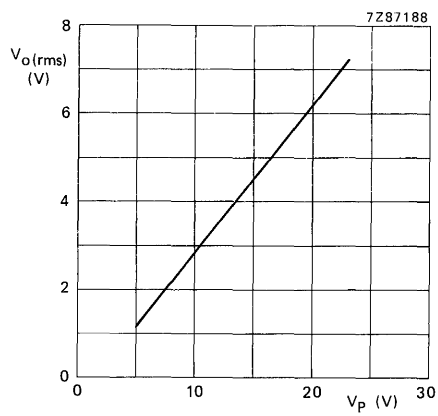


Fig. 9 Output signal level as a function of V_P; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2}$ = 0 V.

APPLICATION INFORMATION (continued)

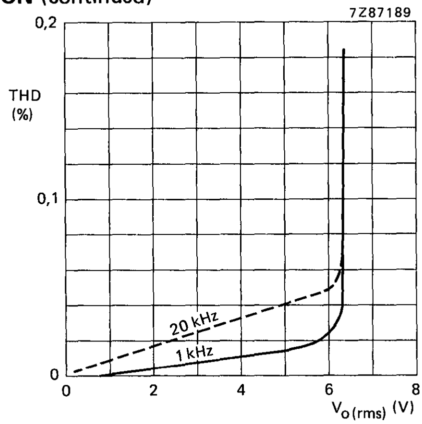


Fig. 10 Total harmonic distortion as a function of the output level; V_P = 20 V; R_L = 4,7 kΩ; V_{c1} = V_{c2} = 0 V (linear, $G_{v\,tot}$ = 1). ——— f = 1 kHz; – – – – f = 20 kHz.

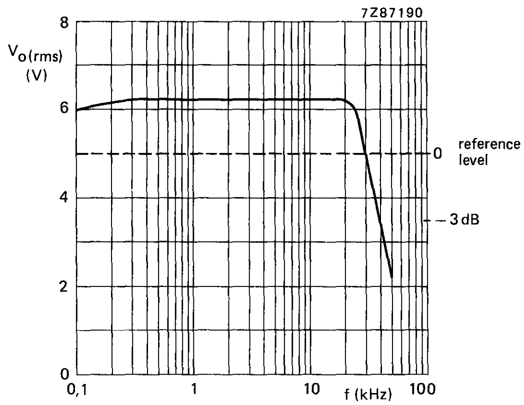


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

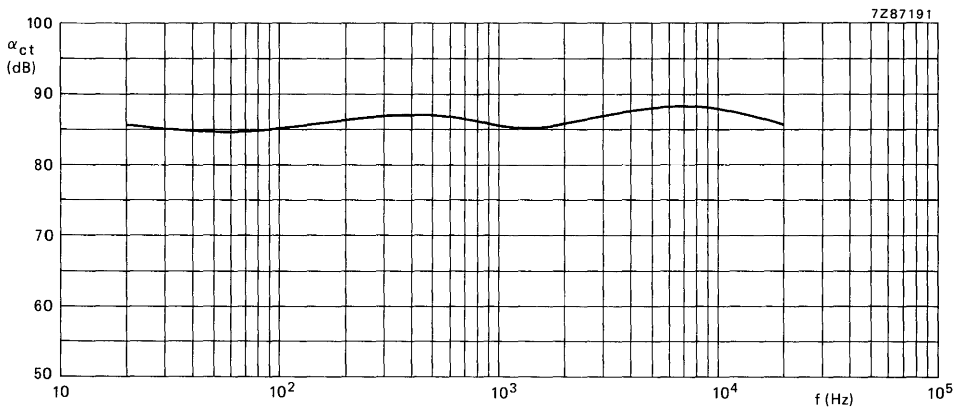
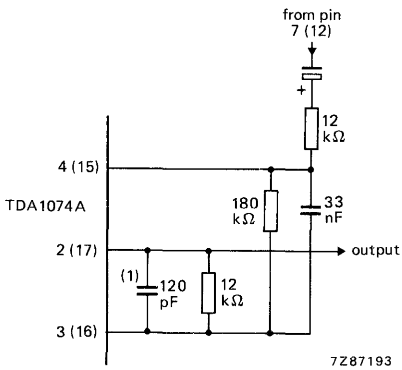


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting (V_{c1} = V_{c2} = 0 V); V_i = 5 V; R_G = 60 Ω; R_L = 4,7 kΩ.

Application recommendations

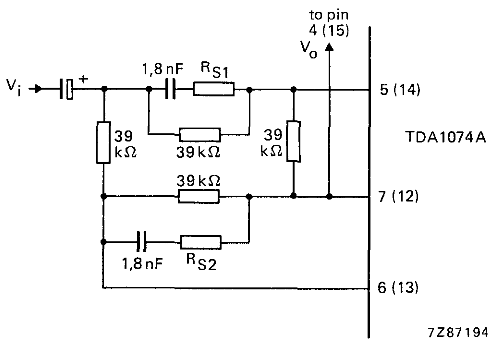
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8(V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For $R_{S1} = R_{S2}$ = 3,3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

24 W BTL OR 2 × 12 W STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1510/TDA1510A is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6 Ω). With a supply voltage (V_P) of 14,4 V, an output power of 24 W can be delivered into a 4 Ω Bridge Tied Load (BTL), or when used as a stereo amplifier, 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Features

- Flexibility – stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range:						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	28,0	V
non-operating, load dump protection		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current		I_{so}	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$\|Z_I\|$	1	–	–	MΩ
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

TDA1510: 13-lead SIL-bent-to-DIL; plastic power (SOT141B).
TDA1510A: 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

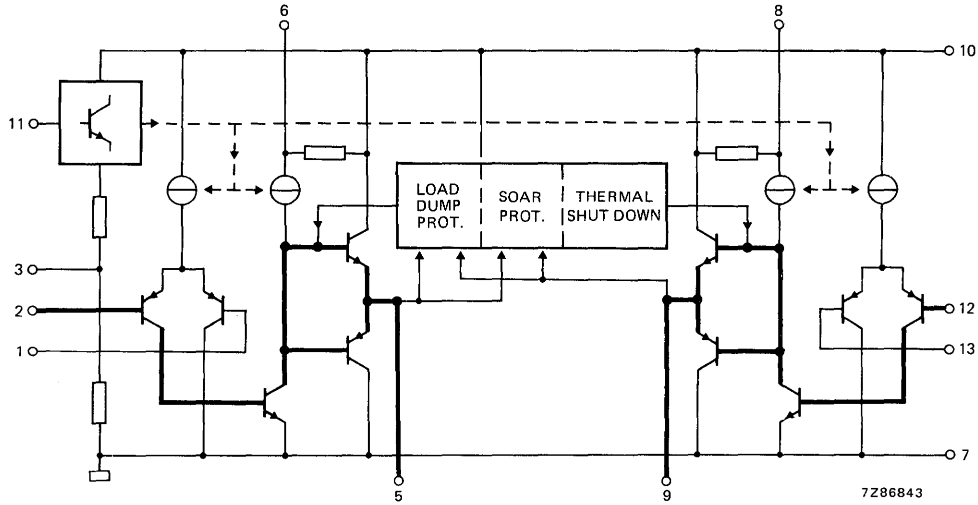
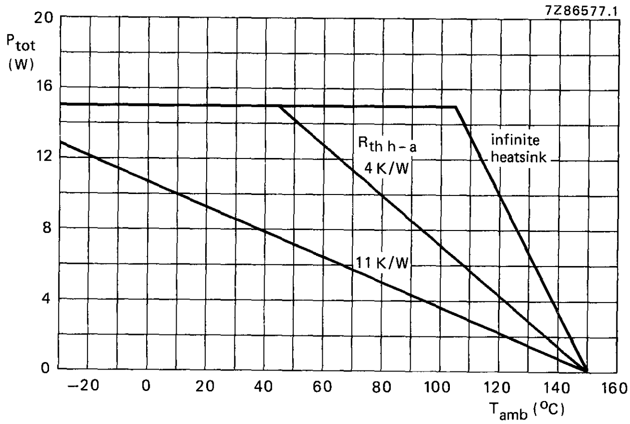


Fig. 1 Functional diagram; heavy lines indicate signal paths.

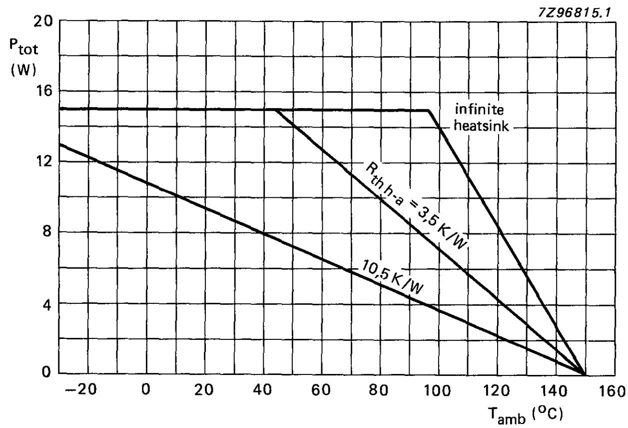
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage:					
operating	pin 10	V_P	–	18	V
non-operating		V_P	–	28	V
non-operating, load dump protection	during 50 ms	V_P	–	45	V
Peak output current		I_{OM}	–	6	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Crystal temperature		T_c	–	+ 150	°C



(a)



(b)

Fig. 2 Power derating curves; (a) TDA1510, (b) TDA1510A.

HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

TDA1510 ($R_{th\ j\text{-}mb}$) = 3 K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3 = 4\ \text{K/W}$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3 = 11\ \text{K/W}$$

TDA1510A ($R_{th\ j\text{-}mb}$) = 3,5 K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3{,}5 = 3{,}5\ \text{K/W}$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3{,}5 = 10{,}5\ \text{K/W}$$

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	6,0	14,4	18,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current	$V_{11} \leqslant V_{10}$; note 1	I_{so}	0,15	0,35	0,80	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

parameter	parameter	symbol	min.	typ.	max.	unit
Bridge Tied Load application (BTL)						
Output power with bootstrap	note 6; R_L = 4 Ω					
	V_P = 13,2 V					
	d_{tot} = 0,5%	P_o	–	15,0	–	W
	d_{tot} = 10%	P_o	–	20,0	–	W
	V_P = 14,4 V					
	d_{tot} = 0,5%	P_o	15,5	18,0	–	W
	d_{tot} = 10%	P_o	20,0	24,0	–	W
Open loop voltage gain		G_o	–	75	–	dB
Closed loop voltage gain	note 2	G_c	39,5	40,0	40,5	dB
Frequency response	at –3 dB; note 3	f_r	–	20 to > 20 k	–	Hz
Input impedance	note 4	$\|Z_i\|$	1	–	–	MΩ
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz					
	R_S = 0 Ω	$V_{n\ (rms)}$	–	0,2	–	mV
	R_S = 10 kΩ	$V_{n\ (rms)}$	–	0,35	0,8	mV
	R_S = 10 kΩ; according to IEC 179 curve A	$V_{n\ (rms)}$	–	0,25	–	mV
Supply voltage ripple rejection	f = 100 Hz; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$\|\Delta V_{5-9}\|$	–	2	50	mV
Power bandwidth	–1 dB; d_{tot} = 0,5%	B	–	30 to > 40 k	–	Hz

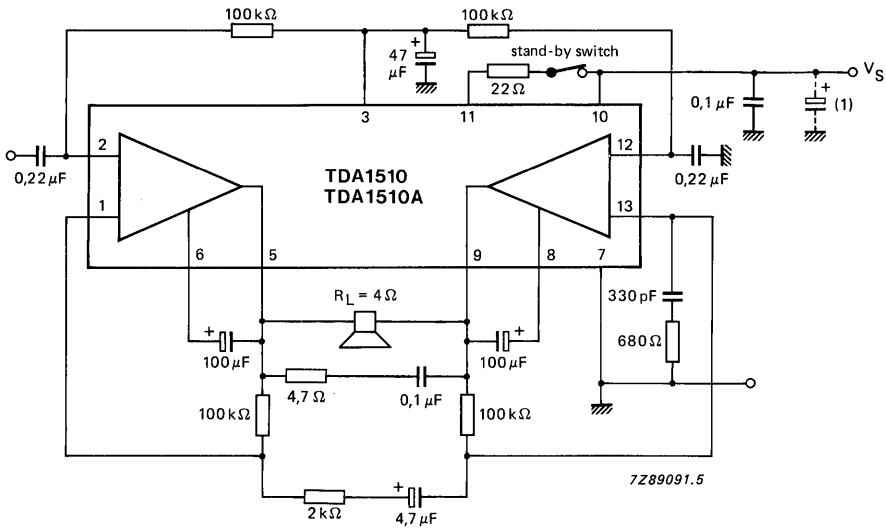
A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power; with bootstrap	note 6;					
	$R_L = 4\ \Omega$					
	$V_P = 13,2$ V					
	$d_{tot} = 0,5\%$	P_o	–	4,5	–	W
	$d_{tot} = 10\%$	P_o	–	6,0	–	W
	$V_P = 14,4$ V					
	$d_{tot} = 0,5\%$	P_o	4,5	5,5	–	W
	$d_{tot} = 10\%$	P_o	6,0	7,0	–	W
	$R_L = 2\ \Omega$					
	$V_P = 13,2$ V					
	$d_{tot} = 0,5\%$	P_o	–	7,5	–	W
	$d_{tot} = 10\%$	P_o	–	10,0	–	W
	$V_P = 14,4$ V					
	$d_{tot} = 0,5\%$	P_o	7,75	9,0	–	W
	$d_{tot} = 10\%$	P_o	10,0	12,0	–	W
Output power; without bootstrap	notes 6, 8 and 9					
	$R_L = 4\ \Omega$					
	$V_P = 14,4$ V					
	$d_{tot} = 10\%$	P_o	–	6	–	W
Frequency response	notes 3 and 6					
	–3 dB	f_r	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	f = 1 kHz	SVRR	–	50	–	dB
Channel separation	$R_S = 10\ k\Omega$;					
	f = 1 kHz	α	40	50	–	dB
Closed loop voltage gain	note 7	G_c	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz;					
	$R_S = 0\ \Omega$	$V_{n(rms)}$	–	0,15	–	mV
	$R_S = 10\ k\Omega$	$V_{n(rms)}$	–	0,25	–	mV
	$R_S = 10\ k\Omega$; according to IEC179 curve A	$V_{n(rms)}$	–	0,2	–	mV

Notes to the characteristics

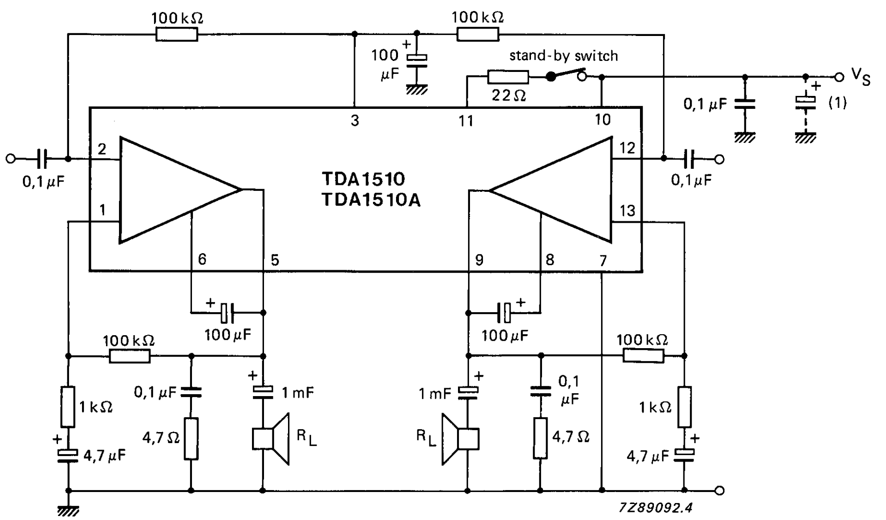
1. If $V_{11} > V_{10}$ then I_{11} must be < 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 and the 100 μF capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.

APPLICATION INFORMATION



(1) belongs to power supply

Fig. 3 Test and application circuit; Bridge Tied Load (BTL).



(1) belongs to power supply

Fig. 4 Test and application circuit; stereo mode.

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