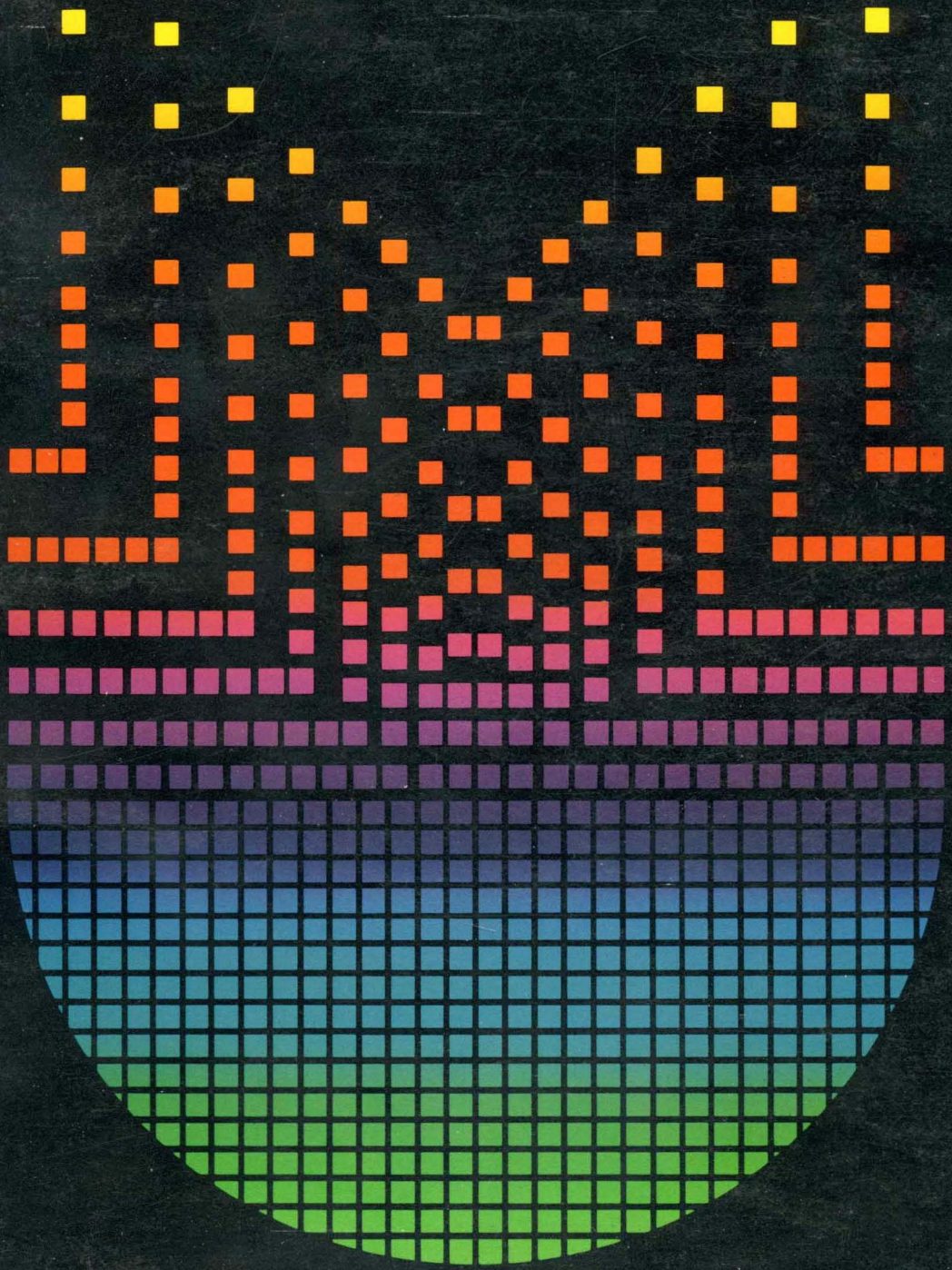
MICROCOMPUTER COMPONENTS

RAYTHEON



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INTRODUCTION

THE THIRD REVOLUTION

Over the past three years, the semiconductor industry has experienced the third revolutionary period of its relatively short history. The first of these occurred in the fifties with the introduction of mass-produceable transistors, which not only revolutionized the computer and communications industries, but also spawned a number of new companies and expanded the horizons of a number of older ones who elected to participate in this infant technology.

The second revolution occurred in the sixties when the first integrated circuits appeared. These first I.C.'s, featuring one or two gates per chip and selling for $20 to $30, created an even greater impact than the transistor itself. From the users' standpoint, I.C.'s allowed an order-of-magnitude increase in the complexity of the equipment they were designing (or an order-of-magnitude decrease in size, depending on the nature of that equipment) and, simultaneously, an order-of-magnitude improvement in cost-effectiveness. Coupled with this was a change in the engineering disciplines required by the user, since circuit designers, as such, were being replaced by logic designers and systems architects.

The second revolution caused a similar change in the semiconductor industry since it was now hiring the circuit designers who were leaving the end-equipment field. In addition, manufacturing, reliability and marketing skills began to expand, converting the industry from one dominated by the semi-conductor "black-art" specialists to one somewhat more balanced in its approach to business. Those companies that recognized the revolution (including many new ones) survived and prospered while those that didn't dropped out.

Similar changes are occurring today during the third revolution—this one created by the development of microprocessors. Once again order-of-magnitude improvements are being enjoyed by those users who have recognized the significance of microcomputer technology, and once again the engineering disciplines employed by the end user are changing, the emphasis now being placed on programming and other software development activities.

From the semiconductor manufacturer's standpoint, the changes are equally significant. Logic design and system architecture are becoming necessary skills for those who hope to succeed in the seventies. Marketing and sales will also be upgraded as semiconductor manufacturers begin selling "systems" rather than "components." Applications, training, software and hardware development tools and development systems are all new demands placed on the semiconductor manufacturer who hopes to survive the third revolution.

As with the first two revolutions, the inception of the microprocessor was characterized by the introduction of many different device types from many different manufacturers using many different technologies. Some of these will become high volume, multi-sourced, industry standard products (like TTL) and others will survive at lower volumes because they have certain performance advantages which the "standard" devices cannot match in selected applications (similar to the role played by CMOS and ECL).

Most, however, will fall by the wayside as manufacturing efficiency and competitive pressures force the price to a point where the non-standard types become unprofitable. This point is rapidly approaching in the microprocessor area. The selection of the right microprocessor, therefore, is one of the current challenges facing today's system designer.

There are, today, basically two markets for microprocessors and two basic approaches being employed by semiconductor manufacturers to satisfy those markets. The two markets can best be defined as the *logic replacement market* and the *performance market.* The logic replacement market is best characterized by a certain cost-performance inelasticity which states that once a certain minimal performance level is achieved, no additional cost (and presumably selling price) can be justified in terms of additional units sold. Thus, the emphasis in the logic replacement market is either cost reduction at a given performance level or increased performance at no increase in cost. (This market, for example, would use TTL logic in applications where TTL performance was not required, but where TTL was the lowest cost solution.)

In the performance market, cost-performance is relatively elastic; i.e. additional end-equipment performance can demand a higher selling price and still provide the manufacturer with added volume and/or revenue. Here, the tendency would be to use the highest performance technology available in an effort to gain a performance edge over competition.

The two basic technologies which today compete for the total microprocessor market are Metal-Oxide-Semiconductor (MOS) and bipolar. While some overlap does exist, the market generally has accepted MOS in the logic replacement segment and bipolar in the performance segment.

With the large number of MOS alternatives available, the system designer has no simple chore in determining the best solution for his application. Not only does he have a choice of 4, 8, 12, and 16 bit devices, but once settling on the size of his data word, he'll have up to a dozen different n-bit designs to choose from. As with most alternatives of this nature, any one of a number of different designs will meet his system requirements and the designer will be apt to choose one of the two or three types within each category that appear to be "industry standards."

The situation is not quite as confusing in the bipolar arena simply because there are not as many alternatives as with the MOS approach. This is partially explained by the fact that most bipolar designs are bit-slice oriented thus eliminating the need to fix the size of the data word prior to selecting a particular bit slice design.

Perhaps even more significant in explaining the relatively small number of bipolar alternatives is the nature of the performance market which uses the technology. Since this

market tends to be smaller than the logic replacement market in terms of the number of users, the breadth of applications and the total amount of end-user equipment shipped, there is not the need for nor the incentive to create a large number of different device types. Thus, the semiconductor industry—at least to this point in time—has elected to concentrate their efforts on a relatively small number of device types.

One of these types (in fact the only one currently supported by more than two manufacturers) is the 2900 family, a bit slice approach introduced to the market in 1975. This state-of-the art family consists of a series of MSI/LSI devices designed to complement and enhance one another in typical microcomputer applications.

Recognizing the need for multi-sourcing in the market served by bipolar microprocessors, Raytheon, in 1975, became the first alternate source for 2900 family products and today has more 2900 family parts than any other semiconductor manufacturer in the industry except for AMD who originated the series. In addition, Raytheon is committed to the continued support of the family, not only to the extent of providing all 2900 series devices, but also in the equally important areas of bipolar memory, logic, and the development tools required for both hardware and software design.

THE 2900 FAMILY

All microcomputers (in fact all practical digital computers) consist of four basic functions—central processing unit (CPU), control, memory, and input/output (I/O). (See Figure 1) Connecting the various functions are the address and data busses plus various control lines. While all microcomputers have essentially the same general architecture (i.e. perform the four functions shown in Figure 1), there are a number of differences in the way the various functions are implemented. The most obvious differences occur between MOS and bipolar technologies.

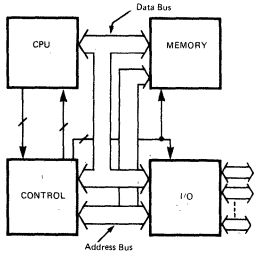


Figure 1. Typical Computer Functions.

In the MOS approach, for example, the most common implementation places the CPU and control function both on one chip. This chip—which was the original "microprocessor"—inputs instructions and data, performs the operation required by the instruction, and outputs the resulting data. It also provides the addressing function to locate the instructions in memory, and to read or write data in memory and/or I/O. Because the decoding circuitry for the instructions (the main portion of the control section) is hardwired on the chip, the same instruction (set of "1's" and "0's") will always cause the same operation (Add, Subtract, Compare, etc.) to be performed, and therefore, the instruction set is said to be "fixed". This is one of the major distinctions between MOS and bipolar microprocessors.

The microprocessor, however, is not a computer until one adds the memory and I/O circuits. In the case of MOS, this normally consists of ROM or PROM for program storage, RAM for data storage, and either discrete logic or special purpose LSI chips for I/O.*

*Some newer MOS devices include some memory and I/O capability or the same chip as the CPU and control. While somewhat limited in capability, these new chips can realistically be called microcomputers without the necessity of external memory or I/O.

With the more popular bipolar microprocessors, such as the 2900 family, the CPU and control function are implemented differently. The CPU, for example, rather than being a fixed number of data bits wide (4, 8, 12, or 16 as in MOS) is actually a 2 or 4 bit slice that can be cascaded to any width that is a multiple of the basic slice. A four bit slice such as the 2901, for example, can be used to implement 4, 8, 12, 16 . . . . . 32, etc. bit microcomputers.

There are some obvious advantages and disadvantages to a bit slice approach when compared to the fixed data word, MOS approach. The disadvantage is, of course, that more chips are required per CPU.

Not only does the CPU function usually require more chips in bipolar designs, but also the control function is not even included on the chip as it is with the MOS devices. There are, however, advantages to bit slices over fixed data word machines; one of the most obvious being the capability of building larger, more powerful machines. In MOS, there simply isn't anything available over 16 bits, while 24, 32, and even 48 bit bipolar microcomputers have been designed and manufactured. Since wider data paths usually mean higher throughput, the bipolar approach can usually provide higher performance simply by building a bigger machine.

The other major architectural difference between MOS and bipolar is in the implementation of the control function. As mentioned previously, the MOS controller shares the same chip with the CPU and features a fixed instruction decoder. The bit slice controller, on the other hand, is constructed using a number of devices including PROMs, registers, and sequencers. (See Figure 2)

As in the case of the MOS controller, the main function of the bipolar equivalent is to accept instructions from memory via the data bus, decode the instruction, and then provide the individual control signals to the CPU, memory, and I/O. These control signals are generated by combining the decoded instruction with a multi-phase clock to provide a properly timed sequence of control words to the various system elements.

As shown in Figure 2, (*) the control signals for the CPU, memory, and I/O are actually outputs from an array of PROMs ③ . Each set of these control signals will cause a specific action to occur during a given clock period. Since it normally takes a series of these signals to actually accomplish what is normally considered to be a machine instruction (add, subtract, etc.), the individual sets are referred to as microinstructions. Thus, a machine instruction (or macroinstruction) consists of a series of microinstructions emanating from the PROM array.

*Figure 2 shows only the major system elements for clarity. Various register and other logic elements will be required in an actual design.

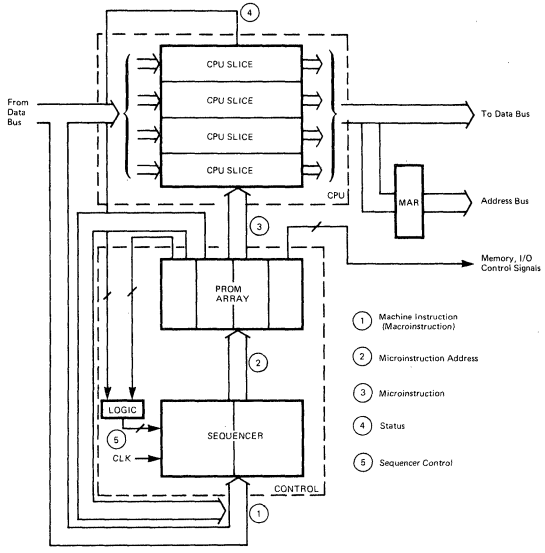


Figure 2. Typical Bit-Slice Implementation for CPU and Control.

As one might expect, the series of microinstructions to accomplish a common machine instruction would be stored in consecutive address locations in the PROMs. Thus to accomplish a machine instruction—say an ADD—one would simply set a counter with the address of the first microinstruction of the ADD sequence and then simply increment the counter as each microinstruction is completed. This would continue until the final microinstruction of the ADD series was executed at which time the control would be set to accept the next machine instruction.

The circuitry that provides the addressing and counting functions is called a sequencer and most bipolar microprocessor families provide special LSI chips to accomplish this function. For example, the 2900 family currently provides two such circuits—the 2909 and 2911—and a third is in development. As with the CPU chips, sequencers are normally provided as slices to allow for a variety of microprogram sizes.

In addition to the addressing and counting functions, most sequencers provide circuitry to accommodate skips, jumps, and branches in the microprogram. This is accomplished by combining CPU status information ④ with a portion of the microcode to exercize control over the source of the next microinstruction address.

As in any microcomputer implementation, the machine instruction is stored in main memory (usually PROM) and is presented to the control circuit via the data bus ①. In most bipolar architectures, the machine instruction is simply the starting address of the sequence of microinstructions which will be used to actually accomplish the machine instruction.

As with the bipolar CPU, there are advantages and disadvantages in the manner in which the control function is implemented. One obvious disadvantage is chip count. It normally requires in excess of 10 packages to construct a bipolar microprocessor controller whereas the MOS controller is provided as part of the CPU chip.

The other factor which is sometimes considered to be a disadvantage is the necessity of generating the microinstructions. While this does, in essence, require twice the programming effort compared with MOS microprocessor programming, it is, at the same time, one of the features which enhances the performance aspects of the bipolar approach. By designing his own instruction set—which is precisely what the microprogrammer is doing—the user can tailor the instructions to his unique application, which improves performance and minimizes macroprogram storage requirements.

The ability to microprogram his machine also allows the user to emulate virtually any computer architecture (including many of today's popular mini's) thus making it possible to utilize existing applications software which often is more costly to generate than the hardware.

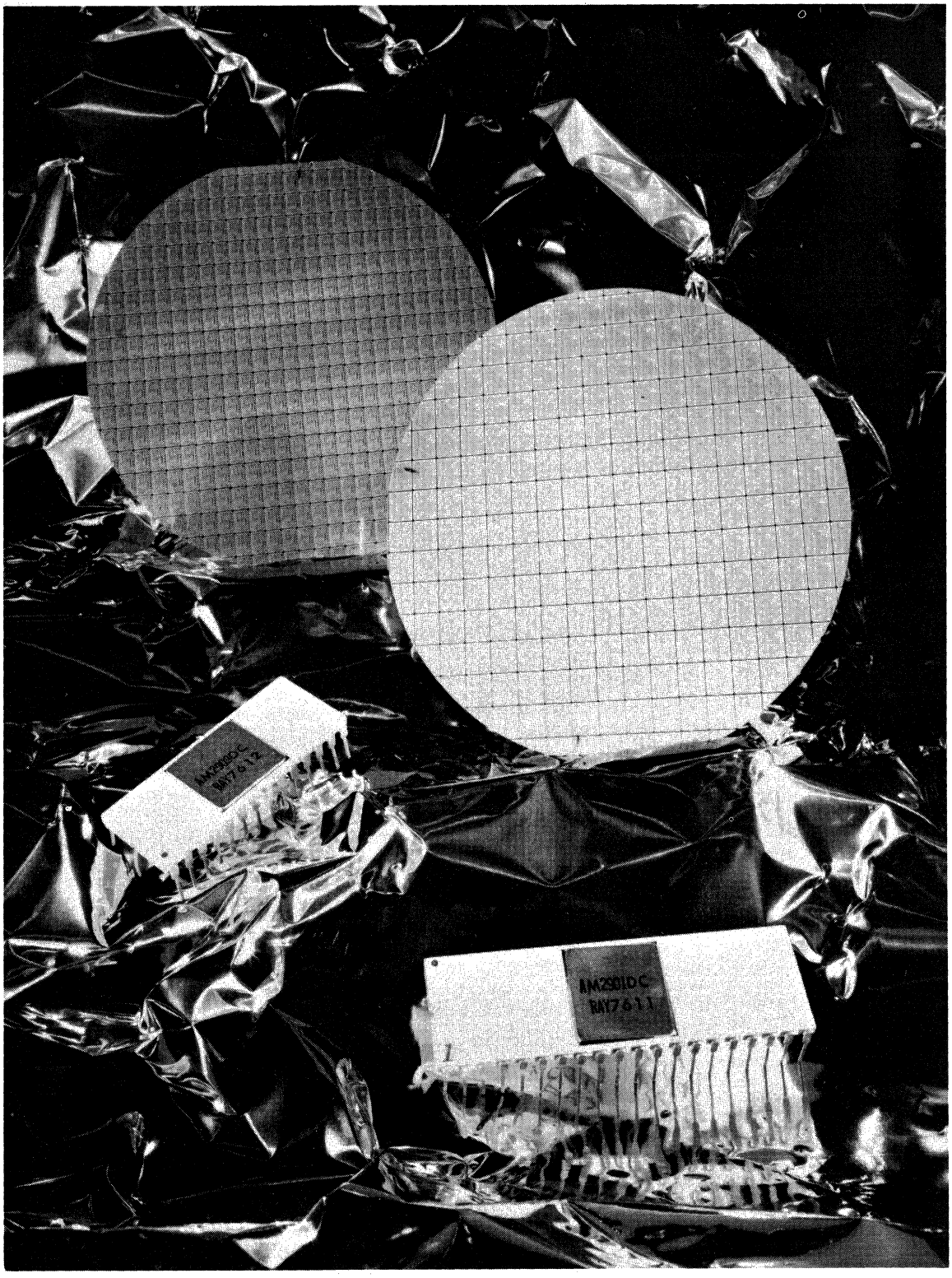
SUMMARY

In the following pages of this catalog, a detailed description of each member of the 2900 family is presented in the form of a data sheet. Where additional information is required to fully explain the function of a given device, a users guide is also provided.

In addition, data sheet and applications information is provided for Raytheon's bipolar memory products (PROMs and RAMs) since they will form an integral part of any bipolar microcomputer design.

Finally, a simple system design is presented to further clarify the basic operation of the 2900 family and to give a typical example of the procedure used to design bipolar microcomputer systems.

If there are any questions regarding the material presented in this catalog or for any additional information or applications assistance, simply contact Raytheon's Application Staff by calling 415-968-9211 and asking for Microprocessor Applications.


AM2901DC
RN7611

Four-Bit Bipolar Microprocessor Slice

Am2901

GENERAL DESCRIPTION

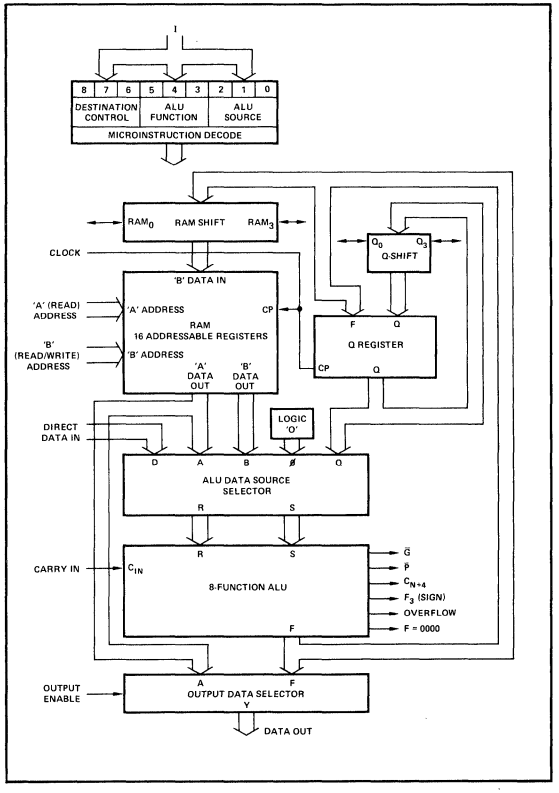
The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.

MICROPROCESSOR SLICE BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2901PC
Hermetic DIP	0°C to +70°C	AM2901DC
Hermetic DIP	–55°C to +125°C	AM2901DM
Hermetic Flat Pack	–55°C to +125°C	AM2901FM
Dice	0°C to +70°C	AM2901XC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2901PC, DC	0°C to +70°C	4.75 V to 5.25 V
Am2901DM, FM	−55°C to +125°C	4.50 V to 5.50 V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Am2901DM,FM
Pre-Seal Visual Inspection	2010	B	100%
Stabilization Bake	1008	C 24-hour 150°C	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%
Centrifuge	2001	B 10,000G	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100%
Gross Leak	1014	C2 Fluorocarbon	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%
Insert Additional Screening here for Class B Parts			
Group A Sample Tests	5005	See below for definitions of subgroups	
Subgroup 1			LTPD = 5
Subgroup 2			LTPD = 7
Subgroup 3			LTPD = 7
Subgroup 7			LTPD = 7
Subgroup 8			LTPD = 7
Subgroup 9			LTPD = 7

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level Am2901DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2 and 3)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
			I_{OH} = −1.0mA, C_{n+4}	2.4			
			I_{OH} = −800µA, OVR, $\overline{P}$	2.4			
			I_{OH} = −600µA, F_3	2.4			
			I_{OH} = −600µA $RAM_{0,3}, Q_{0,3}$	2.4			
			I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA $Y_0, Y_1, Y_2, Y_3, \overline{G}$			0.5	Volts
			I_{OL} = 10mA, C_{n+4}, F=0			0.5	
			I_{OL} = 8.0mA, OVR, $\overline{P}$			0.5	
			I_{OL} = 6.0mA, F_3 $RAM_{0,3}, Q_{0,3}$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Military			0.7	Volts
			Commercial			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX. V_{IN} = 0.5V	Clock, $\overline{OE}$			−0.36	mA
			A_0, A_1, A_2, A_3			−0.36	
			B_0, B_1, B_2, B_3			−0.36	
			D_0, D_1, D_2, D_3			−0.72	
			I_0, I_1, I_2, I_6, I_8			−0.36	
			I_3, I_4, I_5, I_7			−0.72	
			$RAM_{0,3}, Q_{0,3}$ (Note 4)			−0.8	
			C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX. V_{IN} = 2.7V	Clock, $\overline{OE}$			20	µA
			A_0, A_1, A_2, A_3			20	
			B_0, B_1, B_2, B_3			20	
			D_0, D_1, D_2, D_3			40	
			I_0, I_1, I_2, I_6, I_8			20	
			I_3, I_4, I_5, I_7			40	
			$RAM_{0,3}, Q_{0,3}$ (Note 4)			100	
			C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V		50	µA
				V_O = 0.5V		−50	
			$RAM_{0,3}, Q_{0,3}$	V_O = 2.4V (Note 4)		100	
				V_O = 0.5V (Note 4)		−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V V_O = 0.5V	$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−15		−40	mA
			C_{n+4}	−15		−40	
			OVR, $\overline{P}$	−15		−40	
			F_3	−15		−40	
			$RAM_{0,3}, Q_{0,3}$	−15		−40	
I_{CC}	Power Supply Current	V_{CC} = MAX.	Military		185	280	mA
			Commercial		185	280	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.

GUARANTEED OPERATING CONDITIONS OVER TEMPERATURE AND VOLTAGE

Tables I, II, and III below define the timing requirements of the Am2901 in a system. The Am2901 is guaranteed to function correctly over the operating range when used within the delay and set-up time constraints of these tables for the appropriate device type. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

The performance of the Am2901 within the limits of these tables is guaranteed by the testing defined as "Group A, Subgroup 9" Electrical Testing. For a copy of the tests and limits used for subgroup 9, contact Product Marketing.

TABLE I

CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	Am2901DC, PC	Am2901DM, FM
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	105ns	120ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	9.5MHz	8.3MHz
Minimum Clock LOW Time	30ns	30ns
Minimum Clock HIGH Time	30ns	30ns
Minimum Clock Period	105ns	120ns

TABLE II

MAXIMUM COMBINATIONAL PROPAGATION DELAYS (all in ns, $C_L \leq 15pF$)

From Input \ To Output	Am2901DC, PC (0°C to +70°C; 5V ±5%)								Am2901DM, FM (−55°C to +125°C; 5V ±10%)							
	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs		Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 470	OVR	Shift Outputs	
							RAM_0 RAM_3	Q_0 Q_3							RAM_0 RAM_3	Q_0 Q_3
A, B	110	85	80	80	110	75	110	–	120	95	90	90	120	85	120	–
D (arithmetic mode)	100	70	70	70	100	60	95	–	110	80	75	75	110	65	105	–
D (I = X37) (Note 5)	60	50	–	–	60	–	60	–	65	55	–	–	65	–	65	–
C_n	55	35	30	–	50	40	55	–	60	40	30	–	55	45	60	–
I_{012}	85	65	65	65	80	65	80	–	90	70	70	70	85	70	85	–
I_{345}	70	55	60	60	70	60	65	–	75	60	65	65	75	65	70	–
I_{678}	55	–	–	–	–	–	45	45	60	–	–	–	–	–	50	50
$\overline{OE}$ Enable/Disable	40/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A bypassing ALU (I = 2xx)	60	–	–	–	–	–	–	–	65	–	–	–	–	–	–	–
Clock ↓ (Note 6)	115	85	100	100	110	95	105	60	125	95	110	110	120	105	115	65

SET-UP AND HOLD TIMES (all in ns) (Note 1)

TABLE III

From Input	Notes	Am2901DC, PC (0°C to +70°C, 5V ±5%)		Am2901DM, FM (−55°C to +125°C, 5V ±10%)	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
A, B Source	2, 4 3, 5	105 $t_{pw}L$ + 30	0	120 $t_{pw}L$ + 30	0
B Dest.	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ +15	0
D (arithmetic mode)		100	0	110	0
D (I = X37) (Note 5)		60	0	65	0
C_n		55	0	60	0
I_{012}		85	0	90	0
I_{345}		70	0	75	0
I_{678}	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
RAM_0, 3, Q_0, 3		30	0	30	0

Notes: 1. See Figure 11 and 12.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B dest." set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. DV0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

SET-UP AND HOLD TIMES (minimum cycles from each input)

Set-up and hold times are defined relative to the clock LOW-to-HIGH edge. Inputs must be steady at all times from the set-up time prior to the clock until the hold time after the clock. The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into one of the registers.

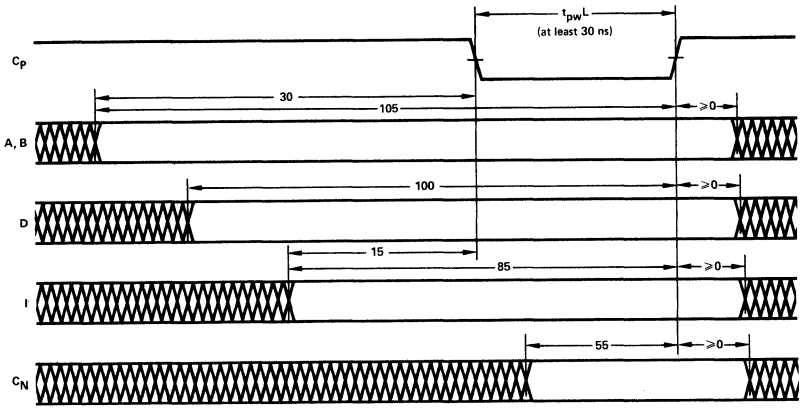
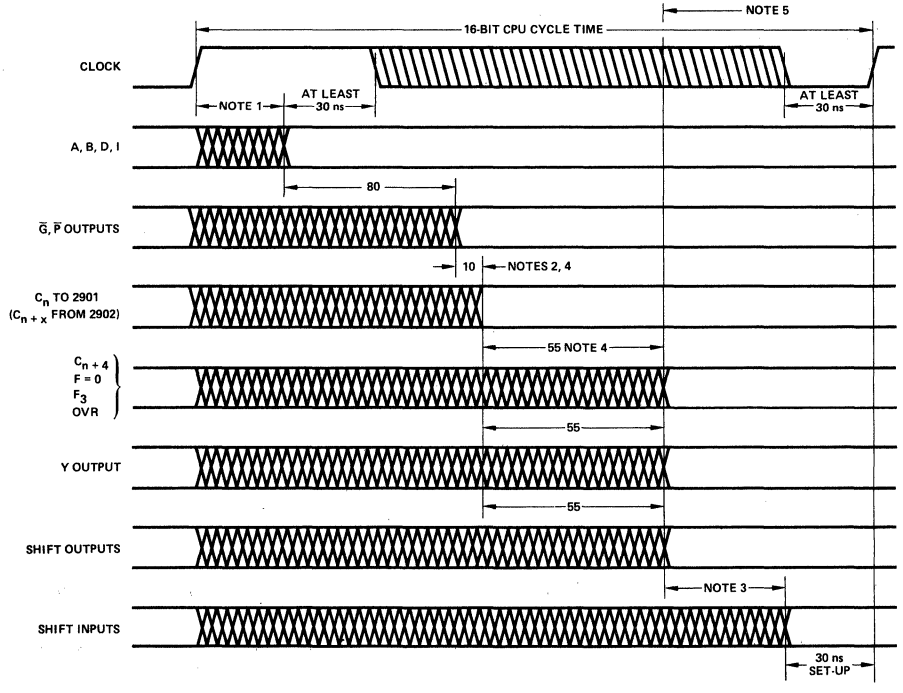


Figure 1. Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for Am2901DC, in ns. See Table III for Detailed Information.



Notes: 1. This delay is the max. t_{pd} of the register containing A, B, D, and I. For the Am2918, use 13ns.
2. 10ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 60ns.
3. This is the delay associated with the multiplexer between the shift outputs and shift inputs on the Am2901s. See Figure 19.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 2. Switching Waveforms for 16-Bit System Assuming A, B, D and I are all Driven from Registers with the same Propagation Delay, Clocked by the Am2901 Clock.

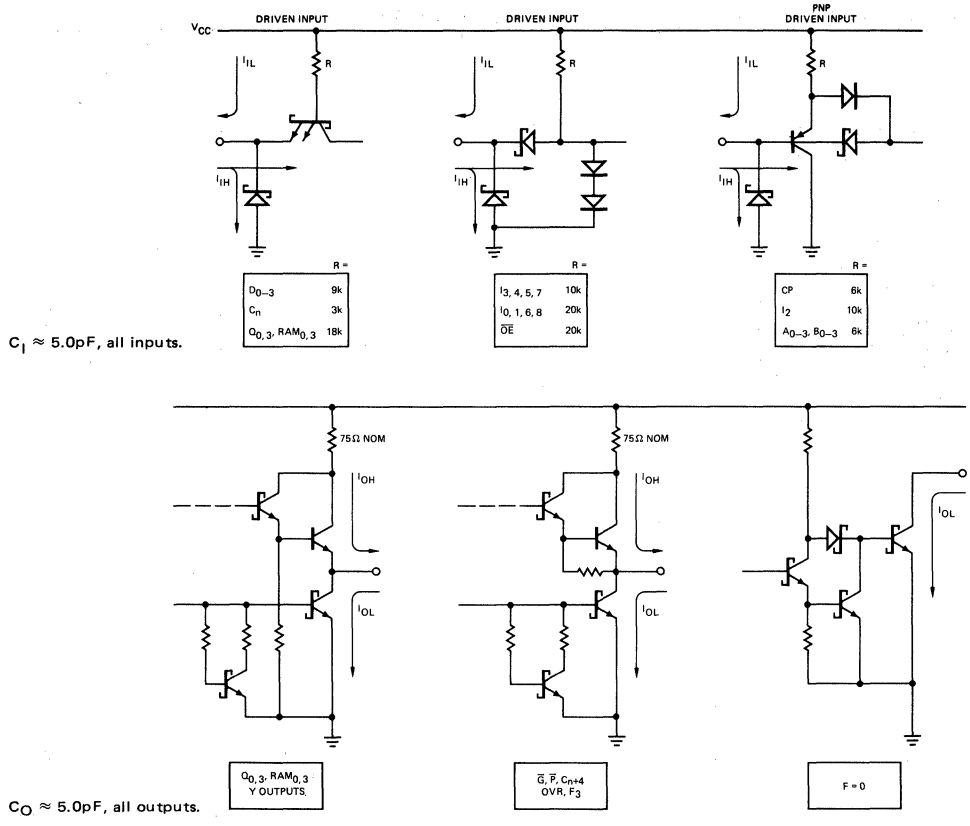


Figure 3. Am2901 Input/Output Current Interface Conditions.

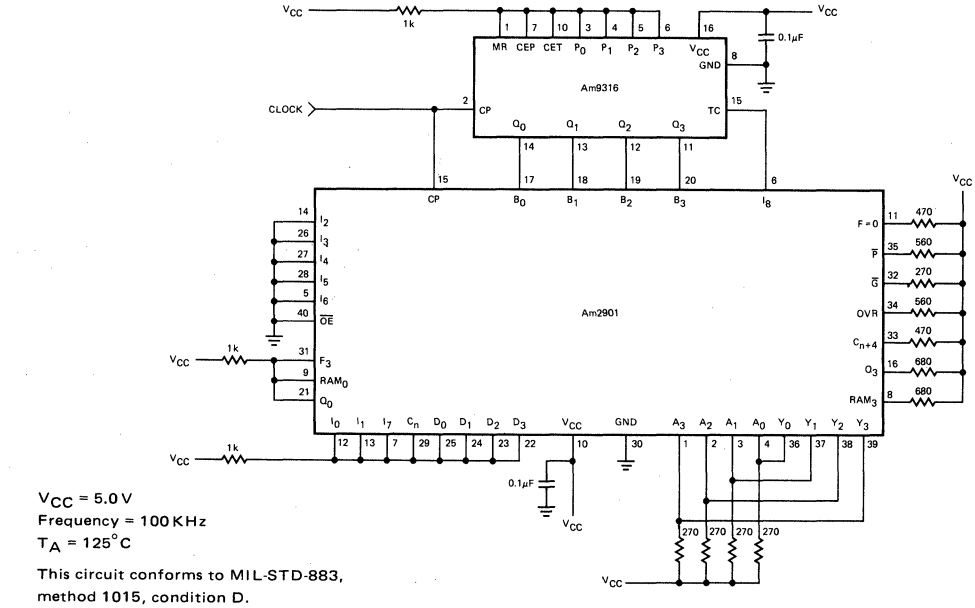
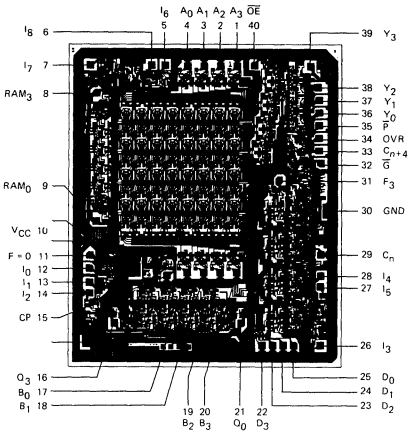


Figure 4. Am2901 Burn-In Circuit.

RAYTHEON

METALLIZATION AND PAD LAYOUT

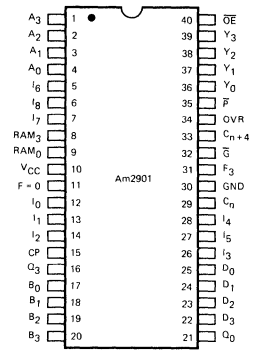


DIE SIZE 0.167" x 0.198"

CONNECTION DIAGRAM

Top View

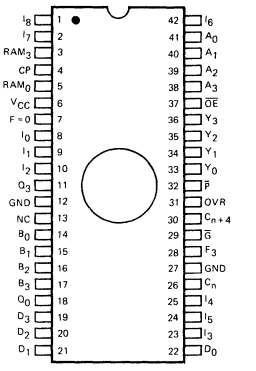
DIP



Note: Pin 1 is marked for orientation.

Top View

FLAT PACK



Note: Both grounds (pins 12 and 27) must be connected.

Figure 5.

DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines to the Am2901, used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the Am2901. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the Am2901. D_0 is the LSB.

Y_{0-3} The four data outputs of the Am2901. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Am2901's ALU. These signals are used with the Am2902 for carry-lookahead. See Figure 8 for the logic equations.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Figure 8 for logic equation.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n The carry-in to the Am2901's ALU.

C_{n+4} The carry-out of the Am2901's ALU. See Figure 8 for equations.

CP The clock to the Am2901. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which comprises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 6, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 7. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function.The definition of these inputs is shown in Figure 8. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902 ('182). A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 9.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 9.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 9.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

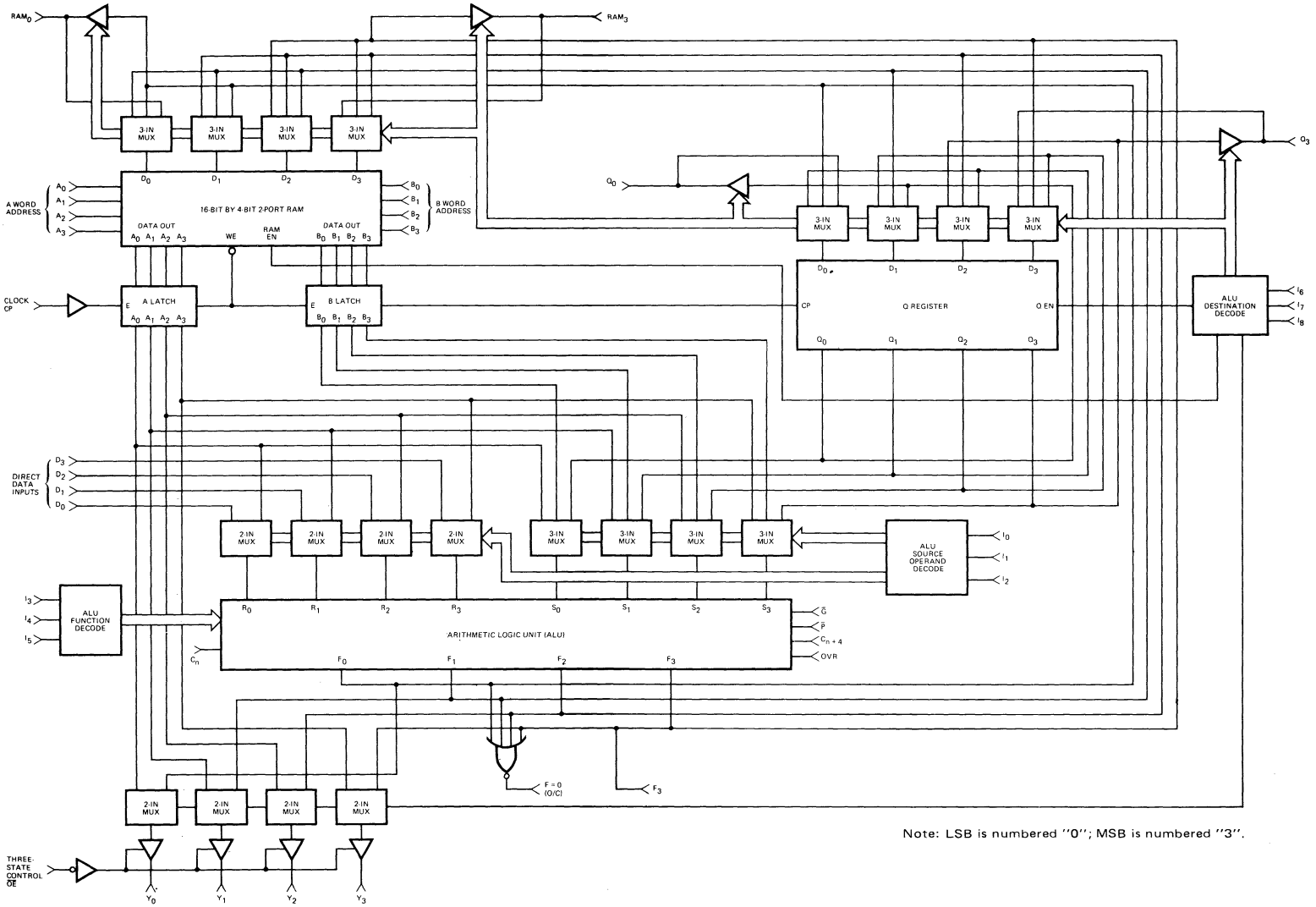


Figure 6. Detailed Am2901 Microprocessor Block Diagram.

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 7. ALU Source Operand Control.

MICRO CODE				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S − R
L	H	L	2	R Minus S	R − S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 8. ALU Function Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 9. ALU Destination Control.

OCTAL I_{210} OCTAL		0	1	2	3	4	5	6	7
I_{543} ALU Source / ALU Function		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 10. Source Operand and ALU Function Matrix.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 11. ALU Logic Mode Functions. (C_n Irrelevant)

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 10 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 11 defines the various logic operations that the Am2901 can perform and Figure 12 shows the arithemtic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 12. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 7.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1} + \overline{P_3P_2P_1P_0\,(G_0 + \overline{C_n})}$	See note

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 13.

FUNCTIONAL DESCRIPTION

The Am2902 is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902 is generally used with the 2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

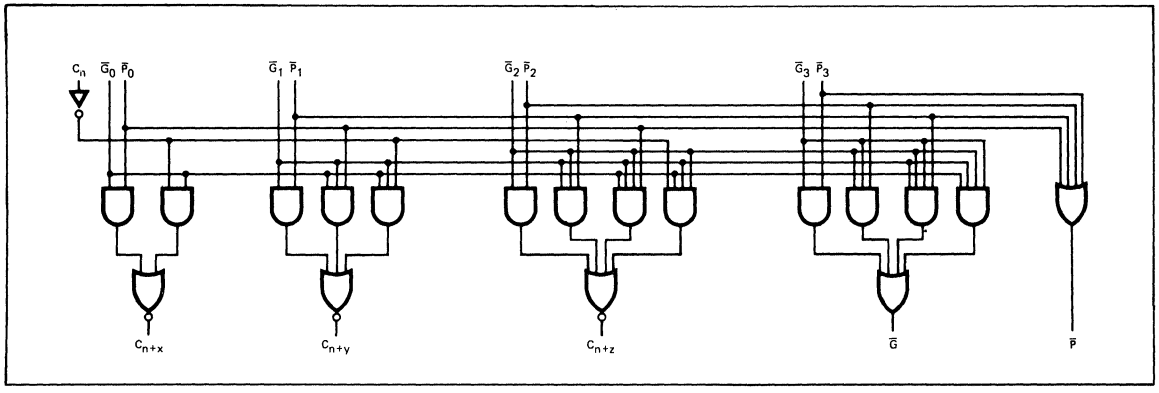
DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries across a group of four Am2901 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 6 ns
- 100% reliability assurance testing in compliance with MIL-STD-883

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2902PC
Hermetic DIP	0°C to +70°C	AM2902DC
Dice	0°C to +70°C	AM2902XC
Hermetic DIP	–55°C to +125°C	AM2902DM
Hermetic Flat Pack	–55°C to +125°C	AM2902FM
Dice	–55°C to +125°C	AM2902XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n			−3.2	mA
			$\overline{P}_3$			−4.8	
			$\overline{P}_2$			−6.4	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8.0	
			$\overline{G}_0, \overline{G}_2$			−14.4	
			$\overline{G}_1$			−16	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	C_n			80	µA
			$\overline{P}_3$			120	
			$\overline{P}_2$			160	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			360	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		62	99	mA
			COM'L		58	94	
		V_{CC} = MAX. All Ouputs HIGH	MIL		37		mA
			COM'L		35		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C, C_L = 15pF, R_L = 400Ω

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t_{PLH}	C_n	C_{n+j}	2	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 0$ V $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{P}_i$	C_{n+j}	3	$\overline{P}_i = 0$ V (j ≥ i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		6.0	8.0	ns
t_{PHL}						6.0	8.0	
t_{PLH}	$\overline{G}_i$	C_{n+j}	3	$\overline{G}_j = 0$ V (j ≥ i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		8.0	10	ns
t_{PHL}						8.0	10	
t_{PLH}	$\overline{P}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{P}_i = 0$ V (j ≥ i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{G}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{G}_i = 0$ V (j ≥ i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		12	14	ns
t_{PHL}						12	14	

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901 microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	L	X	X	L				L	
	X		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

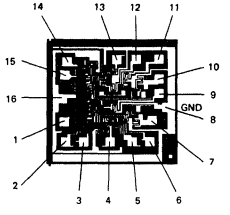
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{G}_1$	1	8.0	–	–
$\overline{P}_1$	2	4.0	–	–
$\overline{G}_0$	3	7.2	–	–
$\overline{P}_0$	4	4.0	–	–
$\overline{G}_3$	5	4.0	–	–
$\overline{P}_3$	6	2.4	–	–
$\overline{P}$	7	–	16	8
GND	8	–	–	–
C_{n+z}	9	–	16	8
$\overline{G}$	10	–	16	8
C_{n+y}	11	–	16	8
C_{n+x}	12	–	16	8
C_n	13	1.6	–	–
$\overline{G}_2$	14	7.2	–	–
$\overline{P}_2$	15	3.2	–	–
V_{CC}	16	–	–	–

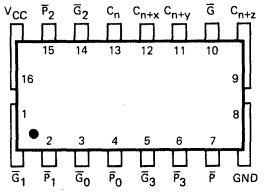
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Metallization and Pad Layout

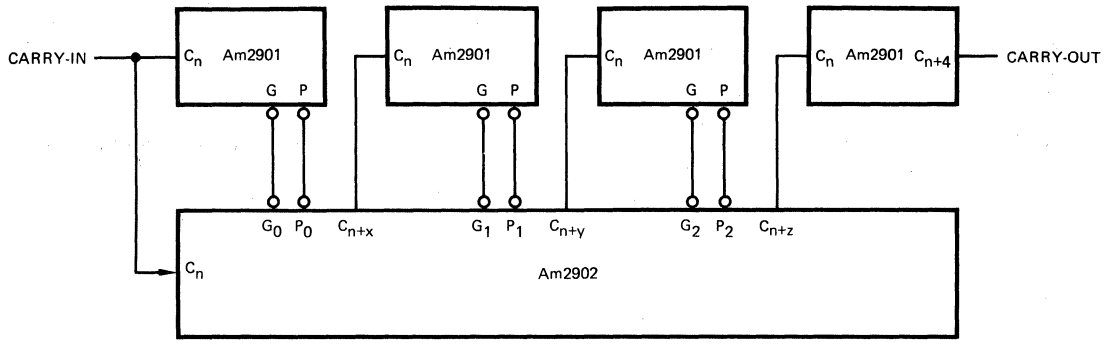
DIE SIZE 0.065" X 0.068"



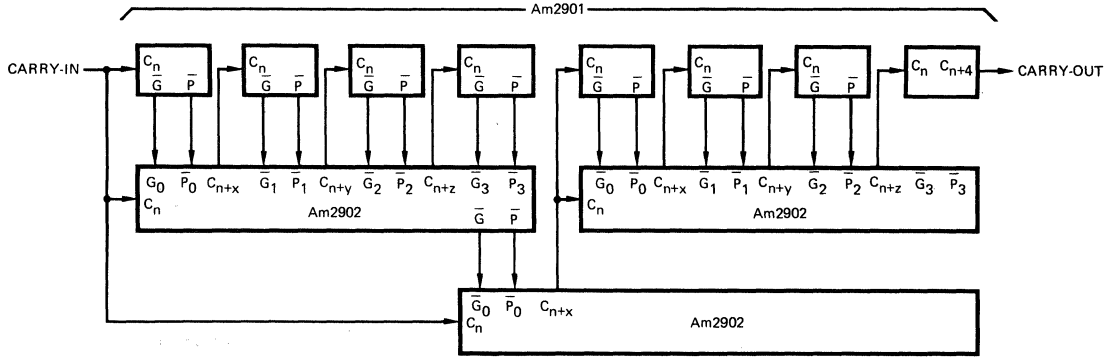
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.



16-BIT CARRY LOOK-AHEAD CONNECTION.



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

FUNCTIONAL DESCRIPTION

The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

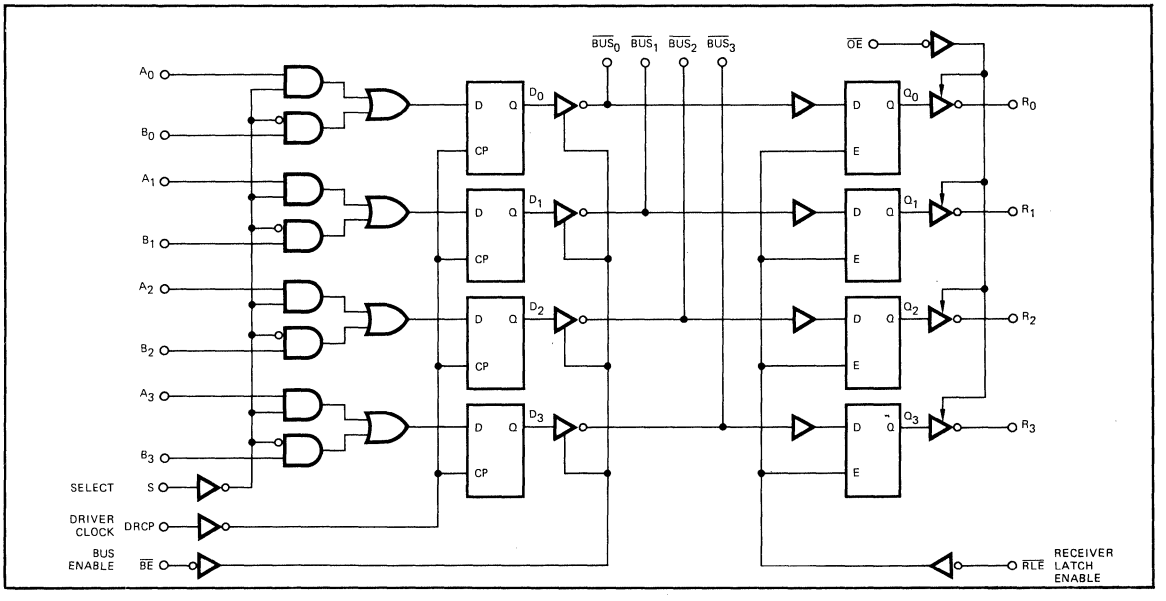
DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2905PC
Hermetic DIP	0°C to +70°C	AM2905DC
Dice	0°C to +70°C	AM2905XC
Hermetic DIP	−55°C to +125°C	AM2905DM
Hermetic Flat Pak	−55°C to +125°C	AM2905FM
Dice	−55°C to +125°C	AM2905XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

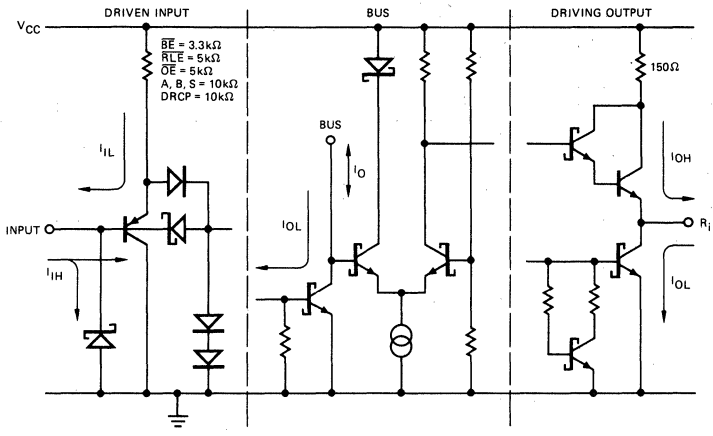
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4$V			20	μA
			$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output	C_L = 5.0 pF, R_L = 2.0 KΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

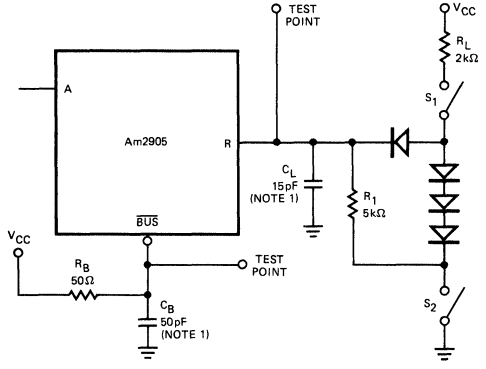
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



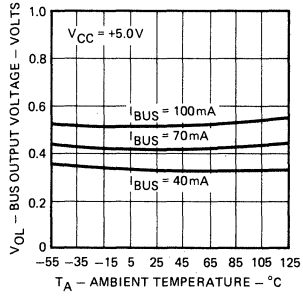
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

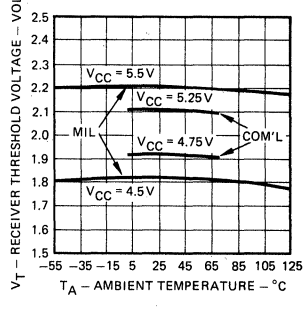
LOAD TEST CIRCUIT



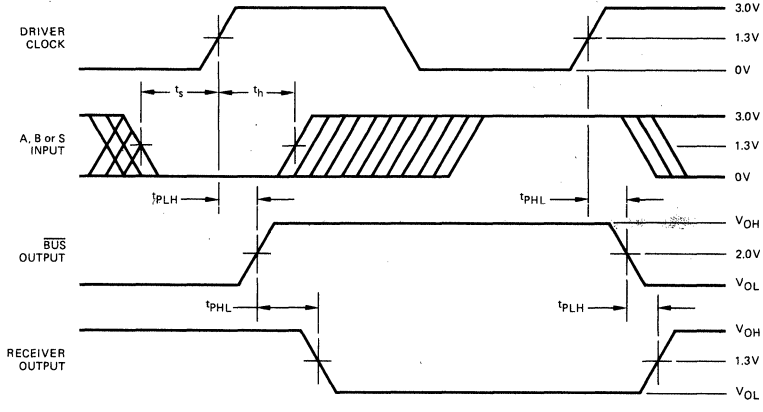
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

RAYTHEON

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW-to-HIGH transition

DEFINITIONS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

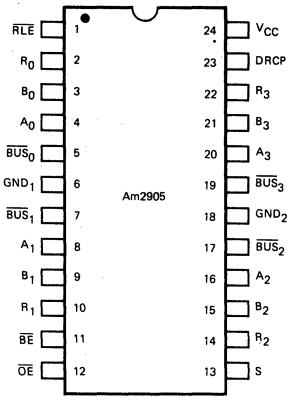
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

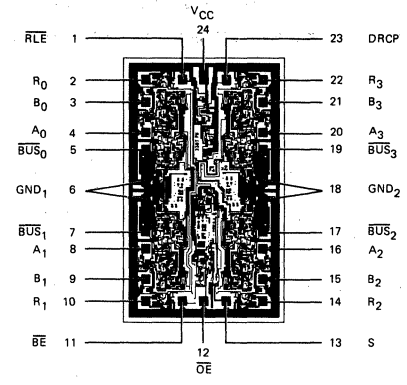
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

CONNECTION DIAGRAM
Top View



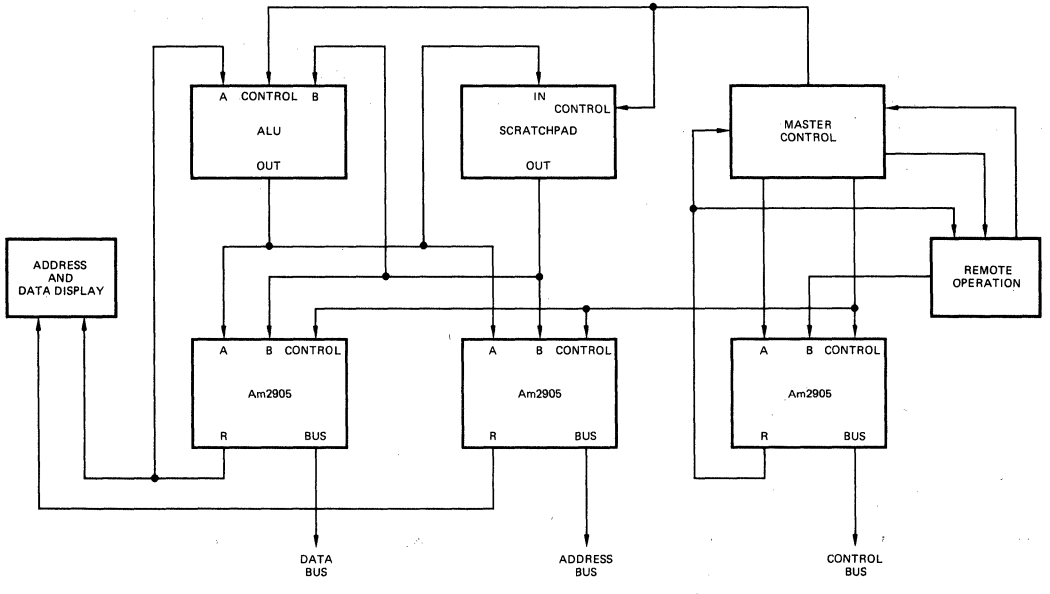
Note: Pin 1 is marked for orientation.

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

RAYTHEON

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

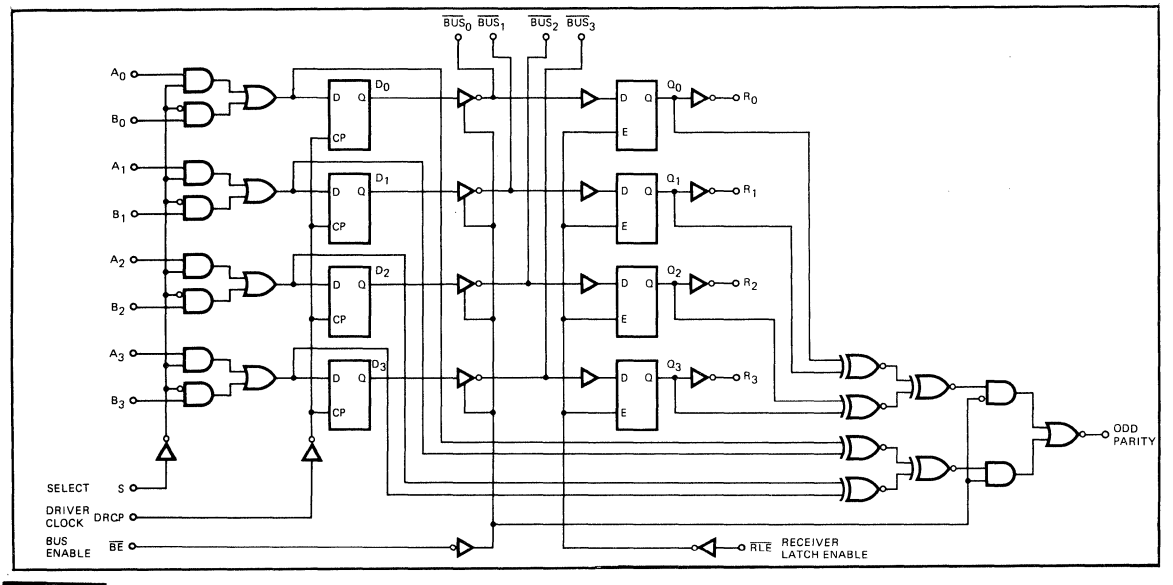
Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2906PC
Hermetic DIP	0°C to +70°C	AM2906DC
Dice	0°C to +70°C	AM2906XC
Hermetic DIP	−55°C to +125°C	AM2906DM
Hermetic Flat Pak	−55°C to +125°C	AM2906FM
Dice	−55°C to +125°C	AM2906XM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

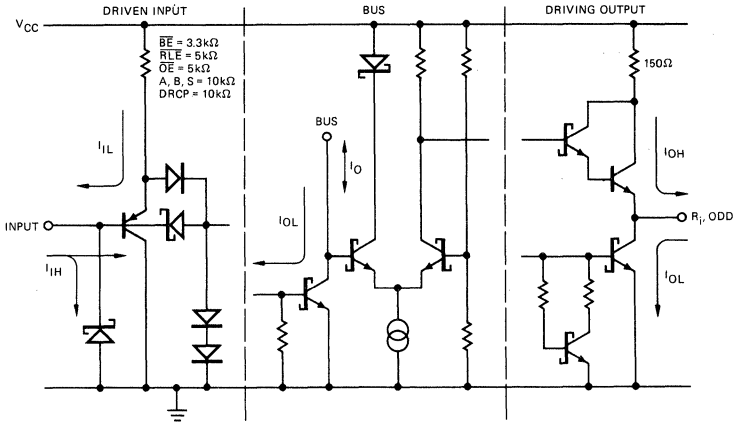
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL		2.5	3.4		
			COM'L		2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.27	0.4	Volts
			$I_{OL} = 8mA$			0.32	0.45	
			$I_{OL} = 12mA$			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL				0.7	Volts
			COM'L				0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	$C_L = 15pF$, $R_L = 2.0k\Omega$	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

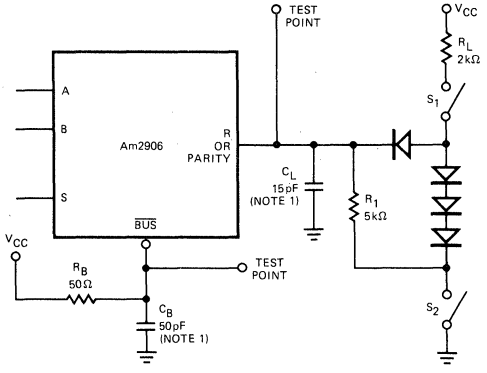
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



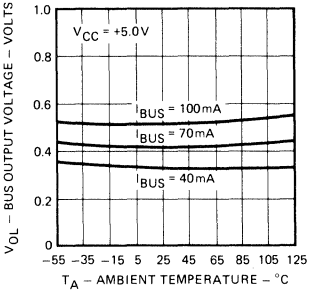
Note: Actual current flow direction shown.

TYPICAL PERFORMANCE CURVES

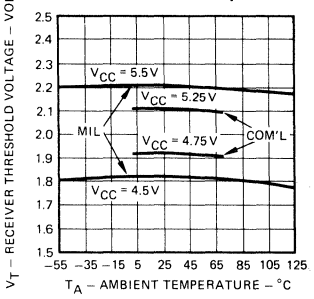
LOAD TEST CIRCUIT



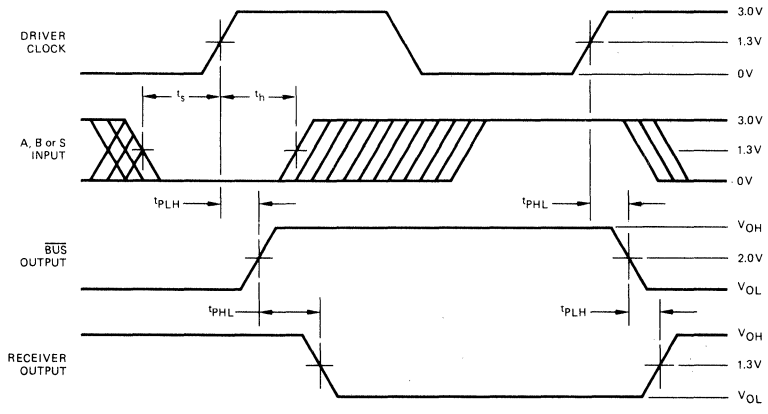
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	Z	X	Driver output disable
X	X	X	X	H	L	X	L	L	H	Driver output disable and receive data
X	X	X	X	H	L	X	H	H	L	via Bus input
X	X	X	X	X	H	X	NC	X	X	Latch received data
L	L	X	↑	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	H	X	X	X	
H	X	L	↑	X	X	L	X	X	X	
H	X	H	↑	X	X	H	X	X	X	
X	X	X	L	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	
X	X	X	X	L	X	L	X	H	X	Drive bus
X	X	X	X	L	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3

L = LOW NC = No change ↑ = LOW-to-HIGH transition

DEFINITIONS

A_0, A_1, A_2, A_3 — The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 — The "B" word data input into the two input multiplexers of the driver register.

S — Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ — The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

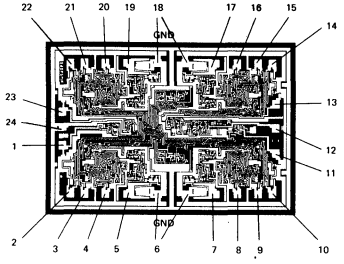
$\overline{RLE}$ — Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD — ODD Parity output. Generates parity with the driver enabled, checks parity with the driver in the HIGH-impedance state.

PARITY OUTPUT FUNCTION TABLE

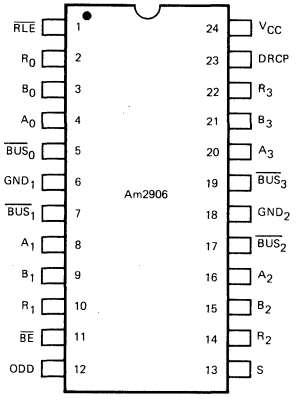
S	$\overline{BE}$	ODD PARITY OUTPUT
L	L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	L	ODD = $B_0 \oplus B_1 \oplus B_2 \oplus B_3$
X	H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

Metallization and Pad Layout

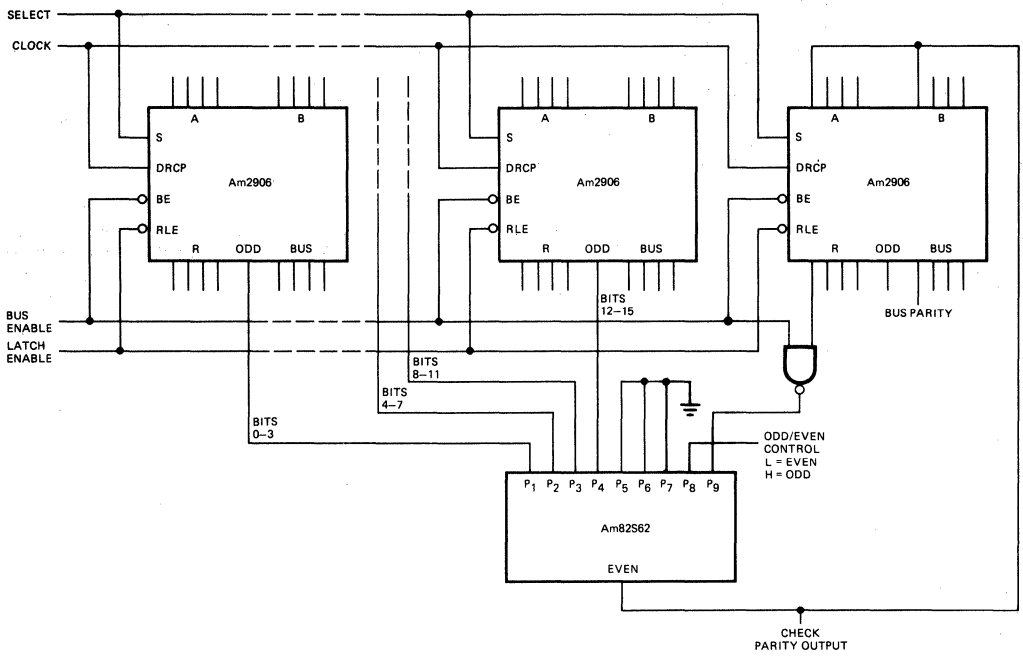


DIE SIZE 0.090" x 0.131"

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.



Generating or checking parity for 16 data bits.

FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input.

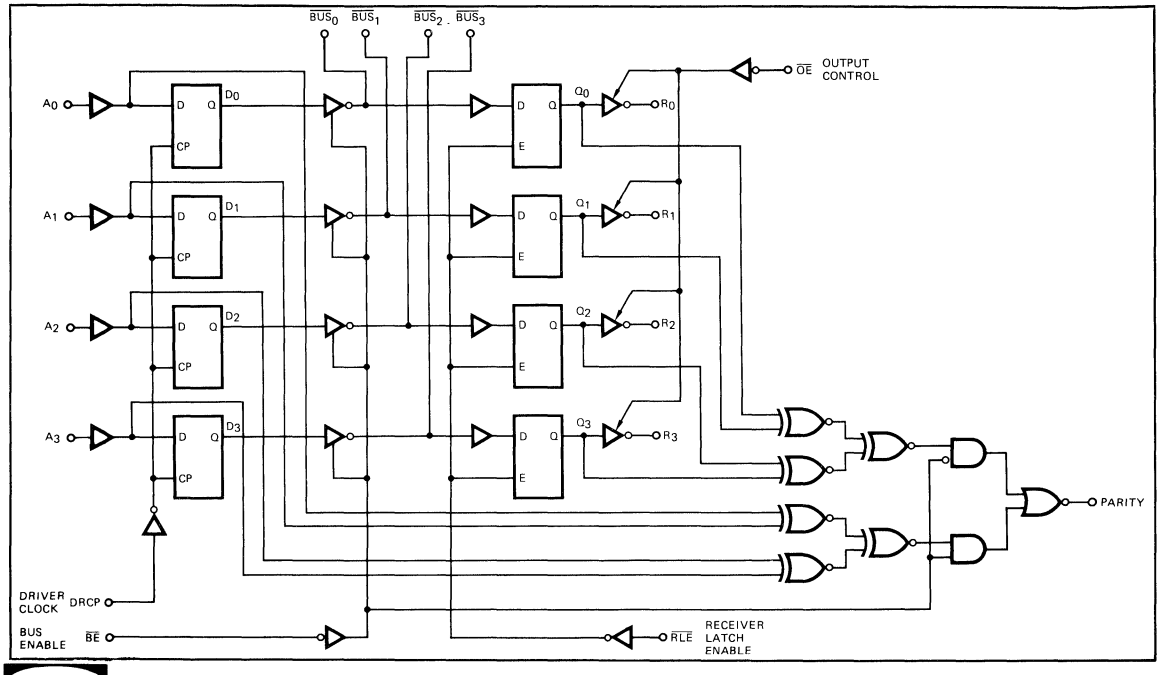
When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2907PC
Hermetic DIP	0°C to +70°C	AM2907DC
Dice	0°C to +70°C	AM2907XC
Hermetic DIP	−55°C to +125°C	AM2907DM
* Hermetic Flat Pak	−55°C to +125°C	AM2907FM
Dice	−55°C to +125°C	AM2907XM

*Available on special order

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2907XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

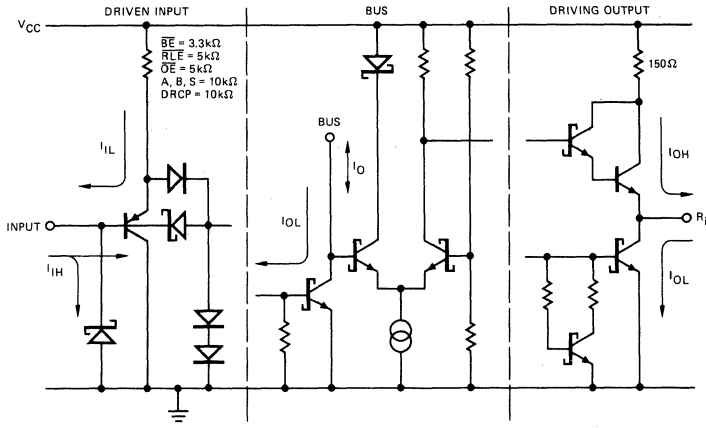
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$	2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$		0.27	0.4	Volts
			$I_{OL} = 8mA$		0.32	0.45	
			$I_{OL} = 12mA$		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$ V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$ V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$ V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$ V			20	μA
			$V_O = 0.4$ V			−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	A Data Inputs	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

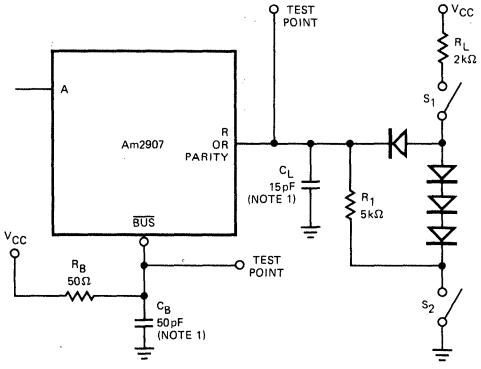
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



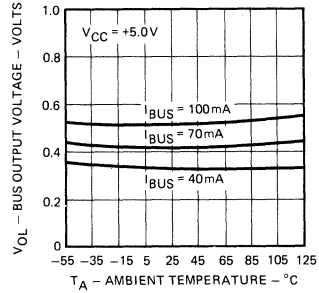
Note: Actual current flow direction shown.

LOAD TEST CIRCUIT

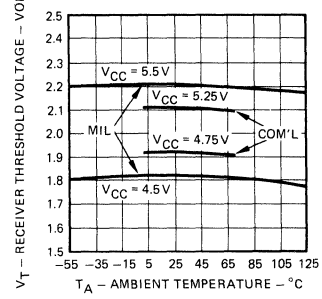


TYPICAL PERFORMANCE CURVES

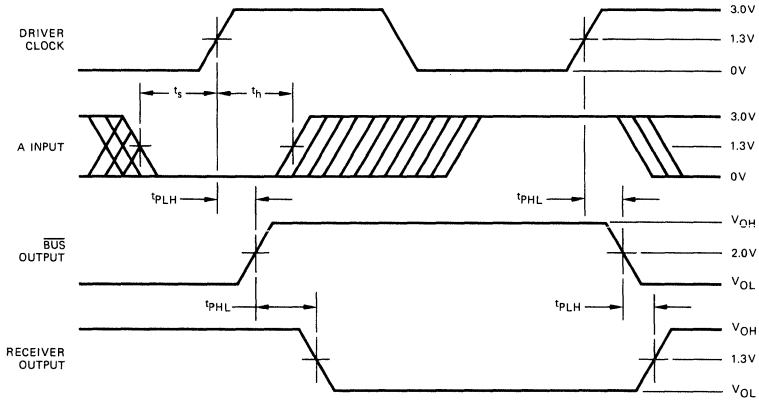
Bus Output Low Voltage Versus Ambient Temperature



Receiver Threshold Variation Versus Ambient Temperature



SWITCHING WAVEFORMS



Note: Bus to Reciever output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

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TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

DEFINITIONS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

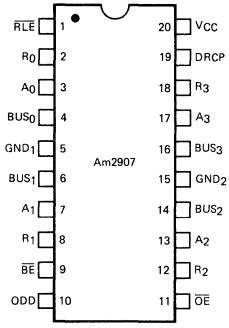
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

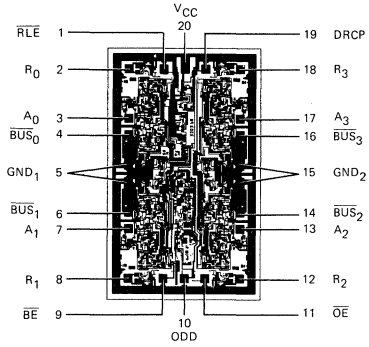
CONNECTION DIAGRAMS
Top Views

DIP



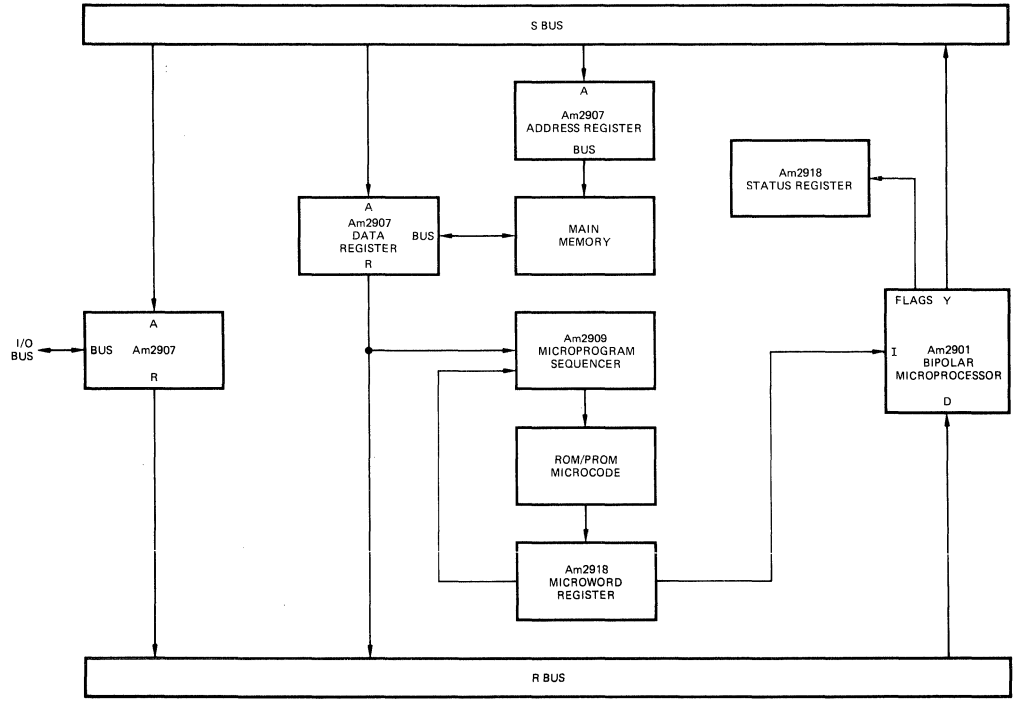
Note: Pin 1 is marked for orientation.

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

RAYTHEON

GENERAL DESCRIPTION

The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package.

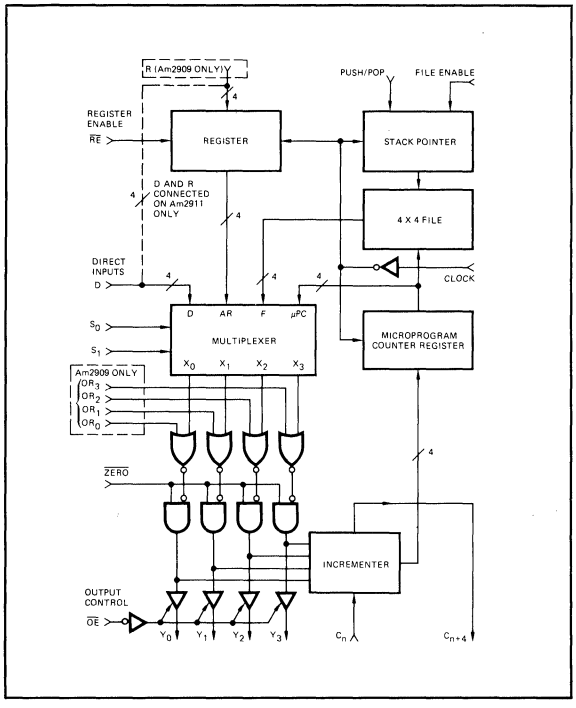
ORDERING INFORMATION

Package Type	Temperature Range	Am2909 Order Number	Am2911 Order Number
Molded DIP	0°C to +70°C	AM2909PC	AM2911PC
Hermetic DIP	0°C to +70°C	AM2909DC	AM2911DC
Hermetic DIP	−55°C to +125°C	AM2909DM	AM2911DM
Hermetic Flat Pak	−55°C to +125°C	Am2909FM	–
Dice	0°C to +70°C	Am2909XC	–

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines.
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only).
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2909/2911DC, PC	0°C to +70°C	4.75 V to 5.25 V
Am2909/2911DM, FM	−55°C to +125°C	4.50 V to 5.50 V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Am2909/Am2911DM,FM
Pre-Seal Visual Inspection	2010	B	100%
Stabilization Bake	1008	C 24-hour 150°C	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%
Centrifuge	2001	B 10,000 G	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100%
Gross Leak	1014	C2 Fluorocarbon	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%
Insert Additional Screening here for Class B Parts			
Group A Sample Tests			
Subgroup 1			LTPD = 5
Subgroup 2			LTPD = 7
Subgroup 3		See below for	LTPD = 7
Subgroup 7	5005	definitions of subgroups	LTPD = 7
Subgroup 8			LTPD = 7
Subgroup 9			LTPD = 7

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level Am2909/Am2911DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA (Note 5)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)				80	130	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	μA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

All parameters are guaranteed worst case over the operating voltage and temperature range for the device type. (Grade C = 0°C to +70°C, 4.75V to 5.25V; Grade M = −55°C to +125°C, 4.5V to 5.5V)

TABLE I
MINIMUM CLOCK REQUIREMENTS

Minimum Clock LOW Time	50
Minimum Clock HIGH Time	30

TABLE II
MAXIMUM COMBINATORIAL PROPAGATION DELAYS

OUTPUTS / INPUTS	Y_i	C_{n+4}
$\overline{OE}$	25	–
$\overline{ZERO}$	35	45
OR_i	20	32
S_0, S_1	40	50
D_i	20	32
C_n	–	18

TABLE III
MAXIMUM DELAYS FROM CLOCK TO OUTPUTS

FUNCTIONAL PATH	GRADE	CLOCK TO Y_i	CLOCK TO C_{n+4}
Register (S_1 S_0 = LH)	C	48	58
	M	55	65
μ Program Counter (S_1 S_0 = LL)	C	48	58
	M	55	65
File (S_1 S_0 = HL)	C	70	80
	M	80	90

R_L = 2.0kΩ C_L = 15pF

TABLE IV
SET-UP AND HOLD TIME REQUIREMENTS

EXTERNAL INPUTS	t_s	t_h
$\overline{RE}$	20	5.0
R_i	15	0
PUSH/POP	20	5.0
$\overline{FE}$	20	0
C_n	15	0
D_i	20	0
OR_i	20	0
S_0, S_1	40	0
$\overline{ZERO}$	40	0

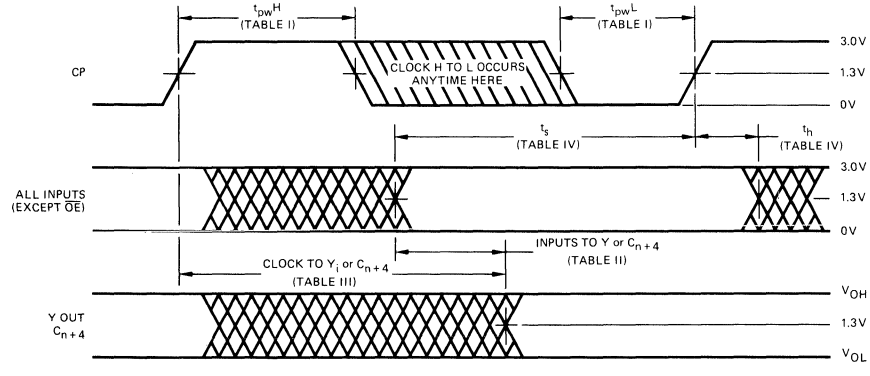


Figure 1. Switching Waveforms. See Tables for Specific Values.

DEFINITIONS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

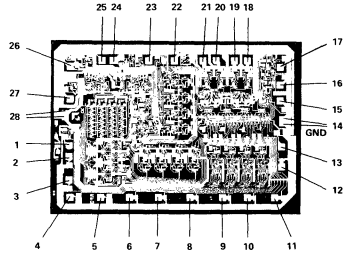
μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

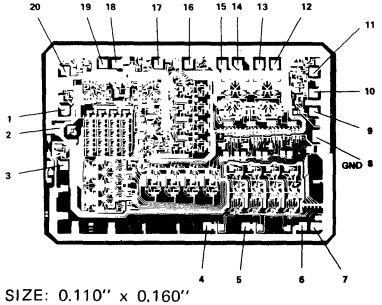
METALLIZATION AND PAD LAYOUT

Am2909



DIE SIZE: 0.110" x 0.160"

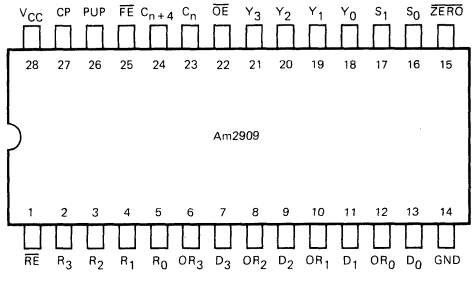
Am2911

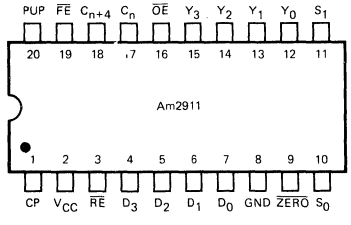


DIE SIZE: 0.110" x 0.160"

CONNECTION DIAGRAMS

Top Views





Note: Pin 1 is marked for orientation.

Figure 2.

ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 4.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

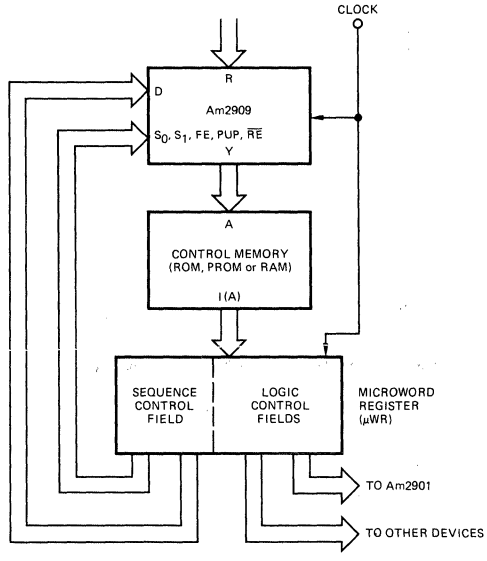
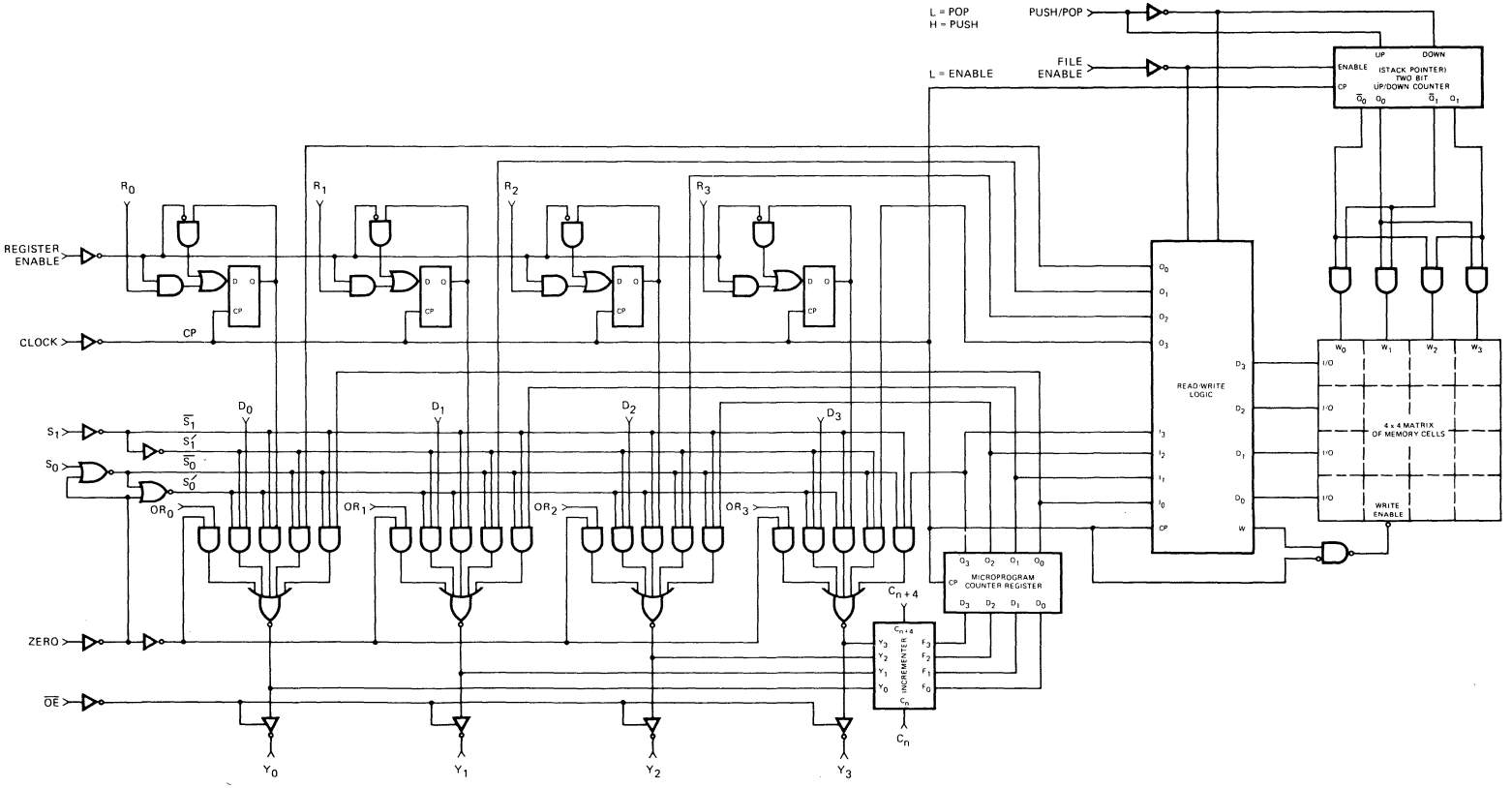


Figure 3. Microprogram Sequencer Control.



Note: R_i and D_i connected together on Am2911 and OR_i removed.

Figure 4. Microprogram Sequencer Block Diagram.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push μPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STKO is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

FUNCTIONAL DESCRIPTION

The Am2915 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

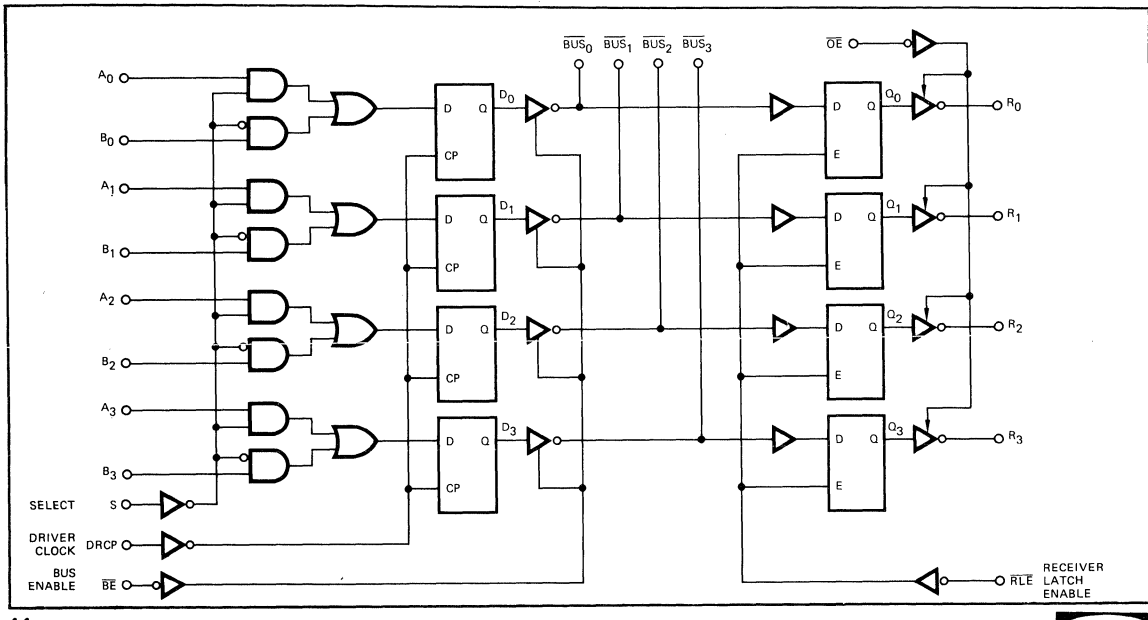
DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2915PC
Hermetic DIP	0°C to +70°C	AM2915DC
Dice	0°C to +70°C	AM2915XC
Hermetic DIP	−55°C to +125°C	AM2915DM
Hermetic Flat Pak	−55°C to +125°C	AM2915FM
Dice	−55°C to +125°C	AM2915XM

LOGIC DIAGRAM



RAYTHEON

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915XC(COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

Am2915XM(MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 40mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915XC(COM'L) $T_A = 0°C$ to $+70°C$ V_{CC}MIN. = 4.75 V V_{CC}MAX. = 5.25 V

Am2915XM(MIL) $T_A = -55°C$ to $+125°C$ V_{CC}MIN. = 4.50 V V_{CC}MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			60	90	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

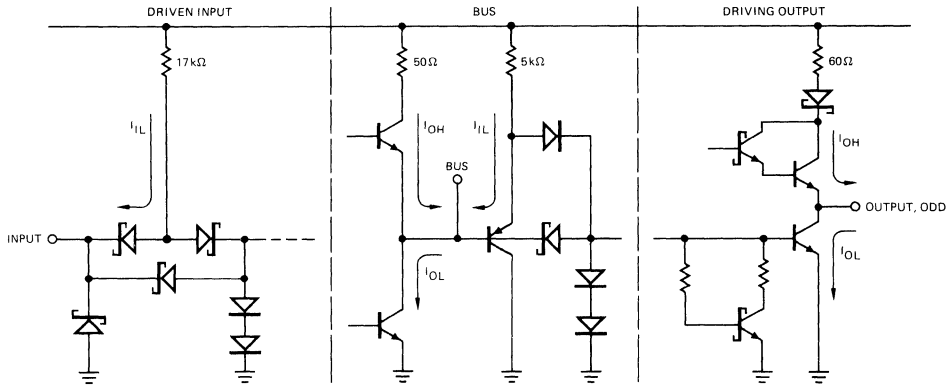
Parameters	Description	Test Conditions	Am2915XM Min.	Am2915XM Typ. (Note 2)	Am2915XM Max.	Am2915XC Min.	Am2915XC Typ. (Note 2)	Am2915XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	Data Inputs (A or B)		23			20			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)	C_L = 15 pF, R_L = 2.0 kΩ		18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		17			14			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output			14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

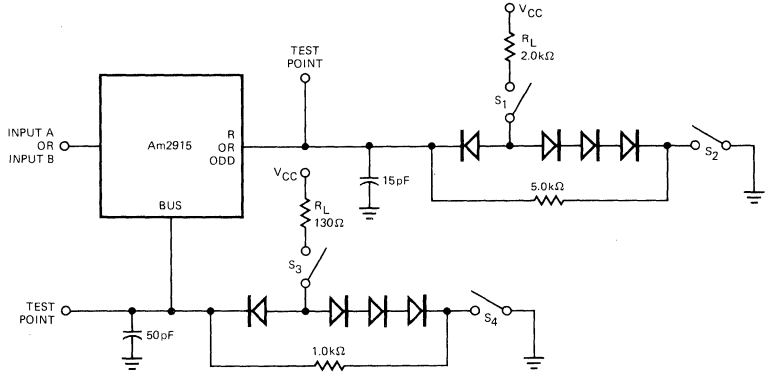
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

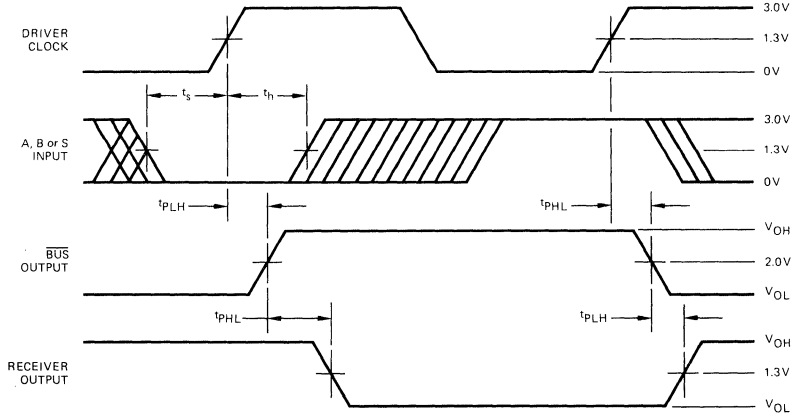


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Reciver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

DEFINITIONS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

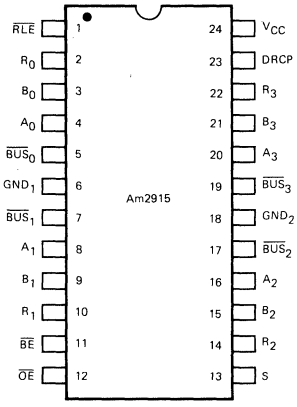
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

CONNECTION DIAGRAM
Top View

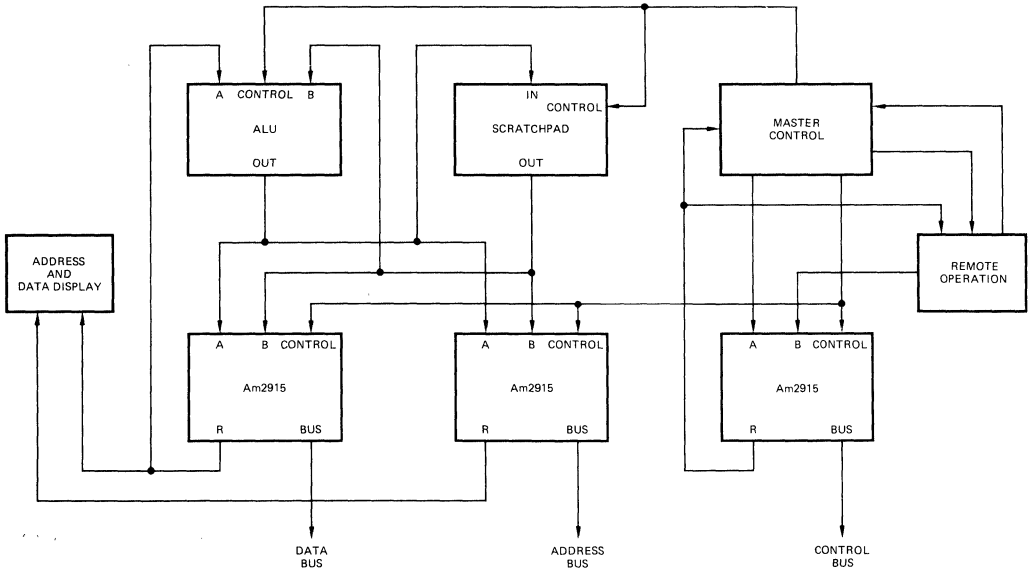


Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

(NOT AVAILABLE AT THE TIME OF THIS PRINTING.)

APPLICATIONS



The Am2915 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

FUNCTIONAL DESCRIPTION

The Am2916 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

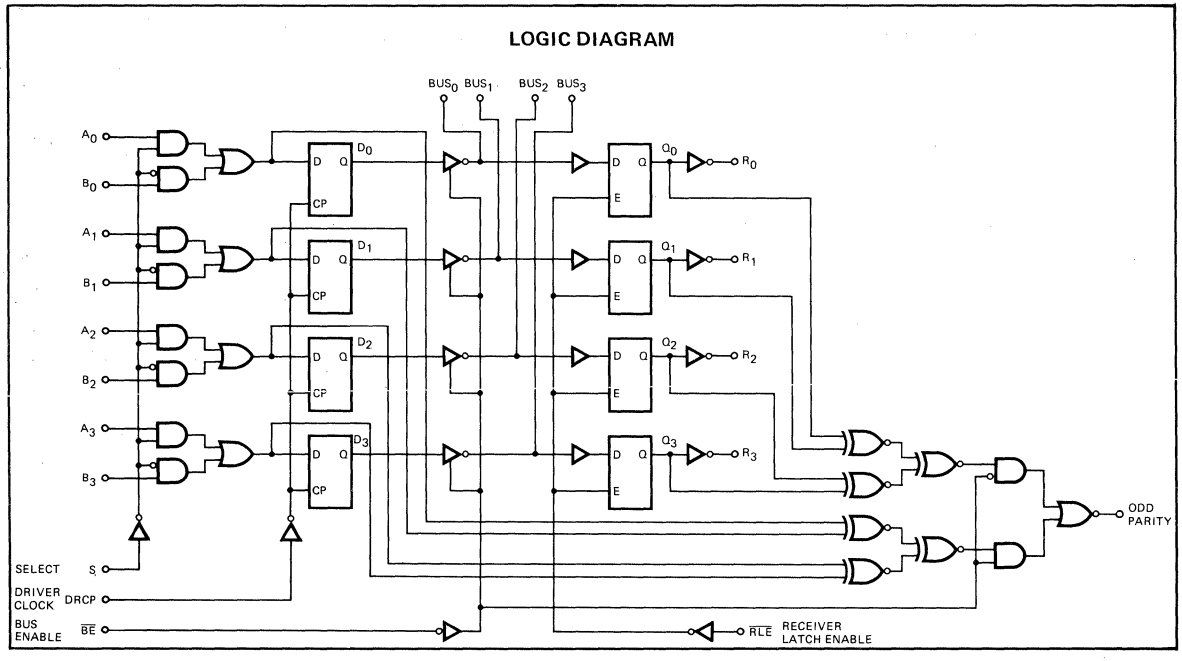
Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

LOGIC DIAGRAM



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ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2916PC
Hermetic DIP	0°C to +70°C	AM2916DC
Dice	0°C to +70°C	AM2916XC
Hermetic DIP	−55°C to +125°C	AM2916DM
Hermetic Flat Pak	−55°C to +125°C	AM2916FM
Dice	−55°C to +125°C	AM2916XM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916XC(COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

Am2916XM(MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 40mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V

Am2916XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

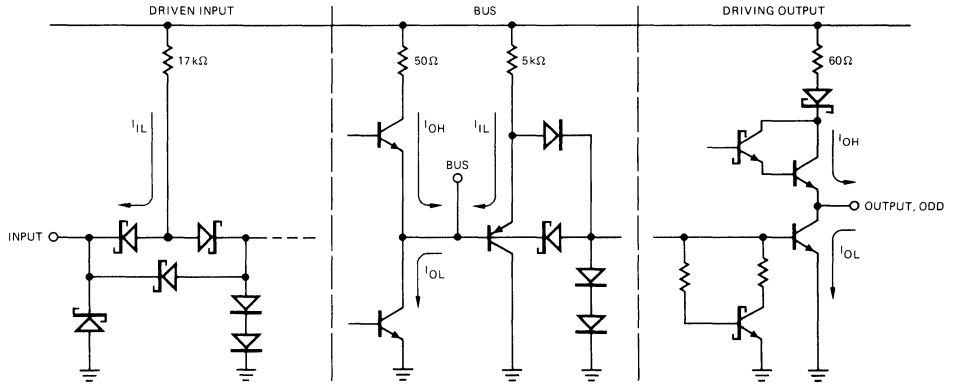
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		$V_{CC} = 5.0$V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0$mA		0.27	0.4	Volts
			$I_{OL} = 8.0$mA		0.32	0.45	
			$I_{OL} = 12$mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0$V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	Am2916XM Min.	Am2916XM Typ. (Note 2)	Am2916XM Max.	Am2916XC Min.	Am2916XC Typ. (Note 2)	Am2916XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	Data Inputs (A or B)		23			20			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		17			14			ns
t_h		$C_L = 15$pF, $R_L = 2.0$kΩ	6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

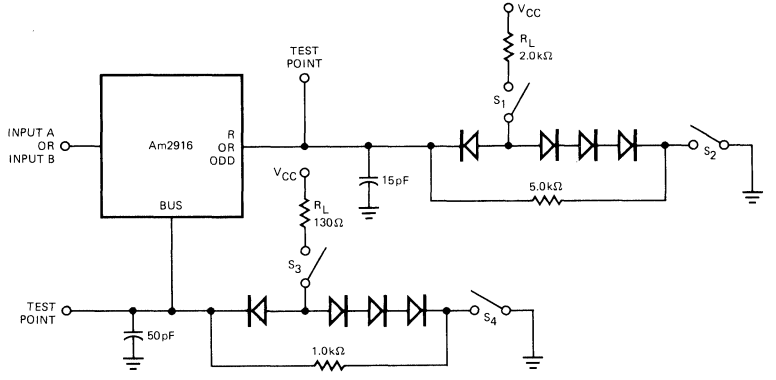
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

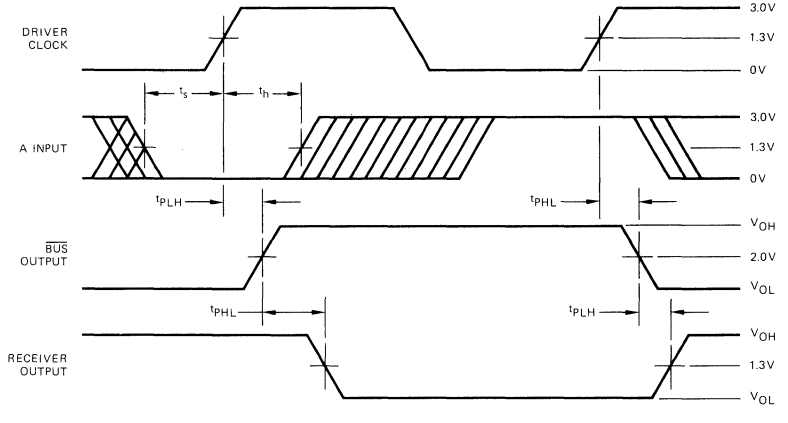


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH
L = LOW
Z = HIGH Impedance
NC = No change
X = Don't care
↑ = LOW-to-HIGH transition
i = 0, 1, 2, 3

DEFINITIONS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

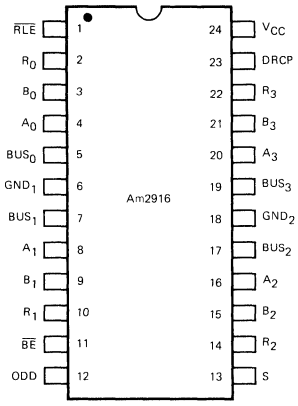
$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

CONNECTION DIAGRAM
Top View

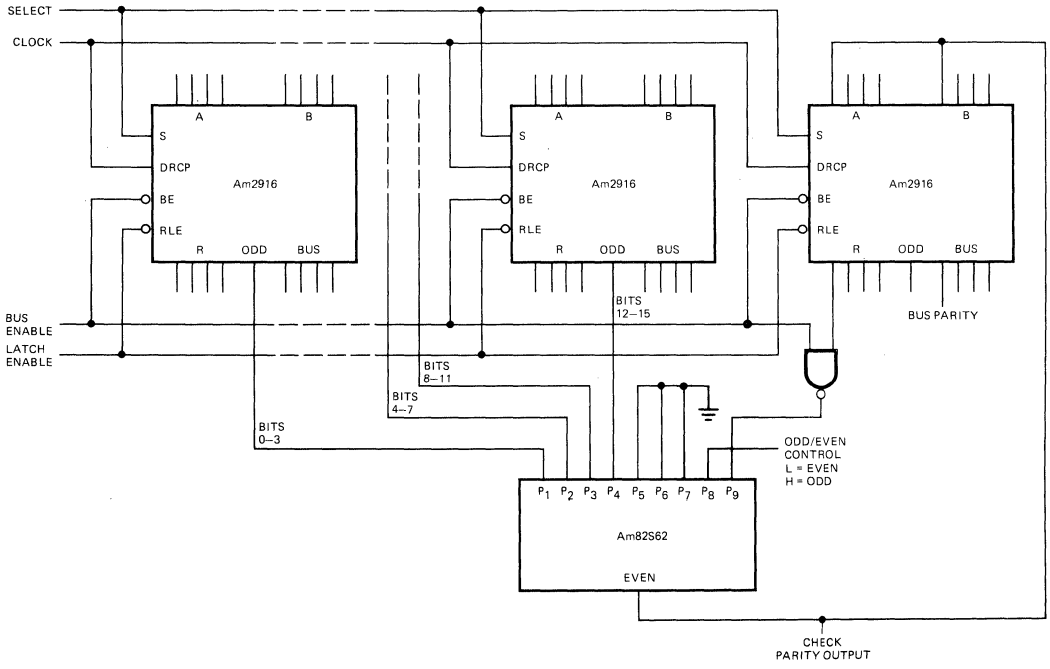


Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

(NOT AVAILABLE AT THE TIME OF THIS PRINTING.)

APPLICATIONS



Generating or checking parity for 16 data bits.

FUNCTIONAL DESCRIPTION

The Am2917 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

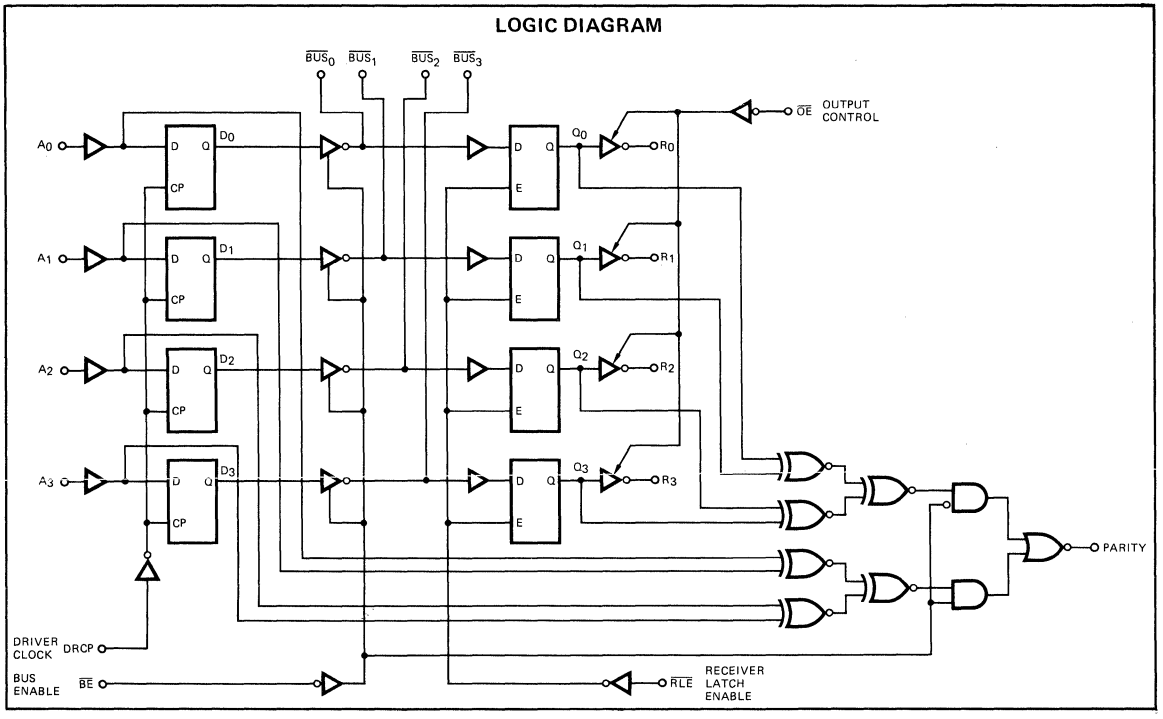
The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 40mA at 0.5V max
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

LOGIC DIAGRAM



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ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2917PC
Hermetic DIP	0°C to +70°C	AM2917DC
Dice	0°C to +70°C	AM2917XC
Hermetic DIP	−55°C to +125°C	AM2917DM
*Hermetic Flat Pak	−55°C to +125°C	AM2917FM
Dice	−55°C to +125°C	AM2917XM

*Available on special order.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V

Am2917XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 40 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −20 mA	2.4			Volts
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V, V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V				0.8	Volts
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0 V		−50	−85	−130	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V

Am2917XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

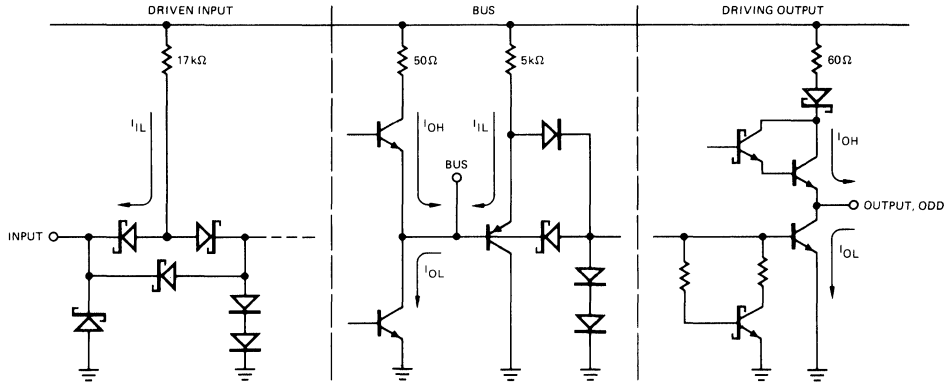
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917XM Min.	Am2917XM Typ. (Note 2)	Am2917XM Max.	Am2917XC Min.	Am2917XC Typ. (Note 2)	Am2917XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus	C_L = 15 pF, R_L = 2.0 kΩ		13	26		13	23	ns
t_{HZ}, t_{LZ}				13	26		13	23	
t_s	A Data Inputs		23			20			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	30		18	27	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	30		21	27	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		17			14			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

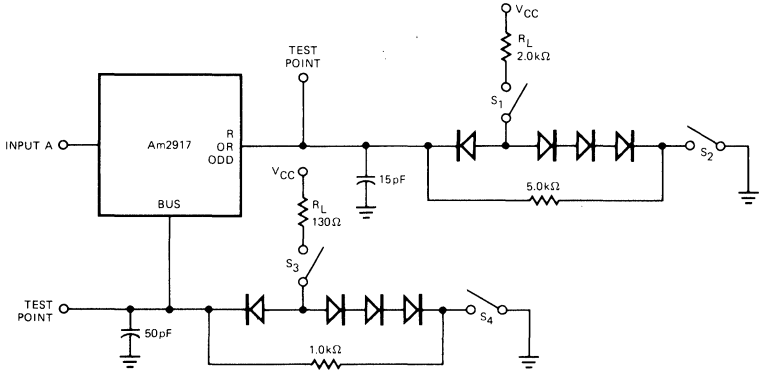
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

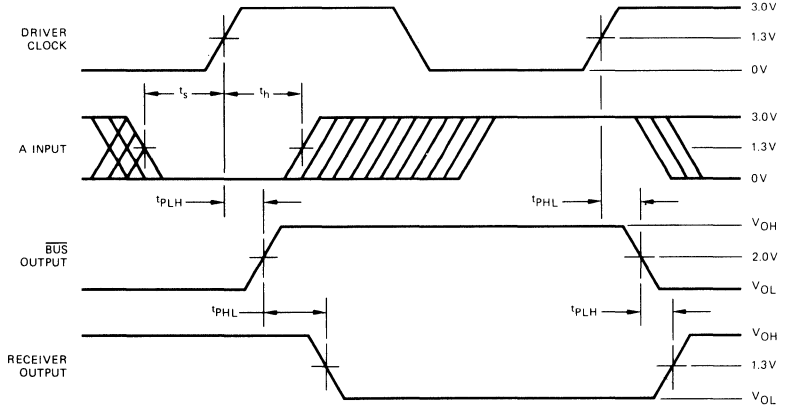


Note: Actual current flow direction shown.

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITIONS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

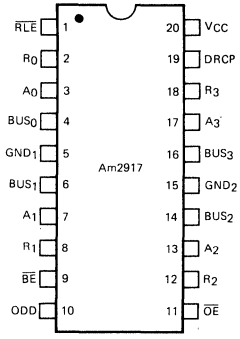
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

CONNECTION DIAGRAM
Top View

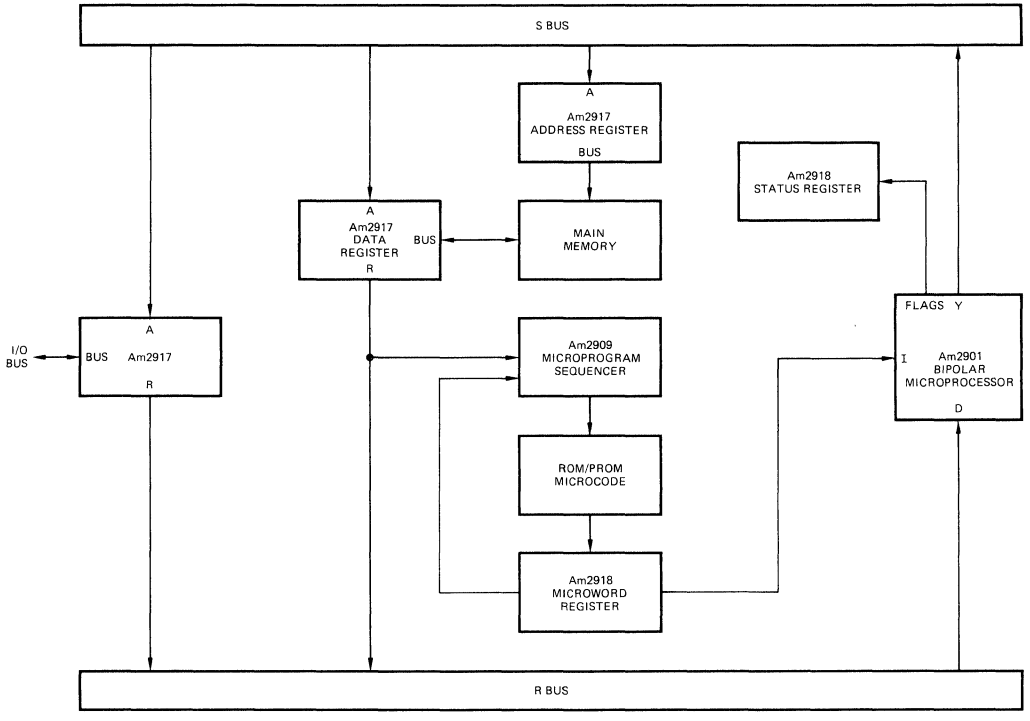


Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

(NOT AVAILABLE AT THE TIME OF THIS PRINTING.)

APPLICATIONS



The Am2917 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration — especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

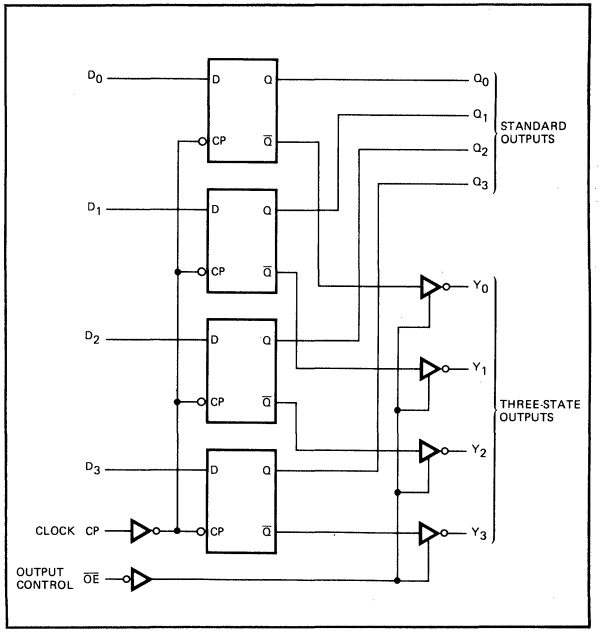
DISTINCTIVE CHARACTERISTICS

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2918PC
Hermetic DIP	0°C to +70°C	AM2918DC
Dice	0°C to +70°C	AM2918XC
Hermetic DIP	−55°C to +125°C	AM2918DM
Hermetic Flat Pack	−55°C to +125°C	AM2918FM
Dice	−55°C to +125°C	AM2918XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2918XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	120	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output	C_L = 15pF		6.0	9.0	ns
t_{PHL}				8.5	13	
t_{pw}	Clock Pulse Width		7.0			ns
t_s	Data		5.0			ns
t_h	Data		3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)			6.0	9.0	ns
t_{PHL}				8.5	13	
t_{ZH}	Output Control to Output	C_L = 5pF		12.5	19	ns
t_{ZL}				12	18	
t_{HZ}		C_L = 50pF		4.0	6.0	
t_{LZ}				7.0	10.5	
f_{max}	Maximum Clock Frequency	C_L = 15pF	75	100		MHz

DEFINITIONS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

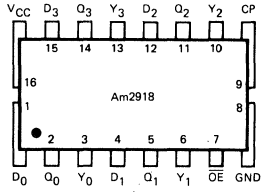
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

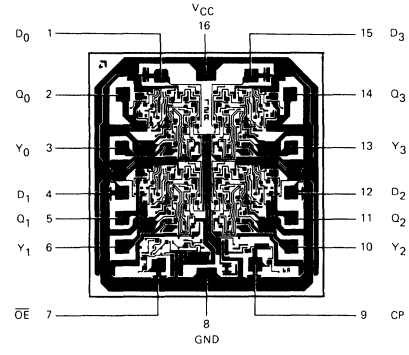
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

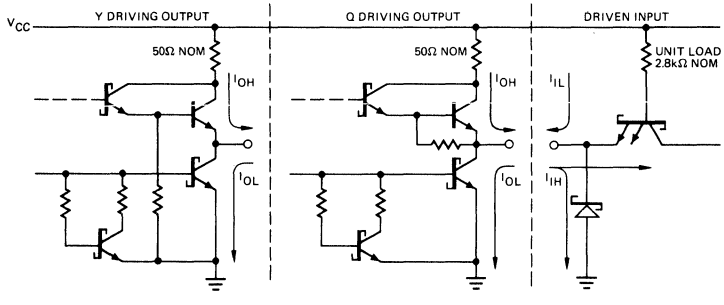
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



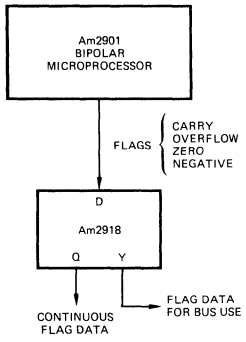
DIE SIZE: 0.067" x 0.090"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

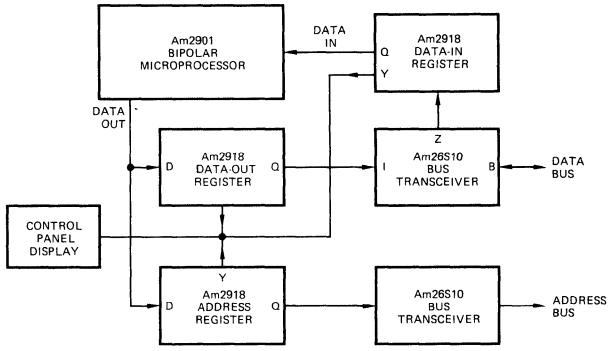


Note: Actual current flow direction shown.

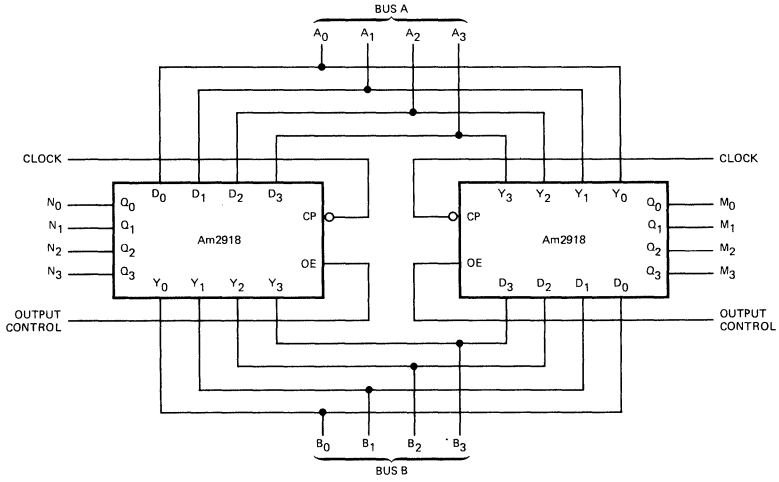
RAYTHEON



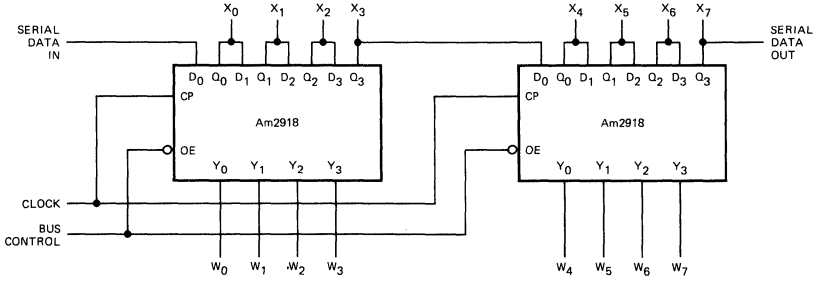
The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.



The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.



8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

DESCRIPTION

The 93411 and 93411A are high speed 256-bit TTL random access memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

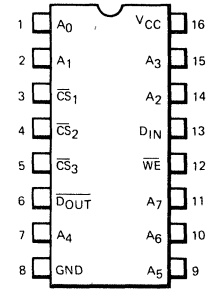
DISTINCTIVE CHARACTERISTICS

- Replacement for 54/74S206 and equivalent devices
- Organization – 256 words by one bit
- Three high speed chip select inputs
- Typical access time

93411A	Commercial	40nsec
93411	Commercial	45nsec
93411	Military	45nsec

- On chip decoding
- Power dissipation – 1.2mW/bit
- Power dissipation decreases with temperature
- Inverted data output

CONNECTION DIAGRAM



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$
$A_0 - A_7$
D_{IN}
$\overline{D}_{OUT}$
$\overline{WE}$

	LOADING (Notes a, b)
Chip Select Inputs	0.5 U.L.
Address Inputs	0.5 U.L.
Data Input	0.5 U.L.
Data Output	10 U.L.
Write Enable	0.5 U.L.

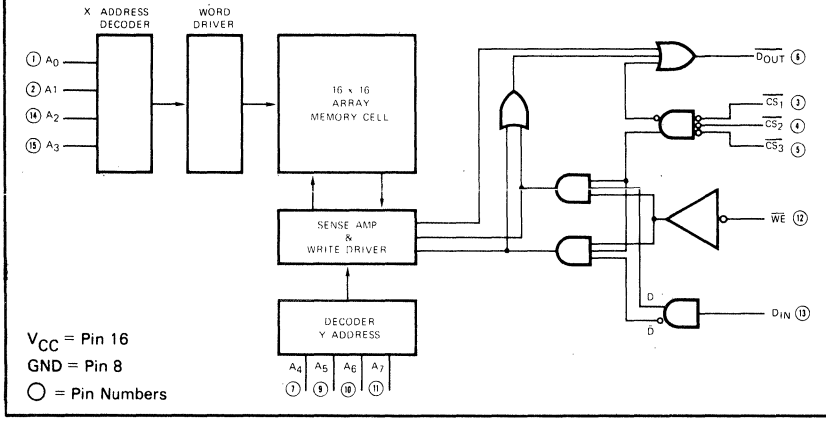
ORDERING INFORMATION

ORDER CODE	PACKAGE	TEMPERATURE*
45 ns Typical Access Time		
93411DC	Ceramic DIP**	Commercial
93411DM	Ceramic DIP**	Military
93411PC	Plastic DIP	Commercial
93411FM	Flatpak	Military
40 ns Typical Access Time		
93411ADC	Ceramic DIP**	Commercial

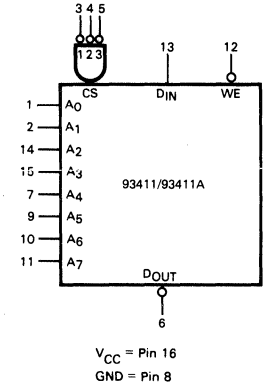
*Commercial = 0°c to +75°C
Military = -55°C to +125°C
**Available in both ceramic DIP package options.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW
b. 10 U.L. is the output LOW drive factor. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V.

LOGIC DIAGRAM



LOGIC SYMBOL



RAYTHEON

FUNCTIONAL DESCRIPTION

The 93411/93411A are fully decoded 256-bit random access memories organized 256 words by one bit. Word selection is achieved by means of an eight-bit address, A_0 thru A_7.

Three chip select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93411's or 93411A's can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\ (MAX)}{16 - F.O.\ (1.6)} \leqslant R_L \leqslant \frac{V_{CC}\ (MIN) - V_{OH}}{n\ (I_{CEX}) + F.O.\ (0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}_1$ PIN 3	$\overline{CS}_2$ PIN 4	$\overline{CS}_3$ PIN 5	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	MODE
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	H	X	X	H	Not Selected
L	L	L	L	L	H	Write "0"
L	L	L	L	H	H	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93411AXC, 93411XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93411XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
I_{CEX}	Output Leakage Current			1.0	50	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93411XC		90	124	mA	T_A = +75°C	V_{CC} = MAX, $\overline{WE}$ Grounded, all other inputs @ 4.5 V
		93411AXC		100	135		T_A = 0°C	
		93411XM		90	117		T_A = +125°C	
				100	143		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93411AXC MIN	93411AXC TYP (Note 3)	93411AXC MAX	93411XC MIN	93411XC TYP (Note 3)	93411XC MAX	93411XM MIN	93411XM TYP (Note 3)	93411XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		25	30		25	30		25	40		See Test Circuit
t_{RCS}	Chip Select Recovery Time		25	25		25	25		25	35	ns	and Waveforms
t_{AA}	Address Access Time		40	45		45	55		45	65		Note 5
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time	10	20	35	10	20	35	10	20	45		
t_{WR}	Write Recovery Time		25	40		25	40		25	50	ns	
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	40	25		40	25		50	25			See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	0	0		0	0		0	0			Note 6
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	0	0		0	0		0	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0		0	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Lead Capacitance		4	5		4	5		4	5	pF	Measured with
C_O	Output Lead Capacitance		7	8		7	8		7	8		pulse technique

NOTES:

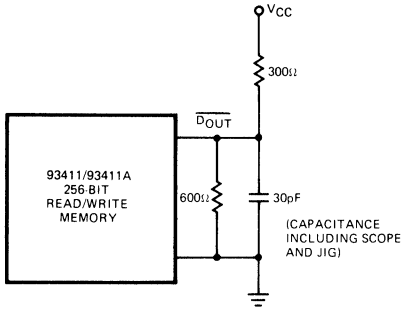
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C / Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C / Watt, Ceramic DIP; 110°C / Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C / Watt, Ceramic DIP; 25°C / Watt, Plastic DIP; 10°C/Watt, Flatpak.

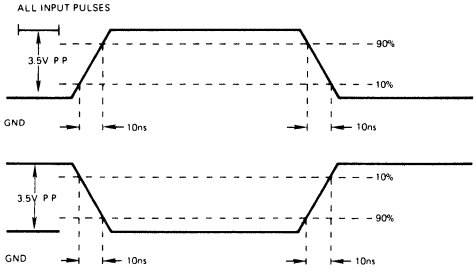
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



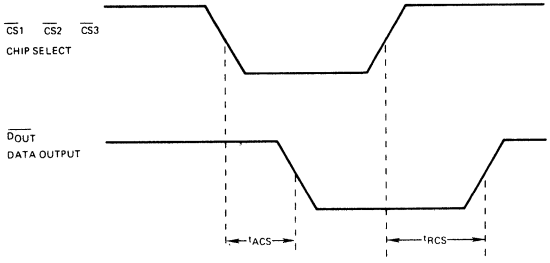
INPUT PULSES



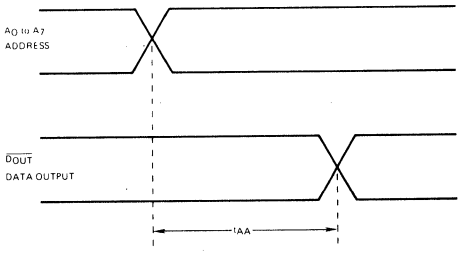
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

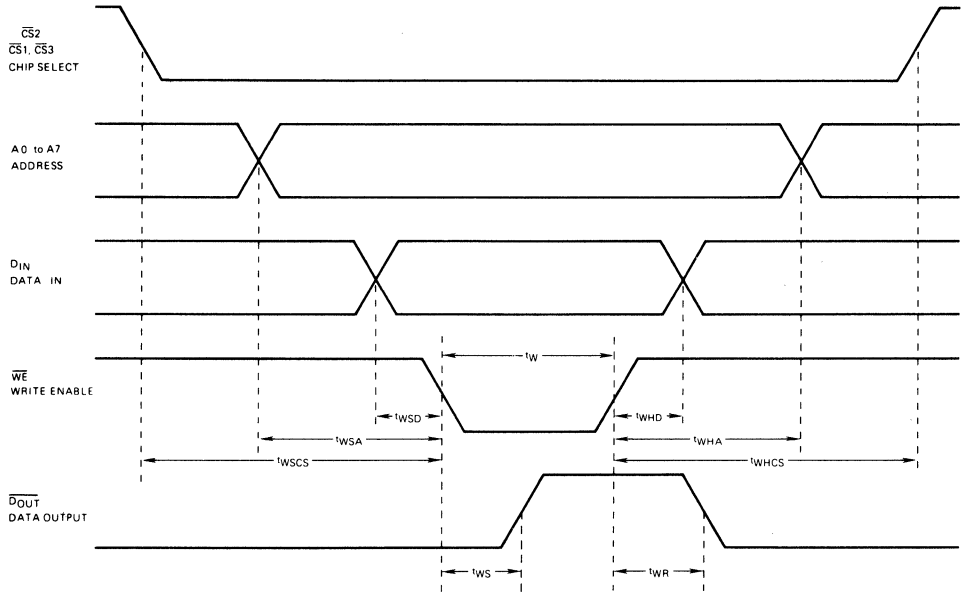


PROPAGATION DELAY FROM ADDRESS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE MODE



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

DESCRIPTION

The 93415 and 93415A are 1024-bit read/write random access memories organized 1024 words by one bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical access times of 40nsec for the 93415 and 30nsec for the 93415A.

The 93415 and 93415A include full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select. They are fully compatible with standard DTL and TTL logic families and have an uncommitted collector output for ease of memory expansion.

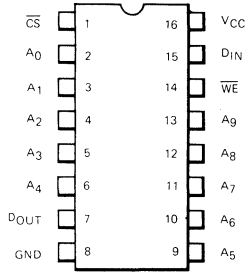
DISTINCTIVE CHARACTERISTICS

- Uncommitted collector output
- TTL inputs and output
- Non-inverting data output
- Organized 1024 words by one bit
- Typical read access time

93415A	Commercial	30nsec
93415	Commercial	40nsec
93415	Military	40nsec

- Chip select access time 15nsec typical
- Power dissipation 0.5mW/bit typical
- Power dissipation decreases with increasing temperature

CONNECTION DIAGRAM



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

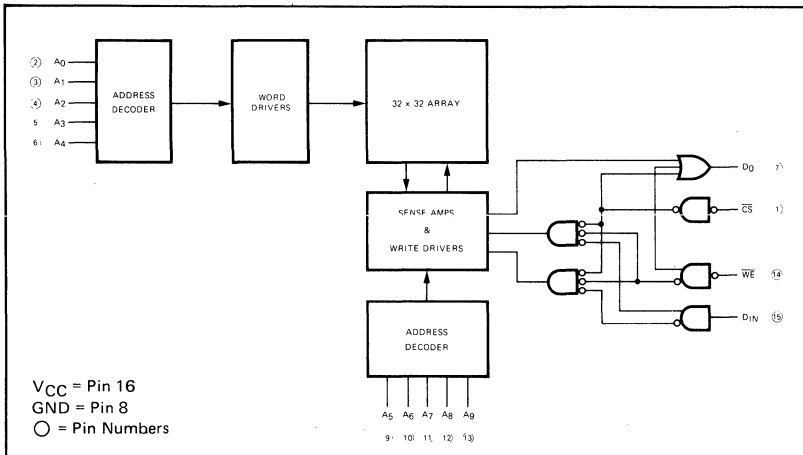
$\overline{CS}$	Chip Select
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

ORDERING INFORMATION

ORDER CODE	PACKAGE	TEMPERATURE *
40 ns Typical Access Time		
93415DC	**Ceramic DIP**	**Commercial**
93415DM	**Ceramic DIP**	**Military**
93415PC	**Plastic DIP**	**Commercial**
93415FM	**Flatpak**	**Military**
30 ns Typical Access Time		
93415ADC	**Ceramic DIP**	**Commercial**
93415APC	**Plastic DIP**	**Commercial**

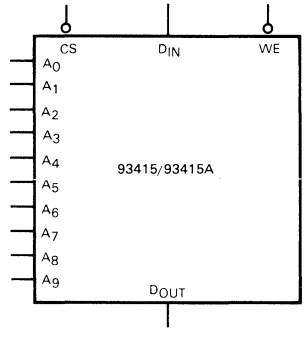
*Commercial = 0°C to +75°C
Military = -55°C to +125°C

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

RAYTHEON

FUNCTIONAL DESCRIPTION

The 93415/93415A are fully decoded 1024-bit random access memories organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 to A_9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable (WE, Pin 14). With WE held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and in non-inverted.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415's or 93415A's can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC(MIN)}}{I_{OL} - FO(1.6)} \leqslant R_L \leqslant \frac{V_{CC(MIN)} - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One unit load = 40μA HIGH/1.6mA LOW.

TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93415XC, 93415AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93415XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current		95	130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				155	mA	$T_A = 0°C$	
				170	mA	$T_A = -55°C$	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93415AXC			93415XC			93415XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	30		15	40		15	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		15	30		20	40		20	50		
t_{AA}	Address Access Time		30	45		40	70		40	75		
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time		20	30		20	40		20	45	ns	
t_{WR}	Write Recovery Time		20	40		25	50		45	55		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	35	25		50	25		55	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		15	0		15	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	
C_O	Output Pin Capacitance		7	8		7	8		7	8		

NOTES:

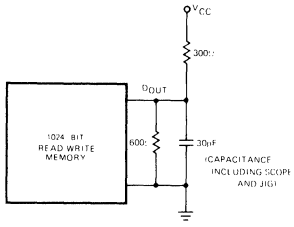
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values at V_{CC} = 5.0 V, T_A = 25°C, and MAX loading.
4. Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

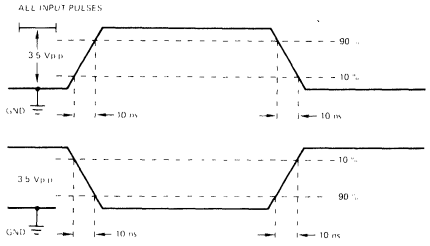
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



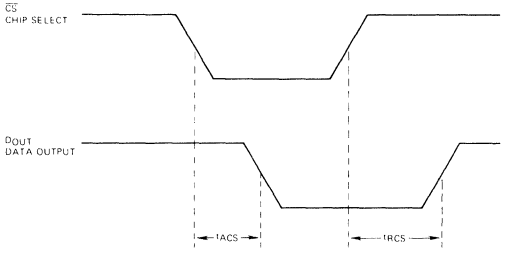
INPUT PULSES



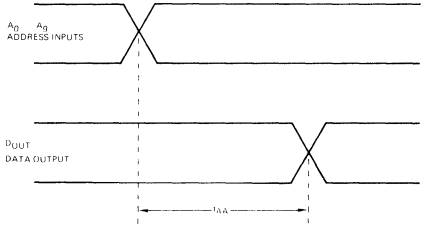
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

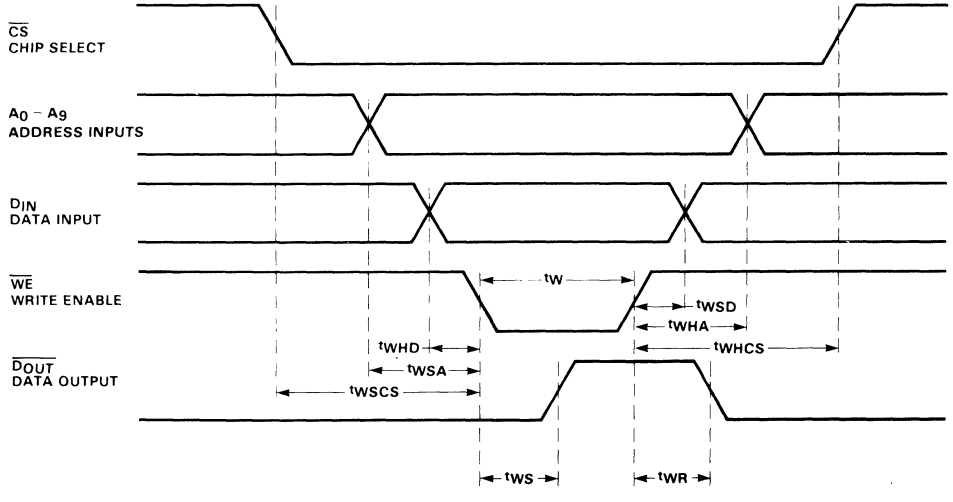


PROPAGATION DELAY FROM ADDRESS INPUTS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE MODE

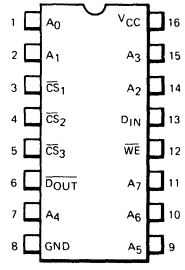


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

DESCRIPTION

The 93421 and 93421A are high speed 256-bit random access memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

CONNECTION DIAGRAM



PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$
$A_0 - A_7$
D_{IN}
$\overline{D_{OUT}}$
$\overline{WE}$

	LOADING (Notes a, b)
Chip Select Inputs	0.5 U.L.
Address Inputs	0.5 U.L.
Data Input	0.5 U.L.
Data Output	10 U.L.
Write Enable	0.5 U.L.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

DISTINCTIVE CHARACTERISTICS

- 3-state output
- Replacement for 54/74S200 and equivalent devices
- Organization – 256 words by one bit
- Three high speed chip select inputs
- Typical read access time
  - 93421A Commercial 30nsec
  - 93421 Commercial 35nsec
  - 93421 Military 35nsec
- On chip decoding
- Power dissipation – 1.2mW/bit
- Power dissipation decreases with temperature
- Inverted data output

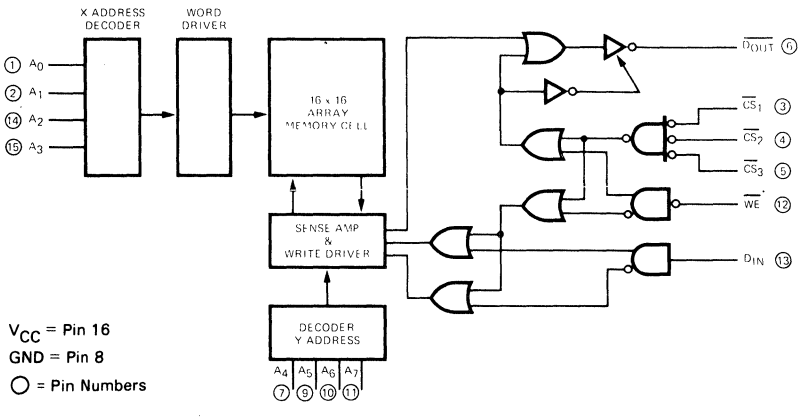
ORDERING INFORMATION

ORDER CODE	PACKAGE	TEMPERATURE*
35 ns Typical Access Time		
93421DC	Ceramic DIP**	Commercial
93421DM	Ceramic DIP**	Military
93421PC	Plastic DIP	Commercial
93421FM	Flatpak	Military
30 ns Typical Access Time		
93421ADC	Ceramic DIP**	Commercial

*Commercial = 0°C to +75°C
Military = −55°C to +125°C
**Available in both Ceramic DIP package options

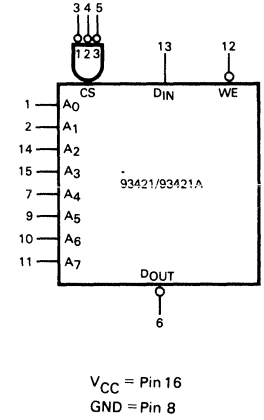
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW
b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V, and will source a minimum of 10 mA at 2.4 V.

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

RAYTHEON

FUNCTIONAL DESCRIPTION

The 93421/93421A are fully decoded 256-bit random access memories organized 256 words by one bit. Word selection is achieved by means of an eight-bit address, A_0 through A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	MODE
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = HIGH Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	$\overline{\text{Stored Data}}$
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93421AXC, 93421XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93421XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current	93421XC		90	124	mA	T_A = +75°C; V_{CC} = MAX, $\overline{WE}$ Grounded, all other inputs @ 4.5 V
		93421AXC		100	135		T_A = 0°C
		93421XM		90	117		T_A = +125°C
				100	143		T_A = −55°C
V_{OH}	Output HIGH Voltage	93421XC,AXC	2.4			V	I_{OH} = −10.3 mA
		93421XM	2.4			V	I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93421AXC MIN	93421AXC TYP (Note 3)	93421AXC MAX	93421XC MIN	93421XC TYP (Note 3)	93421XC MAX	93421XM MIN	93421XM TYP (Note 3)	93421XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	30		20	30		25	40		See Test Circuit
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	30		20	40	ns	and Waveforms
t_{AA}	Address Access Time		30	40		35	50		35	60		Note 5
WRITE MODE	DELAY TIMES											
t_{ZWS}	Write Disable to HIGH Z	10	20	35	10	20	35	10	20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	10		30	10		40	10			See Test Circuit
t_{WSD}	Data Set-Up Time Prior to Write	0	0		0	0		0	0			and Waveforms
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			Note 6
t_{WSA}	Address Set-Up Time	0	0		0	0		0	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0		0	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Capacitance		2.5	3.5		2.5	3.5		2.5	3.5	pF	Measured with
C_O	Output Capacitance		5	7		5	7		5	7		pulse technique

NOTES:

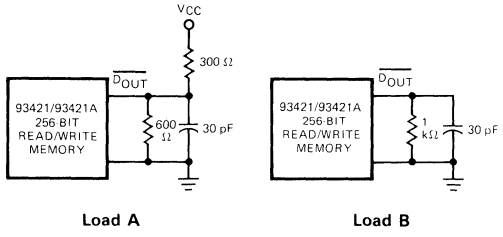
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C / Watt, Ceramic DIP; 65°C / Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C / Watt, Ceramic DIP; 110°C / Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C / Watt, Ceramic DIP; 25°C / Watt, Plastic DIP; 10°C / Watt, Flatpak.

5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

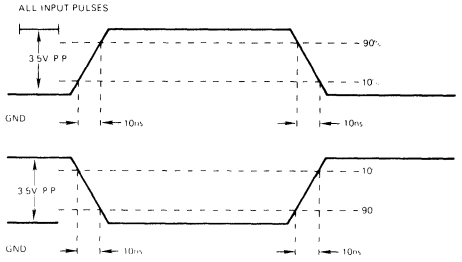
AC TEST LOAD AND WAVEFORM

LOADING CONDITION



Load A Load B

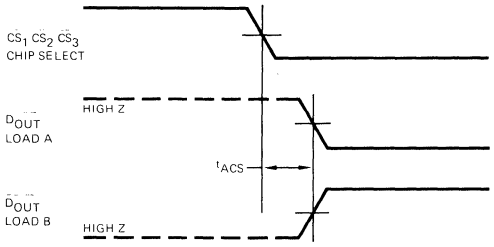
INPUT PULSES



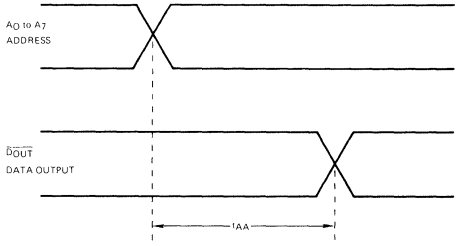
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

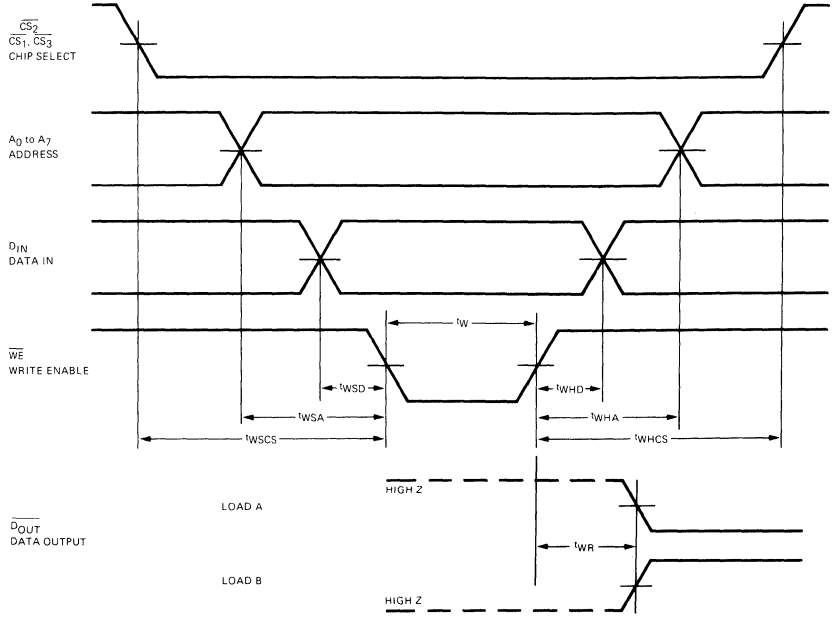


PROPAGATION DELAY FROM ADDRESS



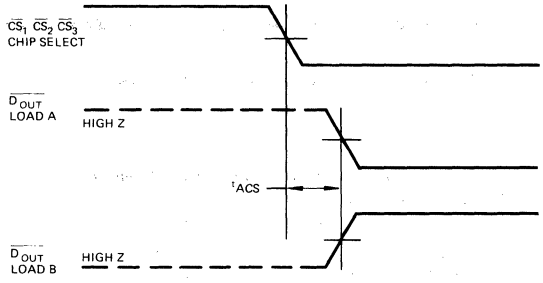
(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE MODE

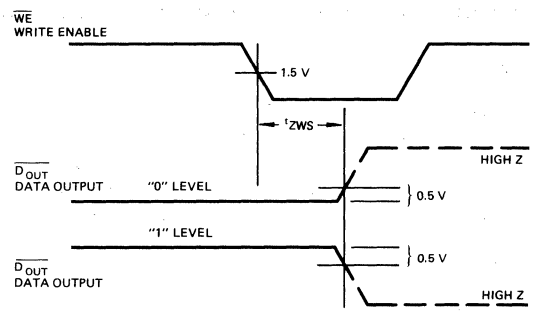


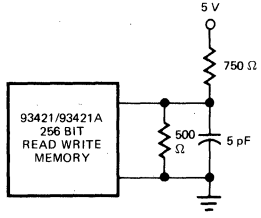
(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



WRITE ENABLE TO HIGH Z DELAY





Load C

(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

DESCRIPTION

The 93425 and 93425A are 1024-bit read/write random access memories organized 1024 words by one bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical address access times of 40nsec for the 93425 and 30nsec for the 93425A.

The 93425 and 93425A include full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select and Write Enable. They are fully compatible with standard DTL and TTL logic families. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

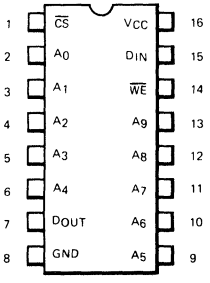
DISTINCTIVE CHARACTERISTICS

- 3-state output
- Organized 1024 words by one bit
- TTL inputs and output – 16mA drive capability
- Typical read access time

93425A	Commercial	30nsec
93425	Commercial	40nsec
93425	Military	40nsec

- Chip select access time 15nsec typical
- Non-inverting data output
- Power dissipation 0.5mW/bit typical
- Power dissipation decreases with increasing temperature

CONNECTION DIAGRAM



PIN NAMES

$\overline{CS}$	Chip Select
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

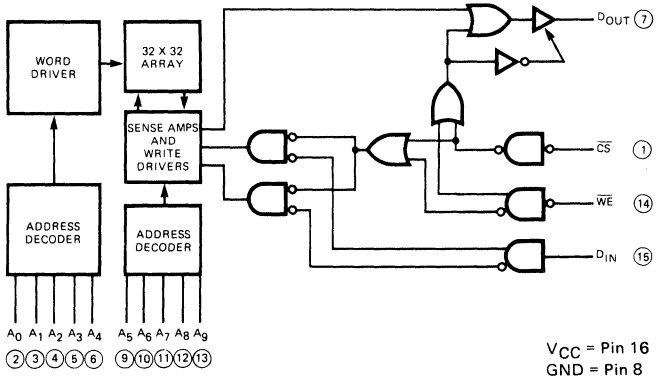
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ORDERING INFORMATION

ORDER CODE	PACKAGE	TEMPERATURE*
93425DC	Ceramic DIP	Commercial
93425DM	Ceramic DIP	Military
93425PC	Plastic DIP	Commercial
93425FM	Flatpak	Military
93425ADC	Ceramic DIP	Commercial
93425APC	Plastic DIP	Commercial

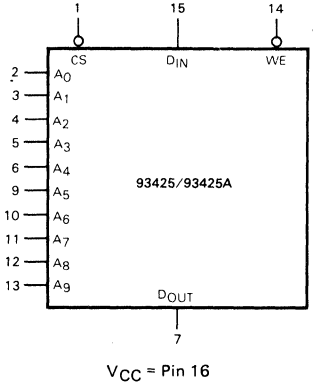
*Commercial = 0°C to +75°C
Military = −55°C to +125°C

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION

The 93425/93425A are fully decoded 1024-bit random access memories organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0 to A_9.

The chip select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW write enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at $\overline{D_{OUT}}$ and is non-inverted.

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	NOT SELECTED
L	L	L	HIGH Z	WRITE "0"
L	L	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired.)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93425XC, 93425AXC	4.75 V	5.0 V	5.25 V	0°C to +75 C
93425XM	4.50 V	5.0 V	5.50 V	−55 C to +125 C

X package type: F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7
V_{OH}	Output HIGH Voltage	93425XC	2.4			V	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%
		93425XM	2.4			V	I_{OH} = −5.2 mA
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current				130	mA	$T_A \geq 75°C$; V_{CC} = MAX, All Inputs Grounded
				95	155	mA	$T_A = 0°C$; V_{CC} = MAX, All Inputs Grounded
					170	mA	$T_A = -55°C$; V_{CC} = MAX, All Inputs Grounded

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93425AXC MIN	93425AXC TYP	93425AXC MAX	93425XC MIN	93425XC TYP	93425XC MAX	93425XM MIN	93425XM TYP	93425XM MAX	UNITS	CONDITIONS
		(Note 3)			(Note 3)			(Note 3)				
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	30		15	40		15	45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to HIGH Z		15	30		20	40		20	50		
t_{AA}	Address Access Time		30	45		40	70		40	75		
WRITE MODE	DELAY TIMES											
t_{ZWS}	Write Disable to HIGH Z		20	30		20	40		20	45	ns	
t_{WR}	Write Recovery Time		20	40		25	50		45	55		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	30	25		50	25		55	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		15	0		15	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		7	8		

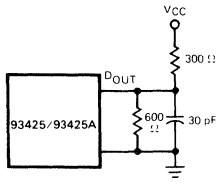
NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50 C/Watt, Ceramic DIP; 65 C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90 C/Watt, Ceramic DIP; 110 C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25 C/Watt, Ceramic DIP; 25 C/Watt, Plastic DIP; 10 C/Watt, Flatpak.

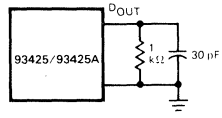
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS

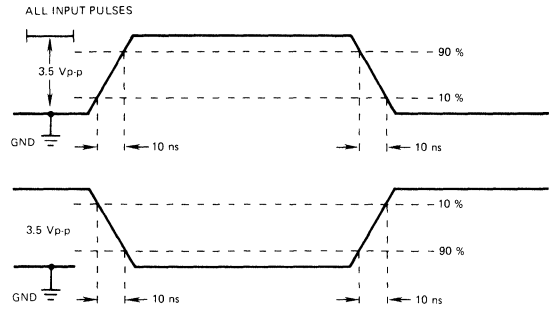


Load A



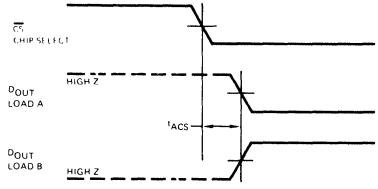
Load B

INPUT PULSES

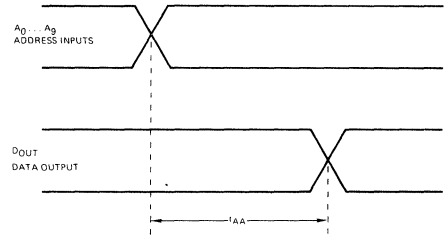


READ MODE

PROPAGATION DELAY FROM CHIP SELECT



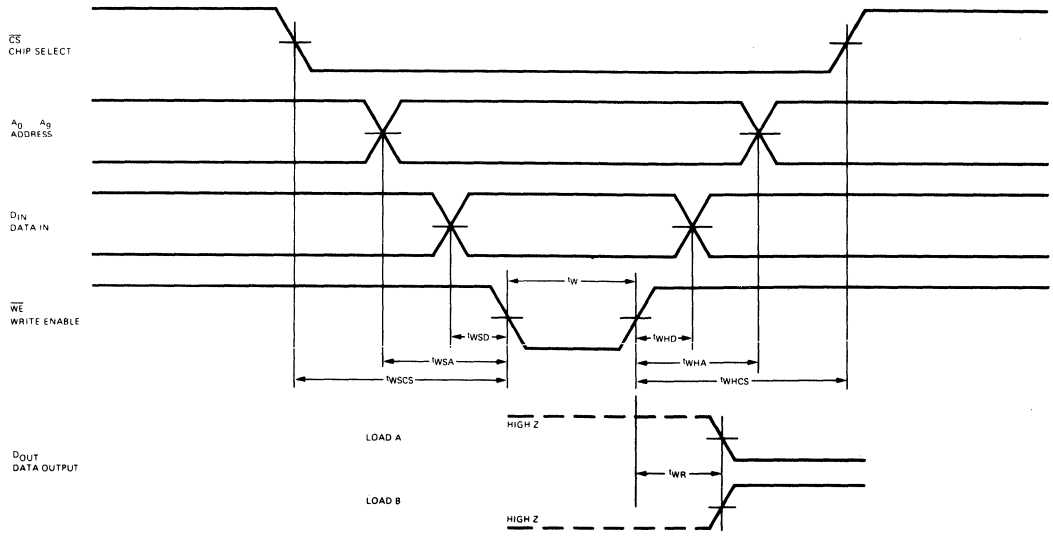
PROPAGATION DELAY FROM ADDRESS INPUTS



(All time measurements referenced to 1.5 V)

AC WAVEFORMS (Cont'd)

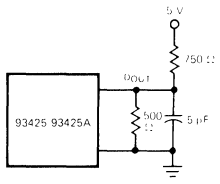
WRITE MODE



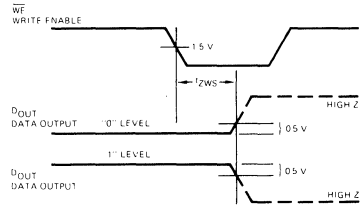
(All above measurements referenced to 1.5 V)

RAYTHEON

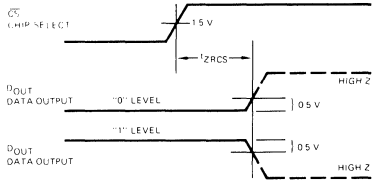
WRITE ENABLE TO HIGH Z DELAY



Load C



PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

FUNCTIONAL DESCRIPTION

The R29600 and the R29601 are electrically programmable Low-Power Schottky TTL read only memories. Both devices are organized as 256 words of 8 bits each; the R29600 has open collector outputs and the R29601 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of fuse material which is conductive, but which can be opened by passing a short high-current pulse through it.

The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input.

After programming, the device can be used for microprogram storage or random logic function generation, like any read-only memory. If either chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

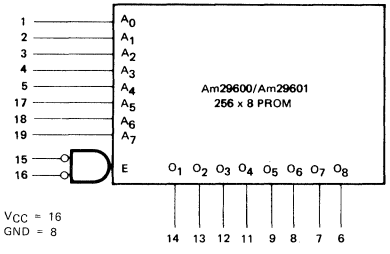
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	R29600DC
Hermetic DIP	–55°C to +125°C	R29600DM
Hermetic Flat Pak	–55°C to +125°C	R29600FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	R29601DC
Hermetic DIP	–55°C to +125°C	R29601DM
Hermetic Flat Pak	–55°C to +125°C	R29601FM

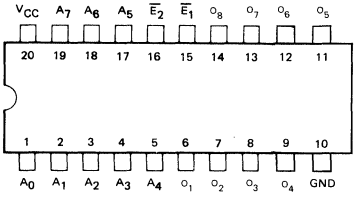
DISTINCTIVE CHARACTERISTICS

- Field programmable read only memory
- Highly reliable nichrome fuses
- Pin compatible with other popular 256 by 8 PROMS
- Typical fusing time of 95μs/bit
- 70ns access time at 25°C
- Three-state and open-collector versions

LOGIC SYMBOL

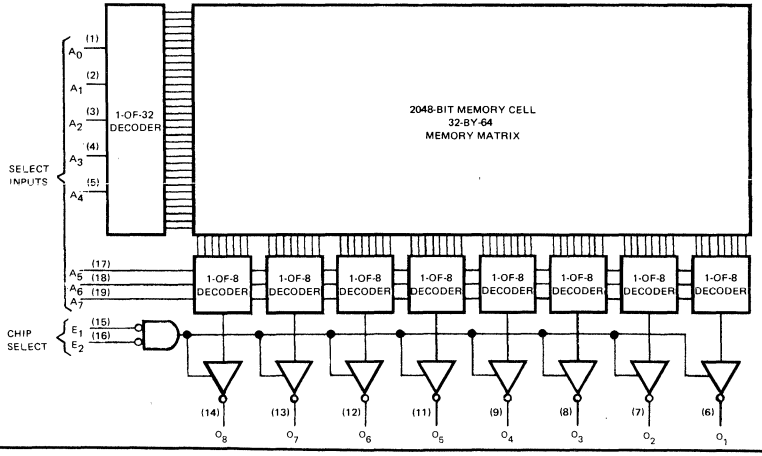


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM



RAYTHEON

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Input Voltage (Address Inputs)	−0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	26V
Output Current into Outputs During Programming	125 mA
DC Input Voltage (Chip Select Input – Pin)	−0.5V to +33V
DC Input Current	−30mA to +5mA

OPERATING RANGE

R29600XC, R29601XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%	COM'L
R29600XM, R29601XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIL

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (R29601 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA			0.4	Volts
			I_{OL} = 16mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			−60	−250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				10	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_I (Pin 15 Only)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V				1.0	mA
I_{SC} (R29601 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−85	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.			90	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = 18mA				−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_{CS} = 2.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			−40	

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

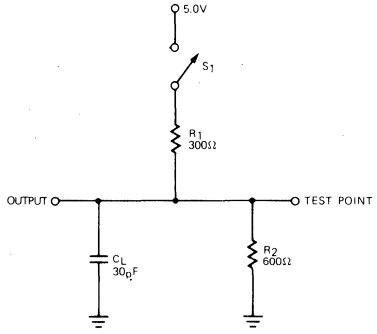
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

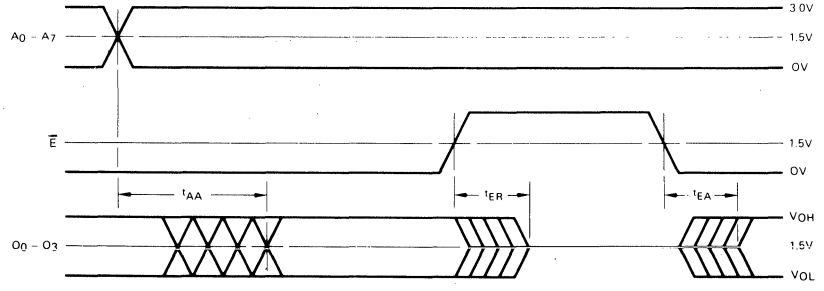
Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 25°C	Max. Com'l	Max. Mil	Units
t_{AA}	Address Access Time	C_L = 30 pF R_L = 300 Ω to V_{CC} and 600 Ω to GND (16 mA Load) Note 1	50				ns
t_{EA}	Enable Access Time		20				ns
t_{ER}	Enable Recovery Time		20				ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

AC TEST CIRCUIT



SWITCHING WAVEFORMS



Note: Level on output while E is HIGH is determined externally.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

ROGRAMMING INSTRUCTIONS

DEVICE DESCRIPTION

he device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a ni-hrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There re 1024 fusible links on the chip. Programming equipment can be obtained from Data I/O, Inc., and other manufacturers of /ROM programming equipment.

PROGRAMMING DESCRIPTION

o select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_7, a V_{CC} f 5.50 V is applied or left applied, and the program pin (Enable $\overline{E}_1$) and the output to be programmed are taken to an evated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, nce internal decoding circuitry is capable of sinking only one unit of programming current at a time.

ENABLE E_2

nable $\overline{E}_2$ (pin 16) is a logic enable and is not used during programming. It may be high, low or open during programming. 'hen checking that an output is programmed (which is called verification) enables $\overline{E}_1$ and $\overline{E}_2$ must be low to activate the evice. Since $\overline{E}_2$ must be low during verification and the state is irrelevant during programming, the simplest procedure is to round $\overline{E}_2$ during programming and verification.

TIMING

he programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that he output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before he output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The pro-ramming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 4.

VERIFICATION

fter programming a device, it can be checked for a low output by taking both enables low. Since we must guarantee opera-on at minimum and maximum V_{CC}, current and temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} nd 0.2 mA at 6.0 V V_{CC} at room temperature.

BOARD PROGRAMMING

nits may be programmed at the board level by bringing the program pin of each package to the card connector. To program particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs gether as required by the system function and only apply V_{CC} to the device to be programmed. The number of units oldered on a board should be consistant with expected programming yields to avoid rework.

UNPROGRAMMABLE UNITS

isual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high pro-amming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will pen without actually programming it. **UNITS RETURNED TO RAYTHEON AS UNPROGRAMMABLE MUST BE AC-OMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PRO-RAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

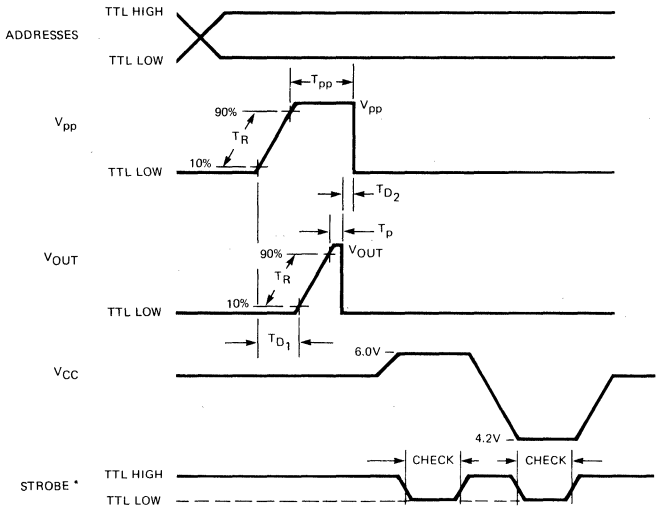
ROGRAMMING SPEED

ypically fuses will blow on the rise time of the pulse.

automated programmers which must copy devices in a short time because of production requirements, the following pulse d voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be veri-ed after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



T_R	0.4 V/μs ± 15%
T_{pp}	95 ± 15 μs
T_p	1 μs min., 8 μs max.
T_{D_1}	80 ± 10 μs
T_{D_2}	100 ns min.

*NOTE: Output Load = 0.2 mA during 6.0 V check
Output Load = 12 mA during 4.2 V check

REQUIRED INFORMATION FOR RAYTHEON TO PROGRAM TO YOUR TRUTH TABLE

TRUTH TABLES

Raytheon can program devices at our facility from Raytheon truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

		OUTPUTS							
WORD	PIN →	14	13	12	11	9	8	7	6
NUMBER		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	H	L	H	L	L	H
1		L	H	L	H	H	H	H	L
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
255		L	H	H	H	H	H	H	H

Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 255 = LHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to Raytheon in an ASCII tape format. Information can be sent to us by air mail or TWX 910-379-6481. The tape reading equipment at Raytheon only recognizes ASCII characters B, P, N, and F and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters B, H, L, F. Word addresses must begin with zero and count sequentially to word 255.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is $O_8, O_7, O_6, O_5, O_4, O_3, O_2, O_1$, not $O_1, O_2, O_3, O_4, O_5, O_6, O_7, O_8$.

A typical list of characters and their machine interpretations are shown in the next page.

SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY

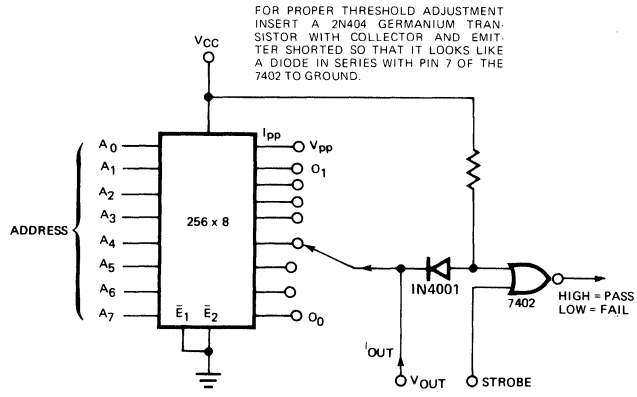
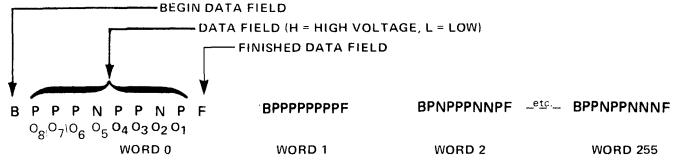


FIGURE 5.
THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

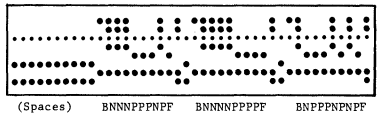
RAYTHEON PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below:

```
BLARNEY ELECTRONICS 408-735-8140
TWX 911-338-9225
P0142              BNNNPPPNPF BNNNNPPPPF BNPPPNPNPF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF
29601              BNNNNNNNNF BNNNPPPNPF BPPPPPPPPF BNPPNPNNNF BNPPPNNNPF BNNNNNNNNF BPPPPPPPPF BNNNNNNPPF
```

8 LEVEL TWX:



Interpretation: (Spaces) BNNNPPPNPF BNNNNPPPPF BNPPPNPNPF

PROGRAMMING PARAMETERS – Do Not Test These Limits or You May Program the Device

SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50V V_{out} = 5.0V to 25V V_{pp} = 4.50V		0		mA
		V_{pp} = 27V		77		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 27V, V_{CC} = 5.50V V_{out} = 9.0V		0.1		mA
		V_{out} = 20V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 27V V_{out} =20V V_{CC} = 5.50V		0.1		mA
T_R	Rise Time of Program Pulse Applied to the Data Out or Program Pin		0.34	0.4	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV_1}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 4.2V	11	12	13	mA
I_{OLV_2}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 6.0V	0.19	0.2	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		27	27	33	V
V_{out}	Required Programming Voltage on the Output Pin		20	20	26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33V V_{out} = 26V V_{CC} = 5.50V	150			mA
T_{pp}	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		80	95	110	μs
T_{D_1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
T_{D_2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			ns

FUNCTIONAL DESCRIPTION

The R29660 and R29661 are electrically programmable Low-Power Schottky TTL read only memories. Both devices are organized as 256 words of 4 bits each; the R29660 has open collector outputs and the R29661 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of fuse material which is conductive, but which can be opened by passing a short, high-current pulse through it.

The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input.

After programming, the device can be used for microprogram storage or random logic function generation, like any read-only memory. If either chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

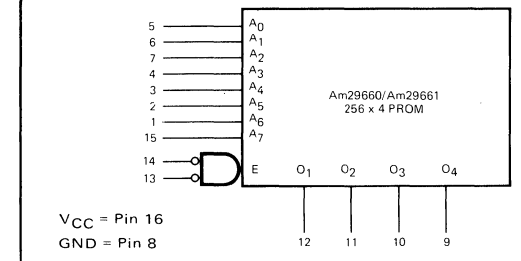
DISTINCTIVE CHARACTERISTICS

- Field programmable read only memory
- Highly reliable nichrome fuses
- Pin compatible with other popular 256 by 4 PROMS
- Typical fusing time of 95μs/bit
- 60ns access time at 25°C
- Three-state and open-collector versions

ORDERING INFORMATION

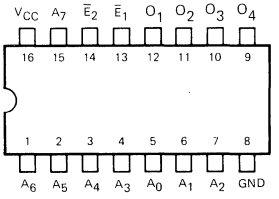
Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	R29660DC
Hermetic DIP	−55°C to +125°C	R29660DM
Hermetic Flat Pak	−55°C to +125°C	R29660FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	R29661DC
Hermetic DIP	−55°C to +125°C	R29661DM
Hermetic Flat Pak	−55°C to +125°C	R29661FM

LOGIC SYMBOL



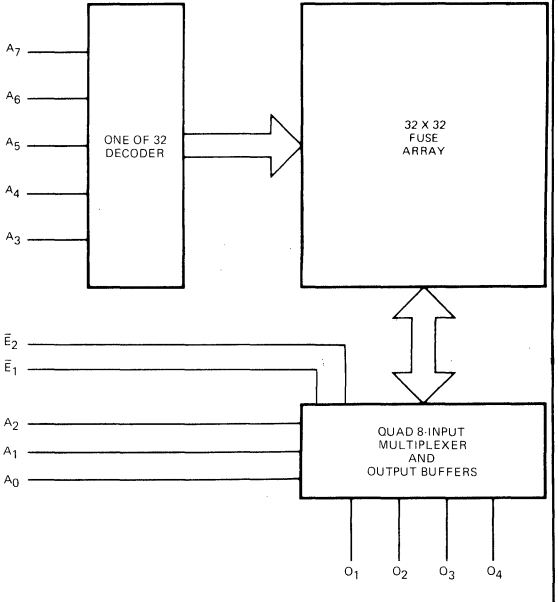
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLOCK DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Input Voltage (Address Inputs)	−0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	26V
Output Current into Outputs During Programming	125 mA
DC Input Voltage (Chip Select Input – Pin 13)	−0.5V to +33V
DC Input Current	−30mA to +5mA

OPERATING RANGE

R29660XC, R29661XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%	COM'L
R29660XM, R29661XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIL

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29661 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA I_{OL} = 16mA			0.4 0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			−60	−250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				10	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_I (Pin 13 Only)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V				1.0	mA
I_{SC} (Am29661)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−85	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.			90	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = 18mA				−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_{CS} = 2.4V	V_O = 4.5V V_O = 2.4V V_O = 0.4V			100 40 −40	μA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

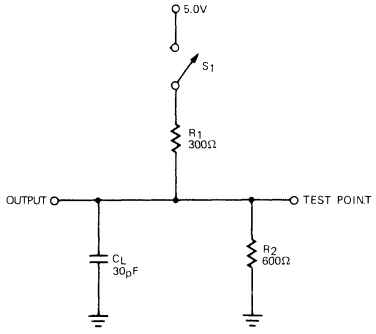
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

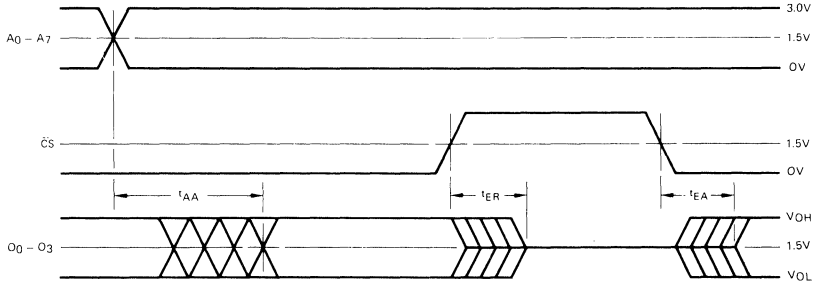
Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 25°C	Max. Com'l	Max. Mil	Units
t_{AA}	Address Access Time	C_L = 30 pF R_L = 300 Ω to V_{CC} and 600 Ω to GND (16 mA Load) Note 1	45	60	70	80	ns
t_{EA}	Enable Access Time		20	30	35	40	ns
t_{ER}	Enable Recovery Time		20	30	35	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

AC TEST CIRCUIT



SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Note: Level on output while $\overline{E}$ is HIGH is determined externally.

PROGRAMMING INSTRUCTIONS

1) DEVICE DESCRIPTION

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. There are 1024 fusible links on the chip. Programming equipment can be obtained from Data I/O, Inc., and other manufacturers of P/ROM programming equipment.

2) PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on A_0 through A_7, a V_{CC} of 5.50 V is applied or left applied, and the program pin (Enable E_1) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

3) ENABLE E_2

Enable E_2 (pin 14) is a logic enable and is not used during programming. It may be high, low or open during programming. When checking that an output is programmed (which is called verification) enables E_1 and E_2 must be low to activate the device. Since E_2 must be low during verification and the state is irrelevant during programming, the simplest procedure is to ground E_2 during programming and verification.

4) TIMING

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 4.

5) VERIFICATION

After programming a device, it can be checked for a low output by taking both enables low. Since we must guarantee operation at minimum and maximum V_{CC}, current and temperature, the device must be required to sink 12 mA at 4.20 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

6) BOARD PROGRAMMING

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistant with expected programming yields to avoid rework.

7) UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO RAYTHEON AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULDN'T BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

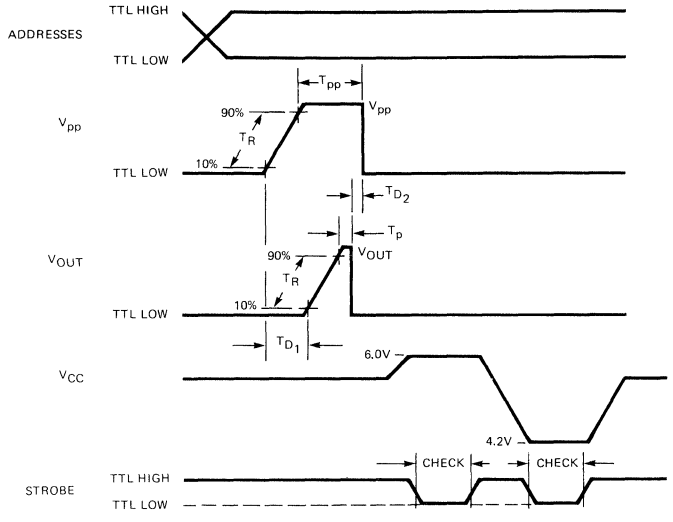
PROGRAMMING SPEED

Typically fuses will blow on the rise time of the pulse.

In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAM TIMING



T_R	0.4 V/μs ± 15%
T_{pp}	95 ± 15 μs
T_P	1 μs min., 8 μs max.
T_{D_1}	80 ± 10 μs
T_{D_2}	100 ns min.

*NOTE: Output Load = 0.2 mA during 6.0 V check
Output Load = 12 mA during 4.2 V check

TRUTH TABLES

Raytheon can program devices at our facility from Raytheon truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

WORD NUMBER	PIN →	OUTPUTS 9	10	11	12
		O_4	O_3	O_2	O_1
0		H	H	H	L
1		L	H	L	H
-		.	.	.	.
-		.	.	.	.
255		L	H	H	H

Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 255 = HHHHHHHH.

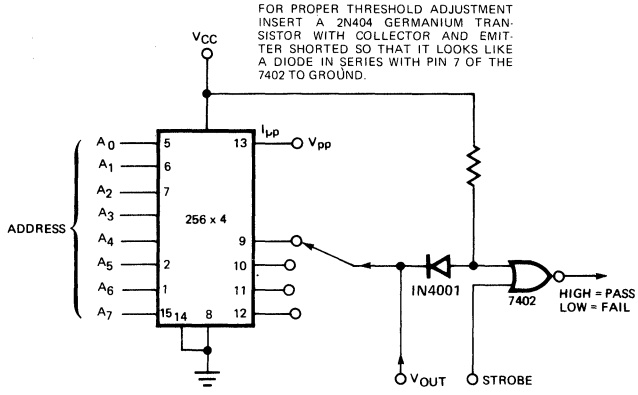
PAPER TAPE FORMAT

Truth tables can also be sent to Raytheon in an ASCII tape format. Information can be sent to us by air mail or TWX 910-379-6481. The tape reading equipment at Raytheon only recognizes ASCII characters S, B H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 255.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_4, O_3, O_2, O_1, not O_1, O_2, O_3, O_4.

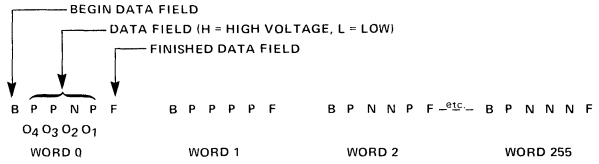
A typical list of characters and their machine interpretations are shown on the next page.

SUGGESTED IMPLEMENTATION OF THE VERIFICATION CIRCUITRY



THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES

FIGURE 5.
THE 1N4001 DIODE PROTECTS THE INPUT OF THE 7402 FROM THE HIGH PROGRAMMING VOLTAGES



The required heading information at the beginning of the tape is as follows:

CUSTOMERS NAME AND PHONE _____ TRUTH TABLE NUMBER _____

CUSTOMERS TWX NUMBER _____ NUMBER OF TRUTH TABLES _____

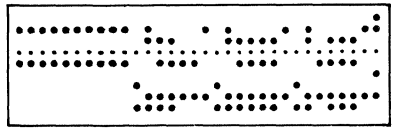
PURCHASE ORDER NUMBER _____ TOTAL NUMBER OF PARTS _____

RAYTHEON PART NUMBER _____ NUMBER OF PARTS OF EACH TRUTH TABLE _____

CUSTOMER SYMBOLIZED PART NUMBER _____ 25 BELL OR RUBOUT CHARACTERS _____

An example is shown below:

BLARNEY ELECTRONICS 408-735-8140
TWX 911-338-9225
PO142 BNNNPF BNNNNF BNPNPF BNPPPF BNNPPF BPPPPF BNNNPF BNPNPF BNNNNF
29660 BNNNNF BNPNPF BNNPPF BPPPNF BPPNNF BNNPPF BPPNNF BNNPPF BNPNPF
0431
12 8 level
1 TWX
3
3



RAYTHEON

PROGRAMMING PARAMETERS – Do Not Test These Limits or You May Program the Device

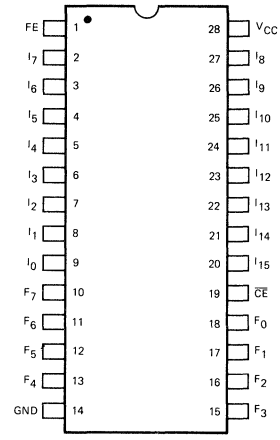
SYMBOL	PARAMETERS	TEST CONDITION See Figure 4	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current Program Pin During Programming, Before and After Fuse Has Blown	V_{CC} = 5.50V V_{out} = 5.0V to 25V V_{pp} = 4.50V		0		mA
		V_{pp} = 27V		77		mA
I_{out}	Current into Output During Programming Before the Fuse Has Programmed	V_{pp} = 27V, V_{CC} = 5.50V V_{out} = 9.0V		0.1		mA
		V_{out} = 20V		16		mA
I_{out}	Current into Output During Programming After the Fuse Has Programmed	V_{pp} = 27V V_{out} =20V V_{CC} = 5.50V		0.1		mA
T_R	Rise Time of Program Pulse Applied to the Data Out or Program Pin		0.34	0.4	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV_1}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 4.2V	11	12	13	mA
I_{OLV_2}	Output Current Required During Verification	Both Chip Enables Low T_A = 25°C, V_{CC} = 6.0V	0.19	0.2	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required Programming Voltage on Program Pin		27	27	33	V
V_{out}	Required Programming Voltage on the Output Pin		20	20	26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{pp} = 33V V_{out} = 26V V_{CC} = 5.50V	150			mA
T_{pp}	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		80	95	110	μs
T_{D_1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
T_{D_2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			ns

FUNCTIONAL DESCRIPTION

The R29690 and R29691 are field programmable random logic arrays. The R29691 has three-state outputs and the R29690 has open collector outputs. The devices have 16 data inputs and contain 48 intermediate product terms. Random logic functions are implemented by using the device like 8 large AND-OR-INVENT gates. Up to 48 AND functions may be generated in the device, where each AND function is the product of any or all of the 16 inputs (I_0–I_{15}) or their complements. Any of the AND functions which have been generated may then be OR'ed to form an output function on one of the F outputs. The F output may also be programmed to invert, i.e., form an AND-OR-INVERT function, rather than AND-OR.

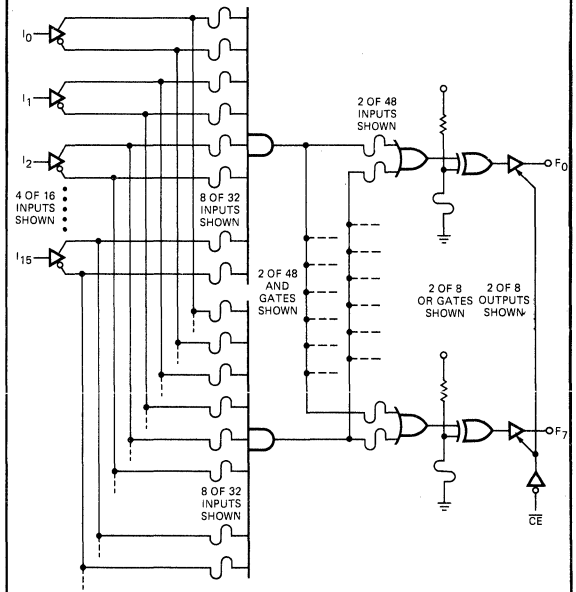
Units are shipped with all fuses intact, and all outputs LOW. Each of the 48 AND functions contains both true and complement of each of the 16 input variables. (Therefore all AND functions are initially false). A variable (or its complement) is inserted into an AND gate by blowing the fuse for the undesired state. A variable is removed from an AND gate by blowing both the true and complement fuses. Each OR function contains the outputs of all 48 AND functions. AND functions are removed from the OR gates by blowing the proper fuse. If the output is to be negated, then a fuse is blown on an EXCLUSIVE-OR gate at the output. That output then becomes an AND-OR-INVERT function of the inputs. The chip enable input ($\overline{CE}$) forces all outputs OFF when HIGH. When LOW, the outputs will be OFF or LOW for the R29690, or HIGH or LOW for the R29691.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC BLOCK DIAGRAM



DISTINCTIVE CHARACTERISTICS

- LSI replacement for random logic and inefficiently used ROMs and PROMs
- 16 inputs – 8 outputs – 48 product terms
- Logic equation for each output field programmed by fusing nichrome links
- Each output can be programmed to be active HIGH or active LOW
- 100% processing in accordance with MIL-STD-883
- Three-state or open collector outputs controlled by active LOW chip enable.

ORDERING INFORMATION

This data is based on design goals and is subject to change following complete characterization.

RAYTHEON

OPERATING RANGE

Part No.	Ambient Temperature	V_{CC}
R29690DC, R29691DC	T_A = 0° C to +75° C	5.0V ±5%
R29690DM, R29691DM	T_A = 55° C to +125° C	5.0V ±10%

PRELIMINARY

THESE SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (RA29691 Only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 12mA V_{IN} = V_{IH} or V_{IL}			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−0.03	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V			<1	25	μA
I_{SC} (Am29791 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−90	mA
I_{CC}	Power Supply Current	$\overline{CE}$ = GND, all other inputs = 4.5V V_{CC} = MAX.			120		mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{CEX}, I_{OLK}	Output Leakage Current	$V_{\overline{CE}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.45V	−40			

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			RA29690DC RA29691DC			RA29690DM RA29691DM			
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
$t_{PZL}(\overline{CE})$ $t_{PZH}(\overline{CE})$	Delay Chip Select to Output Active HIGH or LOW	C_L = 30pF R_L = 300Ω to V_{CC} and 600Ω to GND (16mA Load) Note 2		25			40		ns
$t_{PLZ}(\overline{CE})$ $t_{PHZ}(\overline{CE})$	Delay Chip Select HIGH to Output OFF			25			40		ns
$t_{PLH}(I)$	Delay Input to Output HIGH			30			50		ns
$t_{PHL}(I)$	Delay Input to Output LOW								

Note 2. 300Ω resistor opened for t_{DIS} and t_{EN} measurements between HIGH and OFF states.

PROGRAMMING PROCEDURE

Programming is facilitated by two internal 1-of-48 decoders used to select one of the 48 product terms. One of these decoders is activated by applying high-voltage logic to inputs I_0-I_5, and the other by applying high voltage logic to outputs F_0-F_5.

Input variables which are not desired in a particular AND gate are fused out by selecting the AND gate with the decoder on output F_0-F_5, applying a HIGH or LOW TTL level to the input variable to be fused, applying high voltage levels to all other input variables, and pulsing the chip enable input.

Product terms which are to be removed from an OR gate are fused out by selecting the appropriate AND gate using the decoder on inputs I_0-I_5, applying a high voltage level to the output for the desired OR gate, and pulsing the chip enable input.

The polarity of the output may be inverted by deselecting the chip, applying a high voltage to the desired output, and pulsing the FE input.

BASIC SYSTEM ARCHITECTURE

The Am2901 is designed to be used in microprogrammed systems. Figure 15 illustrates such an architecture. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2909 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2909 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901's, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

EXPANSION OF THE Am2901

The Am2901 is a four-bit CPU slice. Any number of Am2901's can be interconnected to form CPU's of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901's to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 14. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901's are connected together and to a pull-up resistor. This line will go HIGH if and only if the output of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic

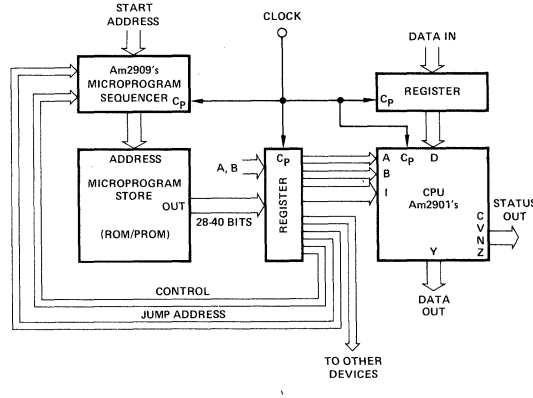


Figure15. Microprogrammed Architecture Around Am2901's.

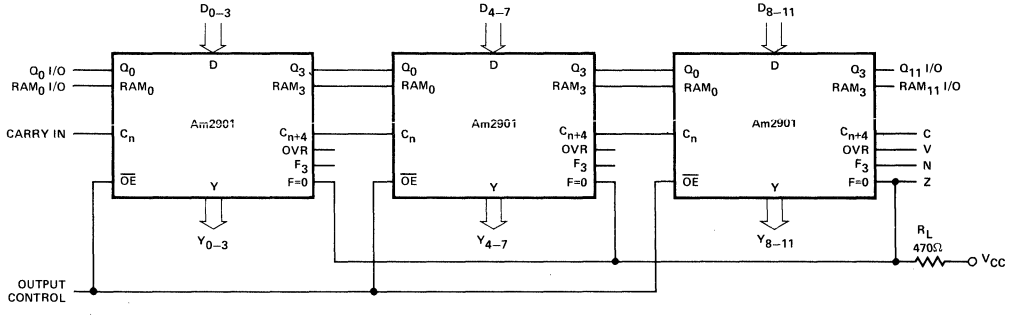


Figure 16. Three Am2901's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figures 17 and 18 illustrate single and multiple level lookahead.

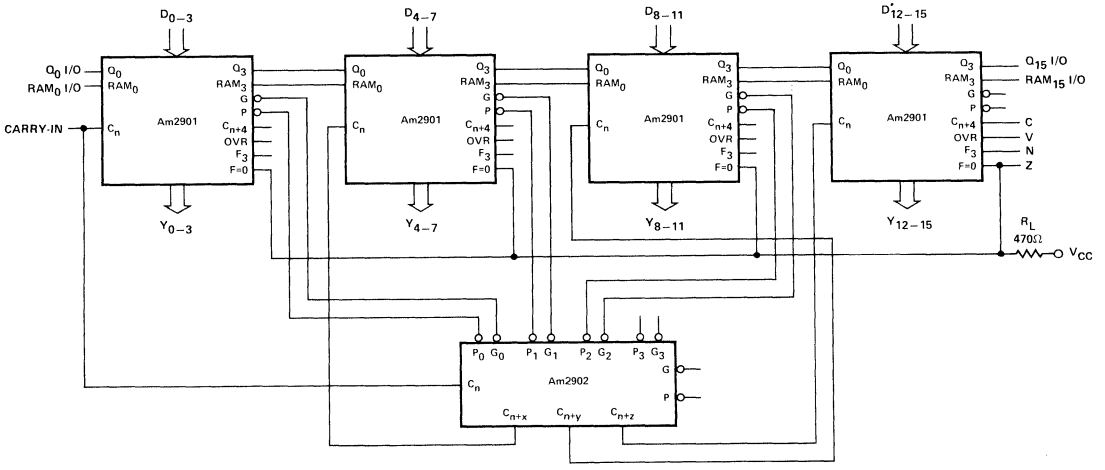


Figure 17. Four Am2901's in a 16-Bit CPU using the Am2902 for Carry Lookahead.

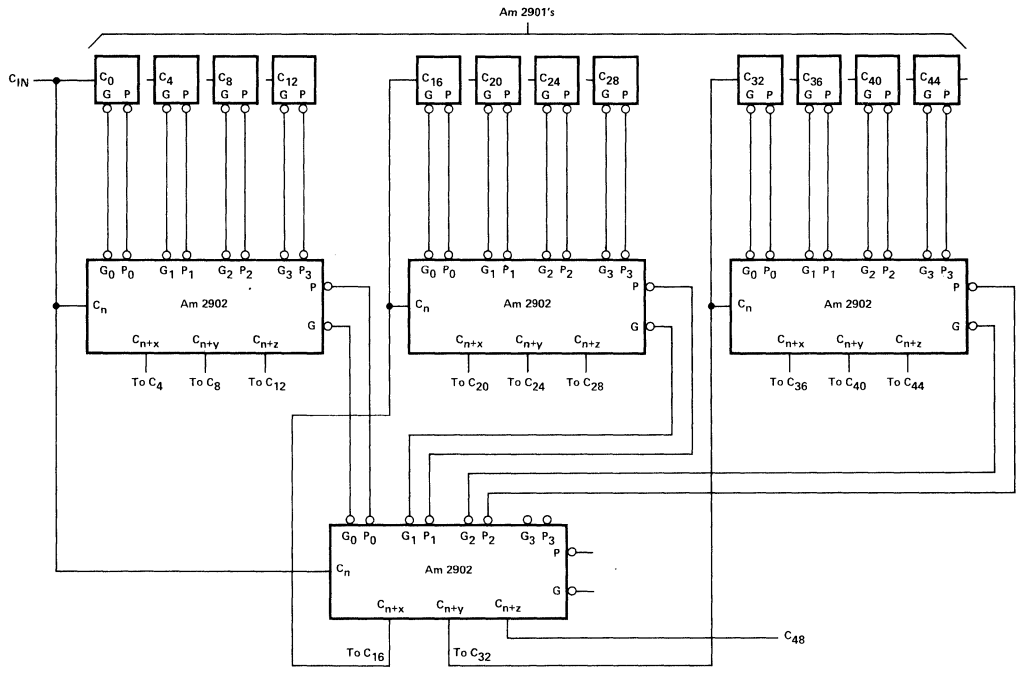


Figure 18. Carry Lookahead Scheme for 48-Bit CPU using 12 Am2901's. The Carry-Out Flag (C_{48}) Should be Taken from the Lower Am2902 Rather than the Right-Most Am2901 for Higher Speed.

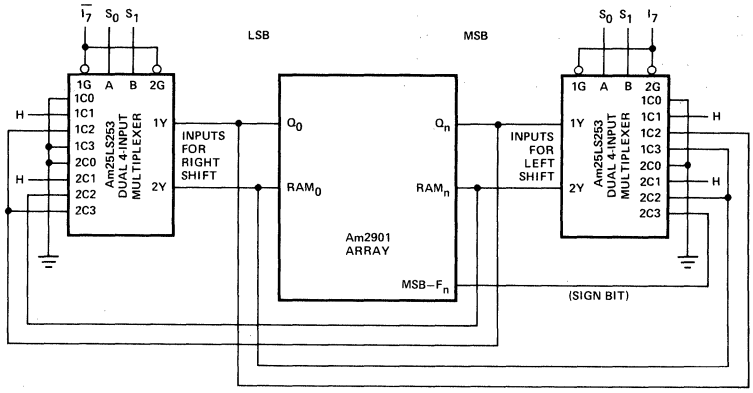


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM up/down shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}	(Right)	One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1	(Left)	One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output and both Q and ALU output are shifted down one place. The instruction lines to the Am2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901's shift up or down as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

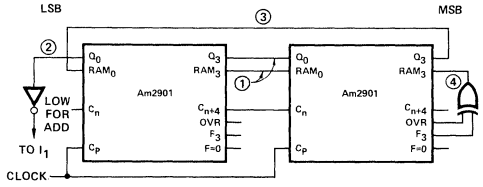


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 Bit) (Corresponding A, B and I Connected Together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F}_3$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight

$$(Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0).$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901's for each step of a signed, two's complement multiplication.

Initial Register States

R

0	Multiplier
1	Multiplicand
2	X
3	X

Am2901 Microcode

Program 2's Comp. Multiply

Date 8/5/75 By J. S.

Final Register States

R

0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = Q_0 \overline{LO}$	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = \overline{Q_0 LO}$	1	–	RAM_0	–	$F_3 \forall OVR$		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing an up shift of one place; then the ALU is shifted up one more place prior to storage.

Byte Swap of R_0

$A = B = 0$ $I = 701$ $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the Am2909 microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the Am2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the Am2909 instruction register. The fetch operation requires only two microcycles.

INTRODUCTION:

One of the main functions of digital logic systems is the generation of timing and control sequences. In the past, sequence control logic has been implemented by unique designs using flip-flops and gates. Current designs often use microprogram techniques based on combinations of counters and P/ROMs, due to the wide spread availability of low cost, high speed P/ROMs. These combinations of counters and P/ROMs tend to be significantly more flexible than their flip-flop logic, or hard wired, complements. Counter and P/ROM designs also tend to be significantly more powerful in the sense that they can be used to solve problems of much higher complexity and with a much lower chip count than is practical with a hard wired design.

The Am2909 Microprogram Sequencer is, in a sense, a sophisticated counter, which is used in conjunction with high speed P/ROMs in microprogram sequence control designs. Designs using the 2909 cover a broad range. Two of the better known examples include: Computer Control Units, which provide the sequence control for instruction execution in computers, and the I/O controllers for sophisticated computer Peripheral devices, such as high speed magnetic disc files and high speed magnetic tape units. Other examples include control units for high speed communication processing, and general purpose machine control at rates from DC to above 5 MHz. In order to understand the applicability of the Am2909 with sequence control, we will first examine the sequence control problem in general and the methods employed to solve it.

SEQUENCE CONTROL – SIMPLE PROBLEMS AND SOLUTIONS:

An example of a simple sequence control problem is the sequencer for an automatic coffee vending machine. In the automatic coffee vending machine, the user selects a machine operating sequence by pressing the appropriate button on the coffee machine's front panel. There may be six such buttons labeled: coffee black, coffee cream, coffee sugar, coffee cream & sugar, hot chocolate, soup. Each of these buttons must cause a specific sequence of actions inside the coffee machine in order to deliver a filled cup of coffee to the user. The sequence control unit for the coffee machine must generate signals such as: hot water on, coffee release, chocolate release, cream release, etc. In addition, it must generate these signals according to which of the six buttons was pressed. Furthermore, it must ignore the buttons until the coin has been inserted, during sequence operation, and until another coin has been inserted after the selected sequence is complete.

A block diagram of a hypothetical coffee machine and its sequence control are shown in Figure 1. The sequence list corresponding to each of the push buttons is shown in Figure 2. A coffee machine sequence controller can be designed using combinations of flip-flops and gates. An example of this type of design is shown in Figure 3. This approach is called the hard wired logic or random logic approach. The design in Figure 3 uses various gates, flip-flops and one-shots. This approach is typical of solid state sequence controller designs used in the past. The advantage

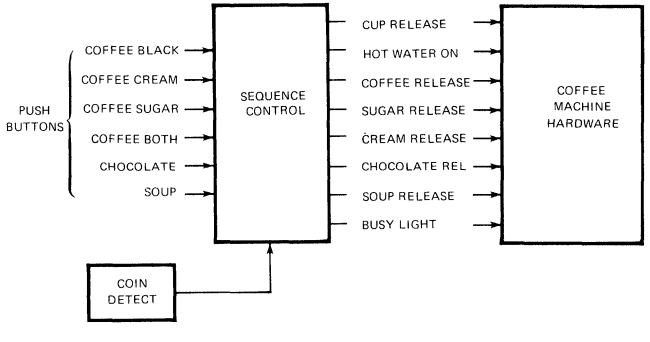


Figure 1. Coffee Machine Block Diagram.

STEP NUMBER	CUP RELEASE	WATER ON	COFFEE RELEASE	SUGAR RELEASE	CREAM RELEASE	CHOCOLATE RELEASE	SOUP RELEASE	BUSY LIGHT	COMMENTS
1	X							X	START
2								X	X = ALL SEQUENCES
3								X	A = COFFEE SEQUENCES
4								X	B = COFFEE & SUGAR SEQ.
5		X						X	C = COFFEE & CREAM SEQ.
6		X						X	D = CHOCOLATE ONLY
7		X	A			D	E	X	E = SOUP ONLY
8		X	A			D	E	X	
9		X	A			D	E	X	
10		X	A			D	E	X	
11		X	A			D		X	
12		X		B		D		X	
13		X		B		D		X	
14		X		B				X	
15		X			C			X	
16		X			C			X	
17		X			C			X	
18		X			C			X	
19		X						X	
20		X						X	
21		X						X	
22		X						X	
23		X						X	
24		X						X	END

Figure 2. Coffee Machine Combined Sequence List.

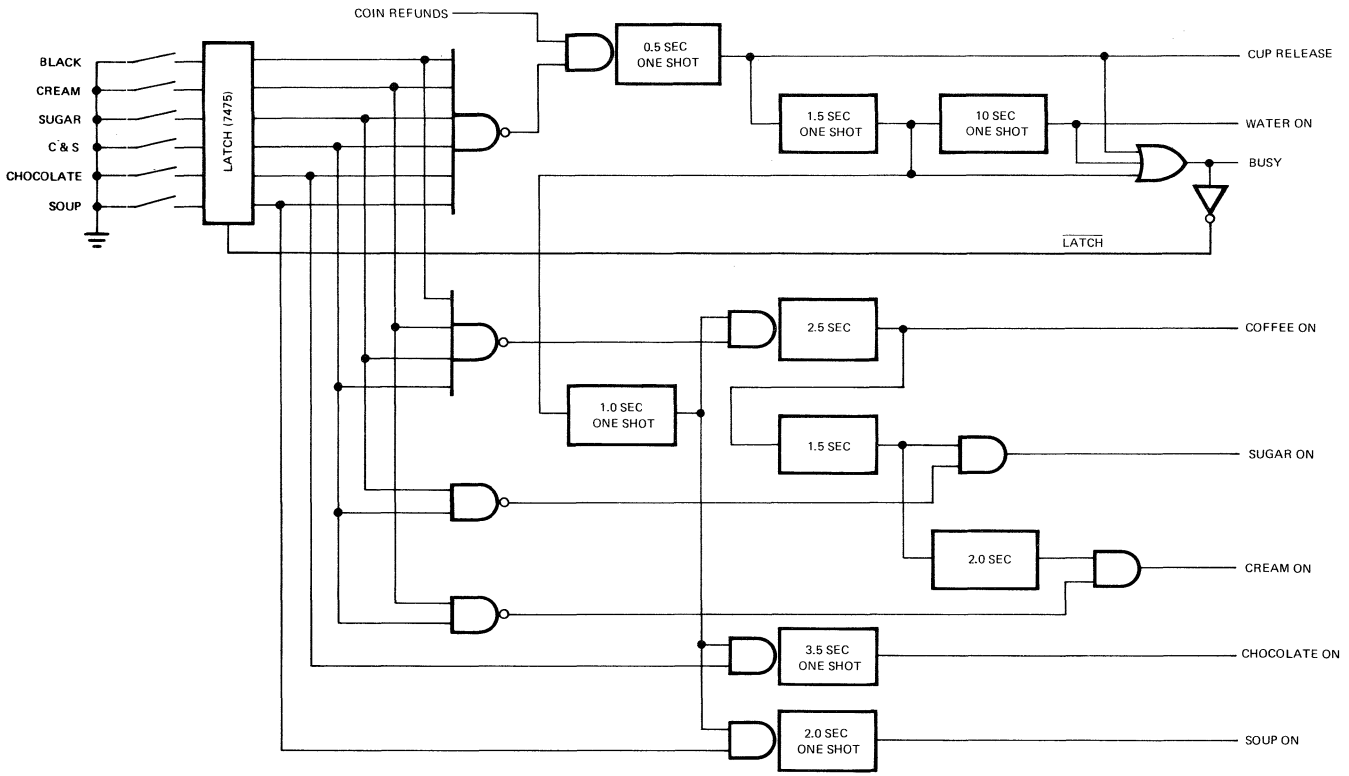


Figure 3. Coffee Machine Sequencer: Random Logic.

of this approach is that it results in a design with a reasonable part count and may closely parallel that of a previous design based on electro–mechanical components, such as relays and timers.There are several disadvantages with this design approach, however. The first disadvantage is that it is a unique design. The sequence controller for a soft drink machine, for instance, will be similar but different. A second, related disadvantage is that a redesign of the control logic may be required if the control sequence must be changed to accommodate different coffee machine hardware, such as using a different type of hot water valve. It involves, in any case, an evaluation of the effect of the sequence change upon the control logic to determine whether the design will have to be modified or redone. These two problem areas expand with the complexity of the sequence control problem. In the random logic design approach, the totality of the design is contained in the connection pattern of the integrated circuits, and the number of connections possible is approximately proportional to the square of the number of integrated circuits. This would indicate that the design complexity, probability of error, and probable number of design changes should also increase at about the same rate.

Microprogram techniques using counters and P/ROMs attack the disadvantages of the random logic approach as described above. The combination of a counter and a P/ROM can generate a single sequence, such as the black coffee sequence for a coffee machine, as shown in Figure 4. The contents of the P/ROM, which is also the sequence chart, is shown in Figure 5. The counter shown in Figure 4 is a binary counter and the P/ROM serves as a programmable decoder. The P/ROM decodes each count value and activates the corresponding output lines as determined by the P/ROM contents or program. The counter is started at zero and steps to a maximum count of 31 in this case. The counter is incremented by pulses from a 2Hz Oscillator. This allows sequences of up to 16 seconds with a resolution of ½ second. This counter and P/ROM combination is directly analogous to an electro-mechanical cam-and-timer type sequence generator with a revolution time of 16 seconds and a programmable cam resolution of 1/32 of a circle or approximately 11 degrees. Notice, however, that the choice of a 5 bit binary counter allowing 32 possible counts, and the corresponding 32 word P/ROM, is arbitrary. It is equally practical to use an 8 bit counter and a 256 word P/ROM. This would allow generation of sequences up to 128 seconds long with a half second resolution. The sequencer shown in Figure 4 creates output signals according to the pattern shown in Figure 5. Figure 5 shows the contents of each of the 32 locations of the P/ROM. The 5 bit binary counter begins with a count value of zero and increments sequentially through a count value of 31. Each count value is decoded by the P/ROM and the corresponding output signals, as indicated in Figure 5 are generated.

The sequence generator shown in Figure 6 has the capability of eight individually selectable sequences. This is done by using a 256 word P/ROM and using the upper 3 bits of the P/ROM address to select one of eight possible thirty-two step sequences. If these 3 bits are 000, the 5 bit counter will step through the address sequence zero through 31. If these 3 bits are 001, the counter will step through 32 through 47, etc. We can apply this sequence

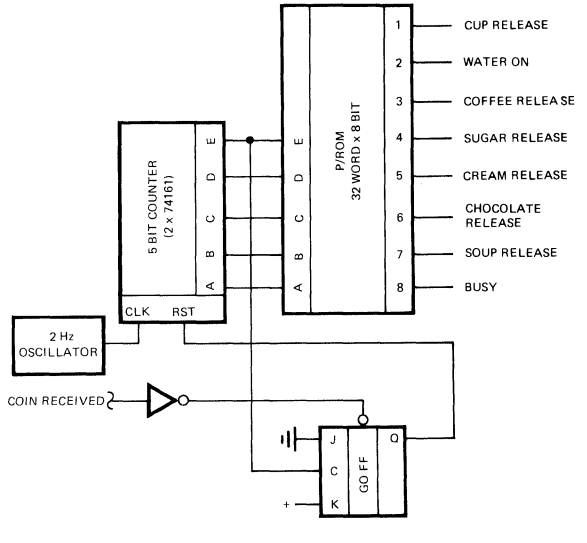


Figure 4. Simple Sequencer: Counter/ROM

P/ROM ADDRESS	CUP RELEASE	WATER ON	COFFEE RELEASE	SUGAR RELEASE	CREAM RELEASE	CHOCOLATE RELEASE	SOUP RELEASE	BUSY LIGHT	COMMENTS
0									"REST" ADDRESS
1	X							X	
2								X	
3								X	
4								X	
5		X						X	
6		X						X	
7		X	X					X	
8		X	X					X	
9		X	X					X	
10		X	X					X	
11		X	X					X	
12		X						X	
13		X						X	
14		X						X	
15		X						X	
16		X						X	
17		X						X	
18		X						X	
19		X						X	
20		X						X	
21		X						X	
22		X						X	
23		X						X	
24		X						X	
25								X	
26								X	
27								X	
28								X	
29								X	
30								X	
31								X	

Figure 5. Counter/ROM Sequence Chart (Black Coffee).

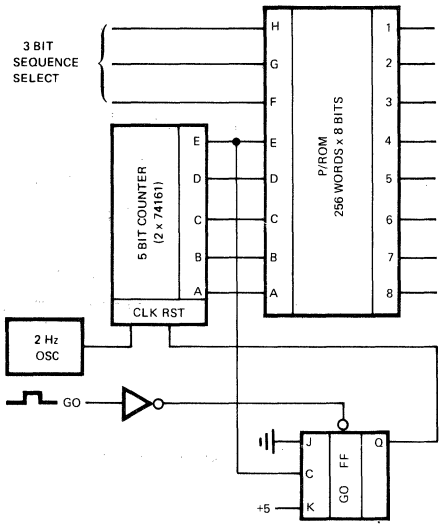


Figure 6. 8 Sequence Controller.

generator to our coffee machine problem by adding some circuitry as shown in Figure 7. Figure 7 shows the six push buttons, a register for holding the button status between the time it was pressed and the end of a sequence, and an encoder. The encoder converts the signal from each push button into a 3 bit binary number which is applied to the most significant 3 bits of the P/ROM. Push buttons 1 through 6 will generate binary codes 0 through 5, respectively. The 74148 encoder used performs this conversion as well as indicating whether or not any button is active. This activity output is used in conjunction with the output of a flip-flop which indicates a coin has been deposited and the button has been pushed. Once these two events have occurred, the sequence counter will step through the appropriate sequence locations in the P/ROM as shown in Figure 8. When the selected sequence is ended, the BUSY P/ROM output bits are used to clear the coin flip-flop, restoring the system to the initial conditions for the next cup.

We have now built a sequence controller, using 9 chips, which is capable of 8 selectable sequences of up to 32 steps each. Also, any and all sequences may be changed by modifying the contents of the P/ROM, a single chip, without any rewiring or other modifications to the hardware.

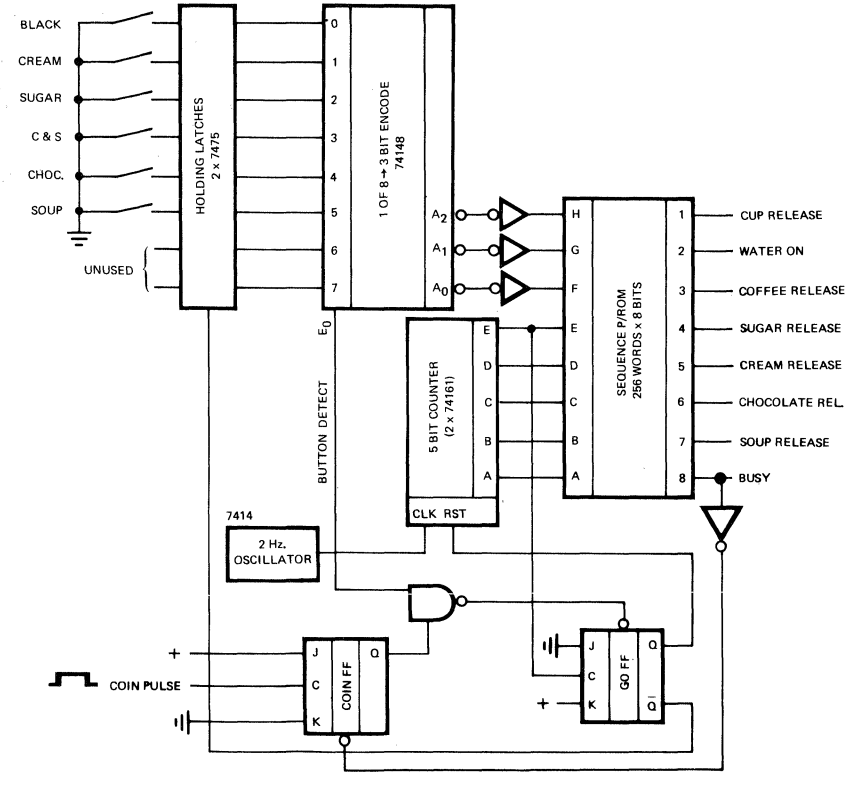


Figure 7. Coffee Machine ROM/Counter Sequencer.

P/ROM ADDRESS		CUP RELEASE	WATER ON	COFFEE	SUGAR	CREAM	CHOCOLATE	SOUP	BUSY	COMMENTS
32N +	0									"REST" ADDRESS
"	1	X							X	CUP RELEASE SEQUENCE
"	2								X	
"	3								X	
"	4								X	
"	5		X						X	
"	6		X						X	
"	7		X	A			D	E	X	
"	8		X	A			D	E	X	
"	9		X	A			D	E	X	
"	10		X	A			D	E	X	
"	11		X	A			D		X	
"	12		X		B		D		X	
"	13		X		B		D		X	
"	14		X		B				X	
"	15		X			C			X	
"	16		X			C			X	
"	17		X			C			X	
"	18		X			C			X	
"	19		X						X	
"	20		X						X	
"	21		X						X	
"	22		X						X	
"	23		X						X	
"	24		X						X	
"	25								X	
"	26								X	
"	27								X	
"	28								X	
"	29								X	
"	30								X	
32N +	31								X	

X = ALL SEQUENCES
A = COFFEE SEQUENCES:
N = 0, 1, 2, 3
B = SUGAR SEQUENCES
N = 1, 3
C = CREAM SEQUENCES
N = 2, 3
D = CHOCOLATE SEQUENCES
N = 4
E = SOUP SEQUENCE
N = 5

N = 0: BLACK COFFEE
N = 1: COFFEE & SUGAR
N = 2: COFFEE & CREAM
N = 3: COFFEE & C & S
N = 4: CHOCOLATE
N = 5: SOUP

Figure 8. Combined ROM/Counter Sequence Chart.

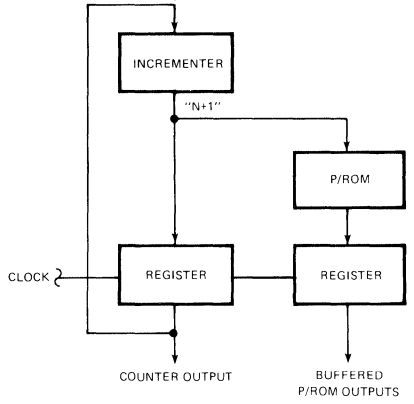


Figure 9. Pipelined Counter /ROM System.

Although in our coffee machine example the sequencer is stepped along at a rate of 2 hertz, the circuit is practical at rates to several megahertz. At rates above one megahertz, the decoding time of the P/ROM becomes significant. This can be avoided by using a modification of the original counter and P/ROM technique. The modified technique has various names, such as pipelining and look-ahead. This method puts a register at the P/ROM outputs to hold the output values, while the P/ROM itself is decoding the next set of outputs. Figure 9 shows a block diagram of such a system. In this system, a counter is created using an incrementer and a register. This incrementer and register combination is characteristic of the internal design of synchronous counter chips, such as the 74163. In Figure 9 these two functions have been separated to grant access to the path between the incrementer and the register. The incrementer output creates the next count value and applies it to the count register input. The incrementer output is also applied to the address input of the sequence P/ROMs. The sequence P/ROMs decode this next count value and apply their decoded outputs to another register. When a clock pulse is applied, the counter will increment since it will be loaded with the current count value plus one. Likewise, the P/ROM buffer register will be loaded immediately with the decoded P/ROM data for that state. The advantage of this approach is that the decoded P/ROM data is available almost immediately after the clock pulse, as opposed to 60 to 80 nanoseconds later, as determined by propagation delay to the P/ROMs. This is shown in the timing diagram of Figure 10. An additional feature of the pipelined approach is that the outputs remain stable from one clock period to the next. In the simpler counter and P/ROM system, the P/ROM outputs are undefined for a period of typically 60 to 80 nanoseconds after the clock pulse. Not only are they undefined during this interval, but they may change rapidly and create positive or negative pulses. This is due to changes occurring in the internal decode logic of the P/ROM.

The Am2909 is designed to be used in pipelined systems. The 2909 contains an incrementer and logic for generating the next P/ROM state. Figure 11 shows a 2909 based pipelined sequencer. Some of the features of the 2909, which will be discussed below, are not shown for the sake of clarity. Note that the sequencer in Figure 11 differs

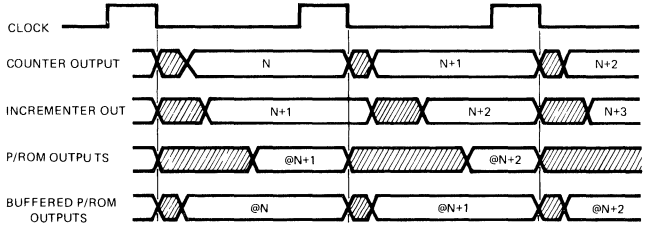


Figure 10. Pipelined Counter /ROM Timing Diagram.

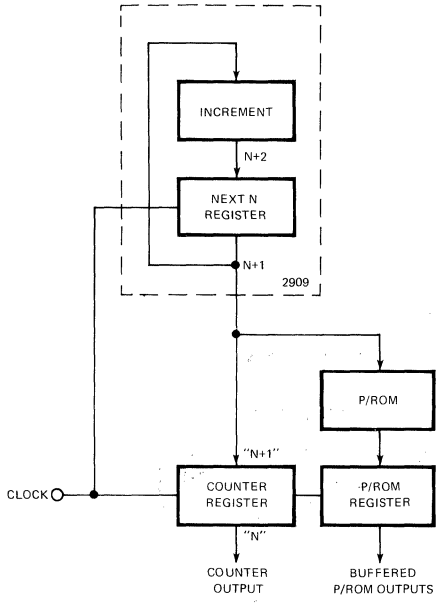


Figure 11. 2909 Pipelined System.

slightly from the sequencer shown in Figure 9. In the 2909, a register is placed after rather than before the incrementer. This register holds the value of the next P/ROM address, the decoded contents of which will be loaded into the P/ROM buffer register. The incrementer takes the 2909 outputs and increments them to form the next address plus one, to be loaded into the 2909 microprogram counter register. This arrangement provides high speed since the next address is available from this next address microprogram counter register almost immediately after the rise of the clock pulse. The inherently slower generation of the incremented value thus occurs between clock pulses. This is, in a sense, further pipelining of the system. Because of this arrangement, microprogram step times as low as 100 nanoseconds are possible.

COMPLEX PROBLEMS AND SOLUTIONS

The simple sequencers described above are useful and practical for small and medium sized sequence control systems. As the system's size expands, in terms of number of selectable sequences, and/or number of steps per sequence, the P/ROM memory required expands proportionally. As the P/ROM memory size, and therefore cost, starts becoming significant in our design, we naturally look for methods of reducing the size of memory required. There is one fundamental technique with several implementation methods for reducing memory size, and this is to identify and eliminate redundant sequences.

There are two general methods of identifying and eliminating redundant sequences. One method is repetition, where a single step or group of steps is repeated a number of times. In our sequence list of Figure 8, we can see several areas in each sequence where the outputs do not change from one P/ROM address to the next. These redundant states can be reduced to a single state with a repeat counter to cause those outputs to remain unchanged until they have been repeated the appropriate number of clock steps. This same technique can be applied in cases where a number of steps are repeated several times. The second general method is to identify common subsequences where a group of identical steps are used in several different sequences or even several times within the same sequence. A sub-sequence, called a subroutine, typically performs some commonly used function. An example is the cup release sequence shown in the Chart in Figure 8.

A wide variety of ways exist for implementing the repeat function. A simple method of implementing the repeat function for single P/ROM states or micro-instructions is shown in Figure 12. In this figure we have added a synchronous counter, a 74163 in this case, which is loaded from the pipeline P/ROMs at the same time the P/ROM buffer, or micro-instruction register, is loaded. This counter has an output which detects when the 4 bits of the counter are all ones. This output is used to gate the clock pulse to the sequencer control system, including the 2909 microprogram counter register and the micro-instruction register. This signal is also used to enable the load enable input to the counter itself. If the counter is loaded with all ones for every clock pulse, the sequencer will operate as before, with the 2909 micro-program counter register and the micro-instruction register being loaded on every clock pulse. If the counter is loaded with other than all ones, for instance with all zeros, the clock for the rest of the system will be disabled until the counter reaches all ones, in this case after 15 counts. This means that the micro-instruction register outputs will remain unchanged for a total of 16 counts, 15 counts corresponding to the clock being disabled plus one count during which the clock was enabled. In order to execute a micro-instruction in N times, one simply loads the repeat counter with a value of 16 minus N.

It may be desirable to repeat a group of several instructions. In this case, we will require somewhat more complicated logic. In order to perform this repeat, we must go back to the first instruction in the repeated group. The logic to perform this is shown in Figure 13. A sequence chart example is shown in Figure 14. In order to repeat a group of instructions, we must be able to conditionally go from the last step of the group sequence to the first step of the group sequence. The hardware in Figure 13 does this. An added P/ROM, buffer register, and a multiplexer in the 2909 provides a method of selecting a next address different from the current address plus one. This next address will typically be the starting address of our repetitive sequence, the repeat address. Our repeat counter is now used to control this multiplexer. When we reach the last step in the repetitive sequence, the repeat counter all ones detect output is used to control 2909 multiplexer selection. If the repeat counter detect output is zero, then the multiplexer selects the repeat address from the P/ROM buffer register. If the repeat counter detect output is one, then the current address plus one is selected, which is in the 2909 microprogram counter register.

Note that the repeat counter is incremented only when it is used to control the multiplexer. In this way it will be incremented once per repetition of the group, or once per loop, rather than once per clock pulse. This circuit can be

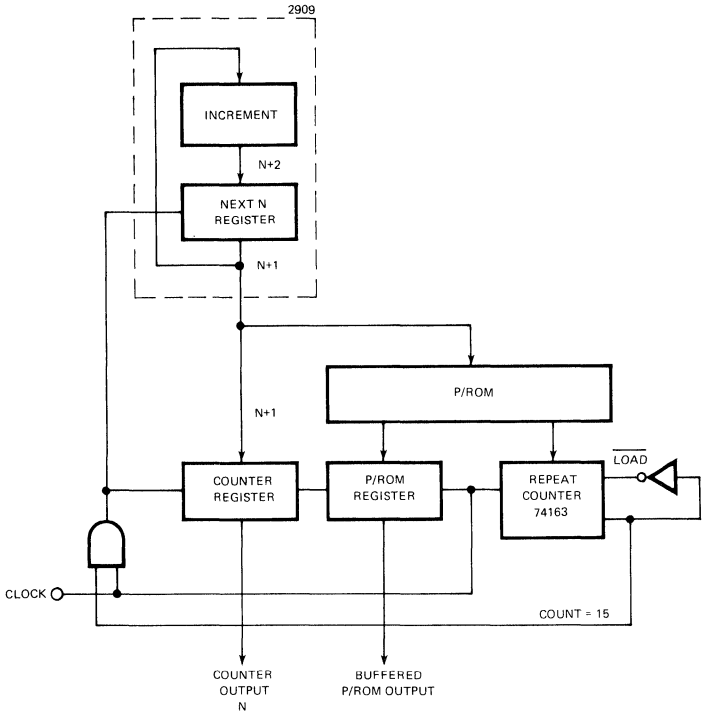


Figure 12. Single Instruction Repeat.

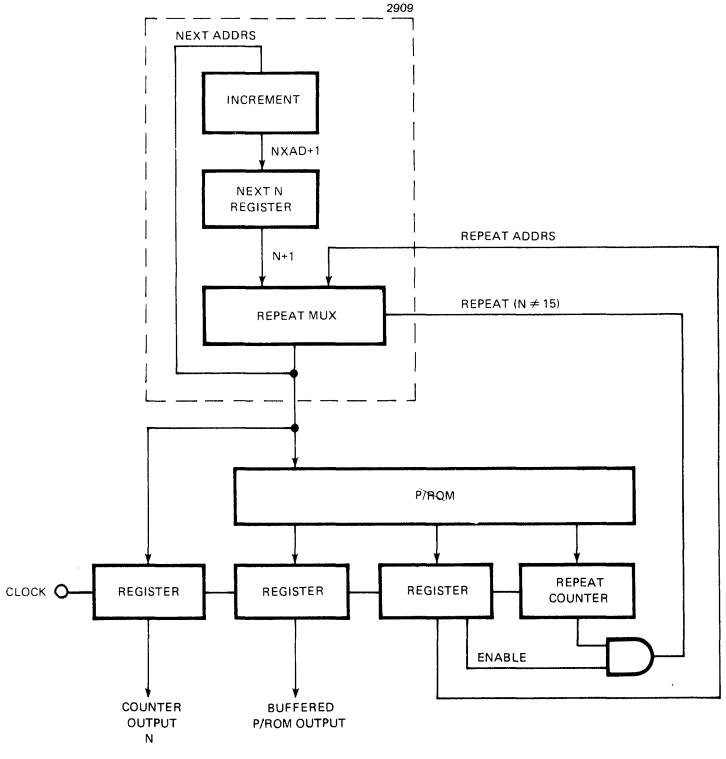


Figure 13. Group Repeat Logic.

CURRENT COUNTER VALUE	NEXT COUNTER VALUE	ACTIVITY
23	24	
24	25	LOAD REPEAT COUNTER
25	26	1st STEP OF REPEAT SEQUENCE INCREMENT REPEAT COUNTER
26	27	2nd STEP
27	28	3rd STEP, ETC.
28	29/26	4th STEP: GO TO 26 IF REPEAT
29	30	—— (CONTINUE)
30	31	——

Figure 14. Repeat Sequence Example.

used to implement a single micro-instruction repeat function by simply causing the address P/ROM output to be equal to the address of the current micro-instruction. Note also that we no longer use the repeat counter every cycle. It can therefore be loaded from another source within the overall system at an arbitrary time. In a computer control unit context, our repeat counter might be loaded with a shift count from the instruction register at some time before the shifting operation was actually performed.

The second method of eliminating redundant coding in the P/ROM memory is by using sub-sequences or sub-routines. In this case, a sub-sequence exists which is used in a variety of different sequences in the P/ROM memory. For example, the cup release sub-sequence in our coffee vending machine example is used in all sequences. Instead of having six different sets of codes doing the same function, one set of code is used plus a method to get to the code and return to the original sequence when the sub-sequence is complete. With the addition of the address generation P/ROM shown in Figure 13, we now have a method of going from a current location to some entirely different location within the memory. To implement sub-sequences, we need a method of returning to the next location in our original sequence. To be specific, we wish the next P/ROM address to be the first address in our commonly used sub-sequence, or subroutine, and at the end of that subroutine we wish to return to our current address plus one. In order to do this we must be able to (1) Select a desired subroutine address as the next P/ROM value, and (2) Save the current P/ROM address value plus one as the next P/ROM value to be used upon completion of our subroutine. This can be done by using the logic of Figure 13, which allows us to select an arbitrary next P/ROM address value, plus the addition of a register to save our normal next address value, which is the current P/ROM address value plus one. The design of this subroutine logic shown in Figure 15 and its operation is shown in the sequence chart of Figure 16.

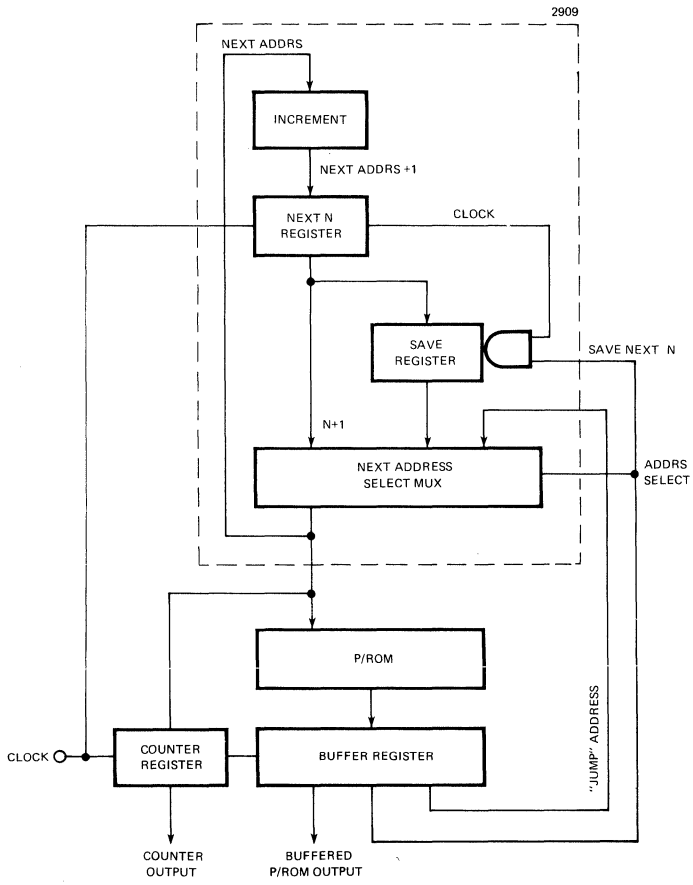


Figure 15. Next Address Save Logic.

CURRENT COUNTER VALUE	NEXT COUNTER VALUE	SAVE REGISTER CONTENTS	ACTIVITY
23	24	——	——
24	37	——	GO TO 37 AND SAVE RETURN
37	38	25	1st STEP OF SUBROUTINE
38	39	25	2nd STEP OF SUBROUTINE
39	40	25	3rd STEP OF SUBROUTINE
40	25	25	4th STEP OF SUBROUTINE AND RETURN (SELECT SAVE REG AS NEXT COUNTER VALUE)
25	26	25	CONTINUE
26	27	25	——
27	28	25	——

Figure 16. Subroutine Sequence Example.

The 2909 contains a save register. In fact, it is implemented as a Last In, First Out stack of 4 registers. This may be considered as a set of bi-directional shift registers which allow data to be shifted in or out according to the 2909 controls. These effective shift registers are 4 bits long. Having more than one save register allows one subroutine to use, or call, another subroutine. This process of calling a subroutine which in turn calls another subroutine, can be repeated up to 4 times in the 2909. At the completion of each subroutine, the last return value which was put into the save shift registers is used to set the next P/ROM address value. This Last-In-First-Out function is called a stack because it is conceptionally similar to a stack of plates. The current output of the 2909 LIFO stack corresponds to the last value shifted into the stack in a similar manner to a stack of plates, where the top-most plate on the stack corresponds to the last one placed there.

There exists another method of sub-sequence selection. In this case, the sequence selection register is decoded more than once. This is shown in Figure 17. Here we are assuming that the original command selection is stored in a register, and that this register has a P/ROM at its output which decodes its contents to produce a P/ROM address value corresponding to the selected sequence. In the above discussions, we have assumed that this command register (the push button register) is decoded once and the selected

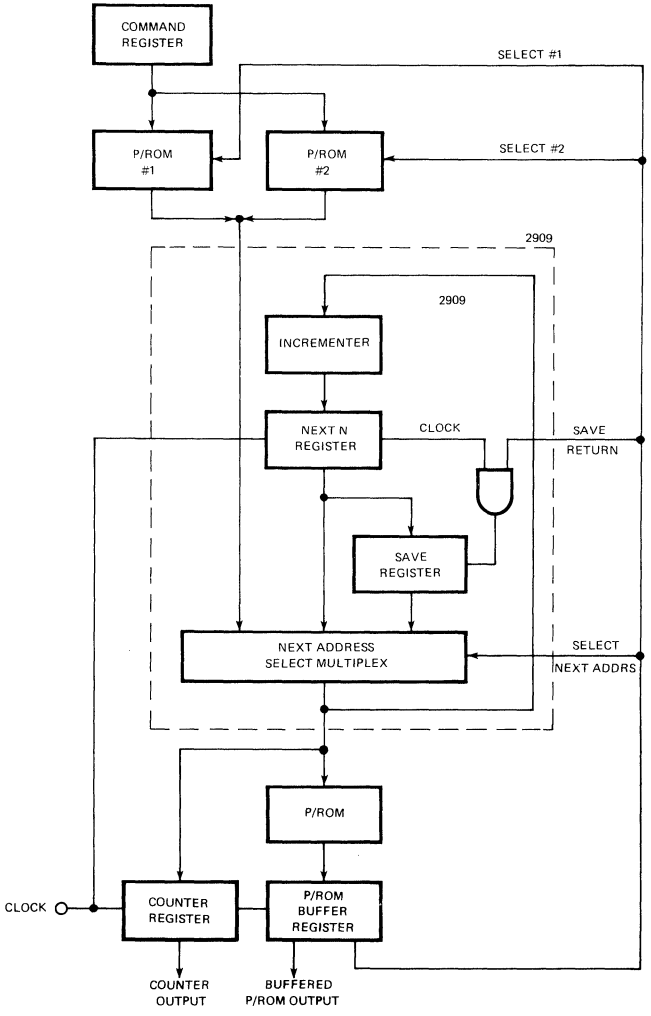


Figure 17. Multiple Decode Subsequence Select.

sequence runs through to completion. Another possibility is to use the same command register to select several sub-sequences rather than one main sequence. This means that our command register is decoded several times. The first time it is decoded, it selects the first sub-sequence. At the end of this sub-sequence, a second decode P/ROM is enabled which decodes the command register a second time. This selects a second sub-sequence, etc. In this manner, as many sub-sequences as desired may be selected by sequentially decoding this command register. This method has the advantage of not requiring a special set of P/ROM outputs for address generation. In some cases, it may save a micro-instruction step which would be required to generate a subroutine call.

A general purpose sequence control system using 2909's is shown in Figure 18. This is a semi-pipelined system. This means that part of the system is pipelined for high-speed functions which must have signals available at the beginning of the cycle and part of the system is not pipelined, meaning that the next P/ROM address is simply loaded into a register which is decoded by P/ROMs, the outputs of which are not needed until the middle or the end of the micro-instruction cycle. The timing diagram for this system is shown in Figure 19. Note that in this 2909 system we have included a repeat counter and a condition testing multiplexer which can select the repeat counter output or any of several other external signals to control the source of the next P/ROM address. These external signals are synchronized with the buffer register to insure that their outputs will remain stable during the micro-cycle. This allows the look-ahead P/ROMs sufficient time for their outputs to stabilize and drive the inputs to the micro-instruction register.

Now that our general purpose sequence controller has been designed, all that remains is to determine the number of high-speed, pipelined P/ROM outputs and lower-speed, non-pipelined P/ROM outputs required by our particular application. Also, we must determine the number and source of our condition control inputs. Last of all, we must create the pattern to be placed into our control

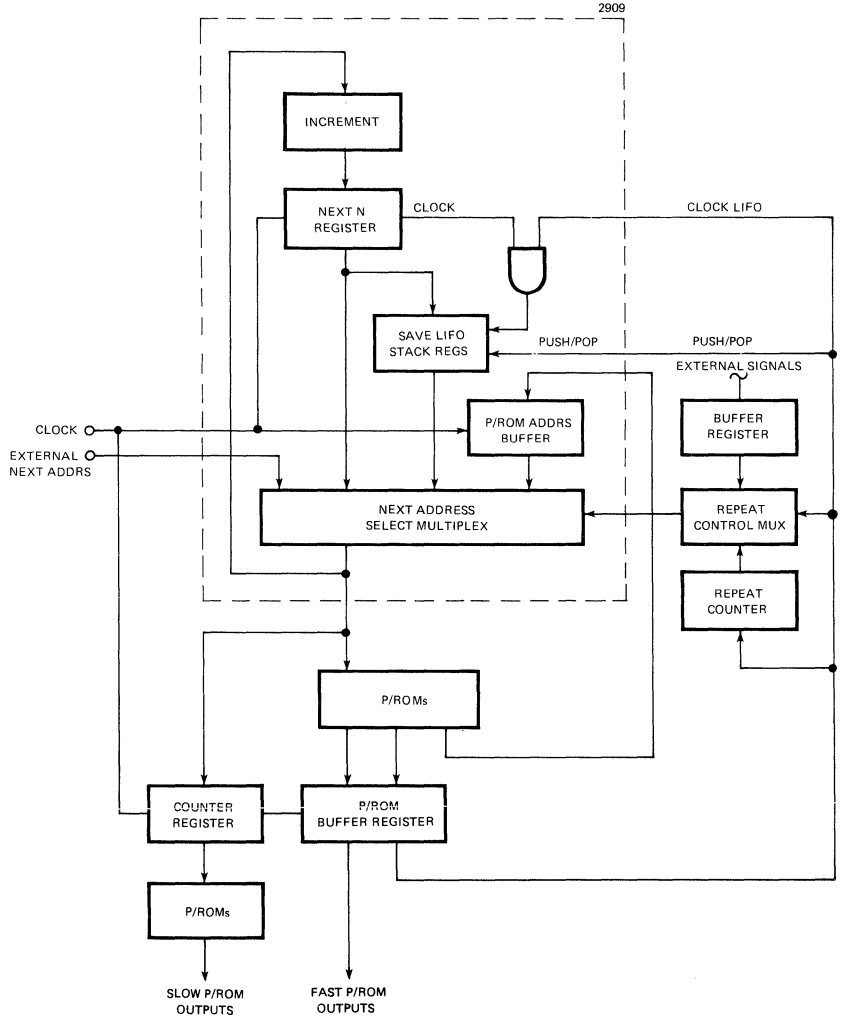


Figure 18. General Purpose 2909 Sequencer.

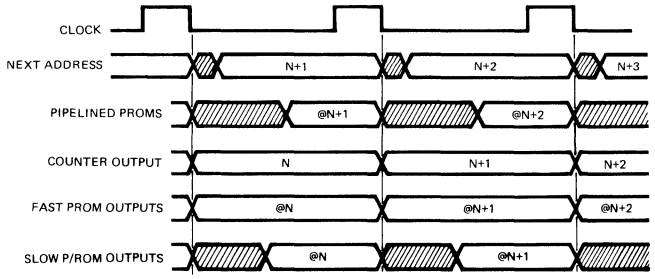


Figure 19. 2909 Sequencer Timing Diagram.

P/ROMs. All three of these tasks are part of the system design for a particular sequence control system. The last, however, can be supported by the RAYASM micro-assembler which is designed to simplify the generation of P/ROM patterns and the corresponding P/ROM programming tapes.

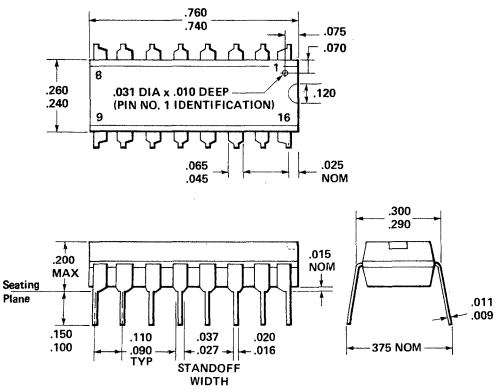
These two methods of sub-sequence generation, subroutine call and multiple command decode, may both be used within a given system. The method of subroutine call is the most general and can be used to create very long effective sequences. It is useful in medium and large systems. The method of multiple command decode has the advantage of eliminating the subroutine call micro-instructions and their corresponding execution time. It is useful in systems which have a large number of short sequences where execution time is important. The subsequences are typically few and short in computer control units since this provides not only fast instruction execution but also minimizes interrupt and DMA latency times. In many computer control units, interrupt and DMA activities are allowed to occur only between instructions. This means that the waiting period, or latency time, between an interrupt or DMA request in the beginning of the micro-program sequence which services that request can be long as the execution time of the longest instruction in the instruction set. For this reason, the multiple decode method is often used in CCU's, since it is desirable and sometimes necessary in these types of systems to keep the instruction execution sequences for all instructions below some maximum figure.

PACKAGING INFORMATION

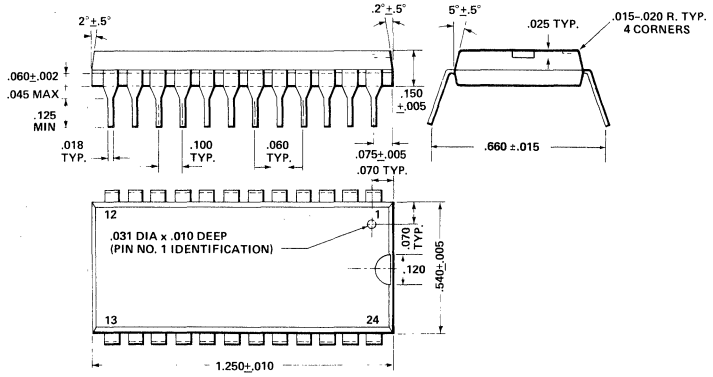
These drawings are preliminary and subject to change when the final product is complete.

DUAL IN-LINE PLASTIC

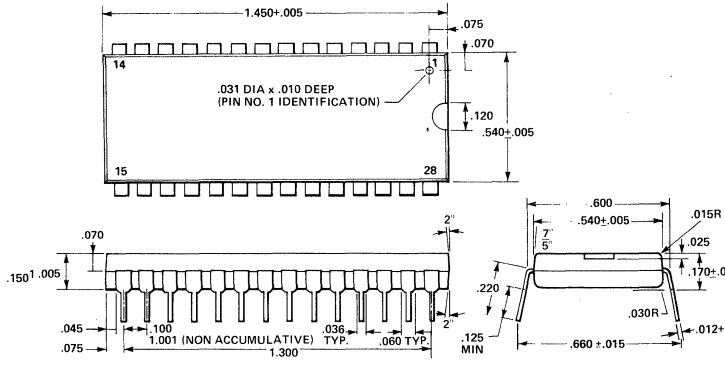
16-Pin Plastic DIP
BM/MB



24-Pin Plastic DIP
PU

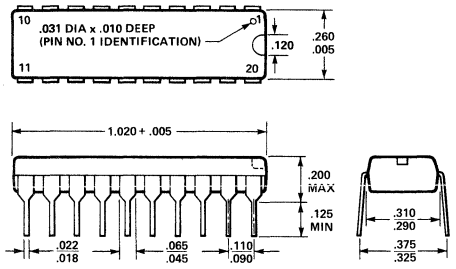


28-Pin Plastic DIP
PV

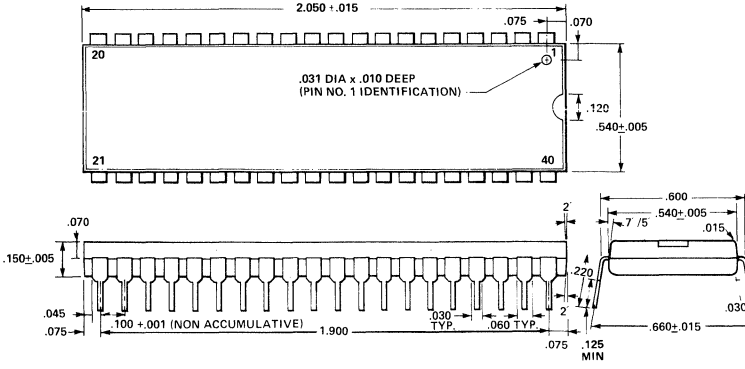


NOTES:
Board-drilling dimensions should equal your practice for .020 inch diameter lead
The .037/.027 dimension does not apply to the corner leads.

20-Pin Plastic DIP
PS



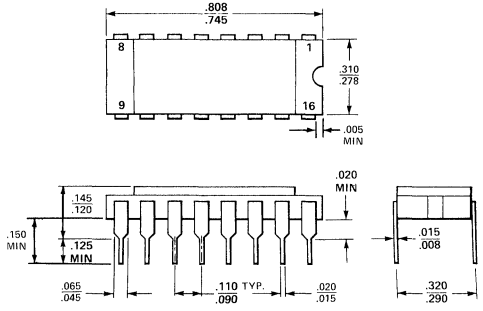
40-Pin Plastic DIP
PZ



RAYTHEON

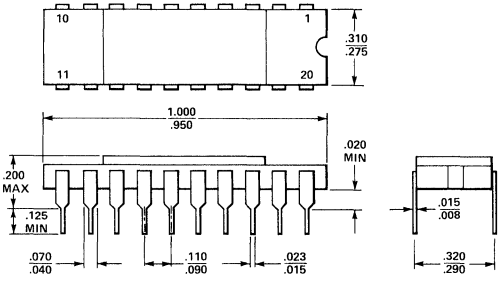
DUAL IN-LINE CERAMIC
SIDE BRAZED

16-Pin Ceramic
Side Brazed
ML

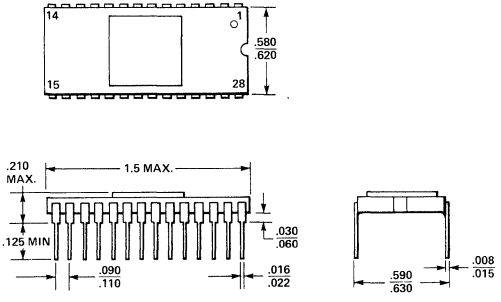


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar

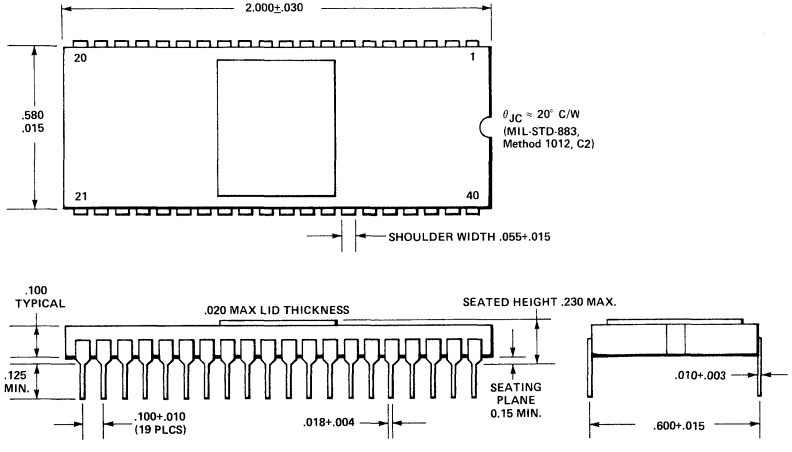
20-Pin Ceramic
Side Brazed
MS



28-Pin Ceramic
Side Brazed
MV

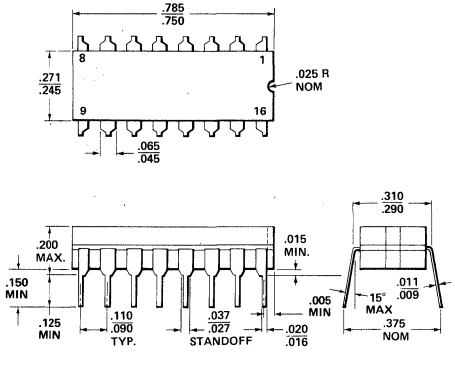


40-Pin Ceramic
Side Brazed
MZ



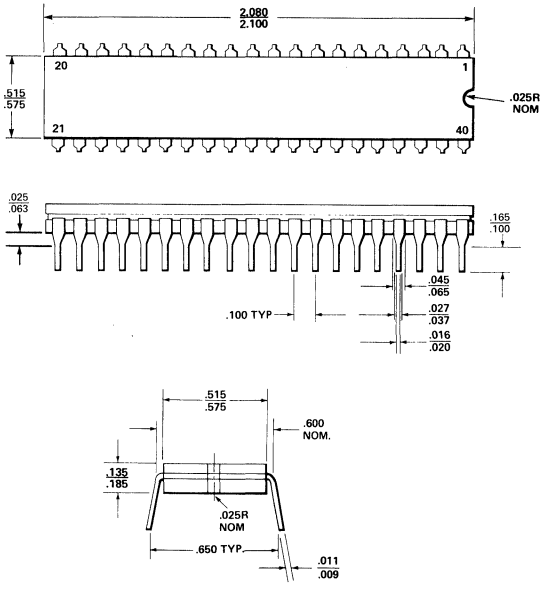
DUAL IN-LINE CERAMIC CERDIP

16-Pin CERDIP DD

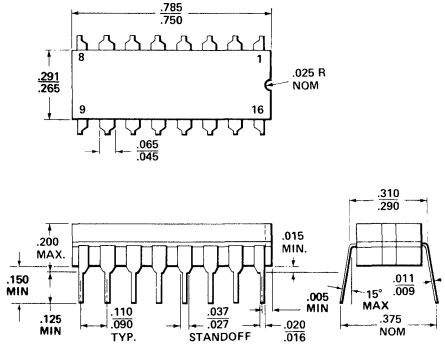


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated alloy 42
*The .037/.027 dimension does not apply to the corner leads

40-Pin CERDIP DZ

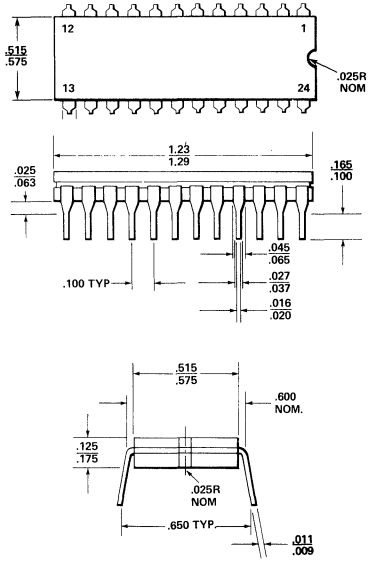


16-Pin CERDIP DM



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated alloy 42
*The .037/.027 dimension does not apply to the corner leads

24-Pin CERDIP R



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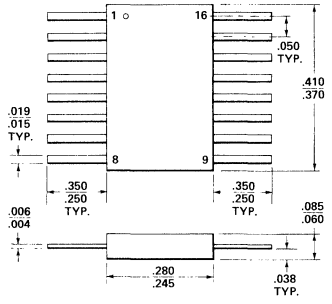
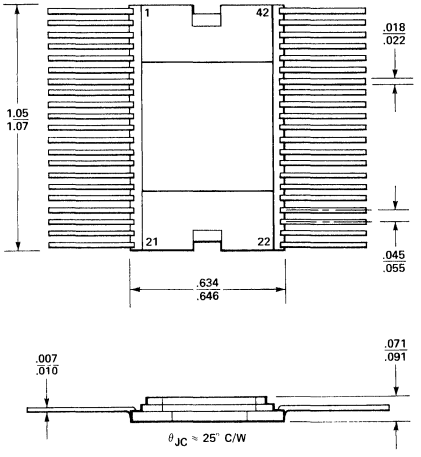
FLAT PACKAGES

16-Pin CERPAK
CL

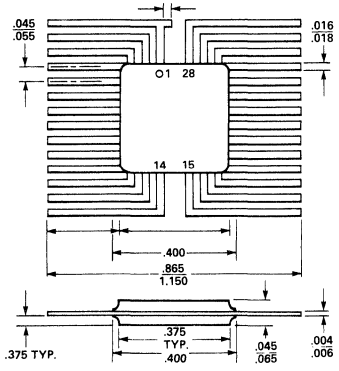


NOTES:
All dimensions in inches
Leads are tin-plated alloy 42

42-Pin Metal
F2



28-Pin Metal
FV



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