Technical Series IC-40
Suggested Price $2.00

RCA linear integrated circuit fundamentals

- design
- application

Radio Corporation of America
Electronic Components and Devices, Harrison, N. J.

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7/66
Printed in U.S.A.

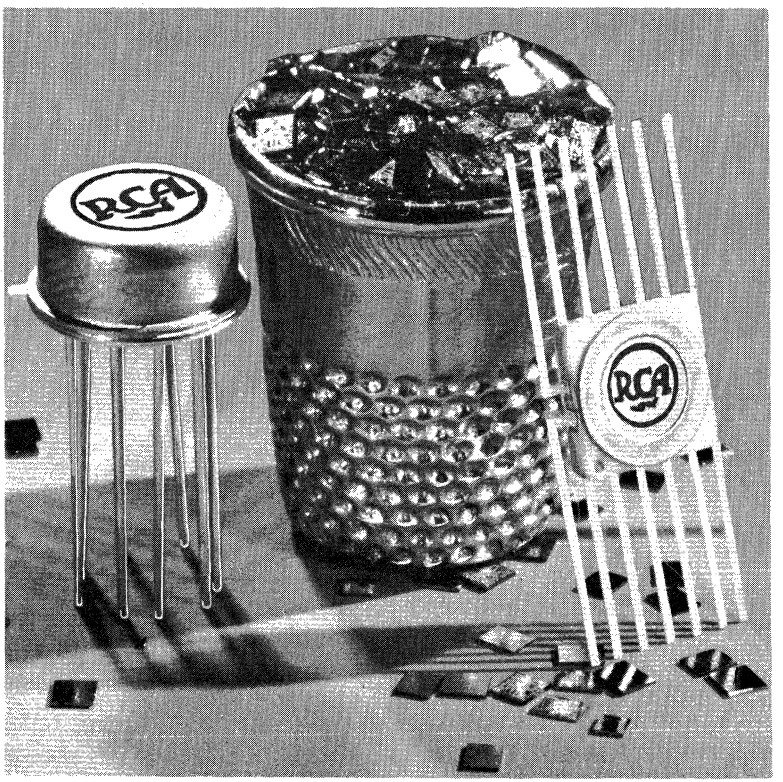
RCA linear integrated circuit fundamentals

This Manual has been prepared to provide an understanding of the basic principles involved in the design and application of linear integrated circuits. It may be used as a guide by circuit and system designers in determining optimum design specifications with regard to integrated-circuit capabilities and system requirements. Effects of the silicon monolithic fabrication process on circuit design are described, and design equations and performance criteria are derived for basic integrated-circuit configurations. Schematic diagrams, operating characteristics, and performance data are included for a broad family of multiple-function RCA silicon integrated circuits that can be adapted for use in a variety of linear applications.

Acknowledgment is given to **M. E. Malchow** and his staff for the design information on differential and operational amplifiers and for their technical guidance and review of other material in the Manual. Many other people in RCA are also thanked for their valuable contributions to this new book.

RADIO CORPORATION OF AMERICA
Electronic Components and Devices Harrison, N.J.

RCA linear integrated circuits



Thimble holds tiny integrated-circuit wafers to be packaged in TO-5 style case (shown at left) or in flat pack (shown at right).

General Design Considerations for Linear Integrated Circuits

THE design of linear circuits involves the selection and interconnection of an optimum combination of active and passive components to accomplish a signal-processing function with maximum efficiency and minimum cost. This general rule is valid whether the components are conventional ones fabricated separately by a variety of processes or integrated components formed simultaneously by a single technology. The new design considerations introduced by the advent of integrated-circuit technology arise not from any differences in the fundamental electronic properties of the components individually, but from the technical and economic implications of simultaneous fabrication and interconnection. This section describes the technology used for the fabrication of integrated circuits, and discusses the aspects that introduce factors not present when discrete components are used and their implications with regard to the design of linear circuits.

INTEGRATED-CIRCUIT FABRICATION

The fundamental requirement of an integrated circuit is that components be processed simultaneously from common materials. A variety of technologies can be used to satisfy this requirement. If a circuit function can be represented solely by linear reciprocal networks consisting of resistive and capacitive elements, any one of several thin-film technologies using such materials as tantalum, nichrome, or tin oxide can be used effectively. The use of more sophisticated thin-film techniques makes it possible to form active as well as passive components. A cadmium sulfide technology developed by RCA is capable of fabricating both field-effect transistors and passive components on a common substrate.

The technology presently used for achieving circuit integration, however, is based not on thin-film approaches, but on the silicon planar technology developed for transistors. This technology has become dominant because of its ability to provide higher-quality active devices than any competing technology.

The basic steps of the silicon process are shown in Figs. 1 through 4. The starting material is a uniform single crystal of n-type or p-type silicon, as shown in Fig. 1. Diffusion processing techniques permit the introduction of impurities to desired depths and widths in the starting material. Vertical penetration of the impurities is controlled by the diffusion temperature and time, and lateral control of the diffusions is made possible by combination of the masking properties of silicon dioxide with photochemical techniques.

When localized n-type regions are diffused into p-type starting material, as shown in Fig. 2, isolated circuit nodes are achieved.

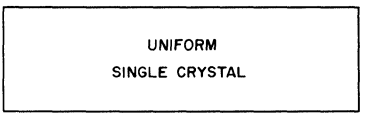


Fig. 1 — Silicon wafer used as starting material for an integrated circuit.

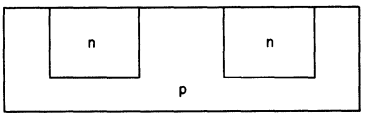


Fig. 2 — Diffusion of n-type areas to provide isolated circuit nodes.

The diodes formed by the p-type substrate and the n-type nodes accomplish electrical isolation between the nodes. Diffusion of additional p-type and n-type regions forms transistors, as shown in Fig. 3. The silicon wafer is then coated with an insulating oxide layer, and the oxide is opened selectively to permit metallization and interconnection, as shown in Fig. 4. When resistors are required, the n-type emitter diffusion is omitted and two ohmic

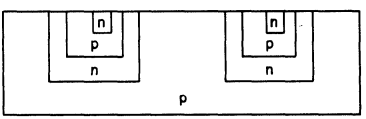


Fig. 3 — Diffusion of additional p-type and n-type regions to form transistors.

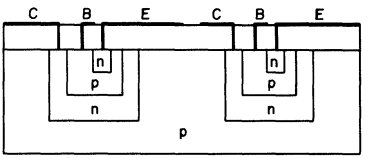


Fig. 4 — Addition of metallized contacts to transistor elements.

contacts are made to a p-type region formed simultaneously with the base diffusion, as shown in Fig. 5. When capacitors are required, the oxide itself is used as a dielectric, as shown in Fig. 6.

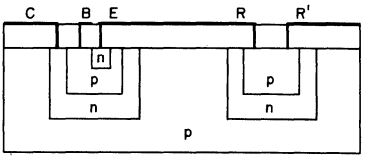


Fig. 5 — Connection of contacts to p-type region to form integrated resistor.

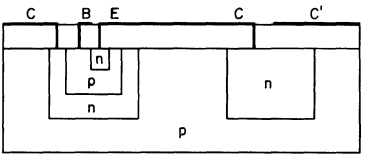


Fig. 6 — Use of oxide as a dielectric to form integrated capacitor.

Fig. 7 shows the combination of the three types of elements on a single wafer.

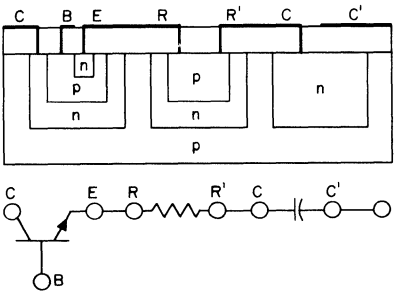


Fig. 7 — Completed silicon chip containing transistor, resistor, and capacitor.

COMPARISON OF DISCRETE AND INTEGRATED COMPONENTS

Because the basic fabrication process for integrated circuits is almost identical with that used to fabricate transistors, transistors formed by this technology are similar to discrete units. The major difference between discrete and integrated transistors is the extra capacitance associated with the substrate isolation diode.

Integrated resistors, however, are significantly different from discrete versions. Discrete resistors are normally made in standard form factors, and different values are obtained by variations in the

resistivity of the material. In integrated circuits, the resistivity of the material cannot be varied to obtain different resistance values because it is determined by the optimum value required for the transistor base diffusion. The value of the resistor then depends primarily on its geometry. The resistor value R is determined by the product of its diffusion-determined sheet resistance R_s and the ratio of its length l to its width w (i.e., $R = R_s \times l/w$). As a result, large resistors are long and narrow and small resistors are short and squat.

The value of an integrated capacitor C is equal to the product of its area A and the ratio of the dielectric constant E of the diffused material and the oxide thickness d (i.e., $C = A \times E/d$). Because d is kept constant, capacitor values vary directly with area.

COST FACTORS

Most of the cost of fabricating a monolithic silicon circuit is incurred in processing the silicon wafers through the various epitaxial, diffusion, and photochemistry operations. Because these costs are the same for any circuit wafer, the smaller the circuit, the more circuits that can be obtained per wafer and the lower the cost per circuit. Therefore, area minimization is an important consideration. The relative area requirements of different integrated components are as follows:

Component	*Relative Area*
Transistor	1
1000-ohm Resistor	2
10-pF Capacitor	3

These ratios are approximations that will be continually modified as technological advances are made. However, the basic relationships (that transistors use less area than resistors, which in turn are more compact than capacitors) will persist. Because area determines cost, these relationships indicate that economical integrated-circuit design requires minimization of the number of passive components. The requirement is exactly the reverse of the economic design rule for discrete-component circuits.

TEMPERATURE CONSIDERATIONS

One undesirable aspect of semiconductor resistors is their relatively large variation with temperature. This temperature dependence makes it difficult to achieve close tolerances on absolute

values of resistors. However, the ratios of integrated-circuit resistors can be closely controlled by control of the geometry of photolithographic masks used in the fabrication process. As a result, it is desirable that integrated-circuit design be made dependent on ratios rather than absolute values of resistors.

Integrated transistors on the same circuit chip have a number of advantages over discrete units as a result of their proximity. Adjacent transistors receive almost identical processing and thus are closely matched in characteristics. Because of the close spacing, minimum temperature differences occur between components and this close match is maintained over a wide operating range. In addition, integrated circuits can contain many more transistors per given area than discrete components. In a typical high-frequency silicon transistor, less than 10 per cent of the wafer area is used by the active device. The remaining area serves as a support for the bonding pads and as a "handle" for the transistor. Six integrated transistors in a circuit would use less silicon than the single discrete transistor shown in Fig. 8. Therefore, integrated-circuit

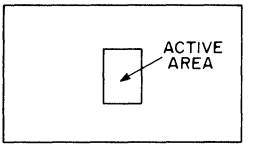


Fig. 8 — Discrete-transistor chip.

technology is most efficiently utilized when circuit designs are based on the use of a maximum number of matched active components.

BASIC DESIGN RULES

In summary, integrated-circuit technology offers the circuit designer a new approach to the synthesis of electronic functions. To use this approach most effectively, a designer should observe the following basic rules:

(a) maximize the number of active components,
(b) use resistor ratios rather than absolute values,
(c) take advantage of matched component parameters.

Basic Configuration — The Differential Amplifier

FIG. 9 shows the basic circuit configuration used for a broad line of multiple-function, all-monolithic-silicon integrated circuits designed for a wide variety of linear analog applications at frequencies from dc into the vhf region. The configuration is basically that of a balanced differential amplifier in which the currents to the emitter-coupled differential pair of transistors are supplied from a controlled source (i.e., a constant-current sink transistor). Temperature-compensating networks can be readily

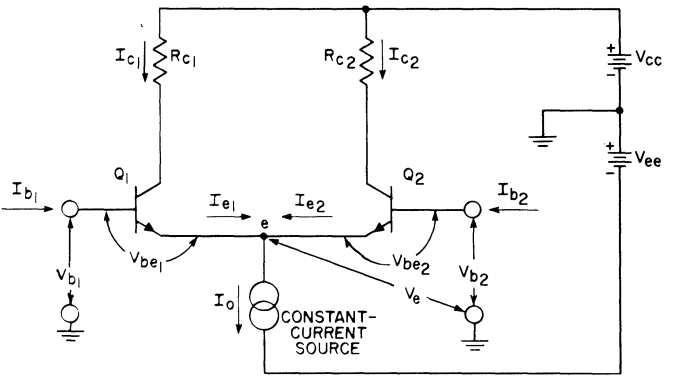


Fig. 9 — Schematic of the balanced differential amplifier used as the basic configuration for the linear integrated circuits.

incorporated as an integral part of the controlled-source circuit to assure that the gain, the dc operating point, and other important characteristics vary as required over the temperature range from −55°C to +125°C.

In the selection of the basic configuration for linear integrated circuits, the differential amplifier was chosen over other possible circuits (e.g., a feedback pair) for the following reasons:

1. Advantage can be taken of the exceptional balance between the differential-amplifier inputs that results from the inherent match in base-to-emitter voltage and in short-circuit current gain of two transistors which are processed in exactly the same way and are located very close to each other on the same silicon chip.
2. The differential-amplifier circuit requires a minimum number of capacitors.
3. The use of large resistors can usually be avoided, and the gain of the circuit can be made a function of resistance ratios rather than of actual resistance values.
4. The differential amplifier is much more versatile than other possible configurations. This circuit can provide linear amplification from dc through the audio and video frequencies into the vhf region, and may also be used for such functions as limiting, frequency multiplication, amplitude modulation, mixing, product detection, signal generation, gain control, squelch, and temperature compensation.

BASIC CHARACTERISTICS OF THE DIFFERENTIAL AMPLIFIER

In the differential-amplifier circuit shown in Fig. 9, the sum of the emitter currents of the differential pair of transistors Q_1 and Q_2 must be equal to the total amount of current (I_o) supplied to the constant-current sink, as shown by the application of Kirchoff's second law at node e:

$$I_{e1} + I_{e2} = I_o \tag{1}$$

The emitter-to-base voltages V_{be1} and V_{be2} of the emitter-coupled transistors Q_1 and Q_2 are expressed as follows:

$$V_{be1} = V_{b1} - V_e \tag{2}$$

$$V_{be2} = V_{b2} - V_e \tag{3}$$

where V_e is the voltage at the node e and V_{b1} and V_{b2} are defined as indicated in Fig. 9.

If the V_e term is eliminated in Eqs. (2) and (3), the following result is obtained:

$$V_{b1} - V_{b2} = V_{be1} - V_{be2} \tag{4}$$

This latter equation defines the differential input voltage for the differential amplifier.

Transfer Characteristics

The familiar equations for the current relationships in a transistor and for the voltage across the base-emitter diode are employed in the derivation of the transfer characteristics of the differential-amplifier circuit.

The basic transistor current relationships are expressed by the following equations which express the collector (I_c) and base (I_b) currents of transistors Q_1 and Q_2 in terms of their emitter current (I_e):

$$\begin{aligned} I_{c1} &= \alpha I_{e1} \\ I_{c2} &= \alpha I_{e2} \end{aligned} \tag{5}$$

$$\begin{aligned} I_{b1} &= (1 - \alpha)\, I_{c1} \\ I_{b2} &= (1 - \alpha)\, I_{e2} \end{aligned} \tag{6}$$

where alpha (α) is the fractional part of the emitter current that reaches the collector of the transistor. In this discussion, alpha is assumed to be the same for both transistors (Q_1 and Q_2) of the differential pair.

The base-emitter diode equation relates the base-to-emitter voltage (V_{be}) of a transistor to the emitter current (I_e) as follows:

$$I_e = I_s \left(\exp \frac{V_{be}}{h} - 1 \right) \tag{7}$$

where I_s is the saturation current of the transistor, and h is defined by the ratio KT/q where K is Boltzmann's constant, T is the temperature in degrees Kelvin, and q is the charge on an electron. At 300°K, a saturation current I_s in the order of 0.2×10^{-15} ampere is typical for some integrated-circuit transistors, and the factor h is approximately 26 millivolts.

For emitter currents of 1 nanoampere or more, the -1 term in the bracketed expression of Eq. (7) becomes insignificant, and the equation can be rewritten for the integrated-circuit transistors Q_1 and Q_2, respectively, as follows:

$$I_{e1} = I_{s1} \exp \frac{V_{be1}}{h} \tag{8}$$

$$I_{e2} = I_{s2} \exp \frac{V_{be2}}{h} \tag{9}$$

If the two transistors Q_1 and Q_2 are assumed to be identical, the following basic equalities can also be assumed:

$$\begin{aligned} I_{s1} &= I_{s2} = I_s \\ \alpha_1 &= \alpha_2 = \alpha \\ T_1 &= T_2 = T \end{aligned} \tag{10}$$

On the basis of the relationships expressed by Eqs. (4) through (10), Eq. (1) can be rewritten as follows:

$$\begin{aligned} I_o &= I_s \exp \frac{V_{be1}}{h} + I_s \exp \frac{V_{be2}}{h} \\ &= I_s \exp \frac{V_{be1}}{h} \left(1 + \exp \frac{V_{b2} - V_{b1}}{h}\right) \end{aligned} \tag{11}$$

Eqs. (8) and (9) can then be rewritten to express the emitter currents I_{e1} and I_{e2} in terms of the total source current I_o as follows:

$$I_{e1} = \frac{I_o}{1 + \exp \dfrac{V_{b2} - V_{b1}}{h}} \tag{12}$$

$$I_{e2} = \frac{I_o}{1 + \exp \dfrac{V_{b1} - V_{b2}}{h}} \tag{13}$$

The collector currents I_{c1} and I_{c2}, given by Eq. (5), may also be defined in terms of the current I_o, as follows:

$$I_{c1} = \frac{\alpha I_o}{1 + \exp \dfrac{V_{b2} - V_{b1}}{h}} \tag{14}$$

$$I_{c2} = \frac{\alpha I_o}{1 + \exp \dfrac{V_{b1} - V_{b2}}{h}} \tag{15}$$

The collector-current transfer curves defined by Eqs. (14) and (15) are shown in Fig. 10. In this figure, the abscissa represents the differential input voltage $V_{b1} - V_{b2}$ and is calibrated in units of the factor $h = KT/q$. The ordinate, which represents the collector current I_c, is calibrated in units of αI_o.

When V_{b1} is equal to V_{b2}, the two transistors Q_1 and Q_2 are balanced, and one-half the total current I_o flows through each transistor. This condition presents the usual operating point for an analog differential amplifier.

The transfer curves shown in Fig. 10 provide several important points of information about the differential amplifier:

1. The transfer characteristics are linear in a region about the operating point. For the curves shown (KT/q ≈ 26 millivolts), this linear region corresponds to an input-voltage swing of approximately 50 millivolts peak-to-peak.
2. The maximum slope of the curves, which occurs at the operating point, defines the effective transconductance of the differential amplifier.
3. The slope of the transfer curves (i.e., the transconductance) is dependent upon the value of the total current I_o supplied to the constant-current sink. The slope of the

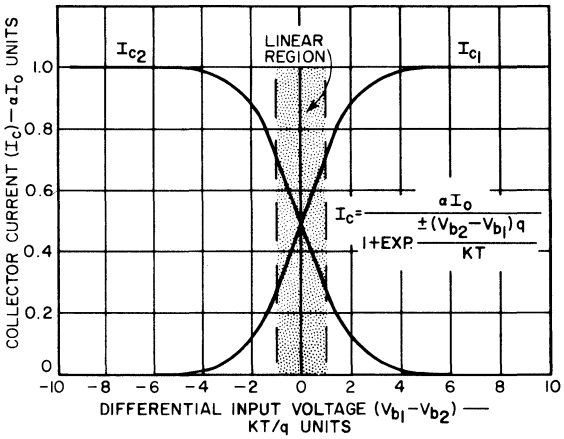


Fig. 10 — Transfer characteristics of the basic differential-amplifier circuit.

transfer curves can be changed, without changing the linear input region, by varying the value of I_o. This relationship implies that automatic gain control is inherent in the differential amplifier when the current I_o is controlled.

4. The transfer characteristics and the slopes of these characteristics are a function of the alpha of the transistors and of the temperature, both of which are predictable, and of two physical constants.
5. The differential amplifier is a natural limiter; when input

excursions exceed ±4KT/q (approximately ±100 millivolts for the curves shown), no further increase in the output is obtained.

6. The output current of an amplifier is the product of the input voltage and the transconductance. In the differential amplifier, the transconductance is proportional to the controlled current I_o; this circuit, therefore, may be used for mixing, frequency multiplication, modulation, or product detection when the current I_o is made a multiplicand and the input waveform is the multiplier.

Transconductance Characteristics

As mentioned in the preceding paragraph, the slope of either of the transfer curves shown in Fig. 10 defines the transconductance of the differential amplifier. The transfer equation [Eq. (14) or Eq. (15)] can be differentiated, therefore, to obtain the general equation for the transconductance g_m as a function of the input voltage $V_{b1} - V_{b2}$. The following result is obtained:

$$\frac{di_c}{de_b} = g_m = \frac{\alpha \frac{I_o}{h} \exp \frac{e_b}{h}}{\left(1 + \exp \frac{e_b}{h}\right)^2} \tag{16}$$

where e_b represents $V_{b1} - V_{b2}$ and h is again equal to KT/q.

When the transconductance is evaluated at the operating point ($e_b = 0$), Eq. (16) reduces to

$$g_m = \frac{q\alpha I_o}{4KT} \tag{17}$$

Eq. (17) reveals that, for the same value of source current I_o, the effective transconductance of the differential amplifier is one-fourth that of a single transistor. This condition results from the fact that, at the operating point, exactly one-half of the total current I_o flows through each transistor of the differential pair and the input voltage must be divided equally between the two transistors.

When the differential amplifier is operated to provide double-ended outputs so that the output voltage is measured between the collectors of the differential pair of transistors, the output currents through the load impedance contribute equally to the output voltage from each transistor. As a result, the output voltage is twice that obtained for single-ended operation. This

increase in output voltage results because the load impedance is doubled, not because of any doubling of the transconductance. However, if an impedance is connected between the two collectors and the shunt collector-feed resistors are large compared to this load impedance, the load current is twice as large as can be expected from a single-ended circuit. This condition indicates an apparent effective transconductance, $g_{m(app)}$, for the double-ended circuit which is expressed by the following equation:

$$g_{m\,(app)} = \frac{q\alpha I_o}{2KT} \tag{18}$$

Effect of Emitter Resistors

Fig. 11 shows a curve of transconductance as a function of differential input voltage $V_{b_1} - V_{b_2}$ as obtained from Eq. (16). A study of this curve indicates that it may be desirable to increase

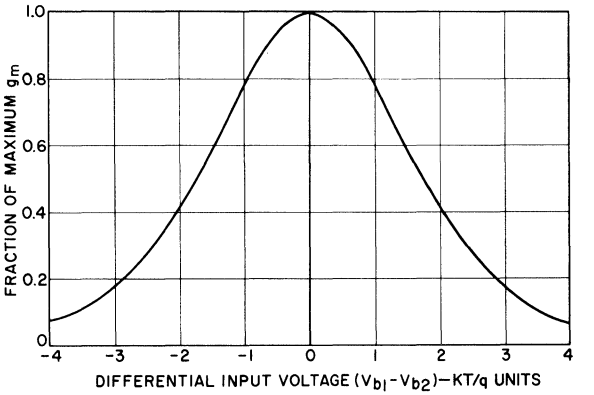


Fig. 11 — Transconductance of the basic differential amplifier as a function of the differential input voltage.

the range of linearity of the transconductance and, thus, suggests the use of emitter degeneration. Fig. 12 shows the basic differential amplifier with two identical emitter resistors (R_e) added. The degeneration introduced by the emitter resistors reduces the gain (transconductance) of the differential pair of transistors, but it also increases the linearity of both the transfer characteristics and the transconductance.

The combination of the nonlinear circuit characteristics and the linear emitter resistors does not lend itself immediately to a

facile mathematical solution. A new transfer curve, which is a function of the actual level of the current I_o and the value of the emitter resistance R_e, can be constructed more easily by graphical

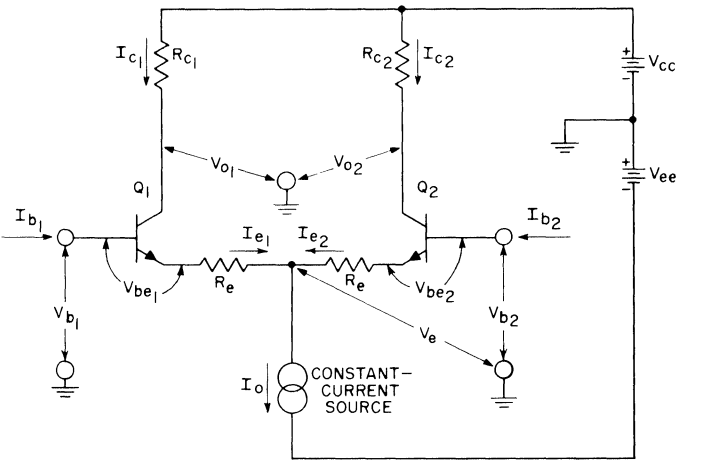


Fig. 12 — Schematic of the basic differential amplifier in which emitter degeneration is employed.

techniques. The new transfer curve, shown in Fig. 13, is obtained from the addition, at a constant current, of the original differential-amplifier voltage drop and the voltage drop across the emitter resistor.

When the effects of two equal emitter resistors (used as shown in Fig. 12) are considered, it is apparent that the differential input voltage must include the ohmic differential voltage drop across the two resistors. This ohmic voltage-drop component, $V_{Re_1} - V_{Re_2}$, can be expressed as follows:

$$V_{Re_1} - V_{Re_2} = I_{e_1} R_e - I_{e_2} R_e \tag{19}$$

If the relationship expressed by Eq. (1) is used, Eq. (19) becomes

$$V_{Re_1} - V_{Re_2} = (2I_{e_1} - I_o) R_e \tag{20}$$

or

$$V_{Re_1} - V_{Re_2} = (I_o - 2I_{e_2}) R_e \tag{21}$$

Eq. (20), which expresses the ohmic differential voltage drop in terms of the emitter current of transistor Q_1, may be rewritten

to express this voltage drop in terms of the transistor collector current, as follows:

$$V_{Re1} - V_{Re2} = \left(\frac{2I_{c1}}{\alpha} - I_o\right) R_e \qquad (22)$$

where I_{c1} is defined as indicated in Eq. (5):

Eq. (22) is represented graphically by the straight line in Fig. 13, which gives the IR drop as a function of the differential input voltage for the circuit shown in Fig. 12 at a constant current I_o of 2 milliamperes.

When emitter resistors are used, therefore, the new transfer characteristics for a differential amplifier can be determined for any given value of the current I_o by addition of the voltage drops of the differential amplifier to those of the emitter resistors. Thus, at the current value P in Fig. 13, the voltage drop across the differential pair of transistors is PQ and that across the emitter

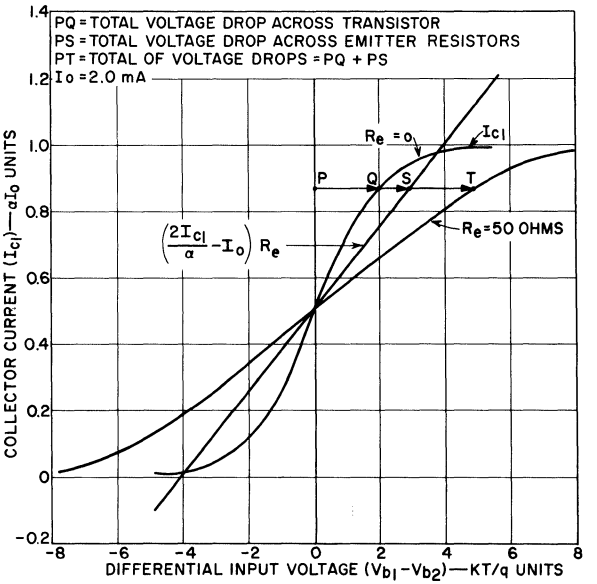


Fig. 13 — Effect of emitter degeneration on the transfer characteristics of the basic differential amplifier.

resistors is PS. The point on the combined transfer curve that corresponds to these conditions is PQ + PS = PT.

This simple graphical addition of voltages at various current levels suggests a mathematical approach that may be used to de-

termine the effects that the degeneration introduced by emitter resistors has on transconductance. In this approach, the transistor current relationship given by Eq. (13) or Eq. (14) is first solved for the differential input voltage $V_{b_1} - V_{b_2}$. In this inverted form, Eq. (14) becomes

$$V_{b_1} - V_{b_2} = -h \ln \left(\frac{\alpha I_o}{I_{c_1}} - 1 \right)$$

This expression for $V_{b_1} - V_{b_2}$, however, does not include the ohmic differential voltage drop across the emitter resistors. When this voltage $V_{Re_1} - V_{Re_2}$, as given by Eq. (22), is added, the equation for $V_{b_1} - V_{b_2}$ becomes

$$V_{b_1} - V_{b_2} = -h \ln \left(\frac{\alpha I_o}{I_{c_1}} - 1 \right) + \left(\frac{2I_{c_1}}{\alpha} - I_o \right) R_e \qquad (23)$$

The derivative of Eq. (23) is then taken to obtain the following relationship:

$$\frac{d(V_{b_1} - V_{b_2})}{dI_{c_1}} = - h \left(\frac{\alpha I_o}{I_{c_1}^2} \right) \left(\frac{I_{c_1}}{\alpha I_o - 1} \right) + \frac{2R_e}{\alpha} \qquad (24)$$

At the operating point ($I_{c_1} = \alpha I_o/2$), Eq. (24) reduces to

$$\frac{d(V_{b_1} - V_{b_2})}{dI_c} = \frac{4h}{I_o} + \frac{2R_e}{\alpha} = \frac{4KT}{qI_o} + \frac{2\,R_e}{\alpha} \qquad (25)$$

The reciprocal of this derivative is the effective transconductance, g_m', of the differential amplifier when emitter resistors are used, as given by

$$g_m' = \frac{1}{\frac{1}{g_m} + \frac{2\,R_e}{\alpha}} = \frac{\alpha g_m}{\alpha^2 + 2R_e g_m} \qquad (26)$$

where g_m is the transconductance of the basic differential amplifier at the operating point, as defined by Eq. (17).

Because α is approximately unity, Eq. (26) is usually simplified to the following form:

$$g_m' \approx \frac{g_m}{1 + 2R_e g_m} \qquad (27)$$

For a differential amplifier having an original transconductance (g_m) of 20×10^3 micromhos, as would be expected for a current I_o of 2 milliamperes, the effective transconductance (g_m') becomes approximately one-third the original value when emitter resistors (R_e) of 50 ohms are used.

The transconductance curves for a differential amplifier which employs emitter degeneration may be constructed as follows: First, the reciprocal of Eq. (24) is taken to obtain the transconductance as a function of the current. The differential input voltage that corresponds to the current is then obtained from Eq. (23). Fig. 14 shows transconductance curves constructed in this manner for the differential amplifier shown in Fig. 12. These curves show the variation in transconductance as a function of the differential input voltage for emitter resistors (R_e) of 50 ohms and of 100 ohms. For comparison, the normalized transconductance of the circuit when no emitter resistors are used is also shown on the same scale.

The increased linearity of the transconductance characteristic that results from the degeneration introduced by the emitter

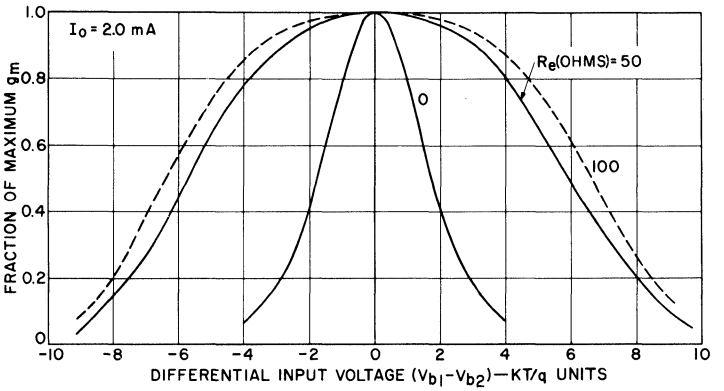


Fig. 14 — Effect of emitter degeneration on the transconductance of the basic differential amplifier.

resistors is evident from the curves shown in Fig. 14. This increased linearity, however, is accompanied by a reduction in the absolute value of the transconductance. As mentioned previously, the use of 50-ohm emitter resistors reduces the absolute value of transconductance to one-third the original value (for an I_o of 2 milliamperes). The use of 100-ohm emitter resistors further reduces the transconductance by approximately 40 per cent.

The preceding discussion has shown that the introduction of emitter degeneration decreases the slope of the transfer characteristics (results in a more linear transconductance) and reduces the sharpness of the cutoff "knee." As a result of these factors, a higher input voltage is required to produce distortion or limiting in the differential amplifiers when emitter resistors are used.

Experimental confirmation of the change in transfer characteristics that results from the use of emitter resistors is provided by the calculated and measured data shown in Fig. 15. The coordinate plane on the right shows one-half of the transfer curves obtained when no external emitter resistors are used. The co-

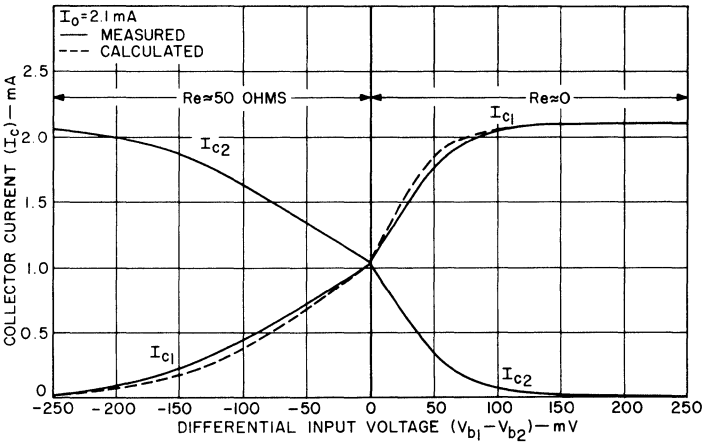


Fig. 15 — DC characteristics of the basic differential amplifier with and without emitter degeneration for a source current I_o of 2.1 milliamperes.

ordinate plane on the left shows one-half the transfer curves obtained when emitter resistors having a nominal value of 50 ohms are included in the differential amplifier.

The theoretical (calculated) curves shown in Fig. 15 are graphical representations of Eqs. (14) and (23). The small differences between the measured and theoretical curves can be attributed to the few ohms of emitter-contact and bulk resistance inherent in the transistor. The exact amount of this emitter resistance can best be calculated from measured transconductance curves since measurements of slopes on curves such as those shown in Fig. 15 are not highly accurate.

The effect of the absolute value of the total current I_0 on the transfer and transconductance characteristics, when a fixed-value emitter resistor is used, is also an important consideration in the differential-amplifier integrated circuit. This effect is illustrated in Fig. 16, which shows the dc transfer characteristics at a current I_0 of 0.188 milliampere, rather than at an I_0 of 2.1 milliamperes as shown in Fig. 15.

At the lower current level, the transfer characteristics of the differential-amplifier transistors are not greatly altered by the use of the 50-ohm emitter resistors (R_e). At this current, the internal diffusion resistance (r_e) of each transistor is in the order of 260 ohms, and the 50-ohm emitter resistors (R_e) are relatively small

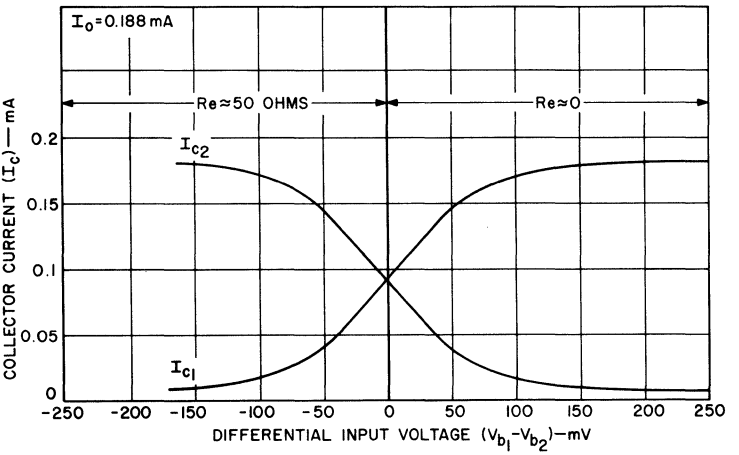


Fig. 16 — DC characteristics of the basic differential amplifier with and without emitter degeneration for a source current I_o of 0.188 milliampere.

in comparison. Eq. (23) shows that when the voltage drop across the differential pair of transistors (as represented by the first term of the equation) is equal to KT/q, the total input voltage drop across each resistor R_e (as given by the second term of the equation) is 0.28 KT/q for an I_o of 0.188 milliampere and 3.1 KT/q for an I_o of 2.1 milliamperes. This behavior suggests that, when gain control is provided by variations in the value of I_o, the signal-handling capability of the differential amplifier can be extended at maximum gain by the use of emitter resistors. As the current I_o (and consequently the circuit gain) is reduced, however, the increase in signal-handling capability gradually disappears because the effect of the emitter resistors R_e becomes relatively insignificant compared to that of the internal diffusion resistance r_e of the transistors.

The family of curves shown in Fig. 17 illustrates the effect of emitter resistors on the transconductance at various current levels. Because of the inherent symmetry of the differential amplifier for positive and negative input signals, the same graph can be used to show the transconductance as a function of the input

voltage for operation of the circuit at many different current values, with and without emitter resistors. The curves in Fig. 17 also show that the effects of a fixed-value emitter resistor become more pronounced, in relation to both the reduction in gain and

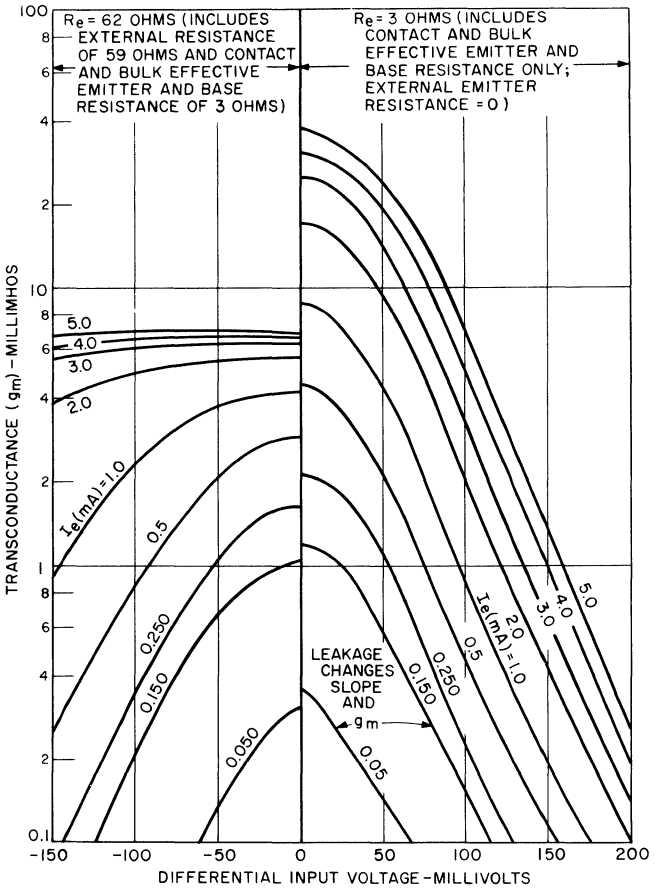


Fig. 17 — Transconductance of the basic differential amplifier as a function of differential input voltage for operation with and without emitter degeneration.

the increase in linearity, as the current is increased. The experimental curves shown in Fig. 17 are in agreement with the theory presented thus far provided that the following postulations are used in the theoretical calculations:

1. The total of the effective emitter-contact and bulk resistance, r_e, inherent in each transistor of the differential pair is assumed to be 3 ohms.*
2. The actual value of each diffused emitter resistor R_e is 59 ohms, rather than the nominal value of 50 ohms used previously.
3. A leakage current of approximately 12 microamperes is assumed.**

When the inherent effective emitter resistance of the transistors is assumed to be 3 ohms, the measured transconductance curves shown on the right coordinate plane in Fig. 17 coincide (within the limits of experimental error) with theoretical curves calculated from Eqs. (17) and (27), except when the total αI_o is equal to or less than 1 milliampere. At these low current levels, the theoretical curves must be corrected to compensate for leakage effects. The leakage current of 12 microamperes is subtracted from the nominal value of αI_o, and the theoretical transconductance values are thus decreased.

For the left coordinate plane, coincidence between theoretical and experimental curves requires that a value of 62 ohms be used in Eq. (27) for the emitter resistor R_e. When the effective internal emitter resistance of 3 ohms is subtracted from this value, the actual value of the external diffused emitter resistors is shown to be 59 ohms, as postulated above.

The excellent correlation of the theoretical assumptions with the actual measured data suggests that a more rigorous equation for the transconductance can be derived.

As can be determined from Fig. 12, the total voltage drop from base to base of the differential pair of transistors Q_1 and Q_2 may be expressed as follows:

$$V_{b_1} - V_{b_2} = V_{be_1} + I_{e_1} R_e - I_{e_2} R_e - V_{be_2} \qquad (28)$$

**The emitter resistance r_e is the sum of the emitter-contact and bulk resistance and the effective base resistance referred to the emitter, $(1 - \alpha) r_b'$. For the transistors in question, the resistance r_e consists of about 2 ohms of emitter resistance and 1 ohm of effective base resistance.*

*** This leakage-current value of 12 microamperes was based on experimental data obtained on early units. Tests on recent units indicate that processing improvements have substantially reduced the leakage in linear integrated circuits.*

In a balanced circuit, the emitter-to-base voltages of transistors Q_1 and Q_2 are given by Eqs. (29) and (30), respectively:

$$V_{be1} = (1 - \alpha)\, I_{e1}\, r_b' + \frac{KT}{q} \ln \frac{I_{e1}}{I_s} + I_{e1}\, r_{ec} \tag{29}$$

$$V_{be2} = (1 - \alpha)\, I_{e2}\, r_b' + \frac{KT}{q} \ln \frac{I_{e2}}{I_s} + I_{e2}\, r_{ec} \tag{30}$$

where r_b' is the internal base resistance, r_{ec} is the internal emitter-contact resistance, and the following matching equalities are assumed:

$$\begin{aligned} I_s &= I_{s1} = I_{s2} \\ \alpha &= \alpha_1 = \alpha_2 \\ r_b' &= r_{b1}' = r_{b2}' \\ r_{ec} &= r_{ec1} = r_{ec2} \\ R_e &= R_{e1} = R_{e2} \end{aligned} \tag{31}$$

(The effects of the offsets that result from an unbalance in any of the matching parameters are analyzed in the next section.)

The relationships expressed by Eqs. (28), (29), and (30), together with those given by Eqs. (1), (5), and (6), are used to obtain equations for the transconductance in terms of the collector currents I_{c1} and I_{c2} of transistors Q_1 and Q_2, respectively, as follows:

$$V_{b1} - V_{b2} = [(1 - \alpha)\, r_b' + r_{ec} + R_e] \left(\frac{2I_{c1}}{\alpha} - I_o \right) + h \ln \frac{I_{c1}}{\alpha I_o - I_{c1}} \tag{32}$$

$$V_{b1} - V_{b2} = [(1 - \alpha)\, r_b' + r_{ec} + R_e] \left(I_o - \frac{2I_{c2}}{\alpha} \right) + h \ln \frac{\alpha I_o - I_{c2}}{I_{c2}} \tag{33}$$

Eqs. (32) and (33) are differentiated, and the results are evaluated at the operating point (at $I_{c1} = I_{c2} = \alpha I_o/2$) to obtain the following relationships:

$$\frac{d(V_{b1} - V_{b2})}{dI_{c1}} = \frac{2(1 - \alpha)\, r_b'}{\alpha} + \frac{(r_{ec} + R_e)\, 2}{\alpha} + \frac{4h}{\alpha I_o} \tag{34}$$

$$\frac{d(V_{b1} - V_{b2})}{dI_{c2}} = -\frac{2(1 - \alpha)\, r_b'}{\alpha} - \frac{(r_{ec} + R_e)\, 2}{\alpha} - \frac{4h}{\alpha I_o} \tag{35}$$

Eqs. (34) and (35) are inverted to obtain the required equations for the transconductance of transistors Q_1 and Q_2, respectively, as follows:

$$g_{m1} = \frac{dI_{c1}}{d(V_{b1} - V_{b2})} = \frac{\alpha}{2(1-\alpha)\, r_b' + 2(r_{ec} + R_e) + 4h/I_o} \quad (36)$$

$$g_{m2} = \frac{dI_{c2}}{d(V_{b1} - V_{b2})} = \frac{-\alpha}{2(1-\alpha)\, r_b' + 2(r_{ec} + R_e) + 4h/I_o} \quad (37)$$

The negative sign of Eq. 37 reflects the negative slope, shown in Fig. 10, of the transfer characteristic for I_{c2}.

OFFSETS IN THE DIFFERENTIAL-AMPLIFIER INTEGRATED CIRCUITS

In the preceding analyses, it has been assumed that the parameters of the pair of transistors in the differential-amplifier integrated circuits are perfectly matched. In general, this assumption is justified because, although finite differences in the parameters exist, they are usually negligible. Nevertheless, variations in the amount of the differences from unit to unit result in a statistical distribution, and practical production limits on the allowable deviations in corresponding parameters of the differential pair of transistors must be established. It is convenient to evaluate the effects of circuit and device unbalances in terms of a quantity, referred to as offset, which is a measure of the total accumulative unbalances.

Offset Evaluation Techniques

The amount of offset in a differential amplifier can be determined by output-voltage offset measurements, by input-voltage offset measurements, or by input-current offset measurements. Each of these basic measurement techniques is straightforward and provides accurate results when employed at low frequencies. The measurements may also be used to determine the offset in cascaded differential amplifiers and in operational amplifiers.

Output-Voltage Offset Measurements — An offset in the differential-amplifier circuit is indicated by a difference in potential between the two outputs (V_{o1} and V_{o2}, as defined in Fig. 12) of the transistors when there is no signal applied to the input of

either transistor. This type of offset is a measure of any unbalance caused by the flow of base currents from the differential pair of transistors Q_1 and Q_2 through the two external base resistors to ground. Under these conditions, the voltages V_{b_1} and V_{b_2} are both unequal to zero; an offset exists if these voltages are also unequal to each other (i.e., if $V_{b_1} - V_{b_2} \neq 0$).

A common method used to determine the offset at the output is to reduce the two base resistors to zero. This effect is achieved when the inputs of the transistors Q_1 and Q_2 are shorted to ground. The output offset determined in this manner is restricted in that unbalances caused by unequal base currents (betas) or by unequal external base resistors are excluded. All other unbalances, however, are included in the measurement.

Input-Voltage Offset Measurements — An offset voltage referred to the input is simply the differential output offset voltage divided by the double-ended voltage gain of the circuit. This definition indicates a convenient method that may be used to measure the offset. In this method, a voltage is applied to one input of the differential amplifier and is varied until the differential output voltage $V_{o_1} - V_{o_2}$ is reduced to zero. The value of the input voltage is then the offset voltage referred to the input.

Input-Current Offset Measurements — The offset in a differential amplifier can also be determined by the amount of current that must be introduced at one input to obtain a differential output voltage equal to zero. This type of measurement, together with the output offset measurement in which the inputs of the circuit are shorted to ground, tends to segregate unbalances in base currents (betas) and in the input base resistors.

Dependence of Offset on Base-to-Emitter Voltages

Offsets in the differential-amplifier integrated circuits can, in general, be attributed to three basic types of device or circuit unbalances:

1. Differences in the base-to-emitter voltage V_{be} and in the beta of the differential pair of transistors because of initial deviations in the geometry or the diffusion-concentration profiles of the transistors;
2. Differences in the V_{be}, the beta, or the internal resistances of the transistors that result from finite variations in thermal resistance or heat flow paths;

3. Differences in the values of resistors used in the collector, base, or emitter leads of the two transistors.

In the following discussion, the base-to-emitter voltage is analyzed to show the functional dependence of this quantity on the transistor parameters and on temperature. An expression for the differential-amplifier offset in terms of V_{be} is then derived, and the relative effects of differences in the various parameters of the differential pair of transistors and in the emitter resistors of these transistors on the offset are evaluated. The effects of temperature on the offset are also discussed.

Analysis of the Base-to-Emitter Voltage — The voltage between the base and emitter leads of a transistor, V_{be}, includes the fundamental voltage drop across the emitter-base junction, as given by the diode equation [Eq. (7)], together with the voltage drops that are produced by the flow of base current through the intrinsic base resistance r_b' and by the flow of emitter current through the emitter-contact and bulk resistance r_{ec}. V_{be} can be expressed in terms of these voltage drops, as follows:

$$V_{be} = \left(\frac{KT}{q} \ln \frac{I_e}{I_s}\right) + I_e r_{ec} + I_e (1 - \alpha)\, r_b' \qquad (38)$$

The emitter-contact and bulk resistance r_{ec} should not be confused with the diffusion resistance r_e, which is given by the familiar T-circuit representation as follows:

$$r_e = \frac{KT}{qI_e} \qquad (39)$$

The voltage drop across the diffusion resistance r_e is included in the logarithmic term of Eq. (38).

The voltage V_{be} is obviously a nonlinear function of the transistor current and, therefore, cannot be represented properly by any lumped-constant linear equivalent circuit. Eq. (38), which contains no approximation, provides the best means for the calculation of this voltage.

The bulk saturation current I_s is best determined from a measured curve at an emitter current which is low enough so that the voltage drops across the internal resistances (r_b' and r_{ec}) of the transistor are negligible. Fig. 18 shows curves of V_{be} as a function of temperature at various emitter currents for a typical integrated-circuit transistor. This transistor has an intrinsic base resistance r_b' of 40 ohms, an emitter-contact and bulk resistance r_{ec} of approximately 3 ohms, and a beta of about 50. The V_{be}

curve obtained at an emitter current of 100 microamperes can be used satisfactorily in the determination of the current I_s.

At an emitter current of 100 microamperes, the base current of the transistor is about 2 microamperes. The resultant voltage drop produced across the intrinsic base resistance r_b' then is about 0.08 millivolt. At this level of emitter current, the voltage

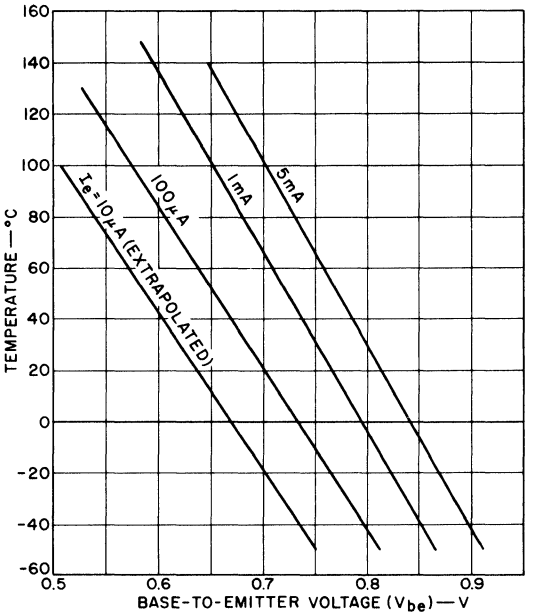


Fig. 18 — Effect of temperature and emitter current on the base-to-emitter voltage of an integrated-circuit transistor.

drop across the emitter-contact and bulk resistance r_{ec} is approximately 0.3 millivolt. Thus, at 100 microamperes of emitter current, the total voltage drop (approximately 0.38 millivolt) across the internal resistances of the transistor is negligible, and the measured value obtained for V_{be} can be attributed almost entirely to the logarithmic term in Eq. (38).

Fig. 18 shows that V_{be} is 0.7 volt for an emitter current of 100 microamperes and a temperature of 20°C. When the values of transistor parameters given by these conditions are substituted in Eq. (8), the following result can be obtained:

$$\frac{I_e}{I_s} = \exp \frac{700}{26} = 5 \times 10^{11}$$

$$I_s = 0.2 \times 10^{-15} \text{ ampere}$$

For each decade change in the emitter current, the logarithmic component of the base-to-emitter voltage V_{be} changes by an amount equal to KT/q ln 10, or 60 millivolts at 300°K. Fig. 18 shows, however, that the V_{be} curve for an emitter current of 1 milliampere is shifted 65 millivolts upward from the V_{be} curve obtained at 100 microamperes. The additional 5 millivolts of change is exactly equal to the voltage drop developed across the internal resistances of the transistor at the 1-milliampere level. For an emitter current of 5 milliamperes, the sum of the voltage drops across the internal resistances is in the order of 19 millivolts, and the logarithmic component of V_{be} is increased from the value obtained at 1 milliampere of emitter current by an amount equal to KT/q ln 5, or 42 millivolts at 300°K. These results show that the base-to-emitter voltage V_{be} is largely dependent upon the bulk saturation current I_s. At a given temperature, this current, in turn, is a function of the geometry of the base-emitter junction and the diffusion-concentration profile.

The curves in Fig. 18 also show that the dependence of the base-to-emitter voltage on temperature is varied by a change in the level of emitter current. The variation in V_{be} with temperature changes from −1.6 millivolts per °C at low emitter currents (0.1 miliampere or less) to 1.3 millivolts per °C at 5 milliamperes of emitter current. This reduction in the negative temperature coefficient of V_{be} with an increase in emitter current is a result of the positive temperature coefficient of the transistor resistors.

Relative Effects of Various Circuit and Device Unbalances — The relative effects of differences in various transistor parameters and in emitter resistors on the offsets in the differential-amplifier integrated circuit can be evaluated on the basis of the preceding discussion of transistor base-to-emitter voltage. For this evaluation, an equation for offset voltage in terms of the various circuit and device parameters is derived for the differential-amplifier circuit shown in Fig. 12 so that the effects of an unbalance between corresponding parameters on the offset voltage can be readily determined.

In the offset-voltage derivation, the base currents I_{b_1} and I_{b_2} are assumed to enter the bases of the differential pair of transistors Q_1 and Q_2 through external base resistors R_{b_1} and R_{b_2}, respectively, from the ground reference. Kirchoff's first law then dictates that the sum of the voltage drops from the ground reference across R_{b_1}, the base-emitter junction of transistor Q_1, the two equal emitter resistors R_{e_1} and R_{e_2}, the base-emitter junction

of transistor Q_2, R_{b_2}, and back to the ground reference must be zero. This summation may be expressed as follows:

$$I_{b_1} R_{b_1} + V_{be_1} + I_{e_1} R_{e_1} - I_{e_2} R_{e_2} - V_{be_2} - I_{b_2} R_{b_2} = 0 \quad (40)$$

Eq. (40) may be rewritten as follows:

$$(1-\alpha_1)\, I_e R_{b_1} + I_{e_1} R_{e_1} + V_{be_1} = (1-\alpha_2)\, I_{e_2} R_{b_2} + I_{e_2} R_{e_2} + V_{be_2} \quad (41)$$

This equation is then solved for I_{e_1} to obtain

$$I_{e_1} = \frac{I_{e_2} R_{b_2} (1 - \alpha_2) + R_{e_2}}{R_{b_1} (1 - \alpha_2) + R_{e_1}} + \frac{V_{be_2} - V_{be_1}}{R_{b_1} (1 - \alpha_1) + R_{e_1}} \quad (42)$$

In Eq. (42), the voltage drops across the intrinsic emitter and base resistances (r_{ec} and r_b') need not be explicitly expressed because these voltage drops are implied in the $V_{be_2} - V_{be_1}$ term. Alternatively, if the $V_{be_2} - V_{be_1}$ term is used to represent the purely logarithmic component of the base-to-emitter voltage, the voltage drops across the intrinsic resistances, when they are significant, can be lumped with the external resistors.

The current-transfer relationships given by Eq. (5) are used to rewrite Eq. (42) in terms of the collector currents I_{c_1} and I_{c_2} of transistors Q_1 and Q_2, respectively, as follows:

$$\frac{I_{c_1}}{\alpha_1} = \frac{I_{c_2}}{\alpha_2} \left[\frac{R_{b_2} (1 - \alpha_2) + R_{e_2}}{R_{b_1} (1 - \alpha_1) + R_{e_1}} \right] + \frac{V_{be_2} - V_{be_1}}{R_{b_1} (1 - \alpha_1) + R_{e_1}} \quad (43)$$

Eq. (41) may also be written in terms of the common-emitter current gain, i.e., the transistor beta (β), when the following relationships are employed:

$$\beta = \frac{\alpha}{1 - \alpha} \quad (44)$$

$$\alpha = \frac{\beta}{\beta + 1} \quad (45)$$

The resultant equation is given by

$$I_{c_1} = \frac{\beta_1}{\beta_2} \left[\frac{R_{b_1} + (\beta_2 + 1) R_{e_2}}{R_{b_1} + (\beta_1 + 1) R_{e_1}} \right] I_{c_2} + \frac{\beta_1 (V_{be_2} - V_{be_1})}{R_{b_1} + (\beta_1 + 1) R_{e_1}} \quad (46)$$

As stated previously, an offset in a differential-amplifier circuit is indicated by a difference in the collector outputs of the differential pair of transistors. This offset-voltage difference is given by the following equation:

$$V_{o_1} - V_{o_2} = I_{c_2} R_{c_2} - I_{c_1} R_{c_1} \quad (47)$$

where V_{o1} and V_{o2} are the collector outputs of the differential-amplifier transistors Q_1 and Q_2, respectively, and R_{c1} and R_{c2} are the collector load resistors for these transistors.

The effects on the offset of differences in corresponding parameters of the differential pair of transistors Q_1 and Q_2 can be approximated by examination of Eqs. (43), (46), and (47) when such differences are introduced. In such examinations, differences in only one set of parameters are allowed at any given time, and the effects of these differences on the offset are noted.

In the evaluations, R_{e1} and R_{e2} are used to denote the total of the extrinsic and intrinsic emitter resistance, and R_{b1} and R_{b2} are used to denote the total of the extrinsic and intrinsic base resistance. The following initial assumptions are also made for a perfectly balanced differential amplifier:

$R_{e1} = R_{e2} =$ 50 ohms extrinsic + 3 ohms intrinsic
$R_{b1} = R_{b2} =$ 40 ohms intrinsic + 0, 1000, or 10,000 ohms extrinsic
$R_{c1} = R_{c2} =$ 1000 ohms
$I_{e1} = I_{e2} \approx$ 1 milliampere
$\beta_1 = \beta_2 \approx 60$

Figs. 19 to 25 show the effects on the offset of differences in corresponding pairs of the various parameters as calculated from Eqs. (46) and (47). Because these calculations all result in straight-line curves, the effects of the various unbalances can be readily compared by the graphic presentation. The effect of unbalanced conditions other than those shown, such as differences in collector resistors, may also be compared by the use of these simple graphic techniques.

Fig. 19 shows the effects on offset of unequal betas. Curves are shown for an external base resistance of zero and for transistor betas in the range of 20, 60, and 100. These curves represent the first term of Eq. (46).

Fig. 20 shows the effect of different values of base resistances ($R_{b1} = R_{b2}$) on the offset when the betas of the differential-amplifier transistors are unequal. The curves in this figure show that a serious increase in the offset occurs when the external base resistances are significantly larger than the nominal value. Figs. 21 and 22, however, indicate that the use of larger external base resistances reduces the offset that is produced when the betas are

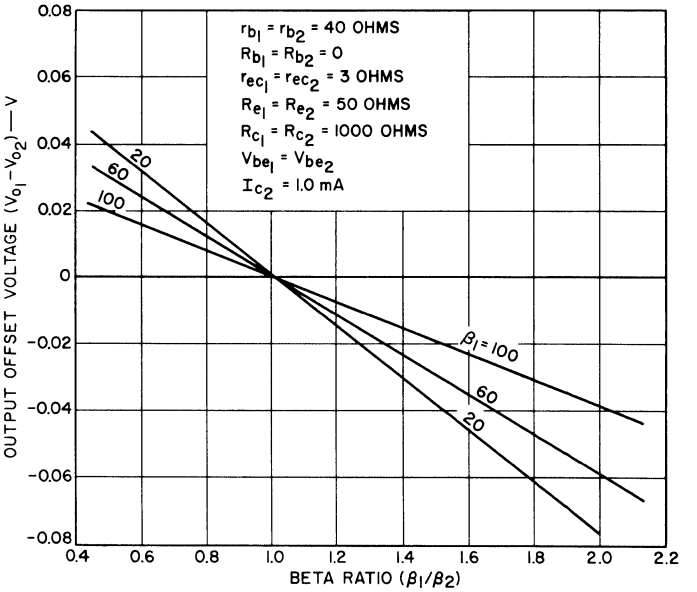


Fig. 19 — Effect of absolute values and ratios of the betas of the differential pair of transistors on the output offset voltage.

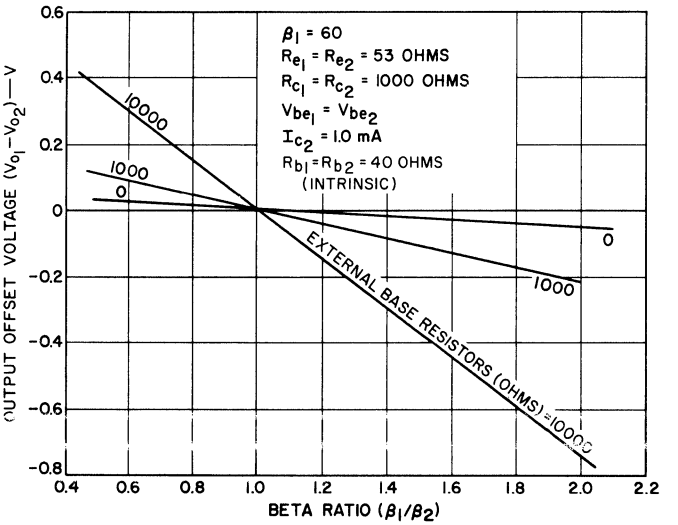


Fig. 20 — Output offset voltage as a function of the beta ratio of the differential pair of transistors for several values of external base resistors.

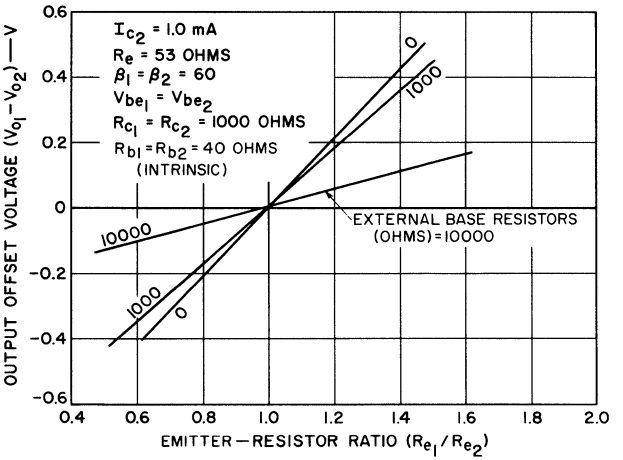


Fig. 21 — Output offset voltage as a function of the emitter-resistor ratio of the differential pair of transistors for several values of external base resistors.

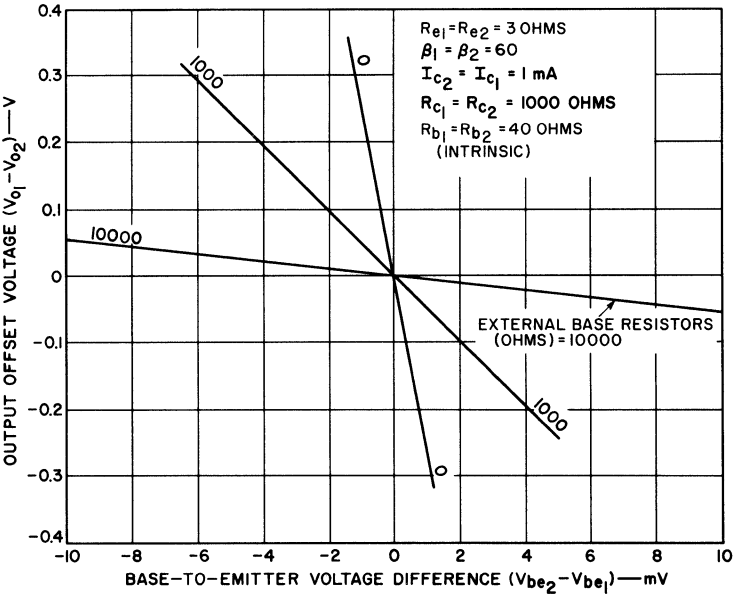


Fig. 22 — Output offset voltage as a function of the difference in the base-to-emitter voltage of the differential pair of transistors for several values of external base resistors.

the same and a difference exists between the emitter resistors or the base-to-emitter voltages.

Fig. 23 shows that the offset that results from differences in the emitter resistors is increased by the use of larger emitter resistors. Fig. 24 shows that the offset caused by differences in

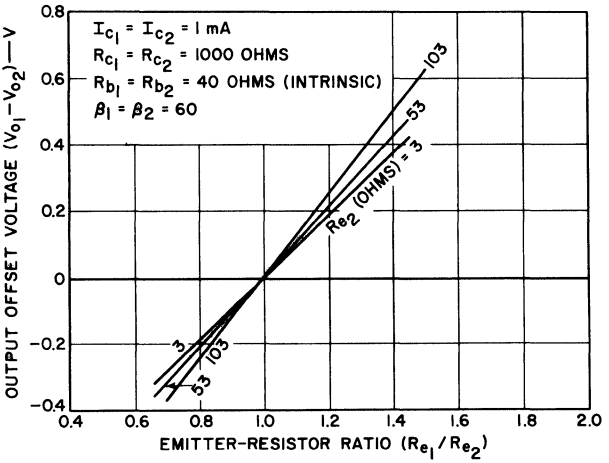


Fig. 23 — Effect of absolute values and ratios of the emitter resistors of the differential pair of transistors on the output offset voltage.

the V_{be} of the differential pair of transistors is reduced by the use of emitter resistors.

Fig. 25 shows the offset as a function of differences in the base-to-emitter voltages of the transistors for transistor betas ($\beta_1 = \beta_2$) of 20, 60, and 100. The curves in this figure, which represent the second term in Eq. (46), indicate that the effects of the absolute values of the betas on this term are the opposite of those on the first term, as shown in Fig. 19.

Effects of Temperature — Each parameter in Eqs. (46) and (47) is dependent to some extent on temperature, even though this dependence cannot be readily expressed as a straightforward mathematical relationship. An analytical expression of the offset as a function of temperature is, therefore, of small practical value. It is more meaningful to relate the offset to temperature-caused differences in the values of the base-to-emitter voltages, betas, or resistances of the differential-amplifier transistors.

One of the main advantages of differential-amplifier integrated circuits is that each component for a given transistor is physically

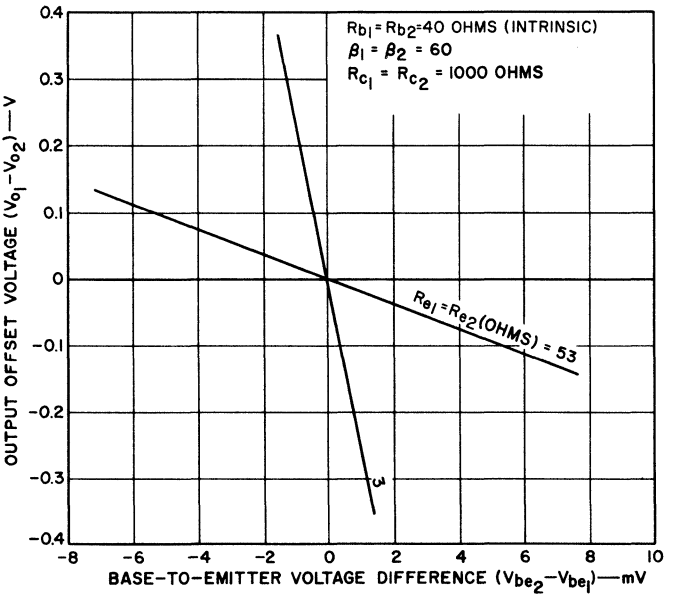


Fig. 24 — Output offset voltage as a function of the difference in the base-to-emitter voltages of the differential pair of transistors for several values of the total emitter resistance (internal + external) of each transistor.

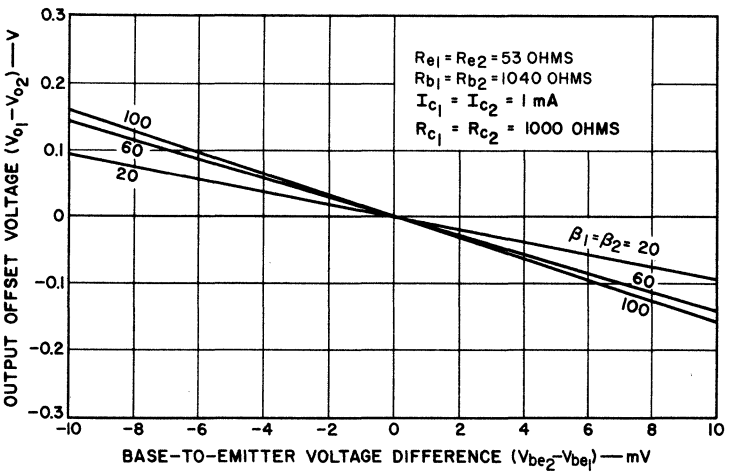


Fig. 25 — Output offset voltage as a function of the difference in the base-to-emitter voltages of the differential pair of transistors for several beta values.

located very close to the corresponding component of the second transistor of the differential pair. As a result, the temperature environments for the pairs of components should be very similar. This feature is successfully exploited in the design of the integrated circuits, so that the effects of temperature on corresponding components is remarkably similar.

Experimental data on sample units have shown that the change in output offset varies from no measurable drift up to 10 millivolts for temperature variations over the 180-degree range from $-55°C$ to $+125°C$. These limits correspond to an input offset of between 0 and 2.5 microvolts per °C. Statistical production controls usually allow for greater maximum drifts, e.g., 5 to 10 microvolts per °C.

CHARACTERISTICS OF THE CONSTANT-CURRENT SINK

The constant-current sink for the source current I_o, which is a significant factor in the transfer and transconductance characteristics of the differential amplifier, may be realized physically by a resistor and a dc power supply or by a transistor circuit and a dc power supply. The transistor-current-sink circuit has a higher ac-to-dc impedance ratio, which results in higher common-mode rejection. In addition, the gain characteristics and bias network of the transistor sink circuit make possible temperature compensation, gain control, squelch or switch action, and frequency multiplication in the differential amplifier. The transistor current sink, therefore, is clearly superior in versatility to the resistor current sink for use in the differential-amplifier integrated circuits. The characteristics of the transistor current sink are developed in detail below.

General Circuit Configuration

Fig. 26 shows the general configuration of a transistor current-sink circuit in which diode temperature stabilization is employed. In this general circuit, all diodes are assumed to be forward-biased. D_1 represents the number (0, 1, 2, . . .) of forward-biased diodes in series with resistor R_1, and D_2 represents the number (0, 1, 2, . . .) of forward-biased diodes in series with resistor R_2.

The sink current I_o of the differential amplifier is the collector current of the current-sink transistor. This current is expressed in terms of the emitter current of the current-sink tran-

sistor by Eq. (5), which relates the collector and emitter currents of a single transistor, as $I_c = \alpha I_e$, where in this case the I_e is the emitter current of the current-sink transistor. Each diode used in the integrated circuits is actually a transistor connected to operate as a diode. The voltage drop V′ across each diode used in the current-sink circuit can be expressed as follows:

$$V' = \left(\frac{KT}{q} \ln \frac{I}{I_s}\right) + Ir \tag{48}$$

where r is the sum of all the internal resistance of the diode.

The resistance r is generally very small in comparison to the external resistors R_1 and R_2 in series with the diodes, and the voltage drop Ir can usually be neglected. For this condition, the voltage drop V′ is expressed by the first term of Eq. (48), and, as determined from Fig. 18, is about 0.765 volt for a current of 1 milliampere. The voltage drop Ir in Eq. (48) represents an additional 5 millivolts.

For a diode formed by the connection of the collector of a transistor to the base ($V_{CB} = 0$), the total currents and Ir drops are very similar to those of the transistor connection. For other possible connections of transistor terminals to form diodes, more of the diode current flows through r_b' and a higher forward voltage drop results. In Fig. 26, this additional voltage drop is lumped with the voltage drops across the external resistors R_1 and R_2.

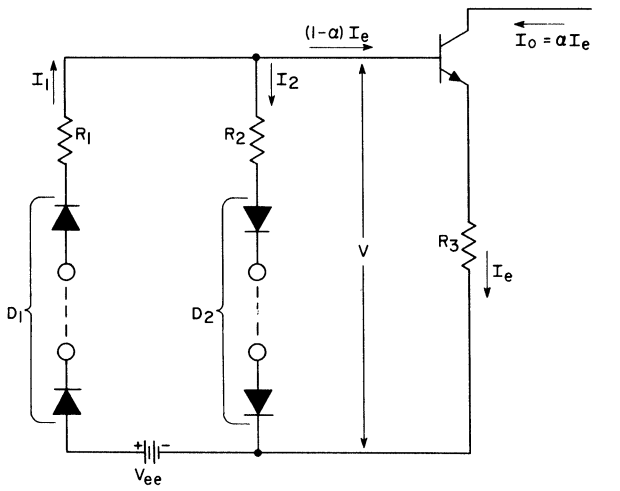


Fig. 26 — General configuration for a diode-stabilized transistor current-sink circuit.

For the transistor in the current-sink circuit, the voltage drop V′ is considered to be expressed by the logarithmic term in Eq. (38). The second and third terms of this equation represent voltage drops that, although identified separately, can be lumped with the resistive drops in the base and emitter paths for the circuit shown in Fig. 26.

For the general current-sink circuit shown in Fig. 26, the following equations are necessary and sufficient to define the operating requirements and characteristics:

$$I_1 = I_2 + (1 - \alpha)\, I_e \tag{49}$$

$$V_{ee} - (D_1 - D_2)\, V' = I_1 R_1 + I_2 R_2 \tag{50}$$

$$D_2 V' + I_2 R_2 = (1 - \alpha)\, r_b' + V' + (r_{ee} + R_3)\, I_e \tag{51}$$

Solution of these three equations in terms of the emitter current I_e of the current-sink transistor yields the following relationship:

$$I_e = \frac{X\,[V_{ee} - (D_1 + D_2)\, V'] + (D_2 - 1)\, V'}{R_3 + r_{ee} + (1 - \alpha)\,(r_b' + R_1 X)} \tag{52}$$

where

$$X = \frac{R_2}{R_1 + R_2} \tag{53}$$

Temperature Characteristics

In Eq. (52), the emitter resistor R_3 is usually the dominant term of the denominator; however, if the beta of the current-sink transistor is low, the contribution of the base resistance ($r_b' + R_1X$) may also be significant. The effect of the base resistance can be particularly noticeable at the low extreme of the temperature range where the current gain [$\beta = \alpha/(1 - \alpha)$] is minimum. The temperature coefficient of the denominator of Eq. (52), therefore, results from the combination of the temperature coefficients of the resistors and the effects of temperature on the transistor beta and, hence, on $1 - \alpha$.

In the numerator of Eq. (52), V′ is the main temperature-dependent parameter. The multipliers ($D_1 + D_2$) and ($D_2 - 1$), therefore, may be used to control the temperature characteristics in the numerator.

These statements indicate that the effects of temperature on the operation of the current-sink circuit can be controlled by the values selected for D_1, D_2, X, and V_{ee}. The effect of each of

these parameters on the emitter current I_e, as given by Eq. (52), and hence on the output current of the current-sink circuit ($I_o = \alpha I_e$) is evaluated below.

In the use of Eq. (52) to evaluate the effects of temperature on the current-sink circuit, it is convenient to represent the numerator and denominator of the equation by more compact symbols, as follows:

$$I_e = \frac{E}{R_t} \tag{54}$$

where

$$E = X\,[V_{ee} - (D_1 + D_2)\,V'] + (D_2 - 1)\,V' \tag{55}$$

and

$$R_t = R_3 + r_{ec} + (1 - \alpha)\,(r_b' + R_1 X) \tag{56}$$

In Eqs. (54) and (55), the term E represents the effective emitter voltage of the current-sink transistor.

Fig. 27 illustrates the effects of temperature on the resistance R_t. In this figure, curves B, C, and D show R_t as a function of

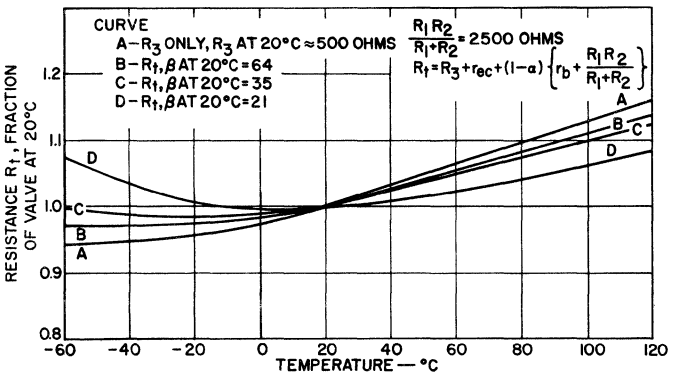


Fig. 27 — Resistance ratio R_t as a function of temperature for several values of the beta of the current-sink transistor.

temperature for three beta values when the nominal value of R_3 at 20°C is 500 ohms. Curve A shows variations in the value of resistor R_3 with temperature. The temperature coefficient of beta is considered linear. The slopes of this coefficient for the beta values of 64, 35, and 21 used in Fig. 27 are 0.26, 0.14, and 0.12 per °C, respectively.

These slopes are average values based on the measured performance of a number of transistors. The temperature coefficient

of resistor R_3, as represented by curve A in Fig. 27, is also determined from measured values.

Fig. 28 indicates that the effect of beta variations with temperature on the composite resistance R_t is reduced as the

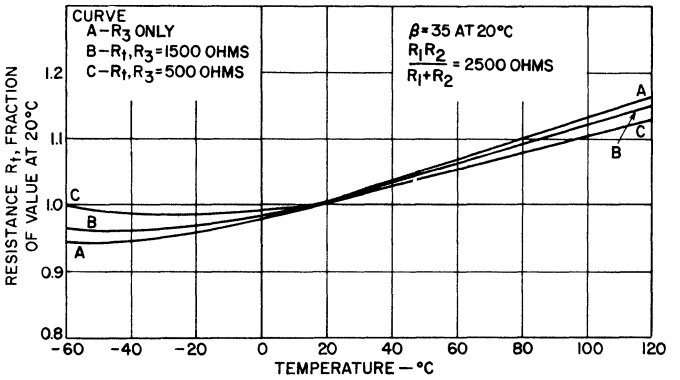


Fig. 28 — Resistance ratio R_t as a function of temperature for several values of the emitter resistor (R_3) of the current-sink transistor.

value of R_3 is increased. Figs. 27 and 28 illustrate the following main factors in this relationship:

1. As the temperature rises, the resistance R_t increases; the emitter current I_e and, therefore, the source current I_o then decrease unless the voltage E is made to increase simultaneously. Eqs. (37) and (38) reveal that the transconductance also decreases as the temperature increases unless the source current I_o is made to increase with temperature.
2. If a collector load resistor tracks the composite resistance R_t over a large portion of the operating temperature range, the operating point is independent of temperature (to a first approximation) only if the factor E has a zero temperature coefficient.

It is desirable, therefore, to examine the factor E, given by Eq. (55), to determine (a) a zero temperature coefficient for E, and (b) a coefficient for E that is large enough to cause the current I_o to increase with increases in temperature.

It is convenient to define the voltage drop V′ as follows:

$$V' = V_o + C\triangle T \tag{57}$$

where V_o is the value of V′ at room temperature, C is the temperature coefficient of V′ (e.g., −1.43 millivolts per °C), and ΔT is the change in temperature from room temperature.

When the relationship expressed by Eq. (57) is used in Eq. (55), the value of E is given by

$$E = \frac{X}{M}(MV_{ee} - V_o - C\Delta T) \tag{58}$$

where

$$M = \frac{X}{(D_1 + D_2)\left(X - \frac{D_2 - 1}{D_1 + D_2}\right)} \tag{59}$$

The proportional change in E with temperature can be expressed as follows:

$$\frac{\Delta E}{E} = \frac{-C\Delta T}{MV_{ee} - V_o} \tag{60}$$

Because the temperature coefficient C is negative, the ratio $\Delta E/E$ can be positive only if M is positive and if MV_{ee} is greater than V_o. A zero temperature coefficient for E is approached when M approaches infinity; resistance ratio X is then given by

$$X = \frac{D_2 - 1}{D_1 + D_2} \tag{61}$$

When M is equal to or less than 1, the ratio $\Delta E/E$ is very small and, for conventional dc power supplies ($V_{ee} >> V_o$), is positive. In the evaluation of M, it is important to remember that D_1 and D_2 are positive integers, and that X is a positive number between 0 and 1 (i.e., $0 < X < 1$). The value of X is restricted even further by practical circuit considerations. Eqs. (54), (55), and (56) show that the operating point of differential-amplifier integrated circuits is dependent upon the value of the resistance ratio X. This ratio, therefore, must be easy to maintain at the required value during production to assure a predictable operating point. The more closely the resistors R_1 and R_2 are matched in geometry, the more easily the value of the ratio X can be maintained at the required value.

Eq. (53) can be rewritten to obtain the following expression for X:

$$X = \frac{1}{\frac{R_1}{R_2} + 1}$$

If production tolerances restrict the ratio R_1/R_2 to a value between 0.5 and 2 (i.e., $0.5 \leq R_1/R_2 \leq 2$), X is then constrained to the region between 0.33 and 0.67 (i.e., $0.33 \leq X \leq 0.67$).

Practical considerations also dictate that the number of compensating diodes used in the current-sink circuit be limited to the minimum required to provide the necessary temperature compensation. The maximum value for D_1 or D_2 is limited to 3. A systematic exploration of all possible combinations is best accomplished by evaluation of Eqs. (59) and (60) as functions of X, D_1, and D_2, as D_1 and D_2 are assigned values of 0, 1, 2, and 3 in turn.

For $D_2 = 0$, Eq. (59) becomes

$$M = \frac{X}{D_1 X + 1} \tag{62}$$

M is positive for all values of X. Substitution of Eq. (62) into Eq. (60) shows that infinite points occur whenever $MV_{ee} = V_o$. When MV_{ee} is less than V_o, the ratio $\Delta E/E$ is negative; otherwise, this ratio is positive.

The change in $\Delta E/E$ that results from a 100°C rise in temperature is shown in Figs. 29 through 34, for various conditions. Fig. 29 shows this proportional change in E as a function of X for different values of D_1 when $D_2 = 0$ and $V_{ee} = 3.0$ volts. As X is varied from 0 to 1, the increase in temperature causes negative increases in E that rise to infinity. As X is increased further, the proportional change in E becomes positive and becomes smaller and smaller as X approaches 1. The use of higher values of D_1 increases the value of X at which the turnover occurs and, in general, results in a higher positive value for $\Delta E/E$.

Fig. 30 shows $\Delta E/E$ as a function of X for the same conditions as those given in Fig. 29, except that V_{ee} is 6 volts. With V_{ee} doubled, the turnover point occurs closer to the origin, and the positive changes in E are smaller.

It is obvious that D_2 must equal 0 for a positive change in E to result from a temperature increase and for a negative change in E to result from a temperature decrease. The exact amount of change in E, together with the expected operating points, dictates the value of D_1 and of the ratio X.

For the condition $D_2 = 1$, Eq. (59) becomes

$$M = \frac{1}{1 + D_1} \tag{63}$$

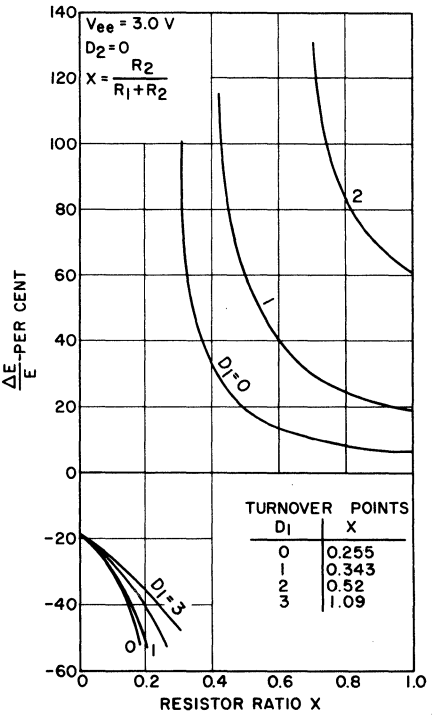


Fig. 29 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when no diodes D_2 are used.

This equation obviously is independent of the ratio X. The voltage E, therefore, is dependent upon only the power supply. This condition, however, does not permit the designer the option to introduce any quantitative change by the proper selection of X. For this reason, the condition $D_2 = 1$ is rejected and will not be considered further.

For the condition $D_2 = 2$, Eq. (59) is given as follows:

$$M = \frac{X}{(D_1 + 2)\left(X - \frac{1}{D_1 + 2}\right)} \tag{64}$$

For values of $X = 1/(2 + D_1)$, M is infinite, and Eq. (60) shows that $\Delta E/E$ becomes zero. When X is less than $1/(2 + D_1)$, M is negative, and negative values are obtained for $\Delta E/E$ as the

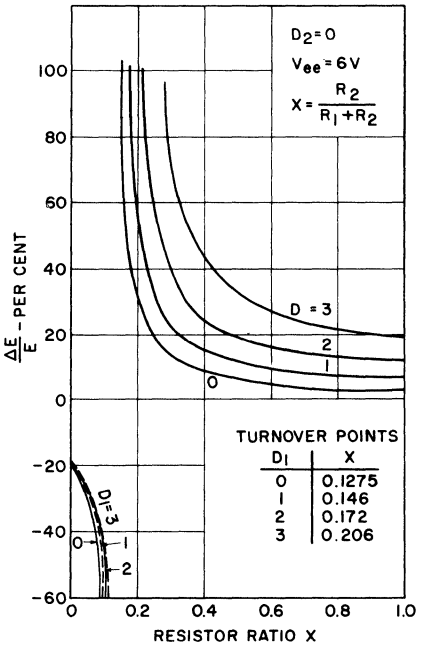


Fig. 30 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when no diodes D_2 are used.

temperature rises. When X is greater than $1/(2 + D_1)$, M is positive.

When the voltage V_{ee} is low enough, the ratio $\Delta E/E$ may again approach infinity and then become negative. As illustrated in Fig. 31, which shows variations in $\Delta E/E$ as a function of X for a V_{ee} of 3.0 volts and $D_1 = 3$, this condition can produce large positive coefficients. These coefficients are somewhat smaller when a higher V_{ee} is employed, as shown in Fig. 32 for $V_{ee} =$ 6.0 volts.

When $D_2 = 3$, Eq. (59) can be written as follows:

$$M = \frac{X}{(3 + D_1)\left(X - \frac{2}{3 + D_1}\right)} \tag{65}$$

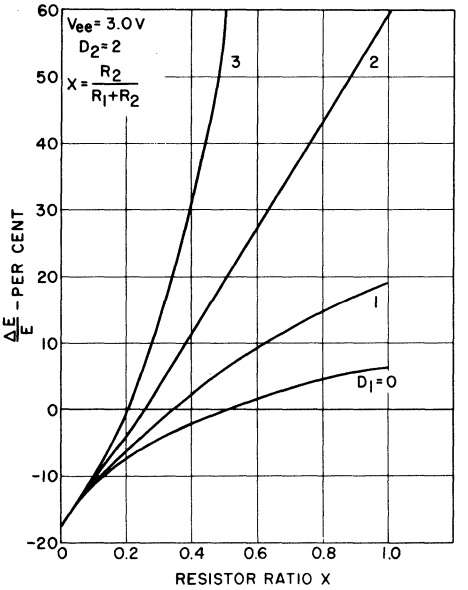


Fig. 31 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when two diodes D_2 are used.

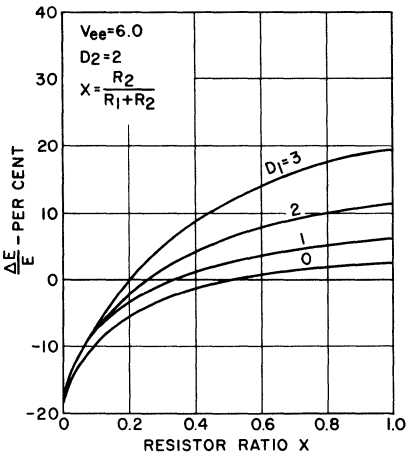


Fig. 32 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when two diodes D_2 are used.

The results for this condition are similar to those obtained for $D_2 = 2$, except that the points of the zero-temperature effect are shifted to higher values of X. The results for $D_2 = 3$ are illustrated in Figs. 33 and 34.

The simplest arrangement that results in a zero temperature coefficient is defined by the conditions $D_2 = 2$ and $D_1 = 0$. For these conditions, only two diodes are used, and the zero-temperature effect is obtained for $X = 0.5$. Little need then exists for the use of more diodes, particularly in view of the fact that the requirement for high positive coefficients is fulfilled by the condition $D_1 = D_2 = 0$, which does not require the use of any diodes.

Gain-Control Characteristics

More precise expressions than those thus far presented must be derived for the operating point and gain of a differential pair of transistors operated with a transistor current sink before an intelligent selection of the parameters for the sink circuit can be made.

Operating-Point Considerations — Eqs. (5) and (54) are used to obtain the following definition for the collector currents of the differential pair of transistors at the operating point:

$$I_{c1} = I_{c2} = \frac{\alpha^2}{2}\left(\frac{E}{R_t}\right) \tag{66}$$

The voltage drop across the collector load resistor of each transistor is given by

$$I_c R_L = \left(\frac{\alpha^2}{2}\right)\left(\frac{ER_L}{R_t}\right) \tag{67}$$

If U is used to represent the ratio R_L/R_t, Eq. (67) may be rewritten as follows:

$$I_c R_L = \left(\frac{\alpha^2}{2}\right) EU \tag{68}$$

For a given positive collector supply voltage V_{cc}, the collector voltage V_{oc} of each transistor at the operating point is given by

$$V_{oc} = V_{cc} - \left(\frac{\alpha^2}{2}\right) UE \tag{69}$$

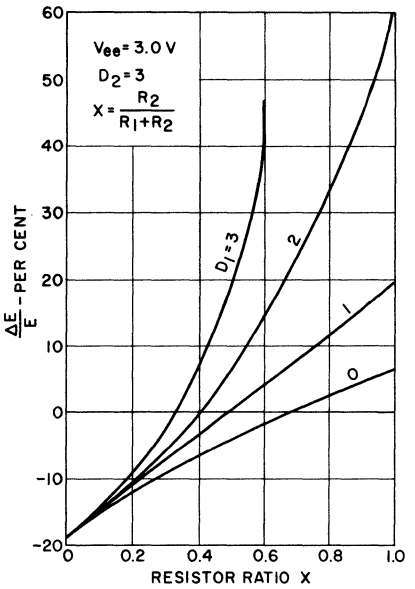


Fig. 33 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when three diodes D_2 are used.

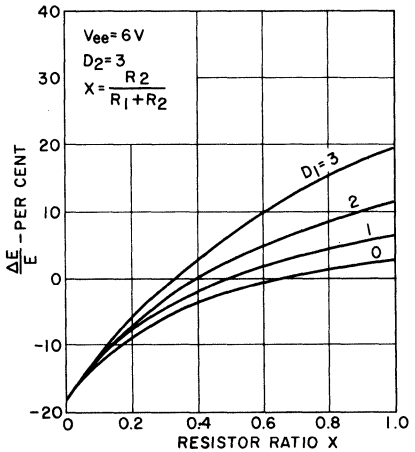


Fig. 34 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when three diodes D_2 are used.

When an output emitter follower is used, the output voltage becomes

$$V_{oc} = V_{ec} = \left(\frac{\alpha^2}{2}\right) UE - V' \tag{70}$$

The gain G of each transistor at the operating point is equal to $|g_m R_L|$. On the basis of the relationships given by Eqs. (36), (54) and (67), this parameter can be defined as follows:

$$|G| = |g_m R_L| = \frac{\alpha U}{2\left[\frac{(1-\alpha) r_b' + (r_{ec} + R_e)}{R_t}\right] + \frac{4h}{\alpha E}} \tag{71}$$

Substitution of Eq. (58) into Eqs. (69) and (70) yields the following results:

$$V_{oc} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + V_o\left(\frac{\alpha^2}{2}\frac{UX}{M}\right) + \frac{C\triangle T\alpha^2}{2}\left(\frac{UX}{M}\right) \tag{72}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2 UXV_{ee}}{2} + V_o\left(\frac{\alpha^2 U}{2}\frac{X}{M} - 1\right) - C\triangle T\left(1 - \frac{\alpha^2 UX}{2M}\right) \tag{73}$$

For the conditions $D_1 = D_2 = 0$ and $X/M = 1$, Eqs. (72) and (73) may be rewritten as follows:

$$V_{oc} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + \frac{V_o\alpha^2 U}{2} + C\triangle T\frac{\alpha^2 U}{2} \tag{74}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + V_o\left(\frac{\alpha^2 U}{2} - 1\right) - C\triangle T\left(1 - \frac{\alpha^2 U}{2}\right) \tag{75}$$

For the conditions $D_1 = 0$, $D_2 = 2$, and $X/M = 0$, the equations for V_{oc} and V_{oe} become

$$V_{oc} = V_{cc} - \frac{\alpha^2 U}{2} X V_{ee} \tag{76}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} - V_o - C\triangle T \tag{77}$$

Eqs. (74) through (77) show that the operating point for the differential amplifier is dependent upon the resistor ratios U

and X, upon the dc supply voltages V_{cc} and V_{ee}, and upon the α of the transistors.

Gain-Temperature Relationships — With the exception of α and U, which are expected to vary by small amounts with temperature, the only temperature-dependent terms in the expressions for the output voltage are those multiplied by $C\Delta T$. For the conditions under which Eq. (76) is applicable (i.e., $D_1 = 0$, $D_2 = 2$, and $X/M = 0$), the output-voltage equation contains no temperature-dependent terms except α and U. For the condition $D_1 = D_2 = 0$, Eq. (75) indicates the possibility of zero temperature coefficient for the output voltage of the differential amplifier when an output emitter follower is used and $\alpha^2U/2$ approaches unity. For this condition ($D_1 = D_2 = 0$), the gain relationship, Eq. (71), becomes

$$|G| = \frac{\alpha U}{\frac{2R_{te}\,U}{R_e} + \frac{4KT\left(1 + \frac{\Delta T}{T_o}\right)}{q\,(V_{ee}X - V_o - C\Delta T)}} \tag{78}$$

where T_o represents the room temperature, ΔT is the amount of deviation in °C from the room temperature, and R_{te} is given by

$$R_{te} = (1 - \alpha)r_b' + (r_{ec} + R_e) \tag{79}$$

At room temperature (20°C), the gain is given by

$$|G|_{20°C} = \frac{\alpha\,U}{\frac{R_{te}\,U}{R_L} + \frac{4K\,T_o}{\alpha q\,(V_{ee}\,X - V_o)}} \tag{80}$$

For the conditions used to obtain Eq. (76), i.e., $D_1 = 0$ and $D_2 = 2$, the general gain equation is as follows:

$$|G| = \frac{\alpha U}{\frac{2R_{te}\,U}{R_L} + \frac{4KT_o\left(1 + \frac{\Delta T}{T_o}\right)}{\alpha q\,V_{ee}\,X}} \tag{81}$$

At room temperature, this equation reduces to

$$|G|_{20°C} = \frac{\alpha\,U}{\frac{2R_{te}\,U}{R_L} + \frac{4KT_o}{\alpha q\,V_{ee}\,X}} \tag{82}$$

The gain of the differential amplifier is thus found to depend upon the resistor ratios U, X, and R_{te}/R_L, upon α, and upon the dc supply voltage V_{ee}.

Relative Merits of the Various Operating Modes — The variations in α and in α^2 with temperature are shown in Figs. 35 and 36, respectively. The effect of temperature on the resistance ratio U is shown in Fig. 37 for several values of resistor R_3 and a medium beta. The effect of different values of beta on the temperature dependence of the ratio U is shown in Fig. 38 for a resistor R_3 of 1000 ohms.

The graphical data presented in Figs. 35 through 38, together with the relationships expressed by Eqs. (74) through (82), permit certain conclusions to be drawn about differential-amplifier integrated circuits. On the basis of the these conclusions, the relative merits of the various operating modes in the current-sink circuit can be evaluated with respect to the effects of temperature variations on the operating point and gain of differential-amplifier integrated circuits.

For the basic differential-amplifier circuit in which no output emitter follower is employed, Eq. (76) shows that when temperature-compensating diodes are used, the basic shift in the operating point with a change in temperature results entirely from a variation in α with temperature. Such α-caused shifts in the operating point result in small negative changes in the output voltage as the temperature increases.

When the compensating diodes are not used, Eq. (74) indicates that the decrease in output voltage will be more pronounced for the same increase in temperature. This condition is implied by the fact that the last term in Eq. (74) is negative for a rise in temperature. Although the amount of change in voltage can never become zero, it can be reduced by an increase in the value of resistor R_3.

When the emitter-follower output is used, the "diodes in" mode of operation can result in partial or complete cancellation of the negative-going decrease in voltage that occurs with rises in temperature. The degree of cancellation is dependent upon the values of U, X, and V_{ee}. For low values of V_{ee}, the trend may well be a rise in output voltage with temperature.

In the "diodes out" mode of operation, the change in output voltage with temperature, is also largely dependent on the ratio U. If $\alpha^2U/2$ is greater than 1, the temperature coefficient of the output voltage may be negative. If $\alpha^2U/2$ is approximately equal to 1, the "diodes out" performance approaches the "diodes in" performance because the temperature-sensitive terms become very small and the variation of α with temperature is the only

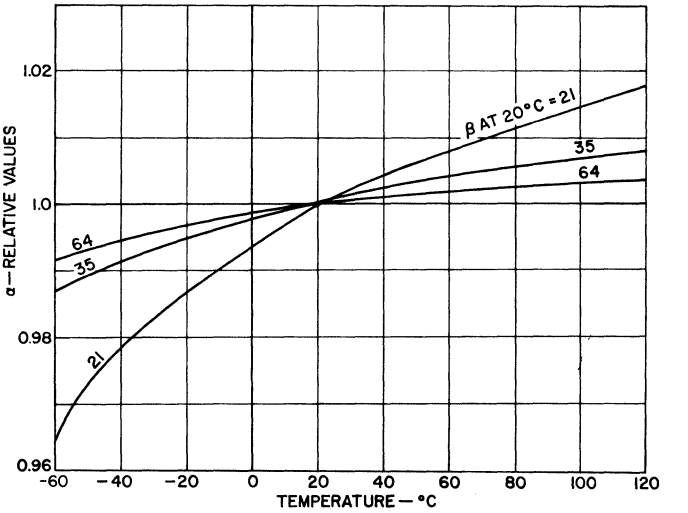


Fig. 35 — Relative values of the alpha for the current-sink transistor as a function of temperature for several beta values.

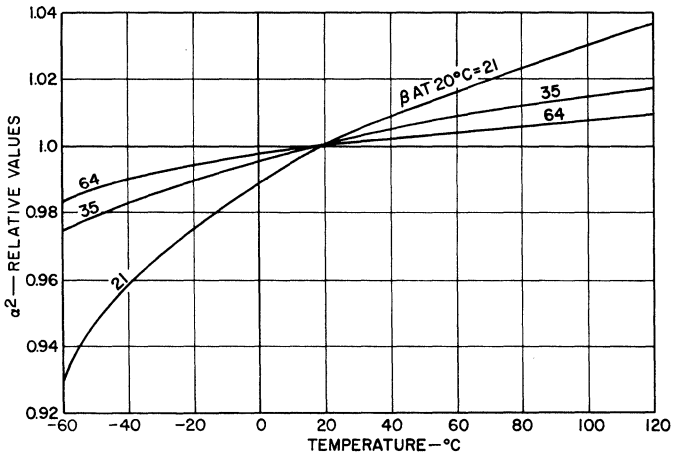


Fig. 36 — Relative values of the square of the alpha for the current-sink transistor as a function of temperature for several beta values.

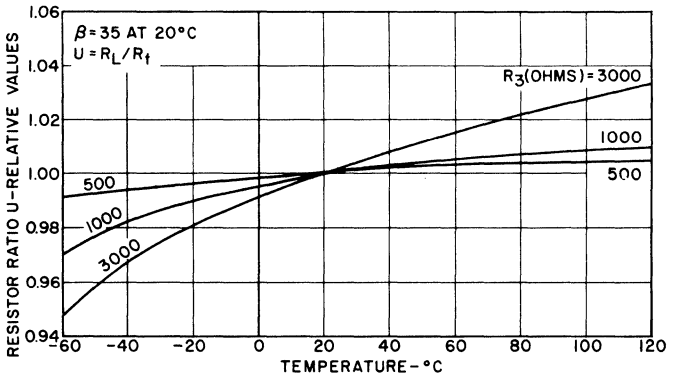


Fig. 37 — Resistor ratio U as a function of temperature for several values of the emitter resistor (R_3) of the current-sink transistor.

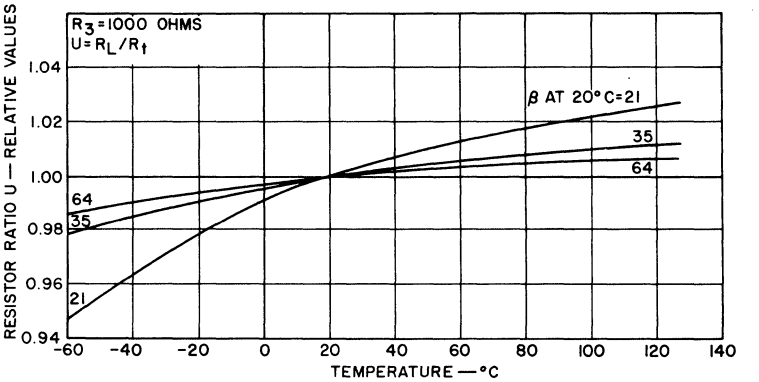


Fig. 38 — Resistor ratio U as a function of temperature for several values of the beta for the current-sink transistor.

determining factor. If $\alpha^2 U/2$ is substantially less than 1, the positive-temperature-coefficient terms should predominate, and an operating point that rises with increases in temperature will result.

Eq. (78) indicates that the basic decrease in g_m as the temperature rises (because of the KT/q term) can be cancelled or overcome if the value selected for the supply voltage V_{ee} or for the ratio X is low enough. This condition implies that, with the diodes out of the circuit, the gain can be made to decrease, remain constant, or increase with an increase in temperature.

With the diodes in the circuit, the decrease in gain with rises in temperature is not compensated and is about 2 dB per 100°C rise for very small values of the emitter resistors R_e. These emitter resistors tend to diminish the difference in the temperature characteristic for operation with the diodes in and with the diodes out. Thus, in circuits in which the external emitter resistors are not used, a greater difference will be observed for the two conditions in both gain and operating-point temperature dependence.

Even if there were no significant difference in the temperature characteristics of the two modes of operation, the inclusion of the diodes would be worthwhile because they allow a change in operating point without substantial change in the ratio X, as would be necessary if diodes were not used. Such variation in the ratio X could result in very undesirable temperature characteristics for some operating points as shown in Figs. 30 and 31.

Selection of Parameters for the Current-Sink Circuit

Equations have been derived to show the dependence of the gain and operating point of the differential-amplifier integrated circuits on temperature. These equations, which have been verified experimentally, provide accurate predictions of the characteristics of these important parameters with changes in temperature. Engineering judgment can then be used to specify all resistor ratios for any given combination of gain, operating point, and supply voltage.

Absolute values for the collector load resistor R_L and the resistor combination R_t are established by the bandwidth requirements of the circuit. The absolute value of the resistors R_1 and R_2, which determines the ratio X, is not controlled except as required by the following practical considerations:

1. The power dissipated in the bias circuit is inversely proportional to the absolute values of the resistors R_1 and R_2. Thus, the smaller the absolute values of the resistors, the higher the power dissipated in the bias circuit becomes.
2. The dependence of the ratio U on beta is reduced as the absolute values of the resistors R_1 and R_2 are decreased. Thus, the smaller the resistors are, the smaller the variations in U with changes in beta.

These conflicting considerations indicate that a compromise is required in the selection of the absolute values of R_1 and R_2.

Another factor that must be considered, before a final decision of the absolute value of R_1 is made, is the effect of the impedance in the base circuit on the output impedance of the current-sink transistor.

The output impedance of the current-sink transistor is both finite and frequency-dependent, rather than infinite and constant with frequency as implied in an ideal current source. Moreover, the output impedance is dependent upon the input impedance because of the non-unilateral characteristic of the current-sink transistor.

The output impedance must be high compared to the parallel emitter input impedances of the differential pair of transistors; otherwise, the current-source requirements are not met. Also, the common-mode gain is simply one-half the ratio of the differential-amplifier collector resistor to the equivalent impedance feeding the emitters. Because the common-mode gain in a differential amplifier should be as low as possible, the larger the impedance of the current source, the higher the common-mode rejection should be. (Common-mode rejection is the ratio of the differential gain to the common-mode gain.)

A quantitative evaluation of the output impedance and its dependence on the base resistor values may be made with the help of a transistor model. The model that best represents the integrated-circuit transistor used in the linear analog (differential-amplifier) integrated-circuits is shown in Fig. 39. In this model, the substrate series resistance R_s is small enough so that its effect is negligible below frequencies of 100 MHz. The substrate-to-collector leakage

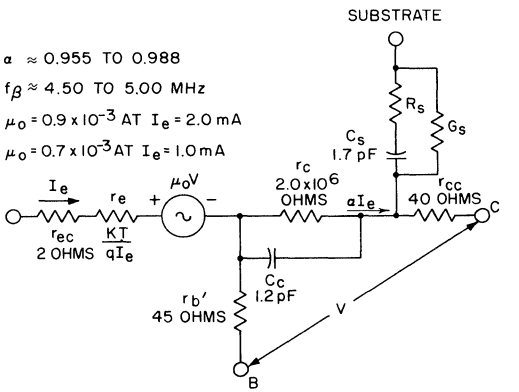


Fig. 39 — Equivalent-circuit model of an integrated-circuit transistor.

G_s is small, but not necessarily negligible, and therefore is represented.

From this model, the output admittance Y_{out} of a common-emitter single stage that has a base termination admittance of P times the common-emitter short-circuit input admittance is given by the following equation:

$$Y_{out} = G_s + j\omega C_s = \frac{\alpha U_o}{D}\frac{P}{1+P} + \frac{1}{DZ_c}\left[R_e + r_b' + \frac{\beta R_e}{1+P}\right] \quad (83)$$

where

$$D = R_e + (1-\alpha)r_b' \approx R_e \quad (84)$$

and R_e includes any external emitter resistor plus the internal emitter resistances r_{ec} and r_e. When Eq. (84) is substituted in Eq. (83), the expression for Y_{out} becomes

$$Y_{out} = G_s + j\omega C_s = \frac{\alpha U_o}{r_e}\frac{P}{1+P} - \frac{1}{Z_c}\left[1 + \frac{r_b'}{R_e} + \frac{\beta}{1+P}\right] \quad (85)$$

Fig. 40 shows the low-frequency output impedance of the current-sink transistor as a function of the base terminating resistance for various values of the emitter resistor. It is evident that the smaller the termination resistance in the base, the higher

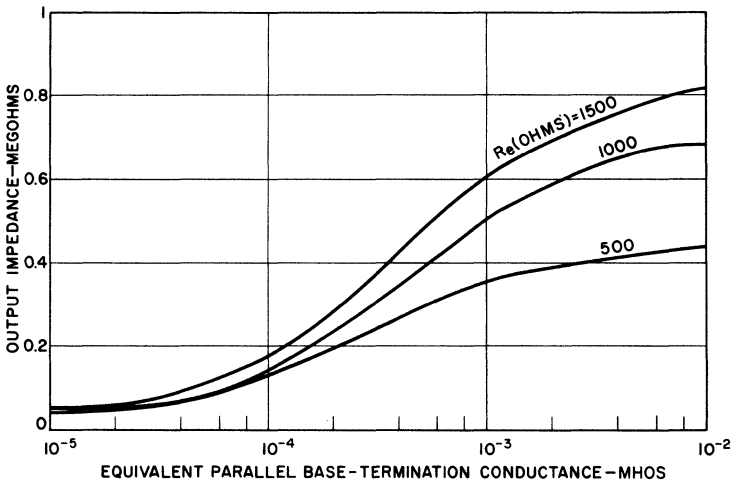


Fig. 40 — Low-frequency output impedance of the current-sink transistor as a function of the equivalent parallel base-termination conductance for several values of the emitter resistance.

the output impedance becomes. The selection of a very small resistor, however, is precluded by the high power dissipation that results in the base bias network.

Fig. 41 shows that the absolute value of output impedance varies inversely with frequency, primarily because of the collector capacitances. Even at frequencies as high as 100 MHz, the im-

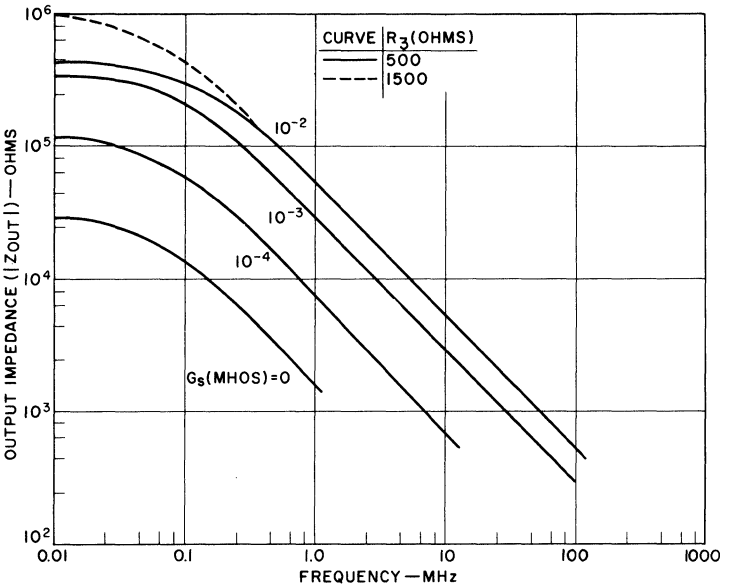


Fig. 41 — Absolute value of output impedance of the current-sink transistor as a function of frequency for several values of the base-termination conductance.

pedance is several hundred ohms for a base terminating conductance of 1 millimho (i.e., $G_s = 10^{-3}$ mho). This relatively high impedance, which is many times greater than the emitter impedances at the junctions of the differential pair of transistors, implies that, although the common-mode rejection will not be as high as desired at 100 MHz, the signal path will not be appreciably shunted by the constant current-sink transistor.

Fig. 42 shows the effects of the emitter resistor on the rate of the inverse change in output impedance with frequency. In effect, the larger the value selected for the emitter resistor, the higher the low-frequency output impedance becomes, and the

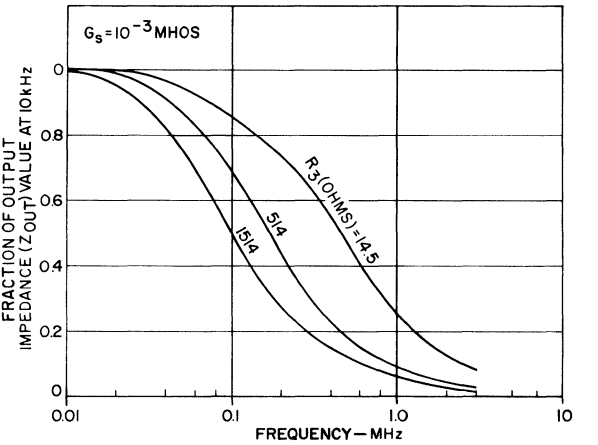


Fig. 42 — Effect of the emitter resistor (R_3) of the current-sink transistor on the change in output impedance with frequency.

lower the frequency at which the roll-off caused by the collector capacitances occurs.

Figs. 43 and 44 show that the phase angle of the output reaches 90 degrees (the condition which represents a pure capacitive output impedance) at a frequency of a few megahertz.

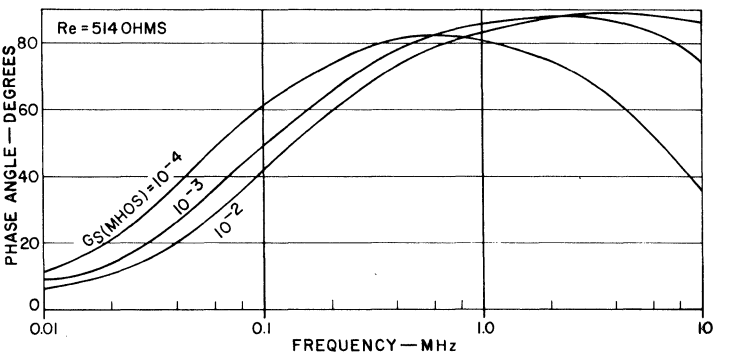


Fig. 43 — Output-impedance phase angle of the current-sink transistor as a function of frequency for several values of base-termination conductance.

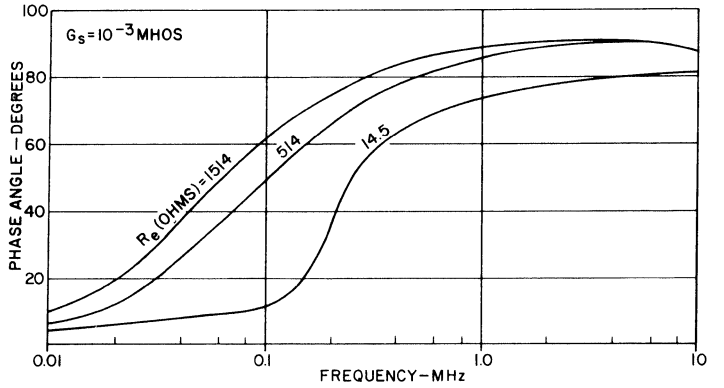


Fig. 44 — Output-impedance phase angle of the current-sink transistor as a function of frequency for several values of emitter resistance.

The curves in these figures also show the relative effects of the emitter resistor and the base-termination resistance on the relationship between frequency and phase angle.

The variation in the power dissipated in the base bias network as a function of the sum of the base bias resistors, for a supply voltage V_{ee} of 6 volts, is shown in Fig. 45. The sum of

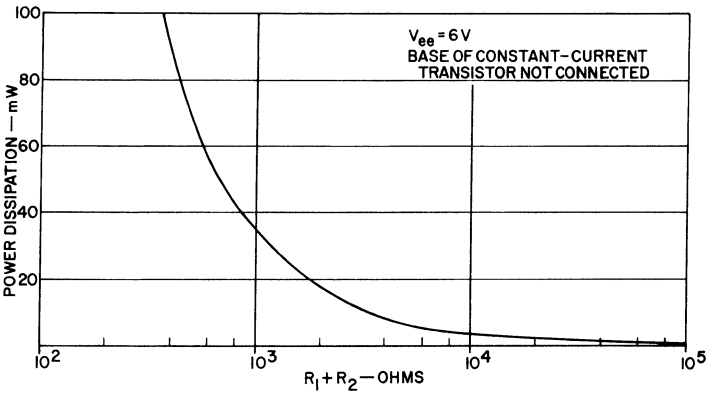


Fig. 45 — Power dissipation in the bias network of the current-sink transistors as a function of the sum of base-bias resistors R_1 and R_2.

the base-bias resistors, R_1 and R_2, should be greater than 7000 ohms to limit the dissipation to less than 5 milliwatts.

On the basis of these considerations, the final values for the parameters in the current-sink circuit can be selected. The value of the resistor R_1 is chosen as 5000 ohms. For the conditions $D_1 = 0$ and $D_2 = 2$ ("diodes in" mode of operaton), the ratio X is 0.5, and R_2 is also 5000 ohms. The sum $R_1 + R_2$ then is 10,000 ohms. The equivalent base termination resistance R_1X can be calculated as follows:

$$R_1X = R_1\left(\frac{R_2}{R_1 + R_2}\right) = 2500 \text{ ohms}$$

At a temperature of 20°C and for a transistor beta of 35, the quantity $(1 - \alpha)\ R_1X$ is about 70 ohms, which is more than 10 per cent of the value of a 500-ohm emitter resistor but only about 3 per cent of the value of a 3000-ohm emitter resistor.

For the "diodes out" mode of operation ($D_1 = D_2 = 0$), if the value of R_1 is again 5000 ohms and the ratio X is 0.36, R_1X is 1800 ohms. The quantity $(1 - \alpha)\ R_1X$ then represents a resistance of 50 ohms. The ratio R_1/R_2, as determined from Eq. (53), is 1.78, and the value of R_2 becomes 2800 ohms. The sum $R_1 + R_2$ is then 7800 ohms.

The circuit adopted as the final configuration for the transistor constant-current sink is shown in Fig. 46. This circuit

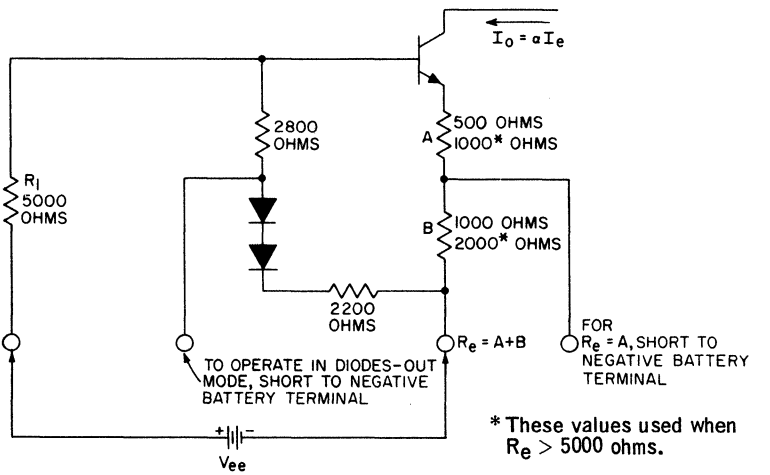


Fig. 46 — Current-sink configuration used in linear (differential-amplifier) integrated circuits.

which includes provisions for both modes of operation ("diodes in" and "diodes out") is used as the standard constant-current sink for RCA linear integrated circuits. Circuits that have a high value of collector load resistance (i.e., low-frequency, high-gain circuits) require larger values of emitter resistors than circuits that have low values of collector load resistance. The resistor values for each operating condition are indicated on the circuit schematic shown in Fig. 46.

Integrated-Circuit Operational-Amplifier Configuration

An operational amplifier is basically a very-high-gain direct-coupled amplifier which uses feedback for control of response characteristics. This circuit can be used to synthesize a broad variety of intricate transfer functions and thus can be adapted for use in many widely diverse applications. The operational amplifier is principally used to perform various mathematical functions, such as differentiation, integration, analog comparisons, and summation. This versatile circuit, however, may also be used for numerous other applications that have significantly different transfer and response requirements. For example, the same operational amplifier may be adapted to provide either the broad, flat frequency-gain response required of video amplifiers or the peaked responses required of various types of shaping amplifiers.

GENERAL CONSIDERATIONS

The configuration most commonly used for operational amplifiers is a cascade of two differential-amplifier circuits, such as that described in the preceding section, together with an appropriate output stage. The cascaded differential-amplifier stages not only fulfill the operational-amplifier requirement for a high-gain direct-coupled amplifier circuit, but also provide significant advantages with respect to the application of the operational amplifier.

From an applications standpoint, the versatility of an operational amplifier that has a differential input is substantially greater than that of the single-input type of operational amplifier. The increased versatility of the differential-input operational amplifier results from the greater flexibility allowed in the selection of the

feedback configuration. In the single-input operational amplifier, only the inverting type of feedback configuration can be employed. When differential inputs are employed, the operational amplifier may use either an inverting feedback configuration or a noninverting feedback configuration, which is dependent upon the common-mode rejection for its negative feedback. The characteristics of an operational amplifier may differ significantly depending upon the type of feedback used. The two types, therefore, tend to complement each other. Moreover, because the characteristics provided by each feedback configuration are required equally often, the differential-input operational amplifier is, from an applications standpoint, twice as versatile as the single-input operational amplifier.

The differential-input operational amplifier is readily adapted to integrated-circuit construction techniques. As pointed out in the preceding section, a differential-amplifier circuit is a stable dc-amplifier configuration that lends itself particularly well to the monolithic diffusion process used in the construction of the silicon integrated circuits. In addition, symmetrical differential-amplifier stages can be dc-cascaded readily, provided that each succeeding stage is driven push-pull by the preceding stage. The common-mode effects that result from this arrangement make possible stable, direct-coupled cascades.

The capabilities and limitations of operational amplifiers are firmly defined by a few very simple equations and rules, which are based on a certain set of criteria that an operational amplifier must meet. Effective use of these simple relationships, however, requires knowledge of the conditions under which each is applicable so that errors that may result from various approximations are held to a minimum. This section explores the theory of the design and use of operational amplifiers, and develops each pertinent design equation in a general way. Evaluations are then made to determine the assumptions that must be made (or the criteria the operational amplifier must meet) to reduce these general equations to classical operational-amplifier design equations.

Frequency instabilities in the operational amplifier and the methods used to prevent them are also discussed. A thorough understanding of the principles of frequency stability is imperative to the successful application of operational amplifiers. The basic concepts and techniques involved in phase compensation (frequency stabilization) are explained in terms of (1) basic frequency-

stability requirements, (2) the problems that may result from an uncontrolled frequency response, and (3) the techniques that may be used to correct these undesirable effects. (Specific applications of practical integrated-circuit operational amplifiers are described in a subsequent section.)

Finally, the basic criteria for an operational amplifier are given. This discussion is placed last because a basic insight to the theory of application is required before the effects of many of the operational-amplifier requirements can be fully appreciated.

BASIC THEORY OF OPERATIONAL AMPLIFIERS

In the development of the basic equations and concepts associated with the use of operational amplifiers, the precise formulations for the transfer functions, the input impedances, the output impedances, and the loop gains are presented for both the inverting and the noninverting feedback configurations, and classical design equations are then derived from these precise formulations. The effects of the load impedance and of common-mode gain (or common-mode rejection) on the inverting and noninverting feedback configurations are considered separately.

Inverting Feedback Configuration

An operational amplifier operated with an inverting feedback configuration is shown in Fig. 47. The load resistor R_L is assumed

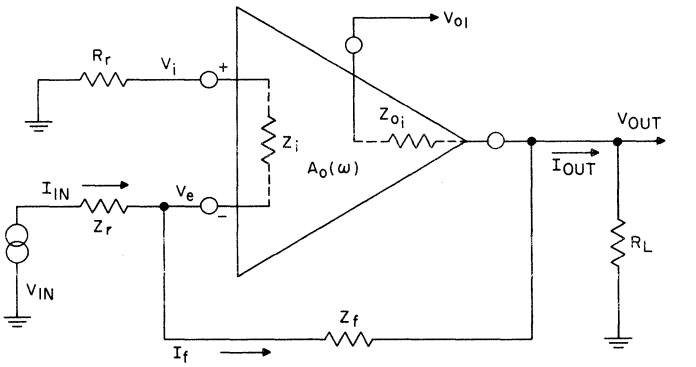


Fig. 47 — Inverting-feedback operational-amplifier configuration.

to be large enough so that its effect on the transfer characteristic is negligible, i.e., $I_{OUT} = 0$. (The effects of a finite R_L are in-

vestigated and evaluated subsequently in the discussion of the equivalent-circuit model of an operational amplifier.)

Certain differential-input operational amplifiers require a significant flow of bias current at each input. For this condition, the dc paths to ground for each input must be equal so that a minimum dc offset voltage (error) is developed at the output. Thus, for the terminology employed in Fig. 47, R_r must equal the parallel combination of $Z_r(\omega = 0)$ with the series combination of $Z_f(\omega = 0)$ and Z_{oi} $(\omega = 0)$.

In the circuit of Fig. 47, the drive-source impedance affects the feedback in the inverting configuration and, therefore, must be considered part of the Z_- term. For brevity, the symbol Z_r is defined to include the source impedance as well as certain feedback design elements. The impedances Z_i and Z_{oi} are the open-loop *intrinsic* input and output impedances of the operational amplifier. Ordinarily, these impedances are assumed in the amplifier symbol. In Fig. 47, however, they are identified to emphasize their importance in the ensuing equations. The term $A_o(\omega)$ is the open-loop differential voltage gain of the operational amplifier; this parameter is frequency-dependent. The terminals on the operational-amplifier symbol labeled minus $(-)$ and plus $(+)$ refer to the inverting and noninverting input, respectively.

Inverting-Configuration Transfer Function — The transfer function or closed-loop gain of an operational amplifier is generally considered to express the relationship between the input and output voltages. (It is relatively simple to convert the voltage transfer function to another desired transfer relationship.) In the derivation of the transfer function for the schematic in Fig. 47, the following differential-amplifier relationship is used as the starting point:

$$V_{o1} = -A_o(\omega)\,(V_e - V_i) \tag{86}$$

where V_e and V_i are defined as follows:

$$V_e = \frac{V_{IN}\,(Z_f+Z_{oi})/\!/(Z_i+R_r)}{Z_r + (Z_f+Z_{oi})/\!/(Z_i+R_r)} + \frac{V_{o1}\,Z_r/\!/(Z_i+R_r)}{Z_f + Z_{oi} + Z_r/\!/(Z_i+R_r)} \tag{87}$$

and

$$V_i = V_e\,R_r/(Z_i + R_r) \tag{88}$$

(In these and subsequent equations, the load resistor R_L is assumed to approach infinity.)

If the expressions for V_e and V_i given by Eqs. (87) and (88)

are substituted in Eq. (86), the resulting expression can be simplified as follows:

$$V_{o_1} = \frac{-A_o(\omega)\, Z_i\, (Z_f + Z_{o_i})\, V_{IN}}{(Z_f + Z_{o_i})\, (Z_i + R_r) + Z_r\, (Z_f + Z_{o_i} + Z_i + R_r) + A_o(\omega) Z_i\, Z_r} \tag{89}$$

The output voltage V_{OUT} is expressed in terms of V_{o_1} and V_{IN} by the following equation:

$$V_{OUT} = \frac{V_{o_1}\, [Z_f + Z_r /\!\!/ (Z_i + R_r)]}{Z_{o_i} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN}\, Z_{o_i}\, (Z_f + Z_{o_i}) /\!\!/ (Z_i + R_r)}{(Z_f + Z_{o_i})\, [Z_r + (Z_f + Z_{o_i}) /\!\!/ (Z_i + R_r)]} \tag{90}$$

With V_{o_1} defined as indicated by Eq. (89), the accurate equation for the transfer response (for $R_L \rightarrow \infty$) becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{o_i}\, (Z_i + R_r) - A_o(\omega)\, Z_i\, Z_f}{(Z_f + Z_{o_i})\, (Z_i + R_r) + Z_r\, (Z_f + Z_{o_i} + Z_i + R_r) + A_o(\omega)\, Z_i Z_r} \tag{91}$$

If Z_i is assumed to be much greater than the combination of Z_r in parallel with $Z_f + Z_{oi}$, and if Z_{oi} is assumed to be much smaller than Z_f, then the closed-loop gain (or transfer function) may be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{-A_o(\omega)\, Z_f}{Z_f + Z_r + A_o(\omega)\, Z_r} \tag{92}$$

In addition, if the open-loop gain $A_o(\omega)$ is the dominant term in either Eq. (91) or (92), the transfer-function equation for the inverting configuration simplifies to the following familiar expression:

$$\frac{V_{OUT}}{V_{IN}} \underline{\underline{\quad A_o(\omega) \rightarrow \infty \quad}} - \frac{Z_f}{Z_r} \tag{93}$$

Eq. (93) is considered to be the classical or ideal expression for the closed-loop gain (transfer function) for an operational amplifier that uses the inverting type of feedback configuration.

The difference between the open-loop gain and the closed-loop gain is in itself an important design parameter. This "gain throwaway", which is known as the loop gain L.G., is defined by the following equation:

$$\text{L. G.} = \frac{\text{open-loop gain, } A_o(\omega)}{\text{closed-loop gain, } \dfrac{V_{OUT}}{V_{IN}}} \tag{94}$$

When the transfer function is given by Eq. (92), the loop-gain equation may be written as follows:

$$\text{L. G.} = -\frac{Z_f + Z_r}{Z_f} - \frac{A_o(\omega)}{\frac{Z_f}{Z_r}} \tag{95}$$

Moreover, when the open-loop gain is very large, the inverting loop gain can be considered to be the open-loop gain divided by the *ideal* inverting closed-loop gain. The equation for L.G. then becomes

$$\text{L. G.} \doteq \frac{-A_o(\omega)}{\frac{Z_f}{Z_r}} \tag{96}$$

The loop-gain parameter can be used to predict the accuracy of the approximate operational-amplifier relationships. In general, the higher the loop gain, the more accurate the results provided by the approximate (or classical) relationships. This correlation is demonstrated in Table I, which compares values of V_{OUT}/V_{IN} obtained from the precise transfer expression, Eq. (91), with

Table I—*Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Inverting Configuration)*

Conditions: $A_o(\omega) = 1000\ \underline{/0°}$, $Z_i = 15{,}000\ \underline{/0°}$, $Z_{o_i} = 200\ \underline{/0°}$, $Z_r = 1000\ \underline{/0°}$.

$Z_f\ \underline{/0°}$ (ohms)	V_{OUT}/V_{IN} from Eq. (83) (dB)	V_{OUT}/V_{IN} from Eq. (91) (dB)	Error (dB)	L.G. (dB)
200,000	46.0	44.3	1.70	14.0
100,000	40.0	39.1	0.90	20.0
30,000	29.6	29.3	0.30	30.4
10,000	20.0	19.9	0.10	40.0
2,000	6.03	6.0	0.03	54.0

values obtained from the classical approximation, Eq. (93), for various gain settings. The tabular data show that the classical equation is accurate to within 1 dB provided the loop gain is at least 20 dB. Eq. (96) was used to calculate all of the loop-gain values given in the table.

Inverting-Configuration Input Impedance, Z_{IN} — The input impedance Z_{IN} for the inverting-feedback configuration of an operational amplifier, shown in Fig. 47, can be expressed as follows:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{97}$$

where

$$I_{IN} = \frac{V_{IN} - V_e}{Z_r} \tag{98}$$

Therefore,

$$Z_{IN} = \frac{Z_r}{1 - \frac{V_e}{V_{IN}}} \tag{99}$$

The ratio V_e/V_{IN} may be determined by substituting the expression for V_{o_1} given by Eq. (89) into Eq. (87) and dividing through by V_{IN} (with $R_L \rightarrow \infty$.) The resultant equation is then simplified to obtain the following relationship:

$$\frac{V_e}{V_{IN}} = \frac{(Z_f+Z_{o_i})\,(Z_i + R_r)}{Z_r\,(Z_f+Z_{oi}+Z_i+R_r) + Z_f+Z_{o_i})\,(Z_i+R_r) + A_o(\omega)Z_i\,Z_r} \tag{100}$$

If this expression for V_e/V_{IN} is substituted into Eq. (99), the result can be simplified to obtain the following precise expression for the closed-loop input impedance:

$$Z_{IN} = Z_r + \frac{Z_r\,(Z_{o_i}\,Z_i + Z_fR_r + Z_f\,Z_i)}{Z_r\,(Z_f+Z_{o_i}+Z_i) + R_r\,(Z_r+Z_{o_i}) + A_o(\omega)Z_i\,Z_r} \tag{101}$$

If $A_o(\omega)$ is dominant and Z_{o_i} is small, Eq. (101) reduces to

$$Z_{IN} \doteq Z_r + \frac{Z_f\,(Z_i + R_r)}{A_o(\omega)\,Z_i} \tag{102}$$

A further simplification is possible when R_r is much smaller than Z_i, which is a common condition. In this case, the equation for the input impedance becomes

$$Z_{IN} \doteq Z_r + \frac{Z_f}{A_o(\omega)} \tag{103}$$

Eqs. (102) and (103), which are important in voltage-summing or scaling-adder* applications, can be used to predict the degree of interaction among multiple inputs.

When $A_o(\omega)$ is large enough, Eqs. (102) and (103) may be rewritten as follows:

$$Z_{IN} \xrightarrow{A_o(\omega)\rightarrow\infty} Z_r \tag{104}$$

Eq. (104) is the "classical" equation for the input impedance of an operational amplifier when an inverting-feedback configuration is used. This equation, together with Eq. (101), implies the existence of a condition known as a virtual ground at the node-assigned voltage V_e (shown in Fig. 47). That is, the node is at

**A scaling adder is an inverting operational-amplifier configuration which weights and sums multiple voltages. (See Fig. 191 in section on "Characteristics and Applications of RCA Linear Integrated Circuits.")*

ground potential even though there is no electrical connection between this point and ground. [This statement can be verified either intuitively by the use of Eq. (104) or directly if $A_o(\omega)$ is assumed to be infinite in Eq. (100)]. Moreover, no current flows into the negative terminal of the amplifier when the open-loop gain is infinite because the voltage V_e is zero while the impedance at the negative terminal (i.e., $Z_i + R_r$) is not zero. The concept of a virtual ground leads to an extremely simple three-step analysis procedure for an inverting operational-amplifier configuration.

1. Because of the virtual ground ($V_e = 0$), the input current I_{IN} and feedback current I_f can be defined as follows:

$$I_{IN} = \frac{V_{IN}}{Z_r} \tag{105}$$

$$I_f = \frac{-V_{OUT}}{Z_f} \tag{106}$$

2. Zero current flow into the inverting terminal ($V_e = 0$) indicates the following relationships:

$$I_{IN} = I_f \tag{107}$$

$$\frac{V_{IN}}{Z_r} = \frac{-V_{OUT}}{Z_f} \tag{108}$$

3. Eq. (108) can then be rewritten to obtain the classical gain equation, as follows:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_f}{Z_r} \tag{109}$$

Although the foregoing analysis is certainly an idealized one, it is nevertheless practical because the required approximations are usually valid. Eq. (100) serves as a measure of the deviation from a true virtual ground.

Inverting-Configuration Output Impedance, Z_{OUT} — The closed-loop output impedance is the ratio of the unloaded output voltage V_{OUT} to the short-circuit output current I_{OUT} as follows:

$$Z_{OUT} = \frac{V_{OUT}\ (R_L \rightarrow \infty)}{I_{OUT}\ (R_L \rightarrow 0)} \tag{110}$$

It is apparent from Fig. 47 then that the output current I_{OUT} is given by

$$I_{OUT}\ (R_L \rightarrow 0) = \frac{-A_o(\omega)\ (V_e - V_i)}{Z_{oi}} \tag{111}$$

If the expression given by Eq. (88) is substituted for V_i, Eq. (111) can be rewritten as follows:

$$I_{OUT}\ (R_L \rightarrow 0) = \frac{-A_o(\omega)\ Z_i\ V_e}{Z_{oi}\ (Z_i + R_r)} \tag{112}$$

Under short-circuit conditions ($R_L = 0$), the voltage V_e in terms of V_{IN} is given by

$$V_e = \frac{V_{IN}\ Z_f /\!\!/ (Z_i+R_r)}{Z_r + Z_f /\!\!/ (Z_i+R_r)} = \frac{V_{IN}\ Z_f\ (Z_i+R_r)}{Z_r\ (Z_f+Z_i+R_r) + Z_f\ (Z_i+R_r)} \tag{113}$$

Therefore, I_{OUT} (at $R_L = 0$) can be expressed in terms of V_{IN} as follows:

$$I_{OUT} = \frac{-A_o(\omega)\ Z_i\ Z_f\ V_{IN}}{Z_{oi}\ [Z_r\ (Z_f+Z_i+R_r) + Z_f\ (Z_i+R_r)]} \tag{114}$$

If this expression for I_{OUT} is substituted in Eq. (110) and consideration is given to the intransience of V_{IN} in going from an unloaded to a fully loaded condition, the equation for Z_{OUT} becomes

$$Z_{OUT} = \frac{Z_{oi}\ [Z_r\ (Z_f+Z_i+R_r) + Z_f\ (Z_i+R_r)]}{-A_o\ (\omega)\ Z_i\ Z_f} \left(\frac{V_{OUT}}{V_{IN}}\right) \tag{115}$$

Finally, the desired equation for the closed-loop output impedance is obtained if the expression for V_{OUT}/V_{IN} given by Eq. (91) is substituted into Eq. (115), as follows:

$$Z_{OUT} = \frac{Z_{oi}[Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)][A_o(\omega)Z_iZ_f-Z_{oi}(Z_i+R_r)]}{A_o(\omega)Z_iZ_f[Z_r(Z_f+Z_{oi}+Z_i+R_r)+(Z_f+Z_{oi})(Z_i+R_r)+A_o(\omega)Z_iZ_r]} \tag{116}$$

If the open-loop gain term $A_o(\omega)$ is dominant, Eq. (116) simplifies to

$$Z_{OUT} \doteq \frac{Z_{oi}\ [Z_r\ (Z_f + Z_i + R_r) + Z_f\ (Z_i + R_r)]}{A_o(\omega)\ Z_i\ Z_r} \tag{117}$$

This expression for Z_{OUT} does not simplify to its "classical" equation unless Z_i is dominant also; in this case, Eq. (117) becomes

$$Z_{OUT} \doteq Z_{oi}\ \frac{1 + \dfrac{Z_f}{Z_r}}{A_o(\omega)} \tag{118}$$

The assumption that Z_i is a dominant term is not always valid, especially if bipolar transistor inputs are employed. Eq. (117), therefore, may be considered to take precedence over Eq. (118).

Noninverting Feedback Configuration

Fig. 48 shows the general circuit for an operational amplifier operated with a noninverting feedback configuration. In this section, the equations for the transfer function and the closed-loop

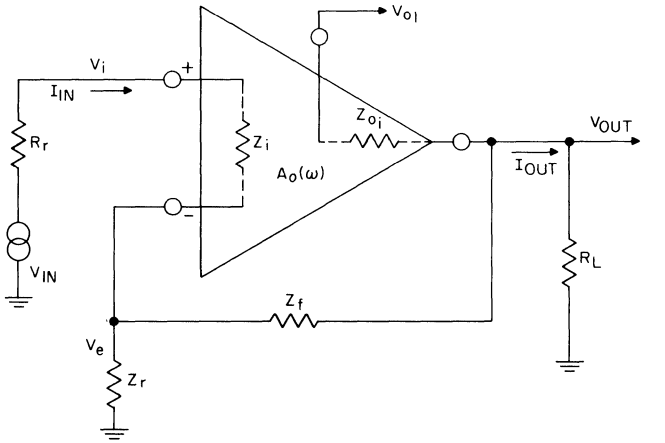


Fig. 48 — Noninverting-feedback operational-amplifier configuration.

input impedance for this type of operational-amplifier circuit are derived. These derivations, as did those for the inverting circuit, assume that the load resistor R_L is large enough so that its effect is negligible, i.e., $R_L \to \infty$ and $I_{OUT} = 0$. (The effects of a finite load resistance on the noninverting operational amplifier are evaluated in the discussion of the equivalent-circuit model of an operational amplifier.)

A noninverting operational amplifier, unlike the inverting type, requires a differential-input arrangement because it uses the common-mode effect in its feedback scheme. The following basic requirements and definitions that apply to the inverting circuit shown in Fig. 47 are also valid for the general noninverting circuit of Fig. 48:

1. The dc return paths to ground for the two inputs must be equal and finite for amplifiers that require a significant amount of input bias current.
2. The input and output impedances, Z_i and Z_{o_i}, are inherent in the basic amplifier unit and are shown on the diagram to emphasize their importance in the relationships to be derived.

3. The open-loop gain is frequency-dependent and is represented by the symbol $A_o(\omega)$.
4. The plus and minus labels on the input terminals designate the noninverting and inverting terminals, respectively.

In the noninverting circuit, however, the source impedance is included in the passive element R_r rather than the frequency-dependent parameter Z_r, as in the inverting circuit.

Noninverting-Configuration Transfer Function — As with the inverting circuit, the transfer function developed for the noninverting operational amplifier shows the relationship between the input and output voltages. It is relatively simple to convert this relationship to another type of transfer function.

When the load resistor R_L approaches infinity, the output voltage V_{OUT} for the general circuit shown in Fig. 48 can be expressed as follows:

$$V_{OUT} = \frac{V_{o1}\,[Z_f + Z_r /\!\!/ (Z_i + R_r)]}{Z_{o_i} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN}\,Z_{o_i}\,[Z_r /\!\!/ (Z_f + Z_{o_i})]}{(Z_f + Z_{o_i})\,[Z_i + R_r + Z_r /\!\!/ (Z_f + Z_{o_i})]} \tag{119}$$

Eq. (119) may be rewritten in the following form:

$$V_{OUT} = \frac{V_{o1}\,[Z_f\,(Z_r + Z_i + R_r) + Z_r\,(Z_i + R_r)] + Z_r\,Z_{o_i}\,V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i})} \tag{120}$$

The voltage V_{o_1} is defined by the differential-gain expression, as follows:

$$V_{o1} = A_o(\omega)\,(V_i - V_e) \tag{121}$$

where V_i is the source voltage V_{IN} less the voltage drop across R_r, as given by

$$V_i = V_{IN} - I_{IN}\,R_r \tag{122}$$

where

$$I_{IN} = \frac{V_i - V_e}{Z_i} \tag{123}$$

The voltage V_i, given by Eq. (122), can now be expressed in terms of the voltages V_{IN} and V_e, as follows:

$$V_i = \frac{Z_i\,V_{IN} + R_r\,V_e}{Z_i + R_r} \tag{124}$$

It can be determined from Fig. 48 that, when R_L approaches infinity, the voltage V_e is given by the following equation:

$$V_e = \frac{V_{o1}\, Z_r /\!\!/ (Z_i + R_r)}{Z_{o_i} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN}\, Z_r /\!\!/ (Z_f + Z_{o_i})}{Z_i + R_r + Z_r /\!\!/ (Z_f + Z_{o_i})} \tag{125}$$

If the relationships for V_{o1} and V_i given by Eqs. (121) and (124), respectively, are used, V_e can be expressed solely in terms of V_{IN}, as shown by the following equation:

$$V_e = \frac{(Z_r\, Z_f + Z_r\, Z_{o_i} + A_o(\omega)\, Z_i\, Z_r)\, V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\, Z_i\, Z_r} \tag{126}$$

Eqs. (121), (124), and (126) are now used to express V_{o1} in terms of V_{IN}, as follows:

$$V_{o1} = \frac{A_o(\omega)\, Z_i\,(Z_r + Z_f + Z_{o_i})\, V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\, Z_i\, Z_r} \tag{127}$$

If this expression for V_{o1} is substituted into Eq. (120), the new equation that results can be simplified and divided through by V_{IN} to obtain the desired transfer function, as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_r\, Z_{o_i} + A_o(\omega)\, Z_i\,(Z_r + Z_f)}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\, Z_i\, Z_r} \tag{128}$$

The transfer function that is usually associated with the noninverting feedback configuration of an operational amplifier can be derived from Eq. (128) if the impedance Z_{o_i} is assumed to be zero and the impedance Z_i is assumed to be very high. When these assumptions are made, Eq. (128) becomes

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{(Z_r + Z_f)\, A_o(\omega)}{(Z_r + Z_f) + Z_r\, A_o(\omega)} \tag{129}$$

Eq. (129) may be rewritten as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + Z_f/Z_r}} \tag{130}$$

If the term $A_o(\omega)$ is dominant in Eq. (130), the following "classical" expression for the noninverting transfer response results:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} 1 + \frac{Z_f}{Z_r} \tag{131}$$

The term $1 + Z_f/Z_r$ represents the closed-loop gain for the *ideal* noninverting configuration. This term, which is referred to as the *ideal feedback characteristic,* is basic to operational-amplifier frequency-stabilization theory.

As might be expected, the loop gain of an operational amplifier is defined in the same way [by Eq. (94)] regardless of the type of feedback configuration. Under the conditions for which Eq. (130) is a valid expression for the transfer response, the loop gain for the noninverting configuration is given by

$$\text{L. G.} = 1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \tag{132}$$

If the second term of Eq. (132) is very large, this equation reduces to

$$\text{L. G.} \doteq \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \tag{133}$$

Table II compares the values calculated from the precise and the approximate expressions [Eqs. (128) and (131), respectively] for the closed-loop gain of the noninverting operational-amplifier configuration. The approximate formula is accurate to

Table II—*Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Noninverting Configuration)*

Conditions: $A_o(\omega) = 1000 \angle 0°$, $Z_i = 15{,}000 \angle 0°$, $Z_{o_i} = 200 \angle 0°$, $Z_r = 1000 \angle 0°$.

$Z_f \angle 0°$ (ohms)	V_{OUT}/V_{IN} from Eq. (131) (dB)	V_{OUT}/V_{IN} from Eq. (129) (dB)	Error (dB)	L. G. from Eq. (133) (dB)
199,000	46.0	44.3	1.70	14.0
99,000	40.0	39.1	0.90	20.0
29,000	29.6	29.3	0.30	30.4
9,000	20.0	19.9	0.10	40.0
1,000	6.03	6.0	0.03	54.0

within 1 dB provided the loop gain is 20 dB or more. A comparison of Tables I and II shows that the error introduced by the use of the classical gain formula for the noninverting configuration [Eq. (131)] is identical to that introduced by the use of the classical gain formula for the inverting configuration [Eq. (93)].

Noninverting-Configuration Input Impedance, Z_{IN} — The following equation gives the basic definition of the input impedance Z_{IN}:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{134}$$

It can be readily determined from Fig. 48 that the input current I_{IN} is given by

$$I_{IN} = \frac{V_{IN} - V_e}{Z_i + R_r} \tag{135}$$

When this relationship is applied in Eq. (134), the expression for the noninverting input impedance becomes

$$Z_{IN} = \frac{Z_i + R_r}{1 - \frac{V_e}{V_{IN}}} \tag{136}$$

If the expression for the ratio of V_e/V_{IN}, given previously by Eq. (126), is substituted into Eq. (136), the result can be simplified to obtain the following precise expression for the input impedance (for $R_L \to \infty$):

$$Z_{IN} = Z_i + R_r + Z_r \frac{Z_f + Z_{o_i} + A_o(\omega)\, Z_i}{Z_r + Z_f + Z_{o_i}} \tag{137}$$

For the case where Z_i is dominant and Z_{o_i} is small, Eq. (137) reduces to

$$Z_{IN} \doteq Z_i + \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{138}$$

The following expression for the input impedance results if $A_o(\omega)$ is also considered dominant:

$$Z_{IN} \doteq \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{139}$$

Eq. (139) states that the noninverting input impedance is equal to the intrinsic input impedance Z_i multiplied by the loop gain.

Noninverting-Configuration Output Impedance, Z_{OUT} — As in the inverting configuration, the closed-loop output impedance for the noninverting configuration is defined as the ratio of the open-circuit output voltage, V_{OUT}, to the short-circuit output current, I_{OUT}, as follows:

$$Z_{OUT} = \frac{V_{OUT}\ (R_L \to \infty)}{I_{OUT}\ (R_L \to 0)} \tag{140}$$

where

$$I_{OUT}\ (R_L \to 0) = \frac{A_o(\omega)\ (V_i - V_e)}{Z_{o_i}} \tag{141}$$

For the general noninverting operational-amplifier configuration, the voltages V_i and V_e are given by the following equations for the conditions indicated:

$$V_i\ (R_L \rightarrow 0) = \frac{V_{IN}\ (Z_i + Z_r /\!\!/ Z_f)}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{142}$$

and

$$V_e\ (R_L \rightarrow 0) = \frac{V_{IN}\ Z_r /\!\!/ Z_f}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{143}$$

On the basis of the relationships expressed by Eqs. (142) and (143), Eq. (141) may be rewritten as follows:

$$I_{OUT}\ (R_L \rightarrow 0) = \frac{A_o(\omega)\ V_{IN}\ Z_i\ (Z_r + Z_f)}{Z_{o_i}\ [(Z_r + Z_f)\ (R_r + Z_i) + Z_r\ Z_f]} \tag{144}$$

The output impedance Z_{OUT} then becomes

$$Z_{OUT} = Z_{o_i}\left[\frac{Z_r\ Z_f + (Z_r + Z_f)\ (R_r + Z_i)}{A_o(\omega)\ Z_i\ (Z_r + Z_f)}\right]\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{145}$$

Finally, the following precise equation for the output impedance Z_{OUT} is obtained when the ratio for V_{OUT}/V_{IN} is replaced by its impedance equivalent, as given by Eq. (128):

$$Z_{OUT} = Z_{o_i}\ [(Z_r+Z_f)\ (R_r+Z_i) + Z_r\ Z_f]\ [Z_r\ Z_{o_i} + A_o(\omega)Z_i\ (Z_r+Z_f)] \tag{146}$$

If $A_o(\omega)$ is dominant, then Eq. (146) becomes

$$Z_{OUT} \doteq Z_{o_i}\left[\frac{Z_r\ Z_f + (Z_r + Z_f)\ (R_r + Z_i)}{A_o(\omega)\ Z_i\ Z_r}\right] \tag{147}$$

The expression for the closed-loop output impedance does not revert to its classical form unless both the intrinsic input impedance Z_i and the open-loop gain $A_o(\omega)$ are very large. Under such conditions, the equation for the output impedance reduces to

$$Z_{OUT} \doteq Z_{o_i}\frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)} \tag{148}$$

This classical expression indicates that the output impedance of the noninverting configuration is equal to the intrinsic output impedance Z_{o_i} divided by the loop gain. It should be noted that the classical expressions for the closed-loop output impedances for the inverting and noninverting configurations [Eq. (118) and (148), respectively] are identical.

Equivalent-Circuit Model of a Closed-Loop Operational Amplifier

Fig. 49 shows the equivalent circuit of a closed-loop operational amplifier. This equivalent circuit is valid for either the inverting or the noninverting configuration. In the inverting

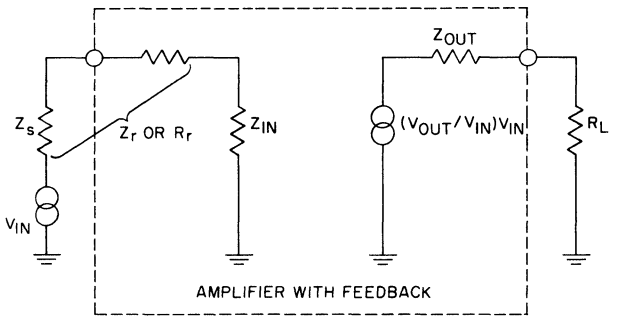


Fig. 49 — Equivalent-circuit model of a closed-loop operational amplifier.

configuration, Z_r is used to represent the impedance in series with the closed-loop input impedance Z_{IN}. In the noninverting configuration, term Z_r is replaced by R_r to show that the components thus represented are independent of frequency. The closed-loop input and output impedances (Z_{IN} and Z_{OUT}, respectively) and the transfer function V_{OUT}/V_{IN} were defined previously.

Effect of a Finite Load Impedance on Operational-Amplifier Characteristics — One of the important features of the equivalent-circuit model is that it accurately accounts for the effects of a finite load impedance, R_L. For example, if a 2000-ohm load impedance is used on the 46-dB (approximate) inverting amplifier for which data are given in Table I, the equation for the transfer response must be modified as follows:

$$V_{OUT} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) V_{IN}\, R_L}{R_L + Z_{OUT}} \tag{149}$$

If Eq. (91) is used to determine the value of V_{OUT}/V_{IN} and Eq. (115) is used to determine the value of Z_{OUT}, the transfer-function

ratio for an R_L of 2000 ohms can be calculated from Eq. (149) as follows:

$$\frac{V_{OUT}}{V_{IN}} = 164 \left(\frac{2000 \text{ ohms}}{37.4 \text{ ohms} + 2000 \text{ ohms}} \right) = 162 \qquad (150)$$

Thus, a ratio of 44.15 dB is obtained, as compared to 44.3 dB for an open-circuit load. Similarly, if a 2000-ohm load is used for the 6-dB amplifier, the gain becomes 5.98 dB, as compared to 6 dB indicated in Table I for an open-circuit load. The error in neglecting a 2000-ohm load, therefore, is 0.15 dB for the 46-dB amplifier and only 0.02 dB for the 6-dB amplifier (for the conditions given in Table I).

Effect of the Common Mode Gain (CMG) on Operational-Amplifier Characteristics — In the developments of the basic equations for the inverting and noninverting feedback configurations of the operational amplifier, it was tacitly assumed that the common-mode gain was essentially zero (infinite attenuation). The common-mode gain is defined as the ratio of the output voltage, V_{OUT}, to the input voltages, V_i and V_e, when V_i and V_e are identical in amplitude and phase. The validity of this assumption is considered separately in this section because the basic feedback equations become burdensome when common-mode effects are included. As a result, the salient features of these equations become obscured.

An examination of Figs. 47 and 48 shows that, in either the inverting or noninverting configuration, the differential gain acts on the difference between the voltages V_i and V_e. On the other hand, the common-mode gain acts on those portions of V_i and V_e that are in phase and identical in magnitude. That is, the common-mode gain acts on the smaller of the two in-phase signals (V_i or V_e). In the inverting configuration V_i is less than V_e, but in the noninverting configuration V_i is greater than V_e. These conditions are reflected by the output-voltage equations when the effects of the common-mode gain (CMG) are considered, as follows:

1. For the inverting configuration,

$$V_{o1} = A_o(\omega)(V_i - V_e) - (CMG)(V_i) \qquad (151)$$

2. For the noninverting configuration,

$$V_{o1} = A_o(\omega)(V_1 - V_e) - CMG(V_e) \qquad (152)$$

If these two equations are developed further, the following gain expressions are obtained for $Z_{o_i} = 0$ (i.e., $V_{o_i} = V_{OUT}$):

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\, Z_i\, Z_f - (CMG)\, R_r\, Z_f}{Z_r\,(Z_f+Z_i+R_r)+Z_f\,(Z_i+R_r)+Z_i\, Z_r\, A_o(\omega)+R_r\, Z_r\,(CMG)} \tag{153}$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\, Z_i\,(Z_r + Z_f) - (CMG)\, Z_r\, Z_f}{(Z_r+Z_f)\,(R_r+Z_i)+Z_r\, Z_f+A_o(\omega)\, Z_i\, Z_r+(CMG)\, Z_r\,(Z_i+R_r)} \tag{154}$$

In each case, the criteria for the common-mode gain, CMG, to be negligible compared to the open-loop gain, $A_o(\omega)$, are as follows:

1. For the inverting configuration,

$$CMG \ll \frac{A_o(\omega)\, Z_i}{R_r} \tag{155}$$

2. For the noninverting configuration,

$$CMG \ll \frac{A_o(\omega)\, Z_i}{Z_i + R_r} \tag{156}$$

Eq. (153) or inequality (155) shows that the gain of an inverting configuration is not affected by the common-mode gain when the input impedance V_i is assumed to be infinite. However, when this same assumption is made for a noninverting configuration, the gain is dependent upon the common-mode gain provided the open-loop gain is finite.

Inequalities (155) and (156) may be given in terms of the common-mode rejection, CMR, which is the open-loop gain, $A_o(\omega)$, divided by the common-mode gain, CMG. The following inequalities are then obtained:

1. For the inverting configuration,

$$CMR \ll \frac{R_r}{Z_i} \tag{157}$$

2. For the noninverting configuration,

$$CMR \gg \frac{Z_i + R_r}{Z_i} \tag{158}$$

Neither of these inequalities places a stringent restriction on common-mode rejection.

FEEDBACK PHASE SHIFTS IN OPERATIONAL AMPLIFIERS

In an operational amplifier, as in any other feedback amplifier, the phase of the feedback must be controlled to assure that the design is stable with frequency and that the desired gain-frequency response is obtained. Fig. 50 shows the gain and phase characteristics as functions of frequency for a typical 60-dB operational amplifier in which no phase-compensation techniques

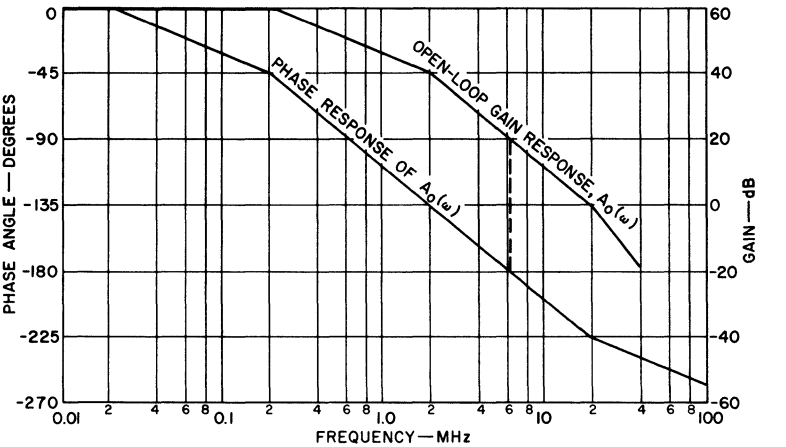


Fig. 50 — Gain and phase response of an open-loop operational amplifier operated without phase compensation.

are employed. Over the frequency range shown, the change in the phase of the feedback is substantially greater than 180 degrees. This phase response indicates that a low-frequency negative feedback can become positive and cause the amplifier to be unstable at high frequencies unless phase-compensation methods are employed to stabilize and control the response of the amplifier.

Effect of Excessive Phase Shift on Frequency Stability

The transfer equation for the inverting configuration, Eq. (92), can be rearranged so that it reflects the same classical feedback form as that for the noninverting configuration, given by Eq. (130). These equations, which are based on the assumptions

that Z_i approaches infinity and Z_{oi} is zero, are repeated below for convenience:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z_f}{Z_f + R_r}\right)\left[\frac{-A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}}}\right]$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}}}$$

If the phase angle of the feedback term, $A_o(\omega)/(1 + Z_f/Z_r)$, reaches 180 degrees (not asymptotically) while the magnitude of the term is still unity or greater, oscillations will occur. [If the term is greater than unity, the oscillations will build until limiting occurs. This limiting decreases $A_o(\omega)$, and thus the entire feedback term, until unity magnitude at a phase angle of 180 degrees is achieved.] These unstable conditions can be predicted readily. Fig. 51 shows a superposition of the gain-frequency curve shown

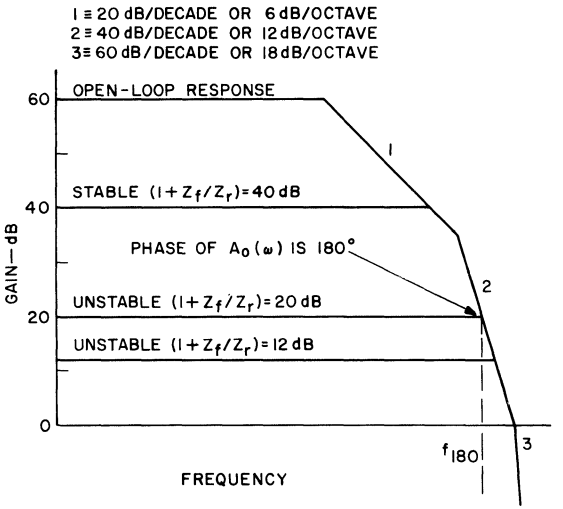


Fig. 51 — Open-loop response and stability characteristics of an operational amplifier.

in Fig. 50 on several sample plots of the ideal feedback characteristic, as given by $1 + Z_f/Z_r$ when Z_f and Z_r are purely resistive. Because the crucial frequency for a purely resistive feedback network is that at which $A_o(\omega)$ has a phase angle of 180 degrees, the magnitude of $A_o(\omega)/(1 + Z_f/Z_r)$ at this frequency (f_{180}) determines whether the configuration is stable. If $A_o(f_{180})/(1 + Z_f/Z_r)$ is equal to or greater than unity, the configuration is *unstable*. On the other hand, if this term is less than unity, then the configuration is *stable*. This stability-determination technique is applied to the various values of $1 + Z_f/Z_r$ shown in Fig. 51; in each case, the gain of the amplifier at the frequency for which the phase angle is 180 degrees is assumed to be 10 [i.e., $A_o(f_{180})=10$].

When $1 + Z_f/Z_r = 100\underline{/0°}$, the stability ratio is calculated as follows:

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10\underline{/180°}}{100\underline{/0°}} = 0.10\underline{/180°}$$

Because the value of 0.10 obtained for the stability ratio is less than unity, the configuration is stable.

When $1 + Z_f/Z_r = 10.0\underline{/0°}$, the stability ratio becomes

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10\underline{/180°}}{10\underline{/0°}} = 1.0\underline{/180°}$$

For this case, the stability ratio is unity, and the configuration therefore, is unstable. As a check, an examination of the transfer expressions for both the inverting and the noninverting configuration [Eqs. (92) and (130)] reveals that for the condition specified, each contains the following term:

$$\frac{1}{1 + 1\underline{/180°}}$$

which is not finite and, therefore, indicates an oscillating condition.

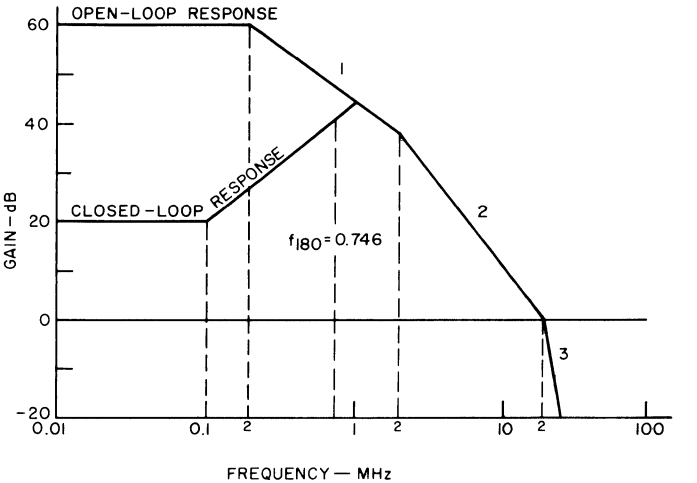
When $1 + Z_f/Z_r = 4.0\underline{/0°}$,

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10\underline{/180°}}{4\underline{/0°}} = 2.50\underline{/180°}$$

The value obtained is greater than unity, and the circuit, therefore, is unstable.

When Z_f and Z_r are not restricted to purely resistive values, a more general situation exists because the phase of $A_o(\omega)/(1 + Z_f/Z_r)$ is no longer dependent solely upon $A_o(\omega)$. Two examples which essentially cover the field are given below.

Example No. 1 — A characteristic of differentiating or peaking circuits is that the feedback term $1 + Z_f/Z_r$ is in the form $K(1 + jf/f_1)$, where K and f_1 are constants. Fig. 52 shows a curve



$$A_o(\omega) = \frac{1000}{\left(1 + j\,\frac{f}{0.2\ \text{MHz}}\right)\left(1 + j\,\frac{f}{2\ \text{MHz}}\right)\left(1 + j\,\frac{f}{20\ \text{MHz}}\right)}$$

$$1 + \frac{Z_f}{Z_r} = \left(1 + j\,\frac{f}{0.1\ \text{MHz}}\right)$$

Fig. 52 — Basic peaking response characteristics of an operational amplifier.

of this term as a function of frequency, for K = 10 and f_1 = 0.1 MHz, superimposed upon an operational-amplifier open-loop transfer curve. The equation for the open-loop characteristic can be derived from Fig. 51, as follows:

$$A_o(\omega) = \frac{1000}{\left(1 + j\,\frac{f}{0.2\ \text{MHz}}\right)\left(1 + j\,\frac{f}{2\ \text{MHz}}\right)\left(1 + j\,\frac{f}{20\text{MHz}}\right)} \qquad (159)$$

The frequency at which the stability ratio $A_o(\omega)/1 + Z_f/Z_r$ has a phase angle of 180 degrees and the magnitude of the ratio for this frequency can then be calculated. The computation reveals that the phase angle is 180 degrees at a frequency (f_{180}) of 0.746 MHz, and the magnitude of the ratio is 3.22 at that frequency. The stability ratio is greater than one; therefore, the configuration is *unstable*. The point of instability (f_{180}) is marked in Fig. 52.

The stability of an operational amplifier may be determined more easily from an *estimate* of the phase angle of the ratio $A_o(\omega)/(1 + Z_f/Z_r)$ at the frequency of intersection (where the magnitude of the ratio is unity). If the estimate shows that the phase angle is less than 180 degrees, the configuration is stable. On the other hand, if the estimate indicates a phase angle in excess of 180 degrees, the circuit is unstable. When the estimate shows that the phase angle is near 180 degrees, an accurate calculation is required to determine whether the operational amplifier is stable. This border-line type of configuration, however, is generally undesirable from the standpoint of frequency response, as discussed later.

In the application of the estimation technique to the problem presented in Fig. 52, the following conditions should be noted: The feedback characteristic $1 + Z_f/Z_r$ increases at the rate of 6 dB per octave (20 dB per decade) for a full decade before it intersects the open-loop response, $A_o(\omega)$. The intersection occurs near the second corner of the open-loop response, which decreases at the rate of 6 dB per octave for almost a full decade. The classical phase relationships associated with these observations are used to obtain the following phase estimates:

$$\text{Phase of } (1 + Z_f/Z_r) = +90°$$
$$-135° < \text{Phase of } A_o(\omega) < -90°$$

Therefore, the following phase estimate is obtained at the frequency of the intersection:

$$-225° < \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) < -180°$$

Thus, the configuration is *unstable*.

Example No. 2—An inherent characteristic of integrating or band-limiting configurations is that the feedback term $1 + Z_f/Z_r$ has the following form:

$$\frac{K}{1 + jf/f_1}$$

An example of this type of feedback characteristic is shown in Fig. 53 for $K = 10$ and $f_1 = 4$ MHz. The application of the phase-estimation technique to this problem results in the following estimates:

$$-45° > \text{Phase of } 1 + Z_f/Z_r > -90°$$
$$-135° > \text{Phase of } A_o(\omega) > -225°$$

At the frequency of intersection, therefore, the phase estimate is given by

$$-45° > \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) > -180°$$

Thus, the configuration is *stable*.

If the three basic types of feedback characteristics shown in Figs. 51, 52, and 53 are compared, it becomes evident that the

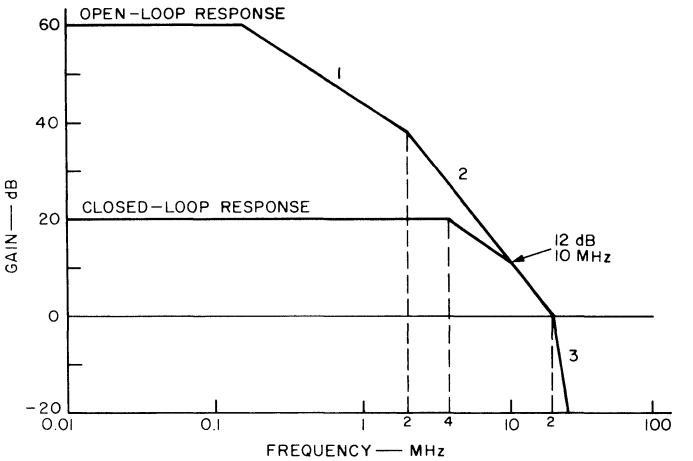


Fig. 53 — Basic integrating response characteristics of an operational amplifier.

differentiating or frequency-peaking configuration is the most unstable and that the integrating or low-pass configuration is the most stable. In fact, the techniques used to devise this latter configuration may be considered a form of phase compensation for certain situations, as discussed later.

Effects of Excessive Phase-Shift on Frequency Response

The criterion evolved for frequency stability neither precludes uncontrolled frequency peaking nor provides for a 3-dB closed-loop bandwidth prediction. The conditions that are required to

develop a stable, controlled-response feedback amplifier are evolved in this section.

Criteria for a Peaked Response — Frequently peaking results when the magnitude of the true closed-loop gain, as given by Eq. (92) for the inverting configuration and by Eq. (130) for the noninverting configuration, is greater than the magnitude of the ideal closed-loop gain (Z_f/Z_r for an inverting circuit and $1 + Z_f/Z_r$ for a noninverting circuit). The criteria for frequency peaking can be expressed for both configurations by the following expression:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| > \left| 1 + \frac{Z_f}{Z_r} \right| \tag{160}$$

Inequality (160) may be used to develop a set of criteria that predict frequency peaking (or preclude the occurrence of frequency peaking).

The following substitution is first made in inequality (160):

$$\frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \equiv B\underline{/\theta} \tag{161}$$

If both sides of inequality (160) are then divided by the left-hand term, the following result is obtained:

$$1 > \left| 1 + \frac{1}{B}\underline{/-\theta} \right| \tag{162}$$

Inequality (162) may be rewritten in either of the following forms:

$$1 > \left[\left(1 + \frac{1}{B} \cos\theta \right)^2 + \left(-\frac{1}{B} \sin\theta \right)^2 \right]^{\frac{1}{2}} \tag{163}$$

or

$$1 > \left[1 + \frac{2}{B} \cos\theta + \left(\frac{1}{B} \right)^2 \right]^{\frac{1}{2}} \tag{164}$$

The real and imaginary parts of inequality (163) must also be less than unity, so that

$$1 > \left| 1 + \frac{1}{B} \cos \theta \right| \tag{165}$$

and

$$1 > \frac{1}{B} \left| - \sin \theta \right| \tag{166}$$

It is apparent from inequality (165) that

$$B > \frac{1}{2} \tag{167}$$

and from inequality (164) that

$$\cos \theta < - \frac{1}{2} B \tag{168}$$

The substitution indicated by the identity (161) is again made, and both sides of inequality (160) are then divided by the right-hand term to obtain the following expressions:

$$\left| \frac{B/\underline{\theta}}{1 + B/\underline{\theta}} \right| > 1 \tag{169}$$

or

$$| B/\underline{\theta} | > | 1 + B/\underline{\theta} | \tag{170}$$

Inequality (170) can be solved to reveal that

$$| B/\underline{\theta} | < 2.62$$

For peaking to occur, therefore, the following relationships must be in effect:

$$0.5 < | B/\underline{\theta} | < 2.62$$

$$\cos \theta < - \frac{1}{2} B$$

3-dB Bandwidth Prediction — The 3-dB bandwidth of an operational amplifier is defined by the following condition:

$$\left| \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}}} \right| = \frac{\left| 1 + \dfrac{Z_f}{Z_r} \right|}{\sqrt{2}} \tag{171}$$

The terms of Eq. (171) are rearranged and the definition for B $\underline{/\theta}$ given by the identity (161) is used to obtain the following relationships:

$$\left| 1 + \frac{1}{B}\underline{/-\theta} \right| = \sqrt{2}$$

$$\left(1 + \frac{1}{B}\cos\theta\right)^2 + \left(-\frac{1}{B}\sin\theta\right)^2 = 2$$

$$1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B}\right)^2 = 2 \tag{172}$$

Eq. (172) yields the following criteria for the 3-dB point:

$$1 \geq B > \frac{1}{1+\sqrt{2}} = 0.414 \tag{173}$$

$$\cos\theta = \frac{B^2 - 1}{2B} \tag{174}$$

Inequality (173) predicts the possibility of a 3-dB bandwidth greater than that indicated by the intersection of $A_o(\omega)$ and $1 + Z_f/Z_r$ (B = 1 point). However, it should be realized that this "bandwidth extension" is actually caused by a slight peaking effect. Special care should be exercised in any attempt to use this effect to advantage.

Inequality (174) stipulates that the phase angle must be 90 degrees to obtain the 3-dB bandwidth where B = 1. This stipulation essentially coincides with a "rule of thumb" that has become a standard in the industry. This rule may be stated as follows: *For an unconditionally stable configuration, the ideal feedback characteristic, $1 + Z_f/Z_r$, must intersect the open-loop response, $A_o(\omega)$, at a slope less than 12 dB per octave.* An examination of this "rule of thumb" in terms of the phase relationship indicates that the phase angle asymptotically approaches 180 degrees when the change in amplifier response with frequency occurs at a rate of 12 dB per octave. Therefore, the amplifier is on the threshold of instability. Frequency dependence of less that 12 dB per octave indicates that the amplifier is stable; a dependence of greater than 12 dB per octave indicates that the amplifier is unstable.

PHASE-COMPENSATION TECHNIQUES FOR OPERATIONAL AMPLIFIERS

The design problems (i.e., ac instability and uncontrolled frequency response) created by excessive phase shift in the feedback can be solved by use of compensating techniques that alter the feedback response so that excessive phase shifts no longer occur. The frequency response can be controlled by limiting the slope of the intersection of the ideal feedback characteristic, $1 + Z_f/Z_r$, with the open-loop gain response, $A_o(\omega)$, to a safe value. Theoretically, this slope can have a maximum value of 12 dB per octave under certain conditions. In general, however, the maximum slope allowed for practical lumped-parameter systems is 6 dB per octave. In an operational amplifier, effective phase compensation can be accomplished only by a modification in one or more of the following parameters:

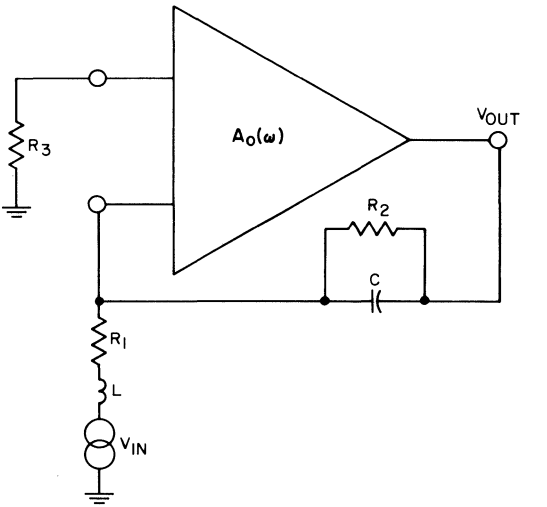
1. the ideal closed-loop gain (feedback characteristic), $1 + Z_f/Z_r$;
2. the open-loop input impedance, Z_i;
3. the open-loop gain, $A_o(\omega)$.

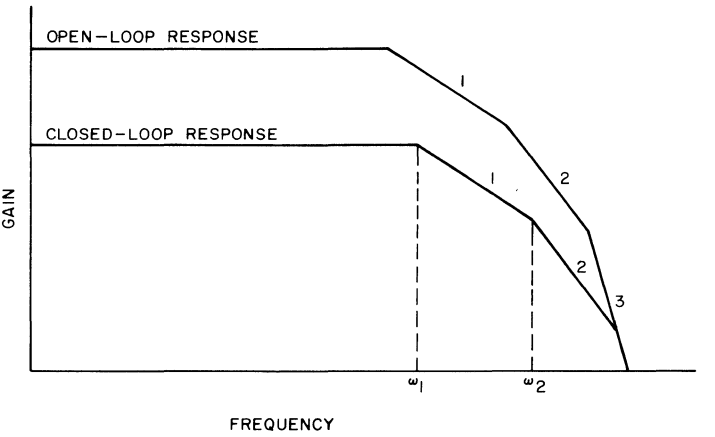
Closed-Loop Compensation Method

Phase compensation can be accomplished by modification of the closed-loop gain characteristic (i.e., the $1 + Z_f/Z_r$ term) for only those applications in which the intersection of the $1 + Z_f/Z_r$ characteristic with the open-loop response occurs in a region where the open-loop response rolls off at a slope of 12 dB per octave or 18 dB per octave. When the intersection occurs in a 12-dB-per-octave region of the $A_o(\omega)$ response, compensation techniques are used that cause the slope of the $1 + Z_f/Z_r$ response to roll off at 6 dB per octave near the intersection. As a result of these techniques, the slope of the intersection becomes 6 dB per octave. (An example of this method of phase compensation was discussed earlier, in the section on "Criteria for a Peaked Response", and the response curves for this example were shown in Fig. 53.)

For applications in which the use of an inductor is permissible, phase compensation in the 18-dB-per-octave region of the open-loop response can be accomplished by techniques that cause the $1 + Z_f/Z_r$ response to roll off at 12 dB per octave near the intersection. An example of this method of phase compensation, together with the appropriate response curves, is shown in Fig. 54.

In this example, the Z_f term is altered by a shunt capacitor and the Z_r term is altered by a series inductor so that the $1 + Z_f/Z_r$ response has the required 12-dB-per-octave roll-off. The location





$$R_3 = R_1 /\!/ R_2$$

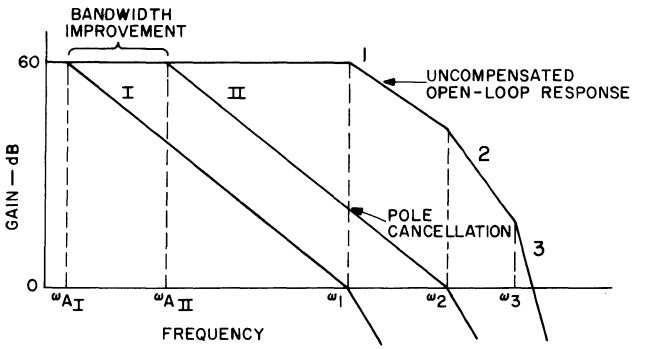
$$\frac{V_{OUT}}{V_{IN}} = \frac{-\dfrac{R_2}{1 + j\omega CR_2}}{R_1 + j\omega L} = -\frac{R_2}{R_1}\left[\frac{1}{\left(1 + j\,\dfrac{\omega L}{R_1}\right)(1 + j\omega CR_2)}\right]$$

Fig. 54 — Phase compensation of operational amplifier permissible in the "three-slope region."

of these frequency-dependent components in the feedback configuration is unique for this type of phase compensation.

Open-Loop Compensation Methods

Phase-compensation techniques that alter either the open-loop input impedance or the open-loop gain permit the introduction of a zero, in addition to the low-frequency pole, into the open-loop gain characteristic. This zero can be designed to cancel one of the poles in the open-loop gain characteristic and thus to increase substantially the bandwidth of the operational amplifier. Alternatively, the operational-amplifier bandwidth can be increased by the introduction of a pole at a frequency low enough so that all the other corner points will occur at frequencies below that at which the open-loop response, $A_o(\omega)$, intersects the closed-loop response, $1 + Z_f/Z_r$. The two methods are compared in Fig. 55. It is apparent that the pole-cancellation method of phase compensation is superior to the method in which the other corner



I—Compensated open-loop response using simple depression of higher corner frequencies.

II—Compensated open-loop response using pole cancellation.

Fig. 55 — Phase compensation of operational amplifier by use of pole cancellation.

frequencies are depressed. In the phase-compensation techniques discussed below, therefore, the pole-cancellation method is employed.

Modification of the Open-Loop Input Impedance — The following analysis shows the limitations imposed on alterations in

the open-loop input impedance of an operational amplifier in order to provide phase compensation. In this phase-compensation technique, an appropriate network is connected between the input terminals so that it appears in parallel with the intrinsic input impedance, Z_i. Eqs. (92) and (130), which define the closed-loop inverting and noninverting responses, respectively, are used as the basis for establishing the conditions and the mechanisms involved in this kind of compensation.

If Z_i is used to represent the modified open-loop input impedance and the open-loop output impedance, Z_{oi}, is assumed to be zero, the following equations for the closed-loop response are obtained:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\, Z_i'\, Z_f}{Z_f\,(Z_i' + R_r) + Z_r\,(Z_f + Z_i' + R_r) + A_o(\omega)\, Z_i'\, Z_r} \tag{175}$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\, Z_i'\,(Z_r + Z_f)}{(Z_i' + R_r)\,(Z_r + Z_f) + Z_r\, Z_f + A_o(\omega)\, Z_i'\, Z_r} \tag{176}$$

A judicious rearrangement of terms in Eqs. (175) and (176) reveals the effect that the altered open-loop input impedance has on the open-loop response. With this rearrangement, the equation for the inverting configuration becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_f}{Z_f + \dfrac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \tag{177}$$

The equation for the noninverting configuration is then written as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] (Z_r + Z_f)}{Z_f + \dfrac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \tag{178}$$

For each configuration, the modified open-loop response is defined as follows:

$$A_o'(\omega) \equiv \frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'} \tag{179}$$

It is apparent from Eq. (179) that the alteration of the open-loop input impedance has no effect on the open-loop response unless

Z_i' is, at most, of the same order of magnitude as the $R_r + Z_r$ term. If Z_i' is made much less than $R_r + Z_r$, Eq. (179) becomes

$$A_o'(\omega) \doteq \frac{A_o(\omega)\, Z_i'}{R_r + Z_r} \tag{180}$$

As predicted by Eqs. (179) and (180), three limitations are imposed in the use of the input-impedance modification technique to provide phase compensation: (1) the feedback impedance term Z_r is restricted in value and configuration by the phase-compensation requirements; (2) the effective open-loop input impedance must be smaller in magnitude than and different in configuration from the intrinsic input impedance, Z_i (thus the closed-loop input impedance, Z_{IN}, also is smaller and different); and (3) the dc open-loop gain is less for some input-impedance configurations.

Two examples of the input-impedance phase-compensation technique are shown in Figs. 56 and 57. In the method shown in Fig. 56, the required modification of the open-loop response is achieved by proper choice of the frequency characteristics for the network connected in shunt with the input terminals of the operational amplifier. Fig. 57 shows that the required modification of the response can be achieved by the appropriate choice of the frequency characteristics of R_r and Z_r. Both techniques employ pole-zero cancellation to extend the 6 dB-per-octave roll-off region depicted. The technique illustrated in Fig. 56 causes an early roll-off, while the one shown in Fig. 57 results in a reduction in the dc open-loop gain. Eqs. (179) and (180) indicate that phase-compensation can also be effected by an increase in the magnitude of $R_r + Z_r$, provided that the frequency characteristics of this parameter are controlled. However, this technique relies on the accuracy of the value of Z_i and therefore is unsatisfactory. (The intrinsic input impedance of an operational amplifier may vary significantly from unit to unit.)

Modification of Open-Loop Gain Characteristics — Phase compensation that is effected by internal modification of the open-loop gain response is the most widely accepted technique for integrated-circuit operational amplifiers. This method offers two distinct advantages over other types of phase compensation. First, the internal-modification technique affords complete isolation of the phase-compensation networks from the feedback parameters. This isolation is not possible with the compensation methods discussed previously. Second, the point at which the phase com-

pensation is applied can be selected so that the open-loop response is altered in such a way that one of the existing 3-dB corner frequencies becomes the early roll-off corner in the compensated response. The advantage stems from the fact that no new corner frequencies are introduced, and an improved compensated response is thus obtained.

Internal phase compensation can be accomplished by either of two basic methods. In one method, referred to as the straight roll-off, an appropriate RC network is connected across a suitable internal resistor of the operational amplifier. With this method, the early roll-off starts at the corner frequency produced by the phase-compensating capacitor and the internal resistor. The other method is the Miller-effect roll-off. In this method, the phase-compensating network still appears electrically to be placed across an appropriate internal resistance of the amplifier, but is actually connected between the input and the output of an inverting-gain

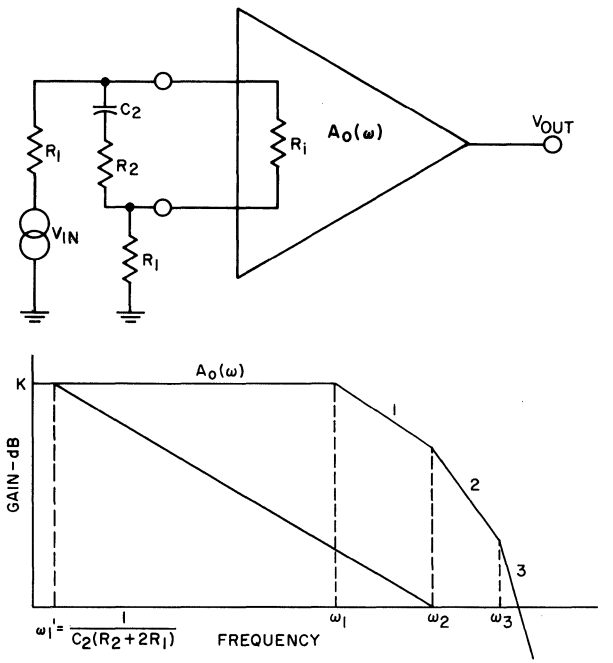


Fig. 56 — Phase compensation of operational amplifier in which open-loop response is modified by connection of a compensating network that provides the required frequency characteristics in shunt with input terminals. (Mathematical relationships for this phase compensation technique are shown on page 93.)

stage in the operational amplifier. The impedance of the compensating network then appears to be divided by the gain of that stage.

The Miller-effect roll-off technique requires a much smaller phase-compensating capacitor than that which must be used with the straight roll-off method. Moreover, the reduction in swing capability which is inherent in the straight roll-off is delayed significantly when the Miller-effect roll-off is used. Fig. 58 illustrates the solution to the problem of phase compensation of an operational amplifier in which a straight roll-off is used to cause the second 3-dB corner frequency to occur at unity gain. Fig. 59 illustrates the use of a Miller-effect roll-off to solve the same problem. For the same early corner frequency, the compensating

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Mathematical relationships for phase-compensation technique shown in Fig. 56

$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain
R_i = low-frequency intrinsic input impedance

$$A_o(\omega) = \frac{\pm A_o(\omega) R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \frac{1}{j\omega C_2}\right) 2R_1 + R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}$$

$$A_o'(\omega) = \left[\frac{\pm A_o(\omega) R_i}{2R_1 + R_i}\right]\left[\frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 \left(R_2 + \frac{2R_i R_1}{2R_1 + R_i}\right)}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \pm A_o(\omega) \frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 (R_2 + 2R_1)}$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and if $$R_2 C_2 = \frac{1}{\omega_1}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) = \frac{K}{[1 + j\omega C_2 (R_2 + 2R_1)]\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + \frac{\omega}{\omega_3}\right)}$$

capacitance required in the Miller-effect method is less than that required in the straight roll-off method by a factor of $1 + g_{m_{II}}R_{c_2}$ ($g_{m_{II}}$ and R_{c_2} are defined in Fig. 59).

DESIGN CRITERIA FOR OPERATIONAL AMPLIFIERS

It is apparent from the previous discussions that a completely universal design of an operational amplifier would have to satisfy an impossible set of criteria. As a result, the design of operational amplifiers is a somewhat specialized process in that a particular amplifier is usually designed for specific applications. For example, certain operational amplifiers are designed to provide high-frequency gain at the expense of other performance characteristics, while other operational amplifiers provide very high gain or high input impedance in low-frequency applications. Integrated-circuit operational amplifiers, which are fabricated by the diffusion

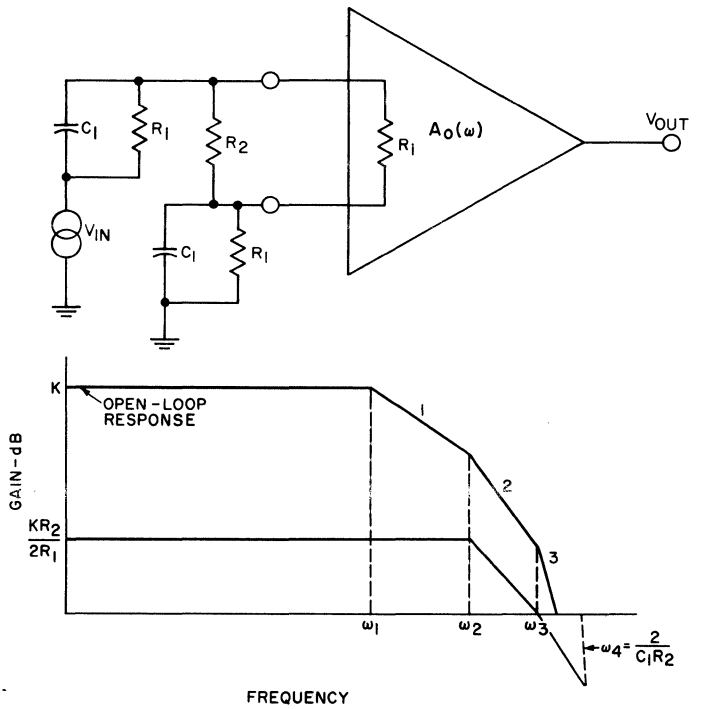

Fig. 57 — Phase compensation of operational amplifier in which open-loop response is modified by alteration of the $R_r + Z_r$ term to provide the required frequency characteristics. (Mathematical relationships for this phase-compensation technique are shown on page 95.)

process, can be made suitable for comparator applications or can be processed to provide high gain at low dissipation levels. For these reasons, any discussion of the criteria for operational amplifiers must be of a general nature unless a specific application is being considered.

Input and Output DC Levels

In general, an operational amplifier should be designed so that the dc bias levels at the input and the output are equal. This

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Mathematical relationships for phase-compensation technique shown in Fig. 57

$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = \frac{\pm A_o(\omega)\, R_2\, R_i}{(R_2 + R_i)\left(\dfrac{2\,R_1}{1 + j\omega_1 R_1 C_1}\right) + R_2 R_i}$$

$$= \left[\frac{\pm A_o(\omega)\, R_2\, R_i}{2R_1(R_2+R_i) + R_2 R_i}\right]\left[\frac{1 + j\omega\, R_1 C_1}{1 + j\omega \dfrac{R_1 R_2\, R_i C_1}{2R_1(R_2+R_i) + R_2\, R_i}}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \left(\frac{\pm A_o(\omega)\, R_2}{2R_1 + R_2}\right)\left(\frac{1 + j\omega\, R_1\, C_1}{1 + j\omega \dfrac{C_1 R_1\, R_2}{2R_1 + R_2}}\right)$$

If $R_2 << R_1$, the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \left(\frac{\pm A_o(\omega)\, R_2}{2R_1}\right)\left(\frac{1 + j\omega R_1\, C_1}{1 + j\omega C_1 \dfrac{R_2}{2}}\right)$$

For
$$A_o(\omega) = \frac{K}{\left(1 + j\dfrac{\omega}{\omega_1}\right)\left(1 + j\dfrac{\omega}{\omega_2}\right)\left(1 + j\dfrac{\omega}{\omega_3}\right)}$$

and
$$R_1\, C_1 \equiv \frac{1}{\omega_1},$$

the compensated open-loop gain $A_o'(\omega)$ is given by

$$A_o'(\omega) = \frac{\pm K}{2\dfrac{R_1}{R_2}\left(1 + j\omega C_1 \dfrac{R_2}{2}\right)\left(1 + \dfrac{\omega}{\omega_2}\right)\left(1 + \dfrac{\omega}{\omega_3}\right)}$$

condition is desirable to assure that the resistive feedback network can be connected between the input and the output without upsetting either the differential or the common-mode dc bias. Moreover, for applications in which two (positive and negative) power supplies are used, the operational amplifier should be designed so that it is possible to establish a set of standard supply values for which the equal input and output bias levels are at zero potential with respect to circuit ground. This latter condition is particularly important in direct-coupled cascade and comparator applications.

Output-Power Capability

As with any amplifier circuit, the output-power requirements for an operational amplifier depend almost entirely on the application. A few general conclusions can be drawn concerning the

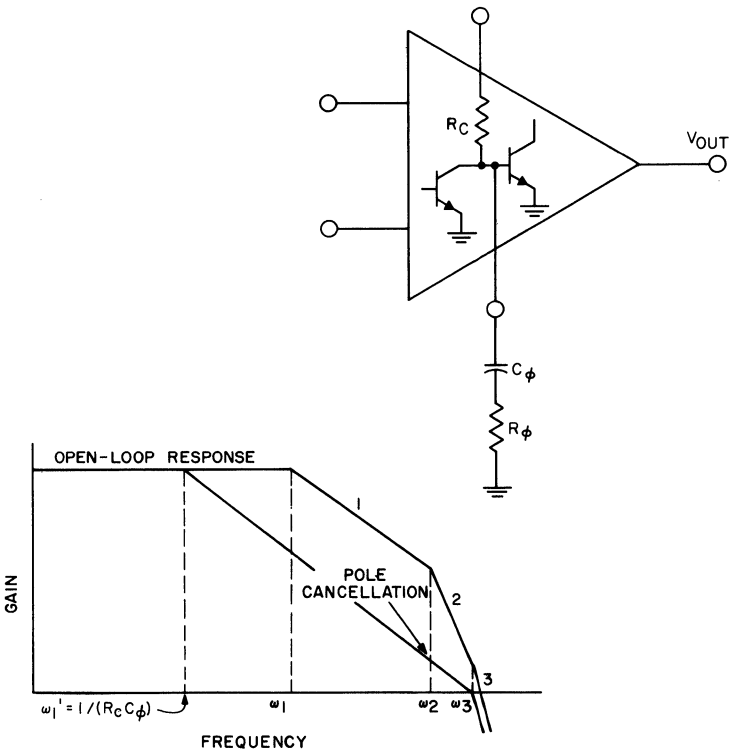

Fig. 58 — Phase compensation of operational amplifier by use of straight-rolloff method to modify open-loop response. (Mathematical relationships for this phase-compensation technique are shown on page 97.)

design of the output stage. First, this stage should provide a voltage swing essentially equal to the sum of the power-supply voltages. It should have sufficient gain so that it is the first stage to limit when the amplifier is overdriven. Finally, because of the design trade-off that is always required between output-power capability and dissipation, the output stage should be sufficiently versatile so that the output capability and dissipation can be tailored to the power needs of the particular application in which the operational amplifier is used.

Gain and Frequency-Response Characteristics

The numerical values of the open-loop gain and the 3-dB bandwidth of an operational amplifier are of relatively little importance in themselves. The important requirement is that the

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Mathematical relationships for phase-compensation technique shown in Fig. 58

$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the equation above accounts for the modification of the ω_1 3-dB corner.

For $$R_\phi C_\phi = \frac{1}{\omega_2}$$

and $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{(1 + j\omega R_c C_\phi)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner-frequency term, which occurs because of the time constant of R_ϕ and the input capacitance of the succeeding stage, should also be included in the equation above; the effects of this corner frequency, however, is appreciable only at very high frequencies (and usually at a gain less than unity). Because the corner frequency normally occurs well out of the active region, it is omitted in the expression for $A_o'(\omega)$.

open-loop gain must be much greater than the closed-loop gain of the transfer response over the frequency range of interest if an accurate transfer function is to be maintained. (This requirement is explained in detail in the discussions of transfer functions for both the inverting and noninverting configurations.) For example, if a 40-dB amplifier and a 60-dB amplifier are used in a 20-dB gain configuration and the open-loop gain is decreased 50 per cent in each case, the closed-loop gain of the 40-dB amplifier varies only 9 per cent and that of the 60-dB amplifier varies only 1 per cent.

The frequency roll-off characteristics are the prime determinants of the frequency response of an operational amplifier. The greater the rate of roll-off prior to the intersection of the feedback-ratio frequency characteristic with the open-loop response (in the active region), the more difficult phase compensation of the operational amplifier becomes. An 18-dB-per-octave roll-off is generally

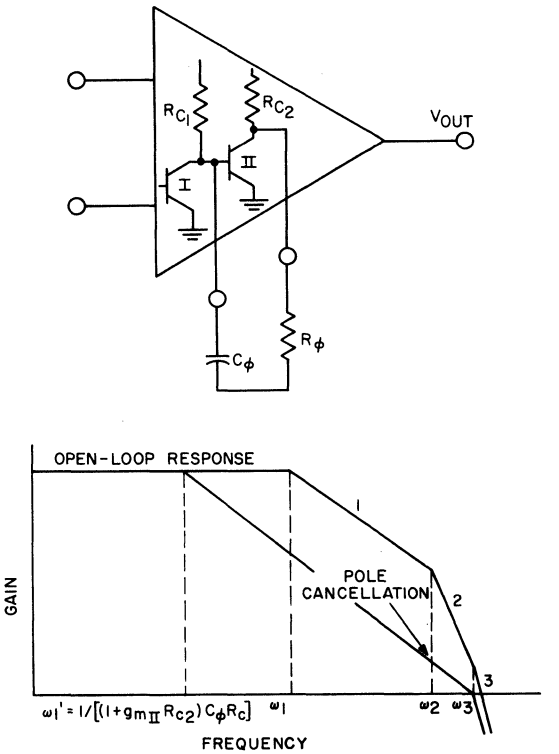

Fig. 59 — Phase compensation of operational amplifier by use of Miller effect to modify open-loop response. (Mathematical relationships for this phase-compensation technique are shown on page 99.)

considered the maximum slope that can occur in the active region before proper phase compensation becomes extremely difficult or impossible to achieve (as indicated in the discussion on the effects of feedback phase shifts). In addition, because operational amplifiers have useful applications down to and including unity gain, the active region of the amplifier may be considered as the entire portion of the frequency characteristic above its 0-dB bandwidth. Therefore, a well-designed amplifier should roll off at no greater than 18 dB per octave until well below unity gain.

Intrinsic Input and Output Impedances

The ideal values for the input and output impedances of an operational amplifier are infinity and zero, respectively (as mentioned in the discussions on input and output impedances for both inverting and noninverting configurations). The degree to

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Mathematical relationships for phase-compensation technique shown in Fig. 59

$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c (1 + g_{mII} R_{c_2}) C^\phi}$$

The $1 + j\,\omega/\omega_1$ term in the expression for $A_o'(\omega)$ accounts for the modification of the ω_1 3-dB corner.

For
$$R_\phi C_\phi = \frac{1}{\omega_2}$$

and
$$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

The expression for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{[1 + j\omega (1 + g_{mII} R_{c_2}) C_\phi R_c]\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner frequency, which results from the time constant of R_ϕ and the feedback capacitance C_{bc}', is neglected in the expression for $A_o'(\omega)$, because this corner frequency occurs well out of the active region.

which a practical amplifier approximates these values depends, for the most part, upon the application. A 5000-ohm open-loop input impedance may be quite sufficient for one application, while a 0.1-megohm intrinsic input impedance may not be sufficient for another. In most applications, however, the restrictions on the intrinsic input impedance are not severe. The closed-loop input impedance, which is equal to the product of the intrinsic input impedance and the gain "throwaway" or loop gain, is a more critical parameter. This parameter effectively increases the input impedance (decreases input capacitance) and is the reason that many operational amplifiers that have an input roll-off in the active region have no input roll-off in this region after negative feedback is applied.

Because the closed-loop output impedance is also affected by the loop gain (the proportionality is inverse), the same conclusions might be drawn about the importance of the intrinsic output impedance. Another factor, however, affects the restrictions placed upon the open-loop output impedance. A limiting situation in an inverting-configuration application affords an alternate path to the signal when the intrinsic output impedance is sufficiently high. The loop gain decreases to zero as the open-loop gain decreases when overdrive occurs. Therefore, the closed-loop output impedance increases until it equals the intrinsic value at full limiting. Thus, the intrinsic output must be much less than the lowest practical value of feedback impedance or an alternate signal path that effectively bypasses the limiting amplifier will exist through the feedback network.

Common-Mode Rejection

Under differential drive conditions, the common-mode rejection has no drastic effects on the performance of the operational amplifier unless the rejection ratio is extremely low (as discussed in respect to the effects of common-mode gain). However, in a common-mode drive situation, such as in a comparator type of application, high common-mode rejection is imperative. For example, if a 60-dB differential amplifier having a 50-dB common-mode rejection is used to compare a 1-volt signal against a 1-volt reference, the output will be 3.2 volts when it should be zero. Such results would be disastrous for almost any application of this type. In general, the common-mode rejection should be a minimum of 20 dB greater than the differential gain.

Input Bias Current

Although an amplifier may have a high intrinsic input ac impedance, it can still require a significant amount of dc input bias current. This condition is undesirable in applications in which the drive source cannot accommodate a significant dc current. Examples of such applications are those that require very high impedance sources or sources of a magnetic nature that can be severely unbalanced by a flow of dc current. Unfortunately, the bipolar transistor remedies for this effect add so much capacitance that the frequency response of the amplifier is impaired. Therefore, either field-effect devices should be used in the differential input stage or a scheme should be available to assure that a very low bias current is obtained when it is absolutely necessary. The latter technique requires that sufficient leads be provided so that two external transistors can be added to form a Darlington or a modified Darlington input configuration.

Offset Voltage and Current

The offset voltage of an operational amplifier is the deviation of the output dc level from the arbitrary input-output level usually taken as ground reference when both inputs are shorted together. The offset current is the deviation when the inputs are driven by two identical dc input bias-current constant-current sources. These two offset parameters are usually referred to the input because their output values are dependent on feedback. Under normal operating conditions, the offset in the amplifier results from a combination of the two factors. For example, if an operational amplifier has a 1-millivolt input offset voltage and a 1-microampere input offset current with the inputs returned to ground through 1000-ohm resistors, the total input offset is either zero or 2 millivolts depending upon the phase relationship between the two offset parameters. The offset of an operational amplifier is a dc error and should be minimized for numerous reasons, including the following: (1) The use of an operational amplifier as a true dc amplifier is limited to signal levels much greater than the offset. (2) Comparator applications require that the output voltage be zero (within limits) when the two input signals are equal and in phase. (3) In a direct-coupled cascade, such as a video amplifier chain, the input offset of the first stage determines the offset characteristics of the entire system. Hence, the gain of the system must be limited to a value that is insufficient to cause limiting at rated output voltage. This value is reduced when the offset is significant.

Power-Supply Stability

The power-supply stability is a measure of the sensitivity that the offset has to power-supply variations. Because the value of the offset at the output is dependent on feedback, this sensitivity is normally referred to the input and expressed in microvolts per volt. In a fixed-installation application that employs heavily regulated power supplies, this parameter is of little importance. In battery-operated applications of the operational amplifier, however, the sensitivity of the offset to power-supply variations is of the utmost importance. In a single-supply system, this sensitivity should be an absolute minimum. In a two-supply system, the difference in the sensitivities to each supply can be minimized because the supplies in many dual systems tend to track. This tracking results in a cancellation, or at least a partial cancellation, of the two sensitivities.

Temperature-Stability Requirements

Temperature stability of an operational amplifier requires stable thermal characteristics for most of the parameters discussed in this section. The stability demands imposed on the temperature characteristics of an operational amplifier are determined to a large extent by the application in which the circuit is used. In certain applications, stable temperature characteristics are of utmost importance; in other applications, the ability of the operational amplifier to perform the required functions is not appreciably affected by variations in circuit parameters with temperature.

In general, the dependence of the open-loop gain on temperature is of less importance than the thermal behavior of the amplifier frequency response. Variations in the intrinsic input and output impedances with temperature are of little consequence provided that the input impedance remains large enough and the output impedance remains small enough to satisfy the requirements of the application. If the value of the input bias current is important for the application in which the operational amplifier is used, stable temperature behavior is just as important. Variations in the offset voltage and current with temperature should always be small because they directly affect the internal biases, and thus the operation, of the operational amplifier.

Characteristics and Applications of RCA Linear Integrated Circuits

The basic differential-amplifier configuration in which a differential pair of transistors is fed from a controlled, constant-current source (transistor current-sink circuit) is the fundamental building block for the broad family of RCA linear integrated circuits. Because of the exceptional versatility of these circuits, a single name cannot, in general, completely categorize any one of them. For convenience, however, each circuit is identified by a generic designation which is indicative of the basic functions for which it may be used. The generic names, together with the RCA type numbers, for the basic family of differential-amplifier (linear) integrated circuits are listed below:

Descriptive Name	*RCA Type No.*
DC Amplifier	CA3000
Audio Amplifier	CA3007
Video Amplifier	CA3001
IF Amplifier	CA3002
RF Amplifier	CA3004, CA3005, and CA3006

In addition, the linear family of integrated circuits includes two operational amplifiers, RCA Types CA3008 and CA3010, which consist basically of a two-stage direct-coupled cascade of differential-amplifier circuits, together with an appropriate output stage. Cascaded direct-coupled differential amplifiers are also used as the basis for the design of four FM-if integrated circuits used to provide amplification, limiting, and FM demodulation in the sound channel of intercarrier television receivers and in FM

broadcast or communications receivers. These circuits include the CA3011 and CA3012 wide-band amplifiers and the CA3013 and CA3014 amplifier-discriminators.

PRACTICAL CONSIDERATIONS AND DESIGN FEATURES

The basic differential amplifier, shown in Fig. 9, must be augmented by emitter followers to obtain the practical configurations used for the RCA linear integrated circuits. Emitter followers are required to compensate for the effects of monolithic capacitances. Output emitter followers are used to obviate the effects of the capacitance inherent in monolithic circuits between coupling capacitors and the substrate. A potential loss of video bandwidth because of the shunt capacitance between a capacitor plate and ground can be effectively negated by use of an emitter-follower voltage source to drive the capacitor plate. Input emitter followers provide the high input impedance required for successful iterative operation (e.g., in if amplifiers) because of the small values (approximately 15 picofarads) of coupling capacitors. (The use of an emitter follower at one input requires the use of a second emitter follower at the other input to preserve the differential-amplifier balance.)

Practical configurations of the differential-amplifier integrated circuits also include a suitable output stage which provides the required gain and output-impedance characteristics. In addition, it is often necessary to use external components to modify the responses and transfer functions of the basic circuits, as required for a particular application.

RCA linear integrated circuits are characterized by excellent gain characteristics, high common-mode rejection, temperature stability, and exceptional versatility. Moreover, the inherently matched pairs of components in the differential-amplifier configuration make possible excellent output-to-input isolation, eliminate the need for neutralization, and simplify feedback arrangements. The differential-amplifier configuration also permits easy access to external circuit points and thus facilitates circuit "outboarding."

The transistor constant-current-sink circuit, shown in Fig. 46, contains built-in temperature-compensating networks that provide gain and dc operating-point stability for the linear circuits. The temperature stability provided by the constant-current-sink circuit permits satisfactory operation of the linear integrated circuits over the temperature range of −55°C to 125°C.

The amount of dc source current (I_o) supplied to the emitters of the differential pair of transistors can be readily controlled by variation of the magnitude of the base-to-emitter voltage of the current-sink transistor. Because the current I_o has a significant effect on the transfer and transconductance characteristics and on the slopes of these characteristics, the use of the basic differential-amplifier configuration provides the linear integrated circuits with an inherent gain-control capability.

In general, there are four possible operating modes for RCA linear integrated circuits. For a given circuit, each mode is characterized by a specific dc operating point and corresponding voltage gain, both of which have a particular temperature dependence. The dc operating point and voltage gain of the circuit are dependent upon the value of resistance in the emitter circuit of the current-sink transistor. As shown in Fig. 46, either of two values may be selected. For either value of emitter resistance, it is possible to operate the circuit with or without the temperature-compensating diodes shown in Fig. 46. The temperature dependence of the dc operating point and the voltage gain is significantly different, depending upon whether the diodes are in or out of the circuit.

The availability of four possible operating modes, together with the easy access that the differential-amplifier configuration provides to external circuit points, makes possible the exceptional versatility of RCA linear integrated circuits. These versatile circuits are supplied in convenient, reliable packages, shown in Fig. 60, which further increase their utility. With the exception of the

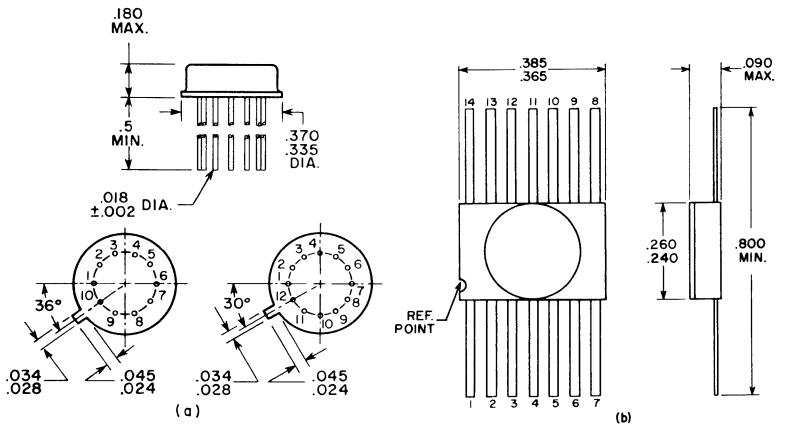


Fig. 60 — Package configurations for the linear integrated circuits: (a) 10- or 12-terminal, low-silhouette, hermetically sealed TO-5 style package; (b) 14-terminal ceramic-and-metal flat-pack.

CA3008 operational amplifier, the linear integrated circuits are supplied in 10- or 12-terminal, hermetically sealed, low-silhouette TO-5 style packages. The CA3008 is supplied in a 14-terminal ceramic-and-metal flat package.

INTEGRATED-CIRCUIT DC AMPLIFIER

Fig. 61 shows the schematic diagram of the CA3000 dc amplifier. This stabilized and compensated differential amplifier pro-

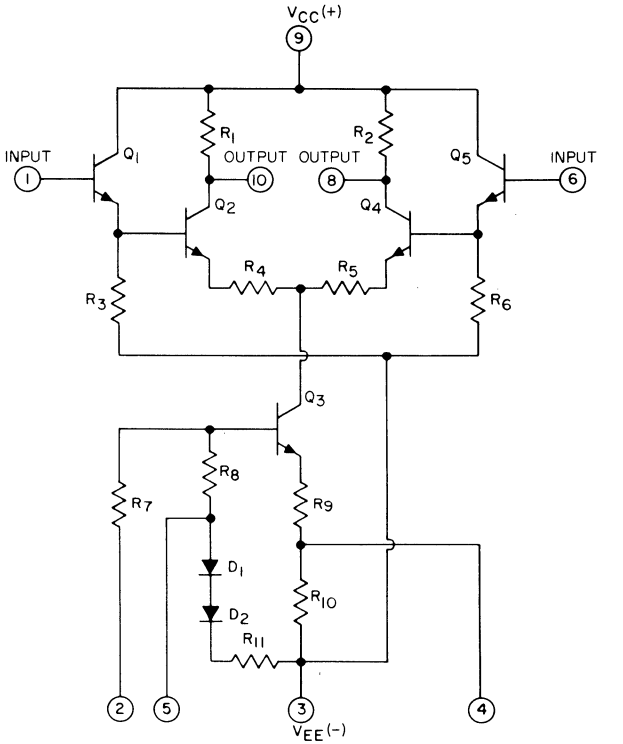


Fig. 61 — Schematic diagram of the CA3000 integrated-circuit dc amplifier.

vides push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to 1 MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils.

The circuit, which is supplied in a 10-terminal TO-5 style package, is basically a single-stage differential amplifier (Q_2 and

Q_4) with input emitter-followers (Q_1 and Q_5) and a constant-current sink (Q_3) in the emitter-coupled leg. Push-pull input and output capabilities are inherent in the differential configuration.

The use of degenerative resistors R_4 and R_5 in the emitter-coupled pair increases the linearity of the circuit. The low-frequency output impedance between each output (terminals 8 and 10) and ground is essentially the value of the collector resistors R_1 and R_2 in the differential stage.

Operating Requirements and Characteristics

The CA3000 is designed for operation from a wide range of supply voltages. Operation from either one or two power supplies is feasible, as illustrated by the typical biasing techniques shown in Fig. 62. However, operation from two supplies is recommended because fewer external bias networks are required and, therefore, less power is consumed.

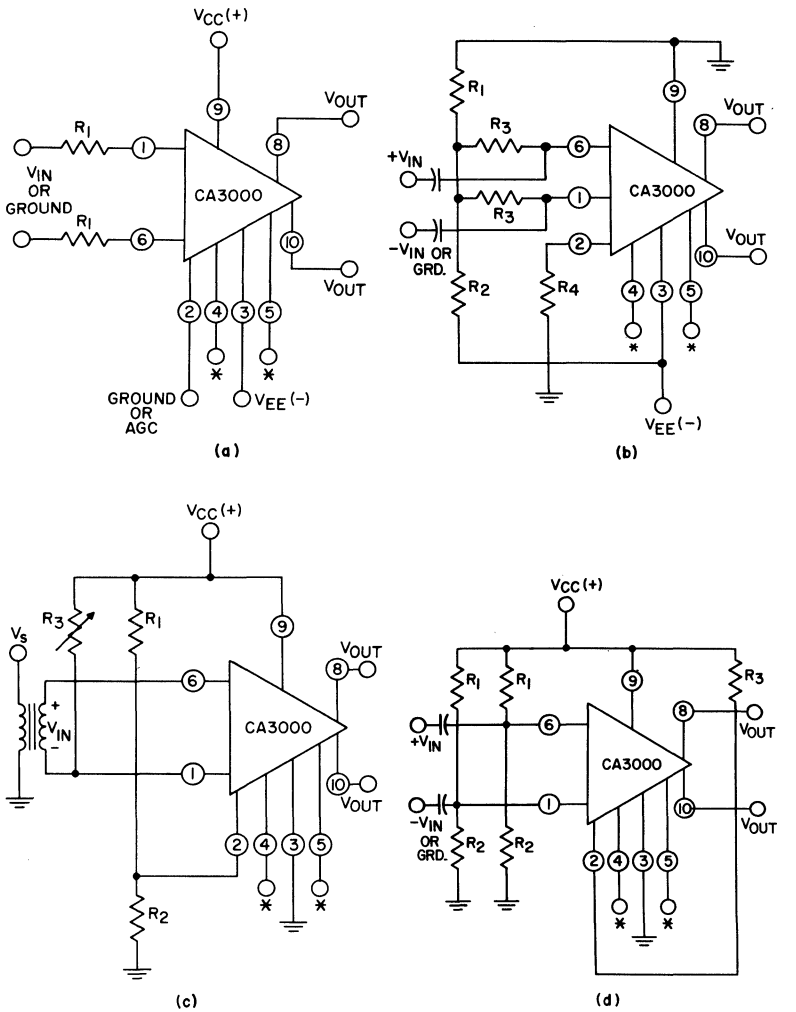
The maximum voltage that can be applied across the circuit (positive supply voltage V_{CC} plus negative supply voltage V_{EE}) is 16 volts. The maximum voltage capability (V_{CE}) of the differential pair is limited to 8 volts. Extra care must be used to ensure that these values are not exceeded when the circuit is used to drive inductive loads.

The operating-current conditions of the differential pair are determined by the base-bias circuit and emitter resistance of the emitter-coupled constant-current sink (Q_3), as well as by the voltage between terminals 2 and 3. Each possible current condition is manifested by (1) a distinct set of dc operating characteristics with differing temperature characteristics, (2) a particular value of gain having its own temperature dependence, and (3) a particular dynamic output-voltage capability. For each value of voltage between terminals 2 and 3 (V_{EE} when terminal 2 is grounded), there are four possible operating modes, as described in Table III.

Table III—*Operating Modes for CA3000 DC Amplifier*

Mode	Shorted Terminals	Condition of Diodes	Q_3 Emitter Resistor
A	none	in	$R_9 + R_{10}$
B	5-3	out	$R_9 + R_{10}$
C	4-3	in	R_9
D	5-4-3	out	R_9

The operating characteristics for these modes of operation are summarized in Table IV for various two-supply configurations with terminal 2 grounded and with V_{EE} values of −3 and −6 volts dc.



* Connection of terminals 4 and 5 depends upon mode of operation.

Fig. 62 — Typical biasing arrangements for the CA3000 for operation from (a) two separate voltage supplies, or (b), (c), and (d) a single voltage supply.

Table IV shows that the positive supply voltage can be adjusted for each mode of operation and for each value of negative supply so that the nominal dc output voltage is zero. (Although the V_{CC} value required for mode C for a V_{EE} of −6 volts dc is in excess of the maximum rating, operation within ratings can be achieved with slightly negative values of output voltage.) The use

Table IV—*Design Characteristics of CA3000 Operating Modes*

DC Supply Volts Positive V_{CC}	DC Supply Volts Negative $-V_{EE}$	Operating Mode	Single-ended Mid-Band Voltage Gain — dB G_{V_S}	DC Output Volts (Term. 8 or 10 to ground) $V_{o_{dc}}$	Positive Voltage Swing $V_{o_{max}}$*	Negative Voltage Swing $V_{o_{min}}$*	Total Power Dissipation — mW
6	−6	A	31.2	+2.3	+3.7	−3.8	40
6	−6	B	27.3	+4.3	+1.7	−5.7	36
6	−6	C	34.6	−1.5■	+7.5	0	61
6	−6	D	32.4	+1.0	+5.0	−2.4	47
3.7	−6	A	31.2	0	+3.7	−1.4	33
1.7	−6	B	27.3	0	+1.7	−1.4	25
10.6▲	−6	C	34.6	0	+10.6	−1.5	83
5.0	−6	D	32.4	0	+5.0	−1.5	43
3	−3	A	27.5	+1.2	+1.8	−2.6	8.8
3	−3	B	16.6	+2.6	+0.4	−4.1	7.4
3	−3	C	32.6	−1.5■	+4.5	0	14
3	−3	D	24.4	+1.9	+1.1	−3.3	8.5
1.8	−3	A	27.5	0	+1.8	−1.5	7.2
0.4	−3	B	16.6	0	+0.4	−1.5	8.4
5.3	−3	C	32.6	0	+5.3	−1.5	19
1.1	−3	D	24.4	0	+1.1	−2.6	6.2

* $V_{o_{max}}$ and $V_{o_{min}}$ are the ac swing extremities above and below $V_{o_{dc}}$.
▲ Over rating. ■ Saturated.

of these adjusted values of positive supply provides two advantages: (1) direct interstage coupling can be effected in a single-ended configuration, and (2) negative feedback can be introduced from a single output back to the appropriate input. For low-level applications in mode D with a negative supply voltage V_{EE} of −3 volts dc and a positive supply voltage V_{CC} of 1.1 volts dc, the CA3000 has a gain of 24.4 dB, a dissipation of 6.2 milliwatts, an output capability of 2.2 volts peak-to-peak, and a dc output-voltage reference level of zero.

The information in Table IV can be modified for single-supply designs by simple addition and/or subtraction of dc values. For example, the correct information for a single supply of 12 volts dc for operating mode A can be obtained from the conditions shown in the table for mode A for V_{CC} = 6 Vdc and V_{EE} = −6 Vdc by the addition of 6 volts to the values shown for V_{CC}, V_{EE}, Vo_{dc}, Vo_{max}, and Vo_{min}. (It should be noted that the required

voltage levels at the input terminals 1 and 6 and at terminal 2 are also 6 volts higher.)

As mentioned previously, the four operating modes exhibit different temperature characteristics. Fig. 63 shows theoretical curves of dc output voltage as a function of temperature for each

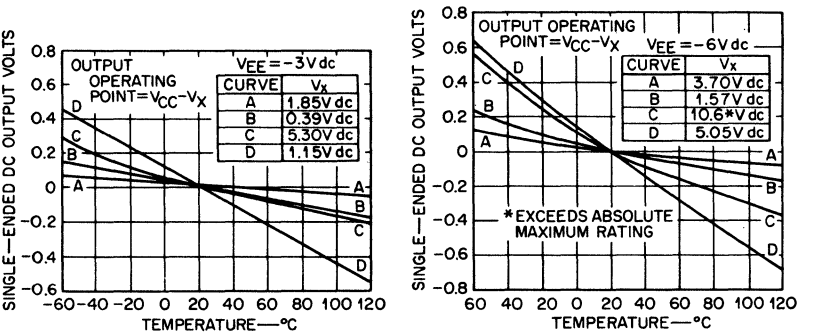


Fig. 63 — Theoretical curves of dc output voltage as a function of temperature for negative-supply voltages of −3 and −6 volts dc (calculated for $\beta = 35$ at 20°C).

operating mode for negative supply voltages V_{EE} of −3 and −6 volts dc. The experimental curves shown in Fig. 64 are in excellent agreement with the theoretical curves except in the case of mode

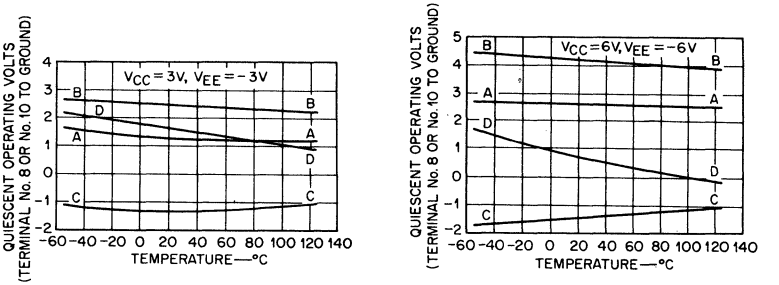
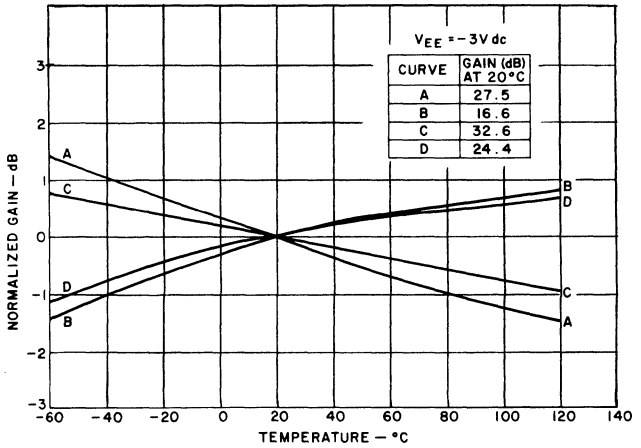


Fig. 64 — Measured curves of dc output voltage as a function of temperature for negative-supply voltages of −3 and −6 volts dc.

C. In this mode, the differential-pair transistors Q_2 and Q_4 were driven into saturation as a result of the use of symmetrical supplies ($V_{CC} = V_{EE}$) for the experimental data. The discrepancy could be corrected by use of somewhat higher values of positive supply voltage.

Fig. 65 shows theoretical curves of gain as a function of temperature for the four operating modes with V_{EE} values of −3 and −6 volts dc. With the diodes in (modes A and C), the gain decreases for both values of V_{EE}. With the diodes out (modes B and D), on the other hand, the gain increases with temperature for a negative supply of −3 volts dc, but decreases with temperature



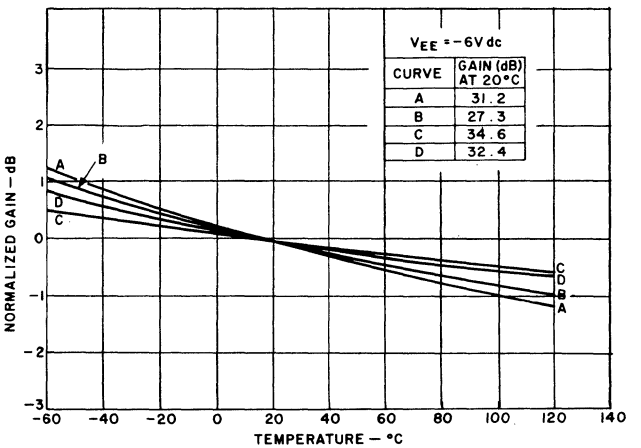


Fig. 65 — Theoretical curves of gain as a function of temperature for negative-supply voltages of −3 and −6 volts dc (calculated for $\beta = 35$ at 20°C).

for a negative supply of −6 volts dc. With the diodes out, there is a value of negative supply (approximately −4.5 volts dc) for which the gain is independent of temperature. Fig. 66 shows measured values of single-ended and push-pull gain for mode A with

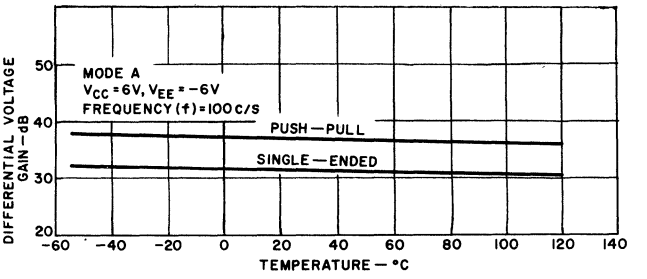


Fig. 66 — Measured values of single-ended and push-pull gain for mode A operation with symmetrical power supplies of ±6 volts dc.

symmetrical power supplies of ±6 volts dc. (This configuration is used in the remaining discussion because it provides the maximum sinusoidal output capability, as shown in Table IV, and because of the convenience of ±6-volt dc supplies.)

The typical single-ended voltage-gain/frequency-response curve of the CA3000 for dc supplies of ±6 volts in operating mode A is shown in Fig. 67, together with the test circuit used for voltage-gain measurements. The responses of the CA3000 are virtually independent of source impedance up to 10,000 ohms because of the emitter-follower inputs. The curves in Fig. 68 show that gain and bandwidth are virtually independent of temperature for operation in mode A with ±6-volt dc supplies.

Fig. 69 shows agc characteristics for the CA3000 for an input frequency of 1 kHz, together with the agc voltage-gain test circuit. When the agc voltage at terminal 2 is varied from 0 to −6 volts, the amplifier gain can be varied over a range of 90 dB.

Fig. 70 shows the test circuit used to measure common-mode rejection, together with curves of common-mode rejection as a function of frequency and temperature. Typical rejection is 97 dB at a frequency of 1 kHz. Fig. 71 shows the test circuit used to measure the dc unbalance of the amplifier (referred to the input), together with a curve of the input offset voltage as a function of temperature. Typical input offset voltage (with an assumed push-pull differential gain of 37 dB) is 1.5 millivolts. Fig. 72 shows

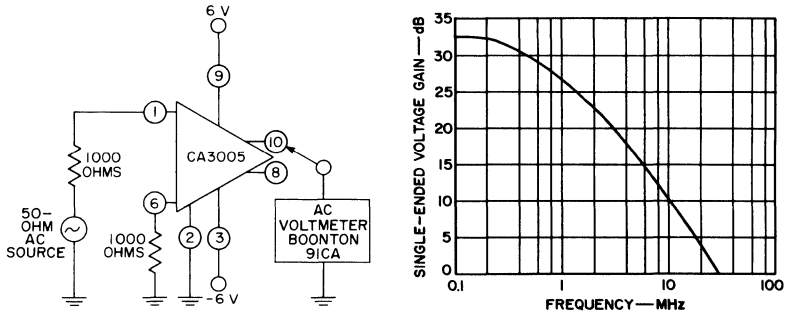


Fig. 67 — Single-ended voltage gain of CA3000 as a function of frequency in test circuit shown.

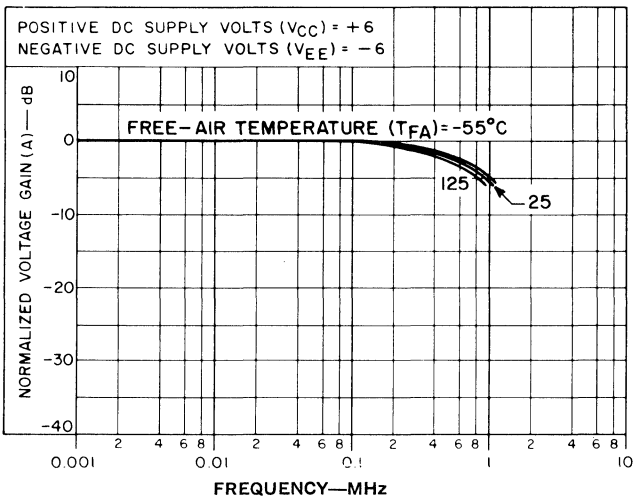
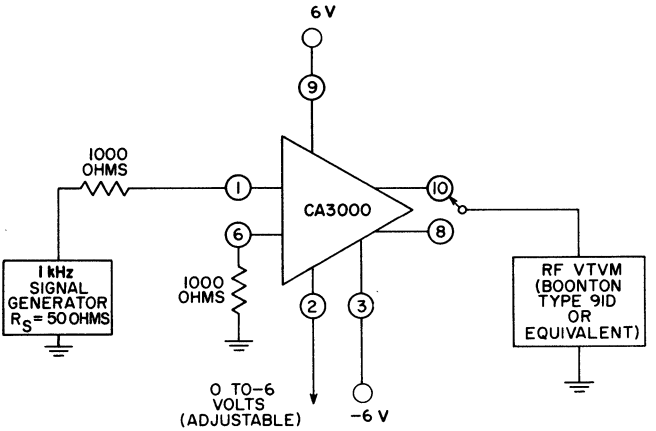


Fig. 68 — Normalized gain-frequency curves for CA3000 at three different temperatures.

curves of input bias current, input impedance, and dynamic output voltages as functions of temperature.

Applications of the DC Amplifier

The full gain-control capability inherent in the CA3000 makes possible the use of this circuit as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer, or a product detector. When suitable external components are added, it can also be used as an



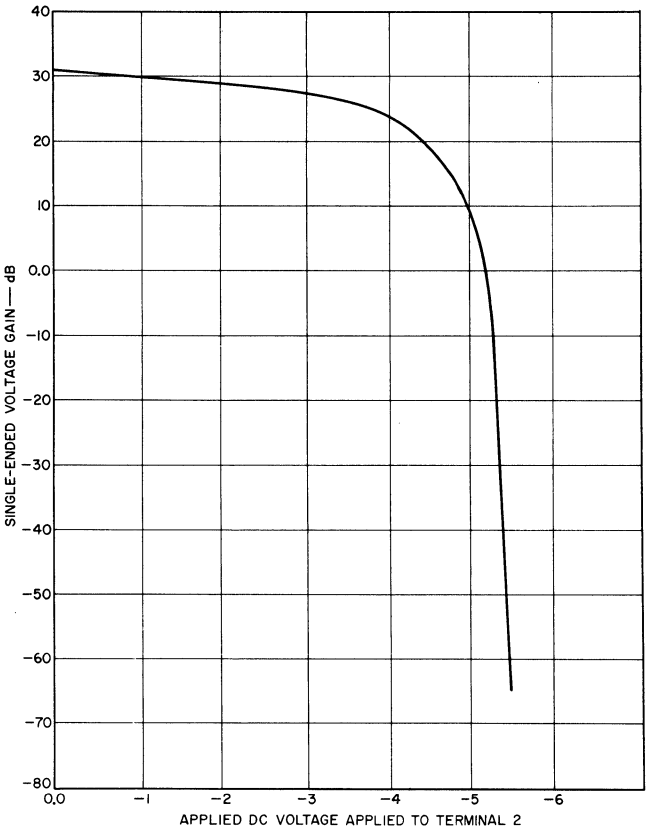
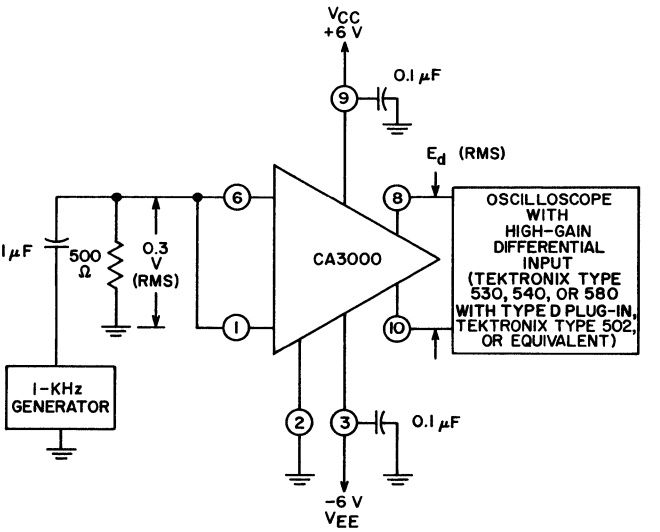


Fig. 69 — AGC characteristics of CA3000 in test circuit shown at frequency of 1 kHz.



COMMON-MODE REJECTION RATIO (CMR) = 20 log $\frac{(A^*)(2)(0.3)}{E_d\,(RMS)}$

*A = SINGLE-ENDED VOLTAGE GAIN AS MEASURED IN CIRCUIT SHOWN IN FIG. 68

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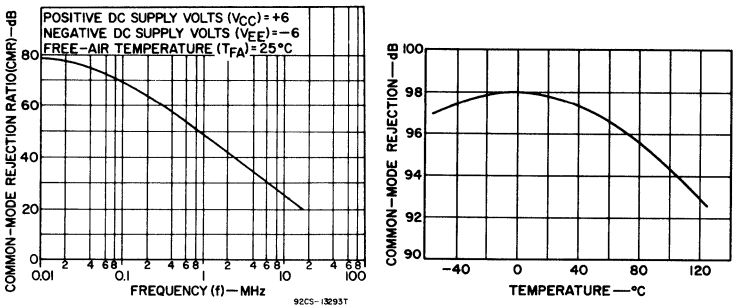


Fig. 70 — Common-mode rejection of CA3000 as a function of frequency and of temperature in test circuit shown.

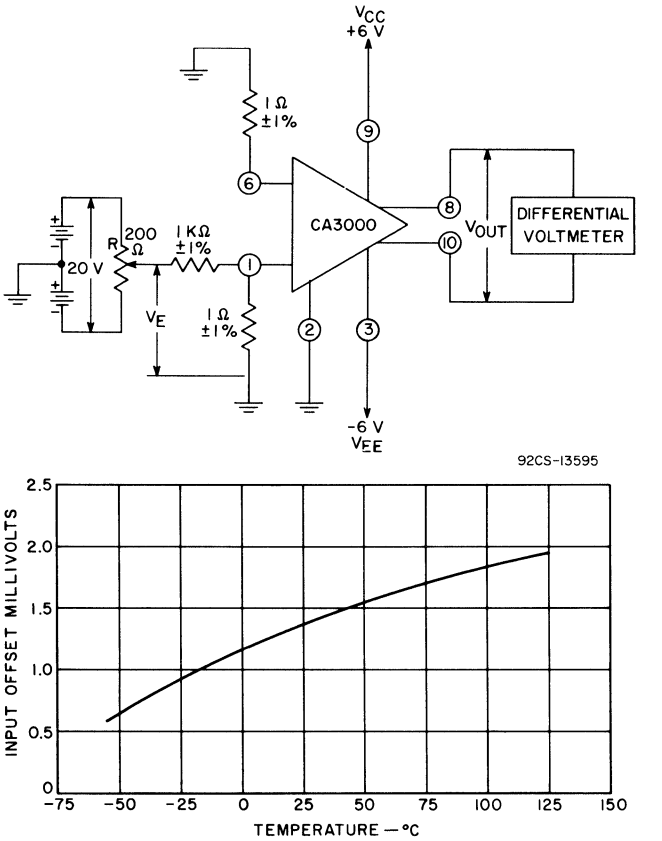


Fig. 71 — Input offset voltage of CA3000 as a function of temperature in test circuit shown.

oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter, and can handle input signals up to about 80 millivolts rms before significant cross-modulation or intermodulation products are generated. Some of the applications of the CA3000 are discussed below.

Crystal Oscillator — The CA3000 can be used as a crystal oscillator at frequencies up to 1 MHz by connection of a crystal between terminals 8 and 1 and use of two external resistors, as shown in Fig. 73(a). The output is taken from the collector that is not connected to the crystal (in this case, terminal 10). If a variable-feedback ratio network is used, as shown in Fig. 73(b), the feedback may be adjusted to provide a sinusoidal oscillation. Output waveforms for both circuits are also shown. The frequency

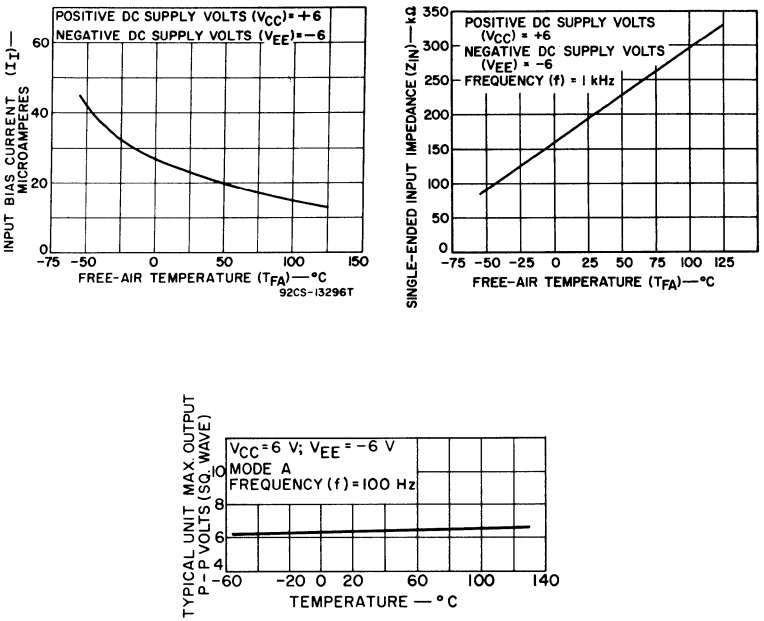


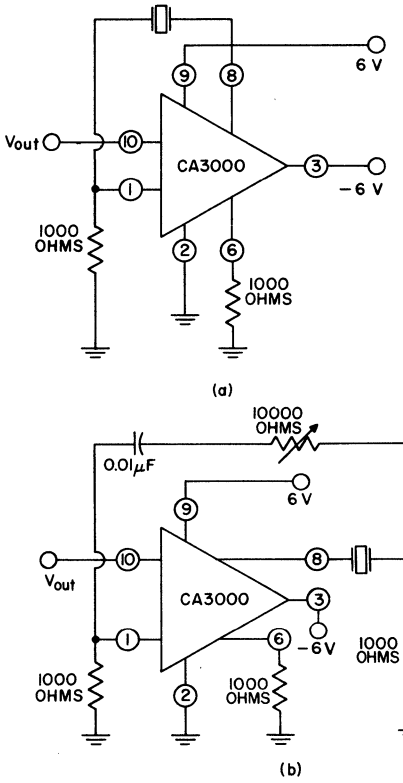
Fig. 72 — Input bias current, input impedance, and dynamic output voltage of CA3000 as functions of temperature.

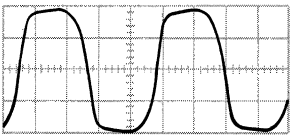
in each circuit is 455 kHz, as determined by the crystal. The range of these crystal oscillators can be extended to frequencies of 10 MHz or more by use of collector tuning.

Modulated Oscillator — If a low-frequency signal is connected to terminal 2, as shown in Fig. 74, the CA3000 can function as an oscillator and produce an amplitude-modulating signal. The waveform in Fig. 74 shows the modulated signal output produced by the modulated oscillator circuit when a 1-kHz signal is introduced at terminal 2 and a high-pass filter is used at the output.

Low-Frequency Mixer — In a configuration similar to that used in modulated-oscillator applications, the CA3000 amplifier may be used as a mixer by connection of a carrier signal at the base input of either differential-pair transistor (terminal 1 or 6) and connection of a modulating signal to terminal 2 or 5.

Cascaded RC-Coupled Feedback Amplifier — The two-stage feedback cascade amplifier shown in Fig. 75 produces a typical open-loop mid-band gain of 63 dB. This circuit uses a 100-picofarad capacitor C_1 to shunt the differential outputs of the first stage. This capacitor staggers the high-frequency roll-offs of the amplifier and thus improves stability.





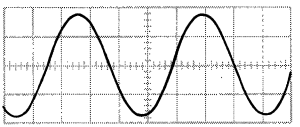
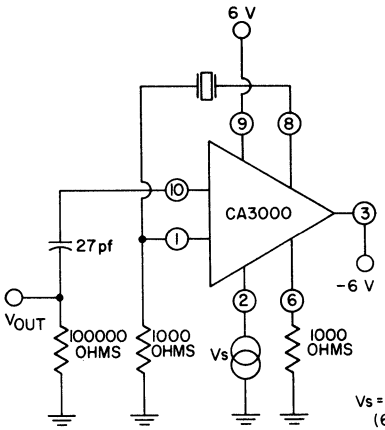


Fig. 73 — Schematic diagrams and output waveforms of (a) crystal oscillator and (b) crystal oscillator with variable feedback.



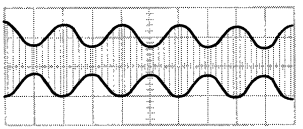


Fig. 74 — Schematic diagram and output waveform of CA3000 modulated oscillator.

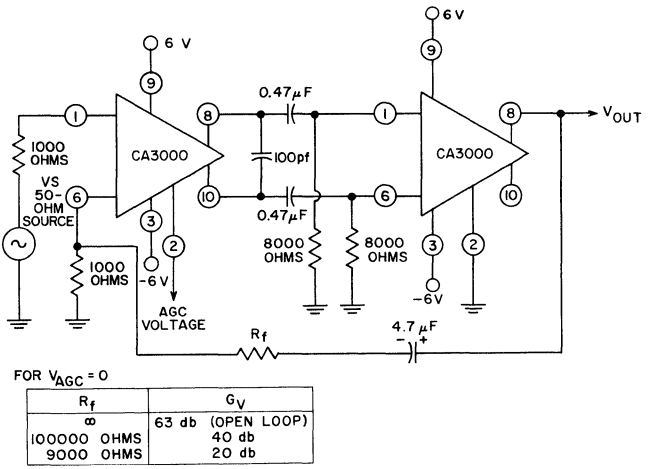


Fig. 75 — Cascaded RC-coupled feedback amplifier using two CA3000 circuits.

The gain-frequency characteristic of the feedback amplifier is shown in Fig. 76(a) for a feedback resistance R_f approaching infinity. The low-end roll-off of the amplifier is determined by the interstage coupling. Because agc may be applied to the first stage, the amplifier of Fig. 75 may be used in high-gain video-agc applications under open-loop conditions. If feedback is used to control the gain, agc may still be applied successfully.

Fig. 76(b) shows the agc characteristics for the two-stage amplifier under open-loop and two closed-loop conditions at a frequency of 1 kHz. As shown in Fig. 76(a), the open-loop bandpass is 18 Hz to 135 kHz; under closed-loop conditions, the bandpass is 1.3 Hz to 2 MHz for 40-dB gain and 0.13 Hz to 6.6 MHz for 20-dB gain. The negative feedback thus improves low-frequency performance sufficiently so that the use of the small coupling capacitors C_2 and C_3 involves little sacrifice in low-frequency response. If three or more CA3000 amplifiers are cascaded, the low-frequency roll-offs must be staggered as well as those at the high end to prevent oscillation. A three-stage cascade has a midband gain of approximately 94 dB.

Narrow-Band Tuned Amplifier — Because of its high input and output impedances, the CA3000 is suitable for use in parallel tuned-input and tuned-output applications. There is comparative freedom in selection of circuit Q because the differential amplifier exhibits inherently low feedback qualities provided the following

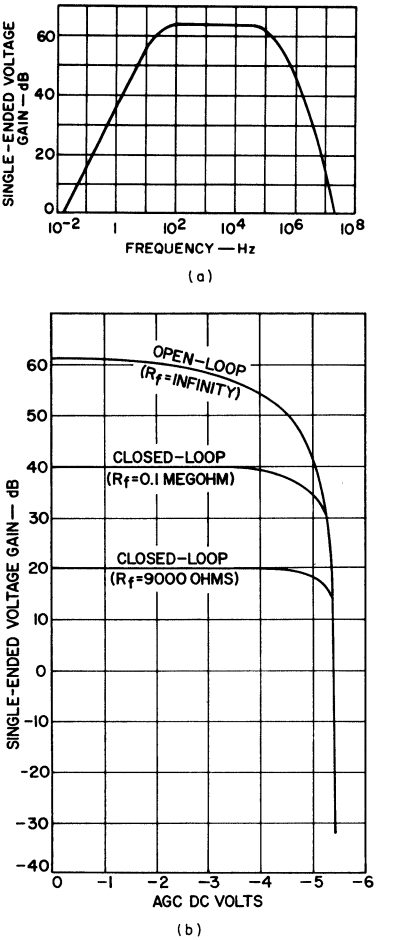


Fig. 76 — Gain-frequency (a) and agc (b) characteristics of feedback amplifier shown in Fig. 75.

conditions are met: (1) the collector of the driven transistor is returned to ac ground and the output is taken from the non-driven side, and (2) the input is adequately shielded from the output by a ground plane.

The CA3000 has an output capacitance of approximately 9 picofarads at a frequency of 10 MHz. This capacitance will

resonate a 28-microhenry coil at this frequency and give a minimum Q of 4.55 when the collector load resistor is the only significant load. With this low Q, stagger tuning may be unnecessary for many broad-band applications.

Fig. 77 shows the CA3000 in a narrow-band, tuned-input, tuned-output configuration for operation at 10 MHz with an input Q of 26 and an output Q of 25; the response curve of the amplifier is also shown. The 10-MHz voltage gain is 29.6 dB, and the total effective circuit Q is 37. There is very little feedback skew in the response curve. The CA3000 can be used in tuned-amplifier applications at frequencies up to the 30-MHz range.

Schmitt Trigger — The CA3000 can be operated as an accurate, predictable Schmitt trigger provided saturation of either side of the differential amplifier is prevented (hysteresis is less predictable if saturation occurs). Non-saturating operation is accomplished by operation in mode B (terminals 3 and 5 shorted together) in the configuration shown in Fig. 78. Large values are required for external resistors R_1 and R_2 because they receive the total collector current from terminal 10. Because of the high impedances, resistor R_2 is actually a parallel combination of the input impedance (approximately 0.1 megohm) of the CA3000 and the 0.25-megohm external resistor. The Schmitt-trigger design equations (for $\alpha = 1$) are summarized below. In these equations, Q_2 and Q_4 are the differential-pair transistors, Q_1 and Q_5 are the emitter-follower transistors, and Q_3 is the constant-current sink.

State I: Q_2 off, Q_4 conducting (not saturated)

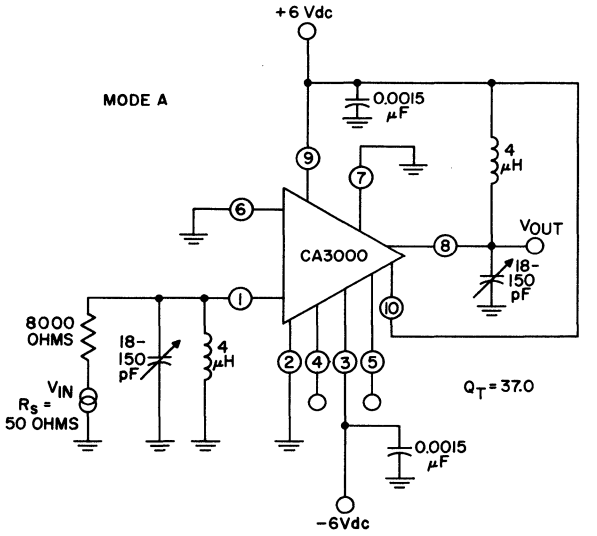
$$V_{6I} = \frac{V_{CC}\,(R_2) - V_{EE}\,(R_1 + 8000)}{R_1 + R_2 + 8000}$$

where 8000 ohms is the output impedance of Q_4 (obtained from the published data). For $R_1 = 27000$ ohms and $V_{CC} = V_{EE} = 6$ Vdc,

$$V_{6I} = \frac{6V\,(R_2) - 6V\,(35000)}{R_2 + 35000} \qquad (A)$$

$$R_2 = (R_1 + 8000)\,\frac{V_{EE} + V_{6I}}{V_{CC} - V_{6I}}$$

$$R_2 = (35000)\,\frac{6V + V_{6I}}{6V - V_{6I}} \qquad (B)$$



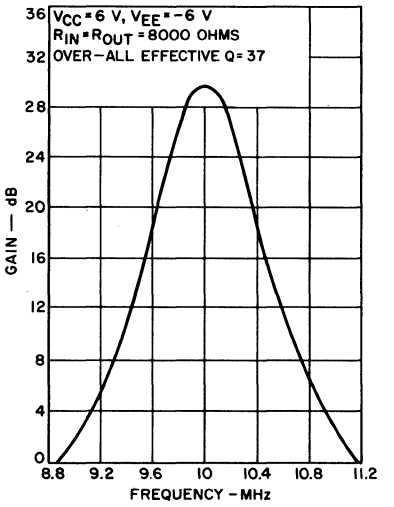


Fig. 77 — Schematic diagram and response curve for 10-MHz tuned-input, tuned-output, narrow-band amplifier using CA3000.

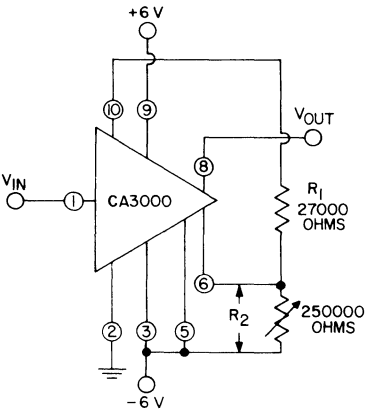


Fig. 78 — Schematic diagram for Schmitt trigger using CA3000.

$$V_{8I} = V_{CC} - I_E\,(8000)$$

where I_E = collector current of transistor Q_3 ($I_E \approx 0.48$ milliampere in operating mode B with $V_{EE} = -6$ volts dc.)

$V_{8I} = 2.14$ V (C)

$V_{FI} \equiv$ Firing voltage for transition from state I to state II

$V_{FI} = V_{6I} - 0.053 - 100\ I_E$ at 25°C

$V_{FI} = V_{6I} - 0.101$ V at 25°C (D)

State II: Q_2 conducting (not saturated), Q_4 off

$V_{8II} = V_{CC}$

$V_{8II} = 6$ V (A)

$$V_{6II} = \frac{(V_{CC} - I_E\,8000)\,R_2 - V_{EE}\,(R_1 + 8000)}{R_1 + R_2 + 8000}$$

$$V_{6II} = \frac{2.14\text{ V}\,(R_2) - 6\text{ V}\,(35000)}{R_2 + 35000} \quad \text{(B)}$$

$V_{FII} \equiv$ Firing voltage for transition from state II back to state I

$V_{FII} = V_{6II} + 0.053 + 100\ I_E$ at 25°C

$V_{FII} = V_{6II} + 0.101$ V at 25°C (C)

Hysteresis Voltage

$$V_{HYS} = V_{F_I} - V_{F_{II}}$$

$$= \frac{3.86\ V\ (R_2)}{R_2 + 35000} = 0.202\ V \text{ at } 25°C$$

From the calculations for state I, it is evident that either V_{6_I} or R_2 must be a known design value. Because R_2 is a composite value, V_{6_I} is the more reasonable choice. The ability of these equations to predict the Schmitt-trigger performance is evidenced by the comparison of calculated and experimental data in Table V.

Table V—*Comparison of Calculated and Experimental Data for Schmitt Trigger*

Condition	Parameter	Calculated	Experimental
1) $V_{6_I} = -2$ V	V_{F_I}	−2.1 V	−2.2 V
	$V_{F_{II}}$	−3.19 V	−3.2 V
	V_{HYS}	+1.09 V	+1.0 V
2) $V_{6_I} = -1$ V	V_{F_I}	−1.10 V	−1.0 V
	$V_{F_{II}}$	−2.51 V	−2.45 V
	V_{HYS}	+1.41 V	+1.4 V
3) $V_{6_I} = 0$	V_{F_I}	−0.101 V	0
	$V_{F_{II}}$	−1.83 V	−1.8 V
	V_{HYS}	+1.73 V	+1.8 V
4) $V_{6_I} = +1$ V	V_{F_I}	+0.9 V	+1.0 V
	$V_{F_{II}}$	−1.15 V	−1.0 V
	V_{HYS}	+2.1 V	+2.0 V
5) $V_{6_I} = +2$ V	V_{F_I}	+1.9 V	+2.0 V
	$V_{F_{II}}$	−0.472 V	−0.5 V
	V_{HYS}	+2.43 V	+2.4 V

INTEGRATED-CIRCUIT AUDIO AMPLIFIER

The CA3007 audio driver, shown in Fig. 79, is a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit, which is intended for use as a direct-coupled driver in a class B audio amplifier, exhibits both gain and operating-point stability over the temperature range from −55 to 125°C. The CA3007 is an excellent controlled-gain audio driver for systems requiring audio squelching. The audio-driver circuit is available in a 12-terminal TO-5 style low-silhouette package.

The input stage of the CA3007 consists of a differential pair of transistors (Q_1 and Q_2) operating as a phase splitter with gain.

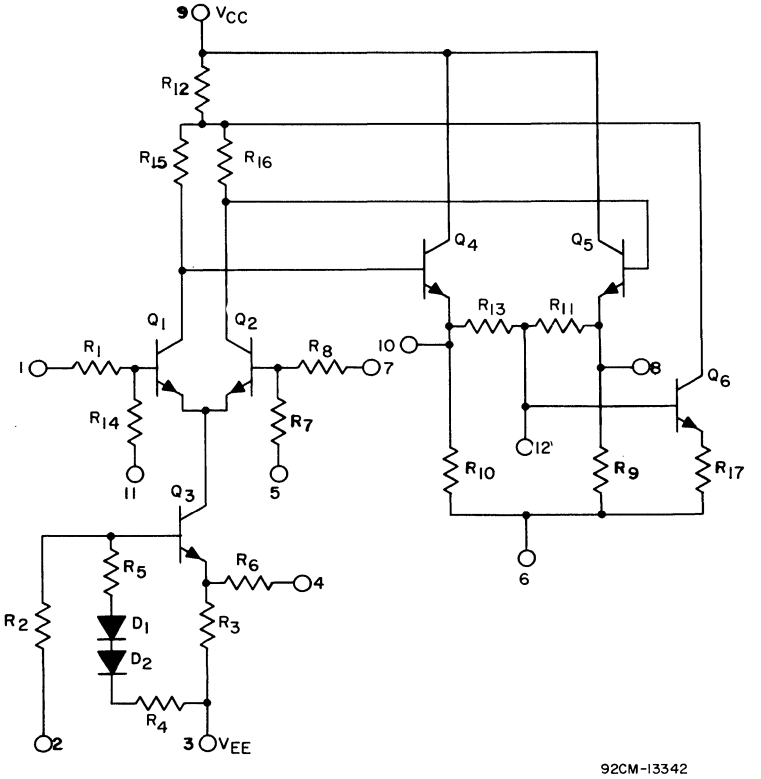


Fig. 79 — Schematic diagram of the CA3007 audio driver.

The two output signals from the phase splitter, which are 180 degrees out of phase, are direct-coupled through two emitter-followers (Q_4 and Q_5). The emitters of the differential pair are connected to the transistor constant-current sink Q_3.

The diodes in the bias circuit of the transistor constant-current sink make the emitter current of Q_3 essentially dependent on the temperature coefficient of the diffused emitter resistor R_3. Because the diffused collector resistors R_{15} and R_{16} should have identical temperature coefficients, constant collector-voltage operating points should result at the collectors of transistors Q_1 and Q_2. However, the quiescent operating voltages at the output terminals 8 and 10 increase as temperature increases because the base-emitter voltage drops of transistors Q_4 and Q_5 decrease as temperature increases. This small variation in the output quiescent operating voltage is sufficient to cause a large variation in the standby current of a class B push-pull output stage when the audio driver and

the output stage are direct-coupled. Resistors R_{11}, R_{12}, R_{13}, and R_{17} and transistor Q_6 form a dc feedback loop which stabilizes the quiescent operating voltage at output terminals 8 and 10 for both temperature and power-supply variations so that variations in the output operating points are negligible.

Resistors R_1, R_7, R_8, and R_{14} form the input circuit; a double-ended input is applied to terminals 1 and 5, and a single-ended input is applied to either terminal 1 or terminal 5, with the other terminal returned to ground. The CA3007 must be ac-coupled to the input source. In addition, any dc resistance between terminal 1 and ground should be added between terminal 5 and ground. Output power-gain stabilization for a direct-coupled driver and output stage is accomplished by means of an ac feedback loop that connects terminals 7 and 11 to the proper emitters of the push-pull output stage, as shown in Fig. 80.

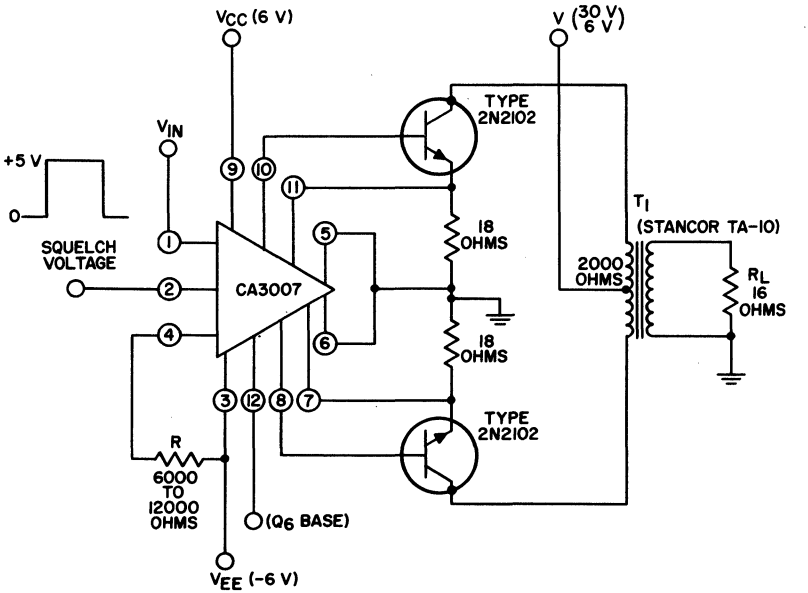


Fig. 80 — CA3007 used as an audio driver for a direct-coupled 300-milliwatt audio amplifier.

Connection of voltage supplies to the CA3007 audio driver requires that the most positive voltage be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). The CA3007 may be operated from various supplies and at various levels. Operation from either

a single supply (as shown in Fig. 81) or from dual power supplies (as shown in Fig. 80) is feasible. For dual-supply operation, symmetrical supplies must be used if the audio driver is to be

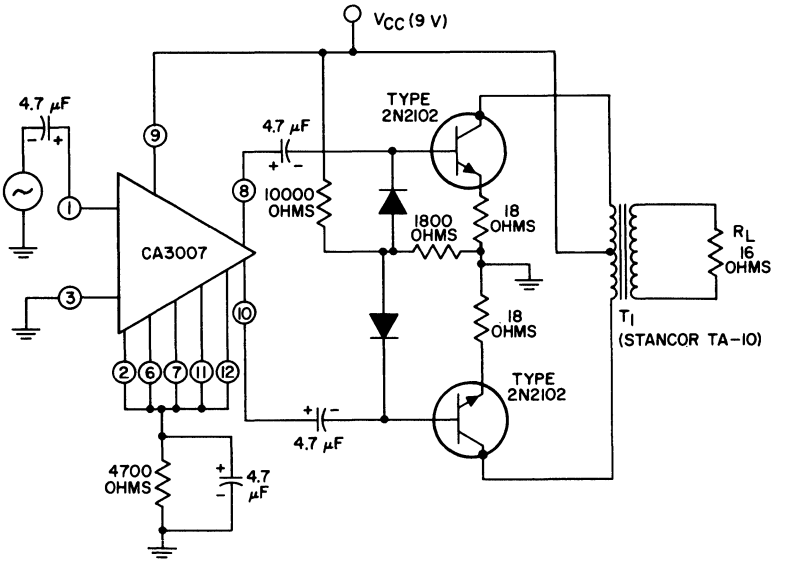


Fig. 81 — CA3007 used as an audio driver for a 30-milliwatt audio amplifier.

direct-coupled to the audio output stage. For single-supply operation, the audio driver must be ac-coupled to the audio output stage, and the number of external components required increases.

For operation from either single or dual supplies, the operating current in transistor Q_3 is determined by the bias voltage between terminals 2 and 3. The more negative terminal of this bias voltage must be connected to terminal 3. For dual-supply systems, terminal 2 is either grounded or connected to a trigger circuit for audio-squelching purposes.

Fig. 80 shows the CA3007 used as a dual-supply audio driver in a direct-coupled audio amplifier. This amplifier provides a power output of 300 milliwatts for an audio input of 0.3 volt rms (V_{CC} = 6 volts, V_{EE} = −6 volts, V = 30 volts). For a voltage V of 6 volts, the output power is 10 milliwatts without transformer optimization; the use of a lower-impedance transformer would permit power outputs in the order of 100 milliwatts.

The external resistor R connected between terminals 3 and 4 is used to set the class B output-stage standby current as required for a particular application. If the standby current is too

low, crossover distortion will result; if it is too high, standby power drain will be excessive. Decreasing the value of resistor R reduces the standby current; for a standby current of 10 milliamperes, R is typically 10,000 ohms.

Terminal 2 must be grounded or, if an audio squelch is desired, must be connected to a positive voltage supply of 5 volts minimum. When terminal 2 is near ground, the audio amplifier functions normally. When terminal 2 is at 5 volts, the differential pair of the audio driver saturates, and the push-pull output stage is cut off. The squelch source must be capable of supplying a current of 1.5 milliamperes in the 5-volt condition, and 0.75 milliampere in the near-ground condition.

For a symmetrical audio driver, there is no ac signal present at the base of transistor Q_6. However, unbalances between the two halves of the circuit may require that the base of Q_6 be bypassed for proper operation. The base of Q_6 may be bypassed by connection of an external capacitor (typically 50 microfarads, 6 volts) from terminal 12 to ground. Bypassing is usually not required unless high undistorted power outputs are required over the complete temperature range of −55 to 125°C.

Table VI shows values of harmonic distortion and intermodulaton distortion for the amplifier of Fig. 80.

Table VI—*Distortion Measurements for Direct-Coupled Amplifier Shown in Fig. 80*

Harmonic Distortion

Power Output (mW)	Output-Signal Level (mV rms) with 2-KHz Input Signal						Harmonic Distortion (%)
	2 kHz	4 kHz	6 kHz	8 kHz	10 kHz	12 kHz	
62.5	1000	9	3.0	—	—	—	0.95
140	1500	18	4.0	2.0	1.4	1.0	1.24
250	2000	25	4.2	5.0	1.0	1.5	1.30
330	2300	27	6.0	9.0	3.0	2.0	1.27

Intermodulation Distortion

Output-Signal Level:	
at f_1 (2 kHz)	1000 mV rms
at f_2 (3 kHz)	1000 mV rms
at $2f_2$-f_1 (4 kHz)	0.7 mV rms
3rd-Order IMD	0.07 %

Fig. 81 shows the CA3007 used as a single-supply audio driver in a capacitor-coupled audio amplifier. This amplifier provides a power output of 30 milliwatts for an audio input of 6.5 millivolts rms (V_{CC} = 9 volts) with the transformer shown.

The connection shown in Fig. 81 still represents a differential-pair phase splitter fed from a constant-current transistor. The two output signals from the phase splitter are direct-coupled through two emitter-followers which are capacitor-coupled to the push-pull output stage. Because of the ac coupling, there is no longer a dc dependence between the driver and the output stage, and any desired audio output design or drive source may be used. As a single stage, the CA3007 audio driver provides a voltage gain of 24 dB for a dc power dissipation of 20 milliwatts with the harmonic distortion reaching 3 per cent for outputs of 0.6 volt rms at terminals 8 and 10 (without feedback).

Both dc and ac feedback loops are eliminated in the circuit of Fig. 81. Although the dc feedback loop is no longer required because of the ac coupling, removal of the ac feedback loop causes the output power gain to decrease about 1 dB for a 50°C rise in temperature.

INTEGRATED-CIRCUIT VIDEO AMPLIFIER

The CA3001 integrated circuit, shown in Fig. 82, is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 is available in a 12-terminal TO-5 style low-silhouette package.

The circuit consists of a differential pair of transistors, Q_3 and Q_5, the current of which is controlled by a constant-current transistor Q_4. Transistors Q_1, Q_2, Q_6, and Q_7 are operated in the common-collector configuration to provide a high-impedance input and low-impedance output. Thus, the CA3001 provides double-ended input and output, and can be iteratively connected with low-value coupling capacitors. The high-frequency response of the circuit is determined primarily by the resistance and capacitance in the collectors of the differential pair Q_3 and Q_5.

Biasing Requirements and Operating Modes

When voltage supplies are connected to the CA3001, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). For typical operation, terminals 2 and 10 are returned to ground. If desired, however, automatic gain control can be applied to terminal 2, and terminal 10 can be connected to the negative supply to permit larger negative-going output swings in the output transistors.

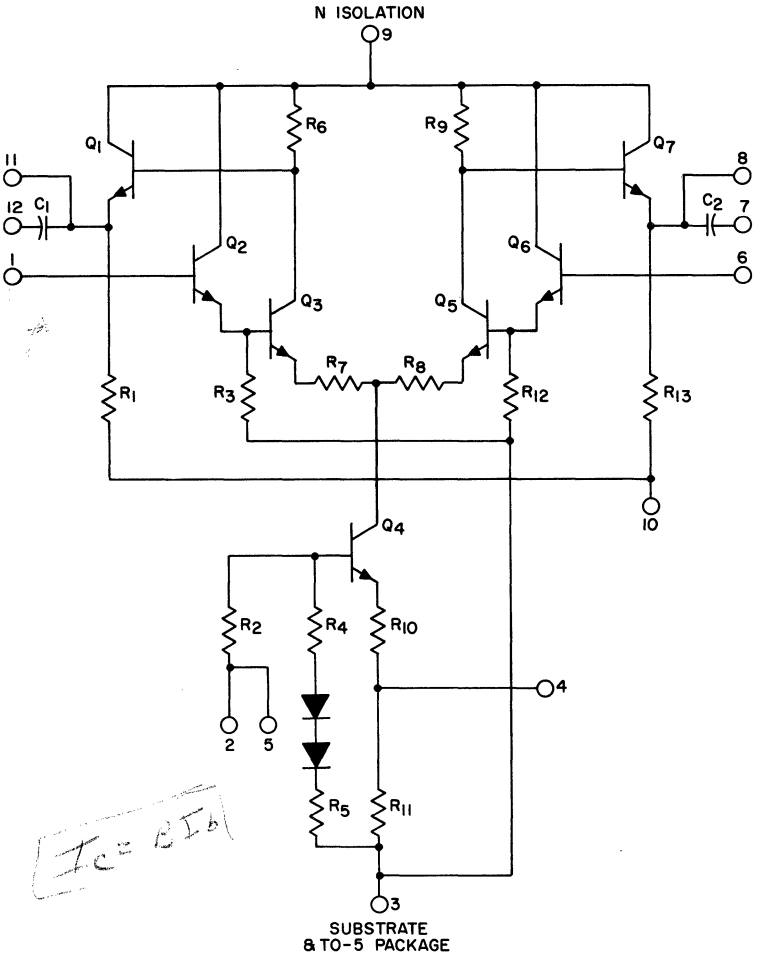


Fig. 82 — Schematic diagram of the CA3001 video amplifier.

The CA3001 may be operated with various supplies and at various levels. Operation from either a single supply or dual supplies is feasible, as shown in Fig. 83. When dual supplies are used, they may be either symmetrical or non-symmetrical. The use of separate positive and negative supplies minimizes the need for external components, as shown in Fig. 83(a). For single-supply applications, a resistor divider and a bypass capacitor must be added, as shown in Fig. 83(b).

When dual supplies are used, the inputs (terminals 1 and 6) are returned to ground through equal external resistors (the maximum recommended value of R is 3300 ohms for linear operation).

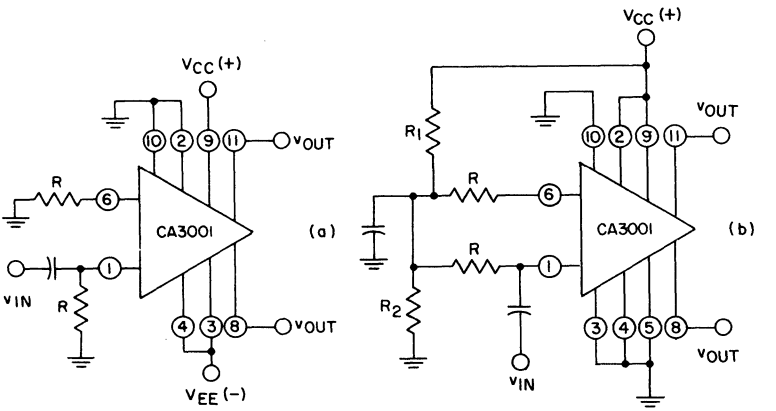


Fig. 83 — Circuit connections for the CA3001 for (a) separate positive and negative voltage supplies, and (b) a single supply.

The current through the resistor divider R_1 and R_2 should be greater than 1.5 milliamperes. For either single or dual supplies, the operating current in transistor Q_4 is determined by the operating mode. For any given bias voltage, four operating modes are possible, as described in Table VII. Each mode is characterized by a distinct operating current and a corresponding voltage gain, both of which have a particular temperature dependence.

Table VII—*Four Possible Operating Modes for CA3001 Amplifier*

Operating Mode	Shorted Terminals	Condition of Diodes	Q_4 Emitter Resistor
A	none	in	$R_{10} + R_{11}$
B	5-3	out	$R_{10} + R_{11}$
C	4-3	in	R_{10}
D	5-4-3	out	R_{10}

Table VIII shows typical design performance characteristics for the four operating modes of the CA3001 at room temperature. The output operating point and voltage gain of the circuit are reasonably independent of resistor value, but the current and power dissipation may vary with resistor values. Figs. 84 and 85 show theoretical curves of output operating point and voltage gain, respectively, as functions of temperature for nominal resistor values with supply voltage V_{EE} of −3 and −6 volts dc. The voltage between terminals 8 and 9 or terminals 11 and 9 is denoted by V_X. Because the variation of voltage gain and operating point with temperature is small for all operating modes, the choice of mode

depends on application requirements. With a supply voltage V_{EE} of −4.5 volts, voltage-gain variation is normally less than 0.5 dB for all operating modes over the temperature range of −55 to 125°C.

Table VIII—*Typical Design Performance Characteristics for the CA3001 Amplifier (terminals 2, 10, 6, and 1 referenced to ground) at 25°C*

Operating Mode	Supplies (±V)	Output Operating Volts (Term. 8 and 11 to ground)	Positive Supply Current (mA)	Negative Supply Current (mA)	Power Dissipation (mW)	Single-Ended Voltage Gain at 1 MHz (dB)
A	6	4.3	8.4	−4.7	79	15.5
B	6	4.8	7.8	−3.9	70	12.7
C	6	2.8	9.9	−7.9	106	17.8
D	6	4.1	8.7	−5.5	85	16.4
A	4.5	3.0	6.0	−3.4	43.6	14.6
B	4.5	3.4	5.6	−2.7	37.6	10.0
C	4.5	2.0	7.2	−5.8	58.4	17.7
D	4.5	2.9	6.0	−3.7	43.6	15.5
A	3	1.8	3.7	−3.9	22.6	13.0
B	3	2.1	3.3	−1.4	14.3	3.8
C	3	1.0	4.4	−3.7	25.5	16.4
D	3	2.0	2.4	−1.9	13.0	10.8

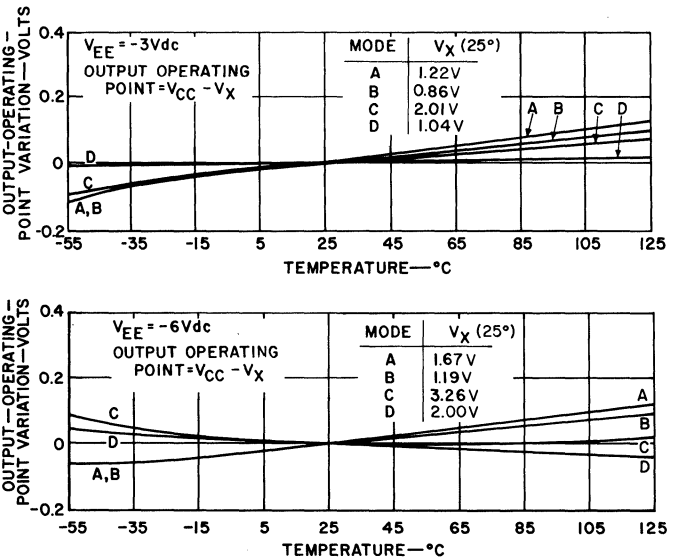


Fig. 84 — Output operating point of the CA3001 (normalized to the 25°C operating point) as a function of temperature for V_{EE} supplies of −3 and −6 volts dc.

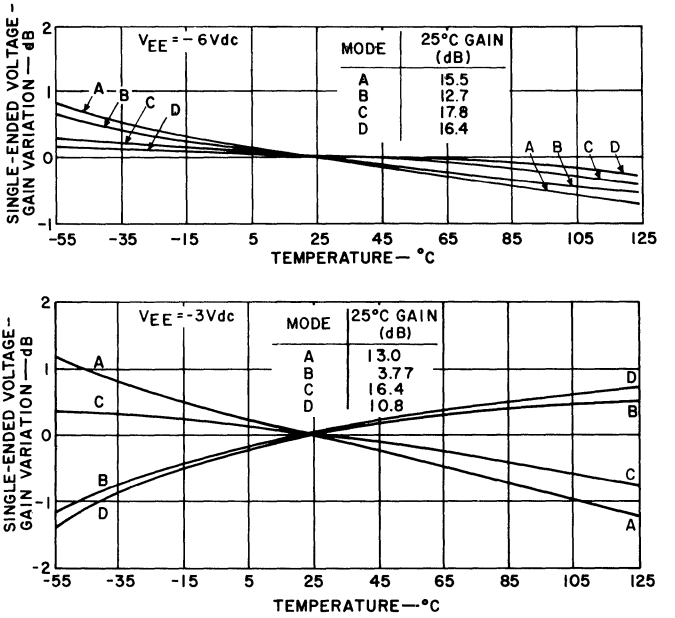
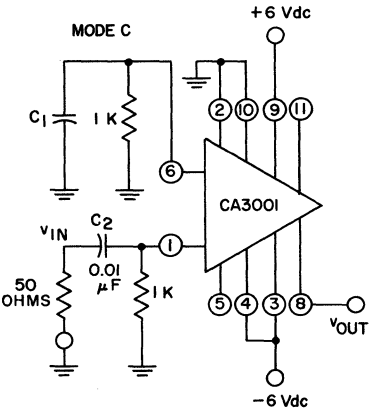


Fig. 85 — Voltage gain of the CA3001 (normalized to the 25°C gain) as a function of temperature for V_{EE} supplies of −3 and −6 volts dc.

Frequency Response

When the CA3001 video amplifier is used in cascade, its high-frequency response is determined primarily by the RC roll-off at the collectors of the differential pair Q_3 and Q_5. The generator source resistance may affect high-frequency bandwidth; for full bandwidth capability, the parallel combination of source resistance and base-bias resistance should not exceed 800 ohms. The low-frequency response is determined by the coupling capacitor and the base-bias resistance value.

Fig. 86 shows the circuit used for evaluation of frequency response of the CA3001, together with the response characteristics obtained. The circuit is operated in mode C with supplies of ±6 volts. The 50-ohm generator simulates the frequency and gain behavior for iterative operation. The curves of Fig. 86 show the measured response characteristics with terminal 6 bypassed and unbypassed. When terminal 6 is bypassed, the voltage gain is down 3 dB at 16 MHz, and is greater than 10 dB through 30 MHz. When the non-driven input (terminal 6 in the circuit shown) is not bypassed, the gain decreases more rapidly as a result of the feedback capacitance between terminals 7 and 6. This feedback



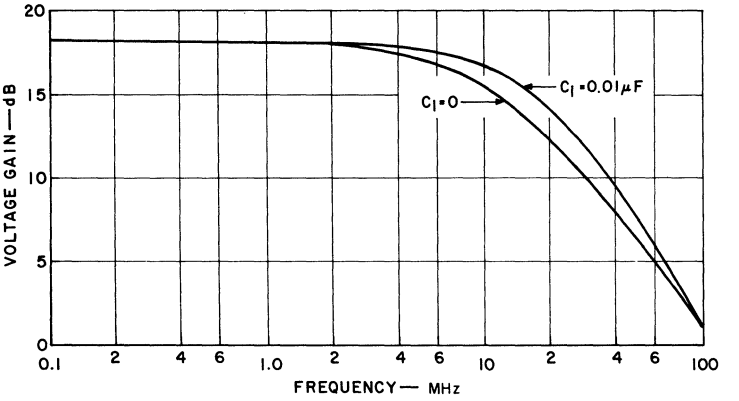


Fig. 86 — Frequency response of the CA3001 as a function of capacitor C_1 in the test circuit shown with terminal 6 bypassed and unbypassed.

can be minimized by use of short leads and inter-terminal shielding. A shielding method is to ground terminal (7).

The high-frequency roll-off of the CA3001 is a function of the values of resistors R_6 and R_9 in Fig. 82 and their variation with temperature. Fig. 87 shows the effect of temperature on high-frequency response. The variation in response can be accounted for by the resistance variation with temperature; capacitance variations with temperature are a secondary effect.

The internal capacitors provided at the outputs of the CA3001 (C_1 and C_2 in Fig. 82) can be used for coupling circuits in cascade for narrow-band applications. Because the value of these

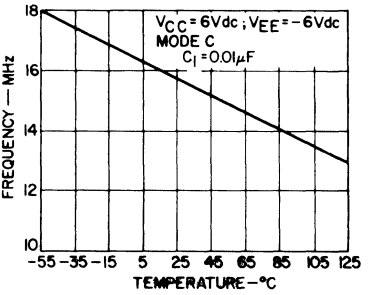


Fig. 87 — High-frequency 3-dB bandwidth of the CA3001 as a function of temperature.

capacitors is small, the external base-bias resistors shown in Fig. 85 should be increased from 1000 to 3300 ohms to improve low-frequency response. Fig. 88 shows the response characteristics for a single stage in which the input is applied to terminal 1 from a 50-ohm generator through a capacitor (equal in value to C_1 in Fig. 82), and the voltage gain is measured from the generator to output terminal 8. Because this arrangement simulates single-ended operation, the results can be applied directly to iterative operation.

The voltage division between the input capacitance and the coupling capacitor causes a reduction in voltage gain at all frequencies. The feedback capacitance from output to input also affects the gain performance, as shown in Fig. 88.

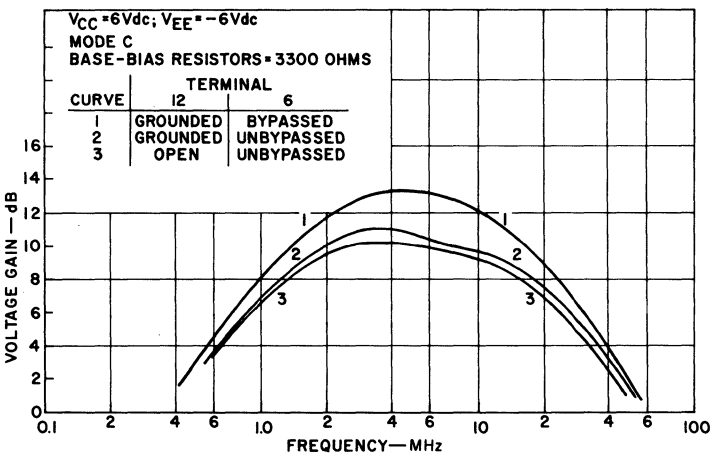


Fig. 88 — Response characteristics of a CA3001 amplifier with capacitor-coupled input.

Input and Output Impedances

Fig. 89 shows the parallel input resistance and capacitance of the CA3001 as a function of frequency. The input capacitance is constant until it begins to decrease at high frequencies. The input

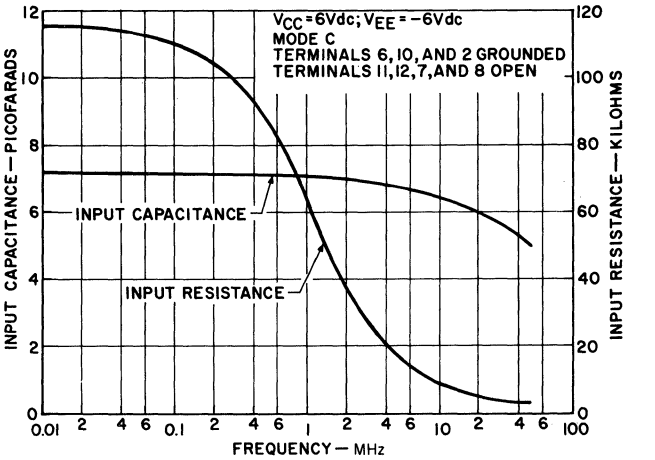


Fig. 89 — Parallel input resistance and capacitance of the CA3001 as functions of frequency.

resistance decreases through the frequency range from 0.1 to 10 MHz. Because the input resistance is high in comparison with the external base-bias resistors used (3300 ohms maximum), the high-frequency response characteristic of the input is determined by the driving-source resistance, the base-bias resistors, and the parallel input capacitance.

The parallel output resistance of the CA3001 is low (approximately 70 ohms), and the output reactance is sufficiently high to provide little or no degradation of frequency response through the usable frequency range.

Noise Figure

Fig. 90(a) shows noise figure as a function of frequency for a 1000-ohm source. The 1/f noise corner occurs at approximately 30 kHz; above this frequency, the noise figure remains flat at approximately 5 dB to 6 MHz, and then begins to rise.

Fig. 90(b) shows noise figure as a function of source resistance for frequencies of 1.75 and 12 MHz. For stages in which noise performance is important, the source resistance should not be less than 500 ohms because of the rapid rise in noise figure at

lower values. The noise figure of the CA3001 increases when non-driven base-bias resistors are unbypassed. For stages in which noise performance is important, the external resistor on an input base that is not receiving the signal must be bypassed if minimum noise figure is to be achieved.

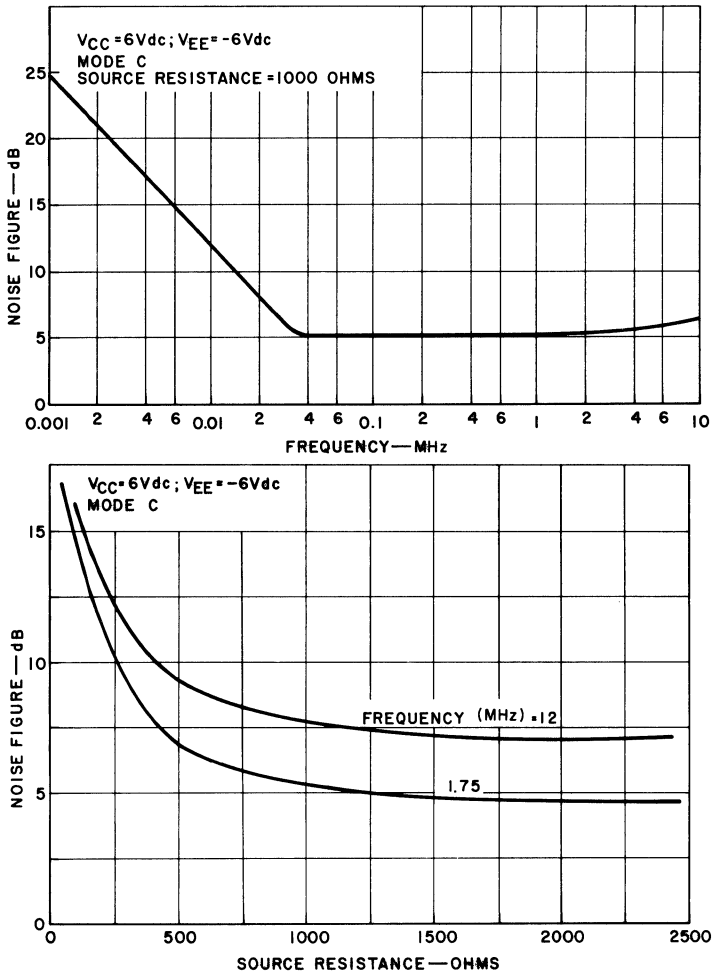


Fig. 90 — Noise figure of the CA3001 as a function of frequency and source resistance.

Gain Control

AGC can be applied to the CA3001 at terminal 2 for any of the four operating modes. Fig. 91 shows representative agc characteristics for modes C and D at a frequency of 1 MHz. The

threshold voltage is higher in mode C than in mode D because of the difference in the base-bias circuit for the constant-current sink transistor (Q_4).

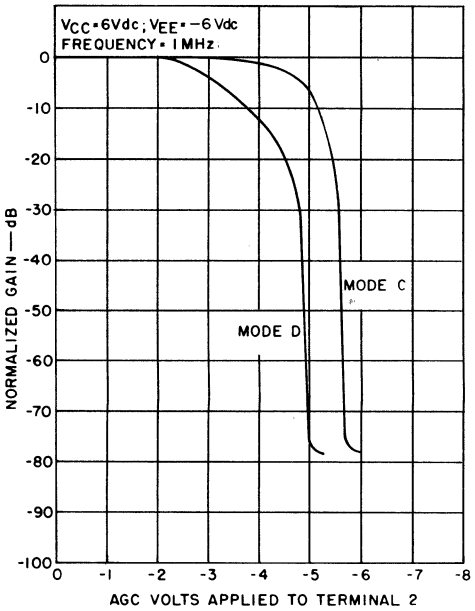


Fig. 91 — AGC characteristics of the CA3001 in modes C and D at 1 MHz.

The agc range is dependent on frequency at high frequencies because the feedthrough parameters are primarily capacitive; therefore, it should eventually decrease at a rate of approximately 20 dB per decade. The average measured agc range at 10 MHz is 62 dB, and is 15 dB less than that at 1 MHz.

Common-Mode Rejection

Fig. 92(a) shows the common-mode rejection of the CA3001 as a function of temperature at a frequency of 1 kHz. The common-mode rejection increases with increasing temperature; a typical value at 25°C is 70 dB.

Because the CA3001 can be used in many applications with a single-ended output at high frequencies, both the single-ended differential gain and the single-ended common-mode gain are of considerable interest. Fig. 92(b) shows both single-ended common-mode and differential-mode gain as functions of frequency.

The common-mode gain is a function of the impedance ratio between the constant-current transistor (Q_4) and the load resistor in one side of the differential pair (Q_3 or Q_5). The common-mode gain increases with increasing frequency.

The common-mode rejection is degraded if sufficient signal is applied to saturate the constant-current transistor (Q_4). The

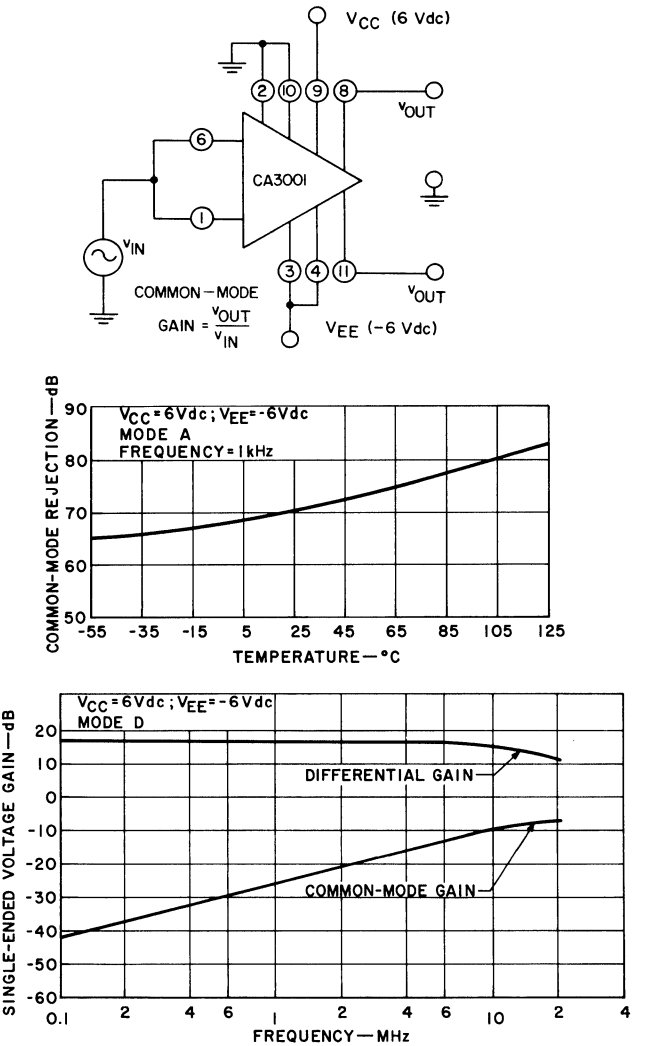


Fig. 92 — Common-mode rejection and voltage-gain characteristics of the CA3001 as a function of temperature and frequency.

maximum peak-to-peak input voltage without degradation of common-mode rejection is a function of the voltage supplies and the operating mode of the constant-current transistor.

Harmonic Distortion and Swing Capability

When equal positive and negative supplies are used, operating mode C provides the largest swing capability because the output operating point is approximately centered. With voltage supplies of ±6 volts dc at a frequency of 1 MHz, the single-ended output is 1.3 volts rms for 3-per-cent distortion in mode C and 0.665 volt rms in mode D.

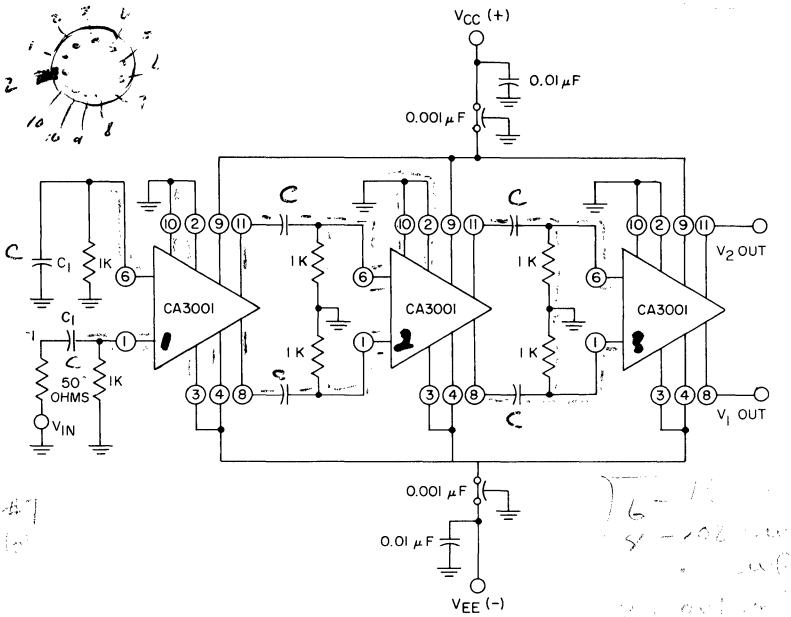
The signal-swing capability was also evaluated as a function of temperature in mode C with voltage supplies of ±6 volts dc. For 3-per-cent distortion, an output swing of 1.2 volts rms can be obtained over the complete temperature range from 25 to 125°C.

For pulse-type signals, the total possible swing capability is important. The voltage at the collectors of the differential pair may rise to the positive supply voltage, V_{CC}, and fall to the saturation level. If the bases of the input emitter-followers are maintained at zero potential, the emitters of the differential pair are negative by twice the base-to-emitter voltage drop, V_{BE}, or approximately −1.4 volts. If the saturation voltage is assumed to be 0.2 volt, the collectors drop to about −1.2 volts before saturation. Therefore, the total swing available at the collectors is approximately V_{CC} + 1.2 volts; for a V_{CC} of 6 volts, the swing is 7.2 volts. The output voltage swing is lower than this value by V_{BE}, or from 5.3 to −2.0 volts. This total swing capability can be realized only when the resistors R_1 and R_{13} (terminal 10) are returned to the negative supply voltage (terminal 10 shorted to terminal 3). Selection of the operating point to obtain most of the available total swing in one direction involves proper choice of the operating mode and the negative supply voltage.

Cascade Operation

Over-all performance characteristics for three CA3001 stages operated in cascade are shown in Fig. 93. The need for supply decoupling is minimized by the symmetry of the circuit, which ensures equal and out-of-phase currents in the supply leads. Three circuits in close proximity can provide stable over-all gains of

approximately 65 dB. A further advantage of the CA3001 in cascade is that a gain increase of 6 dB accrues each time a double-ended output is used.



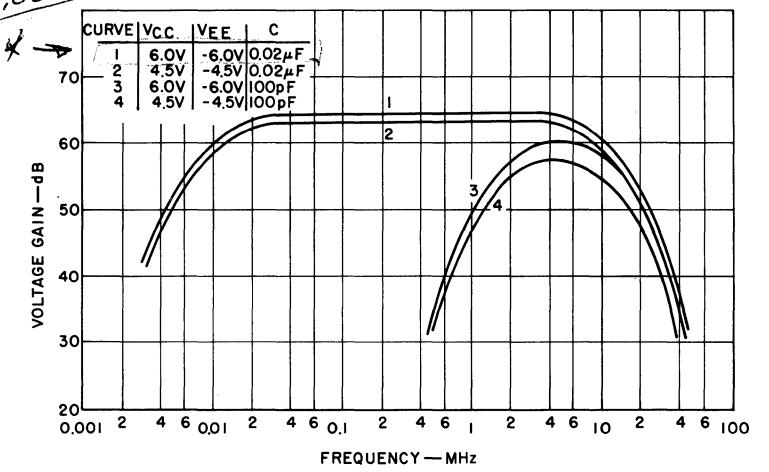


Fig. 93 — Three-stage CA3001 cascade amplifier and frequency-response characteristics.

Table IX and Fig. 93 show the performance of the CA3001 in the three-stage cascade circuit for various values of supplies and coupling capacitors. The only advantage of ±6-volt supplies as compared to ±4.5-volt supplies is a larger output-swing capability.

Table IX—*Performance of CA3001 Cascade Amplifier shown in Fig. 93*

Coupling Capacitor	0.02 μF		100 pF		
Voltage Supplies	±6	±4.5	±6	±4.5	Vdc
Power Dissipation	276	146	276	146	mW
Single-Ended-Output Mid-Band Gain	64.5	63	60.5	57.5	dB
3-dB Response: Upper	9	9	10.5	10.5	MHz
Lower	0.0125	0.0125	1.9	1.9	MHz
AGC Range	65	63	61	59	dB
Output Signal for 3-per-cent Distortion	1.3	1.15	1.15	0.7	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio	26	14	20	18.5	μVrms

The use of ±4.5-volt supplies entails no sacrifice in bandwidth and little gain loss, and provides a saving in power dissipation of almost 2 to 1. Better signal-to-noise performance can be achieved with no change in bandwidth if a higher value of source resistor is used (e.g., 800 ohms, rather than the value of 50 ohms shown in Fig. 93). The agc range of the cascaded circuit was 10 dB less than that for an individual circuit because no interstage shielding was provided and double-ended output was not used.

The CA3001 was also evaluated in a three-stage cascade arrangement in which the internal capacitors were used for coupling. The circuit diagram for this evaluation is shown in Fig. 94, and the measured characteristics are shown in Table X and Fig. 94.

Table X—*Performance of CA3001 Cascade Amplifier shown in Fig. 94*

Operating Mode	C	
Voltage Supplies	±6	Vdc
Power Dissipation	276	mW
Single-Ended-Output Mid-Band Gain	51.5	dB
3-dB Response: Upper	11.3	MHz
Lower	1.8	MHz
Output Signal for 3-per-cent Distortion	0.85	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio	19	μVrms

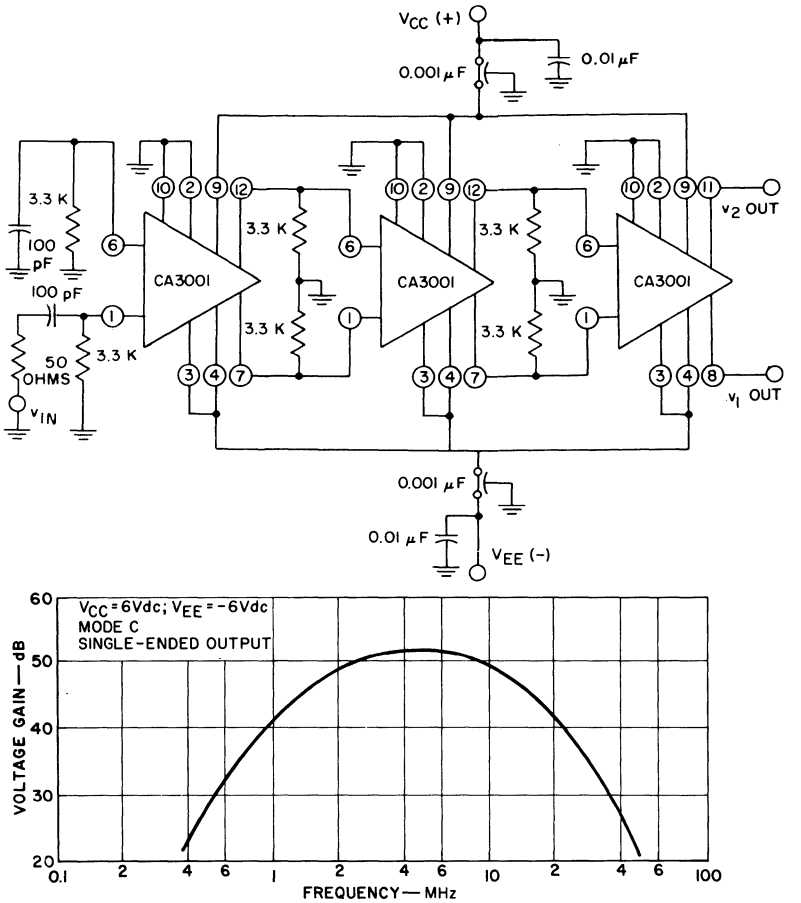


Fig. 94 — Three-stage CA3001 cascade amplifier using internal capacitors for coupling and frequency-response characteristics.

Schmitt-Trigger Operation

The CA3001 has an advantage in Schmitt-trigger applications because the emitter-follower outputs isolate the impedances of the feedback loop from the differential stage. These outputs are also capable of driving low-impedance loads. When symmetrical power supplies of up to ±6 volts are used, the CA3001 operates without saturation of the basic differential pair (Q_3 and Q_5). For each of the four operating modes, a complete offset at the input that causes all the sink-transistor current to pass through either Q_3 or Q_5 does not bring these transistors into saturation. As a result, uncertainties resulting in hysteresis prediction caused by storage time are eliminated.

When the CA3001 is connected as a Schmitt trigger, as shown in Fig. 95, the firing points can be changed by adjustment of the resistor R_2. This resistor value effectively sets the voltage at the

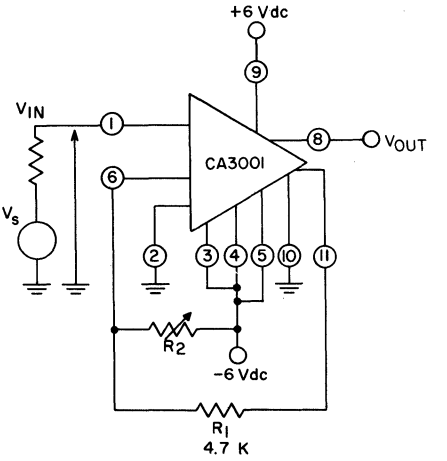


Fig. 95 — CA3001 Schmitt trigger.

input terminal 6 and requires that the input firing voltage at terminal 1 approach this value to obtain trigger action. The hysteresis voltages obtained for various trigger levels in the circuit of Fig. 95 are shown in Table XI.

Table XI—*Performance Data for CA3001 Used as a Schmitt Trigger*

Input Firing Volts			
Transition from State 1 to State 2	Transition from State 2 to State 1	Hysteresis Volts	R_2 Approximate Setting
3.0	1.5	1.5	max. resistance
1.1	0.1	1.0	decreasing R_2
−1.4	−1.9	0.5	
−3.2	−3.2	0	

INTEGRATED-CIRCUIT IF AMPLIFIER

The CA3002 integrated-circuit if amplifier can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors,

and various trigger circuits. The if amplifier is supplied in a 10-terminal TO-5 style low-silhouette package.

Fig. 96 shows the circuit diagram for the CA3002 integrated circuit. The circuit is basically a single-stage balanced differential amplifier (Q_2 and Q_4) with input emitter-followers (Q_1 and Q_5),

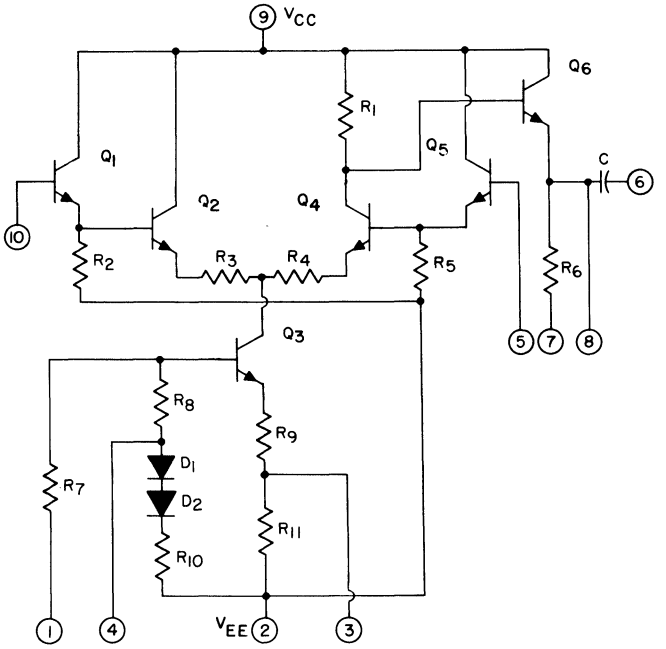


Fig. 96 — Schematic diagram of the CA3002 integrated-circuit if amplifier.

a constant-current sink (Q_3) in the emitter-coupled leg, and an output emitter-follower (Q_6). A single-ended input is connected to terminal 10 or a push-pull input to terminals 10 and 5. A single-ended output is direct-coupled at terminal 8 or capacitance-coupled at terminal 6. Terminals 5 and 10 must be provided with dc returns to ground through equal external base resistors. The emitters of the differential pair (Q_2 and Q_4) are connected through degenerative resistors (R_3 and R_4) to the transistor current source (Q_3). The use of these resistors improves the linearity of the transfer characteristic and increases the signal-handling capability.

Transistor Q_1 provides a high input impedance for the if amplifier. Transistor Q_5 preserves the circuit symmetry, and also partially bypasses the base of Q_4. Additional bypassing can be obtained by connection of an external capacitor between terminal 5 and

ground. The emitter-follower transistor Q_6 provides a direct-coupled output impedance of less than 100 ohms.

Circuit Characteristics

When voltage supplies are connected to the CA3002, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 2 (internally connected to the substrate and case). The CA3002 may be operated from various supplies and at various levels. Operation from either single or dual power supplies is feasible. When two supplies are used, they may be either symmetrical or non-symmetrical. When both positive and negative voltage supplies are used, external components can be minimized, as shown in Fig. 97(a). For single-supply applications, a resistor divider and a bypass capacitor must be added externally, as shown in Fig. 97(b). The current through R_2 and R_3 should be greater than one milliampere. Except in applications that use inductive drive, equal external base resistors must be added at terminals 5 and 10 to provide base-current returns. Terminal 7 can be connected to ground, or to the negative supply if a larger negative-going voltage swing is desired at any operating point.

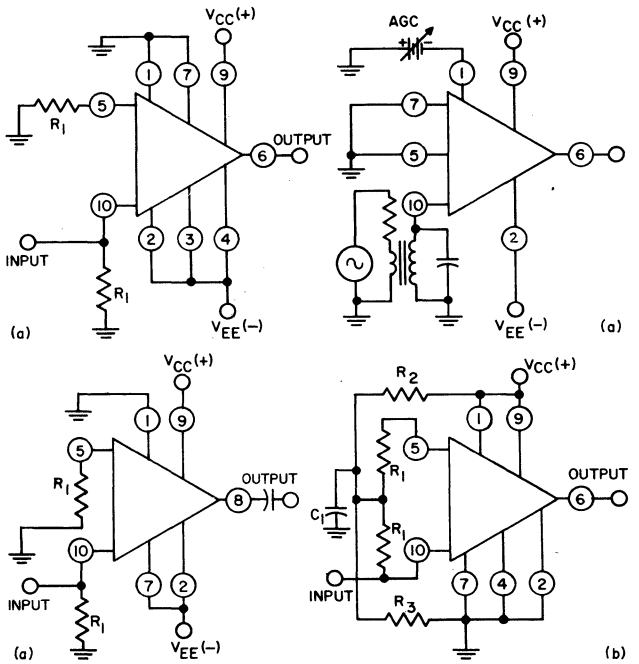


Fig. 97 — Circuit configurations for the CA3002 with (a) dual voltage supplies, and (b) a single supply.

For either single or dual supplies, the operating current in transistor Q_3 is determined by the bias voltage between terminals 1 and 2. The more negative point of this bias voltage must be connected to terminal 2. For dual-supply systems, terminal 1 is usually referenced to ground.

Operating Modes — For any given bias voltage (V_{EE} when terminal 1 is grounded), four operating modes are possible, as described in Table XII. In general, each mode is characterized by (1) a distinct dc operating point with a characteristic temperature dependence, and (2) a particular value of gain that has a distinct temperature dependence.

Table XII—*Identification of CA3002 Operating Modes*

Operating Mode	Shorted Terminals	Condition of Diodes	Q_9 Emitter Resistor
A	none	in	$R_9 + R_{11}$
B	4-2	out	$R_9 + R_{11}$
C	3-2	in	R_9
D	4-3-2	out	R_9

When the diodes are utilized in the bias circuit (modes A and C), the current is essentially dependent on the temperature coefficient of the diffused emitter resistors R_9 and R_{11}, and has a tendency to decrease with increasing temperature at a rate independent of the negative supply voltage. The temperature coefficient of the diffused collector resistor R_1 is the same as that of the emitter resistor, and a constant collector-voltage operating point results at the collector of transistor Q_4. However, the operating point at output terminal 8 is modified by the base-emitter voltage drop of transistor Q_6 and its temperature dependence. Typical variation of the output operating point with temperature is shown in Fig. 98 for the four operating modes for V_{EE} supplies of −3

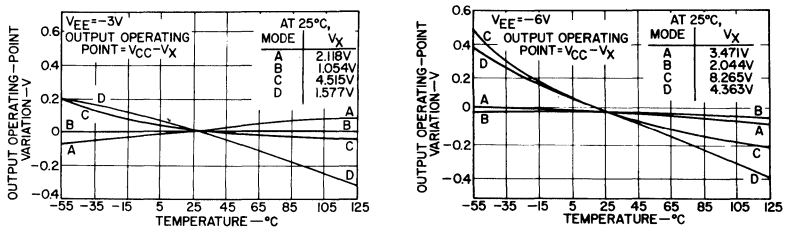


Fig. 98 — Output operating-point variation of the CA3002 (normalized to the 25°C operating point) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

and −6 volts. The voltage between terminals 8 and 9 is denoted by V_X. In mode B (with the diodes out of the bias circuit), it

should be noted that the output operating point is constant with temperature because the change in the collector operating point is cancelled by the change in the base-emitter voltage drop (V_{BE}).

When the diodes are out of the bias circuit, the current-temperature curves become dependent on the negative supply voltage. Therefore, the value of V_{EE} can be adjusted so that the transconductance decreases, increases, or remains constant with temperature. As shown in Fig. 99, the gain increases with temperature for a −3-volt V_{EE} supply, but decreases with increasing temperature for a −6-volt V_{EE} supply. At some intermediate value of V_{EE}

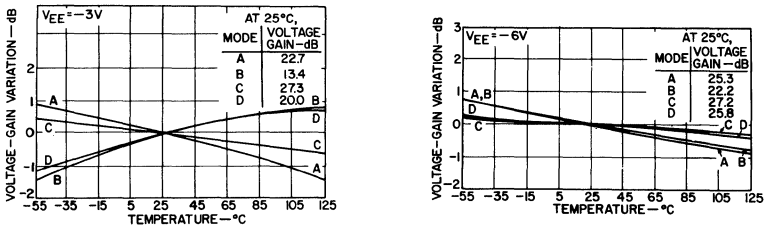


Fig. 99 — Voltage-gain variation of the CA3002 (normalized to the 25°C voltage gain) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

(approximately −4.5 volts), the gain should be constant as a function of temperature. In any case, however, a constant ac gain with temperature is accompanied by a change in the collector operating point of transistor Q_4.

Table XIII lists typical design performance characteristics for the four operating modes of the CA3002. By use of the data

Table XIII—*Typical Design Performance Characteristics for the Four Operating Modes of the CA3002 (Terminals 7 and 1 are grounded; temperature = 25°C)*

Mode	± Supply Volts	Output Operating Volts (Term. 8 to ground)	Voltage Gain (dB) at 1 MHz	+ Supply Current (mA)	− Supply Current (mA)	Power Dissipation (mW)
A	6	2.6	26.4	5.0	4.2	55.2
B	6	3.8	22.5	4.7	3.7	50.4
C	6	0	*	*	*	*
D	6	1.8	25.4	5.1	4.9	60
A	4.5	2.0	24.0	3.6	3.0	29.7
B	4.5	3.0	19.8	3.4	2.6	27.0
C	4.5	0	*	*	*	*
D	4.5	1.8	24.5	3.7	3.3	31.5
A	3	1.1	22	2.3	2.0	12.9
B	3	2.0	14.5	2.1	1.5	10.8
C	3	0	*	*	*	*
D	3	1.5	20	2.2	1.9	12.3

* Transistor Q_4 saturated, transistor Q_6 cut off.

in this table and in Figs. 98 and 99, it is possible to select the proper operating mode to provide the most transconductance per milliwatt of dissipation, the specified output-swing capability, and the desired temperature performance for a particular design requirement.

In operating mode C, a valid non-saturated operating point may be obtained by use of non-symmetrical voltage supplies. For example, when V_{EE} is -3 volts, the operating point will not be in saturation if a positive supply voltage of 4.5 volts or more is used (as indicated by Fig. 98). Resistor R_6 may then be returned to the negative supply instead of to ground to ensure the desired negative swings.

Input Offset Current — Fig. 100 shows a curve of input offset current of the CA3002 as a function of temperature. This offset current determines the maximum value of total effective external

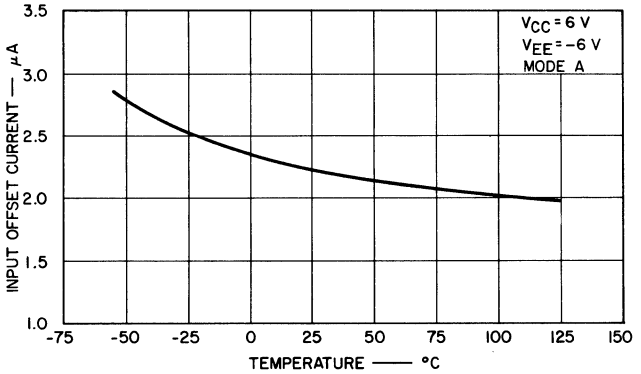


Fig. 100 — Input offset current of the CA3002 as a function of temperature.

resistance that may be used in each base circuit (resistors R_1 in Fig. 97). A maximum value of 10,000 ohms is recommended for each base circuit. However, larger resistances may be accommodated if the resistors can be adjusted to maintain low input offset voltages, or if the operating points of Q_1 and Q_5 are not in the linear region (as in trigger circuits).

Input Impedance — The input impedance of the CA3002 is essentially a characteristic of the input emitter-followers, Q_1 and Q_5. Because these transistors are lightly loaded, they have parallel input impedances that are approximately 0.1 megohm at low frequencies and rise to infinity and become negative at a few megahertz. In most cases, these impedances are negligible in comparison

with the impedances of external base resistors or inductors. The input capacitance is 3 to 5 picofarads.

The input impedance decreases with decreasing operating temperature. A typical low-frequency value of parallel input resistance is 55,000 ohms at −55°C. If a resonant line or tuned circuit that has appreciable impedance in the vhf range is connected to either input terminal, a series parasitic resistor of 50 to 100 ohms should be placed in series with the input lead to prevent vhf oscillation.

Output Impedance — The output impedance of the CA3002 is essentially that of the output emitter-follower Q_6, and is a function of the current in Q_6. The current, in turn, is determined by the operating mode, the supply voltages, and the connection of resistor R_6 to ground or to terminal 2. In operating mode D with R_6 returned to ground and ±6-volt supplies, the output resistance is approximately 80 ohms over most of the useful frequency range and rises to about 110 ohms (its highest value) at −55°C.

Frequency Response — The mid-frequency voltage gain of the CA3002 if amplifier is essentially independent of absolute resistor values, but depends on the resistor ratios. Fig. 101 shows a test circuit used to measure the response characteristics of an iterative-coupled amplifier that uses an input-coupling capacitor of 15 picofarads.

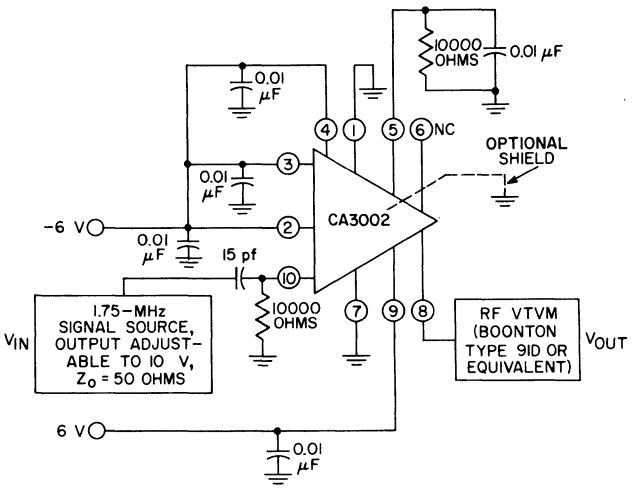
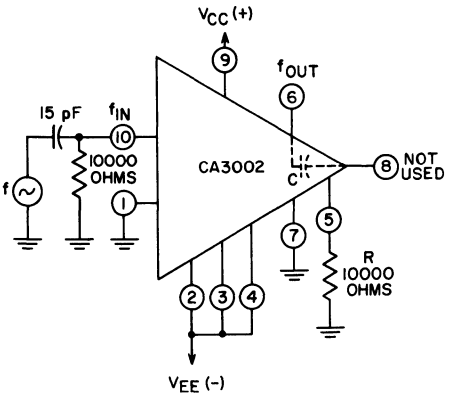


Fig. 101 — Voltage-gain test circuit.

The response curves for several values of positive and negative supply voltage are shown in Fig. 102. The gain of the amplifier is reduced at low frequencies by the 15-picofarad input-coupling capacitor and at high frequencies by the RC roll-off within the circuit. The addition of a 0.01-microfarad bypass capacitor at terminal 5 improves both the high-frequency response and the mid-frequency gain by eliminating ac feedback from terminal 6 to terminal 5.



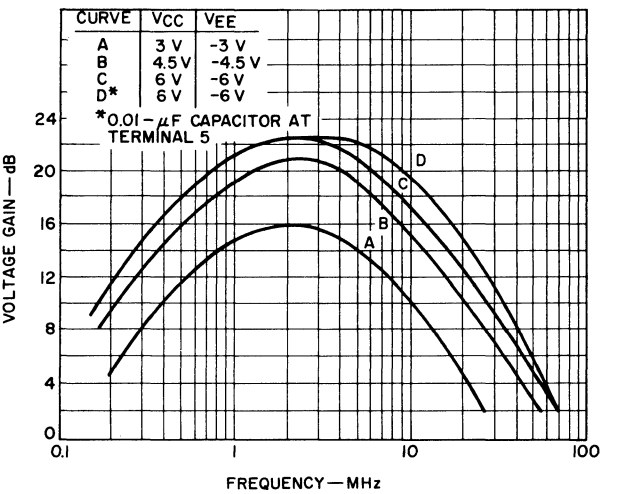


Fig. 102 — Effective single-stage response characteristics of iterative-coupled if amplifier. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).

If a wide-band video response is desired, the 15-picofarad internal silicon output-coupling capacitor of the CA3002 must be replaced with a larger external coupling capacitor connected to terminal 8. The response curves for an iterative-coupled amplifier that uses 0.01-microfarad input-coupling and output-coupling capacitors are shown in Fig. 103. The response of the amplifier is substantially extended at the low frequencies. If 1-microfarad coupling capacitors are used, the low-frequency response can be extended below 100 Hz. Again, the addition of a 0.01-microfarad capacitor at terminal 5 improves the high-frequency performance.

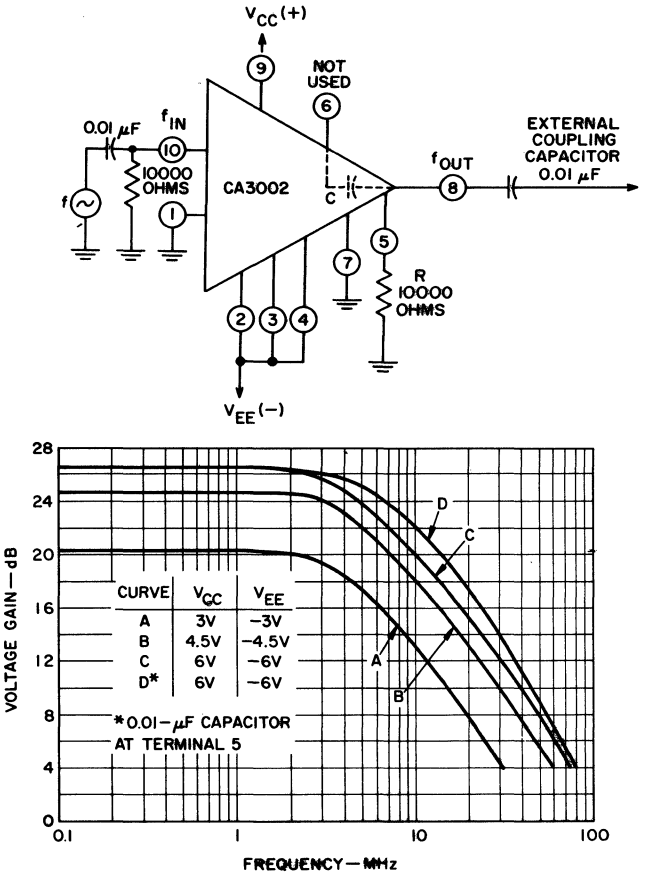


Fig. 103 — Effective single-stage response characteristics for if amplifier using 0.01-microfarad coupling capacitors. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).

A shield separating the external leads at terminals 5 and 6 also reduces the feedback and extends the response.

Gain Control — The voltage gain of the CA3002 can be controlled over a wide range by adjustment of a negative dc voltage applied at terminal 1. Fig. 104 shows the voltage gain at 1.75 MHz (measured in the test circuit of Fig. 101) as a function of the dc voltage. When the gain is controlled in this manner, the

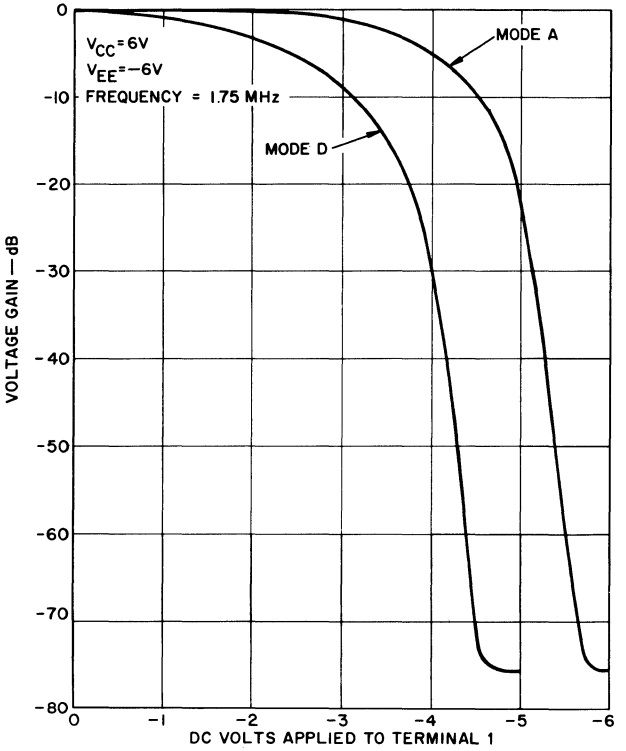


Fig. 104 — Voltage gain of the CA3002 as a function of negative dc supply voltage applied at terminal 1 (normalized to a gain of 26 dB).

CA3002 can be used as an if amplifier with a 75-dB agc range, or as a video gating, squelching, or blanking circuit with a similar range. The circuit function depends only on the manner in which the dc voltage applied to terminal 1 is controlled. The agc range is dependent on frequency, and decreases from 75 dB at 1 MHz to 60 dB at 25 MHz.

Third-Order Intermodulation Distortion — Fig. 105 shows the peak-to-peak input signal required to produce third-order intermodulation distortion of 3 per cent as a function of gain control

for the CA3002 integrated circuit. The maximum tolerable signal input for 3-per-cent intermodulation distortion is relatively constant over the entire agc range, but increases dramatically as cutoff is attained. When the CA3002 is operated in mode A with supplies of ±6 volts and an agc of −30 dB, a peak-to-peak input

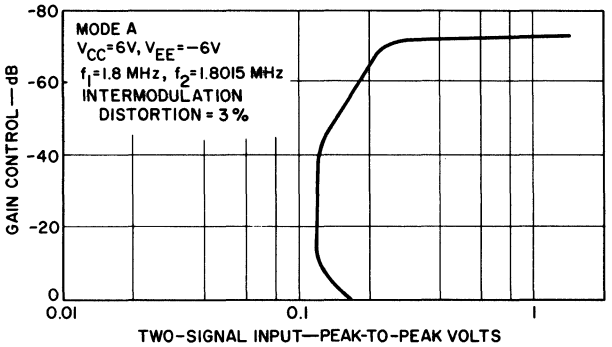


Fig. 105 — Third-order intermodulation-distortion characteristic as a function of agc.

signal in excess of 100 millivolts is typically required for 3-per-cent distortion.

Noise Figure — Because noise figure is an important design parameter for both video and if-amplifier applications, it was evaluated for the CA3002 over the frequency range of 1 kHz to 10 MHz. Fig. 106 shows noise performance as a function of frequency when a 1000-ohm source is used. The noise figure is 4 dB

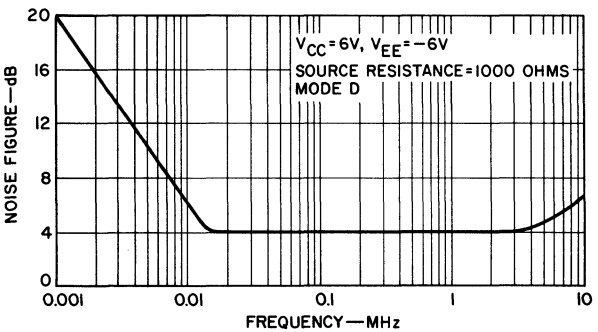


Fig. 106 — Noise figure of the CA3002 as a function of frequency.

over a large portion of the usable range. The 1/f noise corner occurs at approximately 45 kHz, and the high-frequency noise rise begins at approximately 4 MHz. Fig. 107 shows noise figure as a

function of source resistance at 1.75 MHz. The typical noise figure is less than 4 dB. It is reasonably flat for source resistances from 500 to 2500 ohms, but rises rapidly at values below 500 ohms.

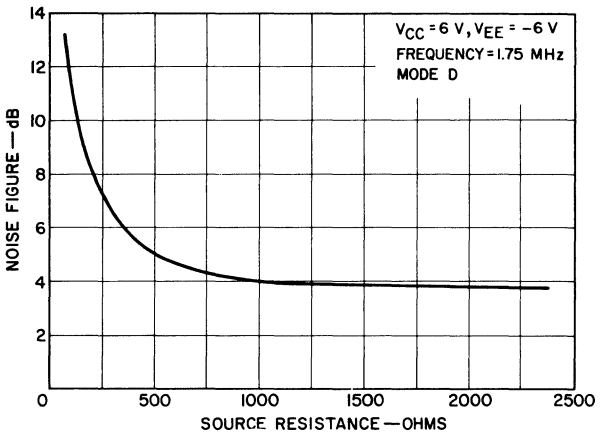


Fig. 107 — Noise figure of the CA3002 as a function of source resistance.

When external base-bias resistors are used, terminal 5 should be bypassed by an external capacitor for any stage in which low noise figure is required. If the base-bias resistors are not bypassed, the noise figure increases. In a practical receiver, bypassing may be avoided if the input at terminal 10 is transformer driven (from a filter) and terminal 5 is grounded. In the later if stages, noise figure can usually be ignored.

Applications of the IF Amplifier

The CA3002 integrated-circuit if amplifier is a versatile circuit that can be used for many diverse applications. The balanced differential amplifier fed from a constant-current source makes an excellent controlled-gain if amplifier. The gain-control function may be extended to include video gating, squelching, and blanking applications. Envelope detection can be achieved by suitable biasing of the emitter-base diode of the output emitter-follower transistor. Product detection can be obtained by re-insertion of the carrier at the base of the constant-current-source transistor. Various trigger and waveform-generating circuits can also be achieved by the addition of suitable external components.

Four-Stage 1.75-MHz IF Amplifier — Effective if design for AM circuits requires consideration of both the signal level at the input stage (as a function of agc range) and the acceptable signal-to-noise ratio at the output. The agc action must be initiated at the first stage at the proper voltage level to prevent excessive modulation distortion throughout the entire agc range. This input-signal voltage level is calculated to be approximately 25 millivolts rms for 100-per-cent modulation at an allowable distortion of 10 per cent. Before the applied signal reaches 25 millivolts, the first stage must be gain controlled and completely cut off before gain control is applied to subsequent stages.

Fig. 108 shows a four-stage 1.75-MHz amplifier used to evaluate the performance of the CA3002 amplifier for AM applications. A tuned circuit and a diode detector are connected to terminal 6 of the output stage to evaluate detected output and signal-to-noise ratio. The audio bandwidth of the detector output filter is 3 dB down at 4.2 kHz. The tuned circuit at the input is driven by a 50-ohm generator and provides a 1000-ohm source to the circuit. The first stage is operated at reduced supply voltages (about ± 3 volts) to reduce the required agc control voltage. This lower supply-voltage level ensures that a sufficient control voltage can be developed by a separate CA3002 unit used as an agc amplifier without introducing a separate supply voltage. An additional advantage of lower-voltage operation in the first stage is a reduction in noise figure.

If desired, the first-stage tuned circuit in Fig. 108 can be replaced by a crystal filter and a transformer. Because the CA3002 input impedance is high and does not vary appreciably with agc, no impedance variations are presented to the crystal filter.

The voltage gain realized from terminal 10 of the first stage to terminal 6 of the fourth stage is 85 dB, or approximately 21 dB per stage. From the 50-ohm input, the typical voltage gain is 98 dB. Because the maximum signal-handling capability of the output stage is slightly greater than 0.7 volt rms, gain control should begin when this value is measured at terminal 6. The modulation distortion is acceptable over the entire 60-dB agc range. For input signals greater than 8 millivolts, modulation distortion begins to increase because of fourth-stage overload. Overloading can be prevented by application of a delayed gain control to the second stage. The signal-to-noise performance as a function of input signal is shown in Fig. 109.

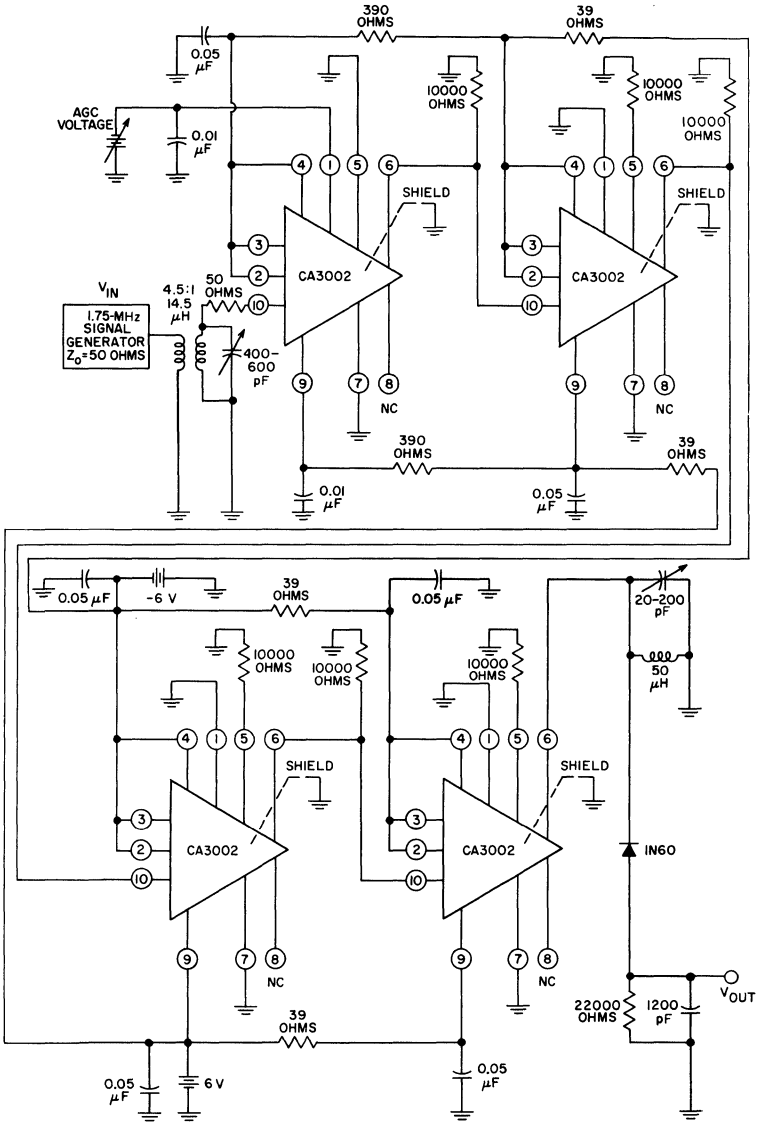


Fig. 108 — Four-stage 1.75-MHz if amplifier.

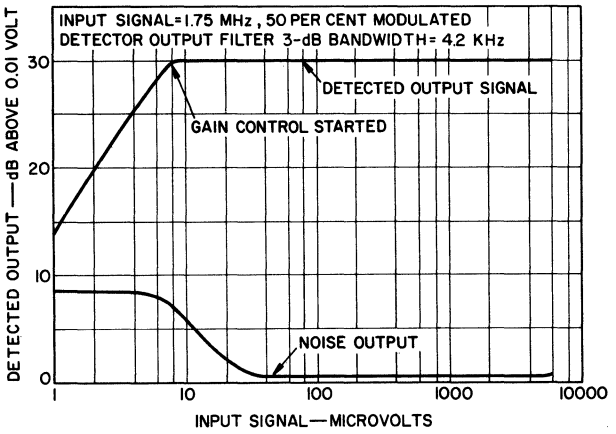


Fig. 109 — Output signal and noise of the amplifier shown in Fig. 108.

Envelope Detector — The CA3002 integrated circuit can be operated as an envelope detector in either of two ways, as shown in Fig. 110: (1) the emitter of the output transistor Q_6 can be operated at zero voltage by connection of an external resistor in the bias loop of the constant-current transistor Q_3, or (2) the current in transistor Q_6 can be reduced by connection of a large resistor (12,000 to 18,000 ohms) in series with its emitter resistor.

In the circuit for method 1, the current in the differential pair (Q_2 and Q_4 in Fig. 96) is increased to the point at which the common-collector output transistor Q_6 is biased almost to cutoff. For this current increase, the constant-current transistor Q_3 is operated with terminal 4 open, and the emitter resistor R_9 is shunt loaded by the external resistor at terminal 3. Envelope detection can be accomplished only in mode A with method 1.

Although the output transistor is nearly cut off, all the other active devices are operating in their linear regions. For small ac signals, therefore, the circuit provides linear operation except for Q_6, which is turned on only by a positive signal. The maximum acceptable input signal depends on the linear range of the differential amplifier. An external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

In the circuit diagram for method 2 shown in Fig. 110, a fixed value of resistance (15,000 ohms) is used to reduce the emitter current in the output transistor (Q_6) to approximately 100 microamperes. This operating point provides the non-linearity

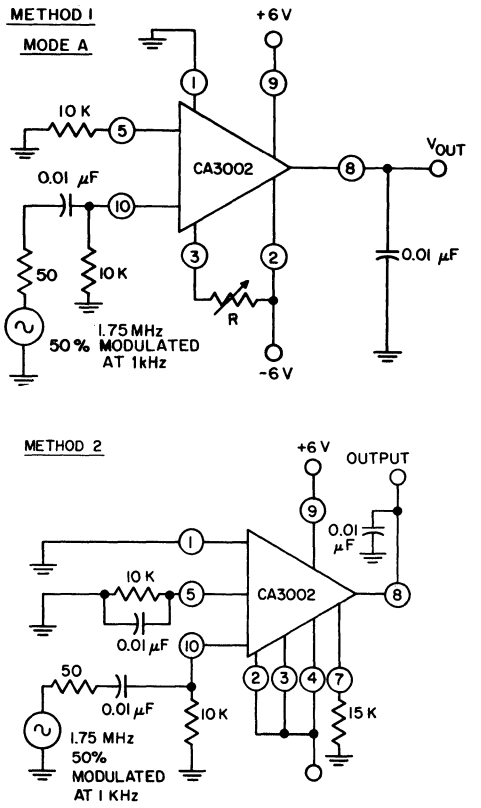


Fig. 110 — Envelope detectors using CA3002 integrated circuits.

for detection in transistor Q_6. Again, the remainder of the circuit produces gain because it is operating linearly. As in the case of method 1, an external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

Fig. 111 shows the input-output characteristics of the envelope-detector circuits shown in Fig. 110. The usable range of input signals for distortion below 3 per cent is 10 to 100 millivolts (20-dB range) for method 1 and 12 to 60 millivolts (14-dB range) for method 2. Automatic gain control of the if amplifier must maintain the input signals to the detector within this range.

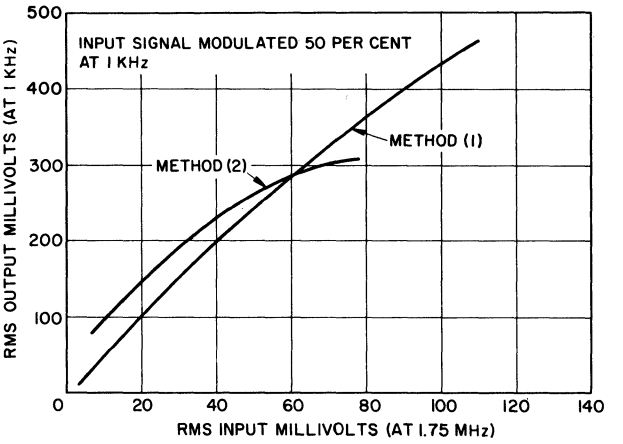


Fig. 111 — Input-output characteristics of the envelope detectors shown in Fig. 110.

Product Detector — A differential pair driven by a constant-current transistor can be used as a product detector if a suppressed-carrier signal is applied to the differential pair and the regenerated carrier is applied to the constant-current transistor. There are two requirements for linearity: (1) the circuit must be operated in a linear region, and (2) the current from the constant-current transistor must be linear with respect to the reinserted carrier voltage.

The CA3002 satisfies these requirements and can be used as a product detector in the circuit shown in Fig. 112. A double-sideband suppressed-carrier signal is applied at terminal 10, and

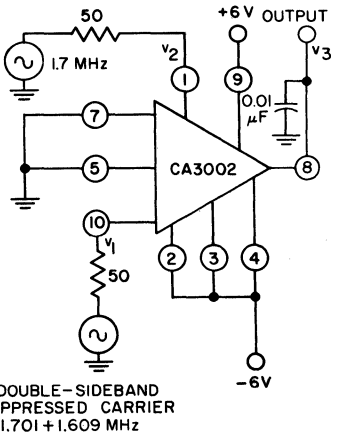


Fig. 112 — Product detector circuit.

the 1.7-MHz carrier is applied to terminal 1. Because of the single-ended output, a high-frequency bypass capacitor (0.01 microfarad) is connected between terminal 8 and ground to provide filtering for the high-frequency components of the oscillator signal at the output.

When the amplitude of the suppressed-carrier signal and of the oscillator signal are varied, the gain and distortion characteristics shown in Table XIV are obtained. The conversion voltage gain is constant at input signals up to 16 millivolts and would be 6 dB less for a single-sideband signal than for the double-sideband

Table XIV—*Performance Data for CA3002 as Product Detector*

V_1 Double-Sideband Voltage (mV)	V_2 Oscillator Voltage at Term. 1 (V)	V_3 Output at Term. 8 at 1 kHz (mV)	Conversion Voltage Gain (dB)	dB down from Fundamental of Harmonics *	
				Harmonic	
				2nd	3rd
1	1.7	12.5	21.9	60	>65
4	1.7	50	21.9	51	61
8	1.7	100	21.9	46	56
16	1.7	200	21.9	37	46
32	1.7	310	19.8	32	30▲
4	0.25	22	15.6	15	42▪
4	0.5	42	20.3	32	52
4	1.0	60	23.5	45	60
4	1.3	60	23.5	49	61
4	1.7	50	21.9	51	61
4	2.0	48	21.6	52	62
4	2.5	31	17.8	49	60
4	3.0	15	11.4	42	60

* 4th and 5th harmonics greater than 65 dB down except as noted.
▲ 4th harmonic 51 dB down, 5th harmonic 64 dB down.
▪ 4th harmonic 44 dB down.

signal. The distortion increases with increasing input signal; for distortion of less than 1 per cent, the input drive level does not exceed 8 millivolts. The gain maximizes for oscillator voltages of 1 to 2 volts, and the distortion characteristic is also best in this region. Distortion increases both at low oscillator drive levels (0.25 volt) and at high levels (3 volts).

Schmitt Trigger — Fig. 113 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5 and both the output and the feedback are taken from the output emitter-follower at terminal 8. The emitter-follower output isolates the feedback loop from the differential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither half of the differential pair saturates as the resistance of the feedback loop is varied. Fig. 113 also shows

the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.

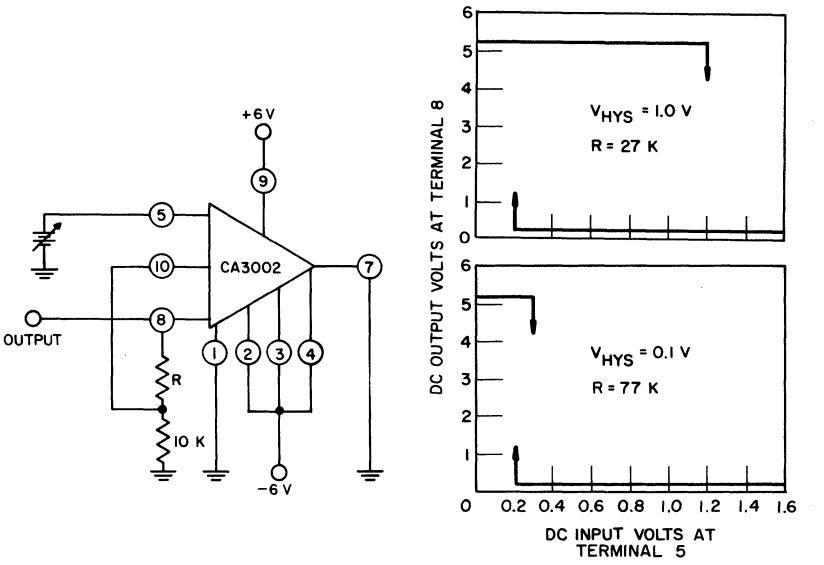


Fig. 113 — Schmitt trigger circuit and output swing and associated hysteresis.

INTEGRATED-CIRCUIT RF AMPLIFIERS

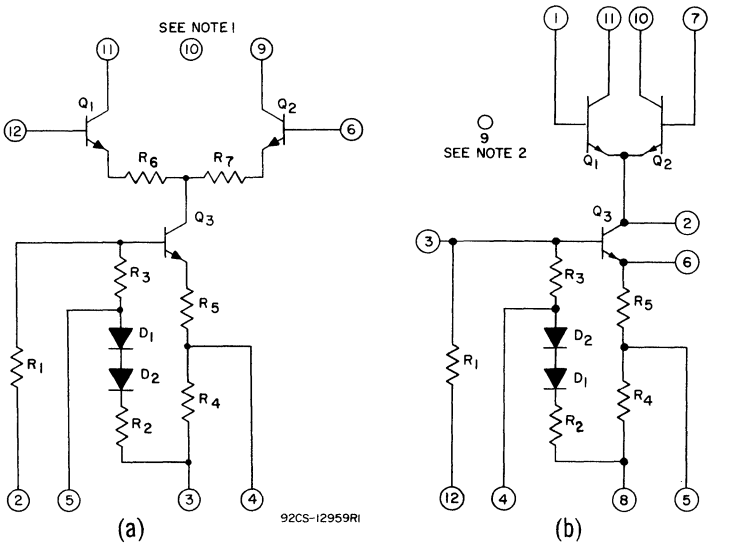
The RCA CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers are supplied in 12-terminal TO-5 style packages. These circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from −55°C to 125°C, at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide the following types of functions:

1. Wide- or narrow-band amplification
2. Mixing
3. Limiting
4. Product detection
5. Frequency generation
6. Generation of pulse or digital waveforms

Operating Requirements and Characteristics

Fig. 114 shows the schematic diagrams for the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. Each circuit

consists of a balanced differential amplifier that is driven from a controlled, constant-current source.



Notes: 1. Connect terminal 10 to most positive dc supply voltage.
2. Connect terminal 9 to most positive dc supply voltage.

Fig. 114 — Schematic diagrams of the integrated-circuit rf amplifiers: (a) CA3004; (b) CA3005 or CA3006.

In the CA3004 circuit, resistors (R_6 and R_7) are included in the emitter leads of the differential pair of transistors, Q_1 and Q_2. The degeneration introduced by these unbypassed emitter resistors improves the linearity of the transfer characteristics and increases the signal-handling capabilities of the circuit. Fig. 115 shows the dynamic transfer and limiting characteristics of the CA3004. The characteristics show that linear operation is possible over a wide range of differential input voltage and, thus, indicate that relatively large input signals can be handled by the circuit without limiting. These features indicate that the CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration.

In the CA3005 and CA3006 circuits, no emitter resistors are provided for the differential pair of transistors. As a result, these circuits have a smaller dynamic range and provide higher gain than the CA3004 circuit. The dynamic transfer and limiting characteristics of the CA3005 and CA3006, given in Fig. 116, show that these circuits are very good limiting amplifiers. A comparison

of the curves in Fig. 116 with those given for the CA3004 in Fig. 115 emphasizes the excellent limiting characteristics of the CA3005 and CA3006.

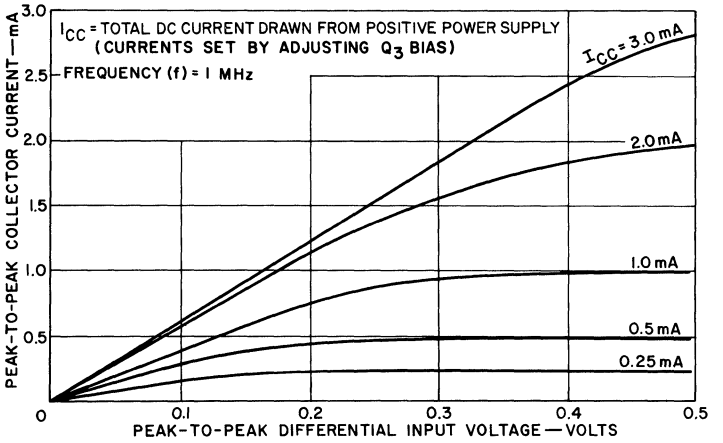


Fig. 115 — Dynamic transfer and limiting characteristics of the CA3004 integrated-circuit rf amplifier.

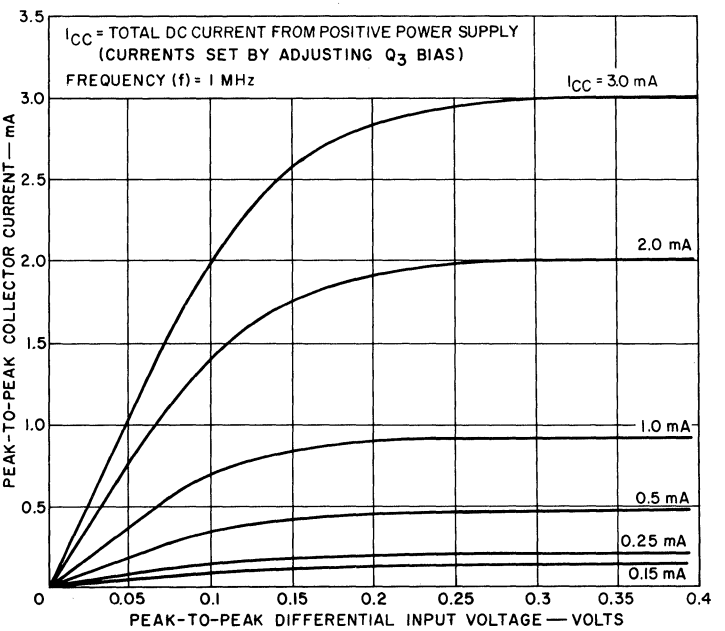


Fig. 116 — Dynamic transfer and limiting characteristics of the CA3005 or CA3006 integrated-circuit rf amplifier operated in the differential-amplifier configuration.

Exceptional versatility in the operation of the CA3005 and CA3006 is made possible by the availability of internal circuit points to which external circuit elements may be connected to alter the basic circuit configuration. As a result of such external modifications, it is possible to operate these circuits as push-pull amplifiers, as cascode amplifiers, or as single amplifiers in cascade or parallel channels.

The CA3005 and CA3006 rf amplifiers are identical except for their input offset voltages. The offset voltage for the CA3006 is typically less than 1 millivolt, while the offset voltage for the CA3005 is normally in the order of 3 millivolts. The low level of input offset voltage makes the CA3006 well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

Supply-Voltage Connections — The CA3004, CA3005, and CA3006 circuits may be operated, at various levels of supply voltage, from single or dual dc power supplies. For dual-supply operation, either symmetrical or nonsymmetrical power supplies may be used.

Fig. 117 shows the supply-voltage connections for differential- and cascode-amplifier operation of the CA3005 or CA3006 from single and dual supplies. When two supplies, one for positive voltage and one for negative voltage, are used, as shown in Fig. 117(a) and 117(c), fewer external components are required. When only one supply is used, an external resistive voltage divider and bypass capacitor must be added to the circuit, as shown in Figs. 117(b) and 117(d). Tuned amplifiers that operate from dual supplies, such as that shown in Fig. 117(a), require the least number of external components.

For either single- or dual-supply operation, the operating current of transistor Q_3 is determined by the bias voltage, V_{EE}, applied between terminals 2 and 3 on the CA3004 or between terminals 8 and 12 on the CA3005 and CA3006 (refer to the circuit diagrams in Fig. 114). The more negative terminal of the bias-voltage source must be connected to terminal 3 on the CA3004 or to terminal 8 on the CA3005 and CA3006. In dual-supply systems, terminal 2 of the CA3004 and terminal 12 of the CA3005 and CA3006 are usually returned to dc ground.

Operating Modes — For any given bias voltage V_{EE}, there are four possible operating modes for the integrated-circuit rf amplifiers. In general, each mode is characterized by (1) a distinct level of operating current and corresponding transconductance, (2) the

degree of dependence of the operating current on temperature, and (3) the way in which the transconductance is affected by temperature. The operating points for the various modes are established by:

1. The emitter resistance selected for the constant-current-source transistor, Q_3;
2. Whether the base-bias network includes the diodes shown in Fig. 114.
3. The magnitude of the bias voltage, V_{EE}, applied to the circuit.

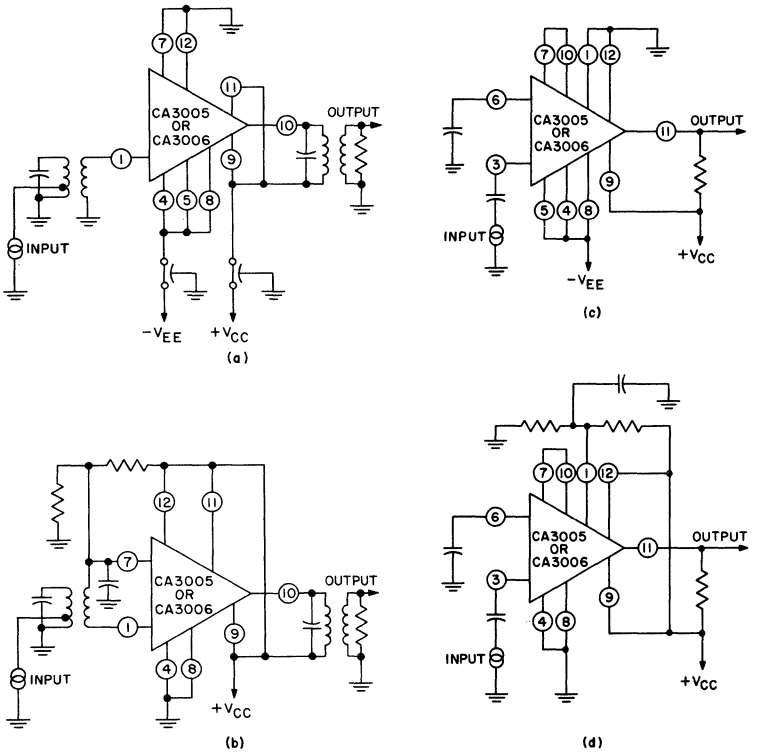


Fig. 117 — Supply-voltage connections for the CA3005 or CA3006 in (a) a differential-amplifier configuration operated from dual supplies, (b) a differential-amplifier configuration operated from a single supply, (c) a cascode configuration operated from dual supplies, and (d) a cascode configuration operated from a single supply.

Table XV lists the required conditions for the four operating modes. The following paragraphs describe the characteristics of

Table XV—*Required Conditions for Each Operating Mode of the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers*

Operating Mode*	CA3004 Terminals Shorted to Term. 3	CA3005 or CA3006 Terminals Shorted to Term. 8	Diodes In or Out of Bias Circuit	Q-3 Emitter Resistor(s)
A	—	—	In	$R_4 + R_5$
B	5	4	Out	$R_4 + R_5$
C	4	5	In	R_5
D	4,5	4,5	Out	R_5

* For all modes, terminals 2, 6, and 12 of the CA3004 and terminals 1, 7, and 12 of the CA3005 and CA3006 are grounded.

the circuits in each operating mode. The data are given for operation of the circuits from symmetrical dual power supplies at three levels of dc supply voltage (±3 volts, ±4.5 volts, and ±6 volts).

Fig. 118 shows the operating current for the various modes as a function of temperature. The current-temperature data show that, in addition to the obvious shift in the level of operating current, the dependence of the operating current on temperature varies significantly with a change in the operating mode.

When the diodes are included in the base-bias circuit (modes A and C), the operating current, which is primarily dependent on the temperature coefficient of the diffused emitter resistor tends to decrease with an increase in temperature at a rate that is relatively independent of the bias supply voltage V_{EE}. When the diodes are not used, however, the shape of the current-temperature curves is dependent on the magnitude of the supply voltage V_{EE}. The operating current then may remain constant or rise as the temperature is increased, depending upon the value of V_{EE}. The positive supply voltages, shown in Fig. 118, have no effect on the operating current, and the current-temperature curves are not changed by increases or decreases in this voltage. Some deviation in the current-temperature curves is to be expected because of normal variations in the absolute resistor values.

Fig. 119 shows the effects of different operating modes and variations in temperature on the single-ended transconductance* of

* The single-ended transconductance is the incremental output current for one collector of the differential pair of transistors divided by the incremental input voltage. The curves shown of this parameter are obtained at an operating frequency of 1 MHz.

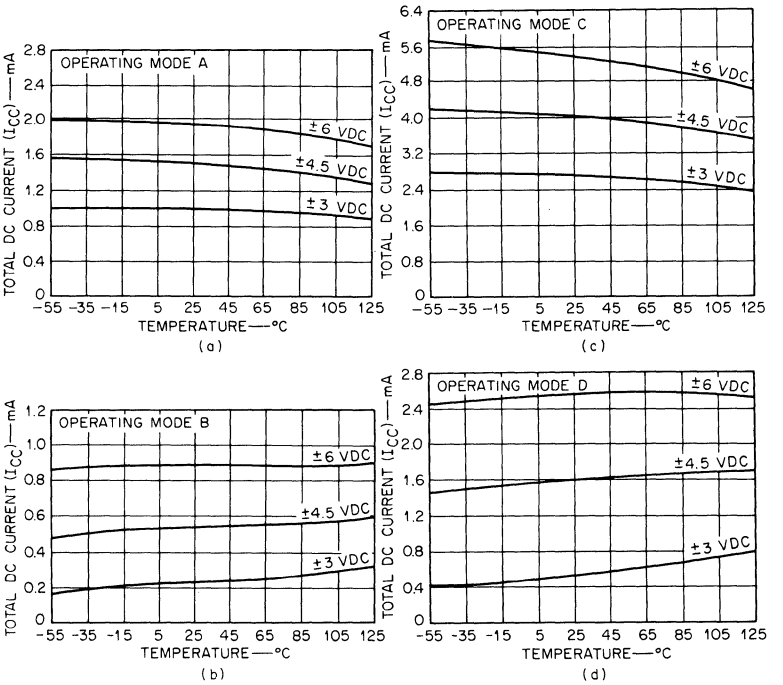


Fig. 118 — Variation in the operating currents of the CA3004, CA3005, or CA3006 as a function of temperature for each operating mode.

the CA3004. In general, when diodes are used in the base-bias network, the transconductance decreases with increases in temperature. If the diodes are not used, the transconductance may decrease, increase, or remain constant as the temperature increases, depending on the value of the negative supply voltage V_{EE}. With the diodes out, however, the collector operating point tends to shift when resistive loads are used. In applications that require a stable collector dc operating point, therefore, operating mode A or C (diodes in) should be used.

Fig. 120 shows transconductance-temperature curves for each operating mode of the CA3005 or CA3006, operated in a differential-amplifier configuration. These transconductance curves differ from those for the CA3004 shown in Fig. 119 primarily because of the emitter resistors used in the CA3004. For each operating mode, the operating points for the differential-amplifier configuration of the CA3005 or CA3006, as well as for the CA3004, pro-

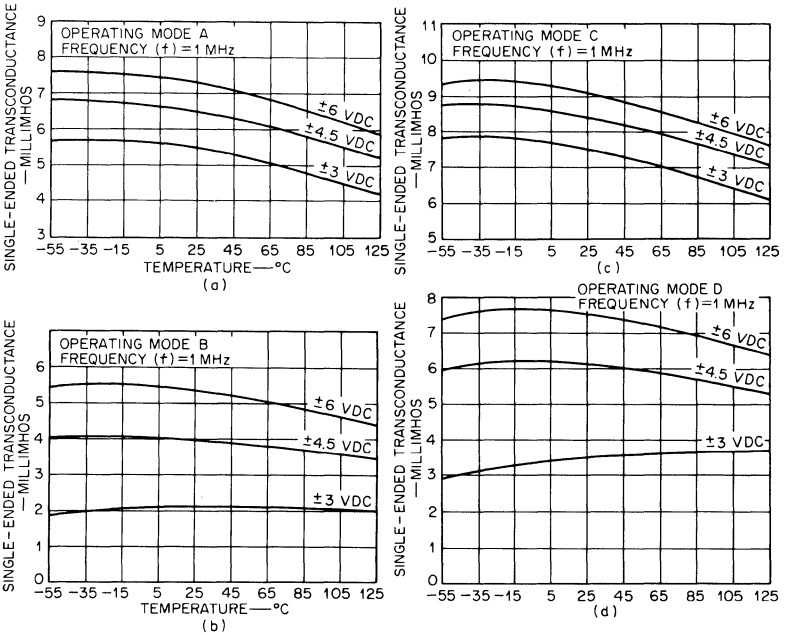


Fig. 119 — Variation in the single-ended transconductance of the CA3004 as a function of temperature for each operating mode.

vide a current in each collector of the differential pair of transistors that is equal to one-half that shown in Fig. 118.

In a cascode configuration of the CA3005 or CA3006, the current through each part of the common emitter-common base cascode is equal to the total current shown in Fig. 118 in each mode. Fig. 121 shows the transconductance-temperature curves for each operating mode of the cascode circuit. These curves show that, in general, the transconductance is higher when the diodes are included in the base-bias network (modes A and C) than it is when the diodes are not used (modes B and D).

The power dissipation of the CA3004, CA3005, or CA3006 is highest when the circuit is operated in mode C. Table XVI shows power dissipation and the single-ended transconductance of the circuits for each operating mode. These data may be used to determine the operating point that provides the highest value of transconductance per milliwatt of circuit dissipation for given design conditions.

Admittance Parameters — In the design of rf and if circuits, the four-terminal blackbox short-circuit admittance parameters

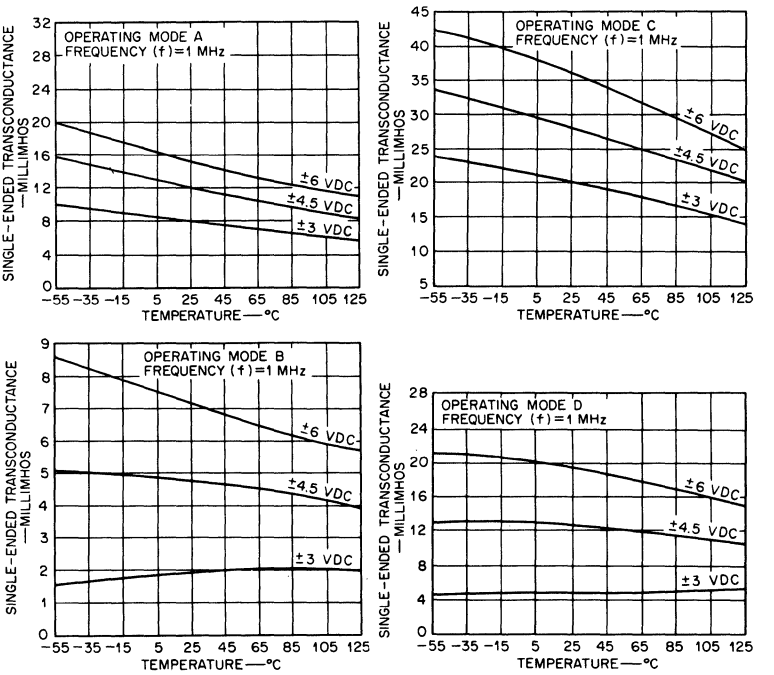


Fig. 120 — Variation in the single-ended transconductance of the CA3005 or CA3006 in a differential-amplifier configuration as a function of temperature for each operating mode.

have become a valuable tool. The determination of stability criteria, input and output impedances as a function of load and source admittance, power gain, and voltage gain in iterative connections are all facilitated by a knowledge of the "y" parameters.

The "y" parameter curves presented in this section have been calculated from a model and verified at several points by measurements. These curves are a valuable aid in the design of systems that use integrated circuits. The admittance curves are all generated for a quiescent operating current of 1.25 milliamperes in each of the transistors Q_1 and Q_2 in the differential-amplifier configurations and for a current of 2.5 milliamperes in transistor Q_3 in the cascode configuration. This operating current is obtained in operating mode D with supply voltages of ±6 volts.

The "y" parameters and their symbols are listed below:

1. Input admittance with the output voltage constant

$$y_i = g_i + jb_i \tag{181}$$

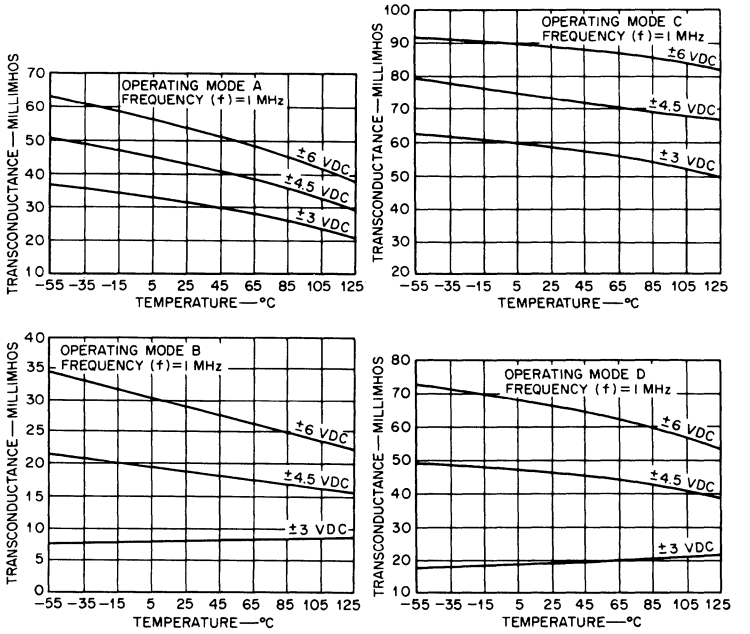


Fig. 121 — Variation in the transconductance of the CA3005 or CA3006 in a cascode configuration as a function of temperature for each operating mode.

where y_i is the complex input admittance, g_i is the input conductance and b_i is the input susceptance.

2. Output admittance with the input voltage constant

$$y_o = g_o + jb_o \tag{182}$$

where y_o is the complex output admittance, g_o is the output conductance, and b_o is the output susceptance.

3. Forward-transfer admittance with the output voltage constant

$$y_f = g_f + jb_f \tag{183}$$

where y_f is the complex forward-transfer admittance, g_f is the forward-transfer conductance, and b_f is the forward-transfer susceptance.

4. Reverse-transfer admittance with the input voltage constant

$$y_r = g_r + jb_r \tag{184}$$

Table XVI—*Relationship Between the Transconductance and the Power Dissipation of the Integrated-Circuit RF Amplifiers in Each Operating Mode**

Operating Mode	Type of Circuit	DC Supply Voltages (volts)	Single-Ended Transconductance (millimhos)	Power Dissipation (milliwatts)
A	CA3004	±3	5.5	6.6
	CA3005 or CA3006		8.5	6.6
	CA3004	±4.5	6.7	15.0
	CA3005 or CA3006		12.8	15.0
	CA3004	±6	7.3	25.0
	CA3005 or CA3006		15.0	25.0
B	CA3004	±3	1.6	2.3
	CA3005 or CA3006		1.9	2.3
	CA3004	±4.5	4.0	7.2
	CA3005 or CA3006		4.9	7.2
	CA3004	±6	5.3	15.0
	CA3005 or CA3006		7.2	15.0
C	CA3004	±3	7.5	17.5
	CA3005 or CA3006		22.0	17.5
	CA3004	±4.5	8.5	40.0
	CA3005 or CA3006		29.0	40.0
	CA3004	±6	9.1	62.8
	CA3005 or CA3006		37.0	62.8
D	CA3004	±3	3.3	4.2
	CA3005 or CA3006		5.0	4.2
	CA3004	±4.5	6.0	17.4
	CA3005 or CA3006		13.0	17.4
	CA3004	±6	7.2	35.9
	CA3005 or CA3006		20.0	35.9

* Circuits are operated in differential-amplifier configurations. The transconductances and power dissipations shown are calculated values for nominal units.

where y_r is the complex reverse-transfer admittance, g_r is the reverse-transfer conductance, and b_r is the reverse-transfer susceptance.

A comparison of the parameters of the various possible circuit configurations with those of the more familiar common-emitter parameters requires a second subscript to indicate the type of configuration being considered. Examples of the use of the second-subscript notation are given below:

The common-emitter reverse-transfer admittance is written as

$$y_{re} = g_{re} + jb_{re} \tag{185}$$

The differential-amplifier reverse-transfer admittance is expressed as

$$y_{rDA} = g_{rDA} + jb_{rDA} \tag{186}$$

The cascode-amplifier reverse-transfer admittance is given as

$$y_{rCAS} = g_{rCAS} + jb_{rCAS} \tag{187}$$

These cumbersome second subscripts will not be used when the type of circuit for which the parameter is given is clearly indicated by an illustration or a descriptive phrase in the text.

In general, it is valuable to understand the essential differences between the "y" parameters of a regular common-emitter stage and those of the compound stages, such as differential and cascode amplifiers.

The differential amplifier, when used at radio frequencies, consists essentially of a common-collector stage that drives a common-base stage. In comparison to the regular, common-emitter "y" parameters, the input admittance y_i, the output admittance y_o, and the forward transfer admittance y_f are decreased, almost exactly, by a factor of two when the differential-amplifier configuration is used.

The reverse-transfer admittance y_r is also less for the differential amplifier than for the single transistor in the common-emitter configuration. The ratio of the imaginary term in the differential-amplifier admittance to that of the single transistor is 1/140 at low frequencies and 1/10 at 100 MHz. Fig. 122 shows the ratios of imaginary parts b_{re}/b_{rDA} and real parts g_{re}/g_{rDA} of the reverse-transfer admittances as a function of frequency.

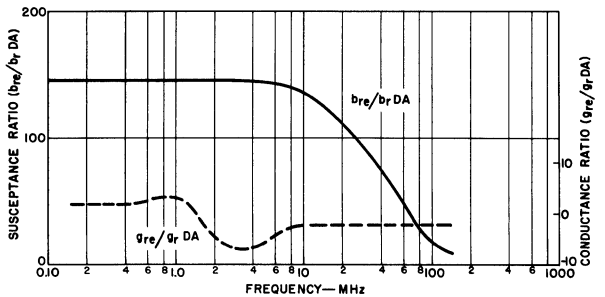


Fig. 122 — Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a differential-amplifier stage as a function of frequency.

In the cascode configuration of the rf amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_i is, therefore, that of a common-emitter stage. The forward-transfer admittance y_f is that of a common-emitter stage times alpha. Because of the high-impedance drive source on the common-base stage, the output admittance y_o is very low (0.06×10^{-5} mho) at low frequencies and is both negative and low at high frequencies. Since the output admittance is low and may be

negative, a conjugate match cannot be obtained at the output. Practical amplifiers are possible, however, provided that the sum $Y_{out} + Y_{load}$ is positive.

The reverse-transfer admittance y_r for the cascode circuit is less than that for the single-stage common-emitter circuit. The ratio of the imaginary terms of these admittances is 1/1200 at low frequencies and 1/35 at 100 MHz. The ratios of the real parts and of the imaginary parts as a function of frequency are shown in Fig. 123.

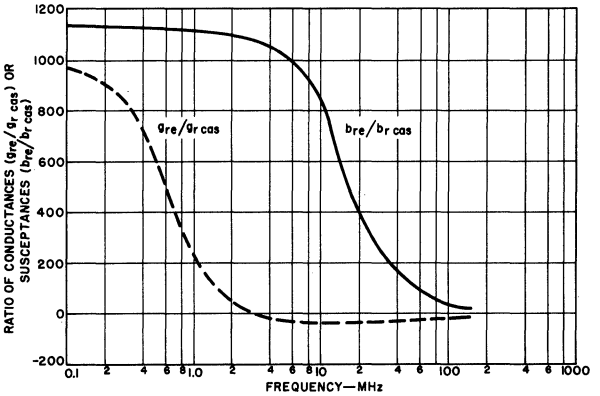


Fig. 123 — Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a cascode stage as a function of frequency.

Although the y_r is low for both the differential and cascode configurations, instability can occur in high-gain amplifiers. A further consideration in high-gain circuits is that the layout can contribute more feedback than the integrated circuit. Shielding and layout therefore are of prime importance if proper advantage is to be taken of the low feedback of these circuits.

The computed y parameters for the CA3004 differential amplifier are shown in Fig. 124. The admittance parameters for differential-amplifier operation of the CA3005 or CA3006 are given in Fig. 125 and those for cascode-amplifier operation of either circuit are given in Fig. 126.

Noise Figure — The noise figure of the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers is a function of the dc operating current and frequency, for both differential and cascode-amplifier configurations. The noise figure increases both with an increase in current and with an increase in frequency. For convenience, noise data are taken in a fixed configuration as the negative supply voltage is varied. On the data plots, the operating

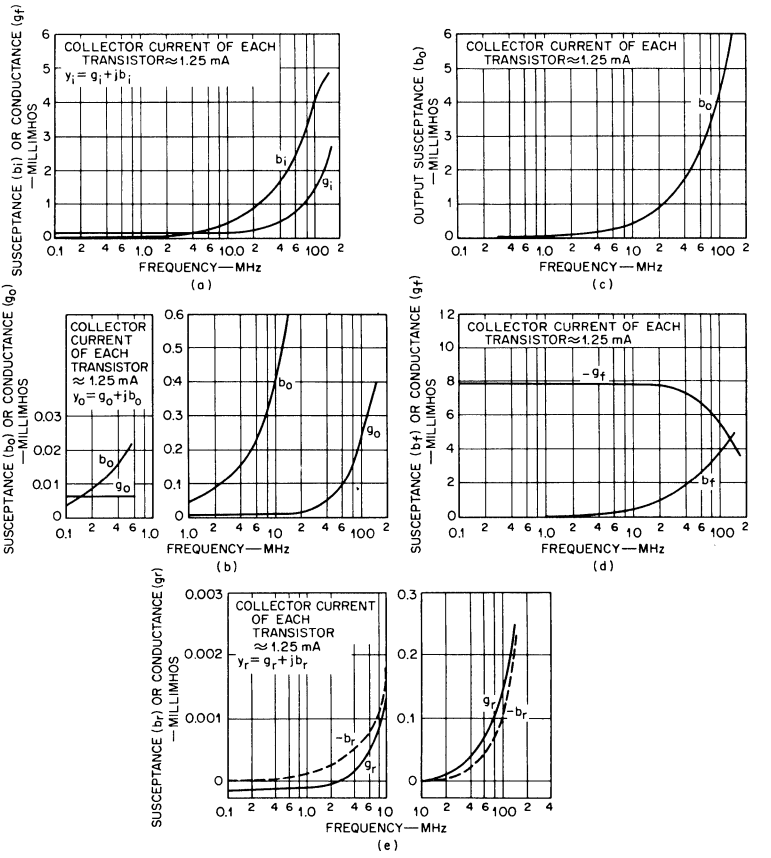


Fig. 124 — Admittance characteristics of a CA3004 differential amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, y_o; (c) Output susceptance, b_o, above 10 MHz; (d) Forward-transfer admittance, y_f; (e) Reverse transfer admittance, y_r.

currents that correspond to the various supply voltages are included as a separate abscissa to show that the noise figure is a direct function of operating current. Figs. 127 and 128 show representative noise-figure data for tuned amplifiers in the differential and cascode configuration, respectively. In each case, the input and output are tuned, and the input is conjugately matched to a 50-ohm noise diode. Practically no change in noise figure occurs with variations of the positive supply voltage V_{CC}.

The curves in Figs. 127 and 128 show that, for optimum single-stage noise performance, the operating current should be

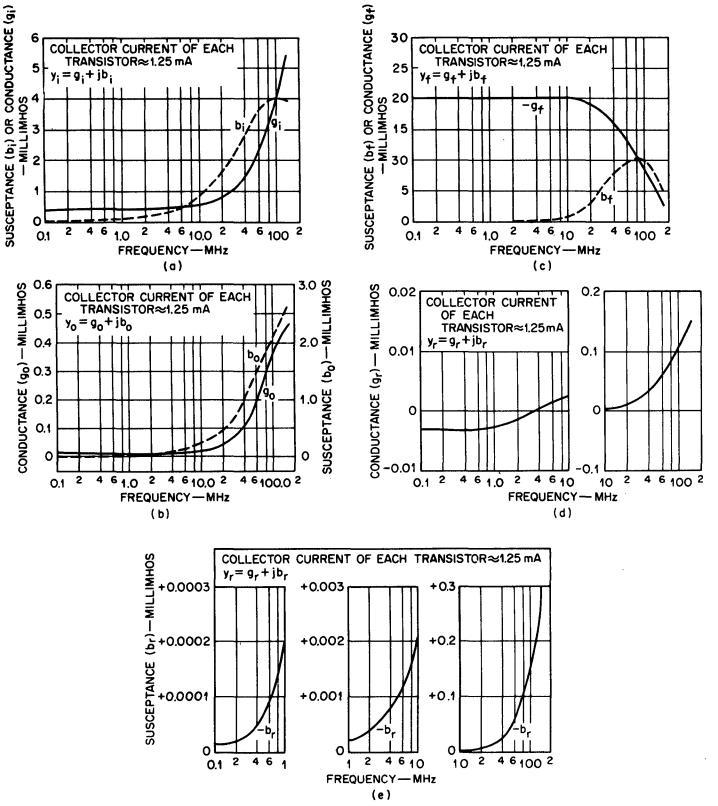


Fig. 125 — Admittance characteristics of a CA3005 or CA3006 differential amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, Y_o; (c) Forward transfer admittance, Y_f; (d) Reverse transfer conductance, g_r; (e) Reverse transfer susceptance, b_r.

low, which results in a low gain. Thus, in system applications of the tuned amplifiers, the operating current in each stage should be adjusted to obtain the optimum over-all noise figure by considering the gain and noise figure of the first stage and the noise figure of the second stage. The operating-current adjustment can be accomplished by a change in the negative-supply voltage (V_{EE}) or by means of the bias connections that are available.

Fig. 129 shows the noise figure as a function of the source resistance for a CA3005 or CA3006 used as a differential amplifier at an operating frequency of 12 MHz. The equation given in the figure can be used to predict noise performance as a function of source resistance for dc operating conditions. The load resistor

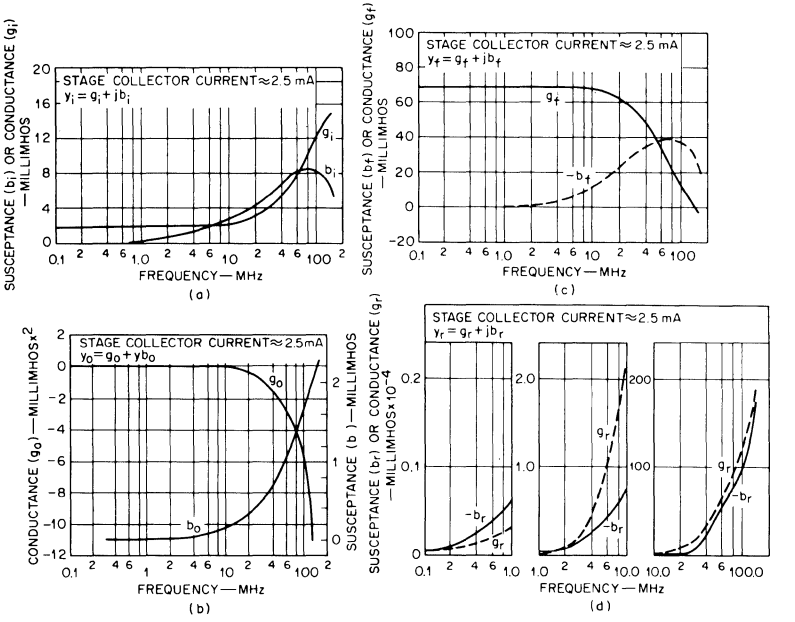


Fig. 126 — Admittance characteristics of a CA3005 or CA3006 cascode amplifier as a function of frequency: (a) Input admittance, y_i; (b) Output admittance, y_o; (c) Forward transfer admittance, y_f; (d) Reverse transfer admittance, y_r.

R_L of the circuit is 2200 ohms and R_N = 800 ohms. (R_N is the equivalent noise resistance.)

Common-Mode Rejection Ratio — The common-mode rejection ratio (the ratio between the full differential gain and the common-mode gain) is a function of the ratio of the impedance of the constant-current transistor Q_3 to the load resistor. The common-mode rejection decreases if the signal applied is large enough to saturate the constant-current transistor. The maximum peak-to-peak input voltage, therefore, is a function of the supply voltages and the bias connections of the constant-current transistor. The common-mode rejection ratio for a 1-kHz signal is shown in Table XVII.

Fig. 130 shows the single-ended common-mode gain* for the CA3004, CA3005, and CA3006 as a function of frequency. (Fig.

* Single-ended common-mode gain: The ratio of the change in the single-ended output voltage, measured from either output terminal with respect to ground, to the change in the input voltage applied simultaneously to both inputs of the circuit, i.e., single-ended common-mode gain = $\triangle V_{in}/\triangle V_{out}$, as shown in Fig. 131.

131 shows the method used to determine the single-ended common-mode gain.) The common-mode rejection decreases with increasing frequency when the CA3004, CA3005, and CA3006 are operated with a single-ended output.

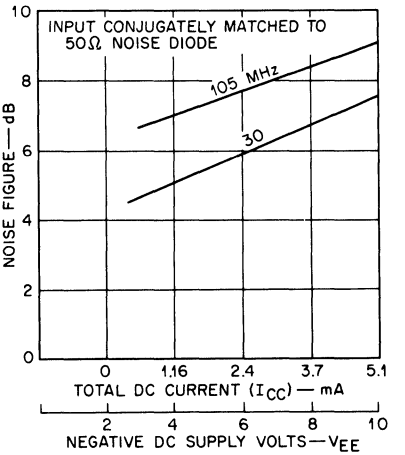


Fig. 127 — Representative noise performance of the CA3004, CA3005, or CA3006 operated in a differential-amplifier configuration (operating mode D).

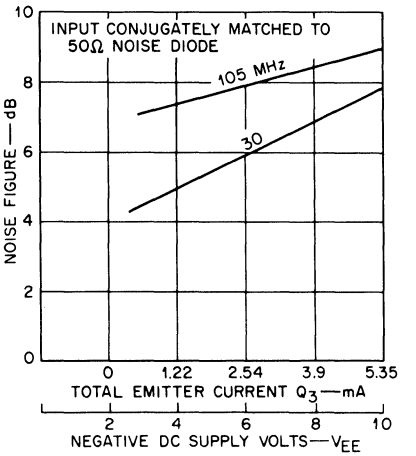


Fig. 128 — Representative noise performance of the CA3005 or CA3006 operated in a cascode-amplifier configuration (operating mode D).

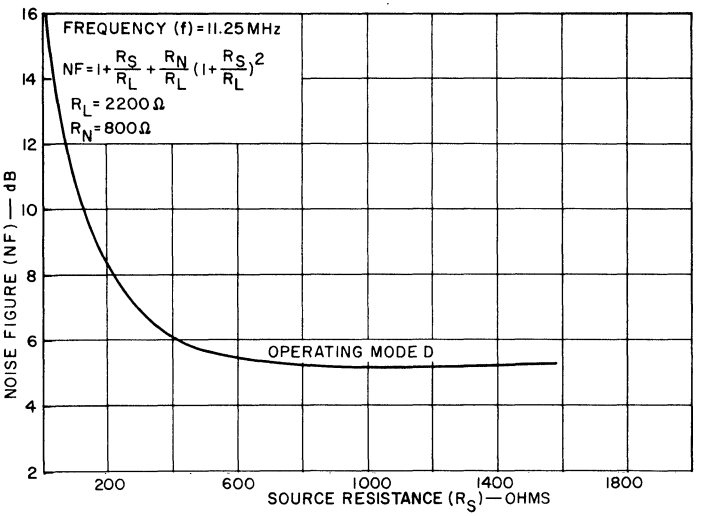


Fig. 129 — Noise figure of the CA3005 or CA3006 in a differential-amplifier configuration as a function of the source resistance (operating mode D).

Table XVII—*Common-Mode Rejection Ratio for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers*

	At —55°C	At 25°C	At 125°C
CA3004	102 dB	98 dB	101 dB
CA3005 or CA3006	108 dB	101 dB	107 dB

Operating frequency = 1 kHz
Load resistance R_L = 1000 ohms in each collector.

Gain Control — The gain of the CA3004, CA3005, and CA3006 circuits may be controlled in either of two ways: (1) the negative voltage applied to the base-bias resistor R_1 can be adjusted to vary the current in transistor Q_3, or (2) a differential offset voltage can be applied to transistors Q_1 and Q_2. In both techniques, the gain-control voltage has a ground reference in a two-supply system, and maximum gain is obtained at zero volts. The first method provides greater gain-control range but also requires more control voltage than the second method. Figs. 132 and 133 show the typical gain control as a function of voltage for the CA3005 or CA3006 for the two methods. Fig. 131 gives the gain-control characteristic for the CA3005 or CA3006 when the gain-control voltage is applied to the base-bias network of transistor Q_3. Since the Q_3 bias networks are the same, the gain characteristics for the CA3004 are nearly the same as those for the

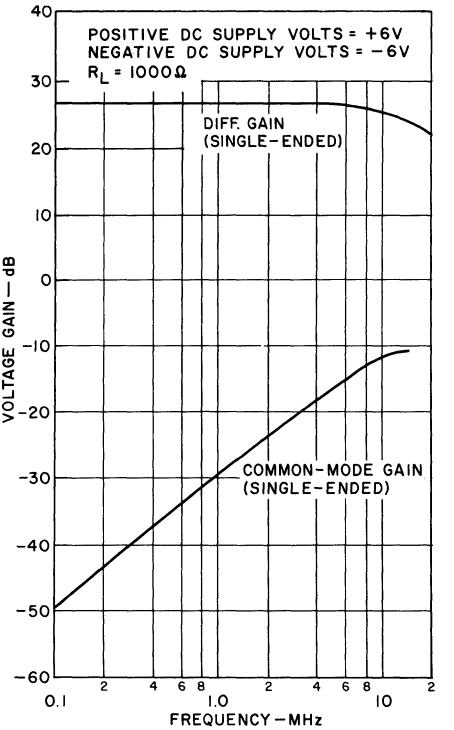


Fig. 130 — Single-ended common-mode and differential gains of the CA3004, CA3005, or CA3006 as a function of frequency.

CA3005 and CA3006. Fig. 133 shows that in the offset method of gain control the gain range is dependent on the polarity of drive. For maximum gain-control range on a single-ended amplifier, the common-collector transistor should be cut off (negative voltage applied to its base). Because of the emitter resistors, R_6 and R_7, the CA3004 circuit will require more dc voltage for the same gain reduction as the CA3005 or CA3006, and the dc voltage required will be a function of the initial operating current.

The maximum gain-control range that can be provided by a reduction in the current of transistor Q_3 varies with frequency as shown in Fig. 134. The maximum gain-control range that can be obtained is dependent on the full gain used, the circuit loading, and the external-circuit layout.

A large part of the variation in the maximum gain control for the different circuits results from differences in the initial gain

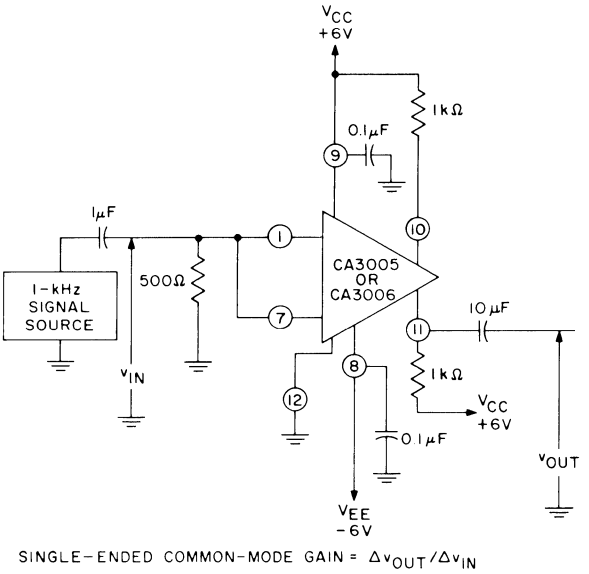


Fig. 131 — Schematic of the circuit used to determine the single-ended common-mode gain.

of the various circuits. Capacitive feedthrough appears less for the cascode than for the differential-amplifier configuration.

The following discussion of cross-modulation and modulation distortion describes variations of the two gain-control techniques.

Cross-Modulation and Modulation Distortion — Cross-modulation and modulation distortion are important considerations in the selection of an amplifier for use in AM systems. Cross-modulation distortion refers to the transfer of modulation from an undesired carrier to the desired carrier by nonlinearities in the amplifier. Modulation distortion is a change in the modulation on the desired carrier caused by the same amplifier nonlinearities that produce cross-modulation. The two forms of distortion are related by the following equation:

$$\frac{D_2}{V_1^2} : \frac{K}{V_2^2} = \frac{3}{8} \text{ m} : 1 \qquad (188)$$

where D_2 is the per cent of distortion in the modulation on the desired carrier (i.e., the modulation distortion), K is the per cent of cross-modulation distortion, V_1 is the amplitude of the desired-carrier voltage at the input, V_2 is the amplitude of the undesired-carrier voltage at the input, and m is the per cent of modulation of the desired carrier.

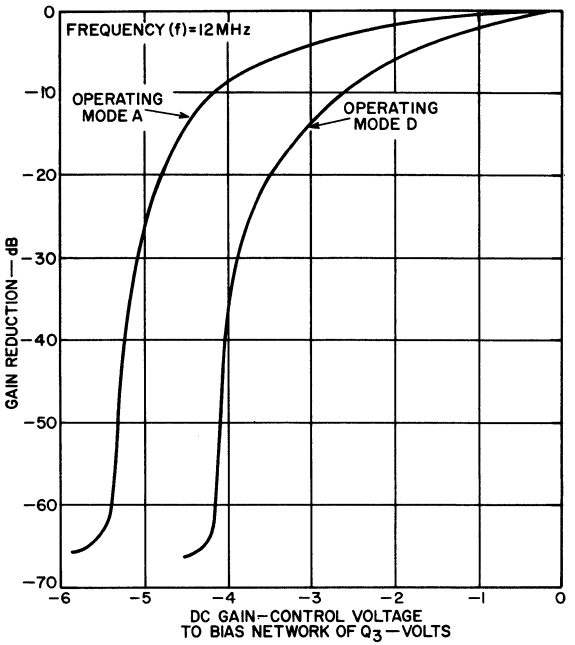


Fig. 132 — Gain-control characteristics of the CA3005 or CA3006 as a function of the dc gain-control voltage applied to the bias network of transistor Q_3.

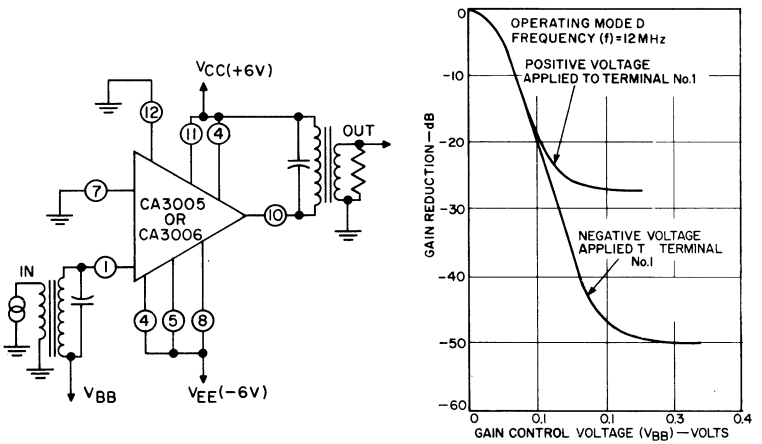


Fig. 133 — Gain-control characteristics of the CA3005 or CA3006 as a function of the dc offset voltage, V_{BB}, applied to the differential pair of transistors Q_1 and Q_2.

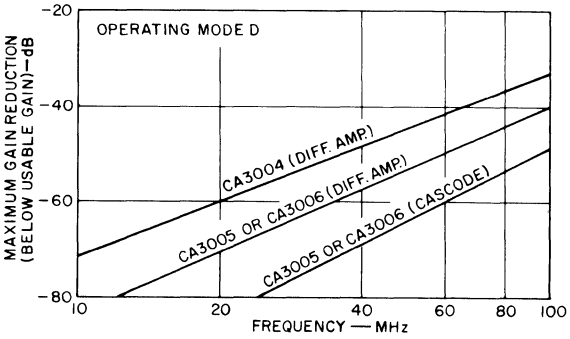


Fig. 134 — Maximum gain control provided by variations in the current through transistor Q_3 as a function of frequency.

When D_2 and K are equal and m is 100 per cent, the ratio of V_1 to V_2 is 1.64. In the following paragraphs, data are given for only the cross-modulation distortion. The modulation distortion can be predicted from these data, however, on the basis of the relationship of V_1 to V_2. For example, in Fig. 135, V_2 is given as 22 millivolts for a gain of 0 dB. The value of V_1, then, is 1.64 × 22, or 36 millivolts.

Figs. 135 through 139 show the cross-modulation distortion of the CA3004, CA3005, and CA3006 integrated circuits as a function of their gain-control characteristics in both differential-amplifier and cascode-amplifier configurations. The amount of cross-modulation distortion is determined by the two-generator method with the input of the circuit under test driven from a 50-ohm source and with its output tuned to the frequency of the desired carrier. The amplitude of the undesired-carrier input voltage is that necessary to produce 10 per cent cross-modulation distortion for each manually determined gain-control setting.

Differential-Amplifier Configurations — The availability of internal connection points make possible several methods of gain control in differential-amplifier configurations of the CA3004, CA3005, and CA3006 circuits. Only two of these methods need be considered, however, to obtain an adequate evaluation of the cross-modulation characteristics. These include (1) the variation of the current in the constant-current transistor, Q_3, and (2) the use of an offset voltage to produce an unbalance in the differential pair of transistors, Q_1 and Q_2.

Fig. 135 shows the cross-modulation distortion characteristics of the CA3004, CA3005, and CA3006 with the differential pair of transistors balanced and with agc applied to the constant-current transistor. Because of the increased linearity that results

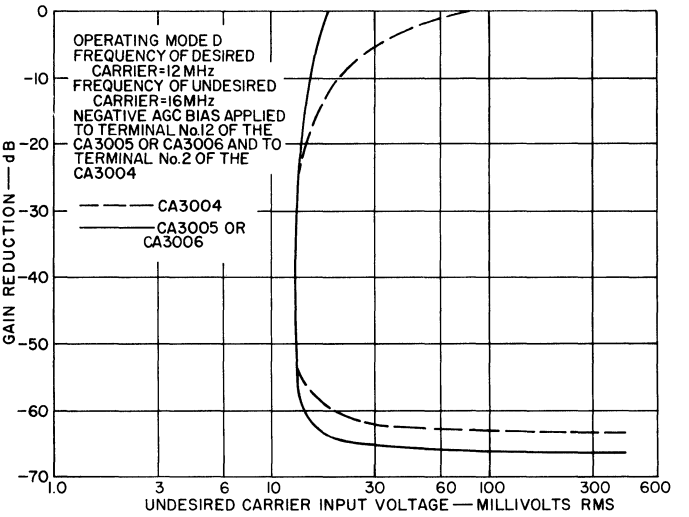
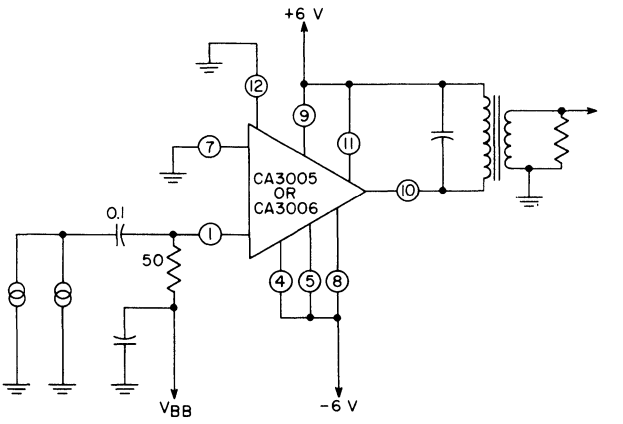


Fig. 135 — Gain control as a function of the input voltage from an undesired carrier that will produce cross-modulation distortion of 10 per cent for balanced differential-amplifier operation of the CA3004, CA3005 and CA3006. The gain-control voltage is applied to bias network of the constant-current transistor, Q_3.

from the emitter resistors R_6 and R_7, the CA3004 has improved cross-modulation characteristics at high current. The interfering signal voltage required to produce 10 per cent of cross-modulation distortion is practically a constant over the entire agc range for the CA3005 and CA3006. The value of the interfering-signal voltage (approximately 15 millivolts) for the CA3005 and CA3006 is twice that calculated from the logarithmic transconductance characteristic of a single transistor.

Fig. 136 shows the cross-modulation distortion characteristic of the CA3005 and CA3006 when an offset voltage is applied to control the gain. The improved cross-modulation performance at −5 dB gain is coincident with an inflection point on the curve of transconductance as a function of input offset voltage. This point occurs at an offset voltage of approximately 50 millivolts.



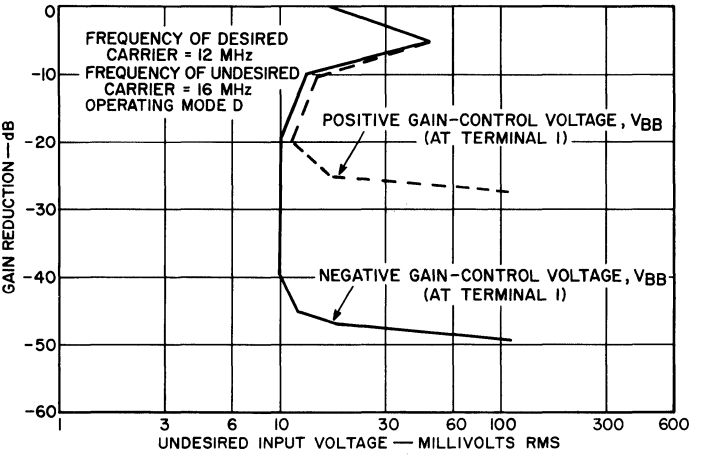


Fig. 136 — Gain control as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion for differential-amplifier operation of the CA3005 or CA3006 when gain control is provided by the application of an offset voltage to the differential pair of transistors.

The cross-modulation performance is improved by the offset of the differential pair of transistors. Fig. 137 shows the cross-modulation data when an initial offset of 50 millivolts is employed and agc is applied to the constant-current transistor. The introduction of the unbalance reduces the cross-modulation distortion to approximately 10 dB less than that of the balanced circuit. This reduction in cross-modulation distortion, however, is accompanied by a decrease in gain of approximately 5 dB.

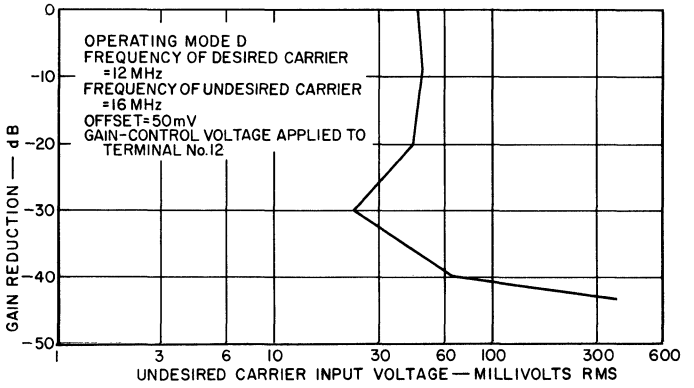


Fig. 137 — Gain control as a function of the input voltage from an undesired carrier that will produce cross modulation distortion of 10 per cent for a differential-amplifier configuration of the CA3005 or CA3006 having a 50-millivolt offset and with the gain control voltage applied to the bias network of the constant-current transistor.

Cascode Configurations — Cross-modulation data for cascode configurations of the integrated-circuit rf amplifiers are given for only the CA3005 and CA3006 circuits, because the CA3004 circuit is not designed for this type of operation. When the CA3005 or CA3006 is operated in the cascode configuration, gain control may be provided by either of two methods: (1) a negative voltage may be applied to the base of transistor Q_3, or (2) a negative voltage may be applied to the base of transistor Q_1.

In the first method, the gain is reduced by the application of a negative-going voltage at terminal 12. As the amplitude of this voltage is increased to the value required to cut off transistor Q_3, the gain of the circuit is decreased. The cross-modulation distortion characteristics for this type of gain control are shown in Fig. 138. The cross-modulation characteristics are comparable to those of a single transistor having a bypassed emitter resistor.

The cross-modulation distortion characteristics obtained for the second method of gain control are shown in Fig. 139. No improvement in cross-modulation characteristics over those obtained for the first gain-control method are observed, although the agc range is greater.

Limiter Characteristics — The following paragraphs describe the limiter characteristics of the integrated-circuit rf amplifiers in both differential-amplifier and cascode configurations.

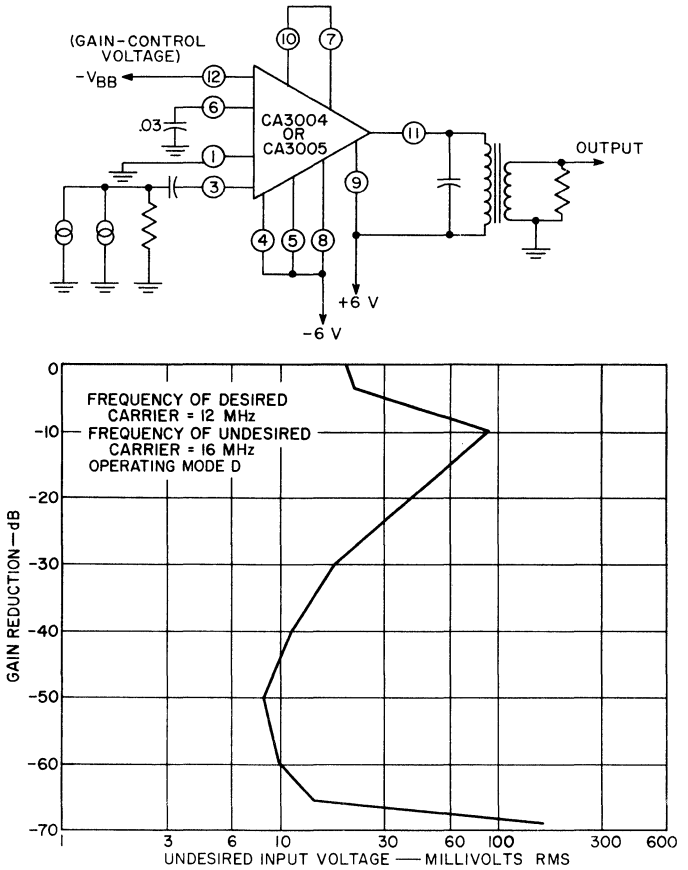


Fig. 138 — Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor Q_3. The schematic diagram illustrates the circuit configuration.

Differential-Amplifier Configurations — The differential-amplifier, driven by a constant-current transistor, is probably the optimum circuit configuration for bipolar transistor limiters. The advantage of such circuits in limiter applications is that collector saturation of either transistor Q_1 or Q_2 can be avoided because of the action of the constant-current transistor Q_3. Figs. 115 and 116 show typical limiting characteristics for the CA3004 and for the CA3005 and CA3006 respectively. For the CA3005 and CA3006 (no emitter degeneration), "hard" limiting is achieved for a peak-to-peak input of 300 millivolts for all values of total dc current (I_{CC}). For the CA3004, the input voltage required for "hard"

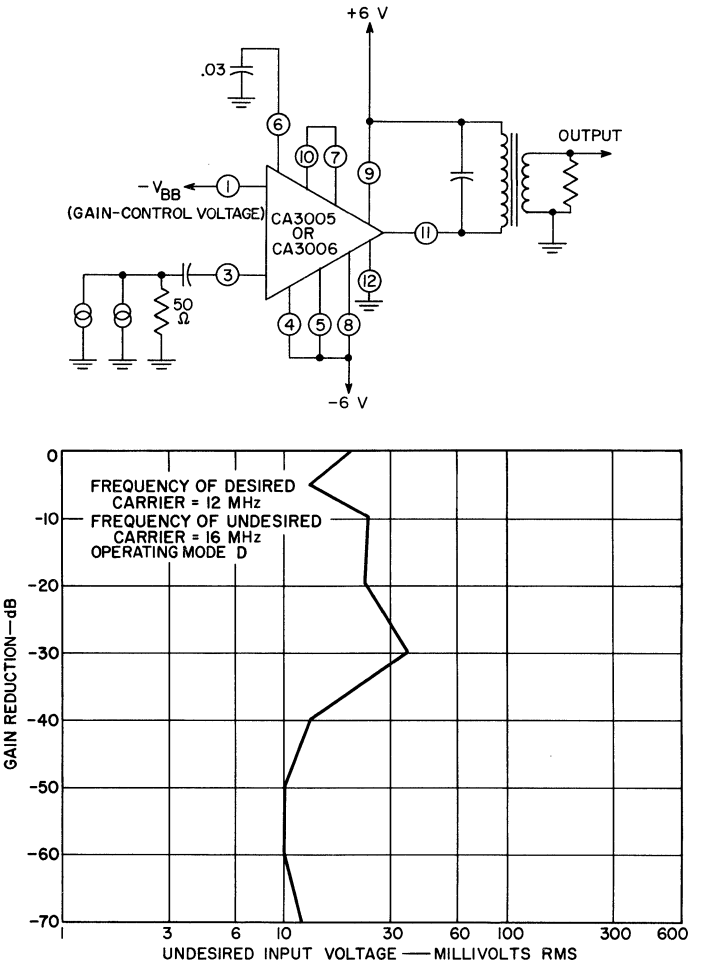


Fig. 139 — Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor Q_1. The schematic diagram illustrates the circuit configuration.

limiting is a function of I_{CC} because of the linearizing effect of the degenerative emitter resistors, R_6 and R_7. As saturation must be prevented for good limiting, a maximum load resistor and low-level voltage gain exists for a given I_{CC} and positive supply voltage. Table XVIII shows the maximum resistor values and voltage gains usable for $V_{CC} = 6$ volts, for the three circuit types. The low-level transconductance can be obtained from the slope near the origin for the curves shown in Figs. 115 and 116. The maximum

voltage gain is independent of I_{CC} in the CA3005 and CA3006 and is dependent on I_{CC} in the CA3004. Figs. 118 through 121 show the I_{CC} currents and transconductance for optional operating conditions.

Table XVIII—*Limiter Performance of a Differential Amplifier*

Supply Volts	$I_{C_1}+I_{C_2}$ (mA)	Max. Resistive Load (ohms)	Max. Tuned Load (ohms)	Voltage Gain With Emitter Degeneration (dB)		Voltage Gain Without Emitter Degeneration (dB)	
				Resistive Load	Tuned Load	Resistive Load	Tuned Load
6	0.5	12000	24000	31	37	35	41
6	1.0	6000	12000	28	34	35	41
6	2.0	3000	6000	25	31	35	41
6	3.0	2000	4000	22	28	35	41

$R_L = \frac{V_{supply}}{I_{C_1}+I_{C_2}}$ Resistive Load; $R_L = \frac{2\,V_{supply}}{I_{C_1}+I_{C_2}}$ Tuned Load; $g_m R_L$ = voltage gain

When the differential amplifier is used for limiting, the emitter-to-base breakdown voltage for transistors Q_1 and Q_2 cannot be exceeded without degradation in performance. For the CA3004, CA3005, and CA3006, this voltage including a safety margin should not exceed 2.5 volts rms. Either of two methods may be used to prevent this value being exceeded: (1) make sure the preceding stage limits before the input voltage reaches 2.5 volts (maximum voltage gain per stage approximately 20 dB), or (2) add one junction diode (D_1), as shown in Fig. 140 (this allows a maximum usable voltage gain consistent with good limiting and stability).

Cascode Amplifier — The limiting characteristics of the CA3005 or CA3006, when used as a cascode amplifier, are dependent on the current limiting in transistor Q_3 or the voltage limiting of transistor Q_1 (high-impedance output load). Limiting

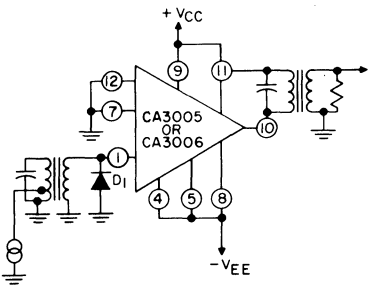


Fig. 140 — Circuit diagram of a CA3005 or CA3006 differential-amplifier limiter that uses a diode to provide input overload protection.

characteristics for both cases are shown in Figs. 141 and 142. The data in Fig. 141 are obtained with a collector load of 500 ohms. This limiting characteristic is "soft" and is acceptable over only a 20-dB range. The peak-to-peak voltage at the collector is never large enough to cause saturation. The limiting characteristic shown in Fig. 142 is obtained with a collector load of 5000 ohms, and saturation of transistor Q_1 occurs. The limiting is harder and covers a broader range, but severe tuned-circuit loading occurs.

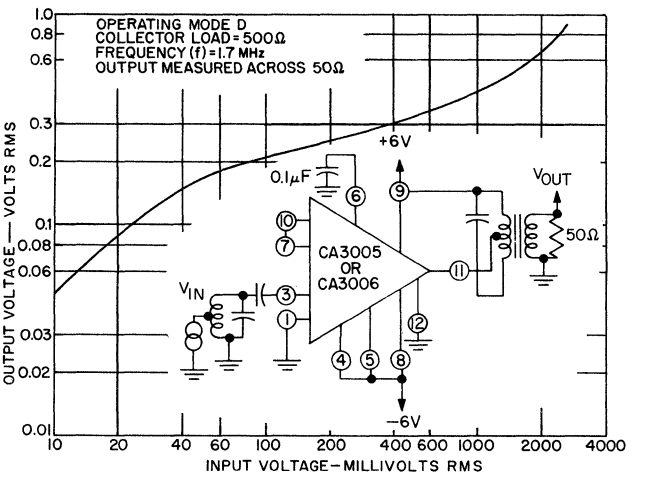


Fig. 141 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 500-ohm collector load impedance.

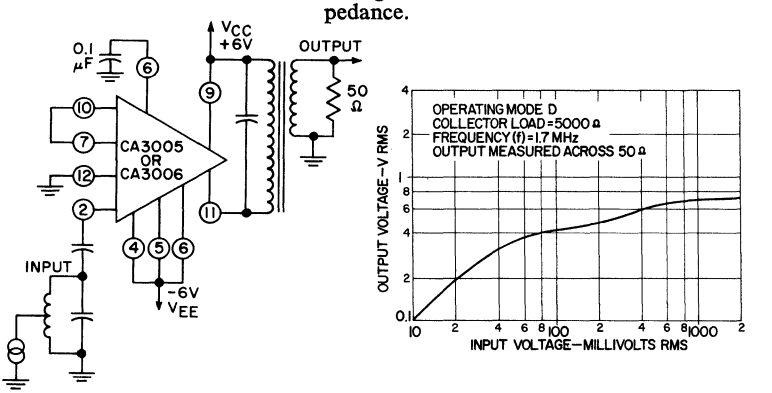
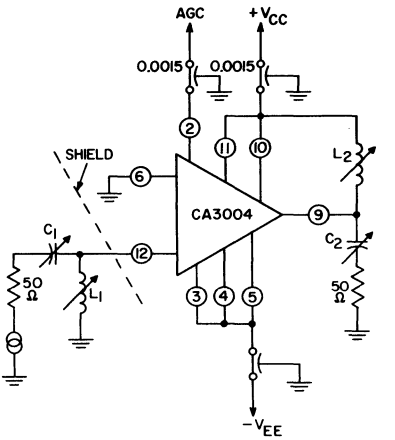


Fig. 142 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 5000-ohm collector load impedance.

RF- and IF-Amplifier Capabilities

Figs. 143, 144, and 145 illustrate the use of the CA3004, the CA3005 or CA3006 differential-amplifier configurations, and the CA3005 or CA3006 cascode configurations, respectively, as single-ended rf amplifiers. Adjustable matching networks, derived from the y parameters, are included in each circuit. The values of the adjustable components, as well as typical power gains, are also shown in the figures. A conjugate match at the input is provided for all configurations. A conjugate match at the output is impossible for the cascode configuration (as pointed out in the discussion of y parameters). At 30 MHz, the CA3005 differential amplifier output was mismatched. At high gains, the circuit feedback (y_r) is low, but the external-circuit layout adds feedback.

Two or more CA3004, CA3005, or CA3006 integrated circuits can be connected in cascade for use as a tuned if amplifier for either AM or FM applications. The schematic diagrams of two



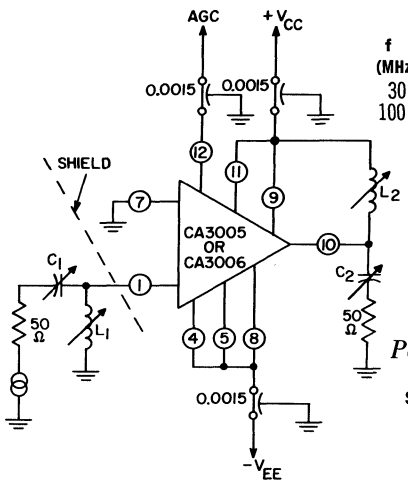
Circuit Elements

f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_2 (pF)
30	1.8-2.7	2-10	1.8-2.7	2-10
.100	0.15-0.3	0.9-7	0.1-0.2	0.9-7

Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	24	12

Fig. 143 — Circuit used to determine the rf performance capabilities of a CA3004 integrated-circuit rf amplifier.



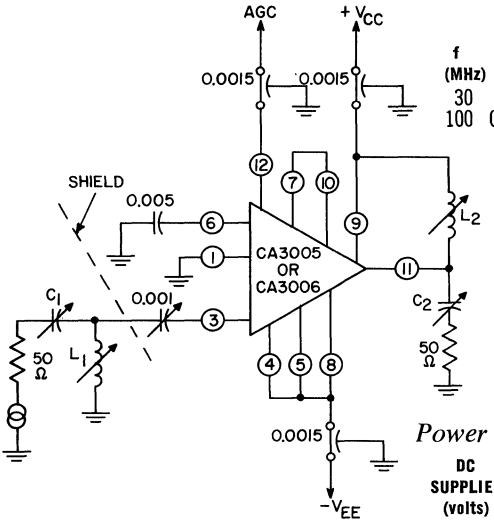
Circuit Elements

f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_1 (pF)
30	1.2-2	5-40	1.2-2	1.5-20
100	0.4-0.7	1-12	0.25-0.5	1-12

Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	29	18
±4.5	27.8	16
±3	23.0	11.5

Fig. 144 — Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a differential-amplifier configuration.



Circuit Values

f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_2 (pF)
30	0.3-0.6	14-150	0.8-1.4	5-40
100	0.07-0.12	5-40	0.15-.3	5-40

Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	36	20
±4.5	33	18.5
±3	21.5	15.0

Fig. 145 — Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a cascode configuration.

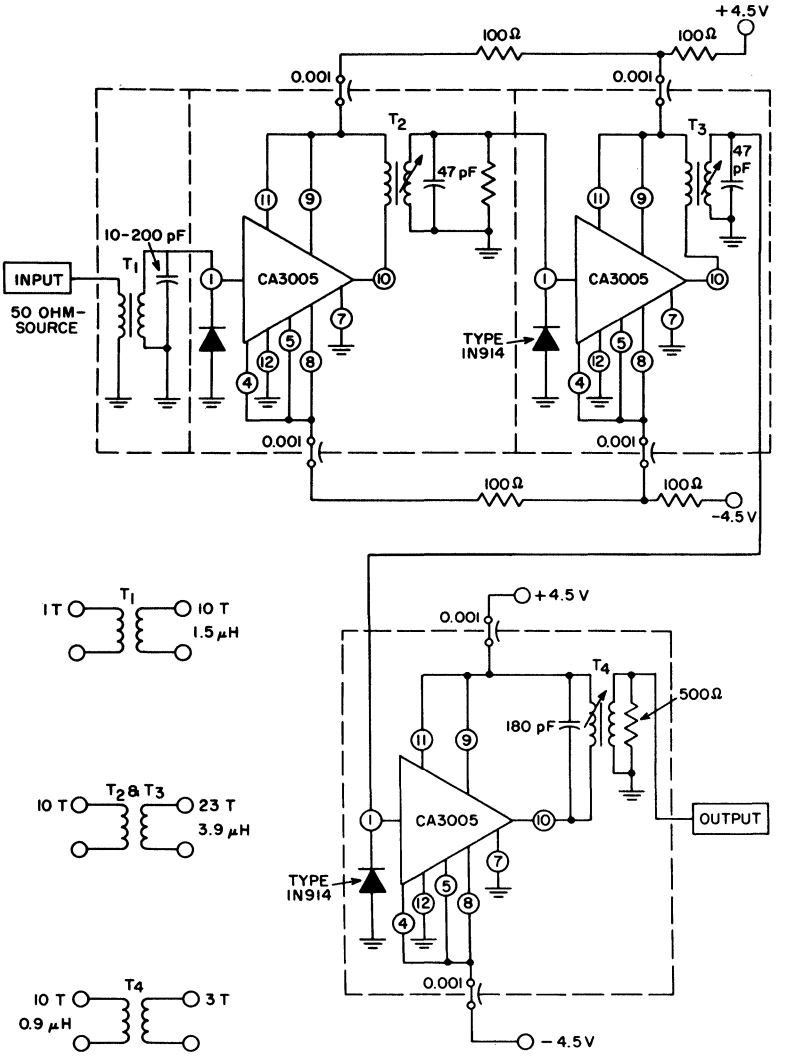
three-stage 12-MHz amplifiers are shown in Figs. 146 and 147, for FM and AM use, respectively. Both if amplifiers are housed in metal boxes, and adequate shielding and supply decoupling are provided.

The amplifier shown in Fig. 146 (limiting amplifier for FM use) is designed to provide a gain per stage of 26 dB. At this gain per stage, diodes are required at the input to prevent base-to-emitter breakdown. For operation as a low-level limiter, the circuit input is matched, and the required gain fixes the unloaded Q of the tuned circuit and the collector load. Good noise performance for the first stage is obtained by the use of a high-Q (200) toroid inductor for input transformer T_1. The other transformers are slug-tuned and have relatively low unloaded Q's (70 to 100) which contribute the necessary insertion loss for the required gain. A lower unloaded Q was required for transformer T_2, so 10,000 ohms of resistance was added in parallel with this transformer. Little or no skew is detectable in the response characteristic for this circuit, shown in Fig. 148. The limiting characteristic of the circuit is shown in Fig. 149. Other typical over-all performance characteristics are:

Total power drain = 48 milliwatts
Over-all power gain = 77 dB
3-dB bandwidth = 300 kHz
Input limiting level = 30 microvolts
Noise figure = 4 dB

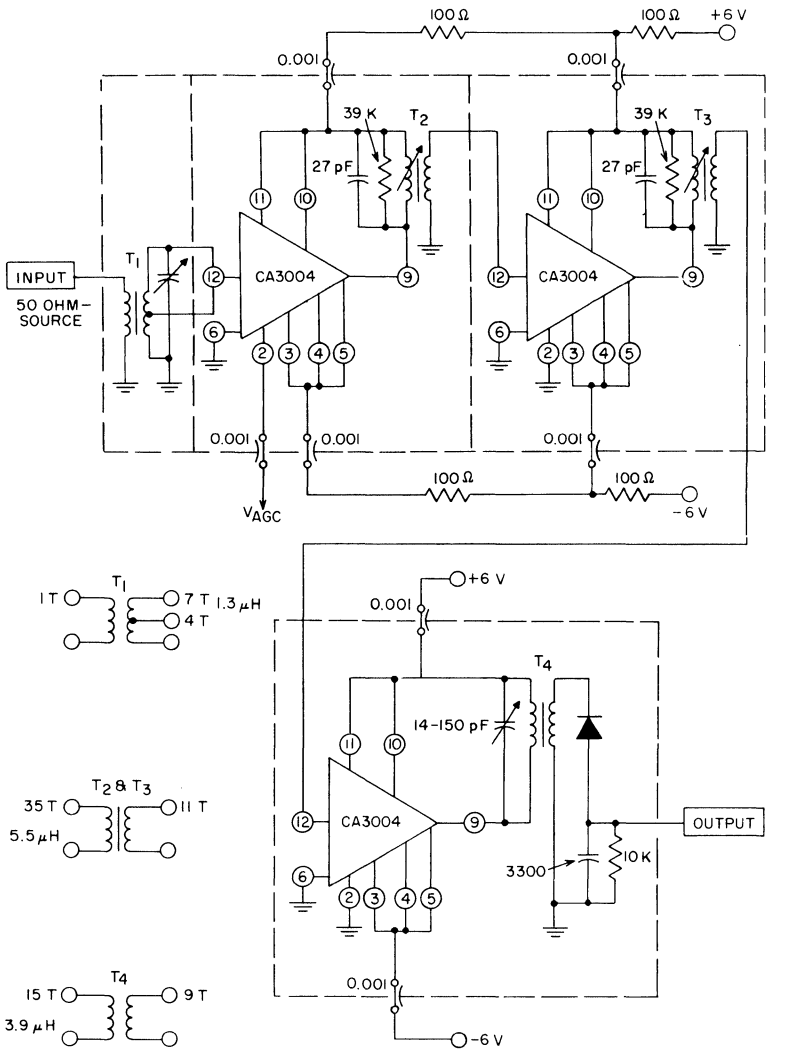
The AM circuit (Fig. 147) uses three CA3004 circuits and is designed to provide a stage gain of 25 dB. The source resistance to the input circuit was chosen as 800 ohms as a satisfactory compromise for gain, noise figure, and modulation-distortion performance. Input and output transformers, T_1 and T_4, have high unloaded Q's (200) to preserve good noise performance and to maximize the output power. The interstage transformers, T_2 and T_3, have low unloaded Q's (37) to achieve the required gain. The second detector has a 3-dB bandwidth of 5.0 kHz. The typical over-all performance characteristics are:

Power drain = 83 milliwatts
Power gain (to second-detector input) = 76 dB
AGC range (1st stage) = 60 dB
Noise figure = 4.5 dB
3-dB bandwidth = 160 kHz



Notes: 1. Transformer T_1 is a Ferramic Q-2 Type (unloaded Q = 200).
2. Transformers T_2, T_3, and T_4 are slug-tuned with carbonyl IT-75 material (unloaded Q = 75).

Fig. 146 — Three-stage, 12-MHz limiting if amplifier that uses CA3005 circuits in operating mode D.



Notes: 1. Transformers T_1 and T_4 are Ferramic Q-2 Toroid Types (unloaded Q = 200).
2. Transformers T_2 and T_3 are slug-tuned with carbonyl IT-71 material (unloaded Q = 70).

Fig. 147 — Three-stage, 12-MHz gain-controlled AM amplifier that uses CA3004 circuits in operating mode D.

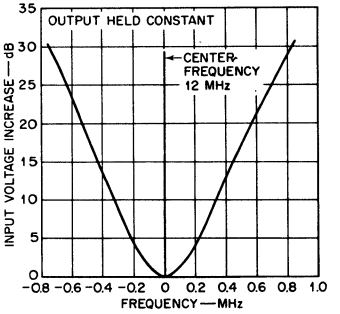


Fig. 148 — Frequency-response characteristics of the 12-MHz limiting amplifier shown in Fig. 146.

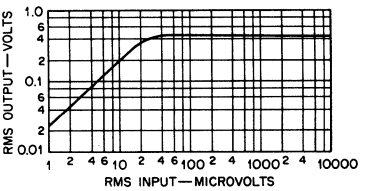


Fig. 149 — Limiting characteristics of the 12-MHz limiting amplifier shown in Fig. 146.

The signal-to-noise ratio of the circuit as a function of the input is shown in Fig. 150, and the frequency-response characteristic is shown in Fig. 151.

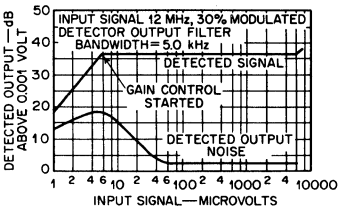


Fig. 150 — Output signal-to-noise ratio as a function of the input signal for the 12-MHz gain-controlled amplifier shown in Fig. 147 when gain control is used in only the first stage.

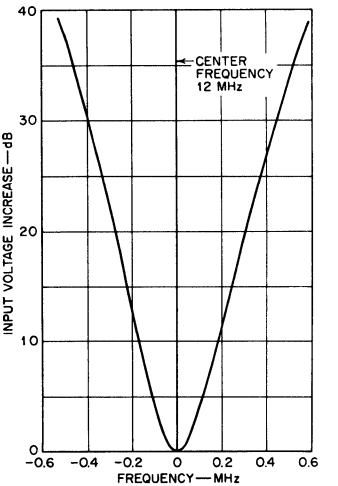


Fig. 151 — Frequency-response characteristics of the 12-MHz gain-controlled amplifier shown in Fig. 147.

Mixer Capabilities

The CA3004, CA3005, and CA3006 integrated circuits may be used as mixers, modulators, and product detectors. The schematic diagrams in Figs. 152(a) and 152(b) illustrate the use of

these circuits in mixer applications. The oscillator input is injected at the base of transistor Q_3 (because there is no direct-base connection available on the CA3004, a higher oscillator drive voltage is required for this circuit); the rf input is injected single- or

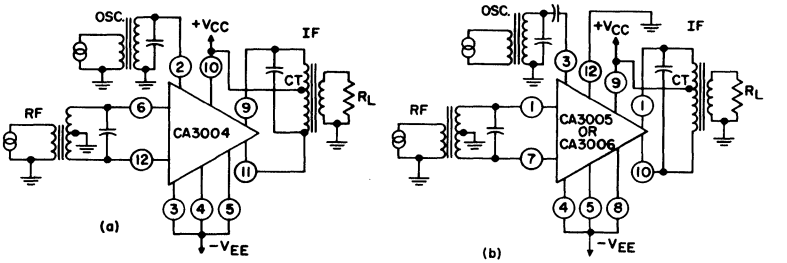


Fig. 152 — Circuit diagrams for the use of the integrated-circuit rf amplifiers as mixers (operating mode D); (a) CA3004; (b) CA3005 or CA3006.

double-ended to the bases of transistors Q_1 and Q_2. The use of a center-tapped inductor for the output tuned circuit (double-ended) allows the common-mode signal of the oscillator to be balanced out so that the oscillator will not overload subsequent stages, and provides carrier suppression for modulators.

The gain performance and generation of harmonics in the CA3004, CA3005, and CA3006 mixer circuits are dependent on the amplitude of the oscillator drive signal and the dc bias. The expression for product detection or frequency multiplication in the CA3005 or CA3006 (consult Fig. 153) is determined as follows:

$$e_o = e_1 g_m Z_L \tag{189}$$

where e_o is the output voltage, e_1 is the differential input voltage, g_m is the transconductance of the differential pair of transistors (Q_1 and Q_2), and Z_L is the load impedance (total between collectors). For a balanced circuit, the transconductance is given by

$$g_m = \frac{\alpha q}{2KT} I_o \tag{190}$$

The term I_o represents the collector current of transistor Q_3 and may be expressed as

$$I_o = g_{m_2} e_2 \tag{191}$$

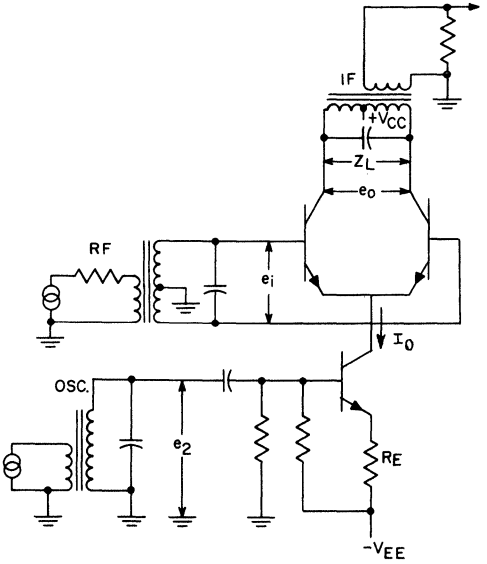


Fig. 153 — Circuit diagram of a CA3005 or CA3006 balanced mixer (operating mode D). The equations derived for product detection or multiplication are based on this circuit.

where g_{m_2} is the transconductance of transistor Q_3 and e_2 is the input voltage applied to transistor Q_3. The output voltage, e_o, therefore, is given by the following equation:

$$e_o = \frac{\alpha q}{2KT} e_1 e_2 g_{m_2} Z_L \tag{192}$$

Eq. (192) is a general expression for the output voltage of the mixer having input signals e_1 and e_2. With emitter degeneration in the constant-current transistor (Q_3), g_{m_2} is essentially constant for a sufficiently large emitter current (greater than 1 milliampere); the current I_o, therefore, follows the applied voltage e_2.

When e_1 and e_2 are sinusoidal and g_m is constant, the input signal voltages are given as follows:

$$e_1 = E_1 e^{j\omega_1 t} + \overset{*}{E}_1 e^{-j\omega_1 t} \tag{193}$$

$$e_2 = E_2 e^{j\omega_2 t} + \overset{*}{E}_2 e^{-j\omega_2 t} \tag{194}$$

($\overset{*}{E}_1$ is the conjugate of E_1, and $\overset{*}{E}_2$ is the conjugate of E_2)

With the substitution of these relationships, the equation for the output voltage for the CA3005 or CA3006 then becomes

$$e_0 = \frac{\alpha q}{2KT} g_{m_2} Z_L [E_1 E_2 e^{j(\omega_1 + \omega_2)t} + \overset{*}{E}_1 \overset{*}{E}_2 e^{-j(\omega_1 + \omega_2)t}]$$

$$+ \frac{\alpha q}{2KT} g_{m_2} Z_L [\overset{*}{E}_1 \overset{*}{E}_2 e^{j(\omega_1 - \omega_2)t} + \overset{*}{E}_1 E_2 e^{-j(\omega_1 - \omega_2)t}] \quad (195)$$

Eq. (195) gives the output voltage for a CA3005 or CA3006 used as a product detector or multiplier. (Note that only the two sideband frequencies are included in the output.) The requirements for product detectors or multipliers are that the circuit should be biased in a linear region with a small signal voltage applied. Because $\alpha q g_{m_2}/2KT$ is essentially constant, the gain of the mixer is determined from Z_L and the $e_1 e_2$ product. The linearity of the CA3006 is illustrated by the curve of the conversion transconductance as a function of the oscillator voltage, shown in Fig. 154. (Although the curve is plotted on logarithmic paper because of the wide range, the relationship is linear.) The gain reaches a

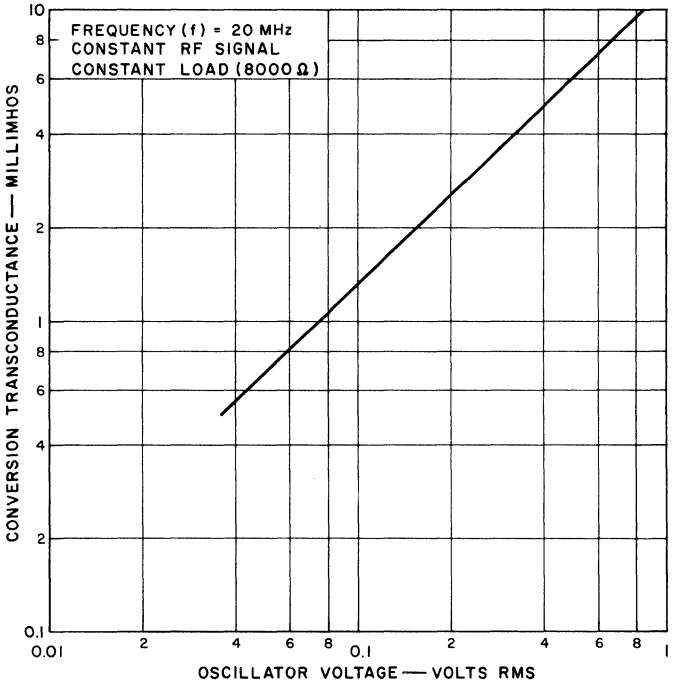


Fig. 154 — Conversion gain of a CA3005 or CA3006 mixer circuit as a function of the oscillator voltage.

maximum value at approximately 2.5 volts rms. Because measurement inaccuracies prevent the use of this curve to determine harmonic generation, spurious-signal measurements were taken on CA3005 and CA3006 mixer circuits. For these measurements, the rf input was untuned and the oscillator and if frequencies were held constant. For a fixed amplitude of oscillator injection on terminal 3, the rf was varied in frequency, and the amplitude of the responses was recorded. The results are shown in Table XIX. The spurious signals generated are a function of oscillator drive. A low oscillator drive (0.1 volt rms) produced only three spurious signals for which the rejection was less than 70 dB down.

Table XIX—*Response of a CA3005 or CA3006 Mixer to Spurious Harmonics*

Frequency	Signal Frequency f_x (MHz)	Difference-Frequency Output (dB relative to $f_o - f_x$) for V_{osc} at Term. 3 (Vrms) of 1	0.7	0.3	0.1
$f_o - f_x$	1.0	0	0	0	0
f_{if}	0.659	7.5	10	18	27
$2f_x - f_o$	1.159	—53.1	—53.1	—54.9	—52.3
$2f_o - 2f_x$	1.329	—76.1	—	—	—
$2f_x - 2f_o$	1.988	—75.5	—	—	—
$f_x - f_o$	2.318	0	0	0	0
$2f_o - f_x$	2.659	—31.7	—35	—39.7	—47.8
$2f_x - 3f_o$	2.813	—79.6	—	—	—
$f_x - 2f_o$	3.977	—31.7	—35	—39.7	—47.8
$3f_o - f_x$	4.309	—35.8	—59.3	—74.7	—
$f_x - 3f_o$	5.627	—38.5	—57	—74	—
$4f_o - f_x$	5.977	—38.9	—63	—	—

f_o = 1.659 MHz; V_{osc} = oscillator injection voltage.
All blank spaces indicate difference-frequency output more than 70 dB below the $f_o - f_x$ output.

These measurable spurious responses were third-order products that involved the second harmonic of either the oscillator or rf signal. The relative if gain increases with decreasing oscillator drive because of lower mixer gain.

The common-mode cancellation of the oscillator signal at the collector outputs is indicative of the carrier suppression that can be provided in modulators. The carrier suppression is a function of output tuned-circuit balance and the transistor offset voltage. The contribution of the offset is illustrated in Figs. 155 and 156 which show the output signal as a function of the offset voltage for the CA3004 and for the CA3005 or CA3006, respectively. These data were obtained on circuits operated with a balanced output tuned to the oscillator frequency.

Mixers — The use of the CA3004 and the CA3005 or CA3006 as balanced mixers to convert 20 MHz to 1.75 MHz, is

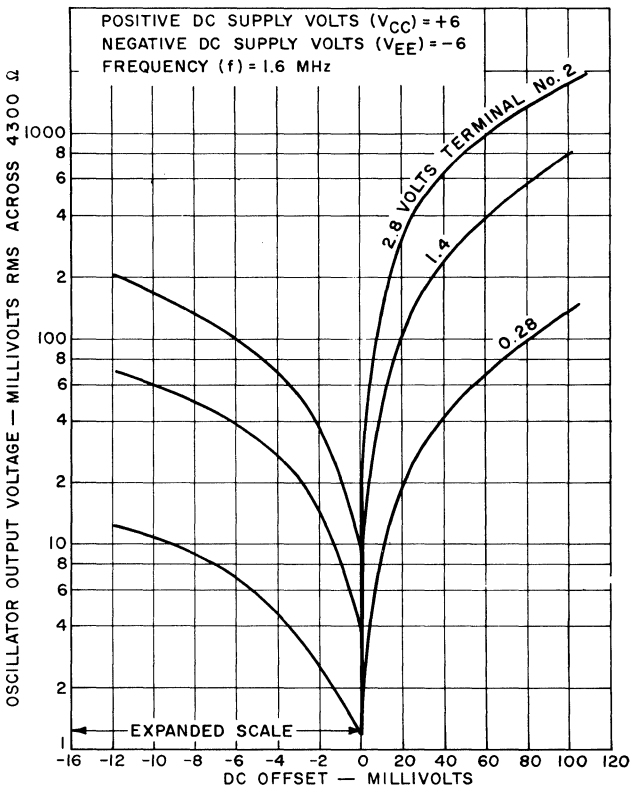


Fig. 155 — Cancellation of the oscillator signal at the output of a CA3004 mixer as a function of the dc offset voltage.

shown in Fig. 157. Because the input impedances of the two circuits differ by a factor of approximately 2:1, typically 4000 ohms for the CA3004 and 2200 ohms for the CA3005 or CA3006, different input transformers (T_1) are required; the other tuned circuits, however, are the same. The output load impedance between collectors is approximately 8000 ohms. The conversion power gain and noise figure as a function of the oscillator drive are shown in Figs. 158 and 159. Power gain increases and noise figure decreases with increases in oscillator drive.

Suppressed-Carrier Modulator and Product Detector — The CA3005 and CA3006 can be used in a suppressed-carrier double-sideband modulator and product detector. The double-sideband modulator is a convenient vehicle to evaluate carrier suppression

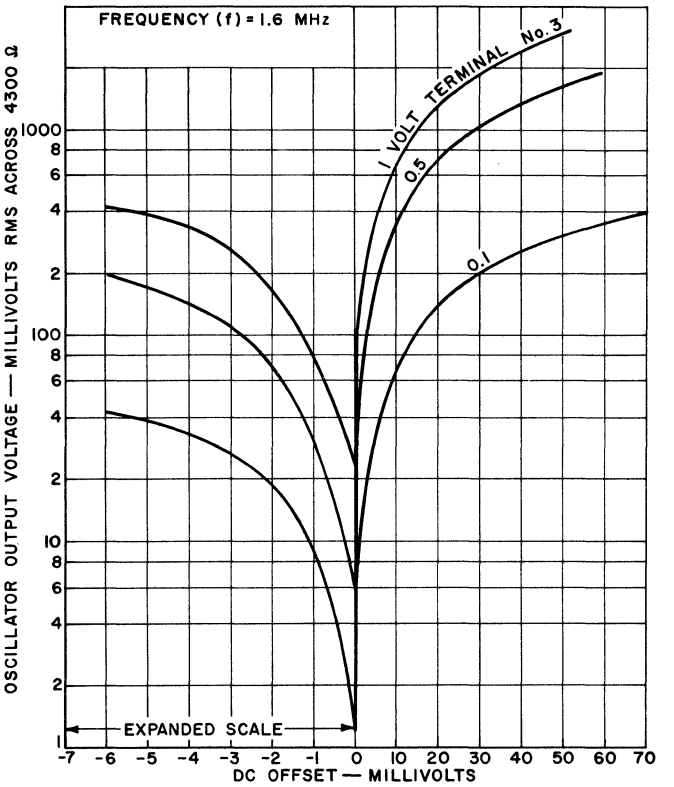


Fig. 156 — Cancellation of the oscillator signal at the output of a CA3005 or CA3006 mixer as a function of the dc offset voltage.

and product detection. With the two circuits coupled together, the relation between modulation distortion and drive levels is readily established.

Feedback may cause oscillation or unbalance; care must, therefore, be taken in the external-circuit layout design. Shielding must also be provided for both the double-sideband modulator and product detector.

The circuit diagram of the double-sideband modulator is shown in Fig. 160. The modulating signal is applied single-ended to the differential pair of transistors, Q_1 and Q_2, and the oscillator signal is applied to the base of transistor Q_3. The output is taken double-ended from the balanced transformer, T_2. The carrier

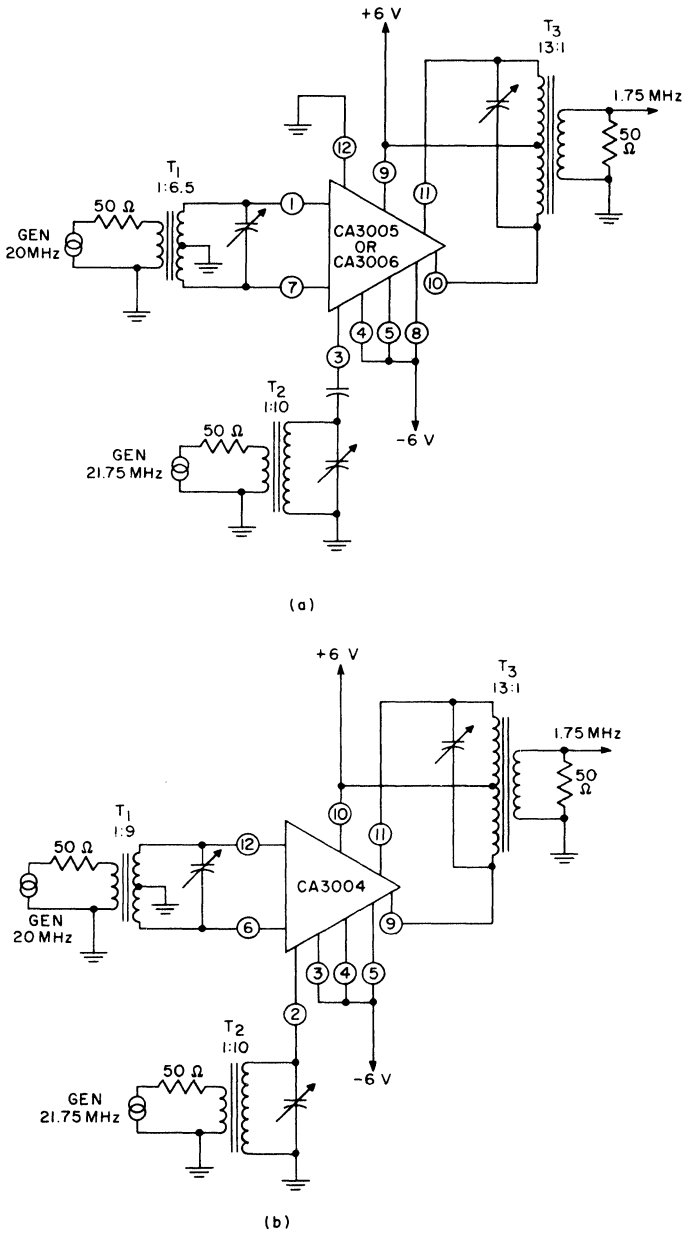


Fig. 157 — Circuit diagrams for the use of CA3004, CA3005, and CA3006 integrated circuits as balanced mixers to convert an input frequency of 20 MHz to an output frequency of 1.75 MHz.

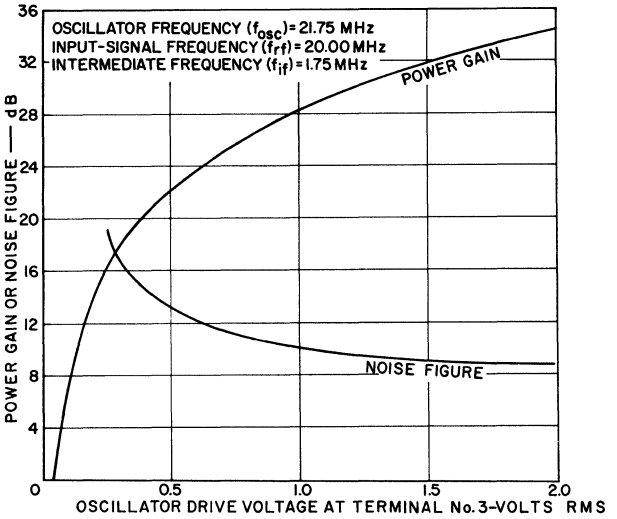


Fig. 158 — Power gain and noise figure as a function of the oscillator drive voltage for the CA3005 or CA3006 balanced mixer.

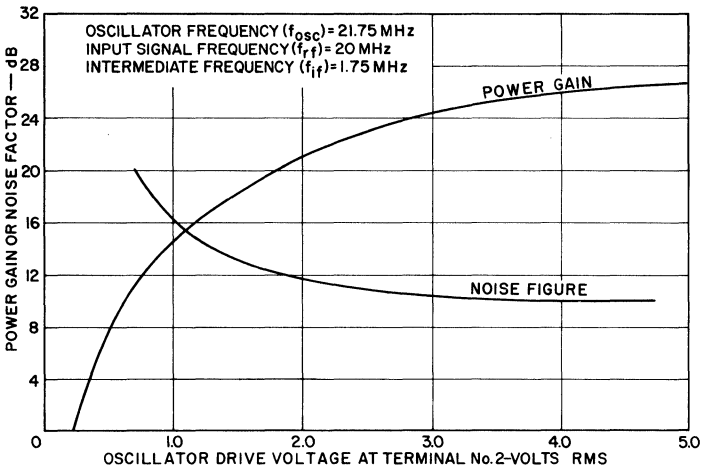


Fig. 159 — Power gain and noise figure as a function of the oscillator drive voltage for the CA3004 balanced mixer.

suppression is a function of bilateral symmetry (offset, output-transformer balance and modulation drive circuits) and the modulation-to-carrier drive ratio. With the external-circuit bilateral symmetry carefully preserved, the carrier output is approximately 25 dB below the double-sideband output for CA3006 units (offset $\leqq$ 1 millivolt) operated with a drive v_1 = 10 millivolts rms and v_2 = 31.5 millivolts rms. Although the signal-to-carrier ratio of

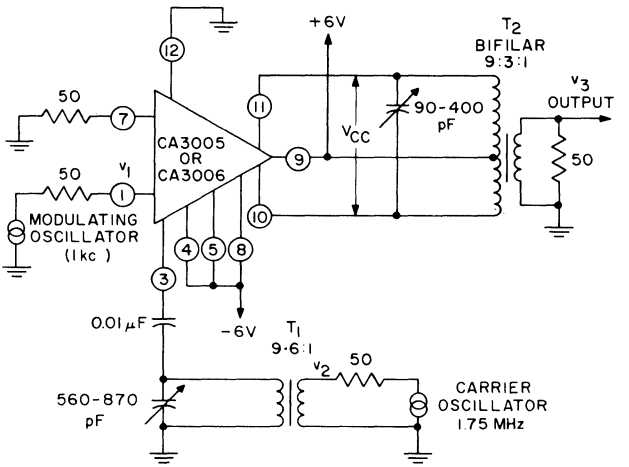


Fig. 160 — Circuit diagram for the use of the CA3005 or CA3006 as a double-sideband, suppressed-carrier modulator.

25 dB represents an inadequate rejection for most systems (40 to 60 dB is usually required), this value relaxes the filter requirements from those necessary on more commonly used single-sideband modulators. An improvement over the 25-dB ratio is obtained if the modulation drive v_1 is increased and the carrier drive v_2 is decreased, because the output is a function of the product of v_1 and v_2.

The circuit diagram for a product detector is shown in Fig. 161. The product detector, which provides the advantage of a double-ended out-of-phase output, is driven through a 50-ohm adjustable feed by the double-sideband signal from the modulator. The levels of v_1, v_2, v_4, and v_5 are altered to establish the relationship between the harmonic distortion and drive levels as well as gain values for typical operation. The results are shown in Table XX. Overdrive by the modulation (v_1) or the modulated signal (v_4) results in third-harmonic distortion of the detected signal. It should be noted that gain is a function of either the product of v_1 and v_2, or the product of v_4 and v_5.

Video-Amplifier Capabilities

The CA3004, CA3005, and CA3006 integrated circuits may be used as video amplifiers, as shown in Figs. 162(a) and 162(b). A relatively large number of external components is required, and

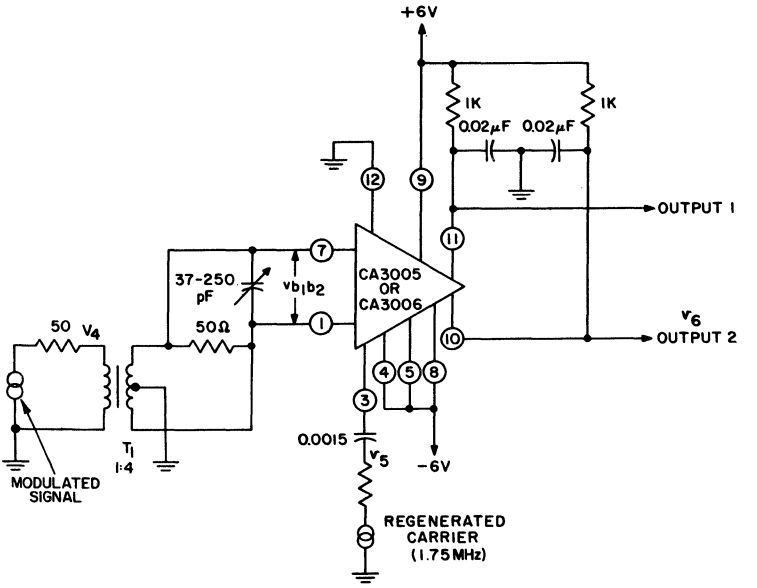


Fig. 161 — Circuit diagram for the use of a CA3005 or CA3006 as a product detector.

the availability of internal-circuit connections for these external components provides a large degree of flexibility to the user with respect to such factors as bandwidth, gain, power dissipation, and peaking. In the circuit shown in Fig. 162(a), R_1 should be equal to R_2 to preserve the circuit balance, and C_2 should be an adequate bypass so that the noise factor and gain are not degraded. For the cascode configuration shown in Fig. 162(b), C_2 is an emitter bypass, and its reactance should be less than 1.5 ohms at the lowest video frequency to be handled.

In either cascode or single-ended differential-amplifier configurations, the feedback is low. Each configuration provides good isolation from output to input; the high-frequency performance therefore can be approximated from the input and output parallel R and C for a single stage or from the total shunt R and C between stages for an iterative connection. The mid-frequency voltage gain can be computed from the familiar $g_m R_L$ product. As an aid to such calculations, Table XXI gives the input and output parallel R and C and the absolute values of g_m for the various circuits and configurations for operation at 1, 10, and 40 MHz. For more precise, but more elaborate calculations, the y parameters may be used for video-amplifier design.

Table XX—*Gain and Distortion as a Function of Different Drive Levels for a Double-Sideband Modulator and Product Detector Using the CA3006*

Variable	Term. 3	Voltages ▲ (mV rms) V_{CC}	v_3	$v_{b_1b_2}$	v_6	3rd Harmonic Distortion (dB below fundamental) *
v_1 varied, $v_2 = 31.5$ mV, $v_4 = 1$ mV, $v_5 = 0.5$ mV						
5	296	46	4.95	4	36	54
10	296	80	8.9	4	36	54
30	296	250	26.6	4	36	37.5
v_2 varied, $v_1 = 10$ mV, $v_4 = 1$ mV, $v_5 = 0.5$ mV						
31.5	296	83	8.9	4	36	54
100	960	262	28	4	36	51
315	2960	830	8.9	4	36	50
v_4 varied, $v_1 = 10$ mV, $v_2 = 31.5$ mV, $v_5 = 0.5$ mV						
0.5	296	83	8.9	2	17.5	54
1	296	83	8.9	4	36	52
3	296	83	8.9	12	110	47.5
5	296	83	8.9	20	188	37▪
v_5 varied, $v_1 = 10$ mV, $v_2 = 31.5$ mV, $v_4 = 1$ mV						
0.315	296	83	8.9	4	23	54‡
0.5	296	83	8.9	4	36	54
1.0	296	83	8.9	4	86	50

▲ See Figs. 160 and 161 for explanation of voltage designations.
* 2nd, 4th, and 5th harmonics more than 60 dB down except as noted.
▪ 2nd harmonic 51 dB down, 5th harmonic 59 dB down.
‡ 2nd harmonic 56 db down.

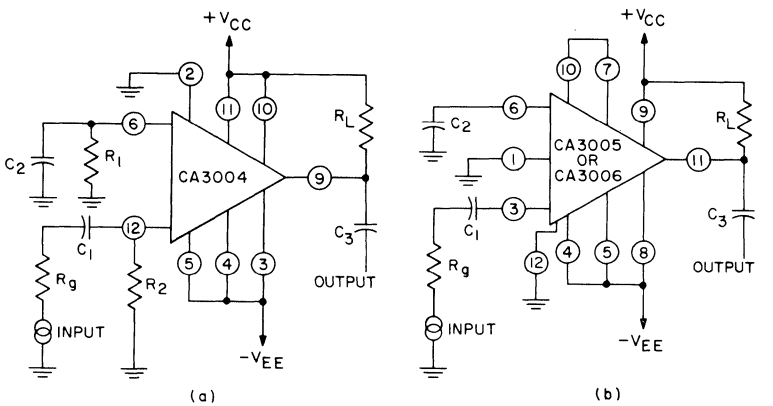


Fig. 162 — Schematic diagrams showing the use of the integrated-circuit rf amplifiers as video amplifiers: (a) CA3004 in a differential-amplifier configuration; (b) CA3005 or CA3006 in a cascode-amplifier configuration.

Table XXI—*Input and Output Parallel RC Network, Transconductance, and Video Performance Data for CA3004, CA3005, and CA3006 RF Amplifiers**

Frequency (MHz)	Input Parallel RC R_{in} (ohms)	Input Parallel RC C_{in} (pF)	Output Parallel RC R_{out} (ohms)	Output Parallel RC C_{out} (pF)	Transconductance g_m (mmhos)
CA3005 or CA3006 Cascode Operation					
1	500	42	-1.67×10^6	3	78
10	500	42	-1.67×10^6	3	77
40	180	22	-6×10^5	3	58
CA3005 or CA3006 Differential-Amplifier Operation					
1	2500	16	10^5	4	20
10	1800	13	4×10^4	4	20
40	670	10.5	2800	7.6	18.6
CA3004 Differential-Amplifier Operation					
1	6650	8	1.7×10^5	6.5	7.8
10	6650	6.2	10^5	6.1	7.8
40	2000	5	2×10^4	6.8	7.6

Video Performance (Simulated Iterative Connection)

Type	Operation	Interstage R_L (ohms)	High-Frequency 3-dB Point (MHz) Meas.	High-Frequency 3-dB Point (MHz) Calc.	Mid-Band Voltage Gain (dB) Meas.	Mid-Band Voltage Gain (dB) Calc.
CA3005 or CA3006	Cascode Differ.	150	23	20	19.3	20.6
CA3005 or CA3006	Ampl. Differ.	500	18	16	19.5	20.0
CA3004	Ampl.	1000	18.4	15	17.2	18.0

* Data obtained for circuits operated from ±6-volt dc supplies in operating mode D.

INTEGRATED-CIRCUIT OPERATIONAL AMPLIFIERS

The RCA CA3008 and CA3010 operational amplifiers are designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from ±3 volts to ±6 volts). The power dissipation in the amplifiers ranges from 7 to 92 milliwatts depending upon the supply-voltage level and the desired output-power level. The amplifiers are primarily intended to operate with externally applied negative feedback; however, they may also be operated successfully under open-loop conditions. The CA3008 operational amplifier is supplied in a 14-terminal flat-pack; the CA3010 operational amplifier is supplied in a 12-terminal TO-5 style package. With the exception of the differences in their package construction, the two operational amplifiers are identical.

Circuit Description

Fig. 163 shows the schematic diagram of the CA3008 or the CA3010 operational amplifier. The numerals shown alongside the circuit terminals indicate the terminal designations for the CA3008 14-terminal flat-pack and CA3010 12-terminal TO-5 package. The numerals enclosed in squares are the designations for the CA3010 package. (The number designations used to refer to

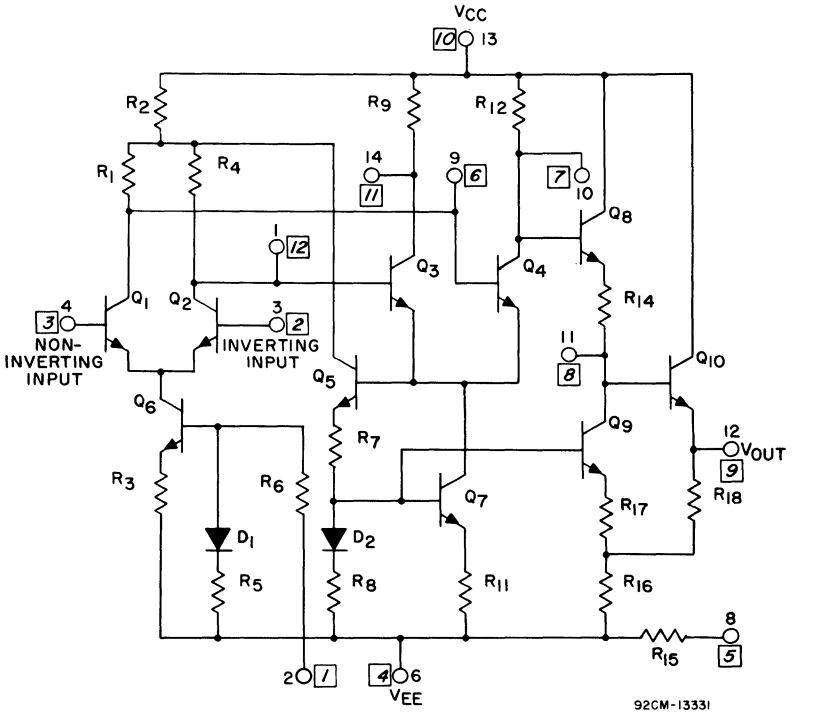


Fig. 163 — Schematic diagram of the CA3008 or CA3010 integrated-circuit operational amplifier.

specific terminals are those for the CA3008 14-terminal flat-pack. The corresponding terminals on the CA3010 12-terminal TO-5 package can be determined from the schematic in Fig. 163.)

Each operational amplifier consists basically of two differential amplifiers and a single-ended output circuit in cascade. The pair of cascaded differential amplifiers are responsible for virtually all the gain provided by the operational-amplifier circuit. The inputs to the operational amplifier are applied to the bases of the

pair of emitter-coupled transistors, Q_1 and Q_2, in the first differential amplifier. The inverting input (at terminal 3) is applied to the base of transistor Q_2, and the noninverting input (at terminal 4) is applied to the base of transistor Q_1. These transistors develop the driving signals for the second differential amplifier. A dc constant-current-sink transistor, Q_6, is also included in the first stage to provide bias stabilization for transistors Q_1 and Q_2. Diode D_1 provides thermal compensation for the first differential stage.

The emitter-coupled transistors, Q_3 and Q_4, in the second differential amplifier are driven push-pull by the outputs from the first differential amplifier. Bias stabilization for the second differential amplifier is provided by current-sink transistor Q_7. Compensating diode D_2 provides the thermal stabilization for the second differential amplifier and also for the current-sink transistor, Q_9, in the output stage.

Transistor Q_5 develops the negative feedback to reduce common-mode error signals that are developed when the same input is applied to both input terminals of the operational amplifier. Transistor Q_5 samples the signal that is developed at the emitters of transistors Q_3 and Q_4. Because the second differential stage is driven push-pull, the signal at this point will be zero when the first differential stage and the base-emitter circuits of the second stage are matched and there is no common-mode input. A portion of any common-mode, or error, signal that appears at the emitters of transistors Q_3 and Q_4 is developed by transistor Q_5 across resistor R_2 (the common collector resistor for transistors Q_1, Q_2, and Q_5) in the proper phase to reduce the error. The emitter circuit of transistor Q_5 also reflects a portion of the same error signal into current-sink transistor Q_7 in the second differential stage so that the activating error signal is further reduced.

Transistor Q_5 also develops feedback signals to compensate for dc common-mode effects produced by variations in the supply voltages. For example, a decrease in the dc voltage from the positive supply results in a decrease in the voltage at the emitters of transistors Q_3 and Q_4. This negative-going change in voltage is reflected by the emitter circuit of transistor Q_5 to the bases of current-sink transistors Q_7 and Q_9. Less current then flows through these transistors. The decrease in the collector current of transistor Q_7 results in a reduction of the current through transistors Q_3 and Q_4, and the collector voltages of these transistors tend to increase. This tendency to increase on the part of the collector voltages par-

tially cancels the decrease that occurs with the reduction in the positive supply voltage. The partially cancelled decrease in the collector voltage of transistor Q_4 is coupled directly to the base of transistor Q_8 and is transmitted by the emitter circuit of this transistor to the base of output transistor Q_{10}. At this point, the decrease in voltage is further cancelled by the increase in the collector voltage of current-sink transistor Q_9 that results from the decrease in current mentioned above.

In a similar manner, transistor Q_5 develops the compensating feedback to cancel the effects of an increase in the positive supply voltage or of variations in the negative supply voltage. Because of the feedback stabilization provided by transistor Q_5, the CA3008 and CA3010 operational amplifiers provide high common-mode rejection, have excellent open-loop stability, and have a low sensitivity to power-supply variations.

In addition to their function in the cancellation of supply-voltage variations, transistors Q_8, Q_9, and Q_{10} are used in an emitter-follower type of single-ended output circuit. The output of the second differential amplifier is directly coupled to the base of transistor Q_8, and the emitter circuit of transistor Q_8 supplies the base-drive input for output transistor Q_{10}. A small amount of signal gain in the output circuit is made possible by the bootstrap connection from the emitter of output transistor Q_{10} to the emitter circuit of transistor Q_9. If this bootstrap connection were neglected, transistor Q_9 could be considered as merely a dc constant-current sink for drive transistor Q_8. Because of the bootstrap arrangement, however, the output circuit can provide a signal gain of 1.5 from the collector of differential-amplifier transistor Q_4 to the output (terminal 12). Although this small amount of gain may seem insignificant, it does increase the output-swing capabilities of the operational amplifiers.

The output from the operational-amplifier circuit is taken from the emitter of output transistor Q_{10} so that the dc level of the output signal is substantially lower than that of the differential-amplifier output at the collector of transistor Q_4. In this way, the output circuit shifts the dc level at the output so that it is effectively the same as that at the input when no signal is applied.

Resistor R_{15} in series with terminal 8 (refer to Fig. 163) increases the ac short-circuit load capability of the operational amplifier, when this terminal is shorted to terminal 12 so that the resistor is connected between the output and the negative supply.

Operating Requirements and Characteristics

The operating characteristics of the CA3008 and CA3010 integrated-circuit operational amplifiers are identical. The characteristics data given in the following paragraphs, therefore, apply equally to each type.

DC Characteristics — The operational amplifiers are designed to operate from two symmetrical dc power supplies at supply voltages in the range from ±3 volts to ±6 volts. For operation with ±3-volt supplies, the power dissipation in the amplifiers is less than 7.0 milliwatts with terminal 8 open or 23 milliwatts with terminal 8 shorted to terminal 12. When ±6-volt supplies are used, the dissipation level increases to either 30 or 92 milliwatts, depending upon whether terminal 8 is open or shorted to terminal 12.

The input offset voltage for the operational amplifiers is typically 1.1 millivolts for all symmetrical supply voltages. This parameter is relatively insensitive to variations in the supply voltages. When ±6-volt supplies are used, the variation in the input offset voltage with fluctuations in supply voltage is typically less than 300 microvolts per volt for either supply. For ±3-volt supplies, the variation is typically 700 microvolts per volt. The offset voltage varies slightly with temperature as shown in Fig. 164. (Fig. 165 shows the schematic diagram of the special test circuit used for the offset-voltage measurements.)

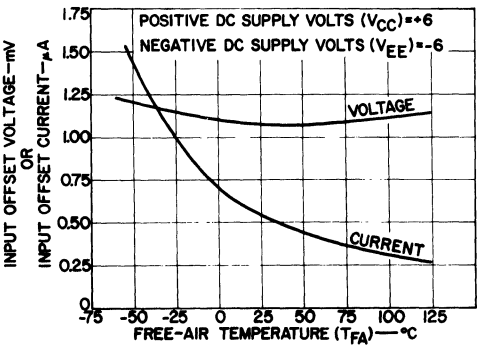
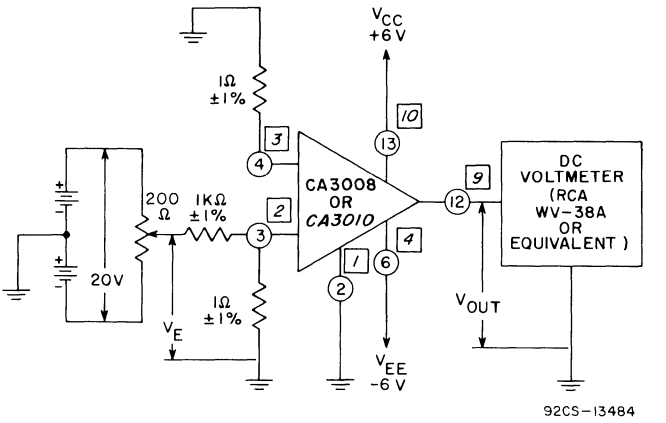


Fig. 164 — Input offset voltage and input offset current as a function of temperature.



Note: Pins 8 and 12 should be shorted for the pertinent power-dissipation measurement only.

Fig. 165 — Test circuit used to measure the input offset voltage.

The input bias current and the input offset current of the amplifiers are typically 5.3 microamperes and 0.54 microampere, respectively, when ±6-volt supplies are used. Figs. 164 and 166 show the variations in these parameters with temperature.

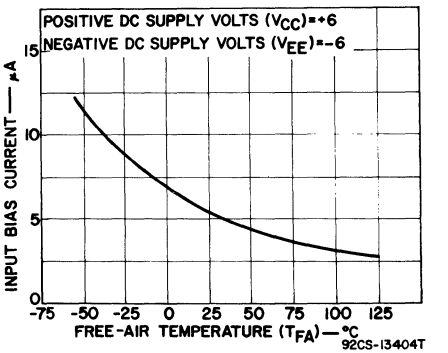


Fig. 166 — Input bias current as a function of temperature.

Gain-Frequency Response — The operational amplifiers provide a gain of 60 dB at low frequencies and have a unity-gain bandwidth of 18 MHz when operated from ±6-volt supplies. The typical gain-frequency response is shown in Fig. 167 for operation of the amplifier at −55°C, at 25°C, and at 125°C. The response

of the amplifier exhibits little change over the temperature range. A typical gain-frequency characteristic for amplifiers operated from ±3-volt supplies at 25°C is shown in Fig. 168.

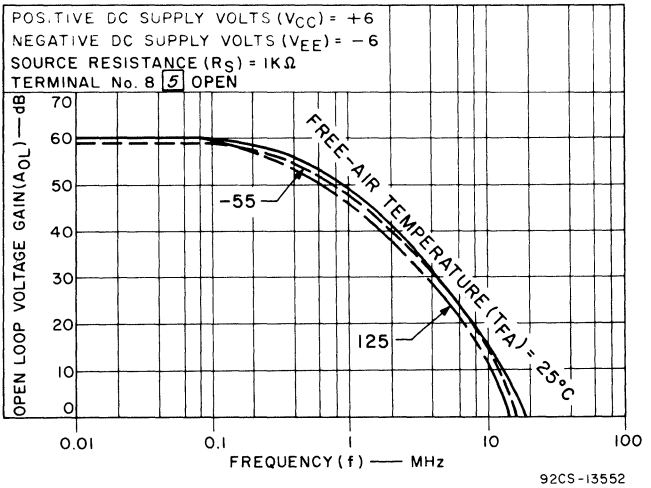


Fig. 167 — Open-loop gain as a function of frequency.

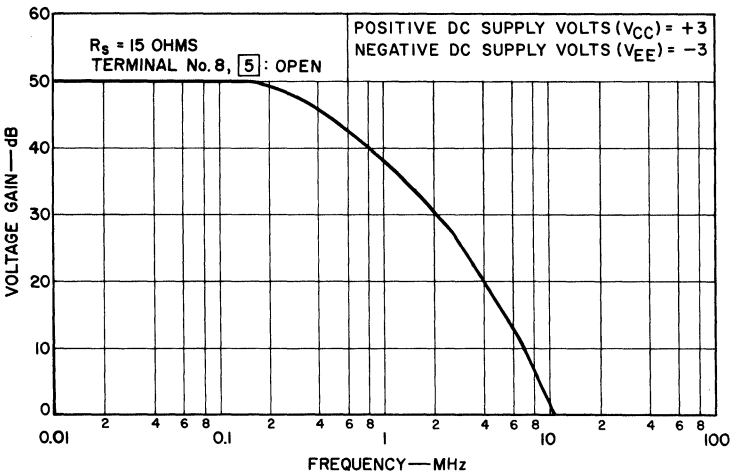


Fig. 168 — Voltage gain as a function of frequency.

Transfer Characteristic — The transfer characteristic of the operational amplifiers is shown in Fig. 169. This characteristic shows that the amplifiers do not exhibit any hysteresis effect.

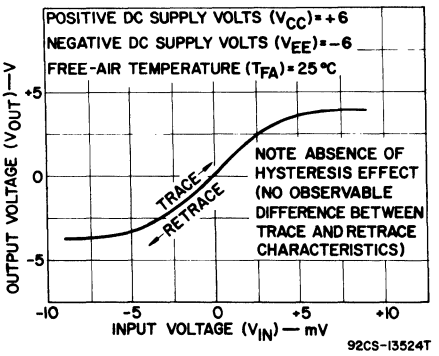


Fig. 169 — Output voltage as a function of input voltage for an open-loop operational amplifier.

Common-Mode Rejection — The common-mode rejection provided by the operational amplifiers is typically 94 dB for operation with ±6-volt supplies. Fig. 170 shows the differential-gain and common-mode gain frequency plots for the amplifiers. Fig. 171 shows the common-mode rejection as a function of frequency.

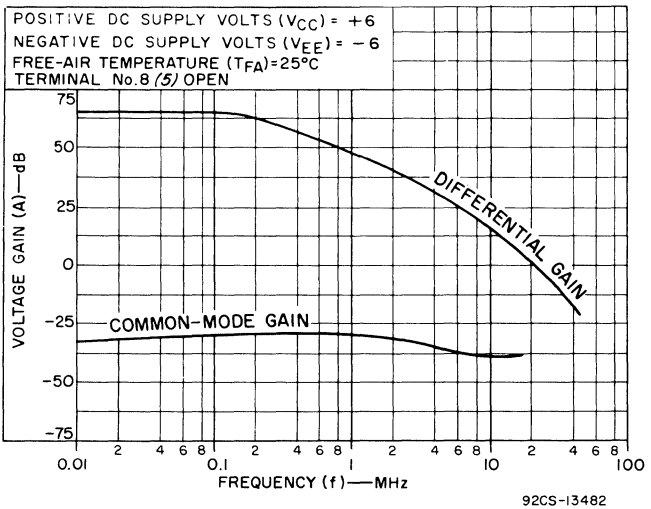


Fig. 170 — Differential and common-mode gain as a function of frequency.

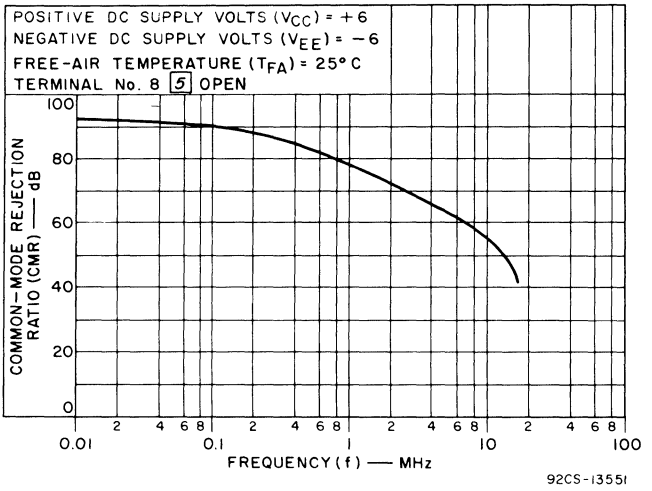


Fig. 171 — Common-mode rejection as a function of frequency.

Output Swing — The operational amplifiers exhibit a maximum dynamic-swing capability of ±3.5 volts with terminal 8 open and of ±3.0 volts with terminal 8 shorted to terminal 12. The output-swing capability varies only slightly with temperature, as shown in Fig. 172. Fig. 173 shows the variation in the output-swing capability with frequency.

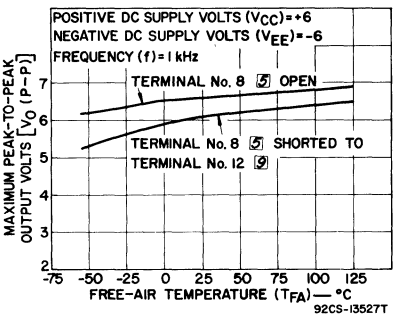


Fig. 172 — Output-swing capabilities as a function of temperature.

Input and Output Impedances — When the CA3008 or CA3010 operational amplifier is operated from ±6-volt supplies,

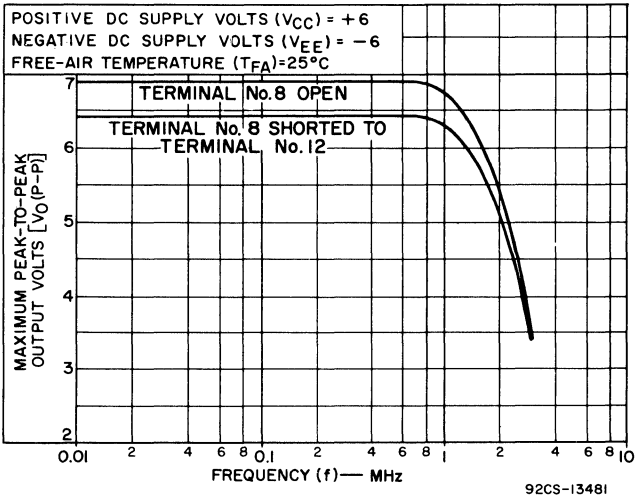


Fig. 173 — Output-swing capabilities as a function of frequency.

it has an input impedance of 14,000 ohms at 1 KHz and an output impedance of 200 ohms (terminal 8 open) or 75 ohms (terminal 8 shorted to terminal 12). The input impedance and output impedance of the amplifier are affected by temperature as shown in Figs. 174 and 175, respectively.

Output-Power Capability — A choice of two output-power capabilities is provided in the CA3008 and CA3010 operational amplifiers. The output can be tailored to the specific load requirements by leaving terminal 8 open and placing an appropriate resistor between terminals 6 and 12. The minimum safe value of load resistance (including the aforementioned resistor) is 200 ohms when ±6-volt supplies are used. In determining the output capability, it should be kept in mind that the feedback network can contribute to the output loading especially in the lower-gain con figurations.

The output-power capability of the operational amplifiers can be increased by the addition of an external emitter-follower output stage or a class B push-pull output stage. The emitter-follower approach is highly inefficient from a dissipation standpoint. A class B push-pull output stage, added as shown in Fig. 176, works well in a closed-loop circuit, but is subject to thermal runaway under

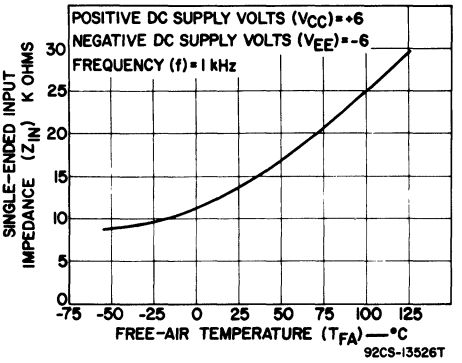


Fig. 174 — Input impedance as a function of temperature.

open-loop conditions. The thermal-runaway effect may be controlled by the introduction of a small amount of emitter degeneration in each of the push-pull transistors. The load requirements, however, are sometimes severe enough to preclude the use of emitter degeneration. Moreover, depending on the choice of complementary transistors, the addition of the push-pull amplifier may limit the over-all bandwidth.

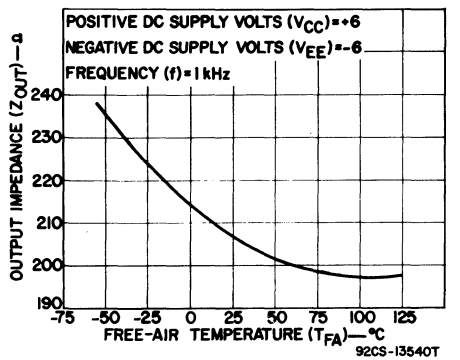


Fig. 175 — Output impedance as a function of temperature.

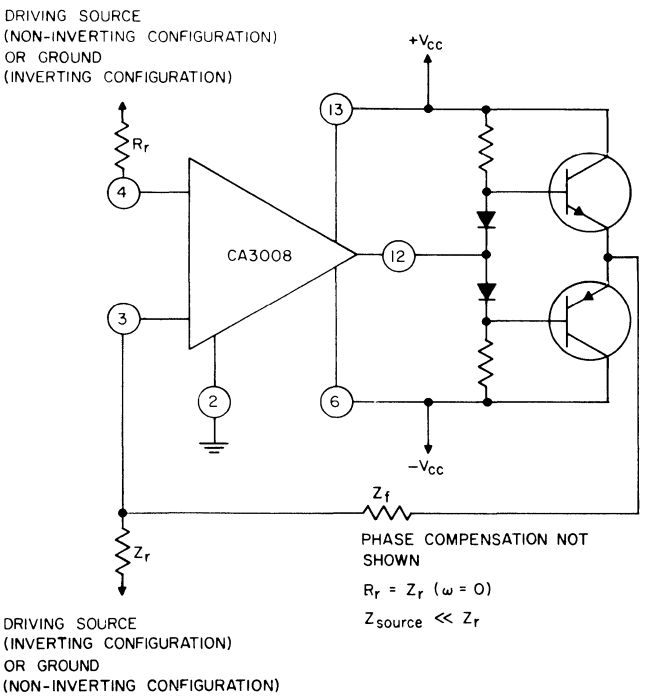
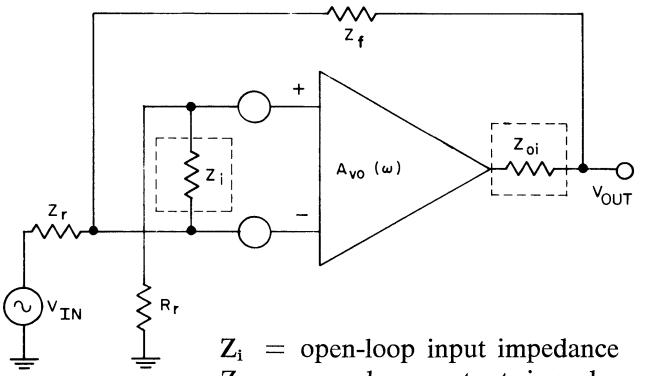


Fig. 176 — Schematic diagram showing the addition of an external push-pull output stage to increase the output capability of an operational amplifier.

Applications of the Operational Amplifiers

The response characteristics of an operational amplifier can be controlled by an external feedback circuit. Because of this feedback control, the amplifier can be used to synthesize a wide variety of transfer functions and is, therefore, useful in many diverse applications. Figs. 177 and 178 show the basic schematic diagrams for the use of the CA3008 or CA3010 operational amplifier in the inverting and noninverting feedback configurations, respectively. For convenience, the "classical" design equations for each type of configuration are repeated below the schematic diagram. In each configuration, the two inputs are returned to ground through dc paths that are effectively identical, as required to assure a minimum offset voltage.



Z_i = open-loop input impedance
Z_{oi} = open-loop output impedance
$A_o(\omega)$ = open-loop gain

$$R_r = Z_r\ (\omega = 0) /\!/ Z_f\ (\omega = 0)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-Z_f}{Z_r + (Z_f + Z_r)/A_o(\omega)} = -\frac{Z_f}{Z_r}$$

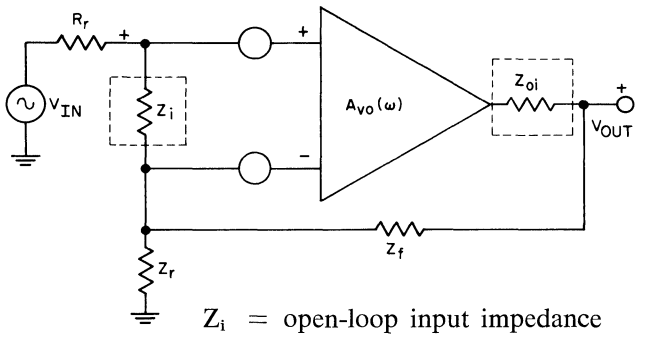
$$Z_{IN} = Z_r + \left(\frac{Z_f}{A_o(\omega)} /\!/ Z_i\right) \doteq Z_r$$

$$Z_o = Z_{oi}\,\frac{1 + \dfrac{V_{OUT}}{V_{IN}}}{A_o(\omega)} \doteq 0$$

Fig. 177 — Inverting-feedback configuration for an operational amplifier.

The open-loop input capacitance of the CA3008 and CA3010 integrated-circuit operational amplifiers is less than 10 picofarads; the frequency response of these amplifiers, therefore, is virtually independent of the drive source impedance. The input-impedance equations given in Figs. 177 and 178 indicate that this lack of dependence is even more pronounced when the amplifiers are operated with negative feedback.

In any given application of the operational amplifiers, small values of capacitance properly added to the circuit will provide the required phase compensation. When ±6-volt supplies are used, two phase-compensating networks, each of which consists of a 27-picofarad capacitor in series with a 2000-ohm resistor, connected between terminals 1 and 14 and between terminals 9 and 10, cause



Z_i = open-loop input impedance
Z_{oi} = open-loop output impedance
$A_o(\omega)$ = open-loop gain

$$R_r = Z_r\ (\omega = 0) /\!/ Z_f\ (\omega = 0)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\ (Z_r + Z_f)}{Z_r + Z_f + Z_o\ Z_r} \doteq 1 + \frac{Z_f}{Z_r}$$

$$Z_{IN} = Z_i \left(1 + \frac{A_o(\omega)}{\dfrac{V_{OUT}}{V_{IN}}} \right)$$

$$Z_o = Z_{oi} \left(\frac{\dfrac{V_{OUT}}{V_{IN}}}{A_o(\omega)} \right)$$

Fig. 178 — Noninverting-feedback configuration for an operational amplifier.

the closed-loop response of the integrated-circuit operational amplifier to roll off at a slope of one (6 dB per octave) all the way to unity gain (where it then breaks into a slope of two). This value of compensation is sufficient to stabilize the amplifier for all resistive-feedback applications including unity gain. The response for this value of phase compensation is compared to the original open-loop response in Fig. 179. Although the two compensating networks are sufficient to ac-stabilize the amplifier, they are not sufficient to produce a flat response (within ±1 dB) for closed-loop gains below 15 dB. Fig. 180 shows a plot of the capacitance required to produce a flat (±1-dB) gain response as a function of closed-loop gain. The capacitors must have a resistor in series with them so that $1/(2\pi RC) = 3$ MHz.

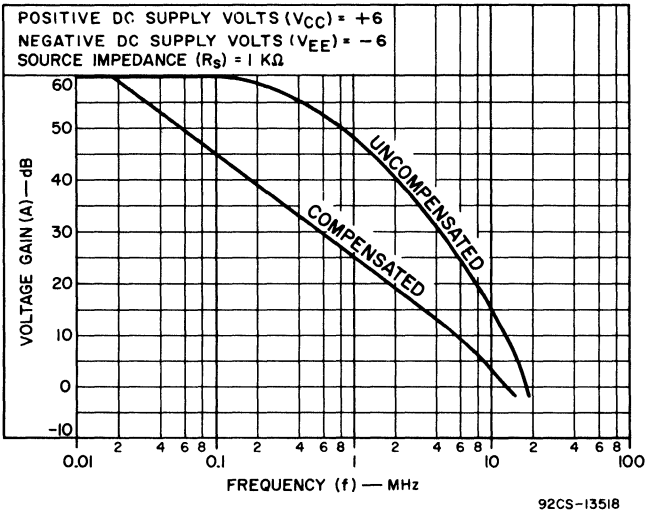


Fig. 179 — Open-loop gain as a function of frequency for both phase-compensated and uncompensated operational amplifiers.

Phase compensation may also be effected conventionally by adding a capacitor in series with a resistor between terminal 11 and ground. A 0.02-microfarad capacitor in series with a 22-ohm resistor is sufficient to ac-stabilize the integrated-circuit operational amplifier at resistive closed-loop gains down to unity.

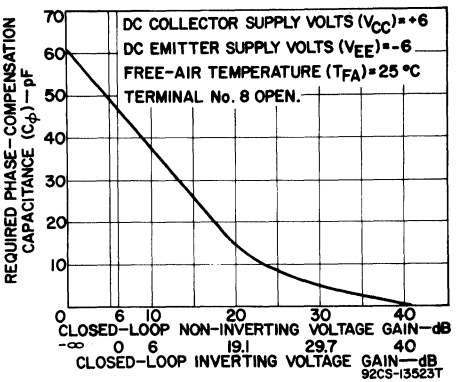


Fig. 180 — Amount of phase-compensating capacitance required to obtain a flat (± 1-dB) gain response as a function of frequency.

The required phase compensation depends upon the feedback configuration and not upon the location of the drive source. Hence, phase-compensating networks that provide sufficient compensation

for a 10-dB noninverting configuration also provide sufficient compensation for a 6-dB inverting configuration because the two feedback configurations are identical.

Video Amplifiers — When the feedback is applied through a purely resistive network and suitable phase compensation is employed, flat gains are attainable from the operational amplifiers. Fig. 181 shows a 30-dB noninverting configuration of a video amplifier, together with the closed-loop response of the circuit. The

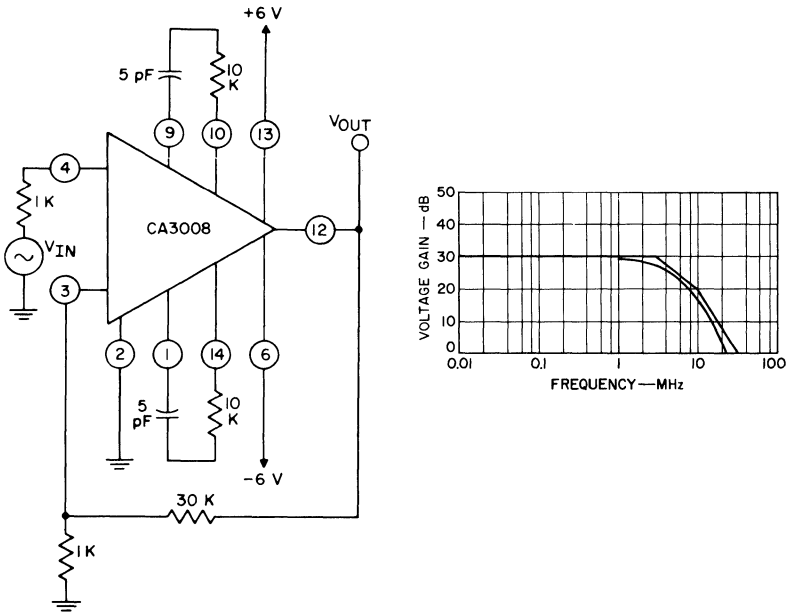


Fig. 181 — Noninverting configuration and closed-loop response of an operational-amplifier type of video amplifier that provides a gain of 30-dB.

phase compensation is provided by a 5-picofarad capacitor in series with a 10,000-ohm resistor. This arrangement provides the required amount of compensation, as predicted in Fig. 180. (For purposes of comparison, the uncompensated response of the 30-dB configuration is shown in Fig. 182. Observe the 13-dB peaking effect at 4.5 MHz.) An alternate method of phase compensation may be used when the intersection of the closed-loop characteristic and the open-loop response occurs in a two-slope region. The technique is to cause the feedback ratio (Z_f/Z_r) to roll off at a slope of one.

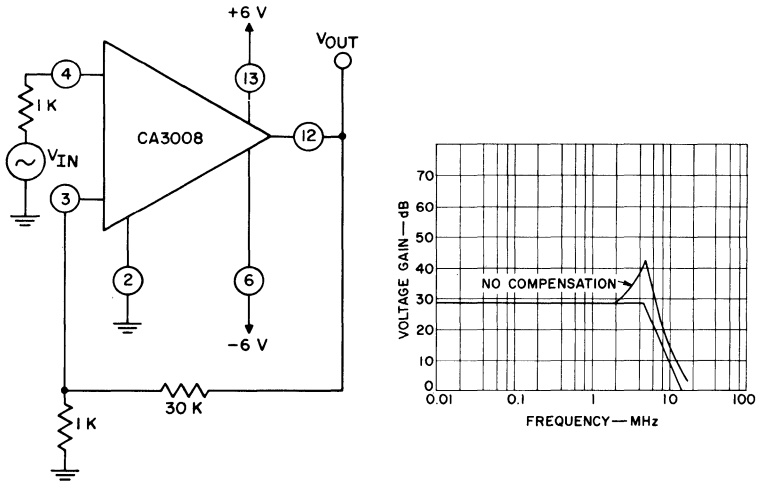


Fig. 182 — Circuit diagram and gain-frequency response of the 30-dB noninverting video amplifier operated without phase compensation.

Fig. 183 illustrates this alternate technique for the 30-dB gain circuit.

The low-frequency input impedance of the 30-dB noninverting configuration is 480,000 ohms, as calculated from the appropriate equation in Fig. 178 (Z_i = 14,000 ohms).

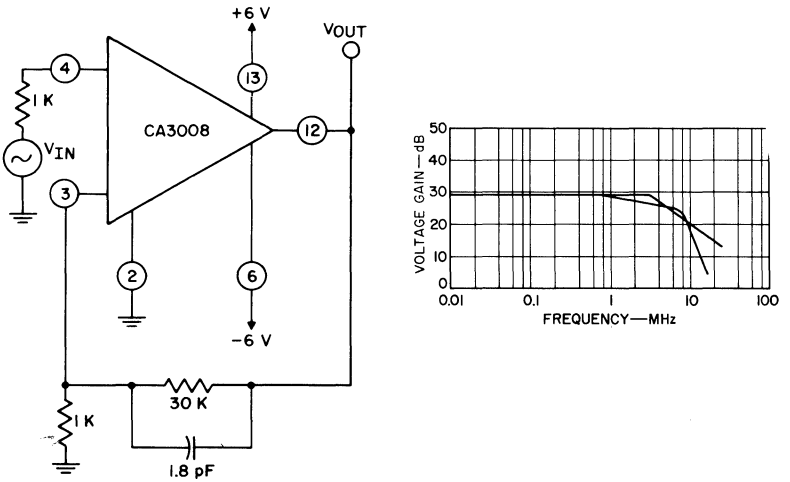


Fig. 183 — Circuit diagram and gain-frequency response of the 30-dB video amplifier when the phase compensation is accomplished by the addition of a capacitor in parallel with the feedback resistor.

Fig. 184 shows the configuration and the response of a 6-dB inverting type of video amplifier. The intersection of the closed-loop characteristic with the compensated open-loop response predicts the 3-dB bandwidth of the video amplifier provided the

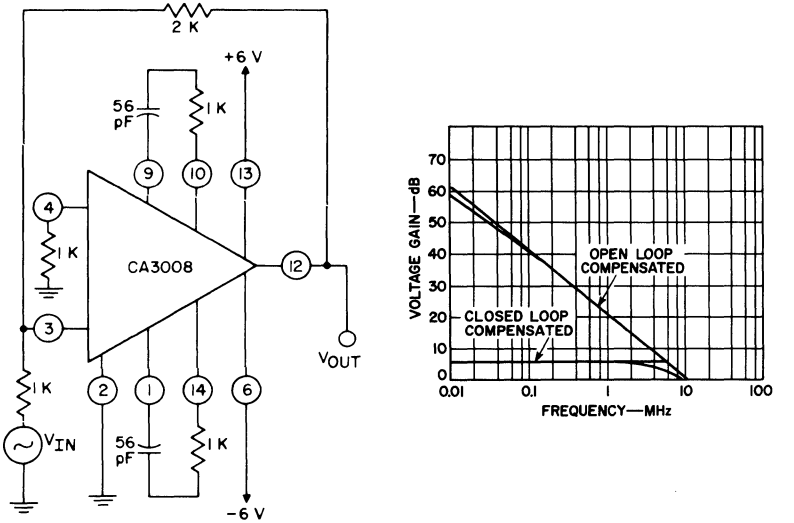


Fig. 184 — Circuit diagram and response of an inverting type of operational amplifier used as a 6-dB video amplifier.

transfer phase shift of the open-loop amplifier is approximately −90 degrees. This relationship suggests a way to extend the bandwidth without peaking. In the 6-dB video amplifier shown in Fig. 185, the 3-dB bandwidth has been increased from 5.6 to 11 MHz by a decrease in the value of the phase-compensating capacitors from 56 to 33 picofarads.

Because a broad-band amplifier should be capable of handling digital signals, data were taken to determine this capability. Figs. 186(a) and 186(b) illustrate the pulse-handling capabilities of the 30-dB noninverting circuit shown in Fig. 181. Fig. 186(a) shows the low-level (non-saturating) pulse response. The input is a 38-millivolt, 960-nanosecond pulse; the output is a 1.1-volt pulse having a 40-nanosecond delay time, a zero storage time, and 125-nanosecond rise and fall times. Fig. 186(b) shows the response of the amplifier for a 960-nanosecond input pulse under 20-dB overdrive conditions. The output pulse has an amplitude of 3.2 volts, a delay time of 32 nanoseconds, a storage time of 160 nanoseconds, a rise time of 500 nanoseconds, and a fall time of 160 nanoseconds.

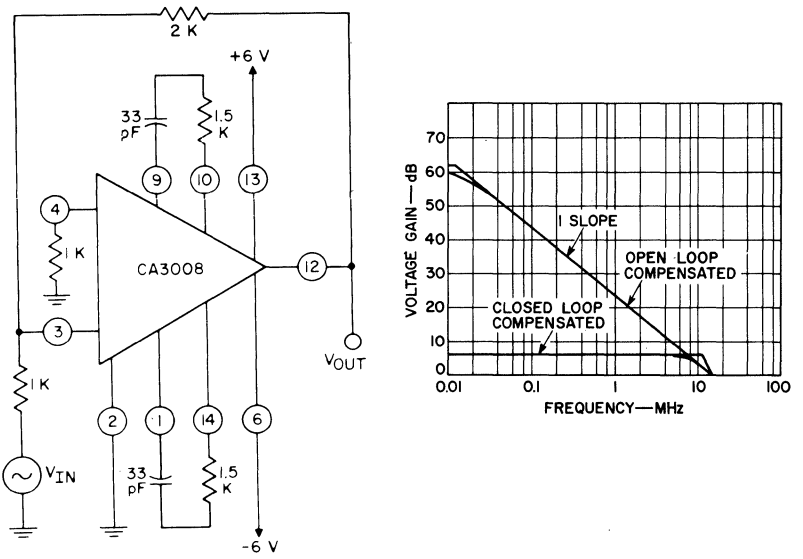
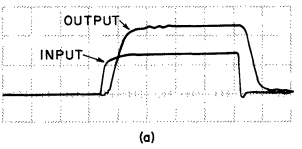
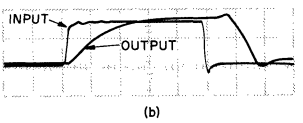


Fig. 185 — Effect of a decrease in the phase-compensating capacitance from 56 picofarads to 33 picofarads on the response of the 6-dB video amplifier.



Low-Level Pulse

$V_{IN} = 38$ mV
$V_{OUT} = 1.1$ V
$t_d = 40$ ns
$t_s = 0$ ns
$t_r = t_f = 120$ ns



Overdriven Pulse

$V_{IN} = 1.27$ V
$V_{OUT} = 3.2$ V
$t_d = 32$ ns
$t_s = 160$ ns
$t_r = 500$ ns
$t_f = 160$ ns

Note:

t_d = DELAY TIME
t_s = STORAGE TIME
t_r = RISE TIME
t_f = FALL TIME

Fig. 186 — Pulse-handling characteristics of the noninverting 30-dB video amplifier: (a) Low-Level pulse response; (b) Pulse response under overdrive conditions.

Frequency-Shaping Amplifiers — The operational amplifiers may be used to create simple frequency-shaped characteristics, such as those associated with band-pass, notched-response, and single-tuned narrow-band amplifiers.

Fig. 187 shows a noninverting amplifier that may be used to synthesize the following peaked-response transfer function:

$$\frac{V_{OUT}}{V_{IN}} = +10 \frac{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_4}\right)}{\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \tag{196}$$

In terms of the notations employed in Fig. 25, the break-frequency equations for the amplifier may be expressed as follows:

$$f_1 = \frac{10}{2\pi C_r(R_f + 10R_r)} = 10 \text{ kHz} \tag{197}$$

$$f_2 = \frac{1}{2\pi C_r R_r} = 40 \text{ kHz} \tag{198}$$

$$f_3 = \frac{1}{2\pi C_n(R_n + R_f)} = 200 \text{ kHz} \tag{199}$$

$$f_4 = \frac{40}{2\pi C_n(40R_n + R_f)} = 800 \text{ kHz} \tag{200}$$

These break-frequency equations are the precise equations derived from the gain equation in Fig. 178. The amount of phase compensation required is that shown in Fig. 180 for a noninverting gain of 20 dB.

Fig. 188 shows the circuit configuration and the frequency response of a narrow-band, 100-KHz tuned amplifier. The circuit Q is 33.3. A true single-tuned response can be obtained from only an inverting circuit configuration, as shown by the gain equation for the two types of configurations given in Figs. 177 and 178 and repeated below:

1. For the inverting configuration, the gain equation is given as:

$$\frac{V_{OUT}}{V_{IN}} = -Z_r/Z_r$$

2. For the noninverting configuration, the following gain equation is used:

$$\frac{V_{OUT}}{V_{IN}} = 1 + Z_r/Z_r$$

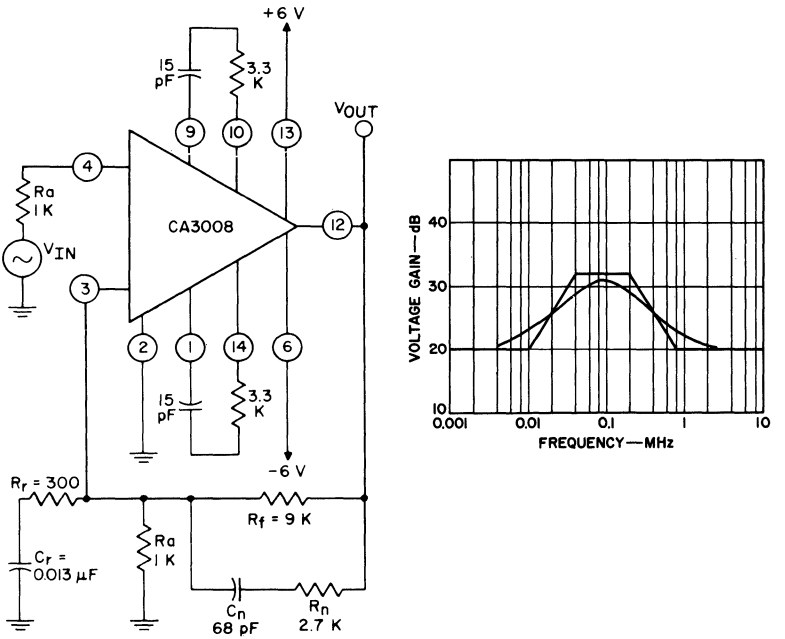


Fig. 187 — Circuit diagram and response of a noninverting type of operational amplifier used to synthesize peaked-response transfer functions.

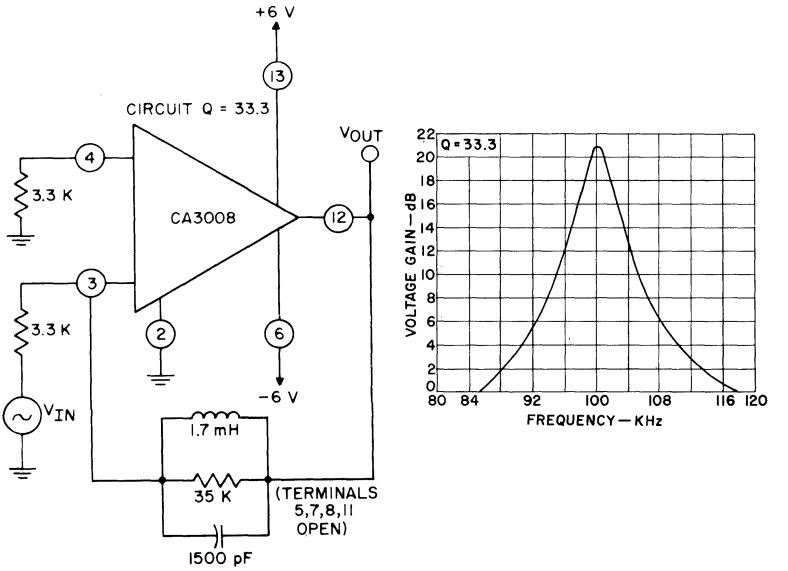


Fig. 188 — Circuit diagram and response of inverting type of operational amplifier used as a narrow-band 100-kHz tuned amplifier.

The "1+" term in the gain expression for the noninverting configuration indicates that the gain of this type of circuit will never decrease to zero as required for a true single-tuned response. The amount of phase compensation required for the narrow-band 100-kHz amplifier is the value given in Fig. 180 for an inverting gain of 0.0 (infinite attenuation).

Comparators — The CA3008 and CA3010 operational amplifiers have excellent transfer characteristics for comparator applications. As shown in Fig. 169, the amplifiers have no observable hysteresis effect; the trace (minus to plus) and retrace (plus to minus) excursions coincide.

Integrators — The important design consideration when an operational amplifier is to be used as an integrator is that the dc feedback path has a time constant which is much shorter than the periods for the frequencies of interest. This relationship is necessary so that an offset (error) voltage cannot continuously charge the feedback capacitor until the amplifier limits. Fig. 189 shows the circuit configuration for the use of the CA3008 or CA3010 operational amplifier as an integrator and the responses of the circuit for 1-kHz square-wave inputs. The dc gain of the circuit is

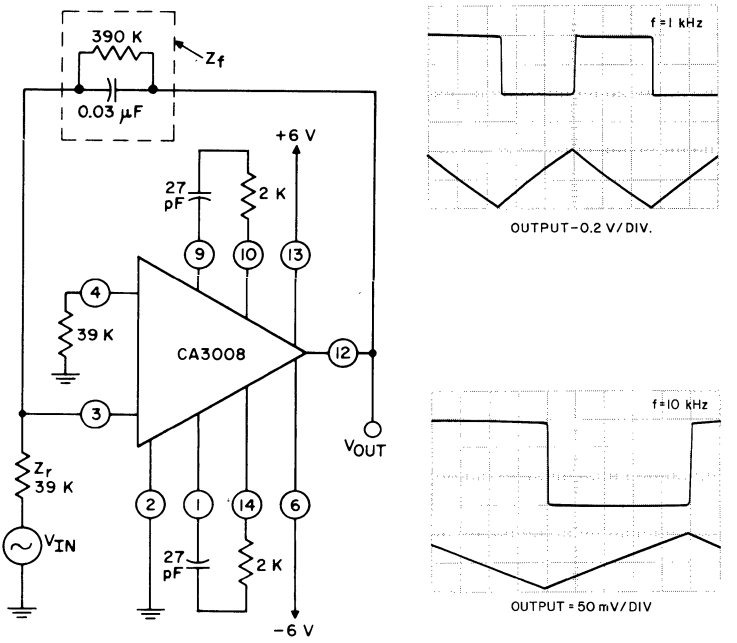


Fig. 189 — Circuit diagram and the input and output waveforms for an operational amplifier used as an integrator.

limited to 20 dB by the 390,000-ohm feedback resistor. The effect of this resistor on the gain, however, becomes negligible for ac signals at frequencies above 13 Hz because of the 0.03-microfarad capacitor in parallel with it. The weighting factor of integration for the circuit is about 1 millisecond (R = 39,000 ohms; C = 0.03 microfarad).

Phase compensation must also be provided in an integrating amplifier circuit to assure ac stability. In general, the amount of compensation required is the maximum value given by Fig. 180, because the closed-loop characteristic of the integrator has rolled off completely at the frequency where the intersection of the open-loop response and the closed-loop characteristic occurs.

Differentiators — The main problem in the design of differentiating amplifiers is that the gain of such amplifiers increases with frequency; hence, they are susceptible to high-frequency noise. The classical remedy for this effect is to connect a small resistor in series with the input capacitor so that the high-frequency gain is decreased. Actually, the addition of the resistor results in a more realistic model of a differentiator because a resistance is always added in series with the input capacitor by the source impedance. The schematic diagram of a CA3008 or CA3010 operational amplifier used as a differentiating circuit and the response of the circuit for 1-kHz square waves are shown in Fig. 190. A value of 51 ohms is selected for the gain-limiting resistor to illustrate that the effect of the source impedance is not necessarily negligible in dif-

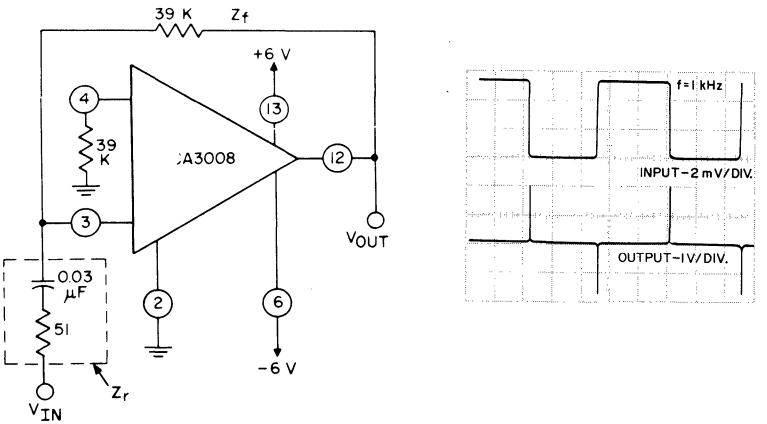


Fig. 190 — Circuit diagram and the input and output waveforms for an operational amplifier used as a differentiator.

ferentiator applications. This 51-ohm resistor limits the high-frequency numerical gain factor of the amplifier to 433.

If the closed-loop gain of a differentiator rises to the open-loop value before the open-loop response has started to roll off, no phase compensation of the circuit is required. In order to assure that the intersection of the closed-loop characteristic with the open-loop response occurs at a slope less than two, the RC time constant of the phase-compensating network must be adjusted so that it does not roll off in the region of the intersection.

Scaling Adders — The inverting feedback configuration of the CA3008 and CA3010 operational amplifiers lends itself not only to summing several different signals, but also to weighting each signal to be summed. The weighting operation is possible because the virtual ground that exists at the junction of the feedback resistor and the inverting input (terminal 3) isolates each signal channel from the others. The weighting operation requires that each input signal enter the virtual-ground node through an impedance of such value that its ratio to the feedback impedance is equal to the desired weighting factor.

Fig. 191 illustrates the use of the CA3008 or CA3010 operational amplifier as a scaling adder (weighting amplifier). This figure also shows a photograph of the output waveform. The minimum phase compensation needed for this circuit is that required for the gain obtained when a single signal drives all the input channels in parallel.

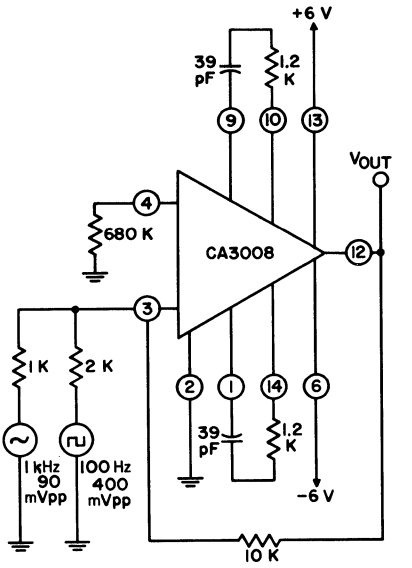
INTEGRATED-CIRCUIT FM IF AMPLIFIERS

The CA3011 and CA3012 wide-band amplifiers and the CA3013 and CA3014 amplifier-discriminators are designed for use in black-and-white or color television receivers or in FM broadcast or communications receivers. The CA3011 and CA3012 are basically if amplifier-limiters intended for use with external FM detectors. The CA3013 and CA3014, however, can provide if amplification, noise limiting, FM detection, and low-level audio amplification in the sound-if section of intercarrier television receivers or in FM receivers without the use of external components other than tuned coupling networks and bypass elements.

Circuit Descriptions

The circuit configurations of the CA3011 and CA3012 are identical; the circuits differ, however, in that the CA3012 is capa-

ble of operation at higher levels of dc voltage and current. Similarly, the CA3013 and CA3014 are identical, except that the CA3014 has higher dc voltage and current ratings.



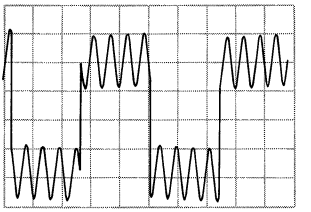


Fig. 191 — Circuit diagram and output waveform obtained when an operational amplifier is used as a scaling adder.

Fig. 192 shows the schematic diagram of the CA3011 or CA3012 wide-band amplifier. The amplifier consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of

an emitter-coupled amplifier and an emitter follower. The operating conditions are selected so that the dc voltage at the output of each stage is identical to that at the input to the stage. This condition is achieved by operation of the bases of the emitter-coupled

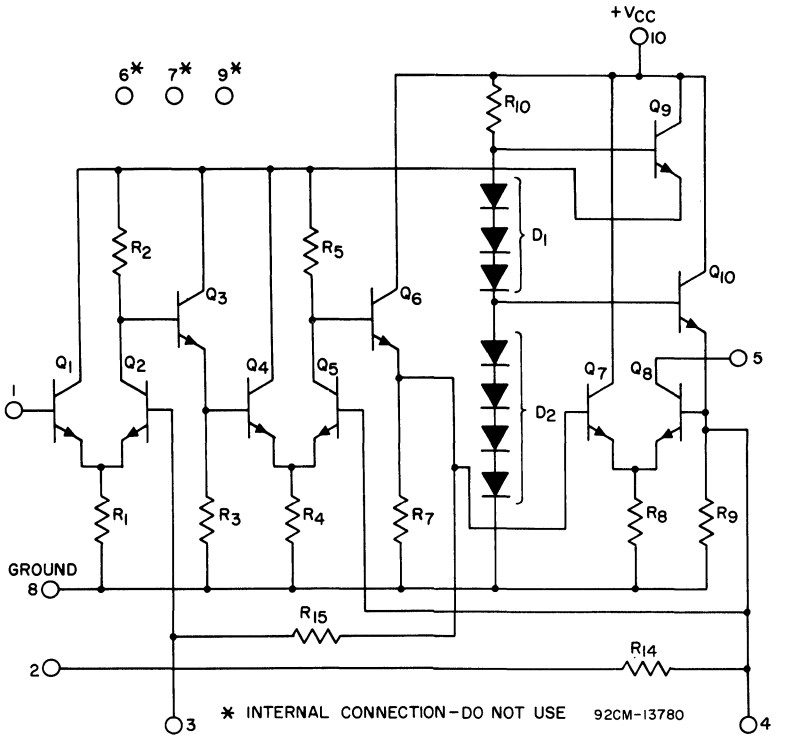


Fig. 192 — Schematic diagram of the CA3011 or CA3012 integrated-circuit wide-band amplifier.

differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor. As a result, the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to V_{BE} plus the common-base potential. The potential at the output of the emitter follower, therefore, is the same as the common-base potential.

Fig. 193 shows the schematic for the CA3013 or CA3014 amplifier-discriminator. Each amplifier-discriminator includes a three-stage, direct-coupled, amplifier-limiter cascade and regulated power supply identical to those in the CA3011 and CA3012 wide-band amplifiers, together with an FM detector and a Darlington

pair low-level audio output stage, on the same silicon chip. The operation of the amplifier-limiter stages and the regulated power supply is identical to that of the wide-band amplifiers.

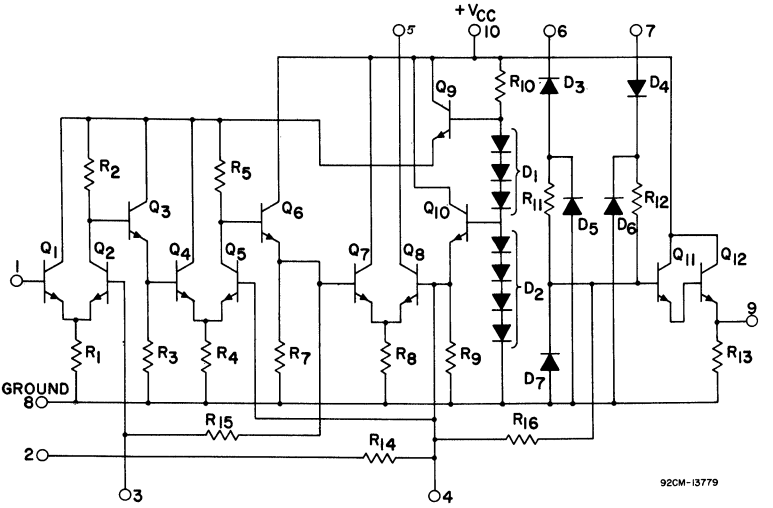


Fig. 193 — Schematic diagram of the CA3013 or CA3014 integrated-circuit amplifier-discriminator.

The FM detector includes all the components required for FM demodulation except the tuned phase-shift transformer. In the design of the integrated detector, the large nonintegrable diode load capacitors conventionally used to obtain peak rectification in balanced phase-shift discriminators and in ratio detectors are eliminated, and average detection is employed with a substantially resistive load. Filtering of the signal frequency and its harmonics is provided by the distributed capacitance of the load resistors; additional filtering is provided by the capacitance of the small reverse-biased diode junctions D_5, D_6, and D_7. The parallel input resistance at the discriminator terminals 6 and 7 is typically 12,000 ohms; the parallel input capacitance at these terminals is typically 7 picofarads.

Characteristics and Applications

The CA3011 and CA3013 are designed to operate at various levels of dc supply voltage up to 7.5 volts. The CA3012 and CA3014, which have higher supply-voltage and dissipation ratings, may be operated at dc supply voltages up to 10 volts. For each circuit, the external dc voltage is applied to terminals 10 and 5; dc voltages required at other terminals are derived from the in-

ternal power supply. When the circuits are operated at the same dc levels, the characteristics of their amplifier-limiter stages are identical. For operation at 7.5 volts with an ac resistive load impedance of 3000 ohms from terminal 5 to ground, the output voltage at terminal 5 with respect to ground is typically 3 volts peak-to-peak. Figs. 194 through 199 show the significant characteristics of the FM-if amplifier integrated circuits.

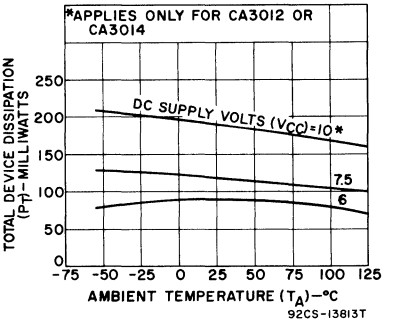


Fig. 194 — Total dissipation as a function of temperature.

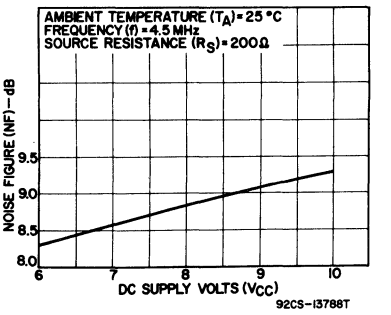


Fig. 195 — Noise figure as a function of dc supply voltage.

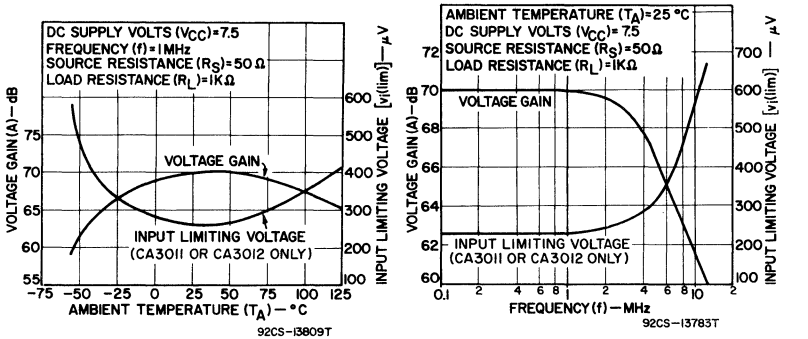


Fig. 196 — Voltage gain and input limiting voltage as a function of temperature and of frequency in test circuit shown.

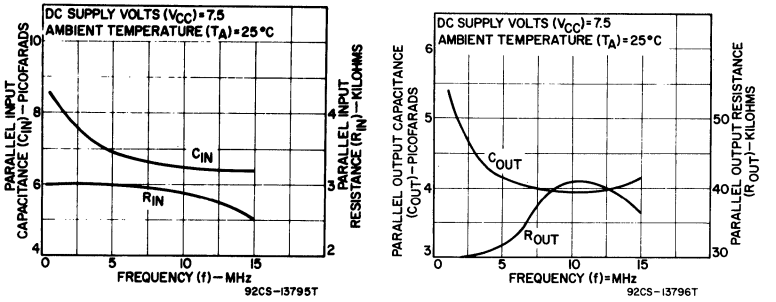


Fig. 197 — Input and output impedance as a function of frequency.

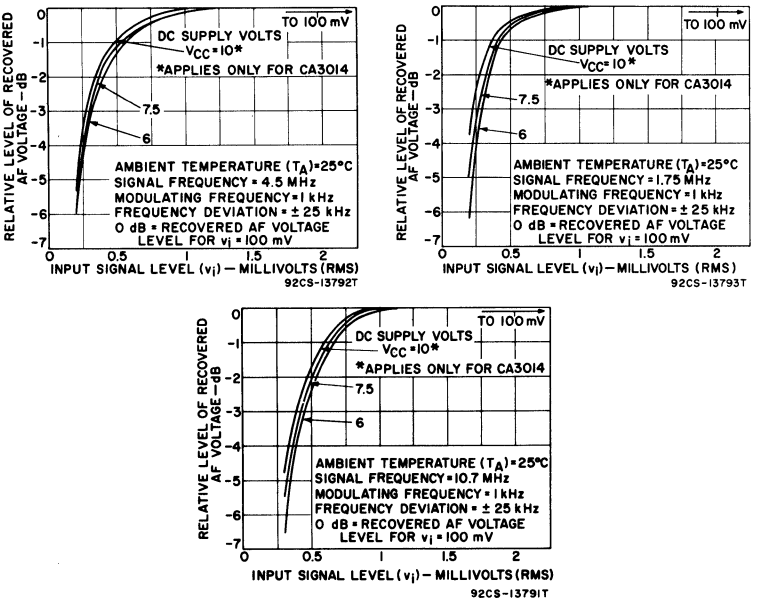


Fig. 198 — Input limiting voltage (knee) and recovered audio-frequency voltage for operation of amplifier-discriminator at 1.75, 4.5, and 10.7 MHz.

The performance of the integrated circuits in the FM sound channel of intercarrier television receivers and in the if amplifier-limiter-detector channel of FM radio receivers is at least equal to that of conventional circuits in every characteristic, and is superior in many of them. In particular, the AM rejection ratio (more than 50 dB) of the integrated circuits is so large that it cannot be measured with commercial FM-AM signal generators because of

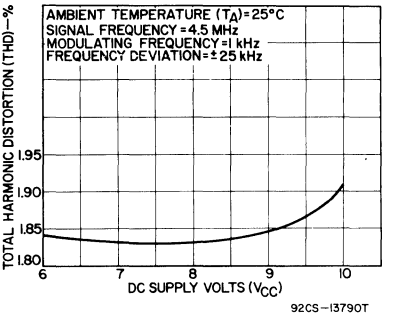


Fig. 199 — Total harmonic distortion as a function of dc supply voltage.

incidental phase modulation of the generators. The block diagram in Fig. 200 shows the use of the CA3013 or CA3014 amplifier-discriminator in the sound channel of an intercarrier television receiver. (Details of discriminator transformer shown in Fig. 200 are given in Fig. 201.) Fig. 202 shows the use of the CA3011 or CA3012 wide-band amplifier in the 10.7-MHz if-amplifier channel of an FM broadcast receiver.

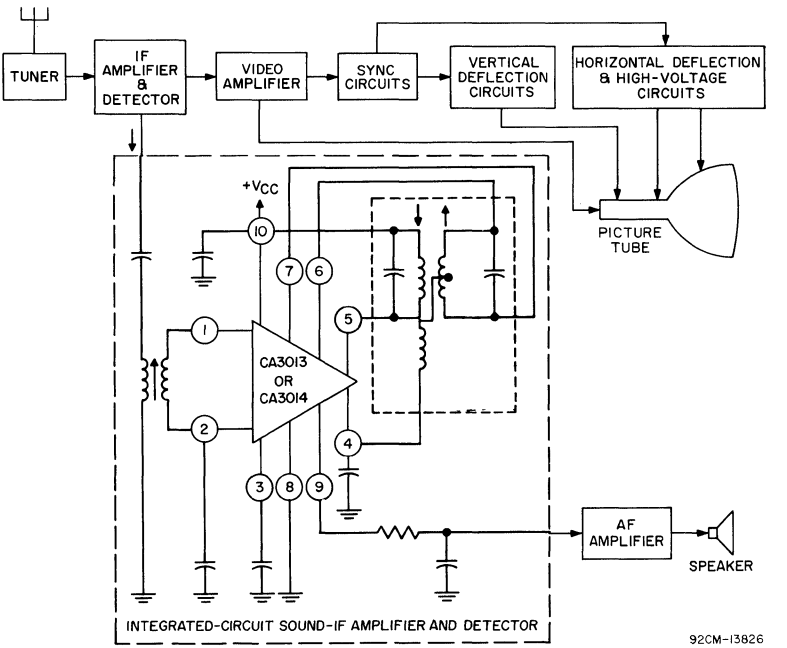
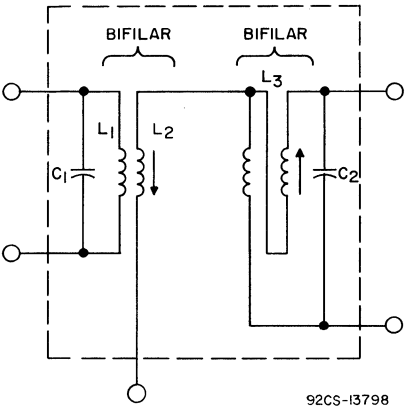


Fig. 200 — Block diagram of typical television receiver using CA3013 or CA3014 integrated-circuit sound if amplifier and detector section.



Discriminator-Transformer Construction Details

Coil-form outside diameter = 7/32 inch.
Slugs: Radio Industries, Inc., Type "E" material, or equiv.
Wire Type: GRIPEZE,* or equiv.

f MHz	Size AWG#	Turns L_1▲	L_2▲	L_3▼	C_1 pF	C_2 pF
1.75	36	44	20	44 total	820	820
4.5▪	40	18	7	22 total	560	330
10.7•	36	18	18	18 total	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products
▲ Wound bifilar
▼ Two sections bifilar wound; bifilar turns = ½ total turns
▪ At this frequency, TRW Type No. 21685, or equiv., may be used for discriminator transformer
• At this frequency, TRW Type No. 21590-R1, or equiv., may be used for discriminator transformer.

Fig. 201 — Details of discriminator transformer shown in Fig. 200.

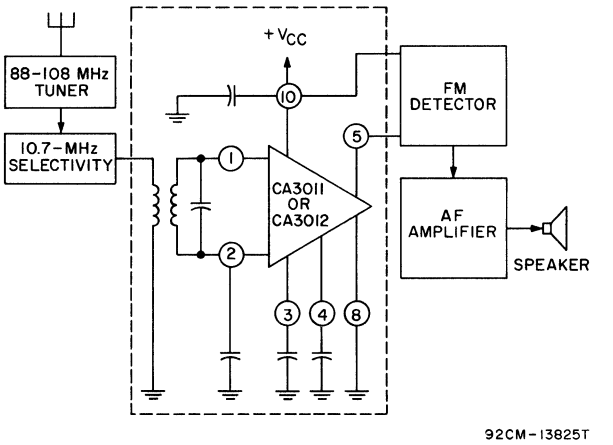


Fig. 202 — Block diagram of typical FM receiver using CA3011 or CA3012 integrated-circuit wide-band amplifier.

Index

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