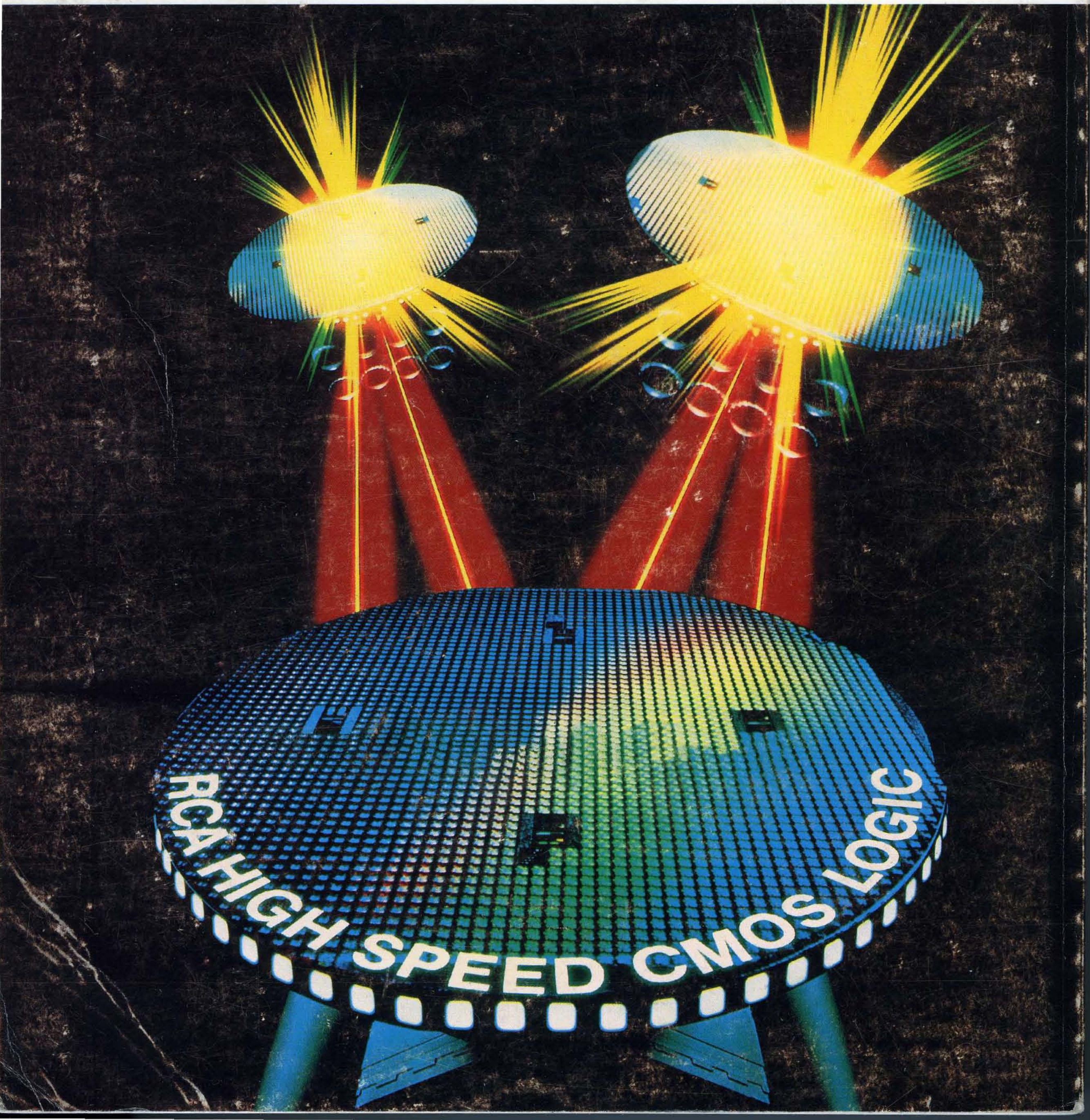
RCA Solid State

DATABOOK



RCA High-Speed CMOS Logic Integrated Circuits

The RCA HC/HCT series of high-speed CMOS logic integrated circuits include an extensive line of products that are pin compatible with many existing bipolar 54/74 LSTTL and CMOS 4000 series of digital logic types. The new HC/HCT series IC's provide high-speed CMOS replacements for the most popular LSTTL devices in existing designs and also offer low-power all-CMOS designs for new digital systems. Key family features of the RCA HC/HCT types include:

- Speeds equivalent to LSTTL types with typical gate delays of 8 ns.
- Fanout to 10 74 LSTTL loads; 15 loads using Bus Driver 54/74 types.
- Operating frequencies equivalent to LSTTL types, typically 50 MHz.
- The high voltage noise immunity characteristic of CMOS, typically 45 percent of Vcc, a two to three times improvement over LSTTL. (HC-Series types.)
- Wide range of power supply operating voltages, 2 to 6 volts.
- CMOS low static power consumption, typically less than 1 microwatt.

With the broad line of CMOS MSI function types currently available, together with performance offered by the RCA HC/HCT series of high-speed CMOS integrated circuits, the designer need not sacrifice speed for power consumption. Add the other classical advantages of CMOS, including high noise immunity and wide power supply and temperature ranges, and the decision to use high-speed CMOS logic is the choice for the 80's. This family provides for the design of more cost-effective systems to serve high-speed market applications.

The RCA product line consists of CD54/74HC-series types, which feature CMOS input voltage level compatibility and CD54/74HCT-series types, which are input voltage level compatible with LSTTL devices. The line also includes a limited number of single-stage, unbuffered inverter types (CD54/74HCU-series) for added versatility in oscillator and amplifier applications.

A general information section defines the distinguishing characteristics of each product series and provides characteristic data and classification and selection charts.

The data pages include a description, special features, truth tables and/or timing diagrams, and significant dynamic electrical characteristics.

The data sections are followed by a Dimensional Outlines section.

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When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.

The device data shown for some types are indicated as product preview or advance information/preliminary data. **Product preview** data are intended for engineering evaluation of product under development. The type designations and data are subject to change or withdrawal, unless otherwise arranged. **Advance information/preliminary** data are intended for guidance purposes in evaluating new product for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. No obligations are assumed for notice of change of these devices. For current information on the status of product preview or advance information/preliminary data programs, please contact your local RCA sales office.

Printed in USA/10-86

Product Selectors

Index to Devices

CMOS Logic		TTL Logic				
Plastic Pkg.	CERDIP	Plastic Pkg.	CERDIP	Page	Description	Pins
CD74HC00E,M	CD54HC00F	CD74HCT00E,M	CD54HCT00F	48	Quad 2-Input NAND Gate	14
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Note: Add package suffix code to part number on all orders.
E = Dual-In-Line Plastic Package — Temp. Range = -40° to + 85°C.
F = Dual-In-Line Frit-Seal Ceramic Package (CERDIP) — Temp. Range = -55° to + 125°C.
H = Chip — Temp. Range = -55° C to 125°C.
M = Dual-In-Line Surface Mounted Package — Temp. Range = -40° to + 85° C.

Product Selection Guide

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HC/HCT02	Quad 2-Input NOR Gate	SSI	52
HC/HCT03	Quad 2-Input NAND Gate with Open Drain	SSI	56
HC/HCT10	Triple 3-Input NAND Gate	SSI	68
HC/HCT20	Dual 4-Input NAND Gate	SSI	80
HC/HCT27	Triple 3-Input NOR Gate	SSI	88
HC/HCT30	8-Input NAND Gate	SSI	92
HC/HCT4002	Dual 4-Input NOR Gate	SSI	462
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HC/HCT11	Triple 3-Input AND Gate	SSI	72
HC/HCT21	Dual 4-Input AND Gate	SSI	84
HC/HCT32	Quad 2-Input OR Gate	SSI	96
HC/HCT86	Quad 2-Input EXCLUSIVE-OR Gate	SSI	125
HC/HCT4075	Triple 3-Input OR Gate	SSI	548
HC7266	Quad Exclusive NOR Gate	SSI	600
	Inverters/Buffers/Bus Drivers		
HC/HCT04	Hex Inverter/Buffer	SSI	60
HCU04	Hex Inverter (Unbuffered)	SSI	628
HC/HCT125*	Quad 3-State Buffer	MSI	155
HC/HCT126*	Quad 3-State Buffer	MSI	160
HC/HCT240*	Octal Buffer/Line Driver; 3-State; Inverting	MSI	298
HC/HCT241*	Octal Buffer/Line Driver; 3-State	MSI	298
HC/HCT244*	Octal Buffer/Line Driver; 3-State	MSI	298
HC/HCT365*	Hex Buffer/Line Driver; 3-State	MSI	380
HC/HCT366*	Hex Buffer/Line Driver; 3-State Inverting	MSI	380
HC/HCT367*	Hex Buffer/Line Driver; 3-State	MSI	385
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting	MSI	385
HC/HCT540*	Octal Buffer/Line Driver; 3-State; Inverting	MSI	429
HC/HCT541*	Octal Buffer/Line Driver; 3-State	MSI	429
HC4049	Hex Inverting HIGH-to-LOW Level Shifter	SSI	510
HC4050	Hex HIGH-to-LOW Level Shifter	SSI	510
	Flip-Flops		
HC/HCT73	Dual JK Flip-Flop with Reset; Negative-Edge Trigger	FF	104
HC/HCT74	Dual D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger	FF	109
HC/HCT107	Dual JK Flip-Flop with Reset; Negative-Edge Trigger	FF	134
HC/HCT109	Dual JK Flip-Flop with Set and Reset; Positive-Edge Trigger	FF	139
HC/HCT112	Dual JK Flip-Flop with Set and Reset; Negative-Edge Trigger	FF	144
HC/HCT173*	Quad D-Type Flip-Flop with Set and Reset; Positive-Edge Trigger; 3-State	MSI	232
HC/HCT174	Hex D-Type Flip-Flop with Reset; Positive-Edge Trigger	MSI	238
HC/HCT175	Quad D-Type Flip-Flop with Reset; Positive-Edge Trigger	MSI	243
HC/HCT273	Octal D-Type Flip-Flop with Reset; Positive-Edge Trigger	MSI	342
HC/HCT374*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State	MSI	396
HC/HCT377	Octal D-Type Flip-Flop with Data Enable; Positive-Edge Trigger	MSI	401
HC/HCT534*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting	MSI	424
HC/HCT564*	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting	MSI	424
HC/HCT574*	Octal D-Type Flip-Flop; Positive-Edge; 3-State	MSI	396
	Shift/FIFO Buffer/Multiport Registers		
HC/HCT164	8-Bit Serial-In/Parallel-Out Shift Register	MSI	215
HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register	MSI	220
HC/HCT166	8-Bit Parallel/Serial-In Serial-Out Shift Register	MSI	226
HC/HCT194	4-Bit Bidirectional Universal Shift Register	MSI	279
HC/HCT195	4-Bit Parallel Access Shift Register	MSI	285
HC/HCT299*	8-Bit Universal Shift Register; 3-State	MSI	363
HC/HCT597	8-Bit Shift Register with Input Storage	MSI	636
HC/HCT670*	4 x 4 Register File; 3-State	MSI	451
HC/HCT4015	Dual 4-Stage Static Shift Register	MSI	466
HC/HCT4094	8-Stage Shift-and-Store Bus Register; 3-State	MSI	552
HC/HCT7030*	9-Bit x 64 Word FIFO Register; 3-State	MSI	640
HC/HCT40104*	4-Bit Bidirectional Universal Shift Register; 3-State	MSI	613
HC/HCT40105	4 Bits x 16 Words FIFO Register	MSI	619

*Types with a bus driver output stage.

Product Selection Guide (Cont'd)

Type	Function/Description	Classification	Page
CD54/74	**Arithmetic Circuits**		
HC/HCT85	4-Bit Magnitude Comparator	MSI	119
HC/HCT181	4-Bit Arithmetic Logic Unit	MSI	248
HC/HCT182	Look-Ahead Carry Generator	MSI	254
HC/HCT280	9-Bit Odd/Even Parity Generator/Checker	MSI	347
HC/HCT283	4-Bit Full Adder with Fast Carry	MSI	351
HC/HCT583	4-Bit BCD Full Adder with Fast Carry	MSI	434
HC/HCT688	8-Bit Magnitude Comparator	MSI	458
	Counters		
HC/HCT93	4-Bit Binary Ripple Counter	MSI	129
HC/HCT160	Presettable Synchronous BCD Decade Counter; Asynchronous Reset	MSI	205
HC/HCT161	Presettable Synchronous 4-Bit Binary Counter; Asynchronous Reset	MSI	205
HC/HCT162	Presettable Synchronous BCD Decade Counter; Synchronous Reset	MSI	205
HC/HCT163	Presettable Synchronous 4-Bit Binary Counter; Synchronous Reset	MSI	205
HC/HCT190	Presettable Synchronous BCD Decade Up/Down Counter	MSI	260
HC/HCT191	Presettable Synchronous 4-Bit Binary Up/Down Counter	MSI	260
HC/HCT192	Presettable Synchronous BCD Decade Up/Down Counter	MSI	269
HC/HCT193	Presettable Synchronous 4-Bit Binary Up/Down Counter	MSI	269
HC/HCT390	Dual Decade Ripple Counter	MSI	407
HC/HCT393	Dual 4-Bit Binary Ripple Counter	MSI	413
HC/HCT4017	Decade Counter/Divider with 10 Decoded Outputs	MSI	472
HC/HCT4020	14-Stage Binary Ripple Counter	MSI	478
HC/HCT4024	7-Stage Binary Ripple Counter	MSI	483
HC/HCT4040	12-Stage Binary Ripple Counter	MSI	488
HC/HCT4059	Programmable Divide by "N" Counter	MSI	523
HC/HCT4060	14-Stage Binary Ripple Counter with Oscillator	MSI	530
HC/HCT4510	Up/Down Counter, BCD	MSI	559
HC/HCT4516	Up/Down Counter, Binary	MSI	559
HC/HCT4518	Dual Synchronous BCD Counter	MSI	580
HC/HCT4520	Dual 4-Bit Synchronous Binary Counter	MSI	580
HC/HCT40102	8-Bit Synchronous BCD Down Counter	MSI	604
HC/HCT40103	8-Bit Binary Down Counter	MSI	604
	Analog and Digital Multiplexers/Demultiplexers		
HC/HCT151	8-Input Multiplexer	MSI	184
HC/HCT153	Dual 4-Input Multiplexer	MSI	189
HC/HCT157	Quad 2-Input Multiplexer	MSI	200
HC/HCT158	Quad 2-Input Multiplexer; Inverting	MSI	200
HC/HCT251	8-Input Multiplexer; 3-State	MSI	315
HC/HCT253*	Dual 4-Input Multiplexer; 3-State	MSI	321
HC/HCT257*	Quad 2-Input Multiplexer; 3-State; Non-Inverting Outputs	MSI	326
HC/HCT258	Quad 2-Input Multiplexer; 3-State; Inverting Outputs	MSI	330
HC/HCT354*	8-Input Multiplexer/Register; 3-State	MSI	370
HC/HCT356*	8-Input Multiplexer/Register; 3-State	MSI	370
HC/HCT4051	8-Channel Analog Multiplexer/Demultiplexer	MSI	514
HC/HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	MSI	514
HC/HCT4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	MSI	514
HC/HCT4067	16-Channel Analog Multiplexer/Demultiplexer	MSI	542
HC/HCT4351	Analog Multiplexer with Latch	MSI	638
HC/HCT4352	Analog Multiplexer with Latch	MSI	639
HC/HCT4353	Analog Multiplexer with Latch	MSI	639
	Decoders/Encoders		
HC/HCT42	BCD to Decimal Decoder (1-of-10)	MSI	100
HC/HCT137	3-to-8 Line Decoder with Latch; Inverting	MSI	634
HC/HCT138	3-to-8 Line Decoder/Demultiplexer; Inverting	MSI	169
HC/HCT139	Dual 2-to-4 Line Decoder/Demultiplexer	MSI	174
HC/HCT147	10-to-4-Line Priority Encoder	MSI	179
HC/HCT154	4-to-16-Line Decoder/Demultiplexer	MSI	194
HC/HCT237	3-to-8-Line Decoder/Demultiplexer with Address Latches	MSI	635
HC/HCT238	3-to-8-Line Decoder/Demultiplexer	MSI	169
HC/HCT4511	BCD-to-7-Segment Latch/Decoder/Driver	MSI	569
HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latches	MSI	574
HC/HCT4515	4-to-16-Line Decoder/Demultiplexer with Input Latches	MSI	574
HC/HCT4543	BCD-to-7-Segment Latch/Decoder/Driver for LCDs	MSI	594

*Types with a bus driver output stage.

Product Selection Guide (Cont'd)

Type	Function/Description	Classification	Page
CD54/74	**Analog Switches**		
HC/HCT4016	Quad Bilateral Switch	SSI	637
HC/HCT4066	Quad Bilateral Switch	SSI	536
HC/HCT4316	Quad Analog Switch	MSI	638
	Bus Transceivers		
HC/HCT242*	Quad Bus Transceiver; 3-State; Inverting	MSI	304
HC/HCT243*	Quad Bus Transceiver; 3-State	MSI	304
HC/HCT245*	Octal Bus Transceiver; 3-State	MSI	310
HC/HCT640*	Octal Bus Transceiver; 3-State Inverting	MSI	439
HC/HCT643*	Octal Bus Transceiver; 3-State True/Inverting	MSI	439
HC/HCT646*	Octal Bus Transceiver; 3-State	MSI	444
HC/HCT648*	Octal Bus Transceiver; 3-State; Inverting	MSI	444
HC/HCT7038*	9-Bit Bus Transceiver with Latch	MSI	641
	Schmitt Triggers		
HC/HCT14	Hex Inverting Schmitt Trigger	SSI	76
HC/HCT132	Quad 2-Input NAND Schmitt Trigger	SSI	165
	Latches		
HC/HCT75	Dual 2-Input Bistable Transparent Latch	FF	114
HC/HCT259	8-Bit Addressable Latch	MSI	335
HC/HCT373*	Octal Transparent Latch; 3-State	MSI	390
HC/HCT533*	Octal Transparent Latch; 3-State; Inverting	MSI	418
HC/HCT563*	Octal Transparent Latch; 3-State; Inverting	MSI	418
HC/HCT573*	Octal Transparent Latch; 3-State	MSI	390
	One-Shot Multivibrators		
HC/HCT123	Dual Retriggerable Monostable Multivibrator with Reset	MSI	149
HC/HCT221	Dual Monostable Multivibrator with Reset	MSI	291
HC/HCT423	Dual Retriggerable Monostable Multivibrator with Reset	MSI	149
HC/HCT4538	Dual Retriggerable Precision Monostable Multivibrator	MSI	586
	Phase-Locked Loops (PLL)		
HC/HCT297	Digital Phase-Locked Loop Filter	MSI	356
HC/HCT4046A	Phase-Locked Loop with VCO	MSI	493
HC/HCT7046	Phase-Locked Loop with In-Lock Detection	MSI	641

*Types with a bus driver output stage.

Product Classification Chart

GATES								MULTIVIBRATORS	
Single-level			Multi-level					Flip-Flops/Latches	
NOR/NAND		OR/AND	Buffers Line-Drivers	Bus Drivers	Multi-function AOI	Decoders/ Encoders	Schmitt Trigger	Flip-Flops	Latches
CD54/74HC/HCT			CD54/74/HC/HCT					CD54/74HC/HCT	
HC/HCT02	HC/HCT00	HC/HCT08	HC/HCT240●	HC/HCT125	HC/HCT86	HC/HCT42	HC/HCT14	HC/HCT73	HC/HCT75
HC/HCT03†	HC/HCT10	HC/HCT11	HC/HCT241●	HC/HCT126	HC7266	HC/HCT137	HC/HCT132	HC/HCT74	HC/HCT259
HC/HCT27	HC/HCT20	HC/HCT21	HC/HCT244●	HC/HCT241		HC/HCT138		HC/HCT107	HC/HCT373●
HC/HCT4002	HC/HCT30	HC/HCT32	HC/HCT365●	HC/HCT244		HC/HCT139		HC/HCT109	HC/HCT533●
		HC/HCT4075	HC/HCT366●	HC/HCT365		HC/HCT147		HC/HCT112	HC/HCT563●
			HC/HCT367●	HC/HCT366		HC/HCT154		HC/HCT173●	HC/HCT573●
			HC/HCT368●	HC/HCT367		HC/HCT237		HC/HCT174	
			HC/HCT540●	HC/HCT368		HC/HCT238		HC/HCT175	
			HC/HCT541●	HC/HCT540		HC/HCT4511		HC/HCT273	Monostable
				HC/HCT541		HC/HCT4514		HC/HCT374●	HC/HCT123
			Level Shifters	Inverters		HC/HCT4515		HC/HCT377	HC/HCT221
								HC/HCT534●	HC/HCT423
			HC 4049	HC/HCT04				HC/HCT564●	HC/HCT4538
			HC 4050	HCU04				HC/HCT574●	

REGISTERS			COUNTERS		DIGITAL MULTIPLEXERS	PHASE LOCKED LOOPS	BILATERAL SWITCHES	INTERFACE CIRCUITS
Shift	FIFO Buffer	Multiport	Binary Ripple	Synchronous				
CD54/74HC/HCT			CD54/74HC/HCT				CD54/74HC/HCT	
HC/HCT164	HC/HCT40105	HC/HCT670	HC/HCT93	HC/HCT160	HC/HCT151	HC/HCT279	HC/HCT4016 ▲	Bus Transceivers
HC/HCT165	HC/HCT7030		HC/HCT390	HC/HCT161	HC/HCT153	HC/HCT4046A	HC/HCT4066 ▲	
HC/HCT166			HC/HCT393	HC/HCT162	HC/HCT157	HC/HCT7046	HC/HCT4316 ▲	HC/HCT242●
HC/HCT194			HC/HCT4020	HC/HCT163	HC/HCT158		Analog Multiplexers/ Demultiplexers	HC/HCT243●
HC/HCT195			HC/HCT4024	HC/HCT190	HC/HCT251			HC/HCT245●
HC/HCT299●			HC/HCT4040	HC/HCT191	HC/HCT253			HC/HCT640●
HC/HCT597			HC/HCT4060	HC/HCT192	HC/HCT257●		HC/HCT4051	HC/HCT643●
HC/HCT4015			HC/HCT40103	HC/HCT193	HC/HCT258		HC/HCT4052	HC/HCT646●
HC/HCT4094				HC/HCT4017	HC/HCT354●		HC/HCT4053	HC/HCT648●
HC/HCT40104●				HC/HCT4510	HC/HCT356●		HC/HCT4067	HC/HCT7038●
				HC/HCT4516			HC/HCT4351	
				HC/HCT4518			HC/HCT4352	
				HC/HCT4520			HC/HCT4353	
				HC/HCT40102				

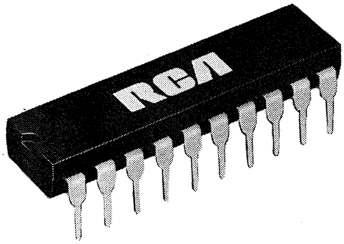
ARITHMETIC CIRCUITS			DISPLAY DRIVERS	
Adders/ Comparators	ALU/Rate Multipliers	Parity Generator/ Checker	For LCD Drive	For LED Drive
CD54/74HC/HCT			CD54/74HC/HCT	
HC/HCT85	HC/HCT181	HC/HCT280	HC/HCT4543	HC/HCT4511
HC/HCT283	HC/HCT182		See Decoders/ Encoders	

† Open Drain

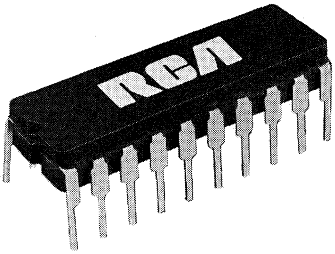
▲ Quad type

● With Bus Driver output stage

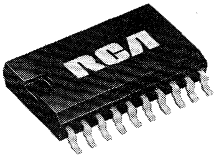
Typical Dual-In-Line
Plastic Package



Typical Dual-In-Line
Frit-Seal Ceramic (CERDIP) Package



Typical SO (Small Outline)
Plastic Package



Technical Overview

HC/HCT Family Description

The RCA HC/HCT series of high-speed CMOS integrated circuits (QMOS) includes a functionally complete set of LSTTL equivalent types and selected equivalent CMOS CD4000 series types. The CD4000 series types selected are unique to the CMOS process. These types are readily produced by the highly versatile CMOS technology, but cannot be implemented by the more restrictive bipolar technology. Each CMOS circuit function is offered in two basic logic series, as follows:

1. **CD54/74HCTXXXX-series types** — feature LSTTL input-voltage-level compatibility and provide high-speed CMOS direct drop-in replacements of LSTTL devices.
2. **CD54/74HCXXXX-series types** — feature CMOS input-voltage-level compatibility and are intended for use in new second-generation all-CMOS systems.

In addition, RCA offers a third category, **CD54/74HCUXX,** which includes unbuffered types intended for linear or high-speed oscillator applications.

The HC/HCT family consists of a comprehensive set of buffers, transceivers, and registers that are popular in computer systems. A wide variety of popular logic, MUX's, encoders/decoders, counters, arithmetic units, mulitvibrators, display drivers, and phase-lock loops complete the family.

Shown below is a breakdown of the HC/HCT family by logic function:

The HC/HCT Family

Device Function	Number of Types
Inverters/Buffers/Bus Drivers	14
Flip-Flops/Latches	20
Bus Transceivers	8
Registers	13
Counters	23
Decoders/Encoders	12
Multiplexers (Analog & Digital)	17
Multivibrators	4
Schmitt Triggers	2
Phase-Lock Loops	3
Bilateral Switches	3
Arithmetic Circuits	7
Gates	15

NOTE: Each function is available in both an HCT and HC version.

HC/HCT Family Features

- Functionally and pin compatible with industry 54 and 74 LSTTL-series and CD4000B-series types.
- CMOS outputs for maximum noise margins.
- Fan-out (over temperature):
  Standard Outputs - 10 LSTTL loads
  Bus-Driver Outputs - 15 LSTTL loads
- Wide operating temperature range:
  CD74HC/HCT/HCU: -40 to +85° C
  CD54HC/HCT/HCU: -55 to +125° C
- Balanced propagation and transition times.
- Significant power reduction compared to LSTTL logic.
- Alternate source - Philips/Signetics

Series Features

CD54HCXXXX and CD74HCXXXX Series

- 2 to 6V operation.
- High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ at $V_{CC} = 5V$.

CD54HCTXXXX and CD74HCTXXXX Series

- 4.5 to 5.5V operation.
- Direct LSTTL input logic compatibility
  $V_{IL} = 0.8V$(max), $V_{IH} = 2.0V$ (min)
- CMOS input compatibility
  I_{IL}, $I_{IH} \leq$ luA at V_{OL}, V_{OH}

Quantitative Comparison of HC/HCT and LSTTL Logic Types

RCA's HC and HCT logic types have many outstanding advantages when compared with the conventional high-current LSTTL logic types which these types can replace in existing and new equipment designs that require devices operating at frequencies in the 20-30 MHz range. Table I compares significant operating characteristics of the HC/HCT vs. LSTTL logic families.

Table I — Quantitative Comparison of HC/HCT and LSTTL Logic Types

Characteristic	74 Series HC/HCT	74 Series LSTTL
1. Quiescent Power		
-per Gate	0.025mW	5.5mW
-per FF	0.05mW	10mW
-4 Stage Counter	0.4mW	95mW
-per Transceiver/Buffer	0.1mW	60mW

2. Operating Power	Frequency			Frequency	
	0.1MHz	1MHz	10MHz	0.1 to 1MHz	10MHz
-per Gate	0.2mW	2mW	20mW	5.5mW	20mW
-per FF	0.15mw	1.5mW	15mW	10mW	15mW
-4 Stage Counter	0.24mW	2.4mW	24mW	95mW	120mW
-per Transceiver/ Buffer	0.25mW	2.5mW	25mW	60mW	90mW

Characteristic	74 Series HC/HCT	74 Series LSTTL
3. Operating Supply Voltage	(HCT) 4.5V to 5.5V (HC) 2V to 6V	4.75V to 5.25V
4. Operating Temperature Range	-40° C to +85° C	0° C to +70° C
5. Noise Margin @ 5V		
LS to LS	----	0.7V/0.4V
HC to HC (HI/LOW)	1.4V/1.4V	----
HCT to HCT	2.9V/0.7V	----
6. Input Switching Voltage Variation with Temp.	Vs ± 60mV	Vs ± 200 mV

Table I — Cont'd

	74 Series HC/HCT	74 Series LSTTL
7. Output Drive Current		
a) Source Current at		
$V_{OH} = 2.4V$	-8mA	-400uA
b) Sink Current		
Std. Logic (V_{OL})	4mA (0.33V)	4mA (0.4V)
BUS Logic (V_{OL})	6mA (0.33V)	12mA (0.4V)
V_{OL}=0.5V	12mA	24mA
8. Typ. Output Transition Time*		
t_{TLH}	6ns	15ns
t_{THL}	6ns	6ns
9. Typical Gate Propagation Delay*: t_{PHL}/t_{PLH} $V_{CC} = 5V$, $C_L = 15pF$	8ns/8ns	8ns/11ns
10. Typical FF Propagation Delay: $V_{CC} = 5V$, $C_L = 15pF$		
t_{PLH}	14ns	15ns
t_{PHL}	14ns	22ns
11. Typ. Clock Rate of an FF	50MHz	33MHz
12. Input Current		
I_{IL}	-1uA	-0.4. to -0.8mA
I_{IH}	1uA	40uA
13. 3-State Output Leakage Current	±5uA	±20uA
14. Reliability		
%/1000 hours at 60% Confidence	.0019 (RCA Report)	.008 (RADC Report)

*Loading coefficient = 0.055ns/pF (both HC/HCT and LSTTL)

HC/HCT IC Structure

The high speeds and low quiescent power dissipation that characterize the RCA HC/HCT family are made possible by utilizing a three-micron, self-aligned silicon gate CMOS process. The three-micron process minimizes the internal parasitic capacitances of the circuit, which results in increased switching speed.

The polysilicon gates of the transistors are deposited over a thin gate oxide before the source and drain diffusions are defined. Ion implantation is then used to form the source and drain areas, with the polysilicon gates acting as a mask for the implantation. The source and drain are automatically aligned to the gate, hence the expression "self-aligned-gate" process. In this manner, gate-to-source and gate-to-drain capacitances are minimized. Junction capacitances, which are proportional to the junction area, are also reduced because of the shallower diffusions. Fig. 1 shows the parasitic capacitances in a CMOS inverter.

In contrast, the source and drain areas in a metal-gate CMOS process are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. These conditions result in higher overlap capacitances than those present in QMOS devices. The metal-gate process also employs deeper diffusions than those in the QMOS process and, consequently, has larger junction capacitances.

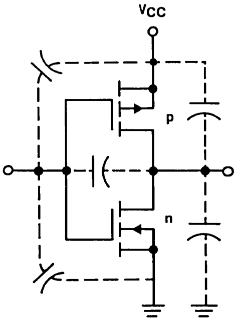


Fig. 1 - Parasitic capacitances in a CMOS inverter

The QMOS structure features a three-micron gate length; the CD4000 series structure has a gate length of seven microns. The equation for the drain current of a MOSFET is:

$$I_{DS} = K'\frac{\text{width}}{\text{length}}[\text{(gate voltage) - (threshold voltage)}]^2$$

where K' is the "beta" of the MOSFET. Therefore, a shorter gate length results in higher drive capability, which in turn increases the speed at which a transistor can charge or discharge capacitance.

The polysilicon in a silicon-gate process is also an interconnect layer, thus, there are three levels of interconnect (diffusion, polysilicon, and metal) instead of the two layers (diffusion and metal) present in a metal-gate process. This situation aids in making a more compact die. Fig. 2 compares the cross sections of the seven-micron metal-gate CMOS structure and the three-micron QMOS structure.

Input Characteristics

The inputs of QMOS devices are voltage-level sensitive, and do not require current, except for input leakage. The definitive switching characteristics for the HC and HCT versions are illustrated in Figs. 3 and 4, respectively.

System designers require the actual MIN/MAX range of expected input switching voltage over the temperature range of -55°C to +125°C. This vital information is contained in the curves of Figs. 5 and 6 for the HC and HCT families, respectively.

The unbuffered HCU04 hex inverter has one stage of active inverting logic from input to output and, therefore, is a special case for input switching voltage as shown in Fig. 7.

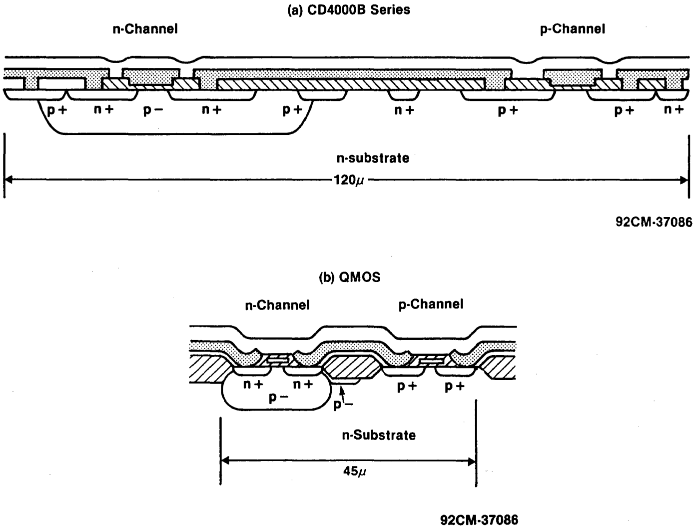


Fig. 2 - Crossectional view of (a) the seven-micron CD4000B Series structure and (b) three-micron QMOS structure

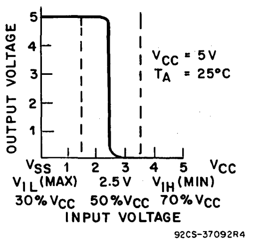


Fig. 3 - Typical switching characteristics of RCA HC series types

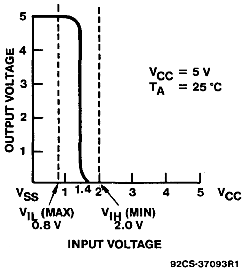


Fig. 4 - Typical switching characteristics of RCA HCT series types

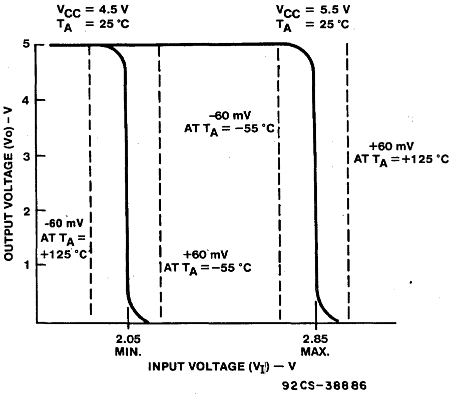


Fig. 5 - Actual Min/Max switching characteristics of RCA HC series types

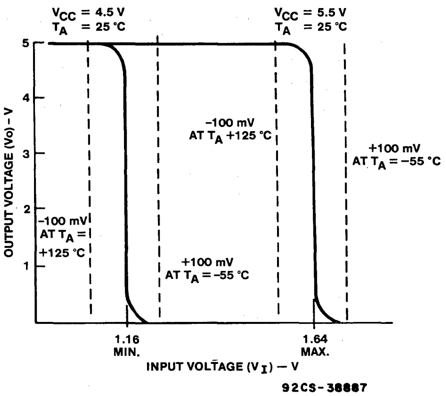


Fig. 6 - Actual Min/Max switching characteristics of RCA HCT series types

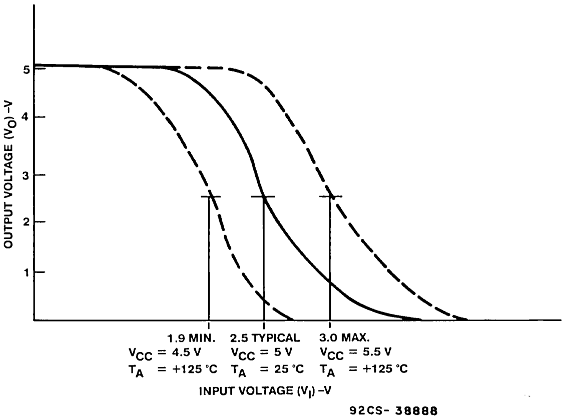


Fig. 7 Actual Min/Max and typical switching characteristics of the HCU04 Unbuffered Hex Inverter

Noise Immunity and Noise Margin

Table II shows the HC, HCT, and HCU input noise immunity and noise margin for use in those applications where like members of the HC, HCT, and HCU families interface with each other at a nominal supply voltage of 5V. Output voltages are also shown.

Table II(a): Noise Immunity and Noise Margin (V_{CC} = 5V).

	HC	HCT	HCU
V_{IL} max.	1.5V	0.8V	1V
V_{IH} min.	3.5V	2V	4V
V_{OL} max.	0.1V	0.1V	0.5V
V_{OH} min.	4.9V	4.9V	4.5V
Noise Margin Low (V_{NML})	1.4V	0.7V	0.5V
Noise Margin High (V_{NMH})	1.4V	2.9V	0.5V

Table II(b) shows noise immunity and noise margin voltages for standard HCT devices interfacing with LSTTL logic types with a fully loaded HCT or LSTTL output at V_{CC} = 4.5V, and a temperature range of 0°C to +70°C. This limited LSTTL temperature range is the only convenient temperature range when using LSTTL characteristics.

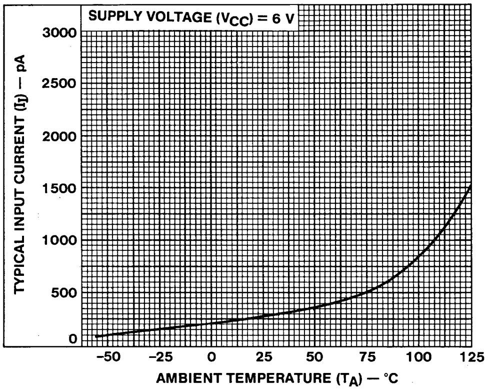
Whenever the HCT output drives either an LS or HCT input, there is an improvement in noise margin over the LSTTL family driving itself or driving HCT. This improvement is especially true for noise margin high where the superior output sourcing current of the rail-to-rail QMOS output swing is far superior to the limited totem-pole pull-up output voltage of LSTTL

Input Current

Fig. 8 is a plot of typical HC/HCT device input current vs. temperature for a V_{CC} of 6V. This actual performance of under 1.5nA over the temperature range of -55°C to +125°C contrasts with maximum family and JEDEC standard input leakage current limit of 100nA for T = -55°C to +25°C, and a limit of 1μa at T_A = 85°C and +125°C. The reason for this difference in performance vs. ratings is high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the limits are end-of-life, thus allowing some leakage current shift due to minor externally introduced foreign material or moisture.

Table II(b) - Noise Immunity and Noise Margin for HCT and LS Device Interfacing

	HCT	LSTTL	HCT → LS	LS → HCT	LS → LS	HCT → HCT
V_{IL} MAX	0.8V	0.8V	—	—	—	—
V_{IH} MIN	2V	2V	—	—	—	—
V_{OL} MAX	0.33V	0.4V	—	—	—	—
V_{OH} MIN	4.4V	2.7V	—	—	—	—
V_{NML}	—	—	0.47V	0.4V	0.4V	0.7V
V_{NMH}	—	—	2.4V	0.7V	0.7V	2.4V



92CS-38889

Fig. 8 - Typical HC/HCT input current Vs. temperature

Input Termination

The very low HC/HCT input current and hence, high input resistance is primarily due to low-level leakage currents of the input ESD protection diodes shown in Fig. 9. This excellent input buffering characteristic of CMOS logic IC's is fundamental to the wide range of very low power applications from pure logic to wide range RC oscillators, high Q crystal oscillators, etc. However, in no situation should this high input resistance be left floating or unterminated. Inputs may be tied directly to V_{CC} or GND via resistors of up to 1Mohm; the upper limit is only related to ac noise immunity, i.e., pick up.

Comparing HC/HCT unused input terminations to LSTTL logic, puts the flexibility of QMOS into a very positive light. It is a stated LSTTL design rule that unused inputs be terminated to V_{CC} via a 1.2kohm resistor and not tied directly to GND or V_{CC} nor left floating.

One additional note on HC/HCT input terminations. There are several bidirectional (transceiver) logic types in the QMOS family with common I/O pins. These I/O pins do not have the input poly resistor (R) of Fig. 9. Hence, these pins cannot be terminated directly to V_{CC} or GND. A terminating resistor to V_{CC} or GND of 10kohm is recommended.

Input/Output ESD Protection

HC/HCT device inputs have a resistor-diode protection network, shown in Fig. 9, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels typically greater then 2kV in all modes pertaining to the input, as shown in Fig. 10. The 2kV figure was arrived at by testing devices in the ESD test circuit shown in Fig. 11 while conforming to the MIL-STD-38510 requirements.

The recommended handling practices for QMOS devices are similar to those described in RCA Application Note ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits".

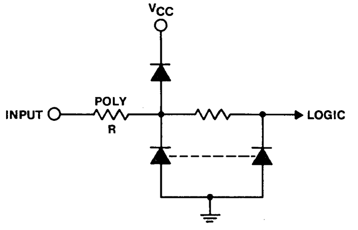


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Fig. 9 - Resistor-diode protection network used on inputs of HC/HCT devices to protect device gate oxide from electrostatic discharge damage(ESD).

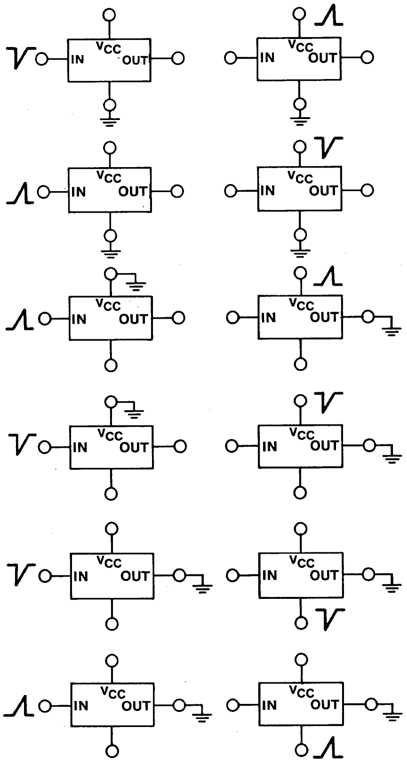

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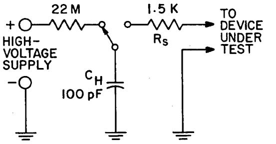
Fig. 10 - HC/HCT ESD test modes



C_H = HUMAN BODY CAPACITANCE TO GROUND
R_S = BODY SOURCE RESISTANCE

92CS-37074

Fig. 11 - Test circuit used to measure electrostatic discharge (ESD) in HC/HCT circuits. The rise time at the output terminal should be 13 ± 2nS.

Input Interaction

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Fig. 12 shows this transistor.

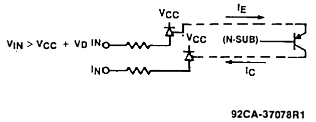
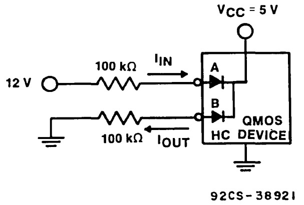


Fig. 12 - Parasitic transistor caused by input-protection network.

This parasitic transistor may cause undesirable interaction between adjacent inputs if the input level is greater than V_{CC}+Vdiode. RCA QMOS devices minimize the alpha ($\propto = I_E/I_C$) to less than 0.05. This feature of RCA QMOS inputs permits proper logic operation in the presence of transients and also allows high-to-low voltage translation via series input resistors. The typical value of $\propto$ for QMOS ICs is .001. Fig. 13 illustrates how control of $\propto$ in RCA QMOS devices provides for safe conversion of 12V control logic levels to 5V HC system logic simply by insertion of a 100k ohm resistor in each input. The only disadvantage is that logic signals are delayed by 1-2uS and therefore, this scheme works well only with rather slow 12V control logic as for example, in automotive applications. When the input diodes are used as clamps for logic level translation, the input current should be kept to 2mA or less.



$$I_I = \frac{6.3\ V}{100\ k\Omega} = 63\ \mu A$$

$$I_0 = \propto I_I = 0.05 \times 63\ \mu A = 3.15\ \mu A$$

$$V_{IL(B)} = 3.15\ \mu A \times 100\ k\Omega = 0.315\ V$$

V_{IL} max (spec.)=1.5 V   Noise Margin=1.5 V -0.315 V=1.2 V Approx.

Fig. 13 - 12V-to-5V logic-level conversion at HC inputs using 100kOhm series resistors

Input-Voltage Considerations and Maximum Forward-Diode Input Current Limits

As a general rule, CMOS logic devices employing input clamp diodes (Fig. 9) to minimize ESD effects should be operated between the power supply rails. If the input series polysilicon resistor shown in Fig. 9 is not considered, then the rule is:

$$-0.5V \leq V_{IN} \leq (V_{CC} + 0.5V)$$

This rule is the industry standard (JEDEC Std. No 7) and is intended to keep users from damaging devices because the devices of some HC/HCT device manufacturers the devices do not have the built-in input series polysilicon resistor. RCA HC/HCT data sheets continue to show the conservative rating established by JEDEC. However, RCA HC/HCT device inputs are capable of meeting the following rating: $-1.5V \leq V_{IN} \leq V_{CC} + 1.5V$.

Furthermore, RCA devices, except for special cases such as transceivers and analog switches or multiplexer signal inputs, can reliably operate with the ±1.5V rule without logic errors. Beyond ±1.5V, maximum forward current poses a second limitation with respect to the V_{CC} and GND rail. This QMOS and JEDEC rating is ±20mA of transient current maximum forced into inputs or outputs.

Latch-Up

Definition

Latch-up within CMOS IC structures may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one or combination of these terminals may initiate turn-on of an SCR-type 4-layer diode parasitic bipolar device, as shown in the simplified diagram of Fig. 14. This parasitic structure, when triggered on, keeps the supply voltage below the V_{CC} voltage and thus permits a high supply current of several hundred mA to flow (see Fig. 14). The resistor values of r_c, $r_{bb'}{}^1$ and $r_{bb'}{}^2$ are dependent on circuit layout geometry and p+ and n+ doping levels.

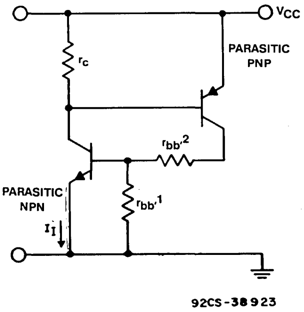


Fig. 14 - Simplified diagram of CMOS 4-layer diode structure

The lower the value of these resistors, the less voltage drop that will occur. A much higher trigger current, therefore, will be required to induce turn on of the SCR structure shown in Fig. 14.

Also important are established layout rules and process parameters that minimize the current gain (Beta) of the parasitic NPN and PNP transistors shown in Fig. 14.

Latch-Up Capability

The trigger current that could potentially trigger latch-up of QMOS ICs is typically ±80mA at any input or output terminal. Measurements are made at all terminals (see next section for preferred measurement technique), so that these terminals have a minimum acceptable latch current of ±40mA. The absolute maximum rating in the QMOS data sheet and in the industry JEDEC Standard No. 7 is ±20mA. The possibility for transient currents in applications are more likely to appear at input terminals where interfaces could cause voltage transients. The voltage required to induce the ±40mA measured capability and the ±80mA typical capability of QMOS ICs as illustrated in Fig. 15, is established by the QMOS built-in 120 ohm minimum current-limiting polysilicon resistor at logic inputs.

Equations:

$V_T = I_TR + V_D + V_{CC}$ $\qquad R = 120$ ohms

$V_D = 0.7V$

$-V_T = -I_TR - V_D$ $\qquad V_{CC} = 4.5V$

Values:

$V_T = 40mA \times 0.12k \text{ ohms} + 0.7V + 4.5V = 10V$ min.

$V_T = 80mA \times 0.12k \text{ ohms} + 0.7V + 4.5V = 14.8V$ typ.

$-V_T = -40mA \times 0.12k \text{ ohms} - 0.7V = -5.2V$ min.

$-V_T = -80mA \times 0.12k \text{ ohms} - 0.7V = -10.3V$ typ.

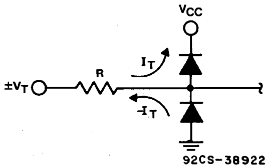


Fig. 15 Input latch transient voltage determination

As developed in Fig. 15, the minimum and typical ±V_T transient input voltages required to induce either ±40mA or ±80mA are relatively large, and far greater than the transients induced in 5V systems where 2 or 3 volts of ringing transients can be induced via wiring inductance effects. This ±40mA QMOS capability is truly a "latch-up free" condition for operation in a 2V to 6V system. If transients are induced in a particular application beyond +10V/-5.2V, then the use of external series-limiting resistors are advised to keep transient currents below ±40mA. Another consideration is unused inputs. If unused QMOS inputs are tied to a V_{CC} of +5.5V and the V_{CC} of the QMOS IC is temporarily grounded, for example, in a 2-power supply system, or when PC cards are replaced with power on, no possibility of latch-up will exist because the input current will be limited to ±40mA via the built-in 120-ohm polysilicon series resistor.

Measuring Latch-Up Sensitivity

Caution

The test methods that follow can damage devices if the following **precautions are not strictly observed**.

- Apply currents for 1ms (min) to 5 seconds (max).
- Limit power supply currents to 200mA.
- Allow a cool-down period between successive tests to be equal to or greater than the time that is required to apply trigger current.
- These tests may be safely adapted to bench-testing with meters or use of a curve tracer

1. Static Input or Output Triggering for Latch-up

V_{CC} supply to 200mA
For input triggering connect other inputs to V_{CC} or GND

All valid logic conditions are subject to test.

For Output Triggering (Figs. 16c/d):

- -Io - Active outputs must be set low
- +Io - Active outputs must be set high
- 3-State outputs - Also set output to high-impedance state

Apply trigger current first (Fig. 17)

- Apply ±I_I or ±I_O(Fig. 16)
- Raise V_{CC} to ±V_{CC} max.
- After the trigger duration, reduce trigger current to zero
- If I_{CC} is less than its quiescent value, the device is not latched.

If the quiescent value of I_{CC} is out of specification, the input and output structure should be electrically checked to determine if the I/O circuitry is damaged and latch-up did not occur. Further device analysis may be required to verify if latch-up did indeed occur.

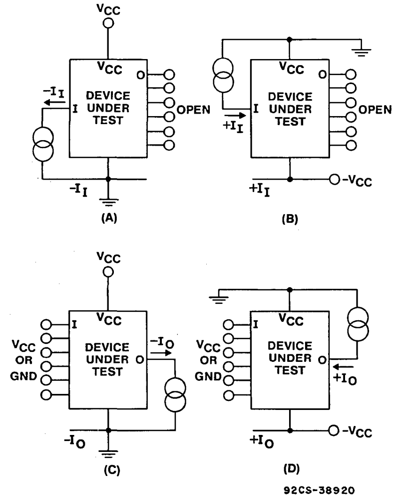


Fig. 16 - Test set-up for positive and negative trigger current

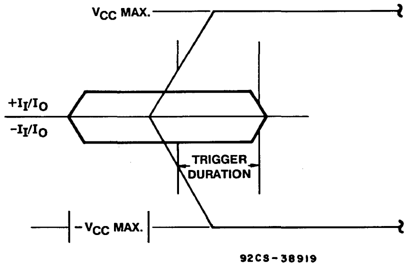


Fig. 17 - Latch test waveforms

2. V_{CC} Triggered Latch-Up Test by Over-Voltage on V_{CC} (Fig. 18)

Latch-up can occur if the voltage of the power supply is raised above the absolute maximum supply voltage rating.

Apply a V_{CC} overvoltage of 2X V_{CC} max. referenced to GND using a 100-mA limited supply.

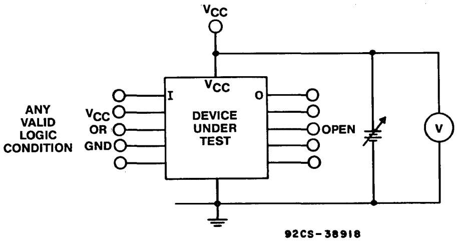


Figure 18: Test set-up for V_C over-voltage latch trigger

Measure the V_{CC} voltage. If it is less than V_{CC} max., the part has latched.

Output Characteristics

QMOS outputs make use of a complementary symmetry transistor configuration, which is different from the LSTTL totem-pole output; both outputs are shown in Fig. 19. QMOS outputs meet the voltage-level requirements necessary to interface to QMOS inputs, and the drive and current requirements needed to interface to bipolar inputs; i.e., TTL, LS, ALS, AS, FAST, etc.

The outputs of the QMOS devices are classified into two categories: standard and bus drive. The two outputs differ in the output transistor widths needed to meet JEDEC standard drive and current requirements. Both standard outputs and bus drive outputs may be active (2-state) or 3-state with a high-impedance mode added and where both the PMOS and NMOS transistors are off. Another type of QMOS output is the open-drain output of the HC/HCT 03 Quad NAND gate shown in Fig. 20. This output has no intrinsic or added diode connected to V_{CC} at the output. The output of this device may be connected to an external load terminated at up to 10V. Thus, outputs can be pulled up above a nominal 5V supply for up-level voltage conversion.

The HC/HCT03 is the only QMOS gate type whose outputs can be used for a "wired OR" arrangement.

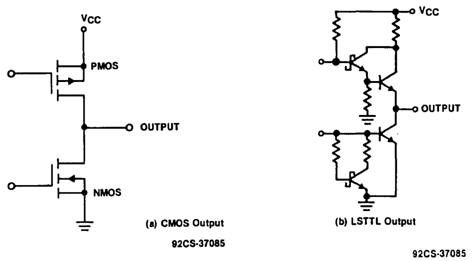


Fig. 19 - Comparison of HC/HCT (a) and LSTTL (b)

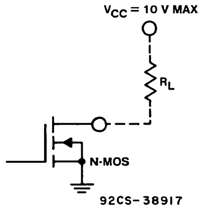


Fig. 20 - HC/HCT 03 output circuit

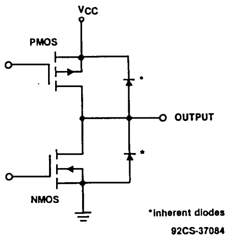


Fig. 21 - Inherent diodes protecting HC/HCT outputs.

Output Protection

The outputs in a QMOS device are protected from ESD damage by diodes. Figure 21 shows these diodes. These intrinsic diodes are effective because of the large geometries (widths) of the output transistors. These diodes are the drain to n-substrate junction of the p device and the drain to p-well junction of the n device. This network provides protection to voltage levels typically greater than 3kV in all ESD discharge modes pertaining to the output (see Fig. 9).

Output Currents

QMOS outputs are specified for both CMOS and LSTTL loads. CMOS inputs are voltage sensitive and the only current is leakage current. The output voltage test for CMOS interfacing is specified for I_O at ±20uA (20 CMOS loads). The outputs are also specified at I_O = 4mA (10 LSTTL loads) and 6mA (15 LSTTL loads) for standard and bus-drive outputs, respectively. The corresponding V_{OL} (max) and V_{OH} (min) for the outputs, are illustrated in Table III.

The maximum current per output pin (I_O) is ± 25mA and ±35mA for standard and bus-drive outputs, respectively. This maximum current rating is specified when the outputs are in their active regions: $-0.5V < V_O < V_{CC} + 0.5V$. The maximum current rating per power pin, V_{CC} or ground, is 50mA and 70 mA, respectively, for standard or bus-drive outputs.

When the output voltage exceeds V_{CC} or is below ground by greater than 500mV, the output protection diodes turn on and conduct current. The maximum diode transient current, $I_{O}K$, should not exceed ±40mA to avoid latch-up as described earlier.

Table III - Output Drive Specifications

	Test Conditions/Limits (V_{CC} =4.5V)				
Characteristic	**I_O**	**25°C**	**-40 to 85°C**	**-55 to 125°C**	**Unit**
High-Level Output Voltage, V_{OH}(min)	-20uA -4mA -6mA (Bus)	4.4 3.98 3.98	4.4 3.84 3.84	4.4 3.7 3.7	V V V
Low-Level Output Voltage, V_{OL}(max)	20uA 4mA 6mA (Bus)	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V

Output-Current and Interfacing Capability

A comparison of the output drive capabilities for QMOS with those of LSTTL is as follows:

> LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst case low and high input thresholds will be met and the existing margins of noise immunity preserved.
>
> QMOS capability is expressed as source/sink current at a specified output voltage. Since QMOS requires virtually no input current, the unit load concept does not apply.

With a specified output drive of 0.4mA at 0.4V, the QMOS-to-QMOS interface capability exceeds 1000 ULs, and with a 20uA/0.1V specification, the QMOS capability is 20ULs. Each standard QMOS output has a drive capability of ten LSTTL loads and maintains a V_{OL} of 0.4V over the full temperature range. Bus driver outputs can drive 15 LSTTL loads under the same conditions.

The output drive capabilities of QMOS expressed in LSTTL unit loads are shown in Table IV.

Output Curves

Output current derating versus temperature is shown in Fig. 22 and is valid for all types of output. Output source and sink drives at V_{CC} = 2, 4.5, and 6V are given in Figs. 23 to 26 which show output currents versus output voltages. These curves indicate the typical output current at 25°C and minimum output currents that can be expected at 25°C, 85°C, and +125°C, and can also serve as a design aid in interface applications and for calculating transmission line effects on charging highly capacitive loads.

Note to Figs. 22 to 25: The expected minimum curves are included as an aid to equipment designers, and are tested only at the points indicated on device data sheets.

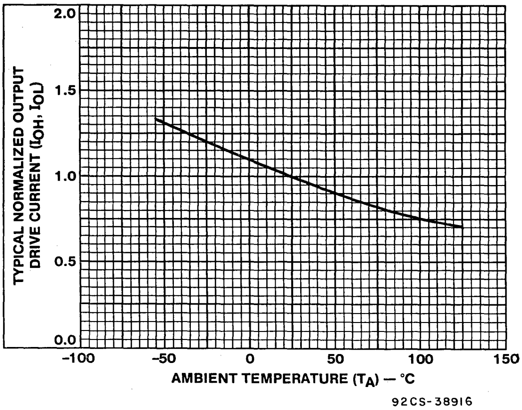


Fig. 22: Output current derating vs. ambient temperature.

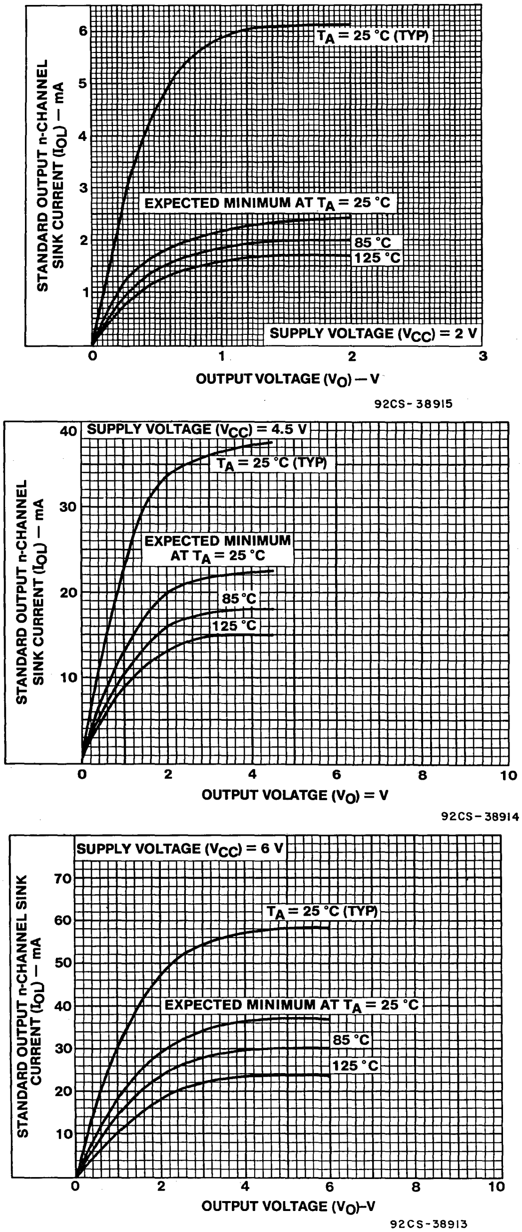


Fig. 23: Standard output n-channel sink current (I_{OL}) for V_{CC}=2V, 4.5V, and 6V.

Table IV: Comparison of Output Drive Capabilities

LS Device	Output Drive	HC/HCT Equivalent	Output Type	Output	Drive
74LS00	4 mA 10 UL	74HC00	Standard	4 mA	10 UL
74LS138	4 mA 10 UL	74HC138	Standard	4 mA	10 UL
74LS245	12 mA 30 UL	74HC245	Bus	6 mA	15 UL
74LS374	12 mA 30 UL	74HC374	Bus	6 mA	15 UL

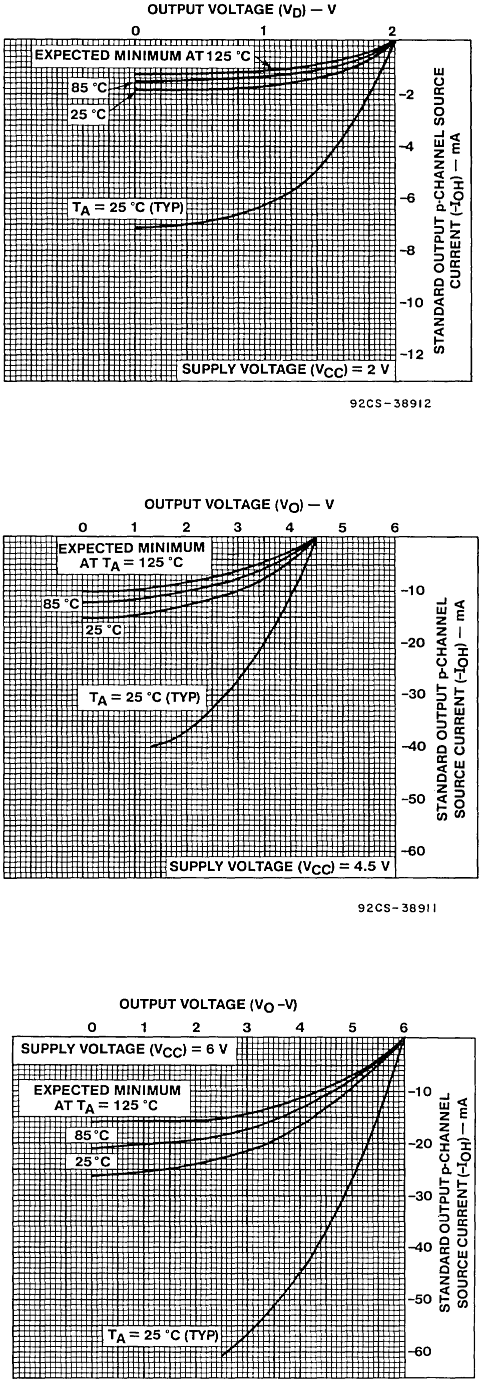


Fig. 24: Standard output p-channel source current (-I$_{OH}$) for V$_{CC}$=2V, 4.5V, and 6V.

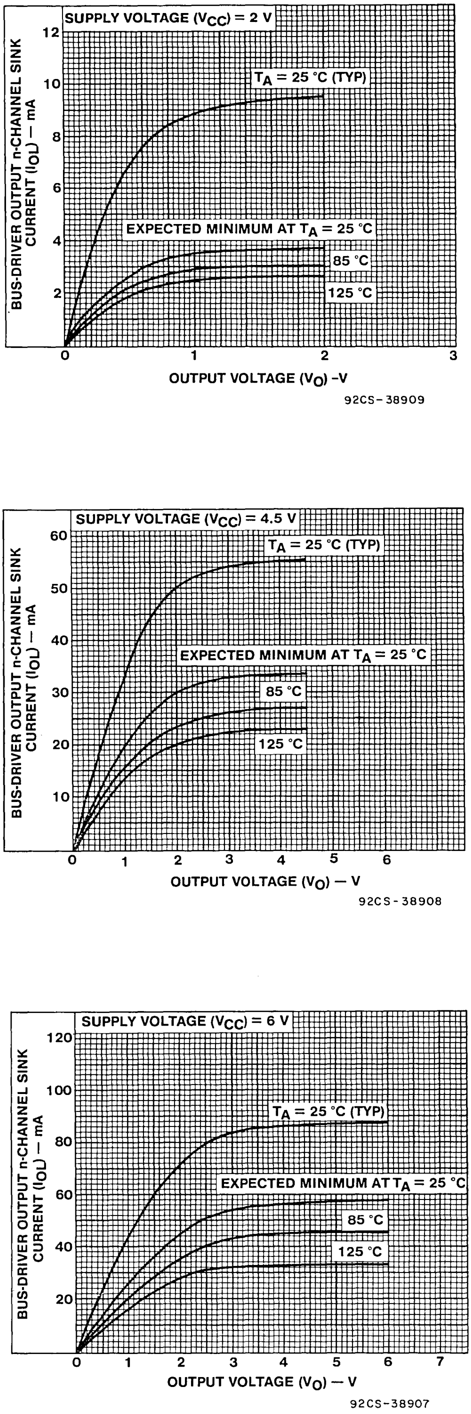


Fig. 25: Bus-driver output n-channel sink current (I$_{OL}$) for V$_{CC}$=2V, 4.5V, and 6V.

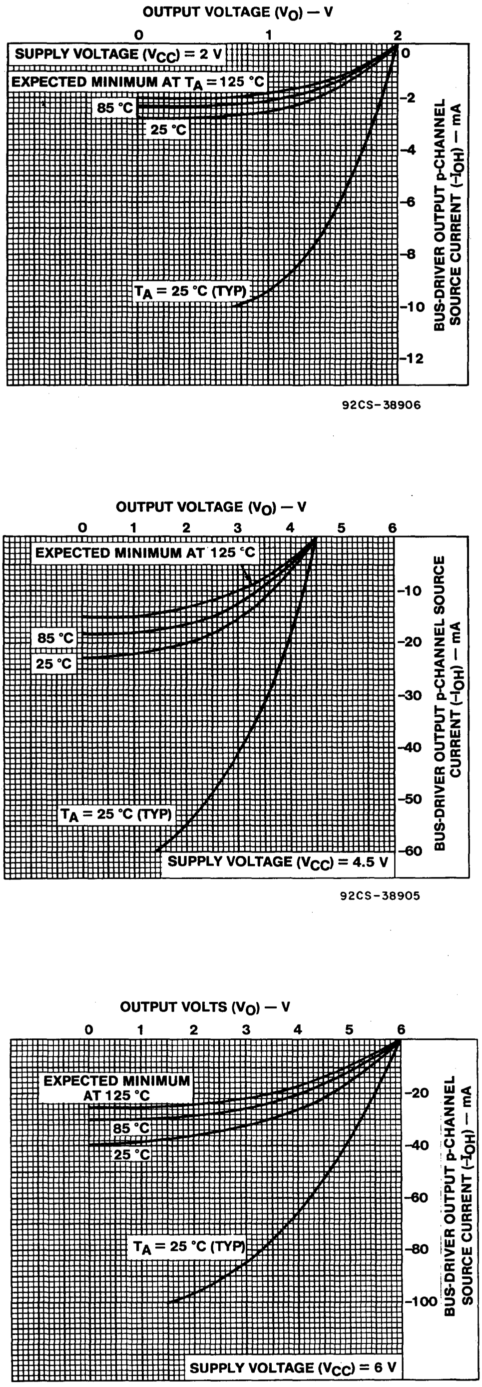


Fig. 26: Bus-driver output p-channel source current ($-I_{OH}$) for V_{CC}=2V, 4.5V, and 6V.

Dynamic Characteristics

The RCA QMOS family is designed to meet the dynamic switching speeds and operating frequency of low-power Schottky TTL. When compared to metal-gate CD4000 and 74C series CMOS, QMOS shows a 10 to 1 improvement in ac performance. QMOS types feature balanced propagation delays and transition times specified at conditions similar to LSTTL at a nominal V_{CC} =5V and C_L = 15pF, so that the user can relate to the equivalent LSTTL specification. Switching speed limits for QMOS are given at a more realistic V_{CC} of 4.5V and a C_L of 50pF. Test waveforms for the HC and HCT types are shown **at the end of this section.**

Capacitive Load (C_L) Determination

The external capacitive loading (C_L) seen by a QMOS output is required to calculate the propagation delay and operating power dissipation of a logic function. The three components of C_L at a logic node are:

1. n C_{IN} where n is the fan-out.
2. m C_{OUT} where m is the number of three-state outputs on a logic bus.
3. C_{STRAY} which is the effective wiring and interconnect capacitance.

$$C_L = n\,C_{IN} + (m - 1)\,C_{OUT} + C_{STRAY} \qquad (1)$$

C_{IN} is shown in Fig. 27 for typical HCT and HC type inputs. Note that C_{IN} has peak values at the respective switch points of HCT (1.4V) and HC(2.5V). Capacitance on either side of the peak is a summation of package, lead-frame, reverse-biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller multiplication of C gate-to-drain in the high-gain linear-transition region. The values of C_{IN} that most typically represent the average loading effect are 4pF for HCT inputs and 3pF for HC inputs. C_{IN} for HCT inputs is higher than that for HC inputs because of the required large gate-to-source/drain capacitance of the large NMOS device widths.

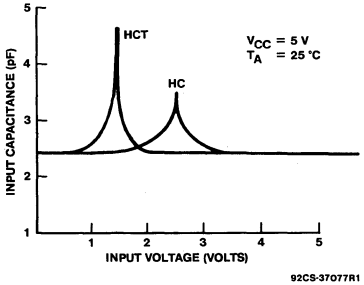


Fig. 27: C_{IN} as a function of V_{IN}.

Output capacitance (C_{OUT}) is typically 10pF for both HCT and HC-type bus-driver outputs when these versions are in their high-impedance state, the only state where C_{OUT} loading is a factor.

The wiring and interconnect capacitance (C_{STRAY}) is determined by estimates of interconnect capacitance and wiring capacitance. These capacitances are highly variable because of differences in interwiring techniques. An often used high-speed wiring technique utilizes strip line with 100-ohm characteristic impedance. C_{STRAY} in this case, is typically 20pF per foot. Capacitances of sockets and connectors are available from their manufacturers.

In a bus system, C_{STRAY} is the largest single C_L component, as the following example illustrates:

Bus Specification:
No. of fan-outs (n) = 10
No. of bus drivers (m) = 5
From Equation (1):
$C_L = 10 \times 2.5pF + 4 \times 10pF + 7 \times 20pF$
$= 25pF + 40pF + 140pF = 205pF$

Propagation Delays

Propagation Delays Vs. Supply Voltage

The dynamic performance of a CMOS device is related to its drain characteristics. The drain characteristics are related to the thresholds and gate-to-source voltage potential, Vgs. The Vgs voltage is equal to the power supply voltage, V_{CC}. Therefore, a reduction in V_{CC} adversely affects the drain characteristics which, in turn increases the propagation delays. An increase in V_{CC} decreases the propagation delays.

The voltage range of the HCT version is 5V ± 10%. Over this range, the effects of propagation delays on performance are minimal. However, the voltage range recommended for the HC version is 2 to 6V. Over such a wide range, the effects on dynamic performance of propagation delay and operating frequency (See Fig. 28) are appreciable.

Propagation Delay Vs. Capacitance

Propagation delay vs. capacitance for the RCA family of HC/HCT types is similar to that of LSTTL types which HC/HCT types may replace in present or new applications.

To determine a propagation delay maximum limit at any value of capacitive loading up to 300pF, the following equation is used:

$$t_{PD}(C_L) = t_{PD}(50pF) + t(C_L)\,[C_L - 50pF] \qquad (2)$$

Where:

$t_{PD}(C_L)$ = maximum propagation delay at the desired C_L
$t_{PD}(50pF)$ = maximum propagation delay from device data sheet at 2V, 4.5V, or 6V (See Table V).
$t(C_L)$ Maximum (ns/pF) multiplying factor from the following table:

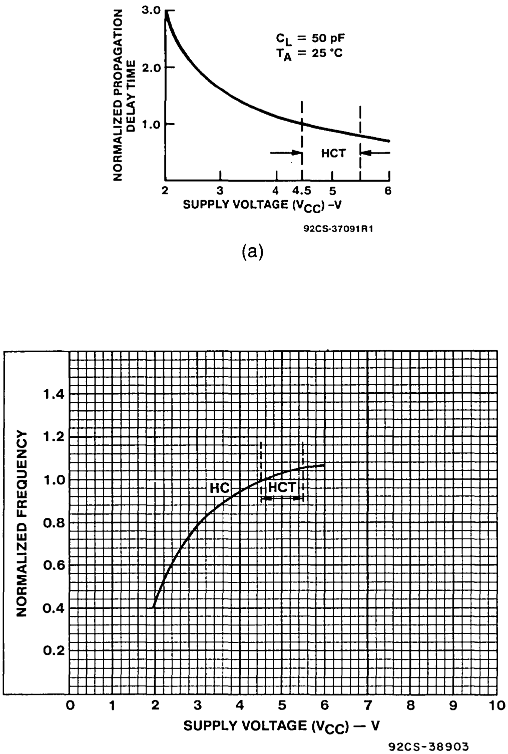
	$t(C_L)$ (nS/pF)	
V_{CC}	**Std. Output**	**Bus Output**
2V	0.272	0.187
4.5V	0.102	0.068
6V	0.082	0.056

Propagation Delay Vs. Temperature

Because an increase in temperature causes a decrease in electron and hole mobilities, a temperature increase will cause an increase in propagation delays. Correspondingly, ac performance improves with lower temperatures. Typically, speeds derate linearly from 25°C at about -0.3%/°C.

The propagation delay, therefore, can be computed at any temperature between -55°C and +125°C by using the following relationship:

$$t_{PD}(T) = t_{PD}(25^\circ C) + [(T(^\circ C)-25)\ (0.003ns/^\circ C)] \qquad (3)$$



(a)

(b)

Fig. 28: Typical switching speed characteristic versus supply voltage normalized to 4.5V.

Output Transition Times

Table V shows the RCA standard and maximum ratings for output transition times applicable to all standard and bus-driver outputs. Typical values are approximately one-half the maximum values. Practical unspecified minimum values are one-fourth the limit values.

Table V - Output Transition Time Limits for C_L = 50pF

Output	V_{CC}(V)	Maximum Output Transition Times (ns)		
		$T_A = 25°C$	$T_A = 85°C$	$T_A = 125°C$
Standard	2 4.5* 6	75 15 13	95 19 16	110 22 19
Bus Driver	2 4.5* 6	60 12 10	75 15 13	90 18 15

*Specification for CD54HCT and CD74HCT types.

Output Transition Time Vs. Capacitive Loading

To determine the maximum output transition time on any capacitive loading up to 300pF, the following formula is used:

$$t_T(C_L) = t_T(50pF) + t'(C_L) [C_L - 50 \text{ pF}] \quad (4)$$

Where:

$t_T(C_L)$ = maximum transition time at the desired C_L
$t_T(50pF)$ = limit at 2V, 4.5V, or 6V(Table V)
$t_TN(C_L)$ = (ns/pF) multiplying factor from the following table:

V_{CC}	$t'(C_L)$ (ns/pF)	
	Std. Output	Bus Output
2V	0.544	0.374
4.5V	0.204	0.131
6V	0.170	0.110

Transition Time Vs. Temperature

Transition time at HC/HCT outputs typically changes by -0.3%/°C. Equation (3) used to compute increase in propagation delay with temperature (see above), can also be used to compute transition time at any temperature by simply substituting t_T for t_{PD}.

Clock Pulse Considerations

All HC/HCT flip-flops and counters contain master-slave devices with level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of voltage threshold levels for clocking is an improvement over ac-coupled clock inputs, however, these levels make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50% of V_{CC} for HC devices, and 28% of V_{CC} for HCT devices (1.4V at V_{CC} = 5V). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground. This condition results in a noise transient that is equal to the algebraic sum of internal and external gound plane noise. When a number of loaded outputs change at the same time, it is possible for the **chip** ground reference level (and therefore, the clock reference level) to rise by as much as 500mV. If the clock input of a positive-edge triggered device is at or near its threshold during a noise transient period, multiple triggering can occur. To prevent this condition, the rise and fall times of the clock inputs should be less than 500ns at V_{CC} = 4.5V, the data sheet maximum value.

In the HC/HCT family, several flip-flops have a Schmitt-trigger circuit at their clock input. This circuit increases the maximum permissable rise/fall time on the clock waveform. The RCA flip-flop types HC/HCT 73, 74, 107, 109 and 112, have special Schmitt-trigger circuits which increase their tolerance to slow rise/fall times and to high levels of ground noise.

Maximum permissible input-clock pulse-frequency ratings on each clocked device type data sheet requires a 50% duty cycle input clock. At these rated frequencies, the outputs will swing rail-to-rail, assuming no dc load on the outputs. This feature is a very conservative and highly reliable method of rating clock-input-frequency limits which for HC/HCT devices, equal or exceed LSTTL ratings.

Power Consumption

The power consumption of a HC/HCT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from transient currents required to charge and discharge the capacitive loads on logic elements, that is, transient currents caused by internal and external capacitance, and transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is represented by the value C_{PD}.

Two equations are used to compute the total IC power consumption. The first equation (A) is applicable to an HC or HCT device when the inputs are driven from GND to V_{CC} (rail-to-rail), as follows:

Equation (A):

$$P = P_{DC} + P_{AC}$$
$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2 f_I + \Sigma\, C_L V_{CC}^2 f_O$$

Where:
I_{CC} = Quiescent Current (Ref. Table VI)
V_{CC} = Supply Voltage
f_I = Input Frequency
f_O = Output Frequency
C_{PD} = Device Equivalent Capacitance
C_L = Load Capacitance

The second equation (B) is applicable only to an HCT device where specific input pins are driven at LSTTL levels defined as $V_{IN} = V_{CC} - 2.1V$:

Equation (B):

$$P = P_{DC} + P_{AC}$$
$$P = I_{CC}V_{CC} + \Delta\, I_{CC}V_{CC}D + C_{PD}V_{CC}^2 f_I + \Sigma\, C_L V_{CC}^2 f_O$$

Where:
$\Delta\, I_{CC}$ = Added dc current when $V_{IN} = V_{CC} - 2.1V$ (LSTTL level)
D = Duty cycle of clock (% of time HIGH)

Table VI - Temperature - Dependent Ratings

	LIMIT						
			T_A = 25° C		-40 to +85° C	-55 to +125° C	
	V_{IN}	V_{CC}	typ	max	74HCT MAX	54HCT MAX	Units
ΔI_{CC} additive dc current per input pin (1-Unit)	V_{CC} - 2.1V	4.5V to 5.5V	100	360	450	490	uA

Table VII HC/HCT and LSTTL Maximum Quiescent Current at $V_{CC} = 5V$

Device Complexity	HC/HCT				LSTTL 125° C
	Typical 25° C	Limit			
		25° C	85° C	125° C	
SSI	2 nA	2 uA	20 uA	40 uA	4.4 mA
FF	4 nA	4 uA	40 uA	80 uA	8 mA
MSI	8 nA	8 uA	80 uA	160 uA	10 mA to 95 mA

The temperature dependent ratings for I_{CC} are given in the table below:

HCT load table by type shown on each data sheet:

	Input	Unit Multiplier
Example:	All	X 0.6

The dynamic power due to outputs is the sum of the ac power at each output. The user must independently determine the C_L and the average frequency at each output. The latter requires estimating the average freguency of data nodes in a logic system. For example, for HC/HCT counter types, each output is inherently operating at different frequencies.

The source of the C_{PD} or device equivalent-power-dissipation capacitance is made up of 2 sources of internal device power consumption:

1) Power consumed by charge and discharge of internal device capacitance.

2) Power consumed through current switching transients.

Fig. 29 illustrates the typical I_{CC} vs. V_{IN} characteristic of HC type devices Note that when V_{IN} = 0.1V or (V_{CC} -0.1V), zero current flows. Thus, no ΔI_{CC} component is required for computing the power consumption of HC device types. However, the transient switching components of an IC consume power and are a part of the C_{PD} value.

Fig. 30 illustrates the typical I_{CC} vs. V_{IN} characteristic of HCT type devices. Again, if input voltages are 0.1V or (V_{CC}= -0.1V), no ΔI_{CC} value exists. Also for V_{IN} = 0.4V, ΔI_{CC} is zero. If V_{IN}, however, is an LSTTL logic high level of (V_{CC} -2.1V) or approximately 3V for V_{CC} = 5V, then **significant** ΔI_{CC} does exit and is indicated in equation (B) as the ΔI_{CC} component.

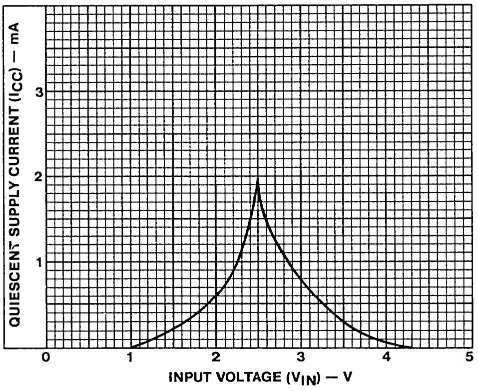


Fig. 29: I_{CC} vs. V_{IN} for RCA HC types

The special input design of RCA's HCT types greatly reduces the value of ΔI_{CC} such that the added power is very small; for example, RCA's HCT power is minimal compared to LSTTL power. If this special input circuitry were not used, the ΔI_{CC} values would be relatively high as demonstrated by the dashed line in Fig. 30, and the HCT type would not have very low power when compared to LSTTL.

NOTE: The low value of I_{CC} is due to a special input design that provides a true low-power HCT capability.

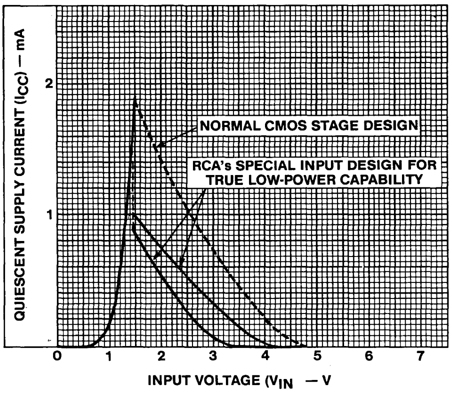


Fig. 30: I_{CC} vs. V_{IN} for HCT types

Because appreciable current flows during device input switching as shown in Figs. 29 and 30, it is important to maintain fast input rise and fall times. The JEDEC and RCA recommended maximum input rise and fall times are:

1000 ns for $V_{CC} = 2V$
500 ns for $V_{CC} = 4.5V$
400 ns for $V_{CC} = 6V$

Since maximum output transition times are 15ns for the standard logic types and 12ns for bus drivers, a designer must only be concerned with exceeding the rise and fall times shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and amplifiers using the HCU04 types.

When Schmitt-trigger types HC/HCT14 and 132 are used for either shaping up slow signals or as RC oscillators, power is increased due to prolonged through-current. For further information on oscillators and their power consumption, refer to RCA Application Note (ICAN-7337), "Astable Multivibrator Design Using High-Speed QMOS IC's".

The adverse effects of power transitions is another reason to maintain input rise and fall times under the recommended limits. Longer transitions may cause oscillations of logic circuits (and hence, logic errors) or premature triggering depending on system V_{CC} and GND noise, which are amplified when input signals hover near the switching voltages illustrated in Figs. 29 and 30. To reduce the effects of slower transitions, the use of Schmitt trigger types is recommended.

Comparison to LSTTL Power

The dynamic power consumption of HC/HCT devices is frequency dependent, but it should be noted that LSTTL power consumption is also frequency dependent at frequencies greater than 1MHz. At frequencies less than 1MHz, the dynamic component is negligible compared to the static component. The average power consumption of HC/HCT and LSTTL equivalents is illustrated in Fig. 31 for four device types. Because all of the functions in a multi—functional LSTTL device are biased when power is applied, the HC/HCT device characteristics are plotted for a single function and for the total package for the purposes of comparison.

Some observations from Fig. 31 are:

1) For SSI gate types, the HC/HCT power approaches LSTTL power at about 1MHz.
2) For higher complexity types such as the RCA HC/HCT 138 3-of-8 line decoder/demultiplexer shown in Fig. 31(c), HC/HCT power approaches LSTTL power at above 10MHz.

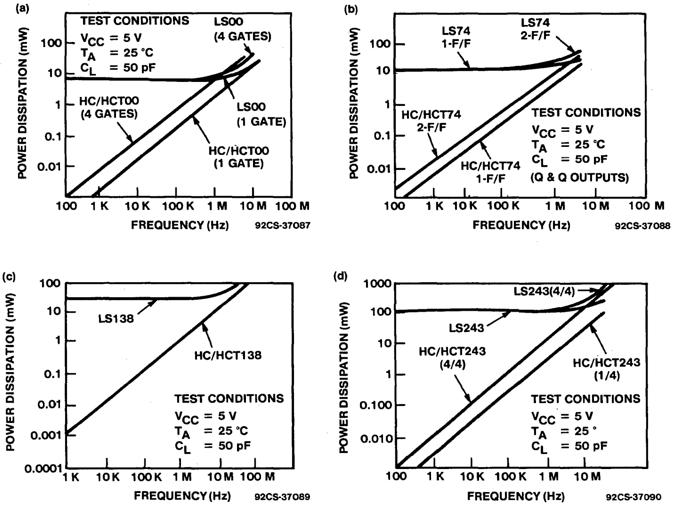


Fig. 31 - Power versus frequency graphs for the (a) LS/HC/HCT00, (b) LS/HC/HCT74, (c) LS/HC/HCT138, and (d) LS/HC/HCT243.

3) Fig. 31 implies continuous operation at the frequencies shown, however, most practical applications of logic in microcomputer systems have variable operation or data/address signal rates. The average operating frequency is much below the peak operating frequency — particularly in the 100KHz region where power savings over LSTTL are several orders of magnitude.

Power-Supply Considerations

Power-Supply Voltages

The RCA HC and HCU versions have a power supply range of 2 to 6V; the absolute maximum voltage rating is 7V. The ability to use RCA's HC types with a 2V supply makes these devices particularly useful in battery-operated equipment, especially systems including memories that feature 2V standby operation. The absolute maximum supply or ground current, per pin, is ±50mA for types with standard output drive, and ±70mA for types with bus driver outputs.

The operating supply-voltage range for RCA's CD74HCT types is 4.5V to 5.5V, 5V ± 10%. These figures indicate that there is more tolerance in the regulation of the low-current system supply than is the case with other technologies. The maximum voltage indicated for HC and HCU versions also applies to HCT versions. The advantages of using HC/HCT/HCU with its wider voltage supply range are illustrated in Fig. 32.

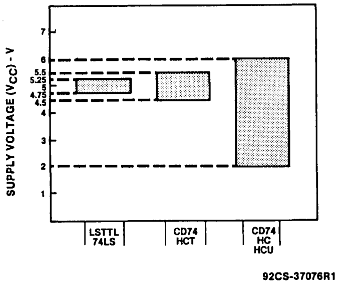


Fig. 32: Power-supply ranges for CD74HCT, CD74HC and CD74HCU versions of the RCA family of devices and 74LS series types.

Battery Back-Up

Battery back-up can be easily implemented in systems of RCA's HC/HCU devices. An example of this arrangement is shown in Fig. 33. The minimum battery voltage required is only 2V plus one diode drop.

In the example, RCA's High-to-Low Level Shifters (HC4049 or HC4050) are used to prevent the flow of positive input currents into the system due to input voltage levels greater than one diode drop above V_{CC}. If the circuit design is such that input voltages can exceed V_{CC}, then external resistors should be included to limit input currents to 2mA. External resistors may also be necessary in the output circuits to limit currents to 2mA, if the output can be pulled above V_{CC} or below GND. These currents are due to inherent V_{CC}/GND diodes that are present in all outputs, including three-state outputs.

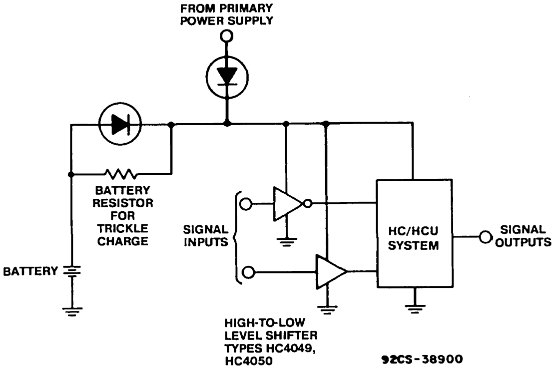


Fig. 33 - Example of an HC/HCU system with battery back-up.

Power Supply Regulation and Decoupling

The wide power supply range of 2 to 6V may suggest that voltage regulation is not necessary, but it must be realized that a changing supply voltage affects system speed, noise immunity and power consumption. Because noise immunity, and even the correct operation of the circuit, can be affected by noise spikes on the supply lines, therefore, matched decoupling is always necessary in dynamic systems.

Both HC and HCT types have the same power supply regulation and decoupling requirement. The best method of minimizing spiking on the supply lines is by implementing good power supply and ground bussing and having low ac impedances from the V_{CC} and GND pins of each device. Because the minimum value of a decoupling capacitor depends on the voltage spikes that can be allowed, it is a general rule to restrict ground and V_{CC} noise peaks to 400mV. A local voltage regulator on the printed-circuit board can be decoupled using an electrolytic capacitor of 10 to 50 uF.

Localized decoupling of devices can be provided by a 22nF capacitor for every two to five packages, and a 1uF tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level sensitive devices can be effectively decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

A practical example of determining the value of a decoupling capacitor is as follows: assume that a buffer output sees a 100-ohm dynamic load and that the output low-to-high transition is 5V, then the current demand is 50 mA per output. For an octal buffer, the current demand would be 0.4A per package, in approximately 6 nS.

The following formula can also be used to determine the value of a decoupling capacitor:

The term Q = CV is differentiated to obtain $\frac{\Delta Q}{\Delta t} = C\frac{\Delta V}{\Delta t}$.

Since $\frac{\Delta Q}{\Delta t} = I$, the equation becomes $I = C\frac{\Delta V}{\Delta t}$.

Hence: $C = \frac{I\Delta t}{\Delta V}$.

For an octal buffer, assuming a change in V_{CC} or GND of 0.4V, then;

$$C = \frac{0.4\ A \times 6 \times 10^{-9} S}{0.4\ V} = 6 \times 10^{-9}\ F = 6\ nF.$$

For further information on power-supply regulation and decoupling, refer to RCA Application Note ICAN7329, "Power-Supply Distribution and Decoupling for QMOS High-Speed IC's."

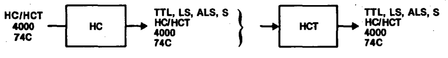
Interfacing

Because of the characteristics of the CMOS output, the HC/HCT family is very versatile in interfacing between different logic families. This capability including the corresponding fanout is illustrated in Fig. 34.

Note that the fanout to CMOS devices is limited only by the input rise and fall times, which are dependent on the capacitive loading, C_L. This dependence can be computed by the following relationship:

$$t_R, t_F = 2.2\ RC_L \qquad (5)$$

where R is the impedance of the output.



Fanout From:	To Corresponding Logic Families:					
HC/HCT	**TTL**	**LS**	**ALS**	**FAST**	**S/AS**	**4000, 74C**
Standard Types	2	10	20	6	2	See Text
Bus Drivers	3	15	30	10	3	

Fig. 34 - HC/HCT interfacing capability and corresponding fanout to other logic families

RCA's HC types cannot be driven from any of the TTL families because the TTL output voltage high, V_{OH} (min), does not satisfy the HC input voltage high, V_{IH}(min) specification. The HCT types can be directly interfaced to the TTL families because the HCT input voltage high, V_{IH} (min) is less than the TTL output voltage high, V_{OH}(min). To meet minimum V_{IH} requirements, HC types can use a pull-up resistor as illustrated in Fig. 35.

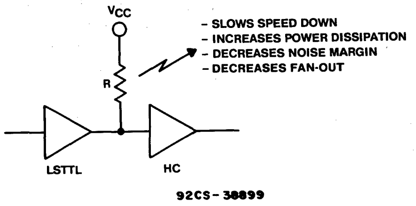


Fig 35 - Use of pull-up resistor to interface TTL and HC devices.

However, the use of a pull-up resistor will not give optimum performance because as noted in Fig. 35, the resistor tends to slow down system speed, increase power dissipation, decrease noise margin, and decrease fan-out.

For further information on interfacing, refer to RCA Application Note ICAN7325, "Interfacing HC/HCT QMOS Logic with Other Families and Various Types of Loads."

Logic-Level Conversion

The HC/HCT family contains logic-level conversion types necessary to interface high-voltage logic levels (up to 15V common in control and automation systems) to low voltage levels (down to 2V) as shown in Fig. 36.

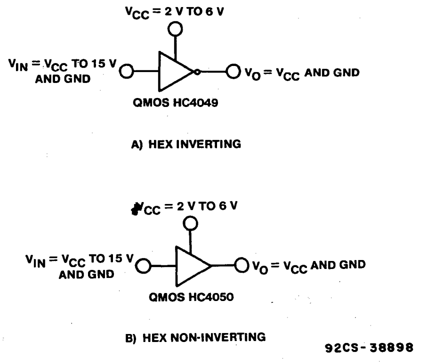


Fig. 36 - High-to-low logic level conversion

The Quad open-drain NAND gate (HC/HCT03) is used to convert from HC (2V to 6V) or HCT (TTL or CMOS) logic levels up to 10V output logic levels as shown in Fig. 37 R_L can be a very wide range of values. For design of this output interface, use the output N-MOS transistor characteristics of Fig. 23. The minimum value of R_L is that necessary to keep the output current below the 25mA HC/HCT family maximum rating. A large value of R_L will prolong the output rise time.

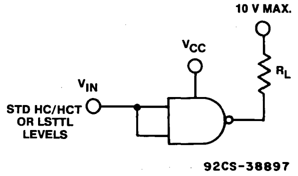


Fig 37 - Low-to-high logic-level conversion

System (Parallel) Clocking

When utilizing the HC/HCT family in synchronously clocked systems the following guidelines should be followed. Because of variations in switching points between devices, a slow clock edge could cause a logic error. If data in one of the synchronously clocked circuits changes before the switching point of the next sequential circuit is reached, a logic error will occur. This situation is illustrated in Fig. 38.

VS1 = Switching point, device 1
VS2 = Switching point, device 2
tp = Propagation delay

Because of variations in input threshold voltages among RCA's HC-version devices, the maximum clock-pulse rise or fall time should adhere to the following relationship:

$$t_r, t_f \text{ (max)} < 2t_p \text{ (max)} \qquad (6)$$

In a system where HC, HCT, and TTL-type families are mixed, the maximum clock pulse rise or fall times should adhere to the following relationship:

$$t_R, t_F \text{ (max)} < t_P \text{ (max)} \qquad (7)$$

It is recommended that a Schmitt-trigger circuit be utilized if wave-shaping is required.

The maximum rise or fall time into any RCA HC or HCT device must be limited to 1000, 500, and 400 nS at 2, 4.5, and 6 volts, respectively. If these limits are exceeded, noise on the input or power supply may cause the outputs to oscillate during transition. This oscillation could cause logic errors and unnecessary power consumption.

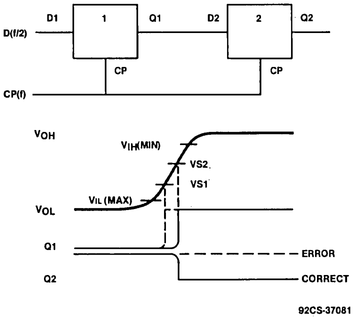


Fig. 38 - Result of changing data in one synchonously clocked circuit before the switching point of the next sequential circuit is reached.

Drop-In Replacement

The use of RCA HCT family devices make it unnecessary to sacrifice noise margins, speed, and quiescent power dissipation in constructing interfaces to achieve mixed-technology designs. This performance is possible because HCT devices are TTL compatible and can directly replace LSTTL counterparts without the addition of pull-up resistors at the LSTTL outputs.

Fan-out capabilities should be taken into account when an HCT device is used to replace a TTL part. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). The outputs of HCT devices are classified in two categories: standard and bus-driver. Table VIII shows the fan-out for the different TTL families.

For further information on drop-in replacements, refer to RCA Application Note ICAN7330, "Replacing LSTTL with QMOS High-Speed Logic IC's".

The fan-out values shown in Table VIII are derived at a voltage drop of maximum 0.4V (V_{OL}). In the "74" TTL series, an extended V_{OL} value is often seen, e.g., 8 mA at 0.5V voltage drop for LSTTL. If this value is used in determining the fan-out of the TTL part, it can result in a higher fan-out than is possible with QMOS. This condition can be resolved by replacing as many of the driven TTL parts as possible by HCT devices to reduce the sink current requirement (the HCT input current is neglegible). Furthermore, the use of HCT devices results in a substantial reduction in power dissipation.

Devices of the HCT family are power-saving, virtually drop-in replacements for LSTTL parts. The total power consumed by a system depends largely on the number of gates switching at any time and on the switching frequency, but in most systems only about 30% of all circuits switch at the maximum system frequency; 70% operate at far lower rates. Thus, even in systems using ALS, AS, S and FAST, the HCT family can be used with consequent power-savings and good reliability improvement in mixed technology designs.

Conversion of LSTTL Test to HCT Test

A simplified technique to convert an LSTTL test program to one that properly tests an HCT type is explained in RCA application note ICAN-7323 "Modification of LSTTL Test Programs to Test HCT High-Speed CMOS Logic IC's".

Bus Systems

Bus systems are commonly used in microcomputer applications. RCA CMOS devices are being increasingly used in these applications, for example, several CMOS versions of popular NMOS processors have recently been introduced.

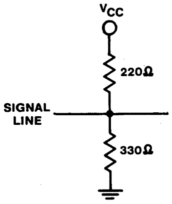
There are several constraints imposed on microprocessor systems in industrial applications, such as electrically noisy environments, battery stand-by requirements and sealed, gas-tight enclosures. QMOS bus systems, e.g., the proposed CMOS STD bus (a non-proprietary CMOS bus proposed standard) provides a low power solution to virtually all of these problems. In comparison with older bipolar digital IC Bus standards, QMOS bus systems offer superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

In order to optimize results with QMOS, particularly in circuits which communicate directly with the bus, the use of only HC devices is recommended, because HC QMOS optimizes input-signal noise immunity with HC QMOS a new low-power bus termination can be introduced (see Fig. 39 (b)) which, unlike the conventional high-current TTL bus termination of Fig 39a, draws no heavy dc current and is more suited to QMOS outputs. Both HC and HCT QMOS have the identical rail-to-rail output drive.

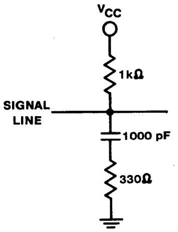
The wider supply voltage range of HC type QMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power

Table VIII: Fan-Out of HCT to TTL Elements

HCT	TTL	LS	ALS	FAST	S & AS
Standard	2	10	20	6	2
Bus-Driver	3	15	30	10	3



(a) Conventional terminations for TTL buses - 0.25 W per line or 2 W per octal drive and termination.



(b) Proposed low-power termination for CMOS STD bus equivalents.

Fig. 39 - Bus Terminations

buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via the card edge-input protection circuit. Such pick-up can exceed the CMOS input current maximum ratings if the input current is not limited by a 10k-ohm series resistor in the QMOS logic line. This series resistor will limit transient current to ±20 mA for external voltages of up to ±200V. However, for correct functioning, the dc input current should be kept below 2 mA. This type of card edge input protection is shown in Fig. 40.

In the circuit of Fig. 40, if the input diode current exceeds 2mA, a QMOS high-to-low level shifter should be used (e.g., HC4049, or HC4050).

Because QMOS bus-drivers do not have built-in hysteresis, slowly rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the QMOS flip-flop series HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt-trigger types HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section, "Propagation Delays and Transition Times".

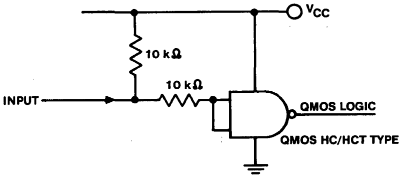


Fig. 40: Example of the card edge-input-protection circuit.

Standardized Capacitance Power Dissipation (CPD) Test Procedure

The purpose of the CPD number is to allow the user to estimate the actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per device" basis. Each part number's unique setup is listed in the "Pin Condition Table." The following paragraphs describe the generic set up for each class of devices:

All part numbers: Measurements are to be made at T_A = 25°C, V_{CC} = 5V, and 3-state outputs both enabled and disabled.

Gates: Switch one input. Bias the remaining inputs such that the output switches.

Latches: Toggle as in a flip-flop.

Flip-flops: Switch the clock pin while changing "D" (or biasing "J" and "K") such that the output(s) change each clock cycle. For part numbers with common clocks, exercise the "D", "J", or "K" inputs of only one flip-flop. Set the inputs of the remaining flip-flops so they do not change state.

Decoders / Demultiplexers: Switch one address pin, which changes two outputs.

Data Selectors / Multiplexers: Switch one address input, with the corresponding data inputs at opposite logic levels, so that the output switches.

Counters: Switch the clock pin, with other inputs biased, such that the device counts.

Shift Registers: Switch the clock, adjust the data inputs such that the shift register fills with alternate 1's and 0's.

Transceivers: Switch one data input. For bi-directional transceivers enable only one direction.

One Shots: TO BE DETERMINED

Parity Generators: Switch one input.

Priority Encoders: Switch the lowest priority input.

Rams: TO BE DETERMINED

Display Drivers: Switch one input such that approximately half the outputs change state.

ALUs / Adders: Switch one least significant input bit, bias the remaining inputs so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

Since CPD is a measure of device power consumption, and not that of the driven load, each output would ideally be unloaded. However, this is impractical with automatic testers which often have 30 to 40 pF hanging on each pin. Therefore, each output which is switching should be loaded with the standard 50 pF. The equivalent load capacitance, based on the number of outputs switching and their frequency, is then subtracted from the measured gross CPD number to obtain the device's actual CPD value.

If a device is tested at a high enough frequency, static supply current will contribute a negligible amount to power consumption and can be ignored. Thus, it is recommended that power consumption be measured at 1 MHz and the following formula be used to calculate CPD:

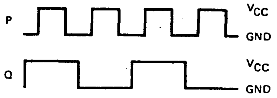
$$\text{CPD} = \frac{(I_{CC})}{(V_{CC})(1E6)} - \text{(equivalent load capacitance)}$$

EXPLANATION OF SYMBOLS

Key

V = V_{CC} (+5 V)
G = ground
H = logic 1 (V_{CC}) – inputs at V_{CC} for HC types; 3.5 V for HCT types
L = logic 0 (ground)
D = don't care – either H or L but not switching
C = a 50 pF load to ground
O = an open pin; 50 pF to ground is allowed
P = input pulse (see illustration)
Q = half frequency pulse (see illustration)
R = 1 kΩ pull-up resistor to an additional 5 V supply other than the V_{CC} supply
B = both R and C

Input pulses



Pin Condition Table for CPD Tests

HC/ HCT Types	Equivalent Load (pF)	Pin Number																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
02	50	C	P	L	O	D	D	G	D	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
03	0	P	H	B	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
U04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
08	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
11	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
20	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
21	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
27	50	P	L	D	D	D	O	G	O	D	D	D	C	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
30	50	P	H	H	H	H	H	G	C	O	O	H	H	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
42	100	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	–	–	–	–	–	–	–	–	–	–	–	–
58	50	P	D	D	D	D	O	G	O	L	L	L	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
73	50	P	H	H	V	D	D	D	O	O	D	G	C	C	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
74	50	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
75	50	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	–	–	–	–	–	–	–	–	–	–	–	–
85	50	L	H	P	H	O	C	O	G	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
86	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	P	–	–	–	–	–	–	–	–	–	–	–	–	–	–
107	50	H	C	C	H	O	O	G	D	D	D	D	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
109	50	H	H	L	P	H	C	C	G	O	O	D	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
112	50	P	H	H	H	C	C	O	G	O	D	D	D	D	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
123	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
125	50	L	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
126	50	H	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
132	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
137	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

Pin Condition Table (Cont'd)

HC/ HCT Types	Equiv-alent Load (pF)	Pin Number																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
138	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
139	100	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
147	50	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
151	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
153	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
154	100	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V	–	–	–	–
157	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
158	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
160	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
161	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
162	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
163	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
164	200	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
165	50	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
166	25	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
173	25	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	–	–	–	–	–	–	–	–	–	–	–	–
174	25	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–
175	50	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
181	250	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	C	L	H	L	H	L	H	V	–	–	–	–
182	150	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	–	–	–	–	–	–	–	–	–	–	–	–
190	60	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
191	53	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
192	60	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
193	50	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
194	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
195	125	H	H	L	D	D	D	D	G	H	P	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
221	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
237	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
238	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
240	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–
241	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	H	V	–	–	–	–	–	–	–	–
242	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
243	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
244	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–
245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
251	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
253B	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
257	50	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
258	50	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
259	25	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–
7266	50	P	L	C	O	D	D	G	D	D	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
273	25	H	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
280	100	L	L	O	L	C	C	G	P	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
283	250	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	–	–	–	–	–	–	–	–	–	–	–	–
297	12	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–

Pin Condition Table (Cont'd)

HC/ HCT Types	Equivalent Load (pF)	Pin Number																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
299	250	H	L	L	C	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	–	–	–	–	–	–	–	–
354	100	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	–	–	–	–	–	–	–	–
356	50	D	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	L	H	C	C	V	–	–	–	–	–	–	–	–
365	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
366	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
367	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
368	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
373	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
374	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
377	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
390	50	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
393	47	P	L	C	C	C	C	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
423	100	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
533	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
534	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
563	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
564	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
573	25	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
574	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
583	250	H	H	H	L	L	C	C	G	C	C	C	H	P	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
7597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
640	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
643	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
646	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
648	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
670	100	Q	Q	Q	L	P	C	C	G	C	C	L	L	L	P	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	C	V	–	–	–	–	–	–	–	–
4002	50	C	P	L	L	L	O	G	O	D	D	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4015	100	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
4016	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	–	–	–	–	–	–	–	–	–	–	–	–
4020	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4024	48	P	L	C	C	C	C	G	O	C	O	C	C	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4040	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4046A	50	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4049	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4050	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4051	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4052	0	O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4053	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4059	17	P	D	H	L	L	L	L	L	L	L	H	G	H	H	L	L	L	L	L	L	L	L	C	V	–	–	–	–
4060	106	C	C	C	C	C	C	C	G	C	C	P	L	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

Pin Condition Table (Cont'd)

HC/ HCT Types	Equivalent Load (pF)	Pin Number																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
4066	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4067	0	O	O	O	O	O	O	O	O	O	P	L	G	L	L	L	O	O	O	O	O	O	O	O	V	–	–	–	–
4075	50	P	L	D	D	D	O	G	L	C	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4094	250	H	Q	P	C	C	C	C	G	C	C	C	C	C	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
4316	0	O	O	O	O	P	D	L	G	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4351	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4352	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	O	O	O	O	O	V	–	–	–	–	–	–	–	–
4353	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4510	55	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4511	200	L	L	H	H	L	L	P	G	C	C	O	O	C	O	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4514	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4515	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4516	50	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4518	50	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4520	47	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4538	100	G	R	H	P	H	C	C	G	O	O	D	D	L	O	G	V	–	–	–	–	–	–	–	–	–	–	–	–
4543	50	H	L	L	H	L	P	L	G	C	C	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
7030	325	G	G	C	P	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	C	C	C	C	C	C	C	C	C	C	P	H	V
7046A	50	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
40102	5	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40103	3	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40104	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
40105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–

RCA Standardized Maximum Ratings and Recommended Operating Conditions for CD54/74HC, CD54/74HCT, and CD54/74HCU Integrated Circuits

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{ V}$):	
STANDARD OUTPUT	±25 mA
BUS DRIVER OUTPUT	±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	
STANDARD OUTPUT	±50 mA
BUS DRIVER OUTPUT	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +60° C (PACKAGE TYPE M)	300 mW
For T_A = +60 to +85° C (PACKAGE TYPE M)	Derate Linearly at 5 mW/° C to 175 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) :	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_o	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	° C
CD54 Types	-55	+125	° C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

Static Electrical Characteristics for CD74HC/CD54HC Types

(Table 1-JEDEC Standard No. 7A)

Symb	Parameter	V_{CC}	Temperature °C						Unit	Test Conditions			
			54HC/74HC 25		74HC − 40 to 85		54HC − 55 to 125						
		v	min	max	min	max	min	max					
V_{IH}	High Level Input Voltage	2.0	1.5		1.5		1.5		v				
		4.5	3.15		3.15		3.15		v				
		6.0	4.2		4.2		4.2		v				
V_{IL}	Low Level Input Voltage	2.0		0.3		0.3		0.3	v				
		4.5		0.9		0.9		0.9	v				
		6.0		1.2		1.2		1.2	v				
										V_I	I_O		
											STD	BUS	Unit
V_{OH} Note 1	High Level Output Voltage	2.0	1.9		1.9		1.9		v	V_{IH} or V_{IL}	− 20.0	− 20.0	µA
		4.5	4.4		4.4		4.4		v		− 20.0	− 20.0	µA
		6.0	5.9		5.9		5.9		v		− 20.0	− 20.0	µA
		4.5	3.98		3.84		3.7		v		− 4.0	− 6.0	mA
		6.0	5.48		5.34		5.2		v		− 5.2	− 7.8	mA
V_{OL}	Low Level Output Voltage	2.0		0.1		0.1		0.1	v	V_{IH} or V_{IL}	20.0	20.0	µA
		4.5		0.1		0.1		0.1	v		20.0	20.0	µA
		6.0		0.1		0.1		0.1	v		20.0	20.0	µA
		4.5		0.26		0.33		0.4	v		4.0	6.0	mA
		6.0		0.26		0.33		0.4	v		5.2	7.8	mA
I_I Note 2	Input Leakage Current	6.0		± 0.1		± 1.0		± 1.0	µA	$V_I = V_{CC}$ or GND			
I_{OZ} Note 3	3-state Output Off-State Current	6.0		± 0.5		± 5.0		± 10.0	µA	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			
I_{CC}	Quiescent Supply Current									$V_I = V_{CC}$ or GND $I_O = 0$			
	SSI	6.0		2.0		20.0		40.0	µA				
	FF	6.0		4.0		40.0		80.0	µA				
	MSI	6.0		8.0		80.0		160.	µA				

Notes:

1. Not applicable to open drain outputs.
2. For digital I/O pins use I_{OZ} limits
3. Also applicable to open drain outputs.

Static Electrical Characteristics for CD74HCT/CD54HCT Types

(Table 2-JEDEC Standard No. 7A)

Symb	Parameter	V_{CC}	Temperature °C						Unit	Test Conditions			
			54HCT/74HCT		74HCT		54HCT						
			25		− 40 to 85		− 55 to 125						
		v	min	max	min	max	min	max					
V_{IH}	High Level Input Voltage	4.5 to 5.5	2.0		2.0		2.0		v				
V_{IL}	Low Level Input Voltage	4.5 to 5.5		0.8		0.8		0.8	v				
										V_I	I_O		
											STD	BUS DRIVER	Unit
V_{OH} Note 1	High Level Output Voltage	4.5	4.4		4.4		4.4		v	V_{IH} or V_{IL}	-20.0	-20.0	μA
		4.5	3.98		3.84		3.7		v		-4.0	-6.0	mA
V_{OL}	Low Level Output Voltage	4.5		0.1		0.1		0.1	v	V_{IH} or V_{IL}	20.0	20.0	μA
		4.5		0.26		0.33		0.4	v		4.0	6.0	mA
I_I Note 2	Input Leakage Current	5.5		± 0.1		± 1.0		± 1.0	μA	$V_I = V_{CC}$ or GND			
I_{OZ} Note 3	3-state Output Off-State Current	5.5		± 0.5		± 5.0		± 10.0	μA	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND			
I_{CC}	Quiescent Supply Current												
	SSI	5.5		2.0		20.0		40.0	μA	$V_I = V_{CC}$ or GND			
	FF	5.5		4.0		40.0		80.0	μA	$I_O = 0$			
	MSI	5.5		8.0		80.0		160.	μA				
ΔI_{CC}	Additional Worst Case Supply Current Note 4	5.5		2.7		2.9		3.0	mA	Per input-pin: $V_I = 2.4V$	Other inputs: at V_{CC} or GND $I_O = 0$		

Notes:

1. Not applicable to open drain outputs.
2. For digital I/O pins use I_{OZ} limits
3. Also applicable to open drain outputs.
4. Total supply current = $I_{CC} + \Sigma\Delta I_{CC}$.

Dynamic Electrical Characteristics

Definitions

Characteristic	Symbol	Limits		Notes
		Max.	Min.	
Propagation Delay:				
Outputs going high to low	t_{PHL}	X		
Outputs going low to high	t_{PLH}	X		
Output Transition Time:				
Outputs going high to low	t_{THL}	X		
Outputs going low to high	t_{TLH}	X		
Pulse Width-Set, Reset, Preset Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}		X	1
Clock Input Frequency	f_{CL}	X		1,2
Clock Input Rise and Fall Time	t_{rCL}, t_{fCL}	X		
Set-Up Time	t_{SU}		X	1
Hold Time	t_{H}		X	1
Removal Time - Set, Reset, Preset-Enable	t_{REM}		X	1
Three State Disable Delay Times:				
High level to high impedance	t_{PHZ}	X		
High impedance to low level	t_{PZL}	X		
Low level to high impedance	t_{PLZ}	X		
High impedance to high level	t_{PZH}	X		

NOTE: (1) By placing a defining min. or max. in front of definition, the limits can change from min. to max., or vice versa.

(2) Clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with the device truth table.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} — Gnd to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than Gnd. Input currents must not exceed 20 mA even when the power supply is off.

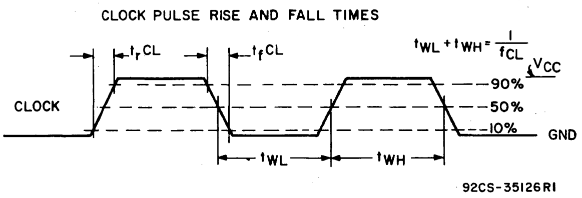
Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or Gnd, whichever is appropriate.

Output Short Circuits

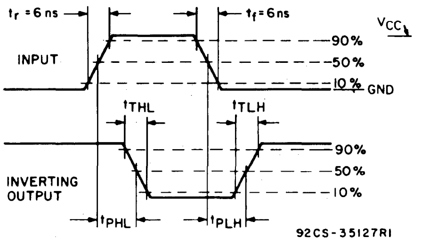
Shorting of outputs to V_{CC} or Gnd may damage CMOS devices by exceeding the maximum device dissipation.

Switching Waveforms for CD54/74HC and CD54/74HCU Integrated Circuits

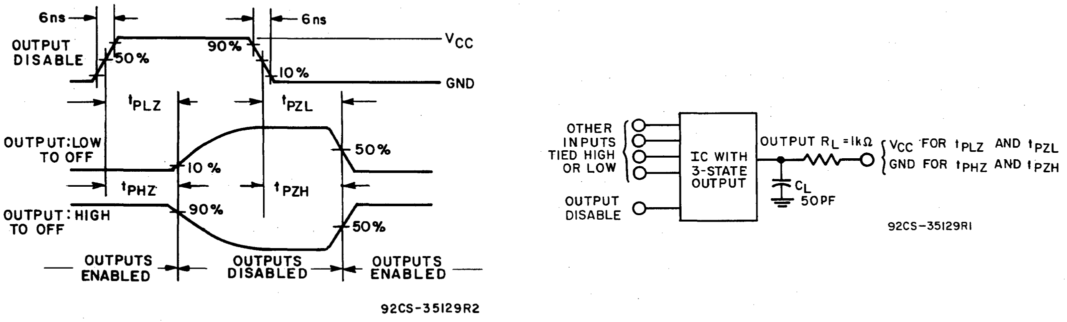


Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{max}, input duty cycle=50%.

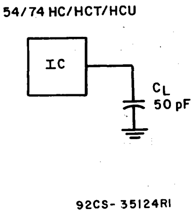
Clock-pulse rise and fall times and pulse width.

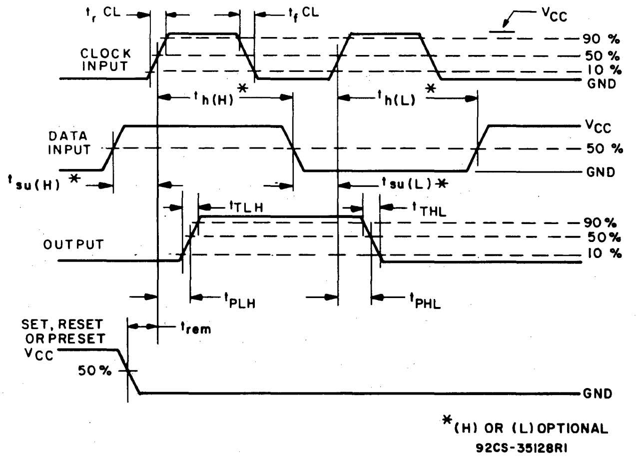


Transition times and propagation delay times, combination logic.



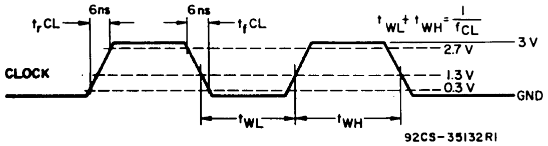
Three-state propagation delay wave shapes and test circuit.





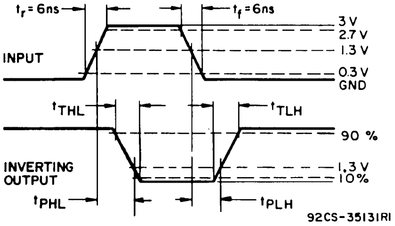
Setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits.

Switching Waveforms for CD54/74HCT Integrated Circuits

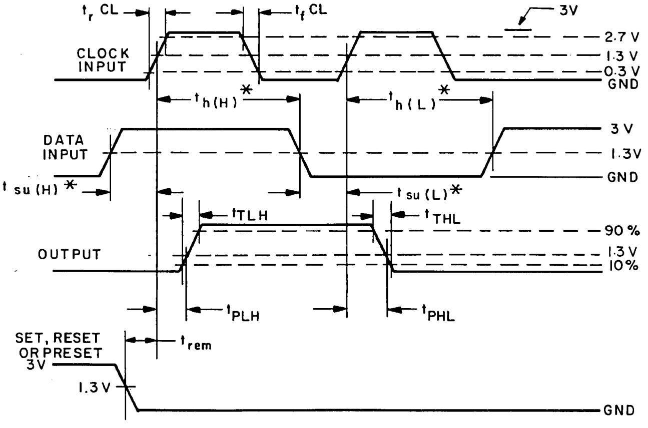


Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{max}, input duty cycle=50%.

Clock-pulse rise and fall times and pulse width.



Transition times and propagation delay times, combination logic.



*(H) OR (L) OPTIONAL

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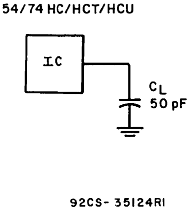
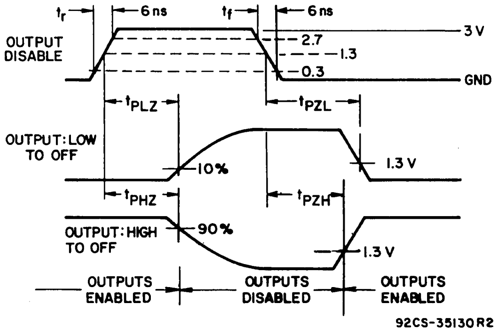
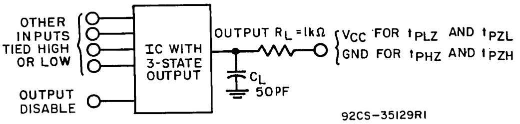
Setup times, hold times, removal time, and propagation delay times for edge triggered sequential logic circuits.







Three-state propagation delay wave shapes and test circuit.

Note:
Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50 pF.

Enhanced Product

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system?

How many devices on each board?

Is the proper device being used for the application?

What are the reliability goals?

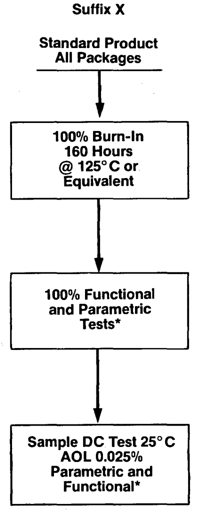
What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in both plastic and frit-seal ceramic packages.
- Offered on the industry's broadest line of circuit functions.
- 0.025% AQL cumulative.
- Reduction in PC board reworking through fewer line rejects.
- Lower warranty requirements through the elimination of infant mortality failures.
- Reduced incoming inspection cost by reduction or complete elimination of test procedures.
- Reduction of system failures and related service expenses and customer complaints.

Screening

Digital IC's (CD Types)



"X" Product

*For the High-Speed CD54/74HC/HCT/HCU products. AC parameters are tested by selecting certain critical propagation delays (which vary from part to part) as indicators of proper AC performance and sample tested to an AQL of 0.025%.

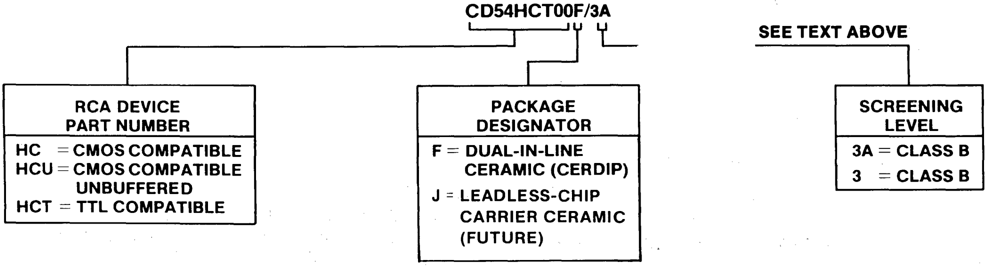
RCA MIL-STD-883 Slash-Series HC/HCT ICs

RCA high-reliability slash-series products are available in both CD54HCXXXX-series and CD54HCTXXXX-series types. These devices are supplied in hermetic dual-in-line frit packages. The CD54HC/HCT (Slash series) types are provided to screening level /3 that corresponds to MIL-STD-883, Method 5004, Class B requirements. This /3 is a non-compliant part using glass die attach. Product is also available as a level /3A which is a fully compliant part using gold eutectic die attach.

Detailed information pertaining to the screening performed can be found in the RCA "High-Reliability Integrated Circuits" DATABOOK, SSD-230B.

Contact your RCA representative for specific timing and availability.

Guide to the Reliability Class and Package of RCA High-Reliability 54HC/HCT Integrated Circuits



High-Speed CMOS Macrocells

High-Speed CMOS (HC/HCT) Macro Cells for RCA Silicon Circuit Board ASIC Design Program

RCA offers a unified Computer-Aided Engineering (CAE) system that supports the high-speed CMOS (HC/HCT QMOS) library of standard logic functions defined as Macro Cells. The system provides not only automatic placement and routing but also the interactive editing of a mixture of CMOS standard cells and rectangular Macro Cells of different sizes.

The HC/HCT Macro Cells are equivalent in performance to the high-speed CMOS HC/HCT series of standard devices as specified in this DATABOOK; only the bond pads have been removed and large drivers down-sized. The Macro Cells are fully characterized and behaviorally described over the operating voltage and temperature ranges. These capabilities provide the system designer a fast, predictable, integration path from a PC board designed with high-speed CMOS or LSTTL, SSI/MSI discrete devices to a single Application-Specific Integrated Circuit (ASIC) that meets all criteria for PC board design.

The Silicon Circuit Board approach to ASIC design is distinctive because it allows the system engineer to develop a circuit using large, predesigned, fully characterized Macros. The characterization data for these Macros provide the engineer with the performance information needed to evaluate the feasibility of differing design approaches quickly and efficiently. The Macros have been developed to provide the optimum performance available within a given technology and are guaranteed to meet these performance specifications over the stated voltage and temperature ranges. All HC/HCT logic functions specified in RCA's QMOS family are included in the Silicon Circuit Board family of logic Macro Cells.

Features of the RCA Silicon Circuit Board and Related User Benefits.

Features:

- Works with 137 high-speed CMOS (QMOS-HC/HCT) standard logic Macro Cells
- Also works with RCA's new ACL standard part Macro Cells
- Intermixes Macros and standard logic function elements providing high-density designs
- Uses double-level metal technology with a polysilicon level option
- Uses fully characterized Macro Cells behaviorally described over the operating voltage and temperature ranges
- Provides simulation based on performance of characterized parts
- Provides fully automatic placement and routing plus interactive editing
- Provides automatic generation of test patterns for use in manufacture
- Integrates with RCA Semicustom FASTRACK system for Standard Cells and Gate Arrays

Benefits:

- Provides high probability of first-time success
- Reduces design development time
- Converts existing HCMOS/TTL boards to CMOS ASICs
- Reduces simulation costs
- Reduces parts costs
- Logic speed increase to x3 or more with high-speed process and ACL Macro Cells

How to Benefit from the RCA Modular Approach to CMOS ASIC Design and Fabrication

The RCA Silicon Circuit Board addresses the most difficult areas in the development of ASICs. These areas are performance, development time, and costs. If the following questions are part of your work assignment in the design of Application-Specific Integrated Circuits, the answers given here will be of significant interest to you.

1. Will the RCA ASIC approach work in my design?

The advantages of the RCA Silicon Circuit Board approach in a specific application can best be determined by a no-cost consultation with our technical staff. We can help you make a reasoned decision whether the RCA modular approach will work in your design. And, if that is the route selected, we will help you save engineering development time and money by working with you on the entire program through to final manufacturing and performance tests.

2. How long will the design take?

The overall development time will be equal to or less than the time normally required for the development of SSI/MSI designs. The RCA Silicon Circuit Board achieves a shortened development time because it incorporates into a design a large number of cells containing from a handful to thousands of gates. Not only is the actual design time reduced, but simulation times also are substantially diminished by the utilization of behavioral modeling of these larger functional levels.

3. Will it work the first time?

The Silicon Circuit Board uses tried and tested high-speed CMOS cells that are fully characterized and behaviorally described. These cells have been developed to provide the optimum performance available within a given technology and are guaranteed to meet those performance specifications over the stated voltage and temperature ranges. Furthermore, RCA will provide any specialized support necessary to assure first-time success.

4. How much will it cost?

This program, involving newly available CAE software and a modular approach, can provide considerable cost savings (as much as 60%) in combined development and die costs. By providing a substantially more efficient methodology for ASIC design, RCA's Silicon Circuit Board greatly reduces engineering development costs. Additionally, the optimized layout of the Macro Cells provides for a significant reduction in the cost of manufacturing the ASIC chip.

How Do I Interface with RCA in Designing a Silicon Circuit Board?

The interface between the RCA Silicon Circuit Board Program and the customer's system engineer is very flexible and can be tailored to fit the specific needs, capabilities, and resources of the customer. Regardless of where the customer enters the system—and it can be anywhere in the flow of the program, as shown in the chart of Fig. 1—RCA will provide the support necessary to assure first-time success in the ASIC design. Following are examples of different interface choices.

One choice is to supply RCA with an SSI/MSI-level schematic, a description of how your circuit works, and timing information so that we can verify its operation in silicon and generate test programs. RCA will handle simulation, placement, routing, mask tooling, and prototype production.

Another choice is for your systems engineer to capture the schematic on a supported popular workstation using a generic SSI/MSI library. Supply RCA with a copy of the schematic, extracted net list, circuit description, and pattern files on magnetic tape or a floppy disk. RCA will then handle the rest.

A third choice is for your system engineer to do all the initial design work on RCA equipment at an RCA Design Center utilizing the assistance and guidance of an RCA applications engineer skilled in ASIC development. Again, RCA will handle the rest.

A fourth choice is for RCA to supply you with the RCA ASIC Design System software tools that will enable you to take your design through the layout step.

For more information on interfacing the RCA Silicon Circuit Board and on the additional benefits this advanced design technology can provide you, contact RCA ASIC Product Marketing at (201) 685-6585 or (201) 685-7119.

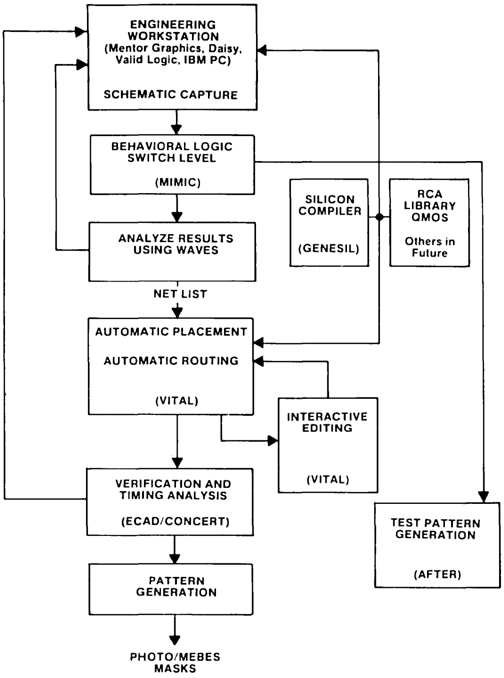


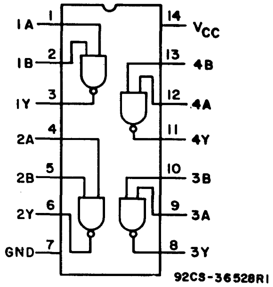
Fig. 1 — Flow Chart of RCA Silicon Circuit Board Design Process

Technical Data

CD54/74HC00
CD54/74HCT00

File Number **1464**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

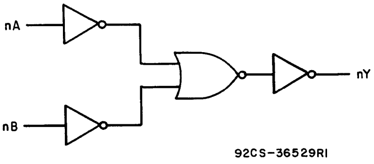
Quad 2-Input NAND Gate

Type Features:

- *Buffered inputs*
- *Typical propagation delay = 7 ns @ V_{CC} = 5V C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC00 and CD54/74HCT00 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC00 and CD54HCT00 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC00 and CD74HCT00 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
    V_{IL}=0.8 V Max., V_{IH}=2 V Min.
  CMOS Input Compatibility
    $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

CD54/74HC00
CD54/74HCT00

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{V}$) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC00
CD54/74HCT00

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC00/CD54HC00										CD74HCT00/CD54HCT00									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level			2	1.5	—	—	1.5	—	1.5	—		4.5								
Input Voltage V_{IH}			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
Low-Level			2	—	—	0.5	—	0.5	—	0.5		4.5								
Input Voltage V_{IL}			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8		5.5								
High-Level	V_{IL}		2	1.9	—	—	1.9	—	1.9	—	V_{IL}									
Output Voltage V_{OH}	or	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	V
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
Low-Level	V_{IL}		2	—	—	0.1	—	0.1	—	0.1	V_{IL}									
Output Voltage V_{OL}	or	0.02	4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	V
CMOS Loads	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
Input Leakage	V_{CC}										Any Voltage Between V_{CC} & Gnd									
Current I_I	or		6	—	—	±0.1	—	±1	—	±1		5.5	—	—	±0.1	—	±1	—	±1	µA
	Gnd																			
Quiescent	V_{CC}										V_{CC}									
Device	or	0	6	—	—	2	—	20	—	40	or	5.5	—	—	2	—	20	—	40	µA
Current I_{CC}	Gnd										Gnd									
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*												4.5								
											V_{CC}-2.1	to	—	100	360	—	450	—	490	µA
												5.5								

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
nA	1.8
nB	1.1

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

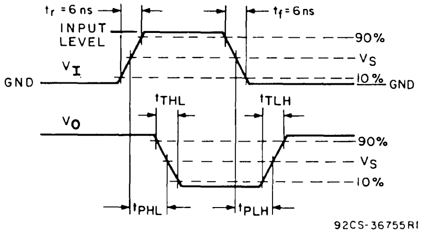
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	Typical		Units
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L=15 pf)	t_{PLH} t_{PHL}	7	8	ns
Power Dissipation Capacitance*	C_{PD}	25	25	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i=input frequency
C_L = output load capacitance
Vcc = supply voltage.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
Input to Output	t_{PHL}	4.5	—	18	—	20	—	23	—	25	—	27	—	30	ns
(Figure 1)		6	—	15	—	—	—	20	—	—	—	23	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
(Figure 1)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—		10		10		10		10		10		10	pF



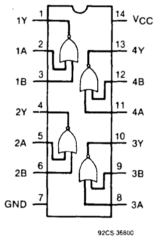
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC02
CD54/74HCT02

File Number **1647**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM and TERMINAL ASSIGNMENT

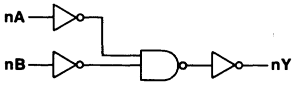
Quad 2-Input NOR Gate

Type Features:

- *Buffered Inputs*
- *Typical Propagation Delay = 7ns @ V_{CC} = 5v, C_L= 15pF, T_A = 25° C*

The RCA-CD54/74HC02 and CD54/74HCT02 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC02 and CD54HCT02 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC02 and CD74HCT02 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-38424RI

LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE		
nA	**nB**	**nY**
L	L	H
L	H	L
H	L	L
H	H	L

CD54/74HC02
CD54/74HCT02

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC02
CD54/74HCT02

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC02/CD54HC02										CD74HCT02/CD54HCT02									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

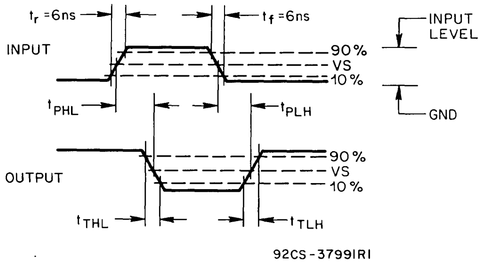
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	15	t_{PLH} t_{PHL}	7	8	ns
Power Dissipation Capacitance*	—	C_{PD}	26	26	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2		90		—		115		—		135		—	
Input to Output	t_{PHL}	4.5		18		21		23		26		27		32	ns
(Fig. 1)		6		15		—		20		—		23		—	
Transition Times	t_{TLH}	2		75		—		95		—		110		—	
(Fig. 1)	t_{THL}	4.5		15		15		19		19		22		22	ns
		6		13		—		16		—		19		—	
Input Capacitance	C_I	—		10		10		10		10		10		10	pF



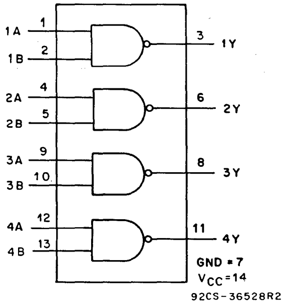
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC03
CD54/74HCT03

File Number **1832**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input NAND Gate With Open Drain

Type Features:

- *Buffered inputs*
- *Typical propagation delay = 8 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*
- *Output pull-up to 10 V*

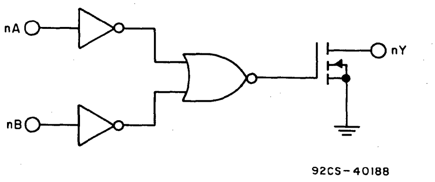
The RCA-CD54/74HC03 and CD54/74HCT03 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

These open-drain NAND gates can drive into resistive loads to output voltages as high as 10 V. Minimum values of R_L required vs. load voltage are shown in Fig. 2.

The CD54HC03 and CD54HCT03 are supplied in 14-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC03 and CD74HCT03 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  - *Standard outputs - 10 LSTTL loads*
  - *Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL input logic compatibility*
    - *V_{IL} = 0.8 V max., V_{IH} = 2 V Min.*
  - *CMOS input compatiblity*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



LOGIC DIAGRAM

TRUTH TABLE

A	B	Y	
L	L	Z #	H *
H	L	Z #	H *
L	H	Z #	H *
H	H	L	

* Requires pull-up (R_L to V_L)

Without pull-up (high impedance)

CD54/74HC03
CD54/74HCT03

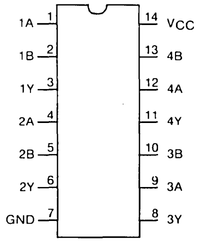
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V)	-20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O$)	-25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Lineary at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input Voltage V_I	0	V_{CC}	V
DC Load Voltage V_L	0	10 #	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
# With pull-up resistor whose value limits output current to 25 mA.



TERMINAL ASSIGNMENT

CD54/74HC03
CD54/74HCT03

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC03/CD54HC03										CD74HCT03/CD54HCT03										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
Output Leakage Current I_{OZ}	V_{IL}	V_O = 10 V thru 1 KΩ	6	—	—	0.5	—	5	—	10	$V_I = V_{IL}$ V_O = 10 V thru 1 KΩ	5.5	—	—	0.5	—	5	—	10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
nA, nB	1

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC03
CD54/74HCT03

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay, (Fig. 1)	t_{PZL}, t_{PLZ}	15	8	9	ns
Power Dissipation Capacitance *	C_{PD}	—	6.4	9	pF

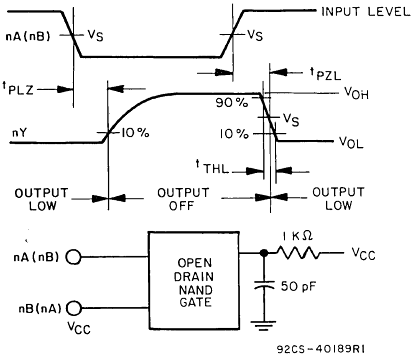
* C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + \Sigma (V_L^2/R_L)$ (Duty Factor "Low")

where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage
Duty factor "low" = percent of time output is "low"
V_L = output voltage
R_L = pull-up resistor

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Output Low to High Impedance and High Impedance to Output Low t_{PLZ} t_{PZL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
	4.5	—	20	—	24	—	25	—	30	—	30	—	36	
	6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times (Figure 1) t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times, propagation delay times, and test circuit.

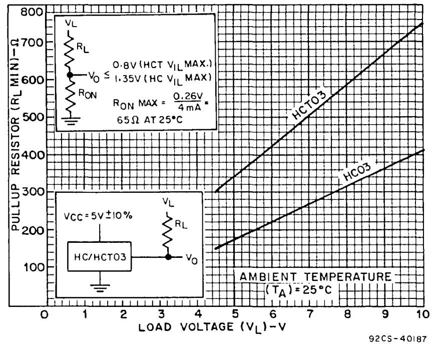
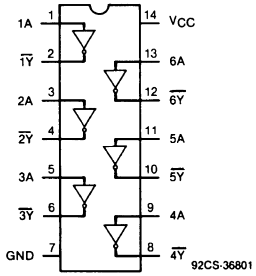


Fig. 2 - Minimum resistive load vs load voltage.

CD54/74HC04
CD54/74HCT04

File Number **1471**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

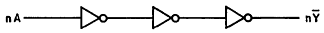
Hex Inverter

Type Features:

- *Input and Output are both buffered*
- *Typical propagation delay = 6 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC04 and CD54/74HCT04 hex inverter utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC04 and CD54HCT04 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC04 and CD74HCT04 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



LOGIC DIAGRAM

TRUTH TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

CD54/74HC04
CD54/74HCT04

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For TA = Full Package Range) VCC:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage VIN, VOUT	0	VCC	V
Operating Temperature TA:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, tr, tf			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC04
CD54/74HCT04

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC04/CD54HC04										CD74HCT04/CD54HCT04									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

***For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.**

HCT Input Loading Table

Input	Unit Loads*
ALL	1.2

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC04
CD54/74HCT04

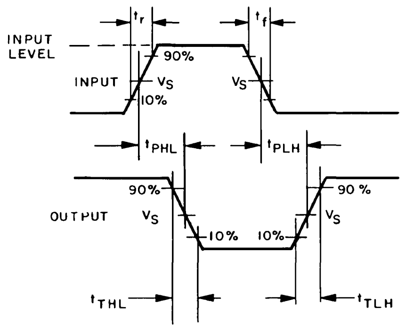
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		Typical		Units
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L = 15 pF)	t_{PLH} t_{PHL}	6	7	ns
Power Dissipation Capacitance*	C_{PD}	21	24	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter where:
$P_D = V_{CC}^2 f (C_{PD} + C_L)$ where f = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	85	—	—	—	105	—	—	—	130	—	—	
Input to Output	t_{PHL}	4.5	—	17	—	19	—	21	—	24	—	26	—	29	ns
(Fig. 1)		6	—	14	—	—	—	18	—	—	—	22	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
(Fig. 1)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50 % V_{CC}	1.3 V

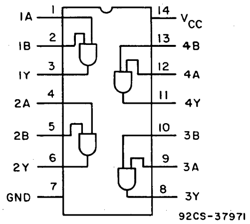
92CS-36948RI

Fig. 1 - Transition times and propagation delay times.

CD54/74HC08
CD54/74HCT08

File Number **1549**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Quad 2-Input AND Gate

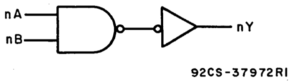
Type Features:

- *Buffered inputs*
- *Typical CD54/74HC08 propagation delay=7 ns @ V_{CC}=5 V, C_L=15 pF, T_A=25° C*

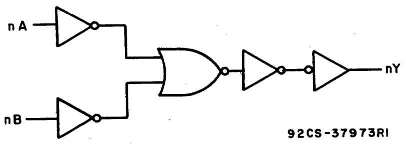
The RCA-CD54/74HC08 and CD54/74HCT08 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC08 and CD54HCT08 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC08 and CD74HCT08 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

LOGIC DIAGRAMS



CD54/74HC08



CD54/74HCT08

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL}=0.8 V Max., V_{IH}=2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

CD54/74HC08
CD54/74HCT08

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_o < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC08
CD54/74HCT08

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC08/CD54HC08										CD74HCT08/CD54HCT08									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or & Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC08
CD54/74HCT08

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L=15 pF)	t_{PLH} t_{PHL}	7	10	ns
Power Dissipation Capacitance*	C_{PD}	37	51	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.

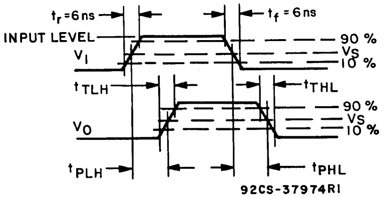
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i=input frequency

C_L=output load capacitance

V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2		90		—		115		—		135		—	ns
		4.5		18		25		23		31		27		38	
		6		25		—		20		—		23		—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2		75		—		95		—		110		—	ns
		4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I			10		10		10		10		10		— 10	pF



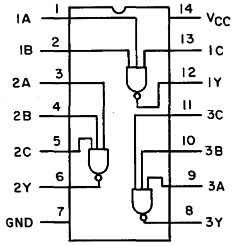
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC10
CD54/74HCT10

File Number **1551**

High-Speed CMOS Logic



92CS-37989

FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

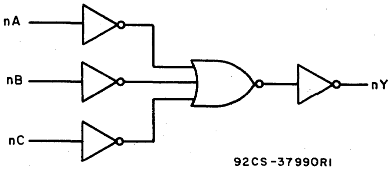
Triple 3-Input NAND Gate

Type Features:

- *Buffered inputs*
- *Typical propagation delay = 8 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC10 and CD54/74HCT10 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC10 and CD54HCT10 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC10 and CD74HCT10 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-37990RI

LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: −40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

CD54/74HC10
CD54/74HCT10

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ + 0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC10
CD54/74HCT10

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC10/CD54HC10										CD74HCT10/CD54HCT10										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V_I V	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

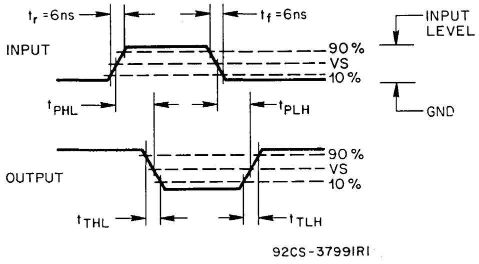
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L=15 pF)	t_{PLH} t_{PHL}	8	9	ns
Power Dissipation Capacitance*	C_{PD}	24	28	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i \ (C_{PD} + C_L)$ where f_i=input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH}	2		100		—		125		—		150		—	ns
	t_{PHL}	4.5		20		24		25		30		30		36	
		6		17		—		21		—		26		—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2		75		—		95		—		110		—	ns
		4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I			10		10		10		10		10		10	pF



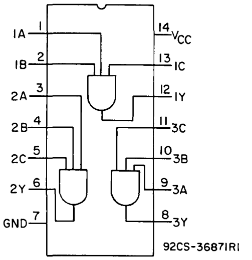
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC11
CD54/74HCT11

File Number **1475**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Triple 3-Input AND Gate

Type Features:

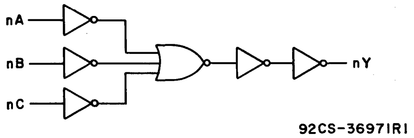
- *Buffered inputs*
- *Typical propagation delay = 8 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC11 and CD54/74HCT11 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC11 and CD54HCT11 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC11 and CD74HCT11 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout [Over Temperature Range]:*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Phillips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



LOGIC DIAGRAM

TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... –0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) .... ±20 mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_o < -0.5V$ OR $V_o > V_{CC} + 0.5V$) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5V < V_o < V_{CC} + 0.5V$) .... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to+85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = –55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... –55 to +125°C
PACKAGE TYPE E, M .... –40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC11
CD54/74HCT11

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC11/CD54HC11										CD74HCT11/CD54HCT11										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or & Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	0.50

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
		4.5	—	20	—	28	—	25	—	35	—	30	—	42	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	Typical		Units
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L = 15 pF)	t_{PLH} t_{PHL}	8	11	ns
Power Dissipation Capacitance*	C_{PD}	26	28	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

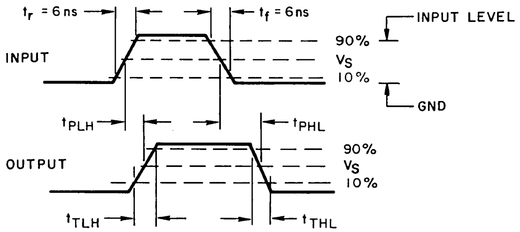


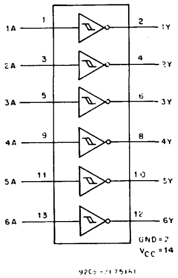
Fig. 1 — Transition times and propagation delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

CD54/74HC14
CD54/74HCT14

File Number **1781**

High-Speed CMOS Logic



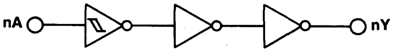
FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Hex Inverting Schmitt Trigger

Type Features:
- *Unlimited input rise and fall times*
- *Exceptionally high noise immunity*

The RCA-CD54/74HC14 and CD54/74HCT14 each contain 6 inverting Schmitt Triggers in one package.

The CD54HC14 and CD54HCT14 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC14 and CD74HCT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM

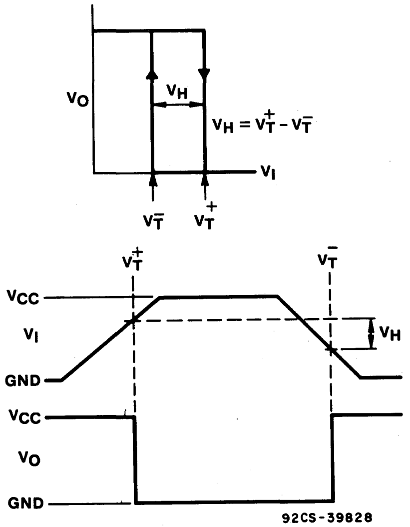


Fig. 1 - Hysteresis definition, characteristic, and test setup.

Family Features:
- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - N_{IL} = 37%, N_{IH} = 51% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - N_{IL} = 18%, N_{IH} = 67% of V_{CC} @ V_{CC} = 4.5V
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High Level
L = Low Level

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC14
CD54/74HCT14

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC14/CD54HC14									CD74HCT14/CD54HCT14								UNITS
	TEST CONDITIONS			74HC/54HC TYPES		74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES		74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C		-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C		-40/ +85°C		-55/ +125°C		
				Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
Input Switch Points V_T+			2	0.7	1.5	0.7	1.5	0.7	1.5			—	—	—	—	—	—	V
			4.5	1.7	3.15	1.7	3.15	1.7	3.15		4.5	1.2	1.9	1.2	1.9	1.2	1.9	
			6	2.1	4.2	2.1	4.2	2.1	4.2		5.5	1.4	2.1	1.4	2.1	1.4	2.1	
V_T-			2	0.3	1	0.3	1	0.3	1			—	—	—	—	—	—	V
			4.5	0.9	2.2	0.9	2.2	0.9	2.2		4.5	0.5	1.2	0.5	1.2	0.5	1.2	
			6	1.2	3	1.2	3	1.2	3		5.5	0.6	1.4	0.6	1.4	0.6	1.4	
V_H			2	0.2	1	0.2	1	0.2	1			—	—	—	—	—	—	V
			4.5	0.4	1.4	0.4	1.4	0.4	1.4		4.5	0.4	1.4	0.4	1.4	0.4	1.4	
			6	0.6	1.6	0.6	1.6	0.6	1.6		5.5	0.4	1.5	0.4	1.5	0.4	1.5	
High-Level Output Voltage V_{OH} CMOS Loads	V_T- or V_T+	-0.02	2	1.9	—	1.9	—	1.9	—	V_T- or V_T+		—	—	—	—	—	—	V
			4.5	4.4	—	4.4	—	4.4	—		4.5	4.4	—	4.4	—	4.4	—	
			6	5.9	—	5.9	—	5.9	—			—	—	—	—	—	—	
TTL Loads	V_T- or V_T+		—	—	—	—	—	—	—	V_T- or V_T+		—	—	—	—	—	—	V
		-4	4.5	3.98	—	3.84	—	3.7	—		4.5	3.98	—	3.84	—	3.7	—	
		-5.2	6	5.48	—	5.34	—	5.2	—			—	—	—	—	—	—	
Low-Level Output Voltage V_{OL} CMOS Loads	V_T- or V_T+	0.02	2	—	0.1	—	0.1	—	0.1	V_T- or V_T+		—	—	—	—	—	—	V
			4.5	—	0.1	—	0.1	—	0.1		4.5	—	0.1	—	0.1	—	0.1	
			6	—	0.1	—	0.1	—	0.1			—	—	—	—	—	—	
TTL Loads	V_T- or V_T+			—	—	—	—	—	—	V_T- or V_T+		—	—	—	—	—	—	V
		4	4.5	—	0.26	—	0.33	—	0.4		4.5	—	0.26	—	0.33	—	0.4	
		5.2	6	—	0.26	—	0.33	—	0.4			—	—	—	—	—	—	
Input Leakage Current I_I	V_{CC} or Gnd		6	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*										V_{CC}-2.1	4.5 to 5.5	Min —	Typ Max 100 360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
nA	0.6

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC14
CD54/74HCT14

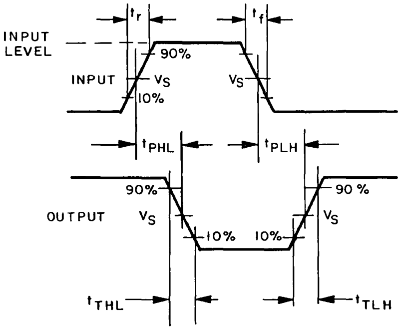
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay, A to Y	t_{PHL}, t_{PLH}	15	11	16	ns
Power Dissipation Capacitance*	C_{PD}	—	20	20	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	ns
A to Y	t_{PHL}	4.5	—	27	—	38	—	34	—	48	—	41	—	57	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Output	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
Transition Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3 V

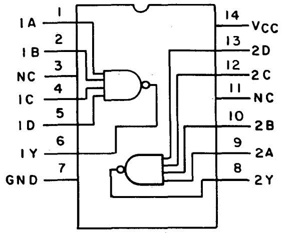
92CS-36948RI

Fig. 2 - Transition times and propagation delay times.

CD54/74HC20
CD54/74HCT20

File Number **1601**

High-Speed CMOS Logic



92CS-38338

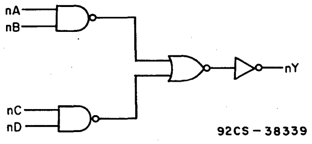
FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Dual 4-Input NAND Gate

Type Features:
- *Buffered inputs (HCT types)*
- *Typical propogation delay=8 ns @ V_{CC}=5V, C_L=15 pF, T_A=25°C (HC types)*

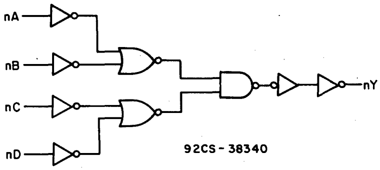
The RCA-CD54/74HC20 and CD54/74HCT20 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC20 and CD54HCT20 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC20 and CD74HCT20 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-38339

HC LOGIC DIAGRAM (1 GATE)



92CS-38340

HCT LOGIC DIAGRAM (1 GATE)

Family Features
- *Fanout (over temperature range):*
  Standard outputs — 10 LSTTL loads
  Bus driver outputs — 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X = Don't Care
L = Low Voltage Level
H = High Voltage Level

CD54/74HC20
CD54/74HCT20

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	± 20 mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} +0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f			ns
at 2V	0	1000	
at 4.5 V	0	500	
at 6V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC20
CD54/74HCT20

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC20/CD54HC20										CD74HCT20/CD54HCT20									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

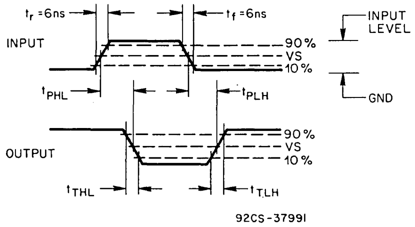
CHARACTERISTIC	SYMBOL	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L = 15 pF)	t_{PLH} t_{PHL}	8	11	ns
Power Dissipation Capacitance*	C_{PD}	26	38	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
		4.5	—	20	—	28	—	25	—	35	—	30	—	42	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



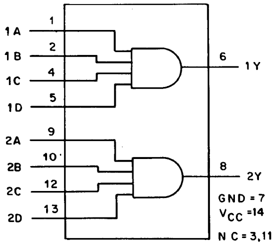
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3V

Fig. 1 — Transition times and propagation delay times.

CD54/74HC21
CD54/74HCT21

File Number **1782**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

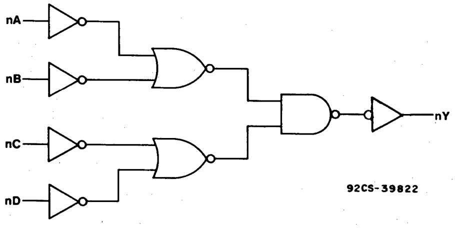
Dual 4-Input AND Gate

Type Features:
- *Buffered inputs*
- *Typical propagation delay = 9ns*
  @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C (HC types)

The RCA-CD54/74HC21 and CD54/74HCT21 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC21 and CD54HCT21 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC21 and CD74HCT21 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



LOGIC DIAGRAM

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X = Don't Care
L = Low Level Voltage
H = High Level Voltage

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC21
CD54/74HCT21

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC21/CD54HC21										CD74HCT21/CD54HCT21										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1		µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40		µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490		µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	1

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

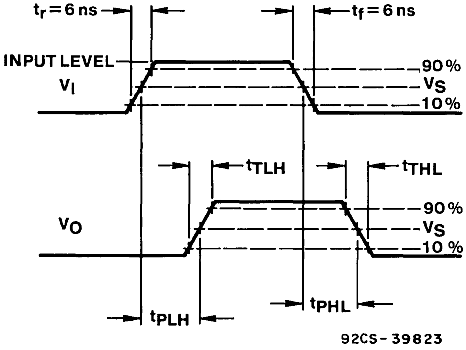
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	t_{PHL}, t_{PLH}	15	9	11	ns
Power Dissipation Capacitance*	C_{PD}	—	36	42	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
Input to Output	t_{PHL}	4.5	—	22	—	27	—	28	—	34	—	33	—	41	
(Fig. 1)		6	—	19	—	—	—	24	—	—	—	28	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
(Fig. 1)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



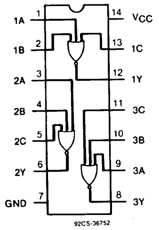
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 — Transition times and propagation delay times.

CD54/74HC27
CD54/74HCT27

File Number **1648**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Triple 3-Input NOR Gate

Type Features:

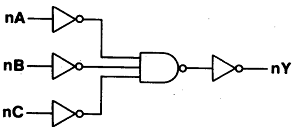
- *Buffered Inputs*
- *Typical CD54/74HC27 Propagation Delay = 7ns @ V_{CC} = 5v, C_L= 15pF, T_A = 25° C*

The RCA-CD54/74HC27 and CD54/74HCT27 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC27 and CD54HCT27 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC27 and CD74HCT27 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-38425

LOGIC DIAGRAM

TRUTH TABLE

nA	nB	nC	nY
L	L	L	H
L	L	H	L
L	H	L	L
H	L	L	L
H	H	L	L
L	H	H	L
H	L	H	L
H	H	H	L

92CS-38425

L = Low Level
H = High Level

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC27
CD54/74HCT27

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC27/CD54HC27										CD74HCT27/CD54HCT27									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

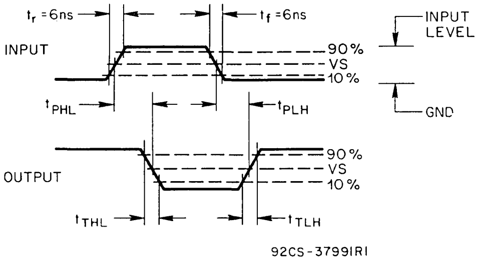
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	15	t_{PLH} t_{PHL}	7	9	ns
Power Dissipation Capacitance*	—	C_{PD}	26	28	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2		95		—		120		—		145		—	ns
		4.5		19		23		24		29		29		35	
		6		16		—		20		—		25		—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2		75		—		95		—		110		—	ns
		4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I		—	10		10		10		10		10		10	pF



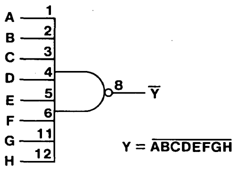
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC30
CD54/74HCT30

File Number **1652**

High-Speed CMOS Logic



92CS-38426

FUNCTIONAL DIAGRAM

8-Input NAND Gate

Type Features:

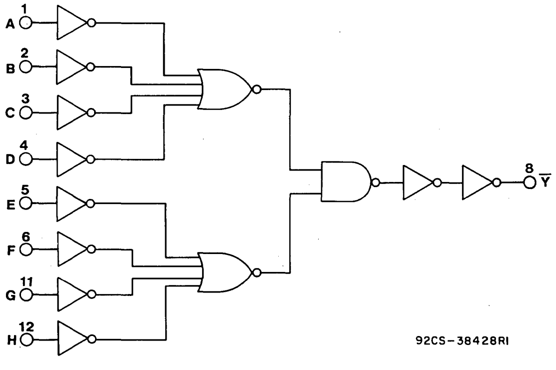
- *Buffered inputs and outputs*
- *Typical propagation delay = 10 ns @ V_{CC}= 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC30 and CD54/74HCT30 each contain an eight-input NAND gate in one package. They provide the system designer with the direct implementation of the positive logic 8-input NAND function.

The CD54HC/HCT30 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT30 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



92CS-38428RI

LOGIC DIAGRAM

TRUTH TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	$\overline{Y}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

CD54/74HC30
CD54/74HCT30

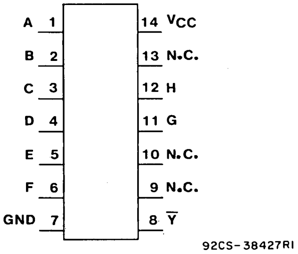
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{V}$) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E. M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC30
CD54/74HCT30

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC30/CD54HC30										CD74HCT30/CD54HCT30									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

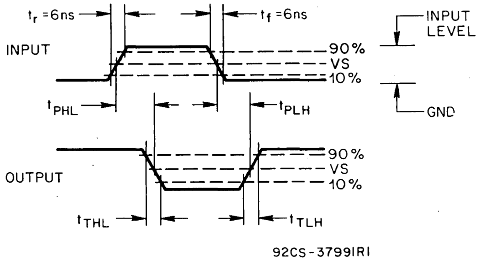
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output $\overline{Y}$ (Fig. 1)	15	t_{PLH} t_{PHL}	10	11	ns
Power Dissipation Capacitance*	—	C_{PD}	25	26	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
PD = V_{CC}^2 f_i (C_{PD} + C_L)
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2		130		—		165		—		195		—	ns
		4.5		26		28		33		35		39		42	
		6		22		—		28		—		33		—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2		75		—		95		—		110		—	ns
		4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I		—	10		10		10		10		10		10	pF



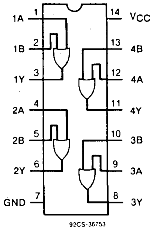
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC32
CD54/74HCT32

File Number **1643**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Quad 2-Input OR Gate

Type Features:

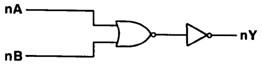
- *Typical propagation delay = 7 ns*
  @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C (HC32)

The RCA-CD54/74HC32 and CD54/74HCT32 contain four 2-input OR gates in one package.

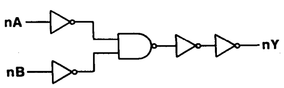
The CD54HC/HCT32 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT32 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



CD54/74HC32



CD54/74HCT32

92CS-38435

Fig. 1 - Logic diagrams.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level.
L = LOW voltage level.

CD54/74HC32
CD54/74HCT32

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC32
CD54/74HCT32

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC32/CD54HC32										CD74HCT32/CD54HCT32									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	1.5

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC32
CD54/74HCT32

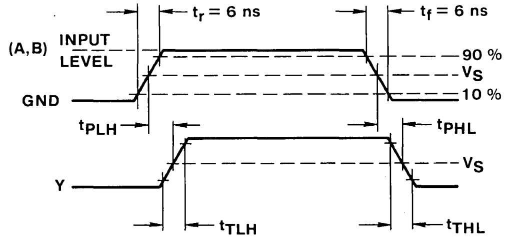
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay A, B to Y	15	t_{PLH} t_{PHL}	7	9	ns
Power Dissipation Capacitance	—	C_{PD}*	22	22	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = f_i V_{CC}^2 (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2		90		—		115		—		135		—	ns
A, B to Y	t_{PHL}	4.5		18		24		23		30		27		36	
Figure 2		6		15		—		20		—		23		—	
Transition Times	t_{TLH}	2		75		—		95		—		110		—	ns
	t_{THL}	4.5		15		15		19		19		22		22	
Figure 2		6		13		—		16		—		19		—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



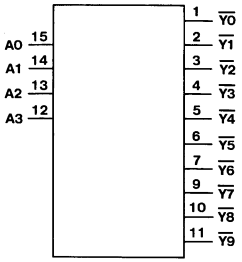
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.

CD54/74HC42
CD54/74HCT42

File Number **1689**

High-Speed CMOS Logic



92CS-38860
FUNCTIONAL DIAGRAM

BCD to Decimal Decoder (1-of-10)

Type Features:

- *Buffered inputs and outputs*
- *Typical propagation delay = 12 ns @ V_{CC} = 5V, C_L = 15 pF T_A = 25° C (HC42)*

The RCA-CD54/74HC42 and CD54/74HCT42 BCD-to-Decimal Decoders utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL decoders with the low power consumption of standard CMOS integrated circuits. These devices have the capability of driving 10 LSTTL loads and are compatible with the standard 54LS /74LS logic family. One of ten outputs (low on select) is selected in accordance with the BCD input. Non-valid BCD inputs result in none of the outputs being selected (all outputs are high).

The CD54HC42 and CD54HCT42 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC42 and CD74HCT42 are supplied in 16-lead dual-in-line plastic packages (E suffix), and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

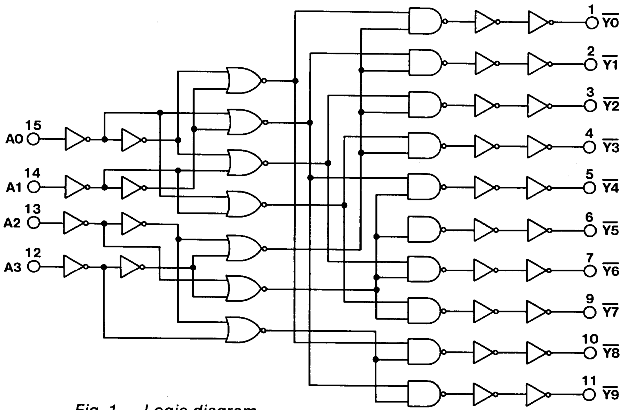
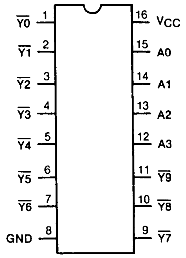


Fig. 1 — Logic diagram

92CS-38861



92CS-38869

TERMINAL ASSIGNMENT

CD54/74HC42
CD54/74HCT42

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE

Inputs				Outputs									
A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

L = Low Voltage Level
H = High Voltage Level

CD54/74HC42
CD54/74HCT42

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC42/CD54HC42										CD74HCT42/CD54HCT42									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage. Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC42
CD54/74HCT42

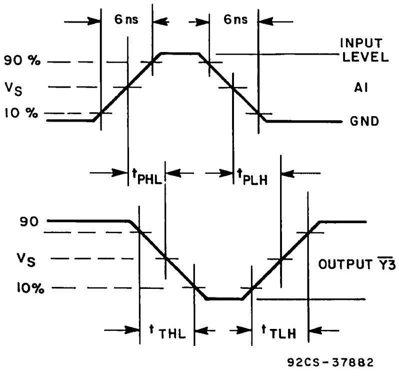
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Any Input to $\overline{Y}$	15	t_{PHL}, t_{PLH}	12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	65	70	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Any Input to $\overline{Y}$	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input			—	—	—	—	—	—	—	—	—	—	—	—	
Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
			—	—	—	—	—	—	—	—	—	—	—	—	

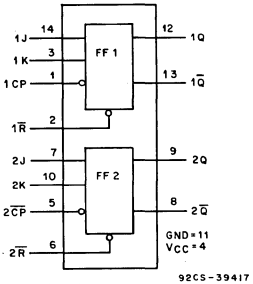


	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Transition times and propagation delay times.

CD54/74HC73
CD54/74HCT73

File Number **1721**



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Reset
Negative-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical $f_{max} = 60MHz$ @ $V_{cc} = 5V$, $C_L = 15pF$, $T_A = 25°C$*

The RCA-CD54/74HC73 and CD54/74HCT73 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low-level input. This device is functionally identical to the HC/HCT 107 but differs in terminal assignment and in some parametric limits.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC73 and CD54HCT73 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC73 and CD74HCT73 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}, @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
  CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

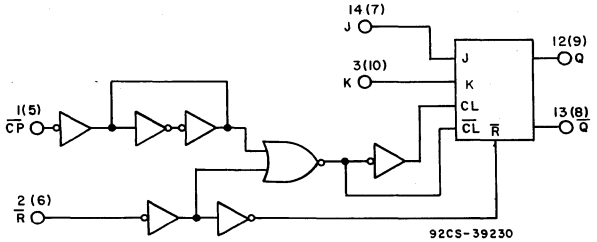


Fig. 1 - Logic diagram.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↘	L	L	No change	
H	↘	H	L	H	L
H	↘	L	H	L	H
H	↘	H	H	Toggle	
H	H	X	X	No change	

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↘ = High-to-Low transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5V < V_O < V_{CC} + 0.5$ V) .... ± 25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

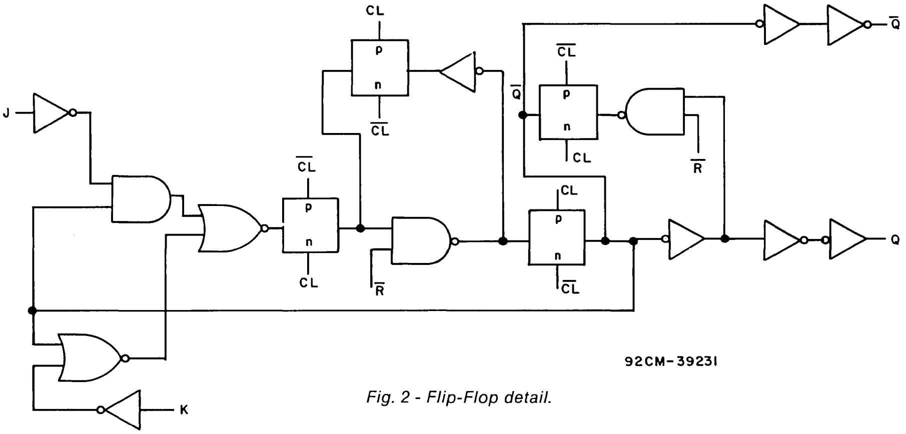


Fig. 2 - Flip-Flop detail.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f†			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.
†Applicable for all inputs except clock.

CD54/74HC73
CD54/74HCT73

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC73, CD54HC73										CD74HCT73, CD54HCT73									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

* For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

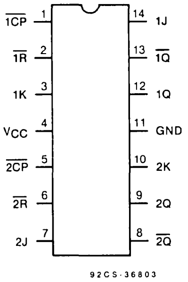
SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay $\overline{CP}$ to Q	t_{PLH} t_{PHL}	15	13	16	ns
$\overline{CP}$ to $\overline{Q}$			13	15	ns
$\overline{R}$ to Q, $\overline{Q}$			12	14	ns
$\overline{CP}$ Frequency	f_{max}	15	60	60	MHz
Power Dissipation Capacitance*	C_{PD}	—	28	28	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 fo$ where fi = input frequency, fo = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	Max.	HCT Min.	Max.	-40°C to +85°C 74HC Min.	Max.	74HCT Min.	Max.	-55°C to +125°C 54HC Min.	Max.	54HCT Min.	Max.	UNITS
Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{CP}$	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{R}$	4.5	16	—	18	—	20	—	23	—	24	—	27	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	
J, K to $\overline{CP}$	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
J, K to $\overline{CP}$	4.5	3	—	3	—	3	—	3	—	3	—	3	—	ns
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	
	4.5	16	—	12	—	20	—	15	—	24	—	18	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{CP}$ Frequency f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	
	4.5	30	—	30	—	25	—	25	—	20	—	20	—	MHz
	6	35	—	—	—	29	—	—	—	23	—	—	—	

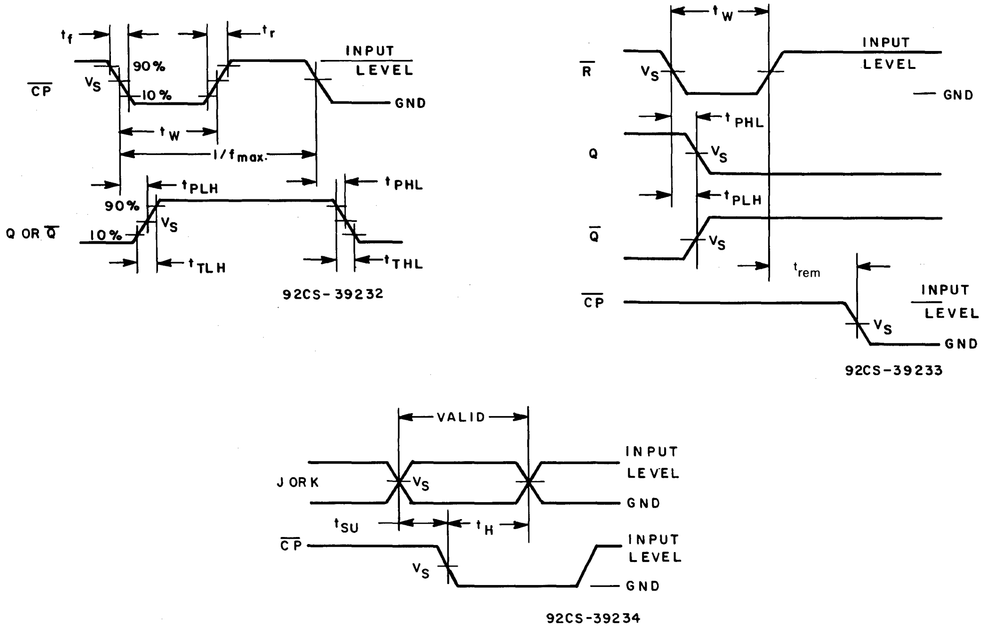


TERMINAL ASSIGNMENT

CD54/74HC73
CD54/74HCT73

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input t_r, $t_f = 6$ ns)

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}, t_{PHL} $\overline{CP}$ to Q	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
	4.5	—	32	—	38	—	40	—	48	—	48	—	57	
	6	—	28	—	—	—	34	—	—	—	41	—	—	
$\overline{CP}$ to $\overline{Q}$	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
	4.5	—	32	—	36	—	40	—	45	—	48	—	54	
	6	—	28	—	—	—	34	—	—	—	41	—	—	
$\overline{R}$ to Q, $\overline{Q}$	2	—	145	—	—	—	180	—	—	—	220	—	—	ns
	4.5	—	29	—	34	—	36	—	43	—	44	—	51	
	6	—	25	—	—	—	31	—	—	—	38	—	—	
Output Transition Time t_{TLH}, t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



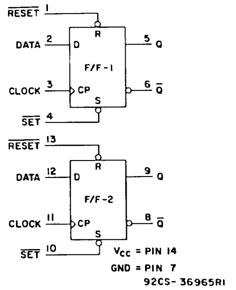
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 - Transition times, propagation delay times, and setup and hold times.

File Number **1476**

CD54/74HC74
CD54/74HCT74

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual D Flip-Flop with Set and Reset

Positive-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Set and Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical $f_{max} = 50$ MHz @ $V_{CC} = 5V$, $C_L = 15$ pF, $T_A = 25°C$*

The RCA-CD54/74HC74 and CD54/74HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC74 and CD54HCT74 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC74 and CD74HCT74 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

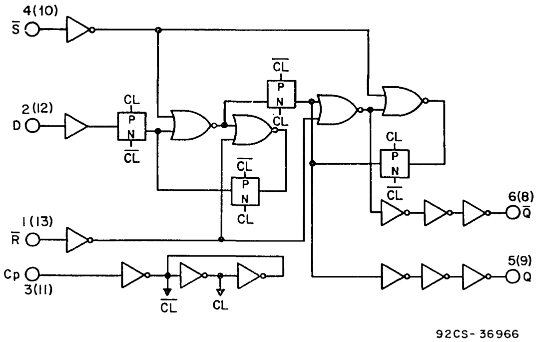


Fig. 1 — Logic Diagram

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to + 85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from Low to High level

NOTES: QO = the level of Q before the indicated input conditions were established.

*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

CD54/74HC74
CD54/74HCT74

MAXIMUM RATINGS, *Absolute-Maximum Values:*

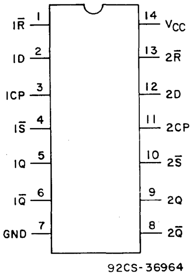
DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	−40	+85	°C
CD54 Types	−55	+125	°C
Input Rise and Fall Times t_r, t_f•			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

•Applicable for all inputs except clock.



TERMINAL ASSIGNMENT

CD54/74HC74
CD54/74HCT74

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC74/CD54HC74										CD74HCT74/CD54HCT74									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D	0.5
$\overline{R}$	0.5
CP	0.7
$\overline{S}$	0.75

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC74
CD54/74HCT74

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay	t_{PLH} t_{PHL}				
CP to Q, $\overline{Q}$ (Fig. 2)		15	14	14	ns
$\overline{R}$ to Q, $\overline{Q}$ (Fig. 3)			17	17	
$\overline{S}$ to Q, $\overline{Q}$ (Fig. 3)			17	17	
CP Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	30	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Data to CP t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
Set-up Time	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
(Fig. 4)	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
(Fig. 4)	6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time t_{REM}	2	30	—	—	—	40	—	—	—	45	—	—	—	
$\overline{R}$, $\overline{S}$ to CP	4.5	6	—	6	—	8	—	8	—	9	—	9	—	
(Fig. 3)	6	5	—	—	—	7	—	—	—	8	—	—	—	
Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{R}$, $\overline{S}$	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
(Figs. 2, 3)	6	14	—	—	—	17	—	—	—	20	—	—	—	
Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
CP	4.5	16	—	18	—	20	—	23	—	24	—	27	—	
(Figs. 2, 3)	6	14	—	—	—	17	—	—	—	20	—	—	—	
CP Frequency f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	25	—	25	—	20	—	20	—	16	—	
	6	35	—	—	—	29	—	—	—	23	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V_{CC} (V)	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
CP to Q, $\overline{Q}$ t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
(Fig. 2)	6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$ t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
t_{PLH}	4.5	—	40	—	40	—	50	—	50	—	60	—	60	
(Fig. 3)	6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Times t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
(Fig. 5)	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

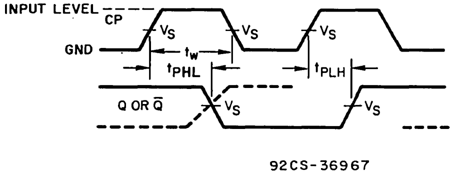


Fig. 2 — Clock pre-requisite and propagation delays.

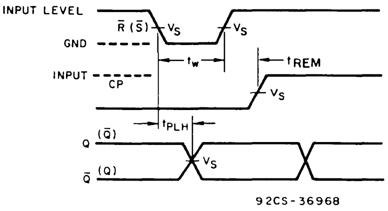


Fig. 3 — $\overline{\text{Reset}}$ or $\overline{\text{Set}}$ pre-requisite and propagation delays

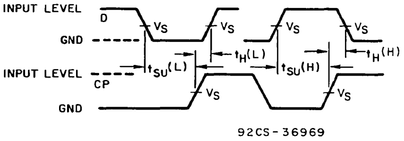


Fig. 4 — Data pre-requisite times.

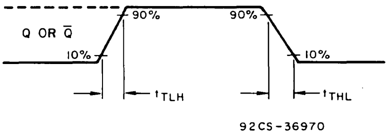


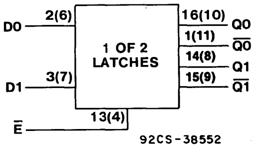
Fig. 5 — Output transition times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

CD54/74HC75
CD54/74HCT75

File Number **1666**

Dual 2-Bit Bistable Transparent Latch



FUNCTIONAL DIAGRAM

Type Features:

- *True and Complementary Outputs*
- *Buffered Inputs and Outputs*

The RCA-CD54/74HC75 and CD54/74HCT75 are dual 2-bit bistable transparent latches. Each one of the 2-bit latches is controlled by separate Enable inputs ($\overline{1E}$ and $\overline{2E}$) which are active LOW. When the Enable input is HIGH data enters the latch and appears at the Q output. When the Enable input ($\overline{1E}$ and $\overline{2E}$) is LOW the output is not affected.

The CD54HC/HCT75 are supplied in 16-lead hermetic dual-in-line packages (F suffix). The CD74HC/HCT75 are supplied in 16-lead dual-in-line plastic package (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: —40 to + 85°C
- *Balanced Propagation delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noice Immunity: N_{IL} *= 30%,* N_{IH} *= 30% of* V_{CC}*;* *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\,\mu A$ *@* V_{OL}, V_{OH}

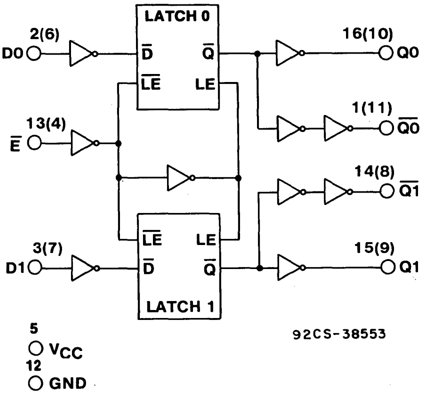


Fig. 1 - Logic Diagram

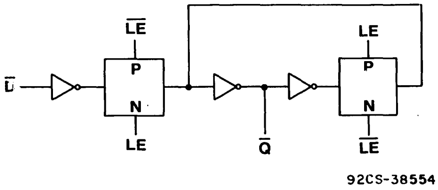


Fig. 2 - Latch Detail

CD54/74HC75
CD54/74HCT75

MAXIMUM RATINGS, *Absolute-Maximum Values:*

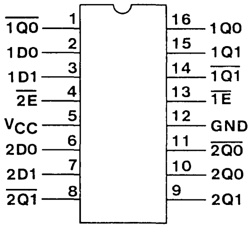
DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ OR $V_O > V_{CC}$ +0.5 V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	
CD54 Types	-55	+125	°C
input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

TRUTH TABLE

Inputs		Outputs	
D	**$\overline{E}$**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q0	$\overline{Q0}$

H = High Level
L = Low Level
X = Don't Care
Q0 = The level of Q before the transition of $\overline{E}$.

CD54/74HC75
CD54/74HCT75

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC75/CD54HC75										CD74HCT75/CD54HCT75									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_1 V	Io mA	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_1 V	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	Vcc or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between Vcc & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	Vcc or Gnd	0	6	—	—	4	—	40	—	80	Vcc or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											Vcc-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DO, D1	**0.8**
$\overline{1E}$, $\overline{2E}$	**1.2**

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6ns)

CHARACTERISTIC		C_L (pF)	SYMBOL	TYPICAL		UNITS
				HC75	HCT75	
Propagation Delay	D to Q	15	t_{PLH}	9	11	ns
	D to $\overline{Q}$	15		10	11	ns
	Enable to Q	15	t_{PHL}	10	11	ns
	Enable to $\overline{Q}$	15		11	12	ns
Power Dissipation Capacitance*		—	C_{PD}	46	46	pF

*C_{PD} is used to determine the dynamic power consumption per latch.
$PD = V_{CC}^2 \, fi \, (C_{PD} + C_L)$
fi = Input Frequency
C_L = Load Capacitance
V_{CC} = Supply Voltage

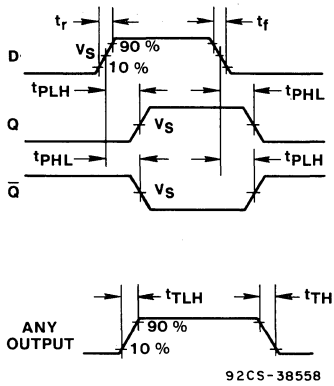
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to + 85°C				-55°C to + 125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width t_W	2	80		—		100		—		120		—		ns
Enable Input	4.5	16		16		20		20		24		24		
	6	14		—		17		—		20		—		
Setup Time t_{SU}	2	60		—		75		—		90		—		ns
D to Enable	4.5	12		12		15		15		18		18		
	6	10		—		13		—		15		—		
Hold Time t_h	2	3		—		3		-		3		—		ns
Enable to D	4.5	3		3		3		3		3		3		
	6	3		—		3		—		3		—		

CD54/74HC75
CD54/74HCT75

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to + 85°C				-55°C to + 125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Q	t_{PLH} t_{PHL}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
		4.5	—	22	—	28	—	28	—	35	—	33	—	42	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay Data to $\overline{Q}$	t_{PLH} t_{PHL}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
		4.5	—	26	—	28	—	33	—	35	—	39	—	42	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Propagation Delay Enable to Q	t_{PLH} t_{PHL}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
		4.5	—	26	—	28	—	33	—	35	—	39	—	42	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Propagation Delay Enable to $\overline{Q}$	t_{PLH} t_{PHL}	2	—	130	—	—	—	165	—	—	—	195	—	—	ns
		4.5	—	26	—	30	—	33	—	38	—	39	—	45	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



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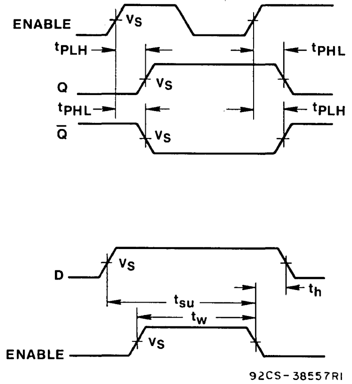

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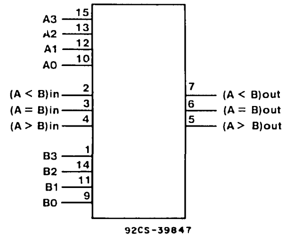
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1770**

CD54/74HC85
CD54/74HCT85

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Magnitude Comparator

Type Features:

- *Buffered inputs and outputs*
- *Typical propagation delay = 13 ns (Data to Output) @ $V_{CC} = 5V$, $C_L = 15$ pF, $T_A = 25°C$*
- *Serial or Parallel expansion without external gating.*

The RCA-CD54/74HC/HCT85 are high-speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

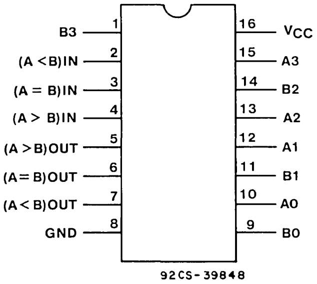
These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs (A > B, A < B, and A = B). The 4-bit input words are weighted (A0 to A3 and B0 to B3), where A3 and B3 are the most significant bits.

The HC/HCT85 are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially-expanded application. The parallel expansion scheme is described by the last three entries in the truth table. Circuits for serial and parallel comparison of 12 bits are shown in figures 3 and 4, respectively.

The CD54HC/HCT85 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT85 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT/HCU: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
  - *$N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
  - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



TERMINAL ASSIGNMENT

CD54/74HC85
CD54/74HCT85

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
 (Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
 For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
 For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
 For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
 For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
 PACKAGE TYPE F, H .... -55 to +125°C
 PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
 Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
 with solder contacting lead tips only .... +300°C

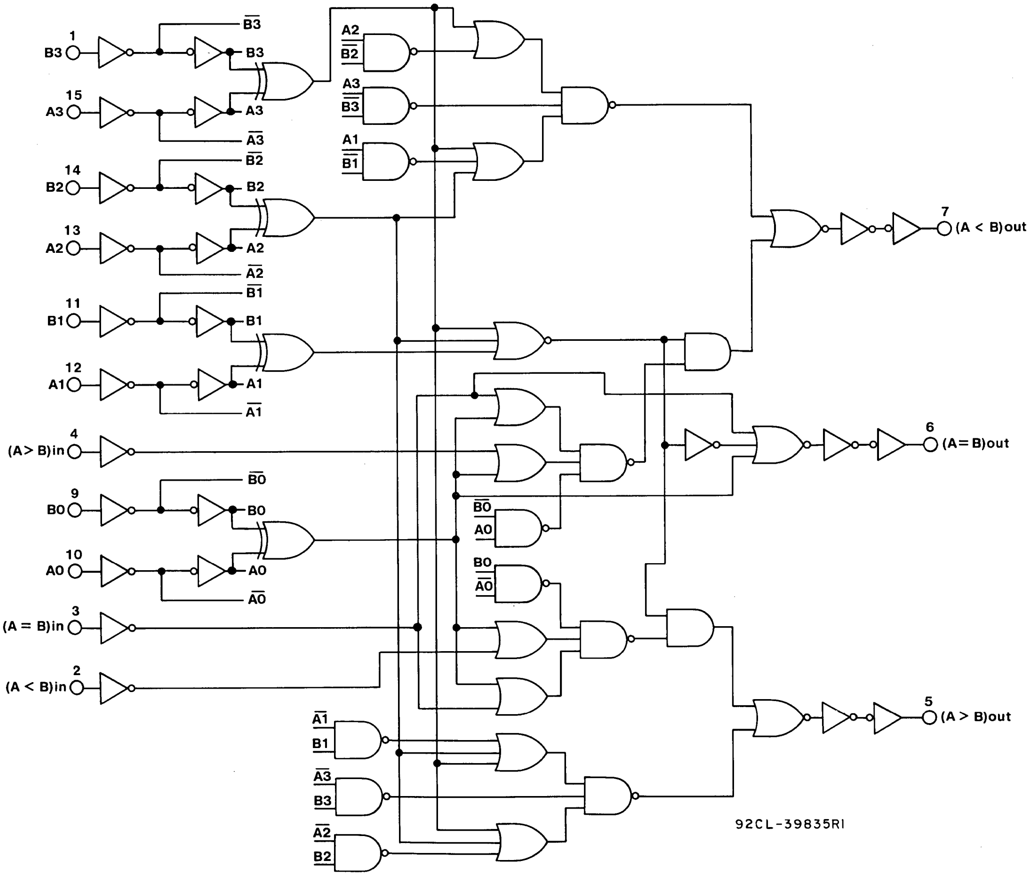


Fig. 1 - Logic diagram

TRUTH TABLE

Comparing Inputs				Cascading Inputs			Outputs			
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**	**A > B**	**A < B**	**A = B**	
A3 > B3	X	X	X	X	X	X	H	L	L	single device or series cascading
A3 < B3	X	X	X	X	X	X	L	H	L	
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L	
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L	
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H	parallel cascading
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L	

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:* CD54/74HC Types CD54/74HCT Types	 2 4.5	 6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: CD74 Types CD54 Types	 -40 -55	 +85 +125	°C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	 0 0 0	 1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC85
CD54/74HCT85

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC85/CD54HC85										CD74HCT85/CD54HCT85									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

* For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0-A3, B0-B3 and (A=B) in	1.5
(A>B) in, (A<B) in	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A 25°C, Input t_r, t_f = 6 ns)

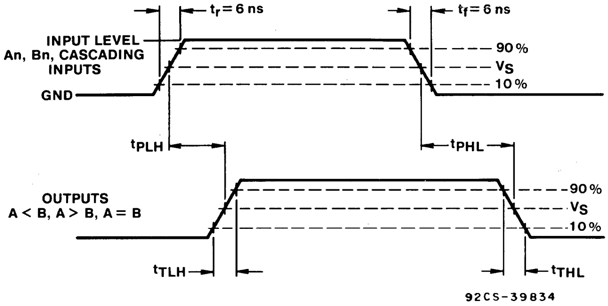
CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay An, Bn to (A>B)out, (A<B)out	t_{PLH} t_{PHL}	15	16	15	ns
An, Bn to (A=B) out			14	17	ns
(A>B)in,(A<B),in (A=B)in to (A>B)out,(A<B)out			11	12	ns
(A=B) in to (A=B)out			9	13	ns
Power Dissipation Capacitance*	C_{PD}	—	24	26	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = V_{CC}^2 fi\ (C_{PD}+C_L)$ where: fi=input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
	V_{CC}	HC		HCT		74HC		74HCT		54HC		54HCT		
	V	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	
An, Bn to (A>B)out, t_{PHL}	4.5	—	39	—	37	—	47	—	46	—	59	—	56	ns
(A<B)out	6	—	33	—	—	—	42	—	—	—	50	—	—	
	2	—	175	—	—	—	240	—	—	—	265	—	—	
An, Bn to	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
(A=B)out	6	—	30	—	—	—	37	—	—	—	45	—	—	
(A>B)in, (A<B)in,	2	—	140	—	—	—	175	—	—	—	210	—	—	
(A=B)in to	4.5	—	28	—	30	—	35	—	38	—	42	—	45	ns
(A>B)out, (A<B)out	6	—	24	—	—	—	30	—	—	—	36	—	—	
	2	—	120	—	—	—	150	—	—	—	180	—	—	
(A=B)in to (A=B)out	4.5	—	24	—	31	—	30	—	39	—	36	—	47	ns
	6	—	20	—	—	—	26	—	—	—	31	—	—	
Output t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time	6	—	13	—	—	—	16	—	—	—	19	—	—	—
Input C_I Capacitance	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times

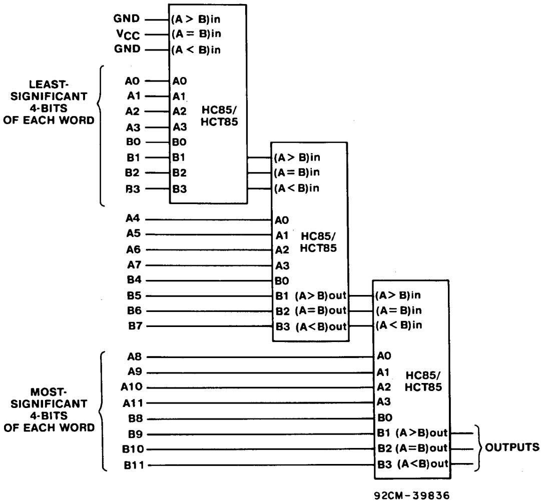


Fig. 3 - Series cascading --- comparing 12-bit words.

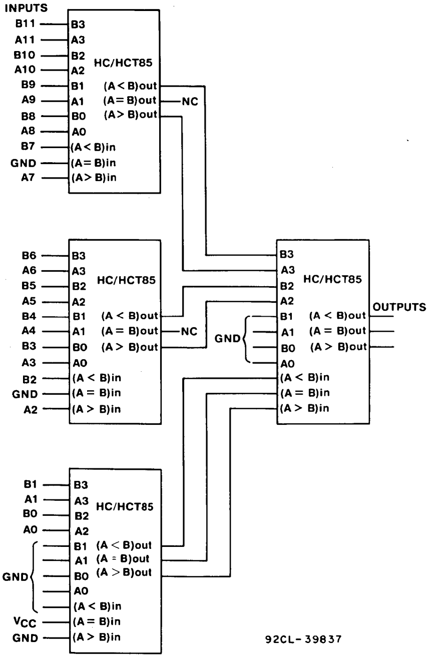
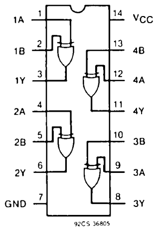


Fig. 4 - Parallel cascading --- comparing 12-bit words.

File Number **1644**

CD54/74HC86
CD54/74HCT86

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Quad 2 - Input EXCLUSIVE - OR Gate

Type Features:

- *Four independent EXCLUSIVE - OR gates*
- *Buffered inputs and outputs*

Applications:

- *Logical comparators*
- *Parity generators and checkers*
- *Adders/Subtracters*

The RCA CD54/74HC86 and CD54/74HCT86 contain four independent EXCLUSIVE-OR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-OR function.

The CD54HC/HCT86 are supplied in 14-lead cermetic dual-in-line packages (F suffix). The CD74HC/HCT86 are supplied in 14-lead plastic dual-in-line packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

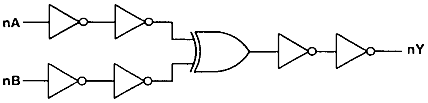


Fig. 1 - Logic diagram each gate.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:* N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility* V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  - *CMOS Input Compatibility* $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level.
L = LOW voltage level.

CD54/74HC86
CD54/74HCT86

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} +0.5$ V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) :
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC86/CD54HC86										CD74HCT86/CD54HCT86										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40		μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	1

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC86
CD54/74HCT86

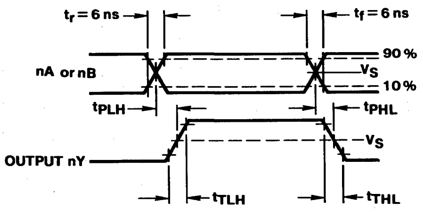
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay, Any Input	15	t_{PLH} t_{PHL}	9	13	ns
Power Dissipation Capacitance*	—	C_{PD}	22	27	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2		120		—		150		—		180		—	
nA, nB to nY	t_{PHL}	4.5		24		32		30		40		36		48	ns
		6		20		—		26		—		31		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
		6		13		—		16		—		19		—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



92CS-38430R2

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.

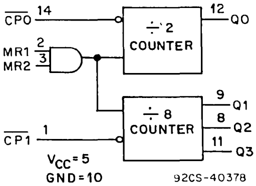
File Number **1849**

CD54/74HC93
CD54/74HCT93

High-Speed CMOS Logic

4-Bit Binary Ripple Counter

Type Features:
- *Can be configured to divide by 2, 8, and 16*
- *Asynchronous Master Reset*



FUNCTIONAL DIAGRAM

The RCA-CD54/74HC93 and the CD54/74HCT93 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL). These 4-bit binary ripple counters consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP0}$ and $\overline{CP1}$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR1 and MR2) is provided which overrides both clocks and resets (clears) all flip-flops.

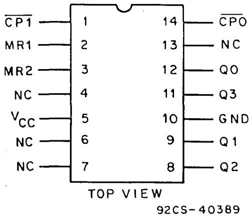
Because the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes.

In a 4-bit ripple counter the output Q0 must be connected externally to input $\overline{CP1}$. The input count pulses are applied to clock input $\overline{CP0}$. Simultaneous frequency divisions of 2, 4, 8, and 16 are performed at the Q0, Q1, Q2, and Q3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP1}$.

Simultaneous frequency divisions of 2, 4, and 8 are available at the Q1, Q2, and Q3 outputs. Independent use of the first flip-flop is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

The CD54HC93 and CD54HCT93 are supplied in 14-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC93 and CD74HCT93 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  $N_{IL}=30\%$, $N_{IH}=30\%$ *of* V_{CC}; @ $V_{CC}=5$ V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL}=0.8$ V *max.,* $V_{IH}=2$ V *min.*
  CMOS input compatibility
  $I_I \leq 1$ μA @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC93
CD54/74HCT93

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	−0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR −0.5 V < V_o < V_{CC} +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = −55 to +100° C (PACKAGE TYPE F,H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F,H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = −40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	−55 to +125° C
PACKAGE TYPE E,M	−40 to +85° C
STORAGE TEMPERATURE (T_{stg})	−65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

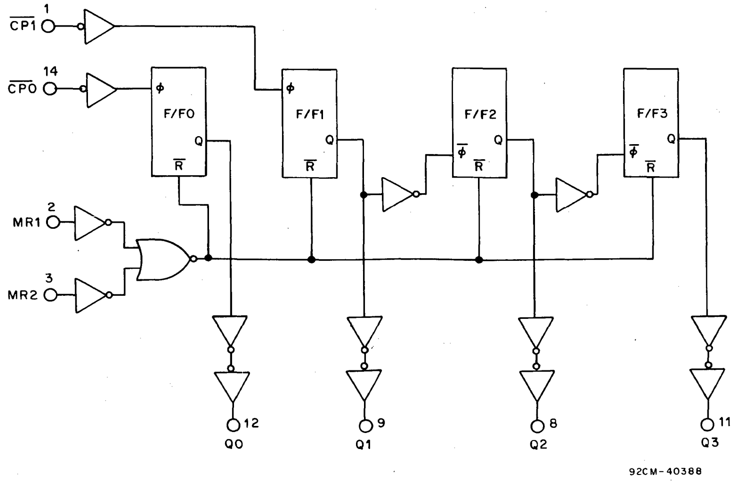


Fig. 1 - HC/HCT93 logic diagram.

FUNCTION TABLE
(Q0 connected to CP1)

COUNT	OUTPUTS Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS MR1	MR2	OUTPUTS Q0	Q1	Q2	Q3
H	H	L	L	L	L
L	H	count			
H	L	count			
L	L	count			

H = HIGH voltage level
L = LOW voltage level

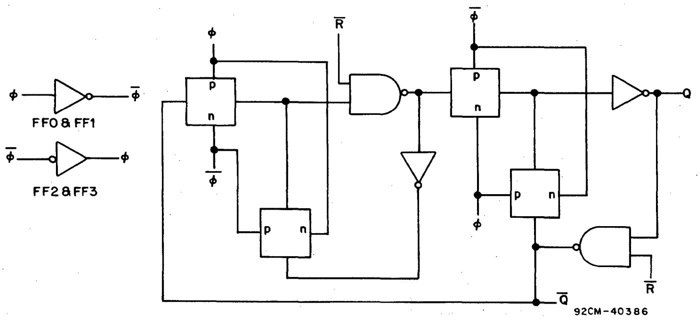


Fig. 2 - Flip-flop (0-3) logic detail.

CD54/74HC93
CD54/74HCT93

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC93/CD54HC93										CD74HCT93/CD54HCT93									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
$\overline{CP0}$, $\overline{CP1}$	0.6
MR1, MR2	0.4

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g. 360 μA max. @ 25° C.

CD54/74HC93
CD54/74HCT93

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

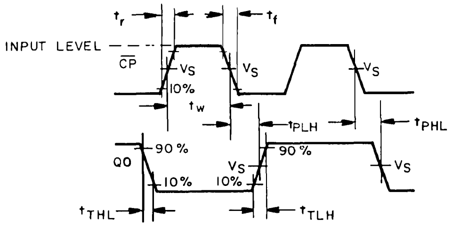
CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay: $\overline{CP0}$ to Q0 Output	t_{PLH} t_{PHL}	15	10	14	ns
$\overline{CP1}$ to Q3			21	24	
MRn to Qn Output			13	13	
Power Dissipation Capacitance*	C_{PD}	—	25	25	pF

*C_{PD} is used to determine the dynamic power consumption, per counter.

$P_D = C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	24	—	24	—	20	—	20	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width $\overline{CP0}$, $\overline{CP1}$	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

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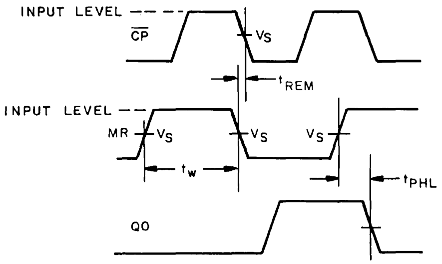
Fig. 3 - Pre-requisite, propagation-delay, and output-transition times.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50%	1.3 V

92CS-38371R2

Fig. 4 - Master-Reset pre-requisite and propagation-delay times.

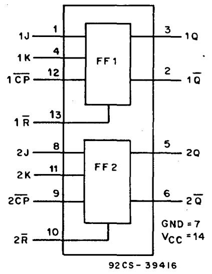
SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	V_{CC}	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
Time: t_{PHL}	4.5	—	25	—	34	—	31	—	43	—	38	—	51	
$\overline{CP0}$ to Q0	6	—	21	—	—	—	26	—	—	—	32	—	—	
	2	—	135	—	—	—	170	—	—	—	205	—	—	
$\overline{CP1}$ to Q1	4.5	—	27	—	34	—	34	—	43	—	41	—	51	
	6	—	23	—	—	—	29	—	—	—	35	—	—	
	2	—	185	—	—	—	230	—	—	—	280	—	—	
$\overline{CP1}$ to Q2	4.5	—	37	—	46	—	46	—	58	—	56	—	69	
	6		31	—	—	—	39	—	—	—	48	—	—	
	2	—	245	—	—	—	305	—	—	—	370	—	—	
$\overline{CP1}$ to Q3	4.5	—	49	—	58	—	61	—	73	—	74	—	87	
	6	—	42	—	—	—	52	—	—	—	63	—	—	
	2	—	155	—	—	—	195	—	—	—	235	—	—	
MR1, MR2 to Qn	4.5	—	31	—	33	—	39	—	41	—	47	—	50	
	6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Transition t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC107
CD54/74HCT107

File Number **1722**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Reset

Negative-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical $f_{max} = 60$ MHz @ $V_{CC} = 5V$, $C_L = 15$ pF, $T_A = 25°C$*

The RCA-CD54/74HC107 and CD54/74HCT107 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low-level input.

This device is functionally identical to the HC/HCT73 but differs in terminal assignment and in some parametric limits.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC107 and CD54HCT107 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC107 and CD74HCT107 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

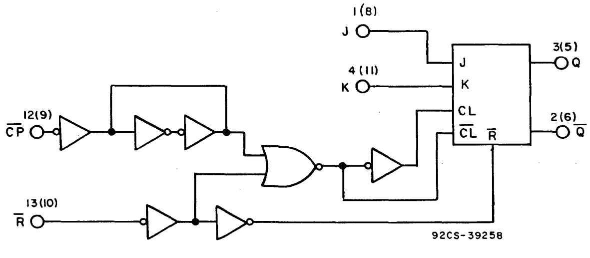


Fig. 1 - Logic diagram.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↘	L	L	No Change	
H	↘	H	L	H	L
H	↘	L	H	L	H
H	↘	H	H	Toggle	
H	H	X	X	No Change	

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↘ = High-to-Low transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

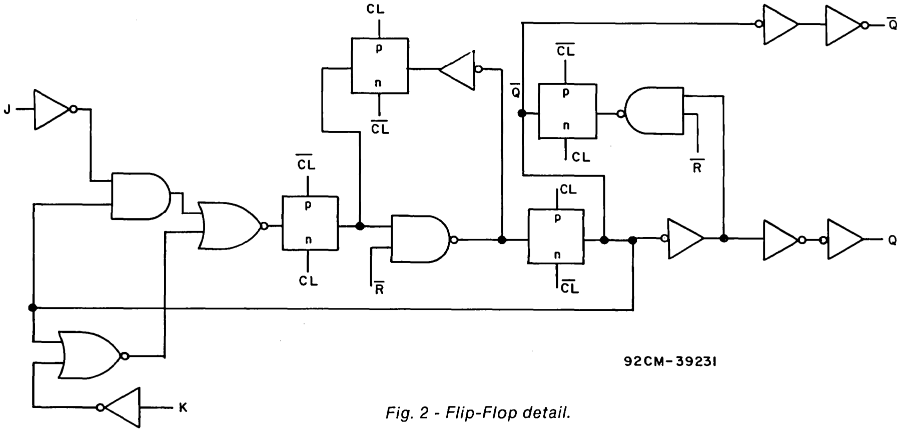


Fig. 2 - Flip-Flop detail.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f •			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
• Applicable for all inputs except clock.

CD54/74HC107
CD54/74HCT107

STATIC ELECTRICAL CHARACTERISTICS

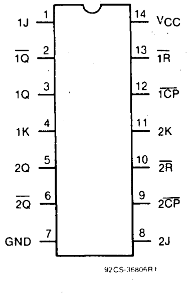
CHARACTERISTIC	CD74HC107, CD54HC107										CD74HCT107, CD54HCT107									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC107
CD54/74HCT107

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay $\overline{\text{CP}}$ to Q	t_{PLH} t_{PHL}	15	14	18	ns
$\overline{\text{CP}}$ to $\overline{\text{Q}}$			14	17	ns
$\overline{\text{R}}$ to Q, $\overline{\text{Q}}$			13	16	ns
$\overline{\text{CP}}$ Frequency	f_{max}	15	60	56	MHz
Power Dissipation Capacitance*	C_{PD}	—	31	30	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2f_i + \Sigma\, C_LV_{CC}^2f_o$ where f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

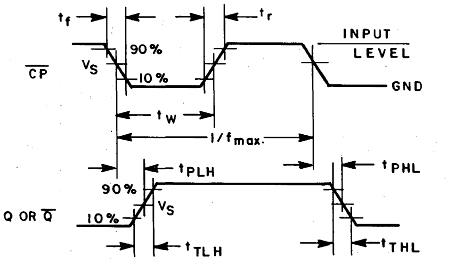
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25°C HC Min	Max	HCT Min	Max	-40°C to +85°C 74HC Min	Max	74HCT Min	Max	-55°C to +125°C 54HC Min	Max	54HCT Min	Max	UNITS
Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{\text{CP}}$	4.5	16	—	18	—	20	—	23	—	24	—	27	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{\text{R}}$	4.5	16	—	24	—	20	—	30	—	24	—	36	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	
J, K to $\overline{\text{CP}}$	4.5	20	—	20	—	25	—	25	—	30	—	30	—	ns
	6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
J, K to $\overline{\text{CP}}$	4.5	3	—	5	—	3	—	5	—	3	—	5	—	ns
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time t_{rem}	2	60	—	—	—	75	—	—	—	90	—	—	—	
	4.5	12	—	12	—	15	—	15	—	18	—	18	—	ns
	6	10	—	—	—	13	—	—	—	15	—	—	—	
$\overline{\text{CP}}$ Frequency f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	
	4.5	30	—	28	—	25	—	22	—	20	—	19	—	MHz
	6	35	—	—	—	29	—	—	—	23	—	—	—	

CD54/74HC107
CD54/74HCT107

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay $\overline{CP}$ to Q	t_{PLH} t_{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	43	—	43	—	54	—	51	—	65	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
$\overline{CP}$ to $\overline{Q}$		2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
$\overline{R}$ to Q, $\overline{Q}$		2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	38	—	39	—	48	—	47	—	57	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



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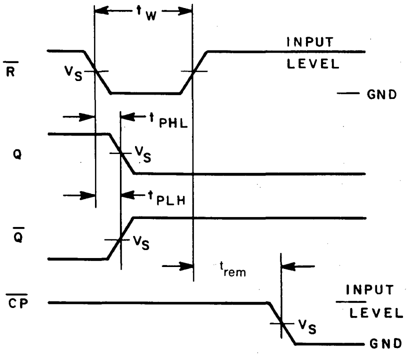

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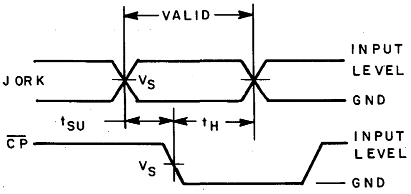


92CS-39234

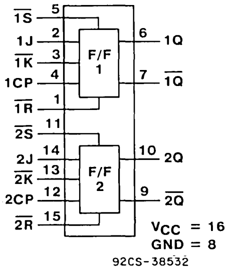
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 3 - Transition times, propagation delay times, and setup and hold times.

File Number **1667**

CD54/74HC109
CD54/74HCT109

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-$\overline{K}$ Flip-Flop with Set and Reset

Type Features:

- *Positive-Edge triggered*
- *Asynchronous Set and Reset*
- *60 MHz Typical Maximum Clock Frequency @ $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25°C$*
- *Typical Propagation Delay = 18 ns @ $V_{cc} = 5V$, $C_L = 15pF$, $T_A = 25°C$*
- *Schmitt Trigger Clock Inputs*

The RCA-CD54/74HC109 and CD54/74HCT109 are dual J-$\overline{K}$ flip-flops with set and reset. The flip-flop changes state with the positive transition of Clock (1CP and 2CP).

The flip-flop is set and reset by active-low $\overline{S}$ and $\overline{R}$, respectively. A low on both the set and reset inputs simultaneously will force both Q and $\overline{Q}$ outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.

The CD54HC109 and CD54HCT109 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC109 and CD74HCT109 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
- *Bus Driver Outputs - 15 LSTTL Loads*
  - *Wide Operating Temperature Range:*
  - *CD74HC/HCT: —40 to + 85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noice Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1$ uA @ V_{OL}, V_{OH}*

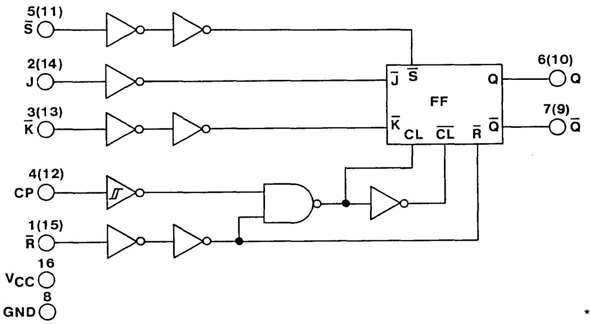


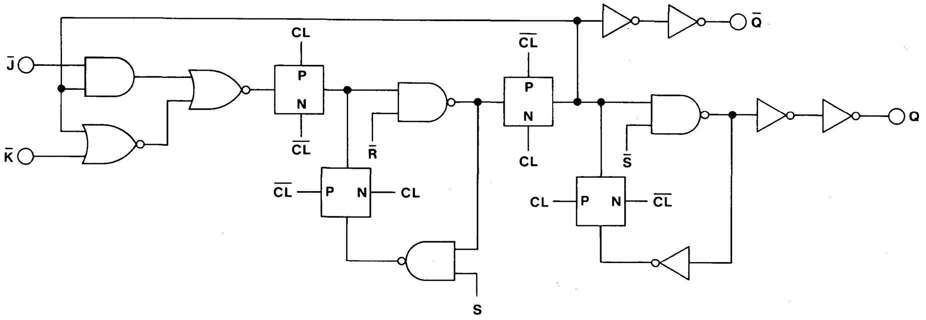
Fig. 1 - Logic diagram

TRUTH TABLE

Inputs					Outputs	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	NO CHANGE	
H	H	↑	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

CD54/74HC109
CD54/74HCT109



92CM-38536

DETAIL OF FLIP-FLOP

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) .... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ OR $V_O > V_{CC} + 0.5$ V) .... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V) .... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): .... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to + 85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	
CD54 Types	-55	+125	°C
Input rise and Fall Times t_r, t_f			
All inputs Except CP at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	
Input Rise and Fall Times tr, tf			
For CP at 2 V	0	unlimited	µs
at 4.5 V	0		
at 6 V	0		

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC109
CD54/74HCT109

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC109 / CD54HC109										CD74HCT109 / CD54HCT109									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	Io mA	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_I V	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.96	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	--	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	Vcc or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between Vcc & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	Vcc or Gnd	0	6	—	—	4	—	40	—	80	Vcc or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional quiescent Device Current ΔI_{CC}* per input pin: 1 unit load											Vcc-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

***For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.**

HCT Input Loading Table

Input	Unit Loads*
All	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C

CD54/74HC109
CD54/74HCT109

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A, = 25° C, Input t_r,t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	Typical		UNITS
			54/74HC	54/74HCT	
Propagation Delay, CP → Q, Q	t_{PLH} t_{PHL}	15	14	17	ns
$\bar{S}$ → Q	t_{PLH}	15	9	12	ns
$\bar{S}$ → $\bar{Q}$	t_{PHL}	15	13	19	ns
$\bar{R}$ → Q	t_{PHL}	15	15	19	ns
$\bar{R}$ → $\bar{Q}$	t_{PLH}	15	14	15	ns
CP Frequency	f_{MAX}	15	60	54	MHz
Power Dissipation Capacitance*	C_{PD}*	—	30	33	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$PD = C_{PD} V_{CC}^2 fi + \Sigma V_{CC}^2 C_L fo$ where:

fi = Input Frequency

C_L = Output Load Capacitance
V_{CC} = Supply Voltage
fo = Output Frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Set-up Time	t_{SU}	2	80		—		100		—		120		—		ns
J, $\bar{K}$ to CP		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20		—		
Hold Time	t_h	2	5		—		5		—		5		—		ns
J, $\bar{K}$ to CP		4.5	5		3		5		3		5		3		
		6	5		—		5		—		5		—		
Removal Time	t_{REM}	2	80		—		100		—		120		—		ns
$\bar{R}$, $\bar{S}$ to CP		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20		—		
Pulse Width	t_W	2	80		—		100		—		120		—		ns
CP, $\bar{R}$, $\bar{S}$		4.5	16		18		20		23		24		27		
		6	14		—		17		—		20	—	—		
CP Frequency	f_{MAX}	2	6		—		5		—		4		—		MHz
		4.5	30		27		25		22		20		18		
		6	35		—		29		—		23		—		

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to + 85°C				-55°C to + 125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PHL}	2		175		—		220		—		265		—	
CP → Q, $\bar{Q}$	t_{PHL}	4.5		35		40		44		50		53		60	ns
		6		30		—		37		—		45		—	
		2		120		—		150		—		180		—	
$\bar{S}$ → Q	t_{PLH}	4.5		24		30		30		38		36		45	ns
		6		20		—		26		—		31		—	
		2		155		—		195		—		235		—	
$\bar{S}$ → $\bar{Q}$	t_{PHL}	4.5		31		45		39		56		47		68	ns
		6		26		—		33		—		40		—	
		2		185		—		230		—		280		—	
$\bar{R}$ → Q	t_{PHL}	4.5		37		45		46		56		56		68	ns
		6		31		—		39		—		48		—	
		2		170		—		215		—		255		—	
$\bar{R}$ → $\bar{Q}$	t_{PLH}	4.5		34		37		43		46		51		56	ns
		6		29		—		37		—		43		—	
Transition	t_{TLH}	2		75		—		95		—		110		—	
Times	t_{THL}	4.5		15		15		19		19		22		22	ns
		6		13		—		16		—		19		—	
Input				—		—		—		—		—		—	
Capacitance	C_I			10		10		10		10		10		10	pF
				—		—		—		—		—		—	

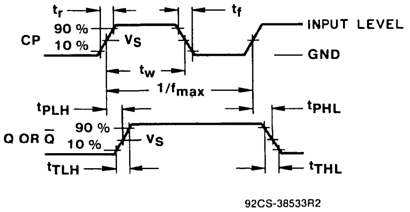


Fig. 2 - Clock to output delays and clock pulse width.

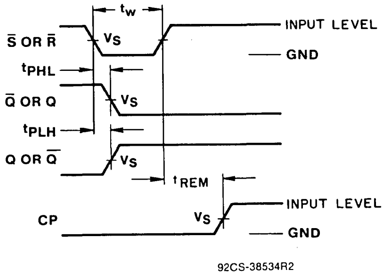


Fig. 3 - $\overline{\text{Reset}}$ or $\overline{\text{Set}}$ prerequisite and propagation delays.

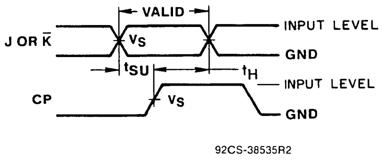


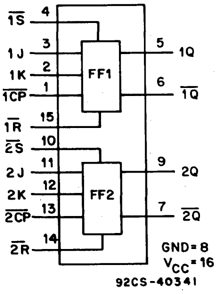
Fig. 4 - Data set-up and hold times.

	54/74 HC	54/74 HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3V

CD54/74HCT112
CD54/74HCT112

File Number **1843**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Set and Reset

Negative-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times*
- *Asynchronous set and reset*
- *Complementary outputs*
- *Buffered inputs*
- *Typical f_{max} = 60 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC112 and CD54/74HCT112 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Set, Reset, and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Set and Reset are accomplished asynchronously by low-level inputs.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC112 and CD54HCT112 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC112 and CD74HCT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	L*
H	H	↘	L	L	No Change	
H	H	↘	H	L	H	L
H	H	↘	L	H	L	H
H	H	↘	H	H	Toggle	
H	H	H	X	X	No Change	

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

* Output states unpredictable if $\overline{S}$ and $\overline{R}$ go High simultaneously after both being low at the same time.
H = High steady state.
L = Low steady state.
X = Irrelevant.
↘ = High-to-Low transition.

CD54/74HCT112

CD54/74HCT112

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

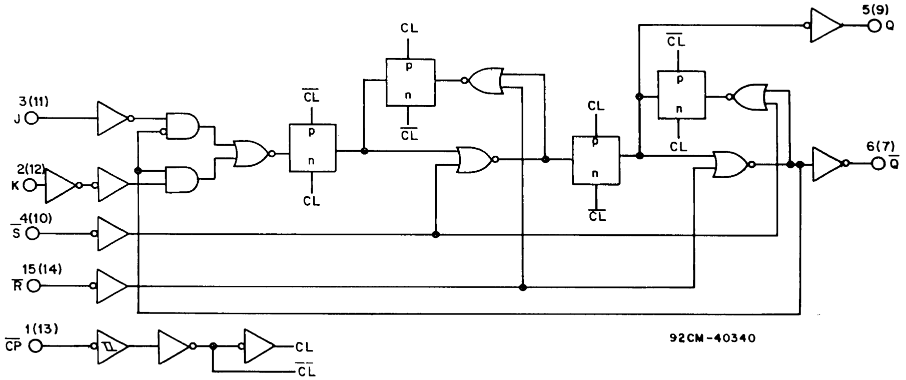


Fig. 1 - Flip-flop logic diagram.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f •			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

• Applicable for all inputs except clock.

CD54/74HCT112
CD54/74HCT112

STATIC ELECTRICAL CHARACTERISTICS

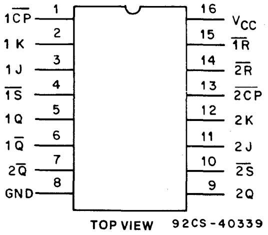
CHARACTERISTICS	CD74HC112, CD54HC112										CD74HCT112, CD54HCT112										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
$\overline{1S}$, $\overline{2S}$	0.5
1K, 2K	0.6
$\overline{1R}$, $\overline{2R}$	0.65
1J, 2J, $\overline{1CP}$, $\overline{2CP}$	1

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HCT112
CD54/74HCT112

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay $\overline{CP}$ to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	15	14	14	ns
$\overline{S}$ to Q, $\overline{Q}$			13	13	ns
$\overline{R}$ to Q, $\overline{Q}$			15	14	ns
$\overline{CP}$ Frequency	f_{max}	15	60	60	MHz
Power Dissipation Capacitance *	C_{PD}	—	12	20	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where:
f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

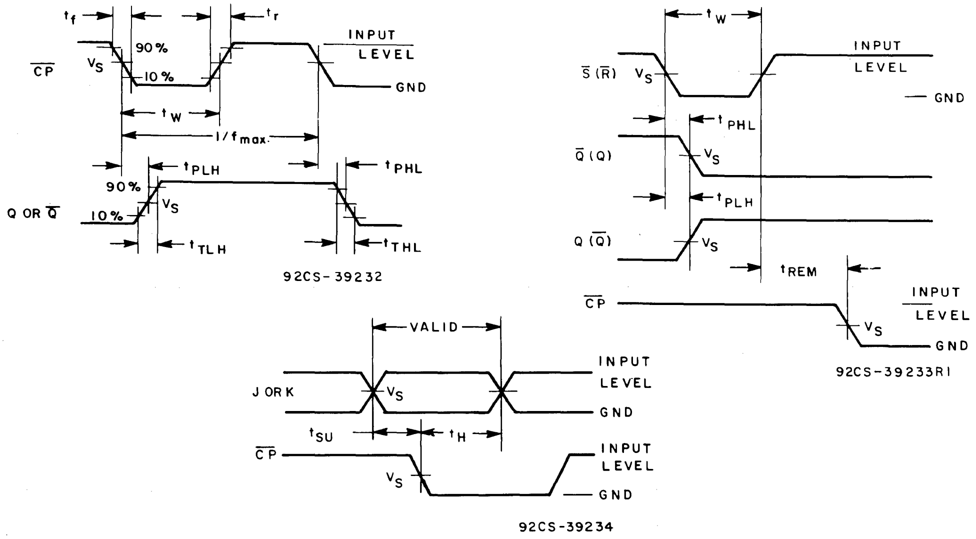
CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
$\overline{CP}$		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{R}$, $\overline{S}$		2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
J, K to $\overline{CP}$		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
J, K to $\overline{CP}$		4.5	0	—	3	—	0	—	3	—	0	—	3	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Removal Time	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
$\overline{R}$ to $\overline{CP}$		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
$\overline{S}$ to $\overline{CP}$		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{CP}$ Frequency	f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	

CD54/74HCT112

CD54/74HCT112

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay $\overline{CP}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{S}$ to Q, $\overline{Q}$		2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
$\overline{R}$ to Q, $\overline{Q}$		2	—	180	—	—	—	225	—	—	—	270	—	—	ns
		4.5	—	36	—	37	—	45	—	46	—	54	—	56	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

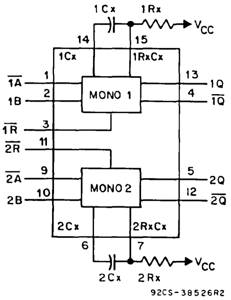
Fig. 2 - Transition times, propagation delay times, and setup and hold times.

File Number **1708**

Advance Information/
Preliminary Data

CD54/74HC123, CD54/74HCT123
CD54/74HC423, CD54/74HCT423

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Retriggerable Monostable Multivibrators with Resets

Type Features:

- *Overriding RESET Terminates Output Pulse*
- *Triggering From the Leading or Trailing Edge*
- *Q and $\overline{Q}$ Buffered Outputs*
- *Separate Resets*
- *Wide Range of Output-Pulse Widths*
- *Schmitt Trigger on both $\overline{A}$ and B inputs*

The RCA-CD54/74HCT123,423 and CD54/74HCT123,423 are dual monostable multivibrators with resets. They are all retriggerable and differ only in that the 123 types can be triggered by a negative-to-positive reset pulse; whereas the 423 types do not have this feature. An external resistor (R_x) and an external capacitor (C_x) control the timing and the accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the $\overline{A}$ and B inputs occur at a particular voltage level and is not related to the rise and fall times of the trigger pulses.

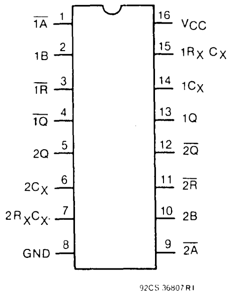
Once triggered, the output pulse width may be extended by retriggering inputs $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset (R) pin. Trailing-edge triggering ($\overline{A}$) and leading-edge triggering (B) are provided for triggering from either edge of the input pulse. If either Mono is not used each input on the unused device ($\overline{A}$, B, and $\overline{R}$) must be terminated high or low.

The minimum value of external resistance, R_x is typically 500 Ω. The minimum value external capacitance, C_x, is 0 pF. The calculation for the pulse width is $t_w = 0.45\ R_xC_x$ at V_{CC} = 5 V.

The CD54HC123,423 and CD54HCT123,423 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC123,423 and CD74HCT123,423 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). All types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC123, CD54/74HCT123
CD54/74HC423, CD54/74HCT423

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC123/CD54HC123 CD74HC423/CD54HC423										CD74HCT123/CD54HCT123 CD74HCT423/CD54HCT423									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	0.35

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC123, CD54/74HCT123
CD54/74HC423, CD54/74HCT423

HC/HCT123 TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H
L	H	↑	⊓	⊔

HC/HCT423 TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{A}$	B	$\overline{R}$	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⊓	⊔
↓	H	H	⊓	⊔
X	X	L	L	H

H = High Level
L = Low Level
X = Irrelevant

↑ = Transition from Low to High
↓ = Transition from High to Low
⊓ = One High Level Pulse
⊔ = One Low Level Pulse

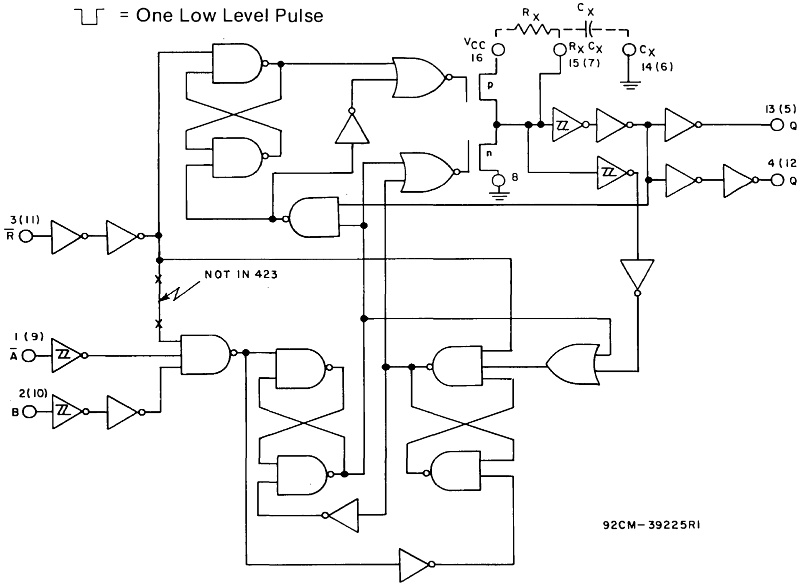


Fig. 1 - Logic diagram for HC/HCT123 and 423.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC123, CD54/74HCT123
CD54/74HC423, CD54/74HCT423

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*				
	CD54/74HC Types	2	6	V
	CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O		0	V_{CC}	V
Operating Temperature T_A:	CD74 Types	-40	+85	°C
	CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f on Input $\overline{R}$	at 2 V	0	1000	ns
	at 4.5 V	0	500	ns
	at 6 V	0	400	ns
Input Rise and Fall Times t_r, t_f on Input B and $\overline{A}$	at 2 V	0	Unlimited	ns
	at 4.5	0	Unlimited	ns
	at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°CC to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Minimum Input Pulse Width $\overline{A}$	t_{WL}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
B	t_{WH}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
$\overline{R}$	t_{WL}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
$\overline{A}$ & B Hold Time	t_H	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Retrigger Time # R_x = 10 KΩ	t_{rT}	5	50 Typ.		50 Typ.		63 Typ.		63 Typ.		76 Typ.		76 Typ.		ns
Output Pulse Width Q or $\overline{Q}$ R_x = 10 KΩ, C_x = 10 nF	tw	5	40	50	40	50	38.7	51.3	38.7	51.3	38.2	51.8	38.2	51.8	us

#Time to trigger depends on the values of R_x and C_x. The output pulse width can only be extended when the time between the active-going edges of the trigger input pulses meet the minimum retrigger time requirement.

CD54/74HC123, CD54/74HCT123
CD54/74HC423, CD54/74HCT423

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	TYPICAL VALUES 54/74HC	TYPICAL VALUES 54/74HCT	UNITS
Propagation Delay				
$\overline{A}$, B, $\overline{R}$ to Q t_{PLH}	15	25	25	ns
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$ t_{PHL}	15	26	27	ns
Output Pulse Width R_x = 10 KΩ, C_x = 10 nF	—	45	45	µs
Pulse Width Match Between Circuits in the same Package R_x = 10 KΩ, C_x = 10 nF	—	±2	±2	%
Power Dissipation Capacitance * C_{PD}	—	—	—	pF

* CPD is used to determine the dynamic power consumption, per multivibrator.

$P_D = (C_{PD} + C_x) V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:

f_i = input frequency.

f_o = output frequency.

C_L = output load capacitance.

C_x = external capacitance.

V_{CC} = supply voltage.

assuming $f_i \ll \frac{1}{t_w}$

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns, R_x = 10 KΩ, C_x = 0)

CHARACTERISTIC	SYMBOL	V_{CC}	LIMITS 25° C HC Min.	Max.	25° C HCT Min.	Max.	-40° C to +85° C 74HC Min.	Max.	-40° C to +85° C 74HCT Min.	Max.	-55° C to +125° C 54HC Min.	Max.	-55° C to +125° C 54HCT Min.	Max.	UNITS
Trigger Propagation Delay, $\overline{A}$, B, $\overline{R}$ to Q	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
		4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	76	—	—	
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	2	—	320	—	—	—	400	—	—	—	480	—	—	ns
		4.5	—	64	—	68	—	80	—	85	—	96	—	102	
		6	—	54	—	—	—	68	—	—	—	82	—	—	
Reset Propagation Delay, $\overline{R}$ to Q or $\overline{Q}$	t_{PHL} t_{PLH}	2	—	215	—	—	—	270	—	—	—	325	—	—	ns
		4.5	—	43	—	48	—	54	—	60	—	65	—	72	
		6	—	37	—	—	—	46	—	—	—	55	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

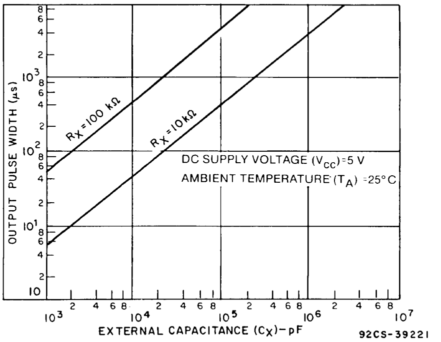


Fig. 3 - Typical output pulse width as a function of C_x for R_x = 10 kΩ and 100 kΩ.

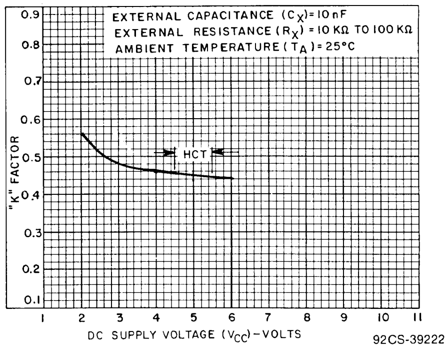


Fig. 4 - Typical "K" Factor as a function of V_{CC}.

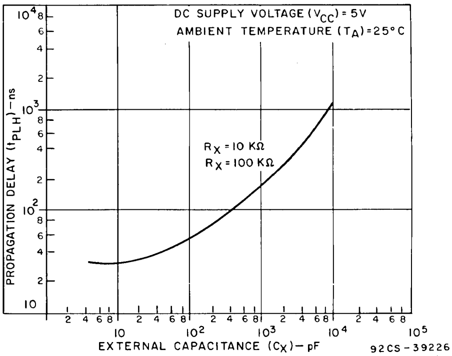
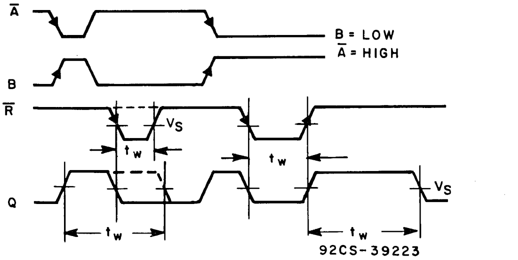
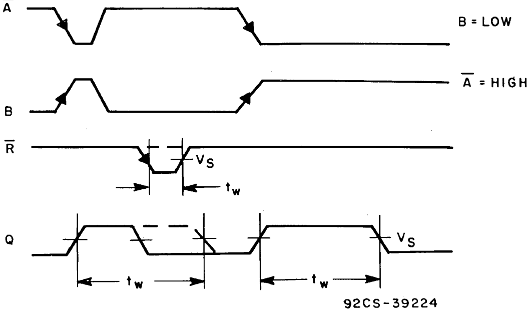


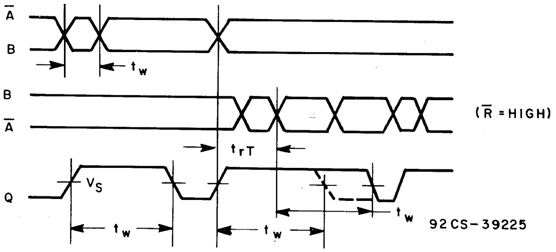
Fig. 5 - Typical propagation delay as a function of External Capacitance (C_x).



Output pulse control using reset input ($\overline{R}$) for 123.



Output pulse control using reset input ($\overline{R}$) for 423.



Output pulse control using retrigger pulse for 123 and 423.

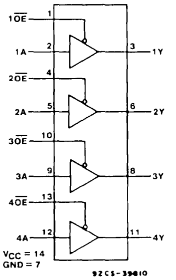
Fig. 2 - Triggering of One Shot by input $\overline{A}$ or input B for a period t_w.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1771**

CD54/74HC125
CD54/74HCT125

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Buffer; 3-State

Type Features:

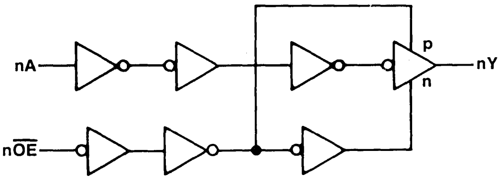
- *Separate output enable inputs*
- *3-state outputs*

The RCA-CD54/74HC125 and CD54/74HCT125 contain 4 independent 3-state buffers, each having its own output enable input, which when "HIGH" puts the output in the high impedance state.

The CD54HC125 and CD54HCT125 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC125 and CD74HCT125 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility I_I, ≤ 1 μA @ V_{OL}, V_{OH}



92CS-39809

Fig. 1 - Logic diagram.

TRUTH TABLE

Inputs		Outputs
nA	**nOE**	**nY**
H	L	H
L	L	L
X	H	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance, OFF State

CD54/74HC125
CD54/74HCT125

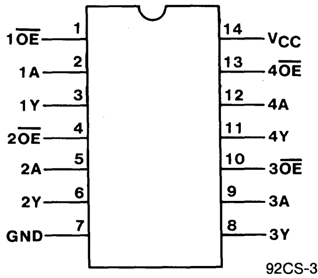
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V) .... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-39808

TERMINAL ASSIGNMENT

CD54/74HC125
CD54/74HCT125

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC125/CD54HC125										CD74HCT125/CD54HCT125									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-6	4.5	3.98	—	—	3.84	—	3.7	—										
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		6	4.5	—	—	0.26	—	0.33	—	0.4										
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
nA, n$\overline{OE}$	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC125
CD54/74HCT125

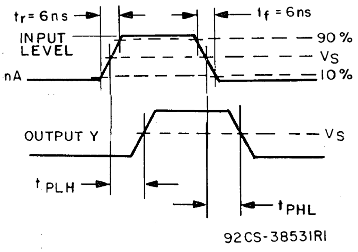
SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

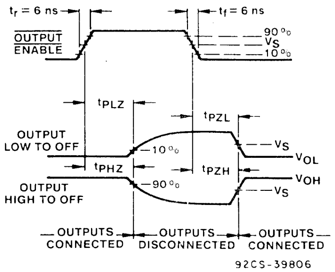
CHARACTERISTIC		C_L pF	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Time: (Fig. 2) nA to nY	t_{PHL} t_{PLH}	15	8	10	ns
Output Enabling Time	t_{PZL}, t_{PZH}	15	10	10	
Output Disabling Time	t_{PLZ}, t_{PHZ}	15	10	11	
Power Dissipation Capacitance*	C_{PD}	—	29	34	pF

*C_{PD} is used to determine the dynamic power consumption, per channel. $P_D=V_{CC}^2 fi\ (C_{PD}+C_L)$ where: fi=input frequency
C_L=load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time nA to nY (Fig. 2)	t_{PLH} t_{PHL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
		4.5	—	20	—	25	—	25	—	31	—	30	—	38	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Enable Delay Time (Fig. 2)	t_{PZH} t_{PZL}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	25	—	31	—	31	—	38	—	38	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Disable Delay Time	t_{PHZ}, t_{PLZ}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	28	—	31	—	35	—	38	—	42	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Ouput Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Transition and propagation delay times.

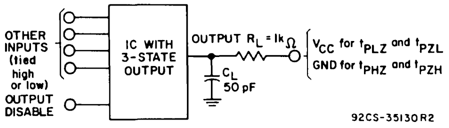
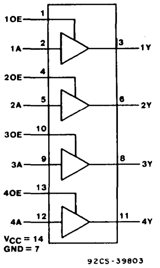


Fig. 3 - Three-state propagation delay test circuit.

CD54/74HC126
CD54/74HCT126

File Number **1772**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Buffer; 3-State

Type Features:

- *Separate output enable inputs*
- *3-state outputs*

The RCA CD54/74HC126 and CD54/74HCT126 contain four independent 3-state buffers, each having its own output enable input, which when "low" puts the output in the high-impedance state.

The CD54HC/HCT126 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT126 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

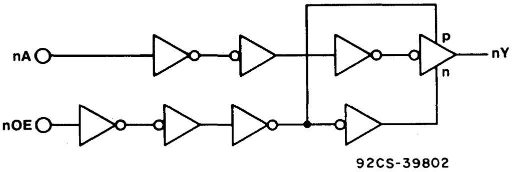


Fig. 1 - Logic Diagram

TRUTH TABLE

Inputs		Outputs
nA	nOE	nY
H	H	H
L	H	L
X	L	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off-State)

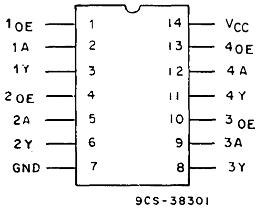
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC126
CD54/74HCT126

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC126/CD54HC126										CD74HCT126/CD54HCT126										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
nA, nOE	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

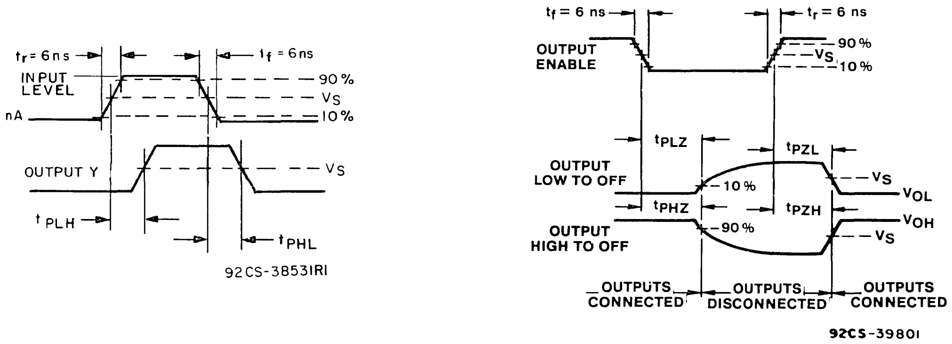
SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Data to Outputs	15	t_{PHL}, t_{PLH}	8	9	ns
Output Enabling Time	15	t_{PZL}, t_{PZH}	10	10	
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	10	11	
Power Dissipation Capacitance*	—	C_{PD}	30	36	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D=V_{CC}^2\ fi\ (C_{PD}+C_L)$ where: fi=input frequency
C_L=load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Outputs	t_{PLH} t_{PHL}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
		4.5	—	20	—	24	—	25	—	30	—	30	—	36	
		6	—	17	—	—	—	21	—	—	—	36	—	—	
Enable Delay Times	t_{PZH} t_{PZL}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	25	—	31	—	31	—	38	—	38	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Disable Delay Times	t_{PHZ} t_{PLZ}	2	—	125	—	—	—	155	—	—	—	190	—	—	
		4.5	—	25	—	28	—	31	—	35	—	38	—	42	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Transition and propagation delay times.

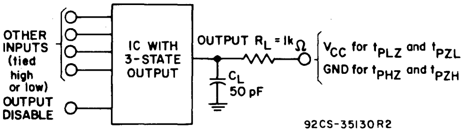


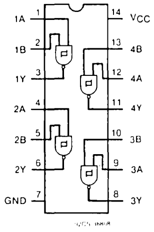
Fig. 3 - Three-state propagation delay test circuit.

Technical Data

File Number **1649**

CD54/74HC132
CD54/74HCT132

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

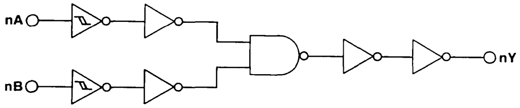
Quad 2-Input NAND Schmitt Trigger

Type Features:

- *Unlimited input rise and fall times*
- *Exceptionally high noise immunity*

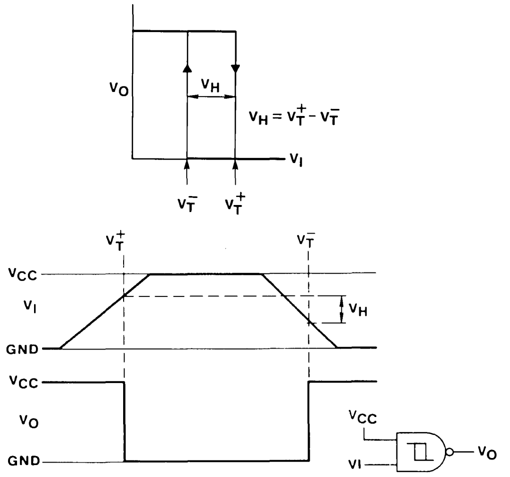
The RCA-CD54/74HC132 and CD54/74HCT132 each contain four 2-input NAND Schmitt Triggers in one package.

The CD54HC132 and CD54HCT132 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC132 and CD74HCT132 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM

92CS-38465RI



92CM-38466

Fig. 1 - Hysteresis definition, characteristic, and test setup.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 37\%$, $N_{IH} = 51\%$ of V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = High level
L = Low level

CD54/74HC132
CD54/74HCT132

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5V$)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC132/CD54HC132									CD74HCT132/CD54HCT132								UNITS
	TEST CONDITIONS			74HC/54HC TYPE		74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE		74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C		-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C		-40/ +85°C		-55/ +125°C		
				Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
Input Switch Points V_T^+			2	0.7	1.5	0.7	1.5	0.7	1.5			—	—	—	—	—	—	V
			4.5	1.7	3.15	1.7	3.15	1.7	3.15		4.5	1.2	1.9	1.2	1.9	1.2	1.9	
			6	2.1	4.2	2.1	4.2	2.1	4.2		5.5	1.4	2.1	1.4	2.1	1.4	2.1	
V_T^-			2	0.3	1	0.3	1	0.3	1			—	—	—	—	—	—	V
			4.5	0.9	2.2	0.9	2.2	0.9	2.2		4.5	0.5	1.2	0.5	1.2	0.5	1.2	
			6	1.2	3	1.2	3	1.2	3		5.5	0.6	1.4	0.6	1.4	0.6	1.4	
V_H			2	0.2	1	0.2	1	0.2	1			—	—	—	—	—	—	V
			4.5	0.4	1.4	0.4	1.4	0.4	1.4		4.5	0.4	1.4	0.4	1.4	0.4	1.4	
			6	0.6	1.6	0.6	1.6	0.6	1.6		5.5	0.4	1.5	0.4	1.5	0.4	1.5	
High-Level Output Voltage V_{OH} CMOS Loads	V_T^-		2	1.9	—	1.9	—	1.9	—	V_T^-		—	—	—	—	—	—	V
	or	-0.02	4.5	4.4	—	4.4	—	4.4	—	or	4.5	4.4	—	4.4	—	4.4	—	
	V_T^+		6	5.9	—	5.9	—	5.9	—	V_T^+		—	—	—	—	—	—	
TTL Loads	V_T^-		—	—	—	—	—	—	—	V_T^-		—	—	—	—	—	—	V
	or	-4	4.5	3.98	—	3.84	—	3.7	—	or	4.5	3.98	—	3.84	—	3.7	—	
	V_T^+	-5.2	6	5.48	—	5.34	—	5.2	—	V_T^+		—	—	—	—	—	—	
Low-Level Output Voltage V_{OL} CMOS Loads	V_T^-		2	—	0.1	—	0.1	—	0.1	V_T^-		—	—	—	—	—	—	V
	or	0.02	4.5	—	0.1	—	0.1	—	0.1	or	4.5	—	0.1	--	0.1	—	0.1	
	V_T^+		6	—	0.1	—	0.1	—	0.1	V_T^+		—	—	—	—	—	—	
TTL Loads	V_T^-			—	—	—	—	—	—	V_T^-		—	—	—	—	—	—	V
	or	4	4.5	—	0.26	—	0.33	—	0.4	or	4.5	—	0.26	—	0.33	—	0.4	
	V_T^+	5.2	6	—	0.26	—	0.33	—	0.4	V_T^+		—	—	—	—	—	—	
Input Leakage Current I_I	V_{CC} or Gnd		6	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	2	—	20	—	40	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*										V_{CC}-2.1	4.5 to 5.5	Min —	Typ 100 Max 360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
nA, nB	0.6

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC132
CD54/74HCT132

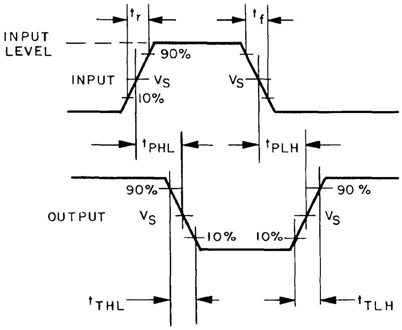
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay A, B to Y	t_{PLH} t_{PHL}	15	10	13	ns
Power Dissipation Capacitance	C_{PD}*	—	30	30	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS	+25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} (V)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	125	—	—	—	156	—	—	—	188	—	—	ns
A, B to Y	t_{PHL}	4.5	—	25	—	33	—	31	—	41	—	38	—	50	
		6	—	21	—	—	—	27	—	—	—	32	—	—	
Output	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
Transition Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50 % V_{CC}	1.3 V

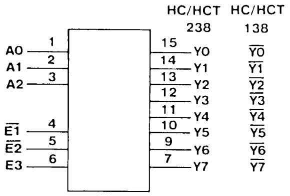
92CS-36948RI

Fig. 2 - Transition times and propagation delay times.

File Number **1477**

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

3-to-8 Line Decoder/Demultiplexer Inverting and Non-Inverting

Type Features:

- *Select one of eight data output [active LOW for 138, active HIGH for 238]*
- *I/O port or memory selector*
- *3 Enable Inputs to simplify cascading*
- *Typical propagation delay of 13ns @ V_{cc} = 5 V, C_L = 15 pF, T_A = +25° C*

The RCA-CD54/74HC138,238 and CD54/74HCT138,238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. Both circuits feature low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic. Both circuits have 3 binary select inputs (A_0, A_1, and A_2). If the device is enabled these inputs determine which one of the eight normally high outputs of the HC/HCT138 series will go low or which of the normally low outputs of the HC/HCT238 series will go high.

Two active low and one active high enables ($\overline{E}_1$, $\overline{E}_2$, and E_3) are provided to ease the cascading of decoders. The decoder's outputs can drive 10 low power Schottky TTL equivalent loads.

The CD54HC138,238 and CD54HCT138,238 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC138,238 and CD74HCT138,238 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout [Over Temperature Range]:*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL}= 30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

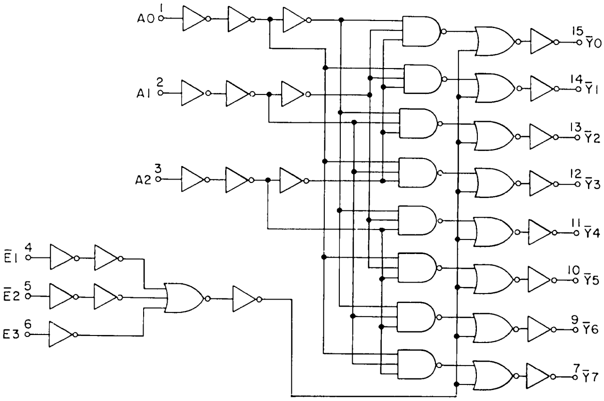


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Fig. 1 — Logic Diagram for HC/HCT 138

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

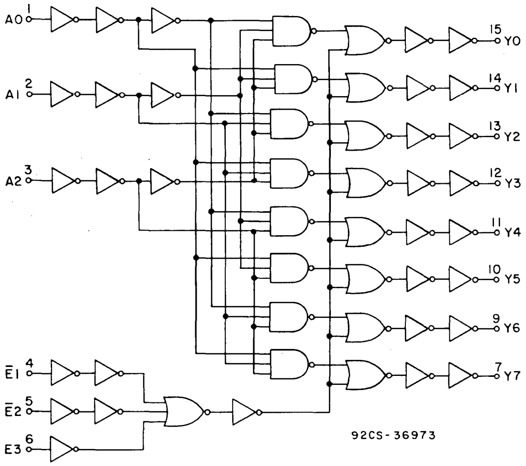


Fig. 2 — Logic Diagram for HC/HCT 238

TRUTH TABLE
CD54/74HC138, CD54/74HCT138

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High level, L = low level, X = don't care

TRUTH TABLE
CD54/74HC238, CD54/74HCT238

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

H = High level, L = low level, X = don't care

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

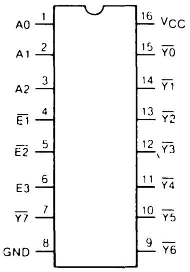
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	**400 mW**
For T_A = +70 to +125°C (PACKAGE TYPE M)	**Derate Linearly at 6 mW/°C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



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TERMINAL ASSIGNMENT FOR HC/HCT138
FOR HC/HCT238 ALL $\overline{Y}$'s ARE Y's

CD54/74HC138, CD54/74HCT138
CD54/74HC238, CD54/74HCT238

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC138/238, CD54HC138/238										CD74HCT138/238, CD54HCT138/238									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0-A2	1.5
$\overline{E1}$, $\overline{E2}$	1.25
E3	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, C_L = 15 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	Typical HC	Typical HCT	Typical Unit
Propagation Delay, Address to Output Y (C_L=15 pF) (Fig. 3)	t_{PLH} t_{PHL}	13	14	ns
Power Dissipation Capacitance*	*C_{PD}	67	67	pF

*C_{PD} is used to determine the dymanic power consumption, per package.
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L output load capacitance
V_{CC} supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	+25° C HC Min.	+25° C HC Max.	+25° C HCT Min.	+25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Address to Output	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Fig. 3)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay,	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Enable to Output	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Fig. 3) HC/HCT138		6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
Enable to Output	t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
(Fig. 4) HC/HCT238		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition Times	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

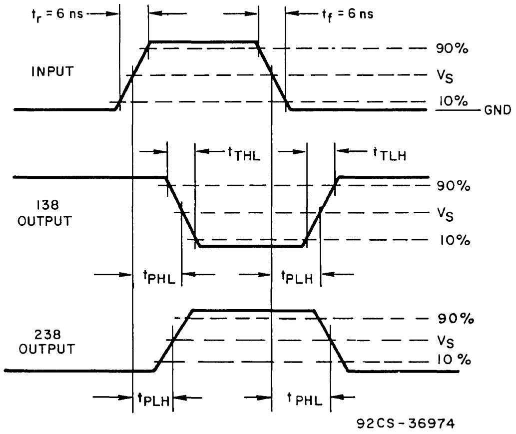


Fig. 3 — Transition times and propagation delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

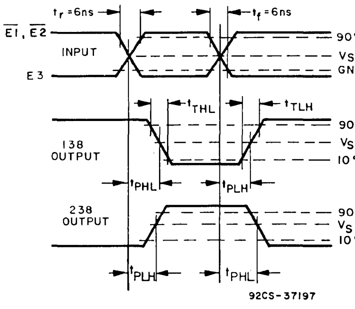


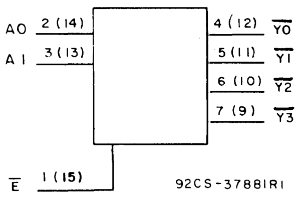
Fig. 4 — Transition times and propagation delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

CD54/74HC139
CD54/74HCT139

File Number **1545**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 2-to-4 Line Decoder/Demultiplexer

Type Features:

- *Multifunction Capability*
  Binary to 1-of-4 Decoders or
  1-to-4 Line Demultiplexer
- *Active Low Mutually Exclusive Outputs*

Applications:

- *Memory Decoding*
- *Data Routing*
- *Code Conversion*

The RCA-CD54/74HC139 and CD54/74HCT139 contain two independent binary to one-of-four decoders each with a single active low enable input ($\overline{1E}$, or $\overline{2E}$). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally high outputs to go low.

If the enable input is high all four outputs remain high. For demultiplexer operation the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded. This device is functionally the same as the CD4556B and is pin compatible with it.

The outputs of these devices can drive 10 low power Schottky TTL equivalent loads. The 54/74HCT logic family is functionally as well as pin equivalent to the 54/74LS logic family.

The CD54HC139 and CD54HCT139 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC139 and CD74HCT139 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

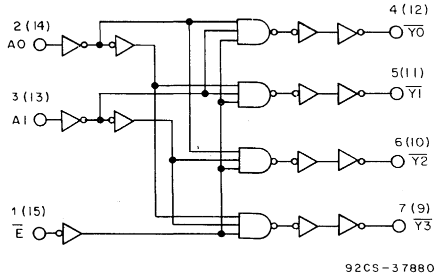


Fig. 1 - Logic diagram for the CD54/74HC/HCT139.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

Inputs Enable	Select		Outputs			
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

X = Don't Care

Logic 1 = High
Logic 0 = Low

CD54/74HC139
CD54/74HCT139

MAXIMUM RATINGS, *Absolute-Maximum Values:*

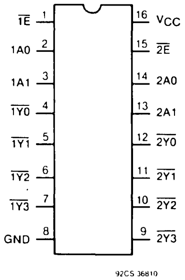
DC SUPPLY-VOLTAGE, (V_{CC}): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING) :	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC139
CD54/74HCT139

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC139/CD54HC139										CD74HCT139/CD54HCT139									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

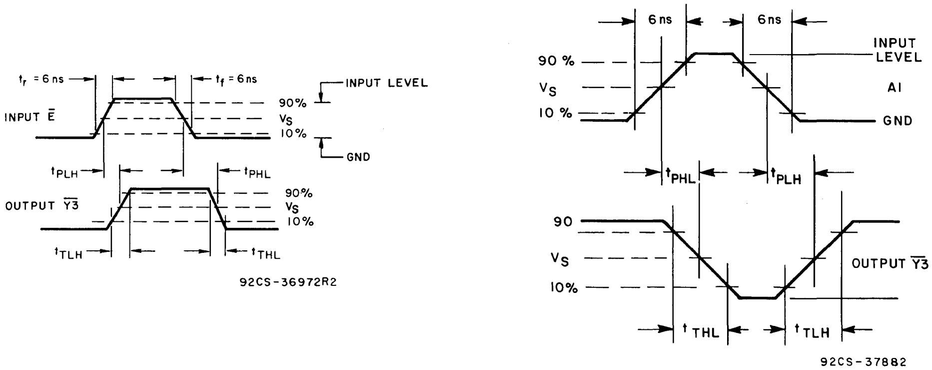
CHARACTERISTIC	C_L (pF)	SYMBOL	Typical		UNITS
			54/74HC	54/74HCT	
Propagation Delay Select to Output	15	t_{PHL} t_{PLH}	12	14	ns
Enable to Output	15		11	14	ns
Power Dissipation Capacitance*	—	C_{PD}	55	59	pF

*C_{PD} is used to determine the dynamic power consumption, per decoder/demux.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
A0, A1 to Outputs	t_{PHL}	4.5	—	29	—	34	—	36	—	43	—	44	—	51	ns
		6	—	25	—	—	—	31	—	—	—	38	—	—	
	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
$\overline{E}$ to Outputs	t_{PHL}	4.5	—	27	—	34	—	34	—	43	—	41	—	51	ns
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC139
CD54/74HCT139



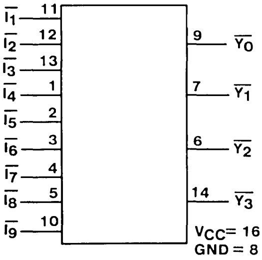
Transition times and propagation delay times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

File Number **1773**

CD54/74HC147
CD54/74HCT147

High-Speed CMOS Logic



92CS-39831
FUNCTIONAL DIAGRAM

10-to-4-Line Priority Encoder

Type Features:

- *Buffered inputs and outputs*
- *Typical CD54/74HC147 propagation delay = 13ns @ V_{cc}=5 V, C_L=15 pF, T_A=25°C*

The RCA-CD54/74HC147 and CD54/74HCT147 are high-speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL).

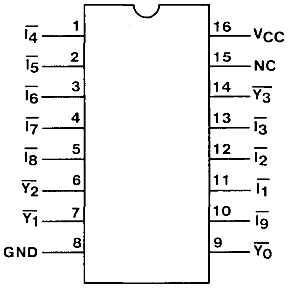
The CD54/74HC147 and CD54/74HCT147 9-input priority encoders accept data from nine active LOW inputs ($\overline{I_1}$ to $\overline{I_9}$) and provide binary representation on the four active LOW outputs ($\overline{Y_0}$ to $\overline{Y_3}$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I_9}$ having the highest priority.

These devices provide the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

The CD54HC/HCT147 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT147 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-39830

TERMINAL ASSIGNMENT

CD54/74HC147
CD54/74HCT147

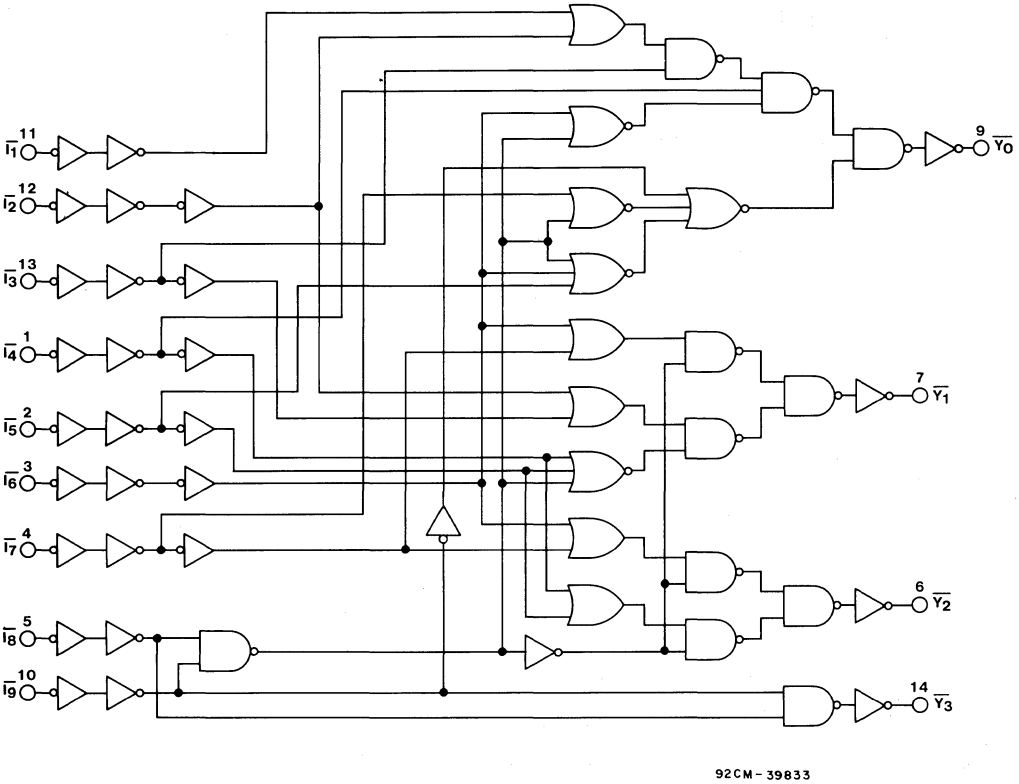


Fig. 1 - Logic Diagram

TRUTH TABLE

Inputs									Outputs			
$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{I}_8$	$\overline{I}_9$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{V} < V_O < V_{CC} + 0.5$ V)	± 25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC147
CD54/74HCT147

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC147/CD54HC147										CD74HCT147/CD54HCT147									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

* For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{I_1}, \overline{I_2}, \overline{I_3}, \overline{I_6}, \overline{I_7}$	1.1
$\overline{I_4}, \overline{I_5}, \overline{I_8}, \overline{I_9}$	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

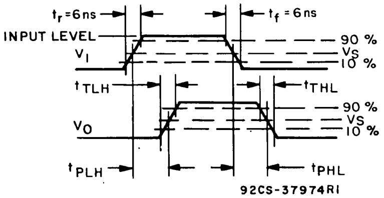
SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L=15 pF)	t_{PLH} t_{PHL}	13	14	ns
Power Dissipation Capacitance*	C_{PD}	32	42	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i= input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH} t_{PHL}	2		160		—		200		—		240		—	ns
		4.5		32		35		40		44		48		53	
		6		27		—		34		—		41		—	
Transition Times (Fig. 1)	t_{TLH} t_{THL}	2		75		—		95		—		110		—	ns
		4.5		15		15		19		19		22		22	
		6		13		—		16		—		19		—	
Input Capacitance	C_I			10		10		10		10		10		10	pF



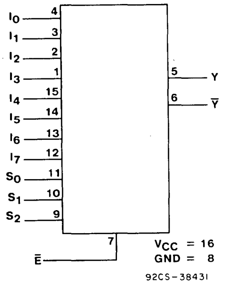
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC151
CD54/74HCT151

File Number **1645**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

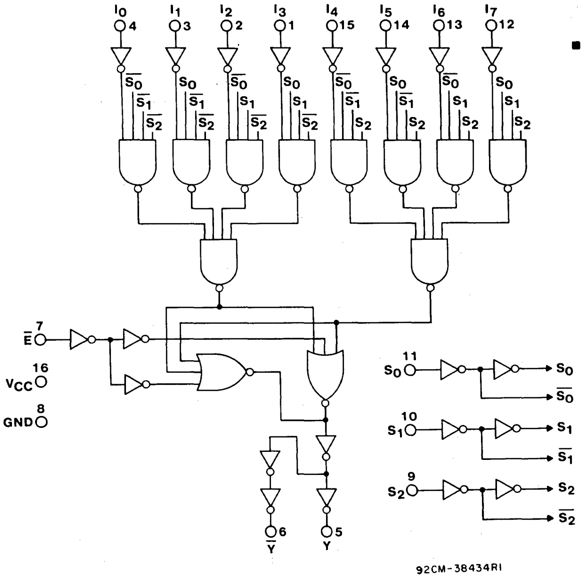
8-Input Multiplexer

Type Features:

- *Complementary data outputs*
- *Buffered inputs and outputs*

The RCA CD54/74HC151 and CD54/74HCT151 are single 8-channel digital multiplexers having three binary control inputs, S0, S1 and S2 and an active low enable ($\overline{E}$) input. The three binary signals select 1 of 8 channels. Outputs are both inverting ($\overline{Y}$) and non-inverting (Y).

The CD54HC/HCT151 devices are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT151 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:* $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC} *@* $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V *Max.,* $V_{IH} = 2$ V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level.
L = LOW voltage level.
X = Don't care.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC151
CD54/74HCT151

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC151/CD54HC151										CD74HCT151/CD54HCT151									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
Select	1.5
Data	0.45
Enable	0.3

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

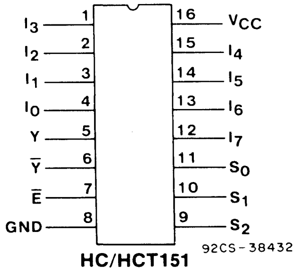
CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delays					
Any data input to Y	15	t_{PLH} t_{PHL}	14	16	ns
Any data input to $\overline{Y}$	15	t_{PLH}/t_{PHL}	15	15	ns
Any select to Y	15	t_{PLH}/t_{PHL}	15	17	ns
Any select to $\overline{Y}$	15	t_{PLH}/t_{PHL}	17	18	ns
Enable to Y	15	t_{PLH}/t_{PHL}	11	12	ns
Enable to $\overline{Y}$	15	t_{PLH}/t_{PHL}	12	15	ns
Power Dissipation Capacitance*	—	C_{PD}	59	58	pF

* C_{PD} is used to determine the dynamic power dissipation per device:
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

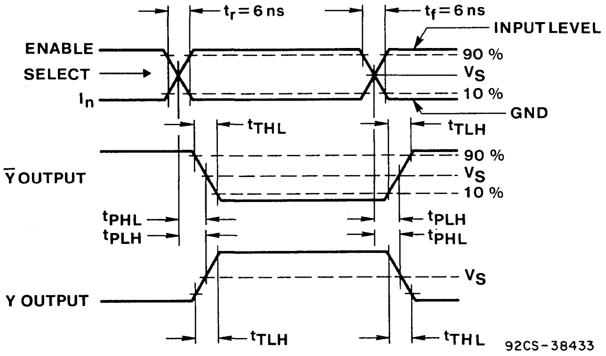
CD54/74HC151
CD54/74HCT151

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay,	t_{PLH}	2		170		—		215		—		255		—	
Any Data Input to Y	t_{PHL}	4.5		34		38		43		48		51		57	ns
		6		29		—		37		—		43		—	
		2		185		—		230		—		280		—	
Any Data Input to $\overline{Y}$	t_{PLH}	4.5		37		36		46		45		56		54	ns
	t_{PHL}	6		31		—		39		—		48		—	
		2		185		—		230		—		280		—	
Any Select to Y	t_{PLH}	4.5		37		41		46		51		56		62	ns
	t_{PHL}	6		31		—		39		—		48		—	
		2		205		—		255		—		310		—	
Any Select to $\overline{Y}$	t_{PLH}	4.5		41		43		51		54		62		65	ns
	t_{PHL}	6		35		—		43		—		53		—	
		2		140		—		175		—		210		—	
Enable to Y	t_{PLH}	4.5		28		29		35		36		42		44	ns
	t_{PHL}	6		24		—		30		—		36		—	
		2		145		—		180		—		220		—	
Enable to $\overline{Y}$	t_{PLH}	4.5		29		36		36		45		44		54	ns
	t_{PHL}	6		25		—		31		—		38		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
		6		13		—		16		—		19		—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



HC/HCT151
TERMINAL ASSIGNMENT



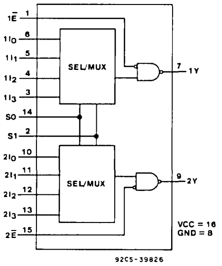
	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Propagation delays to Y and $\overline{Y}$ outputs.

File Number **1774**

CD54/74HC153
CD54/74HCT153

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 4-Input Multiplexer

Type Features:
- *Common select inputs*
- *Separate enable inputs*
- *Buffered inputs and outputs*

The RCA-CD54/74HC153 and CD54/74HCT153 are dual 4-to-1-line selector/multiplexers which select one of four sources for each section by the common select inputs, S0 and S1. When the enable inputs (1Ē, 2Ē) are HIGH, the outputs are in the LOW state.

The CD54HC/HCT153 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT153 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

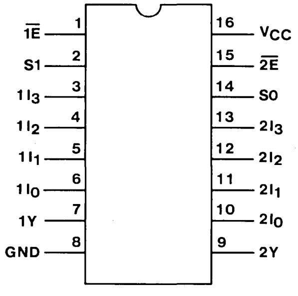
Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} *= 30%,* N_{IH} *= 30% of* V_{CC}*; @* V_{CC} *= 5V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} *= 0.8 V Max.,* V_{IH} *= 2 V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}*,* V_{OH}

TRUTH TABLE

Select Inputs		Data Inputs				Enable	Output
S_1	S_0	I_0	I_1	I_2	I_3	Ē	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care.

LOGIC DIAGRAM



TERMINAL ASSIGNMENT

CD54/74HC153
CD54/74HCT153

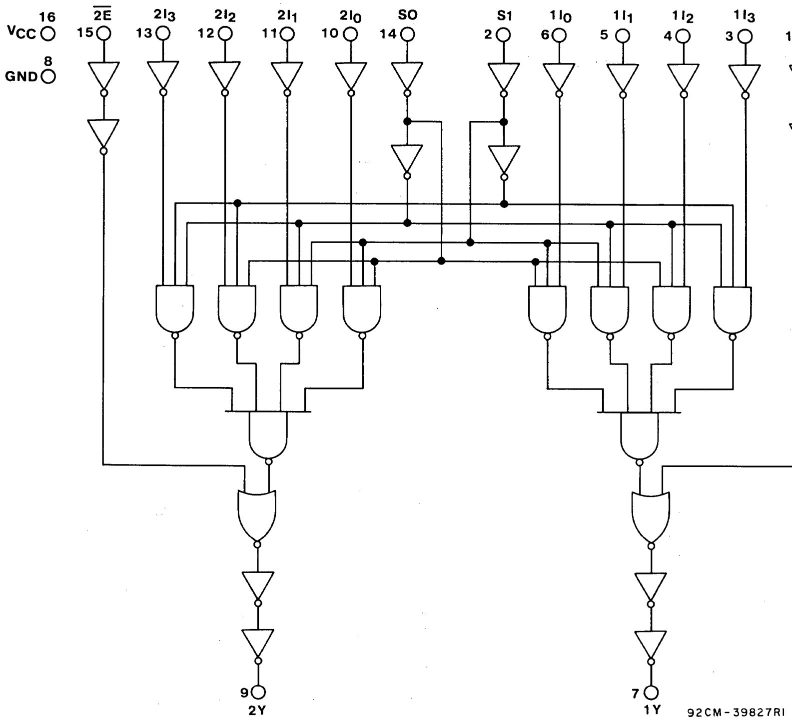


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC153
CD54/74HCT153

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC153/CD54HC153										CD74HCT153/CD54HCT153										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DATA	0.45
ENABLE	0.6
SELECT	1.35

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC153
CD54/74HCT153

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

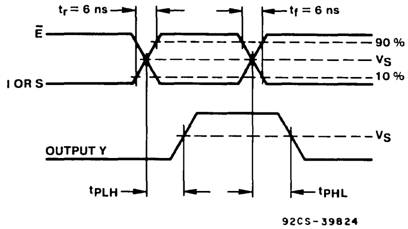
CHARACTERISTIC		CL (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay, Select to Outputs	t_{PHL} t_{PLH}	15	13	14	ns
Data to Outputs	t_{PLH}	15	12	9	
	t_{PHL}	15	12	14	
Enable to Outputs	t_{PLH} t_{PHL}	15	9	11	
Power Dissipation Capacitance*	C_{PD}	—	45	45	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 fi (C_{PD} + C_L)$ where: fi = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, S to Y	t_{PLH} t_{PHL}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
		4.5	—	32	—	34	—	40	—	43	—	48	—	51	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
I to Y	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
		4.5	—	29	—	24	—	36	—	30	—	44	—	36	
		6	—	25	—	—	—	31	—	—	—	38	—	—	
I to Y	t_{PHL}	2	—	145	—	—	—	180	—	—	—	220	—	—	
		4.5	—	29	—	34	—	36	—	43	—	44	—	51	
		6	—	25	—	—	—	31	—	—	—	38	—	—	
$\overline{E}$ to Y	t_{PLH} t_{PHL}	2	—	120	—	—	—	150	—	—	—	180	—	—	
		4.5	—	24	—	27	—	30	—	34	—	36	—	41	
		6	—	20	—	—	—	26	—	—	—	31	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC153
CD54/74HCT153



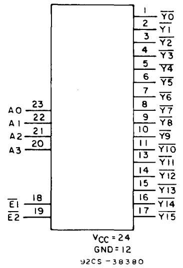
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition and propagation delay times.

CD54/74HC154
CD54/74HCT154

File Number **1657**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-to-16 Line Decoder/Demultiplexer

Type Features:

- *Two enable inputs to facilitate demultiplexing and cascading functions*

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

The RCA CD54/74HC154 and CD54/74HCT154 are 4-to-16 line decoders/demultiplexers with two enable inputs, $\overline{E1}$ and $\overline{E2}$. A High on either enable input forces the output into the High state. The demultiplexing function is performed by using the four input lines, A0 to A3, to select the output lines $\overline{Y0}$ to $\overline{Y15}$, and using one enable as the data input while holding the other enable low.

The CD54HC154 and CD54HCT154 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC154 and CD74HCT154 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

INPUTS						OUTPUTS															
$\overline{E1}$	$\overline{E2}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care.

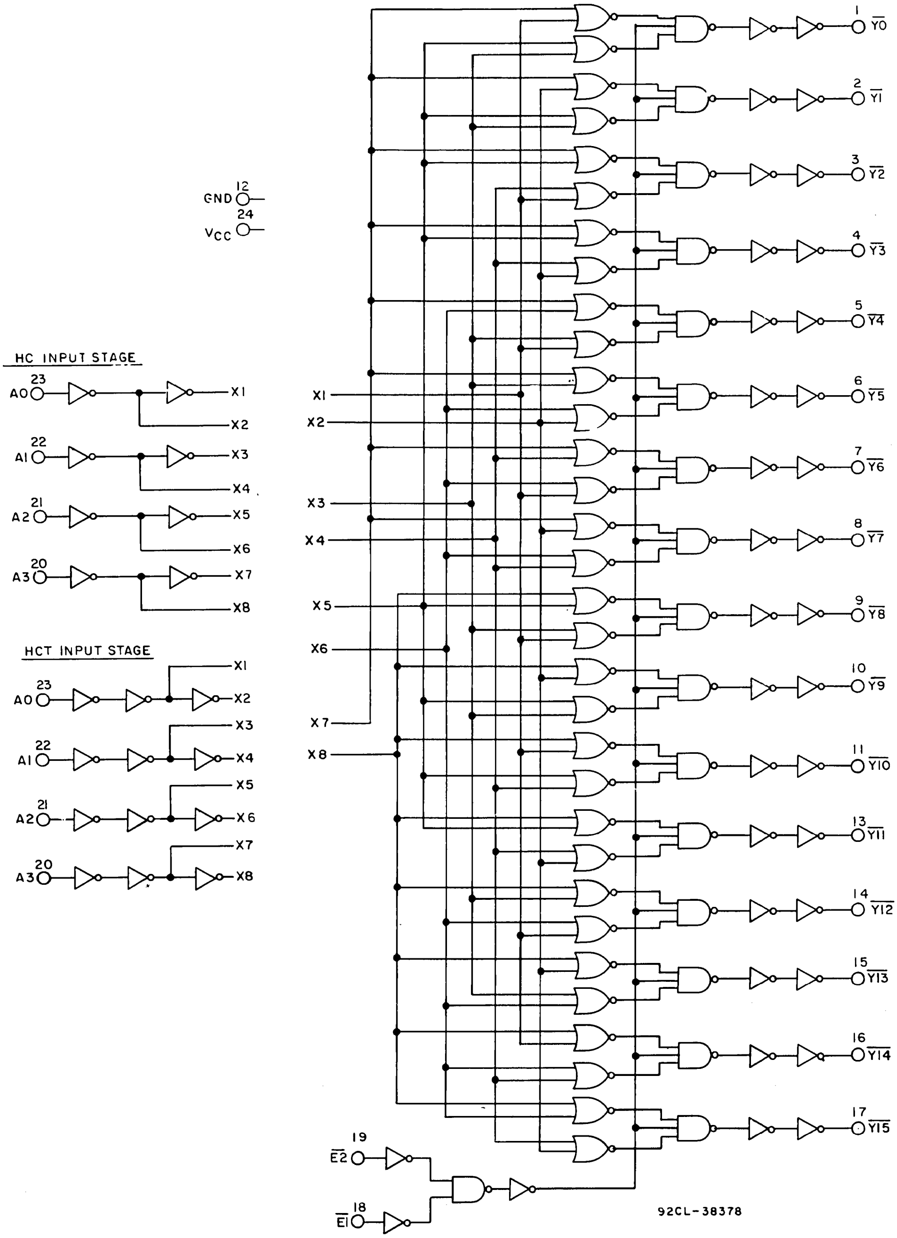


Fig. 1 - Logic diagram.

CD54/74HC154
CD54/74HCT154

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC154
CD54/74HCT154

STATIC ELECTRICAL CHARACTERISTICS

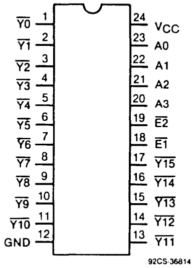
CHARACTERISTICS	CD74HC154/CD54HC154										CD74HCT154/CD54HCT154									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
A0 — A3	1.4
$\overline{E1}, \overline{E2}$	1.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC154
CD54/74HCT154

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

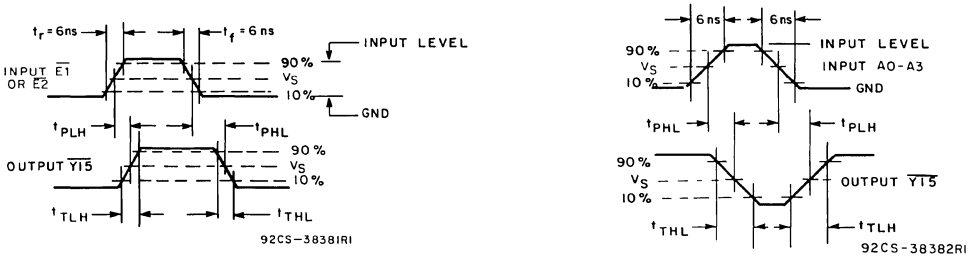
CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay Address to Output	15	t_{PHL} t_{PLH}	14	14	ns
$\overline{E1}$ to Output	15	t_{PHL} t_{PLH}	14	14	ns
$\overline{E2}$ to Output	15	t_{PHL} t_{PLH}	14	14	ns
Power Dissipation Capacitance*	—	C_{PD}	88	84	pF

*C_{PD} is used to determine the dynamic power consumption, per device.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
Address to Outputs	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
$\overline{E1}$ to Outputs	t_{PHL}	4.5	—	35	—	34	—	44	—	43	—	53	—	51	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
$\overline{E2}$ to Outputs	t_{PHL}	4.5	—	35	—	34	—	44	—	43	—	53	—	51	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



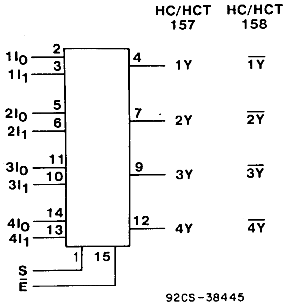
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Propagation delay and transition times.

CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158

File Number **1642**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexers

HC/HCT157 Non-Inverting
HC/HCT158 Inverting

Type Features:

- *Buffered inputs*
- *Typical Propagation Delay (In to Output) = 10 ns (HC157) @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC157, 158 and CD54/74HCT157, 158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When ($\overline{E}$) is HIGH, all of the outputs in the 158, the inverting type, (1Y-4Y) are forced HIGH and in the 157, the non-inverting type, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are forced LOW, regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

The CD54HC157, 158 and CD54HCT157, 158 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line plastic packages (E suffix). The CD74HC157, 158 and CD74HCT157, 158 are supplied in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

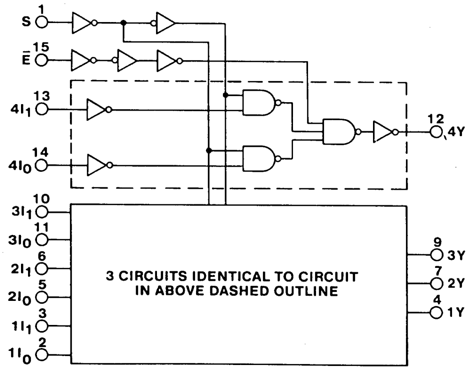


Fig. 1 - Logic Diagram for HC/HCT157. 92CM-38446

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

FUNCTION TABLE

Enable	Select Input	Data Inputs		Output	
				157	158
$\overline{E}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.

CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158

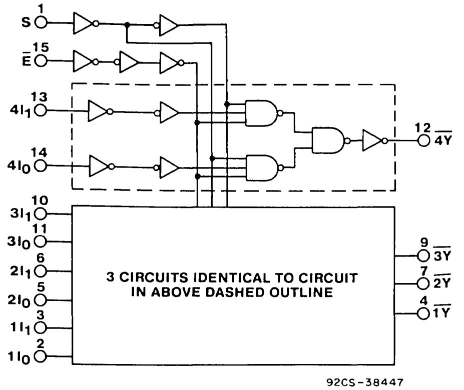
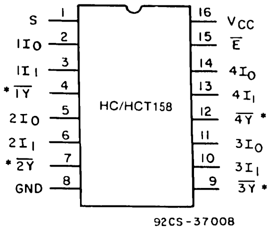


Fig. 2 - Logic Diagram for HC/HCT158.



* For HC/HCT157 these outputs are 1Y, 2Y, 3Y, 4Y.

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC157/158/CD54HC157/158										CD74HCT157/158/CD54HCT157/158										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
				+25° C			-40/ +85° C		-55/ +125° C				+25° C			-40/ +85° C		-55/ +125° C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT 157	HCT 158
I (ALL)	0.95	0.4
$\overline{E}$	0.6	0.6
S	3	2.8

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES				UNITS
			HC157	HCT157	HC158	HCT158	
Data to Output	15	t_{PHL} t_{PLH}	10	12	11	13	ns
Enable to Output	15	t_{PHL} t_{PLH}	11	12	13	15	ns
Select to Output	15	t_{PHL} t_{PLH}	12	15	12	14	ns
Power Dissipation Capacitance*		C_{PD}	62	70	35	35	pF

* C_{PD} is used to determine the dynamic power consumption, per multiplexer.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where:

f_i = input frequency.

f_o = output frequency.

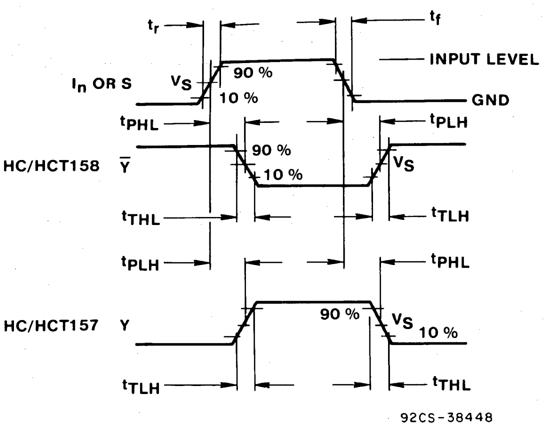
C_L = output load capacitance.

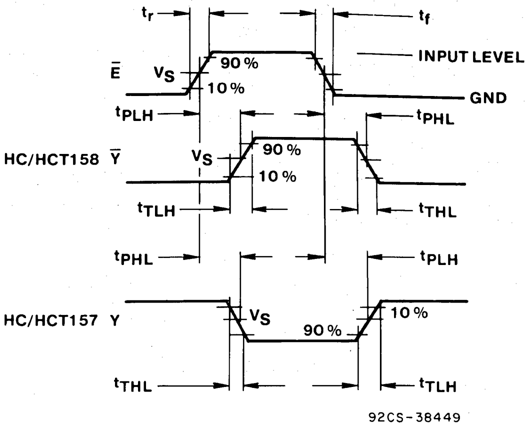
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
Data to Output	t_{PHL}	4.5	—	25	—	30	—	31	—	38	—	38	—	45	ns
(Figure 3) HC/HCT157		6	—	21	—	—	—	26	—	—	—	32	—	—	
Propagation Delay	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
Enable to Output	t_{PHL}	4.5	—	27	—	30	—	34	—	38	—	41	—	45	ns
(Figure 4) HC/HCT157		6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
Select to Output	t_{PHL}	4.5	—	29	—	37	—	36	—	46	—	44	—	56	ns
(Figure 3) HC/HCT157		6	—	25	—	—	—	31	—	—	—	38	—	—	
Propagation Delay	t_{PLH}	2	—	140	—	—	—	175	—	—	—	210	—	—	
Data to Output	t_{PHL}	4.5	—	28	—	32	—	35	—	40	—	42	—	48	ns
(Figure 3) HC/HCT158		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	
Enable to Output	t_{PHL}	4.5	—	32	—	37	—	40	—	46	—	48	—	56	ns
(Figure 4) HC/HCT158		6	—	27	—	—	—	34	—	—	—	41	—	—	
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Select to Output	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figure 3) HC/HCT158		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
(Figure 3 or 4)		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{in}		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC157, CD54/74HCT157
CD54/74HC158, CD54/74HCT158





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 - Inputs or select to output propagation delays and output transition times.

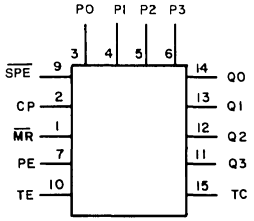
Fig. 4 - Enable to output propagation delays and output transition times.

File Number **1550**

CD54/74HC/HCT160, CD54/74HC/HCT161 CD54/74HC/HCT162, CD54/74HC/HCT163

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



92CS-37958

Presettable Counters

CD54/74HC/HCT160 BCD Decade Counter, Asynchronous Reset
CD54/74HC/HCT161 4-Bit Binary Counter, Asynchronous Reset
CD54/74HC/HCT162 BCD Decade Counter, Synchronous Reset
CD54/74HC/HCT163 4-Bit Binary Counter, Synchronous Reset

Type Features:

- *Synchronous Counting and Loading*
- *Two Count Enable Inputs for n-Bit Cascading*
- *Asynchronous Reset (CD54/74HC/HCT160, 161)*
- *Synchronous Reset (CD54/74HC/HCT162, 163)*
- *Look-Ahead Carry for High-Speed Counting*

The RCA-CD54/74HC/HCT160, 161, 162, and 163 devices are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The CD54/74HC/HCT160 and 161 are asynchronous reset decade and binary counters, respectively; the CD54/74HC/HCT162 and 163 devices are decade and binary counters, respectively and are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, $\overline{\text{SPE}}$, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for $\overline{\text{SPE}}$ are met).

All counters are reset with a low level on the Master Reset input, $\overline{\text{MR}}$. In the CD54/74HC/HCT162 and 163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the $\overline{\text{SPE}}$, PE and TE inputs (and the clock input, CP, in the CD54/74HC/HCT160 and 161 types).

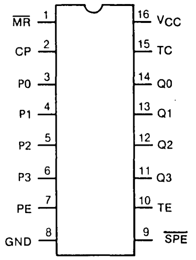
If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54HC160 through 163 and the CD54HCT160 through 163 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC160 through 163 and the CD74HCT160 through 163 are supplied in 16-lead dual-in-line plastic packages (E suffix), and in 16-lead dual-in-line surface mount plastic packages (M suffix). All types are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-36816R1

TERMINAL ASSIGNMENT

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}):	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	**400 mW**
For T_A = +70 to +125° C (PACKAGE TYPE M)	**Derate Linearly at 6 mW/° C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

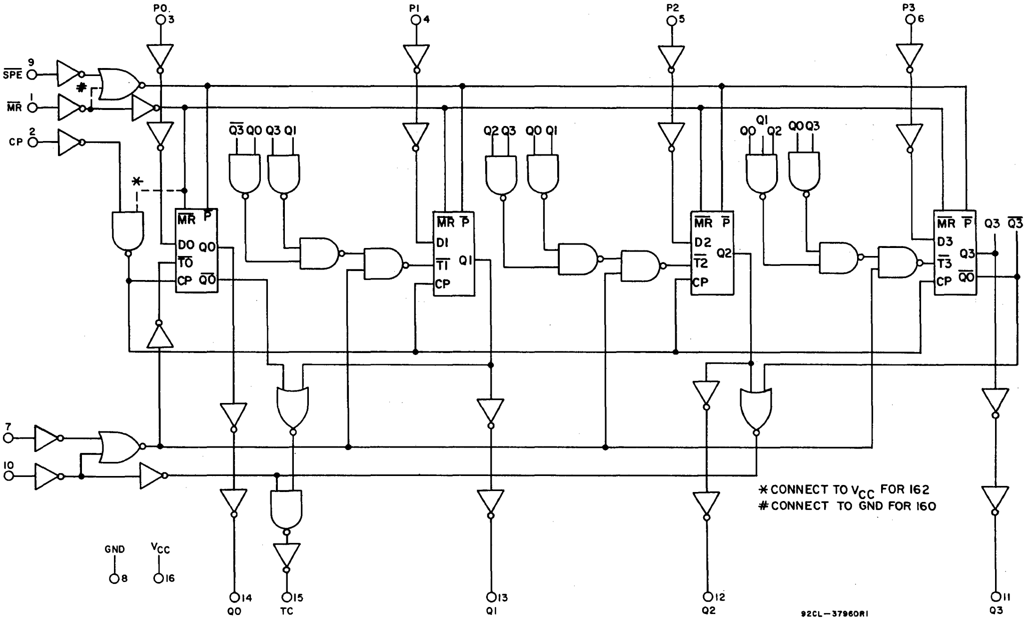
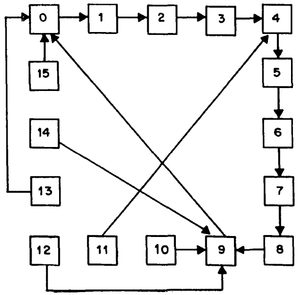


Fig. 1 - Logic diagram for the CD54/74HC/HCT160 and 162.



160,162 STATE DIAGRAM

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE COUNT.

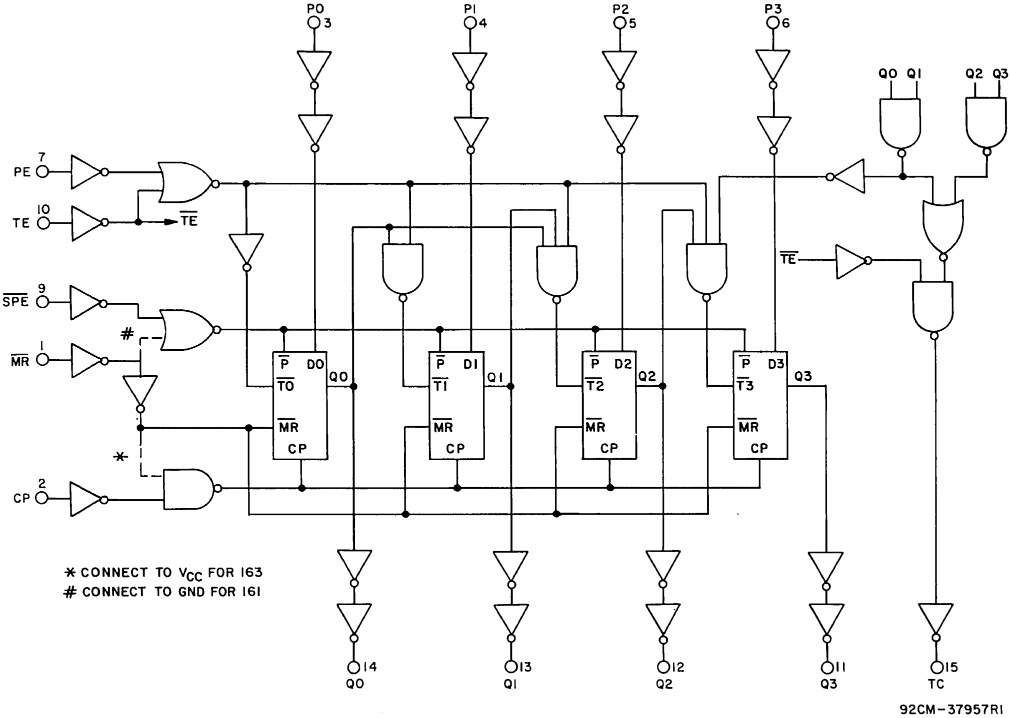


Fig. 2 - Logic diagram for the CD54/74HC/HCT161 and 163.

MODE SELECT - FUNCTION TABLE, 160, 161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	q_n	(a)
	H	X	X	l(b)	h(c)	X	q_n	L

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

MODE SELECT - FUNCTION TABLE, 162, 163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(f)	↑	X	X	l	l	L	L
	h(f)	↑	X	X	l	h	H	(d)
Count	h(f)	↑	h	h	h(f)	X	count	(d)
Inhibit	h(f)	X	l(e)	X	h(f)	X	q_n	(d)
	h(f)	X	X	l(e)	h(f)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES

(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH for 161 and HLLH for 160).
(b) The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{SPE}$ on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(d) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HLLH for 162 and HHHH for 163).
(e) The HIGH-to-LOW transition of PE or TE on the 54/74163 should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{SPE}$ or $\overline{MR}$ on the 54/74163 should only occur while CP is HIGH for conventional operation.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC160-163/CD54HC160-163										CD74HCT160-163/CD54HCT160-163									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
P0-P3	0.25
PE	0.65
CP	1.05
$\overline{MR}$	0.8
$\overline{SPE}$	0.5
TE	1.05

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC/HCT160, CD54/74HC/HCT161 CD54/74HC/HCT162, CD54/74HC/HCT163

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		SYMBOL	CL (pF)	TYPICAL		UNITS
				54/74HC	54/74HCT	
Propagation Delay	CP to TC	t_{PHL} t_{PLH}	15	15	18	ns
	CP to Qn		15	15	16	ns
	TE to TC		15	9	13	ns
	$\overline{MR}$ to Qn (160, 161)	t_{PHL}	15	18	21	ns
Power Dissipation Capacitance *		C_{PD}	—	60	63	pF

* CPD is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency. f_o = output frequency.
C_L = output load capacitance. V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Max. CP Freq. * f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	30	—	24	—	24	—	20	—	20	—	
	6	35	—	—	—	28	—	—	—	24	—	—	—	
CP Width (Low) $t_{W(L)}$	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{MR}$ Pulse Width t_W	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
	4.5	20	—	25	—	25	—	31	—	30	—	38	—	
	6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time t_{SU} Pn to CP	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	10	—	15	—	13	—	18	—	15	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Setup Time t_{SU} PE or TE to CP	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
	4.5	10	—	13	—	13	—	16	—	15	—	20	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	
Setup Time t_{SU} $\overline{SPE}$ to CP	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Setup Time t_{SU} $\overline{MR}$ to CP (162, 163)	2	65	—	—	—	80	—	—	—	100	—	—	—	ns
	4.5	13	—	13	—	16	—	16	—	20	—	20	—	
	6	11	—	—	—	14	—	—	—	17	—	—	—	
Hold Time t_H Pn to CP	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
	4.5	3	—	5	—	3	—	5	—	3	—	5	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Hold Time t_H TE or PE to CP	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	3	—	0	—	3	—	0	—	3	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Hold Time $\overline{SPE}$ to CP 160, 162 t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
161, 163 t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	3	—	0	—	3	—	0	—	3	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time t_{REC} $\overline{MR}$ to CP	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
	4.5	15	—	15	—	19	—	19	—	22	—	22	—	
	6	13	—	—	—	16	—	—	—	19	—	—	—	

* Applies to non-cascaded operation only. With cascaded counters clock to terminal count propagation delays, count enables (PE or TE)-to-clock set-up times, and count enables (PE or TE)-to-clock hold times determine max. clock frequency. For example with these HC devices:

$$f_{max}\text{(CP)} = \frac{1}{\text{CP-to-TC prop. delay + TE-to-CP setup + TE-to-CP Hold}} = \frac{1}{37+10+0} \approx 21\text{ MHz (min.)}$$

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	185	—	—	—	230	—	—	—	280	—	—	
CP to TC	t_{PHL}	4.5*	—	37	—	42	—	46	—	53	—	56	—	63	ns
		6	—	31	—	—	—	39	—	—	—	48	—	—	
	t_{PLH}	2	—	185	—	—	—	230	—	—	—	280	—	—	
CP to Qn	t_{PHL}	4.5	—	37	—	39	—	46	—	49	—	56	—	59	ns
		6	—	31	—	—	—	39	—	—	—	48	—	—	
	t_{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	
TE to TC	t_{PHL}	4.5	—	24	—	32	—	30	—	40	—	36	—	48	ns
		6	—	20	—	—	—	26	—	—	—	31	—	—	
		2	—	210	—	—	—	265	—	—	—	315	—	—	
$\overline{MR}$ to Qn,	t_{PHL}	4.5	—	42	—	50	—	53	—	63	—	63	—	75	ns
(160, 161)		6	—	36	—	—	—	45	—	—	—	54	—	—	
		2	—	210	—	—	—	265	—	—	—	315	—	—	
$\overline{MR}$ to TC	t_{PHL}	4.5	—	42	—	50	—	53	—	63	—	63	—	75	ns
		6	—	36	—	—	—	45	—	—	—	54	—	—	
		2	—	75	—	—	—	95	—	—	—	110	—	—	
Output Transition	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time	t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

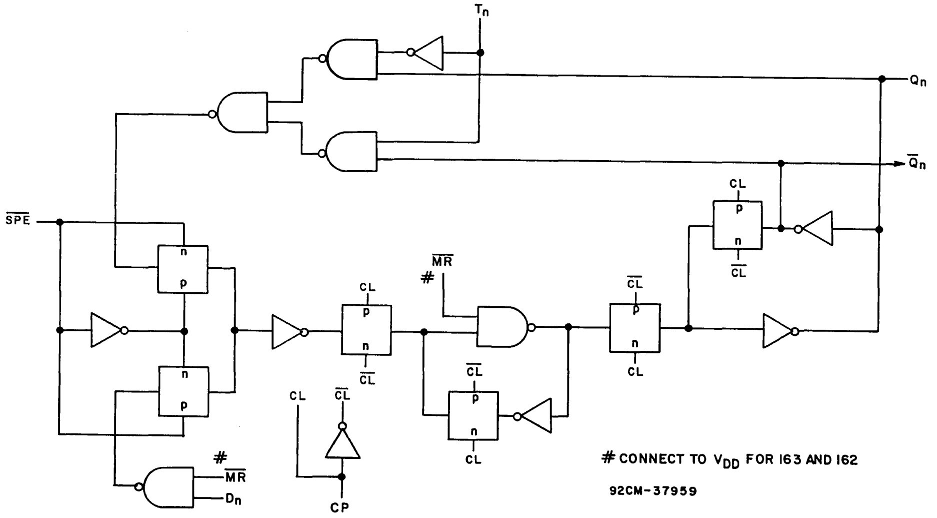
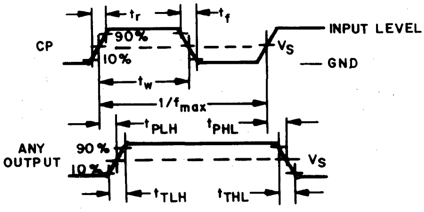


Fig. 3 - Detail of flip-flops for all types.

CD54/74HC/HCT160, CD54/74HC/HCT161 CD54/74HC/HCT162, CD54/74HC/HCT163

Transition times, propagation delay times, setup, hold, and recovery times.



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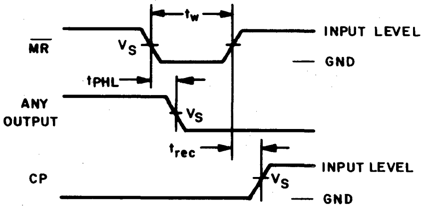

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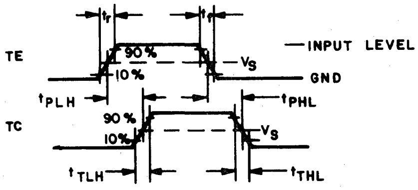

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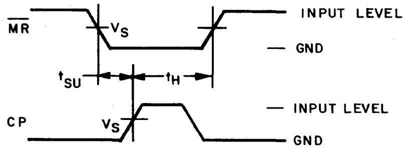

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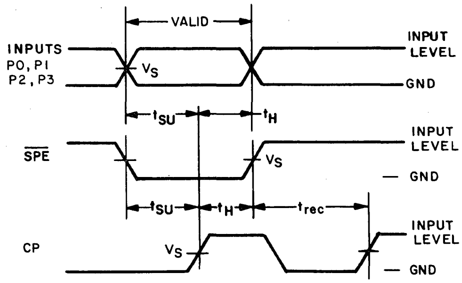

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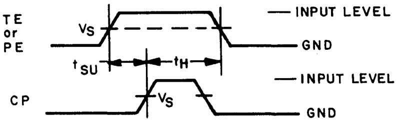
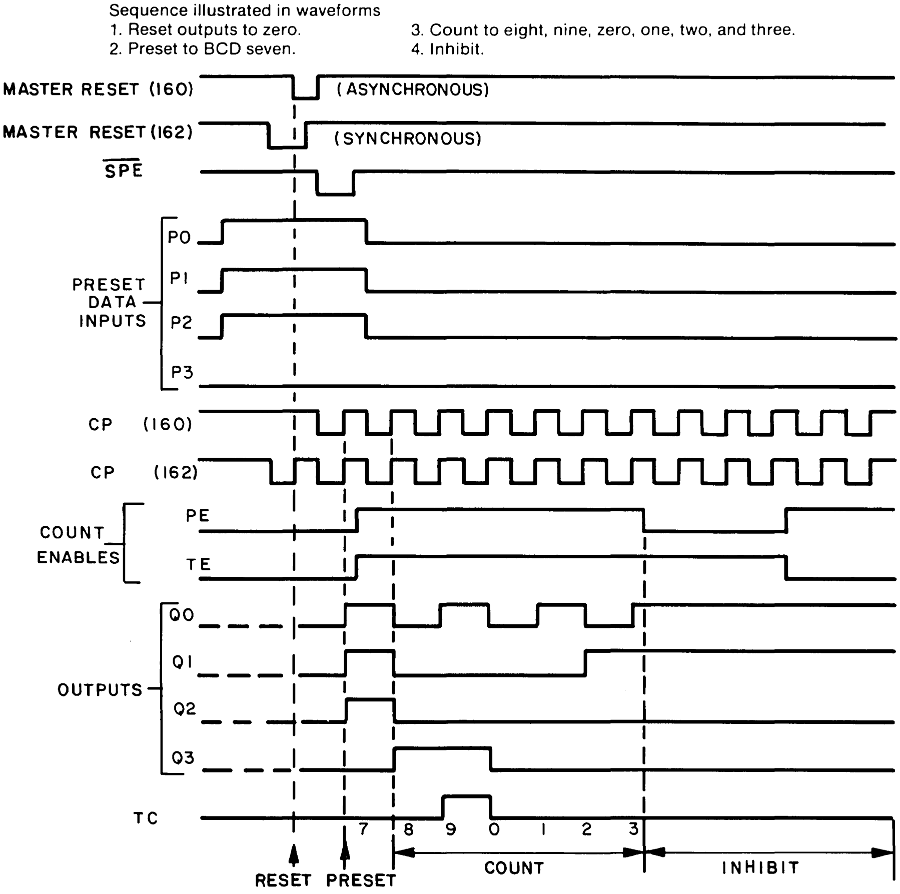


92CS-37969RI

	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
V_s	0.5 V_{CC}	1.3 V

Timing diagrams for the CD54/74HC/HCT160 and 162.

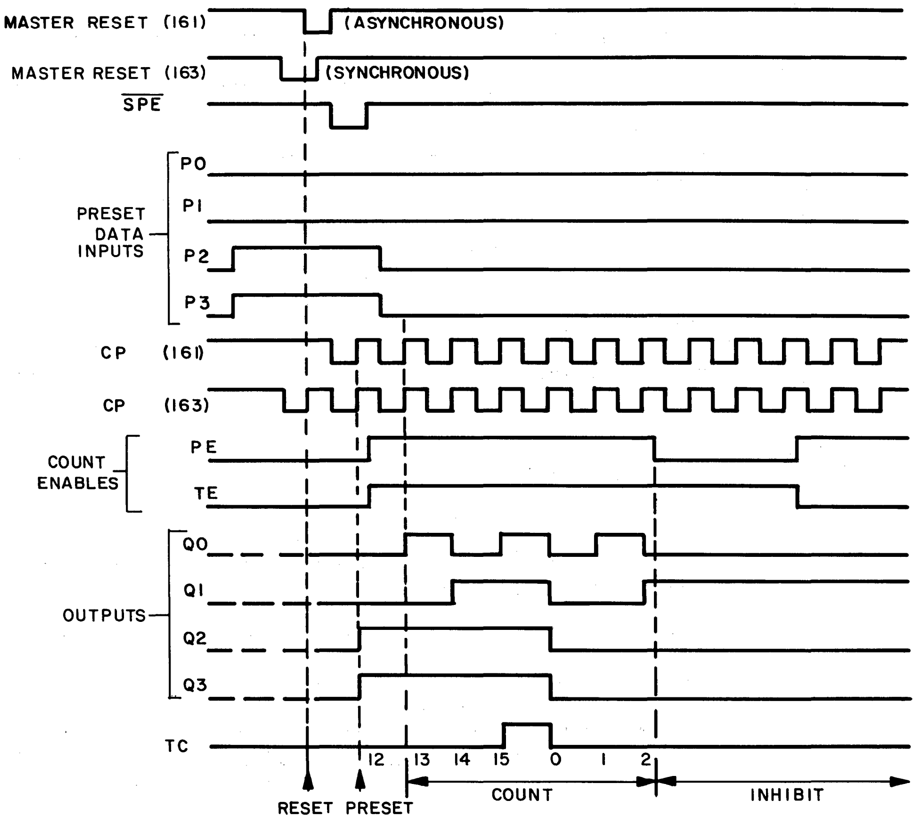


92CM-37963R1

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

Timing diagrams for the CD54/74HC/HCT161 and 163.

Sequence illustrated in waveforms
1. **Reset outputs to zero.**
2. **Preset to binary twelve.**
3. **Count to thirteen, fourteen, fifteen, zero, one, and two.**
4. **Inhibit.**

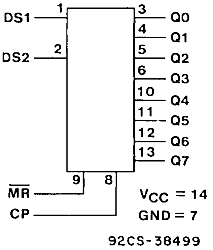


92CM-37962

File Number **1658**

CD54/74HC164
CD54/74HCT164

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Serial-In/Parallel-Out Shift Register

Type Features:

- *Buffered Inputs*
- *Asynchronous Master Reset*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC164 and CD54/74HCT164 are 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

The RCA CD54/74HC164 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT164 are supplied in a 14-lead plastic dual-in-line plastic package (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT164 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL}=30%,N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CD 54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1$ uA @ V_{OL}, V_{OH}*

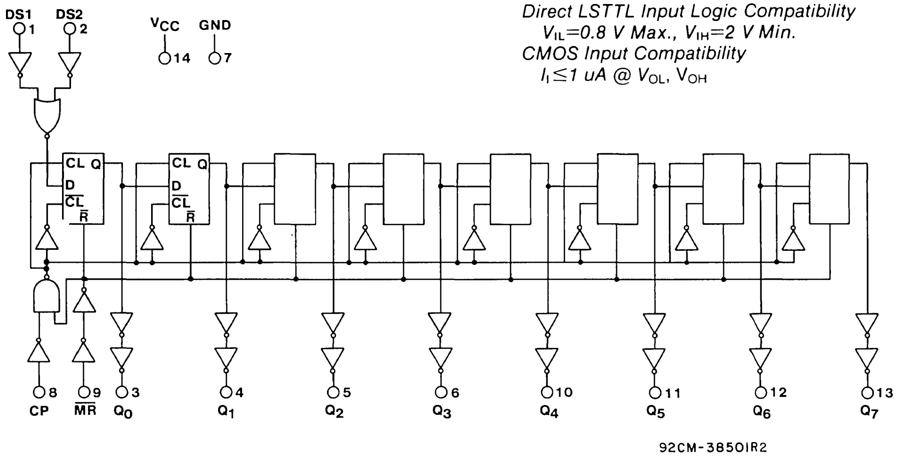


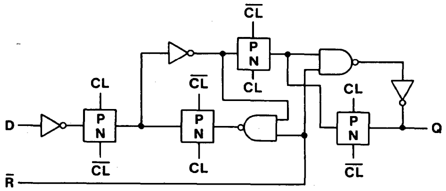
Fig. 1 - Logic diagram for the CD54/74HC164, CD54/74HCT164

CD54/74HC164
CD54/74HCT164

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs				Outputs	
	$\overline{MR}$	CP	DS1	DS2	Q0	Q1 — Q7
Reset (Clear)	L	X	X	X	L	L — L
Shift	H	↑	l	l	L	q_0 — q_6
	H	↑	l	h	L	q_0 — q_6
	H	↑	h	l	L	q_0 — q_6
	H	↑	h	h	H	q_0 — q_6

H=HIGH voltage level.
h=HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L=LOW voltage level.
l=LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q=Lower case letters indicate the state of the reference input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X=Don't care.
↑=LOW-to-HIGH clock transition.



92CS-38500RI

FLIP FLOP DETAIL

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}+0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A + +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE E, M	-40 to +85°C
PACKAGE TYPE F, H	-55 to +125°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC164/CD54HC164										CD74HCT164/CD54HCT164									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Date Shift-In (1,2)	0.3
$\overline{MR}$	0.9
Clock	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC164
CD54/74HCT164

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L pF	SYMBOL	Typical 54/74HC	Typical 54/74HCT	UNITS
Maximum Clock Frequency		15	f_{MAX}	60	54	MH_Z
Propagation Delay:	CP to Qn	15	t_{PLH}, t_{PHL}	14	15	ns
	$\overline{MR}$ to Qn	15	t_{PHL}	11	16	ns
Power Dissipation Capacitance		—	C_{PD}*	47	49	pF

C_{PD} is used to determine the dynamic power consumption, per device.

$P_D = C_{PD} V_{CC}^2 f_I + \Sigma\ (C_L V_{CC}^2 f_O)$ where:

f_I = input frequency.

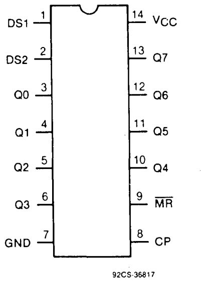
f_O = output frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MH_Z
		4.5	30	—	27	—	24	—	22	—	20	—	18	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
$\overline{MR}$ Pulse Width	t_W	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	18	—	15	—	23	—	18	—	27	—	
		6	10	—	—	—	13	—	—	—	15	—		—	
CP Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time	t_H	2	4	—	—	—	4	—	—	—	4	—	—	—	ns
		4.5	4	—	4	—	4	—	4	—	4	—	4	—	
		6	4	—	—	—	4	—	—	—	4	—	—	—	
$\overline{MR}$ to CP Removal Time	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	



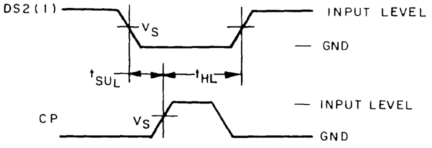
TERMINAL ASSIGNMENT

CD54/74HC164
CD54/74HCT164

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f= 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	170	—	—	—	212	—	—	—	255	—	—	
CP to Qn	t_{PHL}	4.5	—	34	—	36	—	43	—	45	—	51	—	54	ns
		6	—	29	—	—	—	36	—	—	—	43	—	—	
$\overline{MR}$ to Qn		2	—	140	—	—	—	175	—	—	—	210	—	—	
		4.5	—	28	—	38	—	35	—	46	—	42	—	57	ns
	t_{PHL}	6	—	24	—	—	—	30	—	—	—	36	—	—	
Output		2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
	t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

Transition times, propagation delay times, setup, hold times, and removal times.



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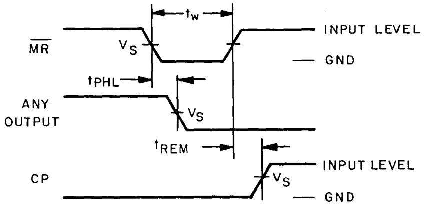

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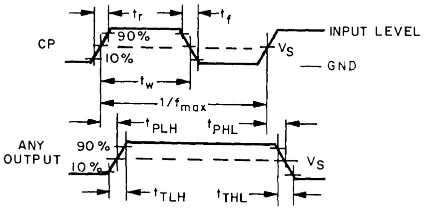
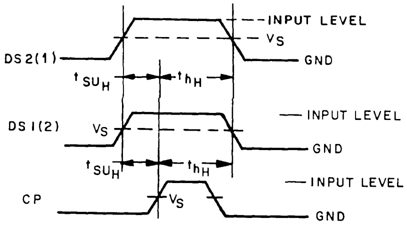


92CS-37964



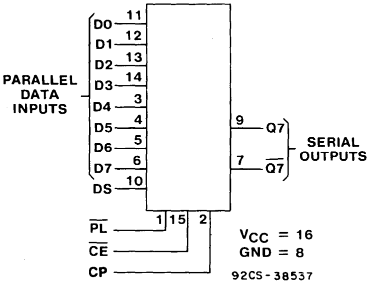
92CS-38398

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

CD54/74HC165
CD54/74HCT165

File Number **1672**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Parallel-In/ Serial-Out Shift Register

Type Features:

- *Buffered Inputs*
- *Asynchronous Parallel Load*
- *Complementary Outputs*
- *Typical* $f_{MAX} = 60$ *MHz @* $V_{CC} = 5V$, $C_L = 15$ *pF*, $T_A = 25°C$

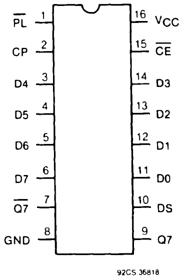
The RCA-CD54/74HC165 and CD54/74HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q7 and $\overline{Q7}$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the $\overline{PL}$ is HIGH, data enters the register serially at the DS input and shifts one place to the right (Q0→Q1→Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q7 output to the DS input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of $\overline{CE}$ should only take place while CP is HIGH. Also, CP and $\overline{CE}$ should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when $\overline{PL}$ goes HIGH.

The CD54HC/HCT165 devices are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT165 devices are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}*; @* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ *V Max.*, $V_{IH} = 2$ *V Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1$ *μA @* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

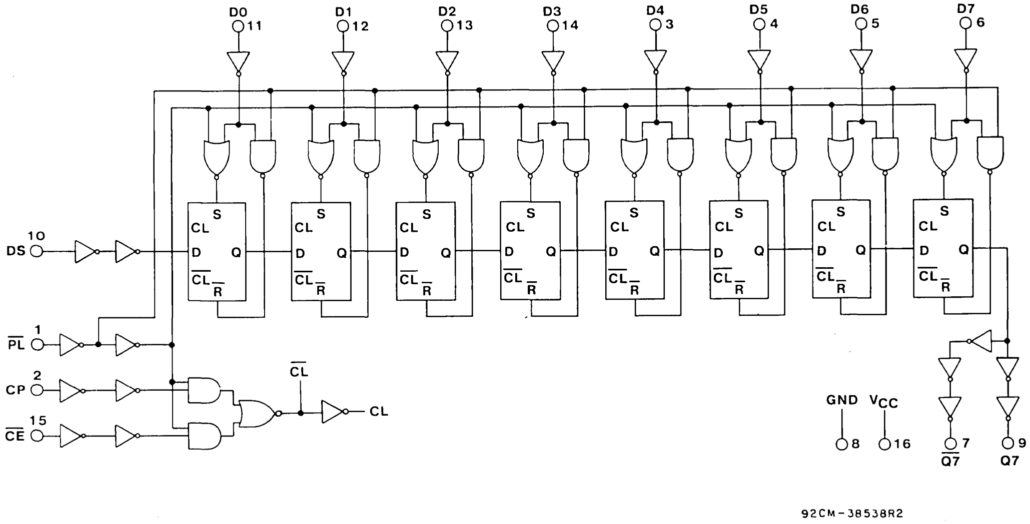


Fig. 1 — Logic diagram for the CD54/74HC165 and CD54/74HCT165.

TRUTH TABLE

Operating Modes	Inputs					Qn Register		Outputs	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0-D7	Q0	Q1-Q6	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	↑	l	X	L	q_0-q_5	q_6	$\overline{q_6}$
	H	L	↑	h	X	H	q_0-q_5	q_6	$\overline{q_6}$
Hold "Do Nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	$\overline{q_7}$

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

CD54/74HC165
CD54/74HCT165

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC165/CD54HC165										CD74HCT165/CD54HCT165									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DS, D0 to D7	0.35
CP, $\overline{PL}$	0.65

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC165
CD54/74HCT165

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Propagation Delay					
CP to Q7	15	t_{PHL}	13	17	ns
$\overline{PL}$ to Q7	15	t_{PLH}	14	17	ns
D7 to Q7	15		12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	17	24	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_O)$ where:

f_i = input frequency

f_o = output frequency

C_L = output load capacitance.

V_{CC} = supply voltage.

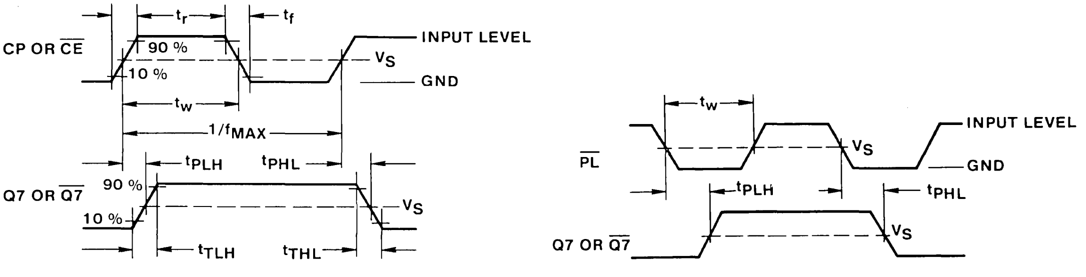
CD54/74HC165
CD54/74HCT165

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_{WL}	2	80	—	—	—	100	—	—	—	120	—	—	—	
	t_{WH}	4.5	16	—	18	—	20	—	23	—	24	—	27	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{PL}$ Pulse Width	t_{WL}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time		2	80	—	—	—	100	—	—	—	120	—	—	—	
DS to CP	t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{CE}$ to CP	$t_{SU(L)}$	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
D0-D7 to $\overline{PL}$	t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time		2	35	—	—	—	45	—	—	—	55	—	—	—	
DS to CP	t_H	4.5	7	—	7	—	9	—	9	—	11	—	11	—	ns
or $\overline{CE}$		6	6	—	—	—	8	—	—	—	9	—	—	—	
		2	0	—	—	—	0	—	—	—	0	—	—	—	
$\overline{CE}$ to CP	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	ns
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time		2	100	—	—	—	125	—	—	—	150	—	—	—	
$\overline{PL}$ to CP	t_{REC}	4.5	20	—	20	—	25	—	25	—	30	—	30	—	ns
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Maximum Clock		2	6	—	—	—	5	—	—	—	4	—	—	—	
Pulse Frequency	f_{MAX}	4.5	30	—	27	—	24	—	22	—	20	—	18	—	MHz
		6	35	—	—	—	28	—	—	—	24	—	—	—	

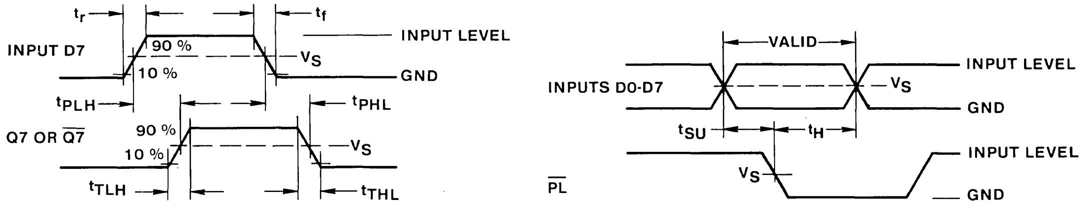
SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
CP or $\overline{CE}$ to	t_{PHL}	4.5	—	33	—	40	—	41	—	50	—	50	—	60	ns
Q7 or $\overline{Q7}$		6	—	28	—	—	—	35	—	—	—	43	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	-	—	265	—	—	
$\overline{PL}$ to Q7 or	t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
$\overline{Q7}$		6	—	30	—	—	—	37	—	—	—	45	—	—	
D7 to Q7 or	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{Q7}$	t_{PHL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Output Transition	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Time		6	—	13	—	—	—	16	—	—	—	19	—	—	
			—	—	—	—	—	—	—	—	—	—	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
			—	—	—	—	—	—	—	—	—	—	—	—	



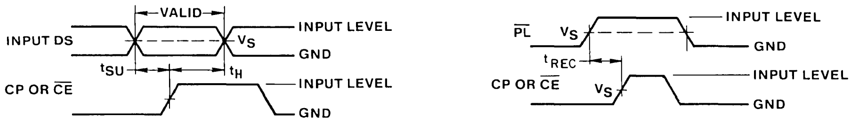
(a) SERIAL-SHIFT MODE
92CS-38539

(b) PARALLEL-LOAD MODE
92CS-38540



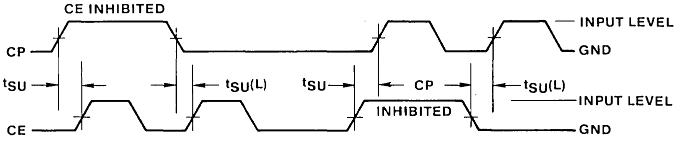
(c) PARALLEL-LOAD MODE
92CS-38541

(d) PARALLEL-LOAD MODE
92CS-38542



(e) SERIAL-SHIFT MODE

(f) SERIAL-SHIFT MODE



(g) SERIAL-SHIFT, CLOCK-INHIBIT MODE
92CM-38543R2

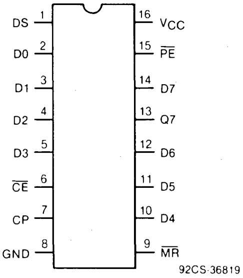
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 — Switching waveforms for the CD54/74HC165 and the CD54/74HCT165

CD54/74HC166
CD54/74HCT166

File Number **1501**

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

8-Bit Parallel-In/Serial-Out Shift Register

Type Features:

- *Buffered inputs*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC166 and CD54/74HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

The CD54/74HCT166 is functionally as well as pin compatible with the standard 54LS/74LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data Input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

The CD54HC166 and CD54HCT166 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC166 and CD74HCT166 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

CD54/74HC166
CD54/74HCT166

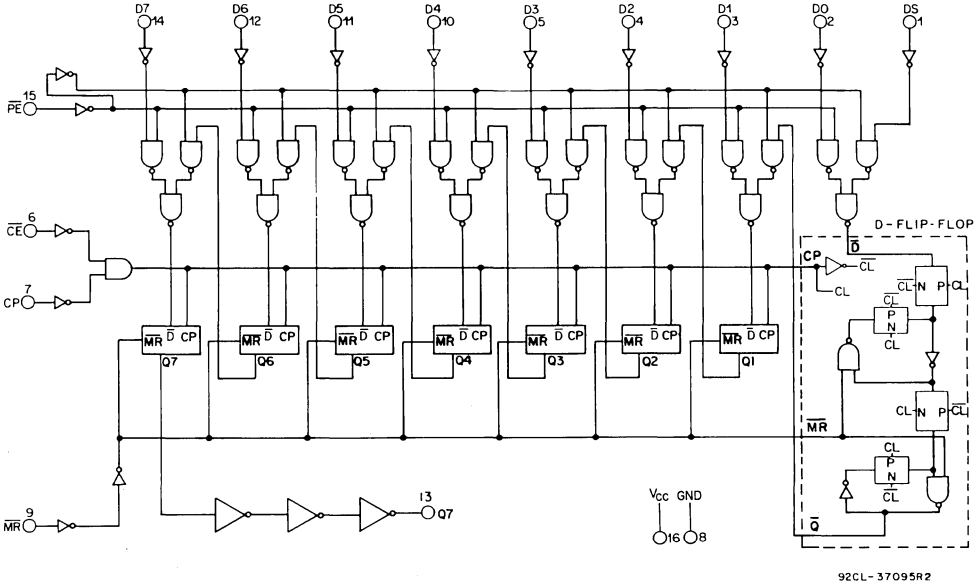


Fig. 1 - Logic diagram.

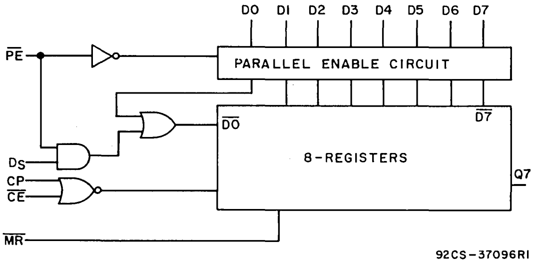


Fig. 2 - Functional diagram.

TRUTH TABLE

Inputs						Internal Q States	Output
					Parallel		
Master Reset	Parallel Enable	Clock Enable	Clock	Serial	D_0 D_7	Q_0 Q_1	Q7
L	X	X	X	X	X	L L	L
H	X	L	L	X	X	Q_{00} Q_{10}	Q_0
H	L	L	↑	X	a . . . h	a b	h
H	H	L	↑	H	X	H Q_{0n}	Q_{6n}
H	H	L	↑	L	X	L Q_{0n}	Q_{6n}
H	X	H	↑	X	X	Q_{00} Q_{10}	Q_{70}

H = high level (steady state).
L = low level (steady state).
X = irrelevant (any input, including transitions).
↑ = transition from low to high level.

a . . . h = the level of steady-state input at inputs D_0 thru D_7, respectively.
Q_{00}, Q_{10}, Q_{70} = the level of Q_0, Q_1, or Q_7, respectively, before the indicated steady-state input conditions were established.
Q_{0n}, Q_{6n} = the level of Q_0 or Q_6, respectively, before the most recent ↑ transition of the clock.

CD54/74HC166
CD54/74HCT166

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC166/CD54HC166										CD74HCT166/CD54HCT166									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	--	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	--	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DS, D0-D7	0.2
$\overline{PE}$	0.35
CP, $\overline{CE}$	0.5
$\overline{MR}$	0.2

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC166
CD54/74HCT166

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For TA = Full Package Temperature Range) VCC:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage VIN, VOUT	0	VCC	V
Operating Temperature TA:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, tr, tf			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	Typical		Units
			HC	HCT	
Propagation Delay- Clock to Q	t_{PLH} t_{PHL}	15	13	17	ns
Maximum Clock Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	41	41	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

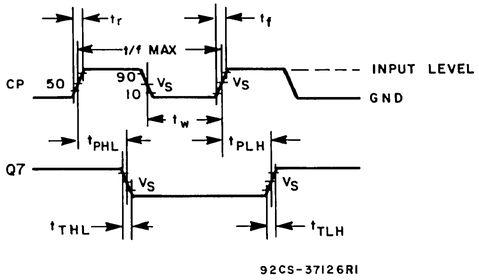
CD54/74HC166
CD54/74HCT166

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION Vcc V	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency f_{max}	2	6		—		5		—		4		—		MHz
Fig. 3	4.5	30		25		25		20		20		16		
	6	35		—		29		—		23		—		
$\overline{MR}$ Pulse Width t_w	2	100		—		125		—		150		—		ns
Fig. 4	4.5	20		35		25		44		30		53		
	6	17		—		21		—		26		—		
Clock Pulse Width t_w	2	80		—		100		—		120		—		ns
Fig. 3	4.5	16		20		20		25		24		30		
	6	14		—		17		—		20		—		
Set-up Time t_{SU}	2	80		—		100		—		120		—		ns
Data and $\overline{CE}$ to	4.5	16		16		20		20		24		24		
Clock, Fig. 5, 6	6	14		—		17		—		20		—		
Hold Time t_H	2	1		—		1		—		1		—		ns
Data to Clock,	4.5	1		0		1		0		1		0		
Fig. 5	6	1		—		1		—		1		—		
Removal Time t_{REM}	2	0		—		0		—		0		—		ns
$\overline{MR}$ to Clock	4.5	0		0		0		0		0		0		
Fig. 4	6	0		—		0		—		0		—		
Set-up Time t_{SU}	2	145		—		180		—		220		—		ns
$\overline{PE}$ to CP	4.5	29		30		36		38		44		45		
Fig. 6	6	25		—		31		—		38		—		
Hold Time t_H	2	0		—		0		—		0		—		ns
$\overline{PE}$ to CP or $\overline{CE}$	4.5	0		0		0		0		0		0		
Fig. 6	6	0		—		0		—		0		—		

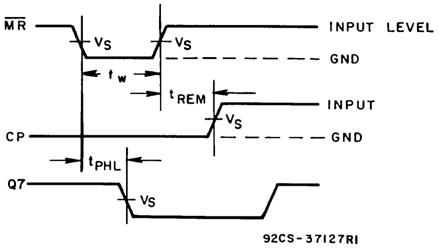
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION Vcc V	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2		160		—		200		—		240		—	ns
Clock to Output t_{PHL}	4.5		32		40		40		50		48		60	
Fig. 3	6		27		—		34		—		41		—	
Output Transition t_{TLH}	2		75		—		95		—		110		—	ns
Time t_{THL}	4.5		15		15		19		19		22		22	
Fig. 3	6		13		—		16		—		19		—	
Propagation Delay t_{PHL}	2		160		—		200		—		240		—	ns
$\overline{MR}$ to Output	4.5		32		40		40		50		48		60	
Fig. 4	6		27		—		34		—		41		—	
Input Capacitance C_I			10		10		10		10		10		10	pF



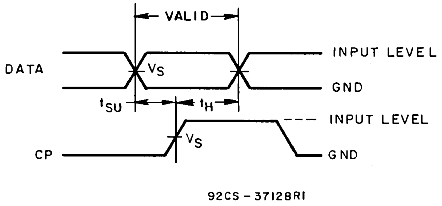
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 3 - Clock pre-requisite times and propagation and output transition times.



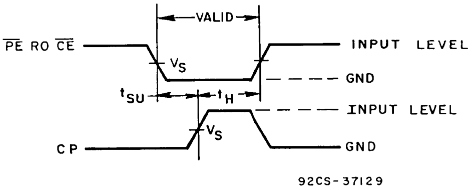
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 4 - Master reset pre-requisite times and propagation delays.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 5 - Data pre-requisite times.



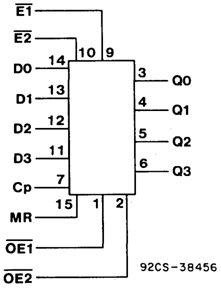
	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3.0 V
V_S	50% V_{CC}	1.3 V

Fig. 6 - Parallel enable or clock enable pre-requisite times.

CD54/74HC173
CD54/74HCT173

File Number **1641**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad D-Type Flip-Flop, 3-State

Positive-Edge Triggered

Type Features:

- *3-state buffered outputs*
- *gated input and output enables*

The RCA CD54/74HC173 and CD54/74HCT173 high speed 3-STATE QUAD D TYPE FLIP-FLOPS are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and 3-STATE feature make these parts ideally suited for interfacing with bus lines in bus oriented systems.

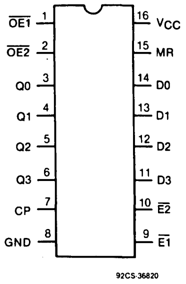
The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The outputs are in the 3-STATE mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The CD54/74HCT173 logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC173 and CD54HCT173 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC173 and D74HCT173 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

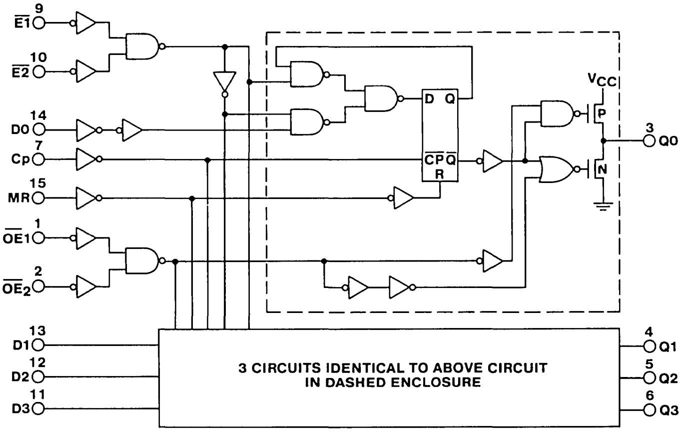
Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC} @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ V *max.,* $V_{IH} = 2$ V *Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



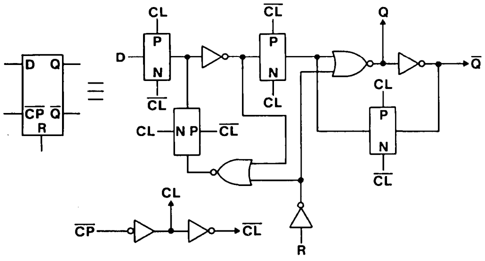
TERMINAL ASSIGNMENT

CD54/74HC173
CD54/74HCT173



92CM-38458RI

Fig. 1 — Logic diagram for the CD54/74HC/HCT173.



92CS-38457

Flip-Flop Detail

TRUTH TABLE

Inputs					Output
		Data Enable		Data	
MR	**CP**	**$\overline{E1}$**	**$\overline{E2}$**	**D**	**Q**
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	_/‾	H	X	X	Q_0
L	_/‾	X	H	X	Q_0
L	_/‾	L	L	L	L
L	_/‾	L	L	H	H
When either $\overline{OE1}$ or $\overline{OE2}$ (or both) is (are) high the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.					

H = high level (steady state)
L = low level (steady state)
_/‾ = low-to-high level transition
X = don't care (any input including transitions)
Q_0 = the level of Q before the indicated steady-state input conditions were established.

CD54/74HC173
CD54/74HCT173

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) .... ± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC173
CD54/74HCT173

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC173/CD54HC173										CD74HCT173/CD54HCT173									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0-D3	0.15
$\overline{E1}$ & $\overline{E2}$	0.15
CP	0.25
$\overline{MR}$	0.2
$\overline{OE1}$ & $\overline{OE2}$	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC173
CD54/74HCT173

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Clock to Q	t_{PLH} t_{PHL}	15	17	18	ns
Propagation Delay, Output Disable and Enable to Q	t_{PLZ} t_{PHZ}	15	12	12	ns
	t_{PZL} t_{PZH}	15	12	14	ns
Maximum Clock Frequency	f_{max}	—	60	60	MHz
Power Dissipation Capacitance*	C_{PD}	—	29	34	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock	2	6		—		5		—		4		—		
Frequency f_{max}	4.5	30		20		24		16		20		13		MHz
Fig. 3	6	35		—		28		—		24		—		
	2	80		—		100		—		120		—		
MR Pulse Width t_w	4.5	16		15		20		19		24		22		ns
Fig. 4	6	14		—		17		—		20		—		
	2	80		—		100		—		120		—		
Clock Pulse Width t_w	4.5	16		25		20		31		24		38		ns
Fig. 3	6	14		—		17		—		20		—		
Set-up Time	2	60		—		75		—		90		—		
Data to Clock	4.5	12		12		15		15		18		18		ns
Fig. 5 t_{SU}	6	10		—		13		—		15		—		
Set-up Time	2	60		—		75		—		90		—		
$\overline{E}$ to Clock	4.5	12		18		15		23		18		27		ns
t_{SU}	6	10		—		13		—		15		—		
Hold Time	2	3		—		3		—		3		—		
Data to Clock	4.5	3		0		3		0		3		0		ns
Fig. 5 t_H	6	3		—		3		—		3		—		
Hold Time	2	0		—		0		—		0		—		
$\overline{E}$ to Clock	4.5	0		0		0		0		0		0		ns
t_H	6	0		—		0		—		0		—		
Removal Time	2	60		—		75		—		90		—		
MR to Clock t_{REM}	4.5	12		12		15		15		18		18		ns
	6	10		—		13		—		15		—		

SWITCHING CHARACTERISTICS (V_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	
Clock to Output	t_{PHL}	4.5	—	40	—	43	—	50	—	54	—	60	—	65	ns
Fig. 3		6	—	34	—	—	—	43	—	—	—	51	—	—	
Propagation Delay		2	—	175	—	—	—	220	—	—	—	265	—	—	
MR to Output	t_{PHL}	4.5	—	35	—	37	—	44	—	46	—	53	—	56	ns
Fig. 4		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay,	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Enable to Q	t_{PHZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PZH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
Fig.6		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
Fig. 3		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10		10		10		10		10		10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

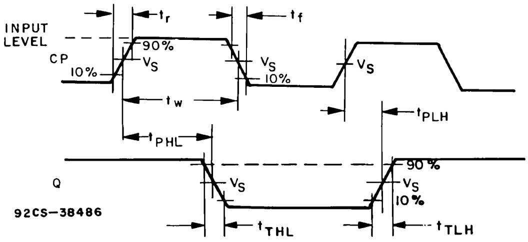


Fig. 3 — Clock to output delays and clock pulse width.

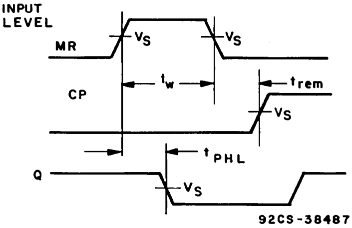


Fig. 4 — Master reset pulse width. Master reset to output delay and master reset to clock recovery time.

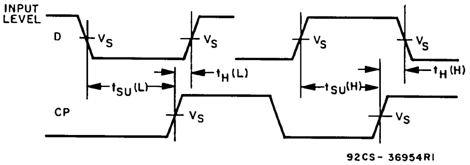


Fig. 5 — Data set-up and hold times.

	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Vs	0.5 V_{CC}	1.3 V

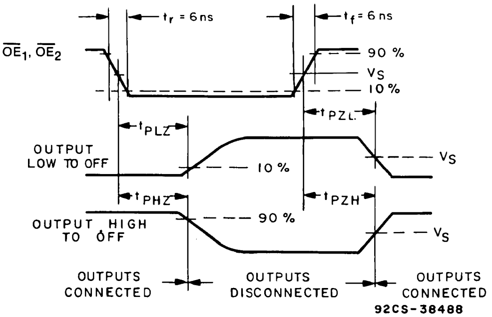
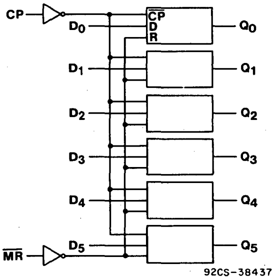


Fig. 6 — Transition times and propagation delay times.

CD54/74HC174
CD54/74HCT174

File Number **1608**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Hex D-Type Flip-Flop with Reset

Positive-Edge Triggered

Type Features:

- *Buffered Positive-Edge-Triggered Clock*
- *Asynchronous Common Reset*

The RCA-CD54/74HC174 and CD54/74HCT174 are edge triggered flip-flops which utilize silicon gate CMOS circuitry to implement D-type flip-flops. They possess low power and speeds comparable to low power Schottky TTL circuits. The devices contain 6 master-slave flip-flops with a common clock and common reset. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The $\overline{MR}$ input, when low, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The CD54/74HCT174 is functionally as well as pin compatible to the 54LS174/74LS174.

The CD54HC174 and CD54HCT174 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC174 and CD74HCT174 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
    $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC};
    @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
    $V_{IL} = 0.8$ V *max.*, $V_{IH} = 2$ V *Min.*
  CMOS Input Compatibility
    $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

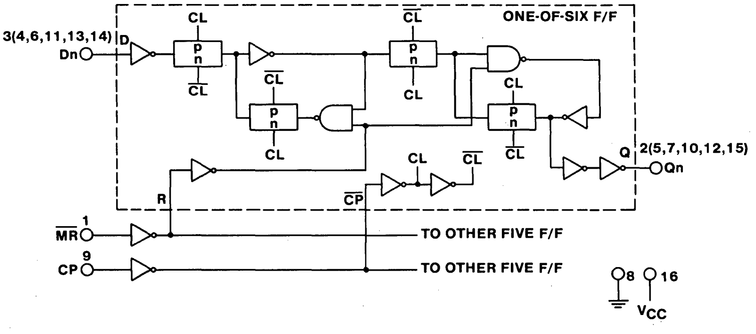


Fig. 1 — Logic diagram (Flip/Flop detail)

CD54/74HC174
CD54/74HCT174

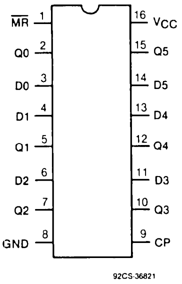
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Qo

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
Qo, = Level Before the Indicated Steady-State
Input Conditions were established



TOP VIEW

TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC174
CD54/74HCT174

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC174/CD54HC174										CD74HCT174/CD54HCT174									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
CP	0.80
$\overline{MR}$	0.55
D	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC174
CD54/74HCT174

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Pulse	2	80	—	—	—	100	—	—	—	120	—	—	—	
Width t_w	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 3	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{\text{MR}}$ Pulse Width t_w	4.5	16	—	25	—	20	—	31	—	24	—	38	—	ns
Fig. 4	6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time Data	2	60	—	—	—	75	—	—	—	90	—	—	—	
to Clock t_{SU}	4.5	12	—	16	—	15	—	20	—	18	—	24	—	ns
Fig. 5	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data	2	5	—	—	—	5	—	—	—	5	—	—	—	
to Clock t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 5	6	5	—	—	—	5	—	—	—	5	—	—	—	
Removal Time	2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{\text{MR}}$ to Clock t_{rem}	4.5	5	—	12	—	5	—	15	—	5	—	18	—	ns
Fig. 4	6	5	—	—	—	5	—	—	—	5	—	—	—	
	2	6	—	—	—	5	—	—	—	4	—	—	—	
Clock Frequency f_{max}	4.5	30	—	25	—	24	—	20	—	20	—	17	—	MHz
	6	35	—	—	—	28	—	—	—	24	—	—	—	

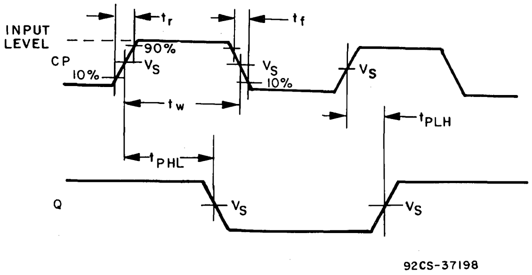
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
Clock to Q t_{PHL}	4.5	—	33	—	40	—	41	—	50	—	50	—	60	ns
Fig. 3	6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{\text{MR}}$ to Q t_{PHL}	4.5	—	30	—	44	—	38	—	55	—	45	—	66	ns
Fig. 4	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Fig. 6	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

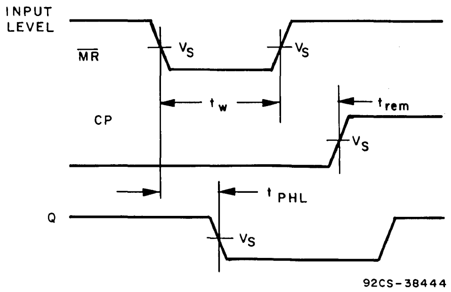
CHARACTERISTIC		C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay — Clock to Q Fig.3	t_{PLH} t_{PHL}	15	13	17	ns
Propagation Delay — MR to Q Fig. 4	t_{PLH} t_{PHL}	15	12	18	ns
Power Dissipation Capacitance*	C_{PD}	—	38	44	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage



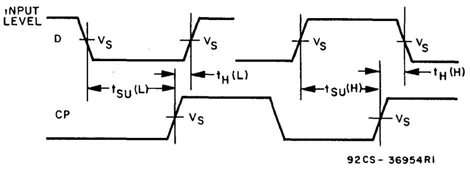
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 — Propagation delay times and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 — Prerequisite and propagation delay times for master reset.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 — Pre

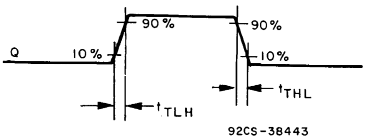
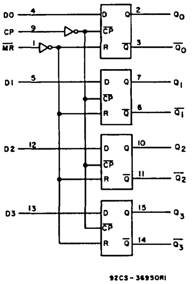


Fig. 6 — Transition times.

File Number **1474**

CD54/74HC175
CD54/74HCT175

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad D Flip-Flop with Reset

Type Features:

- *Common Clock and Asynchronous Reset on four D-Type Flip-Flops*
- *Positive-edge pulse triggering*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA CD54/74HC175 and the CD54/74HCT175 are high speed Quad D-Type Flip-Flops with individual D-inputs and Q, $\overline{Q}$ complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four $\overline{Q}$ outputs to a logic 1.

The CD54HC175 and CD54HCT175 are supplied in 16-lead dual-in-line ceramic packages (F suffix) and the CD74HC175 and CD74HCT175 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

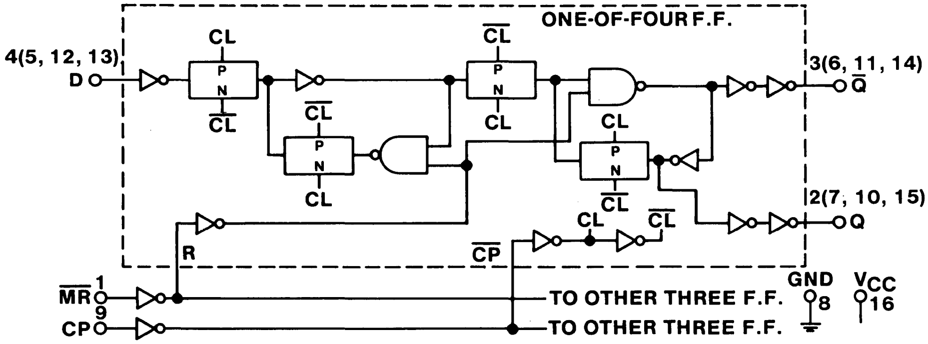


Fig. 1 - Logic block diagram.

92CM-36949R1

CD54/74HC175
CD54/74HCT175

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{V}$) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal conditions should be selected so that operation is always within the following ranges:

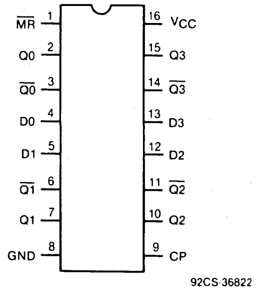
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
RESET ($\overline{MR}$)	CLOCK CP	DATA D_n	Q_n	$\overline{Q_n}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
Q_0, $\overline{Q_0}$ = Levels Before the Indicated Steady-State Input Conditions were Established



TERMINAL ASSIGNMENT

CD54/74HC175
CD54/74HCT175

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC175/CD54HC175										CD74HCT175/CD54HCT175									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{MR}$	1.0
D	0.15
CP	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC175
CD54/74HCT175

PRE-REQUISITE FOR SWITCHING FUNCTION 54/74HC SERIES AND 54/74HCT SERIES

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	Vcc V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Pulse	2	80	—	—	—	100	—	—	—	120	—	—	—	
Width t_W	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 3	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{MR}$ Pulse Width t_W	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 4	6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time Data	2	80	—	—	—	100	—	—	—	120	—	—	—	
to Clock t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 5	6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time Data	2	5	—	—	—	5	—	—	—	5	—	—	—	
to Clock t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 5	6	5	—	—	—	5	—	—	—	5	—	—	—	
Removal Time	2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{MR}$ to Clock t_{REM}	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 4	6	5	—	—	—	5	—	—	—	5	—	—	—	
	2	6	—	—	—	5	—	—	—	4	—	—	—	
Clock Frequency f_{max}	4.5	30	—	25	—	25	—	20	—	20	—	16	—	MHz
	6	35	—	—	—	29	—	—	—	23	—	—	—	

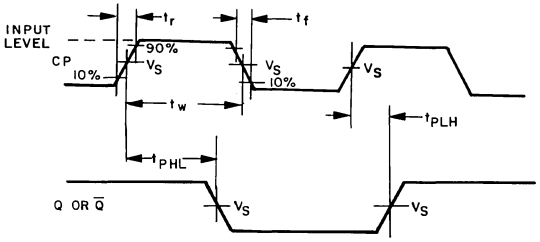
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to + 125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
Clock to Q or $\overline{Q}$ t_{PHL}	4.5	—	35	—	33	—	44	—	41	—	53	—	50	ns
Fig. 3	6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
($\overline{MR}$) to Q or $\overline{Q}$ t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
Fig. 4	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Fig. 6	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	Typical		Units
			HC	HCT	
Propagation Delay- Clock to Q or $\overline{Q}$, Fig. 3	t_{PLH} t_{PHL}	15	14	13	ns
Propagation Delay $\overline{MR}$ to Q or $\overline{Q}$, Fig. 4	t_{PHL} t_{PLH}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	65	67	pF

*CPD is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2f_i + \Sigma C_LV_{CC}^2f_o$ where f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

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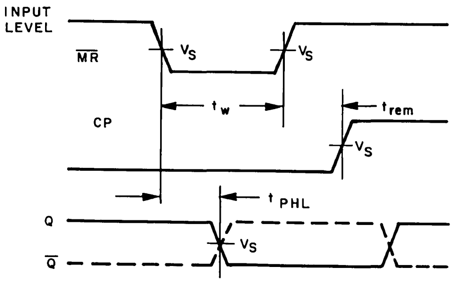
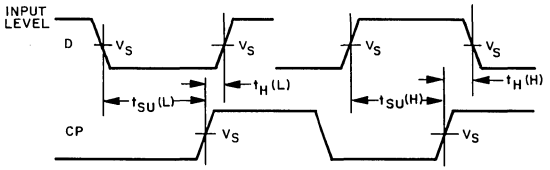
Fig. 3 - Propagation delay times and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-36952

Fig. 4 - Pre-requisite and propagation delay times for master reset.



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	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 - Pre-requisite for clock.

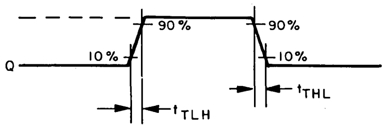

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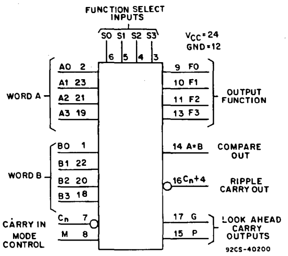
Fig. 6 - Transition times.

CD54/74HC181
CD54/74HCT181

File Number **1829**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM
ACTIVE-HIGH DATA

4-Bit Arithmetic Logic Unit

Type Features:
- *Full look-ahead carry for speed operations on long words*
- *Generates 16 logic functions of two Boolean variables*
- *Generates 16 arithmetic functions of two 4-bit binary words*
- *A = B comparator output available (open drain)*
- *Ripple-carry input and output available*
- *Available in both narrow- and wide-body plastic packages*

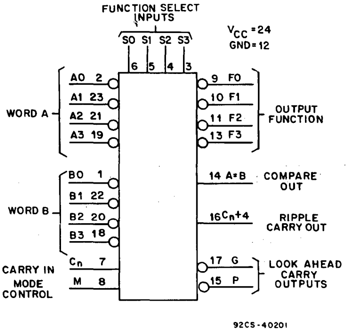
The RCA CD54/74HC181 and CD54/74HCT181 are low-power four-bit parallel arithmetic logic units (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M=High) or arithmetic (M=Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive-OR and -NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The HC/HCT181 operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs, by using the appropriate truth table.

The HC/HCT181 contains logic for full look-ahead carry operation for fast-carry generation using the carry-generate and carry-propagate outputs G and P for the four bits of the HC/HCT181. Use of the HC/HCT182 look-ahead carry generator in conjunction with multiple HC/HCT181s permits high-speed arithmetic operations on long words. A ripple-carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in these devices is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. A=B is an open-drain output that can be wire-AND connected to give a comparison for more than 4 bits. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in the Magnitude Comparison table.

The CD54HC181 and CD54HCT181 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC181 and CD74HCT181 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL}*=30%,* N_{IH}*=30% of* V_{CC}*; @* V_{CC}*=5 V*
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}*=0.8 V max.,* V_{IH}*=2 V min.*
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}*,* V_{OH}



FUNCTIONAL DIAGRAM
ACTIVE-LOW DATA

CD54/74HC181
CD54/74HCT181

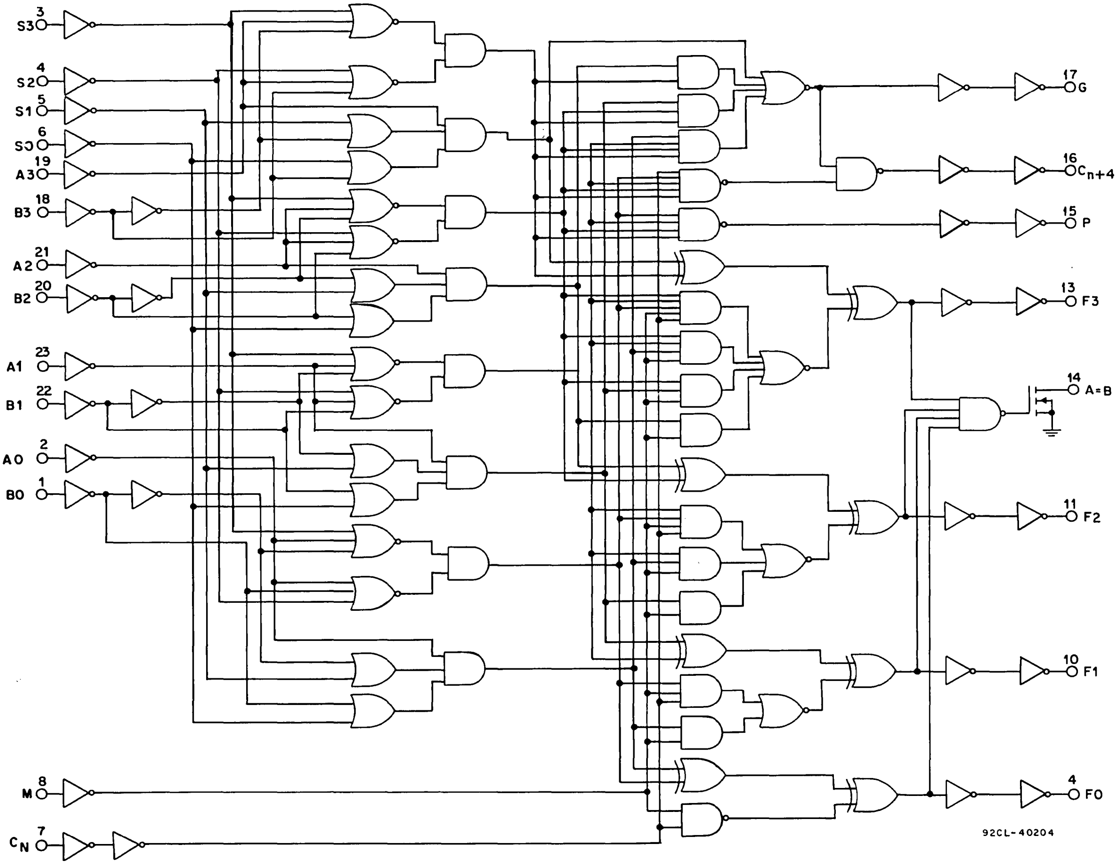


Fig. 1 - Logic diagram.

FUNCTION TABLES

Function Select				Inputs/Outputs Active High		
				Logic Function	Arithmetic Function M = L	
S3	S2	S1	S0	M = H	C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A + B}$	A + B	(A + B) plus 1
L	L	H	L	$\overline{A}B$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
L	L	H	H	Logic 0	minus 1(2's compl.)	Zero
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$	A plus A$\overline{B}$ plus 1
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$	(A+B)plusA$\overline{B}$plus1
L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
L	H	H	H	A$\overline{B}$	A$\overline{B}$ minus 1	A$\overline{B}$
H	L	L	L	$\overline{A}$ + B	A plus AB	A plus AB plus 1
H	L	L	H	$\overline{A \oplus B}$	A plus B	A plus B plus 1
H	L	H	L	B	(A + $\overline{B}$) plus AB	(A+$\overline{B}$)plusABplus1
H	L	H	H	AB	AB minus 1	AB
H	H	L	L	Logic 1	A plus A*	A plus A plus 1
H	H	L	H	A + $\overline{B}$	(A + B) plus A	(A+B) plus A plus 1
H	H	H	L	A + B	(A + $\overline{B}$) plus A	(A+$\overline{B}$) plus A plus 1
H	H	H	H	A	A minus 1	A

Function Select				Inputs/Outputs Active Low		
				Logic Function	Arithmetic Function M = L	
S3	S2	S1	S0	M = H	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	$\overline{A}$	A minus 1	A
L	L	L	H	$\overline{AB}$	AB minus 1	AB
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1	A$\overline{B}$
L	L	H	H	Logic 1	minus 1(2's compl.)	Zero
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A+$\overline{B}$) plus 1
L	H	L	H	$\overline{B}$	AB plus (A + B)	ABplus(A+$\overline{B}$)plus1
L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	(A + $\overline{B}$) plus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	A plus (A+B) plus 1
H	L	L	H	$A \oplus B$	A plus B	A plus B plus 1
H	L	H	L	B	A$\overline{B}$ plus (A + B)	A$\overline{B}$plus(A+B)plus1
H	L	H	H	A + B	A + B	(A + B) plus 1
H	H	L	L	Logic 0	A plus A*	A plus A plus 1
H	H	L	H	A$\overline{B}$	AB plus A	AB plus A plus 1
H	H	H	L	AB	A$\overline{B}$ plus A	A$\overline{B}$ plus A plus 1
H	H	H	H	A	A	A plus 1

H = High Level   L = Low Level

* Each bit is shifted to the next more significant position.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ +0.5 V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F,H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F,H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H .... -55 to +125° C
PACKAGE TYPE E,M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

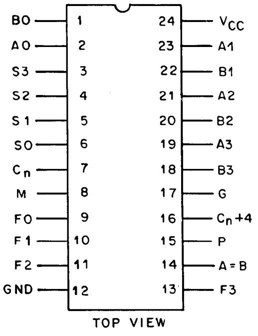
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

MAGNITUDE COMPARISON TABLE

Active - High Data			Active - Low Data		
Input C_n	Output C_{n+4}	Magnitude	Input C_n	Output C_{n+4}	Magnitude
1	1	$A \leq B$	0	0	$A \leq B$
0	1	$A < B$	1	0	$A < B$
1	0	$A > B$	0	1	$A > B$
0	0	$A \geq B$	1	1	$A \geq B$

1 = High Level
0 = Low Level



92CS-40202

TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC181/CD54HC181										CD74HCT181/CD54HCT181									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
S0-S3	1
All A and B (Data)	0.75
M, C_n	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC181
CD54/74HCT181

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
SUM Mode	Propagation Delay: t_{PLH}, t_{PHL}				ns
	A_n or B_n to C_{n+4}	15	19	22	
	A_n or B_n to G	15	18	23	
	A_n or B_n to P	15	14	17	
	A_n or B_n to F_n	15	19	24	
DIFFERENCE Mode	A_n or B_n to C_{n+4}	15	20	23	
	A_n or B_n to G	15	18	23	
	A_n or B_n to P	15	14	17	
	A_n or B_n to F_n	15	20	24	
	A_n or B_n to A = B	15	21	25	
LOGIC Mode	A_n or B_n to F_n	15	19	23	
SUM and DIFFERENCE Mode	C_n to C_{n+4}	15	13	18	
	C_n to F_n	15	17	20	
Power Dissipation Capacitance*	C_{PD}	—	120	140	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

AC Test Setup Reference (Active-Low Data)

Test Delay Times	AC Paths		DC Data Inputs		Mode*
	Inputs	Outputs	To Gnd	To V_{CC}	
SUM_{IN} to SUM_{OUT}	$\overline{B0}$	Any $\overline{F}$	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, M, C_n	All $\overline{A}$'s	ADD
SUM_{IN} to $\overline{P}$	$\overline{A0}$	$\overline{P}$	$\overline{A1}$, $\overline{A2}$, $\overline{A3}$, M, C_n	All $\overline{B}$'s	ADD
SUM_{IN} to $\overline{G}$	$\overline{B0}$	$\overline{G}$	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
SUM_{IN} to C_{n+4}	$\overline{B0}$	C_{n+4}	All $\overline{A}$'s, M, C_n	$\overline{B1}$, $\overline{B2}$, $\overline{B3}$	ADD
C_n to SUM_{OUT}	C_n	Any $\overline{F}$	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
C_n to C_{n+4}	C_n	C_{n+4}	All $\overline{A}$'s, M	All $\overline{B}$'s	ADD
SUM_{IN} to A = B	$\overline{B0}$	A = B	All A's, B1, B2, B3, M	C_n	SUBTRACT
SUM_{IN} to SUM_{OUT} (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All $\overline{A}$'s, C_n	M	EXCLUSIVE-OR

*ADD Mode: S0, S3 = V_{CC}; S1, S2 = Gnd.
SUBTRACT Mode: S0, S3 = Gnd; S1, S2 = V_{CC}.

CD54/74HC181
CD54/74HCT181

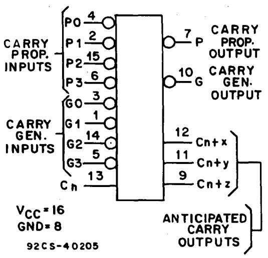
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC	V_{CC} (V)	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, t_{PLH}	2	—	225	—	—	—	280	—	—	—	345	—	—	ns
SUM Mode t_{PHL}	4.5	—	45	—	53	—	56	—	66	—	69	—	80	
A_n or B_n to C_{n+4}	6	—	38	—	—	—	48	—	—	—	59	—	—	
	2	—	210	—	—	—	265	—	—	—	315	—	—	
A_n or B_n to G	4.5	—	42	—	54	—	53	—	53	—	63	—	63	
	6	—	36	—	—	—	45	—	—	—	54	—	—	
	2	—	170	—	—	—	215	—	—	—	255	—	—	
A_n or B_n to P	4.5	—	34	—	41	—	43	—	51	—	51	—	62	
	6	—	29	—	—	—	37	—	—	—	43	—	—	
	2	—	230	—	—	—	290	—	—	—	345	—	—	
A_n or B_n to F_n	4.5	—	46	—	58	—	58	—	58	—	69	—	69	
	6	—	39	—	—	—	49	—	—	—	59	—	—	
Propagation Delay, t_{PHL}	2	—	235	—	—	—	285	—	—	—	355	—	—	
DIFFERENCE Mode t_{PLH}	4.5	—	47	—	55	—	59	—	69	—	71	—	83	
A_n or B_n to C_{n+4}	6	—	40	—	—	—	50	—	—	—	60	—	—	
	2	—	215	—	—	—	270	—	—	—	325	—	—	
A_n or B_n to G	4.5	—	43	—	54	—	54	—	54	—	65	—	65	
	6	—	37	—	—	—	46	—	—	—	55	—	—	
	2	—	170	—	—	—	215	—	—	—	255	—	—	
A_n or B_n to P	4.5	—	34	—	40	—	43	—	50	—	51	—	60	
	6	—	29	—	—	—	37	—	—	—	43	—	—	
	2	—	235	—	—	—	295	—	—	—	355	—	—	
A_n or B_n to F_n	4.5	—	47	—	57	—	59	—	71	—	71	—	86	
	6	—	40	—	—	—	50	—	—	—	60	—	—	
	2	—	245	—	—	—	305	—	—	—	370	—	—	
A_n or B_n to A=B	4.5	—	49	—	60	—	61	—	75	—	74	—	90	
	6	—	42	—	—	—	52	—	—	—	63	—	—	
Propagation Delay, t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	
LOGIC Mode t_{PLH}	4.5	—	46	—	54	—	58	—	68	—	69	—	81	
A_n or B_n to F_n	6	—	39	—	—	—	49	—	—	—	59	—	—	
Propagation Delay, t_{PHL}	2	—	165	—	—	—	205	—	—	—	250	—	—	
SUM & DIFF. Modes t_{PLH}	4.5	—	33	—	42	—	41	—	53	—	50	—	63	
C_n to C_{n+4}	6	—	28	—	—	—	35	—	—	—	43	—	—	
	2	—	200	—	—	—	250	—	—	—	300	—	—	
C_n to F_n	4.5	—	40	—	48	—	50	—	56	—	60	—	68	
	6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC182
CD54/74HCT182

File Number **1830**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Look-Ahead Carry Generator

Type Features:

- *Provides carry look-ahead across a group of four ALU s*
- *Multi-level look-ahead for high-speed arithmetic operation over long word length*

The RCA-CD54/74HC182 and CD54/74HCT182 carry look-ahead generators are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL).

The CD54/74HC/HCT182 accept up to four pairs of active LOW carry propagate ($\overline{P_0}$, $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$) and carry generate ($\overline{G_0}$, $\overline{G_1}$, $\overline{G_2}$, $\overline{G_3}$) signals and an active HIGH carry input(C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The HC/HCT182 also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look ahead.

The logic equations provided at the outputs are:

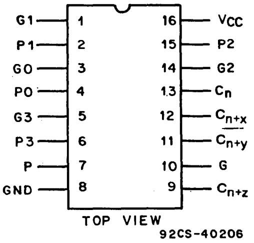
$$C_{n+x} = P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The CD54/74HC/HCT182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

The CD54HC182 and CD54HCT182 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC182 and CD74HCT182 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  - *Standard outputs - 10 LSTTL loads*
  - *Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL input logic compatibility*
    - *V_{IL} = 0.8 V max., V_{IH} = 2 V Min.*
  - *CMOS input compatiblity*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



TERMINAL ASSIGNMENT

CD54/74HC182
CD54/74HCT182

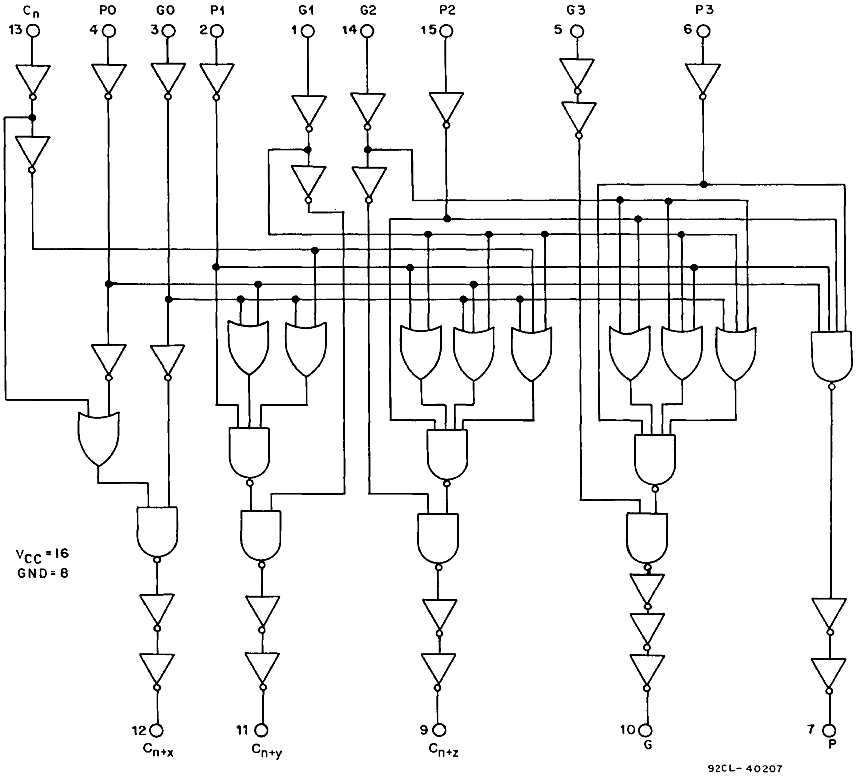


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Lineary at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC182
CD54/74HCT182

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH voltage level L = LOW voltage level X = don't care

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC182/CD54HC182										CD74HCT182/CD54HCT182									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
P_0, P_1, P_2, G_0, G_1	1.5
P_3, G_2, C_n	1.25
G_3	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC182
CD54/74HCT182

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

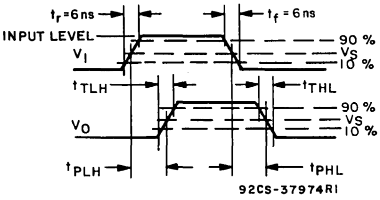
CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Time:					
P_n to P	t_{PHL}, t_{PLH}	15	9	11	ns
C_n to any output	t_{PHL}, t_{PLH}	15	12	17	
P_n to any output	t_{PHL}, t_{PLH}	15	12	13	
G_n to any output	t_{PHL}, t_{PLH}	15	11	13	
Power Dissipation Capacitance *	C_{PD}	—	66	72	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	ns
	t_{PHL}	4.5	—	24	—	28	—	30	—	35	—	36	—	42	
P_n to P		6	—	20	—	—	—	26	—	—	—	31	—	—	
	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	30	—	40	—	38	—	50	—	45	—	60	
C_n to any output		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
	t_{PHL}	4.5	—	29	—	33	—	36	—	41	—	36	—	50	
P_n to any output		6	—	25	—	—	—	31	—	—	—	31	—	—	
	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
	t_{PHL}	4.5	—	27	—	32	—	34	—	40	—	41	—	48	
G_n to any output		6	—	23	—	—	—	29	—	—	—	35	—	—	
Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



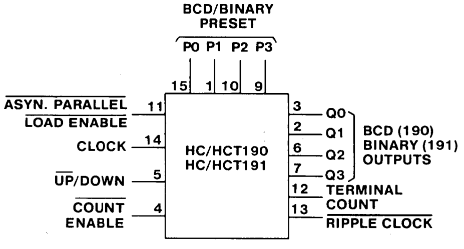
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

File Number **1662**

High-Speed CMOS Logic



92CS-38520R2

FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Up/Down Counters

CD54/74HC/HCT190 BCD Decade Counter
CD54/74HC/HCT191 Binary Counter

Type Features:

- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look-ahead carry for high-speed counting*

The RCA-CD54/74HC/HCT190/191 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a Low asynchronous parallel load input ($\overline{\text{PL}}$). Counting occurs when $\overline{\text{PL}}$ is high, Count Enable ($\overline{\text{CE}}$) is low, and the Up/Down ($\overline{\text{U}}$/D) input is either low for up-counting or high for down-counting. The counter is incremented or decremented synchronously with the low-to-high transition of the clock.

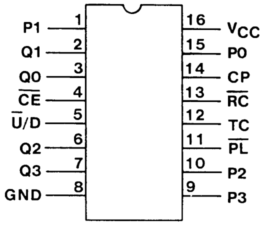
When an overflow or underflow of the counter occurs the Terminal Count output (TC), which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Fig. 6). The TC output also initiates the Ripple Clock. ($\overline{\text{RC}}$) output which, normally high, goes low and remains low for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Clock output as shown in Fig. 7.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one or two counts as shown in state diagrams.

The CD54HC/HCT190 and the CD54HC/HCT191 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT190 and the CD74HC/HCT191 are supplied in a 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT190 and the CD54/74HC/HCT191 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ V *Max.*, $V_{IH} = 2$ V *Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-38521

HC/HCT190, HC/HCT191
TERMINAL ASSIGNMENT

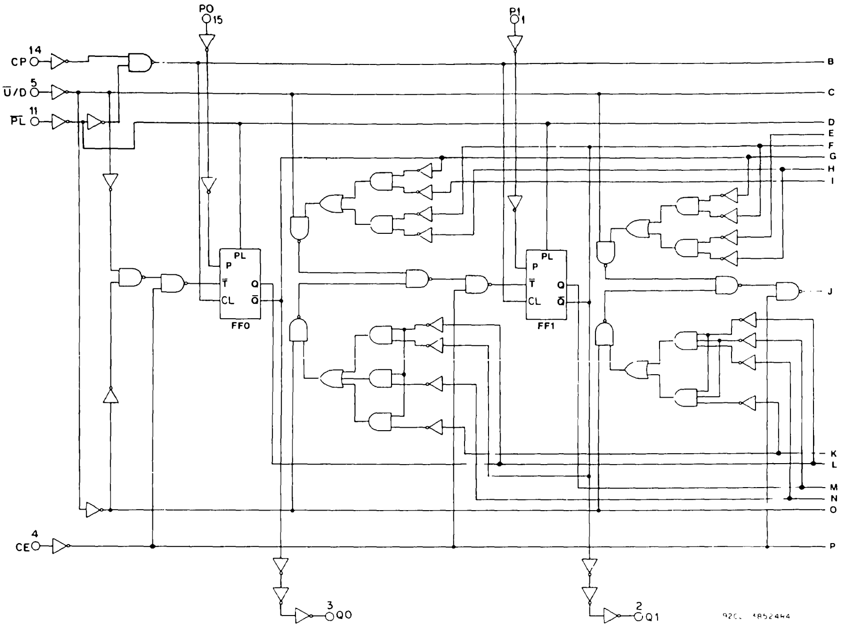


Fig. 1 - Logic diagram for HC/HCT190 (continued on next page).

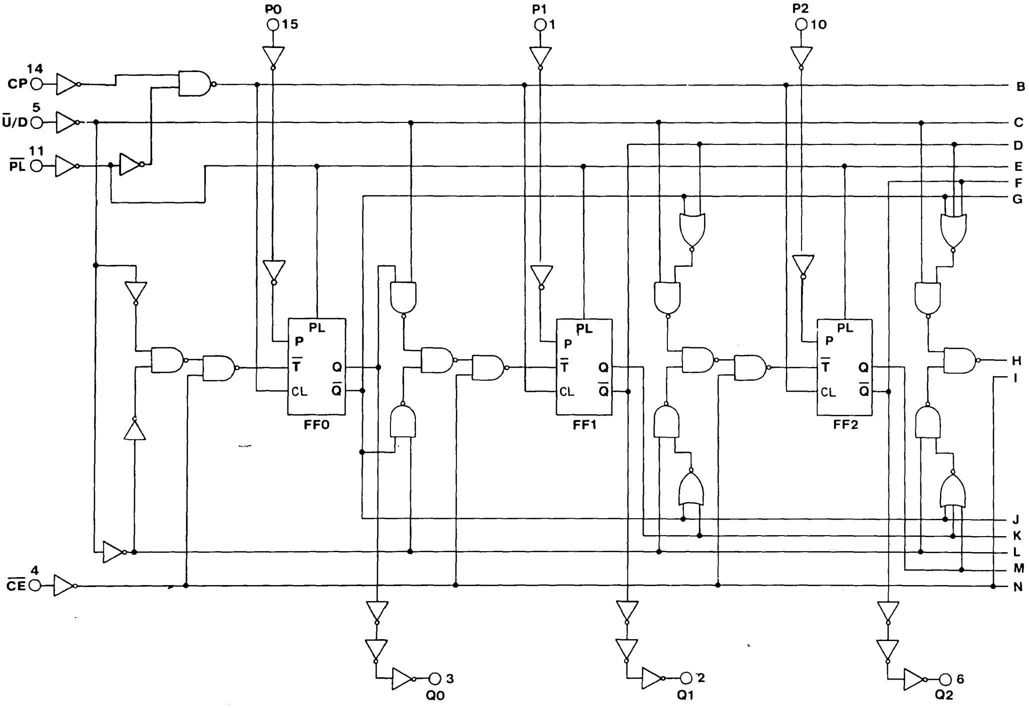


Fig. 2 - Logic diagram for HC/HCT191 (continued on next page).

92CL-38523R3

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

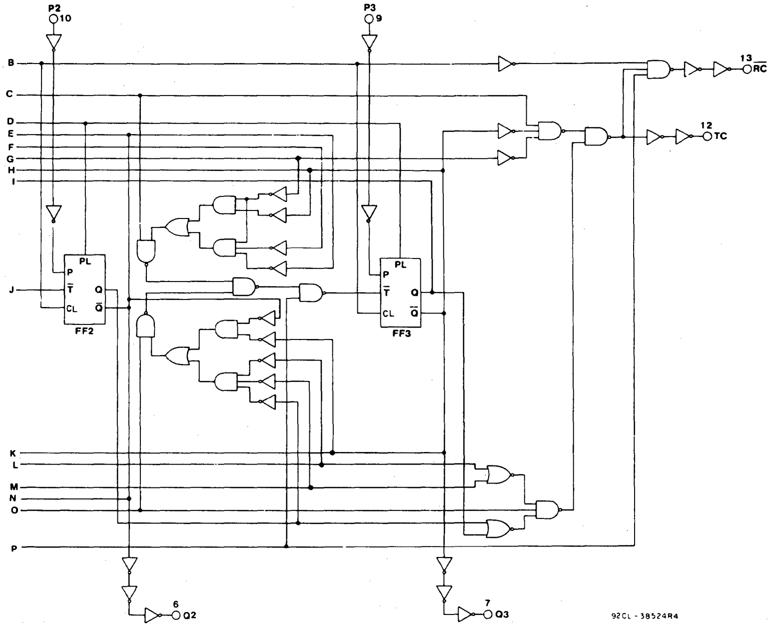


Fig. 1 - Logic diagram for HC/HCT190 (continued from previous page).

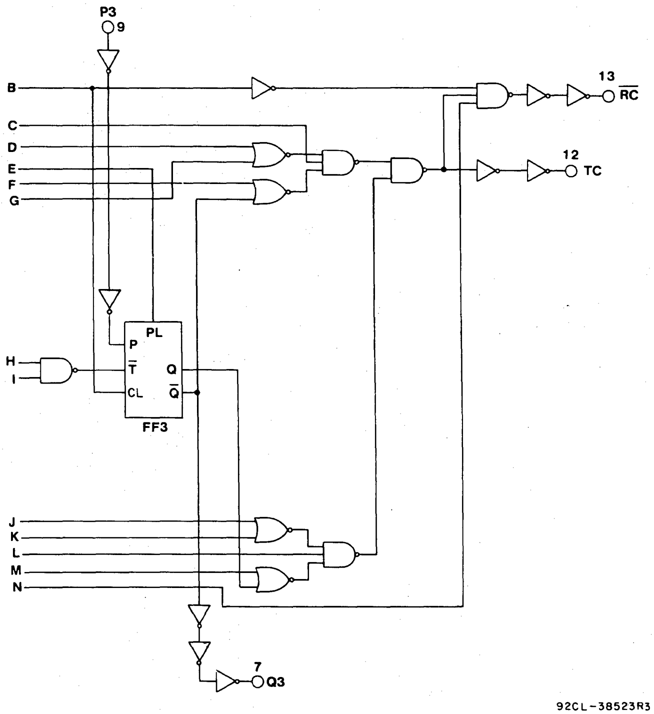


Fig. 2 - Logic diagram for HC/HCT191 (continued from previous page).

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

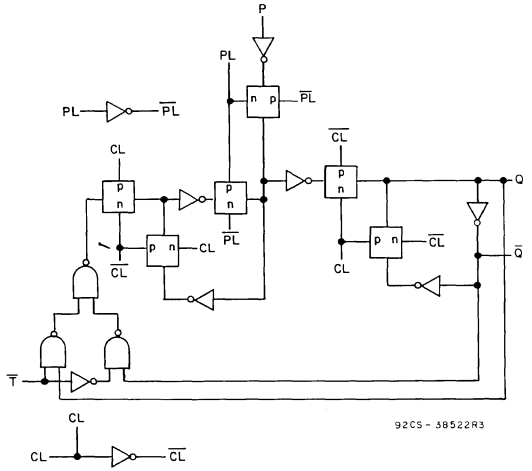


Fig. 3 - Flip-flop cell for HC/HCT190 and HC/HCT191.

TRUTH TABLE

Inputs				Function
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

Note:
$\overline{U}/D$ or $\overline{CE}$ should be changed only when clock is high.
X = Don't care.
↑ Low-to-high clock transition.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC190/CD54HC190 CD74HC191/CD54HC191										CD74HCT190/CD54HCT190 CD74HCT191/CD54HCT191									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.4
$\overline{CP}$	1.5
$\overline{PL}$	1.5
$\overline{U}/D$	1.2
$\overline{CE}$	1.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Setup Time Pn to $\overline{PL}$	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
$\overline{CE}$ to CP		2	60	—	—	—	75	—	—	—	90	—	—	—	
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
$\overline{U}$/D to CP		2	90	—	—	—	115	—	—	—	135	—	—	—	
		4.5	18	—	18	—	23	—	23	—	27	—	27	—	
		6	15	—	—	—	20	—	—	—	23	—	—	—	
Hold Time Pn to $\overline{PL}$	t_H	2	2	—	—	—	2	—	—	—	2	—	—	—	
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	
$\overline{CE}$ to CP		2	2	—	—	—	2	—	—	—	2	—	—	—	
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	
$\overline{U}$/D to CP		2	0	—	—	—	0	—	—	—	0	—	—	—	
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Maximum Frequency*	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Recovery Time	t_{REC}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
CP Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{PL}$ Pulse Width	t_W	2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	

*Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable ($\overline{CE}$)-to-clock set-up times, and count enable ($\overline{CE}$)-to-clock hold times determine max. clock frequency. For example, with these HC devices:

$$f_{max}\,(CP) = \frac{1}{\text{CP-to-TC prop. delay} + \overline{\text{CE}}\text{-to-CP setup} + \overline{\text{CE}}\text{-to-CP Hold}} = \frac{1}{42 + 12 + 2} \approx 18\ \text{MHz}$$

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

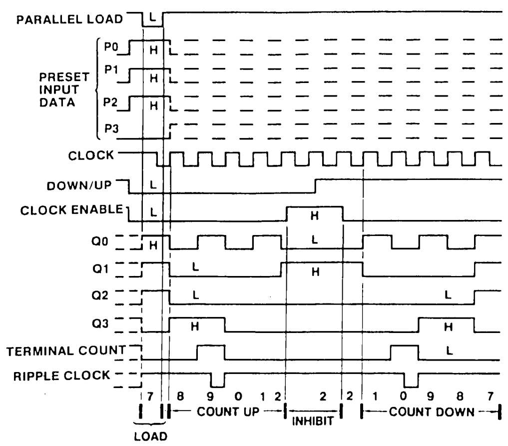
CHARACTERISTIC	SYMBOL	TYPICAL VALUES				UNITS
		HC		HCT		
		190	191	190	191	
Propagation Delay (C_L = 15 pF)						
$\overline{PL}$ to Qn	t_{PLH} t_{PHL}	16	16	17	17	ns
Pn to Qn		14	14	16	16	
CP to Qn		14	14	14	14	
CP to $\overline{RC}$		10	10	11	11	
CP to TC		18	18	18	18	
$\overline{U}$/D to $\overline{RC}$		12	12	12	12	
$\overline{U}$/D to TC		13	13	16	16	
$\overline{CE}$ to $\overline{RC}$		10	10	11	11	
Power Dissipation Capacitance	C_{PD}*	59	55	78	68	pF

*C_{PD} is used to determine the power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i=input frequency f_o=output frequency C_L=output load capacitance V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

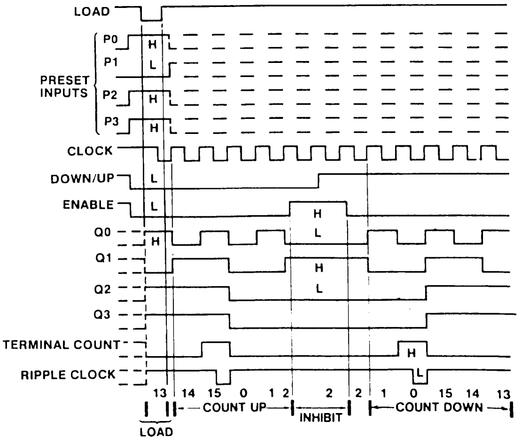
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	ns
$\overline{PL}$ to Qn	t_{PHL}	4.5	—	39	—	40	—	49	—	50	—	59	—	60	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
Pn to Qn	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
	t_{PLH}	2	—	170	—	—	—	215	—	—	—	255	—	—	
CP to Qn	t_{PHL}	4.5	—	34	—	35	—	43	—	44	—	51	—	53	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
CP to $\overline{RC}$	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
	t_{PLH}	2	—	210	—	—	—	265	—	—	—	315	—	—	
CP to TC	t_{PHL}	4.5	—	42	—	42	—	53	—	53	—	63	—	63	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{U}$/D to $\overline{RC}$	t_{PHL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
$\overline{U}$/D to TC	t_{PHL}	4.5	—	33	—	38	—	41	—	48	—	50	—	57	
		6	—	28	—	—	—	35	—	—	—	43	—	—	
	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
$\overline{CE}$ to $\overline{RC}$	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
Qn, TC, $\overline{RC}$		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

TIMING DIAGRAMS



Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

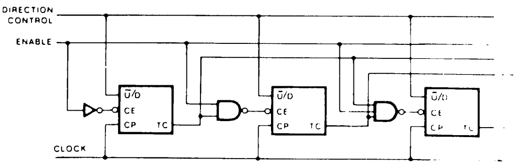
Fig. 4 - HC/HCT190 decade counters typical load, count, and inhibit sequences.



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

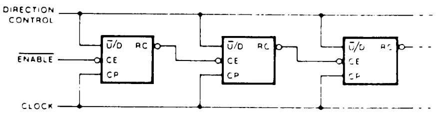
92CM-38402

Fig. 5 - HC/HCT191 binary counters typical load, count, and inhibit sequences.



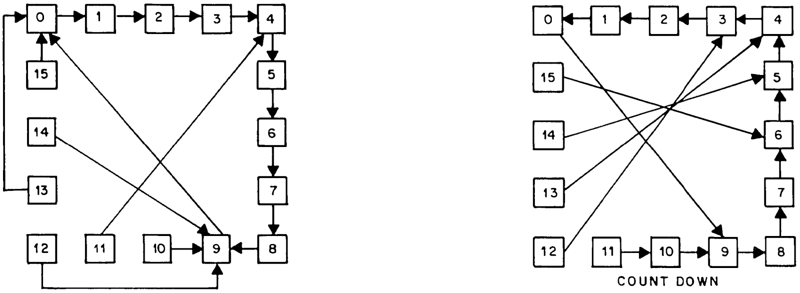
92CS-38400

Fig. 6 - Sychronous n-stage counter with parallel gated Terminal Count.



92CS-38401

Fig. 7 - Synchronous n-stage counter using ripple clock.



COUNT UP

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE COUNT.

COUNT DOWN

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE OR TWO COUNTS.

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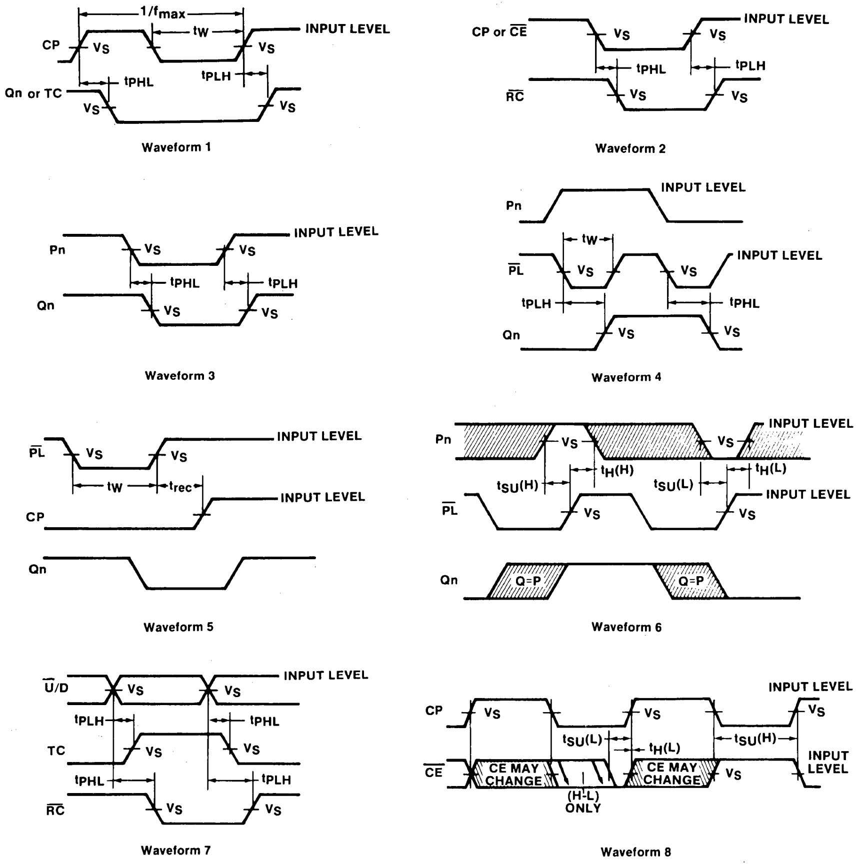
Fig. 8 - HC/HCT190 State Diagrams.

CD54/74HC190, CD54/74HCT190
CD54/74HC191, CD54/74HCT191



Waveform 1

Waveform 2

Waveform 3

Waveform 4

Waveform 5

Waveform 6

Waveform 7

Waveform 8

The shaded areas indicate when the input is permitted to change for predictable output performance

92CL-38403R3

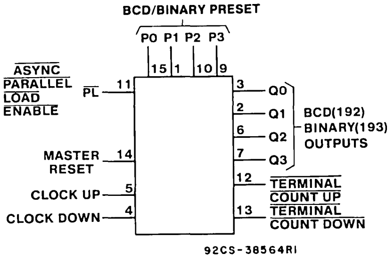
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 9 - Transition, propagation delay, setup and hold, and recovery times.

File Number **1674**

CD54/74HC192, CD54/74HCT192 CD54/74HC193, CD54/74HCT193

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Up/Down Counters

CD54/74HC/HCT192 BCD Decade Counter, Asynchronous Reset
CD54/74HC/HCT193 4-Bit Binary Counter, Asynchronous Reset

Type Features:

- *Synchronous counting and asynchronous loading*
- *Two outputs for n-bit cascading*
- *Look-ahead carry for high-speed counting*

The RCA-CD54/74HC/HCT192/193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

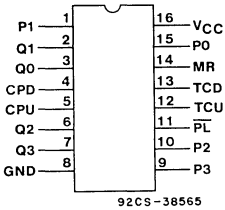
Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (PL). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low-to-high transition of the Clock-Down input (and a high level on the Clock-Up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count Up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The CD54HC/HCT192 and the CD54HC/HCT193 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT192 and CD74HC/HCT193 are supplied in 16-lead plastic dual-in-line packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT192 and the CD54/74HC/HCT193 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

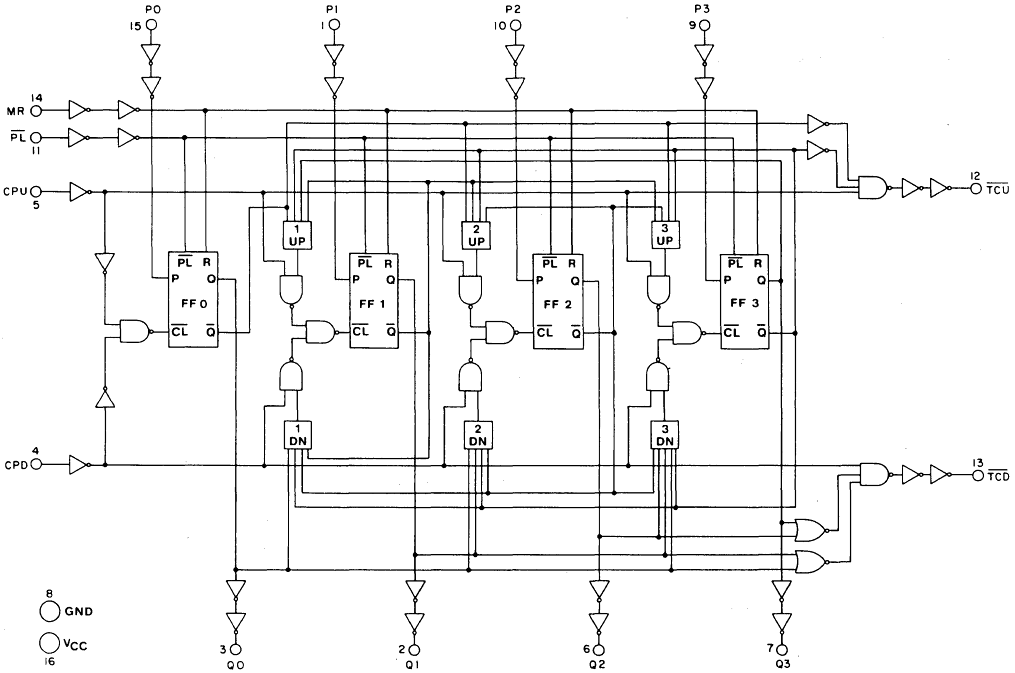
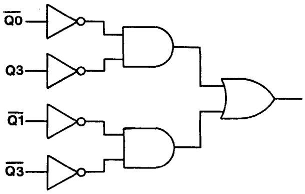
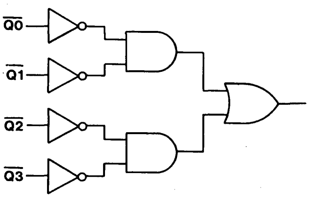


Fig. 1 - Logic diagram for HC/HCT192.

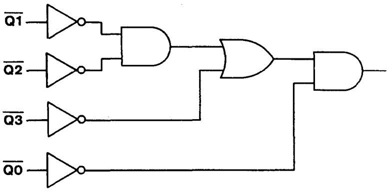
92CL - 38566R1



(a) Cell 1Up

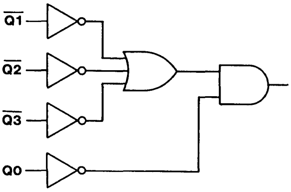


(b) Cell 2UP

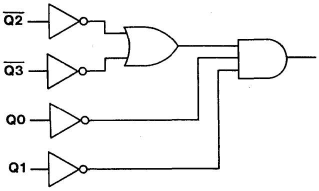


(c) Cell 3UP

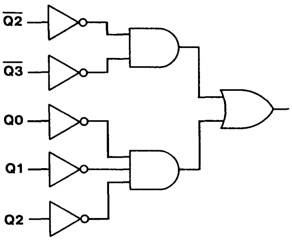
92CS-38570



(d) Cell 1Dn



(e) Cell 2Dn



92CM-38569

Fig. 2 - CARRY logic cells for CD54/74HC/HCT192

(f) Cell 3Dr

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

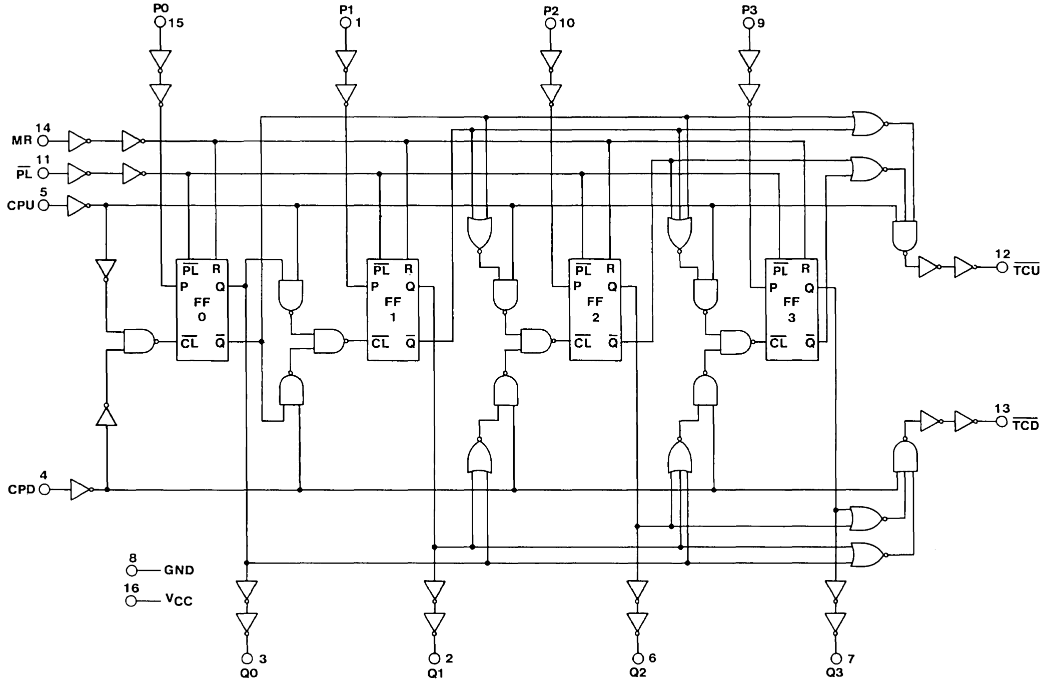


Fig. 3 - Logic diagram for HC/HCT193.

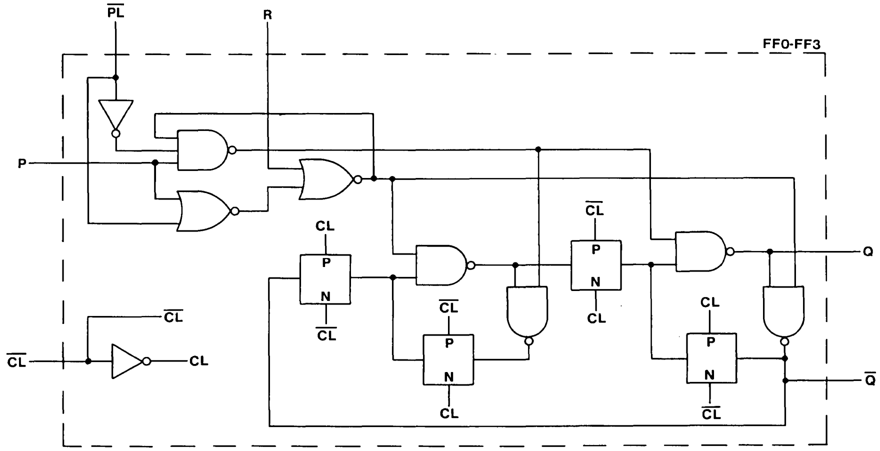


Fig. 4 - Logic diagram of flip-flops for HC/HCT192/193.

TRUTH TABLE

Clock Up	Clock Down	Reset	Parallel Load	Function
_/‾	H	L	H	Count Up
H	_/‾	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

_/‾ = low-to-high transition
x = don't care

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC192/193CD54HC192/193										CD74HCT192/193/CD54HCT192/193									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.4
$\overline{MR}$	1.45
$\overline{PL}$	0.85
CPU, CPD	1.45

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay (C_L = 15 pF)				
CPU to $\overline{TCU}$ and CPD to $\overline{TCD}$	t_{PLH} t_{PHL}	10	11	ns
CPU; CPD to Qn		18	17	
$\overline{PL}$ to Qn		18	21	
MR to Qn	t_{PHL}	17	18	
Power Dissipation Capacitance	C_{PD}*	40	50	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$PD=C_{PD} V_{CC}^2 fi + \Sigma (C_L V_{CC}^2 fo)$ where:
f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

Pre-requisite for Switching Function

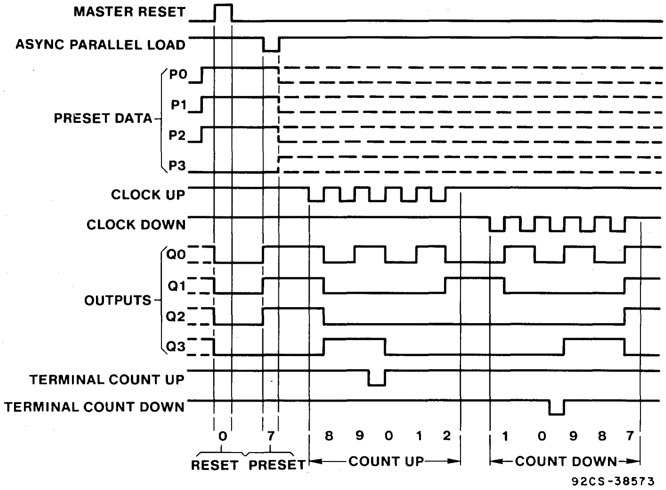
CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width: CPU, CPD 192	t_W	2	115	—	—	—	145	—	—	—	175	—	—	—	ns
		4.5	23	—	23	—	29	—	29	—	35	—	35	—	
		6	20	—	—	—	25	—	—	—	30	—	—	—	
CPU, CPD 193		2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	23	—	25	—	29	—	30	—	35	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
$\overline{PL}$	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR	t_W	2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time Pn to $\overline{PL}$	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	15	—	20	—	19	—	24	—	22	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time Pn to $\overline{PL}$	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Hold Time CPD to CPU or CPU to CPD	t_H	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Recovery Time $\overline{PL}$ to CPU, CPD	t_{REC}	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	15	—	20	—	19	—	24	—	22	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR to CPU, CPD	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Maximum Frequency CPU, CPD 192	f_{MAX}	2	5	—	—	—	4	—	—	—	3	—	—	—	MHz
		4.5	22	—	22	—	18	—	18	—	15	—	15	—	
		6	24	—	—	—	21	—	—	—	18	—	—	—	
CPU, CPD 193		2	5	—	—	—	4	—	—	—	3	—	—	—	
		4.5	25	—	22	—	20	—	18	—	17	—	15	—	
		6	29	—	—	—	24	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	ns
CPU to $\overline{TCU}$	t_{PHL}	4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
		2	—	125	—	—	—	155	—	—	—	190	—	—	
CPD to $\overline{TCD}$		4.5	—	25	—	27	—	31	—	34	—	38	—	41	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
		2	—	220	—	—	—	270	—	—	—	325	—	—	
CPU to Qn		4.5	—	43	—	40	—	54	—	50	—	65	—	60	
		6	—	37	—	—	—	46	—	—	—	55	—	—	
		2	—	220	—	—	—	270	—	—	—	325	—	—	
CPD to Qn		4.5	—	43	—	40	—	54	—	50	—	65	—	60	
		6	—	37	—	—	—	46	—	—	—	55	—	—	
		2	—	220	—	—	—	275	—	—	—	330	—	—	
$\overline{PL}$ to Qn		4.5	—	44	—	47	—	55	—	59	—	66	—	71	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
		2	—	200	—	—	—	250	—	—	—	300	—	—	
MR to Qn		4.5	—	40	—	43	—	50	—	54	—	60	—	65	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Time:	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Q, TCU, TCD	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193

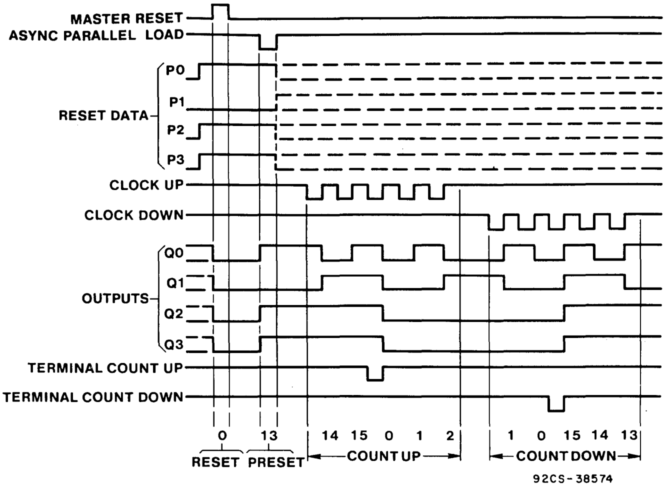
Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, nine, eight and seven.



(a) *HC192 synchronous decade counters. Typical reset, preset and count sequences.*

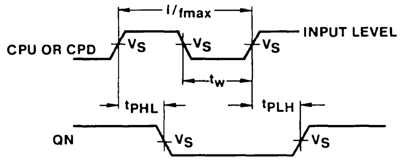
Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Note 1: Master reset overrides load data and clock inputs
Note 2: When counting up, clock-down input must be high; when counting down, clock-up input must be high.

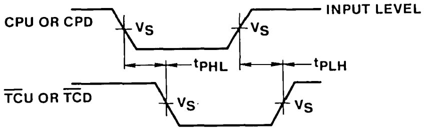


(b) *HC193 synchronous binary counters. Typical reset, preset and count sequences.*

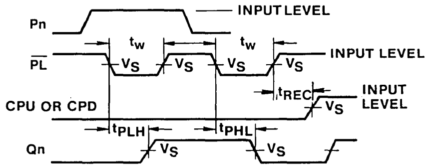
Fig. 6 - Timing diagrams for the CD54/74HC/HCT192(a) and 193(b).



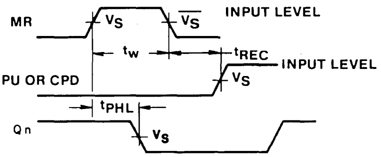
(a) *Clock to output delays and clock pulse width.*



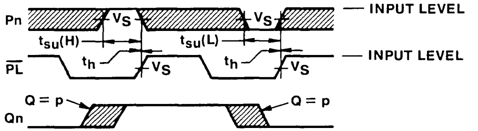
(b) *Clock to terminal count delays.*



(c) *Parallel load pulse width, parallel load to output delays, and parallel load to clock recovery time.*



(d) *Master reset pulse width, master reset to output delay and master reset to clock recovery time.*

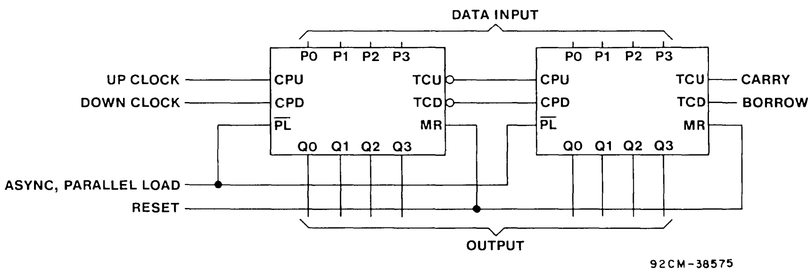


(e) *Setup and hold times data to parallel load (PL).*

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

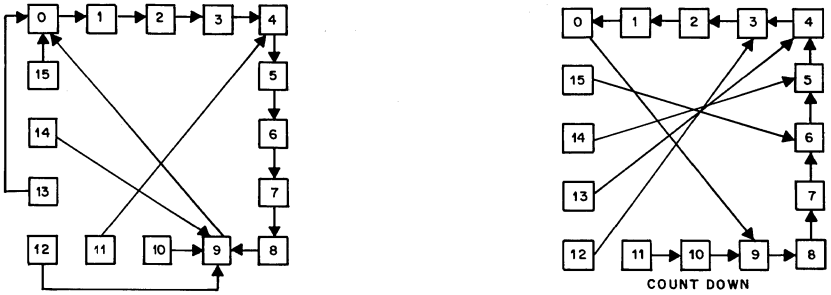
Fig. 5 - AC waveforms.

APPLICATION



CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD

CD54/74HC192, CD54/74HCT192
CD54/74HC193, CD54/74HCT193



COUNT UP

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE COUNT.

COUNT DOWN

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE OR TWO COUNTS.

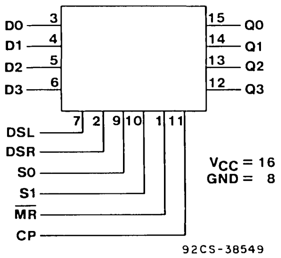
92CM-40338

Fig. 6 - HC/HCT192 State Diagrams.

File Number **1668**

CD54/74HC194
CD54/74HCT194

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Bidirectional Universal Shift Register

Type Features:

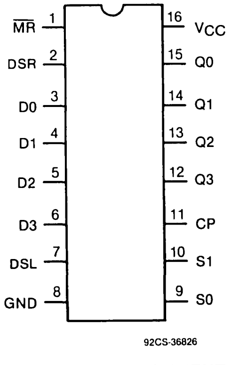
- *Four Operating Modes: Shift Right, Shift Left, Hold and Reset*
- *Synchronous parallel or serial operation*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*
- *Asynchronous Master Reset*

The RCA-CD54/74HC194 and CD54/74HCT194 are 4-bit shift registers with Asynchronous Master Reset ($\overline{MR}$). In the parallel mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift right mode, and at the shift right (DSR) serial input for the shift left mode. Clearing the register is accomplished by a Low applied to the Master Reset ($\overline{MR}$) pin.

The CD54HC/HCT194 devices are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT194 devices are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V *Max.*, $V_{IH} = 2$ V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC194
CD54/74HCT194

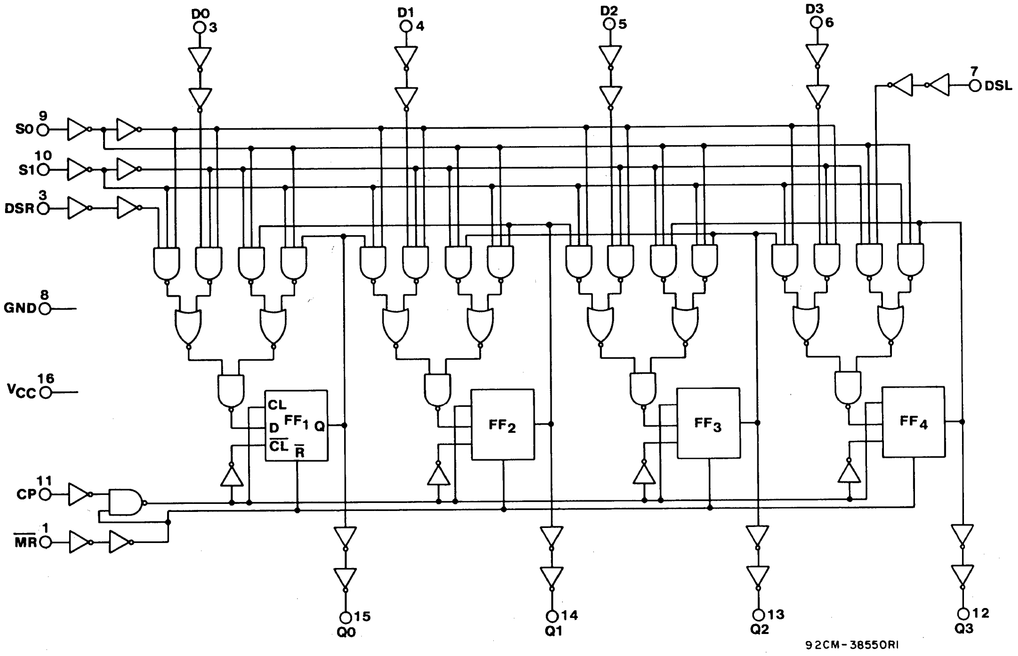


Fig. 1 - Logic diagram for the CD54/74HC194 and CD54/74HCT194.

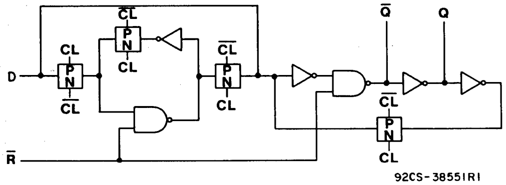


Fig. 2 - Detail of single Flip-Flop for the CD54/74HC194 and CD54/74HCT194.

TRUTH TABLE

Operating Mode	Inputs							Outputs			
	CP	$\overline{MR}$	S_1	S_0	DSR	DSL	D_n	Q0	Q1	Q2	Q3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l(b)	l(b)	X	X	X	q0	q1	q2	q3
Shift Left	_/‾	H	h	l(b)	X	l	X	q1	q2	q3	L
	_/‾	H	h	l(b)	X	h	X	q1	q2	q3	H
Shift Right	_/‾	H	l(b)	h	l	X	X	L	q0	q1	q2
	_/‾	H	l(b)	h	h	X	X	H	q0	q1	q2
Parallel Load	_/‾	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
_/‾ = LOW-to-HIGH clock transition.

NOTE: b. The HIGH-to-LOW transition of the S_0, and S_1 inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

CD54/74HC194
CD54/74HCT194

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ OR $V_O > V_{CC}$ +0.5 V) .... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) .... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): .... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC194
CD54/74HCT194

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/54HC194										CD74HCT/54HCT194									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	Io mA	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_I V	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	Vcc or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between Vcc & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current Icc	Vcc or Gnd	0	6	—	—	8	—	80	—	160	Vcc or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional quiescent Device Current ΔI_{CC}* per input pin: 1 unit load											Vcc-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
CP	0.6
$\overline{MR}$	0.55
DSL, DSR, Dn	0.25
Sn	1.10

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL		UNIT
			HC	HCT	
Propagation Delay, Clock to Q	t_{PLH} t_{PHL}	15	14	15	ns
Maximum Clock Frequency	f_{MAX}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	55	60	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 fi + \Sigma (C_L V_{CC}^2 fo)$ where:
fi = input frequency.
fo = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

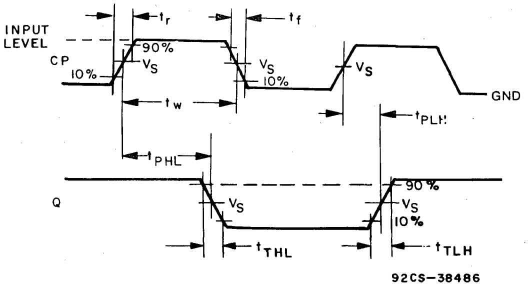
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to + 85°C				-55°C to + 125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Max. Clock Frequency	f_{MAX}	2	6		—		5		—		4		–		
Fig. 3		4.5	30		27		24		22		20		18		MHz
		6	35		—		28		—		23		—		
$\overline{MR}$ Pulse Width	t_W	2	80		—		100		—		120		—		
Fig. 4		4.5	16		18		20		23		24		27		ns
		6	14		—		17		—		20		—		
Clock Pulse Width	t_W	2	80		—		100		—		120		—		
Fig. 3		4.5	16		18		20		23		24		27		ns
		6	14		—		17		—		20		—		
Set-up time	t_{SU}	2	70		—		90		—		105		—		
Data to Clock		4.5	14		14		18		18		21		21		ns
Fig. 5		6	12		—		15		—		19		—		
Removal Time	t_{REM}	2	60		—		75		—		90		—		
$\overline{MR}$ to Clock		4.5	12		14		15		18		18		21		ns
Fig. 4		6	10		—		13		—		15		—		
Set-up Time	t_{SU}	2	80		—		100		—		120		—		
S1, S0 to Clock		4.5	16		20		20		25		24		30		ns
Fig. 6		6	14		—		17		—		20		—		
Set-up Time	t_{SU}	2	70		—		90		—		105		—		
DSL, DSR to Clock		4.5	14		14		18		18		21		21		ns
Fig. 6		6	12		—		15		—		18		—		
Hold Time	t_H	2	0		—		0		—		0		—		
S1, S0 to Clock		4.5	0		0		0		0		0		0		ns
Fig. 6		6	0		—		0		—		0		—		
Hold Time	t_H	2	0		—		0		—		0		—		
Data to Clock		4.5	0		0		0		0		0		0		ns
Fig. 5		6	0		—		0		—		0		—		

CD54/74HC194
CD54/74HCT194

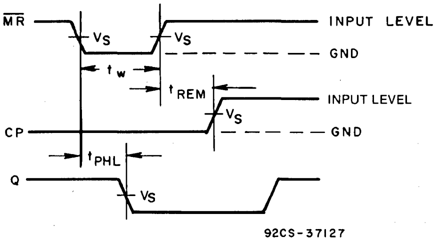
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to + 85° C				-55° C to + 125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2		175		—		220		—		265		—	
Clock to Output	t_{PHL}	4.5		35		37		44		46		53		56	ns
Fig. 3		6		30		—		37		—		45		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
Fig. 3		6		13		—		16		—		19		—	
Propagation Delay	t_{PHL}	2		140		—		175		—		210		—	
$\overline{MR}$ to Output		4.5		28		40		35		50		42		60	ns
Fig. 4		6		24		—		30		—		36		—	
Input Capacitance	C_I	—		10		10		10		10		10		10	pF



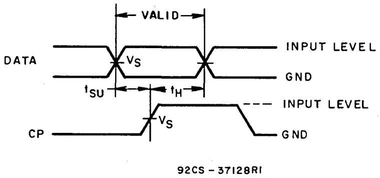
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 3 - Clock pre-requisite times and propagation and output transition times.



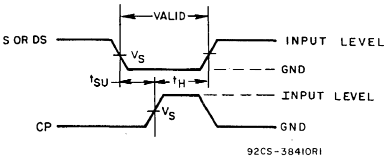
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 4 - Master reset pre-requisite times and propagation delays.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 5 - Data pre-requisite times.



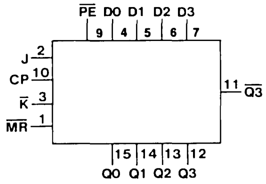
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 6 Parallel load or shift-left/shift-right pre-requisite times.

File Number **1482**

CD54/74HC195
CD54/74HCT195

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Parallel Access Register

Type Features:

- *Asynchronous Master Reset*
- *J, $\overline{K}$, (D) inputs to first stage*
- *Fully synchronous serial or parallel data transfer*
- *Shift right and parallel load capability*
- *Complementary output from last stage*
- *Buffered inputs*
- *Typical f_{MAX}=50 MHz @ V_{CC}=5 V, C_L=15 pF, T_A=25°C*

The functional characteristics of the RCA-CD54/74HC195 and CD54/74HCT195 4-Bit Parallel Access Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

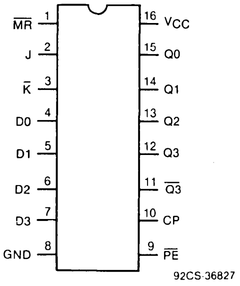
The two modes of operation, shift right (Q0-Q1) and parallel load, are controlled by the state of the Parallel Enable ($\overline{\text{PE}}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{\text{K}}$ inputs when the $\overline{\text{PE}}$ input is high, and is shifted one bit in the direction Q0-Q1-Q2-Q3 following each LOW-to-HIGH clock transition. The J and $\overline{\text{K}}$ inputs provide the flexibility of the JK-type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as four common-clocked D flip-flops when the $\overline{\text{PE}}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D0-D3) is transferred to the respective Q0-Q3 outputs. Shift left operation (Q3-Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the $\overline{\text{PE}}$ input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The HC/HCT195 series utilizes edge-triggering; therefore, there is no restriction on the activity of the J, $\overline{\text{K}}$, Pn and $\overline{\text{PE}}$ inputs for logic operations, other than the set-up and hold time requirements. A LOW on the asynchronous Master Reset ($\overline{\text{MR}}$) input sets all Q outputs LOW, independent of any other input condition.

The CD54HC195 and CD54HCT195 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC195 and CD74HCT195 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: −40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



TERMINAL ASSIGNMENT

CD54/74HC195
CD54/74HCT195

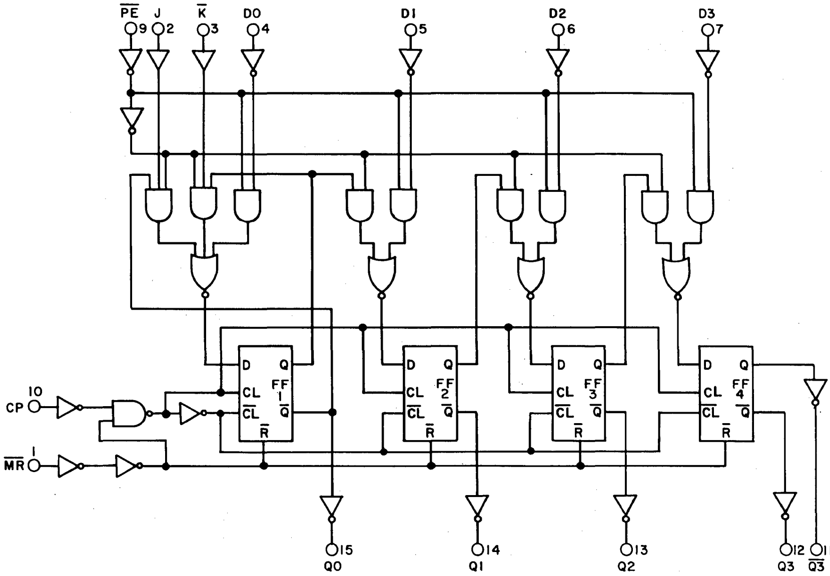


Fig. 1 - Logic diagram.

Function Table

Operating Modes	INPUTS						OUTPUTS				
	$\overline{MR}$	$\overline{CP}$	PE	J	$\overline{K}$	D_n	Q0	Q1	Q2	Q3	$\overline{Q3}$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set first stage	H	_/‾	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset first stage	H	_/‾	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle first stage	H	_/‾	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain first stage	H	_/‾	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	_/‾	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H=HIGH voltage level.
L=LOW voltage level.
X=Don't care.
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
d_n (q_n)=Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
_/‾=LOW-to-HIGH clock transition.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

CD54/74HC195
CD54/74HCT195

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC195/CD54HC195										CD74HCT195/CD54HCT195									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25° C			-40/ +85° C		-55/ +125° C				+25° C			-40/ +85° C		-55/ +125° C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D0-D3	0.3
$\overline{PE}$	-0.65
$\overline{MR}$	0.3
CP	0.3
J, $\overline{K}$	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25° C.

CD54/74HC195
CD54/74HCT195

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range)			
V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical		Units
			HC	HCT	
CP to Qn Propagation Delay	t_{PHL} t_{PLH}	15	14	14	ns
$\overline{MR}$ to Qn	t_{PHL}	15	13	14	ns
Maximum Clock Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	45	50	pF

*C_{PD} is used to determine the dynamic power consumption, per register.
PD = C_{PD} Vcc^2 fi + Σ C_L Vcc^2 fo where
fi = input frequency
fo = output frequency
C_L = output load capacitance
Vcc = supply voltage.

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency (Figure 3)	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	ns
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
$\overline{MR}$ Pulse Width (Figure 3)	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Clock Pulse Width (Figure 3)	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time J, $\overline{K}$, $\overline{PE}$ to Clock (Figure 5)	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time J, $\overline{K}$, $\overline{PE}$ to Clock (Figure 5)	t_h	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time $\overline{MR}$ to Clock (Figure 3)	t_{REM}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay CP to Output (Figure 3)	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay $\overline{MR}$ to Output (Figure 3)	t_{PHL} t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

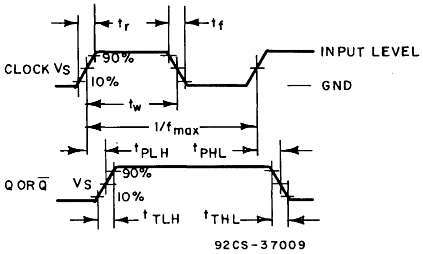


Fig. 3 - Clock pre-requisite and propagation delays and output transition times.

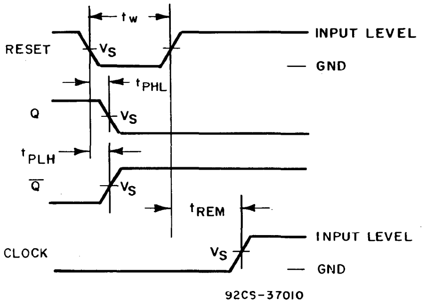


Fig. 4 - Master Reset pre-requisite and propagation delays.

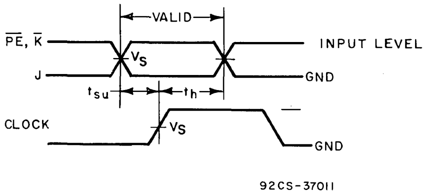


Fig. 5 - J, $\overline{K}$ or Parallel Enable pre-requisite times.

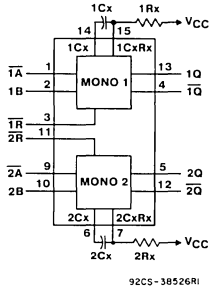
	HC	HCT
INPUT LEVEL	V_{CC}	3V
V_S	50%	1.3V

File Number **1670**

**Advance Information/
Preliminary Data**

CD54/74HC221
CD54/74HCT221

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Monostable Multivibrator with Reset

Type Features:

- *Overriding RESET Terminates Output Pulse*
- *Triggering From the Leading or Trailing Edge*
- *Q and $\overline{Q}$ Buffered Outputs*
- *Separate Resets*
- *Wide Range of Output-Pulse Widths*
- *Schmitt Trigger on B inputs*

The RCA-CD54/74HC221 and CD54/74HCT221 are dual monostable multivibrators with reset. An external resistor (R_x) and an external capacitor (C_x) control the timing and the accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. Pulse triggering on the B input occurs at a particular voltage level and is not related to the rise and fall time of the trigger pulse.

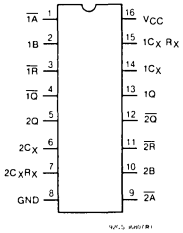
Once triggered, the outputs are independent of further trigger inputs on $\overline{A}$ and B. The output pulse can be terminated by a LOW level on the Reset ($\overline{R}$) pin. Trailing-edge triggering ($\overline{A}$) and leading-edge-triggering (B) inputs are provided for triggering from either edge of the input pulse. On power up, the IC is reset. If either Mono is not used each input (on the unused device) must be terminated either high or low.

The minimum value of external resistance, R_x, is typically 500Ω. The minimum value of external capacitance, C_x, is 0 pF. The calculation for the pulse width is $t_w = 0.7\ R_xC_x$ at $V_{CC} = 4.5$ V.

The CD54HC/HCT221 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT221 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC221
CD54/74HCT221

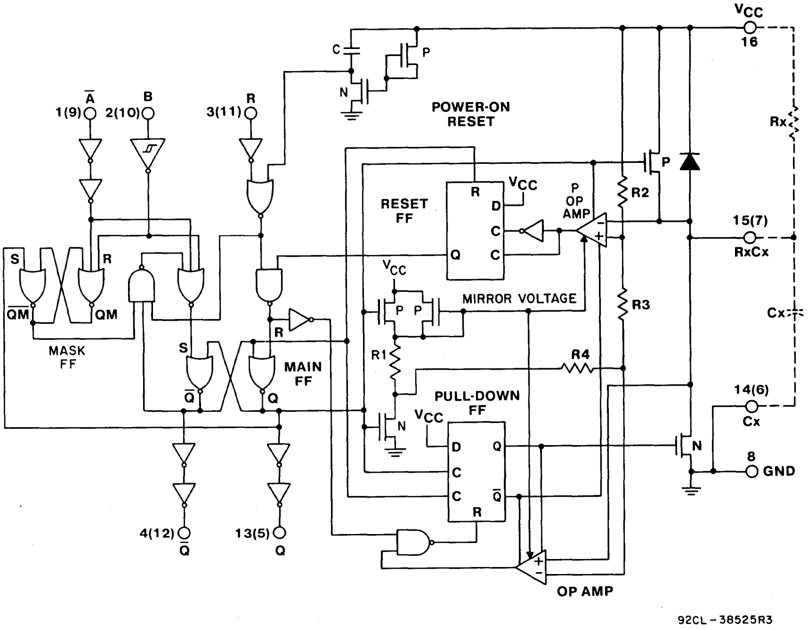


Fig. 1 — Logic diagram

TRUTH TABLE				
INPUTS			OUTPUTS	
A̅	B	R̅	Q	Q̅
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⊔
↓	H	H	⎍	⊔
X	X	L	L	H
L	H	↑	⎍*	⊔*

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

*For this combination the reset input must be low and the following sequence must be used: pin 1 (or 9) must be set high or pin 2 (or 10) set low; then pin 1 (or 9) must be low and pin 2 (or 10) set high. Now the reset input goes from low-to-high and the device will be triggered.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC221/CD54HC221										CD74HCT221/CD54HCT221									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All Inputs	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC221
CD54/74HCT221

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5V$) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5V$) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5 V < V_o < V_{CC} + 0.5V$) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f on Inputs $\overline{A}$ and $\overline{R}$			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns
Input Rise and Fall Times t_r, t_f on Input B			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay					
$\overline{A}$, B, $\overline{R}$ to Q	t_{PLH}	15	18	18	ns
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	15	14	14	ns
Power Dissipation Capacitance*	C_{PD}	—	166	166	pF

*C_{PD} is used to determine the dynamic power consumption, per multivibrator.
$P_D = (C_{PD}+C_x) V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency. f_o = output frequency. C_L = output load capacitance. V_{CC} = supply voltage. assuming $f_i \ll \frac{1}{t_w}$

CD54/74HC221
CD54/74HCT221

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Pulse Width	2	70	—	—	—	90	—	—	—	105	—	—	—	
t_{WL}	4.5	14	—	14	—	18	—	18	—	21	—	21	—	ns
$\overline{A}$	6	12	—	—	—	15	—	—	—	18	—	—	—	
	2	70	—	—	—	90	—	—	—	105	—	—	—	
B t_{WH}	4.5	14	—	14	—	18	—	18	—	21	—	21	—	ns
	6	12	—	—	—	15	—	—	—	18	—	—	—	
	2	70	—	—	—	90	—	—	—	105	—	—	—	
Reset t_{WL}	4.5	14	—	18	—	18	—	23	—	21	—	27	—	ns
	6	12	—	—	—	15	—	—	—	18	—	—	—	
Recovery Time	2	0	—	—	—	0	—	—	—	0	—	—	—	
$\overline{R}$ to $\overline{A}$ or B t_{REC}	4.5	0	—	0	—	0	—	0	—	0	—	0	—	ns
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Output Pulse Width Q or $\overline{Q}$ t_w C_x = 0.1 µF R_x = 10k Ω	5	630	770	630	770	602	798	602	798	595	805	595	805	µs
Output Pulse Width Q or Q t_w C_x = 28 pF, R_x = 2K Ω	4.5	Typical 140		Typical 140		—	—	—	—	—	—	—	—	ns
C_x = 1000 pF, R_x = 2K Ω t_w	4.5	1.5		1.5		—	—	—	—	—	—	—	—	µs
C_x = 1000 pF, R_x = 10K Ω t_w	4.5	7		7		—	—	—	—	—	—	—	—	µs

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	210	—	—	—	265	—	—	—	315	—	—	
Trigger		4.5	—	42	—	42	—	53	—	53	—	63	—	63	ns
$\overline{A}$, B, $\overline{R}$ to Q		6	—	36	—	—	—	45	—	—	—	54	—	—	
		2	—	170	—	—	—	215	—	—	—	255	—	—	
$\overline{A}$, B, $\overline{R}$ to $\overline{Q}$	t_{PHL}	4.5	—	34	—	34	—	43	—	43	—	51	—	51	ns
		6	—	29	—	—	—	37	—	—	—	43	—	—	
Propagation Delay		2	—	160	—	—	—	200	—	—	—	240	—	—	
$\overline{R}$ to Q	t_{PLH}	4.5	—	32	—	38	—	40	—	48	—	48	—	57	ns
		6	—	27	—	—	—	34	—	—	—	41	—	—	
		2	—	180	—	—	—	225	—	—	—	270	—	—	
$\overline{R}$ to $\overline{Q}$	t_{PHL}	4.5	—	36	—	37	—	45	—	46	—	54	—	56	ns
		6	—	31	—	—	—	38	—	—	—	46	—	—	
Output		2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
	t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{in}		—	10	—	10	—	10	—	10	—	10	—	10	pF
Pulse Width match between circuits in the same package C_x=1000 pF,R_x=10KΩ		4.5 to 5.5	Typical ±2		Typical ±2		—	—	—	—	—	—	—	—	%

CD54/74HC221
CD54/74HCT221

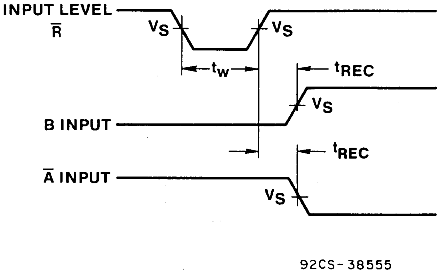


Fig. 2 — Recovery times, R̄ to Ā or B.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

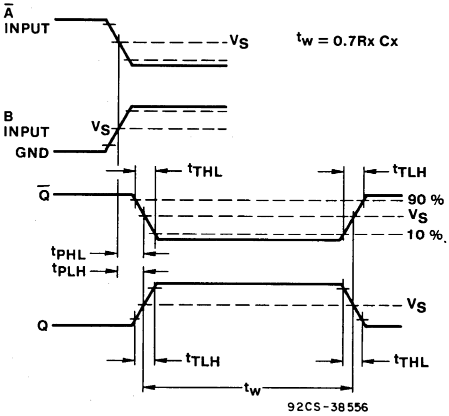


Fig. 3 — Triggering of One Shot by input Ā or input B for a period t_w.

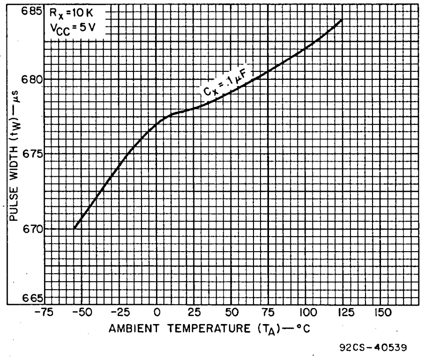


Fig. 4 — HC/HCT221 Output Pulse Width vs. Temperature.

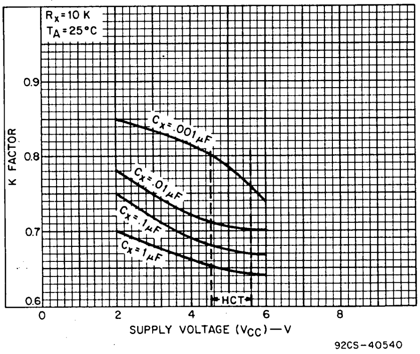


Fig. 5 — HC/HCT221 K Factor vs. Supply Voltage.

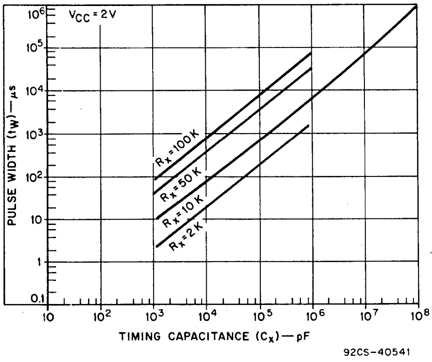


Fig. 6 — HC221 Output Pulse Width vs. C_X.

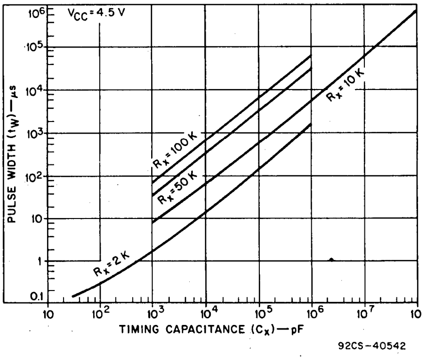


Fig. 7 — HC/HCT221 Output Pulse Width vs. C_X.

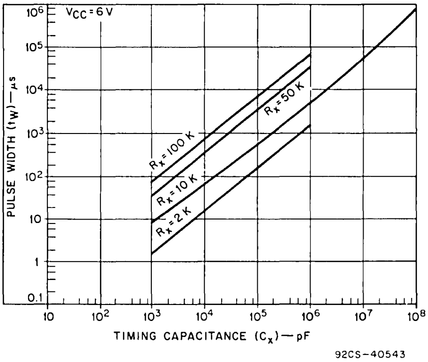
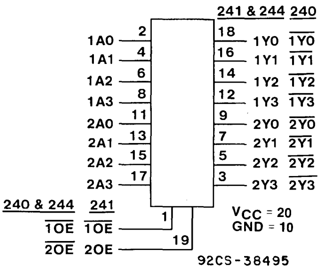


Fig. 8 — HC221 Output Pulse Width vs. C_X.

CD54/74HC240/241/244
CD54/74HCT240/241/244

File Number **1656**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Octal Buffer/Line Drivers, 3-State

CD54/74HC/HCT240 Inverting
CD54/74HC/HCT241 Non-Inverting
CD54/74HC/HCT244 Non-Inverting

Type Features:

- *Typical propagation delay = 8 ns @ V_{CC}=5 V, C_L=15 pF, T_A=25° C for HC240*
- *3-State outputs*
- *Buffered inputs*
- *High-current bus driver outputs*

The RCA-CD54/74HC240 and CD54/74HCT240 are inverting 3-state buffers having two active-low output enables. The RCA CD54/74HC/HCT241 and CD54/74HC/HCT244 are non-inverting 3-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

The CD54HC240/241/244 and CD54HCT240/241/244 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC240/241/244 and CD74HCT240/241/244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT240/241/244 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  $N_{IL}=30\%, N_{IH}=30\%$ *of* V_{CC}; @ $V_{CC}=5$ V
- *CD 54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL}=0.8$ V *Mas.,* $V_{IH}=2$ V *Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

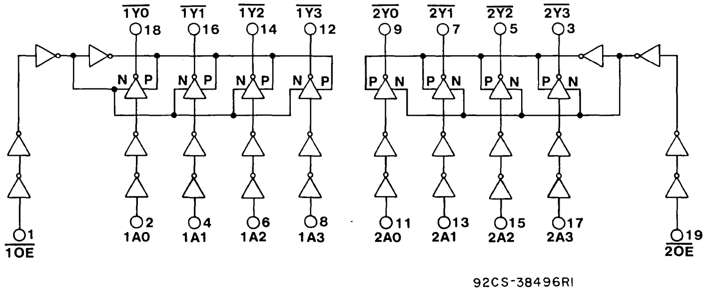


Fig. 1 - CD54/74HC/HCT240 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}$,$\overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

(HC/HCT240)

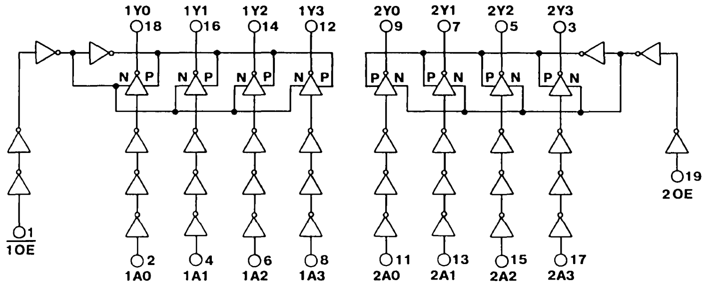


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Fig. 2 - CD54/74HC/HCT241 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

H=HIGH Voltage Level
L=LOW Voltage Level
X=Immaterial
Z=HIGH Impedance

(HCT/HCT241)

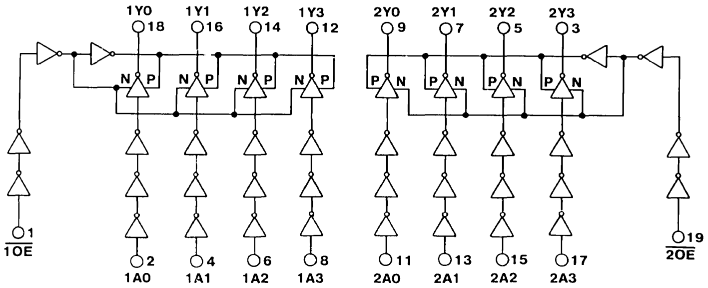

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Fig. 3 - CD54/74HC/HCT244 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE, 2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(HC/HCT244)

CD54/74HC240/241/244
CD54/74HCT240/241/244

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_o < V_{CC}$ +0.5 V)	±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC240/241/244
CD54/74HCT240/241/244

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC240/241/244, CD54HC240/241/244										CD74HCT240/241/244, CD54HCT240/241/244										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-state leakage current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

CD54/74HC240/241/244
CD54/74HCT240/241/244

HCT Input Loading Tables

CD54/74HCT240	
Input	**Unit Loads***
nA0-A3	1.5
$\overline{1\text{OE}}$	0.7
$\overline{2\text{OE}}$	0.7

CD54/74HCT241	
Input	**Unit Loads***
nA0-A3	0.7
$\overline{1\text{OE}}$	0.7
2OE	1.5

CD54/74HCT244	
Input	**Unit Loads***
nA0-A3	0.7
$\overline{1\text{OE}}$	0.7
$\overline{2\text{OE}}$	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	C_L	Typical Values						UNITS
			240		241		244		
		pF	HC	HCT	HC	HCT	HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	8	9	9	10	9	10	ns
Output Disable/Enable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	15	12	12	12	12	12	12	ns
Power Dissipation Capacitance	C_{PD}*	—	38	40	34	38	46	40	pF

C_{PD} is used to determine the dynamic power consumption per channel.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

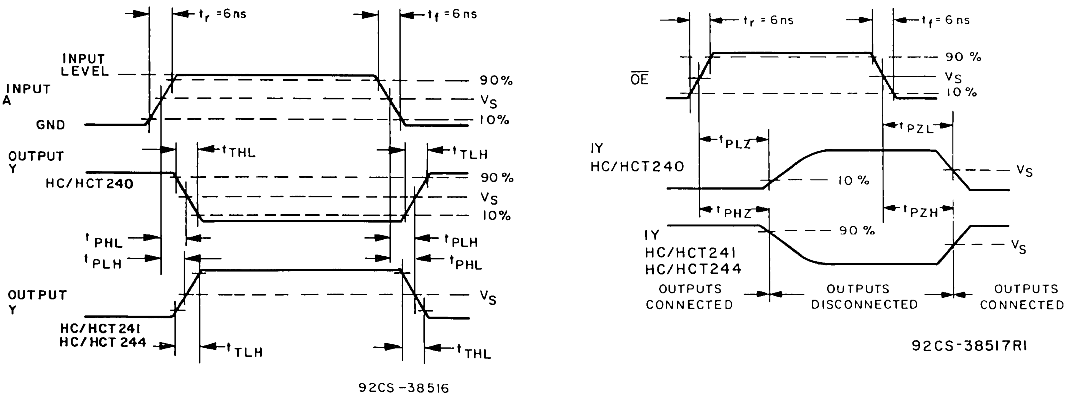
f_i=input frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
Data to Outputs	t_{PHL}	4.5	—	20	—	22	—	25	—	28	—	30	—	33	
HC/HCT 240		6	—	17	—	—	—	21	—	—	—	26	—	—	
Data to Outputs	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT241	t_{PHL}	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Data to Outputs	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT 244	t_{PHL}	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Output	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Enable and	t_{PZL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
Disable Times	t_{PHZ} t_{PLZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output		2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Transition Time	t_{TLH}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
	t_{THL}	6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.

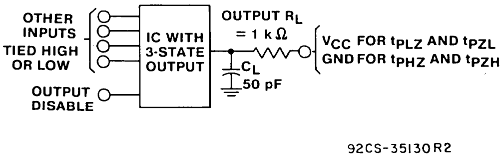


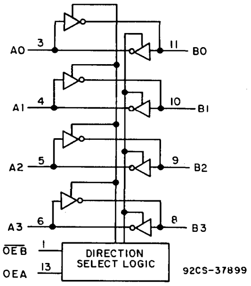
Fig. 4 - Three-state propagation delay test circuit.

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

File Number **1488**

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC242, HCT242

Quad-Bus Transceiver with 3-State Outputs

Type Features:

- *Typical propagation delay (A⟷B) of 7 ns @ $V_{CC} = 5$ V C_L = 15 pF, T_A = 25° C*
- *3-state outputs*
- *Buffered inputs*

The RCA-CD54/74HC242, 243 and CD54/74HCT242, 243 silicon-gate CMOS 3-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads.

The CD54/74HC242 and CD54/74HCT242 are inverting buffers; the CD54/74HC243 and CD54/74HCT243 are non-inverting buffers.

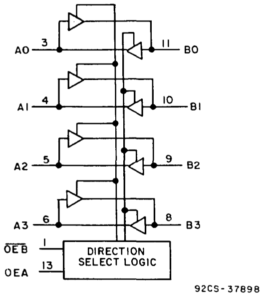
The states of the output enables ($\overline{\text{OEB}}$, OEA) determine both the direction of flow (A to B, B to A), and the 3-state mode.

The CD54HC242, 243 and CD54HCT242, 243 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC242, 243 and CD74HCT242, 243 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

FUNCTIONAL DIAGRAM



CD54/74HC243, HCT243

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

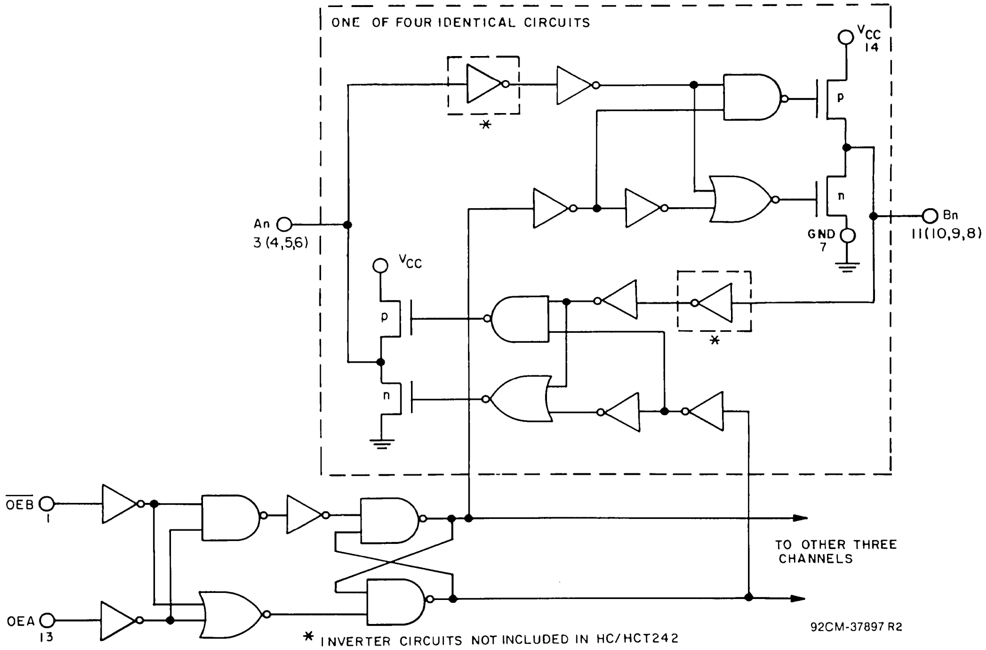


Fig. 1 - Logic diagram for the CD54/74HC/HCT242, 243.

TRUTH TABLE

CONTROL INPUTS		HC, HCT242 Series DATA PORT STATUS		HC, HCT243 Series DATA PORT STATUS	
$\overline{OEB}$	OEA	A_n	B_n	A_n	B_n
H	H	$\overline{O}$	I	O	I
L	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	L	I	$\overline{O}$	I	O

H = High
L = Low
I = Input

O = Output (Same Level as Input)
$\overline{O}$ = Output (Inversion of Input Level)
Z = High Impedance

To prevent excess currents in the High Z modes all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... −0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_o < V_{CC} +0.5$ V) .... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): .... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = −40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... −55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC242/243/CD54HC242/243										CD74HCT242/243/CD54HCT242/243										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V_I V	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-7.8	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
An, Bn	1.1
OEA, $\overline{OEB}$	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical				UNITS
			HC242	HCT242	HC243	HCT243	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	7	8	7	9	ns
Enable to High Z	t_{PHZ}, t_{PLZ}	15	12	14	12	14	ns
Enable from High-Z	t_{PZH}, t_{PZL}	15	12	14	12	14	ns
Power Dissipation Capacitance*	C_{PD}	—	85	90	80	91	pF

*C_{PD} is used to determine the dynamic power consumption, per channel.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:

f_i = input frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
Data to Outputs	t_{PHL}	4.5	—	18	—	20	—	23	—	25	—	27	—	30	ns
HC/HCT242		6	—	15	—	—	—	20	—	—	—	23	—	—	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
Data to Outputs	t_{PHL}	4.5	—	18	—	22	—	23	—	28	—	27	—	33	ns
for HC/HCT243		6	—	15	—	—	—	20	—	—	—	23	—	—	
Output High-Z:	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
to High Level;	t_{PZL}	4.5	—	30	—	34	—	38	—	43	—	45	—	51	ns
to Low Level		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output High Level;	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Low Level	t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
to High-Z		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

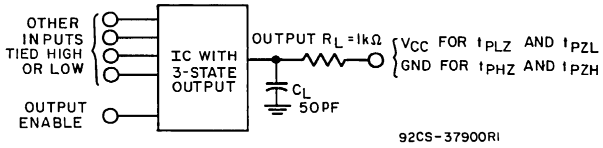
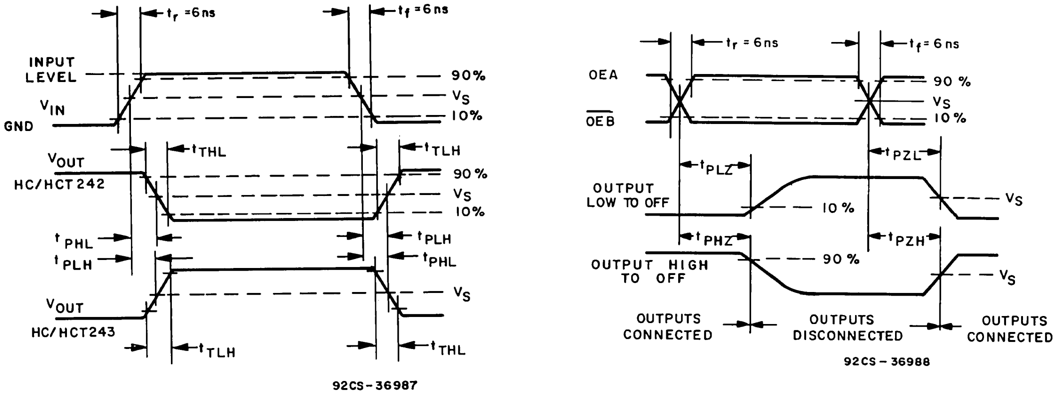
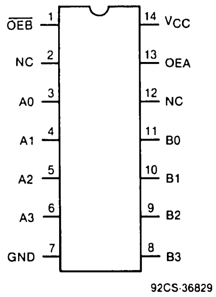


Fig. 2 - Three-state propagation delay test circuit.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 3 - Transition times and propagation delay times.



TERMINAL ASSIGNMENT

ORDERING INFORMATION

RCA CMOS device packages are identified by letters indicated in the following chart. When ordering a CMOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Plastic	E
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Surface Mount Plastic	M
Chip	H

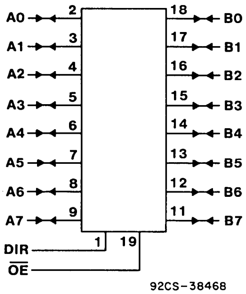
The CD54HC/HCT series is supplied in dual-in-line frit-seal ceramic packages (F suffix). The CD74HC/HCT series is supplied in dual-in-line plastic packages (E suffix) and in dual-in-line surface mount plastic packages (M suffix). Both series are supplied in chip form (H suffix).

For example, a CD54HC242 will be identified as the CD54HC242F. The CD74HC242 will be identified as the CD74HC242E.

CD54/74HC245
CD54/74HCT245

File Number **1651**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:

- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capability*
- *Typical propagation delay (A←→B)*
  9 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C

The RCA-CD54/74HC245 and CD54/74HCT245 are high-speed octal 3-state bidirectional transceivers intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation while driving large bus capacitances. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

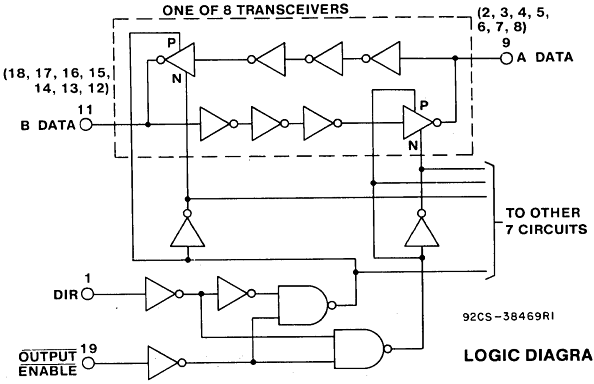
The CD54/74HC245 and CD54/74HCT245 allow data transmission from the A bus to the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input ($\overline{OE}$), when high, puts the I/O ports in the high-impedance state.

The HC/HCT245 is similar in operation to the HC/HCT640 and the HC/HCT643.

The CD54HC245 and CD54HCT245 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC245 and CD74HCT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip (H suffix) form.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V *Max.*, $V_{IH} = 2$ V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



LOGIC DIAGRAM

TRUTH TABLE		
CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (Isolation) modes all I/O terminals should be terminated with 10KΩ to 1MΩ resistors.

CD54/74HC245
CD54/74HCT245

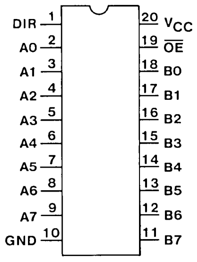
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-36830

TERMINAL ASSIGNMENT

CD54/74HC245
CD54/74HCT245

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC245/CD54HCT245										CD74HC245/CD54HCT245									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A_n or B_n	0.4
$\overline{OE}$	1.5
DIR	0.9

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

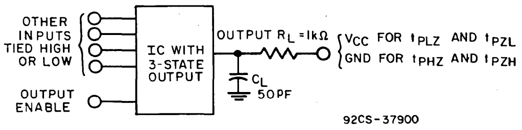
CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	9	10	ns
Enable to High-Z	t_{PHZ}, t_{PLZ}	15	12	12	ns
Enable from High-Z	t_{PZH}, t_{PZL}	15	12	13	ns
Power Dissipation Capacitance*	C_{PD}	—	53	55	pF

*C_{PD} determines the no-load dynamic power consumption per channel. It is obtained by the following relationship:
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency,
C_L = output load capacitance, V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (Input t_r, t_f = 6 ns, C_L = 50 pF)

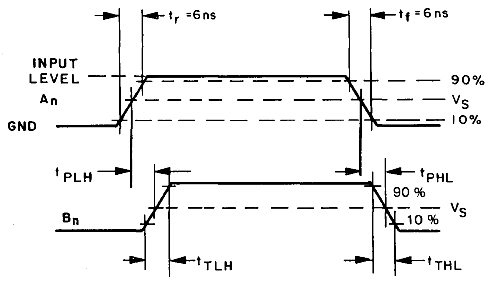
CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
Data to Output	t_{PHL}	4.5	—	22	—	26	—	28	—	33	—	33	—	39	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Output Disable		4.5	—	30	—	30	—	38	—	38	—	45	—	45	
to Output	t_{PHZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Output Enable		4.5	—	30	—	32	—	38	—	40	—	45	—	48	
to Output	t_{PZH}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_o	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC245
CD54/74HCT245



92CS-37900

Three-state propagation delay test circuit.



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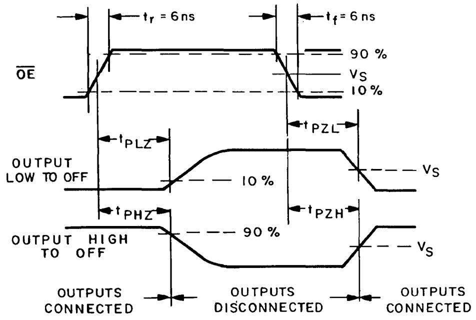


92CS-38407

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

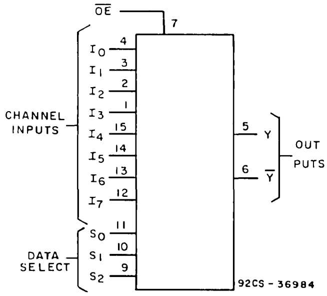
Fig. 1 - Transition times and propagation delay times.

File Number **1489**

CD54/74HC251
CD54/74HCT251

**Advance Information/
Preliminary Data**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Input Multiplexer; 3-State

Type Features:

- *Selects one of eight binary data inputs*
- *3-state output capability*
- *True and complement outputs*
- *Typical (data to output) propagation delay of 14 ns @ V_{CC}=5 V, C_L=15 pF, T_A=+25° C*

The RCA-CD54/74HC251 and CD54/74HCT251 are 8-channel digital multiplexers with 3-state outputs, fabricated with high-speed silicon-gate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The 3-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an output enable ($\overline{OE}$) input. The $\overline{OE}$ must be at a low logic level to enable this device. When the $\overline{OE}$ input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs. The CD54/74HCT251 logic family is speed, function, and pin-compatible with the standard 54LS/74LS251.

The CD54HC251 and CD54HCT251 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC251 and CD74HCT251 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - N_{IL} = 30%, N_{IH} = 30% *of* V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - V_{IL} = 0.8 V *Max.,* V_{IH} = 2 V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

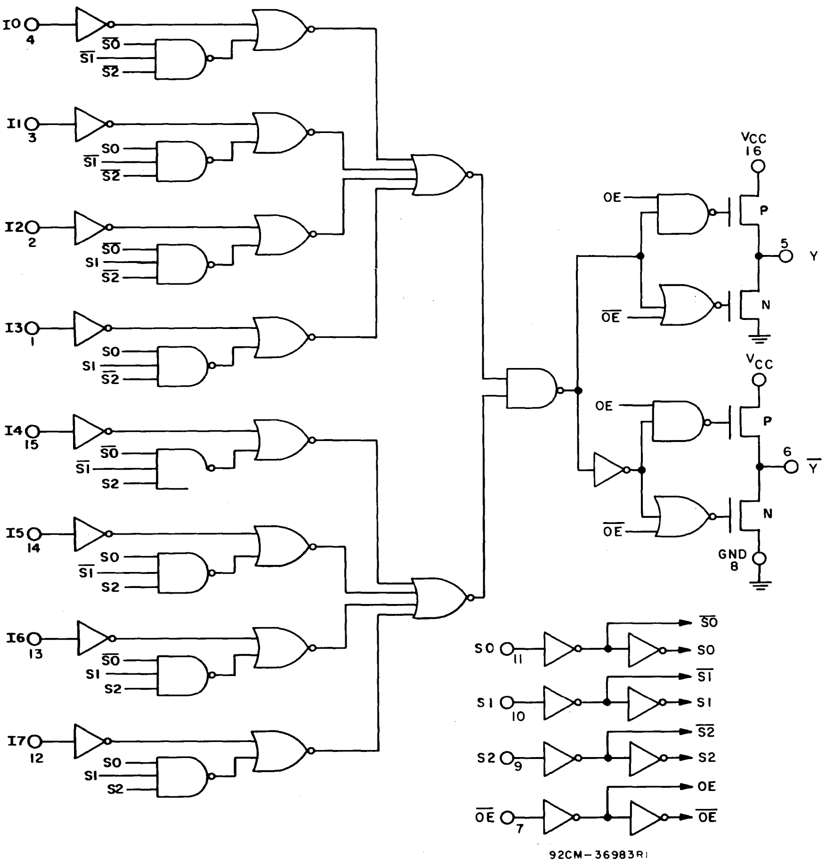


Fig. 3 - Logic diagram for HC/HCT251.

TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			OUTPUT CONTROL $\overline{OE}$	Y	$\overline{Y}$
S2	S1	S0			
X	X	X	H	Z	Z
L	L	L	L	I_0	I_0
L	L	H	L	I_1	I_1
L	H	L	L	I_2	I_2
L	H	H	L	I_3	I_3
H	L	L	L	I_4	I_4
H	L	H	L	I_5	I_5
H	H	L	L	I_6	I_6
H	H	H	L	I_7	I_7

H = high logic level
L = low logic level
X = irrelevant
Z = high impedance (off)
I_0, I_1 . . . . I_7 = the level of the respective input

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC251
CD54/74HCT251

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC251/CD54HC251										CD74HCT251/CD54HCT251									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
S0, S1, S2	0.55
I0-I7	0.5
$\overline{OE}$	2.65

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, = t_f = 6 ns)

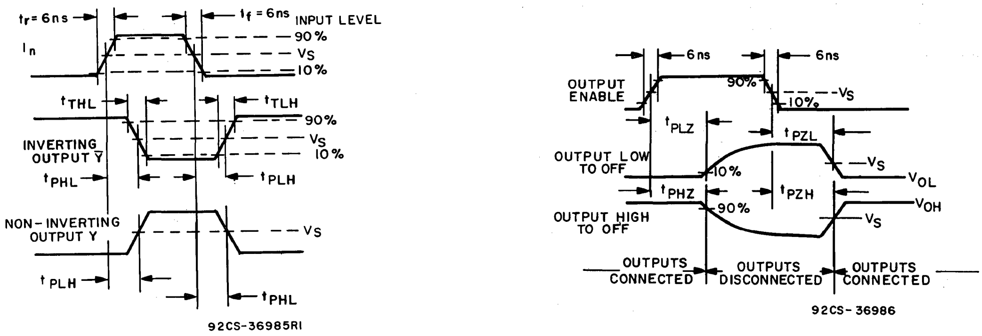
CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Select to Outputs	t_{PHL} t_{PLH}	15	21	18	ns
Data to Outputs		15	12	12	ns
Enable to High-Z and Enable from High-Z	t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH}	15	11	12	ns
Power Dissipation Capacitance*	C_{PD}	—	60	60	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$PD = V_{CC}^2f,(C_{PD} + C_L)$ where f_1 = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, = t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Select to Ouputs	t_{PLH} t_{PHL}	2	—	245	—	—	—	305	—	—	—	370	—	—	ns
		4.5	—	49	—	42	—	61	—	53	—	74	—	63	
		6	—	42	—	—	—	52	—	—	—	63	—	—	
Propagation Delay Data to Outputs	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay Enable to High Z & Enable From High Z	t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
		4.5	—	28	—	30	—	35	—	38	—	42	—	45	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10		10		10		10		10		10	pF
3-State Output Capacitance	C_O		—	15	—	15	—	15	—	15	—	15	—	15	pF

CD54/74HC251
CD54/74HCT251



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

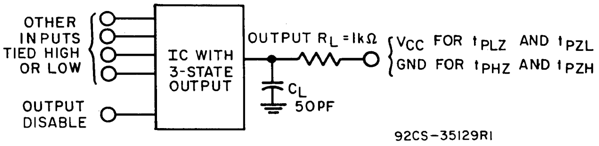
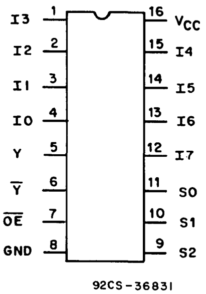


Fig. 2 - Three-state propagation delay test circuit.

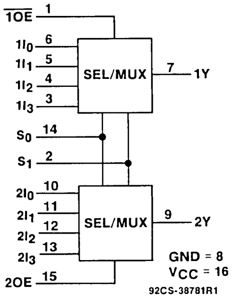


TERMINAL ASSIGNMENT

File Number **1673**

CD54/74HC253
CD54/74HCT253

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 4-Input Multiplexer

Type Features:

- *Common select inputs*
- *Separate output-enable inputs*
- *3-state outputs*

The RCA-CD54/74HC253 and CD54/74HCT253 are dual 4-to-1 line selector/multiplexers having 3-state outputs. One of four sources for each section is selected by the common select inputs, S0 and S1. When the output enable ($\overline{1OE}$ or $\overline{2OE}$) is HIGH, the output is in the high-impedance state.

The CD54HC253 and CD54HCT253 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC253 and CD74HCT253 are in 16-lead dual-in-line plastic packages (E suffix), also in 16-lead dual-in-line surface mount plastic packages (M suffix). These types are also available in chip form (H suffix).

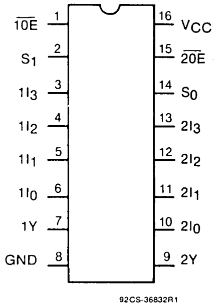
TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Output
S1	S0	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S0 and S1 are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: $N_{IL}=30\%$, $N_{IH}=30\%$ of V_{CC}; @ $V_{CC}=5$ V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL}=0.8$ V max., $V_{IH}=2$ V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC253
CD54/74HCT253

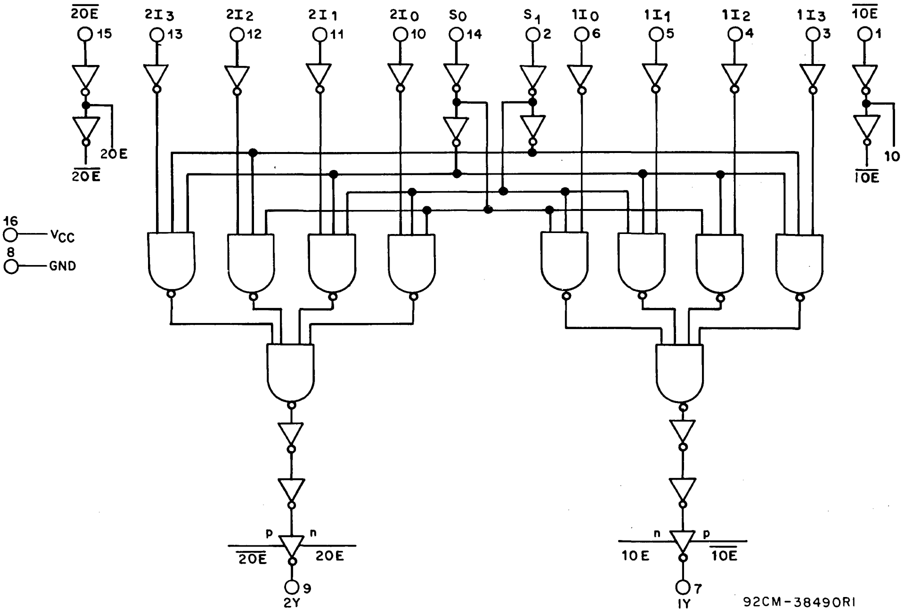


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$ V)	±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

CD54/74HC253
CD54/74HCT253

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC253/CD54HC253										CD74HCT253/CD54HCT253									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Bus Driver	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Bus Driver	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$1I_0$-$1I_3$, $2I_0$-$2I_3$	0.4
$1\overline{E}_0$, $2\overline{E}_0$, S_0, S_1	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC253
CD54/74HCT253

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

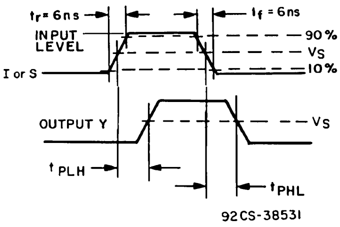
CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay					
Select to Outputs	15	t_{PHL}	14	16	ns
Data to Outputs		t_{PLH}			
Output Enabling Time	15	t_{PZL}, t_{PZH}	9	12	
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	12	12	
Power Dissipation Capacitance*		C_{PD}	46	52	pF

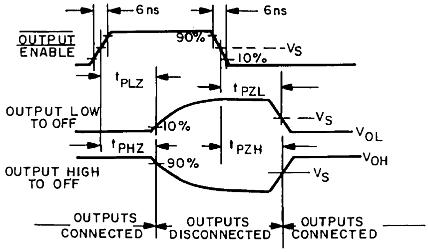
*C_{PD} is used to determine the dynamic power consumption, per multiplexer.

$P_D=V_{CC}^2 fi (C_{PD} + C_L)$ where: fi=input frequency
C_L=load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	VCC	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Select to Outputs	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay Data to Outputs	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Disable Delay Times	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PLZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Enable Delay Times	t_{PZH}	2	—	110	—	—	—	140	—	—	—	165	—	—	
	t_{PZL}	4.5	—	22	—	30	—	28	—	38	—	33	—	45	ns
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Output Transition Time	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	





	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition and propagation delay times.

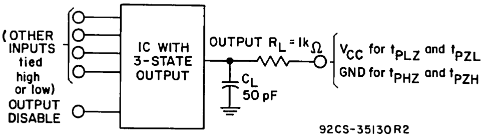
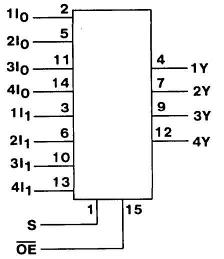


Fig. 3 - Three-state propagation delay test circuit.

CD54/74HC257
CD54/74HCT257

High-Speed CMOS Logic



92CS-38419

FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexer with 3-State Non-Inverting Outputs

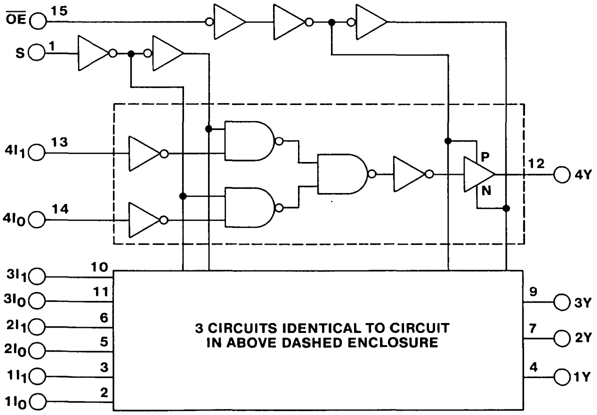
Type Features:

- *Buffered Inputs*
- *Typical Propagation Delay (In to Output) = 12 ns @ $V_{CC} = 5v$, $C_L = 15pF$, $T_A = 25°C$*

The RCA-CD54/74HC257 and CD54/74HCT257 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Output Enable input ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs (1Y-4Y) are in the high impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 257. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

The CD54HC257 and CD54HCT257 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC257 and CD74HCT257 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-38421

LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High level voltage
L = Low level voltage
Z = High impedance (off) state.
X = Don't care

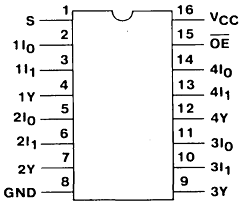
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5$V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC257
CD54/74HCT257

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC257/CD54HC257										CD74HCT257/CD54HCT257									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State leakage current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Data	0.95
S	3
$\overline{OE}$	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

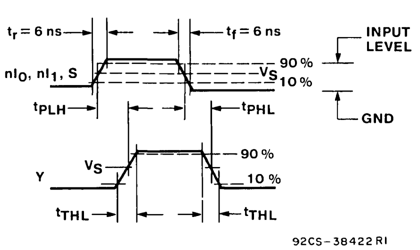
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

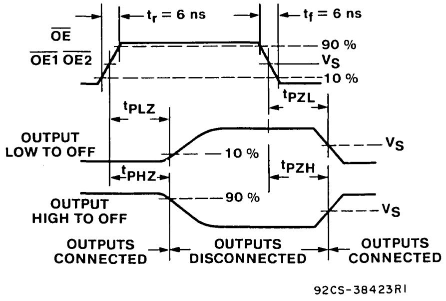
CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
nI_0, nI_1, to Y	15	t_{PHL} t_{PLH}	12	13	ns
$\overline{OE}$ to Y	15	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	12	12	ns
S to Y	15	t_{PHL} t_{PLH}	14	16	ns
Power Dissipation Capacitance*	—	C_{PD}	45	45	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i=input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, In to Y (Fig. 2)	t_{PLH}	2		150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PHL}	4.5		30	—	33	—	38	—	41	—	45	—	50	
		6		26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay S to Y (Fig. 2)		2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PLH}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
	t_{PHL}	6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay $\overline{OE}$ to Y (Fig. 3)	t_{PLZ} t_{PZL} t_{PHZ} t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time (Fig. 2)	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF





	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

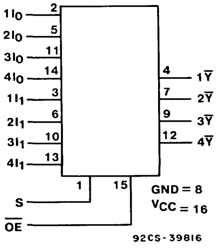
Fig. 2 - Inputs or select to output propagation delays and output transition times.

Fig. 3 - Output Enable to output propagation delays.

CD54/74HC258
CD54/74HCT258

File Number **1775**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexer with 3-State Inverting Outputs

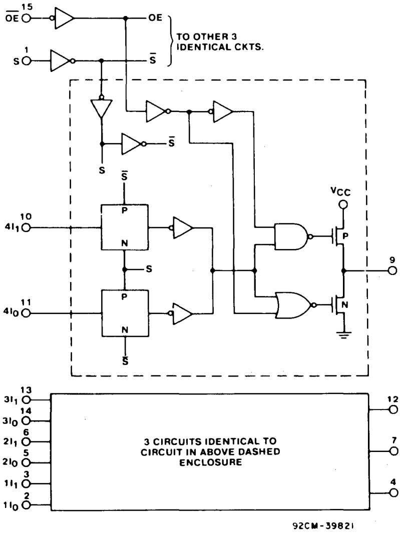
Type Features:
- *Buffered inputs*
- *Typical CD54/74HC258 propagation delay = 7 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC258 and CD54/74HCT258 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Output Enable input (OE̅) is active LOW. When OE̅ is HIGH, all of the outputs (1Y̅-4Y̅) are in the high impedance state regardless of all other input conditions.

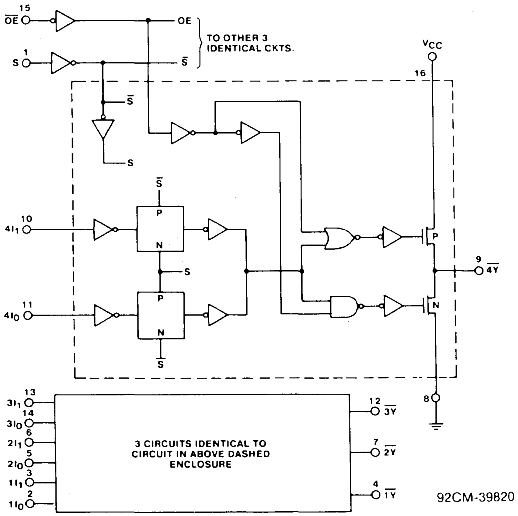
Moving data from two groups of registers to four common output busses is a common use of the 258. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

The CD54HC/HCT258 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT/HCU: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



CD54/74HC258 Logic Diagram



CD54/74HCT258 Logic Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

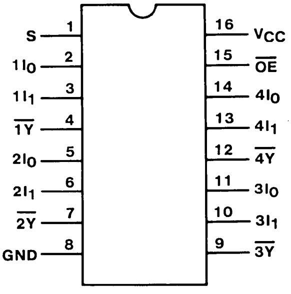
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level voltage
L = Low level voltage
X = Don't care.
Z = High impedance (off) state



TERMINAL ASSIGNMENT

CD54/74HC258
CD54/74HCT258

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC258/CD54HC258										CD74HCT258/CD54HCT258									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-6	4.5	3.98	—	—	3.84	—	3.7	—										
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		6	4.5	—	—	0.26	—	0.33	—	0.4										
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State leakage current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Data	0.5
S	1.5
$\overline{\text{OE}}$	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC258
CD54/74HCT258

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL		UNITS
			HC	HCT	
nI_O, nI_I, to $\overline{Y}$	t_{PHL} t_{PLH}	15	7	11	ns
$\overline{OE}$ to $\overline{Y}$	t_{PZL} t_{PZH}	15	11	11	ns
	t_{PLZ} t_{PHZ}	15	12	12	ns
S to $\overline{Y}$	t_{PHL} t_{PLH}	15	11	14	ns
Power Dissipation Capacitance*	C_{PD}	—	49	49	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 fi (C_{PD} + C_L)$ where: fi = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	95	—	—	—	120	—	—	—	145	—	—	
nI_O, nI_I, to $\overline{Y}$	t_{PHL}	4.5	—	19	—	27	—	24	—	34	—	29	—	41	ns
(Fig. 2)		6	—	15	—	—	—	20	—	—	—	25	—	—	
Propagation Delay		2	—	140	—	—	—	175	—	—	—	210	—	—	
S to $\overline{Y}$	t_{PLH}	4.5	—	28	—	34	—	35	—	43	—	42	—	51	ns
(Fig. 3)	t_{PHL}	6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay		2	—	140	—	—	—	175	—	—	—	210	—	—	
$\overline{OE}$ to Y	t_{PZL}	4.5	—	28	—	28	—	35	—	35	—	42	—	42	ns
(Fig. 4)	t_{PZH}	6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{OE}$ to Y		4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
(Fig. 4)	t_{PHZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
(Fig. 2)		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC258
CD54/74HCT258

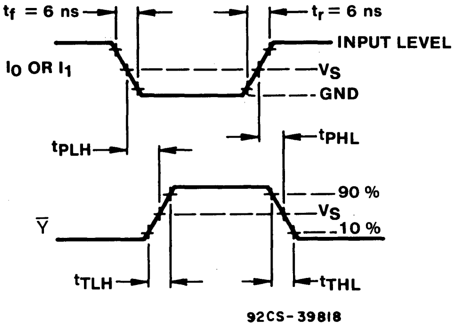


Fig. 2 - Select to output delays.

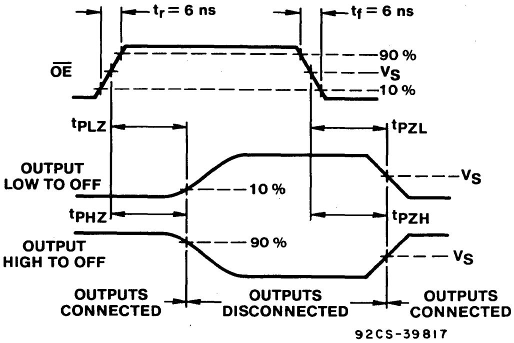


Fig. 4 - Output Enable to output propagation delays.

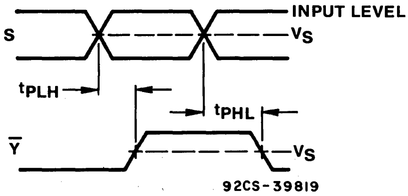


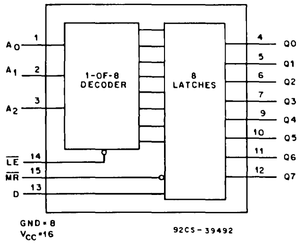
Fig. 3 - Select to output propagation delays.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1727**

CD54/74HC259
CD54/74HCT259

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Addressable Latch

Type Features:

- *Buffered inputs and outputs*
- *Four operating modes*
- *Typical propagation delay of 15 ns @ $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = +25°C$*

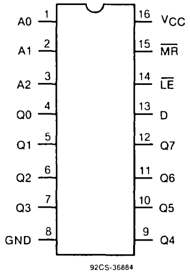
The RCA-CD54/74HC259 and CD54/74HCT259 Addressable Latch features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latch has three active modes and one reset mode. When both the Latch Enable ($\overline{\text{LE}}$) and Master Reset ($\overline{\text{MR}}$) inputs are low (8-line Demultiplexer mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both $\overline{\text{MR}}$ and $\overline{\text{LE}}$ are high (Memory Mode), all outputs are isolated from the Data input, i.e., all latches hold the last data presented before the $\overline{\text{LE}}$ transition from low to high. A condition of $\overline{\text{LE}}$ low and $\overline{\text{MR}}$ high (Addressable Latch mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when $\overline{\text{LE}}$ is high and $\overline{\text{MR}}$ is low.

The CD54HC259 and CD54HCT259 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC259 and CD74HCT259 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
- *Bus driver outputs - 15 LSTTL loads*
  Wide operating temperature range:
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC259
CD54/74HCT259

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	265°C
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	300°C

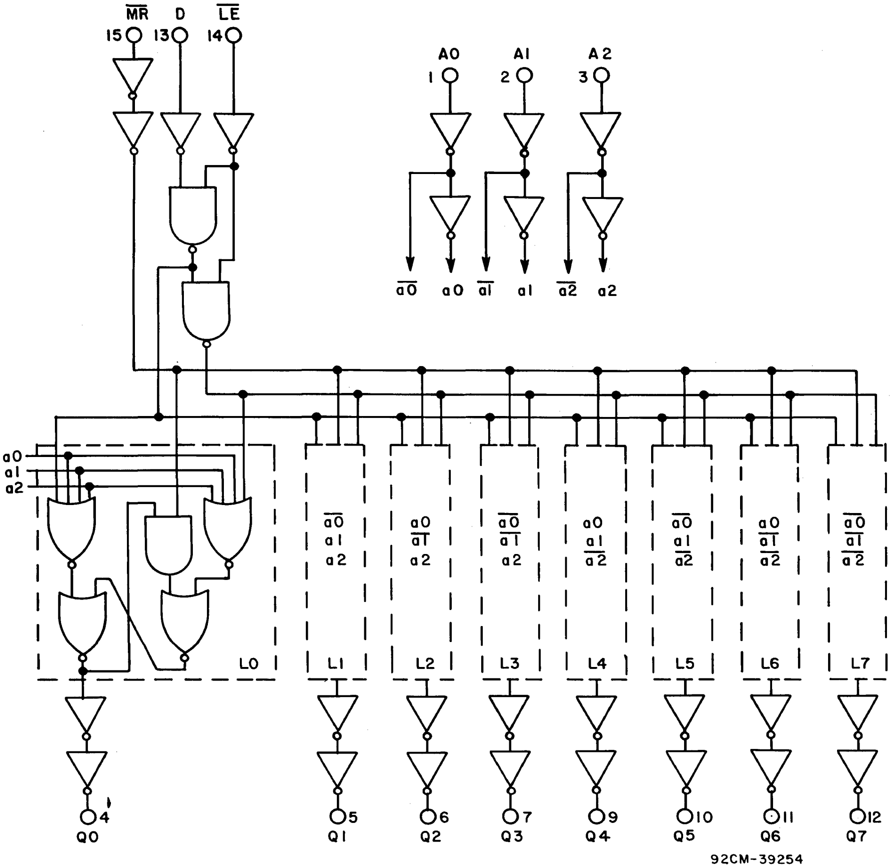


Fig. 1 - Logic diagram.

CD54/74HC259
CD54/74HCT259

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE

INPUTS		Output of Address Latch	Each Other Output	Function
$\overline{MR}$	$\overline{LE}$			
H	L	D	Q_{io}	Addressable Latch
H	H	Q_{io}	Q_{io}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Reset

H = High level L = Low level
D = The level at the data input
Q_{io} = The level of Q_i (i = 0, 1...7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

Select Inputs			Latch Addressed
A2	A1	A0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

CD54/74HC259
CD54/74HCT259

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC259, CD54HC259										CD74HCT259, CD54HCT259									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
A0-A2, $\overline{LE}$	1.5
D	1.2
$\overline{MR}$	0.75

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay D to Q	t_{PLH} t_{PHL}	15	15	16	ns
$\overline{LE}$ to Q			14	16	ns
A to Q			15	17	ns
$\overline{MR}$ to Q		15	13	16	ns
Power Dissipation Capacitance*	C_{PD}	—	21	22	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD}V_{CC}{}^2f_i + \Sigma\, C_LV_{CC}{}^2f_o$ where f_i = input frequency, f_o = output frequency,

C_L = output load capacitance, V_{CC} = supply voltage.

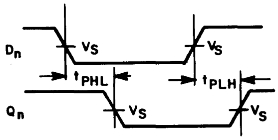
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} V	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pulse Width	t_{WL}	2	70	—	—	—	90	—	—	—	105	—	—	—	
$\overline{LE}$		4.5	14	—	18	—	18	—	23	—	21	—	27	—	ns
		6	12	—	—	—	15	—	—	—	18	—	—	—	
		2	70	—	—	—	90	—	—	—	105	—	—	—	
$\overline{MR}$	t_{WL}	4.5	14	—	18	—	18	—	23	—	21	—	27	—	ns
		6	12	—	—	—	15	—	—	—	18	—	—	—	
Set-up Time	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	
D to $\overline{LE}$		4.5	16	—	17	—	20	—	21	—	24	—	26	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
A to $\overline{LE}$	t_{SU}	4.5	16	—	17	—	20	—	21	—	24	—	26	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	
D to $\overline{LE}$		4.5	0	—	0	—	0	—	0	—	0	—	0	—	ns
		6	0	—	—	—	0	—	—	—	0	—	—	—	
		2	0	—	—	—	0	—	—	—	0	—	—	—	
A to $\overline{LE}$	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	ns
		6	0	—	—	—	0	—	—	—	0	—	—	—	

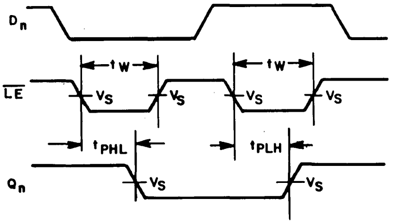
CD54/74HC259
CD54/74HCT259

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

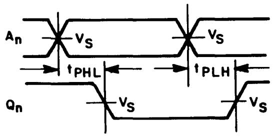
CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay D to Q	t_{PLH} t_{PHL}	2	—	185	—	—	—	230	—	—	—	280	—	—	ns
		4.5	—	37	—	39	—	46	—	49	—	56	—	59	
		6	—	31	—	—	—	39	—	—	—	48	—	—	
$\overline{LE}$ to Q		2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	38	—	43	—	48	—	51	—	57	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
A to Q		2	—	185	—	—	—	230	—	—	—	280	—	—	ns
		4.5	—	37	—	41	—	46	—	51	—	56	—	61	
		6	—	31	—	—	—	39	—	—	—	48	—	—	
$\overline{MR}$ to Q		2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	39	—	39	—	49	—	47	—	59	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



PROPAGATION DELAY
DATA TO OUTPUT



LATCH ENABLE PULSE WIDTH AND
LATCH ENABLE TO OUTPUT PROPAGATION DELAY

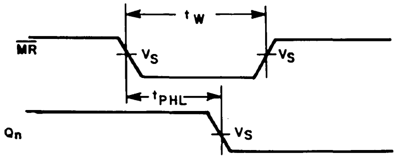


PROPAGATION DELAY
ADDRESS TO OUTPUT

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

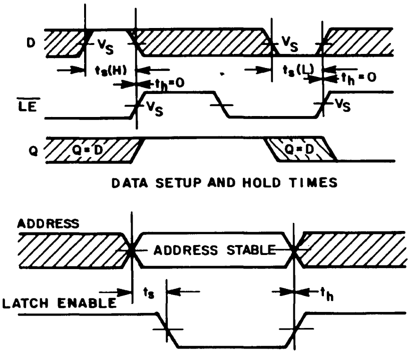
92CM-39256RI

Fig. 2 - AC Waveforms.



MR TO OUTPUT DELAY
AND MR PULSE WIDTH

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V



DATA SETUP AND HOLD TIMES

ADDRESS SETUP AND HOLD TIMES

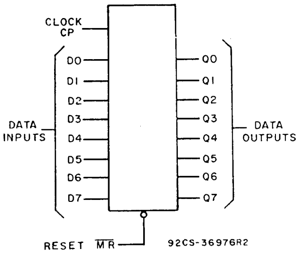
92CM-39259RI

Fig. 3 - AC Waveforms.

CD54/74HC273
CD54/74HCT273

File Number **1479**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D Flip-Flop with Reset

Type Features:

- *Common clock and asynchronous master reset*
- *Positive-edge triggering*
- *Buffered inputs*
- *Typical* $f_{max} = 60$ *MHz @* $V_{CC} = 5$ *V,* $C_L = 15$*pF,* $T_A = 25°$ *C*

The RCA CD54/74HC273 and the CD54/74HCT273 high speed Octal D-Type Flip-Flops with a direct clear input are manufactured with silicon-gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits.

Information at the D input is transferred to the Q outputs on the positive-going edge of the clock pulse. All eight Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

The CD54HC273 and CD54HCT273 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC273 and CD74HCT273 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:* $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC} *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
  - $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  - *CMOS Input Compatibility*
  - $I_I \leq 1$ *µA @* V_{OL}, V_{OH}

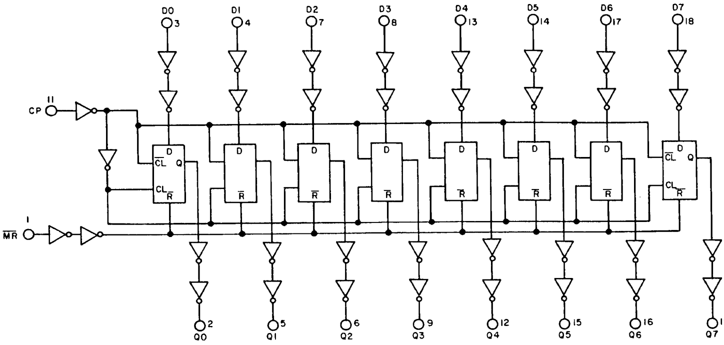


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} +0.5$ V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
RESET (MR)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	_/‾	H	H
H	_/‾	L	L
H	L	X	Qo

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
_/‾ = Transition from Low to High Level
Qo = The Level of Q Before the Indicated Steady-State Input Conditions were Established

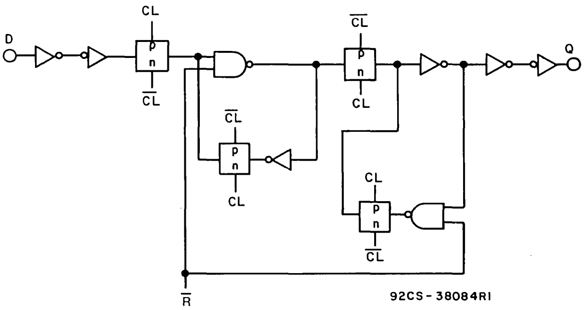


Fig. 2 - Flip-Flop detail.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC273
CD54/74HCT273

STATIC ELECTRICAL CHARACTERISTICS

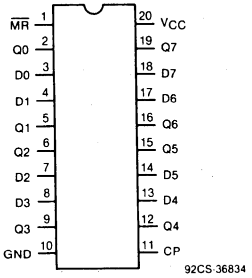
CHARACTERISTIC	CD74HC273/CD54HC273										CD74HCT273/CD54HCT273										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-4	4.5	3.98	—	—	3.84	—	3.7	—											
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		4	4.5	—	—	0.26	—	0.33	—	0.4											
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS#
$\overline{MR}$	1.5
Data	0.4
CP	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.



TERMINAL ASSIGNMENT

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock	2	6		—		5		—		4		—		
Frequency f_{max}	4.5	30		25		25		20		20		16		MHz
Fig. 3	6	35		—		29		—		23		—		
	2	60		—		75		—		90		—		
$\overline{MR}$ Pulse Width t_W	4.5	12		12		15		15		18		18		ns
Fig. 4	6	10		—		13		—		15		—		
	2	80		—		100		—		120		—		
Clock Pulse Width t_W	4.5	16		20		20		25		24		30		ns
Fig. 3	6	14		—		17		—		20		—		
Set-up Time	2	60		—		75		—		70		—		
Data to Clock	4.5	12		12		15		15		18		18		ns
Fig. 5 t_{SU}	6	10		—		13		—		15		—		
Hold Time	2	3		—		3		—		3		—		
Data to Clock	4.5	3		3		3		3		3		3		ns
Fig. 5 t_H	6	3		—		3		—		3		—		
Removal Time	2	50		—		65		—		75		—		
$\overline{MR}$ to Clock t_{REM}	4.5	10		10		13		13		15		15		ns
	6	9		—		11		—		13		—		

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L	TYPICAL		UNITS
		pF	HC	HCT	
Propagation Delay, Clock to Q	t_{PLH} t_{PHL}	15	12	12	ns
Maximum Clock Frequency	f_{max}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	25	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 fi + \Sigma\, C_L V_{CC}^2 fo$ where fi = input frequency, fo = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

CD54/74HC273
CD54/74HCT273

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS 25° C HC Min.	25° C HC Max.	25° C HCT Min.	25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Propagation Delay t_{PLH}	2		150		—		190		—		225		—	
Clock to Output t_{PHL}	4.5		30		30		38		38		45		45	ns
Fig. 3	6		26		—		30		—		38		—	
Propagation Delay	2		150		—		190		—		225		—	
$\overline{MR}$ to Output t_{PHL}	4.5		30		32		38		40		45		48	ns
Fig. 4	6		26		—		33		—		38		—	
Output Transition t_{TLH}	2		75		—		95		—		110		—	
Time t_{THL}	4.5		15		15		19		19		22		22	ns
Fig. 6	6		13		—		16		—		19		—	
Input Capacitance C_i	—		10		10		10		10		10		10	pF

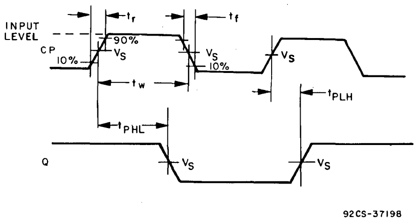


Fig. 3 - Clock to output delays and clock pulse width.

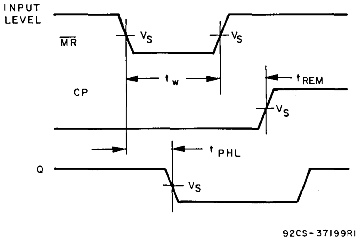
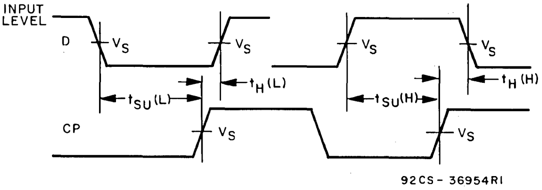


Fig. 4 - Master reset pulse width. Master reset to output delay and master reset to clock recovery time.



	54 74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 - Data set-up and hold times.

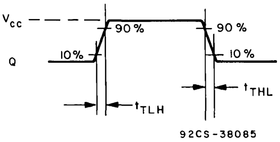


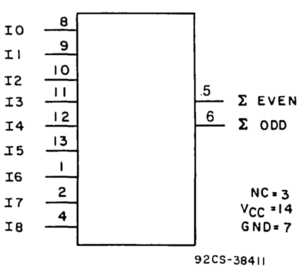
Fig. 6 - Transition times.

File Number **1669**

CD54/74HC280
CD54/74HCT280

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



9-Bit Odd/Even Parity Generator/Checker

Type Features:

- *Typical propagation delay = 17ns @ V_{CC} = 5 V, C_L = 15pF, T_A = 25° C*
- *Replaces 74LS180 types*
- *Easily cascadable*

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range: CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, V_{CC}, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*

The RCA-CD54/74HC280 and CD54/74HCT280 are 9-bit odd/even parity, generator checker devices. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated (ΣE output is high) when an even number of data inputs is high. Odd parity is indicated (ΣO output is high) when an odd number of data inputs is high. Parity checking for words larger than 9 bits can be accomplished by tying the ΣE output to any input of an additional HC/HCT280 parity checker.

The CD54HC280 and CD54HCT280 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC280 and CD74HCT280 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

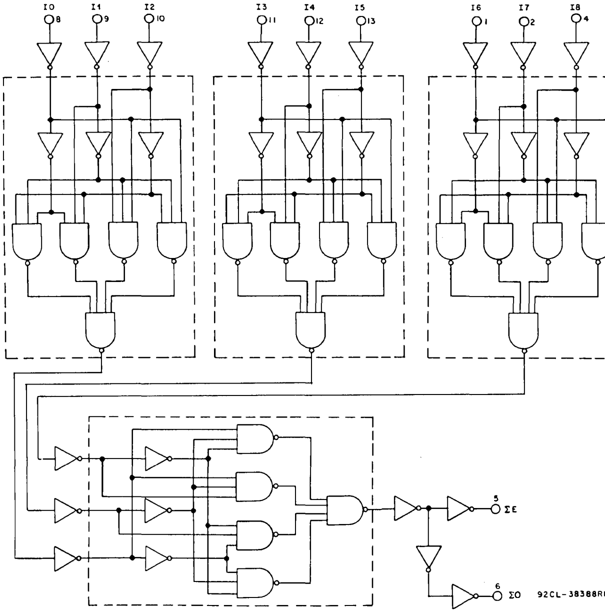


Fig. 1 — Logic Diagram

CD54/74HC280
CD54/74HCT280

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC280/CD54HC280										CD74HCT280/CD54HCT280									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC280
CD54/74HCT280

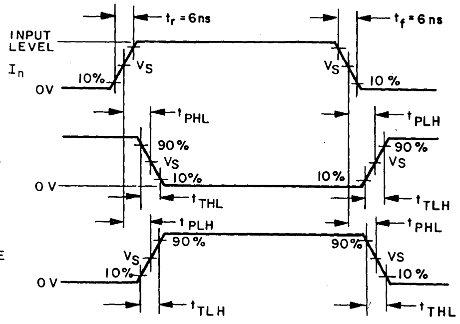
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Any Input to ΣO	15	t_{PHL} t_{PLH}	17	19	ns
Any Input to ΣE	15	t_{PHL} t_{PLH}	17	18	ns
Power Dissipation Capacitance*	—	C_{PD}	58	58	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
PD =V_{CC}^2 f_i (C_{PD} + C_L) where f_i = input frequency,
C_L = output load capacitance.
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f=6 ns)

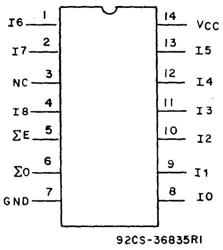
CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Any Input to ΣO	t_{PLH} t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Any Input to ΣE	t_{PLH} t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	42	—	50	—	53	—	60	—	63	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



92CS-38412RI

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 2 — Propagation delay and transition times.



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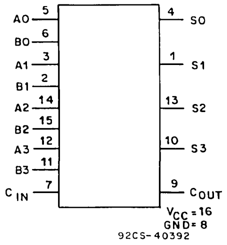
TERMINAL ASSIGNMENT

File Number **1848**

CD54/74HC283
CD54/74HCT283

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Binary Full Adder With Fast Carry

Type Features:

- *Adds two binary numbers*
- *Full internal lookahead*
- *Fast ripple carry for economical expansion*
- *Operates with both positive and negative logic*

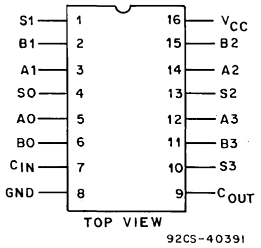
The RCA-CD54/74HC283 and CD54/74HCT283 are binary-full adders that add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

The CD54HC/HCT283 are supplied in 16-lead hermetic dual-in-line frit seal ceramic packages (F suffix). The CD74HC/HCT283 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC283
CD54/74HCT283

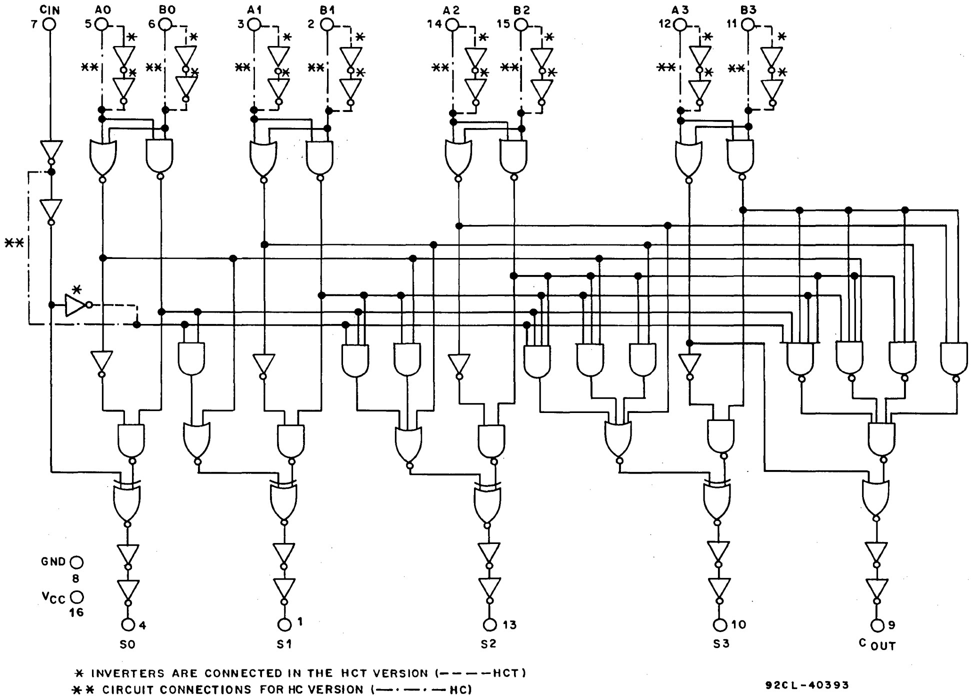


Fig. 1 - Logic diagram for HC/HCT types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
  (Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} +0.5$ V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
  For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
  For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
  For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
  For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
  For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPE F, H .... -55 to +125° C
  PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
  Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm)
    with solder contacting lead tips only .... +300° C

CD54/74HC283
CD54/74HCT283

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC283/CD54HC283										CD74HCT283/CD54HCT283										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
C_{IN}	1.5
B1, A1, A0	1
B0	0.4
B3, A3, A2, B2	0.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC283
CD54/74HCT283

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay,					
C_{IN} to S0	t_{PLH}, t_{PHL}	15	13	13	ns
C_{IN} to S1	t_{PLH}, t_{PHL}	15	15	18	
C_{IN} to S2	t_{PLH}, t_{PHL}	15	16	19	
C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	15	16	19	
C_{IN} to S3	t_{PHL}, t_{PLH}	15	19	22	
A_n, B_n to C_{OUT}	t_{PHL}, t_{PLH}	15	16	20	
A_n, B_n to S_n	t_{PHL}, t_{PLH}	15	18	21	
Power Dissipation Capacitance *	C_{PD}	—	70	82	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

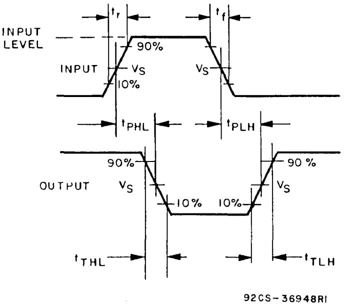
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay C_{IN} to S0	t_{PLH} t_{PHL}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
		4.5	—	32	—	31	—	40	—	39	—	48	—	47	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
C_{IN} to S1	t_{PLH} t_{PHL}	2	—	180	—	—	—	225	—	—	—	270	—	—	
		4.5	—	36	—	43	—	45	—	54	—	54	—	65	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
C_{IN} to S2, C_{IN} to C_{OUT}	t_{PLH} t_{PHL}	2	—	195	—	—	—	245	—	—	—	295	—	—	
		4.5	—	39	—	46	—	49	—	58	—	59	—	69	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
C_{IN} to S3	t_{PLH} t_{PHL}	2	—	230	—	—	—	290	—	—	—	345	—	—	
		4.5	—	46	—	53	—	58	—	66	—	69	—	80	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
A_n, B_n to C_{OUT}	t_{PLH} t_{PHL}	2	—	195	—	—	—	245	—	—	—	295	—	—	
		4.5	—	39	—	48	—	49	—	60	—	59	—	72	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
A_n, B_n to S_n	t_{PLH} t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	49	—	53	—	61	—	63	—	74	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



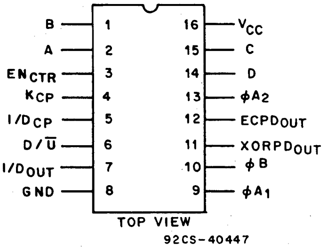
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition and propagation delay times.

CD54/74HC297
CD54/74HCT297

File Number **1852**

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

Digital Phase-Locked-Loop Filter

Type Features:

- *Digital design avoids analog compensation errors*
- *Easily cascadable for higher order loops*
- *Useful frequency range:*
  - *DC to 55 MHz typical (k-clock)*
  - *DC to 35 MHz typical (I/D-clock)*
- *Dynamically variable bandwidth*
- *Very narrow bandwidth attainable*
- *Power-on reset*
- *Output capability:*
  - *Standard - $XORPD_{OUT}$, $ECPD_{OUT}$*
  - *Bus driver - I/D_{OUT}*

The RCA-CD54/74HC/HCT297 are high-speed silicon-gate CMOS devices that are pin-compatible with low power Schottky TTL (LSTTL).

These devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. They contain all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled phase detectors (ECPD) are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

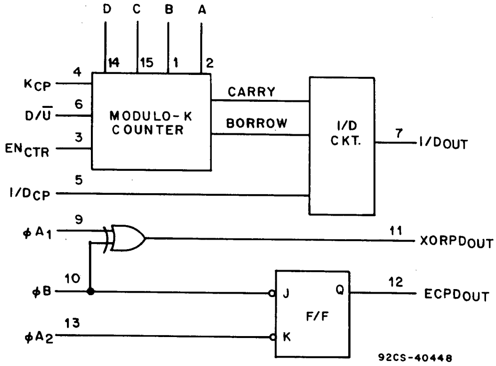
Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 2) or to cascade to higher order phase-locked-loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengths the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximum the overall performance of the digital phase-locked-loop.

The CD54/74HC/HCT297 can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by VCC and temperature variations but depends solely on accuracies of the K-clock and loop propagation delays.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
  - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



FUNCTIONAL DIAGRAM

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error (ϕIN - ϕOUT). Within these limits the phase detector output varies linearly with the input phase error according to the gain K_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\text{HIGH} - \%\text{LOW}}{100}$$

The output of the phase detector will be $K_d\phi_e$, where the phase error

$\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (K_d) for an XORPD is 4 because its output remains HIGH ($\text{XORPD}_{OUT} = 1$) for a phase error of ¼ cycle.

Similarly, K_d for the ECPD is 2 since its output remains HIGH for a phase error of ½ cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 3, ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are ¼ cycle out-of-phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are ½ cycle out of phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c which is a multiple M of the loop center frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(K_d\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is ½ of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry of borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (K_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus:

$f_o = f_c + (K_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus, the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

The CD54HC297 and CD54HCT297 are supplied in 16-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC297 and CD74HCT297 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR

ϕA_1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

ϕA_2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No Change
↑	H or L	No Change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

CD54/74HC297
CD54/74HCT297

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC297/CD54HC297											CD74HCT297/CD54HCT297									UNITS
	TEST CONDITIONS				74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA		V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
					Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}				2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—										
				6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}				2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35										
				6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02		2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
				4.5	4.4	—	—	4.4	—	4.4	—										
				6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	#	I/D									V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	-6	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02		2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
				4.5	—	—	0.1	—	0.1	—	0.1										
				6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	#	I/D									V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	6	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd			6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0		6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*												V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

XORPD, ECPD

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
EN_{CTR}, $D/\overline{U}$	0.3
A, B, C, D, K_{CP}, ϕA_2	0.6
I/D_{CP}, ϕA_1, ϕB	1.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC297
CD54/74HCT297

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock		2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
Frequency	f_{MAX}	4.5	30	—	30	—	24	—	24	—	20	—	20	—	
K_{CP}		6	35	—	—	—	28	—	—	—	24	—	—	—	
		2	4	—	—	—	3	—	—	—	2	—	—	—	MHz
$1/D_{CP}$		4.5	20	—	20	—	16	—	16	—	13	—	13	—	
		6	24	—	—	—	19	—	—	—	15	—	—	—	
Clock Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
K_{CP}		6	14	—	—	—	17	—	—	—	20	—	—	—	
		2	125	—	—	—	155	—	—	—	190	—	—	—	ns
$1/D_{CP}$		4.5	25	—	25	—	31	—	31	—	38	—	38	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
Setup Time		2	100	—	—	—	125	—	—	—	150	—	—	—	ns
$D/\overline{U}$, EN_{CTR} to K_{CP}	t_{SU}	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time		2	0	—	—	—	0	—	—	—	0	—	—	—	ns
$D/\overline{U}$, EN_{CTR} to K_{CP}	t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
I/D_{CP} to I/D_{OUT}	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	34	—	—	—	43	—	—	
		2	—	150	—	—	—	190	—	—	—	225	—	—	
ϕA_1, ϕB to $XORPD_{OUT}$		4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
		2	—	200	—	—	—	250	—	—	—	300	—	—	
ϕB, ϕA_2 to $ECPD_{OUT}$		4.5	—	40	—	40	—	50	—	50	—	60	—	60	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Transition Time		2	—	75	—	—	—	95	—	—	—	110	—	—	
$XORPD_{OUT}$,	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
$ECPD_{OUT}$,	t_{TLH}	6	—	13	—	—	—	16	—	—	—	19	—	—	
		2	—	60	—	—	—	75	—	—	—	90	—	—	
I/D_{OUT}		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

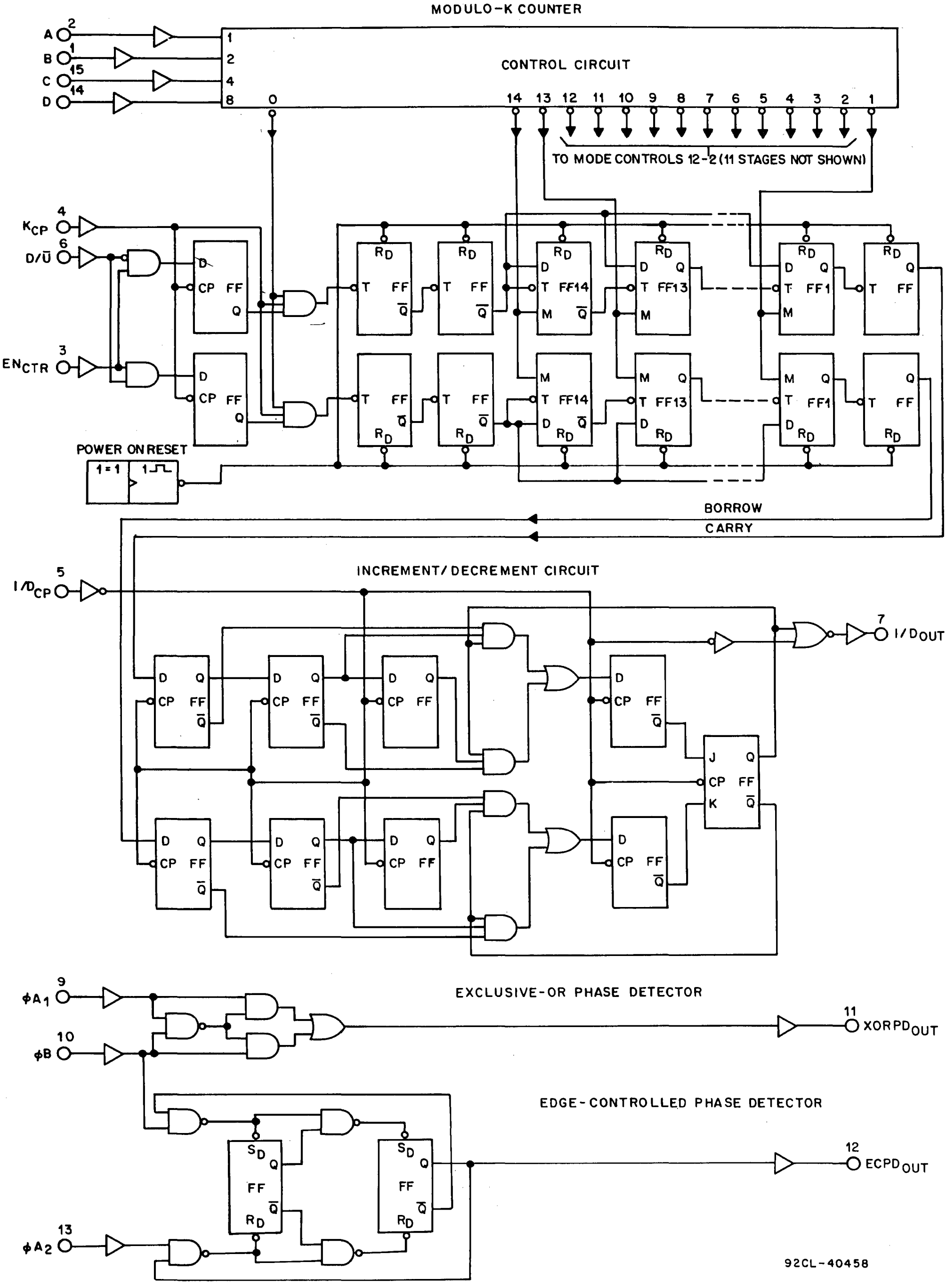


Fig. 1 - Logic diagram.

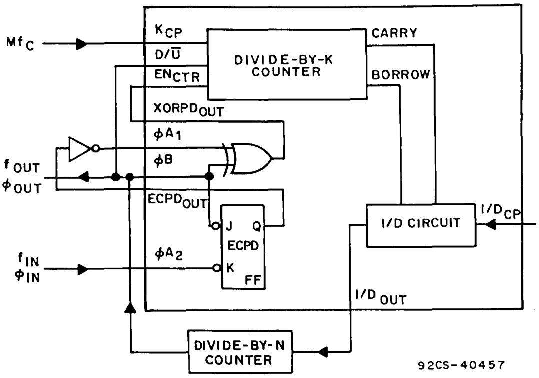


Fig. 2 - DPLL using both phase detectors in a ripple-cancellation scheme.

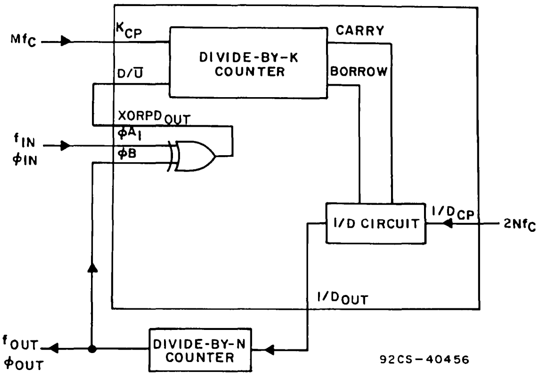


Fig. 3 - DPLL using EXCLUSIVE-OR phase detection.

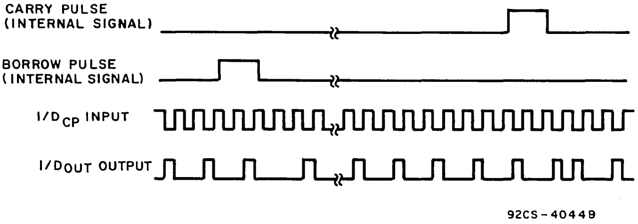
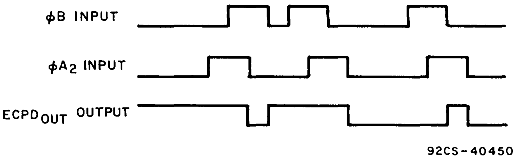


Fig. 4 - Timing diagram: I/D$_{OUT}$ in-lock condition.



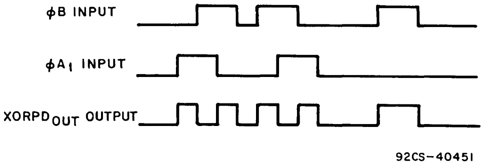


Fig. 5 - Timing diagram: edge-controlled phase comparator waveforms.

Fig. 6 - Timing diagram: EXLUSIVE-OR phase detector waveforms.

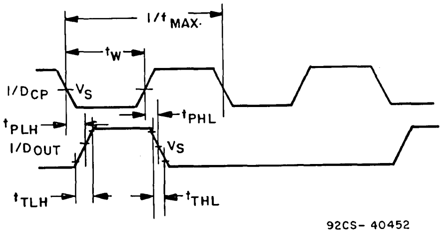


Fig. 7 - Waveforms showing the clock (I/D_{CP}) to output (I/D_{OUT}) propagation delays, clock pulse width, output transition times and maximum clock pulse frequency.

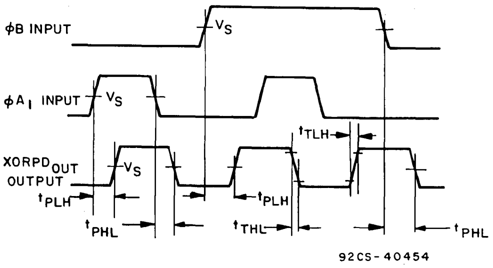


Fig. 8 - Waveforms showing the phase input (ϕB, ϕA_1) to output ($XORPD_{OUT}$) propagation delays and output transition times.

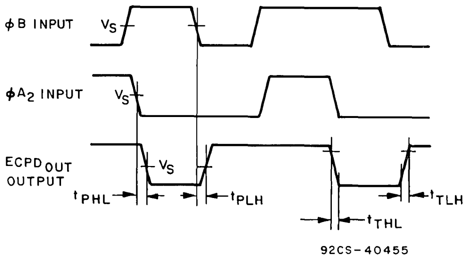
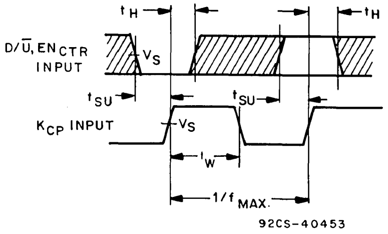


Fig. 9 - Waveforms showing the phase input (ϕB, ϕA_2) to output ($ECPD_{OUT}$) propagation delays and output transition times.



NOTE: THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE.

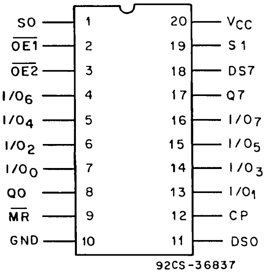
Fig. 10 - Waveforms showing the clock (K_{CP}) pulse width and maximum clock pulse frequency, and the input ($D/\overline{U}$, EN_{CTR}) to clock (K_{CP}) set-up and hold times.

	54/74HC	**54/74HCT**
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1485**

CD54/74HC299
CD54/74HCT299

High-Speed CMOS Logic



TERMINAL ASSIGNMENT

8-Bit Universal Shift Register; 3-State

Type Features:

- *Four Operation Modes: Shift Left, Shift Right, Load and Store*
- *Can be cascaded for N-bit word lengths*
- *I/O_0-I/O_7 bus drive capability and 3-state for bus oriented applications*
- *Buffered inputs*
- *Typical f_{MAX}=50 MHz @ V_{CC}=5 V, C_L=15 pF, T_A=25°C*

The RCA-CD54/74HC299 and CD54/74HCT299 are 8-bit shift/storage registers with 3-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O_0-I/O_7) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be one set-up time prior to the clock positive transition.

The Master Reset ($\overline{MR}$) is an asynchronous active low input. When $\overline{MR}$ output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The 3-state input/output I(/O) port has three modes of operation:

1. Both output enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a 3-state output and an CMOS buffer input.

The CD54HC299 and CD54HCT299 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC299 and CD74HCT299 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
  - *N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

CD54/74HC299
CD54/74HCT299

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$V)
For Q Outputs .... ±25mA
For I/O Outputs .... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +40 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING TEMPERATURE RANGE (T_A)
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

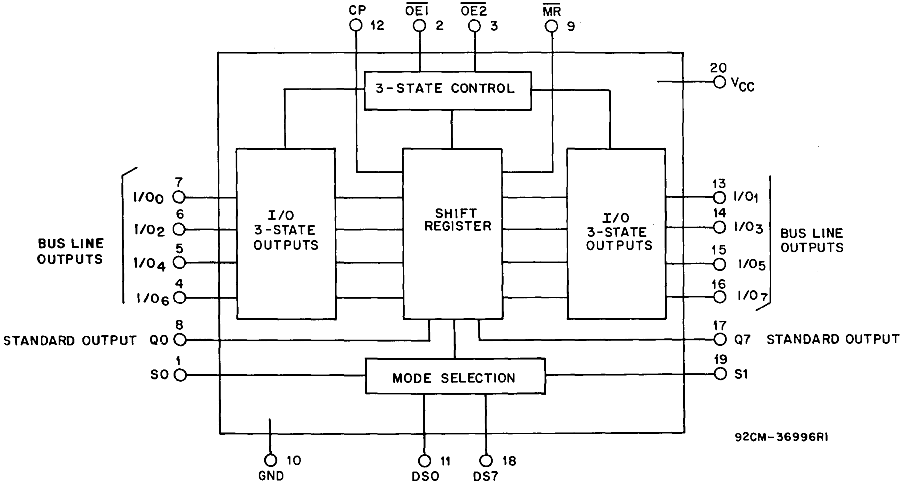


Fig. 1 — Function diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC299/CD54HC299										CD74HCT299/CD54HCT299										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	Qn, I/On									V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-4, -6	4.5	3.98	—	—	3.84	—	3.7	—											
		-5.2, -7.8	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads Bus Driver and Standard Output	V_{IL} or V_{IH}	Qn, I/On									V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		4, 6	4.5	—	—	0.26	—	0.33	—	0.4											
		5.2, 7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1		µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		µA
3-State Leakage Current	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10		µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
S1, $\overline{MR}$	0.25
I/O_0-I/O_7	0.25
DS0, DS7	0.25
$\overline{S0}$, CP	0.6
$\overline{OE1}$, $\overline{OE2}$	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC299
CD54/74HCT299

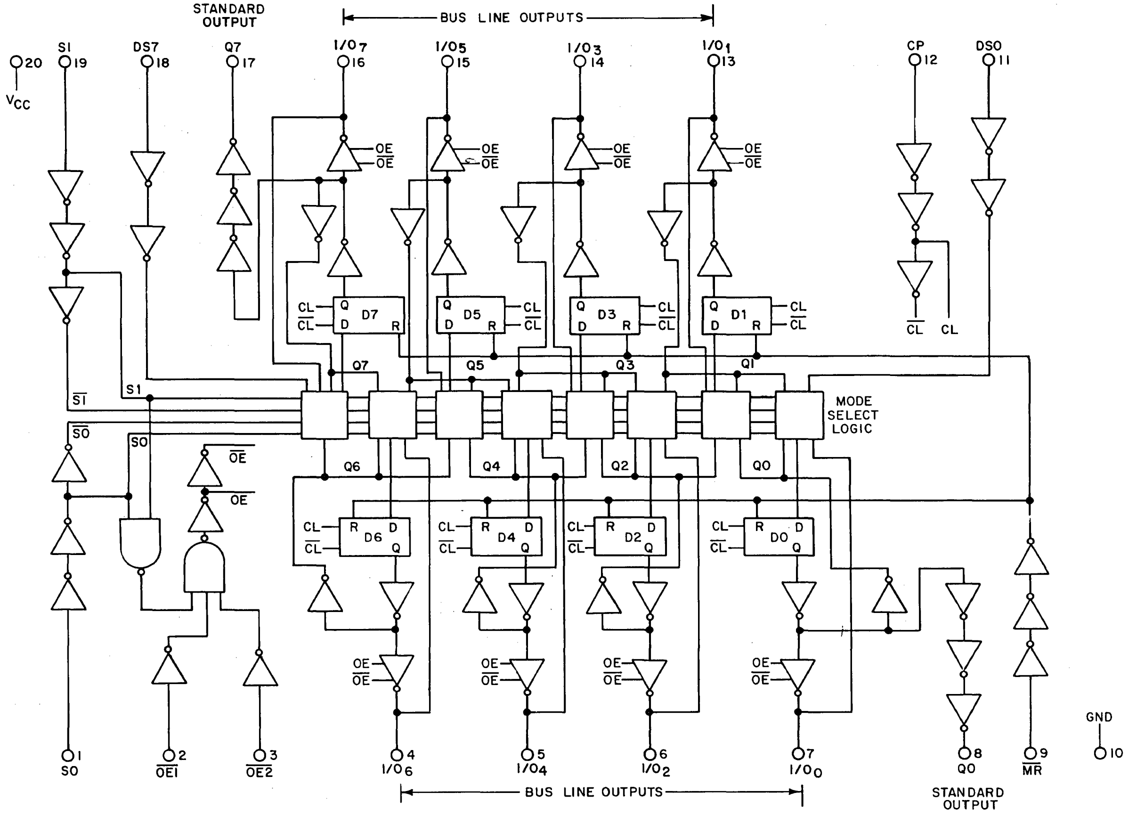


Fig. 2 — Logic diagram.

92CL-37003R2

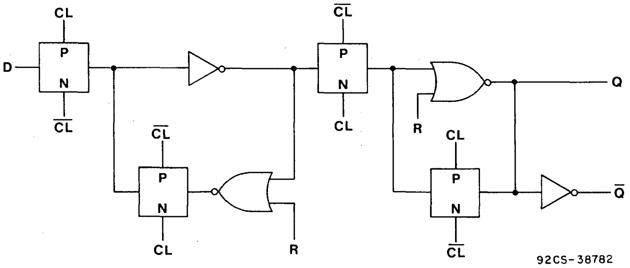


Fig. 3 — Flip-Flop detail (D0-D7).

MODE SELECT-FUNCTION TABLE

REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/On	Q0	Q1	---	Q6	Q7
Reset (Clear)	**L**	**X**	**X**	**X**	**X**	**X**	**X**	**L**	**L**	**---**	**L**	**L**
Shift Right	H	↑	h	l	l	X	X	L	q_0	---	q_5	q_6
	H	↑	h	l	h	X	X	H	q_0	---	q_5	Q6
Shift Left	H	↑	l	h	X	l	X	q_1	q2	---	q_7	L
	H	↑	l	h	X	h	X	q_1	q_2	---	q_7	H
Hold (do nothing)	H	↑	l	l	X	X	X	q_0	q_1	---	q_6	q_7
Parallel Load	H	↑	h	h	X	X	l	L	L	---	L	L
	H	↑	h	h	X	X	h	H	H	---	H	H

MODE-SELECT FUNCTION TABLE
3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (Register)	I/O0 - - - I/O7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/On	I/On = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.
h = Input voltage high one set-up time prior clock transition.
L = Input voltage low level.
l = Input voltge low one set-up time prior clock transition.
q_n = Lower case letter indicates the state of the referenced output one set-up time prior clock transition.
X = Voltage level on logic status don't care.
Z = Output in high impedance state.
↗ = Low-to-high clock transition.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Clock to I/O Outputs (Fig. 4)	t_{PLH} t_{PHL}	15	17	19	ns
Clock Q0 or Q7 (Fig. 4)					
$\overline{MR}$ to Outputs (Fig. 5)	t_{PHL}	15	17	19	
Output Enable and Disable Times (Fig. 6 & 7)	t_{PZL}, t_{PZH} t_{PLZ}, t_{PHZ}	15	10,13,15	10,13,15	
Power Dissipation Capacitance	C_{PD}*	—	150	170	pF

*C_{PD} is used to determine the dynamic power consumption, per register.
$PD = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

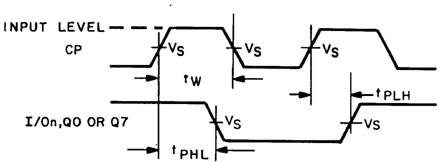
Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
$\overline{MR}$ Pulse Width (Fig. 5)	t_W	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	15	—	13	—	19	—	15	—	22	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Clock Pulse Width (Fig. 4)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time DS0, DS7, I/On to Clock (Fig. 8)	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time DS0, DS7, I/On, S0, S1 to Clock (Fig. 8)	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time $\overline{MR}$ to Clock (Fig. 5)	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Setup Time S1, S0 to Clock	t_{SU}	2	120	—	—	—	150	—	—	—	180	—	—	—	
		4.5	24	—	27	—	30	—	34	—	36	—	41	—	
		6	20	—	—	—	26	—	—	—	31	—	—	—	

CD54/74HC299
CD54/74HCT299

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

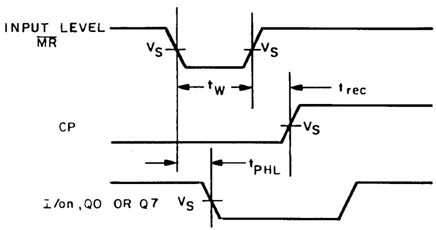
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Clock to I/O Output (Fig. 4)	t_{PLH} t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Clock to Q0 and Q7 (Fig. 4)		2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Propagation Delay $\overline{MR}$ to Output (Fig. 5)	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
		4.5	—	40	—	46	—	50	—	58	—	60	—	69	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output High-Z to High Level (Fig. 6)	t_{PZH}	2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output High Level to High-Z (Fig. 6)	t_{PHZ}	2	—	185	—	—	—	230	—	—	—	280	—	—	
		4.5	—	37	—	37	—	46	—	46	—	56	—	56	
		6	—	31	—	—	—	39	—	—	—	48	—	—	
Output Low Level to High-Z (Fig. 7)	t_{PLZ}	2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	32	—	39	—	40	—	47	—	48	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output High-Z to Low Level (Fig. 7)	t_{PZL}	2	—	130	—	—	—	165	—	—	—	195	—	—	
		4.5	—	26	—	30	—	33	—	38	—	39	—	45	
		6	—	22	—	—	—	28	—	—	—	33	—	—	
Output Transition Time Q0, Q7 (Fig. 9)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
I/O_0 to I/O_7 (Fig. 9)		2	—	60	—	—	—	75	—	—	—	90	—	—	
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



	74/54 HC	74/54 HCT
INPUT LEVEL	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-36997

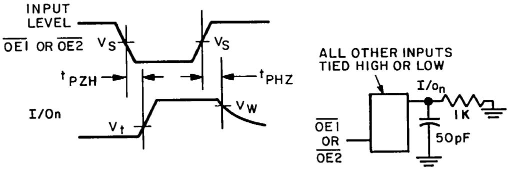
Fig. 4 — Clock pre-requisite and propagation delays.



	74/54HC	74/54 HCT
INPUT LEVEL	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-36998

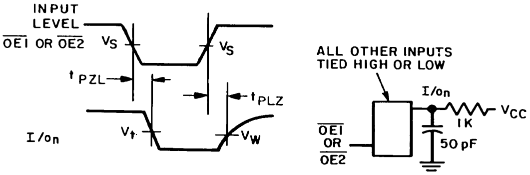
Fig. 5 — Master Reset pre-requisite and propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_W	90% V_{CC}	90% V_{CC}

92CS-36999RI

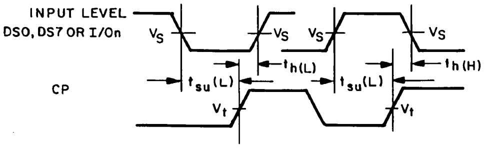
Fig. 6 — 3-state propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_W	10% V_{CC}	10% V_{CC}

92CS-37000RI

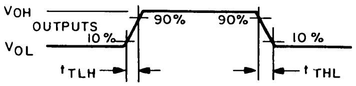
Fig. 7 — 3-state propagation delays.



	74/54 HC	74/54 HCT
INPUT LEVEL	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V

92CS-37001RI

Fig. 8 — Data pre-requisite times.



	74/54 HC	74/54 HCT
INPUT LEVEL	V_{CC}	3V

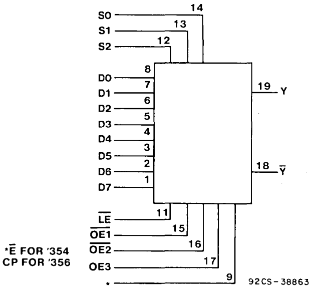
92CS-37002

Fig. 9 — Output transition times.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

File Number **1690**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Input Multiplexer/Register, 3-State

CD54/74HC/HCT354 — Transparent Data & Select Latches
CD54/74HC/HCT356 — Edge-Triggered Data Flip-Flops
Transparent Select Latches

Type Features:

- *Buffered inputs*
- *3-State Complementary Outputs*
- *Bus Line Driving Capability*
- *Typical propagation delay:* $V_{CC} = 5V$, $C_L = 15\ pF$, $T_A = 25°C$
  Data to Output (354) = 18 ns
  Clock to Output (356) = 22 ns

The RCA-CD54/74HC/HCT354 and CD54/74HC/HCT356 are data selectors/multiplexers that select one of eight sources. In both the HC/HCT354 and HC/HCT356 the data select bits S0, S1, and S2 are stored in transparent latches that are enabled by a low latch enable input, $\overline{LE}$.

In the HC/HCT354 the data enable input, $\overline{E}$, controls transparent latches that pass data to the outputs when $\overline{E}$ is high and latches in new data when $\overline{E}$ is low.

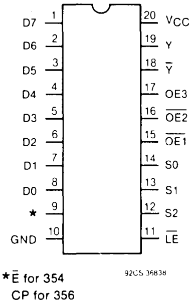
In the HC/HCT356 the data is stored in edge-triggered flip-flops that are triggered by a low-to-high clock transition.

In both types the three-state outputs are controlled by three output-enable inputs $\overline{OE1}$, $\overline{OE2}$, and OE3.

The CD54HC/HCT354/356 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT354/356 are supplied in 20-lead plastic dual-in-line plastic packages (E suffix). The CD54/74HC/HCT354/356 are also supplied in chip form (H suffix). The CD74HC/HCT354/356 are also available in plastic surface mounted packages (M suffix).

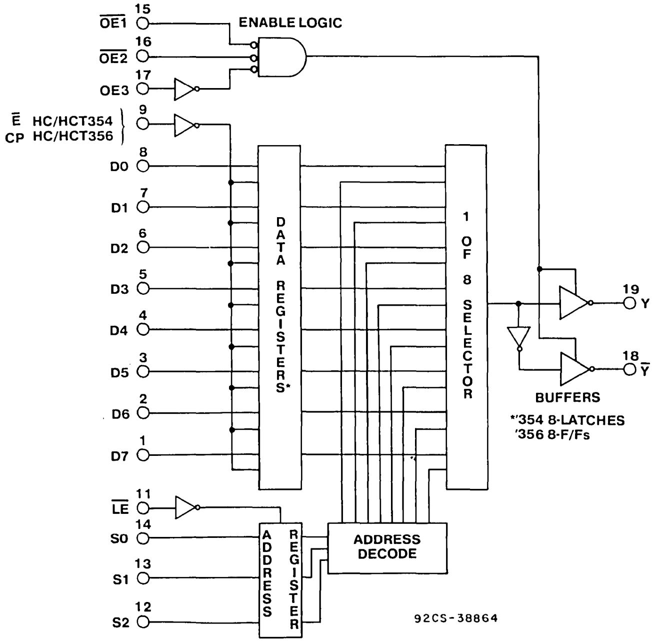
Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; @ $V_{CC} = 5\ V$
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8\ V$ *Max.,* $V_{IH} = 2\ V$ *Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356



Block Diagram

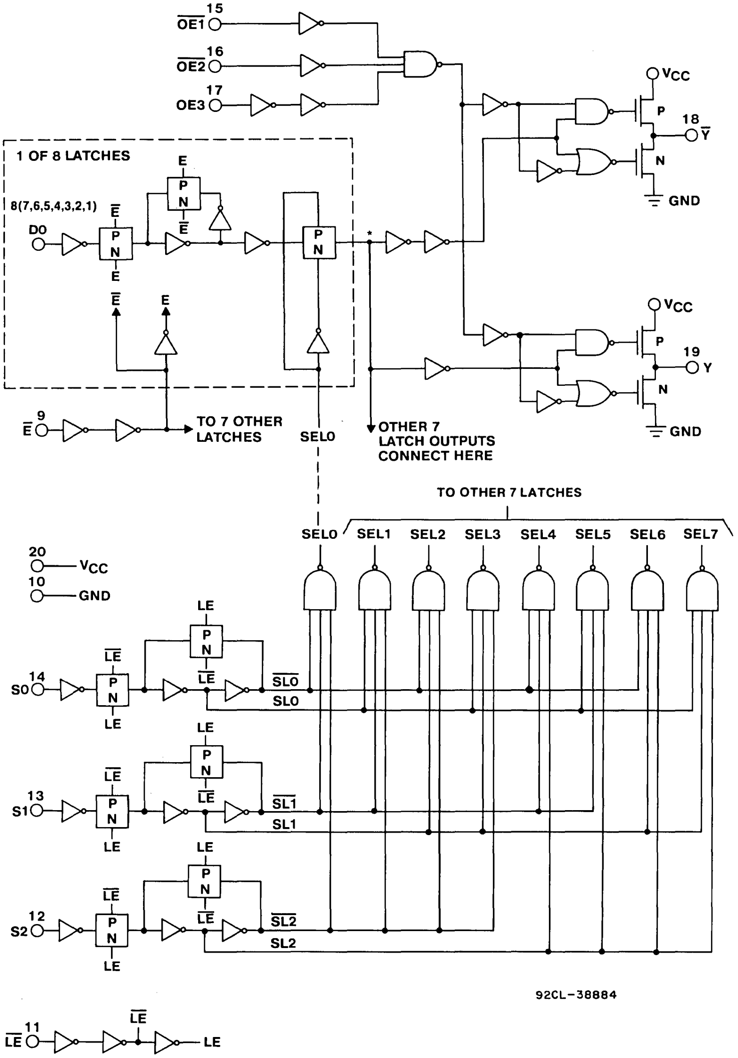
TRUTH TABLE

Inputs								Outputs	
Select #			Enable Data 'HC354 'HCT354	Clock 'HC356 'HCT356	Output Enables				
S2	S1	S0	E	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	Y	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

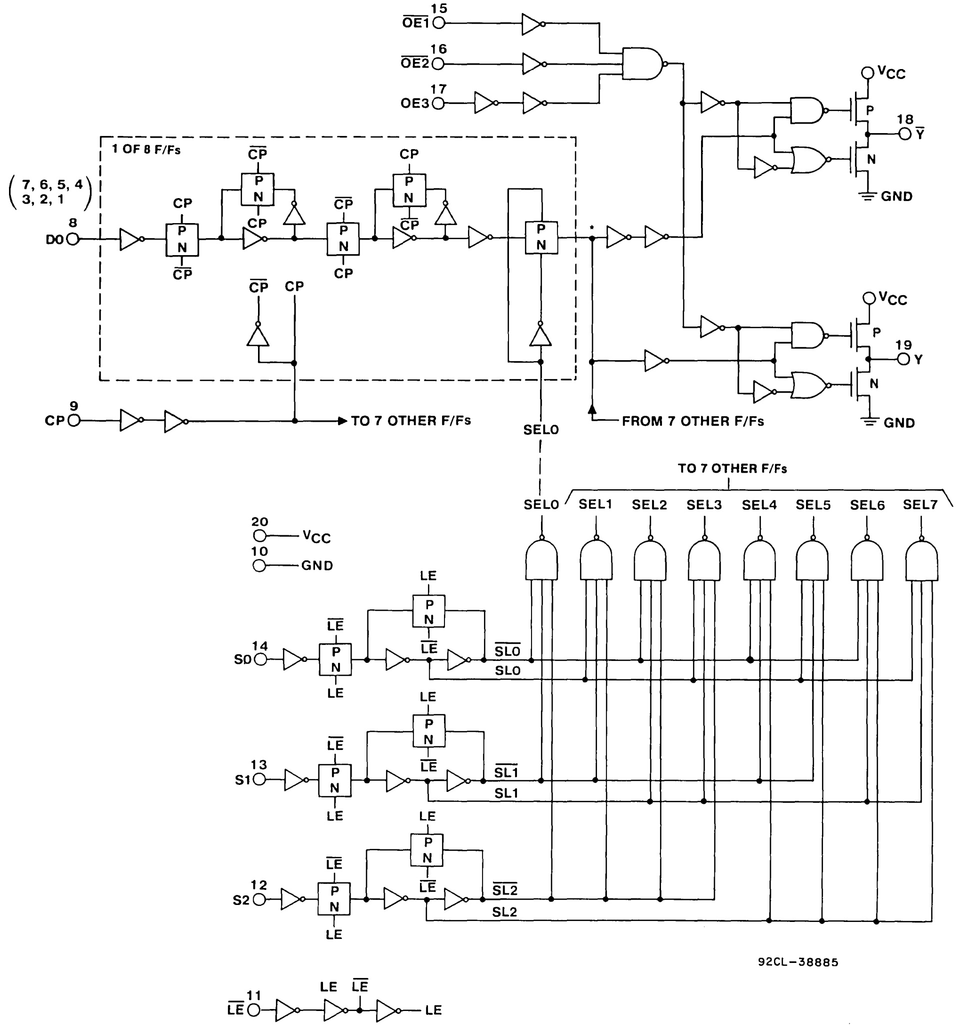
Notes

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0 ... D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of HC356
$D0_n$ ... $D7_n$ = the level of steady state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
This column shows the input address setup with $\overline{LE}$ low

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356



HC/HCT354 Logic Diagram



HC/HCT356 Logic Diagram

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC})	
(Voltages referenced to ground)	-0.5 to +7V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_I < -0.5$ V OR $V_I > 0.5$ V $+V_{CC}$)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC354/356/CD54HC354/356										CD74HCT354/356/CD54HCT354/356									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V_I V	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

HCT354 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE}1$, $\overline{OE}2$	0.80
OE3	0.25
$\overline{LE}$	0.25
$\overline{E}$	0.60

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HCT356 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE}1$, $\overline{OE}2$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns) — HC/HCT354

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay Dn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	18	20	ns
$\overline{E}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	21	23	ns
Sn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	25	ns
$\overline{LE}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	24	25	ns
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	13	13, 16	ns
Output Enabling Time	15	t_{PZL}, t_{PZH}	12, 13	14	ns
Power Dissipation Capacitance*	—	C_{PD}	90	92	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency,
C_L = output load capacitance.
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT354

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{E}$ pulse width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{LE}$ pulse width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set Up Times Dn → $\overline{E}$	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Sn → $\overline{LE}$	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Times Dn → $\overline{E}$	t_H	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	
Sn → $\overline{LE}$	t_H	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns) — HC/HCT354

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Dn → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	ns
		4.5	—	42	—	47	—	53	—	59	—	63	—	71	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
$\overline{E}$ → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	54	—	63	—	68	—	75	—	81	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Sn → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	260	—	—	—	325	—	—	—	390	—	—	ns
		4.5	—	52	—	59	—	65	—	74	—	78	—	89	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
$\overline{LE}$ → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
		4.5	—	58	—	63	—	73	—	79	—	87	—	94	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Output Disabling Time $\overline{OE}$n to Y, $\overline{Y}$	t_{PLZ} t_{PHZ}	2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	33	—	39	—	41	—	47	—	50	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
OE3 to Y, $\overline{Y}$		2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	39	—	39	—	49	—	47	—	59	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Enabling Time $\overline{OE}$n to Y, $\overline{Y}$	t_{PZL} t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	34	—	38	—	43	—	45	—	51	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
OE3 to Y, $\overline{Y}$		2	—	160	—	—	—	200	—	—	—	240	—	—	
		4.5	—	32	—	34	—	40	—	43	—	48	—	51	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-state Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns) — HC/HCT356

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay CP → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	22	ns
Sn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	25	ns
$\overline{LE}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	24	25	ns
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	13	13, 15	ns
Output Enabling Time	15	t_{PZL}, t_{PZH}	12, 13	14	ns
Power Dissipation Capacitance*	—	C_{PD}	51	52	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

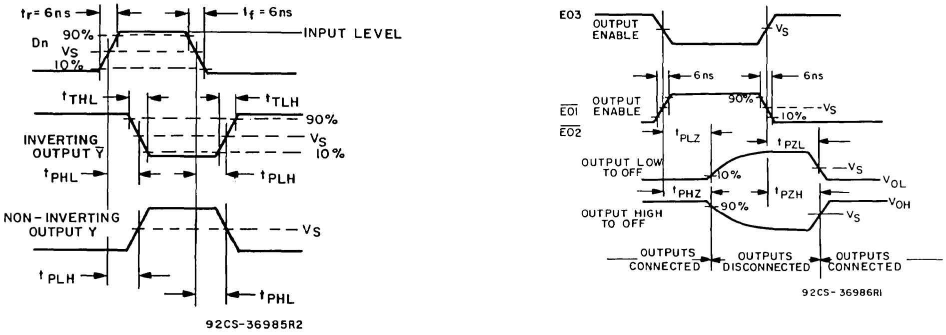
CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT356

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{LE}$ Pulse Width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set Up Times Dn → CP	t_{SU}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	7	—	5	—	9	—	5	—	11	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Sn → $\overline{LE}$	t_{su}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	7	—	5	—	9	—	5	—	11	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Hold Times Dn → CP	t_h	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	
Sn → $\overline{LE}$	t_h	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns) — HC/HCT356

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay: CP → $Y, \overline{Y}$	t_{PLH} t_{PHL}	2	—	255	—	—	—	320	—	—	—	385	—	—	ns
		4.5	—	51	—	51	—	64	—	64	—	77	—	77	
		6	—	43	—	—	—	54	—	—	—	65	—	—	
Sn → $Y, \overline{Y}$	t_{PLH} t_{PHL}	2	—	260	—	—	—	325	—	—	—	390	—	—	ns
		4.5	—	52	—	59	—	65	—	74	—	78	—	89	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
$\overline{LE}$ → $Y, \overline{Y}$	t_{PLH} t_{PHL}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
		4.5	—	58	—	63	—	73	—	79	—	87	—	94	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Output Disabling Time $\overline{OE}1$, $\overline{OE}2$ to $Y, \overline{Y}$	t_{PLZ}	2 4.5 6	—	155	—	—	—	195	—	—	—	235	—	—	ns
			—	31	—	33	—	39	—	41	—	47	—	50	
			—	26	—	—	—	33	—	—	—	40	—	—	
OE3 to $Y, \overline{Y}$	t_{PHZ}		—	155	—	—	—	195	—	—	—	235	—	—	
			—	31	—	37	—	39	—	46	—	47	—	56	
			—	26	—	—	—	33	—	—	—	40	—	—	
Output Enabling Time $\overline{OE}1$, $\overline{OE}2$ to $Y, \overline{Y}$	t_{PZL}	2 4.5 6	—	150	—	—	—	190	—	—	—	225	—	—	ns
			—	30	—	34	—	38	—	43	—	45	—	51	
			—	26	—	—	—	33	—	—	—	38	—	—	
OE3 to $Y, \overline{Y}$	t_{PZH}		—	160	—	—	—	200	—	—	—	240	—	—	
			—	32	—	34	—	40	—	43	—	48	—	51	
			—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-state Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 1 — Transition times and propagation delay times.

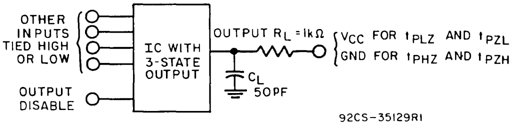


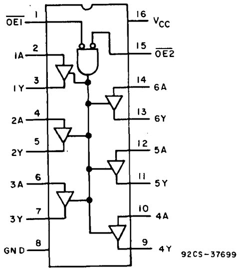
Fig. 2 — Three-state propagation delay test circuit.

CD54/74HC365, CD54/74HCT365
CD54/74HC366, CD54/74HCT366

File Number **1539**

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT



CD54/74HC365, HCT365

Hex Buffer/Line Driver, 3-State Non-Inverting and Inverting

Type Features:

- *Buffered Inputs*
- *High Current Bus Driver Outputs*
- *Typical Propagation Delay t_{PLH}, t_{PHL} = 8 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC365/366 and CD54/74HCT365/366 silicon gate CMOS 3-STATE buffers are general purpose high speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD54/74HC, HCT365 are non-inverting buffers, whereas the CD54/74HC, HCT366 are inverting buffers. These devices have two 3-State control inputs ($\overline{OE1}$ and $\overline{OE2}$) which are NORed together to control all six gates.

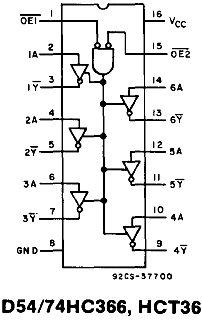
The CD54/74HCT365 and CD54/74HCT366 logic families are speed, function, and pin compatible with the standard 54LS/74LS logic family.

The CD54HC365/366 and CD54HCT365/366 are supplied in 16-lead hermetic dual-in-line packages (F suffix). The CD74HC365/366 and CD74HCT365/366 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30%; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT



CD54/74HC366, HCT366

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V)	±35 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}):	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

TRUTH TABLES

Inputs			Outputs
$\overline{OE_1}$	$\overline{OE_2}$	A	Y
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

CD54/74HC, HCT365

Inputs			Outputs
$\overline{OE_1}$	$\overline{OE_2}$	A	Y
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

CD54/74HC, HCT366

L = LOW voltage level
H = HIGH voltage level
X = Don't Care
Z = High impedance (off) state

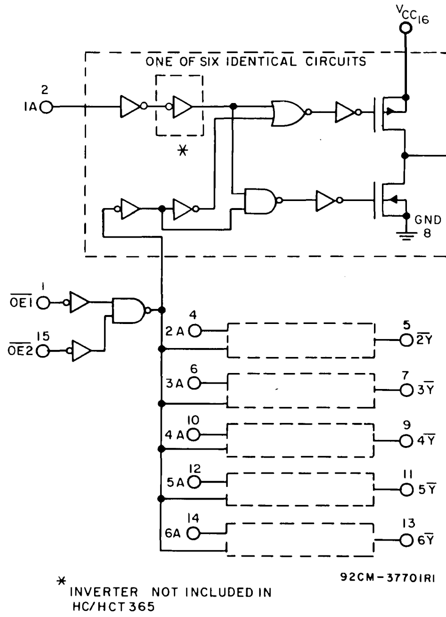


Fig. 1 - Logic diagram for the HC/HCT365 and HC/HCT366. (Outputs for HC/HCT365 are complements of those shown, i.e., 1Y, 2Y etc.)

CD54/74HC365, CD54/74HCT365
CD54/74HC366, CD54/74HCT366

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC365/366/CD54HC365/366										CD74HCT365/366/CD54HCT365/366									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
$\overline{\text{OE1}}$	0.6
All Others	0.55

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:* CD54/74HC Types CD54/74HCT Types	 2 4.5	 6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: CD74 Types CD54 Types	 -40 -55	 +85 +125	°C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	 0 0 0	 1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C, Input t_r, t_f = 6 ns)

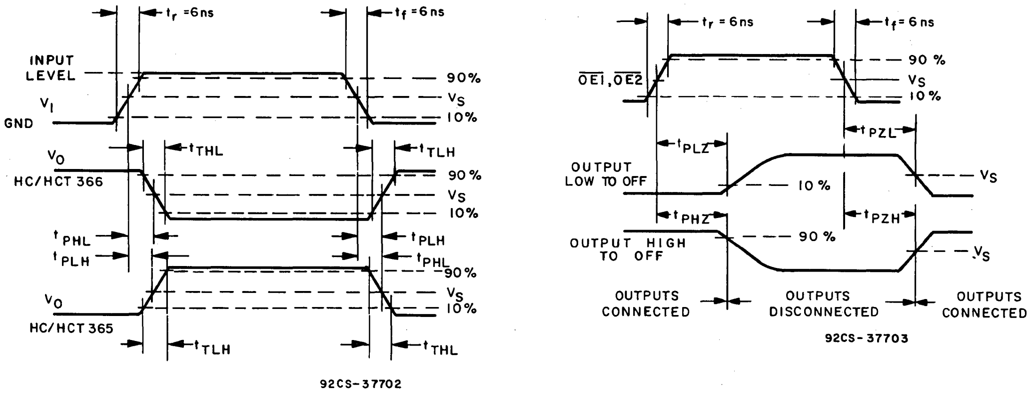
CHARACTERISTIC	SYMBOL	TYPICAL				UNITS
		365		366		
		HC	HCT	HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	8	9	9	11	ns
Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	12	14	12	14	ns
Power Dissipation Capacitance *	C_{PD}	40	42	40	42	pF

* C_{PD} is used to determine the dynamic power consumption, per buffer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency. C_L = output load capacitance. V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	105	—	—	—	130	—	—	—	160	—	—	ns
Data to Outputs	t_{PHL}	4.5	—	21	—	25	—	26	—	31	—	32	—	38	
HC/HCT365		6	—	18	—	—	—	22	—	—	—	27	—	—	
Propagation Delay	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
Data to Outputs	t_{PHL}	4.5	—	22	—	27	—	28	—	34	—	33	—	41	
HC/HCT366		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay	t_{PZH}, t_{PZL},	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Output Enable and	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
Disable to Outputs		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC365, CD54/74HCT365
CD54/74HC366, CD54/74HCT366



	54/74HC	54/74HCT
Input Level	Vcc	3 V
Switching Voltage, Vs	50% Vcc	1.3 V

Fig. 2 - Transition times and propagation delay times.

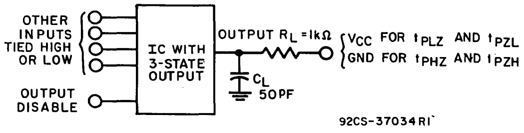


Fig. 3 - Three-stage propagation delay test circuit.

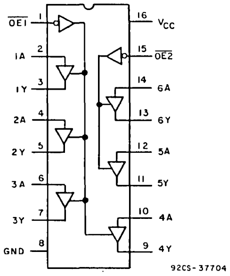
File Number **1538**

**Advance Information/
Preliminary Data**

CD54/74HC367, CD54/74HCT367
CD54/74HC368, CD54/74HCT368

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC367, HCT367

Hex Buffer/Line Driver, 3-State

Non-Inverting and Inverting

Type Features:

- *Buffered inputs*
- *High current bus driver outputs*
- *Two independent 3-state enable controls*
- *Typical propagation delay t_{PHL}, t_{PLH} = 8 ns @ V_{cc} = 5 V, C_L = 15 pF*

The RCA-CD54/74HC367, 368 and CD54/74HCT367, 368 silicon gate CMOS 3-state buffers are general-purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high-speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD54/74HC, HCT367 are non-inverting buffers, whereas the CD54/74HC, HCT368 are inverting buffers. These devices have two output enables, one enable (OE1) controls 4 gates and the other (OE2) controls the remaining 2 gates.

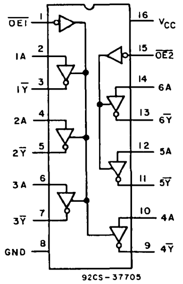
The CD54/74HCT367 and CD54/74HCT368 logic families are speed, function, and pin compatible with the standard 54LS/74LS logic family.

The CD54HC367 and CD54HCT367 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC367 and CD74HCT367 are in 16-lead dual-in-line plastic packages (E suffix), also in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30%; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *I_{IL}, $I_{IH} \leq 1$ μA @ V_{OL}, V_{OH}*

FUNCTIONAL DIAGRAM



CD54/74HC368, HCT368

CD54/74HC367, CD54/74HCT367
CD54/74HC368, CD54/74HCT368

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{cc}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V)	±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to −125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

TRUTH TABLES

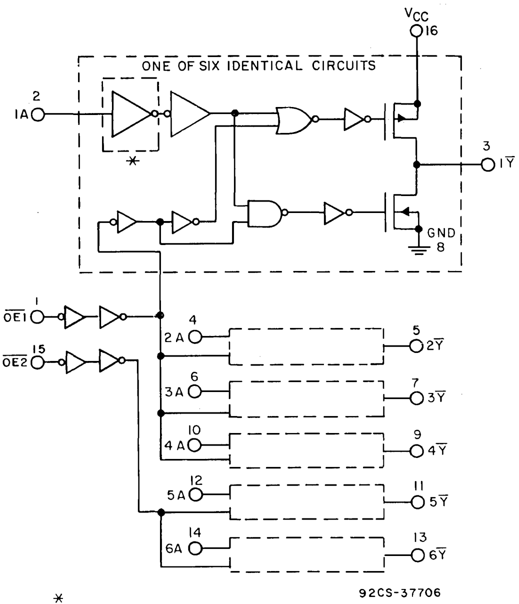
Inputs		Outputs
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	(Z)

CD54/74HC, HCT367

Inputs		Outputs
$\overline{OE}$	A	Y
L	L	H
L	H	L
H	X	(Z)

CD54/74HC, HCT368

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.



*INVERTER NOT INCLUDED IN HC/HCT 367

Fig. 1 - Logic diagram for HC/HCT367 and HC/HCT368. (Outputs for HC/HCT367 are complements of those shown, i.e., 1Y, 2Y, etc.).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC367/368/CD54HC367/368										CD74HCT367/368/CD54HCT367/368										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-7.8	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1		µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10		µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
$\overline{OE1}$	0.6
ALL OTHERS	0.55

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC367, CD54/74HCT367
CD54/74HC368, CD54/74HCT368

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A=Full Package Temperature Range)			
V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, C_L=15 pF, T_A=25° C, Input t_r,t_f=6 ns)

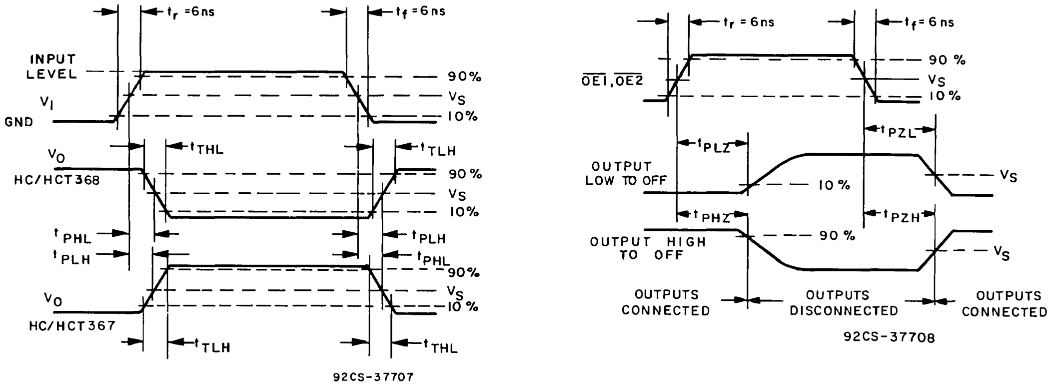
CHARACTERISTIC	SYMBOL	TYPICAL				UNITS
		367		368		
		HC	HCT	HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	8	9	9	11	ns
Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	12	14	12	14	ns
Power Dissipation Capacitance *	C_{PD}	40	42	40	42	pF

*C_{PD} is used to determine the dynamic power consumption, per buffer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	105	—	—	—	130	—	—	—	160	—	—	ns
Data to Outputs	t_{PHL}	4.5	—	21	—	25	—	26	—	31	—	32	—	38	
HC/HCT367		6	—	18	—	—	—	24	—	—	—	27	—	—	
Propagation Delay	t_{PLH}	2	—	105	—	—	—	130	—	—	—	160	—	—	ns
Data to Outputs	t_{PHL}	4.5	—	21	—	30	—	26	—	38	—	32	—	45	
HC/HCT368		6	—	18	—	—	—	24	—	—	—	27	—	—	
Propagation Delay	t_{PZH}, t_{PZL},	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Output Enable & Disable	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
to Outputs		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC367, CD54/74HCT367
CD54/74HC368, CD54/74HCT368



Input Level	54/74HC	54/74HCT
	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.

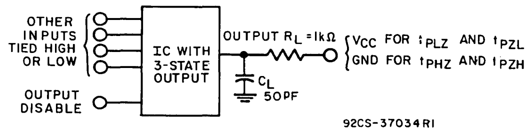
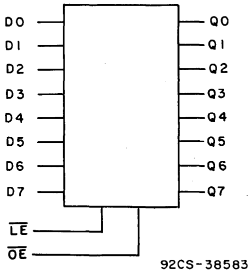


Fig. 3 - Three-state propagation delay test circuit.

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

File Number **1679**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State Output

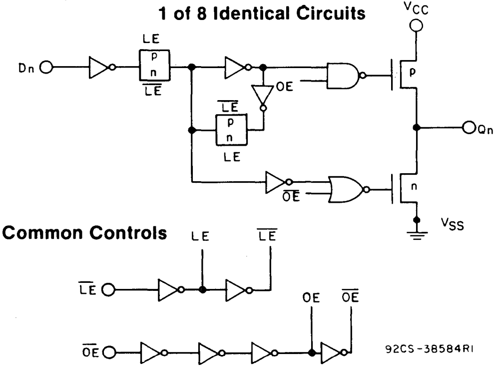
Type Features:

- *Common latch enable control*
- *Common 3-state output enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 12 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C (Data to Output for HC373)*

The RCA CD54/74HC373/573 and CD54/74HCT373/573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD54/74HCT373/573 are functionally as well as pin compatible with the standard 54/74LS373 and 573.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT373/573 are supplied in 20 lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT373/573 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).


1 of 8 Identical Circuits

Common Controls

Fig. 1 - Logic diagram.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

Output Enable	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

Note:
L = Low voltage level
H = High voltage level
X = Don't Care
Z = High Impedance State
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

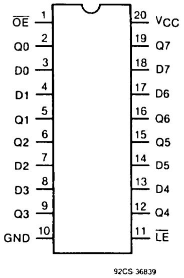
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} +0.5$ V) .... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): .... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

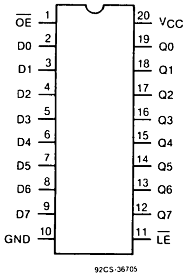
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



CD54/74HC373, CD54/74HCT373
TERMINAL ASSIGNMENT



CD54/74HC573, CD54/74HCT573
TERMINAL ASSIGNMENT

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC373/CD54HC373 CD74HC573/CD54HC573										CD74HCT373/CD54HCT373 CD74HCT573/CD54HCT573									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT373	HCT573
$\overline{OE}$	1.5	1.25
Dn	0.4	0.3
LE	0.6	0.65

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay Data to Qn Output (HC/HCT373) (Fig. 3)	t_{PLH} t_{PHL}	15	12	13	ns
Data to Qn Output (HC/HCT573) (Fig. 3)	t_{PLH} t_{PHL}	15	14	17	ns
$\overline{LE}$ to Qn Output (Fig. 4)	t_{PLH} t_{PHL}	15	14	14	ns
Output Enabling Time (Fig. 6, 7)	t_{PZL} t_{PZH}	15	12	14	ns
Output Disabling Time (Fig. 6, 7)	t_{PLZ} t_{PHZ}	15	12	14	ns
Power Dissipation Capacitance (HC/HCT573, 373)	C_{PD}*	—	51	53	pF

*C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship;
P_D (total power per latch) = $V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency,
C_L = output load capacitance, V_{CC} = supply voltage

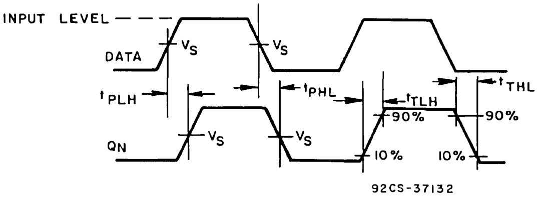
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{LE}$ Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
(Fig. 3)	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Data to $\overline{LE}$ 573	4.5	10	—	13	—	13	—	16	—	15	—	20	—	
(Fig. 4)	6	9	—	—	—	11	—	—	—	13	—	—	—	
Set-up Time t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
Data to $\overline{LE}$ 373	4.5	10	—	13	—	13	—	16	—	15	—	20	—	
(Fig. 4)	6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Time t_H	2	40	—	—	—	50	—	—	—	60	—	—	—	ns
Data to $\overline{LE}$ 573	4.5	8	—	10	—	10	—	13	—	12	—	15	—	
(Fig. 4)	6	7	—	—	—	9	—	—	—	10	—	—	—	
Hold Time t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
Data to $\overline{LE}$ 373	4.5	5	—	10	—	5	—	13	—	5	—	15	—	
(Fig. 4)	6	5	—	—	—	5	—	—	—	5	—	—	—	

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

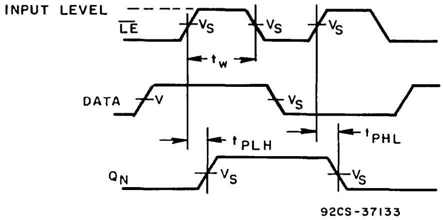
SWITCHING CHARACTERISTICS (Input t_r, t_f = 6 ns, C_L = 50 pF)

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Data to Qn	t_{PHL}	4.5	—	30	—	32	—	38	—	40	—	45	—	48	
(Fig. 2) HC/HCT373		6	—	26	—	—	—	33	—	—	—	38	—	—	
Data to Qn	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
(Fig. 2)	t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	
HC/HCT573		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{LE}$ to Qn	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
(Fig. 3)		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enabling	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Time	t_{PZH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
(Figs. 5 & 6)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Disabling	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Time	t_{PHZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
(Figs. 5 & 6)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
(Fig. 2)		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



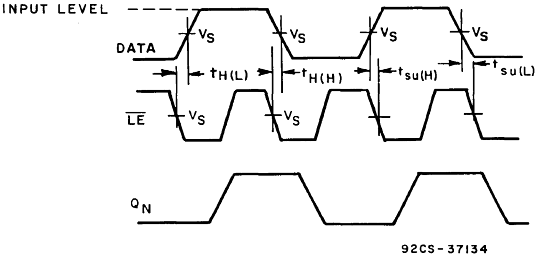
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 2 - Data to Q_n output propagation delays and output transition times.



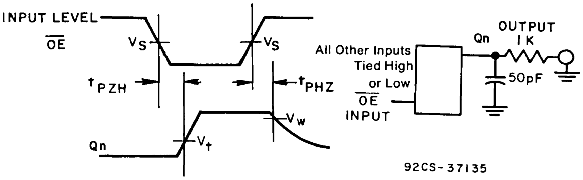
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 - Latch enable propagation delays.



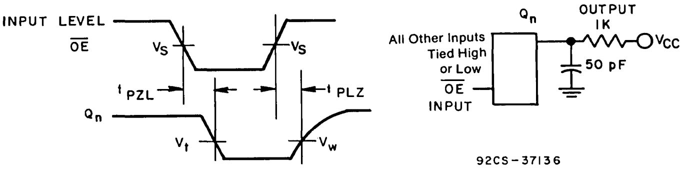
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 - Latch enable prerequisite times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	90% V_{CC}	90% V_{CC}

Fig. 5 - Three-state propagation delays.



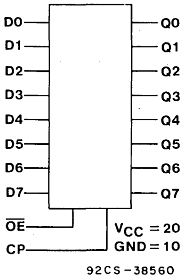
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	10% V_{CC}	10% V_{CC}

Fig. 6 - Three-state propagation delays.

CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

File Number **1663**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

Type Features:

- *Common 3-State Output Enable Control*
- *Buffered Inputs*
- *3-State Outputs*
- *Bus Line Driving Capability*
- *Typical Propagation Delay (Clock to Q) = 15 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA CD54/74HC374/574 and CD54/74HCT374/574 are Octal D-Type Flip-Flops with 3-State Outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When Output Enable ($\overline{OE}$) is HIGH the outputs will be in the high impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT374/574 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD54HC/HCT374/574 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead plastic dual-in-line surface mount plastic packages (M suffix). The CD54HC/HCT374/574 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

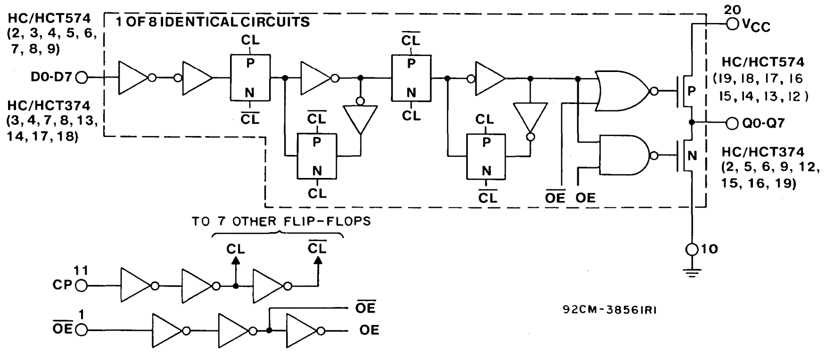


Fig. 1 - Logic diagram.

CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$V)	±35mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE			
INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

HC/HCT374,574

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.
Z = high impedance

CD54/74HC374, CD54/74HCT374 CD54/74HC574, CD54/74HCT574

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC374/CD54HC374 CD74HC574/CD54HC574										CD74HCT374/CD54HCT374 CD74HCT574/CD54HCT574									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*	
	HCT374	HCT574
D0-D7	0.3	0.4
CP	0.9	0.75
$\overline{OE}$	1.3	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Clock to Q	t_{PLH} t_{PHL}	15	15	15	ns
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	15	11	11	ns
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	15	12	12	ns
Max Clock Frequency	f_{max}	15	60	60	MHz
Power Dissipation Capacitance	C_{PD}*	—	39	47	pF

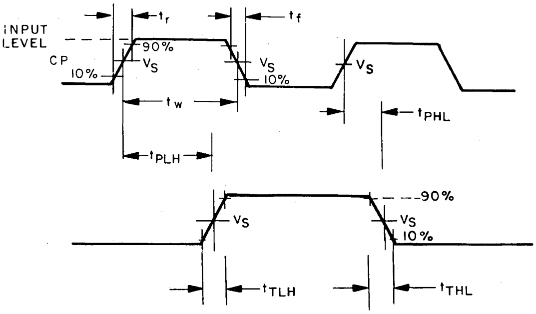
*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L$ where
f_i = input frequency,
f_o = output frequency,
C_L = output load capacitance
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC} V	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock		2	6	—	—	—	5	—	—	—	4	—	—	—	
Frequency	f_{MAX}	4.5	30	—	30	—	25	—	25	—	20	—	20	—	MHz
		6	35	—	—	—	29	—	—	—	23	—	—	—	
		2	80	—	—	—	100	—	—	—	120	—	—	—	
Clock Pulse Width	t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
Fig. 2		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time		2	60	—	—	—	75	—	—	—	90	—	—	—	
Data to Clock		4.5	12	—	12	—	15	—	15	—	18	—	18	—	ns
Fig. 3	t_{SU}	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time		2	5	—	—	—	5	—	—	—	5	—	—	—	
Data to Clock		4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 3	t_H	6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

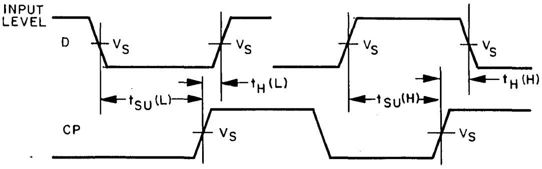
CHARACTERISTIC		V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
Clock to Output	t_{PHL}	4.5	—	33	—	33	—	41	—	41	—	50	—	50	ns
Fig. 2		6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay	t_{PLZ}	2	—	135	—	—	—	170	—	—	—	205	—	—	
Output Disable to Q	t_{PHZ}	4.5	—	27	—	28	—	34	—	35	—	41	—	42	ns
Fig. 4		6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Enable to Q	t_{PZH}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
Fig. 4		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
Fig. 2		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-38404

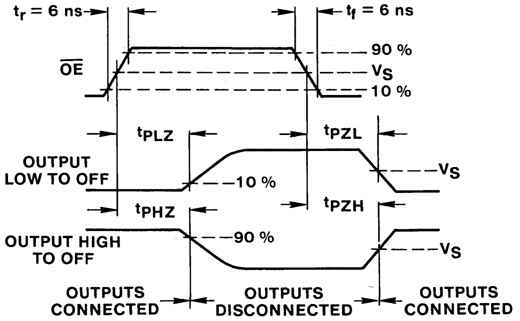
Fig. 2 — Clock to output delays and clock pulse width.



92CS- 36954RI

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

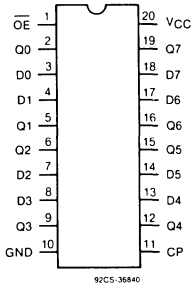
Fig. 3 — Data set-up and hold times.



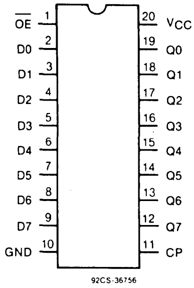
92CS-38562

	54/74HC	54/74HCT
Input Level	**V_{CC}**	**3 V**
Switching Voltage, V_S	**50% V_{CC}**	**1.3 V**

Fig. 4 — Transition times and propagation delay times.



CD54/74HC, HCT374 Types TERMINAL ASSIGNMENT

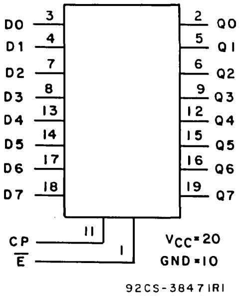


CD54/74HC, HCT574 Types TERMINAL ASSIGNMENT

File Number **1675**

CD54/74HC377
CD54/74HCT377

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop with Data Enable

Type Features:
- *Buffered common clock*
- *Buffered inputs*
- *Typical propagation delay = 17ns @ C_L = 15pF, V_{CC} = 5 V, T_A = 25°C*
- *60 MHz typical maximum clock frequency @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC377 and CD54/74HCT377 are octal D-type flip-flops with a buffered clock (CP) common to all eight flip-flops. All the flip-flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable (E̅) is LOW.

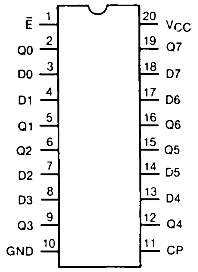
The CD54HC377 and CD54HCT377 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC377 and CD74HCT377 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	E̅	Dn	Qn
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

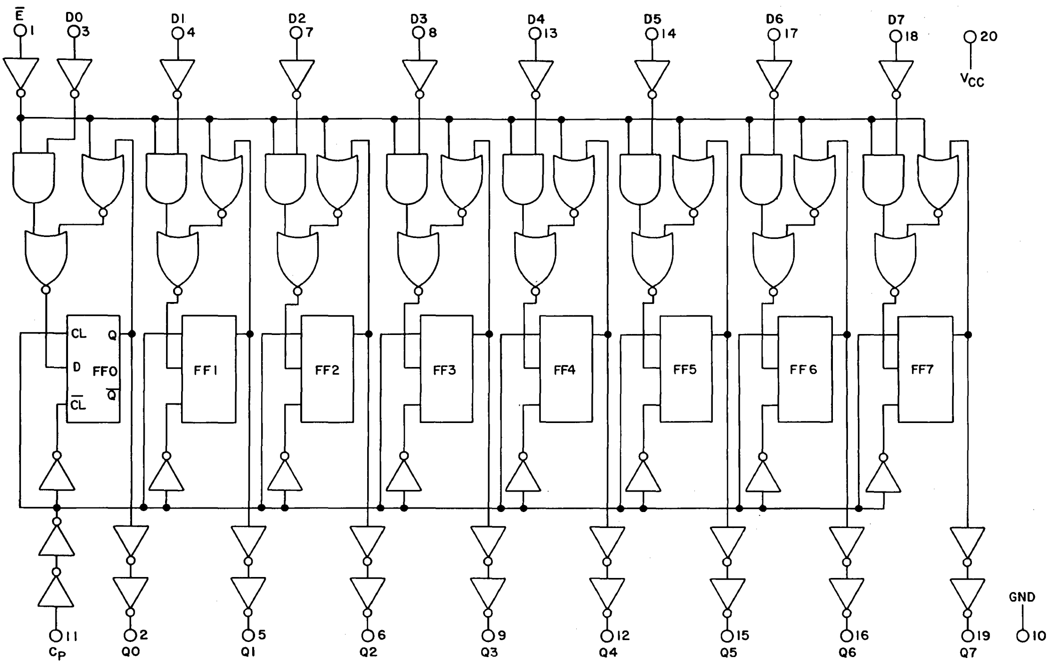
H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑= LOW-to-HIGH clock transition.

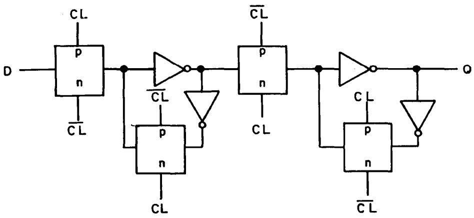
Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}= 30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC377
CD54/74HCT377





Flip-Flop Detail

92CL-38576R1

Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125° C
PACKAGE TYPE E, M .... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			V
CD54/74HC Types	2	6	
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC377
CD54/74HCT377

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC377/CD54HC377										CD74HCT377/CD54HCT377										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{E}$	1.5
CP	0.5
All Dn Inputs	0.25

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Maximum Clock Frequency	15	f_{max}	60	50	MHz
Propagation Delay CP ⟶ Q	15	t_{PLH} t_{PHL}	14	16	ns
Power Dissipation Capacitance*	—	C_{PD}	31	35	pF

*C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_O)$ where:
f_i = input frequency
f_o = output frequency
C_L = output load capacitance.
V_{CC} = supply voltage.

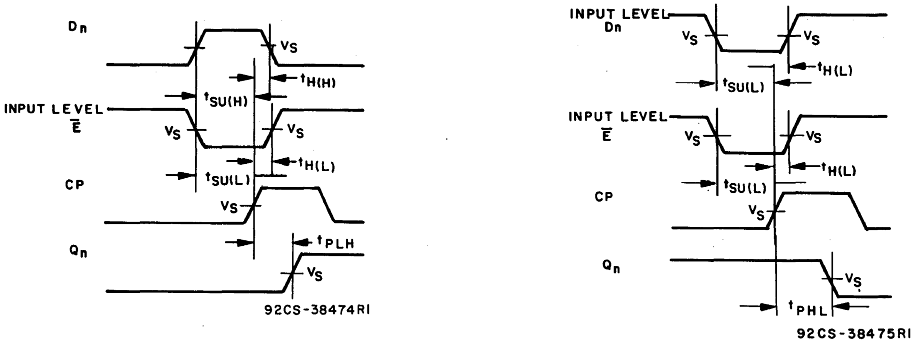
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
Frequency f_{max}	4.5	30	—	25	—	25	—	20	—	20	—	16	—	
	6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
width t_W	4.5	16	—	20	—	20	—	25	—	24	—	30	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
$\overline{E}$, Data to CP t_{SU}	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time,	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
Data to CP t_H	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Hold Time	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
$\overline{E}$ to CP t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
CP to Q t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
Transition Time t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC377
CD54/74HCT377



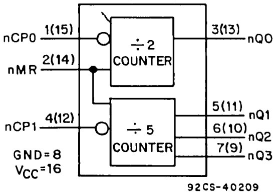
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Setup and hold times and propagation delay times.

File Number **1838**

CD54/74HC390
CD54/74HCT390

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Decade Ripple Counter

Type Features:

- *Two BCD decade or bi-quinary counters*
- *One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100*
- *Two master reset inputs to clear each decade counter individually*

The RCA-CD54/74HC390 and CD54/74HCT390 dual 4-bit decade ripple counters are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL). These devices are divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clock inputs (n$\overline{CP0}$ and n$\overline{CP1}$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. Each section is triggered by the HIGH-to-LOW transition of the input pulses (n$\overline{CP0}$ and n$\overline{CP1}$).

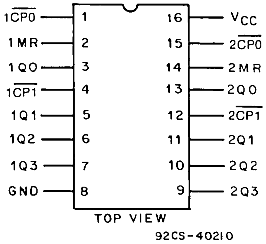
For BCD decade operation, the nQ0 output is connected to the n$\overline{CP1}$ input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the n$\overline{CP0}$ input and nQ0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active-HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clock and sets the four outputs LOW.

The CD54HC390 and CD54HCT390 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC390 and CD74HCT390 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1$ *µA @* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC390
CD54/74HCT390

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A= -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A= +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

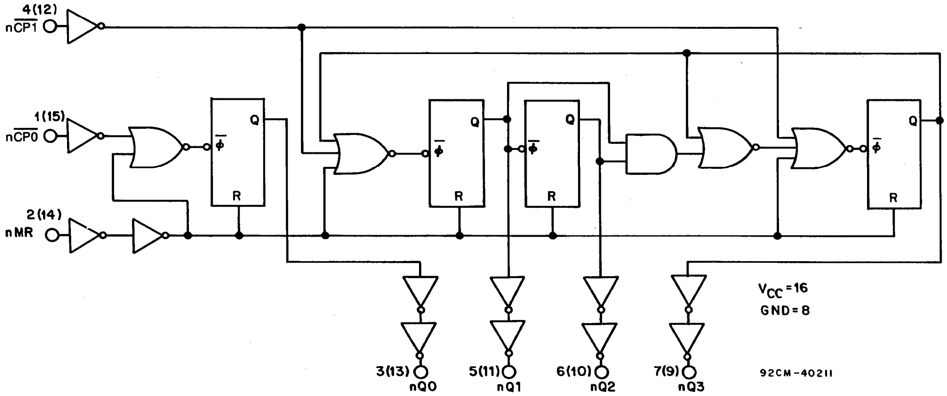


Fig. 1 - Logic diagram, one-half of HC/HCT390.

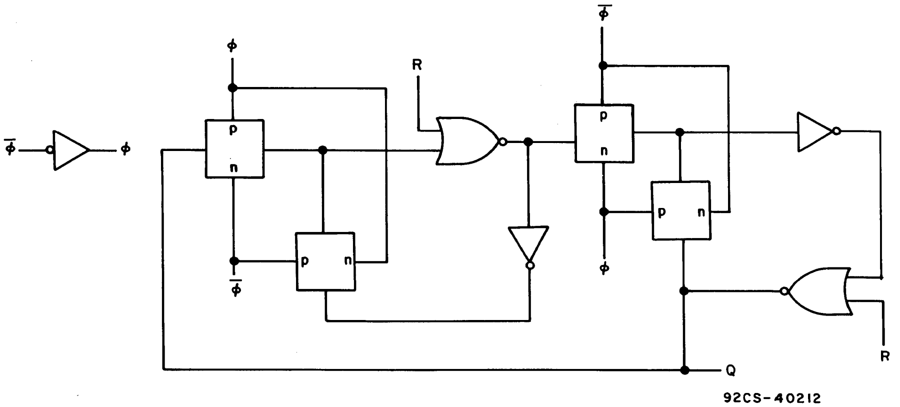


Fig. 2 - Flip-flop logic detail.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE

INPUTS		ACTION
CP	MR	
_/‾	L	NO CHANGE
‾_	L	COUNT
X	H	ALL Qs LOW

H = HIGH voltage level
L = LOW voltage level
X = Don't Care
_/‾ = LOW-to-HIGH ϕ transition
‾_ = HIGH-to-LOW ϕ transition

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note:
Output nQ0 connected to $n\overline{CP1}$ with counter input on $n\overline{CP0}$.

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note:
Output nQ3 connected to $n\overline{CP0}$ with counter input on $n\overline{CP1}$.

CD54/74HC390
CD54/74HCT390

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC390/CD54HC390										CD74HCT390/CD54HCT390										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$n\overline{CP0}$	0.45
$n\overline{CP1}$, MR	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r,t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay	t_{PLH} t_{PHL}	15			ns
n$\overline{\text{CP0}}$ to Q0 Output			14	17	
n$\overline{\text{CP1}}$ to Q3			15	18	
MR to Qn Output	t_{PHL}		16	18	
Power Dissipation Capacitance*	C_{PD}	—	28	32	pF

*C_{PD} is used to determine the dynamic power consumption, per counter.
PD = C_{PD} V_{CC}^2 f_i + Σ (C_L V_{CC}^2 f_o) where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	ns
		4.5	30	—	27	—	24	—	22	—	20	—	18	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width n$\overline{\text{CP0}}$, n$\overline{\text{CP1}}$	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	19	—	20	—	24	—	24	—	29	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time	t_{REM}	2	70	—	—	—	90	—	—	—	105	—	—	—	
		4.5	14	—	15	—	18	—	19	—	21	—	22	—	
		6	12	—	—	—	15	—	—	—	18	—	—	—	
Reset Pulse Width	t_w	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	13	—	13	—	16	—	15	—	20	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	

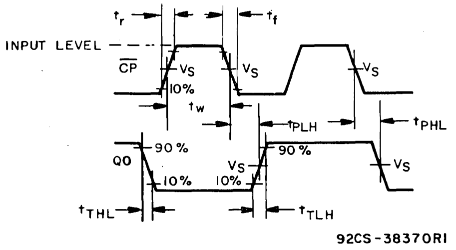


Fig. 3 - Input pulse pre-requisite, propagation-delay, and output-transition times.

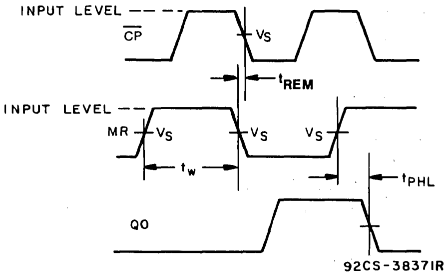


Fig. 4 - Master-Reset pre-requisite and propagation-delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

CD54/74HC390
CD54/74HCT390

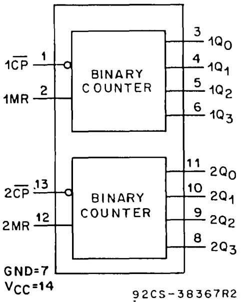
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC	V_{CC} (V)	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Time: t_{PLH} t_{PHL} n$\overline{CP0}$ to nQ0	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	4.5	—	35	—	40	—	44	—	50	—	53	—	60	
	6	—	30	—	—	—	37	—	—	—	45	—	—	
n$\overline{CP1}$ to nQ1	2	—	185	—	—	—	230	—	—	—	280	—	—	
	4.5	—	37	—	43	—	46	—	51	—	56	—	65	
	6	—	31	—	—	—	39	—	—	—	48	—	—	
n$\overline{CP1}$ to nQ2	2	—	245	—	—	—	305	—	—	—	370	—	—	
	4.5	—	49	—	55	—	61	—	69	—	74	—	83	
	6	—	42	—	—	—	52	—	—	—	63	—	—	
n$\overline{CP1}$ to nQ3	2	—	180	—	—	—	225	—	—	—	270	—	—	
	4.5	—	36	—	42	—	45	—	53	—	54	—	63	
	6	—	31	—	—	—	38	—	—	—	46	—	—	
n$\overline{CP0}$ to nQ2 (nQ0 connected to n$\overline{CP1}$)	2	—	365	—	—	—	455	—	—	—	550	—	—	
	4.5	—	73	—	84	—	91	—	105	—	110	—	126	
	6	—	62	—	—	—	77	—	—	—	94	—	—	
MR to Qn	2	—	190	—	—	—	240	—	—	—	285	—	—	
	4.5	—	38	—	42	—	48	—	53	—	57	—	63	
	6	—	32	—	—	—	41	—	—	—	48	—	—	
Output Transition Time t_{THL} t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

File Number **1653**

CD54/74HC393
CD54/74HCT393

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 4-Stage Binary Counter

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Negative-edge clocking*
- *Typical f_{MAX} = 60 MHz @ V_{cc} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC393 and CD54/74HCT393 are 4-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC393 and CD54HCT393 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC393 and CD74HCT393 are supplied in 14-lead dual-in-line plastic package (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
    V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
    I_{IN} ≤ 1 μA @ V_{OL}, V_{OH}

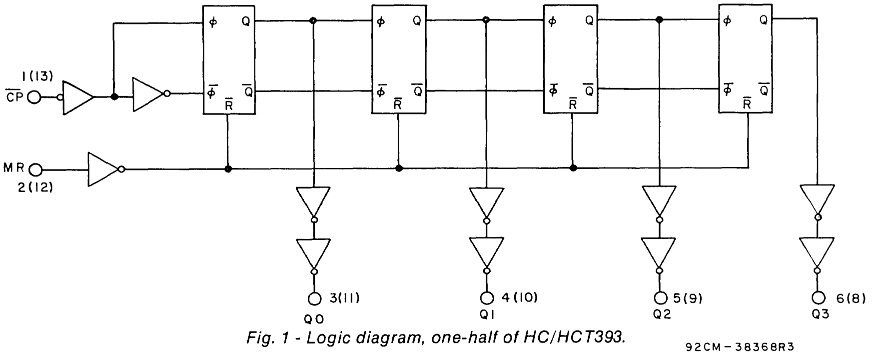


Fig. 1 - Logic diagram, one-half of HC/HCT393.

CD54/74HC393
CD54/74HCT393

MAXIMUM RATINGS, *Absolute-Maximum Values:*

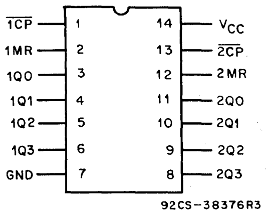
DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_o < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC393
CD54/74HCT393

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC393/CD54HC393										CD74HCT393/CD54HCT393									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
n$\overline{CP}$	0.4
nMR	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC393
CD54/74HCT393

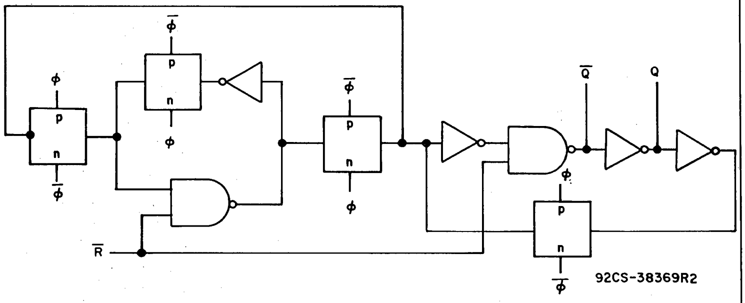


Fig. 2 - Flip-flop logic detail.

TRUTH TABLES

CP COUNT	OUTPUTS Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

CP	MR	OUTPUT
↑	L	NO CHANGE
↓	L	COUNT
X	H	L L L L

X = Don't Care

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical HC	HCT	Units
Propagation Delay n$\overline{CP}$ to nQ0 Output	t_{PLH} t_{PHL}	15	12	13	ns
Propagation Delay Qn to Qn + 1	t_{PLH} t_{PHL}	15	4	4	
Propagation Delay MR to Qn Output	t_{PHL}	15	11	13	
Power Dissipation Capacitance*	C_{PD}	—	20	21	pF

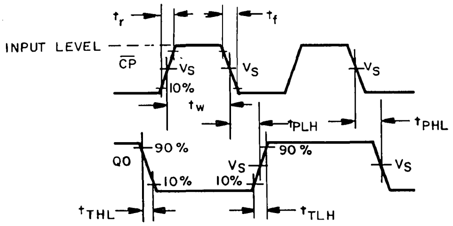
*C_{PD} is used to determine the power consumption.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_i/M)$ where: $M = 2^1, 2^2, 2^3, 2^4$
C_L=output load capacitance
fi=input frequency

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	VCC	25° C HC Min.	HC Max.	HCT Min.	HCT Max.	-40° C to +85° C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55° C to +125° C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	27	—	24	—	22	—	20	—	18	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	19	—	20	—	24	—	24	—	29	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Recovery Time	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

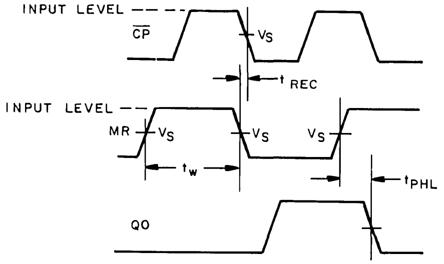
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time: Qn to Qn+1	t_{PLH}	2	—	45	—	—	—	55	—	—	—	70	—	—	ns
	t_{PHL}	4.5	—	9	—	12	—	11	—	15	—	14	—	18	
		6	—	8	—	—	—	9	—	—	—	12	—	—	
n$\overline{CP}$ to nQ0	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	26	—	32	—	38	—	40	—	45	—	48	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
n$\overline{CP}$ to nQ1	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	
	t_{PHL}	4.5	—	38	—	32	—	49	—	55	—	59	—	66	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
nCP to nQ2	t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
	t_{PHL}	4.5	—	48	—	50	—	60	—	70	—	72	—	84	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
n$\overline{CP}$ to nQ3	t_{PLH}	2	—	285	—	—	—	355	—	—	—	430	—	—	
	t_{PHL}	4.5	—	57	—	62	—	71	—	85	—	86	—	102	
		6	—	48	—	—	—	60	—	—	—	73	—	—	
MR to Qn	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
	t_{PHL}	4.5	—	27	—	32	—	24	—	40	—	41	—	48	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Output Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

92CS-38370R2

Fig. 3 - Clock pre-requisite, propagation-delay, and output-transition times.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50%	1.3 V

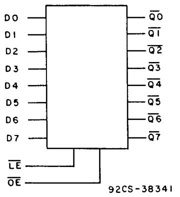
92CS-38371R2

Fig. 4 - Master-Reset pre-requisite and propagation-delay times.

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

File Number **1599**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Inverting Transparent Latch, 3-State Outputs

Type Features:

- *Common latch-enable control*
- *Common 3-state output-enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 13 ns @ $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25°C$ (Data to Output)*

The RCA CD54/74HC/HCT533/563 are high-speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

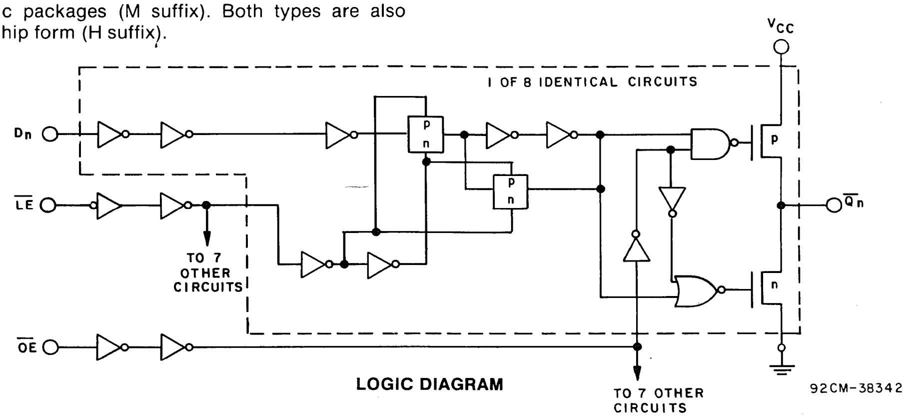
The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs will be in the high impedance state. The latch operation is independent of the state of the output enable.

The CD54/74HC533 and CD54/74HCT533 are identical in function to the CD54/74HC563 and CD54/74HCT563 but have different pinouts. The CD54/74HC533 and CD54/74HCT533 are similar to the CD54/74HC373 and CD54/74HCT373; the latter are non-inverting types.

The CD54HC/HCT533/563 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT533/563 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features

- *Fanout (Over Temperature Range):*
  - *Standard Outputs — 10 LSTTL Loads*
  - *Bus Driver Outputs — 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *$N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1$ μA @ V_{OL}, V_{OH}*



LOGIC DIAGRAM

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

MAXIMUM RATINGS, *Absolute-Maximum Values:*

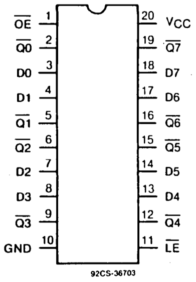
DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) .... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} +0.5$ V) .... ± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): .... ± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:

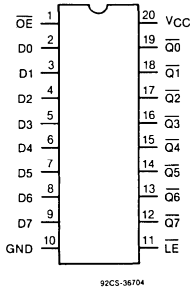
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



CD54/74HC533, CD54/74HCT533
TERMINAL ASSIGNMENT



CD54/74HC563, CD54/74HCT563
TERMINAL ASSIGNMENT

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC533/CD54HC533 CD74HC563/CD54HC563										CD74HCT533/CD54HCT533 CD74HCT563/CD54HCT563										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-7.8	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	VCC or Gnd	5.5	—	—	8	—	80	—	160		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DO — D7	0.15
$\overline{LE}$	0.30
$\overline{OE}$	0.55

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES				UNITS
			HC		HCT		
			533	563	533	563	
Propagation Delay Data to Qn Output Fig. 3	t_{PLH} t_{PHL}	15	13	12	14	12	ns
Propagation Delay $\overline{LE}$ to Qn Output Fig. 4	t_{PLH} t_{PHL}	15	14	13	16	14	
Output High Z to High Level, Fig. 6	t_{PZH}	15	12	12	14	14	
Output High Z to Low Level, Fig.7	t_{PZL}	15	12	12	14	14	
Output High Level to High Z, Fig. 6	t_{PHZ}	15	12	12	12	14	
Output Low Level to High Z, Fig. 7	t_{PLZ}	15	12	12	12	14	
Power Dissipation Capacitance	C_{PD}*	—	42	42	42	42	pF

*C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:
P_D (total power per latch) = $C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS														UNITS
			25° C				-40° C to +85° C				-55° to +125° C						
			HC		HCT		74HC		74HCT		54HC		54HCT				
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
$\overline{LE}$ Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—			ns
(Fig. 4)		4.5	16	—	16	—	20	—	20	—	24	—	24	—			
		6	14	—	—	—	17	—	—	—	20	—	—	—			
Set-up Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—			ns
Data to $\overline{LE}$		4.5	10	—	10	—	13	—	13	—	15	—	15	—			
(Fig. 5)		6	9	—	—	—	11	—	—	—	13	—	—	—			
Hold Time	t_H	2	35	—	—	—	45	—	—	—	55	—	—	—			ns
Data to $\overline{LE}$	533	4.5	7	—	8	—	9	—	10	—	11	—	12	—			
(Fig. 5)		6	6	—	—	—	8	—	—	—	7	—	—	—			
		2	4	—	—	—	4	—	—	—	4	—	—	—			ns
	563	4.5	4	—	5	—	4	—	5	—	4	—	5	—			
		6	4	—	—	—	4	—	—	—	4	—	—	—			

TRUTH TABLE

$\overline{\text{Output Enable}}$	$\overline{\text{Latch Enable}}$	Data	Q Output
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

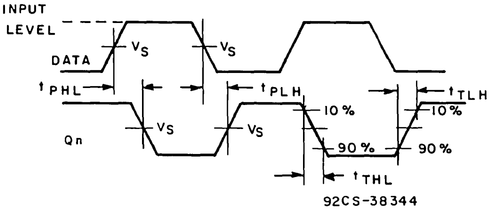
Note:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition
X = Don't care
Z = High impedance state

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

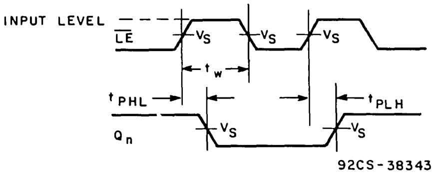
CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
			+25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	ns
Data to Qn	t_{PHL}	4.5	—	33	—	34	—	41	—	43	—	50	—	51	
	533	6	—	28	—	—	—	35	—	—	—	43	—	—	
	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
$\overline{LE}$ to Qn	t_{PHL}	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
	533	6	—	30	—	—	—	37	—	—	—	45	—	—	
Enable Times	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PZL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
	533	6	—	26	—	—	—	33	—	—	—	38	—	—	
Disable Times	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t_{PLZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
	533	6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Data to Qn	t_{PHL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
	563	6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	ns
$\overline{LE}$to Qn	t_{PHL}	4.5	—	33	—	35	—	41	—	44	—	50	—	53	
	563	6	—	28	—	—	—	35	—	—	—	43	—	—	
Enable and	t_{PZH}, t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
Disable Times	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
	563	6	—	26	—	—	—	33	—	—	—	38	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC533, CD54/74HCT533
CD54/74HC563, CD54/74HCT563



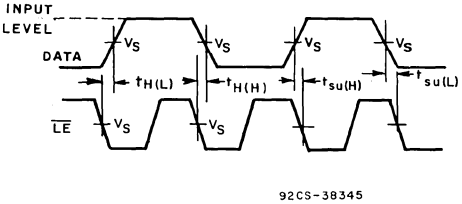
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 3 — Data to Q_n output propagation delays and output transition times.



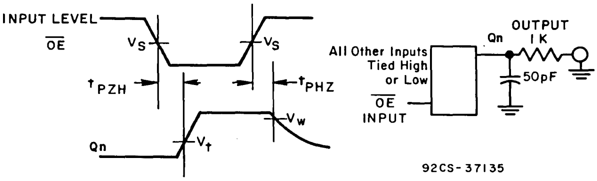
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 4 — Latch enable propagation delays.



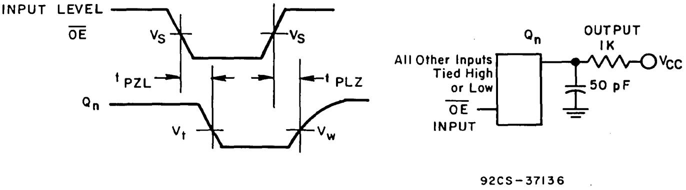
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 — Latch enable pre-requisite times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	90% V_{CC}	4.15 V

Fig. 6 - 3-state propagation delays.



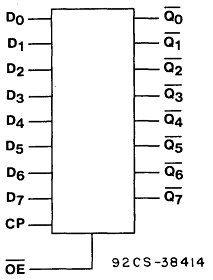
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V
V_t	50% V_{CC}	1.3 V
V_w	10% V_{CC}	0.45 V

Fig. 7 — 3-state propagation delays.

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

File Number **1640**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State, Inverting

Positive-Edge Triggered

Type Features:

- *Common 3-state output-enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capability*
- *Typical propagation delay = 13 ns @ V_{cc} = 5V, C_L = 15 pF, T_A = 25°C (clock to output)*

The RCA-CD54/74HC534, 564 and CD54/74HCT534, 564 are high speed OCTAL D-TYPE FLIP-FLOPS manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

The CD54/74HC534, 564 and CD54/74HCT534, 564 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the Q outputs on the positive going transition of the CLOCK input. When a high logic level is applied to the OUTPUT ENABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The CD54/74HCT logic family is speed, function, and pin compatible with the standard 54LS/74LS logic family.

The CD54HC and CD54HCT devices are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC and CD74HCT devices are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

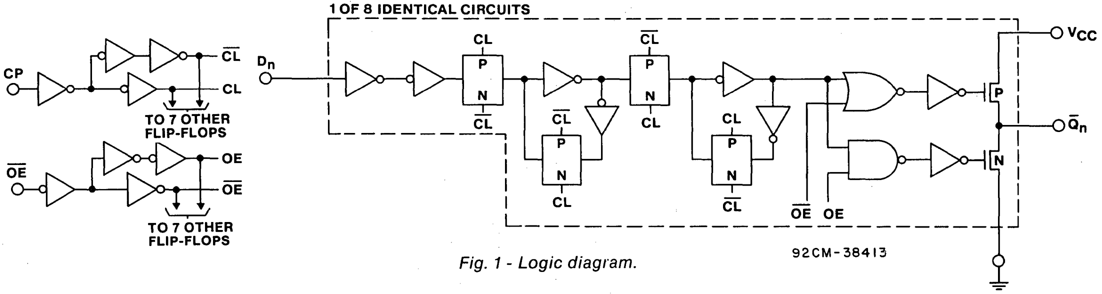


Fig. 1 - Logic diagram.

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V)	± 35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}):	± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

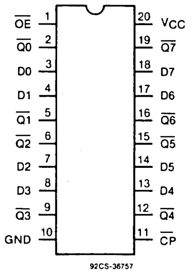
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

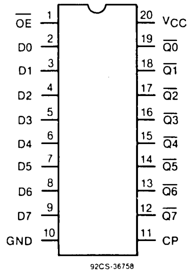
TRUTH TABLE

Inputs			Output
$\overline{OE}$	CP	Dn	$\overline{Qn}$
L	↑	H	L
L	↑	L	H
L	L	X	No Change
H	X	X	Z

Note:
X=Don't care
Z=High impedance state
↑=Low-to-High transition



Top View
CD54/74HC, HCT534 Types
TERMINAL ASSIGNMENT



Top View
CD54/74HC,HCT564 Types
TERMINAL ASSIGNMENT

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC534/CD54HC534 CD74HC564/CD54HC564										CD74HCT534/CD54HCT534 CD74HCT564/CD54HCT564									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D_0—D_7	0.15
CP	0.30
$\overline{OE}$	0.55

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Clock to Q	t_{PLH} t_{PHL}	15	13	14	ns
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	15	12	12	ns
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	15	12	14	ns
Maximum Clock Frequency	f_{max}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	32	36	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where: F_i = input frequency f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

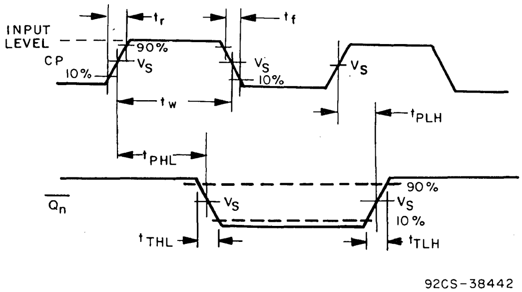
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse Width Fig. 2	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time Data to Clock Fig. 3	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	20	—	15	—	25	—	18	—	30	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock Fig. 3	534 t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
	564 t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	3	—	5	—	3	—	5	—	3	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	

CD54/74HC534, CD54/74HCT534
CD54/74HC564, CD54/74HCT564

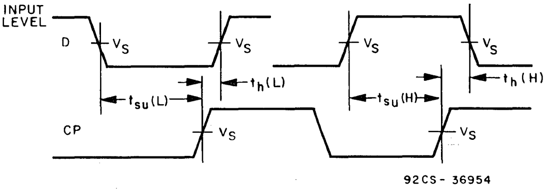
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION V_{cc} V	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Clock to Output Fig. 2 t_{PLH} t_{PHL}	2	—	165	—	—	—	205	—	—	—	250	—	—	ns
	4.5	—	33	—	35	—	41	—	44	—	50	—	53	
	6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay Output Disable to Q Fig. 4 534 t_{PLZ} t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
	6	—	26	—	—	—	33	—	—	—	38	—	—	
Propagation Delay Output Disable to Q Fig. 4 564 t_{PLZ} t_{PHZ}	2	—	135	—	—	—	170	—	—	—	205	—	—	ns
	4.5	—	27	—	30	—	34	—	38	—	41	—	45	
	6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay Output Enable to Q Fig. 4 t_{PZL} t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time Fig. 2 t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
	6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



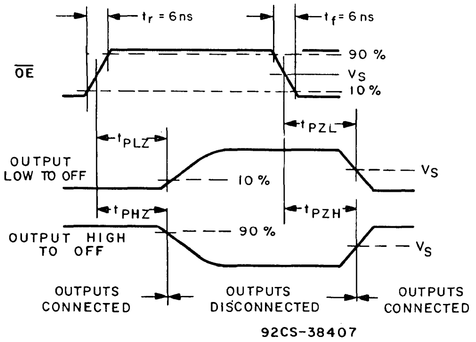
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

Fig. 2—Clock to output delays and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

Fig. 3—Data set-up and hold times.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_s	50% V_{CC}	1.3 V

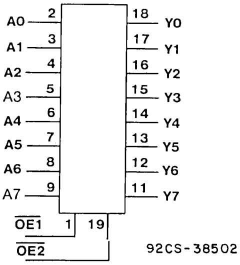
Fig. 4—Transition times and propagation delay times.

Technical Data

File Number **1659**

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Buffer and Line Drivers, 3-State

Type Features:

- *540 Inverting*
- *541 Non-Inverting*
- *Buffered Inputs*
- *3-State Outputs*
- *Bus Line Driving Capability*
- *Typical Propagation Delay = 9 ns @ $V_{CC} = 5$ V, $C_L = 15$pF, $T_A = 25°$ C*

The RCA-CD54/74HC540 and CD54/74HCT540 are Inverting Octal Buffers and Line Drivers with 3-State Outputs and the capability to drive 15 LSTTL loads. The RCA-CD54/74HC541 and CD54/74HCT541 are Non-Inverting Octal Buffers and Line Drivers with 3-State Outputs that can drive 15 LSTTL loads. The Output Enables ($\overline{\text{OE1}}$) and ($\overline{\text{OE2}}$) control the 3-State Outputs. If either $\overline{\text{OE1}}$ or $\overline{\text{OE2}}$ is HIGH the outputs will be in the high impedance state. For data output $\overline{\text{OE1}}$ and $\overline{\text{OE2}}$ both must be LOW.

The CD54HC and CD54HCT devices are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC and CD74HCT devices are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *$N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	An	HC/ HCT540	HC/ HCT541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V)	±35mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC})	±70mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

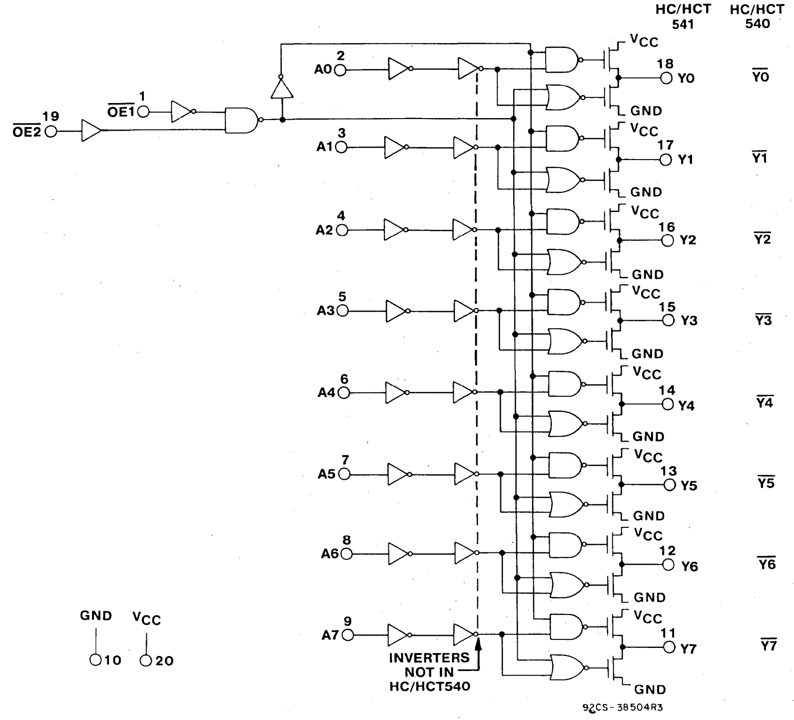


Fig. 1 — Logic diagram for the CD54/74HC/HCT 540 & 541

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC540/CD54HC540 CD74HC541/CD54HC541										CD74HCT540/CD54HCT540 CD74HCT541/CD54HCT541									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	--	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Tables

CD54/74 HCT 540	
Input	Unit Loads*
A_0 — A_7	1
$\overline{OE2}$	0.75
$\overline{OE1}$	1.15

CD54/74 HCT 541	
Input	Unit Loads*
A_0 — A_7	0.4
$\overline{OE2}$	0.75
$\overline{OE1}$	1.15

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC540, CD54/74HCT540
CD54/74HC541, CD54/74HCT541

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

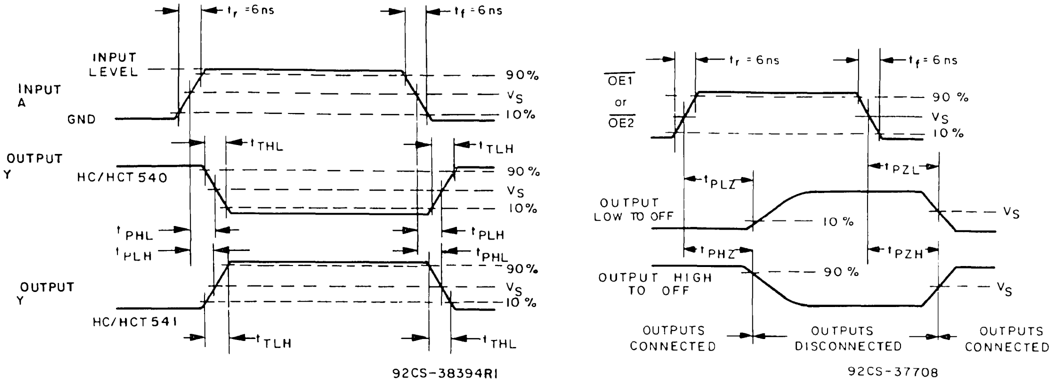
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL				UNITS
			540		541		
			HC	HCT	HC	HCT	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	9	9	9	11	ns
Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	15	13	14	14	14	ns
Power Dissipation Capacitance*	C_{PD}	—	50	55	48	55	pF

*C_{PD} is used to determine the dynamic power consumption per channel.
$PD = V_{CC}^2 f_i (C_{PD} + C_L)$
f_i = input frequency,
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	
Data to Outputs	t_{PHL}	4.5	—	22	—	24	—	28	—	30	—	33	—	36	ns
HC/HCT 540		6	—	19	—	—	—	24	—	—	—	28	—	—	
Propagation Delay	t_{PLH}	2	—	115	—	—	—	145	—	—	—	175	—	—	
Data to Outputs	t_{PHL}	4.5	—	23	—	28	—	29	—	35	—	35	—	42	ns
HC/HCT541		6	—	20	—	—	—	25	—	—	—	30	—	—	
Propagation Delay	t_{PZH}, t_{PZL},	2	—	160	—	—	—	200	—	—	—	240	—	—	
Output Enable and	t_{PHZ},	4.5	—	32	—	35	—	40	—	44	—	48	—	53	ns
Disable to Outputs	t_{PLZ}	6	—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 — Transition times and propagation delay times.

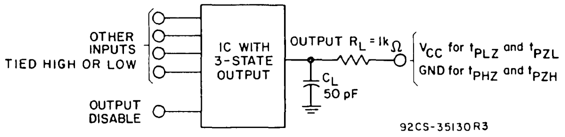
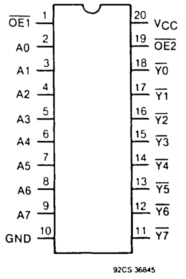
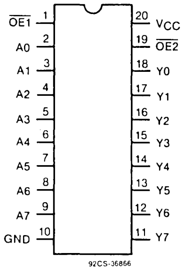


Fig. 4 — Three-state propagation delay test circuit.



CD54/74HC, HCT540 Types
TERMINAL ASSIGNMENT

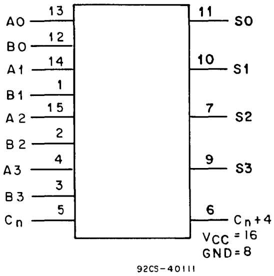


CD54/74HC, HCT541 Types
TERMINAL ASSIGNMENT

CD54/74HC583
CD54/74HC583

File Number **1828**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit BCD Full Adder With Fast Carry

Type Features:

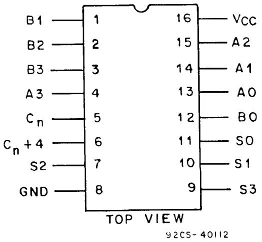
- *Adds two decimal numbers*
- *Full internal lookahead*
- *Fast ripple carry for economical expansion*

The RCA-CD54/74HC583 and CD54/74HCT583 are binary-coded-decimal (BCD) full adders that add two 4-bit BCD numbers and generate a carry-out bit if the sum exceeds 9.

The CD54HC/HCT583 are supplied in 16-lead hermetic dual-in-line frit seal ceramic packages (F suffix). The CD74HC/HCT583 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:* $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5\ V$
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8\ V$ *Max.,* $V_{IH} = 2\ V$ *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC583

CD54/74HC583

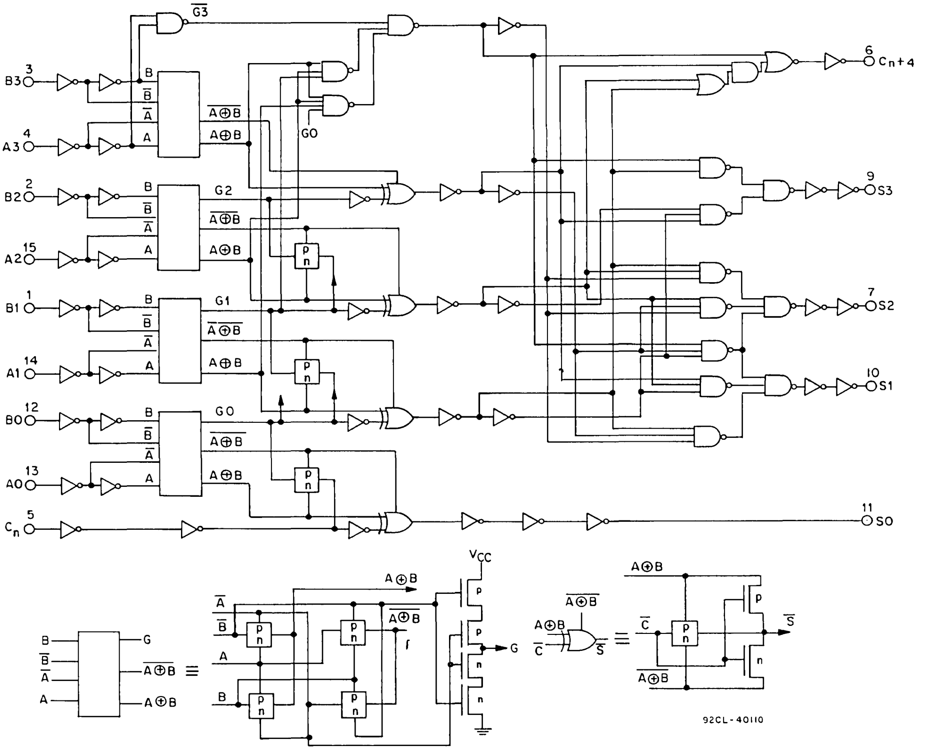


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5\ V$)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC583
CD54/74HC583

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC583/CD54HC583										CD74HCT583/CD54HCT583									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All	1.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

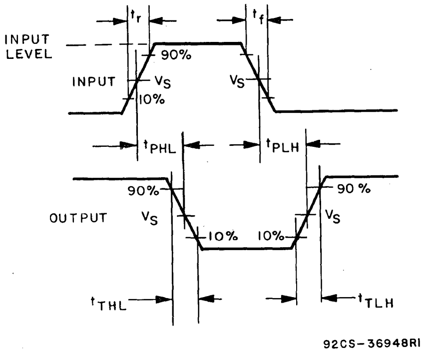
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay,					
C_n to S_n	t_{PHL}, t_{PLH}	15	24	24	ns
A_n or B_n to S_n	t_{PHL}, t_{PLH}	15	23	29	
C_n to $C_n + 4$	t_{PHL}, t_{PLH}	15	15	18	
A_n or B_n to $C_n + 4$	t_{PHL}, t_{PLH}	15	16	22	
Power Dissipation Capacitance *	C_{PD}	—	50	54	pF

*CPD is used to determine the dynamic power consumption, per package
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITIONS V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
	t_{PHL}	4.5	—	58	—	58	—	73	—	73	—	87	—	87	
C_n to S_n		6	—	49	—	—	—	62	—	—	—	74	—	—	
	t_{PLH}	2	—	280	—	—	—	350	—	—	—	420	—	—	
	t_{PHL}	4.5	—	56	—	68	—	70	—	85	—	84	—	102	
A_n or B_n to S_n		6	—	48	—	—	—	60	—	—	—	71	—	—	
	t_{PLH}	2	—	180	—	—	—	225	—	—	—	270	—	—	
	t_{PHL}	4.5	—	36	—	42	—	45	—	53	—	54	—	63	
C_n to $C_n + 4$		6	—	31	—	—	—	38	—	—	—	46	—	—	
	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	
	t_{PHL}	4.5	—	39	—	51	—	49	—	64	—	59	—	77	
A_n or B_n to $C_n + 4$		6	—	33	—	—	—	42	—	—	—	50	—	—	
Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition and propagation delay times.

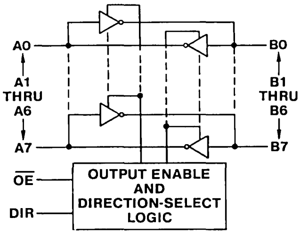
Application

In an application where a binary number whose decimal value is greater than 9 is to be added to a BCD number (0-9), this device can be used to convert the binary number to a BCD number and a carry. The resultant BCD + carry can then be added to the other BCD operand to complete the operation. The conversion from binary to BCD is accomplished by adding the binary number to BCD "0" (binary number on A0-A3 and 0000 on B0-B3).

File Number **1677**

CD54/74HC640, CD54/74HCT640
CD54/74HC643, CD54/74HCT643

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM
INVERTING HC/HCT640

92CS-38780

Octal 3-State Bus Transceivers

Inverting (HC/HCT640)
True/Inverting (HC/HCT643)

Type Features:

- *3-state outputs*
- *Buffered inputs*
- *Applications in multiple-data-bus architecture*

The RCA-CD54/74HC640, 643 and CD54/74HCT640, 643 silicon-gate CMOS 3-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads.

The CD54/74HC640 and CD54/74HCT640 are inverting buffers; the CD54/74HC643 and CD54/74HCT643 are true/inverting buffers.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ($\overline{OE}$); a high $\overline{OE}$ puts these devices in the high impedance mode.

The CD54HC640, 643 and the CD54HCT640, 643 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC640, 643 and CD74HCT640, 643 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). These devices are also supplied in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}= *30%,* N_{IH}=*30% of* V_{CC} *@* V_{CC}=*5 V*
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=*0.8 V max.,* V_{IH}=*2 V min.*
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}

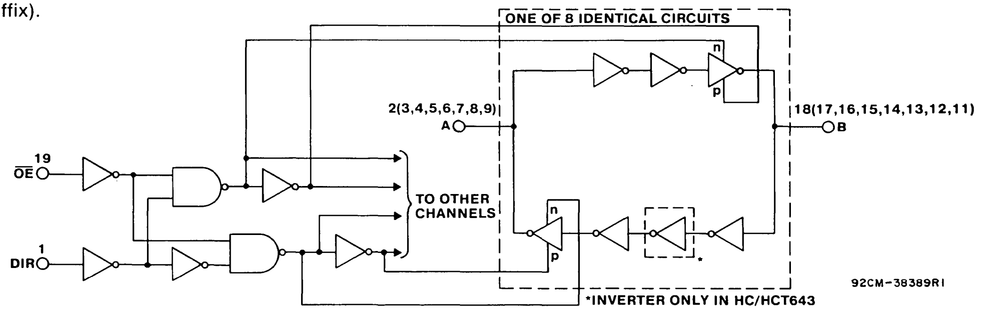
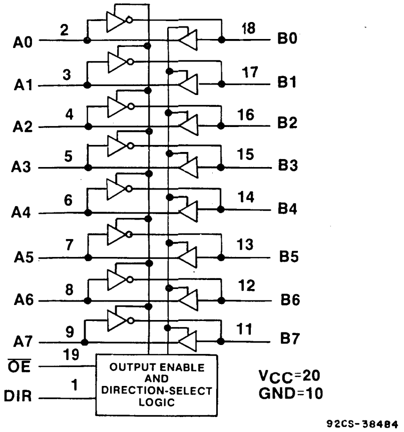


Fig. 1 - Logic diagram.

CD54/74HC640, CD54/74HCT640
CD54/74HC643, CD54/74HCT643



FUNCTIONAL DIAGRAM
TRUE/INVERTING HC/HCT643

TRUTH TABLE

CONTROL INPUTS		HC, HCT640 Series DATA PORT STATUS		HC, HCT643 Series DATA PORT STATUS	
$\overline{OE}$	DIR	A_n	B_n	A_n	B_n
L	L	$\overline{O}$	I	O	I
H	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	H	I	$\overline{O}$	I	$\overline{O}$

To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10KΩ to 1MΩ resistors.

H = High	O = Output (Same Level as Input)
L = Low	$\overline{O}$ = Output (Inversion of Input Level)
I = Input	Z = High Impedance

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC} +0.5$ V)	±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC640, CD54/74HCT640
CD54/74HC643, CD54/74HCT643

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC640/643/CD54HC640/643										CD74HCT640/643/CD54HCT640/643										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Bus Driver	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Bus Driver	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *	
	HCT640	HCT643
DIR	0.9	0.9
$\overline{OE}$, A	1.5	1.5
B	1.5	0.4

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC640, CD54/74HCT640
CD54/74HC643, CD54/74HCT643

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES				UNITS
			HC640	HCT640	HC643	HCT643	
Propagation Delay $A \rightarrow \overline{B}$, $B \rightarrow \overline{A}$	15	t_{PHL}, t_{PLH}	7	9	7	9	ns
$B \rightarrow A$			—	—	9	10	
Enable to High Z		t_{PHZ}, t_{PLZ}	12	12	12	12	
Enable from High Z		t_{PZH}, t_{PZL}	12	12	12	13	
Power Dissipation Capacitance	—	C_{PD}*	38	41	45	55	pF

* C_{PD} is used to determine the dynamic power consumption per channel.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$, where: f_i = input frequency. C_L = output load capacitance. V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
$A \rightarrow \overline{B}$ 640/643	t_{PHL}	4.5	—	18	—	22	—	23	—	28	—	27	—	33	ns
$B \rightarrow \overline{A}$		6	—	15	—	—	—	20	—	—	—	23	—	—	
643	t_{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	
$B \rightarrow A$	t_{PHL}	4.5	—	22	—	26	—	28	—	33	—	33	—	39	ns
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Output High-Z:	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
To High Level, 640	t_{PZL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
To Low Level		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output High Level, 640	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Low Level	t_{PLZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
to High Z		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output High Z:	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
To High Level 643	t_{PZL}	4.5	—	30	—	33	—	38	—	41	—	45	—	50	ns
To Low Level		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output High Level, 643	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Low Level	t_{PLZ}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
to High Z		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_{in}		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_o		—	20	—	20	—	20	—	20	—	20	—	20	pF

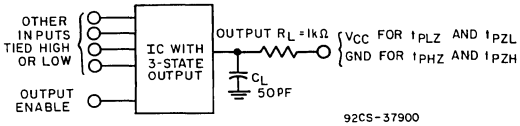
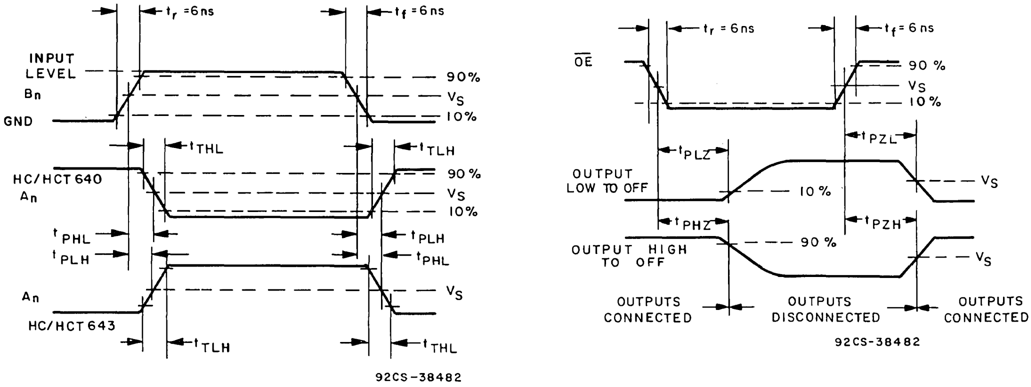
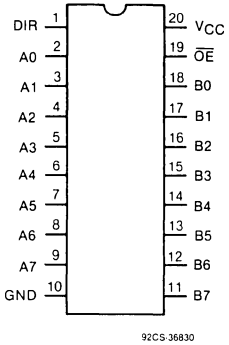


Fig. 2 - Three-state propagation delay test circuit.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 - Transition times and progagation delay times.



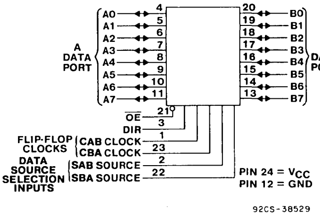
TERMINAL ASSIGNMENT

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

File Number **1664**

**Advance Information/
Preliminary Data**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Bus Transceiver/Register, 3-State

Type Features:

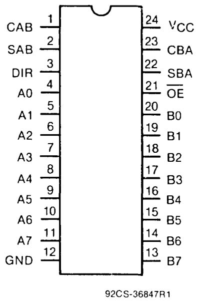
- *Independent Registers for A and B Buses*
- *CD54/74HC/HCT646 Non-Inverting CD54/74HC/HCT648 Inverting*
- *3-State Outputs*
- *Drives 15LSTTL loads*
- *Typical Propagation Delay = 12ns (A ←→ B) @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC646 and CD54/74HCT646 are octal bus transceivers/registers with 3-state non-inverting outputs. The RCA-CD54/74HC648 and CD54/74HCT648 are octal bus transceivers/registers with 3-state inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output enable $(\overline{OE})$ and direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the output enable $(\overline{OE})$ is LOW. In the high impedance mode (output enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the direction (DIR) and output enable $(\overline{OE})$ terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD54HC646, 648 and CD54HCT646, 648 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC646, 648 and CD74HCT646, 648 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

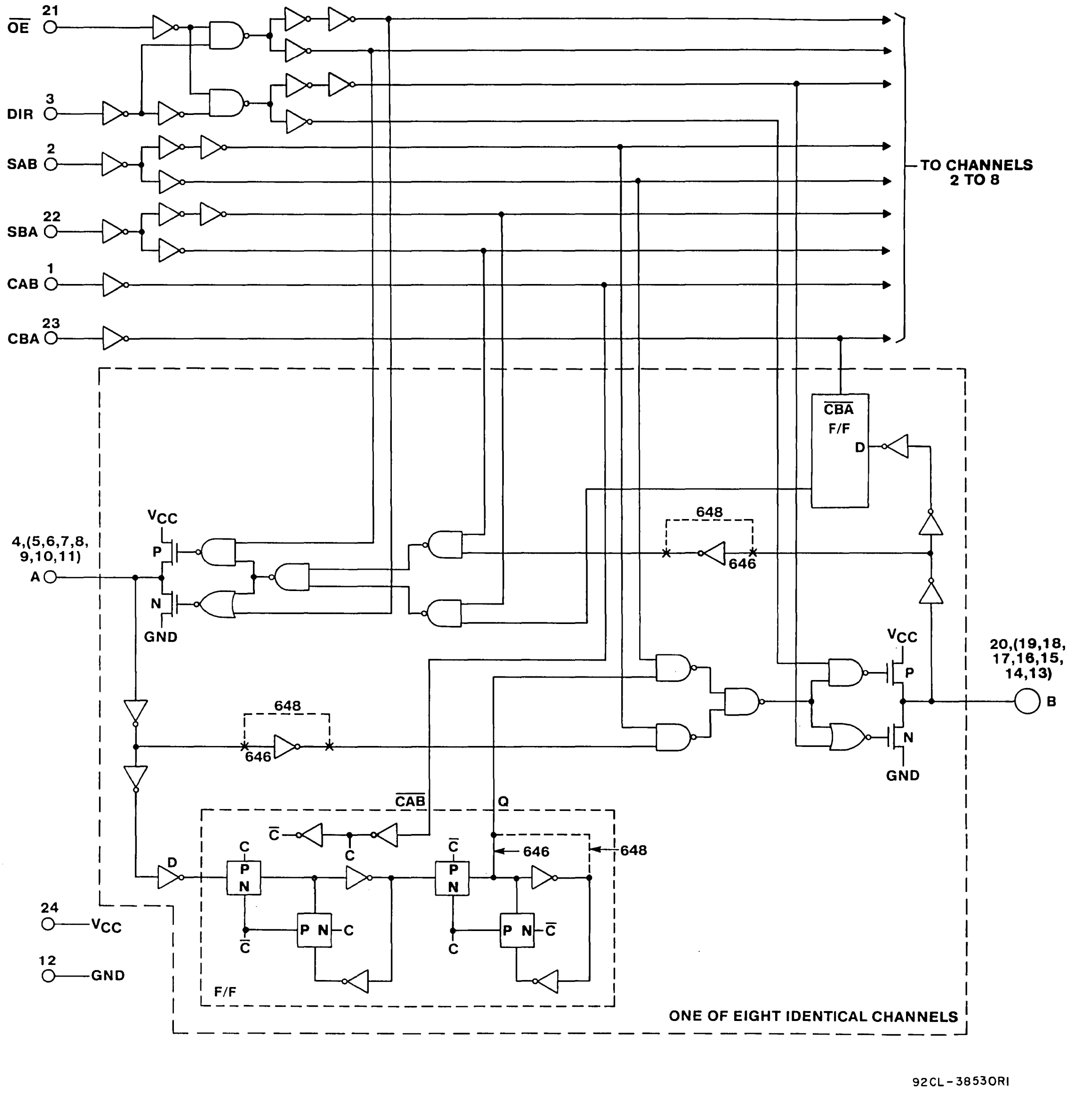


Fig. 1 — Logic Diagram.

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

FUNCTION TABLE

INPUTS						DATA I/O #		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

\# The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 10KΩ resistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{V}$) .... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M .... -40 to +85°C
PACKAGE TYPE F, H .... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC646/CD54HC646 CD74HC648/CD54HC648										CD74HCT646/CD54HCT646 CD74HCT648/CD54HCT648										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	--	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{OE}$	1.3
DIR	0.75
Clock A→B, B→A	0.6
Select A, Select B	0.45
Inputs A0-A7, B0-B7	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delays Store A Data to B Bus (646)	t_{PLH}, t_{PHL}	15	18	18	ns
Store B Data to A Bus (646)	t_{PLH}, t_{PHL}	15	18	18	ns
Store $\overline{A}$ Data to B Bus (648)	t_{PLH}, t_{PHL}	15	20	23	ns
Store $\overline{B}$ Data to A Bus (648)	t_{PLH}, t_{PHL}	15	20	23	ns
A Data to B Bus (646)	t_{PLH}, t_{PHL}	15	12	15	ns
B Data to A Bus (646)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{A}$ Data to B Bus (648)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{B}$ Data to A Bus (648)	t_{PLH}, t_{PHL}	15	12	15	ns
Select to Data (646)	t_{PLH}, t_{PHL}	15	14	19	ns
Select to Data (648)	t_{PLH}, t_{PHL}	15	16	19	ns
3-State Disabling Time	t_{PLZ}, t_{PHZ}	15	14	14	ns
3-State Enabling Time	t_{PZL}, t_{PZH}	15	14	19	ns
Max Frequency	f_{max}	15	60	45	MHz
Power Dissipation Capacitance*	C_{PD}	—	52	52	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o$ where:
C_L = output load capacitance
V_{CC} = supply voltage
f_i = input frequency
f_o = output frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHZ
		4.5	30	—	25	—	25	—	20	—	20	—	17	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Set Up Time Data to Clock	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock	t_H	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	5	—	9	—	5	—	11	—	5	—	
		6	6	—	—	—	8	—	—	—	9	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	25	—	20	—	31	—	24	—	38	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

CD54/74HC646, CD54/74HCT646
CD54/74HC648, CD54/74HCT648

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	2	—	220	—	—	—	275	—	—	—	330	—	—	
Store A data to B bus t_{PLH}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	ns
Store B data to B bus (646) t_{PHL}	6	—	37	—	—	—	47	—	—	—	5.6	—	—	
Store $\overline{A}$ data to B bus t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
Store $\overline{B}$ data to A Bus t_{PHL}	4.5	—	48	—	54	—	60	—	68	—	72	—	81	ns
(648)	6	—	41	—	—	—	51	—	—	—	61	—	—	
A data to B bus t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
B data to A Bus t_{PHL}	4.5	—	27	—	37	—	34	—	46	—	41	—	56	ns
(646)	6	—	23	—	—	—	29	—	—	—	35	—	—	
$\overline{A}$ data to B bus t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{B}$ data to A Bus t_{PHL}	4.5	—	30	—	37	—	38	—	46	—	45	—	56	ns
(648)	6	—	26	—	—	—	33	—	—	—	38	—	—	
Select to Data	2	—	170	—	—	—	215	—	—	—	255	—	—	
t_{PLH}	4.5	—	34	—	46	—	43	—	58	—	51	—	69	ns
(646) t_{PHL}	6	—	29	—	—	—	37	—	—	—	43	—	—	
Select to Data	2	—	190	—	—	—	240	—	—	—	285	—	—	
t_{PLH}	4.5	—	38	—	46	—	48	—	58	—	57	—	69	ns
(648) t_{PHL}	6	—	32	—	—	—	39	—	—	—	48	—	—	
3-State Disabling Time	2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or t_{PLZ}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
Register to Output t_{PHZ}	6	—	30	—	—	—	37	—	—	—	45	—	—	
3-State Enabling Time	2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or t_{PZL}	4.5	—	35	—	45	—	44	—	56	—	53	—	68	ns
Register to Output t_{PZH}	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time	2	—	60	—	—	—	75	—	—	—	90	—	—	
t_{TLH}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
t_{THL}	6	—	10	—	—	—	13	—	—	—	15	—	—	
3-State Output		—	—	—	—	—	—	—	—	—	—	—	—	
Capacitance C_o	—	—	20	—	20	—	20	—	20	—	20	—	20	pF
		—	—	—	—	—	—	—	—	—	—	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

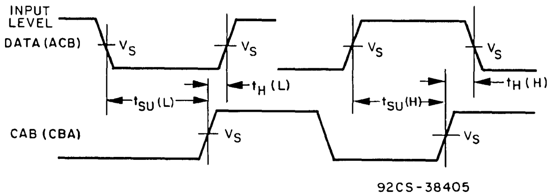
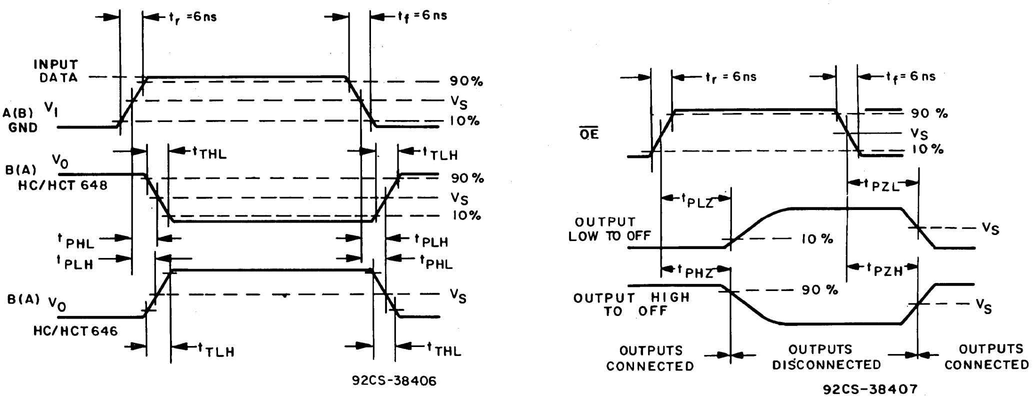


Fig. 2 — Data setup and hold times.



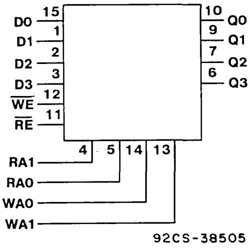
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 — Transition times and propagation delay times.

File Number **1660**

CD54/74HC670
CD54/74HCT670

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4 x 4 Register File

Type Features:

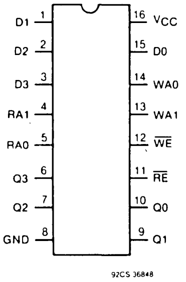
- *Simultaneous and Independent Read and Write Operations*
- *Expandable to 512 Words of n-Bits*
- *3-State Outputs*
- *Organized as 4 Words x 4 Bits Wide*
- *Typical read time: 16 ns for HC670 at V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*
- *Buffered inputs*

The RCA-CD54/74HC670 and CD54/74HCT670 are 16-bit register files organized as 4 words x 4 bits each. Read and write address and enable inputs allow simultaneous writing into one location while reading another. Four data inputs are provided to store the 4-bit word. The write address inputs (WA0 and WA1) determine the location of the stored word in the register. When write enable ($\overline{WE}$) is low the word is entered into the address location and it remains transparent to the data. The outputs will reflect the true form of the input data. When ($\overline{WE}$) is high data and address inputs are inhibited. Data acquisition from the four registers is made possible by the read address inputs (RA1 and RA0). The addressed word appears at the output when the read enable ($\overline{RE}$) is low. The output is in the high inpedance state when the ($\overline{RE}$) is high. Outputs can be tied together to increase the word capacity to 512 x 4 bits.

The RCA CD54HC/HCT670 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT670 are supplied in a 16-lead dual-in-line plastic package (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

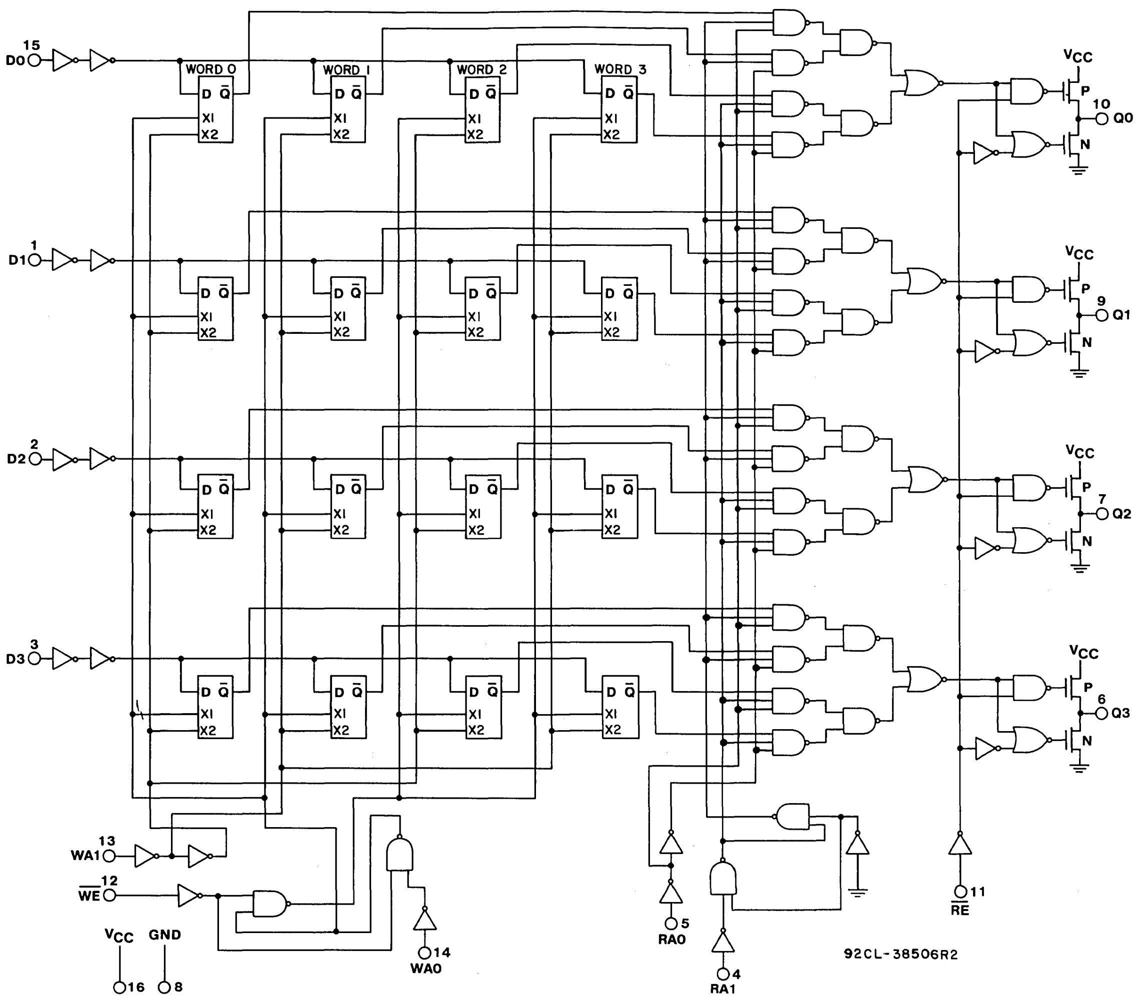
Family Features:

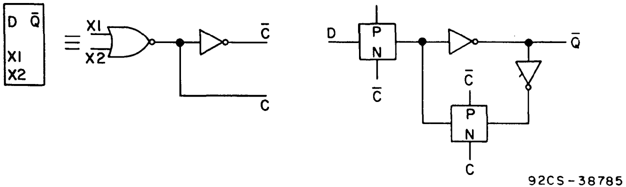
- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%, N_{IH} = 30\%$ *of* V_{CC}*;* @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC670
CD54/74HCT670





Latch Detail

Fig. 1 — Logic Diagram.

CD54/74HC670
CD54/74HCT670

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{WE}$	D_N	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE:
a. The Write Address (WA0 and WA1) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_N
	$\overline{RE}$	INTERNAL LATCHES[b]	
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE:
b. The selection of the "internal latches" by Read Address (RA0 and RA1) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = HIGH impedance "off" state.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5\text{V}$) .... ±35 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC670
CD54/74HCT670

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC670/CD54HC670										CD74HCT670/CD54HCT670										UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Bus Driver	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-6	4.5	3.98	—	—	3.84	—	3.7	—										
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Bus Driver	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		6	4.5	—	—	0.26	—	0.33	—	0.4										
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State leakage current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{WE}$	0.3
WAO	0.2
WA1	0.4
$\overline{RE}$	1.5
DATA	0.15
RAO	0.4
RA1	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Reading any word	15	t_{PLH} t_{PHL}	16	17	ns
Write Enable to Output	15	t_{PLH} t_{PHL}	21	21	ns
Data to Output	15	t_{PLH} t_{PHL}	21	21	ns
Output Disable Time	15	t_{PLZ} t_{PHZ}	12	14	ns
Output Enable Time	15	t_{PZL} t_{PZH}	12	16	ns
Power Dissipation Capacitance*	—	C_{PD}	59	66	pF

*C_{PD} is used to determine the dynamic power consumption, per output.
PD = $C_{PD} V_{CC}^2 f_i + \Sigma\ C_L V_{CC}^2 f_o$ where f_i = input frequency,
f_o = output frequency,
C_L = output load capacitance
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Set-up time Data to $\overline{WE}$	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	14	—	15	—	18	—	18	—	21	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold time Data to $\overline{WE}$	t_h	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Set-up time Write to $\overline{WE}$	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	18	—	15	—	23	—	18	—	27	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold time Write to $\overline{WE}$	t_h	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{WE}$ Pulsewidth	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Latch time $\overline{WE}$ to RA0, RA1	t_{LATCH}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	25	—	25	—	31	—	30	—	38	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	

CD54/74HC670
CD54/74HCT670

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns,)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Reading any word	t_{PLH} t_{PHL}	2	—	195	—	—	—	245	—	—	—	295	—	—	ns
		4.5	—	39	—	40	—	49	—	50	—	59	—	60	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
Write Enable to Output	t_{PLH} t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Data to Output	t_{PLH} t_{PHL}	2	—	256	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Output Disable Time	t_{PLZ} t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Enable Time	t_{PZL} t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	38	—	38	—	48	—	45	—	57	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	10	—	—	—	19	—	—	
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

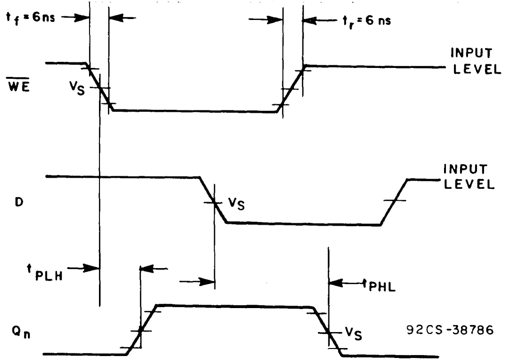


Fig. 2 — Propagation Delay, Write Enable and Data to Output

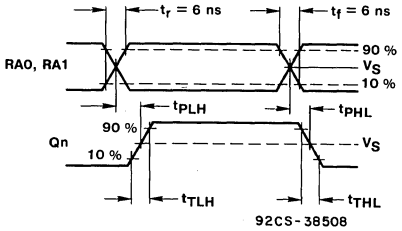


Fig. 3 — Propagation delay, Read Address to Output

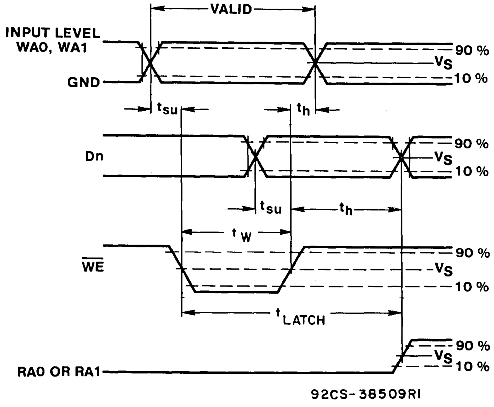


Fig. 4 — Setup and Hold Times, Write Address and Data to Write Enable

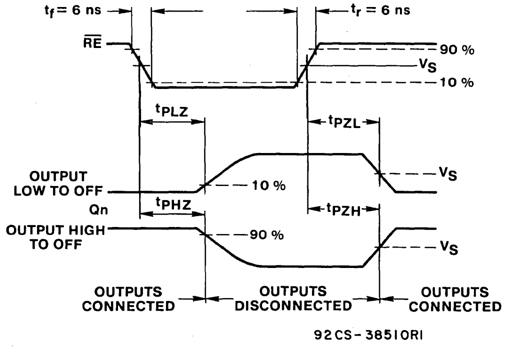


Fig. 5 — 3-State Enable and Disable Times

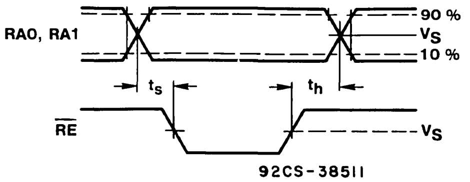


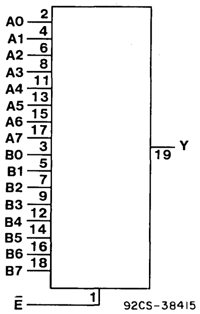
Fig. 6 — Setup and Hold times, Read Address to Read Enable

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

CD54/74HC688
CD54/74HCT688

File Number **1646**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Bit Magnitude Comparator

Type Features:
- *Cascadable*

The RCA-CD54/74HC688 and CD54/74HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

The CD54HC688 and CD54HCT688 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC688 and CD74HCT688 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

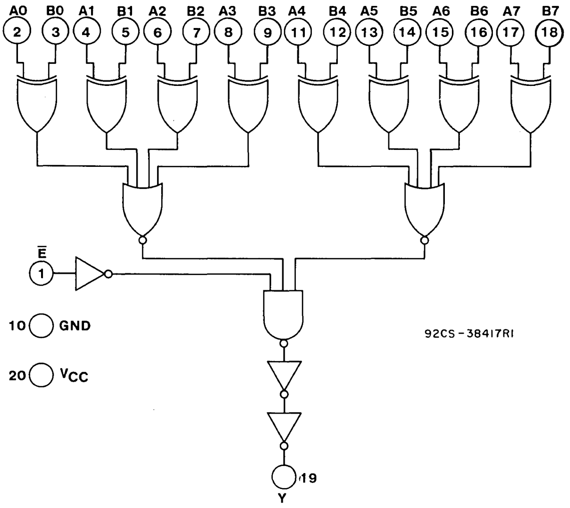


Fig. 1 - Logic diagram.

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: $N_{IL}=30\%, N_{IH}=30\%$ *of* V_{CC}; *@* $V_{CC}=5$ *V*
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL}=0.8$ *V max.,* $V_{IH}=2$ *V min.*
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}

TRUTH TABLE

Inputs		Outputs
A, B	$\overline{E}$	Y
A = B	L	L
A ≠ B	L	H
X	H	H

X = Don't care
L = Low level
H = High level

CD54/74HC688
CD54/74HCT688

MAXIMUM RATINGS, *Absolute-Maximum Values:*

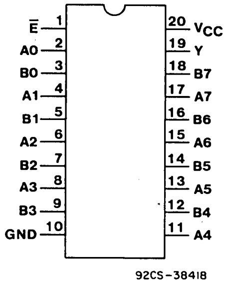
DC SUPPLY-VOLTAGE, (V_{CC}): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_o < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC688
CD54/74HCT688

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC688/CD54HC688										CD74HCT688/CD54HCT688									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Enable	0.7
Data Inputs	0.35

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max.@25° C.

CD54/74HC688
CD54/74HCT688

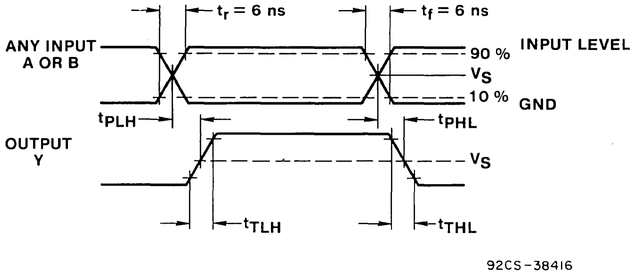
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay A and B Data to Output	t_{PLH} t_{PHL}	15	14	14	ns
Propagation Delay Enable to Output	t_{PLH} t_{PHL}	15	9	9	
Power Dissipation Capacitance*	C_{PD}	—	22	22	pF

*C_{PD} is used to determine the power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i=input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	170	—	—	—	210	—	—	—	255	—	—	
An to Output	t_{PHL}	4.5	—	34	—	34	—	42	—	42	—	51	—	51	ns
		6	—	29	—	—	—	36	—	—	—	43	—	—	
	t_{PLH}	2	—	170	—	—	—	210	—	—	—	255	—	—	
Bn to Output	t_{PHL}	4.5	—	34	—	34	—	42	—	42	—	51	—	51	ns
		6	—	29	—	—	—	36	—	—	—	43	—	—	
	t_{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	
$\overline{E}$ to Output	t_{PHL}	4.5	—	24	—	24	—	30	—	30	—	36	—	36	ns
		6		20	—	—	—	26	—	—	—	30	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Propagation delay and transition times.

CD54/74HC4002
CD54/74HCT4002

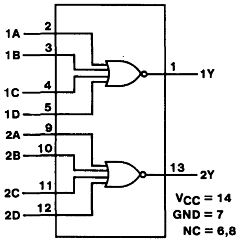
File Number **1776**

High-Speed CMOS Logic

Dual 4-Input NOR Gate

Type Features:

- *Typical CD54/74HC4002 Propagation Delay = 8ns @ V_{CC} = 5V, C_L = 15pF, T_A = 25° C*



92CS-36771R2

FUNCTIONAL DIAGRAM

The RCA-CD54/74HC4002 and CD54/74HCT4002 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC/HCT4002 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4002 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

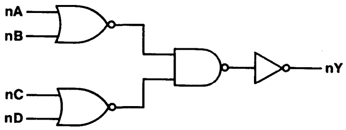


Fig. 1 - LOGIC DIAGRAM (One Gate) for HC4002.

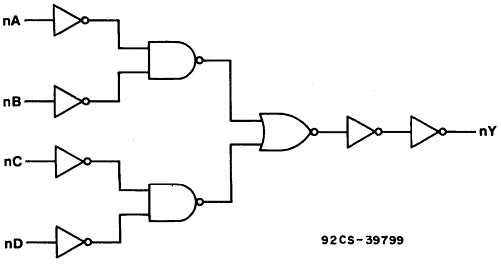


Fig. 2 - LOGIC DIAGRAM for HCT4002.

Family Features:

- *Fanout (over temperature range):*
  Standard Outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide Operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V Min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

H = High Level
L = Low Level
X = Don't Care.

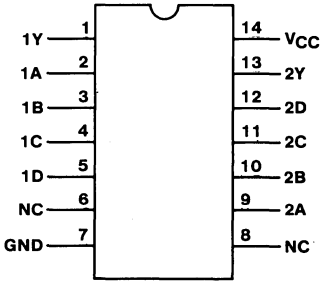
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-39798

TERMINAL ASSIGNMENT

CD54/74HC4002
CD54/74HCT4002

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4002/CD54HC4002										CD74HCT4002/CD54HCT4002									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level			2	1.5	—	—	1.5	—	1.5	—		4.5								
Input Voltage V_{IH}			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
Low-Level			2	—	—	0.5	—	0.5	—	0.5		4.5								
Input Voltage V_{IL}			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8		5.5								
High-Level	V_{IL}		2	1.9	—	—	1.9	—	1.9	—	V_{IL}									
Output Voltage V_{OH}	or	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	V
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
Low-Level	V_{IL}		2	—	—	0.1	—	0.1	—	0.1	V_{IL}									
Output Voltage V_{OL}	or	0.02	4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	V
CMOS Loads	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
All	0.45

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @25° C.

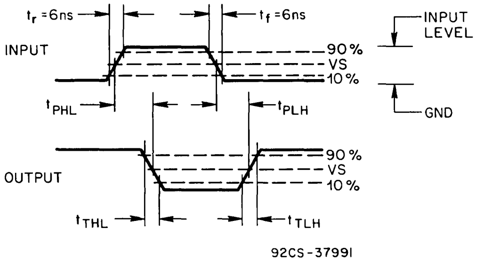
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Time:	t_{PLH}	15	8	9	ns
nA, nB, nC, nD to nY (Fig. 3)	t_{PHL}		8	12	
Power Dissipation Capacitance*	C_{PD}	—	22	22	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
nA, nB, nC, nD		4.5	—	20	—	22	—	25	—	28	—	30	—	33	
to nY (Fig. 3)		6	—	17	—	—	—	21	—	—	—	26	—	—	
		2	—	100	—	—	—	125	—	—	—	150	—	—	
	t_{PHL}	4.5	—	20	—	29	—	25	—	36	—	30	—	44	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
(Fig. 3)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



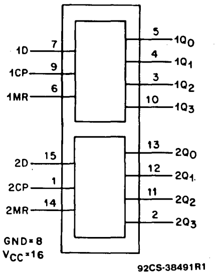
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 - Transition times and propagation delay times.

CD54/74HC4015
CD54/74HCT4015

File Number **1678**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 4-Stage Static Shift Register

Type Features:

- *Maximum frequency, typically 60 MHz*
  C_L = 15 pF, V_{CC} = 5 V, T_A = 25° C
- *Positive-edge clocking*
- *Overriding reset*
- *Buffered inputs and outputs*

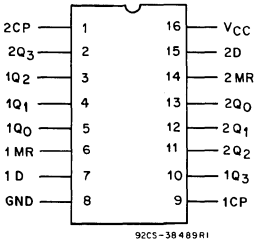
The RCA-CD54/74HC4015 and CD54/74HCT4015 consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK (CP) and RESET (MR) inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line.

The device can drive up to 10 low power Schottky equivalent loads. The CD54/74HCT4015 is an enhanced version of equivalent CMOS types.

The CD54HC4015 and CD54HCT4015 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4015 and CD74HCT4015 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

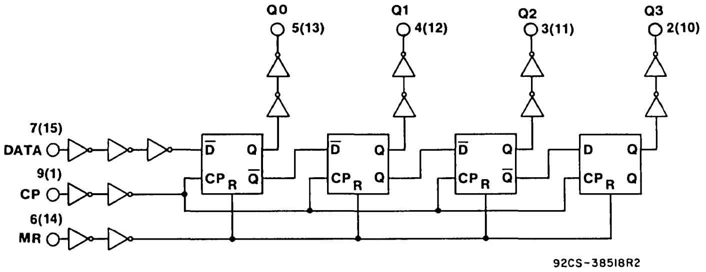


Fig. 1 - Logic diagram for one-half CD54/74HC/HCT4015.

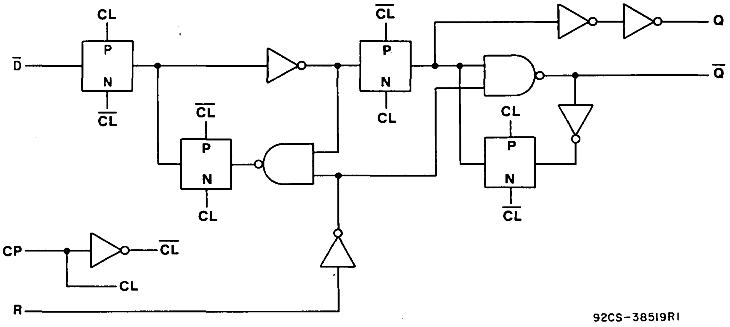


Fig. 2 - Flip-flop detail.

LOGIC TABLE

INPUTS			OUTPUTS			
CP	D	R	Q_0	Q_1	Q_2	Q_3
_/‾	l	L	L	q'_0	q'_1	q'_2
_/‾	h	L	H	q'_0	q'_1	q'_2
‾_	X	L	q'_0	q'_1	q'_2	q'_3
X	X	H	L	L	L	L

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q'_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't Care.
_/‾ = LOW-to-HIGH clock transition.
‾_ = HIGH-to-LOW clock transition.

CD54/74HC4015
CD54/74HCT4015

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):

(Voltages referenced to ground) .... -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) .... ±20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V) .... ±20 mA

DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_o < V_{CC} +0.5$ V) .... ±25 mA

DC V_{CC} OR GROUND CURRENT, (I_{CC}) .... ±50 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60° C (PACKAGE TYPE E) .... 500 mW

For T_A = +60 to +85° C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/° C to 300 mW

For T_A = -55 to +100° C (PACKAGE TYPE F, H) .... 500 mW

For T_A = +100 to +125° C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/° C to 300 mW

For T_A = -40 to +70° C (PACKAGE TYPE M) .... 400 mW

For T_A = +70 to +125° C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/° C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H .... -55 to +125° C

PACKAGE TYPE E, M .... -40 to +85° C

STORAGE TEMPERATURE (T_{stg}) .... -65 to +150° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only .... +300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4015
CD54/74HCT4015

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC4015/CD54HC4015										CD74HCT4015/CD54HCT4015									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
DATA	0.15
CP	0.45
MR	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC4015
CD54/74HCT4015

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical		Units
			HC	HCT	
Propagation Delay CP to Qn	t_{PHL} t_{PLH}	15	14	14	ns
MR to Qn	t_{PHL}	15	25	25	
Maximum Clock Frequency	f_{MAX}	15	60	60	MHz
Power Dissipation Capacitance*	C_{PD}*	—	43	43	pF

*C_{PD} is used to determine the dynamic power consumption, per shift register.
$P_D = C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 fo$ where: fi=input frequency, fo=output frequency
C_L=load capacitance
V_{CC}=supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency (See Fig. 3)	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	24	—	24	—	20	—	20	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width (See Fig. 3)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width (See Fig. 4)	t_W	2	150	—	—	—	190	—	—	—	225	—	—	—	
		4.5	30	—	30	—	38	—	38	—	45	—	45	—	
		6	26	—	—	—	33	—	—	—	38	—	—	—	
MR Recovery Time (See Fig. 4)	t_{REC}	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	15	—	13	—	19	—	15	—	22	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Setup Time Data-In to CP (See Figs. 5 & 6)	t_{SUL} t_{SUH}	2	60	—	—	—	75	—	—	—	90	—	—	—	
		4.5	12	—	16	—	15	—	20	—	18	—	24	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time: Data-In to CP (See Figs. 5 & 6)	t_H	2 4.5 6	0	—	0	—	0	—	0	—	0	—	0	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Clock to Qn	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	270	—	—	ns
		4.5	—	35	—	35	—	44	—	44	—	54	—	54	
		6	—	30	—	—	—	37	—	—	—	46	—	—	
MR to Qn (Clock High)		2	—	275	—	—	—	345	—	—	—	415	—	—	
		4.5	—	55	—	60	—	64	—	75	—	83	—	90	
		6	—	47	—	—	—	54	—	—	—	71	—	—	
MR to Qn (Clock Low)		2	—	325	—	—	—	400	—	—	—	490	—	—	
		4.5	—	65	—	65	—	81	—	81	—	98	—	98	
		6	—	55	—	—	—	69	—	—	—	83	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

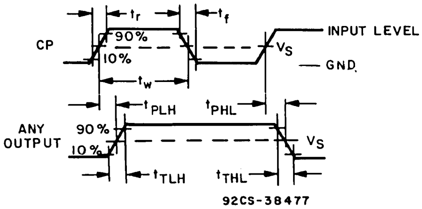


Fig. 3 - Clock-to-output delays and clock pulse width.

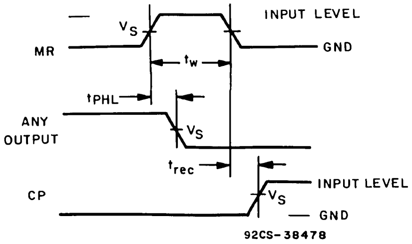


Fig. 4 - Master Reset pulse width. Master Reset to output delay and clock recovery times.

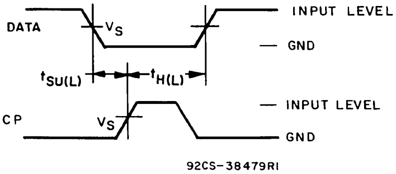


Fig. 5 - Data set-up and hold times.

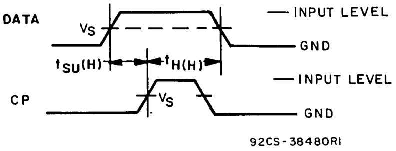


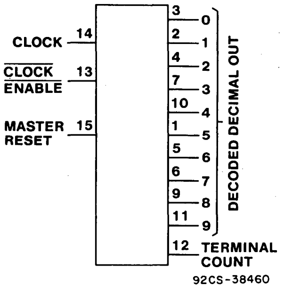
Fig. 6 - Data set-up and hold times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

CD54/74HC4017
CD54/74HCT4017

File Number **1639**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM
CD54/74HC4017, CD54/74HCT4017

Decade Counter/Divider with 10 Decoded Outputs

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Positive edge clocking*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC4017 and CD54/74HCT4017 are high speed silicon gate CMOS 5-stage Johnson counters with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the CLOCK (CP) input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY (TC) output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE ($\overline{CE}$) to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET (MR) input is also provided which when taken high sets all the decoded outputs, except "0", low.

The device can drive up to 10 low power Schottky equivalent loads. The CD54/74HCT4017 is an enhanced version of equivalent CMOS types.

The CD54HC4017 and CD54HCT4017 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4017 and CD74HCT4017 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

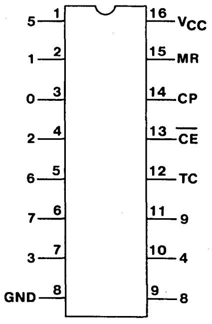
TRUTH TABLE

CP	$\overline{CE}$	MR	Output State*
L	X	L	No Change
X	H	L	No Change
X	X	H	"0"=H, "1"-"9"=L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

H = High Level
L = Low Level
↓ = High-to-Low Transition
↑ = Low-to-High Transition
X=Don't Care
*If n<5 TC=H, Otherwise=L

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs — 10 LSTTL Loads
  Bus Driver Outputs — 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



92CS-38459

TERMINAL ASSIGNMENT

CD54/74HC4017
CD54/74HCT4017

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

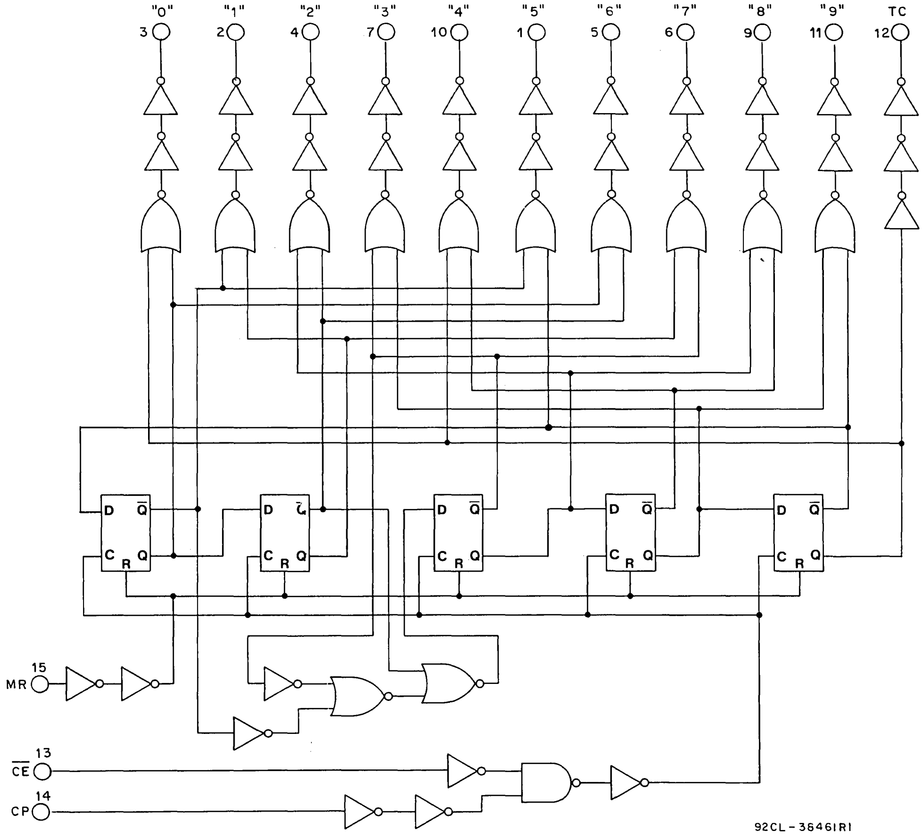


Fig. 1 — Logic diagram for the CD54/74HC/HCT 4017

CD54/74HC4017
CD54/74HCT4017

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4017/CD54HC4017										CD74HCT4017/CD54HCT4017									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

***For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.**

HCT Input Loading Table

Input	Unit Loads*
CP	0.15
$\overline{CE}$	0.25
MR	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC4017
CD54/74HCT4017

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay CP to Out	t_{PLH} t_{PHL}	15	19	19	ns
CP to TC	t_{PLH} t_{PHL}	15	19	19	ns
$\overline{CE}$ to Out	t_{PLH} t_{PHL}	15	21	21	ns
$\overline{CE}$ to TC	t_{PLH} t_{PHL}	15	21	21	ns
MR to Out	t_{PLH} t_{PHL}	15	19	19	ns
MR to TC	t_{PLH} t_{PHL}	15	19	19	ns
Max. CP Frequency	f_{MAX}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	39	39	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

CD54/74HC4017
CD54/74HCT4017

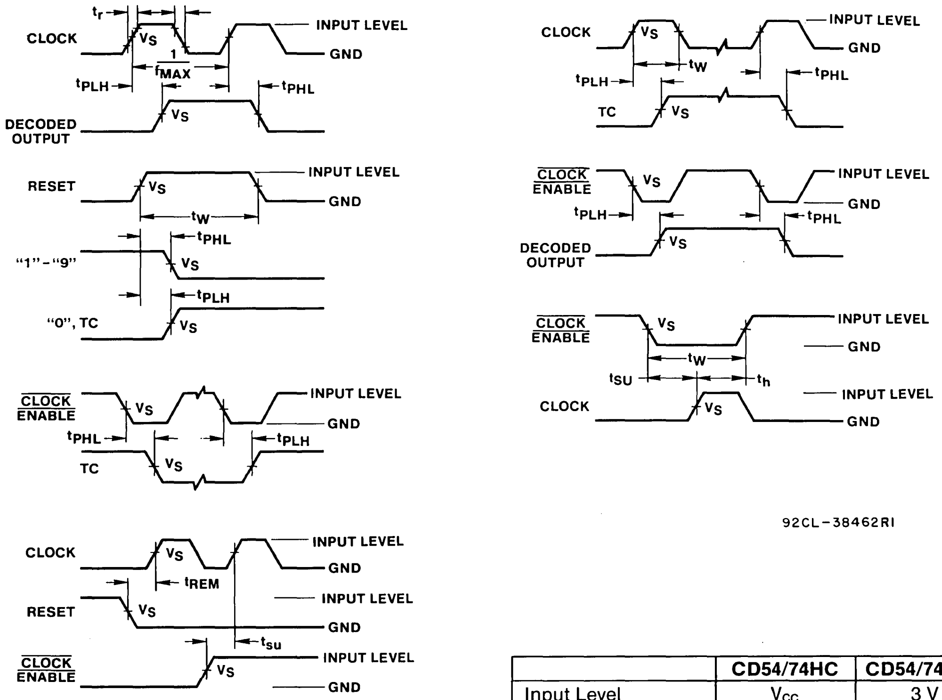
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Max. Clock Freq. f_{CL} (max.)	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	25	—	35	—	20	—	20	—	17	—	
	6	35	—	—	—	49	—	—	—	23	—	—	—	
$\overline{CE}$ to CP Setup Time t_{SU}	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
	4.5	15	—	15	—	19	—	19	—	22	—	22	—	
	6	13	—	—	—	16	—	—	—	19	—	—	—	
$\overline{CE}$ to CP Hold Time t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
MR Removal Time t_{REM}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay CP to any Dec. Out	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
CP to TC	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
$\overline{CE}$ to any Dec. Out	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t_{PHL}	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{CE}$ to TC	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t_{PHL}	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
MR to any Dec. Out	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
MR to TC	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	ns
	t_{PHL}	4.5	—	46	—	46	—	58	—	58	—	69	—	69	
		6	—	39	—	—	—	49	—	—	—	59	—	—	
Transition Time TC, Dec. Out	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4017
CD54/74HCT4017



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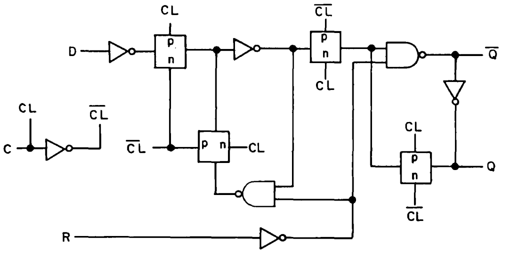
	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
Vs	0.5 V_{CC}	1.3 V

Transition times and propagation delay times.



FF DETAIL

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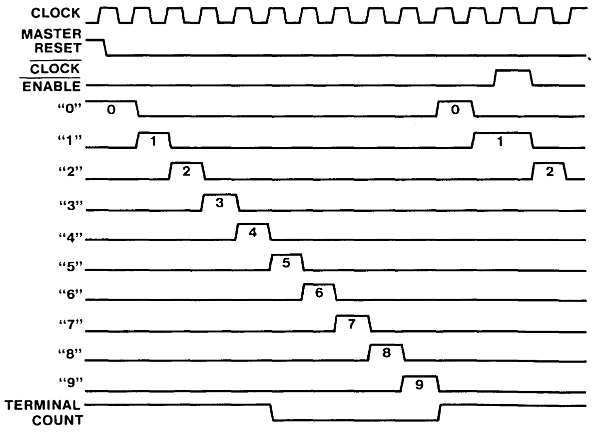


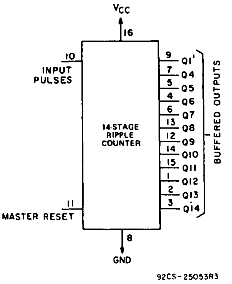
92CM-38463

Timing diagram for the CD54/74HC/HCT4017

CD54/74HC4020
CD54/74HCT4020

File Number **1484**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

14-Stage Binary Counter

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Negative edge pulsing*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15, T_A = 25° C*

The RCA-CD54/74HC4020 and CD54/74HCT4020 are 14-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4020 and CD54HCT4020 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4020 and CD74HCT4020 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

φ	MR	Output State
↗	L	No Change
↘	L	Advance to next state
X	H	All Outputs are low

H = high level (steady state)
L = low level (steady state)
X = don't care

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

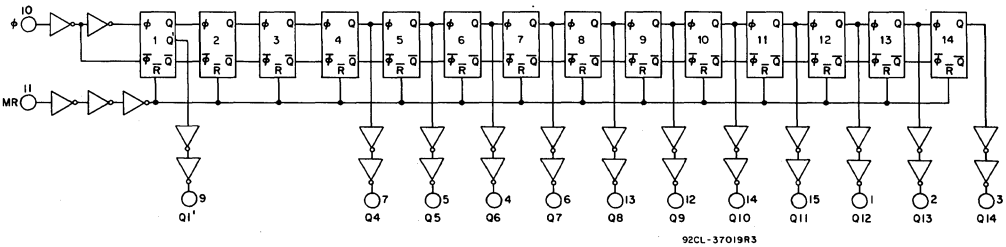


Fig. 1 - Logic block diagram.

CD54/74HC4020
CD54/74HCT4020

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to 125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

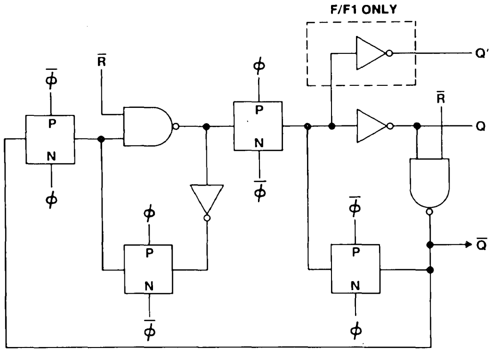


Fig. 2 - Detail for flip-flops 1, 2, 3, 5, 6, 8,10, 11, 13 & 14.

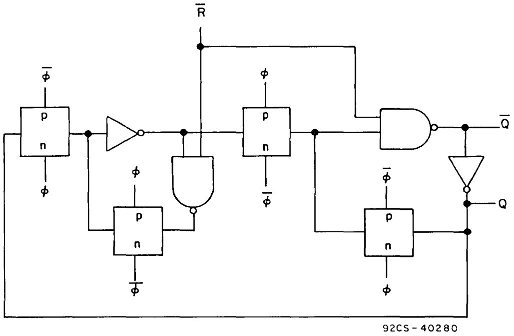


Fig. 3 - Detail for flip-flops 4, 7, 9 & 12.

CD54/74HC4020
CD54/74HCT4020

STATIC ELECTRICAL CHARACTERISTICS

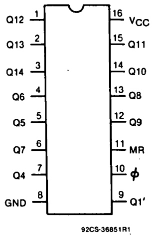
CHARACTERISTIC	CD74HC4020/CD54HC4020										CD74HCT4020/CD54HCT4020									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25° C			-40/ +85° C		-55/ +125° C				+25° C			-40/ +85° C		-55/ +125° C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

***For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.**

HCT Input Loading Table

Input	Unit Loads*
$\overline{MR}$	0.65
∅	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25° C.



TERMINAL ASSIGNMENT

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical HC	Typical HCT	Units
Propagation Delay ϕ to Q1′ Output	t_{PLH} t_{PHL}	15	11	17	ns
Propagation Delay Q_n to Q_{n+1}	t_{PLH} t_{PHL}	15	6	6	ns
Propagation Delay MR to Q_n	t_{PHL}	15	14	17	MHz
Power Dissipation Capacitance*	C_{PD}	—	30	30	pF

*C_{PD} is used to determine the power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_i/M)$ where:
$M = 2^1, 2^4, 2^5 \ldots 2^{14}$
C_L = output load capacitance
fi = input frequency

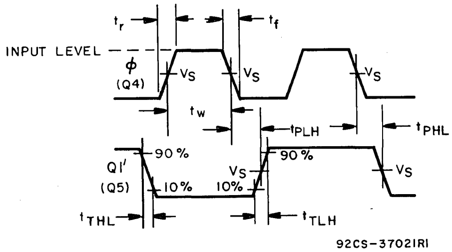
Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C HC Min.	25° C HC Max.	25° C HCT Min.	25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Maximum Input Pulse Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	24	—	—	—	
Input Pulse Width (Figure 4)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time (Figure 5)	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Pulse Width (Figure 5)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

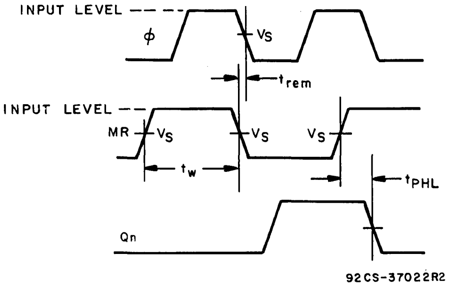
CHARACTERISTIC	SYMBOL	V_{CC}	25° C HC Min.	25° C HC Max.	25° C HCT Min.	25° C HCT Max.	-40° C to +85° C 74HC Min.	-40° C to +85° C 74HC Max.	-40° C to +85° C 74HCT Min.	-40° C to +85° C 74HCT Max.	-55° C to +125° C 54HC Min.	-55° C to +125° C 54HC Max.	-55° C to +125° C 54HCT Min.	-55° C to +125° C 54HCT Max.	UNITS
Propagation Delay ϕ to Q1′ Output (Figure 4)	t_{PLH} t_{PHL}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
		4.5	—	28	—	40	—	35	—	50	—	42	—	60	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay Q_n to Q_{n+1} (Figure 4)	t_{PLH} t_{PHL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Propagation Delay MR to Q_n (Figure 5)	t_{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
Output Transition Time (Figure 4)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4020
CD54/74HCT4020



	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3V
V_S	50%	1.3V

Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times.



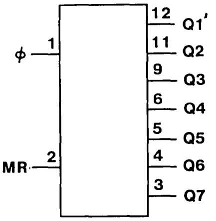
	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3V
V_S	50%	1.3V

Fig. 5 - Master Reset pre-requisite and propagation delays.

File Number **1683**

CD54/74HC4024
CD54/74HCT4024

High-Speed CMOS Logic



92CS-38450RI

CD54/74HC4024, HCT4024 FUNCTIONAL DIAGRAM

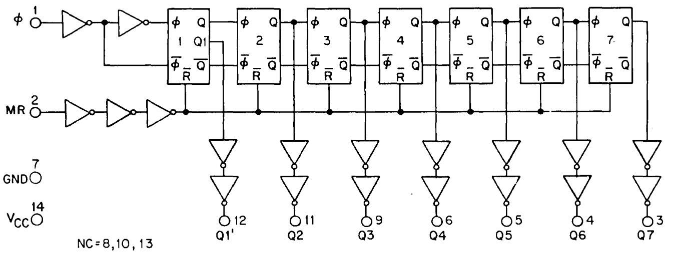
7-Stage Binary Ripple Counter

Type Features:
- *Fully static operation:*
- *Buffered inputs:*
- *Common reset*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC4024 and CD54/75HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4024 and CD54HCT4024 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4024 and CD74HCT4024 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}= 30%, N_{IH}=30% of V_{CC} @ V_{CC} =5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1$ µA @V_{OL}, V_{OH}



92CM-38451R3

Fig. 1 - Logic diagram for the CD54/74HC/HCT4024.

TRUTH TABLE

ϕ	MR	OUTPUT STATE
_/‾	L	No Change
‾_	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

CD54/74HC4024
CD54/74HCT4024

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

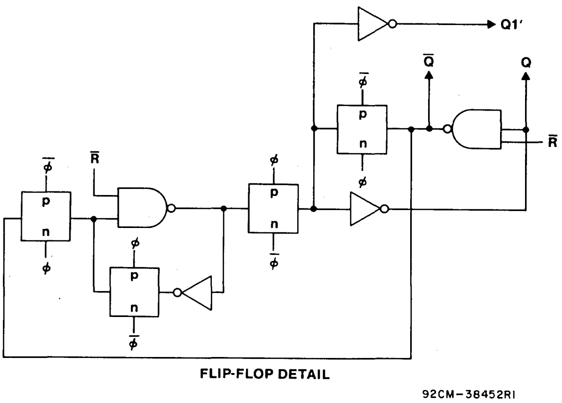


Fig. 2 - Flip-flop No. 1 detail.

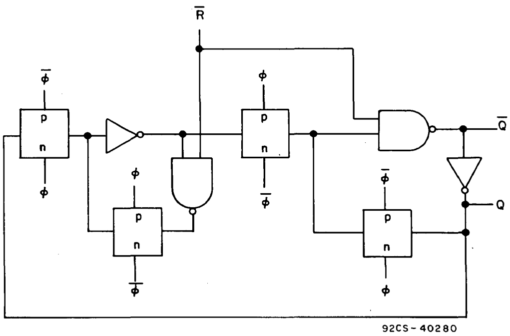


Fig. 3 - Detail for flip-flops 2 through 7.

CD54/74HC4024
CD54/74HCT4024

STATIC ELECTRICAL CHARACTERISTICS

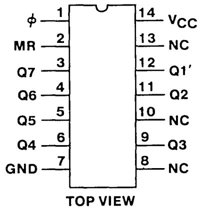
CHARACTERISTICS	CD74HC4024/CD54HC4024										CD74HCT4024/CD54HCT4024									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	--	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ϕ, MR	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max.@25°C.



92CS-38453RI

TERMINAL ASSIGNMENT

CD54/74HC4024
CD54/74HCT4024

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay φ to Q1′	t_{PHL} t_{PLH}	15	11	17	ns
Qn to Qn+1	t_{PHL} t_{PLH}	15	6	6	
MR to Q_n	t_{PHL} t_{PLH}	15	14	17	
Power Dissipation Capacitance*	C_{PD}	—	30	30	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 fi + \Sigma (C_L V_{CC}^2 fi/M)$ where:

$M=2^1,2^2,2^3,2^4,2^5,2^6,2^7$

C_L=output load capacitance

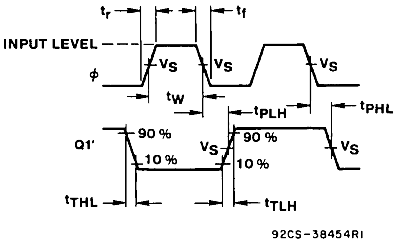
fi=input frequency

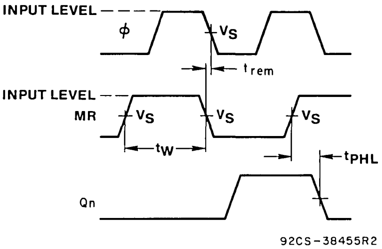
Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	24	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	24	—	—	—	
Input Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, φ to Q1′ Output	t_{PLH} t_{PHL}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
		4.5	—	28	—	40	—	35	—	50	—	42	—	60	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay Qn to Qn+1	t_{PLH} t_{PHL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	13	—	—	—	19	—	—	
Propagation Delay MR to Q_n	t_{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	27	—	—	—	43	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

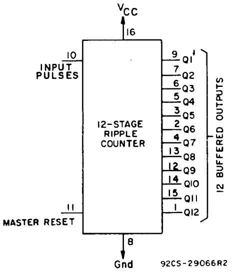
Fig. 4 - Input Pulse pre-requisite times, propagation delays and output transition times.

Fig. 5 - Master Reset pre-requisite and propagation delays.

CD54/74HC4040
CD54/74HCT4040

File Number **1483**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

12-Stage Binary Counter

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Negative edge pulsing*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC4040 and CD54/74HCT4040 are 12-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all stages to their zero state. All inputs and outputs are buffered.

The CD54HC4040 and CD54HCT4040 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4040 and CD74HCT4040 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

ϕ	MR	Output State
_/‾	L	No Change
‾_	L	Advance to next state
X	H	All Outputs are low

H = high level (steady state)
L = low level (steady state)
X = don't care

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL}=0.8 V Max., V_{IH}=2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

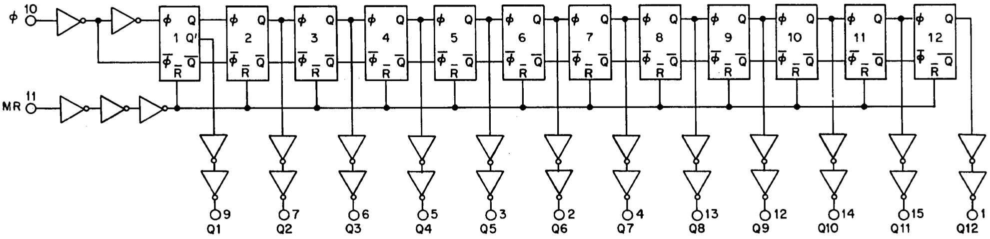


Fig. 1 - Logic block diagram.

92CL-37015R3

CD54/74HC4040
CD54/74HCT4040

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r,t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

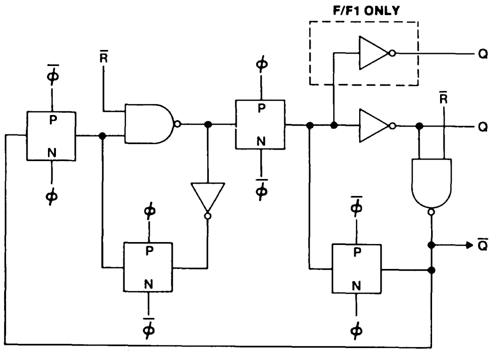


Fig. 2 - Detail for flip-flops 1, 2, 4, 5, 7, 8, 10 & 11.

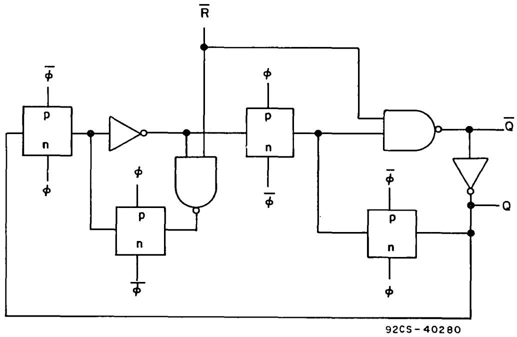


Fig. 3 - Detail for flip-flops 3, 6, 9 & 12.

CD54/74HC4040
CD54/74HCT4040

STATIC ELECTRICAL CHARACTERISTICS

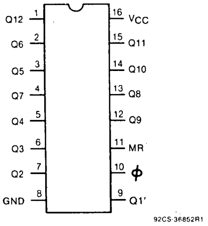
CHARACTERISTIC	CD74HC4040/CD54HC4040											CD74HCT4040/CD54HCT4040									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	--	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{MR}$	0.65
φ	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical		
			HC	HCT	Units
Propagation Delay ϕ to Q1′ Output	t_{PLH} t_{PHL}	15	11	17	ns
Propagation Delay Q_n to Q_{n+1}	t_{PHL} t_{PHL}	15	4	4	ns
Propagation Delay to MR to Q_n	t_{PHL}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	40	45	pF

*C_{PD} is used to determine the power consumption, per package.
$PD = C_{PD} V_{CC}^2 fi + \Sigma (C_L V_{CC}^2 fi/M)$ where:
$M = 2^1, 2^2, 2^3, .. 2^{12}$
C_L = output load capacitance
fi = input frequency

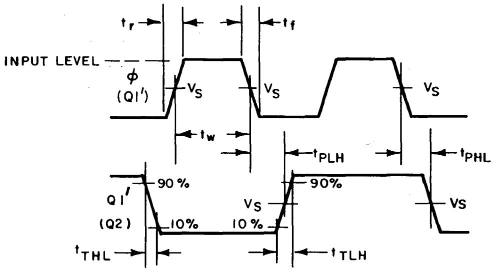
Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	24	—	—	—	
Input Pulse Width (Figure 4)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time (Figure 5)	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Pulse Width (Figure 5)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay ϕ to Q1′ Output (Figure 4)	t_{PLH} t_{PHL}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
		4.5	—	28	—	40	—	35	—	50	—	42	—	60	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay Q_n to Q_{n+1} (Figure 4)	t_{PLH} t_{PHL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Propagation Delay MR to Q_n (Figure 5)	t_{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	37	—	—	—	43	—	—	
Output Transition Time (Figure 4)	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

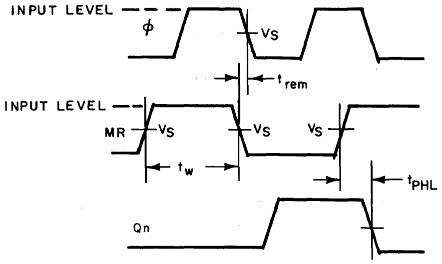
CD54/74HC4040
CD54/74HCT4040



	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3V
V_S	50%	1.3V

92CS-37017

Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times.



	54/74 HC	54/74 HCT
INPUT LEVEL	V_{CC}	3V
V_S	50 % V_{CC}	1.3V

92CS-37018R1

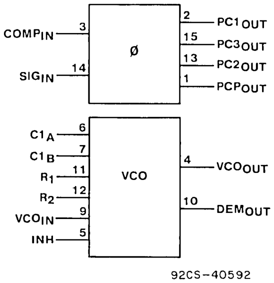
Fig. 5 - Master Reset pre-requisite and propagation delays.

File Number **1854**

**Advance Information/
Preliminary Data**

CD54/74HC 4046A
CD54/74HCT 4046A

High-Speed CMOS Logic



92CS-40592

FUNCTIONAL DIAGRAM

Phase-Locked-Loop with VCO

Features:

- *Operating frequency range of up to 18 MHz (typ.) at V_{CC} = 5 V*
- *Choice of three phase comparators: EXCLUSIVE-OR: edge-triggered JK flip-flop; edge-triggered RS flip-flop*
- *Excellent VCO frequency linearity*
- *VCO-inhibit control for ON/OFF keying and for low standby power consumption*
- *Minimal frequency drift*
- *Operating power supply voltage range: VCO section 3 V to 6 V; digital section 2 V to 6 V*

Applications:

- *FM modulation and demodulation*
- *Frequency synthesis and multiplication*
- *Frequency discrimination*
- *Tone decoding*
- *Data synchronization and conditioning*
- *Voltage-to-frequency conversion*
- *Motor-speed control*

The RCA CD54/74 HC/HCT4046A are high-speed Si-gate CMOS devices that are pin compatible with the CD4046B of the "4000B" series. They are specified in compliance with JEDEC standard no. 7

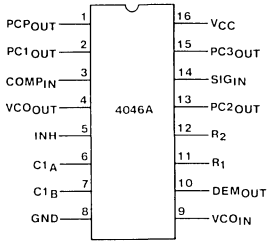
The HC/HCT4046A are phase-locked-loop circuits that contain a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The CD54HC4046A and CD54HCT4046A are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC4046A and CD74HCT4046A are supplied in 16-lead plastic dual-in-line packages (E suffix), and in 16-lead surface mount plastic dual-in-line packages (M suffix). The CD54/74HC/HCT4046A are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range);*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1$ μA @ V_{OL}, V_{OH}



92CS-40591

TERMINAL ASSIGNMENT

CD54/74HC4046A
CD54/74HCT4046A

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (for $-0.5\text{ V} < V_O < V_{CC} + 0.5$ V) .... ±25 mA
DC V_{CC} OR GOUND CURRENT (I_{CC}): .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always with the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (for T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. See logic diagram, Fig. 1.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a guaranteed duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

Phase Comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an Exclusive-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/\pi)\ (\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 2. The average of V_{DEM} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 3.

CD54/74HC4046A
CD54/74HCT4046A

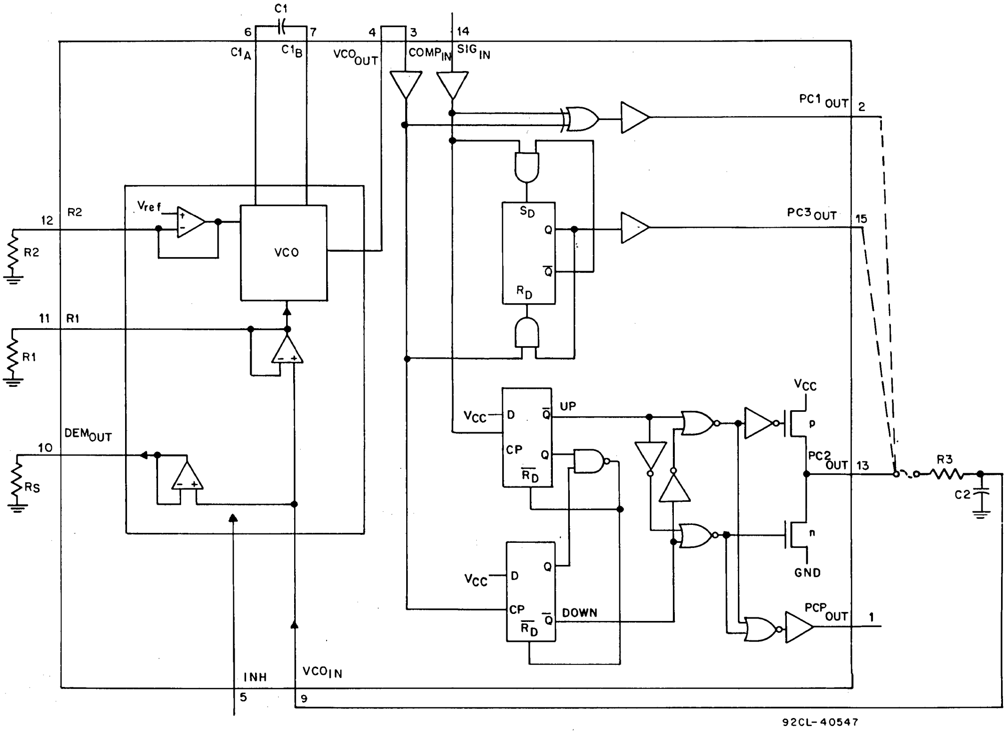


Fig. 1 — Logic diagram.

The frequency capture range ($2f_C$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy input signals. Typical of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

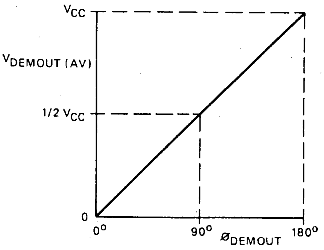


Fig. 2 — Phase comparator 1: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)(\phi_{SIGIN} - \phi_{COMPIN})$;
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

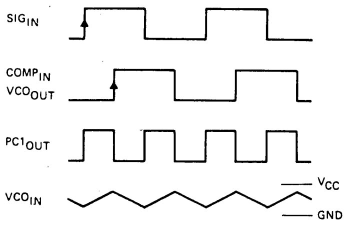


Fig. 3 — Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 1) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUNT} = (V_{CC}/4\pi)(\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10: $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 4. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 5.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n- and p-type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p- and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN}, the VCO adjusts, via PC2, to its lowest frequency.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/2\pi)(\phi_{SIGIN} - \phi_{COMPIN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 6. Typical waveforms for the PC3 loop locked at f_o are shown in Fig.7.

The phase-to-output response characteristic of PC3 (Fig. 6) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the center frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. With no signal present at SIG_{IN}, the VCO adjusts, via PC3, to its highest frequency.

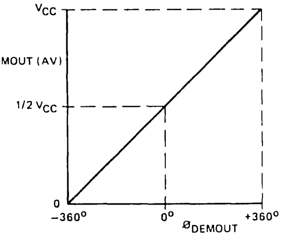


Fig 4 — Phase comparator 2: average output voltage versus input phase difference: $V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/4\pi)(\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

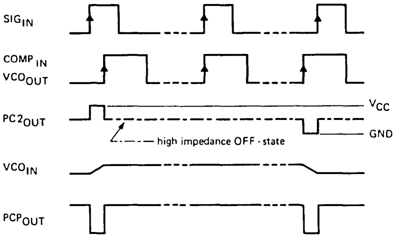


Fig. 5 — Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

The only difference between the HC and the HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and the HCT versions.

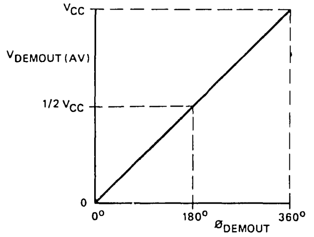


Fig.6 — Phase comparator 3: average output voltage versus input phase difference: $V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)(\phi_{SIGIN} - \phi_{COMPIN})$; $\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

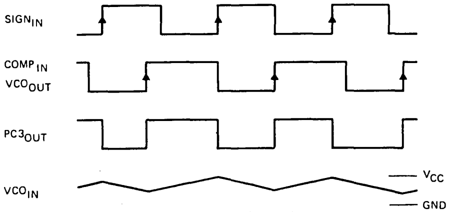


Fig. 7 — Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

CD54/74HC4046A
CD54/74HCT4046A

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
VCO SECTION	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
INH High-Level Input Voltage V_{IH}			3	2.1	—	—	2.1	—	2.1	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
INH Low-Level Input Voltage V_{IL}			3	—	—	0.9	—	0.9	—	0.9		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8		5.5								
VCO_{OUT} High-Level Output Voltage V_{OH}	V_{IL}		3	2.9	—	—	2.9	—	2.9	—	V_{IL}									
	or	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	V
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
VCO_{OUT} Low-Level Output Voltage V_{OL}	V_{IL}		2	—	—	0.1	—	0.1	—	0.1	V_{IL}									
	or	0.02	4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	V
CMOS Loads	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
	V_{IL}										V_{IL}									
TTL Loads	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
C1A, C1B Low Level Output Voltage (Test purposes V_{OL} only)	V_{IL}										V_{IL}									
	or	4	4.5	—	—	0.40	—	0.47	—	0.54	or	4.5	—	—	0.40	—	0.47	—	0.54	V
	V_{IH}	5.2	6	—	—	0.40	—	0.47	—	0.54	V_{IH}	—	—	—	—	—	—	—	—	
INH VCO_{IN} Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
R1 Range			3	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	
			4.5	3	—	300	—	—	—	—		4.5	3	—	300	—	—	—	—	kΩ
			6	—	—	—	—	—	—	—		—	—	—	—	—	—	—	—	
R2 Range			3	—	—	—	—	—	—	—			—	—	—	—	—	—	—	
			4.5	3	—	300	—	—	—	—			3	—	300	—	—	—	—	kΩ
			6	—	—	—	—	—	—	—			—	—	—	—	—	—	—	
C1 Capacitance Range			3 4.5 6	0		No LIMIT							0		No LIMIT					pF
VCO_{IN} Operating Voltage Range	Over the range specified for R1 for Linearity **See Figs. 8 & 35-38** See Note 2		3	0.9		1.9														
			4.5	0.9		3.2						4.5	0.9		3.2					V
			6	0.9		4.6														

NOTES: 1. The value for R1 & R2 in parallel should exeed 2.7 kΩ.
2. The maximum operating voltage can be as high as V_{CC} -0.9 V, however, this may result in an increased offset voltage.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
PHASE COMPARATOR SECTION	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
PCP_{OUT}, PCn OUT High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
PCP_{OUT}, PCn OUT Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
SIG_{IN}, $COMP_{IN}$ Input Leakage Current I_I	V_{CC} or Gnd		2	—	—	±3	—	±4	—	±5	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±30	—	±38	—	±45	μA
			3	—	—	±7	—	±9	—	±11										
			4.5	—	—	±18	—	±23	—	±29										
			6	—	—	±30	—	±38	—	±45										
PC2 OUT 3-State Off-State Current I_{OZ}	V_{IL} or V_{IH}		6	—	—	±0.5	—	±5	—	±10		5.5	—	—	±0.5	±5	—	—	±10	μA
SIG_{IN}, $COMP_{IN}$ Input Resistance R_I	V_I at Self-Bias Oper. Point: $\Delta V_I = 0.5$ V See Fig. 8		3	—	800	—	—	—	—	—		4.5	—	250	—	—	—	—	—	kΩ
			4.5	—	250	—	—	—	—	—										
			6	—	150	—	—	—	—	—										

CD54/74HC4046A
CD54/74HCT4046A

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4046A/CD54HC4046A										CD74HCT4046A/CD54HCT4046A									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
DEMODULATOR SECTION	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
Resistor Range R_s	at $R_s > 300$ kΩ Leakage Current can influence $V_{DEM\,OUT}$		3	50	—	300														kΩ
			4.5	50	—	300						4.5	5	—	300					
			6	50	—	300														
Offset Voltage VCO_{IN}, to V_{DEM} V_{OFF}	$V_I = V_{VCO\,IN} = \frac{V_{CC}}{2}$ Values taken over R_S range See Fig. 15		3	—	±30	—														mV
			4.5	—	±20	—						4.5	—	±20	—					
			6	—	±10	—														
Dynamic Output Resistance at DEM_{OUT} R_D	$V_{DEM\,OUT} = \frac{V_{CC}}{2}$		3	—	25	—														Ω
			4.5	—	25	—						4.5	—	25	—					
			6	—	25	—														
Quiescent Device Current I_{CC}	Pins 3, 5 & 14 at V_{CC} Pin 9 at Gnd. I_1, at Pins 3 & 14 to be excluded		6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current Per Input Pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1 (Excluding Pin 5)	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
INH	1

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4046A
CD54/74HCT4046A

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITIONS		25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		V_{CC}	HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
PHASE COMPARATOR SECTION															
Propagation Delay,		2	—	200	—	—	—	250	—	—	—	300	—	—	ns
SIG_{IN}, $COMP_{IN}$ t_{PLH}		4.5	—	40	—	45	—	50	—	56	—	60	—	68	
to PCI_{OUT} t_{PHL}		6	—	34	—	—	—	43	—	—	—	51	—	—	
SIG_{IN}, $COMP_{IN}$		2	—	300	—	—	—	375	—	—	—	450	—	—	
to PCP_{OUT}		4.5	—	60	—	68	—	75	—	85	—	90	—	102	
		6	—	70	—	—	—	88	—	—	—	109	—	—	
SIG_{IN}, $COMP_{IN}$		2	—	245	—	—	—	305	—	—	—	307	—	—	
to $PC3_{OUT}$		4.5	—	49	—	58	—	61	—	73	—	74	—	87	
		6	—	42	—	—	—	52	—	—	—	63	—	—	
Output Transition		2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
t_{TLH}		6	—	13	—	—	—	16	—	—	—	19	—	—	
Output Enable Time,		2	—	265	—	—	—	330	—	—	—	400	—	—	
SIG_{IN}, $COMP_{IN}$ t_{PZH}		4.5	—	53	—	60	—	66	—	75	—	80	—	90	
to $PC2_{OUT}$ t_{PZL}		6	—	45	—	—	—	56	—	—	—	68	—	—	
Output Disable Time,		2	—	315	—	—	—	395	—	—	—	475	—	—	
SIG_{IN}, $COMP_{IN}$ t_{PHZ}		4.5	—	63	—	68	—	79	—	85	—	95	—	102	
to $PC2_{OUT}$ t_{PLZ}		6	—	74	—	—	—	93	—	—	—	112	—	—	
AC Coupled Input			TYPICAL												
Sensitivity (p-p)	V_I (p-p)	3	11		11										mV
at SIG_{IN} or		4.5	15		15										
$COMP_{IN}$		6	33		33										
VCO SECTION															
Frequency Stability with Temperature Change $\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ R_2 = ∞	3 4.5 6	0.11		0.11										%/°C
Max. Frequency f_{max}	C_1 = 50 pF R_1 = 3.5kΩ R_2 = ∞	3 4.5 6	24		24										MHz
	C_1 = 0 pF R_1 = 9.1kΩ R_2 = ∞	3 4.5 6	38		38										MHz
Center Frequency	C_1 = 40 pF R_1 = 3kΩ R_2 = ∞ $VCO_{IN} = \frac{V_{CC}}{2}$	3 4.5 6	17		17										MHz
Frequency Linearity, Δf_{VCO}	R_1 = 100kΩ R_2 = ∞ C_1 = 100 pF	3 4.5 6	0.4		0.4										%
Offset Frequency	R_2 = 220kΩ C_1 = 1 nF	3 4.5 6	400		400										kHz
DEMODULATOR SECTION															
V_{OUT} Vs f_{IN}	R_1 = 100 kΩ R_2 = ∞ C_1 = 100 pF R_S = 10 kΩ R_3 = 100 kΩ C_2 = 100 pF	3 4.5 6	— 330 —		— 330 —										mV/kHz

CD54/74HC4046A
CD54/74HCT4046A

Figure References for DC Characteristics

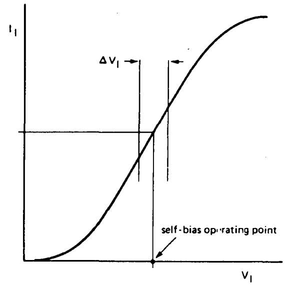


Fig. 8 — Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

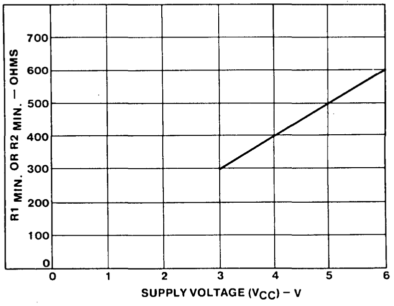


Fig. 9-HC/HCT4046A R1 (min) or R2 (min) vs supply voltage (V_{CC}).

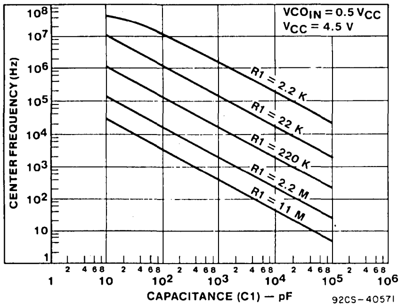


Fig. 10-HCT4046A typical center frequency vs R1, C1 (V_{CC}=4.5 V).

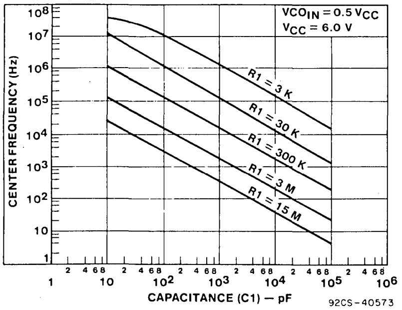


Fig. 11-HC4046A typical center frequency vs R1, C1 (V_{CC}=6 V).

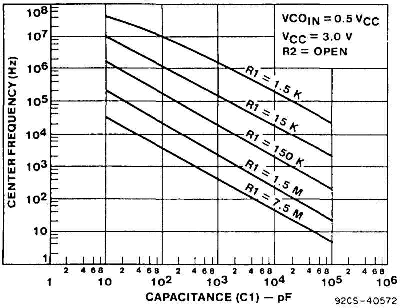


Fig. 12-HC4046A typical center frequency vs R1, C1 (V_{CC}=3 V, R2=open).

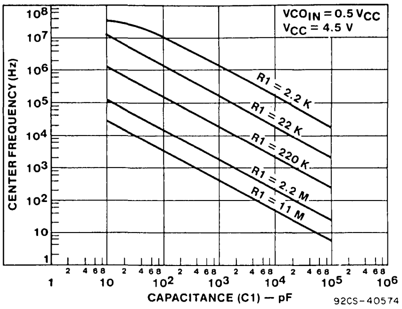


Fig. 13-HCT4046A typical center frequency vs R1, C1 (V_{CC}=4.5 V).

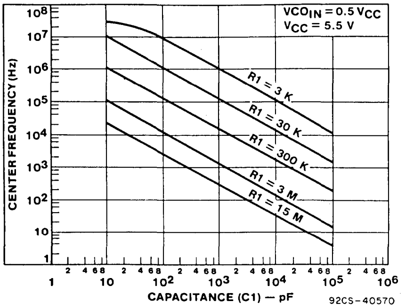


Fig. 14-HCT4046A typical center frequency vs R1, C1 (V_{CC}=5.5 V).

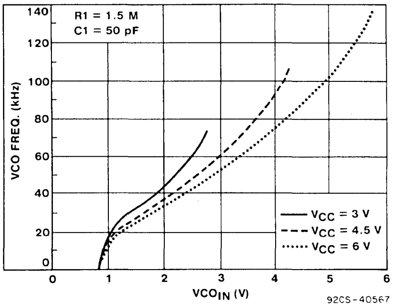


Fig. 15-HC4046A typical VCO frequency vs VCO_{IN} (R1=1.5 MΩ, C1=50 pF).

CD54/74HC4046A
CD54/74HCT4046A

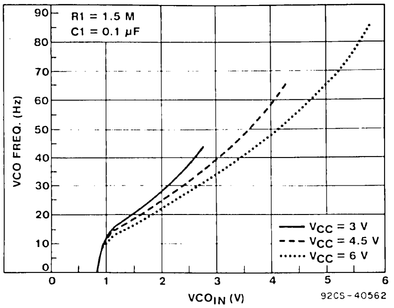


Fig. 16-HC4046A typical VCO frequency vs VCO$_{IN}$ (R1=1.5 MΩ, C1=0.1 µF).

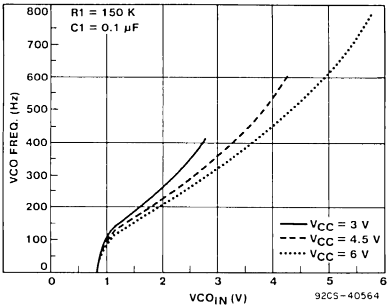


Fig. 17-HC4046A typical VCO frequency vs VCO$_{IN}$ (R1=150 kΩ, C1=0.1 µF).

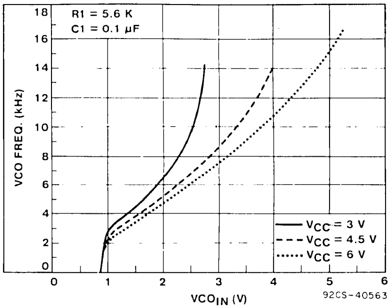


Fig. 18-HC4046A typical VCO frequency vs VCO$_{IN}$ (R1=5.6 kΩ, C1=0.1 µF).

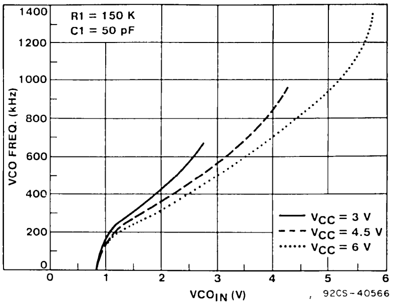


Fig. 19-HC4046A typical VCO frequency vs VCO$_{IN}$ (R1=150 kΩ, C1=50 pF).

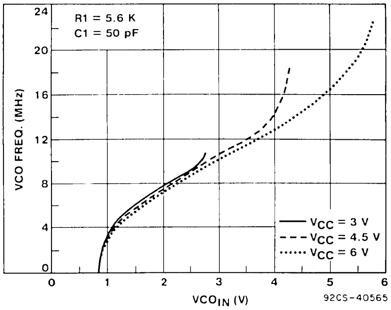


Fig. 20-HC4046A typical VCO frequency vs VCO$_{IN}$ (R1=5.6 kΩ, C1=50 pF).

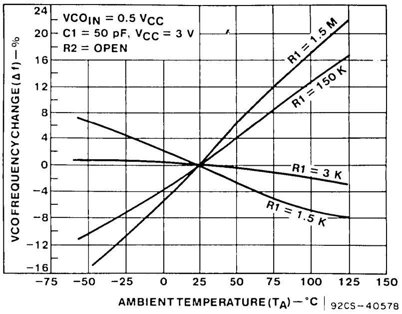


Fig. 21-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 (V$_{CC}$=3 V).

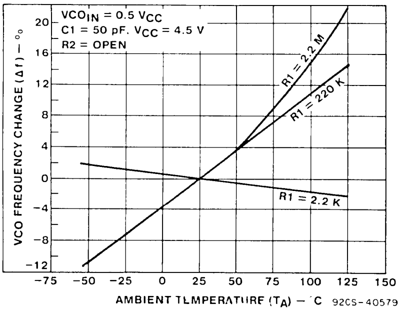


Fig. 22-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 (V$_{CC}$=4.5 V).

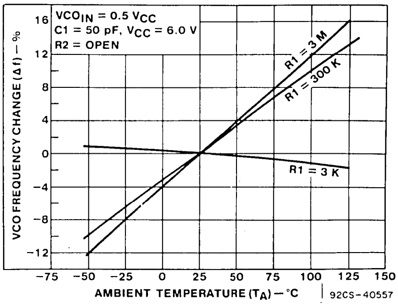


Fig. 23-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 (V$_{CC}$=6 V).

CD54/74HC4046A
CD54/74HCT4046A

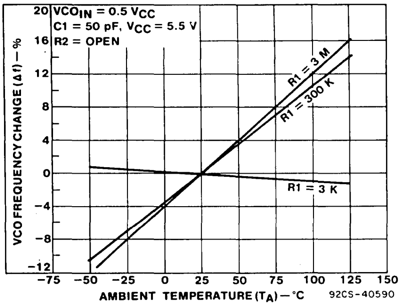


Fig. 24-HCT4046A typical change in VCO frequency vs ambient temperature as a function of R1.

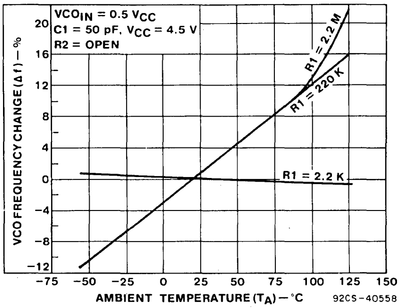


Fig. 25-HC4046A typical change in VCO frequency vs ambient temperature as a function of R1 (V$_{CC}$=4.5 V).

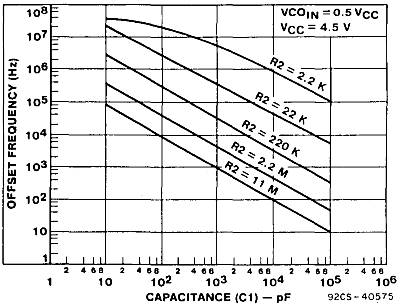


Fig. 26-HC4046A offset frequency vs R2, C1 (V$_{CC}$=4.5 V).

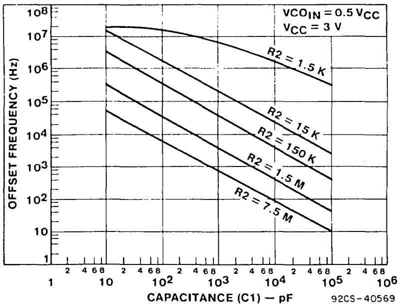


Fig. 27-HC4046A offset frequency vs R2, C1 (V$_{CC}$=3 V).

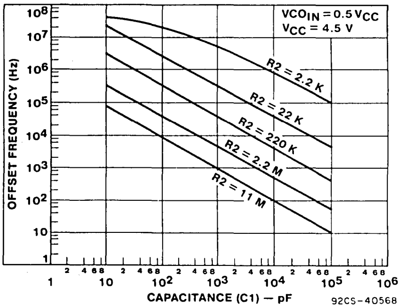


Fig. 28-HCT4046A offset frequency vs R2, C1 (V$_{CC}$=4.5 V).

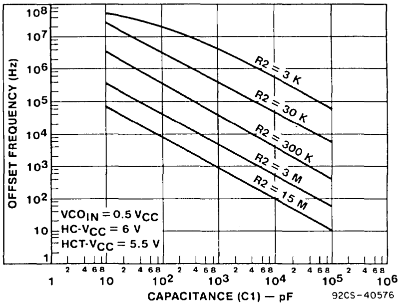


Fig. 29-HC4046A & HCT4046A offset frequency vs R2, C1 (V$_{CC}$=6 V, V$_{CC}$=5.5 V).

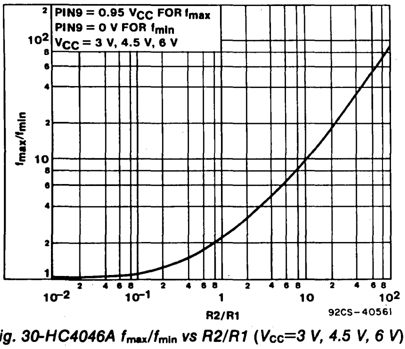


Fig. 30-HC4046A f$_{max}$/f$_{min}$ vs R2/R1 (V$_{CC}$=3 V, 4.5 V, 6 V).

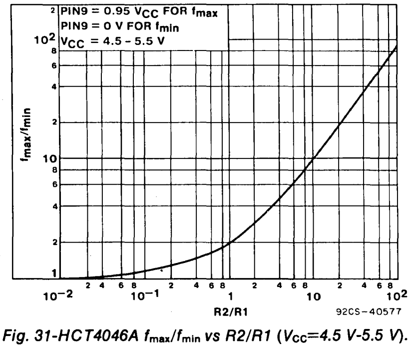


Fig. 31-HCT4046A f$_{max}$/f$_{min}$ vs R2/R1 (V$_{CC}$=4.5 V-5.5 V).

AC WAVEFORMS

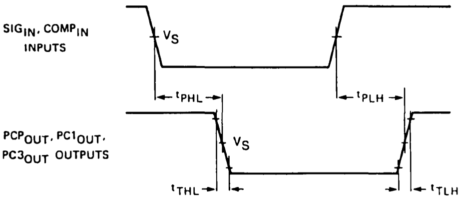


Fig. 32 — Waveforms showing input (SIG_{IN} $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.

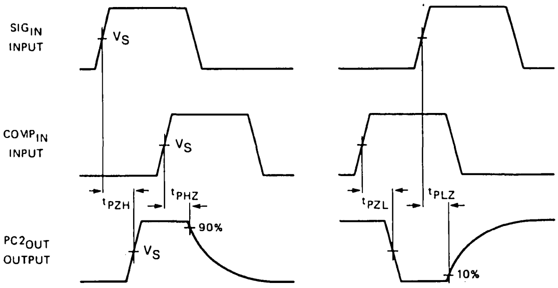
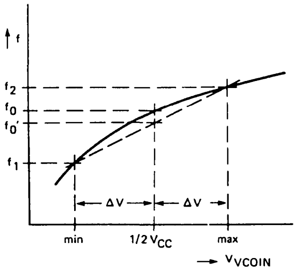


Fig. 33 — Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

	HC	HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V



ΔV = 0.5 V over the V_{CC} range:

for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

Fig. 34 — Definition of VCO frequency linearity.

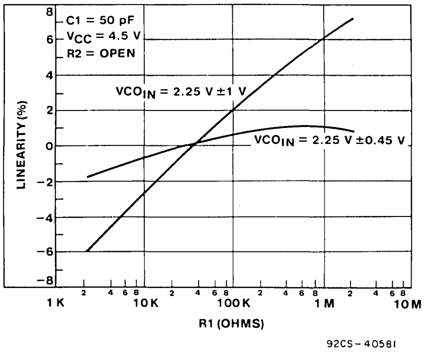


Fig. 35-HC4046A VCO linearity vs R1 (V_{CC}=4.5 V).

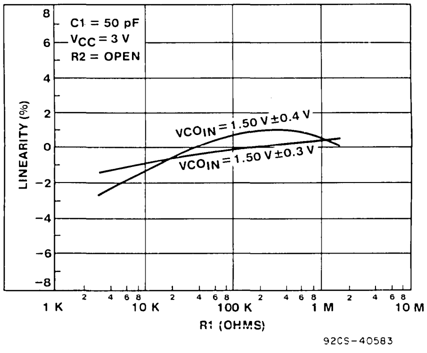


Fig. 36-HC4046A VCO linearity vs R1 (V_{CC}=3 V).

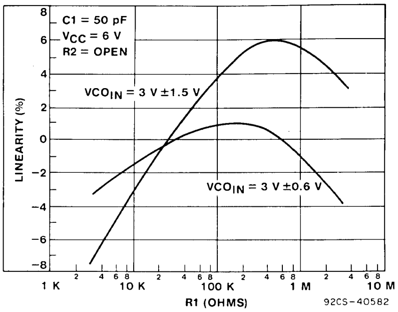


Fig. 37-HC4046A VCO linearity vs R1 (V_{CC}=6 V).

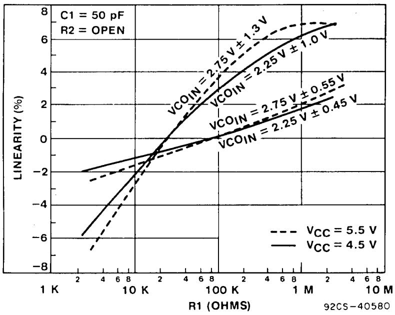


Fig. 38-HCT4046A VCO linearity vs R1 (V_{CC}=4.5 V, V_{CC}=5.5 V).

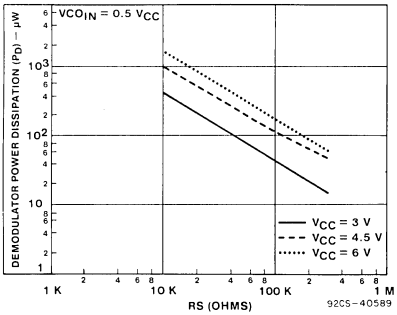


Fig. 39-HC4046A demodulator power dissipation vs RS (typ.) (V_{CC}=3 V; 4.5 V; 6 V).

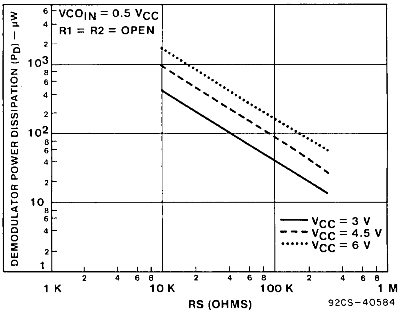


Fig. 40-HCT4046A demodulator power dissipation vs RS (typ.) (V_{CC}=3 V; 4.5 V; 6 V).

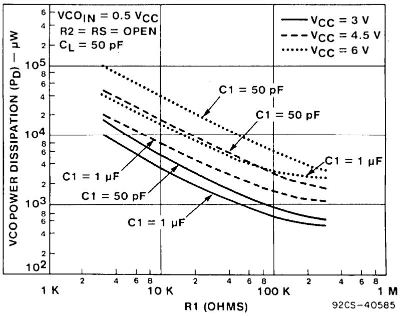


Fig. 41-HC4046A VCO power dissipation vs R1 (C1=50 pF; 1 µF).

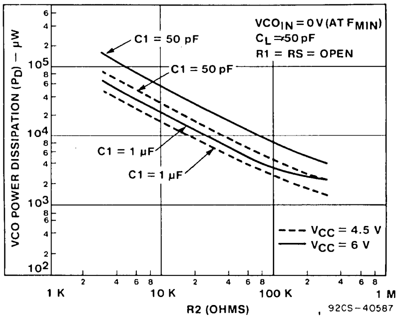


Fig. 42-HCT4046A VCO power dissipation vs R2 (C1=50 pF; 1 µF).

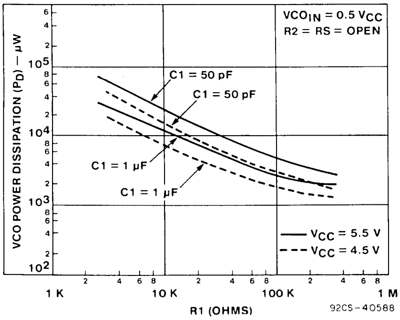


Fig. 43-HCT4046A VCO power dissipation vs R1 (C1=50 pF; 1 µF).

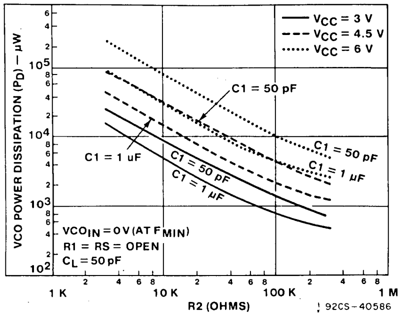


Fig. 44-HC4046A VCO power dissipation vs R2 (C1=50 pF, 1 µF).

HC/HCT 4046A C_{PD}

CHIP SECTION	HC	HCT	UNIT
COMPARATOR 1	48	50	pF
COMPARATORS 2 & 3	39	48	
VCO	61	53	

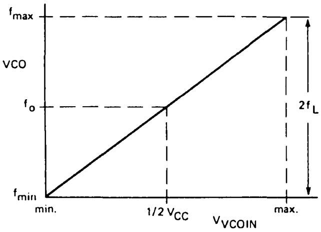
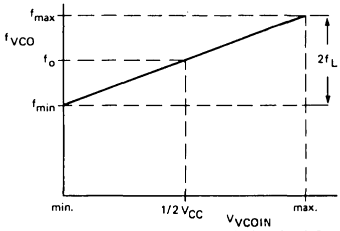
APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs.10 through 14 as indicated in the table.

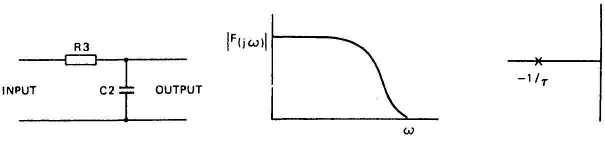
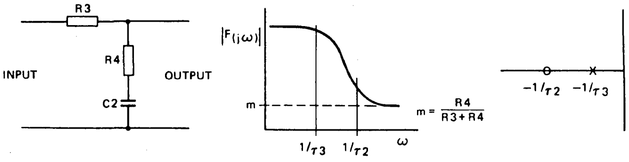
Values of the selected components should be within the following ranges.

R1	between 3 kΩ and 300 kΩ;
R2	between 3 kΩ and 300 kΩ;
R1 + R2	parallel value > 2.7 kΩ;
C1	greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO Frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Figs. 10-14. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  *Fig. 45— Frequency characteristic of VCO operating without offset: f_o = center frequency: $2f_L$ = frequency lock range.*
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Figs. 10-14.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 30. Use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ, < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Figs. 26-29.  *Fig. 46 — Frequency characteristic of VCO operating with offset: f_o = center frequency; $2f_L$ = frequency lock range.*

CD54/74HC4046A
CD54/74HCT4046A

APPLICATION INFORMATION (Cont'd.)

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **with** offset (continued)	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Figs. 26-29. Calculate f_{off} from equation $f_{off} = f_{CO} = f_L$. Obtain the values of C1 and R2 by using Figs. 26-29. Calculate the value of R1 from the value of C1 and the product R1C1.
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with $\phi_{DEMOUT} = 90°$ and $V_{VCOIN} = 1/2\ V_{CC}$ (see Fig. 2).
	PC2	VCO adjusts to f_o with $\phi_{DEMOUT} = -360°$ and $V_{VCOIN} = 0$ V (see Fig. 4).
	PC3	VCO adjusts to f_o with $\phi_{DEMOUT} = +360°$ and $V_{VCOIN} = V_{CC}$ (see Fig. 6).
PLL Frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) $\tau = R3 \times C2$ (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $\tau > 2f_c \approx 1/\pi\ (2\pi f_L/\tau.)^{1/2}$ *Fig. 47— Simple loop filter for PLL without offset.*  (a) $\tau_1 = R3 \times C2$; (b) amplitude characteristic (c) pole-zero diagram $\tau_2 = R4 \times C2$; $\tau_3 \doteq (R3 + R4) \times C2$ *Fig. 48 - Simple loop filter for PLL with offset.*

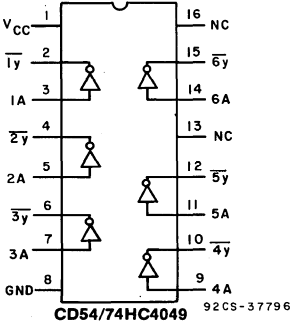
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL locks on harmonics at center frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at $\phi_{DEMOUT} = 90°$
	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0°$
	PC3	$f_r = f_{SIG_{IN}}$, large ripple content at $\phi_{DEMOUT} = 180°$

CD54/74HC4049
CD54/74HC4050

File No. **1543**

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC4049 92CS-37796

Hex Buffers, Inverting and Non-Inverting

Type Features

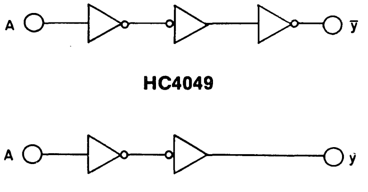
- *Typical propagation delay = 6 ns @ $V_{CC} = 5$ V, $C_L = 15$pF, $T_A = 25°$C*
- *High-to-low voltage level converter for up to $V_I = 16$ V*

The RCA-CD54/74HC4049 and CD54/74HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be used as logic level translators which will convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 0-V to 15-V input logic levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from both positive and negative electrostatic discharge. These parts can also be used as simple buffers or inverters without level translation. The CD54/74HC4049 and CD54/74HC4050 are enhanced versions of equivalent CMOS types.

The CD54HC4049 and CD54/74HC4050 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix) and in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: $N_{IL} = 30\%$, V_{CC}, $N_{IH} = 30\%$ V_{CC}; @ $V_{CC} = 5$ V*



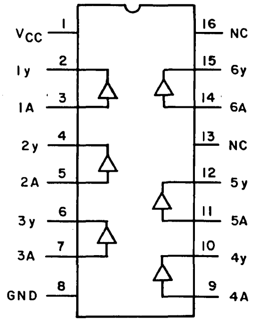
HC4049

HC4050

92CS-37797

LOGIC DIAGRAMS

FUNCTIONAL DIAGRAM



92CS-37798

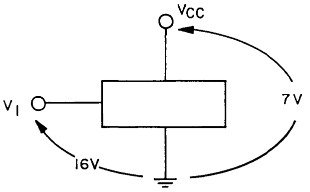
CD54/74HC4050

CD54/74HC4049
CD54/74HC4050

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC})	-0.5 to +7 V
DC INPUT VOLTAGE, (V_I) (Voltages referenced to ground)	-0.5 to +16 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V)	-20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_o < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

Voltage Relationships:
(Maximum Positive Limits)



92CS-37799RI

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
DC Output Voltage, V_O	0	V_{CC}	V
DC Input Voltage (V_I)	0	15	V
Operating Temperature, T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4049
CD54/74HC4050

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD54/74HC4049, CD54/74HC4050										UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		
	V_I V	I_O mA	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	V
			4.5	3.15	—	—	3.15	—	3.15	—	
			6	4.2	—	—	4.2	—	4.2	—	
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	V
			4.5	—	—	1.35	—	1.35	—	1.35	
			6	—	—	1.8	—	1.8	—	1.8	
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V
			4.5	4.4	—	—	4.4	—	4.4	—	
			6	5.9	—	—	5.9	—	5.9	—	
TTL Loads (Standard Output)	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—	
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1	
			6	—	—	0.1	—	0.1	—	0.1	
TTL Loads (Standard Output)	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4	
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	μA
	15		6	—	—	±0.5	—	±5	—	±5	
Quiescent Device Current I_{CC}	15 or Gnd	0	6	—	—	2	—	20	—	40	μA

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		SYMBOL	54HC AND 74HC	
			TYPICAL	UNITS
Propagation Delay, Data Input to Output (C_L = 15 pF)	HC4049 HC4050	t_{PLH}, t_{PHL}	6	ns
Power Dissipation Capacitance*		C_{PD}	35	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter
$P_D = V_{CC}^2 f_i(C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C		-40° C to +85° C		-55° C to +125° C		UNITS
			HC		74HC		54HC		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay nA to n$\overline{Y}$ HC4049 nA to nY HC4050	t_{PLH}, t_{PHL}	2	—	85	—	105	—	130	ns
		4.5	—	17	—	21	—	26	
		6	—	14	—	18	—	22	
Transition Time	t_{TLH}, t_{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	—	10	—	10	—	10	pF

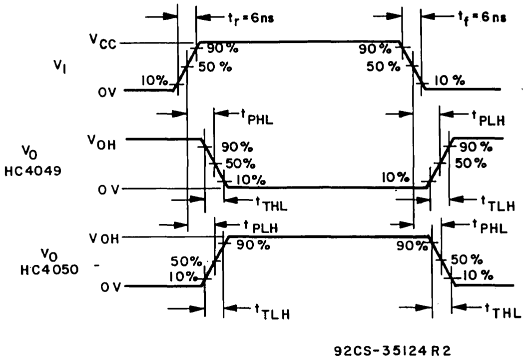
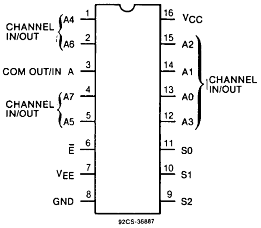


Fig. 1 - Transition times and propagation delay times, combination logic.

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053
High-Speed CMOS Logic

File Number **1676**



CD54/74HC/HCT4051
TERMINAL ASSIGNMENT

Analog Multiplexers/ Demultiplexers

Type Features:

- *Wide analog input voltage range: ± 5 V max.*
- *Low "on" resistance:*
  70 Ω typ (V_{CC}-V_{EE} = 4.5 V)
  40 Ω typ (V_{CC}-V_{EE} = 9 V)
- *Low crosstalk between switches*
- *Fast switching and propagation speeds*
- *"Break-before-make" switching*

The RCA CD54/74HC/HCT4051, 4052, and 4053 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They' are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which when, high, disables all switches to their "off" state.

The CD54HC/HCT4051, 4052, and 4053 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT 4051, 4052, and 4053 are supplied in 16-lead plastic packages (E suffix) and in 16-lead surface mount plastic packages (M suffix). All devices are also available in chip form (H suffix).

Family Features:

- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation, control; 0 to 10 V, switch
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation, control; 0 to 10 V, switch
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

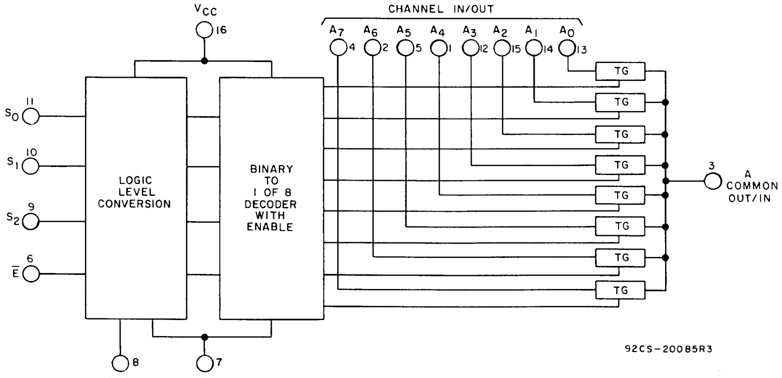


Fig. 1 - Functional diagram of HC/HCT4051.

TRUTH TABLE

CD54/74HC/HCT4051

INPUT STATES				"ON"
ENABLE	**S2**	**S1**	**S0**	**CHANNELS**
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	NONE

X = Don't Care

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

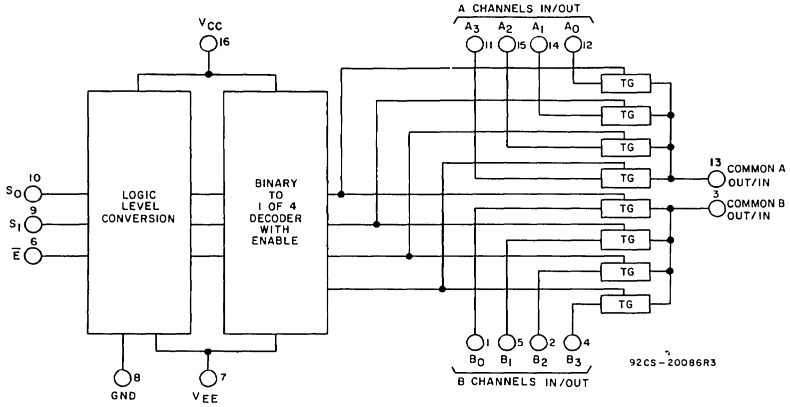
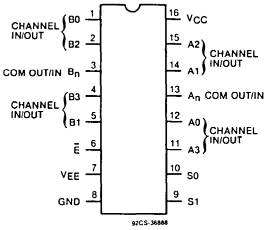


Fig. 2 - Functional diagram of HC/HCT4052.



CD54/74HC/HCT4052 TERMINAL ASSIGNMENT

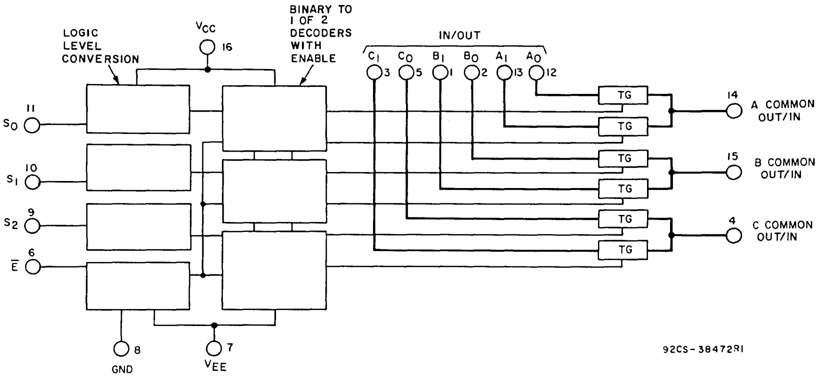
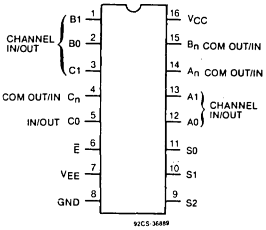


Fig. 3 - Functional diagram of HC/HCT4053.



CD54/74HC/HCT4053 TERMINAL ASSIGNMENT

TRUTH TABLES (Continued)

CD54/74HC/HCT4052

INPUT STATES			"ON" CHANNELS
ENABLE	S1	S0	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2, B2
L	H	H	A3. B3
H	X	X	NONE

X = Don't Care

CD54/74HC/HCT4053

INPUT STATES				"ON" CHANNELS
ENABLE	S2	S1	S0	
L	L	L	L	A0 B0 CO
L	L	L	H	A0 B0 C1
L	L	H	L	A0 B1 CO
L	L	H	H	A0 B1 C1
L	H	L	L	A1 B0 CO
L	H	L	H	A1 B0 C1
L	H	H	L	A1 B1 CO
L	H	H	H	A1 B1 C1
H	X	X	X	NONE

X = Don't Care

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

MAXIMUM RATINGS, *Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)*

DC SUPPLY-VOLTAGE (V_{CC}-V_{EE})	-0.5 to 11 V
DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to +7 V
DC SUPPLY-VOLTAGE (V_{EE})	+0.5 to -7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_i < V_{EE}$ -0.5 V OR $V_i > V_{CC} + 0.5$ V)	±20 mA
• DC SWITCH CURRENT (FOR $V_i > V_{EE}$ -0.5 V OR $V_i < V_{CC} + 0.5$ V)	+25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
DC V_{EE} CURRENT (I_{EE})	-20 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	**400 mW**
For T_A = +70 to +125° C (PACKAGE TYPE M)	**Derate Linearly at 6 mW/° C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

• In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{ON} values shown in Electrical Characteristics chart). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14 and 15 on the HC/HCT4053.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}-V_{EE} CD54/74HC Types CD54/74HCT Types **See Fig. 4**	2	10	V
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{EE}:* CD54/74HC Types CD54/74HCT Types **See Fig. 5**	0	-6	V
DC Input Control Voltage, V_I	Gnd	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature T_A: CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

Recommended Operating Area as a Function of Supply Voltages.

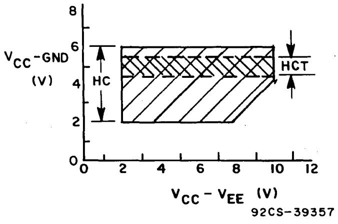


Fig. 4

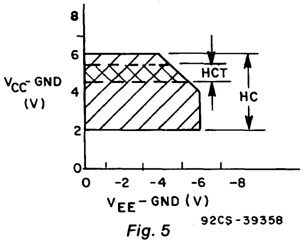


Fig. 5

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/CD54HC4051,4052,4053											CD74HCT/CD54HCT4051,4052,4053											UNITS
	TEST CONDITIONS				74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS				74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_{IS} V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_{IS} V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
					Min	Typ	Max	Min	Max	Min	Max					Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}				2	1.5	—	—	1.5	—	1.5	—	Same as HC	Same as HC		4.5 to 5.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—												
				6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage V_{IL}				2	—	—	0.5	—	0.5	—	0.5				4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35												
				6	—	—	1.8	—	1.8	—	1.8												
"On" Resistance I_O = 1 mA R_{on}	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	—	70	160	—	200	—	240			0	4.5	—	70	160	—	200	—	240	Ω
			0	6	—	60	140	—	175	—	210			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	40	120	—	150	—	180			-4.5	4.5	—	40	120	—	150	—	180	
	V_{CC} to V_{EE}		0	4.5	—	90	180	—	225	—	270			0	4.5	—	90	180	—	225	—	270	Ω
(Fig. 15)			0	6	—	80	160	—	200	—	240			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	45	130	—	162	—	195			-4.5	4.5	—	45	130	—	162	—	195	
Maximum "On" Resistance between any two channels ΔR_{on}			0	4.5	—	10	—	—	—	—	—			0	4.5	—	10	—	—	—	—	—	Ω
			0	6	—	8.5	—	—	—	—	—			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	5	—	—	—	—	—			-4.5	4.5	—	5	—	—	—	—	—	
Switch On/Off Leakage Current I_{IZ}	For Switch OFF: When V_{IS}=V_{CC} V_{OS} = V_{EE}; When V_{IS}=V_{EE}, V_{OS} = V_{CC} For Switch ON: All Applicable Combinations of V_{IS} & V_{OS} Voltage Levels	V_{IL} or V_{IH}																					μA
1&2 Channels (4053)			0	6	—	—	±0.1	—	±1	—	±1			0	6	—	—	±0.1	—	±1	—	±1	
			-5	5	—	—	±0.1	—	±1	—	±1			-5	5	—	—	±0.1	—	±1	—	±1	
4 Channels (4052)			0	6	—	—	±0.1	—	±1	—	±1			0	6	—	—	±0.1	—	±1	—	±1	
			-5	5	—	—	±0.2	—	±2	—	±2			-5	5	—	—	±0.2	—	±2	—	±2	
8 Channels (4051)			0	6	—	—	±0.2	—	±2	—	±2			0	6	—	—	±0.2	—	±2	—	±2	
			-5	5	—	—	±0.4	—	±4	—	±4			-5	5	—	—	±0.4	—	±4	—	±4	
Control Input Leakage Current I_{IL}	—	V_{CC} or Gnd	0	6	—	—	±0.1	—	±1	—	±1	—	**		5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC} I_O = 0	When V_{IS} = V_{EE}, V_{DS} = V_{CC}, When V_{IS} = V_{CC}, V_{OS} = V_{EE}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	Same as HC	Same as HC	0	5.5	—	—	8	—	80	—	160	μA
			-5	5	—	—	16	—	160	—	320			-4.5	5.5	—	—	16	—	160	—	320	
Additional Quiesecent Device Current per input pin: 1 unit load ΔI_{CC}*													V_{CC}-2.1		4.5 to 5.5	—	100	360	—	450	—	490	μA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specifications is 1.8 mA.

** Any voltage between V_{CC} & Gnd.

HCT Input Loading Table

Type	Input	Unit Loads*
4051, 4053	All	0.5
4052	All	0.4

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

SWITCHING CHARACTERISTICS (V_{cc} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical						UNITS
			4051		4052		4053		
			HC	HCT	HC	HCT	HC	HCT	
Propagation Delay Switch IN to OUT	t_{PHL} t_{PLH}	15	4	4	4	4	4	4	ns
Switch Turn-off (S or $\overline{E}$)	t_{PHZ}, t_{PLZ}	15	19	19	21	21	18	18	ns
Switch Turn-on (S or $\overline{E}$)	t_{PZH}, t_{PZL}	15	19	23	27	29	18	20	ns
Power Dissipation Capacitance*	C_{PD}	—	50	52	74	76	38	42	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 fi + \Sigma (C_L + C_S) V_{CC}^2 fo$
fo = output frequency
f_i = input frequency.
C_L= output load capacitance.
C_s = switch capacitance
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		SYMBOL	V_{EE}	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
					HC		HCT		74HC		74HCT		54HC		54HCT		
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Switch In to Out	4051, 4052, 4053	t_{PLH} t_{PHL}	0	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
			0	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
			0	6	—	10	—	—	—	13	—	—	—	15	—	—	
			-4.5	4.5	—	8	—	8	—	10	—	10	—	12	—	12	
Maximum Switch Turn "Off" Delay from S or $\overline{E}$ to Switch Output	4051	t_{PHZ} t_{PLZ}	0	2	—	225	—	—	—	280	—	—	—	340	—	—	
			0	4.5	—	45	—	45	—	56	—	56	—	68	—	68	
			0	6	—	38	—	—	—	48	—	—	—	57	—	—	
			-4.5	4.5	—	32	—	32	—	40	—	40	—	48	—	48	
	4052		0	2	—	250	—	—	—	315	—	—	—	375	—	—	
			0	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
			0	6	—	43	—	—	—	54	—	—	—	65	—	—	
			-4.5	4.5	—	38	—	38	—	48	—	48	—	57	—	57	
	4053		0	2	—	210	—	—	—	265	—	—	—	315	—	—	
			0	4.5	—	42	—	44	—	53	—	55	—	63	—	66	
			0.	6	—	36	—	—	—	45	—	—	—	54	—	—	
			-4.5	4.5	—	29	—	31	—	36	—	39	—	44	—	47	
Maximum Switch Turn "On" Delay from S or E to Switch Output	4051	t_{PZL} t_{PZH}	0	2	—	225	—	—	—	280	—	—	—	340	—	—	
			0	4.5	—	45	—	55	—	56	—	69	—	68	—	83	
			0	6	—	38	—	—	—	48	—	—	—	57	—	—	
			-4.5	4.5	—	32	—	39	—	40	—	49	—	48	—	59	
	4052		0	2	—	325	—	—	—	405	—	—	—	490	—	—	
			0	4.5	—	65	—	70	—	81	—	68	—	98	—	105	
			0	6	—	55	—	—	—	69	—	—	—	83	—	—	
			-4.5	4.5	—	46	—	48	—	58	—	60	—	69	—	72	
	4053		0	2	—	220	—	—	—	275	—	—	—	330	—	—	
			0	4.5	—	44	—	48	—	55	—	60	—	66	—	72	
			0	6	—	37	—	—	—	47	—	—	—	56	—	—	
			-4.5	4.5	—	31	—	34	—	39	—	43	—	47	—	51	
Input (Control) Capacitance		C_I	—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

ANALOG CHANNEL CHARACTERISTICS — TYPICAL VALUES AT T_A = 25°C

CHARACTERISTIC	SYMBOL	CONDITIONS	TYPES	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNITS
Switch Input Capacitance	C_I		All			5	pF
Common Capacitance	C_{COM}		4051			25	
			4052			12	
			4053			8	
Minimum Switch Frequency Response @ -3 dB Figs. 11, 13, 15	f_{MAX}	See Fig. 6 Notes 1, 2	4051	-2.25	2.25	145	MHz
			4052			165	
			4053			200	
			4051	-4.5	4.5	180	
			4052			185	
			4053			>200	
Crosstalk Between Any Two Switches Note 4		See Fig. 7 Notes 2, 3	4051	-2.25	2.25	N/A	dB
			4052			(TBE)	
			4053			(TBE)	
			4051	-4.5	4.5	N/A	
			4052			(TBE)	
			4053			(TBE)	
Sine-Wave Distortion		See Fig. 8	All	-2.25	2.25	0.035	%
			All	-4.5	4.5	0.018	
$\overline{E}$ or S to Switch Feedthrough Noise		See Fig. 9 Notes 2, 3	4051	-2.25	2.25	(TBE)	mV
			4052				
			4053				
			4051	-4.5	4.5	(TBE)	
			4052				
			4053				
Switch "OFF" Signal Feedthrough Figs. 12, 14, 16		See Fig. 10 Notes 2, 3	4051	-2.25	2.25	-73	dB
			4052			-65	
			4053			-64	
			4051	-4.5	4.5	-75	
			4052			-67	
			4053			-66	

Notes:
1. Adjust input voltage to obtain OdBm @ V_{OS} for f_{in} = 1 MHz.
2. V_{IS} is centered at (V_{CC} - V_{EE})/2.
3. Adjust input for OdBm.
4. Not applicable for HC/HCT4051.

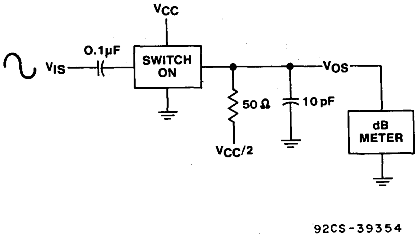


Fig. 6 - Frequency response test circuit.

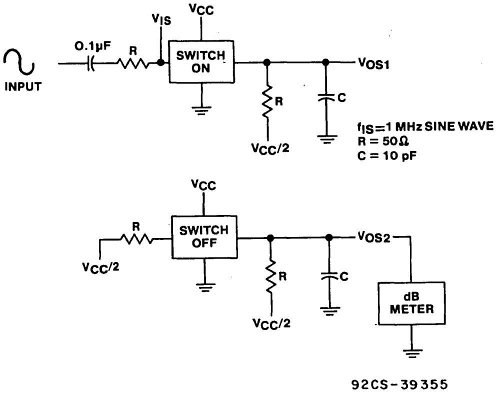


Fig. 7 - Crosstalk between two switches test circuit.

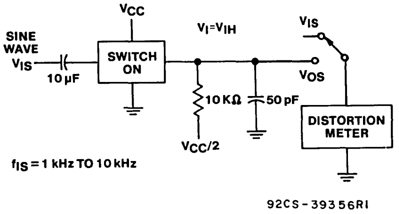


Fig. 8 - Sine wave distortion test circuit.

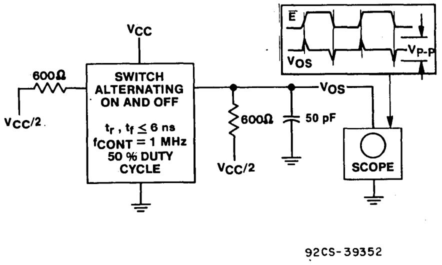


Fig. 9 - Control-to-switch feedthrough noise test circuit.

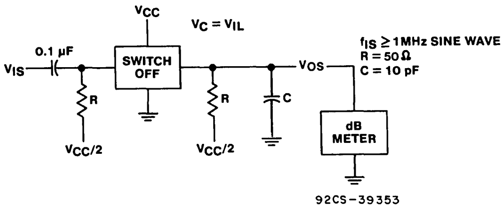


Fig. 10 - Switch off signal feedthrough.

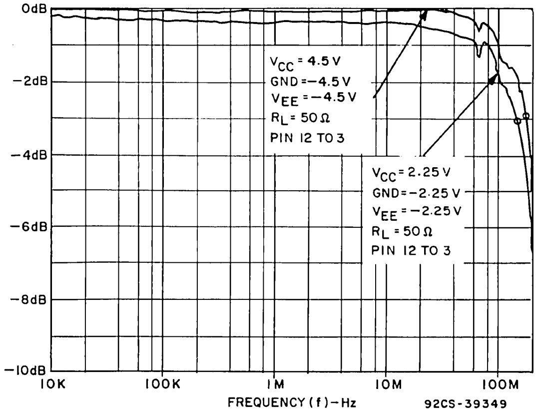


Fig. 11 - Channel on bandwidth (HC/HCT4051).

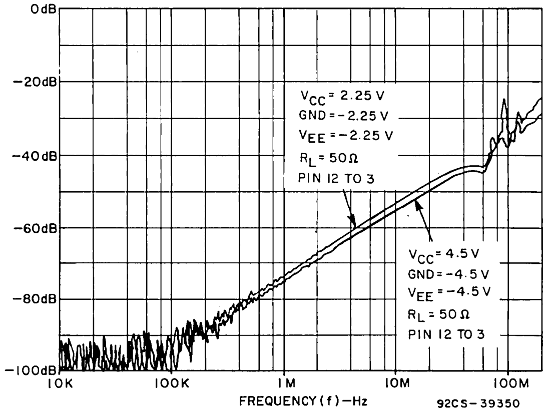


Fig. 12 - Channel off feedthrough (HC/HCT4051).

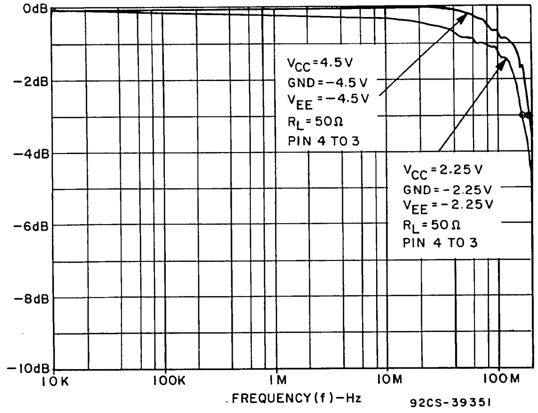


Fig. 13 - Channel on bandwidth (HC/HCT4052).

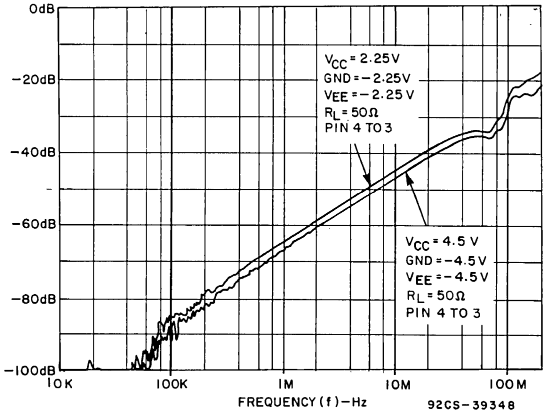


Fig. 14 - Channel off feedthrough (HC/HCT4052).

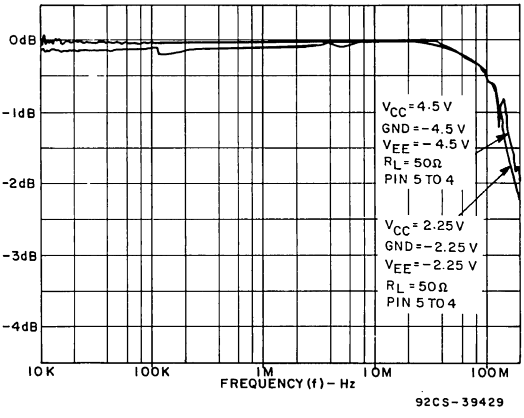


Fig. 15 - Channel on bandwidth (HC/HCT4053).

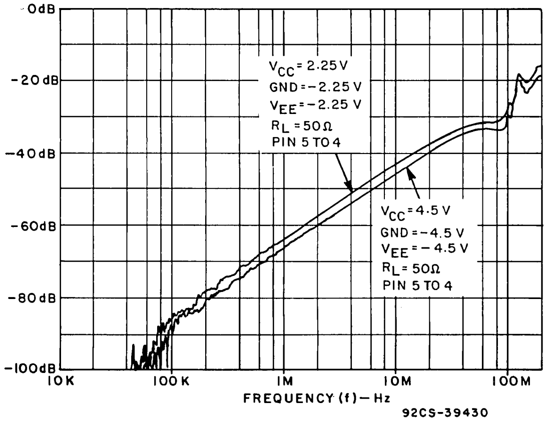


Fig. 16 - Channel off feedthrough (HC/HCT4053).

CD54/74HC4051, CD54/74HCT4051
CD54/74HC4052, CD54/74HCT4052
CD54/74HC4053, CD54/74HCT4053

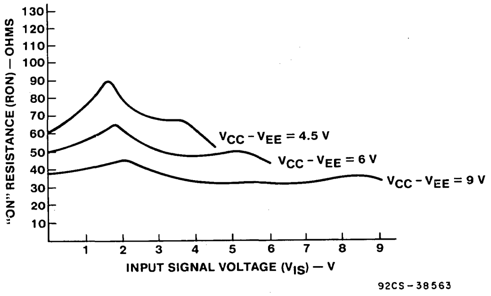
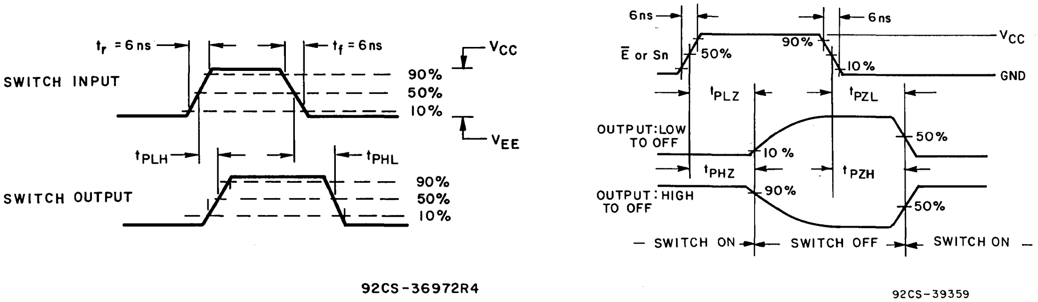
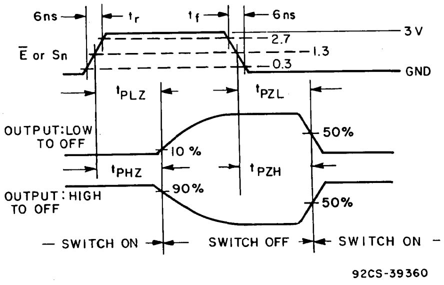


Fig. 17 - Typical ON resistance vs. input signal voltage.

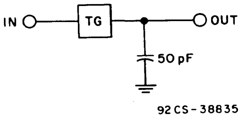


HC4051, 4052, 4053



HCT4051, 4052, 4053

Fig. 18 - Switch propagation delay, turn-on, turn-off times.



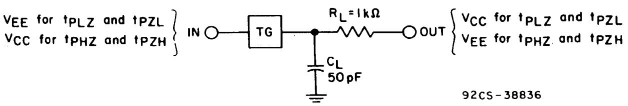


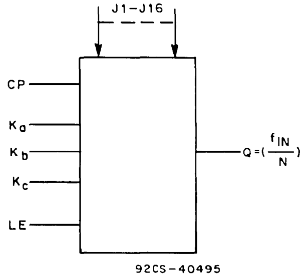
Fig. 19 - Switch on/off propagation delay test circuit.

Fig. 20 - Switch In to Switch Out Propagation delay test circuit.

File Number **1853**

CD54/74HC4059
CD54/74HCT4059

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

CMOS Programmable Divide-by-"N" Counter

Type Features:
- *Synchronous programmable ÷ N counter: N = 3 to 9999 or 15999*
- *Presettable down-counter*
- *Fully static operation*
- *Mode-select control of initial decade counting function (÷ 10, 8, 5, 4, 2)*
- *Master preset initialization*
- *Latchable ÷ N output*

The RCA-CD54/74HC4059 and the CD54/74HCT4059 are high-speed silicon-gate devices that are pin-compatible with the CD4059B devices of the CD4000B series. These devices are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock cycle wide occurring at a rate equal to the input frequency divided by N. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set "high", Kb "high" and Kc "low". Jam inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counter can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

Applications:
- *Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.*
- *Fixed or programmable frequency division*
- *"Time out" timer for consumer-application industrial controls*
- *Companion Application Note, ICAN-6374, "Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"*

from which counting down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table I. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷ 5 mode is selected. Whenever the master preset mode is used, control signals Kb = "low" and Kc = "low" must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig. 1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used, the counter jumps back to the "Jam" count when the output pulse appears.

A "high" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "low". If the Latch Enable is "low", the output pulse will remain high for only 1 cycle of the clock-input signal.

The CD54HC4059 and CD54HCT4059 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4059 and CD74HCT4059 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

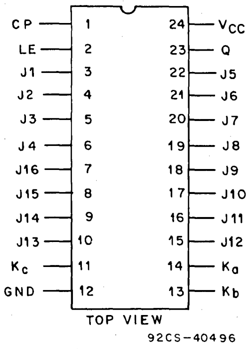
Table I

Mode Select Input			First Counting Section			Last Counting Section			Counter Range	
									Design	Extended
Ka	Kb	Kc	Mode Divides by:	Can be preset to a max. of:	Jam• inputs used:	Mode Divides by:	Can be preset to a max. of:	Jam• inputs used:	Max.	Max.
H	H	H	2	1	J1	8	7	J2,J3,J4	15,999	17,331
L	H	H	4	3	J1,J2	4	3	J3,J4	15,999	18,663
H	L	H	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
L	L	H	8	7	J1,J2,J3	2	1	J4	15,999	21,327
H	H	L	10	9	J1,J2,J3,J4	1	0	—	9,999	16,659
X	L	L	Master Preset			Master Preset			—	—

X = Don't Care

•J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷ 5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷ 5 mode. At power turn-on, Kc must be "low" for a period of 3 input clock pulses after V_{CC} reaches a minimum of 3 volts.



TERMINAL ASSIGNMENT

How to Preset the CD54/74HC/HCT4059 to Desired ÷ N

The value N is determined as follows:

$$N = (\text{MODE}^*)\ (1000 \times \text{Decade 5 Preset} + 100 \times \text{Decade 4 Preset} + 10 \times \text{Decade 3 Preset} + 1 \times \text{Decade 2 Preset}) + \text{Decade 1 Preset} \qquad (1)$$

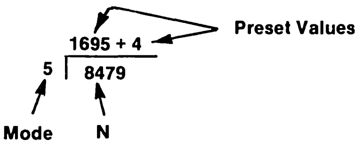
*MODE = First counting section divider (10, 8, 5, 4, or 2)

To calculate preset values for any N count, divide the N count by the Mode. The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\textbf{Preset Value} = \frac{\textbf{N}}{\textbf{Mode}} \qquad (2)$$

Example:

N = 8479, Mode = 5



Mode Select = 5

Ka	Kb	Kc
H	L	H

Program Jam Inputs (BCD)

4			1	5				9				6			
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**	**J11**	**J12**	**J13**	**J14**	**J15**	**J16**
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L

To verify the results, use Equation 1:

N = 5 (1000 x 1 + 100 x 6 + 10 x 9 + 1 x 5) + 4
N = 8479

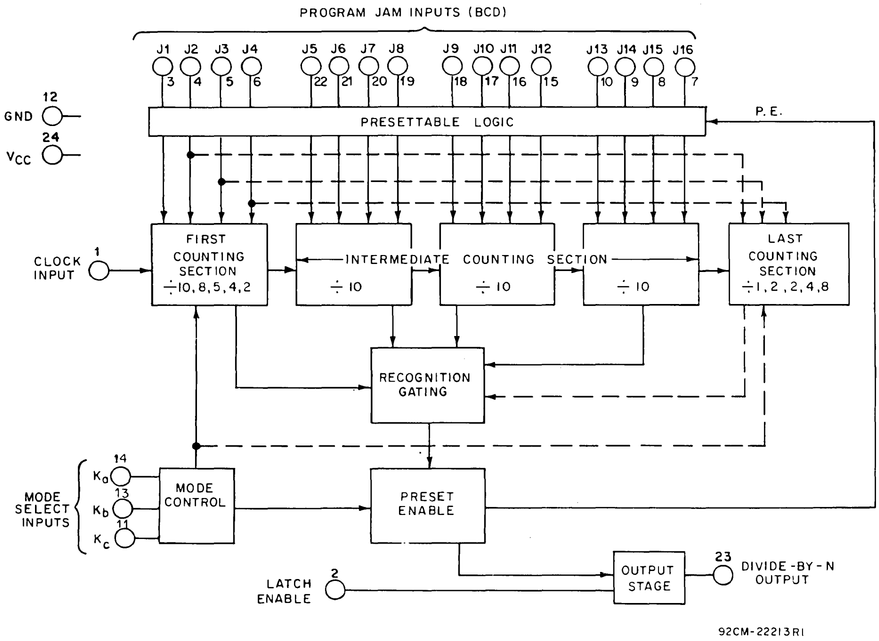


Fig. 1 - Functional block diagram.

CD54/74HC4059
CD54/74HCT4059

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F,H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	-55 to +125°C
PACKAGE TYPE E,M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4059/CD54HC4059										CD74HCT4059/CD54HCT4059									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
All J Inputs	0.5
CP	0.65
LE	1.65
Ka	1
Kb	1.5
Kc	0.85

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4059
CD54/74HCT4059

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay: CP to Q	t_{PLH} t_{PHL}	15	17	19	ns
LE to Q			14	19	
CP Frequency	f_{MAX}	15	54	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	36	36	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

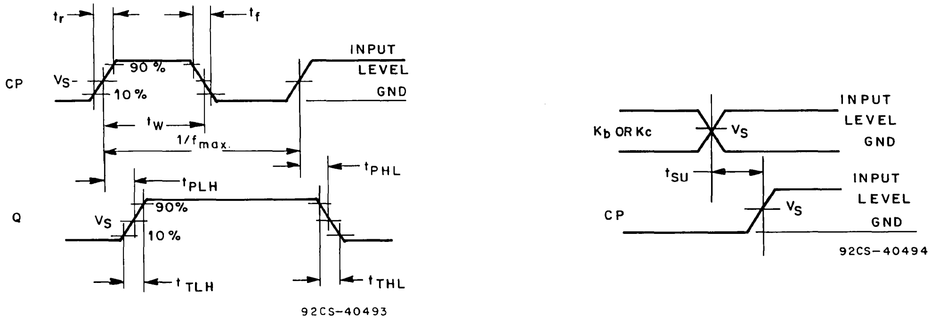
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width CP	t_W	2	90	—	—	—	115	—	—	—	135	—	—	—	ns
		4.5	18	—	20	—	23	—	25	—	27	—	30	—	
		6	15	—	—	—	20	—	—	—	23	—	—	—	
Setup Time Kb, Kc to CP	t_{SU}	2	75	—	—	—	95	—	—	—	110	—	—	—	
		4.5	15	—	15	—	19	—	19	—	22	—	22	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
CP Frequency	f_{MAX}	2	5	—	—	—	4	—	—	—	4	—	—	—	MHz
		4.5	27	—	25	—	22	—	20	—	18	—	17	—	
		6	32	—	—	—	26	—	—	—	21	—	—	—	

CD54/74HC4059
CD54/74HCT4059

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
	t_{PHL}	4.5	—	40	—	46	—	50	—	58	—	60	—	69	
CP to Q		6	—	34	—	—	—	43	—	—	—	51	—	—	
LE to Q		2	—	175	—	—	—	220	—	—	—	265	—	—	
		4.5	—	35	—	46	—	44	—	58	—	53	—	69	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



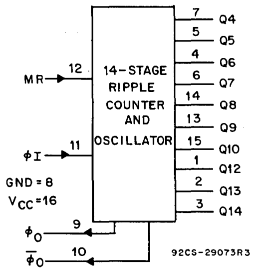
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times, and setup times.

CD54/74HC4060
CD54/74HCT4060

File Number **1654**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

14-Stage Binary Counter with Oscillator

Type Features:

- *Onboard oscillator*
- *Common reset*
- *Negative edge clocking*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC4060 and CD54/74HCT4060 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_I (and ϕ_O). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

In order to achieve a symmetrical waveform in the oscillator section the HCT4060 input pulse switchpoints are the same as in the HC4060; only the MR input in the HCT4060 has TTL switching levels.

The CD54HC4060 and CD54HCT4060 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4060 and CD74HCT4060 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

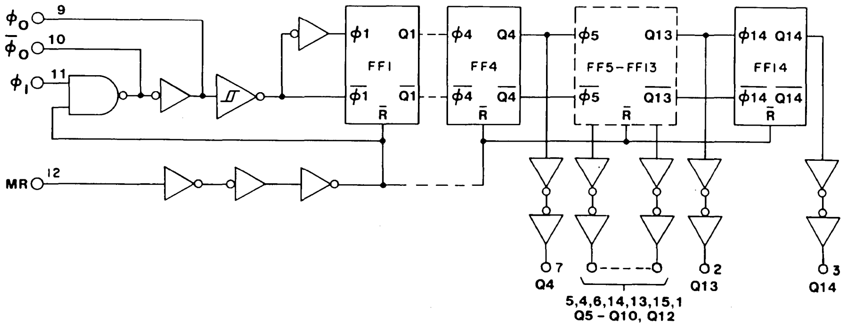


Fig. 1 - Logic block diagram.

CD54/74HC4060
CD54/74HCT4060

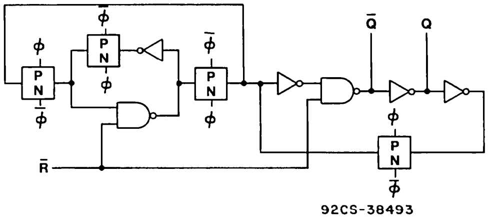


Fig. 2 - Flip-flop detail.

TRUTH TABLE

ϕ_I	MR	OUTPUT STATE
_/¯	L	No Change
¯_	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_o < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4060
CD54/74HCT4060

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4060, CD54HC4060										CD74HCT4060, CD54HCT4060									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} Q Outputs CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL}** or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage V_{OH} Q Outputs TTL Loads	V_{IL} or V_{IH}										V_{IL}** or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} Q Outputs CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL}** or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage V_{OL} Q Outputs TTL Loads	V_{IL} or V_{IH}										V_{IL}** or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										

**For Pin 11 V_{IH}=3.15 V, V_{IL}=0.9 V.

STATIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CD74HC4060, CD54HC4060 TEST CONDITIONS V_I V	I_O mA	V_{CC} V	74HC/54HC TYPES +25°C Min	Typ	Max	74HC TYPE -40/+85°C Min	Max	54HC TYPE -55/+125°C Min	Max	CD74HCT4060, CD54HCT4060 TEST CONDITIONS V_I V	V_{CC} V	74HCT/54HCT TYPES +25°C Min	Typ	Max	74HCT TYPE -40/+85°C Min	Max	54HCT TYPE -55/+125°C Min	Max	UNITS
High-Level Output Voltage V_{OH} $\overline{\phi}_O$ Output (Pin 10) CMOS Loads	V_{CC} or Gnd	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{CC} or Gnd	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
High-Level Output Voltage V_{OH} $\overline{\phi}_O$ Output (Pin 10) TTL Loads ◇	V_{CC} or Gnd	-2.6	4.5	3.98	—	—	3.84	—	3.7	—	V_{CC} or Gnd	4.5	3.98	—	—	3.84	—	3.7	—	V
		-3.3	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} $\overline{\phi}_O$ Output (Pin 10) CMOS Loads	V_{CC} or Gnd	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{CC} or Gnd	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
Low-Level Output Voltage V_{OL} $\overline{\phi}_O$ Output (Pin 10) TTL Loads	V_{CC} or Gnd	2.6	4.5	—	—	0.26	—	0.33	—	0.4	V_{CC} or Gnd	4.5	—	—	0.26	—	0.33	—	0.4	V
		3.3	6	—	—	0.26	—	0.33	—	0.4										
High-Level Output Voltage V_{OH} ϕ_O Output (Pin 9) TTL Loads	V_{IL} or V_{IH}	-3.2	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} ** or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} ϕ_O Output (Pin 9) TTL Loads	V_{IL} or V_{IH}	3.2	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} ** or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

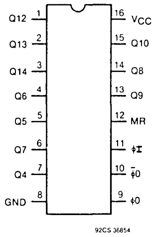
**Pin II V_{IL} = 0.9V, V_{IH} = 3.15V

◇Limits not valid when pin 12 (instead of pin 11) is used as control input.

HCT INPUT LOADING

INPUT	UNIT LOADS*
MR	0.35

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC4060
CD54/74HCT4060

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L pF	Typical		UNITS
			HC	HCT	
Propagation Delay ϕ_I to Q_4	t_{PLH} t_{PHL}	15	25	25	ns
Propagation Delay Qn to Qn+1	t_{PLH} t_{PHL}	15	6	6	ns
Propagation Delay MR to Qn Output	t_{PHL}	15	14	17	ns
Propagation Dissipation Capacitance*	C_{PD}	—	40	40	pF

C_{PD} is used to determine the dynamic power consumption, per package.

$PD = C_{PD} V_{CC}^2 f_I + \Sigma (C_L V_{CC}^2 f_I/M)$ where:

$M = 2^1, 2^2, 2^3..2^{14}$

C_L = output load capacitance

fi = input frequency

Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse		2	6	—	—	—	5	—	—	—	4	—	—	—	
Frequency	t_{MAX}	4.5	30	—	30	—	25	—	25	—	20	—	20	—	MHz
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Input Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Figure 4)		4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time	t_{REM}	2	100	—	—	—	125	—	—	—	150	—	—	—	
(Figure 5)		4.5	20	—	26	—	25	—	33	—	30	—	39	—	ns
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Figure 5)		4.5	16	—	25	—	20	—	31	—	24	—	38	—	ns
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6ns)

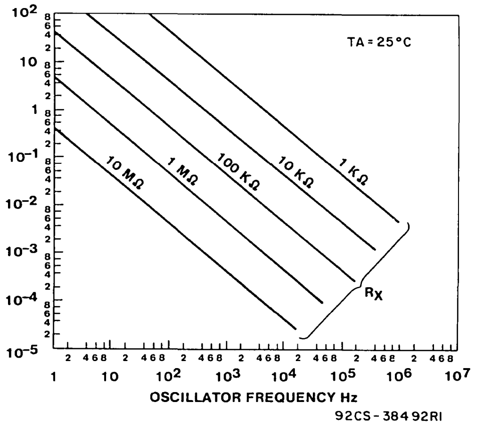
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
ϕ_I to Q_4	t_{PHL}	4.5	—	60	—	66	—	75	—	83	—	90	—	100	ns
(Figure 4)	—	6	—	51	—	—	—	64	—	—	—	78	—	—	
Propagation Delay	t_{PLH}	2	—	80	—	—	—	100	—	—	—	120	—	—	
Q_n to Q_{n+1}	t_{PHL}	4.5	—	16	—	16	—	20	—	20	—	24	—	24	ns
(Figure 4)	—	6	—	14	—	—	—	17	—	—	—	20	—	—	
Propagation Delay	t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	
MR to Q_n		4.5	—	35	—	44	—	44	—	55	—	53	—	66	ns
(Figure 5)		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
(Figure 4)	—	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I*														

*TBD

TYPICAL LIMIT VALUES FOR R_x AND C_x

CHARACTERISTIC	TEST CONDITIONS	VOLTAGE	TYPICAL MAXIMUM LIMITS
R_x Min.	$C_x > 1000$ pF	2	1 KΩ
	$C_x > 10$ pF	4.5	
	$C_x > 10$ pF	6	
R_x Max.	$C_x > 10$ pF	2	20 MΩ
	$C_x > 10$ pF	4.5	
	$C_x > 10$ pF	6	
C_x Min.	$R_x > 10$ KΩ	2	10 pF
	$R_x > 10$ KΩ	4.5	
	$R_x > 10$ KΩ	6	
	$R_x = 1$ KΩ	2	1000 pF
	$R_x = 1$ KΩ	4.5	10 pF
	$R_x = 1$ KΩ	6	10 pF
Maximum Astable Oscillator Frequency	$C_x = 1000$ pF, $R_x = 1$ KΩ	2	0.5 MHz*
	$C_x = 100$ pF, $R_x = 1$ KΩ	4.5	3 MHz*
	$C_x = 100$ pF, $R_x = 1$ KΩ	6	3 MHz*

*At very high frequencies f = 1/2.2 R_xC_x no longer gives an accurate approximation.



OSC FREQUENCY ≈ 1/2.2 R_XC_X

FOR 1 MΩ > R_X > 1 KΩ,

C_X >10 pF, f < 1 MHZ

Fig. 3 - Frequency of on-board oscillator as a function of C_X and R_X.

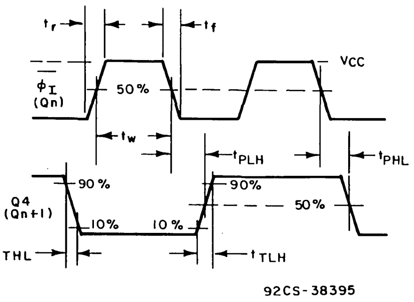
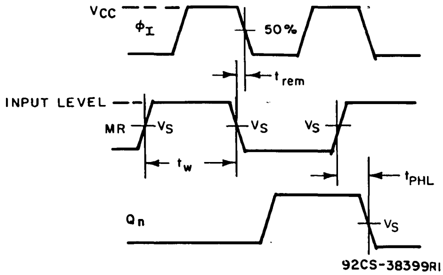


Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times for both HC and HCT types.



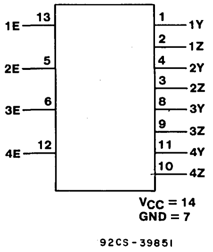
	54/74HC	54/74HCT
MR Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 5 - Master Reset pre-requisite and propagation delays.

CD54/74HC4066
CD54/74HCT4066

File No. **1777**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Bilateral Switch

Type Features:

- *Wide analog-input-voltage range: 0-10 V*
- *Low "ON" resistance: 25 Ω @ V_{CC} = 4.5 V*
  15 Ω @ V_{CC} = 9 V
- *Fast switching and propagation delay times*
- *Low "OFF" leakage current*

The RCA CD54/74 HC/HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear "ON"-resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

The CD54HC4066 and CD54HCT4066 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4066 and CD74HCT4066 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Alternate Source: Philips/Signetics*
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *CD54HC/CD74HC types:*
  2 V to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V & 10 V
- *CD54HCT/CD74HCT types:*
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS input compatiblity
  $I_I \leq 1$ μA @ V_{OL}, V_{OH}

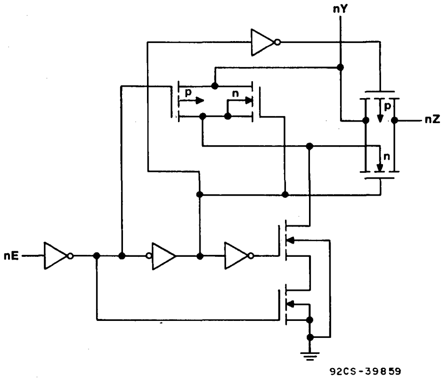


Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

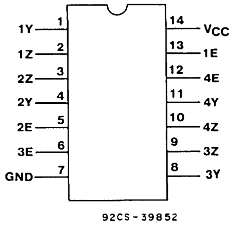
INPUT nE	SWITCH
L	off
H	on

H = HIGH Level
L = LOW Level

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	
HCT Types	-0.5 to +7 V
HC Types	-0.5 to +10.5 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
• DC SWITCH CURRENT, I_O, (FOR $V_I > -0.5$ V OR $V_I < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

- In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{on} values shown in the Electrical Characteristics Chart). No V_{CC} current will flow through R_L if the switch current flows into terminals 2, 3, 9 and 10.



TERMINAL ASSIGNMENT

CD54/74HC4066
CD54/74HCT4066

RECOMMENDED OPERATING CONDITIONS: For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	10	V
CD54/74HCT Types	4.5	5.5	
DC Input Voltage, V_C, and Analog Switch Voltage, $V_{I/O}$	0	V_{CC}	
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f (Control Inputs)			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 9 V	0	250	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4066/CD54HC4066										CD74HCT4066/CD74HCT4066										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS			74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	CONTROL V_I V	SWITCH V_{IS} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		CONTROL V_I V	SWITCH V_{IS} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max				Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}	—	—	2	1.5	—	—	1.5	—	1.5	—	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—											
			9	6.3	—	—	6.3	—	6.3	—											
Low-Level Input Voltage V_{IL}	—	—	2	—	—	0.5	—	0.5	—	0.5	—	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	
			4.5	—	—	1.35	—	1.35	—	1.35											
			9	—	—	2.7	—	2.7	—	2.7											
Input Leakage Current (Any Control) I_{IL}	V_{CC} or Gnd	—	10	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	—	5.5	—	—	±0.1	—	±1	—	±1	µA
Off-Switch Leakage Current I_Z	V_{IL}	V_{CC} or Gnd	10	—	—	±0.1	—	±1	—	±1	V_{IL}	V_{CC} or Gnd	5.5	—	—	±0.1	—	±1	—	±1	
"On" Resistance I_O = 1 mA (Fig. 2) R_{on}	V_{CC}	V_{CC} or Gnd	4.5	—	25	80	—	106	—	128	V_{CC}	V_{CC} or Gnd	4.5	—	25	80	—	106	—	128	Ω
			6	—	20	75	—	94	—	113			—	—	—	—	—	—	—	—	
			9	—	15	60	—	78	—	95			—	—	—	—	—	—	—	—	
	V_{CC}	V_{CC} to Gnd	4.5	—	35	95	—	118	—	142	V_{CC}	V_{CC} to Gnd	4.5	—	35	95	—	118	—	142	
			6	—	24	84	—	105	—	126			—	—	—	—	—	—	—	—	
			9	—	16	70	—	88	—	105			—	—	—	—	—	—	—	—	
"On" Resistance Between Any Two Switches ΔR_{on}	V_{CC}	—	4.5	—	1	—	—	—	—	—	V_{CC}	—	4.5	—	1	—	—	—	—	—	
			6	—	0.75	—	—	—	—	—			—	—	—	—	—	—	—	—	
			9	—	0.5								—	—	—	—	—	—	—	—	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	—	6	—	—	2	—	20	—	40	V_{CC} or Gnd	—	5.5	—	—	2	—	20	—	40	µA
			10	—	—	16	—	160	—	320											
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*	—	—	—	—	—	—	—	—	—	—	V_{CC}-2.1	—	4.5 to 5.5	—	100	360	—	450	—	490	

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	1

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Time: Switch In to Out	t_{PHL} t_{PLH}	15	4	4	ns
Switch Turn Off	t_{PHZ}, t_{PLZ}	15	12	14	
Switch Turn On	t_{PZH}, t_{PZL}	15	8	9	
Power Dissipation Capacitance*	C_{PD}	—	25	38	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where: f_i = input frequency　f_o = output frequency
C_L = load capacitance　C_S = switch capacitance
V_{CC} = supply voltage

SWITCHING CHAARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time	t_{PLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Switch In to Out	t_{PHL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		9	—	8	—	—	—	11	—	—	—	13	—	—	
Switch Turn On Delay	t_{PZH}	2	—	100	—	—	—	125	—	—	—	150	—	—	
	t_{PZL}	4.5	—	20	—	24	—	25	—	30	—	30	—	36	
		9	—	12	—	—	—	15	—	—	—	18	—	—	
Switch Turn Off Delay		2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHZ}, t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		9	—	24	—	—	—	30	—	—	—	36	—	—	
Input (Control) Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4066
CD54/74HCT4066

ANALOG CHANNEL CHARACTERISTICS - Typical Values at T_C = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 12)	Fig. 3 Notes 1 & 2		4.5	200	200	MHz
Cross Talk Between Any Two Switches (Fig. 13)	Fig. 4 Notes 2 & 3		4.5	-72	-72	dB
Total Harmonic Distortion	1 KHz, Fig. 5	V_{IS} = 4 Vpp	4.5	0.022	0.023	%
		V_{IS} = 8 Vpp	9	0.008	N/A	
Control to Switch Feedthrough Noise	Fig. 6		4.5	TBE	TBE	mV
			9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 13)	Fig. 7 Notes 2 & 3		4.5	-72	-72	dB
Switch Input Capacitance C_S	—		—	5	5	pF

Notes: 1. Adjust input level for 0 dBm at output, f = 1 MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS}.

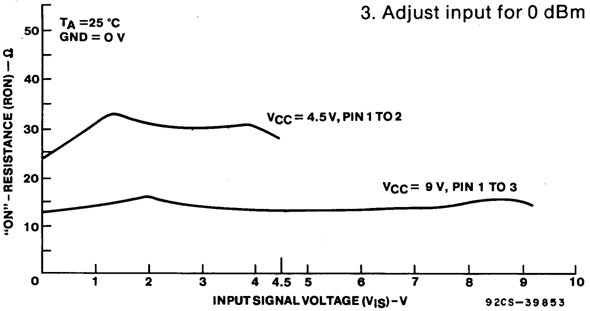


Fig. 2 - Typical "ON" resistance vs. input signal voltage.

ANALOG TEST CIRCUITS

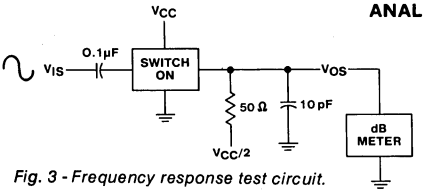


Fig. 3 - Frequency response test circuit.

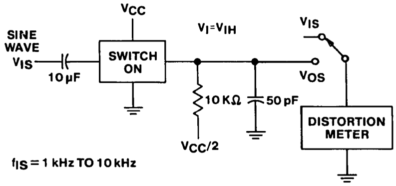


Fig. 5 - Total harmonic distortion test circuit.

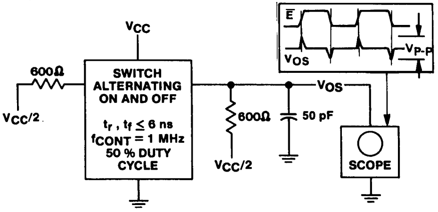


Fig. 6 - Control-to-switch feedthrough noise test circuit.

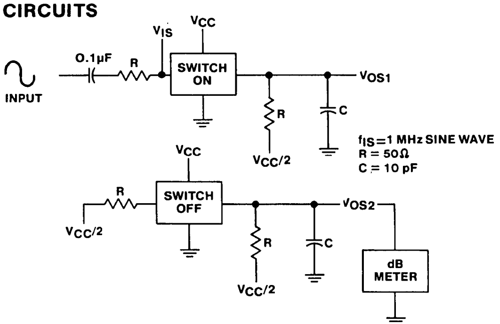


Fig. 4 - Crosstalk between two switches test circuit.

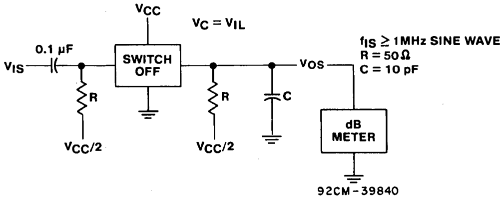


Fig. 7 - Switch off signal feedthrough.

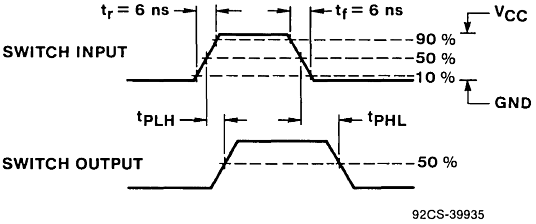


Fig. 8 - Switch propagation - delay times waveforms.

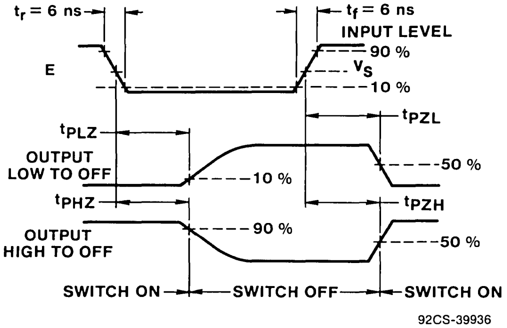


Fig. 9 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

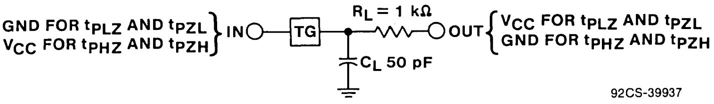


Fig. 10 - Switch on/off propagation delay time test circuit.

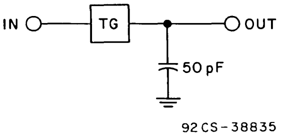


Fig. 11 - Switch-in to switch-out propagation delay time test circuit.

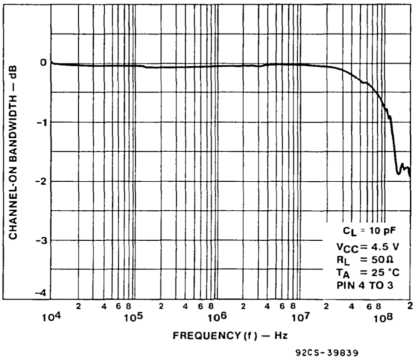


Fig. 12 - Switch frequency response, V_{CC} = 4.5 V.

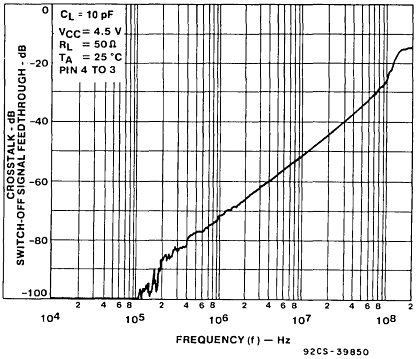


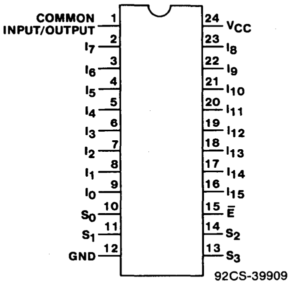
Fig. 13 - Switch-off signal feedthrough and crosstalk vs. frequency, V_{CC} = 4.5 V.

CD54/74HC4067
CD54/74HCT4067

File Number **1783**

Advance Information/ Preliminary Data

High-Speed CMOS Logic



TOP VIEW
TERMINAL ASSIGNMENT

16-Channel Analog Multiplexer/Demultiplexer

Type Features:
- *Wide analog input voltage range:*
- *Low "on" resistance:*
  - *70 Ω typ (V_{CC} = 4.5V)*
  - *60 Ω typ (V_{CC} = 6V)*
- *Fast switching and propagation speeds*
- *"Break-before-make" switching: (6 ns typ @ 4.5V)*
- *Available in both narrow and wide-body plastic packages*

The RCA-CD54/74HC/HCT4067 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.

The CD54HC4067 and CD54HCT4067 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4067 and CD74HCT4067 are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54/74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V*
- *CD54/74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

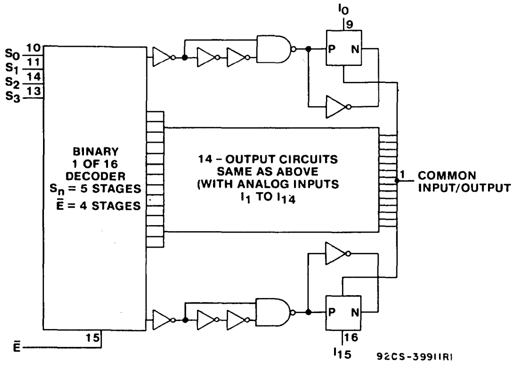


Fig. 1 - Functional diagram.

TRUTH TABLE

S0	S1	S2	S3	$\bar{E}$	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

1 = High Level
0 = Low Level
X = Don't Care.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f (Control Inputs)			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4067
CD54/74HCT4067

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/CD54HC4067										CD74HCT/CD54HCT4067									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	LOGIC V_I V	SWITCH V_{IS} V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		LOGIC V_I V	SWITCH V_{IS} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—										V
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	2	—	—	2	—	2	—	
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5										
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	—	—	0.8	—	0.8	—	0.8	
			6	—	—	1.8	—	1.8	—	1.8										
Maximum "On" Resistance R_{ON} I_O = 1mA	V_{CC} or Gnd	V_{CC} or Gnd	4.5	—	70	160	—	200	—	240	V_{CC} or Gnd	V_{CC} or Gnd	—	70	160	—	200	—	240	Ω
			6	—	60	140	—	175	—	210			—	—	—	—	—	—	—	
	V_{CC} to Gnd	V_{CC} to Gnd	4.5	—	90	180	—	225	—	270	V_{CC} to Gnd	V_{CC} to Gnd	—	90	180	—	225	—	270	
			6	—	80	160	—	200	—	240			—	—	—	—	—	—	—	
Maximum "On" resistance between any two switches ΔR_{ON}	—	—	4.5	—	10	—	—	—	—	—	—	—	—	10	—	—	—	—	—	
	—	—	6	—	8.5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Switch "Off" Leakage Current 16 Channels I_{IZ}	$\overline{E} = V_{CC}$	V_{CC} or Gnd	6	—	—	±0.8	—	±8	—	±8	$\overline{E} = V_{CC}$	V_{CC} or Gnd	—	—	±0.8	—	±8	—	±8	µA
Logic Input Leakage Current I_I	V_{CC} or Gnd	—	6	—	—	±0.1	—	±1	—	±1	**	—	—	—	±0.1	—	±1	—	±1	
Quiescent Device Current I_O = 0mA I_{CC}	V_{CC} or Gnd	—	6	—	—	8	—	80	—	160	V_{CC} or Gnd	—	—	—	8	—	80	—	160	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*	—	—	—	—	—	—	—	—	—	—	V_{CC} -2.1	—	—	100	360	—	450	—	490	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Any Voltage Between V_{CC} & Gnd.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
S_0 - S_3	0.5
$\overline{E}$	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Time: Switch In to Switch Out	t_{PLH}, t_{PHL}	15	6	6	ns
Switch Turn Off					
Ē to Out	t_{PLZ}, t_{PHZ}	15	23	23	
Sn to Out	t_{PLZ}, t_{PHZ}		21	21	
Switch Turn On					
Ē to Out	t_{PZL}, t_{PZH}	15	23	25	
Sn to Out	t_{PZL}, t_{PZH}		25	25	
Power Dissipation Capacitance*	C_{PD}	—	93	96	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where: f_i = input frequency f_o = output frequency

C_L = load capacitance C_S = switch capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC} V	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time	t_{PLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
Switch In to Out	t_{PHL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Switch Turn-On		2	—	275	—	—	—	345	—	—	—	415	—	—	
Ē to Out		4.5	—	55	—	60	—	69	—	75	—	83	—	90	
	t_{PZL}	6	—	47	—	—	—	59	—	—	—	71	—	—	
	t_{PZH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
Sn to Out		4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	76	—	—	
Switch Turn-Off		2	—	275	—	—	—	345	—	—	—	415	—	—	
Ē to Out		4.5	—	55	—	55	—	69	—	69	—	83	—	83	
	t_{PLZ}	6	—	47	—	—	—	59	—	—	—	71	—	—	
Sn to Out	t_{PHZ}	2	—	290	—	—	—	365	—	—	—	435	—	—	
		4.5	—	58	—	58	—	73	—	73	—	87	—	87	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Input (Control) Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

ANALOG CHANNEL CHARACTERISTICS — Typical Values at T_A = 25°C

CHARACTERISTICS		TEST CONDITION	V_{CC} V	HC/HCT	UNITS
Switch Frequency Response at - 3 dB (Fig. 12)		Fig. 3 Notes 1 & 2	4.5	89	MHz
Sine Wave Distortion		Fig. 4	4.5	0.051	%
Feedthrough Noise:					
Ē to Switch		Fig. 5 Notes 2 & 3	4.5	TBE	mV
S to Switch				TBE	
Switch "OFF" Signal Feedthrough (Fig. 13)		Fig. 6	4.5	-75	dB
Switch Input Capacitance	C_S	—	—	5	pF
Common Capacitance	C_{COM}	—	—	50	

NOTES: 1. Adjust input level for 0 dBm at output, f = 1 kHz.

2. V_{IS} is centered at $V_{cc}/2$.

3. Adjust input for 0 dBm. at V_{IS}

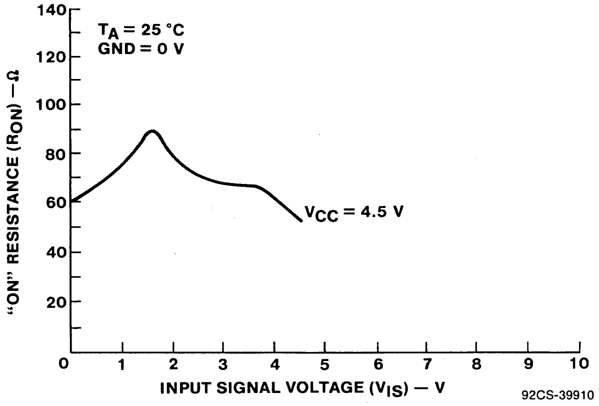


Fig. 2 - Typical "ON" resistance versus input signal voltage.

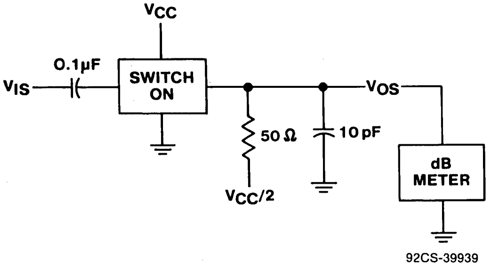


Fig. 3 - Frequency response test circuit.

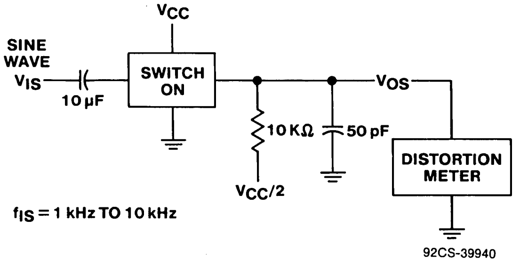


Fig. 4 - Sine wave distortion test circuit.

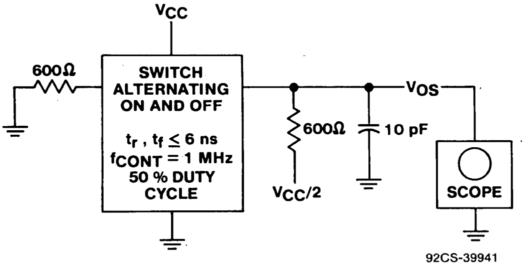


Fig. 5 - Control-to-switch feedthrough noise test circuit.

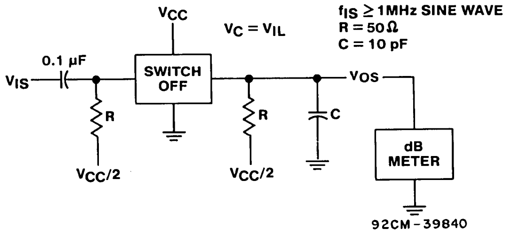


Fig. 6 - Switch off signal feedthrough test circuit.

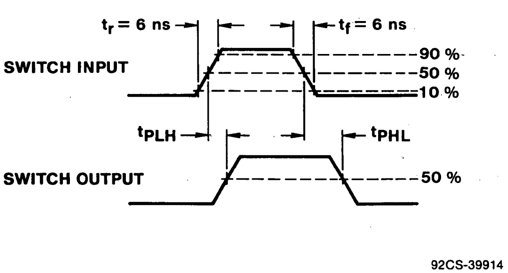


Fig. 7 - Switch propagation-delay times wave forms.

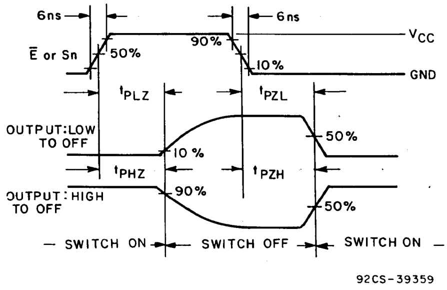


Fig. 8 - Switch turn-on and turn-off propagation delay times wareforms, for HC types.

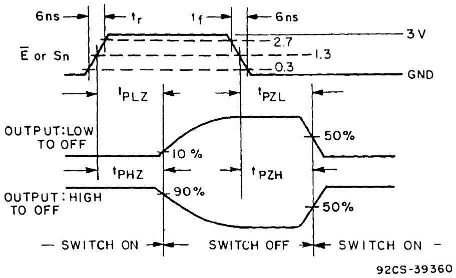


Fig. 9 - Switch turn-on and turn-off propagation delay times waveforms for HCT Types.

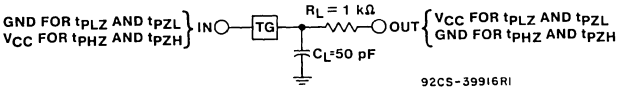


Fig. 10 - Switch on/off propagation delay time test circuit.

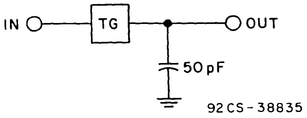


Fig. 11 - Switch In to Switch Out Propagation delay time test circuit.

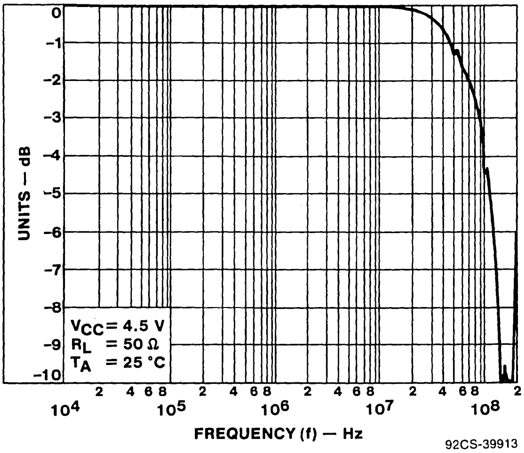


Fig. 12 - Typical switch frequency response.

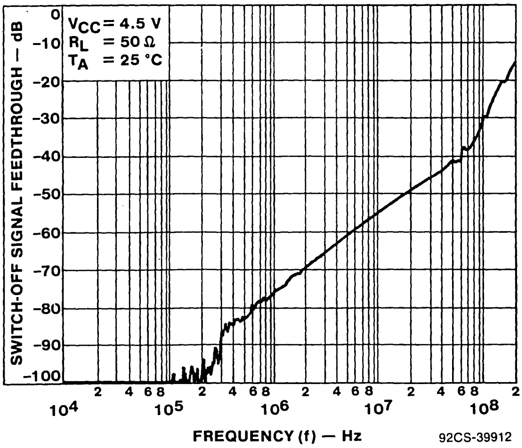
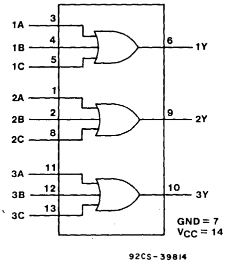


Fig. 13 - Typical switch-off signal feed through vs. frequency.

CD54/74HC4075
CD54/74HCT4075

File Number **1778**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Triple 3-Input OR Gate

Type Features:

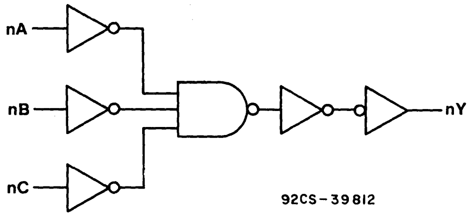
- *Buffered inputs*
- *Typical CD54/74HC4075 Propagation Delay = 8ns @ V_{CC} = 5V, C_L = 15pF, T_A = 25°C*

The RCA-CD54/74HC4075 and CD54/74HCT4075 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC4075 and CD54HCT4075 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4075 and CD74HCT4075 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  - *Standard Outputs - 10 LSTTL loads*
  - *Bus driver outputs - 15 LSTTL loads*
- *Wide Operating temperature range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL input logic compatibility*
    - *V_{IL} = 0.8 V max., V_{IH} = 2 V Min.*
  - *CMOS input compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



LOGIC DIAGRAM

TRUTH TABLE

nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

L = Low voltage Level
H = High voltage Level
X = Don't Care

CD54/74HC4075
CD54/74HCT4075

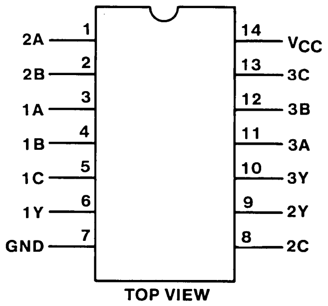
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < $V_O < V_{CC}$ + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-39813

TERMINAL ASSIGNMENT

CD54/74HC4075
CD54/74HCT4075

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4075/CD54HC4075										CD74HCT4075/CD54HCT4075									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
All	1.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @25° C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

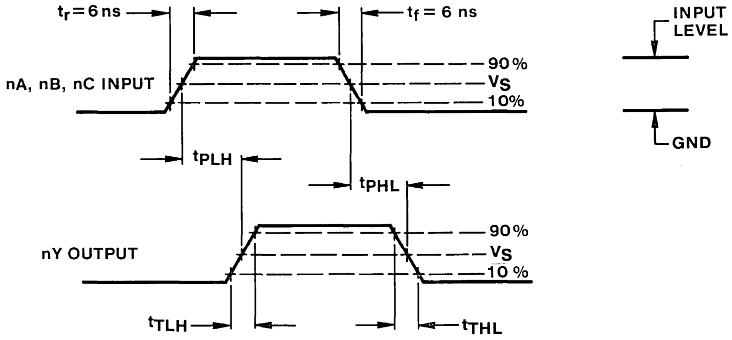
CHARACTERISTIC		CL (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1)	t_{PLH}, t_{PHL}	15	8	9	ns
Power Dissipation Capacitance*	C_{PD}	—	26	28	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = V_{CC}^2 fi (C_{PD} + C_L)$ where: fi = input frequency
C_L = load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	
Input to Output	t_{PHL}	4.5	—	20	—	24	—	25	—	30	—	30	—	36	ns
(Fig. 1)		6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
(Fig. 1)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



92CS-39811

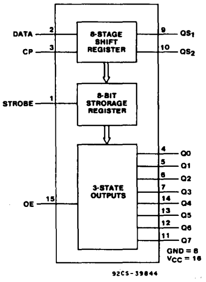
	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 1 - Transition times and propagation delay times.

CD54/74HC4094
CD54/74HCT4094

File Number **1779**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Stage Shift-and-Store Bus Register — 3-State

Type Features:

- *Buffered inputs*
- *Separate serial outputs synchronous to both positive and negative clock edges for cascading.*

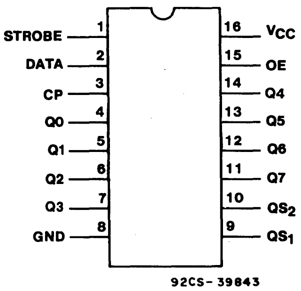
The RCA-CD54/74HC4094 and CD54/74HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Two serial outputs are available for cascading a number of these devices. Data is available at the QS1 serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the QS2 terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise time is slow.

The CD54HC4094 and CD54HCT4094 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4094 and CD74HCT4094 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

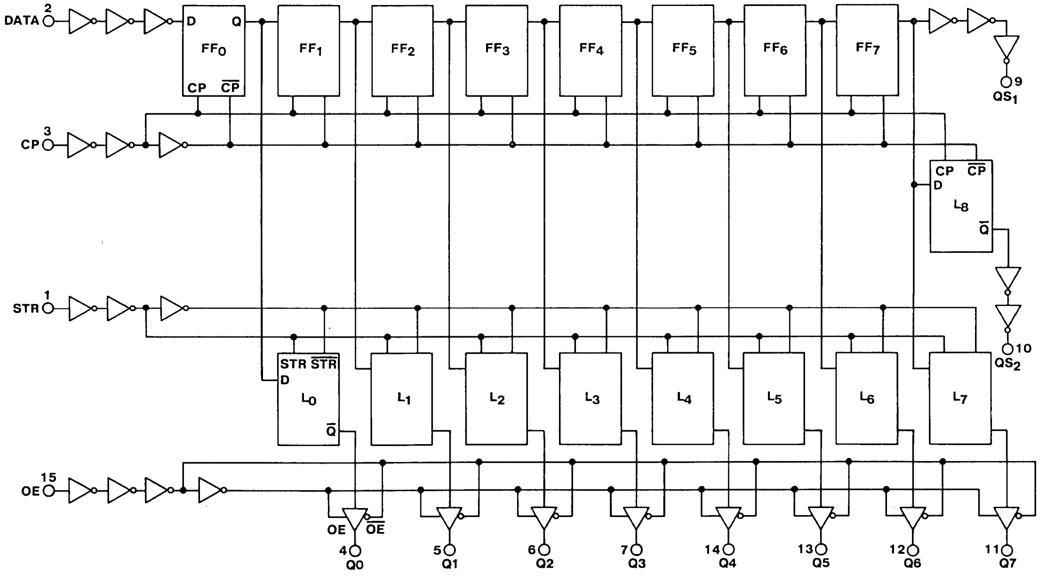


Fig. 1 - Logic diagram.

CD54/74HC4094
CD54/74HCT4094

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	Q0	Qn	QS1*	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	Q7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	Qn-1	Q'6	NC
↑	H	H	H	H	Qn-1	Q'6	NC
↓	H	H	H	NC	NC	NC	Q7

H = HIGH voltage level
L = LOW voltage level
X = don't care
NC = No Change
Z = HIGH impedance OFF-state
↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'6 = the information in the seventh register stage
*At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and QS1 output.

CD54/74HC4094
CD54/74HCT4094

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4094/CD54HC4094										CD74HCT4094/CD54HCT4094									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

* For dual-supply systems theoretical worst case ($V_I = 2.4$ V, $V_{CC} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D	0.40
CP, OE	1.50
STR	1.0

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4094
CD54/74HCT4094

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay CP to Qn	t_{PLH} t_{PHL}	15	16	18	ns
CP to QS1			12	16	
CP to QS2			11	15	
Output Enabling Time	t_{PZH} t_{PZL}		14	14	
Output Disabling Time	t_{PHZ} t_{PLZ}		10	14	
Max. CP Frequency	f_{MAX}		60	60	MHz
Power Dissipation Capacitance*	C_{PD}	—	90	110	pF

*C_{PD} is used to determine the dynamic power consumption, per register.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i=input frequency C_L=output load capacitance
f_o=output frequency V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	30	—	39	—	38	—	49	—	45	—	59	ns
CP to QS1		6	—	26	—	—	—	33	—	—	—	38	—	—	
		2	—	135	—	—	—	170	—	—	—	205	—	—	
		4.5	—	27	—	36	—	34	—	45	—	41	—	54	ns
CP to QS2		6	—	23	—	—	—	29	—	—	—	35	—	—	
		2	—	195	—	—	—	245	—	—	—	295	—	—	
		4.5	—	39	—	43	—	49	—	54	—	59	—	65	ns
CP to Qn		6	—	33	—	—	—	42	—	—	—	50	—	—	
		2	—	180	—	—	—	225	—	—	—	270	—	—	
		4.5	—	36	—	39	—	45	—	49	—	54	—	59	ns
STR to Qn		6	—	31	—	—	—	38	—	—	—	46	—	—	
Output Enable	t_{PZH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
to Qn	t_{PZL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Disable	t_{PHZ}	2	—	125	—	—	—	155	—	—	—	190	—	—	
to Qn	t_{PLZ}	4.5	—	25	—	35	—	31	—	44	—	38	—	53	ns
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Output Transition	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	15	—	15	—	15	—	15	—	15	—	15	pF

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
STR Pulse Width	t_{WH}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Data Setup Time	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Data Hold Time	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	4	—	3	—	4	—	3	—	4	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
STR Setup Time	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
STR Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Max. CP Frequency	$f_{CL(max.)}$	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	24	—	24	—	20	—	20	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	

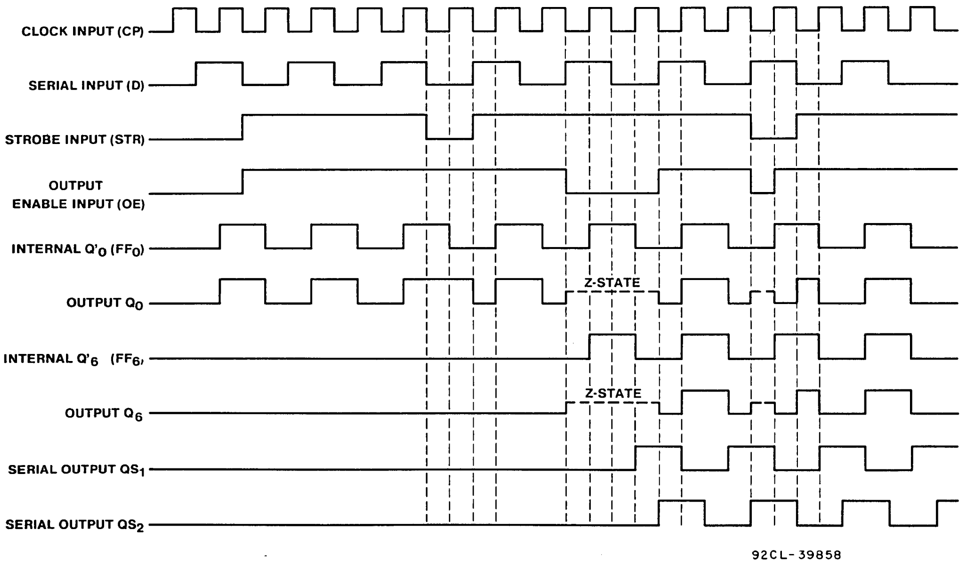


Fig. 2 — Timing Diagram

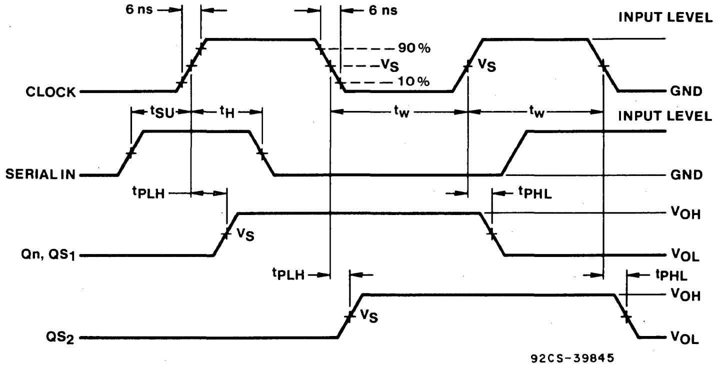


Fig. 3 - Data propagation delays, setup and hold times.

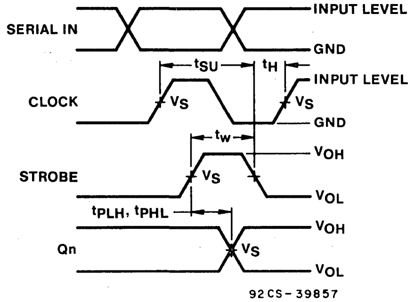


Fig. 4 - Strobe propagation delays, and setup and hold times.

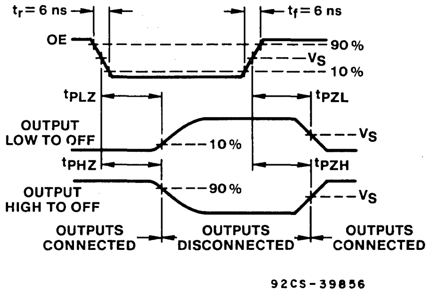


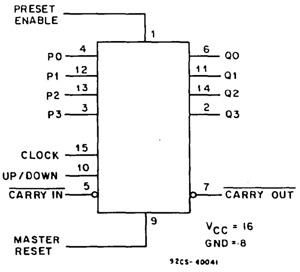
Fig. 5 - Enable and Disable Times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1823**

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Up/Down Counters

CD54/74HC/HCT4510 BCD Decade Counter, Asynchronous Reset

CD54/74HC/HCT4516 4-Bit Binary Counter, Asynchronous Reset

Type Features:

- *Synchronous counting and asynchronous loading*
- *Look-ahead carry for high-speed counting*

The RCA CD54/74HC/HCT4510 presettable BCD up/down counter and the CD54/74HC/HCT4516 presettable binary up/down counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the Master Reset line, and can be preset to any binary number present on the preset inputs by a high level on the Preset Enable line. The 4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

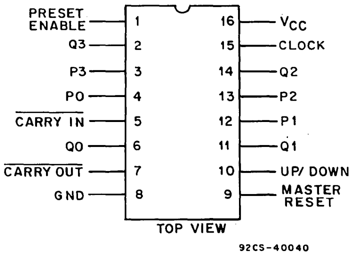
If the Carry-In input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the Carry-Out of a less significant stage to the Carry-In of a more significant stage.

The 4510 and 4516 can be cascaded in the ripple mode by connecting the Carry-Out to the clock of the next stage. If the Up/Down input changes during a terminal count, the Carry-Out must be gated with the clock, and the Up/Down input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 5.)

The CD54HC/HCT4510 and the CD54HC/HCT4516 are supplied in 16-lead ceramic dual-in-line frit-seal packages (F suffix). The CD74HC/HCT4510 and the CD74HC/HCT-4516 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  - *Standard outputs - 10 LSTTL loads*
  - *Bus driver outputs - 15 LSTTL loads*
- *Wide operating temperature range:*
  - *CD74HC/HCT: −40 to +85° C*
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  - *2 to 6 V operation*
  - *High noise immunity:*
    - $N_{IL}=30\%$, $N_{IH}=30\%$ *of* V_{CC}; *@* $V_{CC}=5$ *V*
- *CD54HCT/CD74HCT types:*
  - *4.5 to 5.5 V operation*
  - *Direct LSTTL input logic compatibility*
    - $V_{IL}=0.8$ *V max.,* $V_{IH}=2$ *V min.*
  - *CMOS input compatibility*
    - $I_I \leq 1$ *μA @* V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

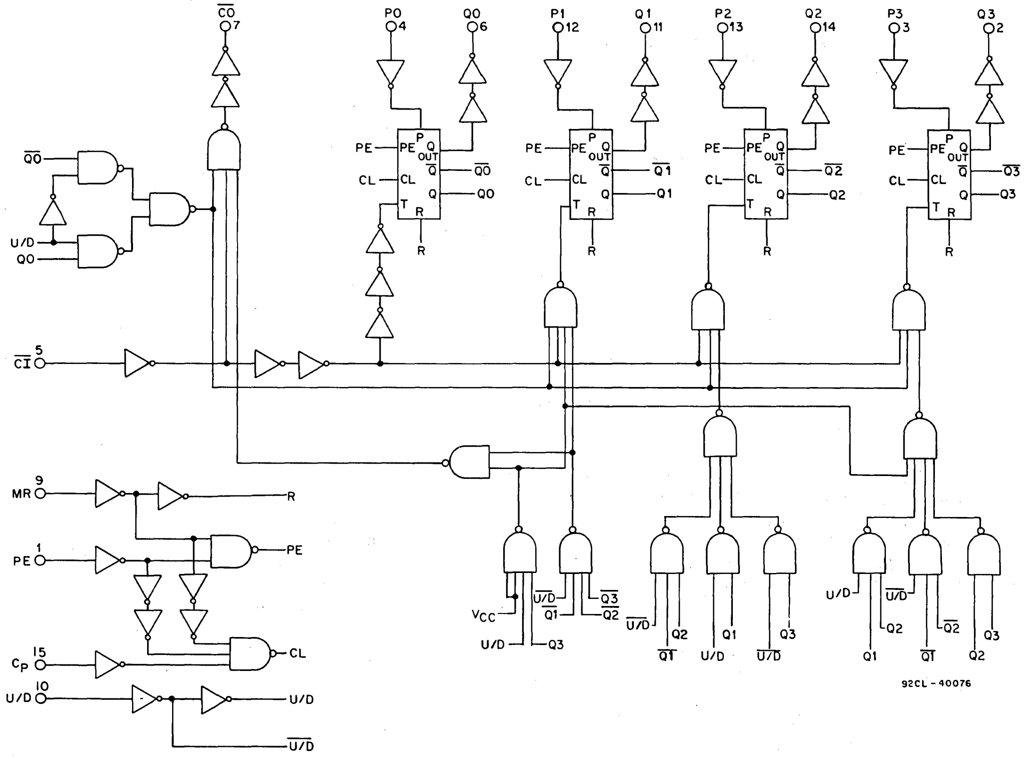


Fig. 1 - Logic diagram for HC/HCT4510.

TRUTH TABLE

CL	$\overline{CI}$	U/D	PE	MR	ACTION
X	H	X	L	L	NO COUNT
↑	L	H	L	L	COUNT UP
↑	L	L	L	L	COUNT DOWN
X	X	X	H	L	PRESET
X	X	X	X	H	RESET

X = Don't Care H = High Voltage Level
L = Low Voltage Level

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

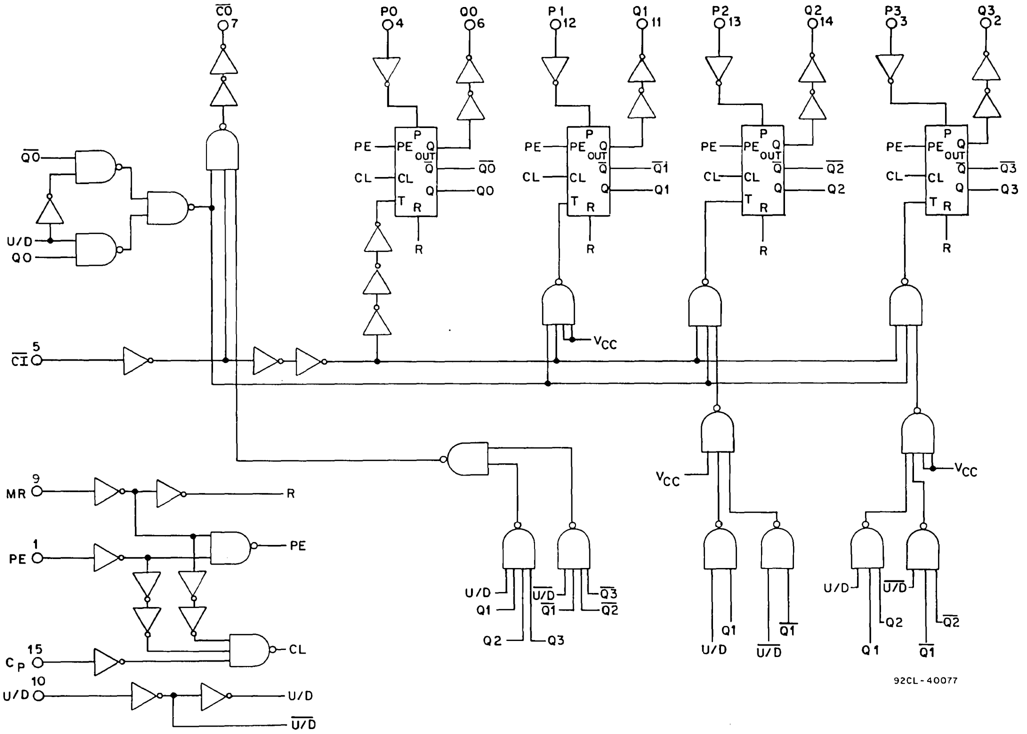


Fig. 2 - Logic diagram for HC/HCT4516.

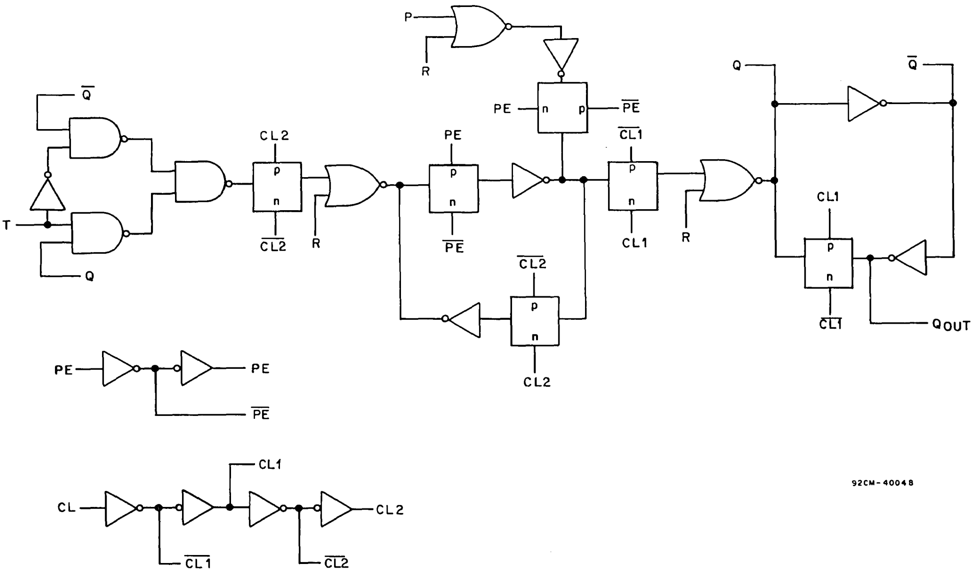


Fig. 3 - Logic diagram of flip-flops for HC/HCT4510/4516.

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC}$ +0.5 V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < $V_o < V_{CC}$ +0.5 V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F,H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F,H .... -55 to +125°C
PACKAGE TYPE E,M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4510/4516/CD54HC4510/4516										CD74HCT4510/4516/CD54HCT4510/4516									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
P0-P3	0.75
MR	1.5
U/D, PE, $\overline{\text{CI}}$	1
CP	1.25

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES				UNITS
			4510		4516		
			HC	HCT	HC	HCT	
Propagation Delay:							ns
CP to Qn	t_{PLH}, t_{PHL}	15	18	21	18	21	
CP to $\overline{CO}$	t_{PLH}, t_{PHL}	15	22	24	22	24	
PE to Qn	t_{PLH}, t_{PHL}	15	21	22	21	22	
PE to $\overline{CO}$	t_{PLH}, t_{PHL}	15	25	28	25	28	
MR to Qn	t_{PHL}	15	18	18	18	18	
MR to $\overline{CO}$	t_{PLH}	15	20	20	20	20	
$\overline{CI}$ to $\overline{CO}$	t_{PLH}, t_{PHL}	15	10	13	10	13	
Power Dissipation Capacitance	C_{PD}*		59	65	68	72	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

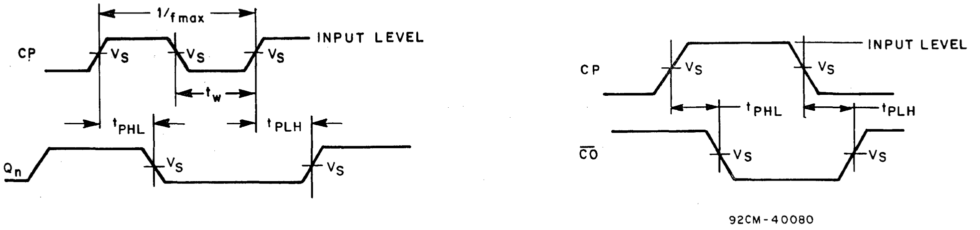
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pulse Width:	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
CP t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	100	—	—	—	125	—	—	—	150	—	—	—	
MR t_W	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
	6	17	—	—	—	21	—	—	—	26	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
PE t_W	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time, t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	
Pn to PE,	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
$\overline{CI}$ to CP	6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time, t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
Pn to PE	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
	2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{CI}$ to CP t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	
	2	0	—	—	—	0	—	—	—	0	—	—	—	
U/D to CP t_H	4.5	0	—	0	—	0	—	0	—	0	—	0	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Removal Time:	2	80	—	—	—	100	—	—	—	120	—	—	—	
MR to CP t_{REM}	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Maximum Frequency	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
CP f_{MAX}	4.5	30	—	30	—	24	—	24	—	20	—	20	—	
	6	35	—	—	—	28	—	—	—	24	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

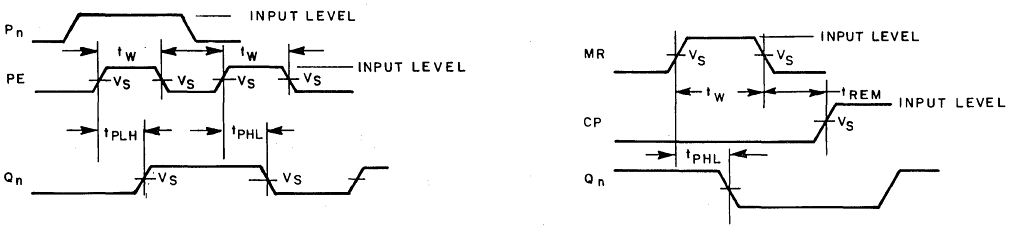
CHARACTERISTIC		V_{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay:	t_{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
CP to Qn	t_{PHL}	4.5	—	44	—	50	—	55	—	63	—	66	—	75	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
	t_{PLH}	2	—	260	—	—	—	325	—	—	—	390	—	—	
CP to $\overline{CO}$	t_{PHL}	4.5	—	52	—	58	—	65	—	73	—	78	—	87	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	
PE to Qn	t_{PHL}	4.5	—	50	—	53	—	63	—	66	—	75	—	80	
		6		43	—	—	—	54	—	—	—	64	—	—	
	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
PE to $\overline{CO}$	t_{PHL}	4.5	—	60	—	68	—	75	—	85	—	90	—	102	
		6	—	51	—	—	—	64	—	—	—	76	—	—	
		2	—	210	—	—	—	265	—	—	—	315	—	—	
MR to Qn	t_{PHL}	4.5	—	42	—	42	—	53	—	53	—	63	—	63	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
		2	—	235	—	—	—	295	—	—	—	355	—	—	
MR to $\overline{CO}$	t_{PLH}	4.5	—	47	—	47	—	59	—	59	—	71	—	71	
		6	—	40	—	—	—	50	—	—	—	60	—	—	
	t_{PLH}	2	—	125	—	—	—	155	—	—	—	190	—	—	
$\overline{CI}$ to $\overline{CO}$	t_{PHL}	4.5	—	25	—	31	—	31	—	39	—	38	—	47	
		6	—	21	—	—	—	26	—	—	—	32	—	—	
Transition Time:	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Qn, $\overline{CO}$	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516



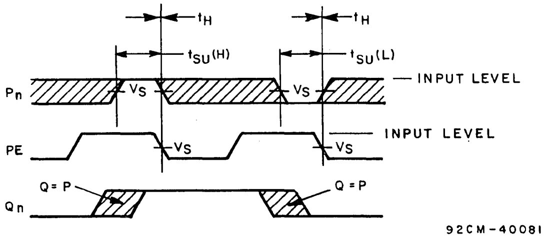
(a) *Clock to output delays and clock pulse width.*

(b) *Clock to carry out delays.*



(c) *Preset Enable pulse width and Preset Enable to output delays.*

(d) *Master reset pulse width, master reset to output delay and master reset to clock removal time.*



(e) *Setup and hold times data to Preset Enable (PE).*

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 4 - AC waveforms.

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516

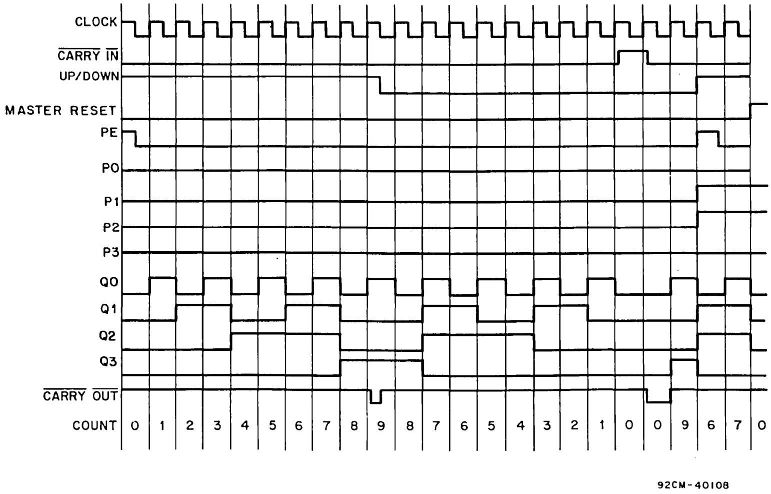


Fig. 5 - Timing diagram for CD54/74HC/HCT4510.

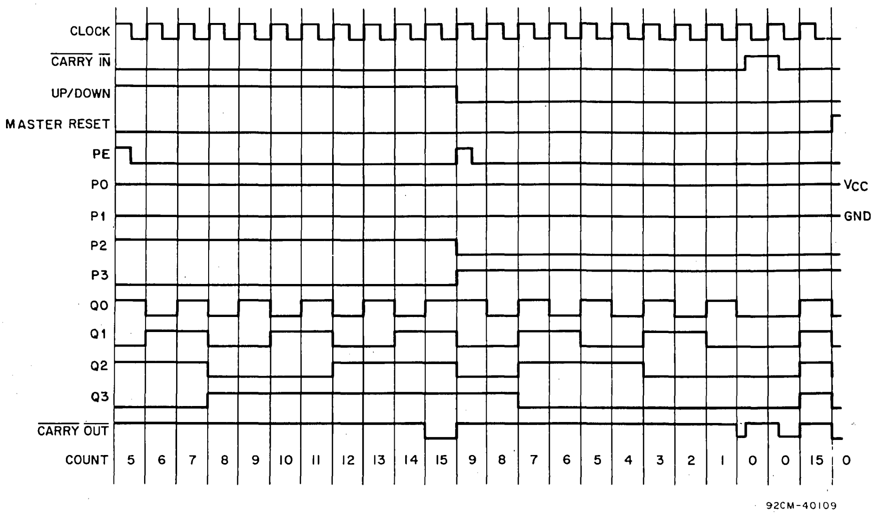
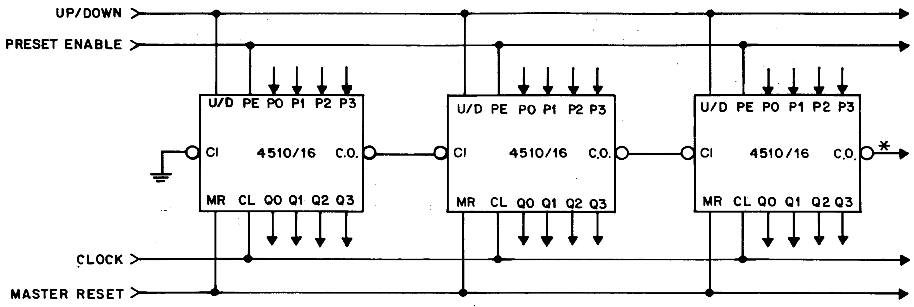


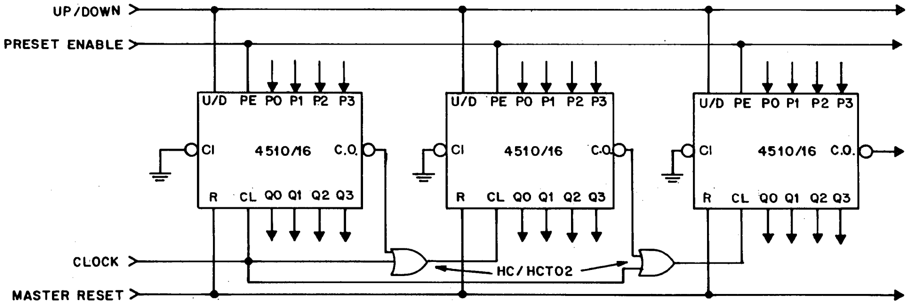
Fig. 6 - Timing diagram for CD54/74HC/HCT4516.

CD54/74HC4510, CD54/74HCT4510
CD54/74HC4516, CD54/74HCT4516



* CARRY OUT LINES AT THE 2ND, 3RD, ETC., STAGES MAY HAVE A NEGATIVE-GOING GLITCH PULSE RESULTING FROM DIFFERENTIAL DELAYS OF DIFFERENT 4510/16 IC'S. THESE NEGATIVE-GOING GLITCHES DO NOT AFFECT PROPER 4510/16 OPERATION. HOWEVER, IF THE CARRY OUT SIGNALS ARE USED TO TRIGGER OTHER EDGE-SENSITIVE LOGIC DEVICES, SUCH AS FF'S OR COUNTERS, THE CARRY OUT SIGNALS SHOULD BE GATED WITH THE CLOCK SIGNAL USING A 2-INPUT OR GATE SUCH AS HC/HCT02.

(*a*) *Parallel clocking.*



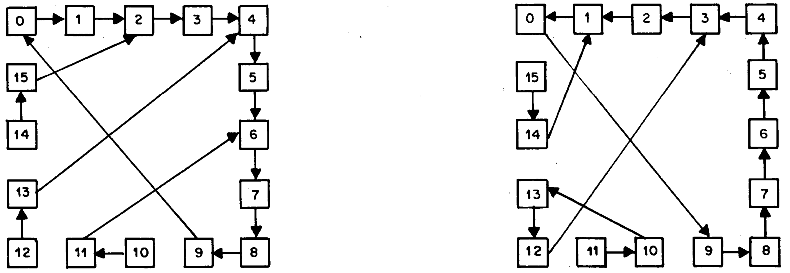
RIPPLE CLOCKING MODE:
THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE "HIGH".

FOR CASCADING COUNTERS OPERATING IN A FIXED UP-COUNT OR DOWN-COUNT MODE, THE OR GATES ARE NOT REQUIRED BETWEEN STAGES, AND $\overline{CO}$ IS CONNECTED DIRECTLY TO THE CL INPUT OF THE NEXT STAGE WITH $\overline{CI}$ GROUNDED.

92CL-40093

(*b*) *Ripple clocking.*

Fig. 7 - Cascading counter packages.



COUNT UP

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE COUNT.

COUNT DOWN

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE OR TWO COUNTS.

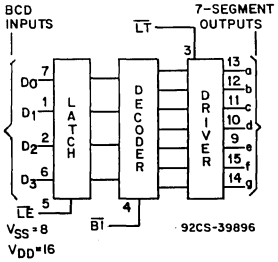
92CM-40491

Fig. 8 - HC/HCT4510 State Diagrams.

File Number **1786**

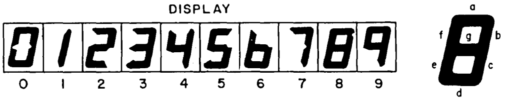
CD54/74HC4511
CD54/74HCT4511

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

BCD-to-7 Segment Latch/Decoder/Drivers



Type Features:

- *High-output sourcing capability-7.5 mA @ 4.5 V, 10 mA @ 6 V (HC4511)*
- *Input latches for BCD code storage*
- *Lamp test and blanking capability*

The RCA CD54/74HC4511 and CD54/74HCT4511 are BCD-to-7 segment latch/decoder/drivers having four address inputs (D_0-D_3), active "Low" blanking and lamp test inputs, and a latch enable input which, when "High", enables the latches to store the BCD inputs. When Latch Enable is "Low", the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

The CD54HC/HCT4511 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4511 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X				*				*

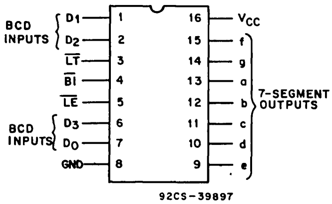
X = Don't Care.

*Depends on BCD code previously appied when $\overline{LE}$ = L.

Note: Display is blank for all illegal input codes (BCD > HLLH).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  N_{IL}=30%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4511
CD54/74HCT4511

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	−0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = −55 to +100°C (PACKAGE TYPE F,H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = −40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	−55 to +125°C
PACKAGE TYPE E,M	−40 to +85°C
STORAGE TEMPERATURE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

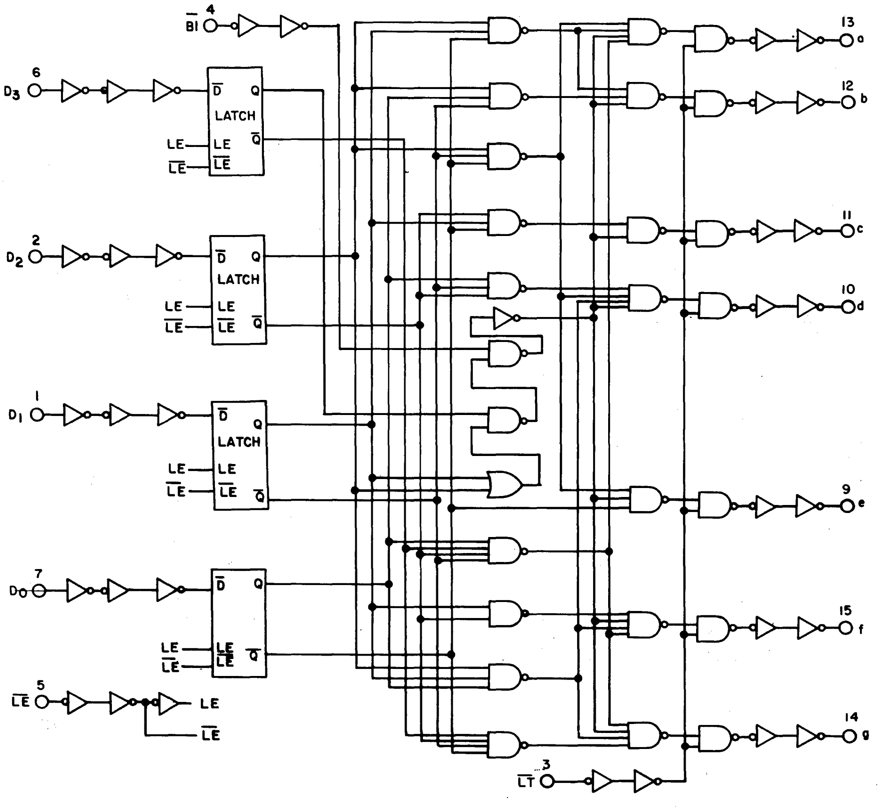


Fig. 1 - Logic diagram.

CD54/74HC4511
CD54/74HCT4511

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4511/CD54HC4511										CD74HCT4511/CD54HCT4511									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V_I V	V_{CC} V	+25° C			-40/ +85° C		-55/ +125° C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Non-Standard Output	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.5	4.5	3.98	—	—	3.84	—	3.7	—										
		-10	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Standard Output	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{LT}$, $\overline{LE}$	1.5
$\overline{BI}$, Dn	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25° C.

CD54/74HC4511
CD54/74HCT4511

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay: D_n to Output	t_{PLH} t_{PHL}	15	25	25	ns
$\overline{LE}$ to Output	t_{PLH} t_{PHL}	15	23	23	
$\overline{BI}$ to Output	t_{PLH} t_{PHL}	15	18	18	
$\overline{LT}$ to Output	t_{PLH} t_{PHL}	15	13	13	
Power Dissipation Capacitance*	C_{PD}	—	114	110	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 fi + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

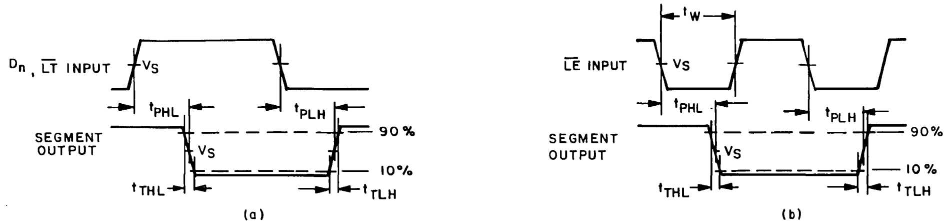
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Setup Time, D_n to $\overline{LE}$	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time, D_n to $\overline{LE}$	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
		4.5	3	—	5	—	3	—	5	—	3	—	5	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
Latch Enable Pulse Width,	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	MHz
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

CD54/74HC4511
CD54/74HCT4511

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
D_n to Output	t_{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	ns
		6	—	51	—	—	—	64	—	—	—	77	—	—	
	t_{PLH}	2	—	270	—	—	—	340	—	—	—	405	—	—	
$\overline{LE}$ to Output	t_{PHL}	4.5	—	54	—	54	—	68	—	68	—	81	—	81	ns
		6	—	46	—	—	—	58	—	—	—	69	—	—	
	t_{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	
$\overline{BI}$ to Output	t_{PHL}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	ns
		6		37	—	—	—	47	—	—	—	56	—	—	
	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	
$\overline{LT}$ to Output	t_{PHL}	4.5	—	32	—	33	—	40	—	41	—	48	—	50	ns
		6	—	27	—	—	—	34	—	—	—	41	—	—	
	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

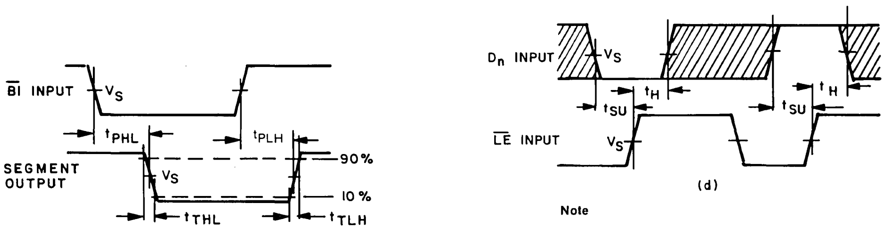


(a)

Input (Dn, $\overline{LT}$) to output propagation delays and output transition times

(b)

Input ($\overline{LE}$) to output propagation delays and latch enable pulse width



(c)

Input ($\overline{BI}$) to output propagation delays.

(d)

Note

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveforms showing the data set-up and hold times for Dn input to $\overline{LE}$ input.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

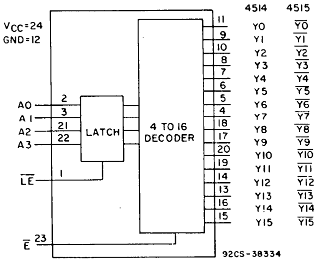
92CM-39899

Fig. 2 - AC waveforms.

CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515

File Number **1597**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-to-16 Line Decoder/Demultiplexer with Input Latches

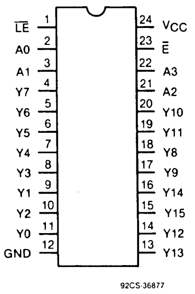
Type Features:
- *Multifunction capability:*
  Binary to 1-of-16 decoder
  1-to-16 line demultiplexer

The RCA CD54/74HC4514, 4515 and CD54/74HCT4514, 4515 are high-speed silicon gate devices consisting of a 4-bit strobed latch and a 4-to-16 line decoder. The selected output is enabled by a low on the enable input ($\overline{E}$). A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using the $\overline{E}$ input as the data input and the select inputs (A0-A3) as addresses. This $\overline{E}$ input also serves as a chip select when these devices are cascaded.

When Latch Enable ($\overline{LE}$) is high the output follows changes in the inputs (see truth table). When $\overline{LE}$ is low the output is isolated from changes in the input and remains at the level (high for the 4514, low for the 4515) it had before the latches were enabled. These devices, enhanced versions of the equivalent CMOS types, can drive 10 LSTTL loads.

The CD54HC4514, 4515 and CD54HCT4514, 4515 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC4514, 4515 and CD74HCT4514, are supplied in 24-lead dual-in-line, narrow-body plastic packages (EN suffix), in 24-lead dual-in-line, wide-body plastic packages (E suffix), and in 24-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features
- *Fanout (over temperature range):*
  Standard outputs — 10 LSTTL loads
  Bus driver outputs — 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$; @ $V_{CC} = 5V$
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 \text{ V} < V_O < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

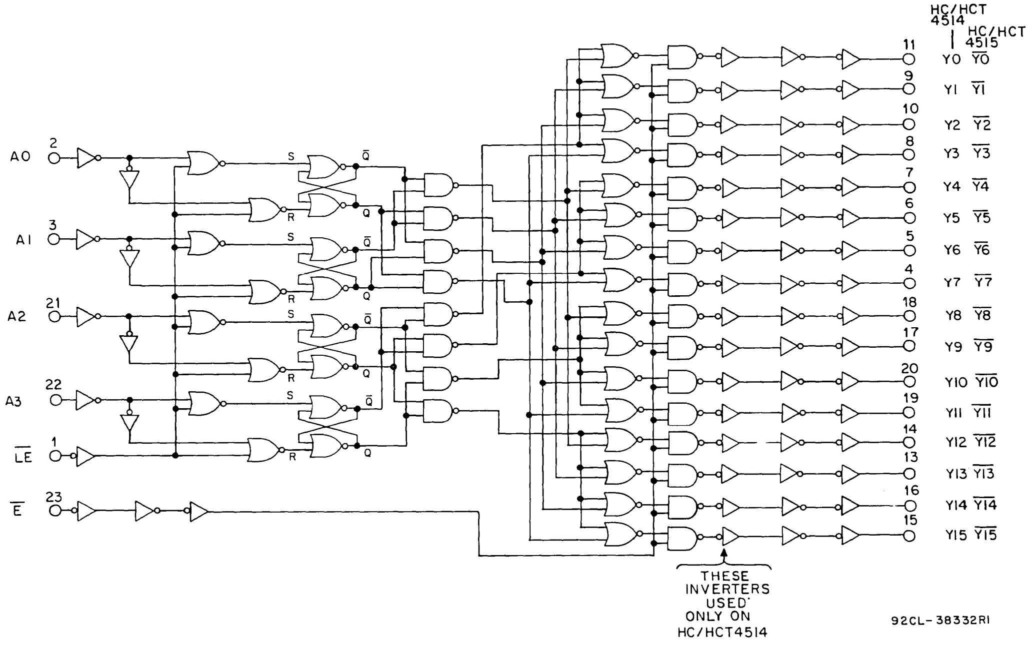


Fig. — Logic diagram for CD54/74HC4514, 4515 and CD54/74HCT4514, 4515.

CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515

DECODE TRUTH TABLE ($\overline{LE}$ = 1)

ENABLE	DECODER INPUTS				ADDRESSED OUTPUT 4514 = Logic 1 (High) 4515 = Logic 0 (Low)
	A3	A2	A1	A0	
0	0	0	0	0	Y0
0	0	0	0	1	Y1
0	0	0	1	0	Y2
0	0	0	1	1	Y3
0	0	1	0	0	Y4
0	0	1	0	1	Y5
0	0	1	1	0	Y6
0	0	1	1	1	Y7
0	1	0	0	0	Y8
0	1	0	0	1	Y9
0	1	0	1	0	Y10
0	1	0	1	1	Y11
0	1	1	0	0	Y12
0	1	1	0	1	Y13
0	1	1	1	0	Y14
0	1	1	1	1	Y15
1	X	X	X	X	All Outputs = 0, 4514 All Outputs = 1, 4515

X = Don't Care Logic 1 = High Logic 0 = Low

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2V	0	1000	ns
at 4.5 V	0	500	ns
at 6V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4514/CD54HC4515										CD74HCT4514/CD54HCT4515									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0 — A3	0.15
$\overline{LE}$	0.85
$\overline{E}$	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4514, CD54/74HCT4514
CD54/74HC4515, CD54/74HCT4515

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	Typical Values		UNITS
			HC	HCT	
Propagation Delay Select to Output	t_{PHL} t_{PLH}	15	23	25	ns
$\overline{LE}$ to Output	t_{PHL} t_{PLH}	15	19	21	ns
$\overline{E}$ to Output	t_{PHL} t_{PLH}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	70	75	pF

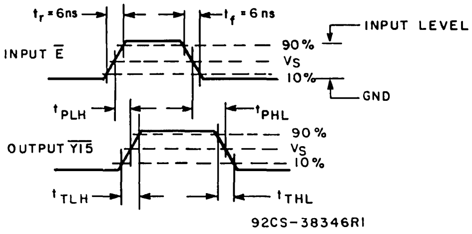
*C_{PD} is used to determine the dynamic power consumption, per package.
PD $=V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency,
C_L = output load capacitance
V_{CC} = supply voltage

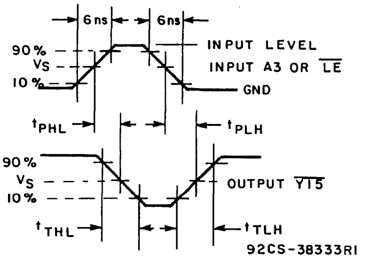
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{LE}$ Pulse Width	t_w	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
		4.5	15	—	30	—	19	—	38	—	22	—	45	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
Select to $\overline{LE}$ Set-up time	t_{su}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Select to $\overline{LE}$ Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	5	—	0	—	5	—	0	—	5	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Select to Outputs	t_{PLH} t_{PHL}	2	—	275	—	—	—	345	—	—	—	115	—	—	ns
		4.5	—	55	—	55	—	69	—	69	—	83	—	83	
		6	—	47	—	—	—	59	—	—	—	71	—	—	
$\overline{LE}$ to Outputs	t_{PLH} t_{PHL}	2	—	225	—	—	—	280	—	—	—	340	—	—	ns
		4.5	—	45	—	50	—	56	—	63	—	68	—	75	
		6	—	38	—	—	—	48	—	—	—	58	—	—	
$\overline{E}$ to Outputs	t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
		4.5	—	35	—	40	—	44	—	50	—	53	—	60	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF





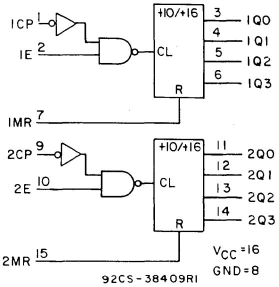
	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, Vs	50% V_{CC}	1.3 V

Propagation delay times and transition times for HC/HCT4515.

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

File Number **1665**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Synchronous Counters

CD54/74HC/HCT4518 — BCD
CD54/74HC/HCT4520 — Binary

Type Features:

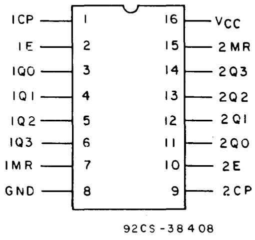
- *Positive or Negative Edge Triggering*
- *Synchronous Internal Carry Propagation*

The RCA CD54/74HC4518 and CD54/74HCT4518 are dual BCD up-counters. The RCA CD54/74HC4520 and CD54/74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting Q3 to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

The CD54HC/HCT4518 and CD54HC/HCT4520 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4518 and CD74HC/HCT4520 are supplied in a 16-lead plastic dual-in-line packages (E suffix), and in 16-lead surface mount plastic dual-in-line packages (M suffix). The CD54/74HC/HCT4518/4520 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; @ $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V *Max.*, $V_{IH} = 2$ V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

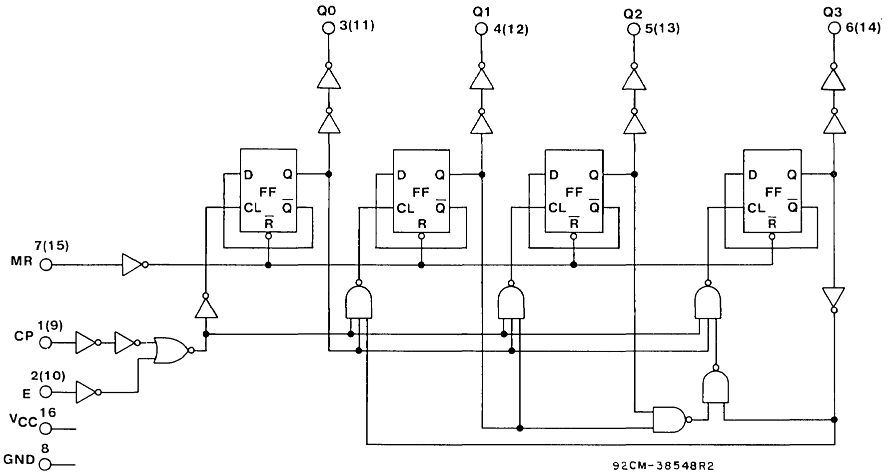


Fig. 1 — CD54/74HC/HCT4518 Logic Diagram

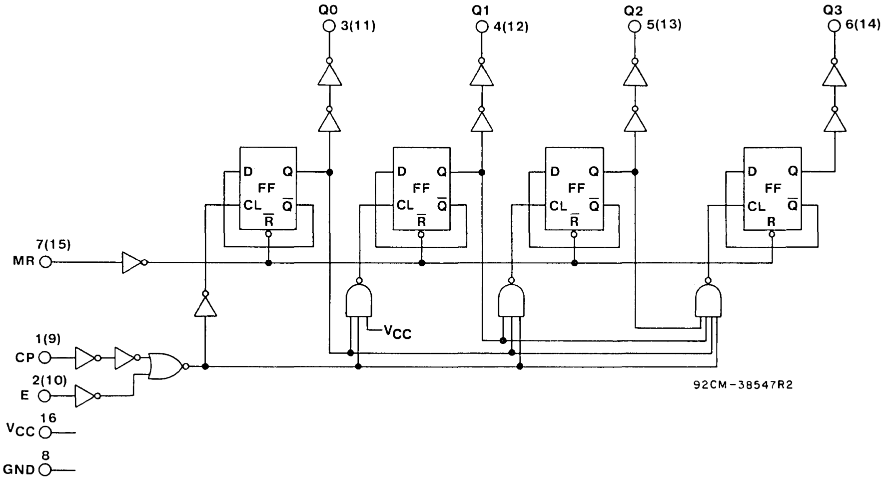


Fig. 2 — CD54/74HC/HCT4520 Logic Diagram

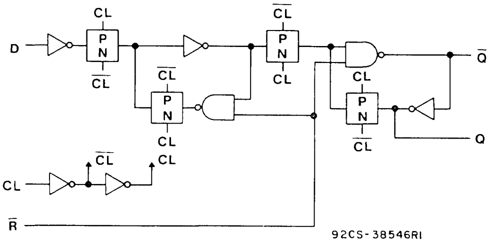


Fig. 3 - Detail of each D Flip-Flop

TRUTH TABLE			
CP	E	MR	ACTION
_/‾	H	L	Increment Counter
L	‾_	L	Increment Counter
‾_	X	L	No Change
X	_/‾	L	No Change
_/‾	L	L	No Change
H	‾_	L	No Change
X	X	H	Q0 thru Q3 = L

X = Don't Care H = High State L = Low State

_/‾ = low-to-high transition

‾_ = high-to-low transition

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < $V_o < V_{CC}$ + 0.5V)	±25mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4518/CD54HC4518 CD74HC4520/CD54HC4520										CD74HCT4518/CD54HCT4518 CD74HCT4520/CD54HCT4520									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

***For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.**

HCT Input Loading Table

Input	Unit Loads*
MR	1.2
CP	0.25
ENABLE	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Maximum Clock Frequency	15	f_{MAX}	60	50	MHz
Propagation Delay CP to Qn	15	t_{PLH} t_{PHL}	20	22	ns
Enable to Qn	15	t_{PLH} t_{PHL}	20	23	ns
MR to Qn	15	t_{PLH} t_{PHL}	12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	33	33	pF

*C_{PD} is used to determine the dynamic power consumption, per counter.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where
f_i = input frequency,
f_o = output frequency,
C_L = output load capacitance
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	24	—	20	—	20	—	17	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width	t_W	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time Enable to CP	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Removal Time MR to CP	t_{REM}	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Setup Time CP to Enable	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Removal Time MR to Enable	t_{REM}	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP to Qn	t_{PLH} t_{PHL}	2	—	240	—	—	—	300	—	—	—	360	—	—	ns
		4.5	—	48	—	53	—	60	—	66	—	72	—	80	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
Enable to Qn	t_{PLH} t_{PHL}	2	—	240	—	—	—	300	—	—	—	360	—	—	ns
		4.5	—	48	—	55	—	60	—	69	—	72	—	83	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
MR to Qn	t_{PHL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t_{THL} t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

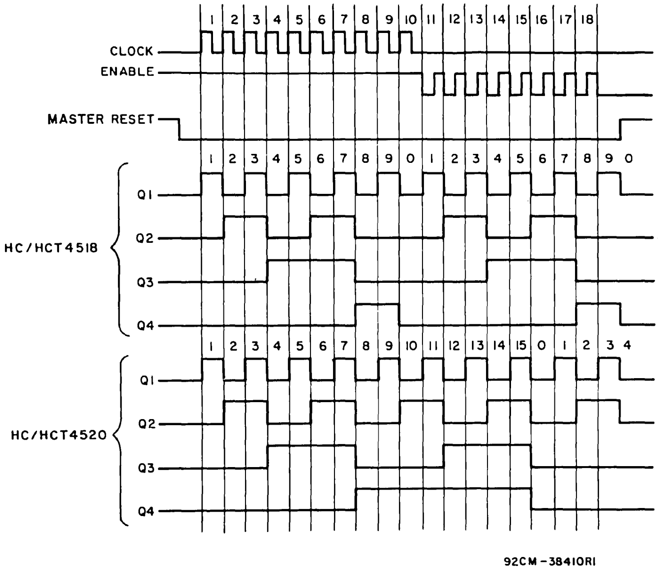


Fig. 4 — Timing Diagrams for CD54/74HC/HCT4518/4520.

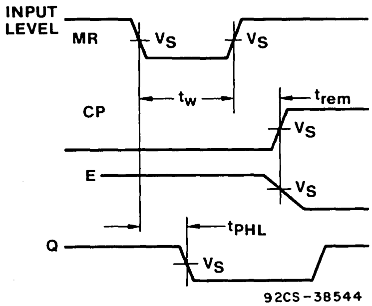


Fig. 5 — Master reset pulse width. Master reset to output delay and master reset to clock recovery times.

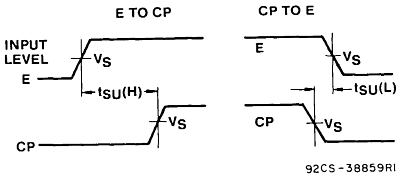


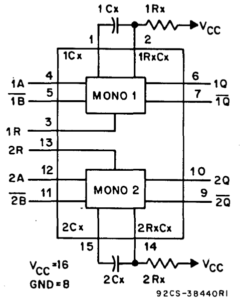
Fig. 6 — Setup Times: E to CP and CP to E.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

CD54/74HC4538
CD54/74HCT4538

File Number **1671**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Retriggerable Precision Monostable Multivibrator

Type Features:

- *Retriggerable/resettable capability*
- *Trigger and Reset propagation delays independent of R_x, C_x*
- *Triggering from the leading or trailing edge*
- *Q and $\overline{Q}$ Buffered Outputs available*
- *Separate Resets*
- *Wide Range of Output-Pulse Widths*
- *Schmitt Trigger input on A and $\overline{B}$ inputs*
- *Retrigger Time is independent of C_x.*

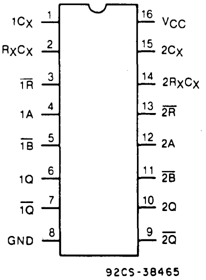
The RCA-CD54/74HC4538 and CD54/74HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (R_x) and an external capacitor (C_x) control the timing and the accuracy for the circuit. Adjustment of R_x and C_x provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_x and C_x.

Leading-edge triggering (A) and trailing edge triggering ($\overline{B}$) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to Gnd and an unused $\overline{B}$ should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-retriggerable mode $\overline{Q}$ is connected to $\overline{B}$ when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering ($\overline{B}$) is used. The period (τ) can be calculated from $\tau = (0.7)\ R_x\ C_x$; R_{min} is 5k ohms. C_{min} is 0 pF.

The CD54HC/HCT4538 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4538 are supplied in 16-lead dual-in-line plastic packages (E suffix), also in 16-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT4538 are also available in chip form (H suffix).

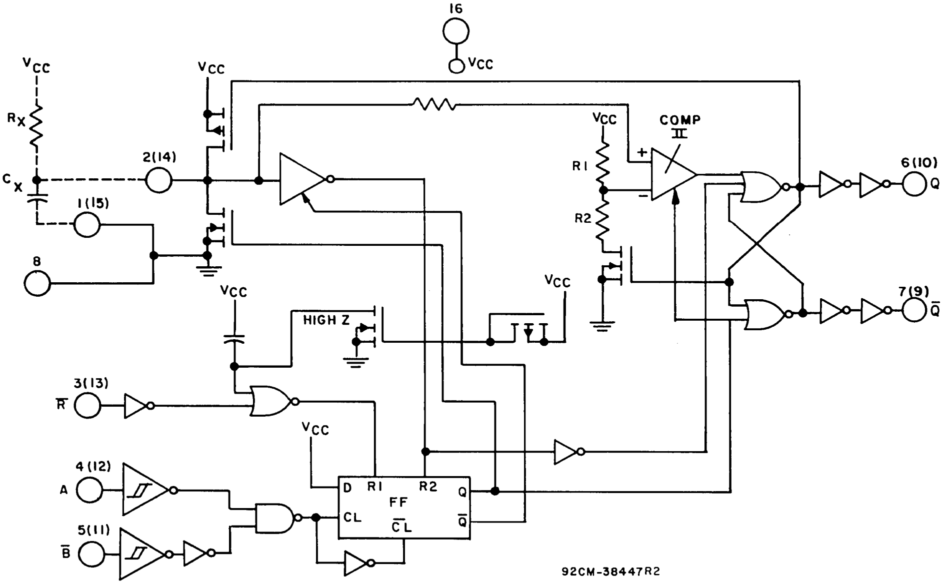
Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85°C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:*
    - *$N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}; @ $V_{CC} = 5$ V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *$V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*



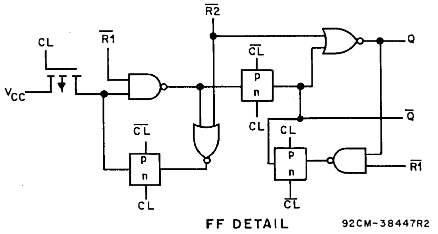
TERMINAL ASSIGNMENT

CD54/74HC4538
CD54/74HCT4538



92CM-38447R2

Fig. 1 - Logic diagram (1 mono).



FF DETAIL 92CM-38447R2

TRUTH TABLE

INPUTS			OUTPUTS	
R̄	A	B̄	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↘	⎍	⊔
H	↗	H	⎍	⊔

H = High Level
L = Low Level
↗ = Transition from Low to High
↘ = Transition from High to Low
⎍ = One High Level Pulse
⊔ = One Low Level Pulse
X = Irrelevant

HC/HCT4538 FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{CC} TO TERM. NO.		Gnd TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO$_1$	MONO$_2$	MONO$_1$	MONO$_2$	MONO$_1$	MONO$_2$	MONO$_1$	MONO$_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

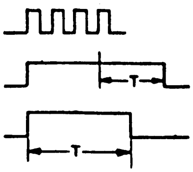
NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (A MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)



CD54/74HC4538
CD54/74HCT4538

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
*DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

*DC INPUT CURRENT FOR C_X R_X PIN = 30 mA

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
Reset Input			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	
Trigger Inputs A or $\overline{B}$			
at 2 V	0	Unlimited	
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	
External Timing Resistor, R_x	5kΩ	#	
External Timing Capacitor, C_X	0	#	

*Unless otherwise specified, all voltages are referenced to Ground.

#The maximum allowable values of R_X and C_X are a function of leakage of capacitor C_X, the leakage of the HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30 mA. Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ.

CD54/74HC4538
CD54/74HCT4538

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4538/CD54HC4538										CD74HCT4538/CD54HCT4538									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Standard Output	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current A, $\overline{B}$, R I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
• Input Leakage Current I_I R_X C_X			6	—	—	±0.05	—	±0.5	—	±0.5		5.5		—	±0.05	—	±0.5	—	±0.5	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Active Device Current Q = High & Pins 2 & 14 @ $V_{CC}/4$ I_{CC}	V_{CC} or Gnd	0	6	—	—	0.6	—	0.8	—	1	V_{CC} or Gnd	5.5	—	—	0.6	—	0.8	—	1	mA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

• When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.

HCT Input Loading Table

Input	Unit Loads*
All	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4538
CD54/74HCT4538

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay					
A, $\overline{B}$ to Q	t_{PLH}	15	21	23	ns
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	15	21	23	ns
$\overline{R}$ to Q	t_{PHL}	15	21	17	ns
$\overline{R}$ to $\overline{Q}$	t_{PLH}	15	21	21	ns
Power Dissipation Capacitance	C_{PD}*	—	136	134	pF

*C_{PD} is used to determine the dynamic power consumption, per one shot.

$P_D = (C_{PD} + C_x) V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:

f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.
assuming $f_i \ll \frac{1}{T}$

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Input Pulse Widths		2	80	—	—	—	100	—	—	—	120	—	—	—	ns
A, $\overline{B}$	t_{WH}	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	t_{WL}	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{R}$	t_{WL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Recovery Time	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Retrigger Time (See Fig. 5)	t_{rr}	5	Typical 175												ns

CD54/74HC4538
CD54/74HCT4538

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, A, $\overline{B}$ to Q	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	55	—	63	—	69	—	75	—	83	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	55	—	63	—	69	—	75	—	83	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{R}$ to Q	t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	40	—	63	—	50	—	75	—	60	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
$\overline{R}$ to $\overline{Q}$	t_{PLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Output Pulse Width R_X=10Ω, C_X=0.1 μF	τ	3	0.64	0.78	—	—	0.612	0.812	—	—	0.605	0.819	—	—	ms
		5	0.63	0.77	0.63	0.77	0.602	0.798	0.602	0.798	0.595	0.805	0.595	0.805	
Output Pulse Width Match, Same Pkg.			Typ ± 1%												
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF

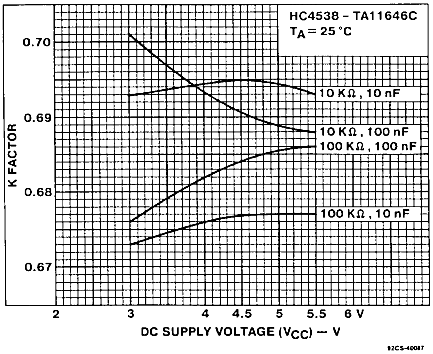


Fig. 2 - K Factor Vs DC Supply Voltage (Vcc)-V.

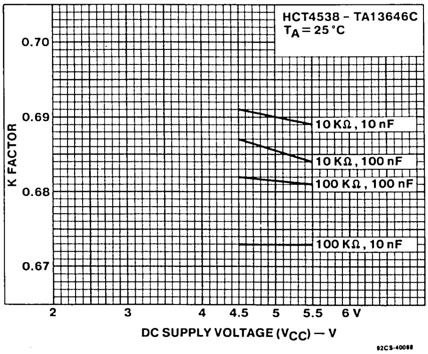


Fig. 3 - K Factor Vs DC Supply Voltage (Vcc)-V.

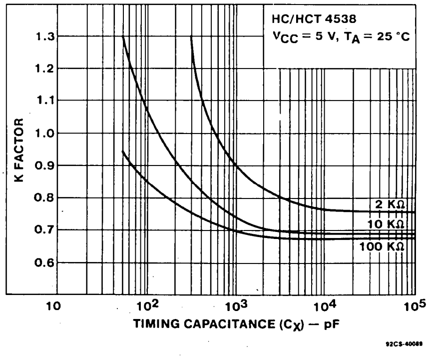


Fig. 4 - K Factor Vs Cx.

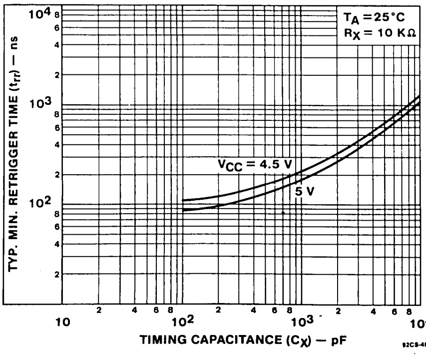
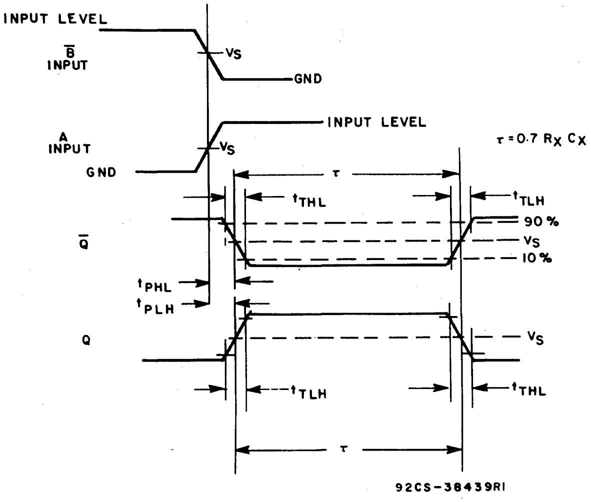
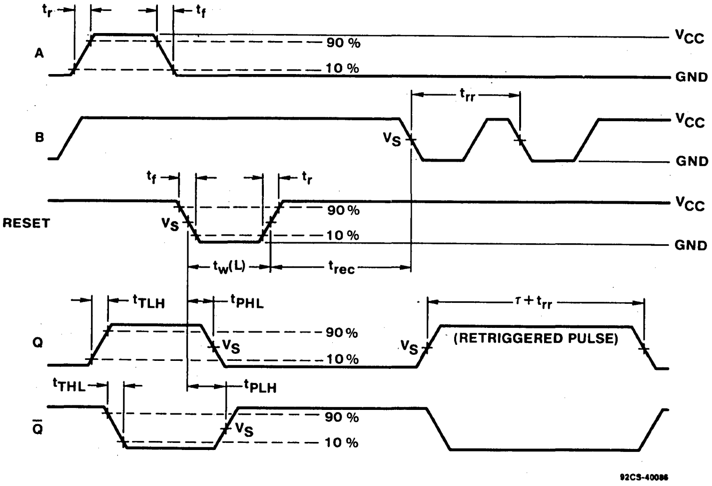


Fig. 5 - Minimum Retrigger Time Vs Timing Capacitance.





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 6 — Switching Waveforms

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Fig. 7.

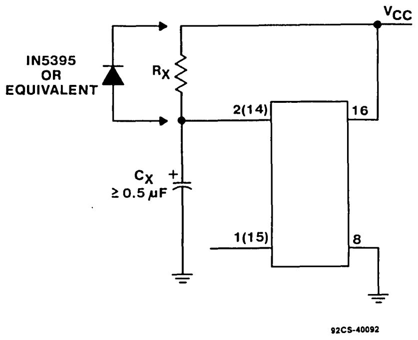


Fig. 7 — Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 8, where a 51-ohm current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

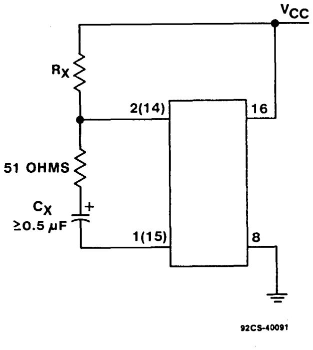
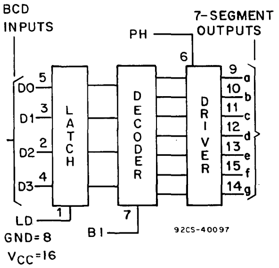


Fig. 8 — Alternate rapid power-down protection circuit.

CD54/74HC4543
CD54/74HCT4543

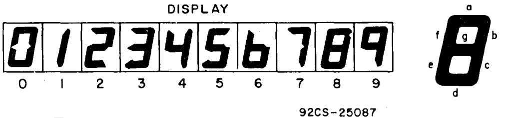
File Number **1822**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

BCD-to-7 Segment Latch/ Decoder/Driver for LCDs



Type Features:
- *Input latches for BCD code storage*
- *Blanking capability*
- *Phase input for complementing outputs*

The RCA CD54/74HC4543 and CD54/74HCT4543 high-speed silicon-gate devices are BCD-to-7 segment latch/decoder/drivers designed primarily for directly driving liquid-crystal displays. They have an active-high disable input (LD), an active high blanking input (BI) and a phase input (PH) to which a square wave is applied for liquid-crystal applications. This square wave is also applied to the backplane of the liquid-crystal display.

These devices can also be used, in conjunction with current amplifying devices, for driving LEDs, incandescent, fluorescent, and gas-discharge displays. For these applications the phase input provides a means for obtaining active-high or active-low segment outputs. (See Function Table.)

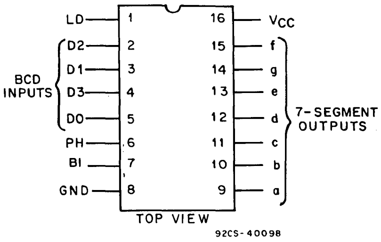
The CD54HC/HCT4543 are supplied in 16-lead ceramic dual-in-line frit-seal packages (F suffix). The CD74HC/HCT-4543 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: −40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity:
  $N_{IL}=30\%$, $N_{IH}=30\%$ *of* V_{CC}; *@* $V_{CC}=5$ *V*
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  $V_{IL}=0.8$ *V max.,* $V_{IH}=2$ *V min.*
  CMOS input compatibility
  $I_I \leq 1$ *µA @* V_{OL}, V_{OH}

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D3	D2	D1	D0	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

**Depends upon the BCD code previously applied when LD = High.



TERMINAL ASSIGNMENT

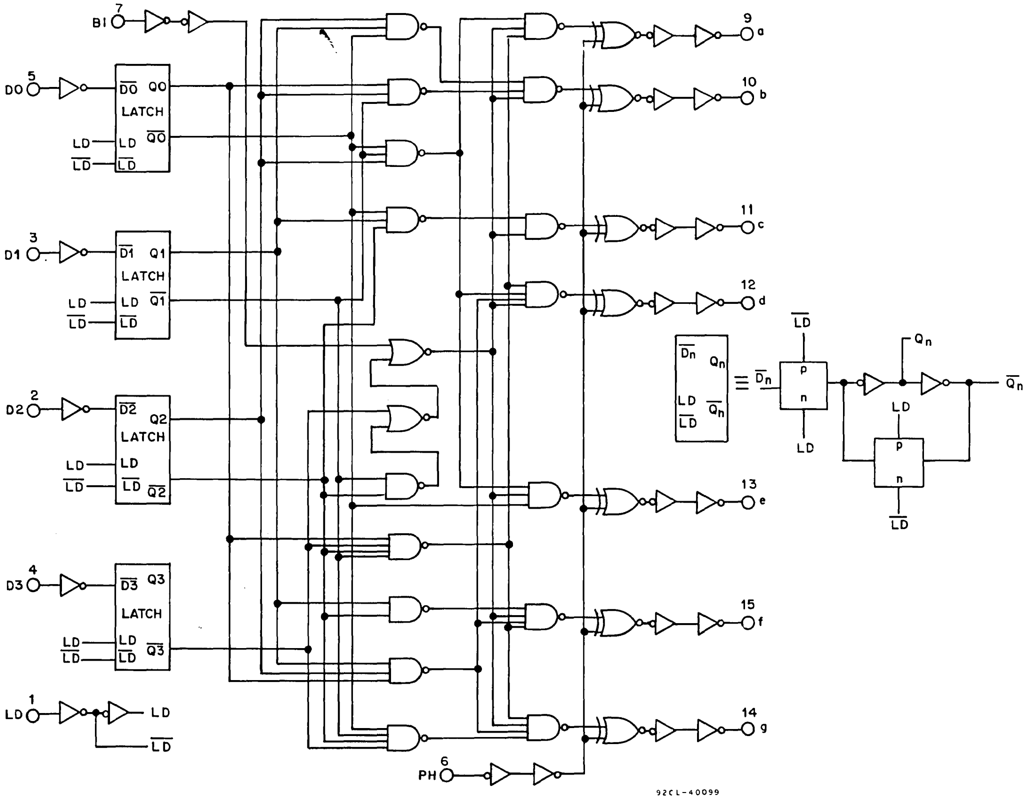


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5 \text{ V} < V_o < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F,H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F,H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	-55 to +125°C
PACKAGE TYPE E,M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

CD54/74HC4543
CD54/74HCT4543

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay: D_n to Output	t_{PLH} t_{PHL}	15	28	33	ns
LD to Output	t_{PLH} t_{PHL}	15	31	32	
BI to Output	t_{PLH} t_{PHL}	15	22	27	
PH to Output	t_{PLH} t_{PHL}	15	17	27	
Power Dissipation Capacitance*	C_{PD}	—	52	54	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 fi + \Sigma\, C_L V_{CC}^2 f_o$ where f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Setup Time, D_n to LD	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time, D_n to LD	t_H	2	30	—	—	—	40	—	—	—	45	—	—	—	
		4.5	6	—	8	—	8	—	10	—	9	—	12	—	
		6	5	—	—	—	7	—	—	—	8	—	—	—	
Latch Disable Pulse Width,	t_W	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	

CD54/74HC4543
CD54/74HCT4543

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4543/CD54HC4543										CD74HCT4543/CD54HCT4543									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads Non-Standard Output	V_{IL} or V_{IH}	-1	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-1.3	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads Non-Standard Output	V_{IL} or V_{IH}	1	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		1.3	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

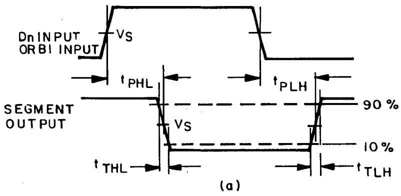
Input	Unit Loads*
D0, D1, D2	1
D3, BI	0.5
PH	1.25
LD	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

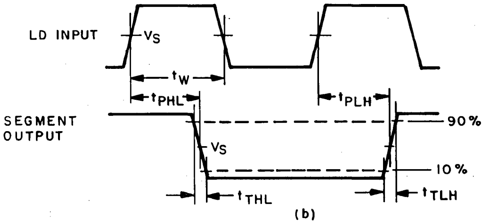
CD54/74HC4543
CD54/74HCT4543

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

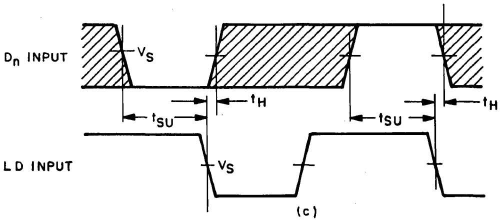
CHARACTERISTIC		V_{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, D_n to Output	t_{PLH}	2	—	340	—	—	—	425	—	—	—	510	—	—	ns
	t_{PHL}	4.5	—	68	—	80	—	85	—	100	—	102	—	120	
		6	—	58	—	—	—	72	—	—	—	87	—	—	
LD to Output	t_{PLH}	2	—	370	—	—	—	465	—	—	—	555	—	—	ns
	t_{PHL}	4.5	—	74	—	77	—	93	—	96	—	111	—	116	
		6	—	63	—	—	—	79	—	—	—	94	—	—	
BI to Output	t_{PLH}	2	—	265	—	—	—	330	—	—	—	400	—	—	ns
	t_{PHL}	4.5	—	53	—	66	—	66	—	83	—	80	—	99	
		6		45	—	—	—	56	—	—	—	68	—	—	
PH to Output	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
	t_{PHL}	4.5	—	40	—	66	—	50	—	83	—	60	—	99	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Time	t_{TLH}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t_{THL}	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



(*a*) WAVEFORMS SHOWING THE ADDRESS AND BLANKING (D_n, BI) TO OUTPUT PROPAGATION DELAYS AND THE OUTPUT TRANSITION TIMES.



(*b*) WAVEFORMS SHOWING THE LATCH DISABLE INPUT (LD) TO OUTPUT PROPAGATION DELAYS AND THE OUTPUT TRANSITION TIMES.



NOTE:
THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE.

(*c*) WAVEFORMS SHOWING THE ADDRESS (D_n) TO LATCH DISABLE (LD) INPUT SET-UP AND HOLD TIMES.

92CM-40103

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - AC waveforms.

APPLICATION CIRCUITS

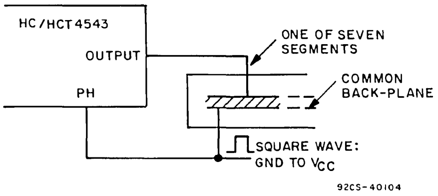


Fig. 3 - Connection to liquid-crystal (LCD) display readout.

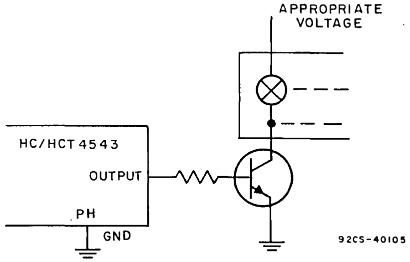


Fig. 4 - Connection to incandescent display readout.

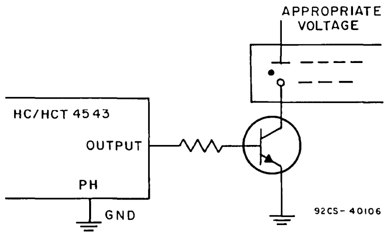


Fig. 5 - Connection to gas-discharge display readout.

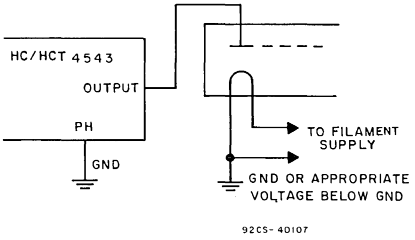
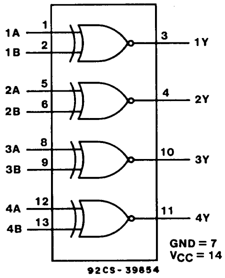


Fig. 6 - Connection to fluorescent display readout.

CD54/74HC7266

File Number **1780**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Exclusive-NOR Gate

Type Features:

- *Four independent Exclusive-NOR gates*
- *Buffered inputs and outputs*

Applications

- *Logical comparators*
- *Parity generators and checkers*
- *Adders/Subtracters*

The RCA CD54/74HC7266 contains four independent EXCLUSIVE-NOR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-NOR function.

This device is functionally the same as the TTL226. They differ in that the HC7266 has active high and low outputs whereas the 226 has open collector outputs.

The CD54HC7266 is supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC7266 is supplied in 14-lead plastic dual-in-line package (E suffix), in a 14-lead dual-in-line surface-mount plastic package (M-suffix), and is also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *2 to 6 V Operation*
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}, @ $V_{CC} = 5$ V
- *CMOS Input Compatibility*
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

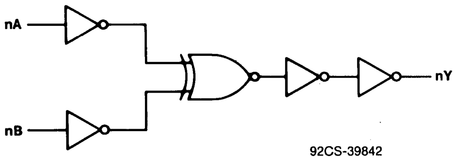


Fig. 1 - Logic diagram each gate.

TRUTH TABLE

INPUTS		OUTPUT
nA	**nB**	**nY**
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level.
L = LOW voltage level.

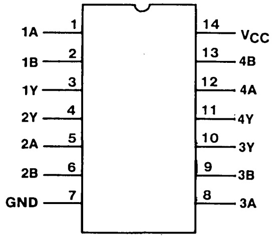
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR V_I <-0.5 V OR $V_I > V_{CC}$ + 0.5 V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR $V_O > V_{CC}$ +0.5 V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < $V_O < V_{CC}$ + 0.5 V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*	2	6	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TOP VIEW
TERMINAL ASSIGNMENT

92CS-39841

TERMINAL ASSIGNMENT

CD54/74HC7266

STATIC ELECTRIC CHARACTERISTICS

CHARACTERISTIC		CD54/74HC7266										UNITS
		TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		
		V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}			2	1.5	—	—	1.5	—	1.5	—	V
				4.5	3.15	—	—	3.15	—	3.15	—	
				6	4.2	—	—	4.2	—	4.2	—	
Low-Level Input Voltage	V_{IL}			2	—	—	0.5	—	0.5	—	0.5	V
				4.5	—	—	1.35	—	1.35	—	1.35	
				6	—	—	1.8	—	1.8	—	1.8	
High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V
				4.5	4.4	—	—	4.4	—	4.4	—	
				6	5.9	—	—	5.9	—	5.9	—	
TTL Loads		V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V
			-5.2	6	5.48	—	—	5.34	—	5.2	—	
Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V
				4.5	—	—	0.1	—	0.1	—	0.1	
				6	—	—	0.1	—	0.1	—	0.1	
TTL Loads		V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V
			5.2	6	—	—	0.26	—	0.33	—	0.4	
Input Leakage Current	I_I	V_{CC} or Gnd		6 —	— —	— —	±0.1 —	— —	±1 —	— —	±1 —	μA
Quiescent Device Current	I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	μA

SWITCHING CHARACTERISTICS ($V_{CC} = 5$ V, $T_A = 25°C$, Input t_r, $t_f = 6$ ns)

CHARACTERISTIC		C_L pF	TYPICAL VALUES 54/74HC	UNITS
Propagation Delay, Any Input	t_{PLH} t_{PHL}	15	9	ns
Power Dissipation Capacitance*	C_{PD}	—	33	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD}+C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input t_r, $t_f = 6$ ns)

CHARACTERISTIC		V_{CC}	25°C		-40°C to +85°C		-55°C to +125°C		UNITS
			HC		74HC		54HC		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}, t_{PHL}	2	—	115	—	145	—	150	ns
		4.5	—	23	—	29	—	35	
		6	—	30	—	25	—	30	
Output Transition Time	t_{TLH}, t_{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	—	10	—	10	—	10	pF

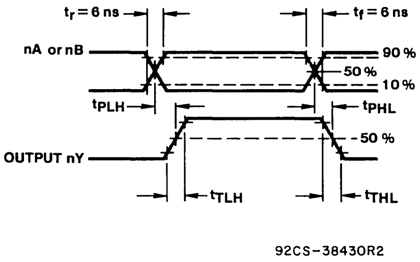
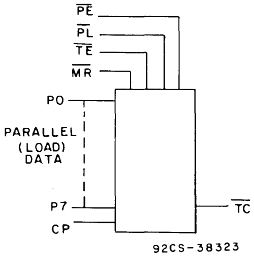


Fig. 2 - Transition times and propagation delay times.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

File Number **1596**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Stage Synchronous Down Counters

40102 - 2-Decade BCD Type
40103 - 8-Bit Binary Type

Type Features:

- *Synchronous or asynchronous preset*
- *Cascadable in synchronous or ripple mode*

The RCA-CD54/74HC40102, 40103 and CD54/74HCT40102, 40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40102 is configured as two cascaded 4-bit BCD counters, and the 40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the $\overline{TC}$ output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the $\overline{TE}$ input is high. The $\overline{TC}$ output goes low when the count reaches zero if the $\overline{TE}$ input is low, and remains low for one full clock period.

When the $\overline{PE}$ input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the $\overline{TE}$ input. When the $\overline{PL}$ input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the $\overline{PE}$, $\overline{TE}$, or CLOCK inputs. Input P0-P7 represent two 4-bit BCD words for the 40102 and a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the 40102 and 225_{10} for the 40103) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{TE}$ are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

The 40102 and 40103 may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity:* $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}; *@* $V_{CC} = 5$ V
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - $V_{IL} = 0.8$ V *Max.,* $V_{IH} = 2$ V *Min.*
  - *CMOS Input Compatibility*
    - $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

These circuits possess the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

The CD54HC40102, 40103, and CD54HCT40102, 40103 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC40102, 40103 and CD74HCT40102, 40103 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V)	±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V)	±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

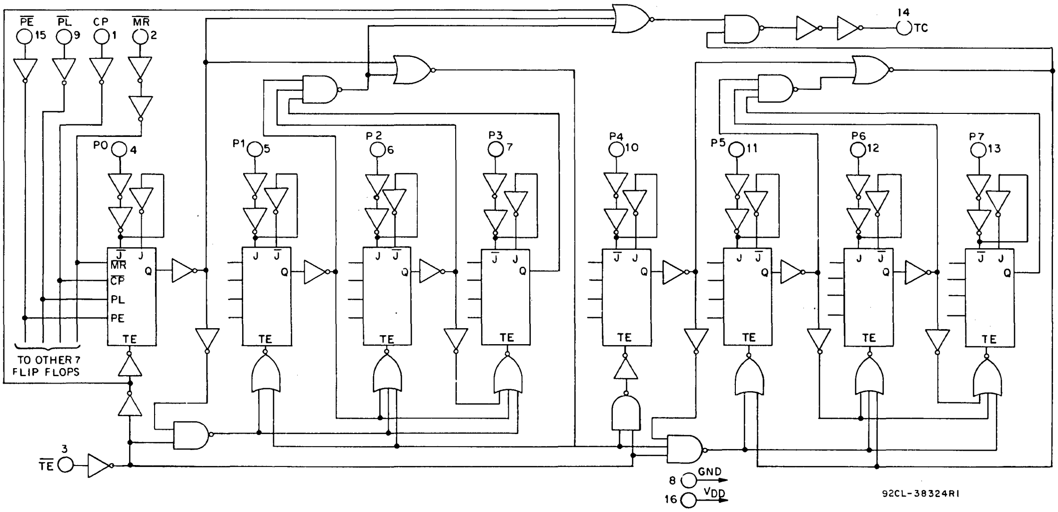


Fig. 1 - Logic diagram for the CD54/74HC/HCT40102.

TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

Notes:

1. 0 = Low Level
   1 = High Level
   X = Don't Care
2. Clock Connected to Clock Input.
3. Synchronous operation: Changes Occur on Negative-to-Positive Clock Transitions.
4. Load Inputs: 40102 BCD: MSD = P7, P6, P5, P4 (P7 is MSB)
   LSD = P3, P2, P1, P0 (P3 is MSB)
   40103 Binary: MSB = P7, LSB = P0

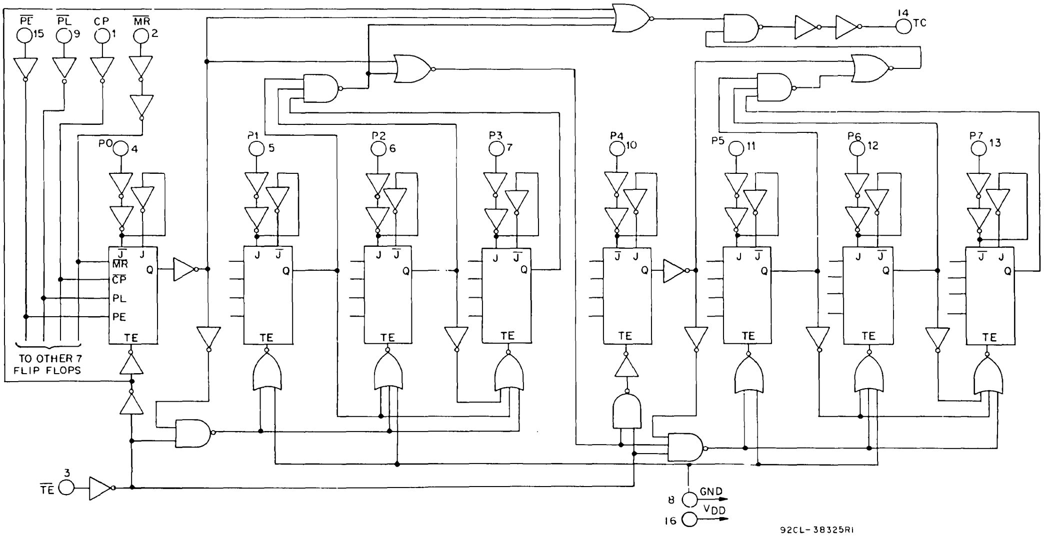
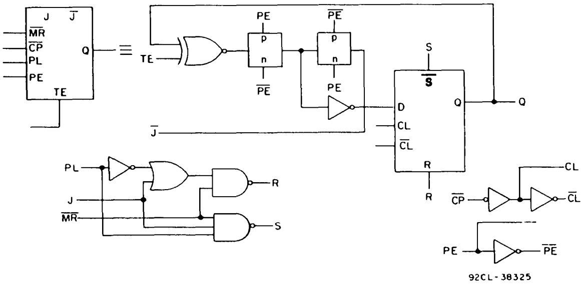


Fig. 2 - Logic diagram for the CD54/74HC/HCT40103.



Flip-Flop detail.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC40102-40103/CD54HC40102-40103										CD74HCT40102-40103/CD54HCT40102-40103									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL}	4.5	4.4	—	—	4.4	—	4.4	—	V
	or		4.5	4.4	—	—	4.4	—	4.4	—	or									
	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
TTL Loads	V_{IL}										V_{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or									
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V
	or		4.5	—	—	0.1	—	0.1	—	0.1	or									
	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
TTL Loads	V_{IL}										V_{IL}	4.5	—	—	0.26	—	0.33	—	0.4	V
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or									
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
P0 - P7	0.20
$\overline{TE}$, $\overline{MR}$	0.40
CP	0.60
$\overline{PE}$	0.80
$\overline{PL}$	1.35

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay CP to $\overline{TC}$ (Sync. Preset)	t_{PHL} t_{PLH}	15	25	25	ns
CP to $\overline{TC}$ (Async. Preset)	t_{PHL} t_{PLH}	15	25	26	ns
$\overline{TE}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	17	21	ns
$\overline{PL}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	23	28	ns
$\overline{MR}$ to $\overline{TC}$	t_{PHL} t_{PLH}	15	23	23	ns
CP Max. Frequency	$f_{MAX.}$	15	25	25	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	27	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + C_L V_{CC}^2 f_o$ where:
f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

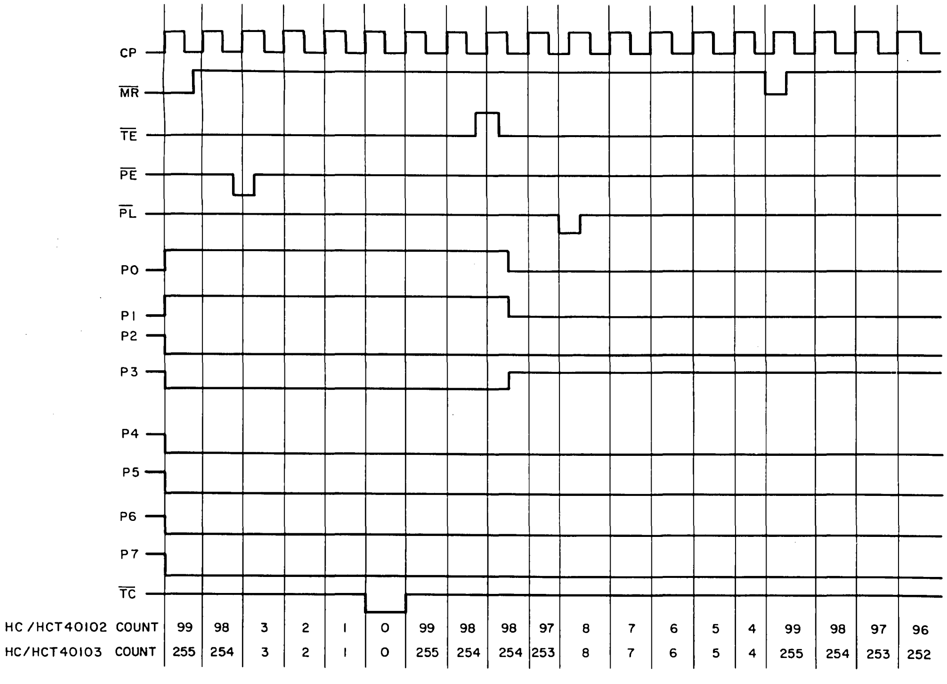


Fig. 3 - Timing diagram for HC/HCT40102 and HC/HCT40103.

CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_W	2	165	—	—	—	205	—	—	—	250	—	—	—	ns
		4.5	33	—	35	—	41	—	44	—	50	—	53	—	
		6	28	—	—	—	35	—	—	—	43	—	—	—	
$\overline{PL}$ Pulse Width	t_W	2	125	—	—	—	155	—	—	—	190	—	—	—	ns
		4.5	25	—	43	—	31	—	54	—	38	—	65	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
$\overline{MR}$ Pulse Width	t_W	2	125	—	—	—	135	—	—	—	190	—	—	—	ns
		4.5	25	—	35	—	31	—	44	—	38	—	53	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
CP Max. Frequency*	$f_{CP(Max.)}$	2	3	—	—	—	2	—	—	—	2	—	—	—	MHz
		4.5	15	—	14	—	12	—	11	—	10	—	9	—	
		6	18	—	—	—	14	—	—	—	12	—	—	—	
P to CP Setup Time	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	24	—	25	—	30	—	30	—	36	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
$\overline{PE}$ to CP Setup Time	t_{SU}	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
		4.5	15	—	20	—	19	—	25	—	22	—	30	—	
		6	13	—	—	—	16	—	—	—	19	—	—	—	
$\overline{TE}$ to CP Setup Time	t_{SU}	2	150	—	—	—	190	—	—	—	225	—	—	—	ns
		4.5	30	—	40	—	38	—	50	—	45	—	60	—	
		6	26	—	—	—	33	—	—	—	38	—	—	—	
P to CP Hold Time	t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{TE}$ to $\overline{CP}$ Hold Time	t_H	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
$\overline{MR}$ to CP Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
$\overline{PE}$ to $\overline{CP}$ Hold Time	t_H	2	2	—	—	—	2	—	—	—	2	—	—	—	ns
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	

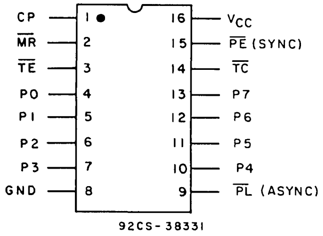
CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	
CP to $\overline{\text{TC}}$	t_{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	ns
(Async Preset)		6	—	51	—	—	—	64	—	—	—	77	—	—	
		2	—	300	—	—	—	375	—	—	—	450	—	—	
CP to $\overline{\text{TC}}$	t_{PLH}	4.5	—	60	—	63	—	75	—	79	—	90	—	95	ns
(Sync Preset)	t_{PHL}	6	—	51	—	—	—	64	—	—	—	77	—	—	
		2	—	200	—	—	—	250	—	—	—	300	—	—	
$\overline{\text{TE}}$ to $\overline{\text{TC}}$	t_{PLH}	4.5	—	40	—	50	—	50	—	63	—	60	—	75	ns
	t_{PHL}	6	—	34	—	—	—	43	—	—	—	51	—	—	
		2	—	275	—	—	—	345	—	—	—	415	—	—	
$\overline{\text{PL}}$ to $\overline{\text{TC}}$	t_{PLH}	4.5	—	55	—	68	—	69	—	85	—	83	—	102	ns
	t_{PHL}	6	—	47	—	—	—	59	—	—	—	71	—	—	
		2	—	275	—	—	—	345	—	—	—	415	—	—	
$\overline{\text{MR}}$ to $\overline{\text{TC}}$	t_{PLH}	4.5	—	55	—	55	—	69	—	69	—	83	—	83	ns
	t_{PHL}	6	—	47	—	—	—	59	—	—	—	71	—	—	
		2	—	75	—	—	—	95	—	—	—	110	—	—	
Output Transition Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
	t_{THL}	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

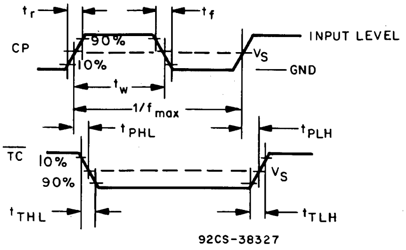
*Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables ($\overline{\text{PE}}$ or $\overline{\text{TE}}$)-to-clock SETUP TIMES, and count enables ($\overline{\text{PE}}$ or $\overline{\text{TE}}$)-to-clock HOLD TIMES determine max. clock frequency. For example, with these HC devices:

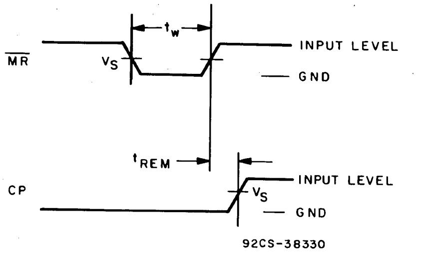
$$C_P\, f_{MAX} = \frac{1}{\text{CP-to-}\overline{\text{TC}}\text{ prop delay} + \overline{\text{TE}}\text{-to-CP Setup Time} + \overline{\text{TE}}\text{-to-CP Hold Time}} = \frac{1}{60+30+0} \approx 11\text{ MHz}$$

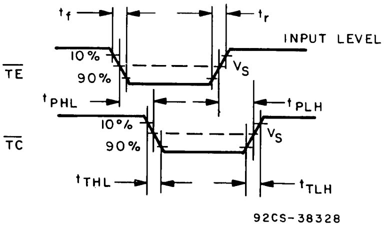


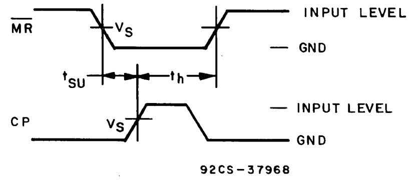
TERMINAL ASSIGNMENT

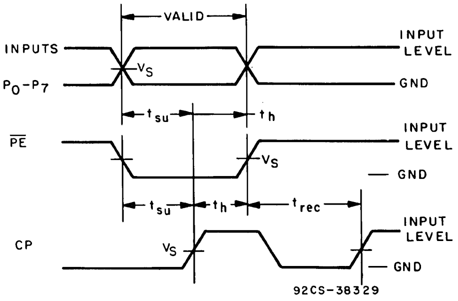
CD54/74HC40102, CD54/74HCT40102
CD54/74HC40103, CD54/74HCT40103

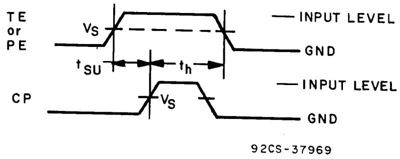












	CD54/74HC	CD54/74HCT
Input Level	Vcc	3 V
Vs	0.5 Vcc	1.3 V

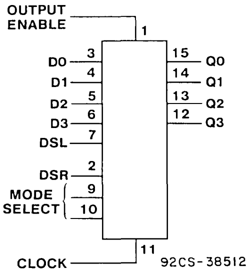
Transition times, propagation delay times, setup and hold times, and removal times.

Technical Data

File Number **1661**

CD54/74HC40104
CD54/74HCT40104

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

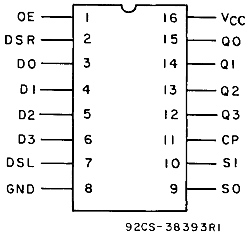
4-Bit Universal Bidirectional Shift Register

Type Features:

- *Four operating modes: shift right, shift left, hold and reset*
- *Three-state outputs*
- *Synchronous parallel or serial operation*
- *Typical* $f_{MAX}=50$ *MHz @* $V_{CC} = 5$ *V,* $C_L = 15$ *pF,* $T_A = 25°$ *C*

The RCA-CD54/74HC40104 and CD54/74HCT40104 are 4-bit shift registers with 3-state bus interface capability. In the parallel mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During parallel loading serial data flow is inhibited. Shift left and Shift right are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and the SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

The CD54HC/HCT40104 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT40104 are supplied in 16-lead plastic dual-in-line packages (E suffix), also in 16-lead surface mount plastic dual-in-line packages (M suffix). These types are also available in chip form (H suffix).

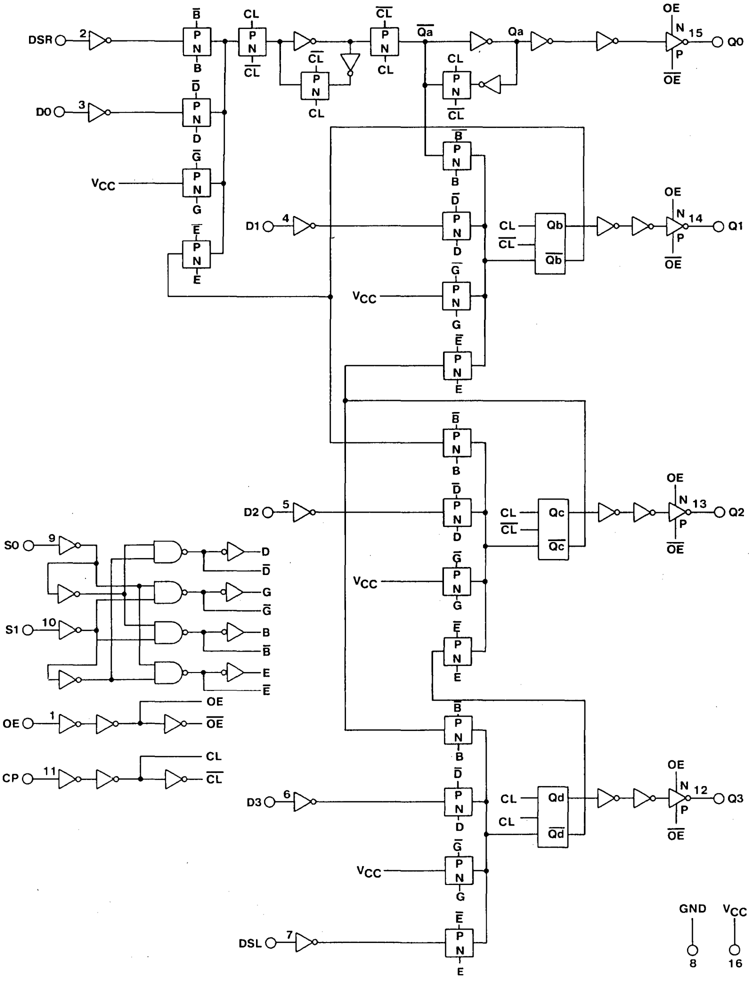


TERMINAL ASSIGNMENT

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: $N_{IL}=30\%, N_{IH}=30\%$ *of* V_{CC}*;*
  @ $V_{CC}=5$ *V*
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
    $V_{IL}=0.8$ *V max.,* $V_{IH}=2$ *V min.*
  CMOS input compatibility
    $I_I \leq 1$ *µA @* V_{OL}*,* V_{OH}

CD54/74HC40104
CD54/74HCT40104



92CL—38513R3

Fig. 1 - Logic diagram.

TRUTH TABLE

CLOCK	MODE SELECT		OUTPUT ENABLE OE	ACTION
	S0	S1		
↑	L	L	H	Reset
↑	H	L	H	Shift right (Q0 toward Q3)
↑	L	H	H	Shift left (Q3 toward Q0)
↑	H	H	H	Parallel load
X	X	X	L	Operations occur as shown above, but outputs assume high impedance

L = Low Voltage Level

H = High Voltage Level

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < 0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC}$ +0.5 V)	±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-65 to +150° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range)			
V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	° C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC40104
CD54/74HCT40104

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC40104/CD54HC40104										CD74HCT40104/CD54HCT40104									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	V_O= V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
OE	1.4
DSR, DSL, D0-D3	0.3
S1, S2	0.7
CP	0.3

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25° C.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES		UNITS
		HC	HCT	
Maximum Frequency (C_L = 15 pF)	f_{MAX}	56	50	MHz
Propagation Delay: (C_L = 15 pF) CP to Qn	t_{PLH} t_{PHL}	17	18	ns
Output Disable Time	t_{PLZ} t_{PHZ}	14	18	
Output Enable Time	t_{PZL} t_{PZH}	12	12	
Power Dissipation Capacitance	C_{PD}*	84	85	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
PD=C_{PD} V_{CC}^2 fi + Σ (C_L V_{CC}^2 fo) where: f_i=input frequency
f_o=output frequency
C_L=output load capacitance
V_{CC}=supply voltage

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	28	—	25	—	22	—	20	—	19	—	17	—	
		6	33	—	—	—	26	—	—	—	22	—	—	—	
Clock Pulse Width	t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Times Dn, DSL, DSR, S1, and S0 to Clock	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Times Dn, DSO, DSI, S1, and S0 to Clock	t_H	2	2	—	—	—	2	—	—	—	2	—	—	—	
		4.5	2	—	2	—	2	—	2	—	2	—	2	—	
		6	2	—	—	—	2	—	—	—	2	—	—	—	

CD54/74HC40104
CD54/74HCT40104

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
CP to Qn	t_{PHL}	4.5	—	40	—	42	—	50	—	53	—	60	—	63	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Output Disable	t_{PLZ}	2	—	175	—	—	—	219	—	—	—	263	—	—	
Time	t_{PHZ}	4.5	—	35	—	44	—	44	—	55	—	53	—	66	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enable	t_{PZL}	2	—	150	—	—	—	188	—	—	—	225	—	—	
Time	t_{PZH}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
		6	—	26	—	—	—	32	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	

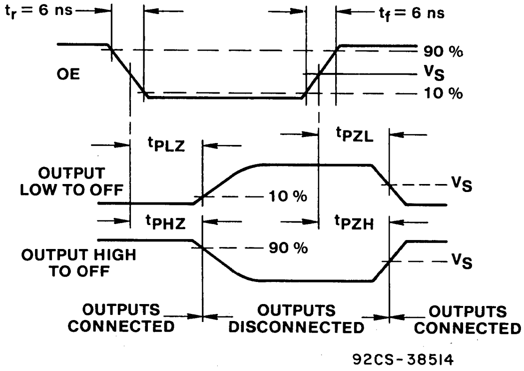


Fig. 2 - Output enable and disable times.

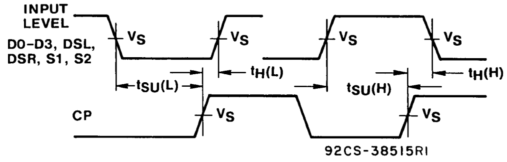


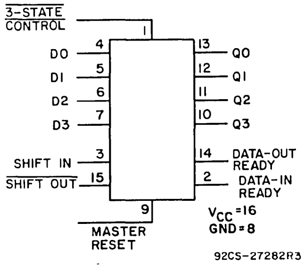
Fig. 3 - Setup and hold times.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

File Number **1834**

CD54/74HC40105
CD54/74HCT40105

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit x 16-Word FIFO Register

Type Features:
- *Independent asynchronous inputs and outputs*
- *Expandable in either direction*
- *Reset capability*
- *Status indicators on inputs and outputs*
- *3-state outputs*
- *Shift-out independent of 3-state control*

Applications:
- *Bit-rate smoothing*
- *CPU/terminal buffering*
- *Data communications*
- *Peripheral buffering*
- *Line printer input buffers*
- *Auto-dialers*
- *CRT buffer memories*
- *Radar data acquisition*

The RCA-CD54/74HC40105 and CD54/74HCT40105 are high-speed silicon-gate CMOS devices that are compatible, except for "shift-out" circuitry, with the RCA-CD40105B. They are low-power first-in-first-out (FIFO) "elastic" storage registers that can store 16 four-bit words. The 40105 is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ *of* V_{CC}, *@* $V_{CC} = 5$ *V*
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  $V_{IL} = 0.8$ *V Max.,* $V_{IH} = 2$ *V Min.*
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ *@* V_{OL}, V_{OH}

Unloading Data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs. Data of other words can be removed by a negative-going transition on the shift-out input ($\overline{SO}$). This negative-going transition causes the DOR signal to go LOW while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go high again, signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH.

CD54/74HC40105
CD54/74HCT40105

If during unloading SI is HIGH, data on the data input of the FIFO is entered in the first location.

Master Reset
A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. Thus, MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D0 to D3) are immediately moved into the first location upon completion of the reset process.

3-State Outputs
In order to facilitate data busing, 3-state outputs (Q0 to Q3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the 3-state control flag (output enable input $\overline{OE}$) forces the outputs into the high-impedance OFF-state mode. Note that the shift-out signal, unlike that in the RCA-CD40105B, is independent of the 3-state output control. In the CD40105B, the 3-state control must not be shifted from High to Low when the shift-out signal is Low (data loss would occur). In the high-speed CMOS version this restriction has been eliminated.

Cascading
The 40105 can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than four bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figs. 3 and 4).

The CD54HC40105 and CD54HCT40105 are supplied in 16-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC40105 and CD74HCT40105 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5 V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC}$ +0.5 V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T_{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

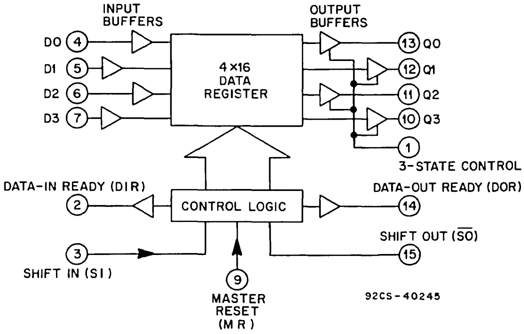
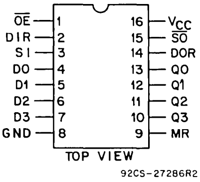


Fig. 1 - Functional block diagram.



TERMINAL ASSIGNMENT

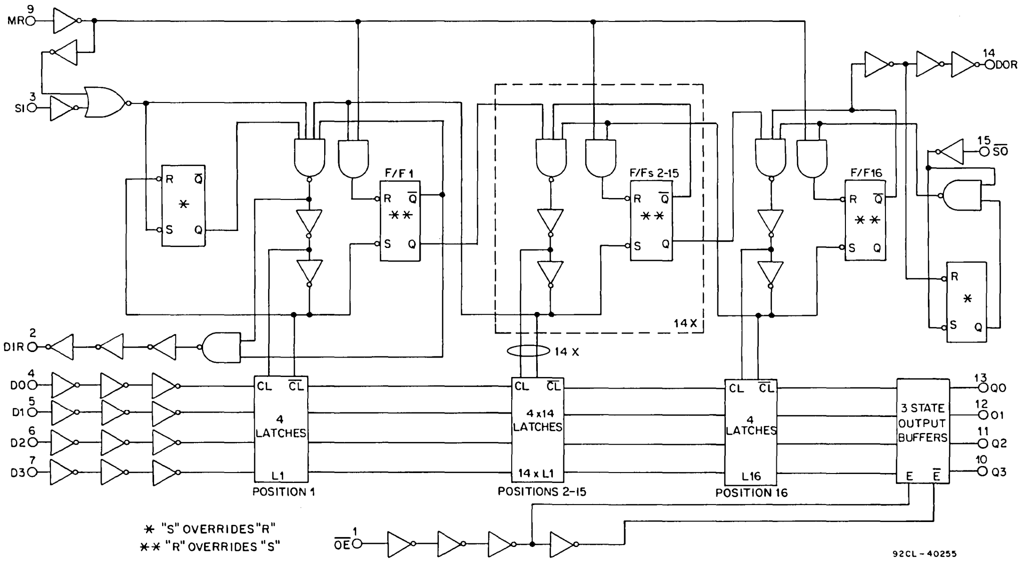


Fig. 2 - Logic diagram.

CD54/74HC40105
CD54/74HCT40105

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC40105/CD54HC40105										CD74HCT40105/CD54HCT40105									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	V_O=V_{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{OE}$	0.75
SI, $\overline{SO}$	0.4
Dn	0.3
MR	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r,t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay	t_{PLH} t_{PHL}	15			ns
MR to DIR, DOR			15	15	
$\overline{\text{SO}}$ to Qn			35	35	
SI to DIR	t_{PHL}		18	18	
$\overline{\text{SO}}$ to DOR			18	18	
Maximum SI, $\overline{\text{SO}}$ Frequency	$f_{max.}$	15	32	32	MHz
Power Dissipation Capacitance*	C_{PD}	—	83	83	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
PD = C_{PD} V_{CC}^2 f_i + Σ (C_L V_{CC}^2 f_o) where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

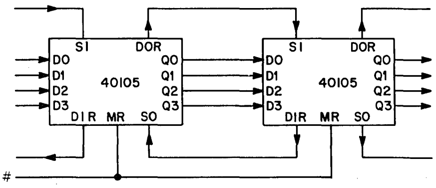
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
SI Pulse Width: t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
HIGH or LOW Fig. 6	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{\text{SO}}$ Pulse Width t_w	2	120	—	—	—	150	—	—	—	180	—	—	—	
HIGH or LOW Fig. 7	4.5	24	—	16	—	30	—	20	—	36	—	24	—	
	6	20	—	—	—	26	—	—	—	31	—	—	—	
DIR Pulse Width t_w	2	200	—	—	—	250	—	—	—	300	—	—	—	
HIGH or LOW Fig. 6	4.5	40	—	40	—	50	—	50	—	60	—	60	—	
	6	34	—	—	—	43	—	—	—	51	—	—	—	
DOR Pulse Width t_w	2	200	—	—	—	250	—	—	—	300	—	—	—	
HIGH or LOW Fig. 7	4.5	40	—	40	—	50	—	50	—	60	—	60	—	
	6	34	—	—	—	43	—	—	—	51	—	—	—	
MR Pulse Width t_w	2	120	—	—	—	150	—	—	—	180	—	—	—	
HIGH Fig. 5	4.5	24	—	24	—	30	—	30	—	36	—	36	—	
	6	20	—	—	—	26	—	—	—	31	—	—	—	
Removal Time t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	
MR to SI Fig. 12	4.5	10	—	15	—	13	—	19	—	15	—	22	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	
Setup Time t_{SU}	2	5	—	—	—	5	—	—	—	5	—	—	—	
Dn to SI Fig. 13	4.5	5	—	0	—	5	—	0	—	5	—	0	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	
Hold Time t_H	2	125	—	—	—	155	—	—	—	190	—	—	—	
Dn to SI Fig. 13	4.5	25	—	25	—	31	—	31	—	38	—	38	—	
	6	21	—	—	—	26	—	—	—	32	—	—	—	
Maximum Pulse f_{MAX}	2	3	—	—	—	2	—	—	—	2	—	—	—	MHz
Frequency Figs. 6, 7	4.5	15	—	15	—	12	—	12	—	10	—	10	—	
SI, $\overline{\text{SO}}$	6	18	—	—	—	14	—	—	—	12	—	—	—	

CD54/74HC40105
CD54/74HCT40105

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		V_{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PLH}	4.5	—	35	—	36	—	44	—	45	—	53	—	54	
MR to DIR, DOR	Fig. 5	6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay,	t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	42	—	53	—	53	—	63	—	63	
SI to DIR	Fig. 6	6	—	36	—	—	—	45	—	—	—	54	—	—	
Propagation Delay,	t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	42	—	53	—	53	—	63	—	63	
$\overline{SO}$ to DOR	Fig. 7	6	—	36	—	—	—	45	—	—	—	54	—	—	
Propagation Delay,	t_{PHL}	2	—	400	—	—	—	500	—	—	—	600	—	—	
	t_{PLH}	4.5	—	80	—	80	—	100	—	100	—	120	—	120	
$\overline{SO}$ to Qn	Fig. 8	6	—	68	—	—	—	85	—	—	—	102	—	—	
Propagation Delay/	t_{PLH}	2	—	2000	—	—	—	2500	—	—	—	3000	—	—	
Ripple thru Delay		4.5	—	400	—	400	—	500	—	500	—	600	—	600	
SI to DOR	Fig. 9	6	—	340	—	—	—	425	—	—	—	510	—	—	
Propagation Delay/	t_{PLH}	2	—	2500	—	—	—	3125	—	—	—	3750	—	—	
Ripple thru Delay		4.5	—	500	—	500	—	625	—	625	—	750	—	750	
$\overline{SO}$ to DIR	Fig. 10	6	—	425	—	—	—	532	—	—	—	638	—	—	
Propagation Delay/	t_{PHL}	2	—	1500	—	—	—	1900	—	—	—	2250	—	—	
Ripple thru Delay	t_{PLH}	4.5	—	300	—	300	—	380	—	380	—	450	—	450	
SI to Qn		6	—	260	—	—	—	330	—	—	—	380	—	—	
3-State Output	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Enable	t_{PZL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
$\overline{OE}$ to Qn	Fig. 11	6	—	26	—	—	—	33	—	—	—	38	—	—	
3-State Output	t_{PHZ}	2	—	140	—	—	—	175	—	—	—	210	—	—	
Disable	t_{PLZ}	4.5	—	28	—	30	—	35	—	38	—	42	—	45	
$\overline{OE}$ to Qn	Fig. 11	6	—	24	—	—	—	30	—	—	—	36	—	—	
Output Transition	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	Fig. 8	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	—	15	—	15	—	15	—	15	



#MASTER RESET pulse must be applied when cascading by 16 N bits.

Fig. 3 - Expansion, 4-bits wide by 16 N-bits long.

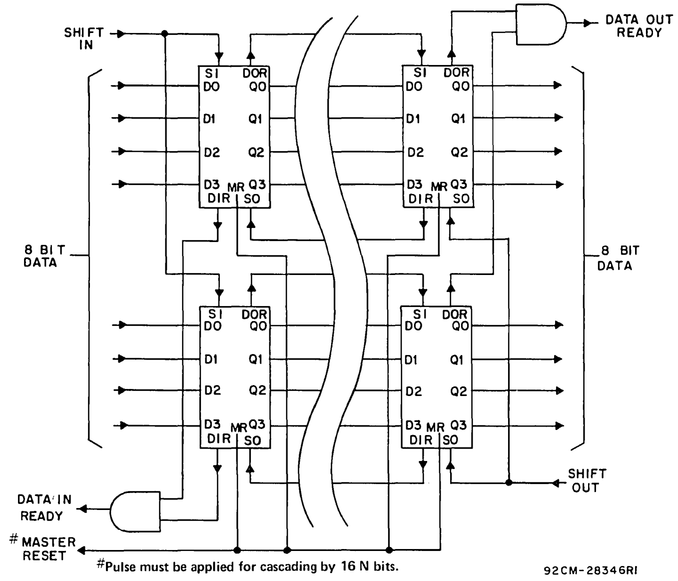


Fig. 4 - Expansion, 8-bits wide by 16 N-bits long using HC/HCT40105.

AC WAVEFORMS

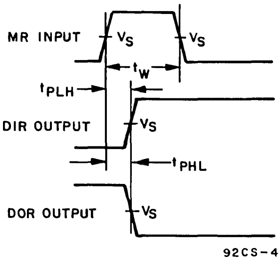


Fig. 5 - Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

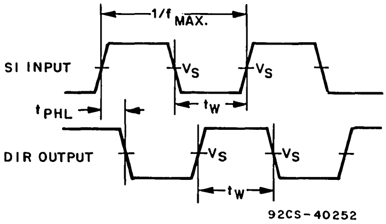


Fig. 6 - Waveforms showing the SI input to DIR output propagation delay. The SI, DIR pulse widths and SI maximum pulse frequency.

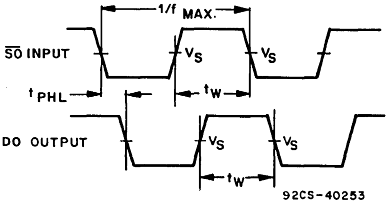


Fig. 7 - Waveforms showing the $\overline{SO}$ input to DOR output propagation delay. The $\overline{SO}$, DOR pulse widths and $\overline{SO}$ maximum pulse frequency.

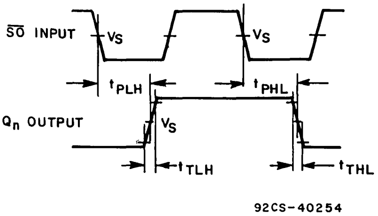


Fig. 8 - Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

CD54/74HC40105
CD54/74HCT40105

AC WAVEFORMS (Cont'd)

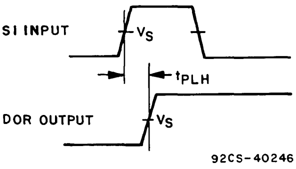


Fig. 9 - Waveforms showing the SI input to DOR output propagation/ripple-through delay.

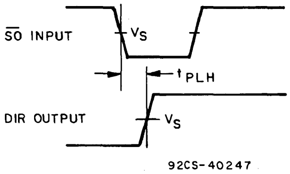


Fig. 10 - Waveforms showing the $\overline{SO}$ input to DIR output propagation/ripple-through delay.

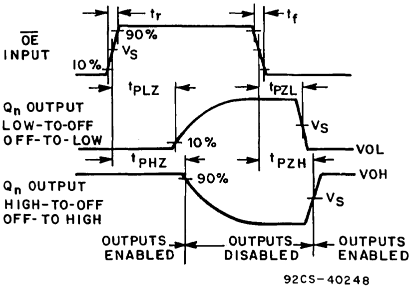


Fig. 11 - Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

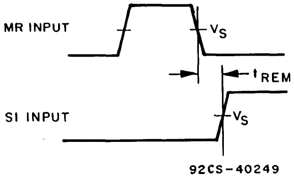
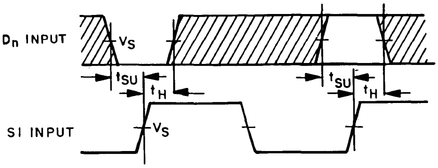


Fig. 12 - Waveforms showing the MR input to SI input removal time.

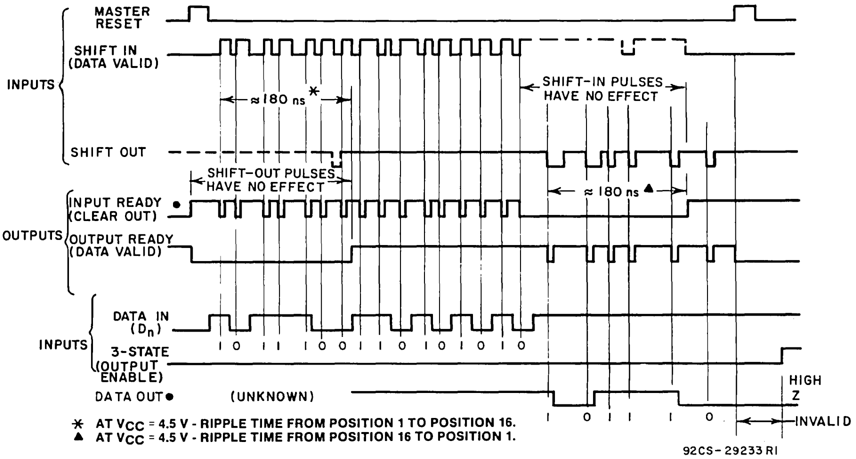


NOTE
THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE. 92CS-40250

Fig. 13 - Waveforms showing hold and set-up times for D_n input to SI input.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

● DATA VALID GOES TO HIGH LEVEL IN ADVANCE OF THE DATA OUT BY A MAXIMUM OF 38 ns AT V_{CC} = 4.5 V, FOR C_L = 50 pF AND T_A = 25°C



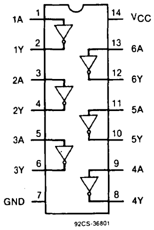
✱ AT V_{CC} = 4.5 V - RIPPLE TIME FROM POSITION 1 TO POSITION 16.
▲ AT V_{CC} = 4.5 V - RIPPLE TIME FROM POSITION 16 TO POSITION 1.

Fig. 14 - Timing diagram for the CD54/74HC/HCT40105.

CD54/74HCU04

File Number **1655**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Hex Inverter

Type Features:

- *Typical propagation delay=6 ns @ V_{CC}=5 V C_L=15 pF, T_A=25° C, fastest part in QMOS line*
- *Wide operating temperature range: CD74HCU04: −40° C to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HCU04/CD74HCU04 types: 2 to 6 V operation High noise immunity: N_{IL}=20%, N_{IH}=30% of V_{CC}; @ V_{CC}=5 V*
- *CMOS input compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

The RCA-CD54/74HCU04 unbuffered hex inverter utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. These devices are especially useful in crystal oscillator and analog applications. Figs. 4 and 5 are supplied as design information for the above applications.

The CD54HCU04 is supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HCU04 is supplied in 14-lead dual-in-line plastic packages (E suffix). The CD74HCU04 is supplied in 14-lead dual-in-line surface mount plastic packages (M suffix). These types are also available in chip form (H suffix).

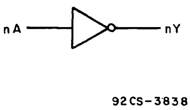


Fig. 1 - Logic diagram.

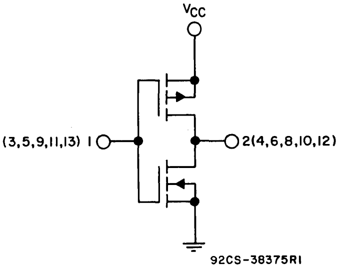


Fig. 2 - Inverter schematic.

CD54/74HCU04

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V)	±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V)	±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} +0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*	2	6	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			°C
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f:			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HCU04

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			CD54HCU04 CD74HCU04		CD74HCU04		CD54HCU04		UNITS
	V_I	I_O	V_{CC}	+25° C		-40° C to +85° C		-55° C to +125° C		
	V	mA	V	Min.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}	—	—	2	1.7	—	1.7	—	1.7	—	V
	—	—	4.5	3.6	—	3.6	—	3.6	—	
	—	—	6	4.8	—	4.8	—	4.8	—	
Low-Level Input Voltage V_{IL}	—	—	2	—	0.3	—	0.3	—	0.3	
	—	—	4.5	—	0.8	—	0.8	—	0.8	
	—	—	6	—	1.1	—	1.1	—	1.1	
High-Level Output Voltage V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.8	—	1.8	—	1.8	—	
			4.5	4	—	4	—	4	—	
			6	5.5	—	5.5	—	5.5	—	
	V_{CC} or Gnd	-4	4.5	3.98	—	3.84	—	3.7	—	
		-5.2	6	5.48	—	5.34	—	5.2	—	
Low-Level Output Voltage V_{OL}	V_{IL} or V_{IH}	0.02	2	—	0.2	—	0.2	—	0.2	
			4.5	—	0.5	—	0.5	—	0.5	
			6	—	0.5	—	0.5	—	0.5	
	V_{CC} or Gnd	4	4.5	—	0.26	—	0.33	—	0.4	
		5.2	6	—	0.26	—	0.33	—	0.4	
Input Leakage Current I_I	V_{CC} or Gnd	—	6	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	2	—	20	—	40	

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL VALUES	UNITS
		CD54/74U04	
Propagation Delay, Data Input to Output Y (Fig. 3) (C_L=15 pF)	t_{PLH} t_{PHL}	5	ns
Power Dissipation Capacitance*	C_{PD}	14	pF

*C_{PD} is used to determine the dynamic power consumption, per inverter when:
$P_D=V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i=input frequency
C_L=output load capacitance
V_{CC}=supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C		-40° C to +85° C		-55° C to +125° C		UNITS
			CD54/74HCU04		CD74HCU04		CD54HCU04		
			Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Input to Output (See Fig. 3)	t_{PLH} t_{PHL}	2	—	70	—	90	—	105	ns
		4.5	—	14	—	18	—	21	
		6	—	12	—	15	—	18	
Transition Times (Fig. 3)	t_{TLH} t_{THL}	2	—	75	—	95	—	110	
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C_I	—	See Fig. 5						

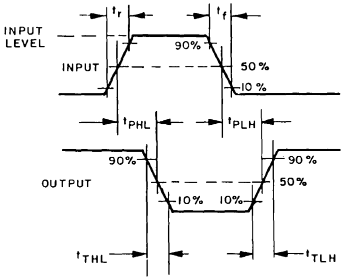


Fig. 3 - Propagation delay and transition times.

DESIGN INFORMATION FOR CRYSTAL OSCILLATOR AND ANALOG APPLICATIONS

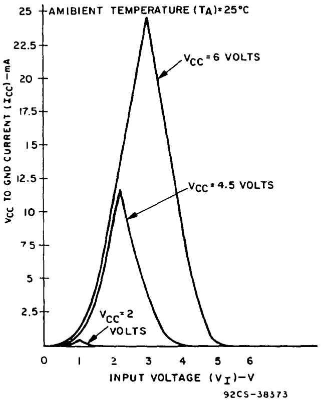


Fig. 4 - Typical inverter supply current as a function of input voltage.

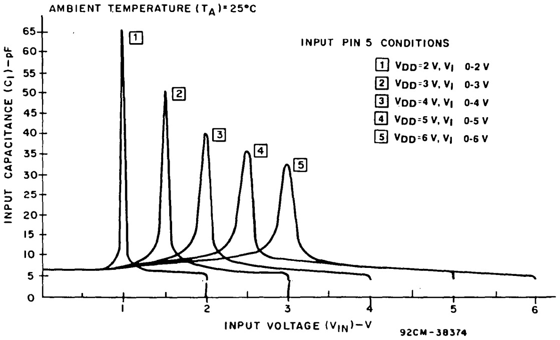


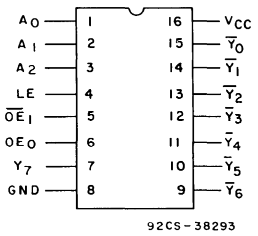
Fig. 5 - Input capacitance as a function of input voltage.

Preview Data

The types shown in the Preview Data section contain information on a product under development. RCA reserves the right to change or discontinue this product without notice.

CD54HC137/74HC137
CD54HCT137/74HCT137

3 to 8 Decoder/Demultiplexer, with Address Latch



TERMINAL ASSIGNMENT

TRUTH TABLE

INPUTS						OUTPUTS							
LE	OE_0	$\overline{OE}_1$	A_2	A_1	A_0	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	*							

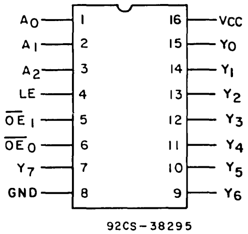
* = Depends upon the address previously applied while LE was at a logic low.

Typical Switching Characteristics (V_{CC} = 5V, GND = 0V, t_r = t_f = 6ns)

CHARACTERISTICS		15pF	50pF	UNITS
		54/74HC/HCT	54/74HC/HCT	
Propagation Delay Time	t_{PHL}	20	23	ns
A to Y	t_{PLH}	14	16	
$\overline{OE}_1$ to $\overline{Y}$	t_{PHL}	15	18	
	t_{PLH}	11	12	
OE_0 to $\overline{Y}$	t_{PHL}	16	18	
	t_{PLH}	12	14	
LE to $\overline{Y}$	t_{PHL}	21	24	
	t_{PLH}	14	17	

CD54/74HC237
CD54/74HCT237

3-to-8 Line Decoder/Demultiplexer with Address-Latches



TERMINAL ASSIGNMENT

TRUTH TABLE

INPUTS						OUTPUTS							
LE	OE_0	$\overline{OE}_1$	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	L	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*							

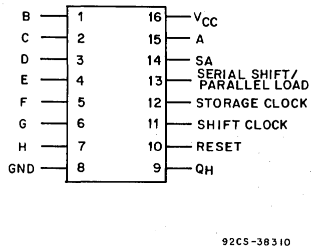
* = Depends upon the address previously.
applied while LE was at a logic low.

Typical Switching Characteristics (V_{CC} = 5V, GND = 0V, t_r = t_f = 6ns)

CHARACTERISTICS		15pF	50pF	UNITS
		54/74HC/HCT	54/74HC/HCT	
Propagation Delay Time	t_{PHL}	15	18	ns
A to Y	t_{PLH}	20	22	
$\overline{OE}_1$ to Y	t_{PHL}	12	14	
	t_{PLH}	17	19	
OE_0 to Y	t_{PHL}	16	18	
	t_{PLH}	17	19	
LE to Y	t_{PHL}	16	18	
	t_{PLH}	21	24	

CD54HC597/74HC597
CD54HCT597/74HCT597

8-Bit Serial- or Parallel Input/Serial-Output Shift Register with Input Storage

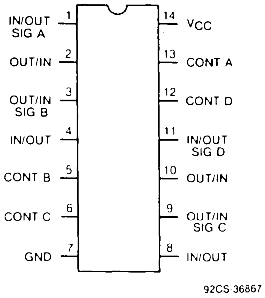


TERMINAL ASSIGNMENT

Typical Switching Characteristics (V_{CC} = 5V, GND = 0V, t_r = t_f = 6ns)

CHARACTERISTICS		15pF	50pF	UNITS
		54/74HC/HCT	54/74HC/HCT	
Propagation Delay Time Shift Clock to Q_H	t_{PHL}, t_{PLH}	14	17	ns
Storage Clock to Q_H	t_{PHL}, t_{PLH}	21	24	
Parallel Load to Q_H	t_{PHL}, t_{PLH}	14	17	

CD54/74HC4016, CD54/74HCT4016 Quad Bilateral Switch



TERMINAL ASSIGNMENT

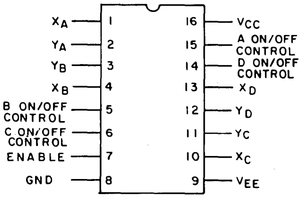
Dynamic Electrical Characteristics @ $T_A = 25°C$, $V_{CC} = 5$ V, t_r, $t_f = 6$ ns

Symbol	Parameter	Test Conditions	Typical	Units
t_{PHL}/t_{PLH}	Propagation Delay: Sw. Input to Output	$C_L = 15$ pF $C_L = 50$ pF	3 5	ns ns
	Turn-On Delay and Turn-Off Delay*	$C_L = 15$ pF $C_L = 50$ pF	6 8	ns ns
R_{ON}	On-State Resistance	$R_L = 1$ KΩ $C_L = 50$ pF	200	Ω

*Turn-On measured 50% to 50%, Turn-Off measured 50% to 10%.

CD54HC4316/74HC4316 CD54HCT4316/74HCT4316

Quad Analog Switch/Multiplexer/ Demultiplexer with Separate Analog and Digital Power Supplies



92CS-38311

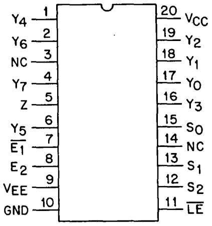
TERMINAL ASSIGNMENT

Typical Switching Characteristics (V_{CC} = 5V, GND = 0, t_r = t_f = 6ns)

CHARACTERISTICS	15pF	50pF	UNITS
	54/74HC/HCT	54/74HC/HCT	
Propagation Delay Time t_{PZL}, t_{PZH} Switch "Turn-ON"	12	14	ns
Switch "Turn-OFF" t_{PHZ}, t_{PLZ}	12	14	

CD54HC4351/74HC4351 CD54HCT4351/74HCT4351

8-Channel Analog Multiplexer/ Demultiplexer with Address Latch



92CS-40544

TERMINAL ASSIGNMENT

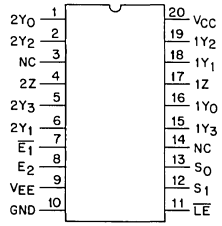
FUNCTION TABLE

Control Inputs					ON Switches (LE = H)*
		Select			
Enable 1	Enable 2	C	B	A	
L	H	L	L	L	Y0
L	H	L	L	H	Y1
L	H	L	H	L	Y2
L	H	L	H	H	Y3
L	H	H	L	L	Y4
L	H	H	L	H	Y5
L	H	H	H	L	Y6
L	H	H	H	H	Y7
H	L	X	X	X	None

X = Don't Care

*When Latch Enable is low, the Channel-Select data is latched, and the switches do not change state.

CD54HC4352/74HC4352 CD54HCT4352/74HCT4352 Dual 4-Channel Analog Multiplexer/ Demultiplexer with Address Latch



92CS-40545

TERMINAL ASSIGNMENT

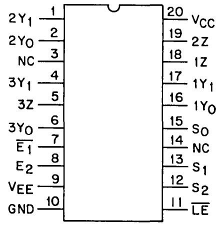
FUNCTION TABLE

Control Inputs				ON Switches (LE=H)*	
		Select			
Enable 1	Enable 2	B	A		
L	H	L	L	1Y0	2Y0
L	H	L	H	1Y1	2Y1
L	H	H	L	1Y2	2Y2
L	H	H	H	1Y3	2Y3
H	L	X	X	None	

X = Don't Care

*When Latch Enable is low, the Channel-Select data is latched, and the switches do not change state.

CD54HC4353/74HC4353 CD54HCT4353/74HCT4353 Triple 2-Channel Analog Multiplexer/Demultiplexer with Latch



92CS-40546

TERMINAL ASSIGNMENT

TRUTH TABLE

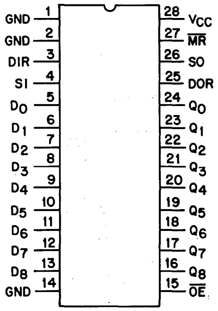
INPUTS						ON CHANNELS		
$\overline{E1}$	E2	LE	S2	S1	S0	NONE		
H	X	X	X	X	X			
X	L	X	X	X	X			
L	H	H	L	L	L	$1Y_0$	$2Y_0$	$3Y_0$
L	H	H	L	L	H	$1Y_0$	$2Y_0$	$3Y_1$
L	H	H	L	H	L	$1Y_0$	$2Y_1$	$3Y_0$
L	H	H	L	H	H	$1Y_0$	$2Y_1$	$3Y_1$
L	H	H	H	L	L	$1Y_1$	$2Y_0$	$3Y_0$
L	H	H	H	L	H	$1Y_1$	$2Y_0$	$3Y_1$
L	H	H	H	H	L	$1Y_1$	$2Y_1$	$3Y_0$
L	H	H	H	H	H	$1Y_1$	$2Y_1$	$3Y_1$
L	H	L	X	X	X	Last Channels "On"		
X	X	↓	X	X	X	Selected Channels Latched		

Typical Switching Characteristics (V_{CC} = 5V, GND = 0V, t_r = t_f = 6ns)

CHARACTERISTICS		CONDITIONS	15pF	50pF	UNITS
		V_{EE} (V)	54/74HC/HCT	54/74HC/HCT	
Propagation Delay Time Switch Input to Output	t_{PHL}, t_{PLH}	GND -5	3 2	5 4	ns
Switch Turn "ON" (R_L = 1k)	t_{PHL}, t_{PLH}	GND -5	14 14	17 17	
Switch Turn "OFF"	t_{PHL}, t_{PLH}	GND -5	17 14	19 17	

9-Bit x 64-Word FIFO Register; 3-State

CD54/74HC7030
CD54/74HCT7030



92CS-40537

TERMINAL ASSIGNMENT

Dynamic Electrical Characteristics @ T_A = 25° C, V_{CC} = 5 V, t_r, t_f = 6 ns

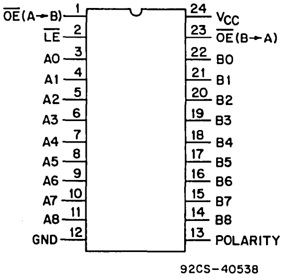
Symbol	Parameter	Test Conditions	Typical		Units
			HC	HCT	
t_{PHL}/t_{PLH}	Propagation Delay: SI, SO to DIR, DOR	C_L = 15 pF C_L = 50 pF	14 17	16 19	ns ns
f_{max}	Maximum Clock Frequency	C_L = 15 pF	40	40	MHz

CD54/74HC7038
CD54/74HCT7038

9-Bit Bus Transceiver with Latch

Features:

- 48 mA Sink Current
- Inverting and Non-Inverting Data Paths



TERMINAL ASSIGNMENT

TRUTH TABLE

CONTROL INPUTS			OPERATION
$\overline{OE}$(A→B)	$\overline{OE}$(B→A)	POLARITY	
L	H	H	D_n to $\overline{Q_n}$
L	H	L	$\overline{D_n}$ to $\overline{Q_n}$
H	L	H	B data to A
H	L	L	$\overline{B}$ data to A
H	H	X	Isolation

Dynamic Electrical Characteristics @ T_A = 25° C, V_{CC} = 4.5 V, t_r, t_f = 6 ns

Symbol	Parameter	Test Conditions	Typical		Units
			HC	HCT	
t_{PZL}/t_{PLZ}	A or $\overline{A}$ → B	C_L = 15 pF	23	23	ns
		C_L = 50 pF	26	26	ns
t_{PHL}/t_{PLH}	B or $\overline{B}$ → A	C_L = 15 pF	10	10	ns
		C_L = 50 pF	13	13	ns

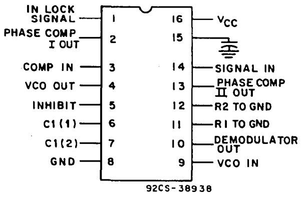
CD54/74HC7046
CD54/74HCT7046

Phase-Locked Loop with VCO and In-Lock Detector

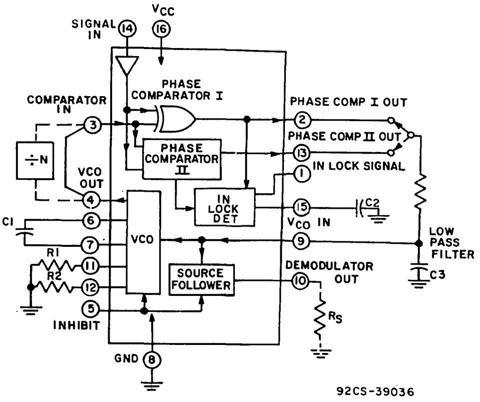
(Voltage Controlled Oscillator)

Feature:

- 11 MHz typ. @ V_{CC}=5 V (output signal)



TERMINAL ASSIGNMENT



Phase-locked loop with in-lock detector block diagram.

Advanced CMOS Logic

Advanced CMOS Logic, ACL, is the next step forward in the evolution of CMOS logic. It matches bipolar FAST* in speed, performance and logic type output drive, but at CMOS power levels.

Just as HC/HCT high-speed CMOS logic became an industry standard competing with LSTTL, ACL is expected to become an industry standard offered by a number of the leading CMOS logic suppliers. A JEDEC committee is currently working on specifications for a standardization of 54/74 AC/ACT devices.

Featuring < 3-ns gate propagation delays, ACL is the fastest CMOS logic yet available. (By contrast, the standard propagation delay for CMOS logic is 95 ns, and for high-speed CMOS logic, 9 ns.) ACL can operate at more than 150 MHz. Output drive capability is 24 mA, compared with 6 mA for HC/HCT. This capability enables ACL to drive transmission lines, yet still generate the voltages necessary to operate the receiving logic devices safely.

Because of its low power consumption, ACL is potentially more reliable than bipolar logic. This quality should make ACL the technology of choice in a number of applications, including computers, peripherals, and telecommunications, and in portable and military equipment.

*FAST is a trademark of Fairchild Semiconductor Corp.

ACL TYPES •		DESCRIPTION	PINS
PLASTIC *	CERDIP *		
CD74AC/ACT00E,M	CD54AC/ACT00F	Quad 2-Input NAND Gate	14
CD74AC/ACT02E,M	CD54AC/ACT02F	Quad 2-Input NOR Gate	14
CD74AC/ACT04E,M	CD54AC/ACT04F	Hex Inverter/Buffer	14
CD74AC/ACT05E,M	CD54AC/ACT05F	Hex Inverter/Buffer with Open-Drain Outputs	14
CD74AC/ACT08E,M	CD54AC/ACT08F	Quad 2-Input AND Gate	14
CD74AC/ACT10E,M	CD54AC/ACT10F	Triple 3-Input NAND Gate	14
CD74AC/ACT20E,M	CD54AC/ACT20F	Dual 4-Input NAND Gate	14
CD74AC/ACT32E,M	CD54AC/ACT32F	Quad 2-Input OR Gate	14
CD74AC/ACT74E,M	CD54AC/ACT74F	Dual D-Type Flip-Flop w/SET and RESET	14
CD74AC/ACT86E,M	CD54AC/ACT86F	Quad 2-Input EXCLUSIVE-OR Gate	14
CD74AC/ACT109E,M	CD54AC/ACT109F	Dual J-K Flip-Flop w/SET and RESET	16
CD74AC/ACT112E,M	CD54AC/ACT112F	Dual J-K Flip-Flop w/SET and RESET	16
CD74AC/ACT138E,M	CD54AC/ACT138F	3-to-8 Line Decoder/Demultiplexer, Inverting	16
CD74AC/ACT139E,M	CD54AC/ACT139F	Dual 2-of-4 Line Decoder/Demultiplexer	16
CD74AC/ACT151E,M	CD54AC/ACT151F	8-Input Multiplexer	16
CD74AC/ACT153E,M	CD54AC/ACT153F	Dual 4-Input Multiplexer	16
CD74AC/ACT157E,M	CD54AC/ACT157F	Quad 2-Input Multiplexer	16
CD74AC/ACT158E,M	CD54AC/ACT158F	Quad 2-Input Multiplexer, Inverting	16
CD74AC/ACT161E,M	CD54AC/ACT161F	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16
CD74AC/ACT163E,M	CD54AC/ACT163F	Synchronous 4-Bit Binary Counter, Synchronous Reset	16
CD74AC/ACT164E,M	CD54AC/ACT164F	8-Bit Serial-In Parallel-Out Shift Register	14
CD74AC/ACT174E,M	CD54AC/ACT174F	Hex D-Type Flip-Flop w/RESET	16
CD74AC/ACT175E,M	CD54AC/ACT175F	Quad D-Type Flip-Flop w/RESET	16
CD74AC/ACT191E,M	CD54AC/ACT191F	Synchronous 4-Bit Binary Up/Down Counter	16
CD74AC/ACT193E,M	CD54AC/ACT193F	Synchronous 4-Bit Binary Up/Down Counter	16
CD74AC/ACT238E,M	CD54AC/ACT238F	3-to-8 Line Decoder/Demultiplexer	16
CD74AC/ACT240E,M	CD54AC/ACT240F	Octal Buffer Line Driver, 3-State, Inverting	20
CD74AC/ACT241E,M	CD54AC/ACT241F	Octal Buffer Line Driver, 3-State	20
CD74AC/ACT244E,M	CD54AC/ACT244F	Octal Buffer Line Driver, 3-State	20
CD74AC/ACT245E,M	CD54AC/ACT245F	Octal Bus Transceiver, 3-State	20
CD74AC/ACT251E,M	CD54AC/ACT251F	8-Input Multiplexer, 3-State	16
CD74AC/ACT253E,M	CD54AC/ACT253F	Dual 4-Input Multiplexer, 3-State	16
CD74AC/ACT257E,M	CD54AC/ACT257F	Quad 2-Input Multiplexer, 3-State	16
CD74AC/ACT258E,M	CD54AC/ACT258F	Quad 2-Line to 4-Line Data Selector	16
CD74AC/ACT273E,M	CD54AC/ACT273F	Octal D-Type Flip-Flop w/RESET	20
CD74AC/ACT280E,M	CD54AC/ACT280F	8-Bit Odd/Even Parity Generator/Checker	14
CD74AC/ACT283E,M	CD54AC/ACT283F	4-Bit Full Adder w/Fast Carry	16
CD74AC/ACT299E,M	CD54AC/ACT299F	8-Bit Universal Shift Register, 3-State	20
CD74AC/ACT323E,M	CD54AC/ACT323F	8-Bit Universal Shift Register, 3-State (with Synchronous Reset)	20
CD74AC/ACT373E,M	CD54AC/ACT373F	Octal Transparent Latch, 3-State	20
CD74AC/ACT374E,M	CD54AC/ACT374F	Octal D-Type Flip-Flop, 3-State	20
CD74AC/ACT533E,M	CD54AC/ACT533F	Octal Transparent Latch, 3-State, Inverting	20
CD74AC/ACT534E,M	CD54AC/ACT534F	Octal D-Type Flip-Flop, 3-State, Inverting	20
CD74AC/ACT540E,M	CD54AC/ACT540F	Octal Buffer Line Driver, 3-State, Inverting	20
CD74AC/ACT541E,M	CD54AC/ACT541F	Octal Buffer Line Driver, 3-State	20
CD74AC/ACT573E,M	CD54AC/ACT573F	Octal Transparent Latch, 3-State	20
CD74AC/ACT574E,M	CD54AC/ACT574F	Octal D-Type Flip-Flop, 3-State	20
CD74AC/ACT646E,M	CD54AC/ACT646F	Octal Bus Transceiver/Register, 3-State	24
CD74AC/ACT648E,M	CD54AC/ACT648F	Octal Bus Transceiver/Register, 3-State, Inverting	24
CD74AC/ACT7060E,M	CD54AC/ACT7060F	14-Stage Counter with Oscillator	20
CD74AC/ACT7202E,M	CD54AC/ACT7202F	1024 x 9-Bit Parallel In-Out FIFO	28
CD74AC/ACT7402E,M	CD54AC/ACT7402F	65 x 5-Bit FIFO	18

• Consult your local Sales Office for availability time frame and other details.

*Package Suffix:
E - Dual-In-Line Plastic
F - Dual-In-Line Frit-Seal Ceramic
M - Surface Mount

Application Notes

Power Consumption in QMOS Logic Circuits

by R. Funk and B. Heinze

QMOS, RCA's high-speed CMOS-logic technology, offers users the best features of both CMOS and TTL technologies: the low-power consumption of CMOS and the fast speeds associated with LSTTL. This Application Note focuses on the primary QMOS feature, low power consumption. The causes of quiescent and dynamic power dissipation in HC and HCT QMOS devices are discussed. The formulas needed to compute the power dissipation in QMOS devices are presented along with sample calculations. A comparison is made of QMOS, LS, and ALS logic types relative to power dissipation.

The significant reduction in power consumption provided by a QMOS logic system compared with the equivalent LSTTL or ALSTTL counterpart design is *the* primary reason that QMOS is destined to be chosen for new designs and to replace LSTTL or ALSTTL parts in many existing designs. The replacement of LSTTL devices with HCT QMOS types[1] achieves power savings in existing designs where decreased power consumption and dissipation are a distinct advantage. In new designs, only QMOS logic lends itself to battery-operated portable equipment, such as portable (lap-held) personal computers, and the switch to QMOS is the major trend in PCs using all-CMOS RAMs, ROMs, and peripherals. All-QMOS designs can be powered down to 2-volts standby, increasing battery life. In nonportable designs, QMOS and CMOS LSI logic are also preferred to significantly reduce, in order of priority, cost, size, and weight. Cost reduction is the result of savings in the cost of supply regulators, the elimination of cooling fans and heat sinks, etc.

An equally powerful motivating force behind the use of logic components that dissipate lower power, such as QMOS, is the proven component and equipment reliability enhancement. The junction temperature of the ICs, as well as the temperature of other equipment components (resistors and capacitors), is much reduced, thereby lengthening life. QMOS failure rates are currently measured at .0015%/1000 hours at 60% UCL for operation at +55° C.

Power consumption in a logic IC must be considered in both of the IC's operating modes, i.e., under static and dynamic conditions. QMOS devices consume only minute amounts of power under static (quiescent) conditions, making power consumed in the dynamic state the major contributor to total power consumption. TTL devices, on the other hand, consume significant amounts of power in the quiescent state, so much in fact, that power consumption in the dynamic state can be masked at frequencies as high as 20 MHz, depending on device complexity. At higher frequencies, the power consumed by TTL devices increases proportionately. Since integrated circuits typically spend a significant percentage of their time either in the quiescent state or operating at average frequencies below 2 MHz, QMOS devices can provide significant and often dramatic power savings.

QUIESCENT POWER CONSUMPTION

The quiescent power consumption of a logic IC is measured when the system input voltage, V_{IN}, equals the device supply voltage, V_{CC}, or is at ground potential. Fig. 1(a) is used to illustrate this discussion. In the quiescent state, either the PMOS or NMOS transistor is fully off, and ideally no direct MOS transistor-channel path exists between V_{CC} and ground. In reality, however, thermally generated minority-charge carriers present in all reverse-biased diode junctions, Fig. 1(b), allow a very small power-supply leakage current to flow between V_{CC} and ground. In QMOS data sheets, this quiescent leakage current is specified as I_{CC}.

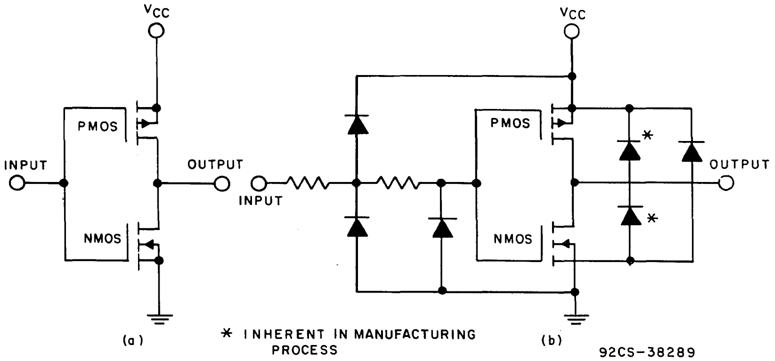


Fig. 1 - (a) Simple QMOS inverter circuit, (b) simple QMOS inverter circuit with input and output ESD protective diodes.

Three factors affect the value of I_{CC} and, therefore, the power dissipation of a device:

Temperature:-Increasing temperature causes an increase in I_{CC} because the minority charge carriers in the reverse-biased diode junctions of QMOS devices are thermally generated.

Device Complexity:-MSI devices will consume more power than SSI devices because there exists a proportionally greater reverse-biased diode-junction area.

V_{CC}:-The minority-charge carriers are linearly related to reverse junction voltage.

Table I shows the JEDEC industry standards for 54/74 HC/HCT high-speed CMOS devices, and illustrates the effect of temperature and device complexity on I_{CC} at the maximum recommended HC operating voltage, V_{CC} = 6 V. At V_{CC} = 2 V, I_{CC} is approximately 1/3 the value shown at V_{CC} = 6 V. Typical I_{CC} values are well under the maximum specified values.

Another factor that may add to quiescent, or dc, power consumption is the through current caused by both the PMOS and NMOS transistors of the input stage, Fig. 1(a), being on, at least to some degree, at the same time. For HC devices,[1] where the switching transition occurs at a nominal $V_{CC}/2$ (see Fig. 2(a)), there is no through current and, hence, no added dc power consumption. That is, with V_{IL} and V_{IH} voltage levels (low-level and high-level input voltages, respectively) at the inputs, either the PMOS or the NMOS transistor of the HC input stage is completely off. However, for HCT devices, where the switching transition occurs at a nominal 1.3 volts, Fig. 2(b), there is a through-current component when an input high-voltage level of under 4 volts is applied to an input. With this amount of voltage applied, the NMOS transistor is fully on and the PMOS transistor not fully off. This is the situation in an HCT device when, in a QMOS/TTL interface, the input voltage of the QMOS device is the V_{OH} (high-level output voltage) of a TTL family device. The 3.5-volt typical V_{OH} output voltage will fully turn-on the QMOS input NMOS transistor (Fig. 1) but not fully turn-off the PMOS transistor. The current flow that results is specified as ΔI_{CC} in QMOS HCT data sheets.

Computing HC Quiescent-Power Consumption

Quiescent power consumption in an HC device is extremely low, typically under 10 microwatts. The ΔI_{CC} plays no part because HC I/O levels are completely compatible: V_{OL} and V_{OH} worst-case specifications are 0.1 and V_{CC} - 0.1 volt, very close to ground and V_{CC}, respectively. Fig. 2(a) illustrates that no I_{CC} will flow with these V_{OL} and V_{OH} voltage levels imposed. However, if inputs are driven beyond V_{IL} and V_{IH} toward the switching voltage (centered typically at 2.3 volts), appreciable I_{CC} will flow. Such a high-current situation exists when an attempt is made to drive an HC input with a TTL output. For example, with a TTL V_{OH} level of 3 volts driving an HC input, not only would a logic error exist, but several milliamperes of I_{CC} would flow. To overcome this problem, an external pull-up resistor could be used, as shown in Fig. 3, but the resistor would cause significant additional system power consumption because it would have to be kept small in value in order to keep system speed high. RCA HCT QMOS devices are the preferred solution when interfacing CMOS with TTL logic.

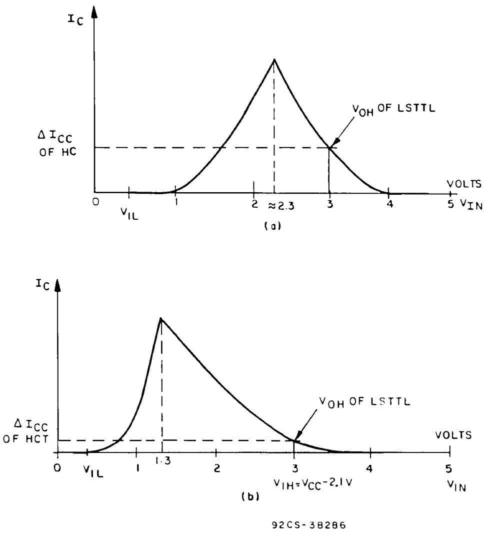


Fig. 2 - (a) HC input, CMOS interface, (b) HCT input, TTL interface.

In power-critical applications, such as portable battery-operated equipment or equipment operating in a battery-powered stand-by mode, HC quiescent power consumption may be a significant component of battery drain. The following formula is used to compute HC quiescent power consumption:

$$P_{dc} = V_{CC} I_{CC} \qquad (1)$$

where V_{CC} is dependent upon the particular application, and I_{CC} is obtained from the data sheet of the particular device for a V_{CC} of 6 volts (HC types). The data sheet value given is also valid within the nominal 5 V ± 10% supply-voltage range of HCT types. The value of I_{CC} at V_{CC} = 6 V can be linearly reduced for any desired V_{CC} voltage; e.g., at V_{CC} = 2 V, use 1/3 of the limits shown in Table I.

Table I - 54/74HC Family Characteristics

Symbol	Parameter	V_{CC}	Temperature (° C)						Units	Test Conditions
			54HC/74HC		74HC		54HC			
			25		-40 to 85		-55 to 125			
		(V)	Min.	Max.	Min.	Max.	Min.	Max.		
I_{CC}	Quiescent Supply Current									
	SSI	6	—	2	—	20	—	40	μA	V_I = V_{CC} or GND
	FF	6	—	4	—	40	—	80	μA	I_O = 0
	MSI	6	—	8	—	80	—	160	μA	

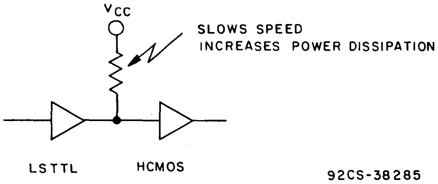


Fig. 3 - Use of pull-up resistor in LSTTL/HC interface.

Computing HCT Quiescent Power Consumption

Because HCT devices can be substituted for LSTTL devices and/or mixed with LS, ALS, AS, or FAST-TTL-family ICs in a system, their consumption of larger amounts of dc power than HC types is not significant. TTL worst-case output voltages are: V_{OL} = 0.4 V(max) and $V_{OH} = V_{CC} - 2.1$ V(min). The V_{OH} (or logic 1) voltages result in the ΔI_{CC} current flow illustrated in Fig. 2(b) and already described above. Note that only a logic-1 input causes appreciable quiescent leakage-current flow; a logic-0 input (0.4 V(max)) is close enough to ground to turn the NMOS transistor fully off. The total HCT-device quiescent power consumption is a function of the number of logic-1 inputs applied at the V_{IH} voltage level.

QMOS HCT data sheets specify ΔI_{CC} at the worst-case input voltage of $V_{CC} - 2.1$ V for V_{CC} ranging from 4.5 volts to 5.5 volts, with normalized limits as shown in Table II. ΔI_{CC} is further specified on a per-input-pin basis. This method of specification allows more accurate calculations if all the functions within a device are not being used or are being used at different input levels. For example, assume that two gates of an HCT10, a triple 3-input NAND Gate, are being driven by a TTL device with a 50% duty cycle. Given the information in Table II, quiescent power dissipation is calculated as follows:

$$P_{dc} = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\text{percent duty cycle high}) \quad (2)$$

where ΔI_{CC} is calculated on a unit-load basis as follows:

$$I_{CC} = (360\ \mu\text{A/unit load}) \times (0.6\ \text{unit loads/input pin}) \times (6\ \text{input pins}) \quad (3)$$
$$= 1.3\ \text{mA}$$

Therefore:

$$P_{dc} = (5\ \text{V})(2\ \mu\text{A}) + (1.3\ \text{mA}) \cong 6.5\ \text{mW}$$

Note that if all of the inputs of an HCT device are driven by HC or equivalent CMOS output levels, only equation (1) need be used to calculate its static power dissipation. Note also that if a 50% duty cycle is assumed for input signals, the average dc power is 3.25 milliwatts for the HCT type. This figure compares with 35 milliwatts for a 74LS10 IC, and shows that the HCT device still provides a big savings in power, even in the worst-case application.

DYNAMIC POWER CONSUMPTION

Three factors affect QMOS dynamic power consumption:

Load capacitance - dissipation of output state, Fig. 4.
Internal circuit capacitance
Switching transition currents (when complementary transistors used in switching are both momentarily on)

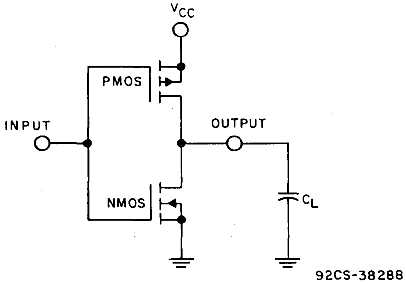


Fig. 4 - Simple QMOS inverter circuit driving a capacitive load.

For power calculation purposes, the load caused by internal device capacitance and switching transition currents is represented in one effective capacitance defined and specified as the C_{pd}, power dissipation capacitance, the effective internal device capacitance used for operating-

Table II - QMOS HC/HCT10 Static Electrical Characteristics and HCT Input Loading Table

Characteristic	CD74HC10/CD54HC10										CD74HCT10/CD54HCT10									Units
	Test Conditions			74HC/54HC Series			74HC Series		54HC Series		Test Conditions		74HCT/54HCT Series			74HCT Series		54HCT Series		
	V_I (V)	I_O (mA)	V_{CC} (V)	+25° C			-40/+85° C		-55/ +125° C		V_I	V_{CC}	+25° C			-40/+85° C		-55/ +125° C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Quiescent Device Device Current per input pin: 1 unit load ΔI_{CC}											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.4 mA.

HCT Input Loading Table

Input	Unit Loads*
All	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. at 25° C.

power calculations. Each of the above power-consuming factors, along with C_{pd}, are explained in further detail below.

Unlike quiescent power consumption, dynamic, or operating-power, consumption is computed in the same way for both HC and HCT devices. Therefore, throughout this section, all equations presented are applicable to both HC and HCT devices.

Internal Capacitance

Inherent in any active semiconductor is internal parasitic capacitance, i.e., capacitance present in diode junctions, MOS transistor structures, and metal and polysilicon interconnections. This internal capacitance produces the same effect on internal active circuits as external capacitive loads, and varies from one device to another depending on the complexity of the device.

QMOS devices are fabricated by means of a self-aligned polysilicon gate process (3-micron gate length) to reduce this internal capacitance. This process minimizes gate-to-source and gate-to-drain capacitances. Junction capacitances, which are proportional to the junction area, are also reduced because shallower diffusions are utilized.

Fig. 5 illustrates the device parasitic capacitance present in a CMOS inverter.

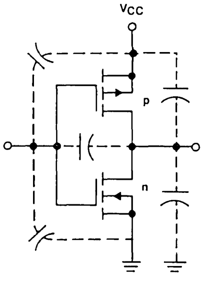


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Fig. 5 - Parasitic capacitances in a CMOS inverter.

Switching Transients

When the basic QMOS inverter circuit, Fig. 6(a), is switching states, either from a logic 1 to a logic 0 or vice-versa, both transistors will be on for a short period of time. This condition creates a momentary low-resistance path between V_{CC} and ground, Fig. 6(b). In this transient state, a momentary dc supply current flows and power is consumed. This low-resistance path is obviously a function of the number of transitions the device makes as well as the input-signal rise and fall time. In other words, power loss resulting from internal device switching is proportional to the input frequency (as is power loss due to internal capacitance).

Power-Dissipation Capacitance

Since power losses resulting from both net internal device capacitance and switching transient currents are frequency dependent, one term representing both factors is used for practical power-consumption calculations. This term is specified as C_{pd}, the no-load power dissipation capacitance.[2] C_{pd} is defined for each QMOS device in each data sheet. Further, it is specified per logic function, that is, for each gate or flip-flop within a device. This method allows for more accurate power consumption calculations when logic functions are operating at different frequencies.

Since C_{pd} encompasses both internal capacitance and switching loads, the internal device operating power per logic function is:

$$P_{pd} = C_{pd} V_{CC}^2 f \qquad (4)$$

where f is the operating frequency of the function.

COMPUTING HC AND HCT TOTAL POWER DISSIPATION

The formulas for total QMOS power dissipation are a combination of both static and dynamic power-consuming states. For HC devices:

$$P_{total} = V_{CC} I_{CC} + C_{pd} V_{CC}^2 f_{in} + C_L V_{CC}^2 f_{out} \qquad (5)$$

Total HCT power dissipation, when driven by TTL logic, is computed as follows:

$$P_{total} = V_{CC} I_{CC} + \Delta I_{CC} V_{CC} D + C_{pd} V_{CC}^2 f_{in} + C_L V_{CC}^2 f_{out} \qquad (6)$$

Where D = Percent duty cycle High

For HCT devices driven by HC devices, or at equivalent I/O voltage levels, equation (5) is used because the input voltage is essentially at V_{CC}, not at V_{CC} - 2.1 V.

QMOS VERSUS LS AND ALS POWER CONSUMPTION

In any integrated circuit, there exists a balance between speed and power consumption. LSTTL logic is relatively fast, but the bipolar circuitry used consumes considerable amounts of dc power. ALSTTL improves upon LSTTL by utilizing advanced finer-line geometry designs and ap-

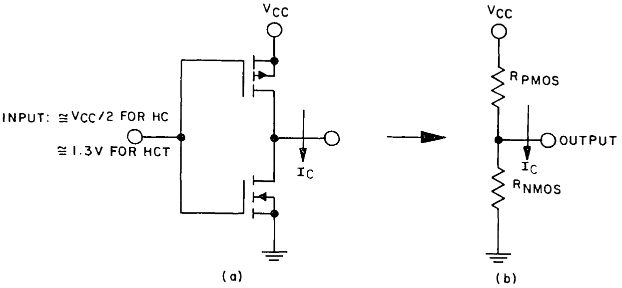

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Fig. 6 - (a) Simple QMOS inverter circuit, (b) equivalent schematic of a QMOS inverter whose transistors represent a low resistance path between V_{CC} and ground.

propriately finer fabrication techniques. These improvements both increase speed and decrease dc power consumption by about 50% total for both factors.

CMOS devices consume minute amounts of quiescent power compared to any given TTL bipolar-logic-family device. However, until the development of the QMOS line of logic devices, CMOS devices were relatively slow. Now, QMOS types, by utilizing finer-line design and fabrication techniques, not only consume the minute amounts of dc and operating power of a CMOS device (depending on operating frequency, as previously defined in equations (5) and (6)), but are fast, as described below.

A popular way to illustrate the differences between IC logic families and their technologies is shown in Fig. 7. In the figure, a 2-input NAND gate is used to illustrate the dc power consumption versus the typical propagation delay for a number of technologies.

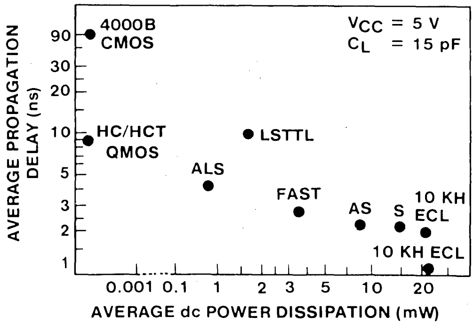

Fig. 7 - Speed/power spectrum for the popular logic technologies.

Table III is a compilation of speed/power products, in picojoules, for two CMOS-logic families and four TTL bipolar-logic families. In the table, SSI and MSI-complexity devices and those with complex flip-flop arrangements are used to illustrate speed/power differences. The major advantages of the new high-speed QMOS (HC/HCT) logic families are apparent:

- CMOS logic families have a 10^3 speed/power advantage over TTL logic families.
- Maximum dc power savings using CMOS are far greater for the more complex MSI logic functions. As shown, a TTLAS160 device consumes 5 x 10^3 times more dc power than an HC160.
- QMOS (HC) logic is approximately 10 times faster than equivalent CMOS devices; but retains the ultra-low dc power consumption of CMOS.

Fig. 8 illustrates the operating power consumption for SSI through MSI, QMOS, and LS devices. Note from the figures that CMOS devices realize their true power savings, from dc to several MHz, depending on device type and complexity. QMOS devices consume significant power only when switching, not when idling. TTL's continuous power consumption is the result of the many active bipolar transistors that must be continuously biased.

Fig. 8 also shows that as device complexity increases, the frequency at which CMOS and TTL devices consume the same amount of power increases, as would be expected.

Table III - Speed Power Comparison - Major TTL and CMOS Logic Families

Generic Type	Logic Family	Max. Prop. Delay[1] (ns)	Max. Power Dissipation[2] (mW)	Speed/Power Product[3] (pj)
Gate	**CMOS** HC00	18	.01	.18
	CD4011	250	.001	.25
	TTL ALS00	13	16.5	215
	LS00	15 (15 pF)	24	363
	AS00	4	95.7	283
	FAST00	5	51	255
FF	**CMOS** HC74	32	.022	.70
	CD4013	300	.006	1.8
	TTL ALS74	17	22	374
	LS74	40 (15 pF)	44	1760
	AS74	8.5	88	748
	FAST74	8	88	704
MSI Counters	**CMOS** HC160	35	.044	1.5
	CD40160	400	.028	11.2
	TTL ASL160	17	116	1964
	LS160	27 (15 pF)	176	4752
	AS160	6	220	1320
	FAST160	10	275	2750

1. V_{CC} = 5 V, C_L = 50 pF (15 pF for LS), T_A = 25° C, max. high or low state.
2. V_{CC} = 5.5 V - max. dc high or low output conditions.
3. Product of max. prop. delay and max. power dissipation.

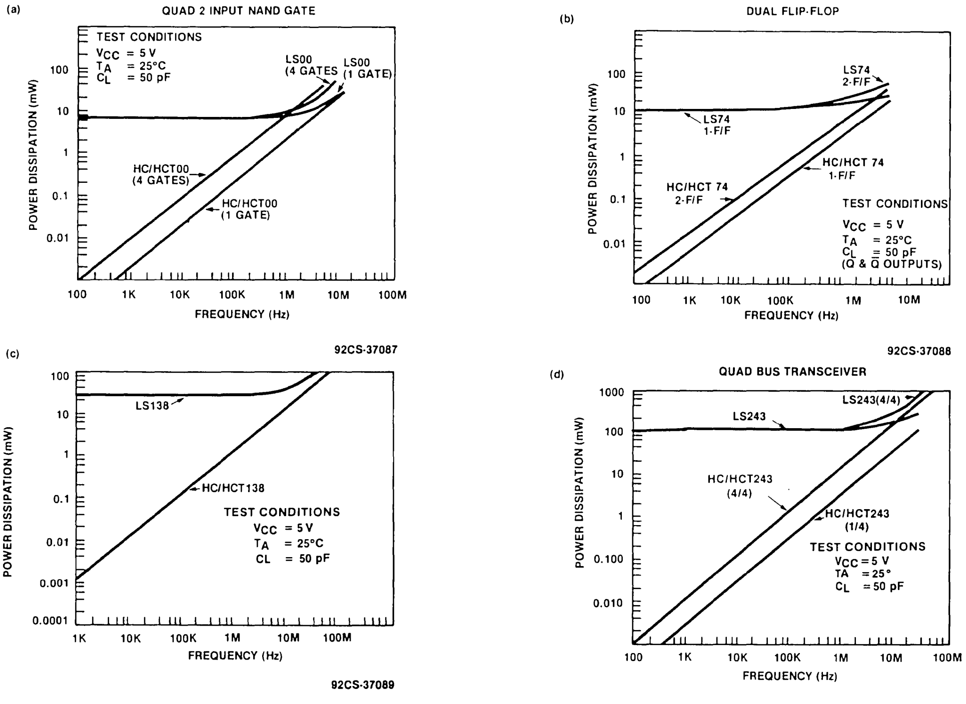

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Fig. 8 - Power versus supply graphs for the (a) LS/HC00, (b) LS/HC74, (c) LS/HCT138, and (d) LS/HC243.

QMOS devices also consume more quiescent power as device complexity increases, but the leakage currents that cause the power consumption are of such small magnitude that they can (in most cases) be ignored (see Table I).

The subject figures also illustrate the operating power differences for one function or n functions in an IC package operating at the frequencies shown.

The power-consumption characteristics of these different logic families are easily translated into total system power. Fig. 9 illustrates the power consumed by the different logic families in a small logic system (one gate and two flip-flops). The figure shows that QMOS substantially outperforms TTL in power consumption at both the device and the system level.

REFERENCES

1. The QMOS family consists mainly of two series, the HC, which features CMOS input-voltage-level compatibility, and the HCT, which features LSTTL input-voltage-level compatibility. For a review of these series, see **QMOS High-Speed CMOS Logic ICs**, RCA Solid State DATABOOK SSD-290.
2. See ref. 1 under "Description of QMOS Product Line" for discussion of C_{pd}.

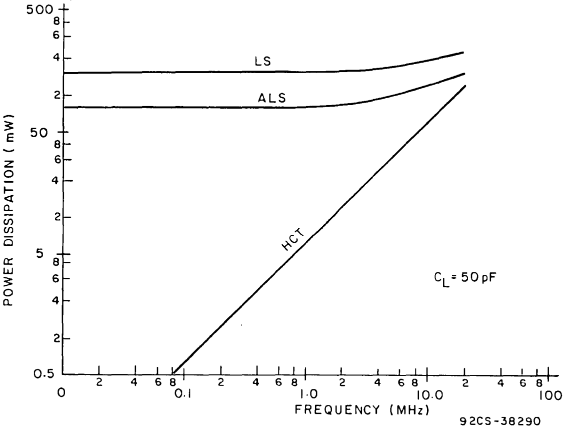


Fig. 9 - Power consumed by different logic families in a small logic system.

Modification of LSTTL Test Programs to Test HCT High-Speed-CMOS Logic ICs

by R. Funk

The QMOS HCT family of high-speed logic ICs is designed and specified not only to replace LSTTL devices having the same type numbers, but to interface with all TTL, CD4000B CMOS, and QMOS HC logic families. As such, it is indeed one of the more, and perhaps the most, interface-flexible logic family. In existing and new-equipment designs where LSTTL devices are, or could be, used, these devices are easily replaced by RCA's HCT logic family because of the several advantages its QMOS technology has over LSTTL:

- Much lower dc and operating-power requirements
- Improved dc noise margin
- Better balance in output current drive and switching speed
- Much lower input current and three-state output leakage current in high-impedance state
- Improved reliability because of lower junction temperature
- Wider 74-family operating temperature (-40°C to +85°C, not LSTTL's 0°C to 70°C)

But the switch from LSTTL to QMOS has made it necessary for test personnel to switch from the testing of LSTTL functions to the testing of the identical HCT functions; this Note has been written to make that switch as easy as possible. The widely used Teradyne J283 test system is used as a basic frame of reference in this Note; however, the test information given is applicable to most other test equipment and bench-test situations.

A few tests (depending on device tested) in the LSTTL test programs designed to test dc and function on the J283 system are invalid for use with HCT devices, and will consistently produce erroneous results. These tests are easily modified and made valid for QMOS general-logic types. A few additional tests require modification if bus drivers and transceivers are to be tested.

LSTTL TESTS REQUIRED TO BE MODIFIED FOR QMOS

Input Current at V_I = 7 V (Appendix I)

Unlike the LSTTL circuit shown in Fig. 1(a), HCT circuits incorporate an input protection network, as shown in Fig. 1(b). Because of this network, input current will flow if the input voltage exceeds V_{CC}. Therefore, when testing HCT types, change the input voltage from 7 volts to V_{CC}. To test for the exact HCT low-level input leakage current, modify the input-voltage setting according to the dc characteristics for 54/74HCT circuits given in Appendix II of this Note.

Input Clamp Voltage

The HCT input-protection network incorporates a series resistor that will cause the input clamp voltage (with an input current of -18 milliamperes) to be much lower than the -1.5 volts specified for LSTTL. Since the input clamp voltage is not specified for HC circuits, this test could be omitted, or changed to have a conservative limit of -5 volts. This limit assumes a 200-ohm poly-resistor at the input plus -1.5 volts of diode-to-ground potential.

Output Short-Circuit Current

As shown in Appendix I, an LS02 has an I_{OS} (short-circuit output current) of -20 to -100 milliamperes. Test one output at a time and do not exceed a one-second test-time duration. For QMOS, make the following current-limit changes:

Standard Logic Types: -20 mA to -70 mA
Bus Driver Types: -40 mA to -90 mA

Note that the I_{OS} test is nonstandard for QMOS HC or HCT types. The standard specified t_{TLH} and t_{THL} (transition times, low-to-high and high-to-low) values in QMOS specifications are a preferred method of directly measuring output speed. The I_{OS} limits are considered to be an indirect (and inaccurate) method of measuring the output sink and source speed characteristics for a given value of load capacitance.

Hysteresis (Bus Driver Types)

Many LSTTL bus-driver types undergo a ΔV_T test using a 0.2-volt-minimum hysteresis limit. For QMOS HC and HCT, change this minimum to zero volts or bypass this test.

Output-Voltage-Low Test Current (Bus-Driver Types)

LSTTL bus drivers have two specifications for V_{OL} (low-level output voltage) test current which must be modified as shown below for QMOS types:

	I_{OL}	
V_{OL} Maximum	**LSTTL**	**HC/HCT Modification**
0.4 V	12 mA	6 mA*
0.5 V	24 mA	8 mA

*Specified on QMOS data sheets

It appears from the table above that QMOS low-level output current is inferior to that of LS, i.e., 24 milliamperes versus only 8 milliamperes. However, the I_{OS} current and output t_{THL} of QMOS are similar to those of LS. The real significance of the 24 milliamperes is the ability of an LSTTL bus driver to directly drive a dc termination, as shown in Fig. 2(a). But

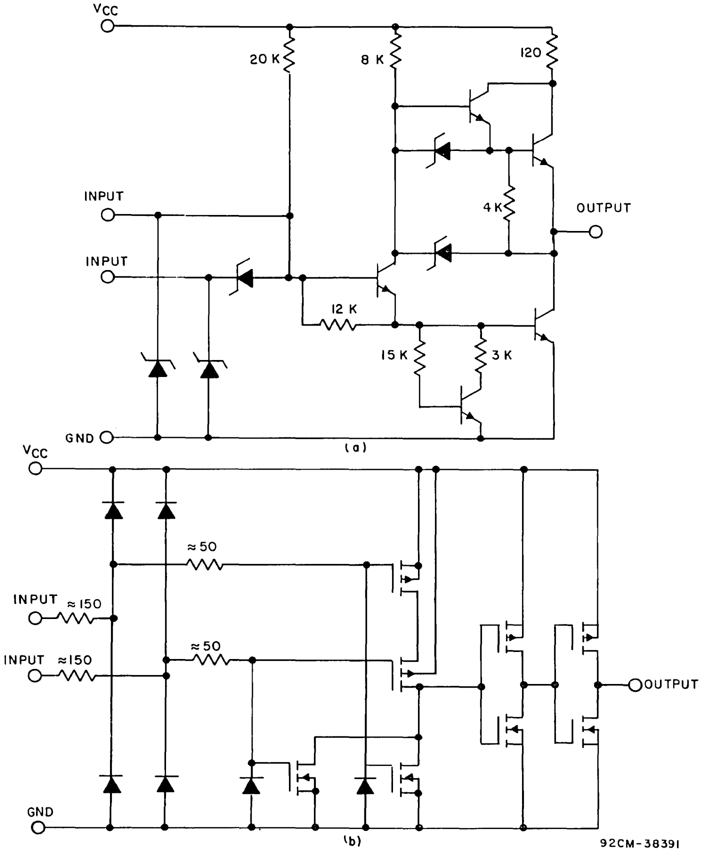


Fig. 1 - Comparison of LSTTL and HCT QMOS circuit structures: (a) two-input LSTTL NAND gate (1/4 54/74LS00), (b) two-input HCT QMOS NOR gate (1/4 CD54/74HCT02).

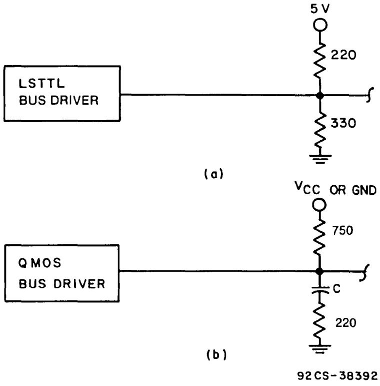


Fig. 2 - 100-ohm-line output termination: (a) LSTTL, 0.25 watt per output, (b) QMOS low-power alternative.

this ability represents a power dissipation of 0.25 watts per output section, and 2 watts per octal. For much lower power dissipation, use a QMOS type and a capacitively coupled 220-ohm resistor as shown in Fig. 2(b). The value of C in the figure depends on data rate.

Continuity Tests

Keep in mind that the QMOS input structure, Fig. 1(b), has a 150-ohm resistor in series with clamp diodes. Therefore, it is important to keep input current to ±20 milliamperes maximum during continuity testing. With this amount of current, the test voltage is ±5.5 volts maximum.

MORE COMPLETE TESTING OF HC OR HCT QMOS

To test HC or HCT QMOS ICs for low-power QMOS datasheet specifications, several tests other than those listed above may be modified. These modifications to existing LSTTL test limits or conditions are described below.

Quiescent Supply Current (Appendix II)

Setting supply current, I_{CC}, for the output-low condition test for HC circuits is no problem, but setting it for the output-high condition is more complicated. If the Teradyne J283 hardware has not been modified to handle CMOS, a comparator should be connected to each of the outputs of the HC circuit when it is placed under test. These comparators cause an extra load current of about 7 microamperes per output; the precise amount of current depends on the specific piece of test equipment. The extra load currents imposed are negligible compared with the I_{CC} of LSTTL circuits, and can be ignored when testing them.

However, these currents can be very significant compared with the total I_{CC} of an HC type, and must be taken into account when testing HC QMOS types. A solution to this problem is to connect the high outputs of the HC type to V_{CC} so that they are excluded from the I_{CC} measuring path. This connection can be made with the Teradyne J283 MTEST VCC1 A B C D, where A, B, C, and D are the outputs in the high state.

High-Impedance (Off-State) Current For Types Having Three-State Outputs

The high-impedance (off-state) LSTTL tests can be run for QMOS types, but only with much tighter limits, as shown below:

	LSTTL	QMOS
I_{OZ}	20 μA	5 μA

where I_{OZ} is three-state output off-state current.

Input Leakage Current (All QMOS Types)

Input-leakage-current LSTTL tests can also be run for QMOS devices but, again, with much tighter limits imposed, as shown below:

	LSTTL	QMOS
I_{IL}	-400 or -800 μA	-1 μA
I_{IH}	+20 μA or +40 μA	+1 μA

where I_{IL} is low-level input current and I_{IH} is high-level input current.

FUNCTION TESTING

QMOS and LSTTL types with the same type numbers have identical truth tables. High level (V_{OH}), low level (V_{OL}), and three-state (≈ 1.5 volts using LS load circuit) conditions are met when HCT devices are used in place of LS. If ac parameters are measured as part of function testing, LS speed limits are almost always met or improved upon.

Test personnel should be aware that actual ac specifications for HC and HCT QMOS logic ICs are much more realistic than for LS, as shown in the ac test-specification comparison in Table I. Therefore, anyone wishing to test ac parameters should use the specifications and waveform definitions found in the prime source of QMOS information, the QMOS DATABOOK.[1]

Table I - AC Test-Specification Comparison

Parameter	LSTTL	HCT QMOS
C_L	15/45 pF	50 pF
V_{CC}	5 V	4.5 V
Temperature	25° C	25° C, 74 (-40 to +85° C) 54 (-55 to +125° C)

REFERENCE

1. **QMOS High-Speed CMOS Logic ICs**, RCA Solid State DATABOOK SSD-290.

Appendix I - DC Characteristics for LSTTL Circuits

These figures are for positive-logic NAND gates and inverters with totem-pole outputs. For the characteristics of other types, refer to published data for LSTTL circuits.
Voltages are referenced to GND (ground = 0 V).

			54LS			74LS				
Parameter	V_{CC}	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating temperature	*	T_{amb}	-55	—	125	0	—	70	°C	
High-level input voltage	*	V_{IH}	2	—	—	2	—	—	V	
Low-level input voltage	*	V_{IL}	—	—	0.8	—	—	0.8	V	
Input clamp voltage	min.	V_{IK}	—	—	-1.5	—	—	-1.5	V	$I_I = -18$ mA
High-level output voltage	min.	V_{OH}	2.5	3.4	—	2.7	3.4	—	V	V_{IL} = max., $I_{OH} = -400$ μA
Low-level output voltage	min.	V_{OL}	—	0.25	0.4	—	—	0.4	V	V_{IH} = 2 V, I_{OL} = 4 mA
Low-level output voltage	min.	V_{OL}	—	—	—	—	0.25	0.5	V	V_{IH} = 2 V, I_{OL} = 8 mA
Input current at V_I = 7 V	max.	I_I	—	—	0.1	—	—	0.1	mA	
High-level input current	max.	I_{IH}	—	—	20	—	—	20	μA	V_{IH} = 2.7 V
Low-level input current	max.	I_{IL}	—	—	-0.4	—	—	-0.4	mA	V_{IL} = 0.4 V
Short-circuit output current	max.	I_{OS}	-20	—	-100	-20	—	-100	mA	

*Over V_{CC} range.

Notes:

For 54LS, V_{CC} = 4.5 V to 5.5 V; for 74LS, V_{CC} = 4.75 V to 5.25 V.
All typical values are at V_{CC} = 5 V, T_{amb} = 25° C.
For short-circuit output current, only one output must be shorted, and for not more than one second

Appendix II - DC Characteristics for the CD54/74HCT Family of Circuits

Voltages are referenced to GND (ground = 0 V)

T_{amb} (°C)

			CD54HCT/74HCT +25			CD74HCT -40 to +85		CD54HCT -55 to +125			Conditions	
Parameter	**V_{CC} (V)**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**V_I**	**Other**
High-level input voltage	4.5-5.5	V_{IH}	2	—	—	2	—	2	—	V		
Low-level input voltage	4.5-5.5	V_{IL}	—	—	0.8	—	0.8	—	0.8	V		
High-level output voltage all outputs	4.5	V_{OH}	4.4	4.5	—	4.4	—	4.4	—	V	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
High-level output voltage standard outputs	4.5	V_{OH}	3.98	—	—	3.84	—	3.7	—	V	V_{IH} or V_{IL}	$-I_O = 4$ mA
High-level output voltage bus-driver outputs	4.5	V_{OH}	3.98	—	—	3.84	—	3.7	—	V	V_{IH} or V_{IL}	$-I_O = 6$ mA
Low-level output voltage all outputs	4.5	V_{OL}	—	0	0.1	—	0.1	—	0.1	V	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
Low-level output voltage standard outputs	4.5	V_{OL}	—	—	0.26	—	0.33	—	0.4	V	V_{IH} or V_{IL}	$I_O = 4$ mA
Low-level output voltage bus-driver outputs	4.5	V_{OL}	—	—	0.26	—	0.33	—	0.4	V	V_{IH} or V_{IL}	$I_O = 6$ mA
Input leakage current	5.5	$\pm I_I$	—	—	0.1	—	1	—	1	μA	V_{IH} or V_{IL}	
Analog switch off-state current per channel	5.5	$\pm I_S$	—	—	0.1	—	1	—	1	μA	V_{IH} or V_{IL}	$V_S = V_{CC}$
3-state output off-state current	5.5	$\pm I_{OZ}$	—	—	0.5	—	5	—	10	μA	V_{IH} or V_{IL}	V_O*
Quiescent supply current												
SSI	5.5	I_{CC}	—	—	2	—	20	—	40	μA	V_{CC} or GND	$I_O = 0$
Flip-flops	5.5	I_{CC}	—	—	4	—	40	—	80	μA		$I_O = 0$
MSI	5.5	I_{CC}	—	—	8	—	80	—	160	μA		$I_O = 0$

*$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$.

Interfacing HC/HCT QMOS Logic with Other Families and Various Types of Loads

by R. Funk

The demand for smaller, lighter, electronic equipment that consumes little power is constant. And today's logic designers want these qualities matched by digital logic with high operating speeds. However, speed and power, while perhaps paramount in the initial choice of a logic family, are not the only basis for decision. Another very important factor is interface flexibility: the inherent capacity of a family to interface with other logic families and to drive various loads.

This Application Note describes the interface capability of the new high-speed CMOS CD54/74 HC/HCT logic families, probably the most interface-capable families yet devised. Fig. 1 illustrates the low dc power consumption and high speed of the HC/HCT families, both prime qualities for interfacing flexibility. Table I lists other important qualities. All of these characteristics, along with HC/HCT-family static and dynamic noise immunity, are discussed in this Note. The Note describes in detail HC/HCT interfaces with LSTTL, CMOS CD4000B-series, NMOS, and ECL devices, and interfaces with terminated buses, displays, and relay or stepping-motor coils, including interfaces with nonstandard output levels.

INTERFACE CONSIDERATIONS

Fig. 1 shows that the speeds of the HC, HCT, and LSTTL logic families are equivalent. In fact, the HCT family is a low-power replacement for the LSTTL family, and is interface compatible with *all* TTL families. The HC family is a low-power, high-noise-immunity alternative to the LSTTL family, and like the HCT family, will drive all TTL and CMOS families directly at various fanouts, depending on family.

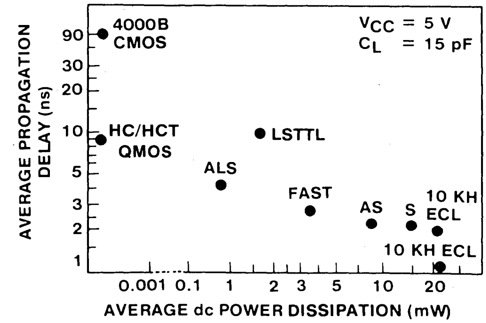


Fig. 1 - Logic-family speed-power chart.

Table II is a tabulation of interface techniques used between various popular logic families; the superiority of the HCT over the TTL family is evident. For example, the table shows there are 4 of 6 possible direct interfaces from HCT and only 2 of 6 for TTL.

CMOS and TTL Output Configurations

The typical output structure of an HC/HCT CMOS IC is shown in Fig. 2(a). When the output is high or low (V_{OH} or V_{OL}), its level is very close to V_{CC} or ground, respectively. In contrast, the high-level output voltage for the standard TTL

Table I - HC/HCT Family Characteristics

Characteristic	**HC**	**HCT**
Supply Voltage	2 V to 6 V	4.5 V to 5.5 V rated 2 V to 6 V capability
Temperature (74 family)	-40° C to +85° C	-40° C to +85° C
Input Switching Voltage		
For V_{CC}=5 V: Typical	2.5 V	1.4 V
Worst Case	1 V to 3.5 V	0.8 V to 2 V (same as TTL families)
Output Voltage:		
Driving other CMOS Logic	GND to V_{CC}	GND to V_{CC}
Driving TTL (V_{OL})	0.4 V (10-15 LSTTL loads)	0.4 V (10-15 LSTTL loads)
(V_{OH})	3.7 V	3.7 V
Typ. Output Transition for C_L = 50 pF	7 ns (balanced)	7 ns (balanced)
Input Current (typ.)	10 pA	10 pA

Table II - Interfacing HC/HCT QMOS to Other Logic Families

TO:	HC 5 V Supply	HCT 5 V Supply	CD5000B 5 V Supply	CD4000B 6-15 V Supply	TTL* 5 V Supply	ECL 10K
FROM:						
HC—5 V supply	direct	direct	direct	CD4504**	direct	10124
HCT—5 V supply	direct	direct	direct	CD4504**	direct	10124
CD4000B—5 V supply	direct	direct	direct	CD4504**	direct	10124
CD4000B 6-15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
TTL*—5 V supply	pull-up resistor	direct	pull-up resistor	CD4504**	direct	10124
ECL—10K/KH	10125	10125	10125	transistor	10124	direct

*Includes LS, S, STD, FAST, ALS, and AS.

**An alternative is a pull-up resistor and the CD40109 type.

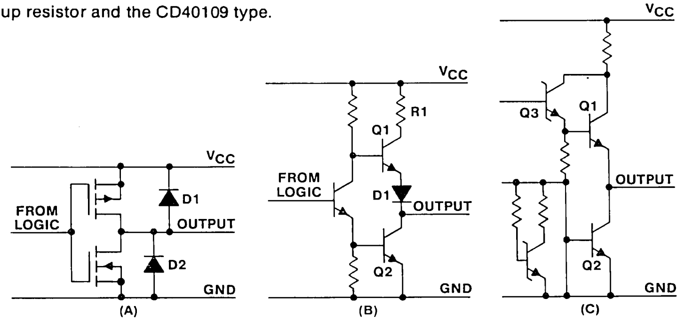


Fig. 2 - Typical output configurations of: (a) HC/HCT devices - D1 and D2 are the inherent diodes of the p-drain and the n-drain, respectively, (b) standard TTL, and (c) low-power Schottky TTL (LSTTL).

circuit shown in Fig. 2(b) is limited by the V_{BE} of Q1 plus the voltage drop across D1, resulting in a maximum V_{OH} of 3.5 volts at a V_{CC} of 5 volts. Further, if a collector current is flowing, R1 will cause an additional voltage drop, and the worst-case V_{OH} minimum specified for TTL, 2.4 volts (at I_{OH} maximum) over the full temperature and power supply range, may be realized. The low-level output voltage for TTL is the collector/emitter saturation voltage of Q2, and V_{OL} will range from 0.2 volt to 0.5 volt maximum depending on the fanout and, hence, total sink current.

In the output structure for the LSTTL device of Fig. 2(c), V_{OH} is limited by the V_{BE} of both Q1 and Q3 (the diode is not considered a part of the LSTTL output structure) and is typically 3.4 volts. LSTTL specifications quote V_{OH}(min) as 2.7 volts over the full temperature range with a V_{CC}(min) of 4.75 volts. The maximum value of V_{OL} for LSTTL can, again, range from 0.2 to 0.5 volt depending on application and temperature conditions.

CMOS Input Structures

The input structure for HC/HCT devices is shown in Fig. 3(a). Under normal operating conditions, the input voltage should swing within the supply voltage limits of V_{CC} and ground, since exceeding these limits can cause a current to flow through the input protection diodes, D1 and D2. The maximum transient current permitted through these diodes is 20 milliamperes; if this limit is exceeded, the functionality of the circuit could be impaired. As the MOS transistors Q1 and Q2 are electrically identical, the typical input switching voltage of the HC device is $V_{CC}/2$.

The input configuration for HCT devices is similar to that for HC circuits, but with the addition of a level-shifting diode, D3, between PMOS transistor Q1 and V_{CC}. This configuration is shown in Fig. 3(b). The effect of D3, combined with the large NMOS transistor Q2, which has a higher gain than PMOS transistor Q1, is to reduce the input switching level to, typically, 1.4 volts.

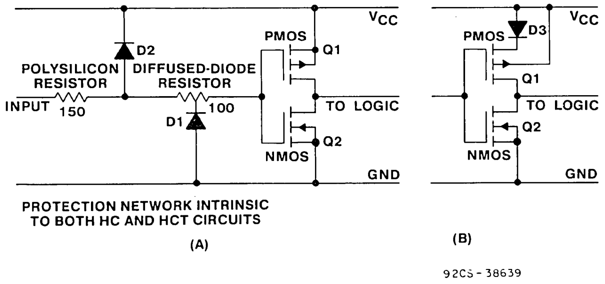


Fig. 3 - Typical input structures of: (a) HC devices, and (b) HCT devices.

The advantage of diode D3 is that it reduces power dissipation when a high input from a TTL output is applied. This high level can be as low as 2.4 volts, and although it will be recognized as a logic 1, the PMOS transistor Q1 will not be fully cut off, allowing a flowthrough current between V_{CC} and ground. However, D3, and the influence of the back-gate (substrate) connection of Q1 to V_{CC}, dramatically reduces the flowthrough current and, therefore, reduces the power dissipation in the input stage while maintaining device input switching levels compatible with LSTTL.

HC/HCT INTERFACES

When HCT and LSTTL devices operate from the same supply, the quiescent flowthrough current, I_C, at V_{IH} = 2.4 V and V_{CC} = 4.5 V is typically only 100 microamperes. This means that the HCT input structure provides low CMOS-type power dissipation, even when driven from TTL. If V_{CC} is increased to 5.5 volts, the minimum high-level output voltage also rises 1 volt to 3.4 volts.

When interfacing LSTTL with HC/HCT devices in a dual-supply-voltage system, the following worst-case conditions apply:

V_{OH}(min) for TTL = 2.4 V
V_{OH}(min) for LSTTL = 2.7 V

and

V_{IH}(min) for HC devices = 3.85 V (70% of V_{CC})
V_{IH}(min) for HCT devices = 2 V

where V_{CC} = 4.75 V for TTL and 5.5 V for HC devices over the full operating temperature range.

It is clear from the above figures that the worst-case TTL high-level output voltage is less than the minimum high-level input voltage for HC devices, and that some special interface technique is required. A solution is provided in the circuit in Fig. 4(a), where pull-up resistor R1 pulls the output voltage of the LSTTL against V_{CC}. However, this technique is not recommended because the time-constant formed by the pull-up resistor and the stray capacitance (C_S), plus the load capacitance (C_L), will increase the propagation delay. Furthermore, with this set-up, the propagation time is less predictable because it relies on both active and passive RC time-constants.

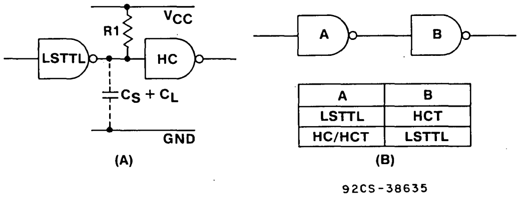


Fig. 4 - Techniques for interfacing: (a) LSTTL with HC devices, and (b) LSTTL with HCT devices, and HC/HCT with LSTTL devices.

Although a low value for R1 will reduce the propagation delay, it will lead to extra power consumption and reduce the noise-margin-low (discussed further below under Noise Immunity) due to the active load. Both of these unwanted occurrences conflict with the purpose of using HC family devices. In addition, the pull-up resistor requires board space and insertion time, thus increasing production costs. Therefore, the pull-up resistor interface should be used only if unavoidable. The practical solution is to use HCT devices (all types in the CD54/74 family are available in both HC and HCT versions), which interface directly with LSTTL, as shown in Fig. 4(b).

Driving LSTTL

Since the output of HC devices swings between V_{CC} and ground, they are TTL-input compatible, and the interface is a direct connection, Fig. 4(b).

When an HCT device is the driving source for an LSTTL device, the speed can be accurately predicted because the LSTTL logic-switching threshold of 1.3 volts is the same as that for HCT ICs. For HC driving sources, the speed difference introduced by the HC logic switching threshold of, typically, $V_{CC}/2$ can be calculated from the specified output transition times (obtained from the appropriate Data Sheets).

Table III gives the driving capability (fanout) of HC/HCT devices for the various TTL families.

Table III - Maximum Fanout for HC/HCT Driving TTL

Receiving Input	Standard Output	Bus-Driver Output
TTL	2	3
LSTTL	10	15
STTL	2	3
FAST	6	10

CD4000 B-Series CMOS

HC/HCT devices can be coupled directly to standard CD4000B-series CMOS ICs if they operate from the same supply voltage. However, if the circuits have different supply voltages, level shifting is necessary. The configuration shown in Fig. 5(a) illustrates the circuit for HC/HCT to CD4000B interfaces using the CD4504 low-to-high level shifter. Note that this IC is capable of interfacing either TTL output logic levels or CMOS logic levels to a higher output-voltage level. The reader is reminded that the CD4000B CMOS logic family may be operated up to 18 volts; the HC/HCT family operates at up to a 6-volt supply-voltage level, but also down as low as 2 volts.

Fig. 5(b) shows how to interface the CD4000B series with HC/HCT ICs using the CD4049/4050B or HC4049/4050 buffer ICs. These buffers do not have an input clamping diode to V_{CC}, so that the maximum input level is 15 volts. The logic-level switching threshold remains referenced to V_{CC2}; therefore, the noise-margin-low will be the same as for the 5-volt specification.

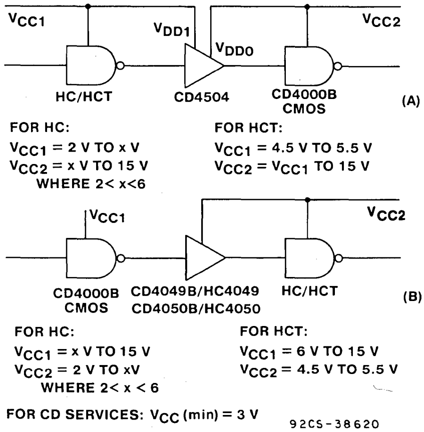


Fig. 5 - Techniques for interfacing: (a) HC/HCT devices with CD4000B series CMOS, and (b) CD4000B series CMOS with HC/HCT devices.

NMOS

The rules for interfacing TTL apply when interfacing HC/HCT devices with NMOS devices (microprocessors, memories, etc.) since NMOS ICs generally have TTL-compatible inputs and outputs. Exceptions are NMOS ICs with open-drain outputs, where a pull-up resistor must be used to load the output. The HCT device inputs directly accept active NMOS output-voltage levels.

ECL 10K

To interface HC/HCT ICs with ECL 10K-series logic, the 10124 TTL-to-ECL and the 10125 ECL-to-TTL translator ICs (for HC/HCT-to-ECL and ECL-to-HC/HCT interfaces, respectively) are used. Note that these devices operate at TTL levels. When employing the 10125 for interfacing HC circuits, the pull-up resistor, R1, must be used in accordance with the instructions for driving HC devices from TTL. The circuit configurations are shown in Figs. 6(a) and 6(b). Note that if an HCT device is used in the ECL interface (the definite preference) the pull-up resistor of Fig. 6(a) is eliminated.

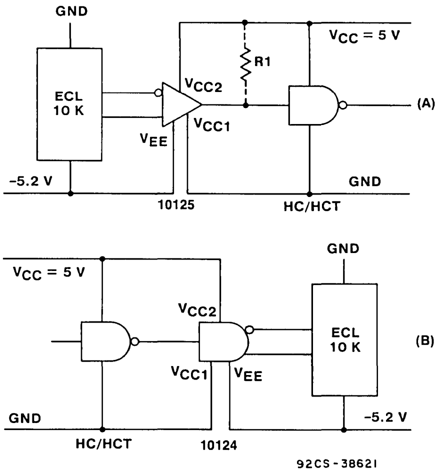


Fig. 6 - Techniques for interfacing: (a) ECL 10K logic with HC/HCT circuits - R1 is only required when driving HC types, and (b) HC/HCT devices with ECL 10K logic.

Terminated Buses

Buses are used chiefly in industrial applications. The harsh environments found in these applications impose several requirements on microprocessor-based systems; electrical-noise immunity and the need for battery back-up are two examples. The CMOS technology provides the ideal solution to these requirements. The HC CMOS devices offer superior noise immunity, similar operating speed, and lower power dissipation over a wider temperature and supply-voltage range in comparison with LSTTL ICs. The noise immunity in the low logic state is the same for HCT devices as for LSTTL.

The development of a new bus standard for CMOS systems should be based on the performance of the devices available with bus-driver outputs, for example, the CD54/74HC245 transceiver. Figs. 7(a) and 7(b) show examples of conventional TTL and HC/HCT bus terminations, respectively.

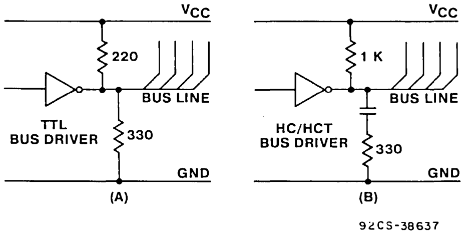


Fig. 7 - Examples of bus terminations used in: (a) conventional bipolar (TTL) technologies and (b) HC/HCT systems.

The particular disadvantage to the theveninized 120-ohm termination of Fig. 7(a), the conventional TTL bus termination, is the 0.25 watt dissipated continuously by the combination of the output driver and the 120-ohm load. This dissipation represents 2 watts for an octal buffer.

The HC/HCT-family bus drivers have a 6-milliampere sink current, not the 12 milliamperes of LSTTL, and are not designed to directly drive the 120-ohm load of Fig. 7(a) for two reasons: first, 2 watts dissipation does not represent a low-power solution, and second, HC/HCT outputs could be designed to match the very high 2-watt-dissipation application of Fig. 7(a), but would also generate much higher switching-current transients, which would push up EMI to inappropriately high levels. Therefore, the interface of Fig. 7(b) is preferred for its much lower power consumption and lower EMI. The value of C in Fig. 7(b) is carefully selected for the range of frequencies (data rates) on the bus.

HC/HCT devices do not generally have input hysteresis, so that Schmitt-trigger circuits should be used if slow, noisy bus rise and fall voltages call for hysteresis in the receiver. The CD54/74HC/HCT14 and 132 are two ICs that can be used for noise-tolerant systems. Five devices in the flip-flop series (CD54/74HC/HCT73, 74, 107, 109, and 112) also have Schmitt triggers in the clock input. Note that HC devices are preferred over HCT devices as bus receivers because of their high low-level-input noise margin (typically 2 volts).

Nonstandard Levels

In many applications, CD54/74 high-speed CMOS ICs will have to interface with nonstandard input and output levels, for example, with industrial or automotive systems operating from a 12 to 24-volt supply. The circuits in Figs. 8(a) and 8(b) show the basic design rules for these interfaces. Fig. 8(c) illustrates an example of a user-edge input circuit for interfacing with input levels greater than V_{CC}. The configuration for HC/HCT devices driving loads from an external power supply is given in Fig. 9(a). Figs. 9(b) and 9(c) show HC/HCT devices driving loads (for example, a relay) on the same supply voltage.

Fig. 10(a) is an interesting low-cost but also lower-speed high-to-low interface: 12 to 5-volt logic levels using only 100-kilohm resistors in series with each input. Fig. 10(b) shows why this interface is reliable with good noise margins; RCA HC/HCT designs guarantee that forced input current into V_{CC} will result in less than 0.05 of this current flowing into ground. In Fig. 10(b), V_{IL} at B is less than 0.34 volt, well under the specified V_{IL} of 1-volt maximum. Other high-to-low voltage-interface combinations with different resistor values may be determined with knowledge of the 0.05 value of current gain (α) between adjacent inputs.

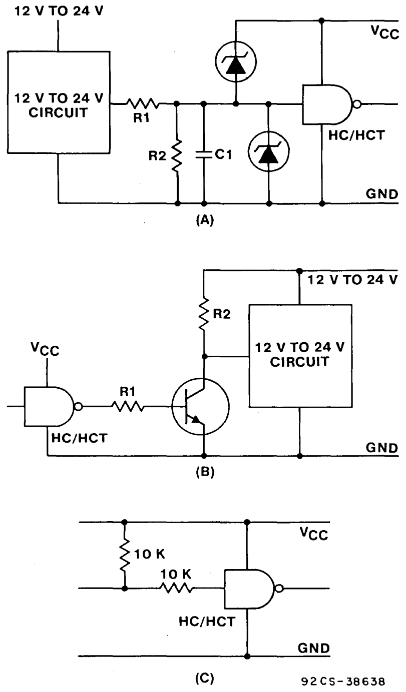


Fig. 8 - Technique for interfacing: (a) nonstandard logic levels with HC/HCT circuits - values of R1 and R2 depend on the output voltage of the driving circuit and C1 depends on the noise and speed, (b) HC/HCT devices with nonstandard logic levels - values of R1 and R2 depend on supply voltage and transistor type, and (c) a user-edge input circuit configuration for interfacing with input voltages greater than V_{CC}.

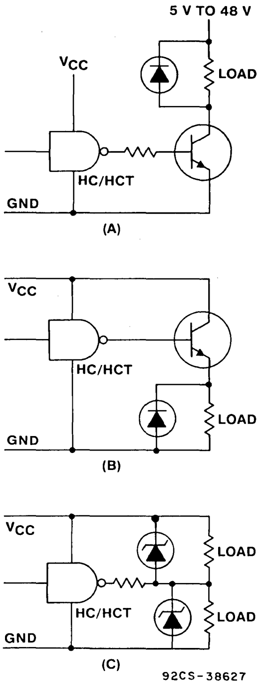


Fig. 9 - Interfacing loaded HC/HCT devices: (a) an external power supply via a transistor, (b) the same power supply via a transistor, (c) the interfacing of HC/HCT directly with loads on the same power supply.

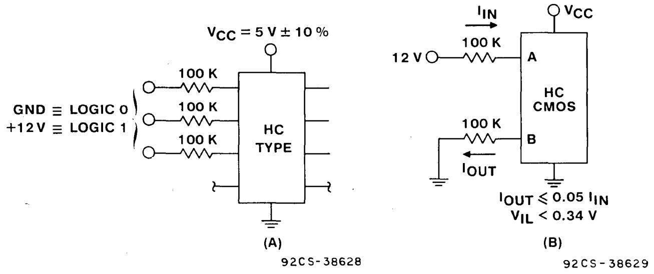


Fig. 10 - Low-cost, low-speed 12-volt-logic to 5-volt-logic interfaces.

The typical value of alpha (α) for the bipolar parasitic input transistor is 0.001. The low value of alpha is an important feature of the RCA HC/HCT family because it eliminates transient logic errors in the presence of transient voltages exceeding V_{CC} at any input.

Displays

The CMOS technology, with its rail-to-rail output switching, is just as ideal for HC/HCT family devices driving LCD displays as it has been for CD4000B-series devices. Fig. 11(a) illustrates the basic BCD-to-7-segment LCD interface (HC/HCT4543) plus the single-segment LCD interface using the HC/HCT 86 type. The popular 4511 type is carried into the HC/HCT family for the basic LED BCD-to-7-segment interface, as illustrated in Fig. 11(b).

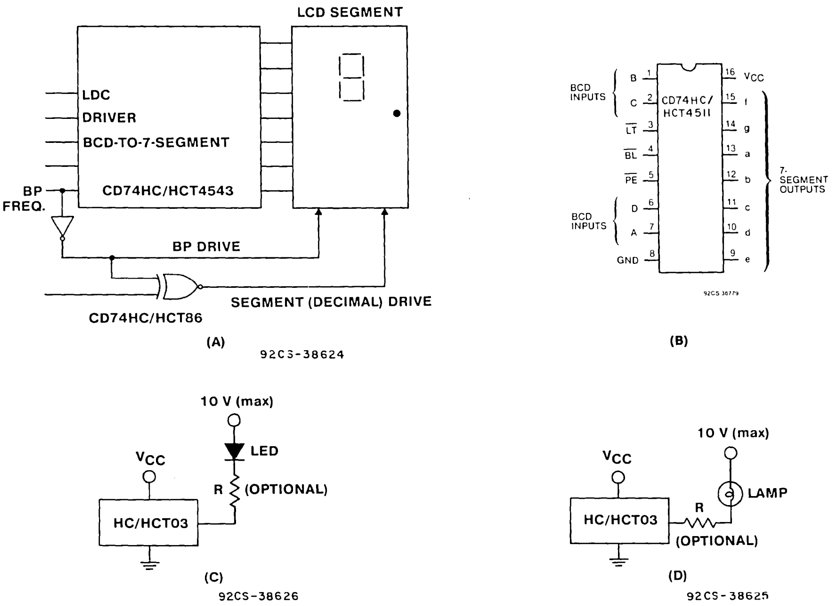


Fig. 11 - Display interfacing: (a) LCD, (b) and (c) LED, (d) lamp.

For single-segment LED interface, the open drain 74HC/HCT03 type is ideal, Fig. 11(c). Since the 03 type does not have an output-to-V_{CC} forward diode in its output circuit, the LED may be supplied by up to 10 volts. R may be useful in limiting current and reducing power. This same 03 type can also be used for driving an indicator lamp, as shown in Fig. 11(d).

Relay or Stepping Motor Coils

Another application of the open drain HC/HCT03 type is the relay or stepping motor interface shown in Fig. 12. The external diode across the coil absorbs the back emf of the coil.

L^2 MOSFET Power Transistor

RCA logic level (L^2) MOS power transistors, Fig. 13, are ideally driven by any HC/HCT output. Higher switching speeds, 200 nanoseconds, are achieved using the bus-drive output types. HC/HCT outputs will reliably switch these new L^2 MOS power devices using only a 5-volt supply for V_{CC}; this is truly a breakthrough in power-transistor-interface applications cost.

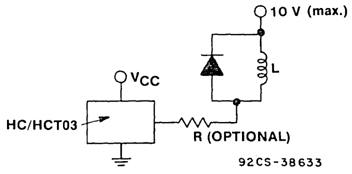


Fig. 12 - Coil driver.

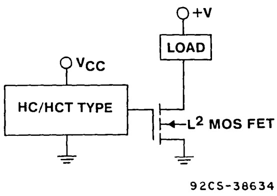


Fig. 13 - L^2 MOSFET power-transistor drive.

NOISE IMMUNITY IN THE HC/HCT FAMILY

General

The noise-immunity characteristics of logic devices can be divided into two categories, static and dynamic. Static noise immunity can be divided further into static noise-immunity-low, the difference between the V_{IL}(max) of the receiving circuit and the V_{OL}(max) from the driving current, and static noise-immunity-high, the difference between the V_{OH}(min) from the driving circuit and the V_{IH}(min) of the receiving circuit.

The guaranteed static noise-immunity characteristics for LSTTL and HC/HCT devices are shown in Table IV. If the static noise margins for LSTTL are assumed to be unity, (for both the high and low states), a direct comparison of LSTTL and HC/HCT static noise margins can be made by taking the ratio shown in Table V. These results are particularly impressive when the extended ambient temperature range and the lower supply voltage of the HC/HCT family is considered.

Table IV - Static Noise Margins for LSTTL at V_{CC}=4.75 V and HC/HCT Systems at V_{CC}=4.5 V

	LSTTL	HC	HCT
V_{OH}(min)	2.7 V	4.4 V	4.4
V_{IH}(min)	2 V	3.15 V	2
Noise-Margin-High	0.7 V	1.25 V	2.4 V
V_{IL}(max)	0.8 V	0.9 V	0.8 V
V_{OL}(max)	0.4 V	0.1 V	0.1 V
Noise-Margin-Low	0.4 V	0.8 V	0.7 V

Table V - Ratio of Static Noise Margins, LSTTL to HC/HCT

	LSTTL	HC	HCT
Noise-Margin-High	1	1.75	3.4
Noise-Margin-Low	1	2	1.75
Ambient Temperature Range (T_{amb})	0 to +70°C	-40 to +85°C	-40 to +85°C
Supply Voltage (V_{CC})	4.75 V	4.5 V	4.5 V

The graph in Fig. 14(a) compares the static noise margins for HC devices with those for LSTTL. The graph illustrates that while HC circuits can drive LSTTL (as V_{OH}(min) for an HC device is greater than V_{IH}(min) for an LSTTL device), the converse is not true (since V_{OH}(min) for LSTTL is less than V_{OH}(min) for HC; there is no overlap in the noise-margin-high regions). Therefore, the noise-margin-high for LSTTL driving HC devices is said to be negative, which explains the reason for the problematical external pull-up resistor interface described in Fig. 4(a).

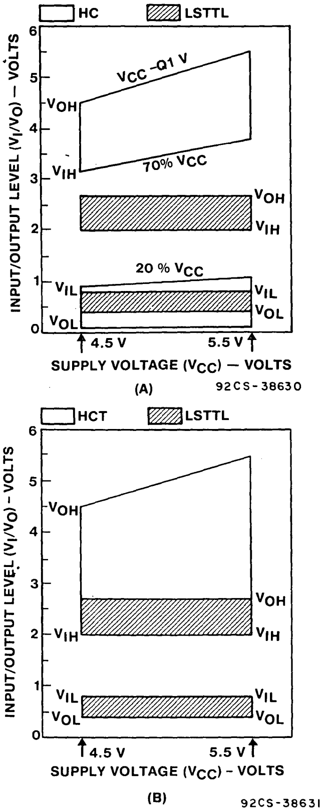


Fig. 14 - Static noise margins for: (a) HC devices compared with LSTTL, and (b) HCT devices compared with LSTTL in a mixed technology system.

In a mixed-technology system with fully loaded HCT outputs driving LSTTL inputs, the static noise-margin-low is equal for both families, and the HCT devices exhibit an excellent static noise-margin-high that encompasses that displayed by LSTTL. This situation is illustrated by the graph in Fig. 14(b), which shows that HCT and LSTTL devices are fully interchangeable in a mixed-technology system.

Dynamic noise immunity

Dynamic noise immunity for HC/HCT circuits also falls into two categories, high and low. The dynamic noise-margin-low is, again, the smaller of the two, and is, therefore, the parameter considered here.

To plot the dynamic noise-margin-low for HC/HCT devices, a pulse of known magnitude, V_P, is applied to the input of a device; its width, t_W, is then increased until the device just begins to switch. The input level on which V_P is based is equal to the switching voltage minus the worst-case static noise-margin-low. Pulse width, t_W, is measured at half pulse height, $V_P/2$, and the rise and fall times, t_r and t_f, are 0.6 nanosecond. V_P is reduced in increments and the t_W for each new value ascertained. The test is repeated over a series of varying supply voltages (V_{CC} between 2 and 6 volts for HC and at 5 volts for HCT) and output currents, I_O.

The resulting graphs in Figs. 15(a) and 15(b) illustrate the

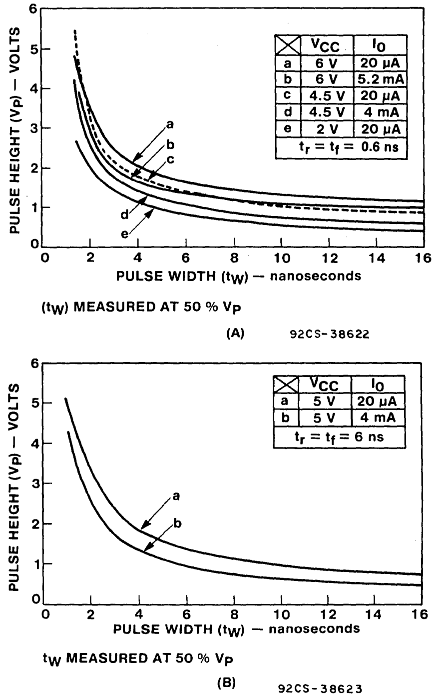


Fig. 15 - Dynamic noise immunity characteristics (worst-case, fully loaded driver) for: (a) HC devices and (b) HCT devices.

dynamic noise immunity characteristics of HC and HCT circuits, respectively. Note that an increase in I_O lowers the curve and reduces the dynamic noise immunity. As these curves illustrate for the worst-case conditions with fully loaded HC/HCT devices, a system using only HC or HCT circuits will demonstrate an increase in dynamic noise immunity, shifting the curves up 0.3 volt.

Derived from the typical input switching threshold levels of 1.3 and 2.5 volts for HC and HCT, respectively, the noise immunity characteristics will show a typical improvement of 0.8 volt in HCT systems and 1.2 volts in HC systems.

Power-Supply Distribution and Decoupling For QMOS High-Speed-Logic ICs

by R. Funk

The HC and HCT high-speed QMOS IC logic families available from RCA offer the user many advantages over TTL logic families. These advantages include much lower power consumption, better noise margin (mainly in the HC devices), wider operating-voltage range, wider operating-temperature range, lower input current, lower three-state current, superior high-to-low and low-to-high output transition time and propagation delay balance, and better reliability. However, HC/HCT CMOS does share one common liability with LSTTL: switching transients generated on the ground and supply rails can dangerously reduce logic noise margin if not compensated.

Higher speeds, faster edges, and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC. The familiar L di/dt voltage transient is developed, its value depending on the inductance in the ground or V_{CC} connection from chip to IC lead. For octal bus-driver types, one volt of L di/dt is possible depending on inductance, device decoupling, and power-supply decoupling. This Note focuses on power-supply distribution and decoupling to reduce switching noise. One source of this noise, an important system factor relative to IC switching, is rf radiated noise, noise that can interfere with communications in the local area. Some general ways to reduce L di/dt rf noise, i.e., voltage generation on ground and supply lines, are described below.

POWER DISTRIBUTION

Before decoupling can provide any noise reduction, there must first be a good power-distribution network. A good ground connection is vital, and so a good connection pattern is required.

The commonly accepted ground pattern shown in Fig. 1 can cause problems. In the figure, an output from device 1 drives an input to device 2, and an output from device 3 drives an input to device 4. Since the signal path 1 to 2 and 3 to 4 are not coupled, there should be no crosstalk. However, devices 1 and 3 share the crosshatched part of the ground line, as shown, and switching of the output of device 1 could produce a spike on the ground of device 3, causing the input to device 4 to switch. It is, therefore, advisable to reduce the single ground path on a double-sided board by using links, as shown in Fig. 2. This advice is especially true for boards where high currents are switched. Avoid using jumpers like the one shown in Fig. 3 for ground and power line (V_{CC}) connections. Jumpers are unlikely to be used in production printed-circuit boards, but they should also be avoided on prototype and single boards because the inductance they introduce into the lines permits coupling between outputs. Printed-circuit boards equipped with premanufactured ground connections or copper strips to connect the pins to ground should be used.

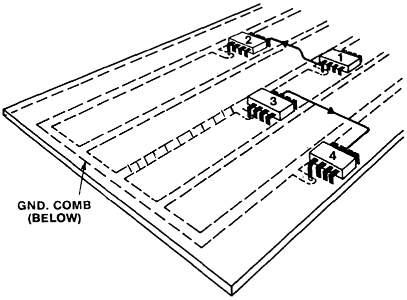


Fig. 1 - Common ground path on two-sided board.

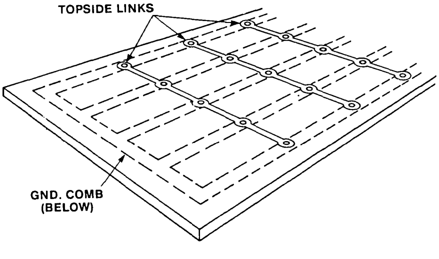


Fig. 2 - Reducing ground paths on two-sided board.

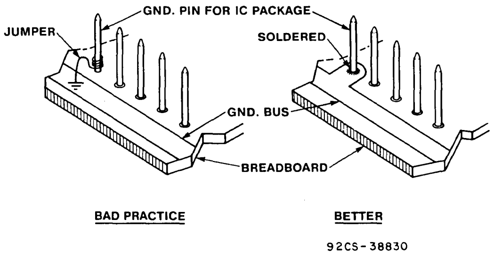


Fig. 3 - Ground connection on a logic board.

An even better solution is to use multilayer printed-circuit boards, where different layers can be used for the supply rails and the copper interconnections. The capacitive coupling between ground and V_{CC} is essential for high-frequency noise-pulse reduction. The capacitive coupling has the distinct advantage of being free from the inductive effects of the interconnections and, therefore, acts like a discrete decoupling capacitor.

Even with double-sided boards, it is advisable to have the V_{CC} and ground lines on opposite sides of the board wherever possible. A less expensive alternative to multilayer boards is the multiwire board, which offers the same high-frequency noise characteristics.

No matter what type of board is used, it is recommended that it have at least five ground pins per connector to assure ground-current distribution. The precautions taken with ground lines also apply to the V_{CC} line. Power-line stability is a must, a difference of only 0.5 V between V_{CC} lines can produce unwanted effects. It is advisable to provide separate power stabilization for each board to isolate noise sources and to eliminate large stabilizer circuits with their heavy-gauge (low-impedance) wiring to each board. However, care must be taken in designing power stabilization because a fault on a board's stabilizer circuit may be transmitted via the HC/HCT input structure to other boards, possibly causing damage.

DECOUPLING

No matter how good the V_{CC} and ground connections, all line-inductance effects cannot be avoided. This is where decoupling plays its part. Ceramic capacitors are the nearest approximation to ideal decoupling capacitors since they have almost no series inductance. But the advantage of using inductance-free capacitors is lost if long connections to the capacitor are used. These over-long connections can result in a tuned LC-circuit with a very high Q factor. The oscillations produced would have a worse effect on the circuit than if there were no decoupling at all. If it is not possible to make the decoupling connections shorter than 20 mm, place tracks in parallel, with a separation of at least one track width, as shown in Fig. 4. Making the connections thicker will have almost no effect.

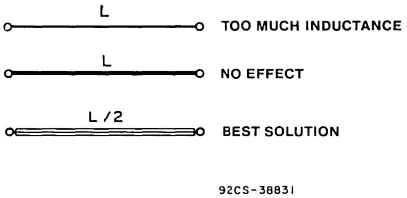


Fig. 4 - Comparison of decoupling tracks.

The capacitors to be used should be carefully selected. Many capacitors are produced with leads bent, as shown in Fig. 5(a); these may introduce unwanted inductance. The best capacitors are those with leads shaped as in Fig. 5(b).

In tests, good decoupling was obtained by using a minimum of:

- one 47 µF bulk capacitor per standard IC card
- one 1 µF tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal bus-driver circuit and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per four packages of SSI logic

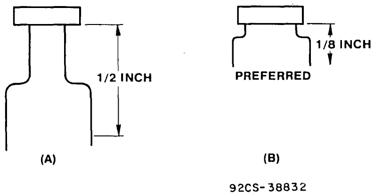


Fig. 5 - Optimum capacitor lead shape.

Replacing LSTTL with QMOS High-Speed Logic ICs

by J. Nadolski

Until the development of RCA HC and HCT high-speed-CMOS logic ICs, high-speed logic devices were available only in the high-power-consuming bipolar technology. The HC/HCT QMOS family features LSTTL speed along with many performance features superior to LSTTL. HCT CMOS ICs have TTL-compatible input-voltage levels and are intended to be CMOS substitutes for bipolar LSTTL logic ICs of the same type. HC CMOS ICs have CMOS voltage-level input compatibility and feature high noise immunity in all-CMOS system designs.

Replacement of an LSTTL IC with an HCT IC provides the identical logic function, same pin out, same speed, and same general-purpose logic fanout of 10 LSTTL loads, but with much less power dissipation. LSTTL bus-driver types can drive 100-ohm transmission-line terminations, but at a huge sacrifice in system power consumption. Techniques that can be used to terminate 100-ohm lines, and other types of low-power terminations involving LSTTL and QMOS ICs, are presented in this Note.

PERFORMANCE COMPARISON

Of paramount importance in the comparison of LSTTL and QMOS (HCT) performance are the identical input-voltage specifications of the two technologies:

$V_{IL}(max) = 0.8$ V

$V_{IH}(min) = 2$ V

Table I is a comparison of all applications-related parameters. It is evident from this table that not only does HCT QMOS substitute easily for LSTTL, but system performance is enhanced through such characteristics as better signal transition time and propagation delay balance, better noise margin, and lower supply and signal-line currents. The comparisons below follow the organization of Table I.

Power Consumption-(dc)—HCT power consumption is essentially zero in comparison to LSTTL. **ac (operating)**—HCT power is frequency dependent and comparable to LSTTL at continuously high operating frequencies. Generally, HCT power is much lower because average logic data rates are under 1 MHz.[1]

Voltage—HC/HCT CMOS requires much less voltage regulation than LSTTL. HCT devices can actually operate at 2 to 6 volts, although they are specified for 4.5 to 5.5 volts.

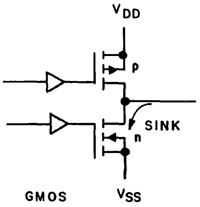
Temperature—Commercial-grade HC/HCT CMOS is more realistically rated than LSTTL, -40° C to +85° C, not the very limiting 0 to +70° C of most LSTTL 74 families.

Noise Margin—HCT interfacing with HCT or with LSTTL provides improved noise margin, particularly at the high end of the operating range where outputs swing to 5 volts.

Stability—The CMOS input PMOS/NMOS pair has less switching-voltage shift with temperature variation than LSTTL, an inherent circuit advantage compared to the LSTTL diode input design with its temperature sensitivity. This HCT advantage provides better noise margin over the device operating-temperature range and better stability of RC astable multivibrators with temperature variation when these circuits employ HCT ICs.

Output Drive Current—HC/HCT CMOS has better source current than LSTTL and sufficient sink current for LSTTL interfacing requirements. Sink current is lower than in LSTTL; this characteristic minimizes current spiking and EMI generation in RCA QMOS devices. This Note will delve into line terminations relative to sink current, the one area where differences in equipment design may exist depending on the high-speed logic family used.

Timing—The HC/HCT output-stage PMOS/NMOS transistors are designed for balance at saturation in order to provide balanced output transition times. All logic stages employ PMOS/NMOS transistor sizing, Fig. 1, to balance propagation delays, Fig. 2.



SINK AND SOURCE = 4 mA (STANDARD) 10 LSTTL LOADS
CURRENT = 6mA (BUS) 15 LSTTL LOADS

92CS-38673

Fig. 1 - Logic stage PMOS and NMOS transistor sizing to balance propagation delays.

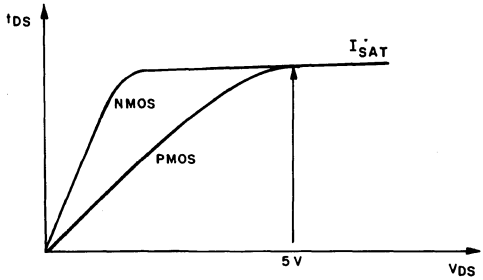


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Fig. 2 - Balanced output transition time and propagation delay.

Table I - Comparison of Characteristics of HCT and LSTTL Circuits

Characteristic	QMOS CD74HCTXXXX			74LSTTLXXXX	
Quiescent Power					
Per Gate	0.025 mW			5.5 mW	
Per Flip-Flop	0.05 mW			10 mW	
4-Stage Counter	0.4 mW			95 mW	
Per Transceiver/Buffer	0.1 mW			60 mW	
Operating Power	**Frequency In**			**Frequency In**	
	0.1 MHz	**1 MHz**	**10 MHz**	**0.1-1 MHz**	**10 MHz**
Per Gate	0.2 mW	2 mW	20 mW	5.5 mW	≅20 mW
Per Flip-Flop	0.15 mW	1.5 mW	15 mW	10 mW	≅15 mW
4-Stage Counter	0.24 mW	2.4 mW	24 mW	95 mW	≅120 mW
Per Transceiver/Buffer	0.25 mW	2.5 mW	25 mW	60 mW	≅90 mW
Operating Supply Voltage	(HCT) 4.5 V to 5.5 V (HC) 2 V to 6 V			4.75 V to 5.25 V	
Operating Temperature Range	-40° C to +85° C			0° C to +70° C	
Noise Margin					
LS to LS	—			0.7 V/0.4 V	
HC to HC (High/Low)	1.4 V/0.9 V			—	
HCT to HCT	2.9 V/0.47 V			—	
Input Switching Voltage Stability over Temp.	$V_S \pm 60$ mV			$V_S \pm 200$ mV	
Output Drive Current					
Source Current at V_{OH}=2.4 V	-8 mA			-400 μA	
Sink Current					
Std. Logic V_{OL}=0.4 V	4 mA			4 mA	
Bus Logic V_{OL}=0.4 V	6 mA			12 mA	
V_{OL}=0.5 V	12 mA			24 mA	
Output Transition Time*					
T_{TLH}	6 ns			15 ns	
T_{THL}	6 ns			6 ns	
Typical Gate Propagation Delay:*					
t_{PHL}/t_{PLH}	8 ns/8 ns			8 ns/11 ns	
V_{CC}=5 V, C_L=15 pF					
Typical Flip-Flop Propagation Delay:					
V_{CC}=5 V, C_L=15 pF					
t_{PLH}	14 ns			15 ns	
t_{PHL}	14 ns			22 ns	
Typical Clock Rate of a Flip-Flop	50 MHz			33 MHz	
Input Current					
I_{IL}	-1 μA			-0.4 to -0.8 mA	
I_{IH}	1 μA			40 μA	
3-State Output Leakage Current	±5 μA			±20 μA	
Reliability					
%/1000 Hours at 60% Confidence	0.0019 (RCA Report)			0.008 (RADC Report)	

*Temperature Coefficient = 0.04 ns/pF for both QMOS and LSTTL.

Frequency—QMOS clock rates are often higher than LSTTL clock rates.

Input Current—A big difference between the two technologies is the relatively large continuous dc current that flows in LSTTL interconnect wiring. Essentially no dc input current flows in HC/HCT CMOS. Typically, a few picoamperes of input back-diode current flows. This HCT advantage means better buffering and a wider frequency range in RC oscillators.

Leakage Current—Bus designs are enhanced by a four-times-lower high-Z output leakage current in HC/HCT CMOS as compared to LSTTL. For low-power designs, larger values of terminating resistors can be used.

Reliability—Reliability at 85° C junction temperature is four times improved with HC/HCT CMOS ICs. In fact, since the higher internal IC dissipation of LSTTL raises junction temperature an average of 10° C per IC, reliability improvement is even greater than the four-times improvement indicated.

INPUT/BUS/TRANSMISSION-LINE TERMINATION

Termination at inputs and outputs may be different for HCT and LSTTL devices. It is good design practice to properly terminate all unused LSTTL inputs. HCT devices can then be substituted directly, provided the unused input is returned to V_{CC}, ground or through a 1.2 kilohm or higher pull-up resistor. Output terminations are handled differently.

A discussion of termination follows. It is primarily in I/O terminations that differences in circuit design could exist and, hence, require design changes when HCT is substituted for LSTTL.

INPUT TERMINATION

The termination of unused inputs in LSTTL is not absolutely necessary because of the internal pull-up of 1.2 kilohms; however, it is good design practice to terminate all unused inputs to prevent linear operation of input circuitry. Such operation causes the circuitry to draw more power than it would under normal operation. The typical resistor values used for pull-up in termination of LSTTL are between 220 ohms and 1.2 kilohms; typical pull-down values are between 680 ohms and 1 kilohm. Unlike the case with LSTTL devices, unused HCT inputs must be terminated since the input is a very high impedance and, if left open, could cause the input circuitry to float into a linear mode of operation, thus drawing excessive current or causing oscillation. HCT devices **must** be terminated to V_{CC} or ground or with a pull-up or pull-down resistor with a value of 1 kilohm to 1 megohm, as shown in Fig. 3. The large-value resistors reduce the power dissipation of the driving devices.

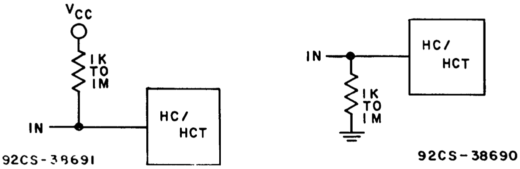


Fig. 3 - Methods of terminating HCT devices: (a) pull-up, (b) pull-down.

If an HCT device is to be used in a plug-in card system, all of the inputs from the card to the system **must** be terminated with pull-up resistance of a minimum value of 10 kilohms. In equipment designs using HC or HCT CMOS devices, where the inputs may be terminated to V_{CC}, there is an inherent current when V_{CC} is momentarily at ground.

One of the major uses of LSTTL is in computer and microprocessor-based systems. Parts such as bus drivers, transceivers, octal latches, and line drivers are widely used. All of these parts have three-state outputs. Three-state outputs allow a large number of circuits to connect to the same data bus by creating an open circuit on the device's output when it is not being accessed or utilized. The buses are usually terminated by a pull-up or a pull-down resistor. This resistance is necessary to prevent noise from being picked up on the bus. For LSTTL, the value of the pull-up resistor ranges from 330 ohms to a maximum of 100 kilohms. The choice of a pull-up or pull-down resistor will depend on whether a high or low state is required on the bus during the high-impedance state.

Termination resistors are usually placed at the most distant point from the bus-driving device. Multiple termination can be used, but these terminations must be individually high enough in resistance value so that the parallel resistive load on the bus driver is not too low; this load should be approximately 100 ohms minimum theveninized R for LSTTL bus drivers.

The typical values of pull-up for HCT bus drivers range from a minimum of 750 ohms to a maximum of 1 megohm. The choice of the resistor value involves a tradeoff between power and bus speed. A larger value of resistance will save power but will slow down the bus; a smaller value of resistance will speed up the bus, but will waste power. Typical values of pull-down resistance range from 680 ohms to 1 kilohm. A bus termination is a **must** for HC/HCT devices if the bus is to be in the high-impedance state for more than 100 microseconds. However, it is usually a good idea to terminate the three-state bus in case the system stops momentarily in the high-Z state or there is noise due to crosstalk in the system.

In any bus-driving configuration, all ICs must be by-passed with ceramic by-pass capacitors of at least 0.01 microfarad, as shown in Fig. 4. The capacitor is placed as close as possible to the ground pin to minimize inductance and, hence, ringing in the ground of the IC. Where HC/HCT is driving a terminated line and some slight ringing into ground exists, and this ringing or noise is above or near the input switching voltage of 1.3 volts, the receiving IC should be an HC CMOS type, which has an input switching point of approximately 2.3 volts (1 volt more than LSTTL or HCT).

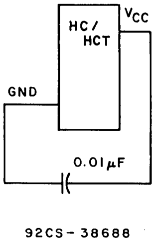


Fig. 4 - IC by-passing arrangement in a bus-driving configuration.

In some critical applications where almost no noise can be tolerated, the board or card can be bypassed with a 10-ohm or lower value resistor of the proper power rating in series with the supply line, and a 33 microfarad or larger capacitor across the supply, as shown in Fig. 5. This RC combination is placed at the point where the power supply comes into the board or card.

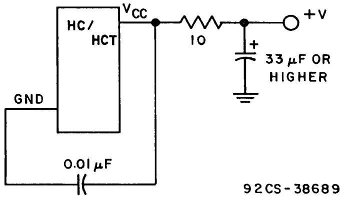


Fig. 5 - By-passing the board or card in a critical operation where almost no noise can be tolerated.

DRIVING TRANSMISSION LINES

Another type of termination required is that for transmission lines. This type of termination is used where data must travel over long distances in a system, in a large backplane, over coaxial cable, or in twisted-pair lines. This termination creates a low impedance that prevents noise and crosstalk from generating false data. Typical LSTTL systems use nominal 100-ohm twisted-pair, strip-line, or coaxial transmission-line impedances. This low impedance is necessary to the transmission of signals at high speeds without data degradation due to line capacitance or inductance. Fig. 6 shows a common LSTTL type of transmission-line termination. In order to drive this 120-ohm load, the LSTTL output sink current is required to be at least 24 milliamperes at a V_{OL} of 0.5 volt.

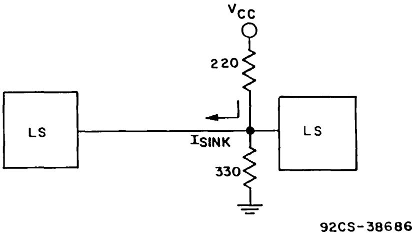


Fig. 6 - Common LSTTL transmission-line termination.

There are two powerful arguments for not duplicating this same 24 mA/0.5 V output specification in a well-designed HC or HCT bus-driver output stage:

1. 0.25 watt per output, 2 watts per octal driver, is high-power design, not moderate or low-power equipment design.
2. A CMOS output sink current of 24 milliamperes at 0.5 volt will give rise to an objectionably high transient current when switching, and will produce EMI which is objectionably large, much larger than the LSTTL output with the same current/voltage level. Fig. 7 shows the much higher I_{sat} in an NMOS output sink transistor versus an n-p-n output sink transistor. I_{sat} is twice as large, as are dv/dt and EMI, in CMOS as in LSTTL devices.

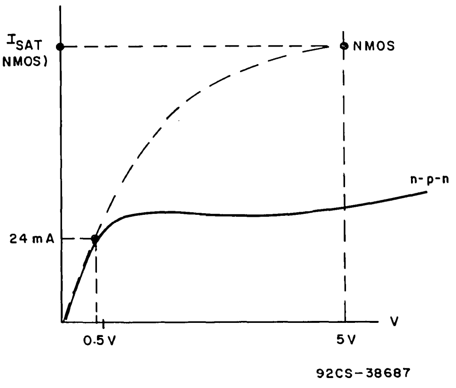


Fig. 7 - Comparison of I_{sat} in an n-p-n transistor and an NMOS transistor.

The RCA QMOS-device output stage is designed to provide typically more than 12 milliamperes at 0.5 volt. The QMOS I_{sat} is, then, similar to the LSTTL I_{sat}. The all-important noise-generation factor (EMI) is also similar at this current/voltage level.

The lowest impedance that an HCT/HC device can drive in the ac/dc termination described above is approximately 700 ohms, as shown in Fig. 8. This impedance is created with a 1.6 kilohm pull-up and 1 kilohm pull-down resistor, a combination that retains the 1/3 pull-down to 2/3 pull-up terminating-resistance design criteria. The terminators should be placed as close as possible to the receiving circuit. Higher values of transmission-line impedance can be used to save power, but the advisability of this choice will be determined by the speed of the data on the transmission line and the distance the data must travel.

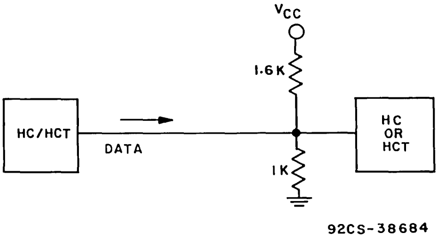


Fig. 8 - Lowest-impedance arrangement in transmission-line termination.

More than one termination of the type described can be used on the same line if required because of long line length or a very noisy environment; but the designer must remember that the worst-case sinking limit is still 12 milliamperes at 0.5 volt, and should treat these terminating impedances as being in parallel and limited to 700 ohms, as shown in Fig. 9.

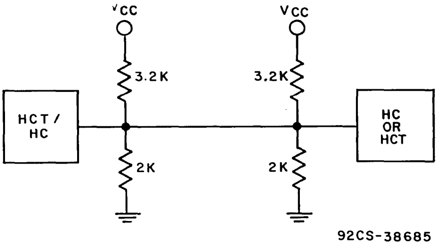


Fig. 9 - Multiple terminations on the same transmission line.

The above termination is useful for both dc and ac transmission-line terminations. With HC/HCT devices, a dc termination is not necessary, but an ac termination is a must. If the designer must have a transmission-line termination in an HC/HCT system, or must intermix families, then a variation on the voltage-divider termination can be used, as shown in Fig. 10.

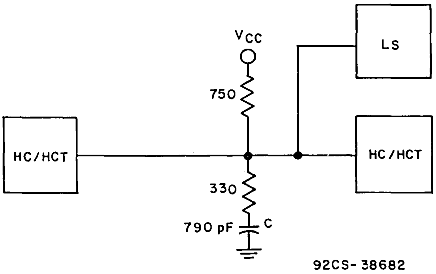


Fig. 10 - Transmission-line termination in HCT system or when families are intermixed.

Capacitor C is used to create a low impedance during switching. HC/HCT outputs can deliver up to 70 milliamperes during switching on bus types and up to 50 milliamperes on standard types. The value of C depends on the maximum frequency, f, of the bus. This value can be determined by the formula:

$$C = \frac{1}{2\pi f X_C} \qquad (1)$$

where Xc is approximately 50 ohms.

A typical value for C when f_{max} is 4 MHz or greater is 790 picofarads. When there is no switching, the only dc current present comes from the pull-up resistor. This configuration not only saves power but allows HC/HCT to drive a modified low-impedance transmission line. The configuration in Fig. 11 pulls the bus into the high state when it is in the high-impedance mode. If a low state is required on the bus, the configuration in Fig. 12 can be used. If more than one of these terminations are required on the same line, the designer must treat the terminations as being in parallel, and should adjust the values of R and C to comply with the maximum dc sink current of 12 milliamperes at 0.5 volt, as shown in Fig. 13.

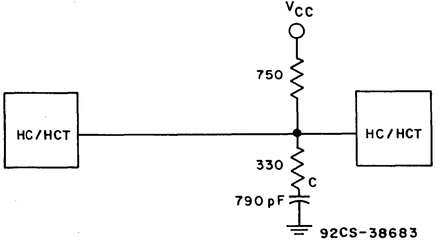


Fig. 11 - Configuration used to pull the bus into the high state when it is in the high-impedance mode.

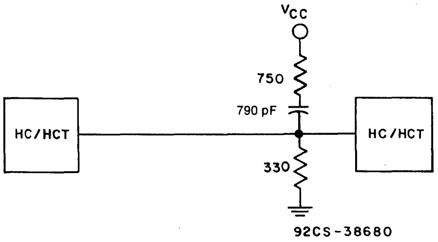


Fig. 12 - Configuration used to pull the bus into the low state when it is in the high-impedance mode.

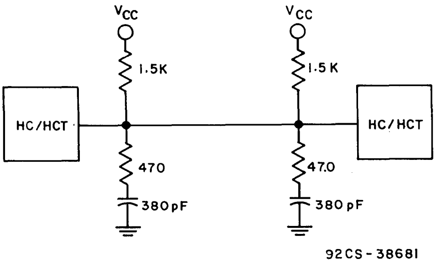


Fig. 13 - When more than one of the terminations of Figs. 11 and 12 are needed, the terminations are adjusted and treated as if they are in parallel.

DRIVING COAXIAL CABLE

LSTTL ICs can drive transmission lines using coaxial cable. Various types of coaxial and triaxial cable are available, but the most commonly used is the 75-ohm RG-59/59U, which has an impedance of 75 ohms at its nominal operating frequency. LSTTL bus drivers can directly drive almost all of the popular terminations used with coaxial-cable drive. One of the most commonly used is shown in Fig. 14. An HC/HCT device cannot drive any of these terminations without exceeding its maximum sink current. However, HC/HCT devices can drive coaxial cable by using the modified transmission-line termination shown in Fig. 15 or a modified resistor terminator, as shown in Fig. 16. The coaxial cable should be terminated at both ends in cable runs over 50 feet, again keeping in mind the maximum limits of HC/HCT sink current. Equation 1 can be used, with the addition of the figure for the capacitance of the coaxial cable, per foot, to calculate the correct value of capacitance C in Fig. 17.

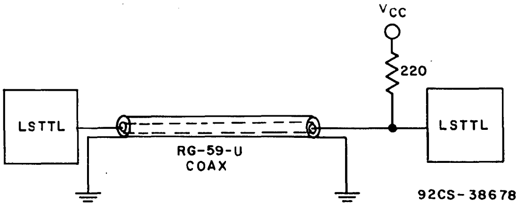


Fig. 14 - A commonly used LSTTL coaxial-cable termination.

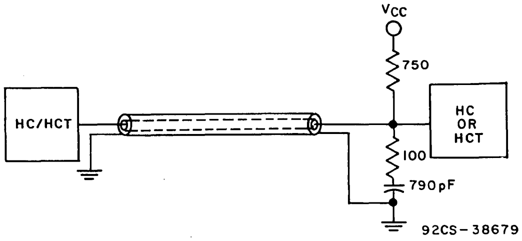


Fig. 15 - Modified transmission-line termination used with HCT devices driving coaxial lines.

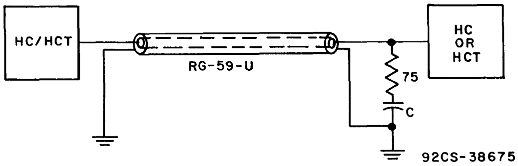


Fig. 16 - Modified resistor termination used with HCT devices to drive coaxial lines.

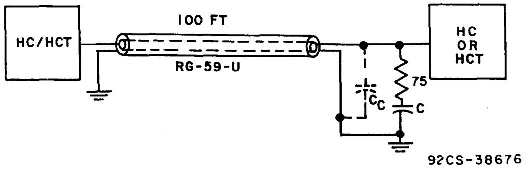


Fig. 17 - Effect of cable capacitance on termination.

By using a modified transmission-line termination for HC/HCT devices, and depending on the maximum frequency to be driven, coaxial cables of various lengths can be CMOS driven. A typical example is shown in Fig. 18, where an HC/HCT device drives more than 50 feet of RG-59U coaxial cable with a modified termination of 75 ohms. A series capacitor in the resistor leg that goes to $+V_{CC}$ is placed at the receiver end of the cable to eliminate degradation which could cause false data to be received.

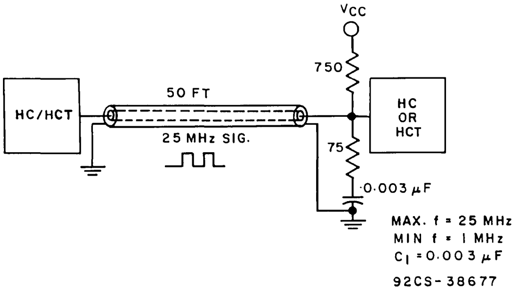


Fig. 18 - Termination configuration used to eliminate possibility of false data at receiver.

DRIVING RIBBON CABLE

When using HC/HCT ICs to drive signals over ribbon cable, there are length limitations resulting from the high impedance of the CMOS input. The drive limit is two feet maximum at normal data rates when driving without any termination and without the use of an alternate ground scheme (alternating signal carrying and grounded wires, as shown in Fig. 19) in the ribbon cable. Beyond two feet, crosstalk between signal lines can cause errors in data. If the receiving IC is an HC type, the maximum drive lengths can double.

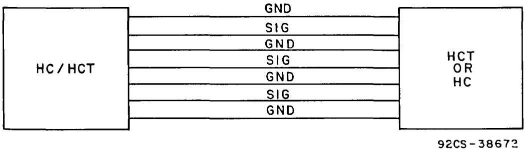


Fig. 19 - Alternate ground arrangement of ribbon cable.

When driving with no termination but with the alternate ground method, the maximum drive length before crosstalk between signal lines can cause errors in data is six feet at normal data rates.

HC/HCT devices can drive longer ribbon cable by using various terminations: pull-up, pull-down, or one of the modified transmission-line terminations. When using a 1-kilohm pull-up resistor per wire as a termination, the maximum length without alternate ground before crosstalk can become a problem is four feet at normal data rates. When using the same setup with an alternate ground scheme, as shown in Fig. 20, the maximum length of drive is seven feet at normal data rates. The maximum drive limit is six feet, as shown in Fig. 21, when a modified transmission-line termination with an impedance of approximately 100 ohms and no alternate ground scheme is used at normal data rates. More than 15 feet can be driven at a data rate of 10 MHz when the alternate ground scheme is employed along with the termination of Fig. 21. The length can be extended by using any of the above terminations at both the receiving and transmitting ends of the cable.

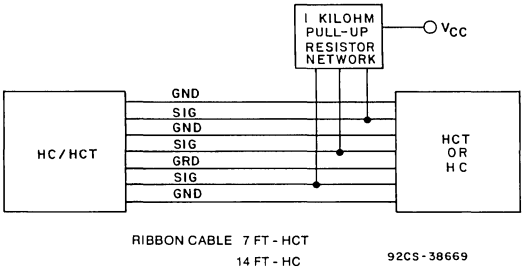


Fig. 20 - Ribbon-cable termination using 1-kilohm pull-up resistor and alternate ground arrangement.

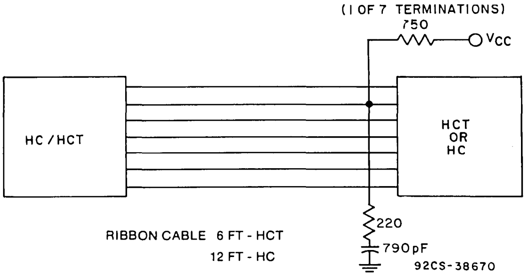


Fig. 21 - HCT ribbon-cable termination for normal data rates using impedance of approximately 100 ohms and no alternate ground system.

There are many other types of transmission-line terminations, but those shown above are the most commonly used with HCT/HC devices. When contemplating terminations of any sort, the designer must remember that HCT/HC devices have a current-sinking limit at 0.4 volt of 6 milliamperes, and at 0.5 volt of 12 milliamperes. These limits **must** be observed. By following the termination criteria described above, system power consumption is reduced, reliability is greatly improved, and system cost is decreased.

REFERENCES

1. For a full discussion of HC/HCT power consumption and how to calculate it, see RCA Solid State Publication ICAN-7315, "Power Consumption in QMOS Logic Circuits," by R. Funk.

Astable Multivibrator Design Using High-Speed QMOS ICs

by L. Marechal

This Note describes the design of astable multivibrators using RCA high-speed-CMOS (QMOS) integrated circuits (CD54/74 HC, HCU, HCT04 and 132), and multivibrator performance at frequencies up to 10 MHz.[1] Algebraic equations permit the values of R and C for a given oscillator frequency to be quickly determined. The effect of supply voltage and temperature variation on multivibrator performance is discussed along with the inherently low power consumption of QMOS relative to LSTTL. In addition to much lower power dissipation than other technologies, a distinct advantage of QMOS RC multivibrator design is the choice of a very wide range of R_XC_X, which leads to an exceptional frequency range.

OPERATING FREQUENCY

Fig. 1 (a) shows the basic multivibrator circuit configuration. Resistor R and capacitor C fix the operating frequency. R_S assures that frequency will be independent of minor supply-voltage variations, and reduces the time-period variations to less than 5% with variations in transfer voltage. Fig. 1(b) shows the operating waveforms of the circuit.

Equation (1) determines the time-period T:

$$T = -RC\ \ln \frac{V_{TR}\,(V_{CC}-V_{TR})}{(V_{CC}+V_D)^2} - \frac{K}{K+1}\,RC\ \ln \frac{K(V_{CC}+V_D)}{K(V_{CC}+V_{TR})+V_{TR}-V_D}$$

$$- \frac{K}{K+1}\,RC\ \ln \frac{K(V_{CC}/V_D)}{K(2V_{CC}-V_{TR})-V_{TR}-V_D} \qquad (1)$$

where V_{CC} is the supply voltage, V_{TR} is the transfer voltage, V_D is the diode forward voltage drop, and K is R_S/R.

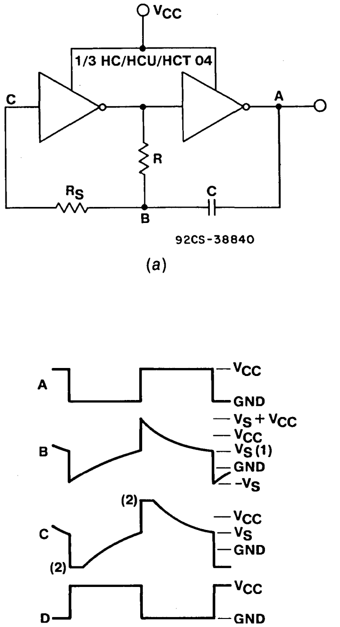
High-speed CMOS devices have a built-in 100 to 150-ohm input resistor which has little influence on speed because C charges and discharges through R and the IC output.

As K approaches infinity, the variation in time period as a function of V_{CC} approaches zero. Variation in period with transfer voltage is reduced by 10% for K=0 and by 5% for large values of K.

Figs. 2(a) and 2(b) are plots of the theoretical time periods, as calculated from equation (1), for HC and HCT devices, respectively. In all calculations $V_D = 0.6$ V. Equation (1) can be simplified for large values of K to the form shown in equation (2):

$$T = -RC\ \ln \left(\frac{V_{TR}}{V_{CC}+V_{TR}} + \ln \frac{V_{CC}-V_{TR}}{2V_{CC}-V_{TR}} \right) \qquad (2)$$

where $K \geq 10$.



NOTES

1.

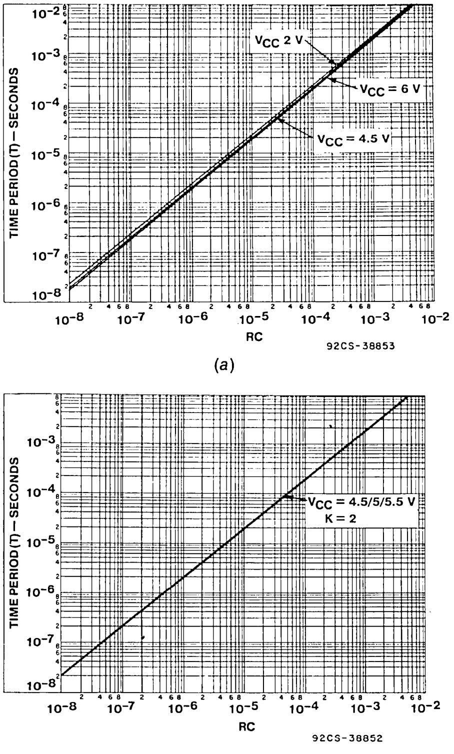
	V_S
HC	0.5 V_{CC}
HCU	0.5 V_{CC}
HCT	1.4 V FOR V_{CC} = 5 V

2. SMALL CLAMPING ACTION OF INPUT DIODES: NEGLIGIBLE FOR LARGE R_S; SIGNIFICANT FOR SMALL R_S

92CS-38839

(b)

Fig. 1 - (a) Astable multivibrator using the CD54/74 HC/HCU/HCT04, (b) waveforms for the circuit of (a).



(a)

(b)

Fig. 2 - Time period (T) as a function of RC using equation (1) for (a) HC04 type and (b) HCT04 type.

Using the HC04 type, equation (2) can be simplified if the valid assumption that $V_{TR} = 0.5\ V_{CC}$ is made. Then:

$$T = 2.2\ RC \qquad (3)$$

Fig. 3 illustrates how little the choice of either equation (1) or (3) affects results in a practical case.

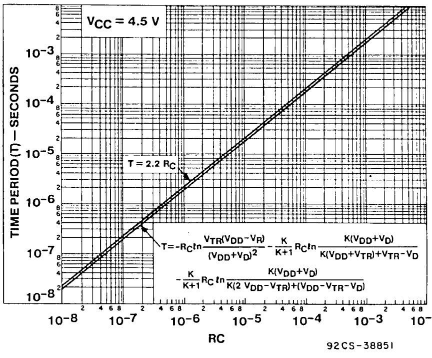
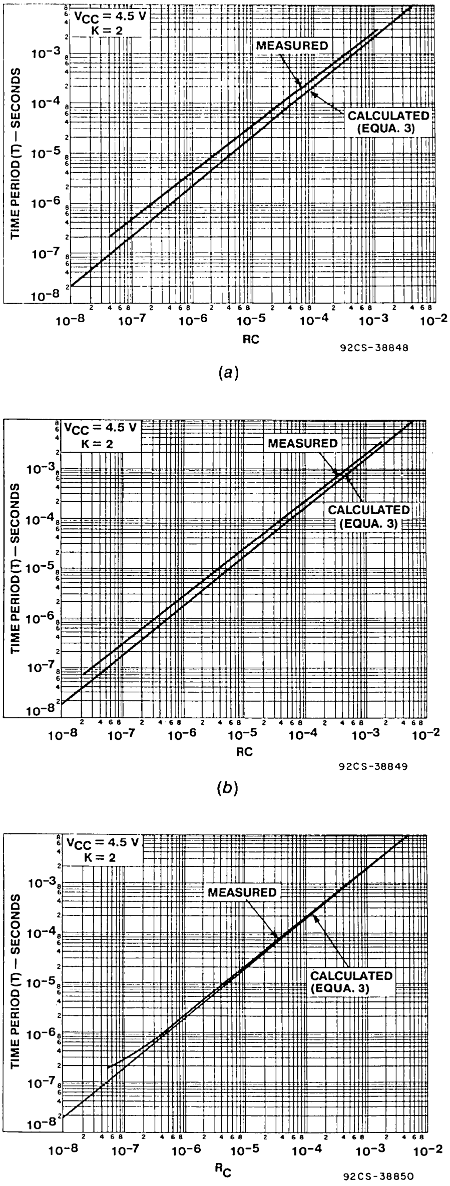


Fig. 3 - Time period as a function of RC using theoretical approach of equation (1) versus equation (3) for type HC04.

Figs. 4(a) through 4(c) show plots of measurements and calculated values of the time-period as a function of the time constant, RC, for the three series HC, HCU, and HCT, respectively. The simplified equation, (3), was used in each case. Note that the plot for the HCT04 (Fig. 4(c)) shows good tracking of calculated values (using equation (3)) with measured values, even though V_{TR}=0.31 V_{CC} instead of 0.5 V_{CC}.



(a)

(b)

(c)

Fig. 4 - Measured versus calculated T as a function of RC for (a) HC04 type, (b) HCU04 type, and (c) HCT04 type.

Fig. 5 identifies the area of validity of R and C for equations (1) and (3). Measurements were made with the time constant as a parameter. The points on the chart are ratios of measured to calculated time period. The design guidelines used to keep the ratio of measured T to calculated T close to one, as shown in Fig. 5, follow.

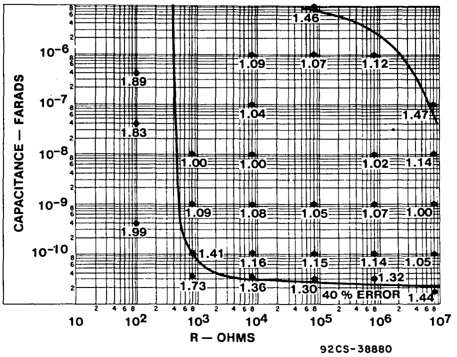


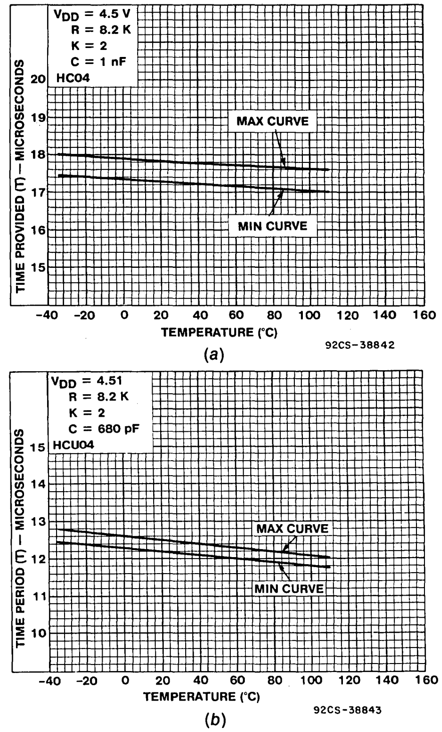
Fig. 5 - Area of theoretical equation validity. Points are ratios of measured to calculated T.

R_S in Fig. 1 must not be made too large, as the multivibrator time constant and phase shift is influenced by this resistance (as well as by stray wiring and breadboard capacitance). A large value of R_S will change the time period and cause spurious oscillations and glitches.

In the oscillator circuit, C should be greater than or equal to 100 pF to eliminate probe and stray capacitance interference. R should be greater than or equal to 100 ohms to support the function of R_S. However, to avoid parasitic oscillation, R must not be made too large. Appropriate values of R and C depend upon circuit design and layout.

Equation (3) is valid for $R \geq 50$ kilohms and $C \geq 1000$ pF; use equation (1) for $R < 50$ kilohms, and $C < 1000$ pF. However, note that, as implied above, if C is less than 1000 pF, stray capacitance will affect the entire system.

CMOS multivibrator designs have long been known to be temperature insensitive. The variation of the input switching voltage (V_S) with temperature in a QMOS device is only ±60 mV over a range of -55° C to +125° C; in contrast, the LSTTL V_S varies ±200 mV over the same temperature range. Figs. 6(a) and 6(b) reflect the minor change in period T, less than 3% for HC and 10% for HCU devices over a 150° C temperature range, resulting from the small variation in QMOS V_S.



(*a*)

(*b*)

Fig. 6 - Time period as a function of temperature for (a) HC04 type and (b) HCU04 type.

POWER CONSUMPTION

One of the major advantages of the CMOS technology and, hence, QMOS ICs, is the low power dissipation. The power consumed by the RC oscillator of Fig. 7, using the HCT04 is:

$$P_D = P_A + P_B \qquad (4)$$

where

$$P_A \text{ and } P_B = (C_{PD} + C/2)V^2 f \qquad (5)$$

C_{PD} is a capacitive value used to represent internal inverter power consumption. C_{PD} is rated at 36 pF on the HC/HCT04 Data Sheet. The C in equation (5) is the RC oscillator capacitance seen as a load that is shared by inverters A and B of Fig. 7.

Table I contains parameters, data, and calculations for five operating frequencies. Fig. 8 shows plots of the measured

Table I - Measured VS Calculated RC-Oscillator Power Dissipation (V_{CC}=5.5 V)

RC	R (ohms)	C (F)	T	T/C (s/F)	f	I meas'rd (mA)	V_I P meas'rd (mW)	$(72\ pF + C)V^2$ 2.2 RC P calculated (mW)	2.2 RC T (ms)	2.2 R T/C (s/F)
$4.7\ 10^{-8}$	470	10^{-10}	166 ns	$1.66\ 10^3$	6.024 MHz	11.066	60.863	50.32	0.1034 μs	$1.034\ 10^3$
$4.7\ 10^{-7}$	4700	10^{-10}	1.4 μs	$1.40\ 10^4$	714 kHz	2.998	16.489	5.032	1.034 μs	$1.034\ 10^4$
$4.7\ 10^{-5}$	47,000	10^{-9}	116 μs	$1.16\ 10^5$	8.62 kHz	0.9082	4.995	0.2946	0.1034	$1.034\ 10^5$
$4.7\ 10^{-3}$	47,000	10^{-7}	12.6 ms	$1.26\ 10^5$	79.36 Hz	0.644	3.542	0.2926	10.34	$1.034\ 10^5$
$4.7\ 10^{-2}$	22,100	$2.2\ 10^{-6}$	12.4 ms	$1.24\ 10^4$	80.64 Hz	0.707	3.888	0.622	106.964	$4.362\ 10^4$

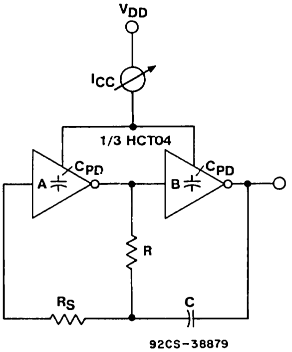


Fig. 7 - RC oscillator circuit.

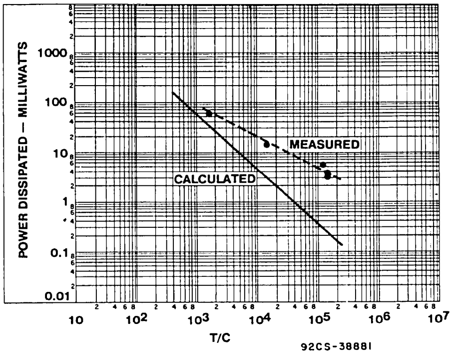


Fig. 8 - Power dissipation in oscillator (using an HCT04) as a function of T/C ratio (V_{CC} = 5.5 V).

versus calculated power. Table I and Fig. 8 illustrate two key points concerning RC oscillator power:

1. Power is heavily dependent on the value of C.
2. Calculations are valid only at higher frequencies, generally above 1 MHz.

Because of the dependence of power on both the frequency and value of C, power is plotted (Fig. 8) as a function of the T/C ratio. Fig. 9 illustrates a common method of reducing QMOS RC-oscillator power consumption. In the circuit, small-valued, current-limiting resistors, R_r, are placed in series with the circuit dc supply voltage, V_{CC}, and with the ground terminals. This arrangement reduces the CMOS flowthrough current during slow switching transitions, when both the PMOS and NMOS transistors conduct transient current from V_{CC} to ground.

In addition to reducing power consumption, resistor R_r also decreases the RC operating frequency. The power reduction is more pronounced with HCU devices, for which the spiking-current component is larger. In these devices, the switch from the low level to the high level and vice versa begins at an input-switching voltage lower in the ground-to-V_{CC} range than in other QMOS types. HC devices do not see a significant reduction in power unless the operating frequency is very high. There is a 20% power reduction at 6 MHz with a 50-ohm R_r, while there is no improvement at all at 10 kHz with the same resistance. In the case of HCU devices, the power benefit from the introduction of the 50-ohm R_r is 60% at 5 MHz, but only 20% at 10 kHz for a V_{CC} of 4.5 V. At low frequency in any QMOS device, the spiking current losses become negligible compared to the power dissipated in the external components.

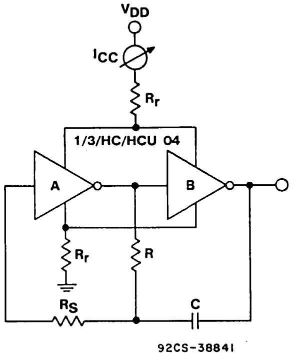
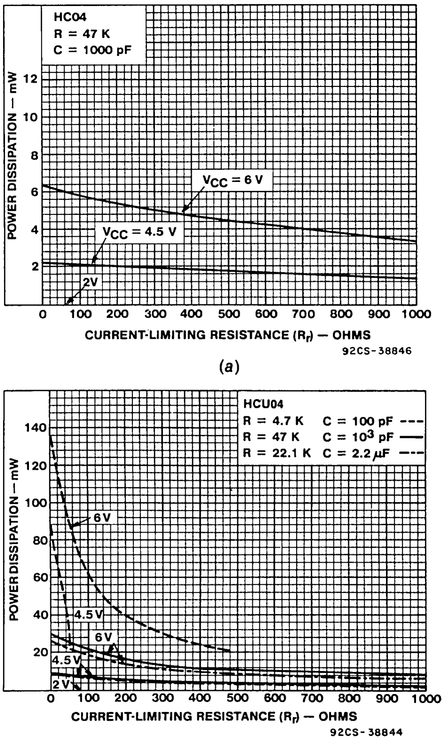


Fig. 9 - Common method of reducing QMOS RC-oscillator power consumption.

The effect of resistor R_r in Fig. 9 is to decrease the output charging current of CMOS inverter (B) into capacitor C, hence the increased charging time of C. The impact of R_r on frequency when large values of resistor R are used is minimal; there is a 2% frequency decrease for HC and a 2.5% decrease for HCU when R is 47 kilohms, C is 1000 pF, and R_r is 1 kilohm. Figs. 10(a) and 10(b) plot power consumption against the value of R_r for the HC04 and HCU04 types, respectively.



(*a*)

(*b*)

Fig. 10 - Power dissipation in an oscillator as a function of R_r. In (a) the oscillator employs an HC04, in (b) an HCU04.

RC OSCILLATOR USING THE HC/HCT132 SCHMITT TRIGGER

The RCA HC/HCT132 can be used in an astable multivibrator, as shown in Fig. 11. The equation used to calculate the period T is:

$$T = RC \ln \frac{V_{CC}-V_N}{V_{CC}-V_P} + RC \ln \frac{V_P}{V_N} \qquad (7)$$

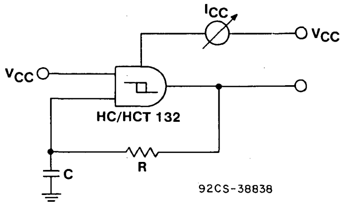


Fig. 11 - The HC/HCT132 in an astable multivibrator circuit.

Fig. 12 plots measured T versus RC for the HC132. Also plotted in Fig. 12 are calculated values of T versus RC using equation (7). Fig. 13 is a plot of measured T versus RC for the HCT132. Figs. 14(a) and 14(b) show measured power dissipation as a function of time-constant RC in oscillators employing the HC132 and HCT132, respectively.

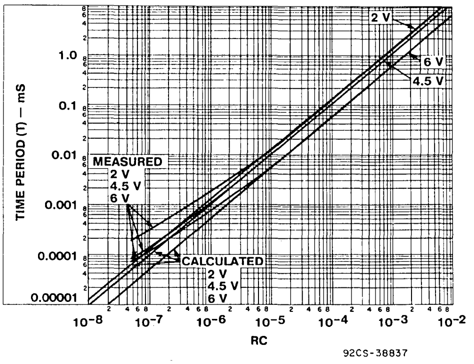


Fig. 12 - Measured and calculated time period of oscillating HC132 as a function of time constant RC.

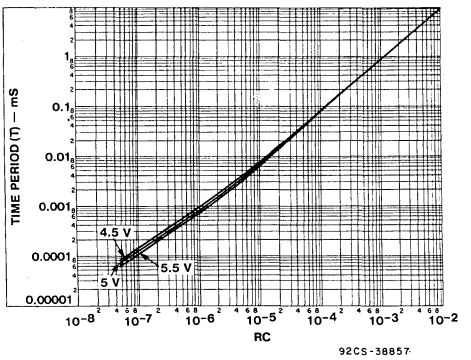
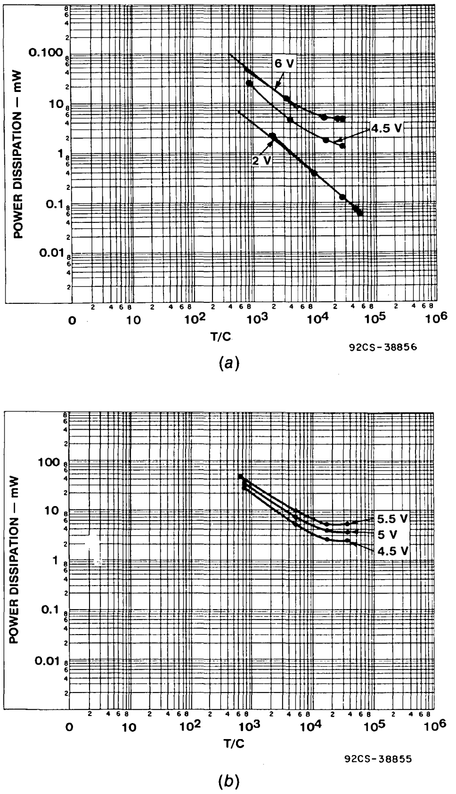


Fig. 13 - Measured time period of oscillating HCT132 as a function of time constant RC.



(*a*)

(*b*)

Fig. 14 - Measured power dissipated as a function of T/C, (a) in an oscillating HC132 and (b) in an HCT132.

REFERENCES

1. For more information on CMOS circuits in oscillators and other timing applications, see:

   "Astable and Monostable Oscillators Using RCA CMOS Digital Integrated Circuits," RCA Solid State Application Note ICAN-6466.

   "Using the CD4047A in CMOS Timing Applications," RCA Solid State Application Note ICAN-6230.

   "Simplified Design of Astable RC Oscillators Using the CD4060B or Two CMOS Inverters," RCA Solid State Application Note ICAN-6883.

2. For a discussion of C_{PD}, see *QMOS High-Speed CMOS Logic ICs*, RCA Solid State DATABOOK SSD-290, under "Description of QMOS product Line."

Linear Application of the CD54/74HCU04 QMOS Hex Inverter

by W. Austin

Because the CD54/74HCU04, Unbuffered Hex Inverter,[1] is a QMOS device based on a 3-micron process, it is an excellent high-speed digital switch. Its linear characteristics feature low capacitance and high current drive. A high transconductance associated with the high current drive is contributed by pairs of complementary NMOS and PMOS transistors, which form relatively simple inverting amplifiers. There are six of these transistor-pair amplifiers in the HCU04; each has a common V_{CC} and ground. A variety of application circuits are included in this Note to illustrate the many uses of the HCU04 amplifier.

The equivalent circuits shown and the characteristics described in this Note will help the user to apply the HCU04 in linear applications (a knowledge of linear-feedback circuit theory is assumed). Fig. 1 shows the internal functional diagram and the circuit schematic of each inverter.

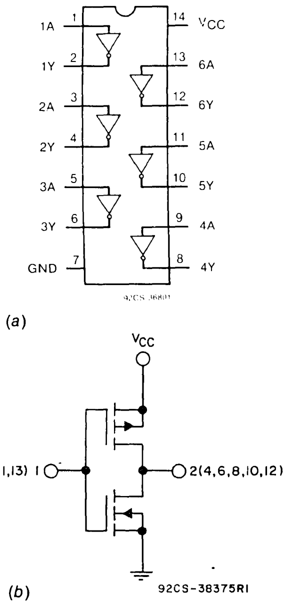


Fig. 1 - The HCU04 Hex Inverter: (a) functional diagram, (b) internal schematic.

PMOS AND NMOS DEVICE CHARACTERISTICS

As mentioned above, each pair of PMOS and NMOS devices in the HCU04 make a relatively simple inverting amplifier; one feedback resistor provides static bias. The amplifier transfer characteristic of each unbuffered inverter has a dynamic range of up to three volts, peak-to-peak, with good linearity in the center one volt, peak-to-peak, region. The transfer characteristic of the HCU04 is shown in Fig. 2.

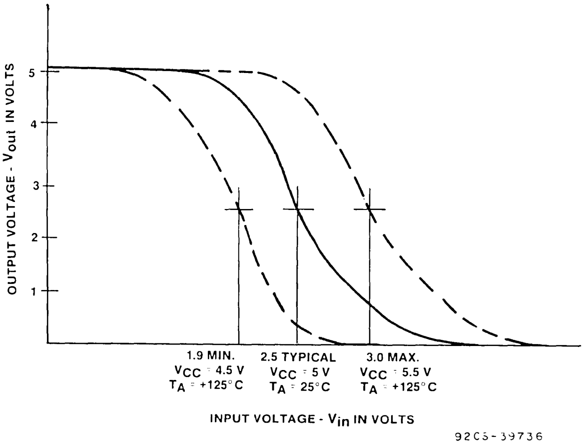
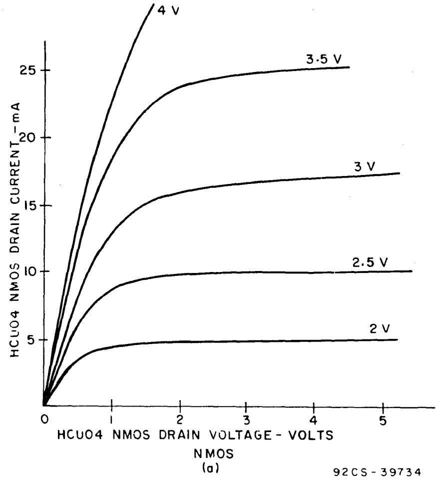


Fig. 2 - Min./max. and typical switching transfer characterstics of the HUC04 Unbuffer Hex Inverter.

The characteristics desired in any high-quality amplifier are high gain, good linearity, and wide bandwidth. The wide bandwidth of the HCU04 is inherent in the QMOS process, but its gain and linearity are a function of the transfer parameters.

The slope of the transfer curve is determined by the transition of the PMOS and NMOS devices; this slope can be evaluated with a sweep at the gate input. On a positive, increasing voltage, the p channel is pinched off near the positive V_{CC} level. The n-channel drain current is enhanced as the voltage increases from ground toward the V_{CC} level. In reverse, the p-channel current is increased with negative-going input voltage, while the n-channel current is decreased.

Families of curves showing typical drain characteristics for both the PMOS and NMOS devices are shown in Fig. 3. The characteristics are standard for n and p enhancement-type devices. The drain currents in the p and n devices are balanced by device design: the typical n-channel width is 800 microns; the typical p-channel width is 1800 microns. This dimension compensates for the lower PMOS-channel hole mobility.



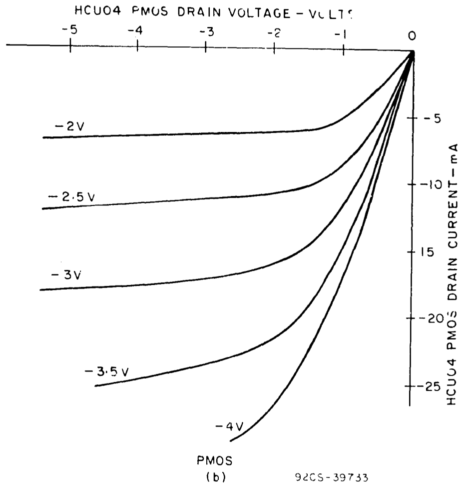


Fig. 3 - Typical drain family characterstics of the HCU04: (a) NMOS and, (b) PMOS sections.

When the inverting amplifier is in an unloaded condition, each PMOS or NMOS device is both a driver and load over some portion of the transfer curve. Since the equity of current in each device must be maintained, and since each device must act as a current sink or source, the amplifier output voltage is determined by the balance of current sink and current source bias conditions. The drain current, I_d, in each amplifier peaks, typically, when both channels are balanced at V_{in} = V_{out} = $V_{CC}/2$. Any imbalance of drain characteristics may cause a deviation in peak drain current, and produce a crossover offset in the transfer characteristic. Typically, the offset is less than ±5% of the V_{CC} range. This figure represents what is called the "offset tolerance."

LOADLINE CHARACTERISTICS

To better show how the HCU04 functions in its linear transitions of the input-voltage range, the PMOS and NMOS drain loadlines have been plotted, as the gate voltage, V_{in}, is stepped, at incremental points of operation; Fig. 4. The figure includes a 75-ohm loadline at $V_{CC}/2$ = 2.5 V as a point of reference.

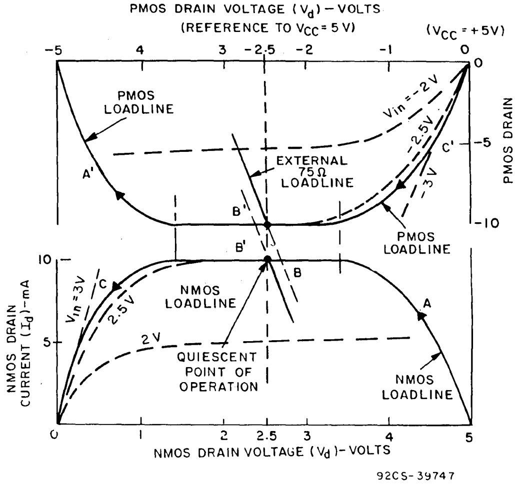


Fig. 4 - Loadline plots on the NMOS and PMOS drain-family characterstics as V_{in} is varied from zero volts to V_{in} = V_{CC} = +5 V in the HCU04.

The loadline curves defined in Fig. 4 by path ABC for the NMOS device and A'B'C' for the PMOS device are the respective loci as V_{in} varies from ground to V_{CC} = +5 V for the unloaded HCU04. An optimum external-resistance loadline of the NMOS device is normally a straight line extending with a negative slope from gate cutoff to the quiescent operating point and through to the saturated knee of the family of drain curves. A similar positive slope loadline applies to the PMOS device. Since an MOS transistor is not a linear load element, the extremes of the loadline exhibit the nonlinearity shown in Fig. 4. And because each saturated PMOS or NMOS device is a load in parallel with any external load, nonlinearity may occur at the extremes of drain-voltage swing. An output voltage range of 1.5 to 3.5 volts will provide a linear high-impedance source resistance in parallel with the external 75-ohm load.

In the NMOS loadline area, A, the loadline rises sharply from coordinates V_d = +5 V and I_d = 0 mA with a slope equal to the saturated channel resistance of the PMOS device. The +5 V and 0 mA point corresponds to the NMOS channel cutoff. Progressing on the loadline locus: as V_{in} increases, the curve rounds from A to B, where the PMOS device changes from a saturated device to an active load. As the slope of the curve flattens, a balance of maximum source and sink current is reached. The transition across the flat portion of the loadline curve will occur with a few millivolts of delta change of V_{in}, and peak I_{CC} current should occur when V_{in} = $V_{CC}/2$.

In the C area of the curve, the PMOS device is a high-impedance active current sink controlling the NMOS drain current, which is decreasing in value as the PMOS channel is being pinched off. A similar description of the PMOS loadline applies to the A'B'C'-curve loadline locus. The combined action of the PMOS and NMOS devices, as V_{in} varies from zero to V_{CC}, produces an active transfer curve.

Balanced PMOS and NMOS characteristics will produce a transition at B and B', where $V_{in} = 2.5$ V when $V_{CC} = 5$ V. Any variation in this balance will produce a crossover offset in the transfer characteristic, as described above.

The transition of the loadline characteristic for $0<V_{in}<V_{CC}$ produces the transfer characteristic of Fig. 5. At either end of the loadline, the effective amplifier source impedance, R_d, is low because the internal load consists of the saturated drain of the p or n device. In the center of the range, both the PMOS and NMOS devices are linear, with high effective R_d. If the V_{in} signal swings beyond the knee (or corners) of the transfer characteristic, compression of the output signal will result. Fig. 5 shows an example of a linear sinewave input and output signal.

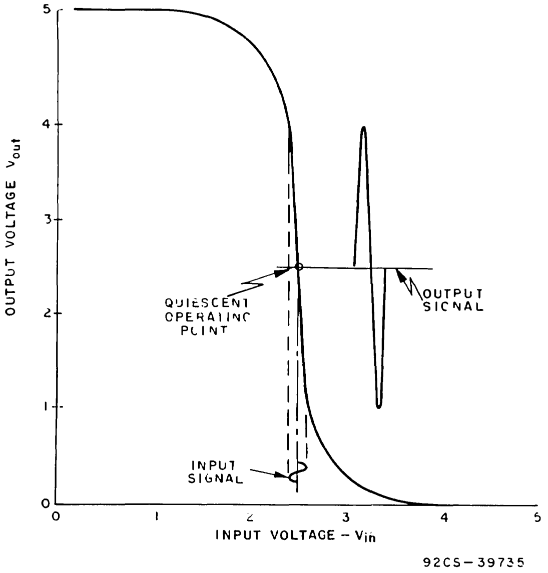


Fig. 5 - Amplifier transfer characteristics of the HCU04 amplifiers.

LINEAR-AMPLIFIER MODEL

A linear-amplifier model of the HCU04 includes the inverting amplifier and its associated input, output, and feedback capacitance, as shown in Fig. 6. An external feedback resistor, R_f, provides bias stability.

If the input coupling capacitor, C_c, is sufficiently large, the op-amp closed-loop gain is given by:

$$A_{fb} = \frac{A_{ol}}{1 + (1/B)(1 - A_{ol})}$$

where A_{ol} is the open-loop gain, and $B = R_f/R_s$, the feedback resistor ratio.

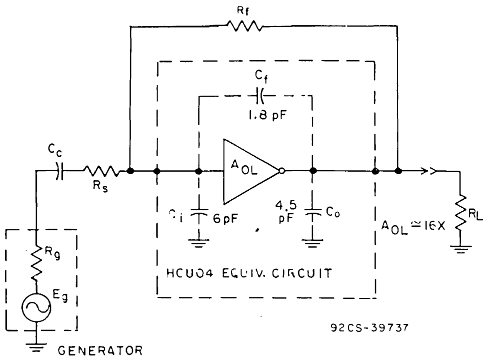


Fig. 6 - Linear model of each of the six amplifiers of the HCU04.

The normal op-amp gain equations usually assume A_{ol} to be very large, and the output impedance very small. For the circuit of Fig. 6, the gain becomes $-(R_f/R_s)$. This approximation will contain some error when applied to the HCU04 because the open-loop gain is typically 16, not a very small number in comparison to the open-loop gain of most op amps.

The feedback-resistor bias will stabilize amplifier operation near the center of the transfer curve; some offset is present, as noted above. The offset will reduce the dynamic range of output, but requires no correction unless dc coupling is used. The expected offset is typically less than ± 0.25 volts.

EQUIVALENT CIRCUIT

Calculations based on an equivalent linear model may be used to predict various biasing results. A two-generator linear-circuit model is shown in Fig. 7.

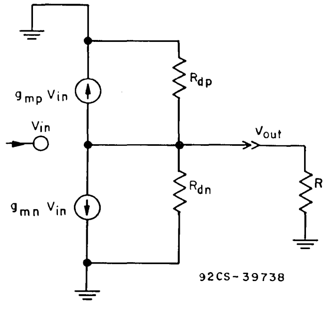


Fig. 7 - Circuit equivalent of the HCU04 with two source generators and no feedback.

Since the V_{out} node equation for the two generator equivalent circuit is:

$$-g_{mp}(V_{in}) - g_{mn}(V_{in}) = V_{out}(1/R_{dn} + 1/R_{dp} + 1/R_L)$$

and

$$A_{ol} = V_{out}/V_{in} = \frac{-(g_{mp} + g_{mn})}{(1/R_{dn} + 1/R_{dp} + 1/R_L)}$$

The source-generator and parallel conductances of the NMOS and PMOS equivalent models may be simply added into one equivalent.

A single-generator model has no restrictions, provided the equivalent circuit is a reasonable linear approximation. A simplified model of the circuit of Fig. 6, with associated capacitance and biasing, is shown in Fig. 8. The single-model equivalent-current generator and effective source impedance may be determined from the separate device models, and is equal to:

$g_m = g_{mp} + g_{mn}$

$R_d = R_{dp} R_{dn}/(R_{dp} + R_{dn})$

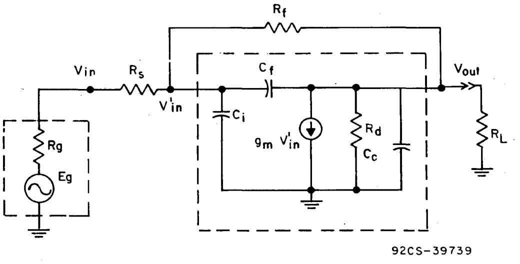


Fig. 8 - Simplified HCU04 circuit model with associated capacitance and biasing.

All further references to g_m and R_d imply a single-generator model. It should be noted, however, that use of the two-generator equivalent model does have practical merit in the analysis of abnormal input-signal conditions or when considering the effects of V_{CC} and ground-terminal impedance.

Determination of the g_m and R_d parameters is based on either direct evaluation from the drain family characteristics of Fig. 3 or measured data. From the curves of Fig. 3, g_m is $\Delta I_d/\Delta V_{in}$, and R_d is the tangential $\Delta V_d/\Delta I_d$ slope on the V_{in} bias line at the point of operation. The simplest way to determine g_m is to measure $A \sim A_{oi}$ when R_f is very large and R_s is small, e.g., 100 kilohm and 50 ohms, respectively.

When R_L is much less than R_d:

$A \sim -g_m R_L$, and $g_m \sim A/R_L$

The gain is then measured under the same conditions with R_L removed (open) and R_d as the effective load. For this condition,

$A \sim -g_m R_d$, and $R_d \sim A/g_m$

A variety of amplifier gain conditions have been measured for the circuit of Fig. 9 and, in some cases, calculations have been made for g_m and R_d. A tabulation of the results is shown in Table I.

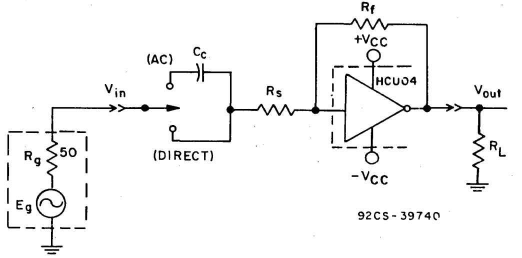


Fig. 9 - Simplified amplifier circuit configuration used to measure gain and equivalent model characteristics. Table I shows results.

Table I - Measured Amplifier-Gain Conditions for the Circuit of Fig. 9.

A. Conditions: $V_{CC} = \pm 2.5$ V, $I_{CC} \sim 6$ mA

	Measurement				
Measurement No.	**AC/Direct (input)**	**R_s (kΩ)**	**R_f (kΩ)**	**R_L (ohms)**	**V_{out}/V_{in} (gain)**
1	Direct	1	3	1000	2
2	Direct	1	3	none	2.4
3	Direct	1	3	75	0.75
4	Direct	0.5	3	75	1.0
5[1]	AC	0.05	100	75	1.4
6[2]	AC	0.05	100	none	25

Calculated: 1. $g_m \sim A/R_L \sim (1.4/75) = 0.0187$ mhos

2. $R_d \sim A/g_m \sim (25/0.0187) = 1340$ ohms

B. Conditions: $V_{CC} = \pm 3$ V, $I_{CC} \sim 10$ mA

	Measurement				
Measurement No.	**AC/Direct (input)**	**R_s (kΩ)**	**R_f (kΩ)**	**R_L (ohms)**	**V_{out}/V_{in} (gain)**
1[1]	AC	1	100	none	16
2[2]	Direct	0.5	100	75	1.5
3	Direct	1	100	75	1.45
4	AC	3	3	none	0.86

Calculated: 1. $R_d \sim A/g_m \sim (16/0.02) = 800$ ohms

2. $g_m \sim A/R_L \sim (1.5/75) = 0.02$ mhos

Operation of the HCU04 in a multiple output configuration is practical. A circuit using all six amplifiers in parallel is shown in Fig. 10. The table of gain results for a variety of conditions is shown in Table II.

OPEN-LOOP GAIN

Unlike op-amp gain, HCU04 amplifier gain is not sufficiently high or the output impedance low enough to allow simple general approximations. However, a simplified method of determining HCU04 amplifier performance in an open-loop condition is possible, and useful, in many applications. A basic open-loop equivalent-circuit model of the HCU04 is shown in Fig. 11. This circuit is based on the equivalent-current-generator model of Fig. 8 with $R_S = 0$. A large value is used for the static bias resistor, R_f, a value much larger than the input source resistance.

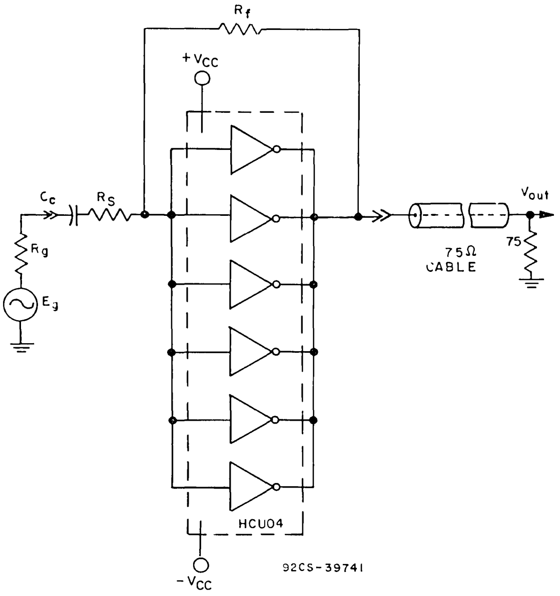


Fig. 10 - Six amplifiers of HCU04 in parallel line driver. Table II *shows results.*

Table II - Measured Results for Multiple Parallel Amplifier of Fig. 10

Conditions: $V_{CC} = \pm 2.5$ V, $I_{CC} \sim 32$ mA

Measurement No.	Measurement R_s (kΩ)	R_f (kΩ)	R_L (ohms)	V_{out}/V_{in} (gain)
1	1	1	none	0.9
2^1	1	100	none	18
3^2	0.05	100	75	6.0

Calculated: 1. $R_d \sim (A/g_m) \sim (18/0.08) = 225$ ohms

2. $g_m \sim A/R_L \sim (6/75) = 0.08$ mhos

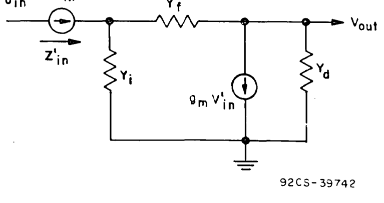


Fig. 11 - Basic equivalent circuit model for simplified gain, Z_{in} and Z_{out} calculations.

Using voltage-node equations with an assumed current drive input, J_{in}, the matrix determinant for the circuit of Fig. 11 is:

$$\Delta = \begin{vmatrix} (Y_i + Y_f) & (-Y_f) \\ (g_m - Y_f) & (Y_d + Y_f) \end{vmatrix}$$

The open-loop gain equation is:

$$A = \frac{V_{out}}{Vin'} = \frac{Y_f - g_m}{Y_d + Y_f} \sim \frac{-g_m}{Y_d + Y_f}$$

The admittance terms include frequency, f, where $\omega = 2\pi f$. The complex terms are:

$Y_f = (1/R_f) + j\omega C_f$
$Y_i = j\omega C_i$
$Y_d = (1/R_d) + j\omega C_o$

For the low-frequency case, the gain is approximately:

$A = -g_m R_d || R_f$

where $R_d || R_f$ is R_d in parallel with R_f. The R_d term may be modified to include R_d in parallel with external load R_L.

In the case where there is no external R_L and $R_d << R_f$, the gain solution simplifies to:

$A \sim -g_m R_d$

In the case where $R_L << R_d$, the gain solution simplifies to:

$A \sim -g_m R_L$

Both of these simplified expressions provide reasonably accurate values of g_m and R_d, and were used to obtain the values in Table I. As the table shows, when the gain (A) was measured as 16 times for the ± 3-volt V_{CC} condition with no load, and 1.5 times with a 75-ohm load, the solutions were readily determined to be $g_m = 0.02$ mhos and $R_d = 800$ ohms. Lower signal levels and smaller values of R_L will contribute to better accuracy.

When the admittance term $(Y_d + Y_f)$ of the gain equation is expanded, there is an output rolloff corner frequency, f_{out}, of:

$$f_{out} = \frac{1}{2\pi(C_f + C_{out})\, R_d || R_f}$$

where, again, $R_d || R_f$ is R_d in parallel in R_f.

It is important to note that the significance of this rolloff corner will depend on the degree of feedback used and the magnitude of R_g or R_s. In the true open-loop condition, where $R_s = 0$ ohms, R_f is large, and R_g is a line or generator source of 50 or 75 ohms, the f_{out} corner frequency is the primary bandwidth-limiting factor. Where capacitance C_{out} is equal to $(C_i + C_o)$, as in the case of cascaded HCU04 stages:

$C_f + C_{out} = C_f + C_i + C_o = (1.8 + 6.0 + 4.5)$ pF $= 12.3$ pF

$R_d || R_f \sim R_d \sim 800$ ohms

and

$f_{out} = 16.17$ MHz

INPUT IMPEDANCE:

The input impedance of the HCU04 may be determined by using an input driving point solution with a J_{in} current generator at the input node. The input impedance is:

$$Z_{in}' = \frac{V_{in}'}{J_{in}}$$

where:

$$V_{in}' = \frac{\begin{vmatrix} J_{in} & (Y_f) \\ 0 & (Y_d + Y_f) \end{vmatrix}}{\Delta} = \frac{J_{in}\,(Y_d + Y_f)}{\Delta}$$

Therefore:

$$Z_{in}' \ \frac{(Y_d + Y_f)}{\Delta}$$

Expanding the determinant and reordering the above equation yields:

$$Z_{in}' = \frac{1}{Y_i + Y_f(1-A)} = \frac{1}{Y_{in}'}$$

The Z_{in}' equation is a statement of all input impedances in parallel at the input. It is important to note that the $Y_f(1-A)$ is the classic Miller-effect feedback factor. Since $Y_f(1-A)$ can be expanded to $[(1-A)/R_f] + j\omega C_f(1-A)$, the effective R_{in} becomes:

$R_{in} = (1-A)/R_f$

and the effective C_{in} becomes:

$C_{in} = [(1-A)C_f + C_i]$

When the signal-source input has a high impedance (R_g or R_s), the input network configuration is equivalent to that shown in Fig. 12. The R_L network has an input corner-rolloff frequency response, f_{in}, of:

$$f_{in} = \frac{1}{2\pi(R_{in}||R_s)C_{in}}$$

where $R_{in}||R_s$ is R_{in} in parallel with R_s.

The complete input-impedance equation for the network of Fig. 12 is:

$Z_{in} = R_s + Z_{in}'$

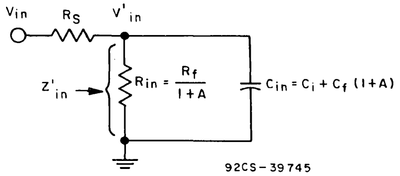


Fig. 12 - Miller-feedback equivalent input circuit of the HCU04.

OUTPUT IMPEDANCE

The output-impedance of the HCU04 may be calculated by using a current generator to drive the output terminal. The resulting calculation should include the correct input network termination.

In the open-loop condition, when R_s or R_g is much less than R_f, the output impedance is simply R_d in parallel with R_f. However, with R_s terminated through R_g at the input, the output impedance may be calculated for the general feedback condition. The second-order determinant was used for the input-impedance calculation and simply adding R_s at the input after finding Z_{in}'. The output impedance can be calculated similarly, using the second order determinant, by including the Y_s admittance term (or $Y_s + Y_g$) in the y11 term of the matrix determinant; i.e.:

$$\Delta = \begin{vmatrix} (Y_s + Y_i + Y_f) & (-Y_f) \\ (g_m - Y_f) & (Y_f + Y_d) \end{vmatrix}$$

When the output node is driven by a current (J_o):

$$V_{out} = J_o(y11/\Delta)$$

and

$$Z_{out} = \frac{Y_s + Y_i + Y_f}{(Y_d + Y_f)[Y_s + Y_i + Y_f(1 - A)]}$$

This equation may be reduced to a simple form for low frequencies:

$$Z_{out} = \frac{R_d || R_f}{1 - A(R_s/(R_s + R_f))}$$

where $R_d || R_f$ is R_d in parallel with R_f.

FEEDBACK EQUATIONS AND GAIN-BANDWIDTH-CIRCUIT MEASUREMENTS

The preceding equations will be very useful in applying the HCU04, particularly in low-frequency applications. However, it is important that the user does not over-simplify solutions and drop terms before evaluating their significance. The general purpose of this Note is to provide fully useful equations and to impress on the user that the standard op-amp equations, for the most part, do not apply well to the HCU04 amplifier.

Because some degree of feedback is desired for good linearity, the need to consider performance with feedback is necessary. An essential consideration is the wideband amplifier performance. The gain-bandwidth response and phase considerations are important, and are treated, with examples, in the following section.

The use of the equations developed above and the gain-bandwidth (GBW) capability of the HCU04 are demonstrated with the aid of Fig. 13. Shown is a single amplifier of the HCU04 in which bypassed 75-ohm resistors are used as protection from power-supply over-voltage. The small-signal equivalent circuit is similar in characteristics to the last example in Table I, except for the power-supply resistors. The g_m and R_d values for that example were determined to be 0.02 mhos and 800 ohms, respectively, and are the values used in the following evaluation.

As noted above, the low-frequency gain may be approximated from the op-amp feedback equation:

$$A_{fb} = \frac{A_{ol}}{1 + (R_s/R_f)(1 - A_{ol})}$$

where:

$$A_{ol} \sim -g_m R_d = -16$$

And for $R_s = R_f = 3000$ ohms, $A_{fb} = -0.88 = -1.11$ dB

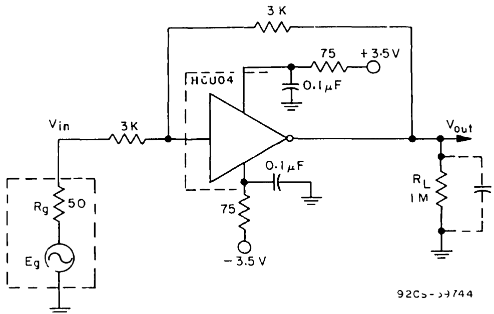


Fig. 13 - Amplifier circuit for gain-bandwidth measurements.

This value is in good agreement with the measured gain-bandwidth (GBW) response curve shown in Fig. 14. In addition, as noted above, the high-frequency GBW response includes the input corner-rolloff frequency resulting from the Miller-effect RC input network of Fig. 12.

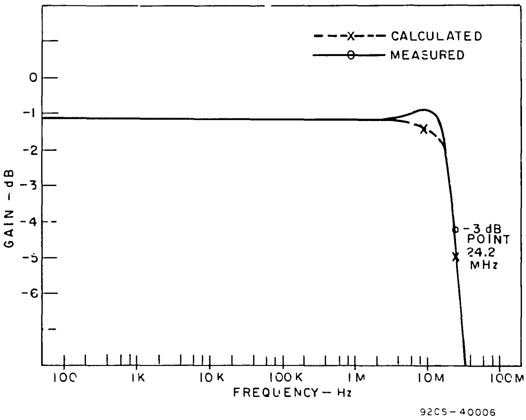


Fig. 14 - Gain-bandwidth measurement showing frequency rolloff response for the circuit of Fig. 13.

The full, high-frequency-gain equation, derived from the third-order determinant, will include both the input and output corner-rolloff frequencies. The matrix determinant is:

$$\Delta = \begin{vmatrix} (Y_s) & (-Y_s) & (0) \\ (-Y_s) & (Y_s + Y_i + Y_f) & (-Y_f) \\ (0) & (-y_f + g_m) & (Y_f + Y_d) \end{vmatrix}$$

and the gain equation is:

$$A_{fb} = \frac{-Y_s\,(g_m - Y_f)}{(Y_f + Y_d)\,(Y_s + Y_i + Y_f(g_m + Y_d)}$$

While this equation may be awkward to use, all of its terms are needed to evaluate stray capacity (C_s) and other loading effects in the application. Normally, g_m is much greater than Y_f, so that $g_m - Y_f \sim g_m$.

The gain equation then reduces to the form:

$$A_{fb} = \frac{A_x}{1 + j\omega B_x - \omega^2 C_x} \qquad (1)$$

Where A_x is the low-frequency gain, and the complex demoninator is the complete factor for gain and phase response versus frequency. The A_x, B_x and C_x terms are defined as follows:

$$A_x = \frac{-g_m R_d}{(1+R_d/R_f) + (R_s/R_f)\,(1 + g_m R_d)}$$

$$B_x = -(A_x/g_m R_d)[(C_o+C_f)R_d + [(C_i+C_o)R_s R_d/R_f] + (C_i+C_f)R_s + g_m C_f R_s R_d]$$

$$C_x = -(A_x/g_m R_d)[R_s R_d(C_f C_i + C_o C_i + C_o C_f)]$$

Using parameter values already defined from the circuits of Figs 6 and 13:

$$A_x = \frac{-0.02 \times 800}{(1 + 800/3000) + (3000/3000)\,(1 + 0.02 \times 800)} = -0.876$$

Before calculating the frequency dependent B_x and C_x terms, it is important to note the special conditions for phase shift. Equating the real term of the denominator of equation 1 to zero yields:

$$\omega^2 C_x = 1$$

The gain equation under this special condition is:

$$A_f b = \frac{A_x}{j\omega B_x}$$

The fact that there is only an imaginary (complex) term in the denominator is a statement of 90° phase lag, which is a defined measurement point on the phase curve of Fig. 15.

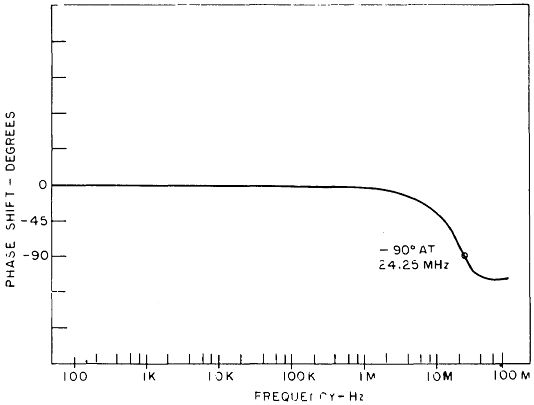


Fig. 15 - Phase measurement showing phase shift for the circuit of Fig. 13.

The capacitance output term for the 90° phase shift is:

$$C_o = \frac{-(g_m/\omega^2 A_x R_s) - C_f C_i}{(C_f + C_i)}$$

Substituting values for the 24.2 MHz point noted on Fig. 15, a phase shift of 90° yields:

$$C_o = 40.5 \text{ pF}$$

The capacitance output term C_o includes all stray capacitance plus the HCU04 equivalent output capacitance of 4.5 pF. The stray and fixturing capacitance, C_s, is:

$$C_s = (40.5 - 4.5) = 36 \text{ pF}$$

To evaluate A_{fb} for this condition, the B_x and C_x values are calculated as follows (using $g_m R_d = (0.02)(800) = 16$, and noting that C in pF times R in kilohms carriers a 10-9 multipler):

$$B_x = -(A_x/g_m R_d)\,[(C_o + C_f)R_d + (C_i + C_o)(R_s/R_f)R_d + (C_i + C_f)R_s + g_m R_d C_f R_s]$$

$$= -(-0.876/16)[40.5 + 1.8)(0.8) + (6.0 + 40.5)(3/3)(0.8) + (6.0 + 1.8)(3) + 16(1.8)3] \times 10^{-9}$$

$$= 9.9 \times 10^{-9}$$

$$C_x = -(A_x/g_m R_d)[(R_s R_d)][(C_f C_i + C_o C_i + C_o C_f)]$$

$$= -\,(-0.876/16[(3)(0.8)][(1.8)(6.0)+(40.5)(6.0)+(40.5\,(1.8)]10^{-18}$$

$$= 42.93 \times 10^{-18}$$

Verifying that $\omega^2 C_x = 1$:

$$\omega^2 C_x = (2\pi f)^2 C_x = (2\pi)^2(24.2 \times 10^6)^2(42.93 \times 10^{-18}) \sim 1$$

Then A_{fb} at 90° is:

$$A_{fb} = A_x/j\omega B_x = (-0.876)/j(2\pi)(24.2 \times 10^6)(9.9 \times 10^{-9})$$

$$= (-0.876/j1.5) = -0.584\angle{-90°}$$

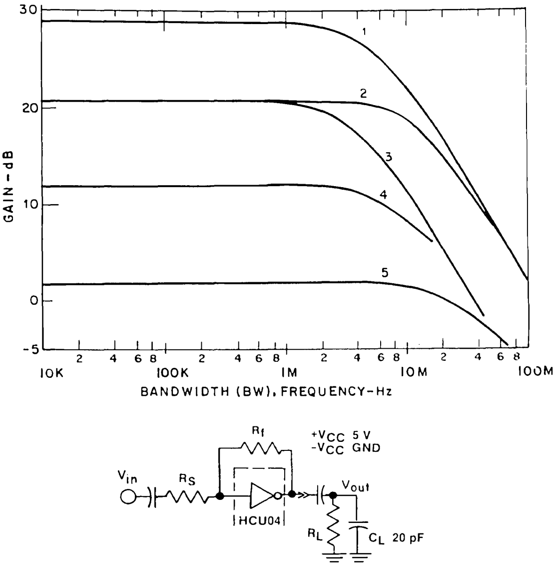
The magnitude of the gain in dB at 90° phase lag is:

$$A_{fb} = 20 \log|0.584| = -4.67 \text{ dB}$$

The actual measured results from the curve of Fig. 14 shows -4.3dB, which verifies, with practical agreement, the actual and calculated results. Using the complex A_{fb} equation to verify the gain at 10 MHz, the results of the gain calculation are -1.47 dB at -40.17° of phase lag.

The slight peaking noted at 10 MHz is not unusual in wideband circuits with feedback. In the range of 10 MHz and beyond, peaking or ripple effects are commonly present in the GBW response because of lead inductance and stray capacitance both in the signal links and in the filtering components. Care must be exercised in circuit layout and in component specification, as an excess of peaking will cause undesired overshoots and ringing on pulse edges.

Additional gain-bandwidth curves are shown in Fig. 16. Note that the high frequency rolloff is a function of load and feedback, but is typically 6-dB per octave. The bandwidth can be extended at a sacrifice of gain. Bandwidth extending may be done with loading or peaking. Both RC and RLC can be used to peak the input signal.



CURVE	RS	Rf	RL
1	0	1M	∞
2	0	1M	1K
3	1K	1M	1K
4	1K	7.5K	1K
5	250	1.5K	75

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Fig. 16 - Linear-amplifier gain/bandwidth curves.

GENERAL APPLICATIONS OF THE 74HCU04

The low output impedance and video-bandwidth capability of the HCU04 suggest a wide variety of applications in linear signal amplifiers. Line-driver capability may be achieved by paralleling output amplifiers and applying feedback to assure low output impedance. The HCU04 may be used for both linear and digital data transfer. Real-time feedback conditions may be modified by using transmission-gate switching with such devices as the QMOS CD74HC4016 or CD74HC4052.

Video Switch

An example of a video-switching video-amplifier is shown in Fig. 17. The CD74HC4052 is a QMOS dual 4-input analog multiplex switch that is used to direct one of four inputs to the HCU04 video amplifier. An LED indicator shows which channel has been selected. One amplifier of the HCU04 is used as a buffer amplifier that drives four other amplifiers in parallel. These four amplifiers, in turn, drive a 75-ohm cable and load.

QMOS CD74HC4052 CD74HCU04 VIDEO SWITCH CIRCUIT

- DUAL 4 TO 1 SWITCH WITH VIDEO AT ONE OUTPUT & LED INDICATOR AT PAIRED OUTPUT
- CD74HC4052 TRANSMISSION GATE SWITCH
- CD74HCU04 UNBUFFERED HEX INVERTER
  - ONE BUFFER AMP. WITH 2X GAIN
  - 4 PARALLELED AMP. TO DRIVE 75 Ω LINE

TYPICAL DATA

- B.W. (-3 dB) 50 MHz
- FEEDTHROUGH -57 dB
- CROSSTALK -66 dB
- NOISE -66 dB
- DIFF. GAIN 2% @ 0.8 Vpp
- DIFF. PHASE 0.75 @ 0.8 Vpp
- I_{DD} 20 mA
- GAIN 2X

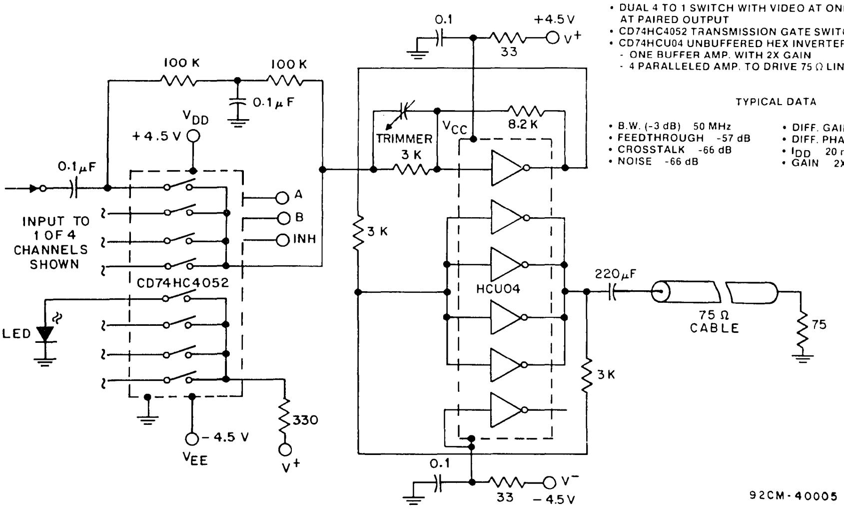


Fig. 17 - Video-switch circuit employing QMOS CD74HC4052 and HCU04.

Bandwidth peaking is accomplished in the first video amplifier by the trimmer capacitor. One amplifier remains open for use as a parallel-signal amplifier, e.g., for audio signals. However, any unused amplifier should have the input returned to V^+ (V_{CC}) or V^- (GND) to eliminate current drain. The peaking circuits provide for an exceptional 50-MHz gain-bandwidth capability at 2X gain. Other typical data is shown in the table accompanying the figure.

Audio/Tone Amplifier

The circuit of Fig. 18 is an audio or tone driver for high-efficiency, 32-ohm speakers or a headset. Although the power output is limited by the 5-volt supply, the use of the HCU04 as a tone amplifier or beeper is practical with this type of circuit.

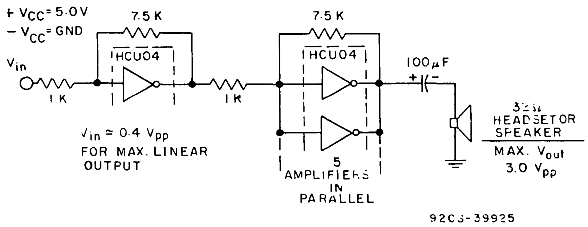


Fig. 18 - Audio/tone amplifier.

Other Linear Applications

The circuits of Fig. 19(a) through 19(h) are general applications of the HCU04 in both the linear and switching modes. With 25 mA of drive capability, the HCU04 amplifier can directly drive LED indicators or provide high-current base drive for a transistor lamp, solenoid, or relay driver, as shown in Figs. 19a and 19b.

Fig. 19(c) shows a possible use of the HCU04 with photocells or thermistors in a sensor amplifier application for light or heat control.

The circuit of Fig. 19(d) shows an HCU04 driving a TTL 2-input NAND gate. This circuit is employed where a TTL interface is needed.

Fig. 19(e), the simplest form of a low-pass filter, shows a capacitor-feedback arrangement in use with the HCU04 amplifier. Additional poles may be added with additional filter stages. In the example shown, the gain is unity and the 3-dB rolloff frequency is 5 kHz.

An emitter-follower may be coupled to the output and included in the feedback loop of the HCU04 amplifier, as shown in Fig. 19(f). The use of positive and negative power-supply voltages is optional. As another option, the output may be changed to a complementary-symmetry drive. With the emitter follower shown, the base-emitter offset of 0.7 volts reduces the linear dynamic range of the output drive signal.

The circuit of Fig. 19(g) is an adjustable current sink in which the current, I_c, in the output transistor, is approximately equal to 2.5/R. Fig. 19(h) shows a more general circuit for adjusting both voltage and current.

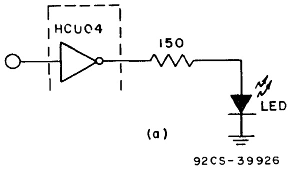


Fig. 19 - (a) LED driver.
Note: For circuits (a) through (e), $+V_{CC}$ = 5 V, $-V_{CC}$ = ground.

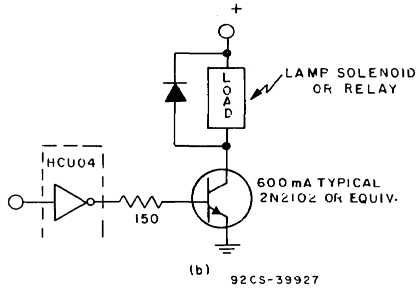


Fig. 19 - (b) Lamp, solenoid, or relay driver.

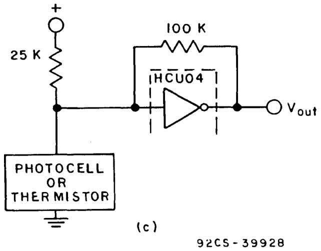


Fig. 19 - (c) Photocell or thermistor driver.

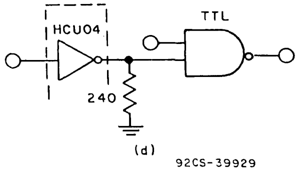


Fig. 19 - (d) TTL driver.

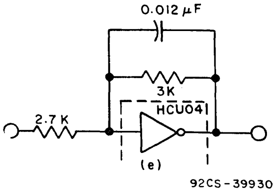


Fig. 19 - (e) Unity gain low-pass filter: 3-dB rolloff ~ 5 kHz.

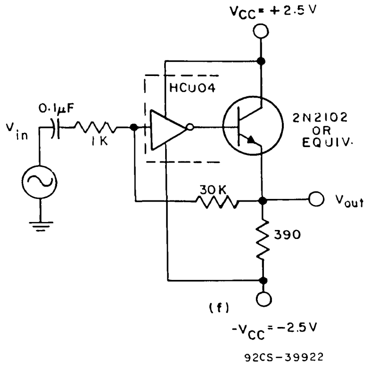


Fig. 19 - (f) Low Z_{OUT} amplifier.

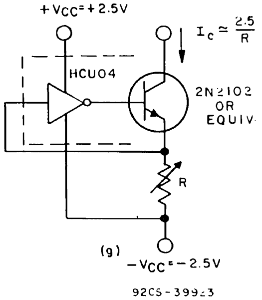


Fig. 19 - (g) Fixed-current-source driver.

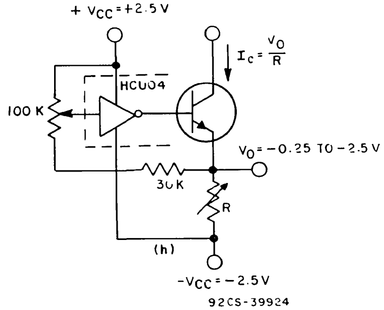


Fig. 19 - (h) Adjustable low-Z$_{OUT}$ dc source or adjustable current sink.

Oscillator Applications

The circuit of Fig. 20(a) is a 3.58 MHz clock generator that may be VCO controlled by replacing the 10 pF capacitor with a varactor.

Uniformity of balance in the HCU04 leads to better frequency-range control in applications where the frequency is crossover dependent. The circuit of Fig. 20(b) can be changed in polarity of pulse and ramp output by changing the polarity of the 1N914 diode. The result is a -2V to +2V adjustable VCO with positive ramp and pulse outputs in the low switch position. In the high position, negative ramp and pulses are generated with a 2.6 V to 7 V control voltage. In both switch positions, the frequency range is 15 kHz to 180 kHz.

The VCO circuits of Figs. 20(c) and 20(d) are simpler, higher-frequency-range circuits with oscillator capability up to 25 MHz. The circuit of Fig. 20(d) shows a method of compensating effects of power-supply frequency change by adding some of the VCO change into the VCO input. At a center frequency of 5 MHz, for V_{in} = 0 V, the power-supply change is effectively cancelled for changes of ±10% V_{CC}.

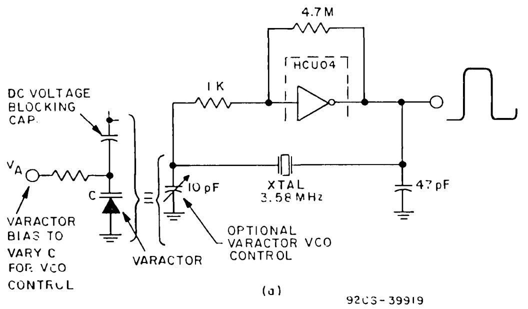
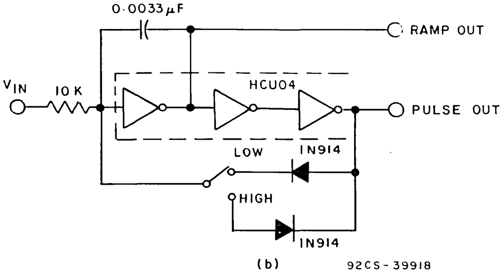
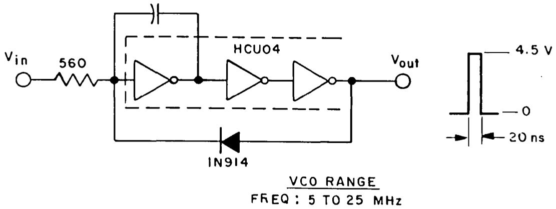


Fig. 20 - (a) 3.58-MHz clock or VCO circuit.
Note: For all Fig. 20 circuits, +V_{CC} = 5 V, -V_{CC} = ground.



POSITIVE RAMP AND PULSE	LOW ADJ RANGE 110 KHz AT 0 V V_{IN}: -2 TO 2 V FREQ: 180 KHz TO 15 KHz
NEGATIVE RAMP AND PULSE	HIGH ADJ RANGE 100 KHz AT 5 V V_{IN}: 2.6 V TO 7 V FREQ: 15 KHz TO 180 KHz

Fig. 20 - (b) VCO pulse and ramp generator.



VCO RANGE
FREQ : 5 TO 25 MHz
V_{in} : 2.5 TO 6 V
(c) 92CS-39920

Fig. 20 - (c) High-frequency VCO pulse generator.

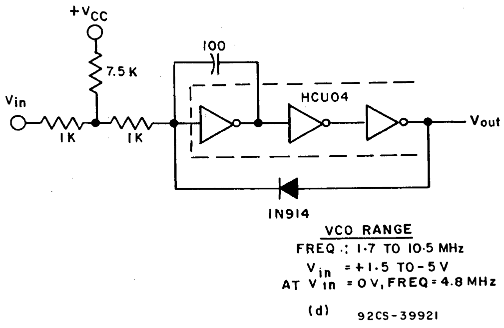


Fig. 20 - (d) V_{CC} -compensated VCO.

SUMMARY

The characterization and applications of the HCU04 shown illustrate how simple, high-speed CMOS device can be more widely used in both linear and digital circuits. Many applications require linear interface for buffer amplifiers, sensors, gain amplifiers, and multiple-line inverter circuits.

The power gain of the HCU04 is very high, although the voltage gain is typically less than 20. This feature makes the HCU04 an excellent driver for bipolar transistors driving lamps, relays, and solenoids.

REFERENCES

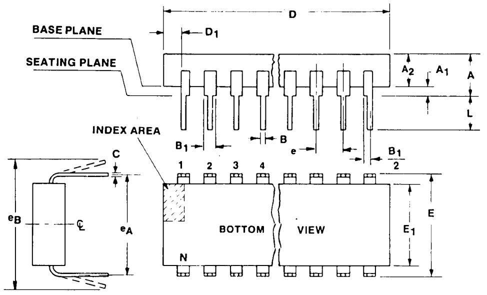
1. "CD54/74HCU04, Hex Inverter Data Sheet; RCA Solid State File No. 1655. The notation CD54/74HCU04 denotes two devices, the CD54HCU04F, the Hex Inverter in a ceramic package, and the CD74HCU04E, the Hex Inverter in a plastic package. Both devices are electrically identical. The notation HCU04 used in this Note refers to either device.

ACKNOWLEDGMENTS

Substantial portions of the gain-bandwidth technical characterization and related circuits in this Note were provided by J. Nadolski; HCU04 device-parameter information was provided by B. Petryna and R. Funk.

Dimensional Outlines

Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $$1, N, \frac{N}{2}, \frac{N}{2}+1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

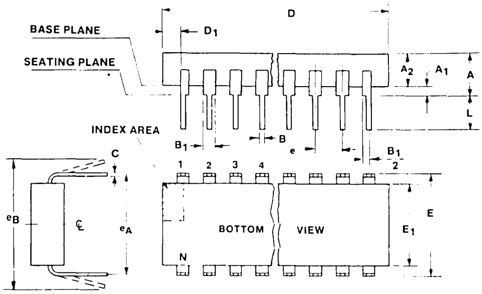
92CS-39900

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

Dual-In-Line Plastic Packages



(EN) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions $$1, N, \frac{N}{2}\ \frac{N}{2}+1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-011-AA)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.150	1.290	29.3	32.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	24		24		11

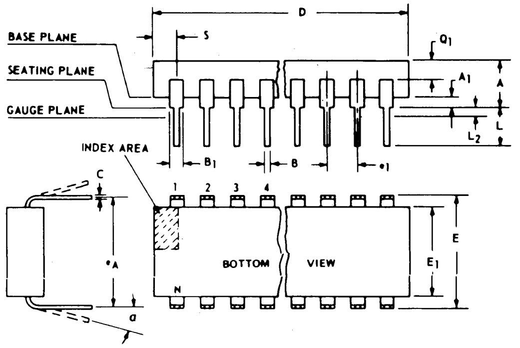
92CS-40000

(E) Suffix (JEDEC MS-011-AB)
28-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.1	39.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	28		28		11

92CS-40001

Dual-In-Line Frit-Seal Ceramic (CERDIP) Packages



NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).
2. Leads within 0.005 in. (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
3. e_A applies in zone L_2 when unit is installed.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(F) Suffix (JEDEC MO-001-AB)
14-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.065	0.090	1.66	2.28	

92SS-4296R3

(F) Suffix (JEDEC MO-001-AC)
16-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

92CM-15967R4

(F) Suffix
20-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.250	3.10	6.30	
A_1	0.020	0.070	0.51	1.77	
B	0.016	0.020	0.407	0.508	
B_1	0.028	0.070	0.72	1.77	
C	0.008	0.012	0.204	0.304	1
D	0.942	0.990	23.93	25.15	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.100	0.200	2.54	5.00	
L_2	0.000	0.030	0.00	0.76	
α	0°C	15°C	0°C	15°C	4
N	20		20		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.040	0.100	1.02	2.54	

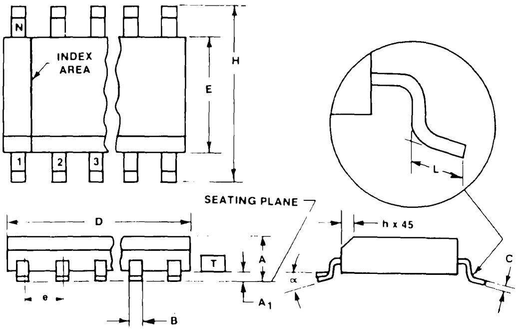
92CM-35137R1

(F) Suffix (JEDEC MO-015-AA)
24-Lead Dual-In-Line Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.250	3.10	6.30	
A_1	0.020	0.070	0.51	1.77	
B	0.016	0.020	0.407	0.508	
B_1	0.028	0.070	0.72	1.77	
C	0.008	0.012	0.204	0.304	1
D	1.200	1.290	30.48	32.76	
E	0.600	0.625	15.24	15.87	
E_1	0.515	0.580	13.09	14.73	
e_1	0.100 TP		2.54 TP		2
e_A	0.600 TP		15.24 TP		2,3
L	0.100	0.200	2.54	5.00	
L_2	0.000	0.030	0.00	0.76	
α	0°C	15°C	0°C	15°C	4
N	24		24		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.040	0.100	1.02	2.54	

92CS-26938R3

Dual-In-Line Surface Mount Plastic Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

(M) Suffix (JEDEC MS-012-AB)
14-Lead Dual-In-Line Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38924R1

(M) Suffix (JEDEC-MS-012-AC)
16-Lead Dual-In-Line Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38925R1

(M) Suffix (JEDEC-MS-013-AC)
20-Lead Dual-In-Line Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38926R1

(M) Suffix (JEDEC MS-013-AD)
24-Lead Dual-In-Line Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39037R1

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