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Rockwell

PARALLEL PROCESSING SYSTEM (PPS)

DATA SHEET

PPS-8 CENTRAL PROCESSOR UNIT (CPU)

INTRODUCTION

The PPS-8 Central Processor Unit, Part No. 11806, is a complete 8-bit parallel processor implemented on a single MOS chip. The Central Processor Unit (CPU) uses four-phase dynamic logic for operation.

The CPU contains:

(a) Logic necessary to receive and decode the instructions

(b) 8-bit parallel adder-accumulator for arithmetic and logical operations

(c) 14-bit P-Register for sequencing through the ROM program

(d) 16-bit L-Register for subroutine linkage, RAM operand addressing, and ROM indirect addressing

(e) Three 8-bit registers, (X, Y and Z) for RAM operand addressing

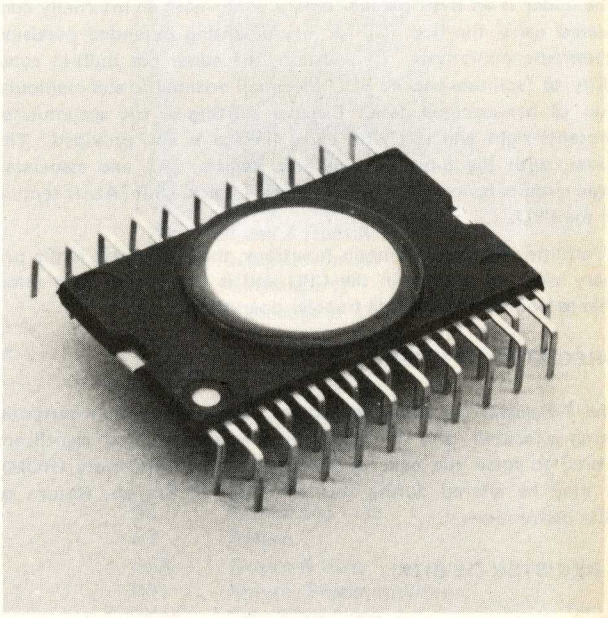
(f) 5-bit stack pointer S for addressing a dedicated RAM area

(g) Logic for processing a priority interrupt structure

(h) Direct memory access (DMA) mode

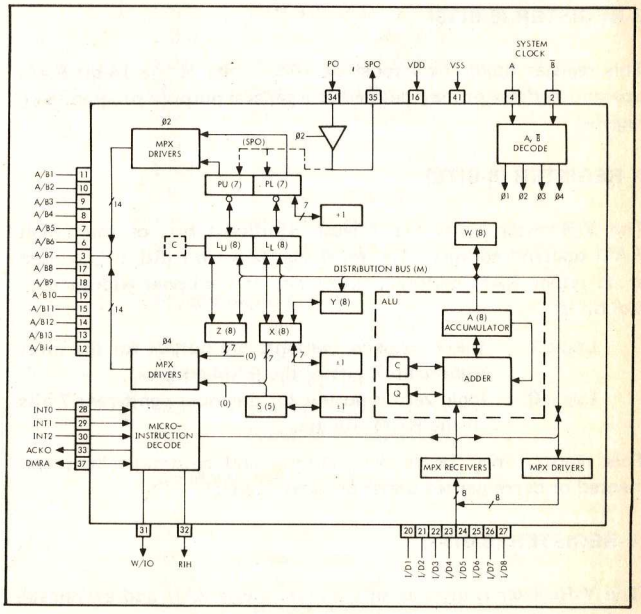
(i) Multiplexed receivers and drivers for interfacing with the 14-bit multiplexed address bus and the 8-bit bi-directional data/instruction bus.

The CPU, through time multiplexing, utilizes an 8-bit bi-directional bus to transfer instructions from ROM to CPU (and I/O) during 04, and to transfer data between the CPU, RAMs and I/O devices during 02.



FEATURES

- Two Microsecond Access Time
- Four Microsecond Complete Instruction Cycle Time
- Over 90 Words Instruction Repertoire
- DMA Up to 8 Prioritized Channels at 256K Bytes/Sec
- Program Controller I/O at 60K Bytes/Sec
- TTL-Compatible Interface
- Three Level Interrupt Structure
- Bi-directional 8- or 16-Bit Parallel Buses
- Single 42-Pin Package



PPS-8 CPU Block Diagram (P/N 11806)

NOTE

The PPS-8 CPU P/N 11806 is functionally identical to the PPS-8 CPU P/N 10806. The pin configuration is entirely different. All new PPS-8 CPU designs should be planned for P/N 11806 chips. Replace Document No. 29000 D04, dated December 1975, with this data sheet.

FUNCTIONAL DESCRIPTION

INSTRUCTION DECODE

The decode portion of the chip contains logic to decode the instructions, sense interrupt or DMA requests, and control data transfer, arithmetic, logical, and indexing operations. Instructions are either one, two, or three bytes in length and require from one to three clock cycles for execution, (one cycle per byte).

ACCUMULATOR REGISTER AND ARITHMETIC LOGIC UNIT (ALU)

The adder is an 8-bit parallel binary adder with an internally connected carry flip-flop (C) for implementing extended precision arithmetic operations. In addition, the adder has built-in capability to facilitate packed BCD (decimal) arithmetic and manipulation of hexadecimal data. Circular shifting of the accumulator contents right and left with carry linkage is also provided. The adder, with the 8-bit Accumulator Register (A), and associated logic circuits forms the Arithmetic and Logical Unit (ALU) section of the CPU.

In addition to its arithmetic functions, the A-Register is the primary working register in the CPU and is the central data interchange point for most data transfer operations.

P-REGISTER (14 BITS)

The P-Register contains the address of the instruction currently being executed, and automatically increments (least significant 7-bits) to fetch the next byte from instruction memory (ROM). It may be altered during the execution of Branch, Return or Skip instructions.

L-REGISTER (16-BITS)

The L-Register is used to save the return address after a subroutine call or an interrupt. It is also used as an address register for indirect ROM operands. It can also be used as an alternate RAM address register or as a general purpose programming register.

Z-REGISTER (8-BITS)

This register holds the 7 most significant bits of the 14-bit RAM operand address or may be used as a general purpose programming register.

X-REGISTER (8-BITS)

The X-Register holds the 7 least significant bits of the 14-bit RAM operand address. The most significant bit (8th bit) is used as an upper RAM address control bit. If the upper address control bit is:

Logic 1 — the Z-Register contents are output for the most significant 7 bits of the RAM address.

Logic 0 — logic zero is output for the most significant 7 bits of the RAM address.

This register may be loaded, stored, and automatically incremented or decremented under program control.

Y-REGISTER (8-BITS)

The Y-Register is used as an alternate lower RAM address register and as a "loop counter" or it may be used as a general purpose programming register.

S-REGISTER (5-BITS)

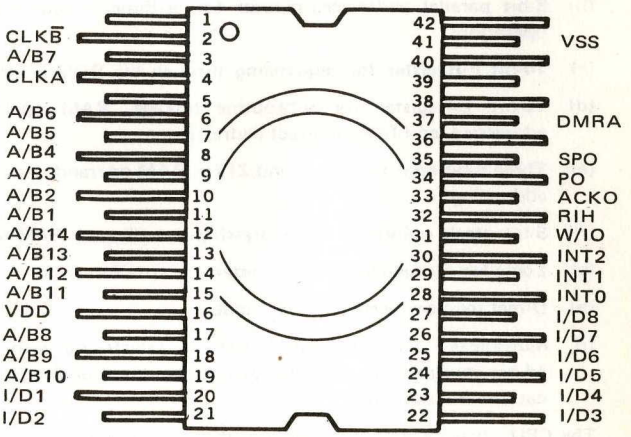
The 5-bit up-down counter S-Register is used as an address pointer to a 32 byte "stack" in RAM. This stack pointer is automatically incremented each time a byte is "pushed" into the stack and decremented each time a byte is "popped" from the stack.

W-REGISTER (8-BITS)

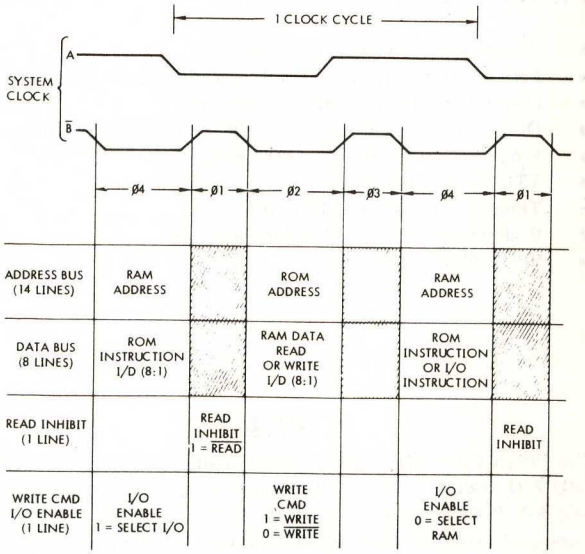
The W-Register serves primarily as an internal buffer register. Additionally, it is used in conjunction with the LAL and PSHL instructions.

POWER-ON RESET (PO)

The Power-On input signal is used to initialize the CPU to a known starting address and state during a power-on sequence. The Power-On (PO) signal is generated external to the CPU. The CPU receives this signal, initializes the internal logic states, and at the same time, generates a Synchronized Power-On output (SPO) signal which is used to initialize other circuits of the PPS-8



PPS-8 CPU Pin Configurations (P/N 11806)



PPS-8 Bus Timing Basic

PPS-8 INSTRUCTION SET LIST

Data Transfer Group

L	Load A
LN	Load A, Increment Address
LD	Load A, Decrement Address
LNXL	Load A, Increment Address, Exchange L
LDXL	Load A, Decrement Address, Exchange L
LNCX	Load A, Increment & Compare Address, Exchange L
LDCX	Load A, Decrement & Compare Address, Exchange L
LNXY	Load A, Increment Address, Exchange Y
S	Store A
SN	Store A, Increment Address
SD	Store A, Decrement Address
SNXL	Store A, Increment Address, Exchange L
SDXL	Store A, Decrement Address, Exchange L
SNCX	Store A, Increment & Compare Address, Exchange L
SDCX	Store A, Decrement & Compare Address, Exchange L
SNXY	Store A, Increment Address, Exchange Y
X	Exchange
XN	Exchange, Increment Address
XD	Exchange, Decrement Address
XNXL	Exchange, Increment Address, Exchange L
XDXL	Exchange, Decrement Address, Exchange L
XNCX	Exchange, Increment & Compare Address, Exchange L
XDCX	Exchange, Decrement & Compare Address, Exchange L
XNXY	Exchange, Increment Address, Exchange Y

Stack Group

PSHA	Push A
PSHX	Push X
PSHY	Push Y
PSHZ	Push Z
PSHL	Push L
POPA	Pop A
POPX	Pop X
POPY	Pop Y
POPZ	Pop Z
POPL	Pop L

Arithmetic Group

A	Add
AC	Add with Carry
ASK	Add, Skip on Carry
ACSK	Add with Carry, Skip on Carry
AISK	Add Immediate, Skip on Carry
INCA	Increment A
DC	Decimal Correct (1)
DCC	Decimal Correct (2)

Logical Group

AN	Logical AND
ANI	Logical AND Immediate
OR	Logical OR
EOR	Logical Exclusive OR
COM	Complement

Increment/Decrement Group

INCX	Increment X
DECX	Decrement X
INXY	Increment X, Exchange Y
DEXY	Decrement X, Exchange Y
INCY	Increment Y
DECY	Decrement Y

Skip/Branch Group

B	Branch
BDI	Branch, Disable Interrupts
NOP	No Operation
SKC	Skip if Carry

Register Group

LX	Load X
LY	Load Y
LZ	Load Z
LAI	Load A Immediate
LXI	Load X Immediate
LYI	Load Y Immediate
LZI	Load Z Immediate
LAL	Load A through Link
LXL	Load X through Link
LYL	Load Y through Link
LZL	Load Z through Link
LXA	Load X from A
LYA	Load Y from A
LZA	Load Z from A
LLA	Load L from A
XY	Exchange Y
XL	Exchange L
XAX	Exchange A and X
XAY	Exchange A and Y
XAZ	Exchange A and Z
XAL	Exchange A and L

Subroutine Group

BL	Branch and Link
RT	Return
RSK	Return & Skip
RTI	Return, Enable Interrupts
SKNC	Skip if No Carry
SKZ	Skip if Zero
SKNZ	Skip if Non-Zero
SKP	Skip if Positive
SKN	Skip if Negative
SKE	Skif if Equal
BBT	Branch if Bit (n) True
BBF	Branch if Bit (n) False
BC	Branch if Carry
BNC	Branch if No Carry
BZ	Branch if Zero
BNZ	Branch if Non-Zero
BP	Branch if Positive
BN	Branch if Negative
BNE	Branch if Not Equal

Input/Output Group

IO4	Digit I/O (C, D)
IN	Input (C, D)
OUT	Output (C,D)
RIS	Read Interrupt Status

Bit Manipulation Group

SC	Set Carry
RC	Reset Carry
RAR	Rotate A Right
RAL	Rotate A Left
MDR	Move Digit Right
MDL	Move Digit Left
SB	Set Bit (n)
RB	Reset Bit (n)

SPECIFICATIONS

OPERATING CHARACTERISTICS

Supply Voltage:

VDD = -17 Volts ±5%
(Logic "1" = most negative voltage V_{IL} and V_{OL}.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage V_{IH} and V_{OH}.)

System Operating Frequencies:

199 kHz or 256 kHz.

Device Power Consumption:

600 mw

Input Capacitance:

<5 pf

Input Leakage:

<10 ua

Operating Temperature (TA):

0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

$|VDD-VSS|$ = 27 volts maximum.

Input Voltage with respect to VSS
-27 volts maximum.

Maximum positive voltage on any pin +0.3 volts.

FUNCTION		SYMBOL	LIMITS (VSS = 0V) MIN	TYP	MAX	LIMITS (VSS = +5V) MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Current (Average)		I_{DD}		26	35		26	35	mA	VDD = -17.85V VSS = 0V F = 256 kHz T_A = 25°C
Input and Output Characteristics — System Bus										VDD = -17V ±5% VSS = 0V
I/D_{1-8} DMRA		V_{IH} V_{IL}	-1.5 -6.5		+0.3 -17.85	+3.5 -1.5		+5.3 -12.85	V V	
	A/B_{1-14}, W/IO, RIH, ACKO	V_{OH} V_{OL}	-1.0 -7.5		+0.3 -17.85	+4.0 -2.5		+5.3 -12.85	V V	
INT_0, INT_1		V_{IH} V_{IL}	-1.5 -4.2		+0.3 -17.85	+3.5 +0.8		+5.3 -12.85	V V	
INT_2		V_{IH} V_{IL}	-1.5 -6.5		+0.3 -17.85	+3.5 -1.5		+5.3 -12.85	V V	OR
SPO		V_{OH} V_{OL}	-0.5 -8.5		+0.3 -17.85	+4.5 -3.5		+5.3 -12.85	V V	
CLKA $CLK\overline{B}$		V_{IH} V_{IL}	-0.5 -10.0		+0.3 -17.85	+4.5 -5.0		+5.3 -12.85	V V	
Input and Output Characteristics — External Interface										
PO		V_{IH} V_{IL}	-2.5 -13.0		+0.3 -17.85	+2.5 -8.0		+5.3 -12.85	V V	VDD = -12V ±5% VSS = +5V ±5%

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