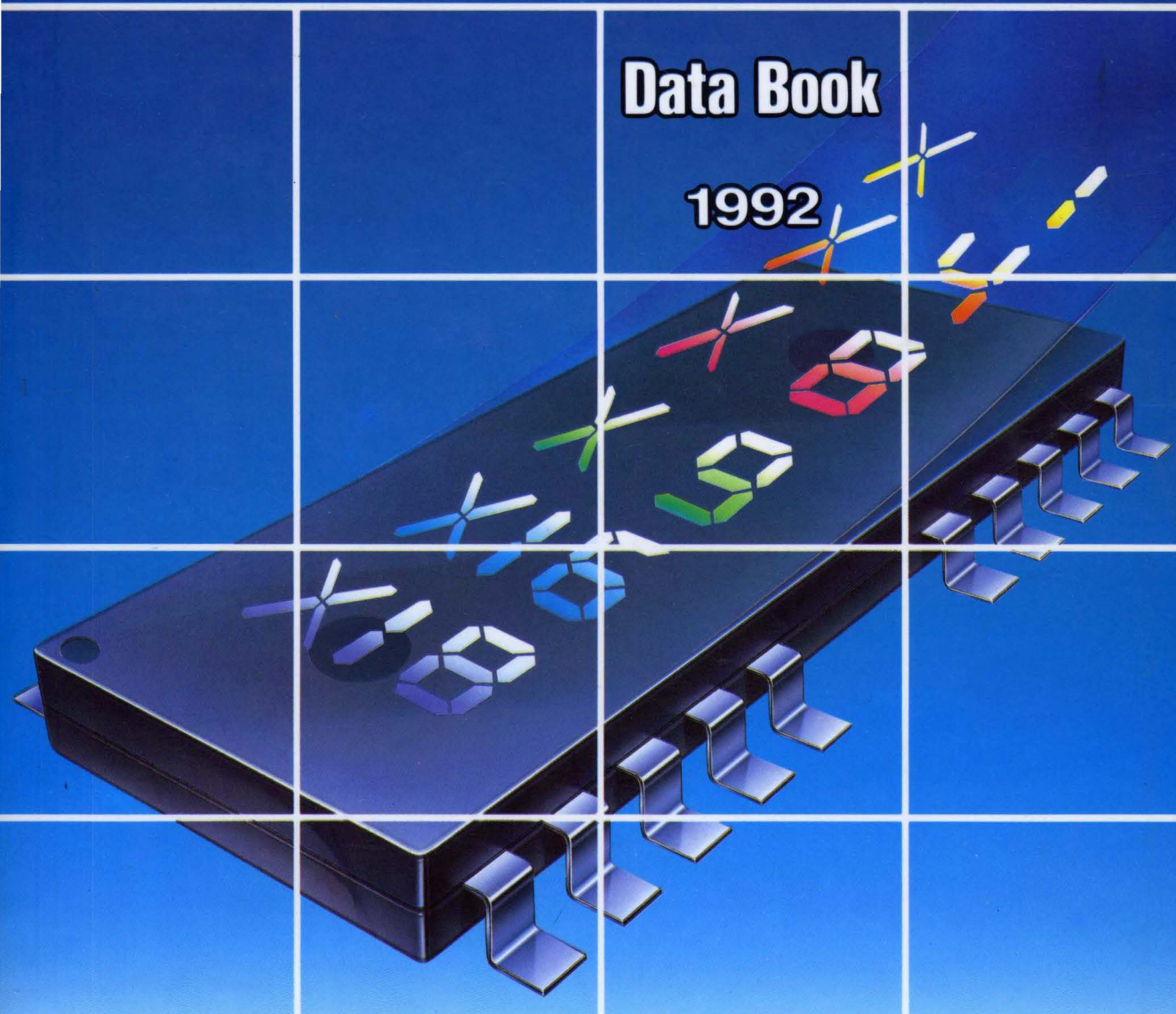
4M DRAM

Data Book

1992



SAMSUNG

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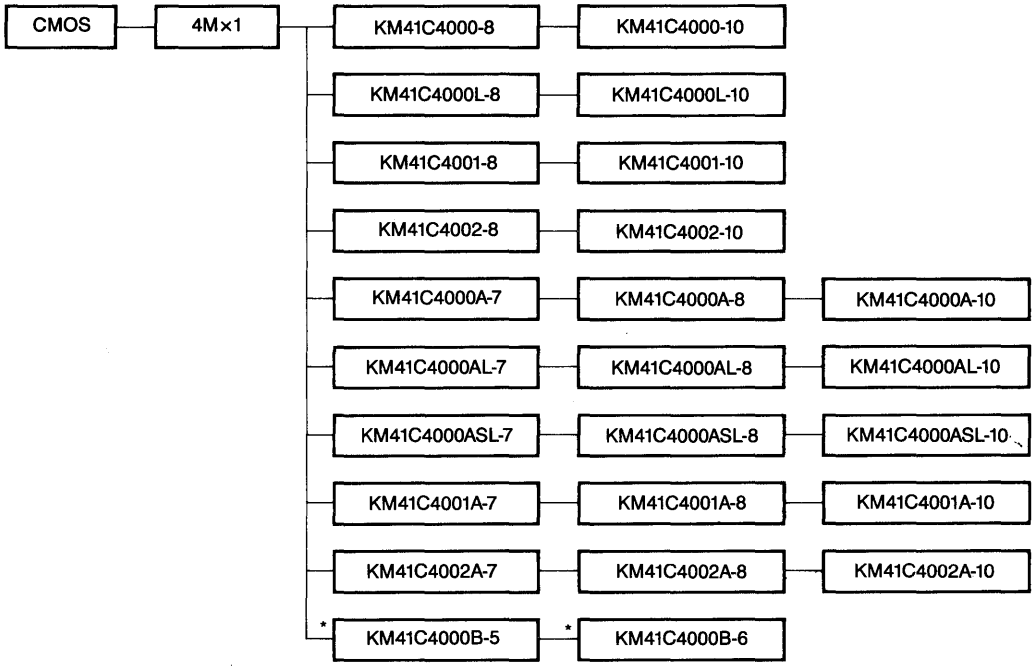
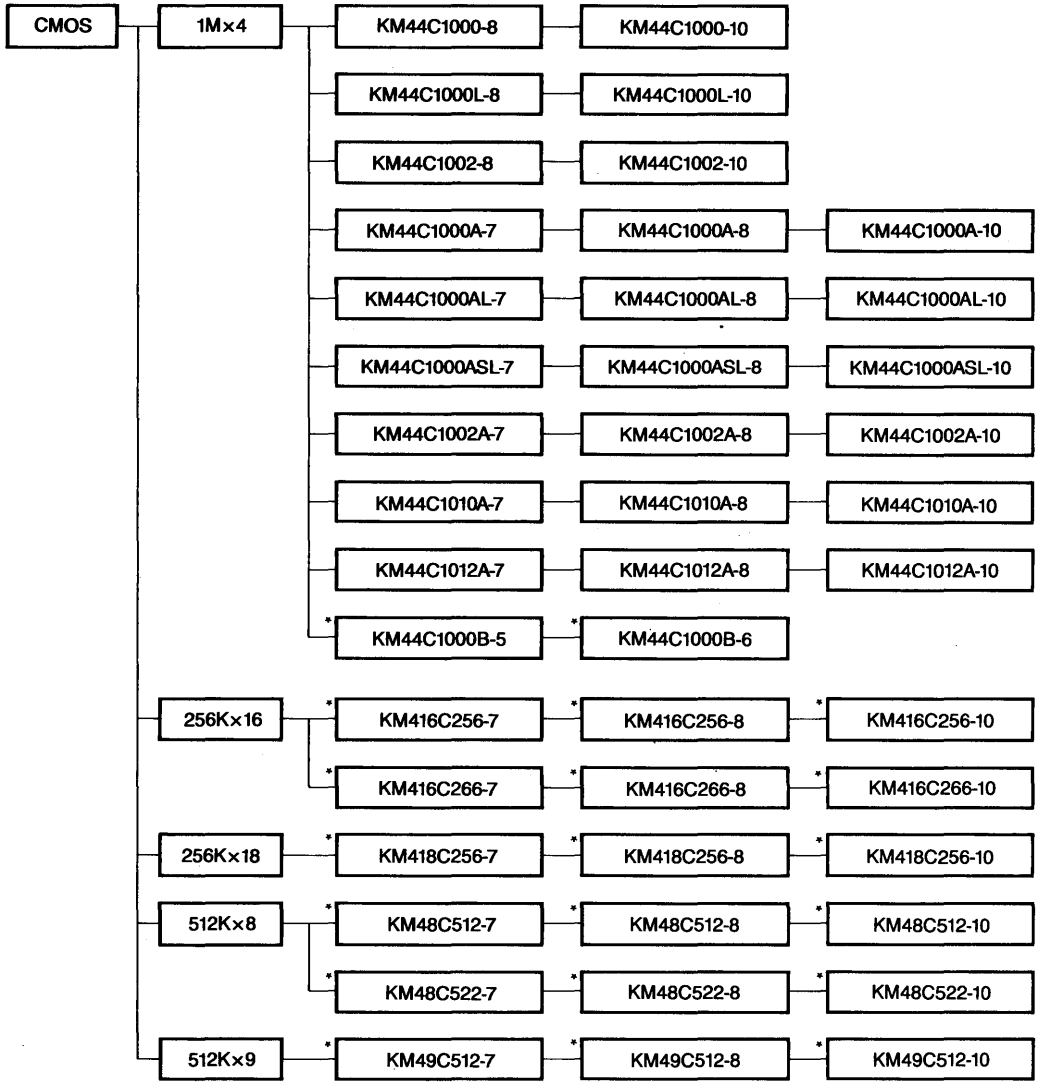
1.1 Dynamic RAM




CMOS
1M×4
KM44C1000-8
KM44C1000-10
KM44C1000L-8
KM44C1000L-10
KM44C1002-8
KM44C1002-10
KM44C1000A-7
KM44C1000A-8
KM44C1000A-10
KM44C1000AL-7
KM44C1000AL-8
KM44C1000AL-10
KM44C1000ASL-7
KM44C1000ASL-8
KM44C1000ASL-10
KM44C1002A-7
KM44C1002A-8
KM44C1002A-10
KM44C1010A-7
KM44C1010A-8
KM44C1010A-10
KM44C1012A-7
KM44C1012A-8
KM44C1012A-10
* KM44C1000B-5
* KM44C1000B-6
256K×16
* KM416C256-7
* KM416C256-8
* KM416C256-10
* KM416C266-7
* KM416C266-8
* KM416C266-10
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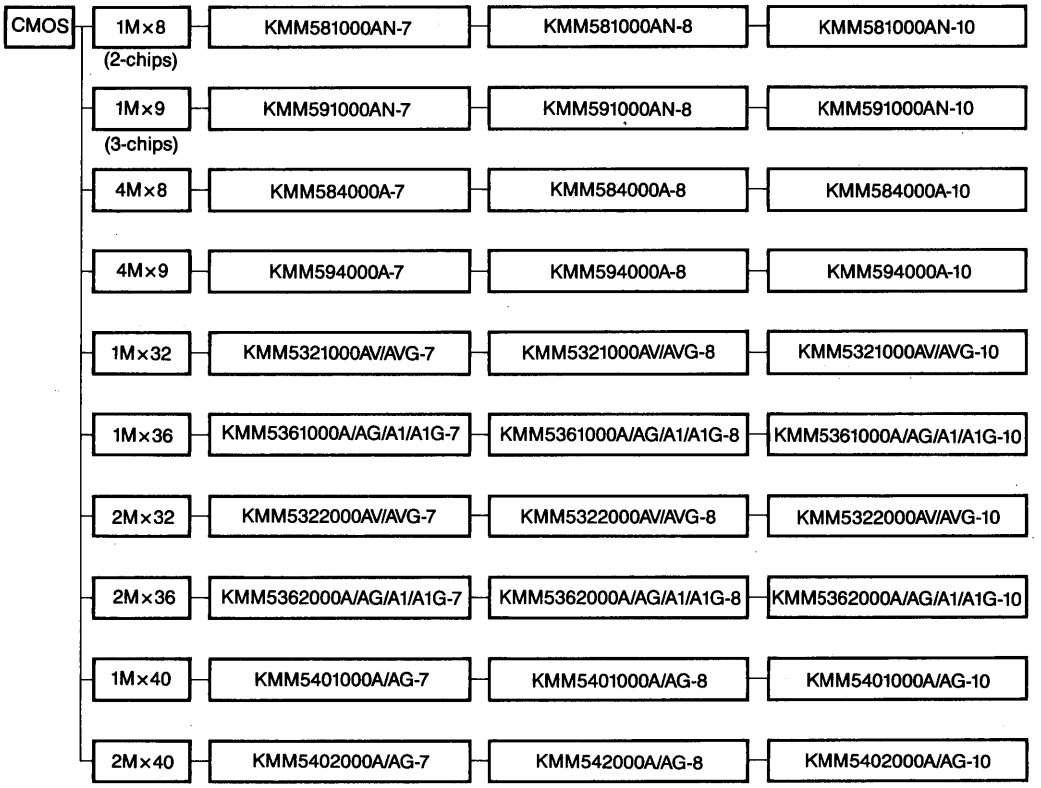
* KM418C256-7
* KM418C256-8
* KM418C256-10
512K×8
* KM48C512-7
* KM48C512-8
* KM48C512-10
* KM48C522-7
* KM48C522-8
* KM48C522-10
512K×9
* KM49C512-7
* KM49C512-8
* KM49C512-10

* New Product

1.2 Dynamic RAM Module



2. Product Guide

2.1 Dynamic RAM

Generation	Part Number	Organization	Speed (ns)	Technology	Feature	Package	Remark
1st Gen.	KM41C4000J	4M x 1	80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000Z	4M x 1	80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000LJ	4M x 1	80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000LZ	4M x 1	80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4001J	4M x 1	80/100	CMOS	Nibble	20 Pin SOJ	Now
	KM41C4001Z	4M x 1	80/100	CMOS	Nibble	20 Pin ZIP	Now
	KM41C4002J	4M x 1	80/100	CMOS	Static Column	20 Pin SOJ	Now
	KM41C4002Z	4M x 1	80/100	CMOS	Static Column	20 Pin ZIP	Now
	KM44C1000J	1M x 4	80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C1000Z	1M x 4	80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000LJ	1M x 4	80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C1000LZ	1M x 4	80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1002J	1M x 4	80/100	CMOS	Static Column	20 Pin SOJ	Now
	KM44C1002Z	1M x 4	80/100	CMOS	Static Column	20 Pin ZIP	Now
2nd Gen.	KM41C4000AJ	4M x 1	70/80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000AP	4M x 1	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C4000AZ	4M x 1	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000AT	4M x 1	70/80/100	CMOS	Fast Page	20 Pin TSOP	Now
	KM41C4000ALJ/ASLJ	4M x 1	70/80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C4000ALP/ASLP	4M x 1	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C4000ALZ/ASLZ	4M x 1	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C4000ALT/ASLT	4M x 1	70/80/100	CMOS	Fast Page	20 Pin TSOP	Now
	KM41C4001AJ	4M x 1	70/80/100	CMOS	Nibble	20 Pin SOJ	Now
	KM41C4001AP	4M x 1	70/80/100	CMOS	Nibble	18 Pin DIP	Now
	KM41C4001AZ	4M x 1	70/80/100	CMOS	Nibble	20 Pin ZIP	Now
	KM41C4002AJ	4M x 1	70/80/100	CMOS	Static Column	20 Pin SOJ	Now
	KM41C4002AP	4M x 1	70/80/100	CMOS	Static Column	18 Pin DIP	Now
	KM41C4002AZ	4M x 1	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
	KM44C1000AJ	1M x 4	70/80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C1000AP	1M x 4	70/80/100	CMOS	Fast Page	20 Pin DIP	Now
	KM44C1000AZ	1M x 4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000AT	1M x 4	70/80/100	CMOS	Fast Page	20 Pin TSOP	Now
	KM441000ALJ/ASLJ	1M x 4	70/80/100	CMOS	Fast Page	20 Pin SOJ	Now
	KM441000ALP/ASLP	1M x 4	70/80/100	CMOS	Fast Page	20 Pin DIP	Now
	KM44C1000ALZ/ASLZ	1M x 4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C1000ALT/ASLT	1M x 4	70/80/100	CMOS	Fast Page	20 Pin TSOP	Now
	KM44C1002AJ	1M x 4	70/80/100	CMOS	Static Column	20 Pin SOJ	Now
	KM44C1002AP	1M x 4	70/80/100	CMOS	Static Column	20 Pin DIP	Now
	KM44C1002AZ	1M x 4	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
	KM44C1010AJ	1M x 4	70/80/100	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C1010AP	1M x 4	70/80/100	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C1010AZ	1M x 4	70/80/100	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C1012AJ	1M x 4	70/80/100	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C1012AP	1M x 4	70/80/100	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C1012AZ	1M x 4	70/80/100	CMOS	Static Column with WPB	20 Pin ZIP	Now
3rd Gen.	*KM41C4000B	4M x 1	50/60	CMOS	Fast Page	20 Pin SOJ	2Q, '92
	*KM44C1000B	1M x 4	50/60	CMOS	Fast Page	20 Pin SOJ	2Q, '92
	*KM416C256J	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	2Q, '92
	*KM416C256Z	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	2Q, '92

Dynamic RAM (Continued)

Generation	Part Number	Organization	Speed (ns)	Technology	Feature	Package	Remark
	*KM416C266J	256K×16	70/80/100	CMOS	Fast Page with WPB	40 Pin SOJ	2Q, '92
	*KM416C266Z	256K×16	70/80/100	CMOS	Fast Page with WPB	40 Pin ZIP	2Q, '92
	*KM418C256J	256K×18	70/80/100	CMOS	Fast Page	40 Pin SOJ	2Q, '92
	*KM418C256Z	256K×18	70/80/100	CMOS	Fast Page	40 Pin ZIP	2Q, '92
	*KM48C512J	512K×8	70/80/100	CMOS	Fast Page	28 Pin SOJ	2Q, '92
	*KM48C512Z	512K×8	70/80/100	CMOS	Fast Page	28 Pin ZIP	2Q, '92
	*KM48C522J	512K×8	70/80/100	CMOS	Fast Page with WPB	28 Pin SOJ	2Q, '92
	*KM48C522Z	512K×8	70/80/100	CMOS	Fast Page with WPB	28 Pin SOJ	2Q, '92
	*KM49C512J	512K×9	70/80/100	CMOS	Fast Page	28 Pin SOJ	2Q, '92
	*KM49C512Z	512K×9	70/80/100	CMOS	Fast Page	28 Pin ZIP	2Q, '92

2.2 Dynamic RAM Module

*S: Single Side
*D: Double Side

Part Number	Organization	Speed (ns)	Technology	Feature	Package	PCB Height [In]
KMM581000AN	1M×8	70/80/100	CMOS	Fast Page Mode	*S, 30 Pin SIMM	0.65
KMM591000AN	1M×9	70/80/100	CMOS	Fast Page Mode	*S, 30 Pin SIMM	0.65
KMM584000A	4M×8	70/80/100	CMOS	Fast Page Mode	*S, 30 Pin SIMM	0.805
KMM594000A	4M×9	70/80/100	CMOS	Fast Page Mode	*S, 30 Pin SIMM	0.805
KMM5321000AV/AVG	1M×32	70/80/100	CMOS	Fast Page Mode	*S, 72 Pin SIMM	0.855
KMM5361000A/AG/A1/A1G	1M×36	70/80/100	CMOS	Fast Page Mode	A/AG: *D, 72 Pin A1/A1G: *S, 72 Pin	A/AG: 1.25 A1/A1G: 1.0
KMM5322000AV/AVG	2M×32	70/80/100	CMOS	Fast Page Mode	*D, 72 Pin SIMM	0.855
KMM5362000A/AG/A1/A1G	2M×36	70/80/100	CMOS	Fast Page Mode	*D, 72 Pin SIMM	A/AG: 1.25 A1/A1G: 1.0
KMM5401000A/AG	1M×40	70/80/100	CMOS	Fast Page Mode	*S, 72 Pin SIMM	1.0
KMM5402000A/AG	2M×40	70/80/100	CMOS	Fast Page Mode	*D, 72 Pin SIMM	1.0

3. Cross Reference

3.1 Dynamic RAM

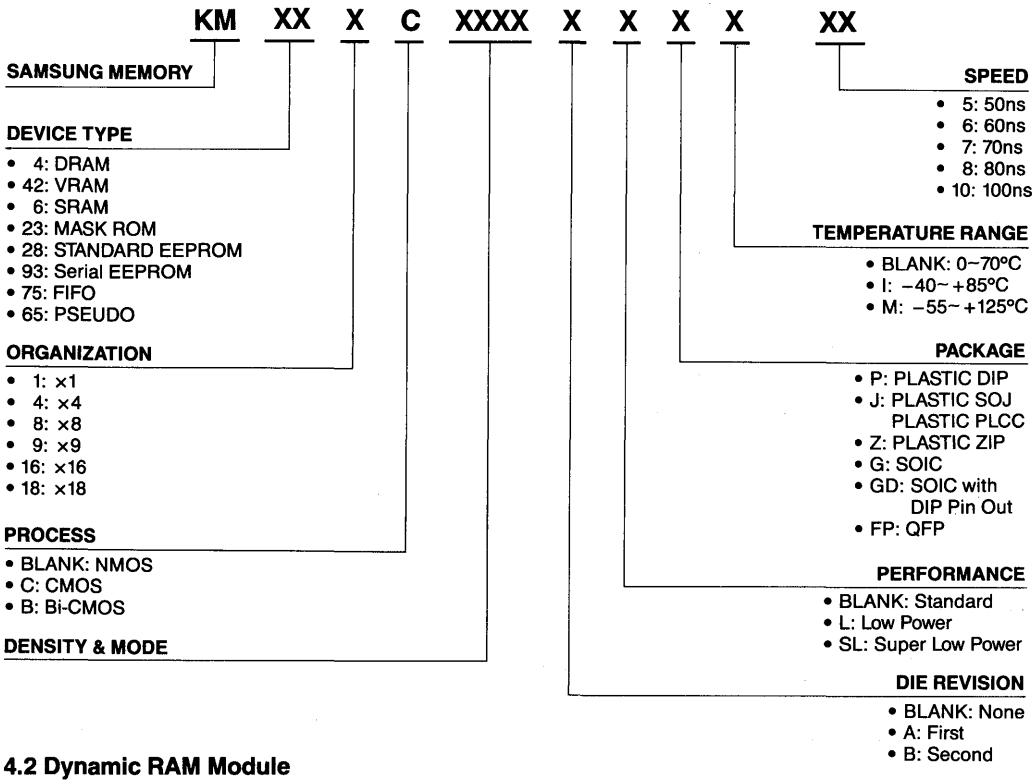
Org.	Mode	Samsung	Toshiba	Hitachi	Fujitsu	NEC	Oki
X1	F. Page	KM41C4000	TC514100	HM514100	MB814100	MPD424100	MSM514100
	Nibble	KM41C4001	TC514101	HM514101	MB814101	MPD424101	MSM514101
	S. Column	KM41C4002	TC514102	HM514102	MB814102	MPD424102	MSM514102
X4	F. Page	KM44C1000	TC514400	HM514400	MB814400	MPD424400	MSM514400
	S. Column	KM44C1002	TC514402	HM514402	MB814402	MPD424402	MSM514402

3.2 Dynamic RAM Module

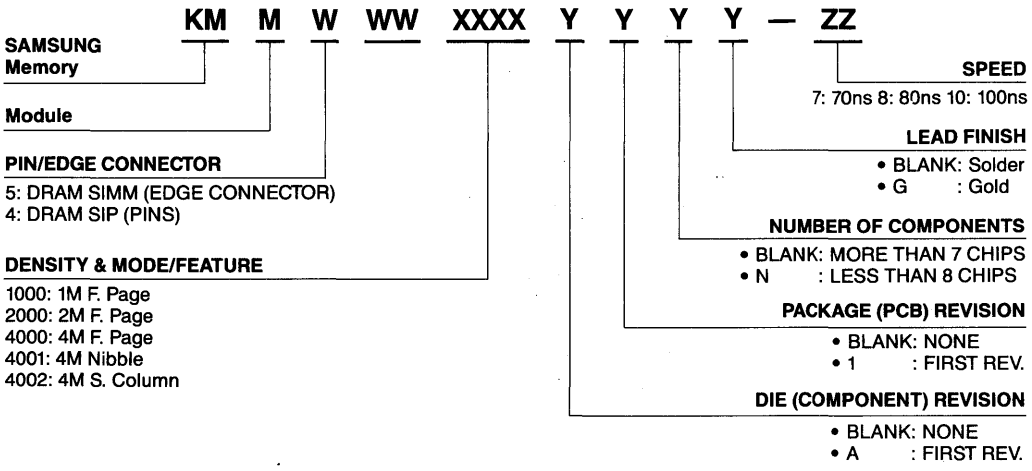
Density	Organization	Samsung	Toshiba	Hitachi	NEC
8M bit	1M x 8 (2C)	KMM581000AN		HB56G18	
9M bit	1M x 9 (3C)	KMM591000AN		HB56G19	
32M bit	4M x 8	KMM584000	THM84000	HB56A48	MC-424100A8
36M bit	4M x 9	KMM594000	THM94000	HB56A49	MC-424100A9
32M bit	1M x 32	KMM5321000	THM321000	HB56D132	
36M bit	1M x 36	KMM5361000	THM5361020	HB56D136	MC-421000A36
64M bit	2M x 32	KMM5322000	THM322020	HB56D232	
72M bit	2M x 36	KMM5362000	THM362020	HB56D236	MC-422000A36
40M bit	1M x 40	KMM5401000	THM401020	HB56A140	
80M bit	2M x 40	KMM5402000	THM402020		

4. Ordering Information

4.1 Dynamic RAM

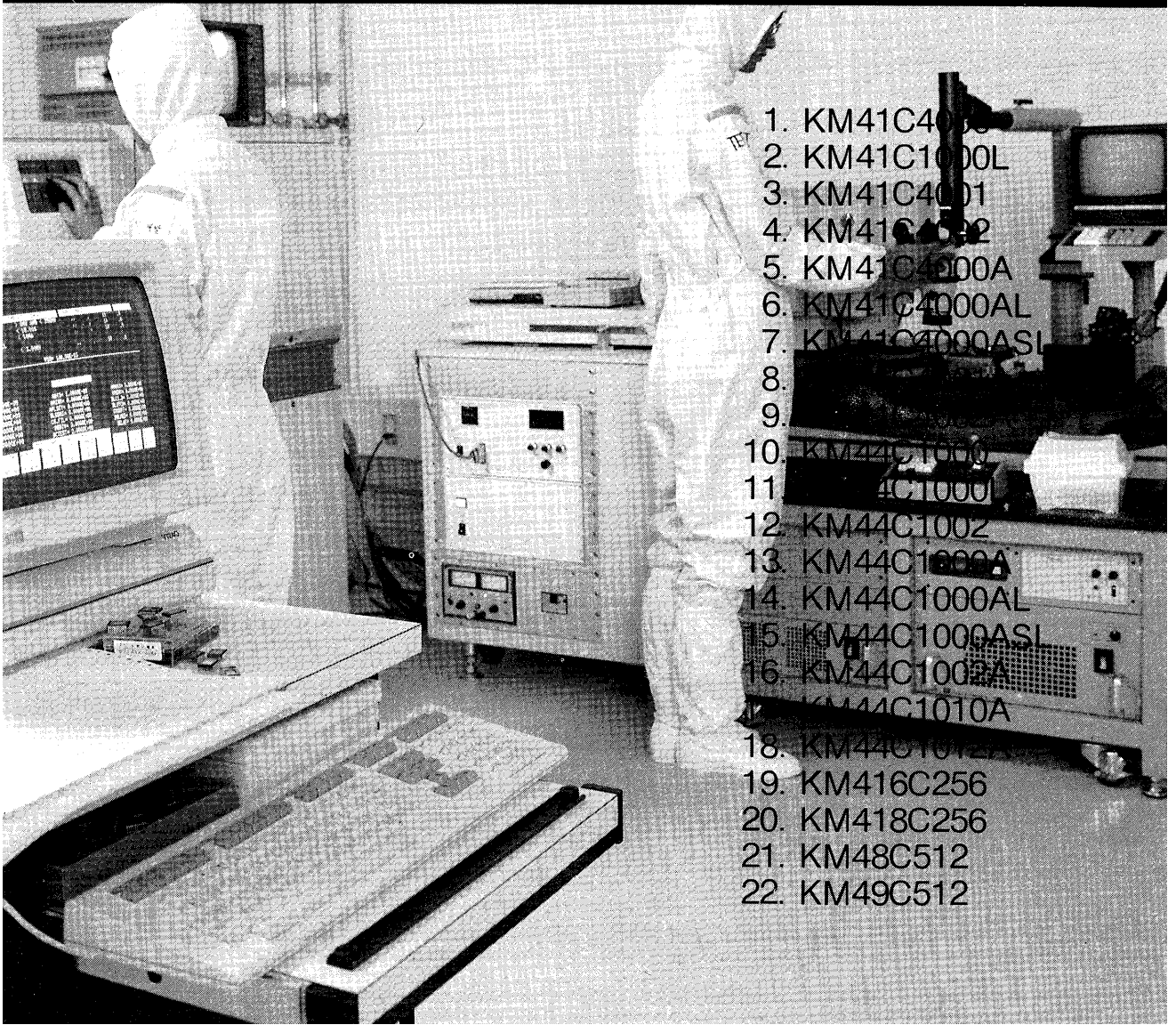


4.2 Dynamic RAM Module



NOTES

4M DRAM DATA SHEETS 2



1. KM41C4[illegible]
2. KM41C1000L
3. KM41C4001
4. KM41C4002
5. KM41C4000A
6. KM41C4000AL
7. KM41C4000ASL
8. [illegible]
9. [illegible]
10. KM44C1000
11. [illegible]4C1000L
12. KM44C1002
13. KM44C1000A
14. KM44C1000AL
15. KM44C1000ASL
16. KM44C1002A
17. KM44C1010A
18. KM44C1012
19. KM416C256
20. KM418C256
21. KM48C512
22. KM49C512

4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000/L- 8	80ns	20ns	150ns
KM41C4000/L-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O capability using Early Write**
- **Single +5V±10% power supply**
- **Refresh Cycles:**
  - **—1024 cycles/16ms**
  - **—1024 cycles/128ms (L-Version)**
- **Power dissipation**
  - **—Standby: 5.5mW**
    1.7mW (L-Version)
  - **—Active : 550mW (80ns)**
    468mW (100ns)
- **JEDEC standard pinout**
- **Available in Plastic SOJ/ZIP**

GENERAL DESCRIPTION

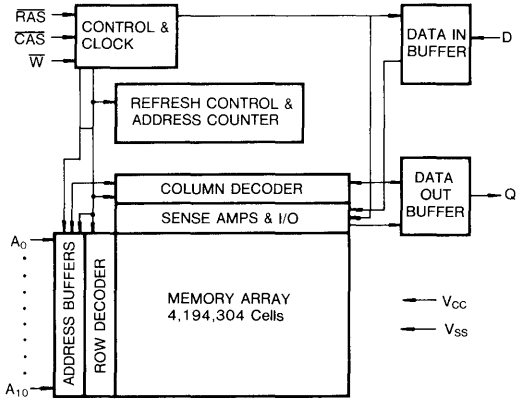
The Samsung KM41C4000/L is a high speed CMOS 4,194,304 bit × 1 dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000/L features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

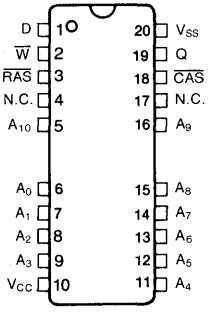
The KM41C4000/L is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

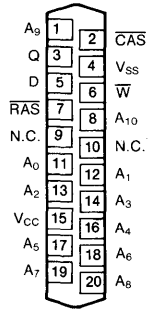


PIN CONFIGURATION (Top Views)

- **KM41C4000J/LJ**



- **KM41C4000Z/LZ**



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000/L- 8	I_{CC1}	—	100	mA
	KM41C4000/L-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM41C4000/L- 8	I_{CC3}	—	100	mA
	KM41C4000/L-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000/L- 8	I_{CC4}	—	60	mA
	KM41C4000/L-10		—	50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)	KM41C4000-8/10	I_{CC5}	—	1	mA
	KM41C4000L-8/10			300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000/L- 8	I_{CC6}	—	100	mA
	KM41C4000/L-10		—	85	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125μs, T_{RAS}=t_{RAS} min.~1μs	KM41C4000L- 8 KM41C4000L-10	I_{CC7}	—	400	μA
Stand Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} Dout Enable)		I_{CC8}	—	5	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C4000/L-8		KM41C4000/L-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		ns	
Read-modify-write cycle time	t_{RWC}	175		210		ns	
Fast Page mode cycle time	t_{PC}	55		60		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4
Access time from column address	t_{AA}		40		50	ns	3,10
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		55	ns	
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	200,000	100	200,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	ns	4,5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C4000/L-8		KM41C4000/L-10		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	12
Write command pulse width	t_{WP}	15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16	ms	
Refresh period (only for L-version, 1024 cycles)	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		25		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		50		ns	7
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		ns	
CAS precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test)	t_{CPT}	40		50		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{WRH}	10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50		55		ns	

TEST MODE CYCLE

(Note. 11)

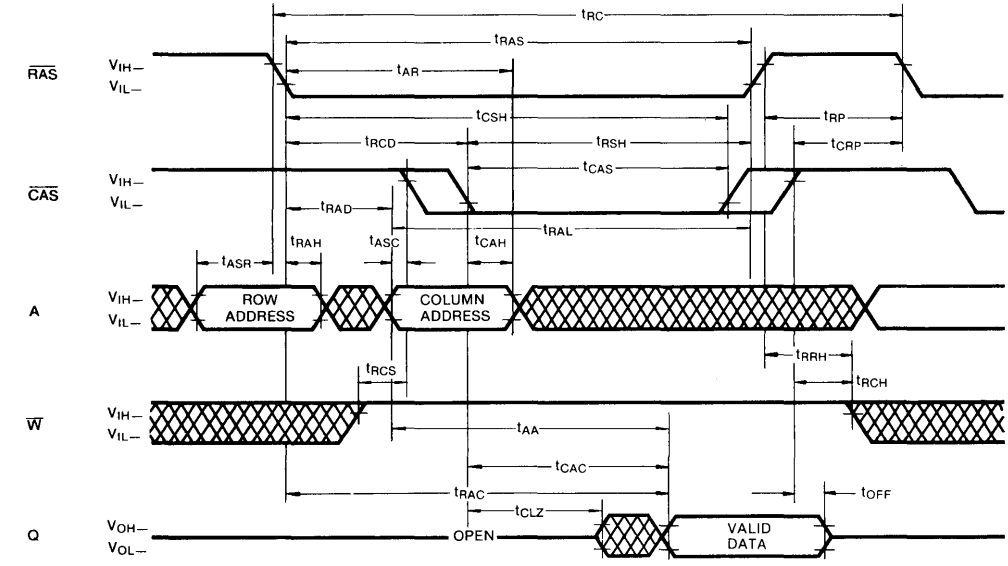
Parameter	Symbol	KM41C4000/L-8		KM41C4000/L-10		Unit	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	155	—	185	—	ns	
Read-Write Cycle Time	t_{RWC}	180	—	215	—	ns	
Fast Page Mode Cycle Time	t_{PC}	60	—	65	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PRWC}	85	—	95	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	105	ns	3,4
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	30	ns	3,4
Access Time from Column Address	t_{AA}	—	45	—	55	ns	3,10
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	55	—	60	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	85	200,000	105	200,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	105	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10,000	30	10,000	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
$\overline{CAS}$ to $\overline{W}$ Delay Time	t_{CWD}	25	—	30	—	ns	7
$\overline{RAS}$ to $\overline{W}$ Delay Time	t_{RWD}	85	—	105	—	ns	7
Column Address to $\overline{W}$ Time	t_{AWD}	45	—	55	—	ns	7

NOTES

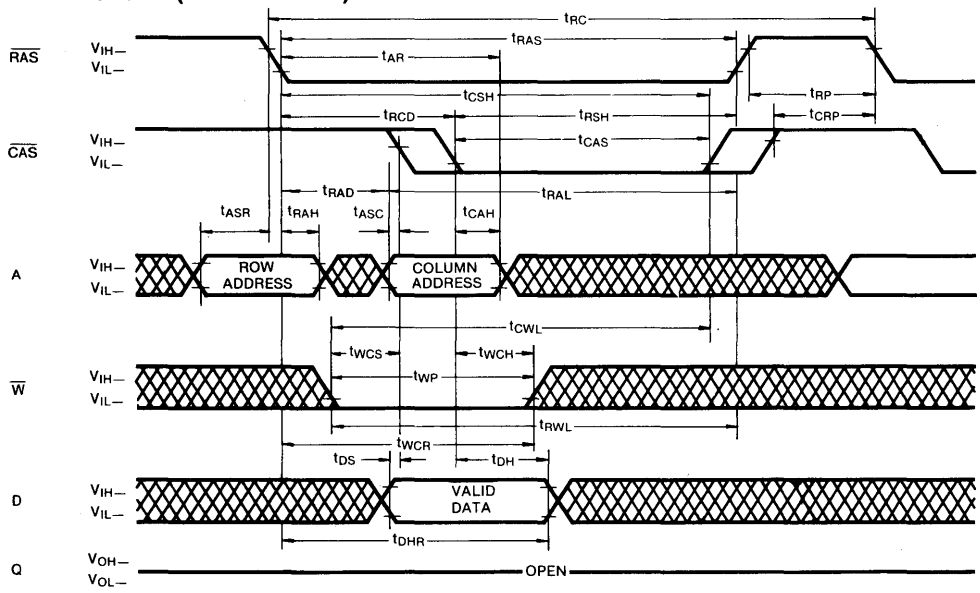
1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



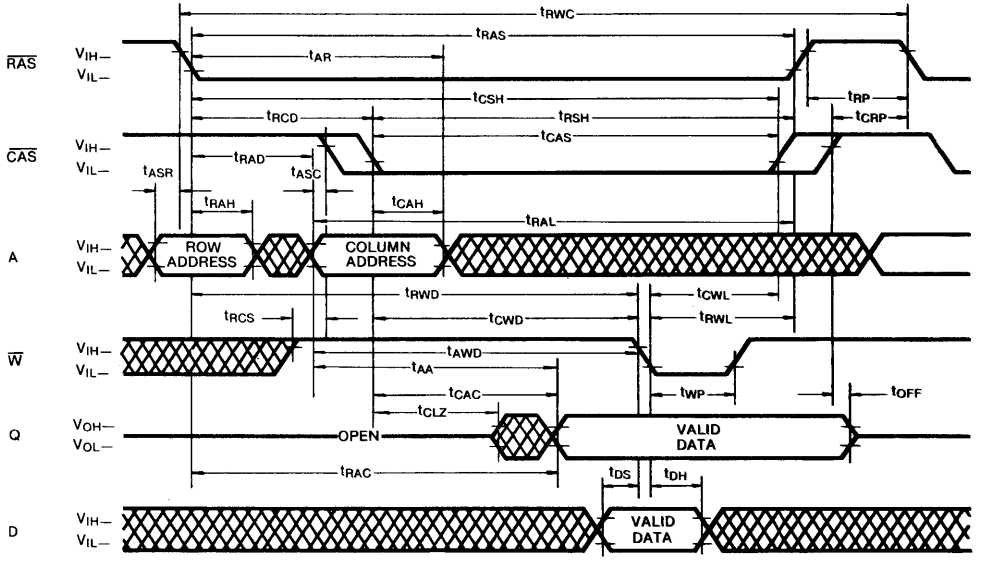
WRITE CYCLE (EARLY WRITE)



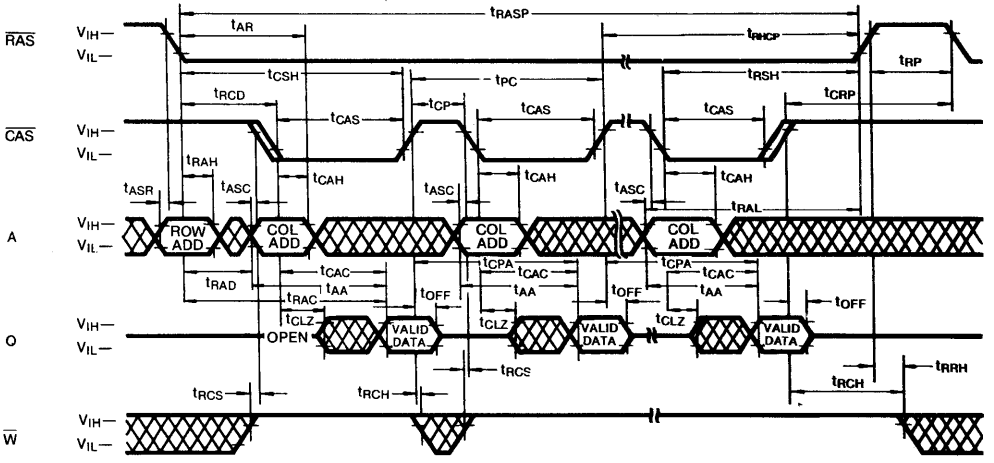
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



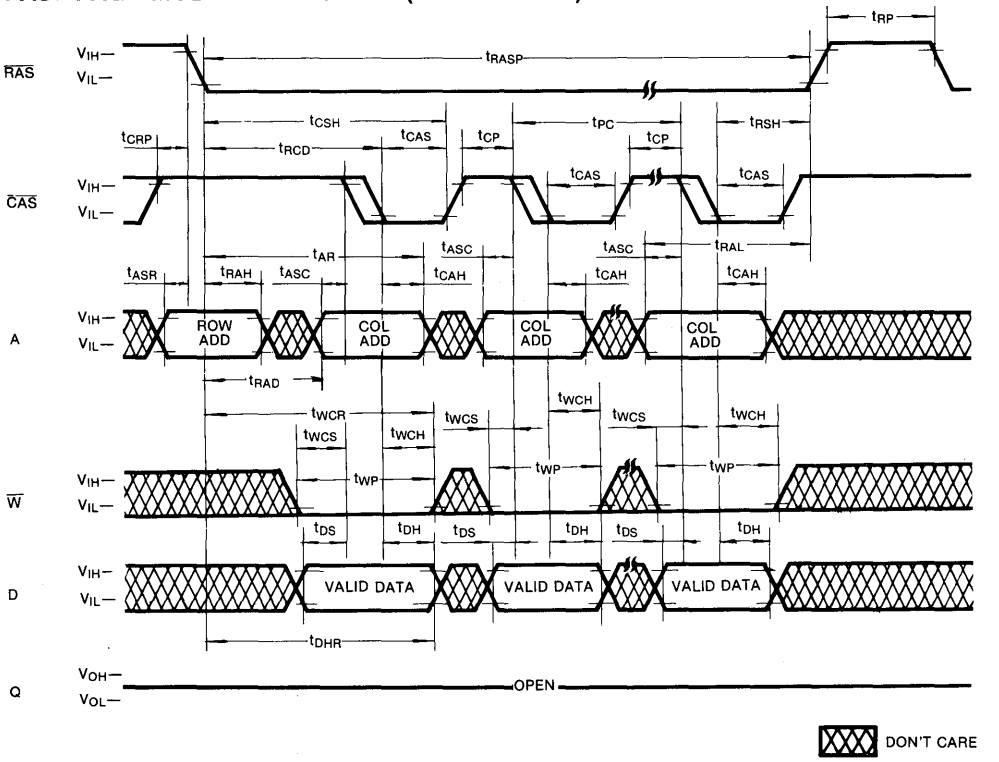
FAST PAGE MODE READ CYCLE



DON'T CARE

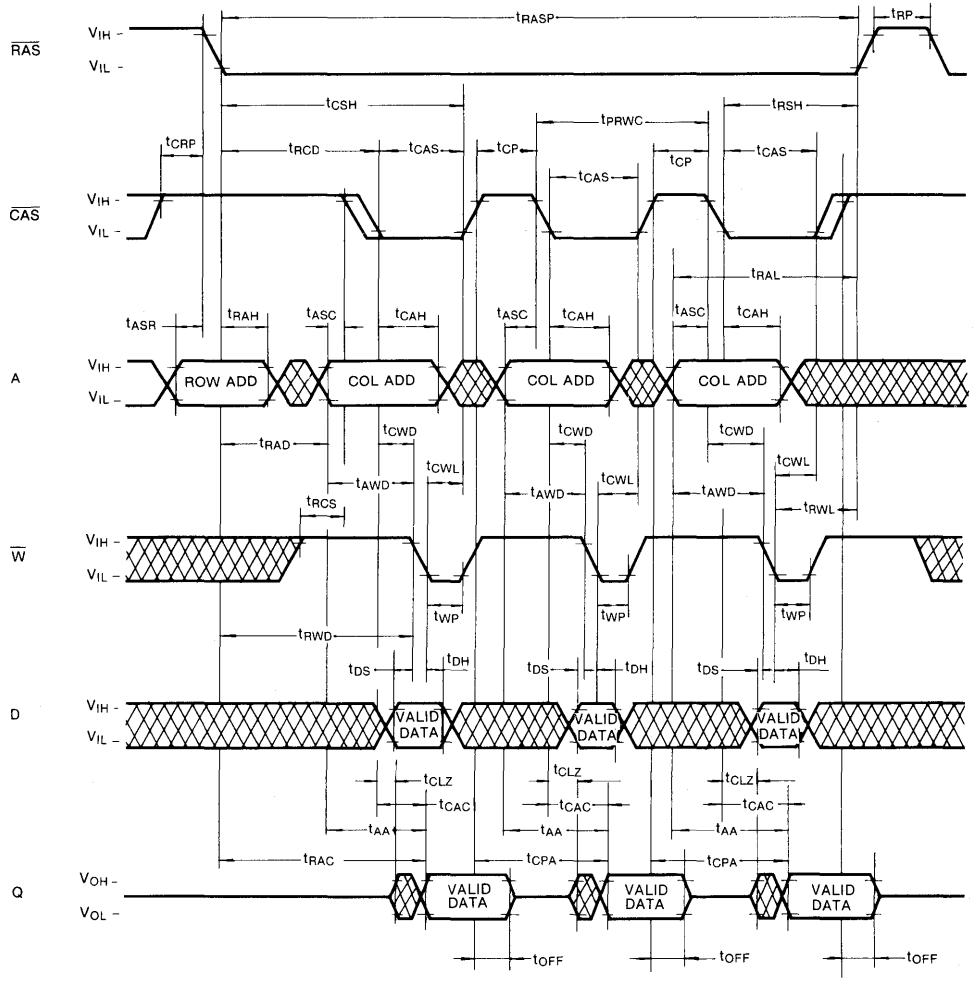
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

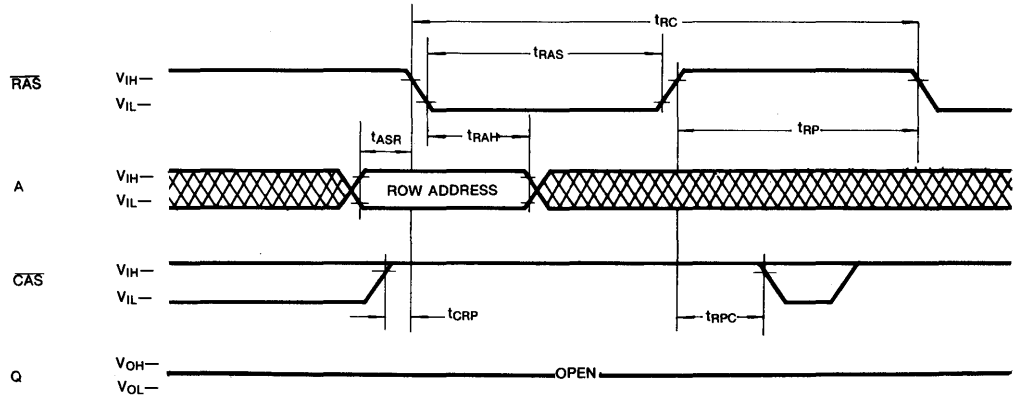
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

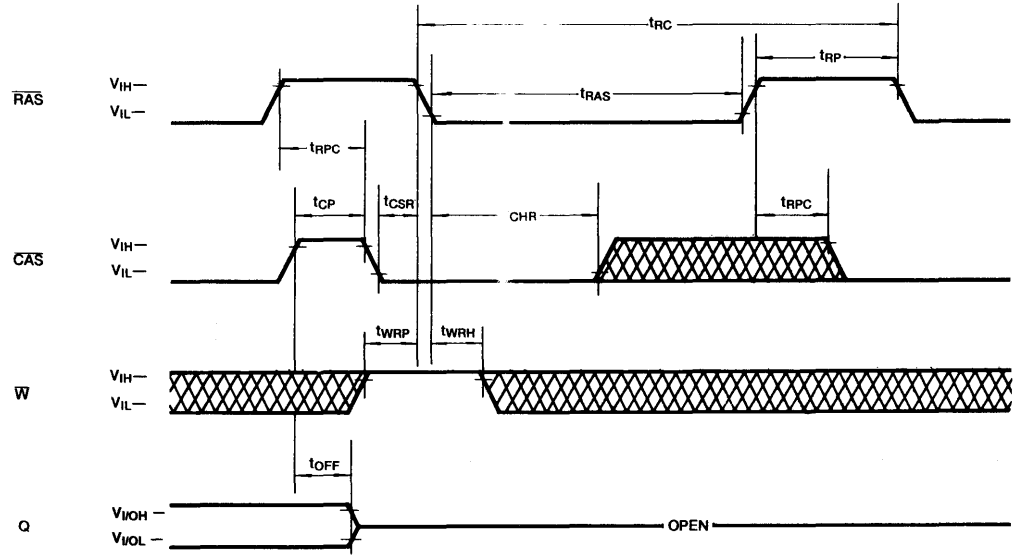
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



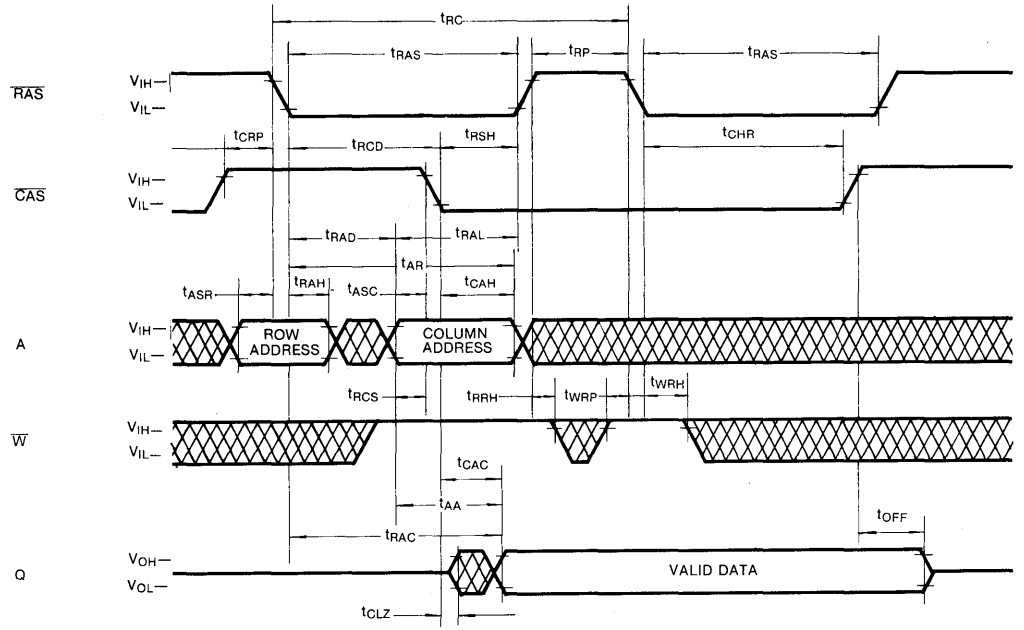
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

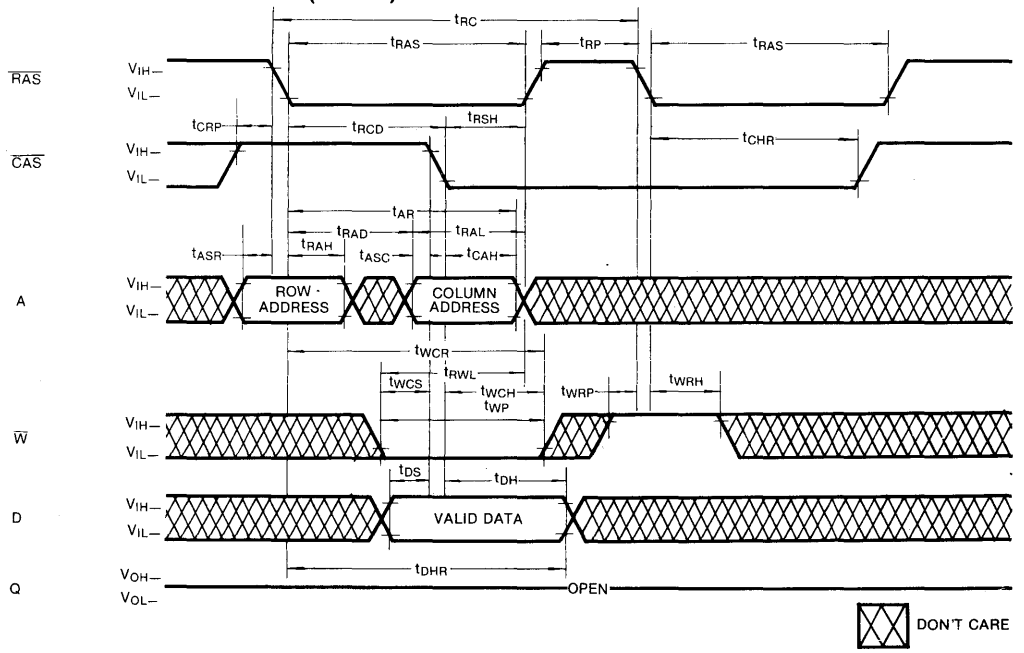


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

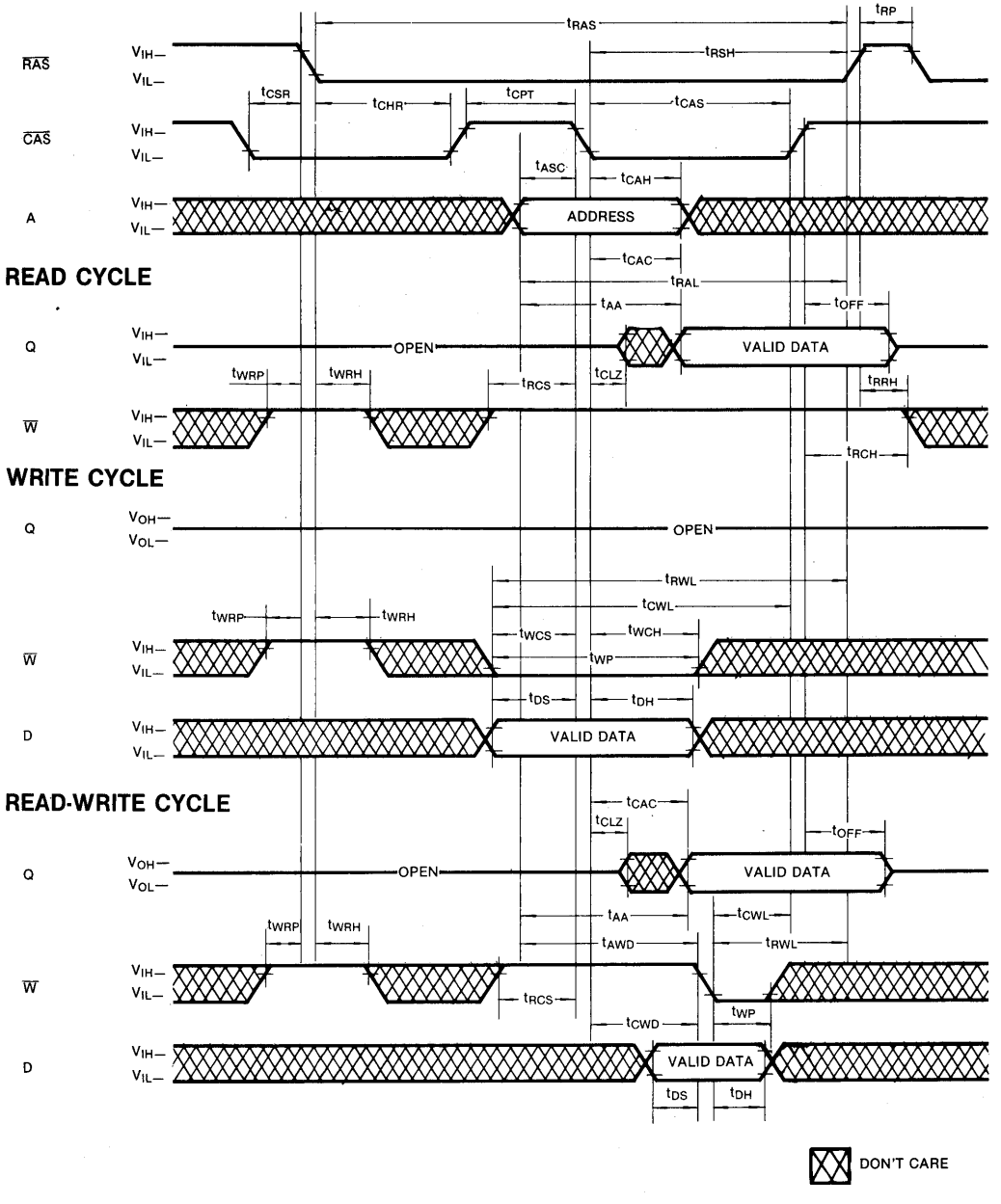


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

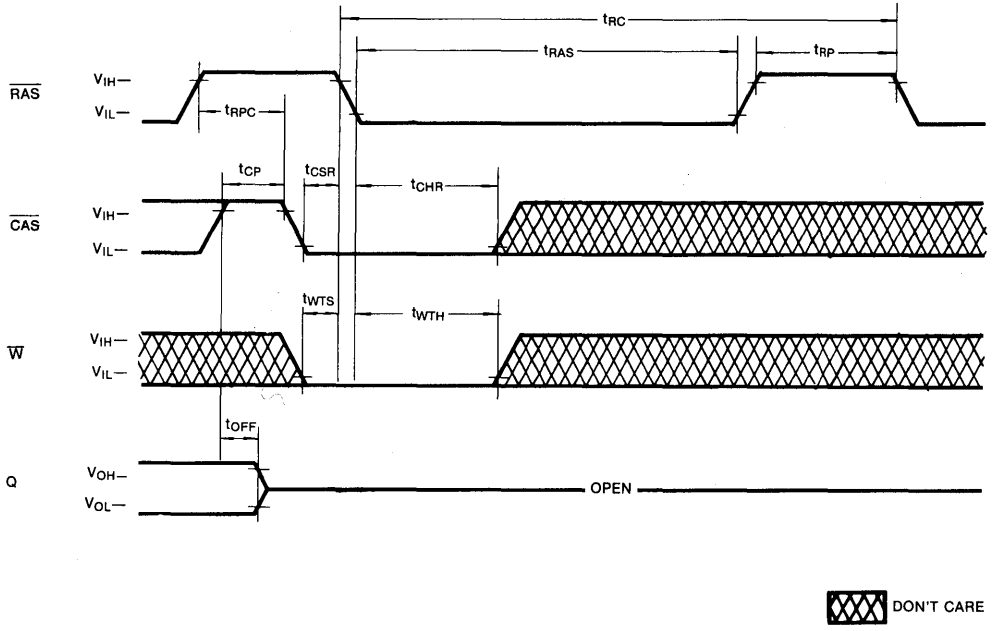
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D. Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4000L is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM $\overline{W}$, $\overline{CAS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000/L contains 4,194,304 memory locations Twenty two address bits are required to address a particular memory location. Since the KM41C4000/L has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000/L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000/L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000/L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000/L can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000/L has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000/L operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000/L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

16/128 (L-version)ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000/L has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000/L hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000/L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000/L has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

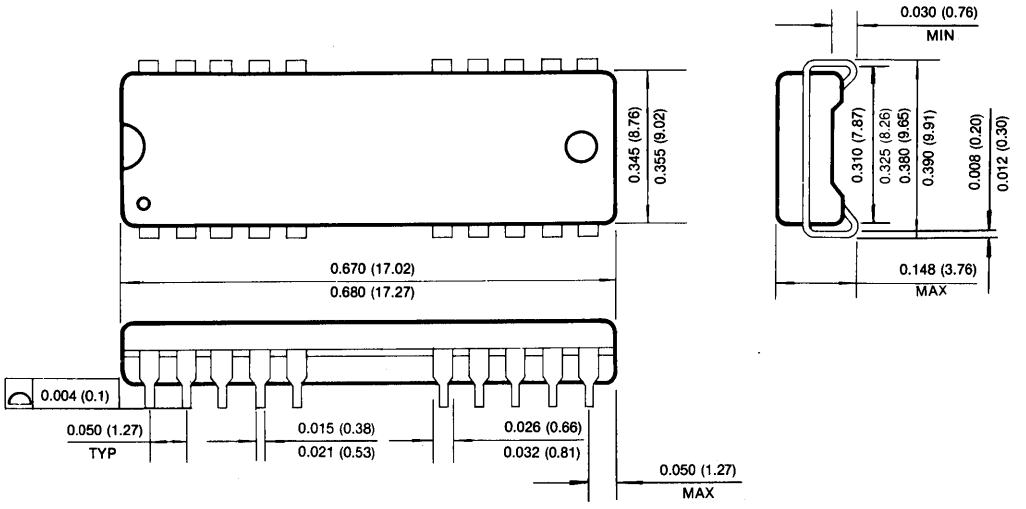
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4000/L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.

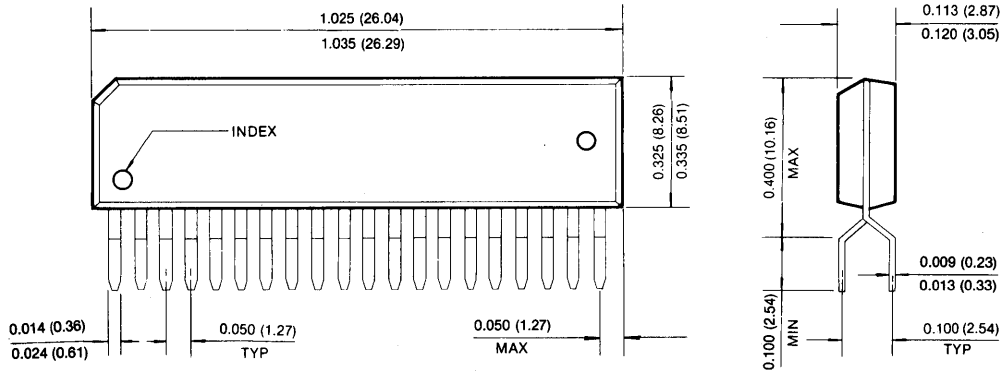
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



4MX1 Bit CMOS Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4001- 8	80ns	20ns	150ns
KM41C4001-10	100ns	25ns	180ns

- **Nibble Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, ZIP**

GENERAL DESCRIPTION

The Samsung KM41C4001 is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

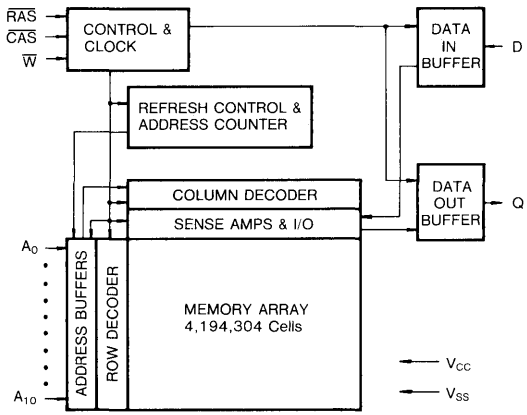
The KM41C4001 features Nibble Mode operation which allows high speed serial access of up to 4 bits of data.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

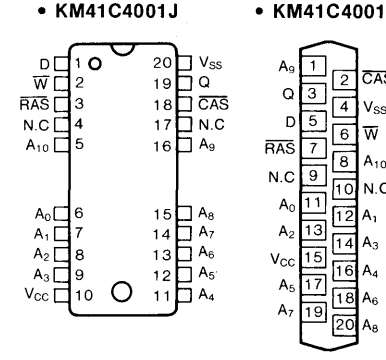
The KM41C4001 is fabricated using Samsung's advanced CMOS process.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4001- 8 KM41C4001-10	I_{CC1}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, @ t_{RC}=min)	KM41C4001- 8 KM41C4001-10	I_{CC3}	— —	100 85	mA mA
Nibble Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling: @ t_{NC}=min.)	KM41C4001- 8 KM41C4001-10	I_{CC4}	— —	60 50	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min.)	KM41C4001- 8 KM41C4001-10	I_{CC6}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} Dout=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. I_{CC} is specified as an average current. Specified value are obtained with the output open. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4001-8		KM41C4001-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		ns	
Read-modify-write cycle time	t_{RWC}	175		210		ns	
Nibble Mode Cycle Time	t_{NC}	40		45		ns	
Nibble Mode Read-Write Cycle Time	t_{NRWC}	65		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4
Nibble Mode Access Time	t_{NCAC}		20		25	ns	
Access time from column address	t_{AA}		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	ns	4,5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	12
Write command pulse width	t_{WP}	15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4001-8		KM41C4001-10		Unit	Notes
		Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ percharge to $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	40		50		ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		25		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10		10		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20		25		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	20		25		ns	
Nibble mode $\overline{W}$ to $\overline{RAS}$ lead time	t_{NRWL}	20		25		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	20		25		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		ns	

TEST MODE CYCLE

(Note. 11)

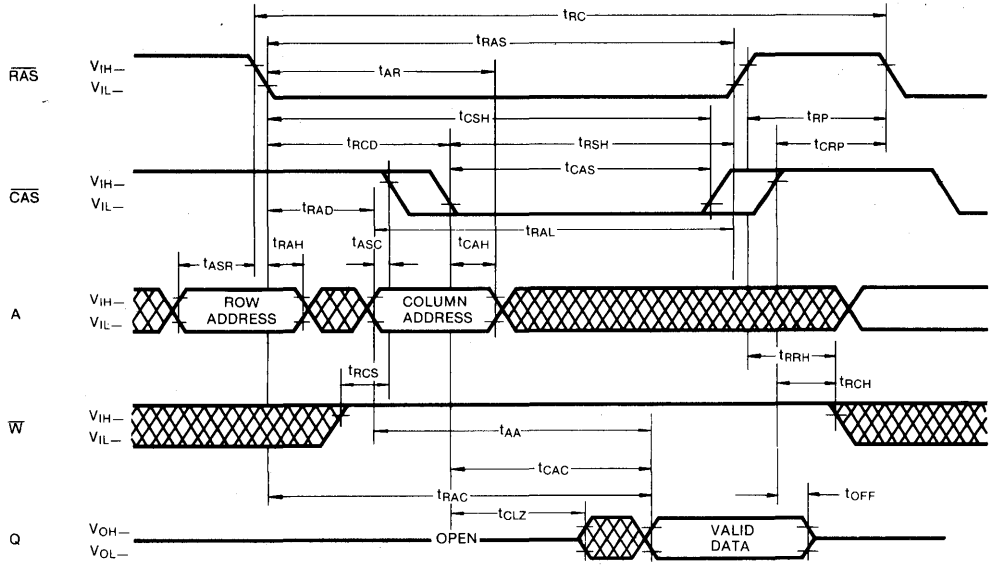
Parameter	Symbol	KM41C4001-8		KM41C4001-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	155		185		ns	
Read-modify-write cycle time	t_{RWC}	180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		85		105	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	3,4
Access time from column address	t_{AA}		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	25		30		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	45		55		ns	7

NOTES

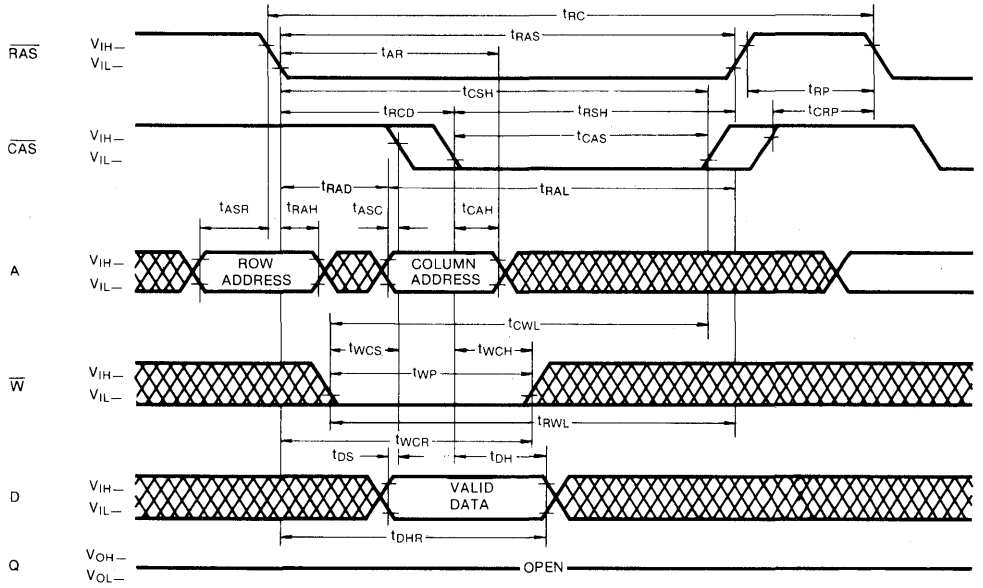
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



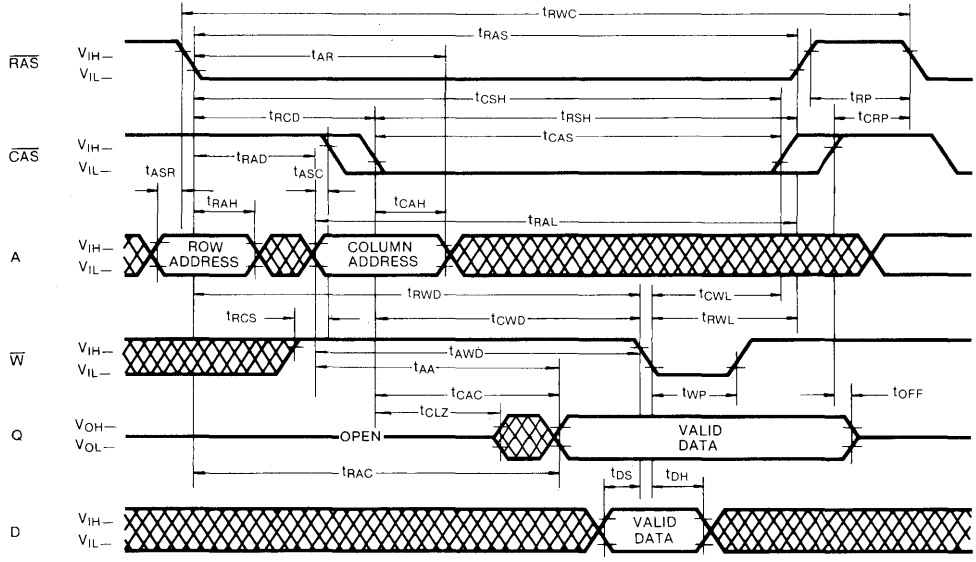
WRITE CYCLE (EARLY WRITE)



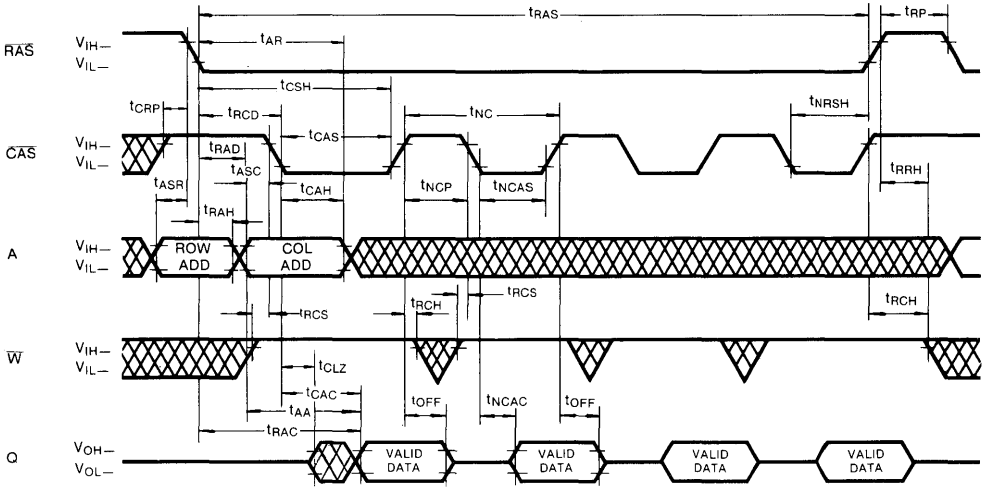
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



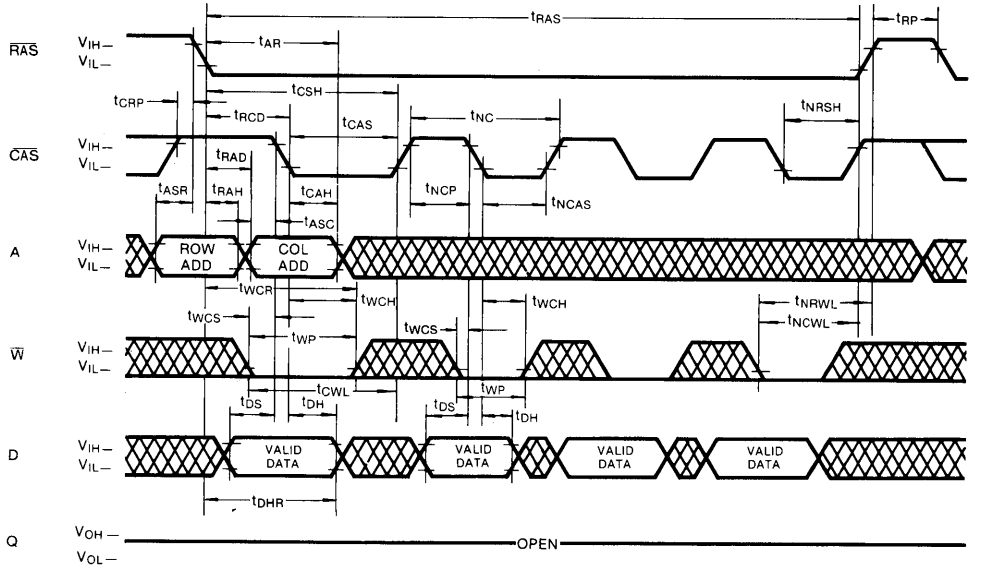
NIBBLE MODE READ CYCLE



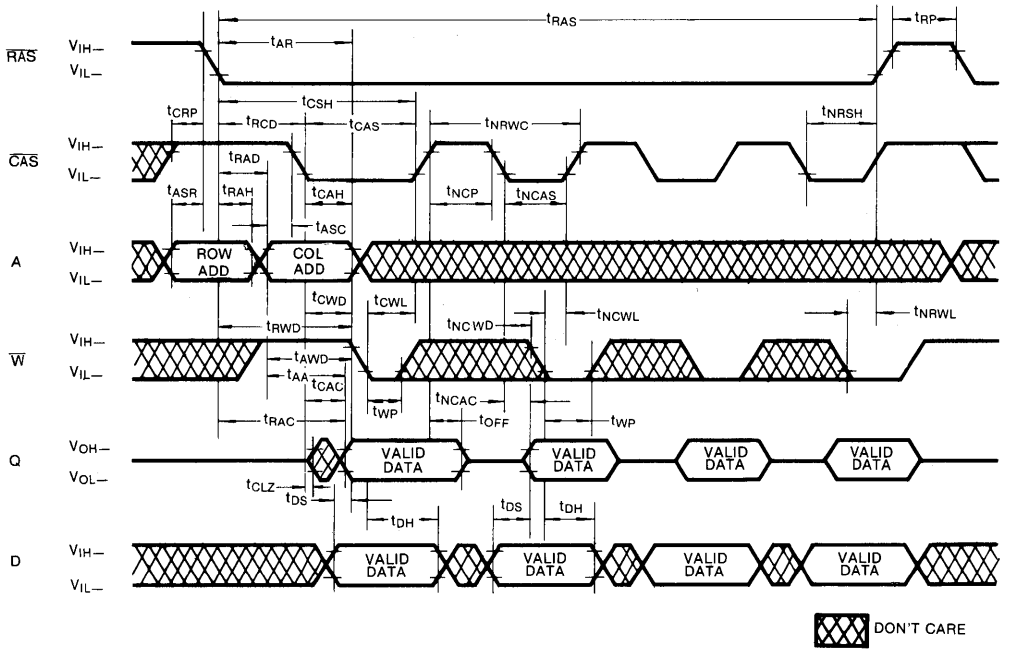
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE WRITE CYCLE (EARLY WRITE)



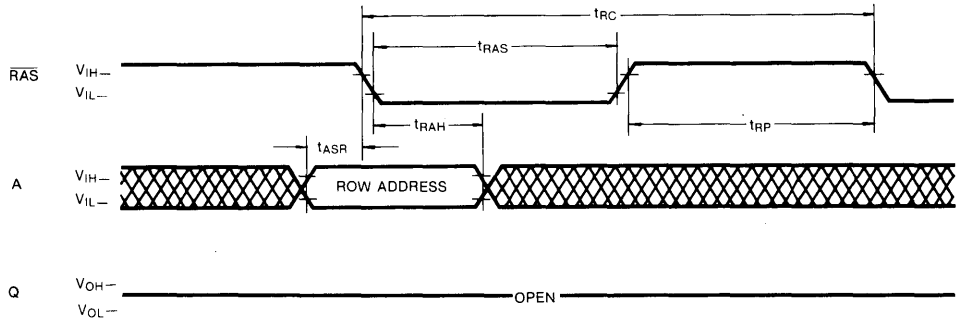
NIBBLE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

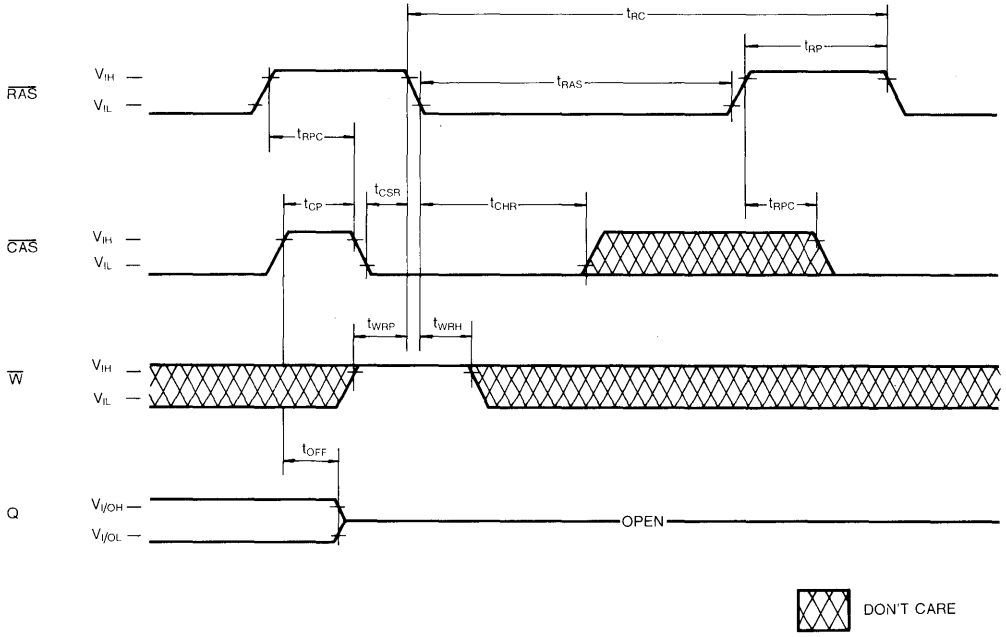
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{CAS}$=V_{IH}, $\overline{W}$,D, A_{10}=Don't Care



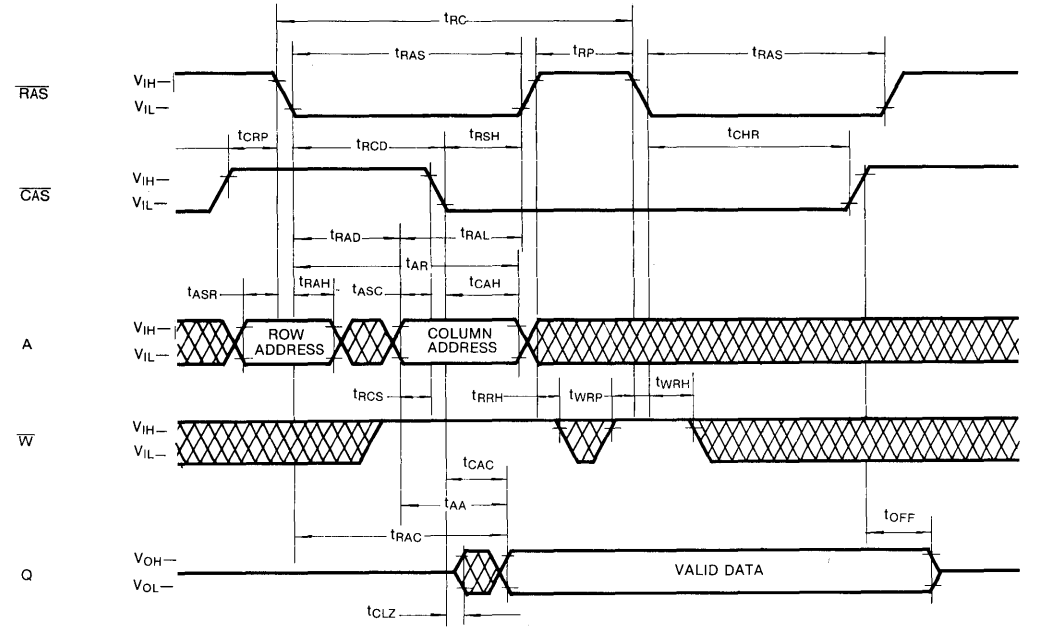
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

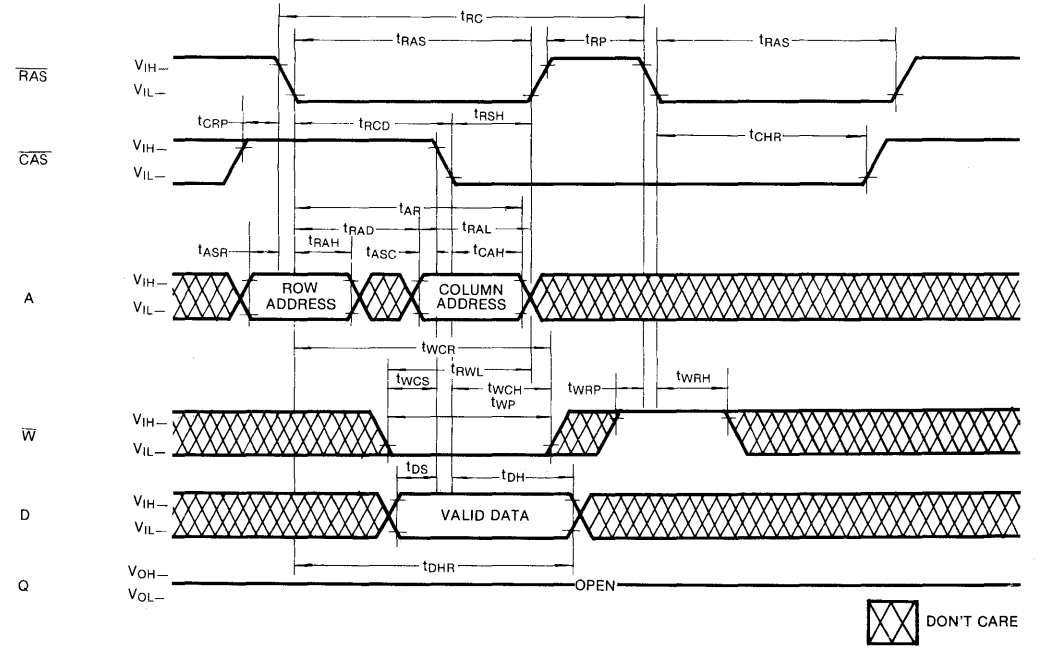


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

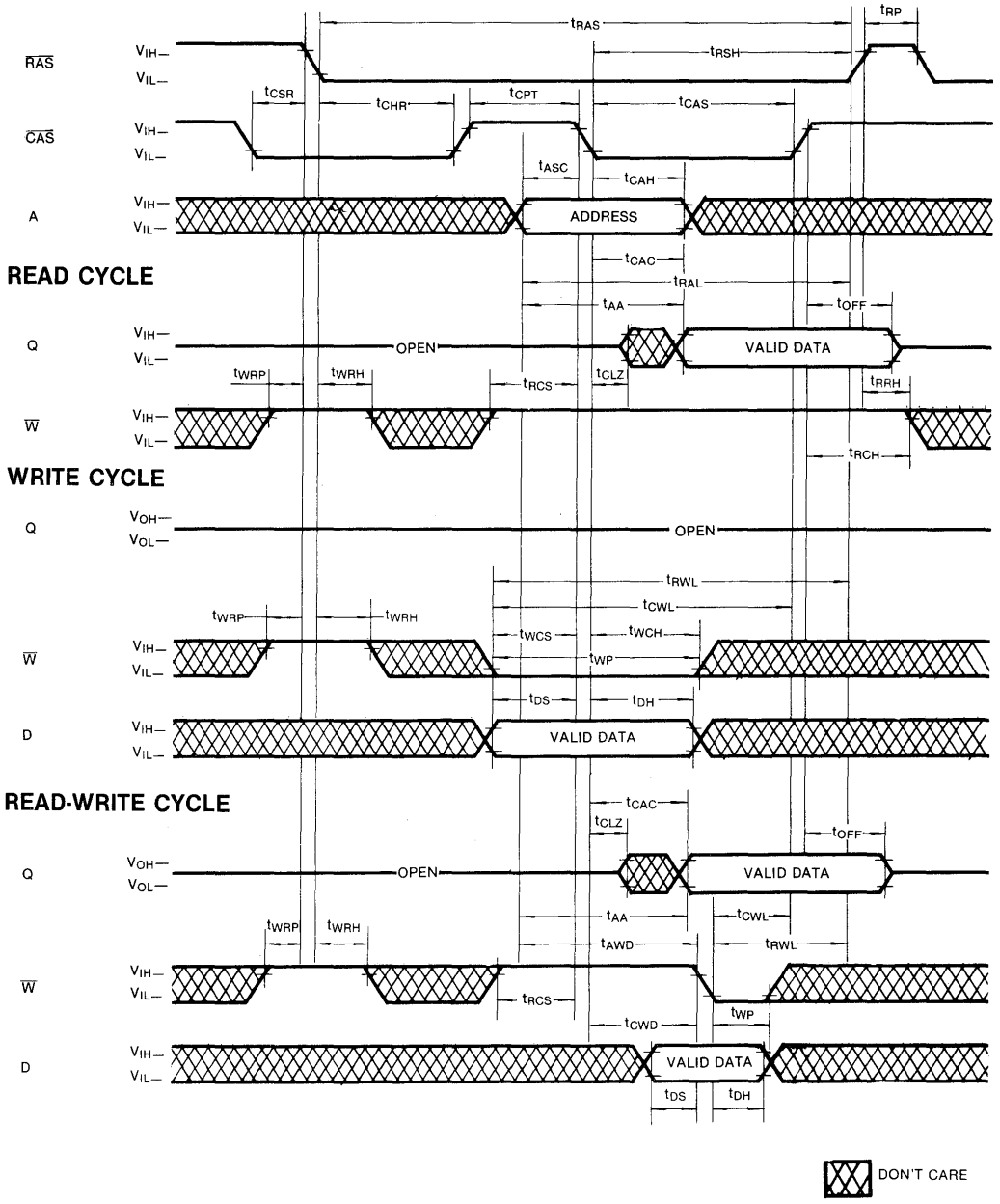


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

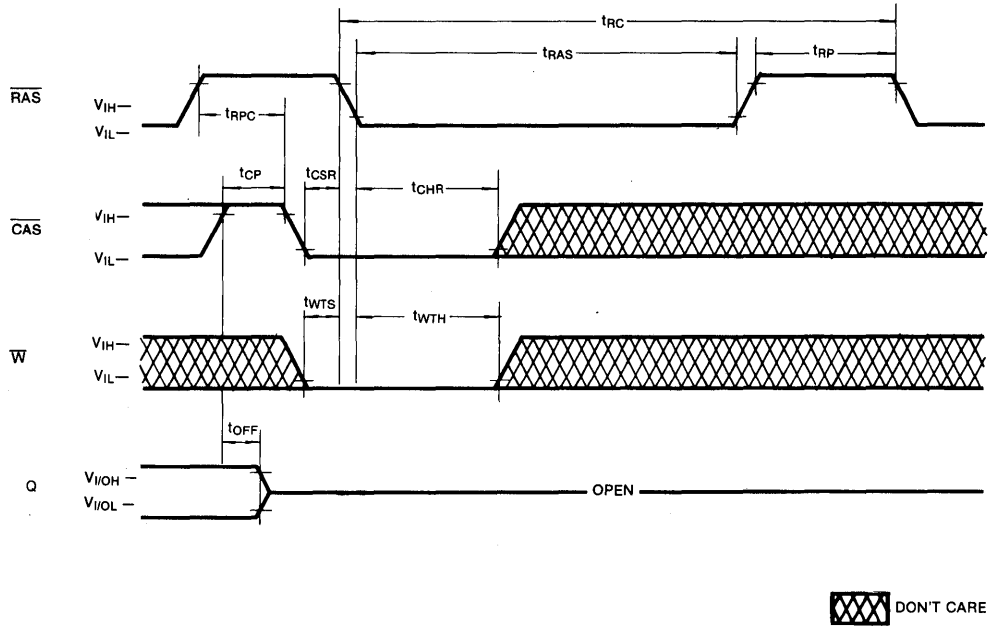
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address = Don't Care



TEST MODE DESCRIPTION

The KM41C4001 is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$ Beofre $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4001 contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4001 has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4001 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4001 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4001 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4001 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4001 has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4001 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-RAS Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4001 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity

DEVICE OPERATION (Continued)

it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4001 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

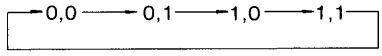
Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4001 hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4001 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Nibble Mode

The KM41C4001 has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 10 row address bits (R_{A0}-R_{A9}) and 10 column address bits (C_{A0}-C_{A9}). The two address bits, C_{A10} and R_{A10} are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A10} R_{A10}) as shown in the following diagram with R_{A10} being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble mode cycle can be a read, write or read-modify-write cycle. Any combinations of reads and writes or read-modify-write be allowed.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

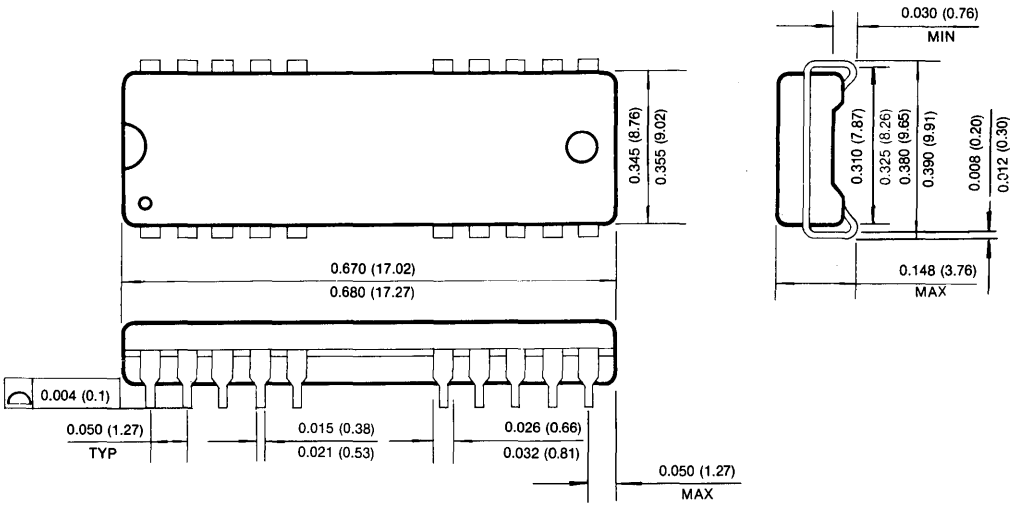
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4001 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh before proper device operation is achieved.

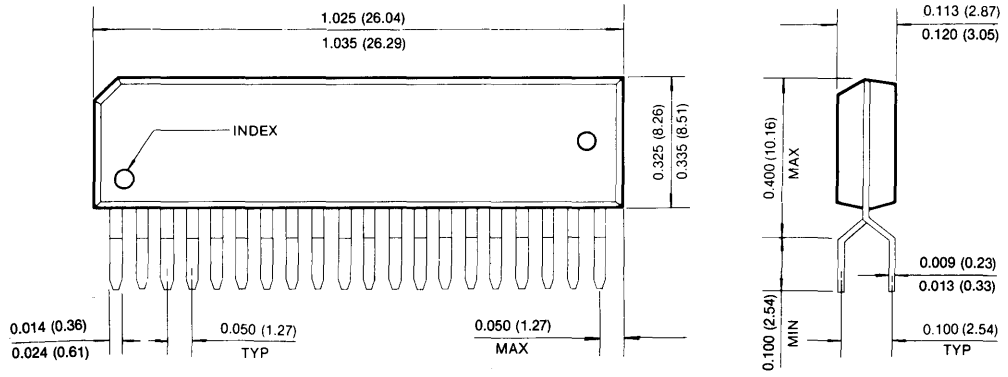
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



4MX1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4002- 8	80ns	20ns	150ns
KM41C4002-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, ZIP**

GENERAL DESCRIPTION

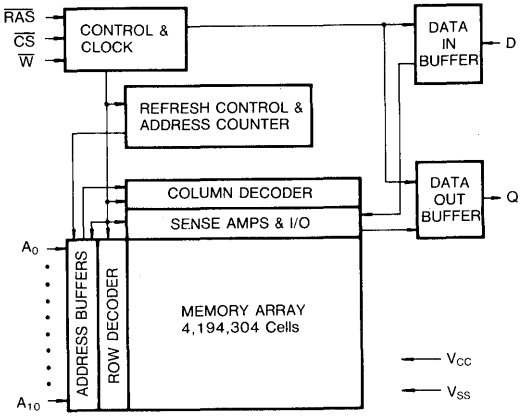
The Samsung KM41C4002 is a high speed CMOS 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4002 features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

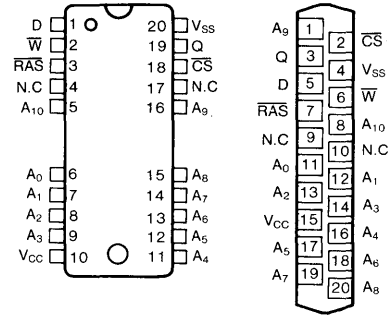
The KM41C4002 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM41C4002J**
- **KM41C4002Z**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM41C4002- 8 KM41C4002-10	I_{CC1}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM41C4002- 8 KM41C4002-10	I_{CC3}	— —	100 85	mA mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address cycling: @ t_{SC}=min.)	KM41C4002- 8 KM41C4002-10	I_{CC4}	— —	60 50	mA mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ cycling @ t_{RC}=min.)	KM41C4002- 8 KM41C4002-10	I_{CC6}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL} Dout=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. I_{CC} is specified as an average current. Specified value are obtained with the output open. I_{CC1}, I_{CC3} , I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4002-8		KM41C4002-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		ns	
Read-modify-write cycle time	t_{RWC}	175		210		ns	
Static column mode cycle time	t_{SC}	45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		25	ns	3,4,5
Access time from column address	t_{AA}		40		50	ns	3,11
Access time from last write	t_{ALW}		75		95	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	7
Output data hold time from column address	t_{AOH}	5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	25	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	60		75		ns	6
Column address hold referenced to $\overline{RAS}$	t_{AR}	95		115		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4002-8		KM41C4002-10		Unit	Notes
		Min	Max	Min	Max		
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		10		ns	
Last write to column address delay time	t_{LWAD}	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	75		95		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	9
Write command hold time	t_{WCH}	15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	6
Write command pulse width	t_{WP}	15		20		ns	
Write command inactive time	t_{WI}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		25		ns	
Data-in set-up time	t_{DS}	0		0		ns	10
Data-in hold time	t_{DH}	15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	40		50		ns	8
$\overline{CS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	0		0		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	40		50		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		ns	

TEST MODE CYCLE

(Note. 13)

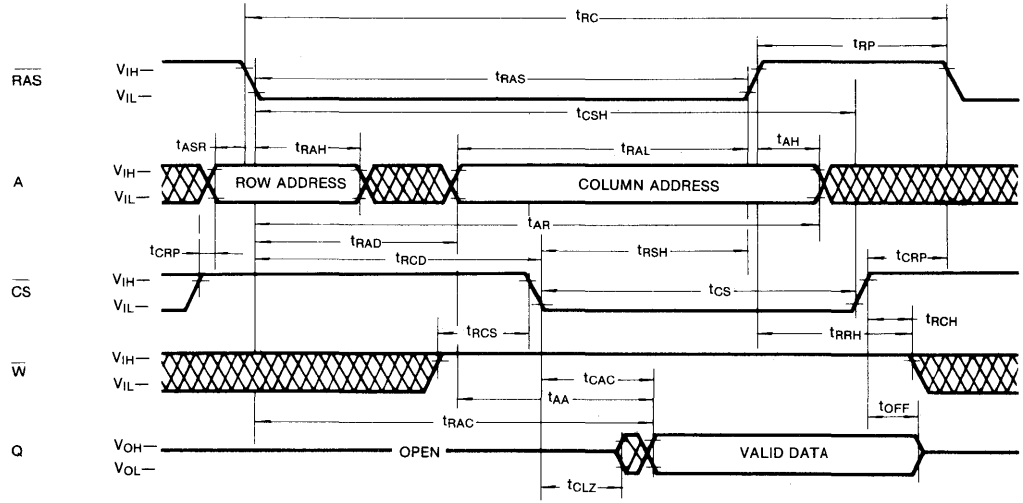
Parameter	Symbol	KM41C4002-8		KM41C4002-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	155		185		ns	
Read-modify-write cycle time	t_{RWC}	180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		30	ns	3,4,5
Access time from column address	t_{AA}		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	25		30		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	45		55		ns	8
Static column mode cycle time	t_{SC}	50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	85		95		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	30	100,000	ns	

NOTES

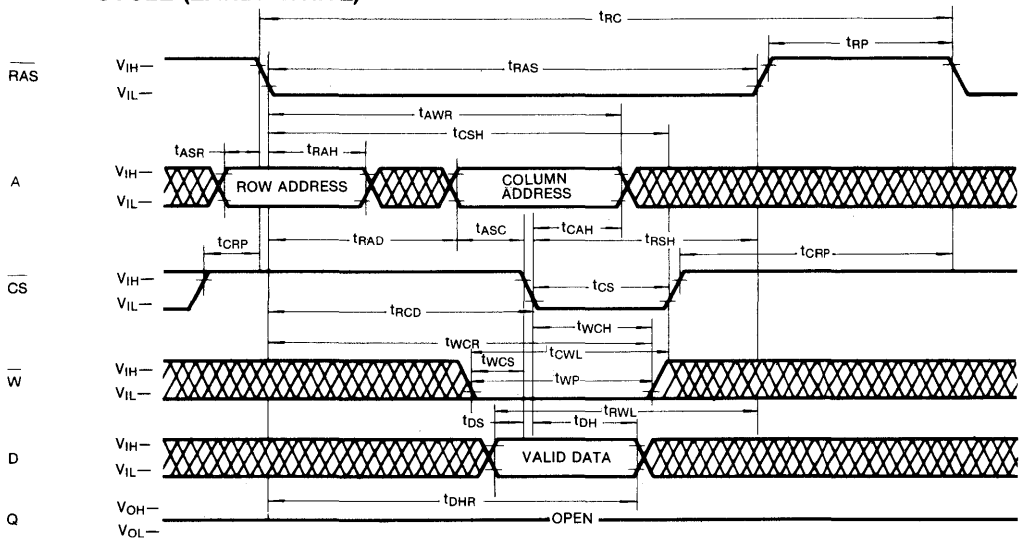
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. If t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE



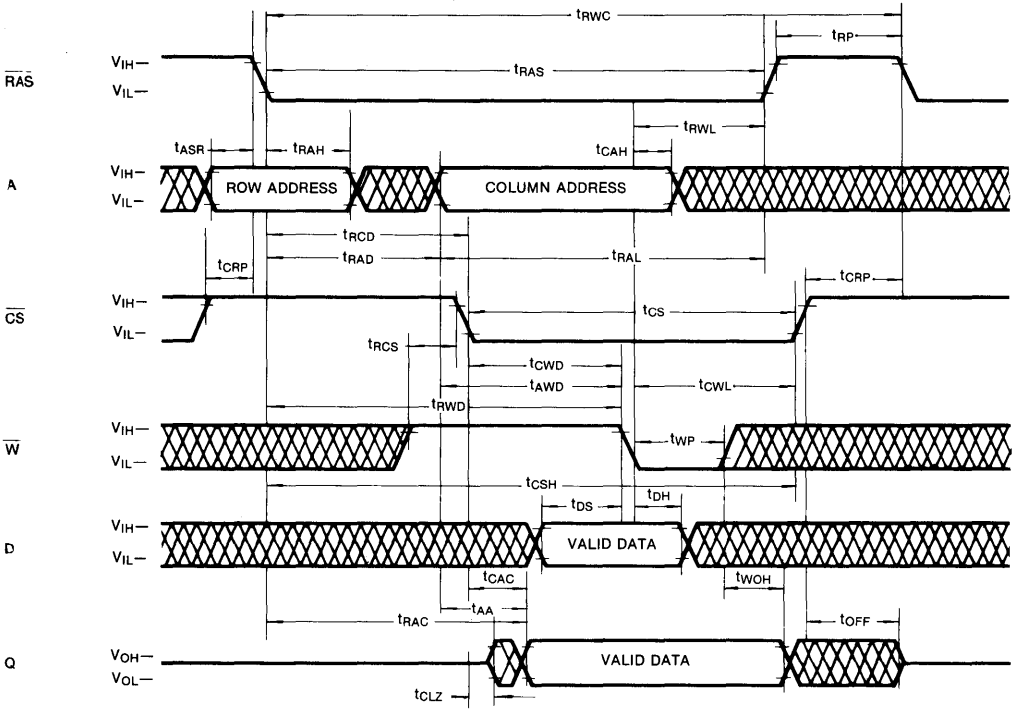
WRITE CYCLE (EARLY WRITE)



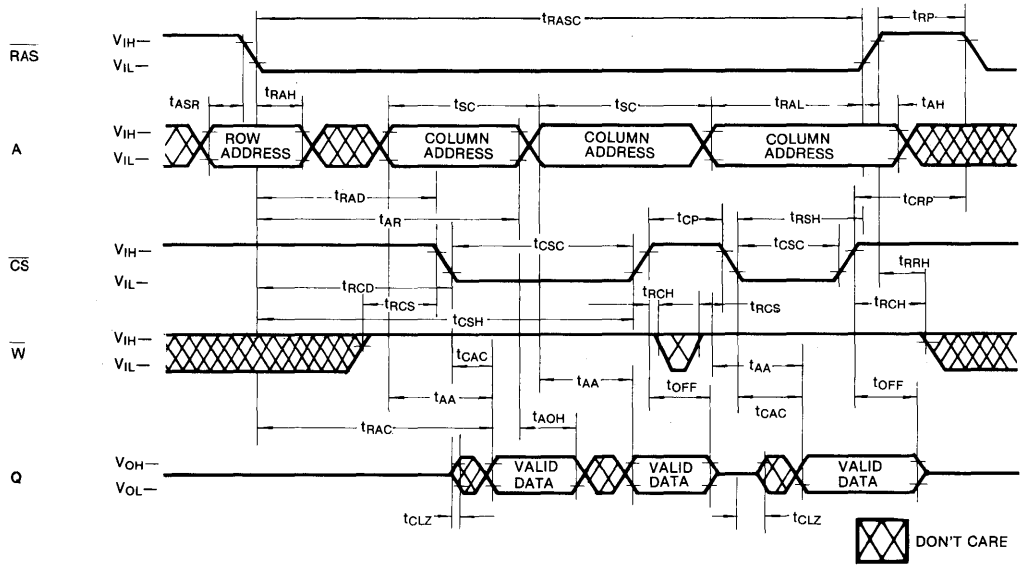
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

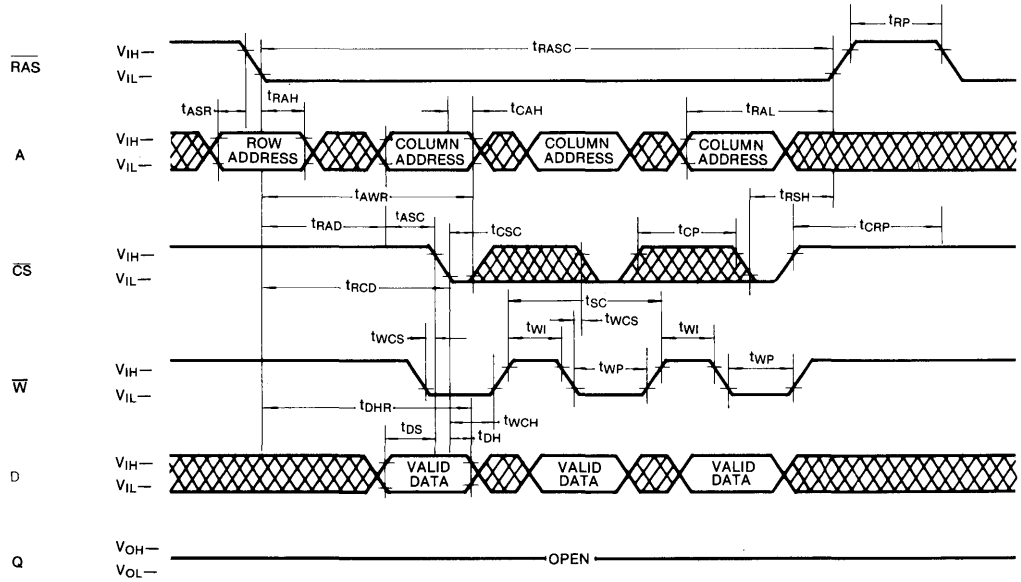


STATIC COLUMN MODE READ CYCLE

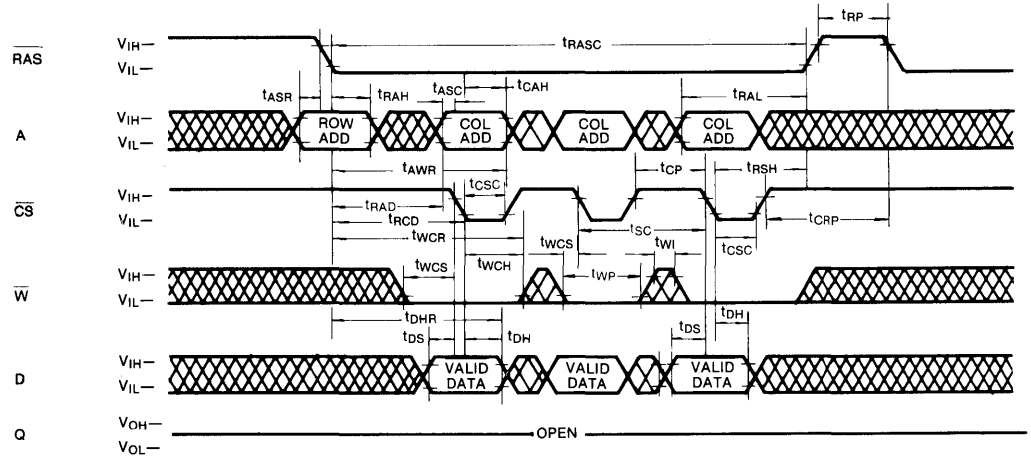


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)



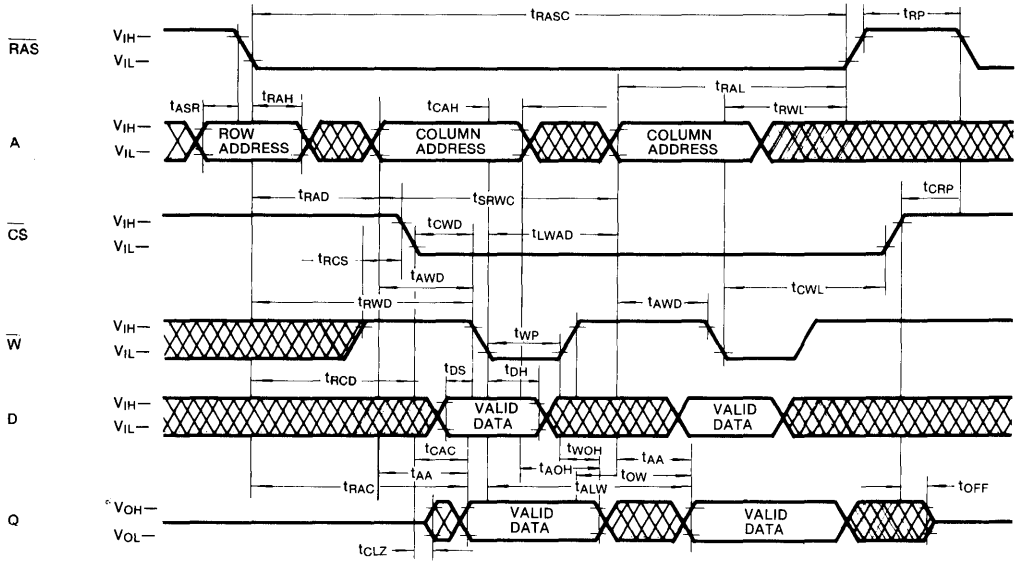
STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



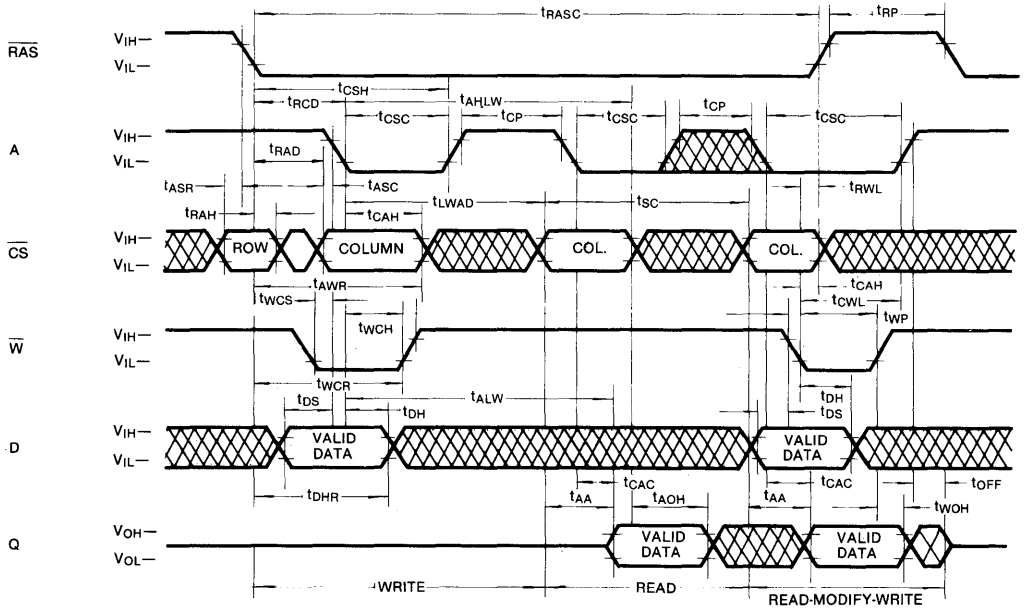
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



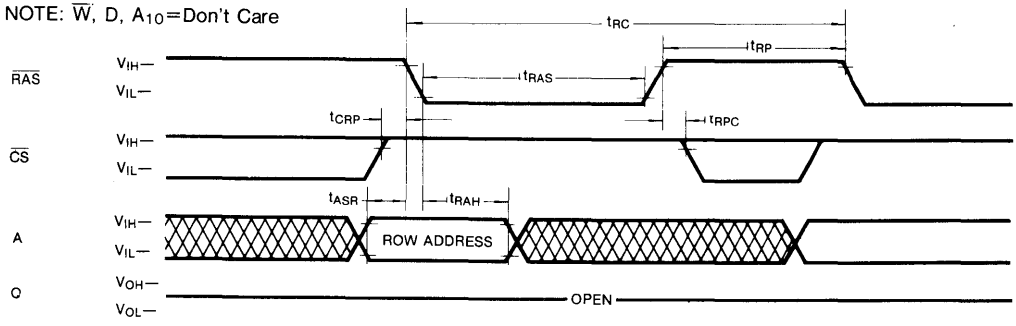
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

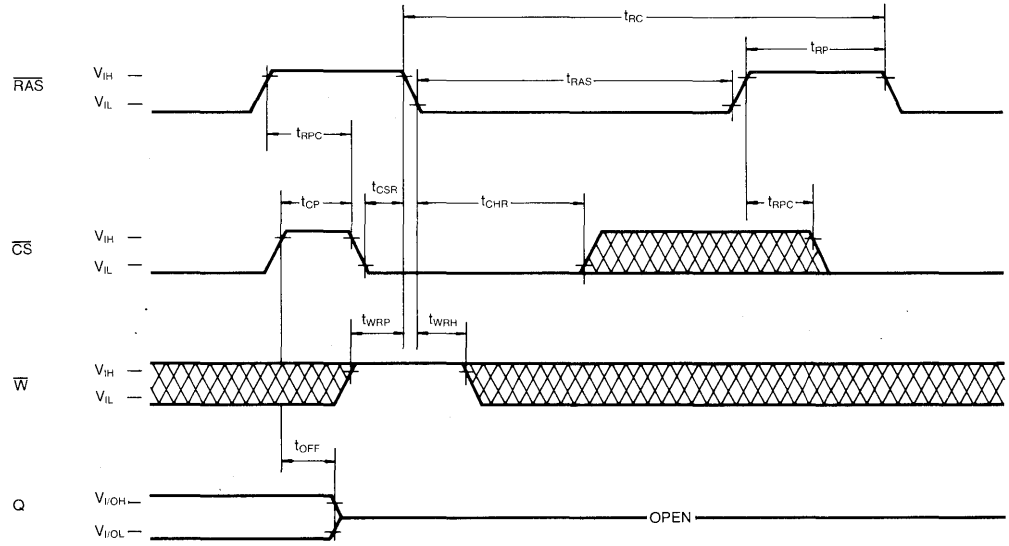
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D, A_{10}=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

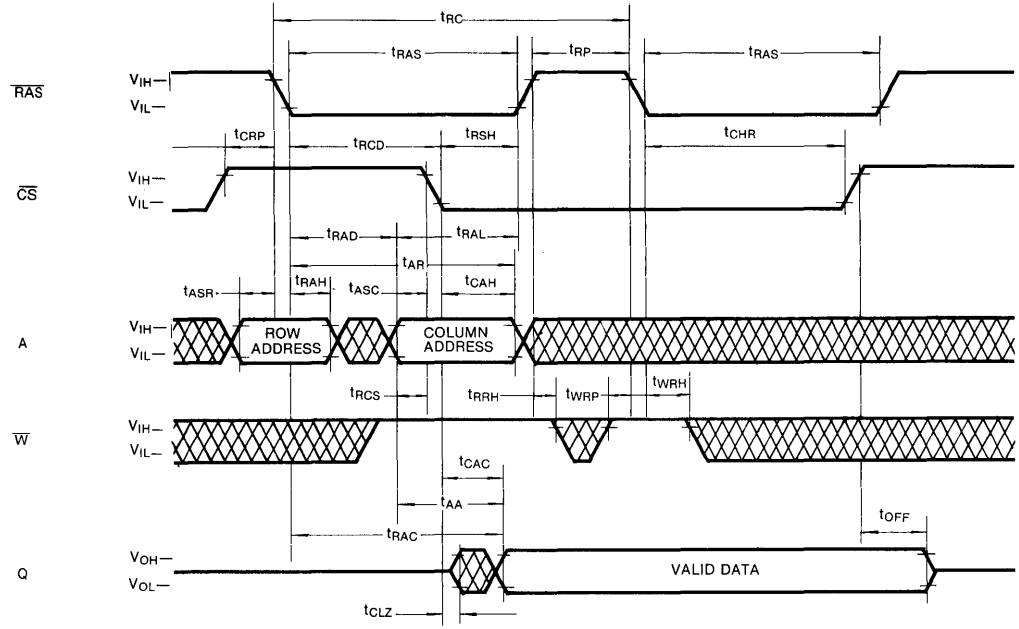
NOTE: Address=Don't Care



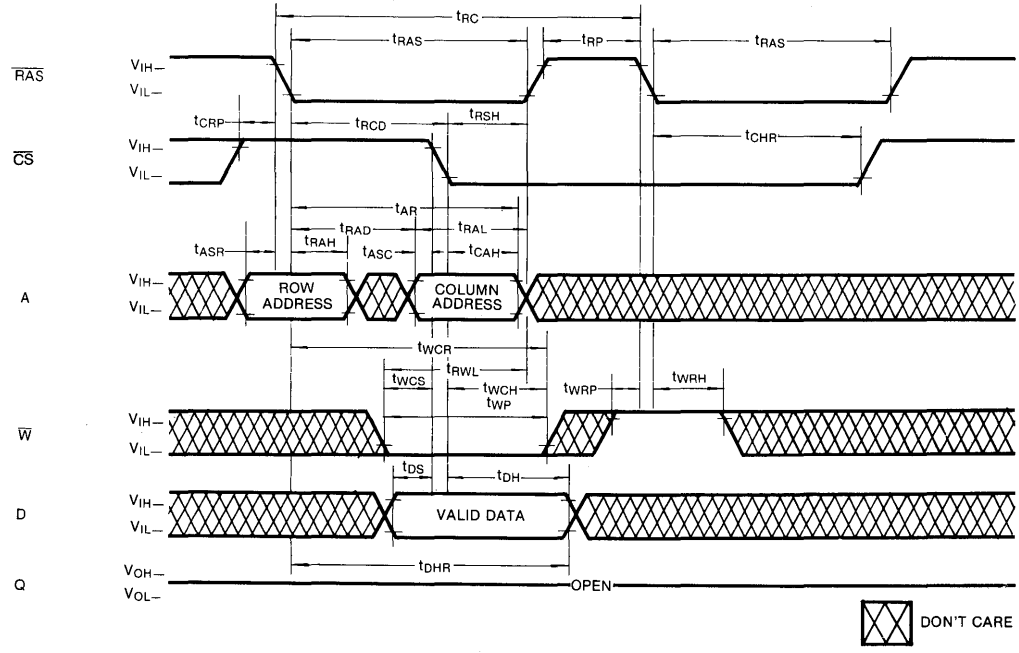
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

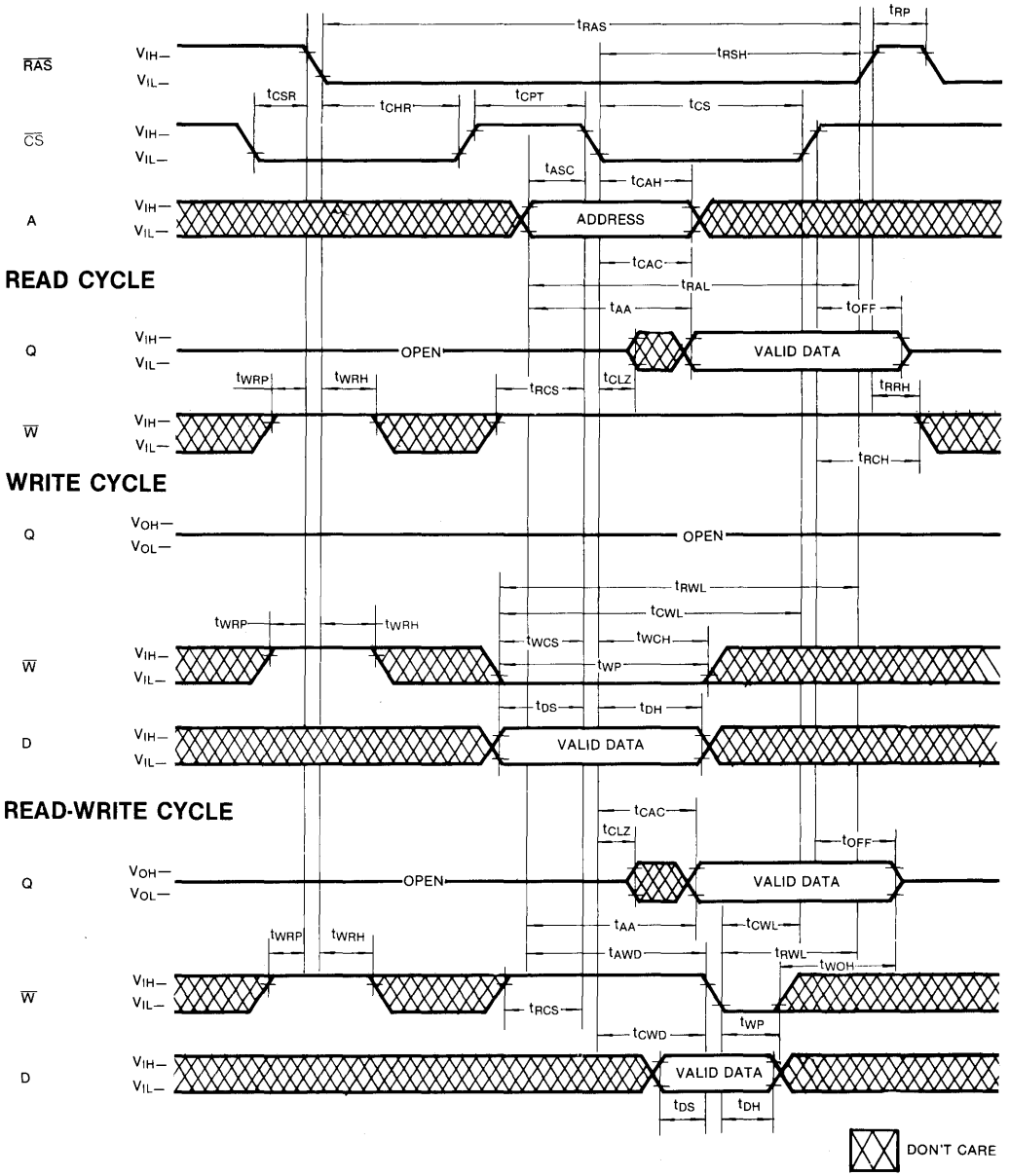


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

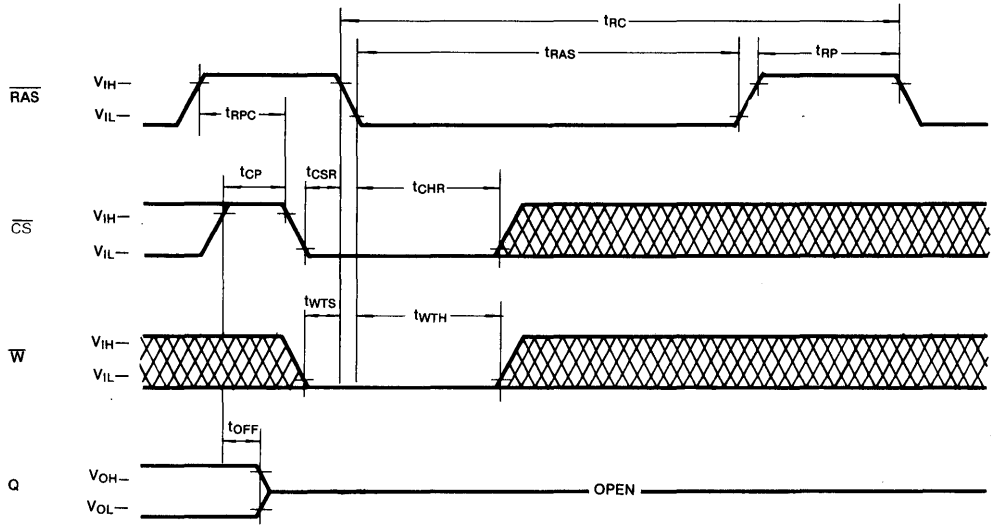
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address= Don't Care



TEST MODE DESCRIPTION

The KM41C4002 is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{OC} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4002 contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002 has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip sellect input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM41C4002 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C4002 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C4002 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002 has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4002 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Staic Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

DEVICE OPERATION (Continued)

Refresh

The data in the KM41C4002 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C4002 has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C4002 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter falling edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. The A_{10} bit is set high internally.

Column ADdress—Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

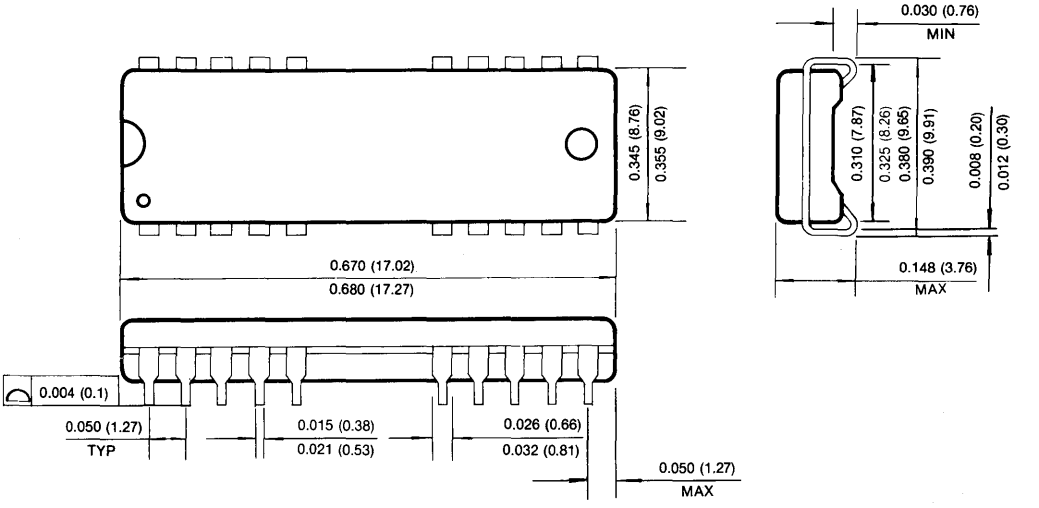
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4002 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh before proper device operation is achived.

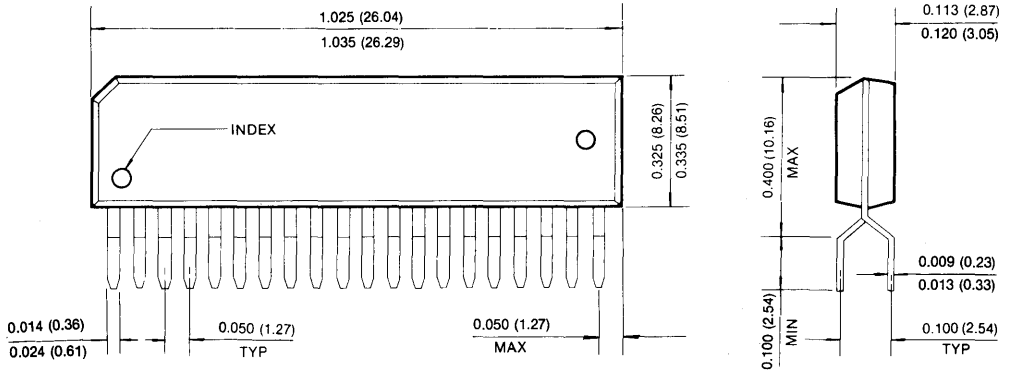
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000A- 7	70ns	20ns	130ns
KM41C4000A- 8	80ns	20ns	150ns
KM41C4000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

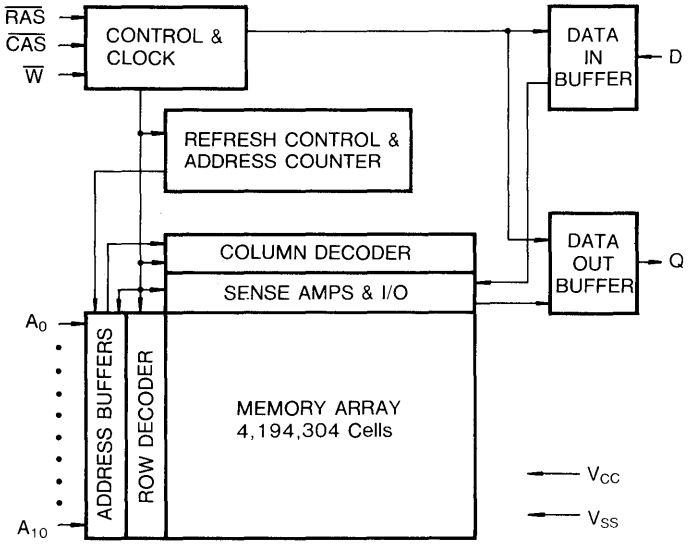
The Samsung KM41C4000A is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

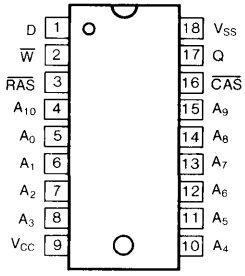
The KM41C4000A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



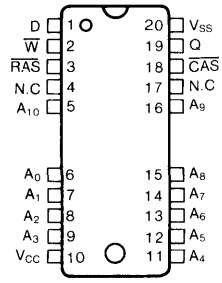
PIN CONFIGURATION (Top Views)

• KM41C4000AP



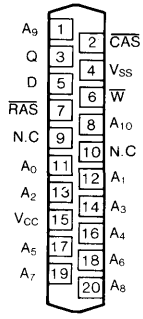
(DIP)

• KM41C4000AJ



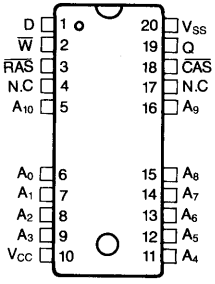
(SOJ)

• KM41C4000AZ



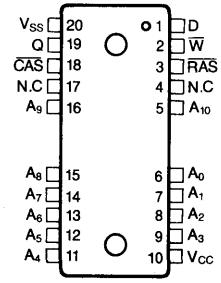
(ZIP)

• KM41C4000AT



(TSOP(II)-Forward Type)

• KM41C4000ATR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000A- 7	I_{CC1}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000A- 7	I_{CC3}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000A- 7	I_{CC4}	—	80	mA
	KM41C4000A- 8		—	70	mA
	KM41C4000A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000A- 7	I_{CC6}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

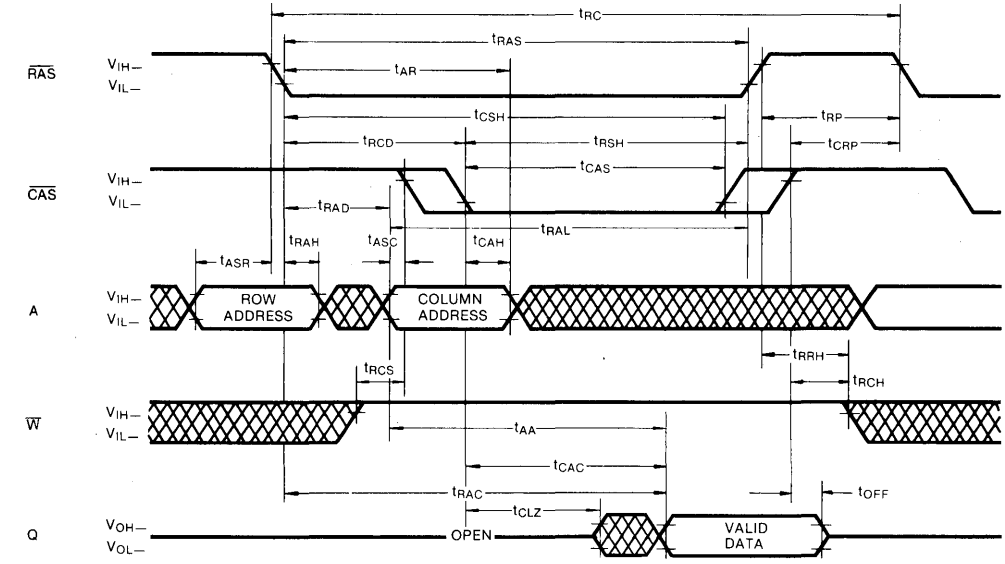
Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

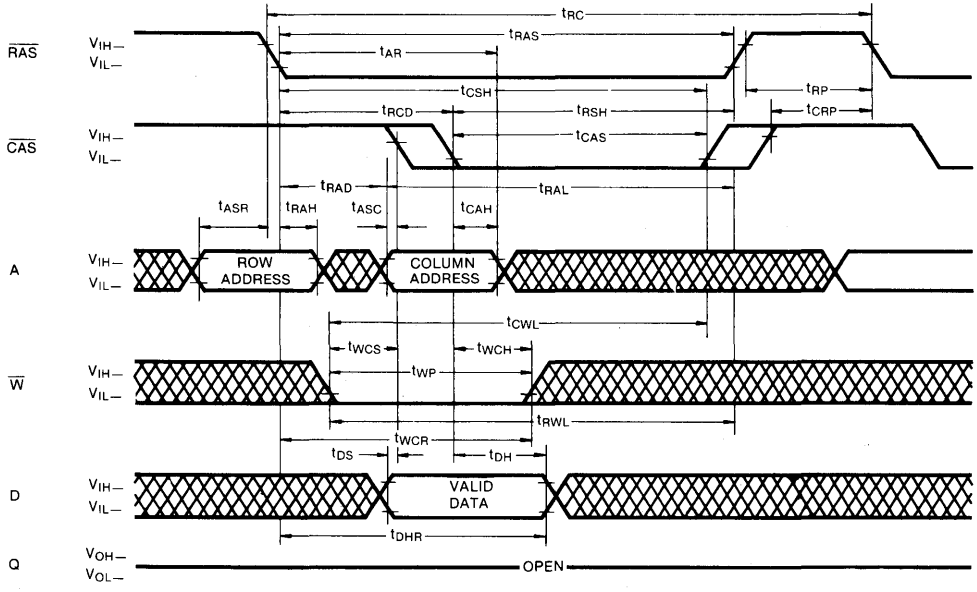
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



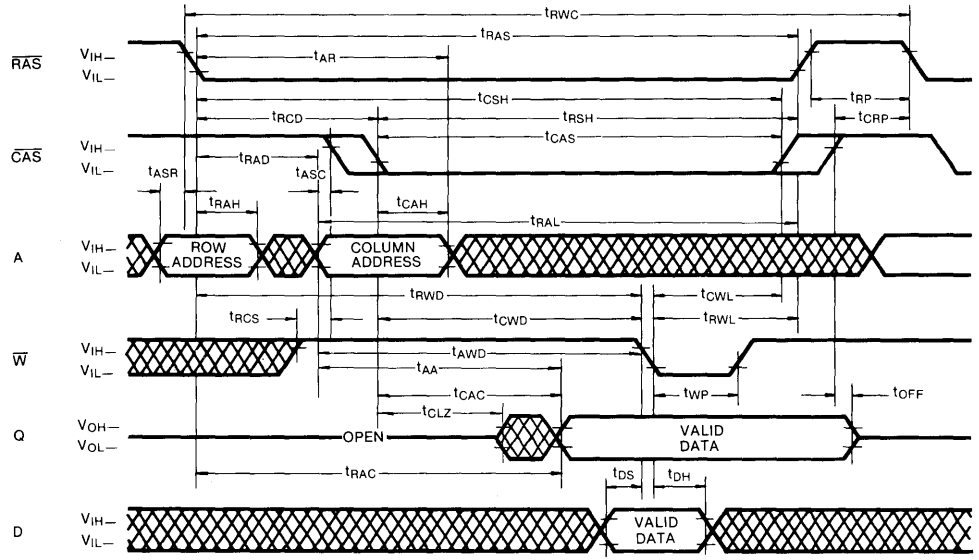
WRITE CYCLE (EARLY WRITE)



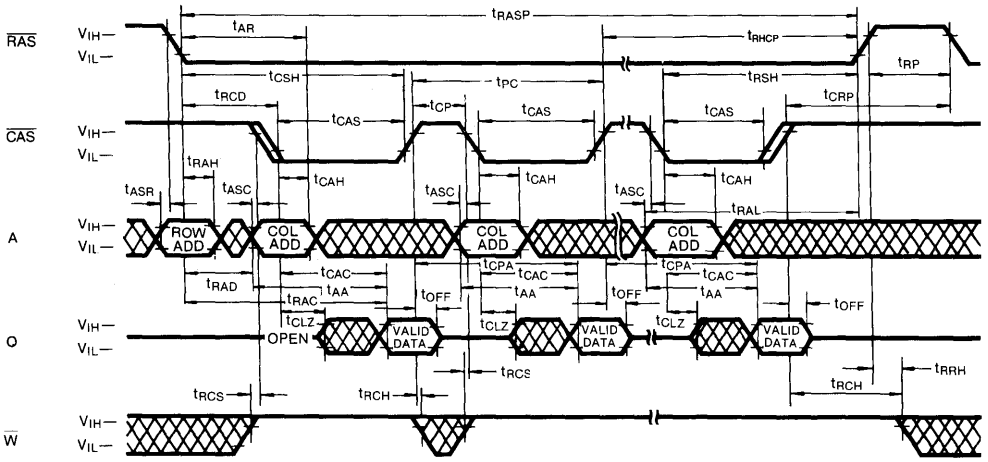
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



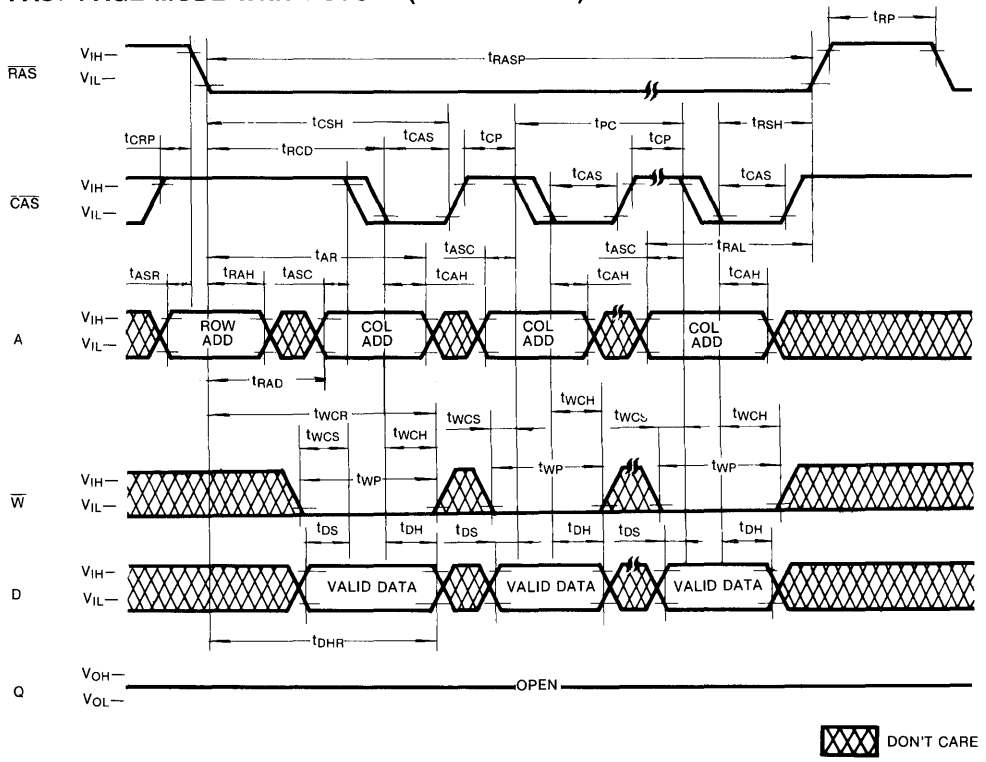
FAST PAGE MODE READ CYCLE



DON'T CARE

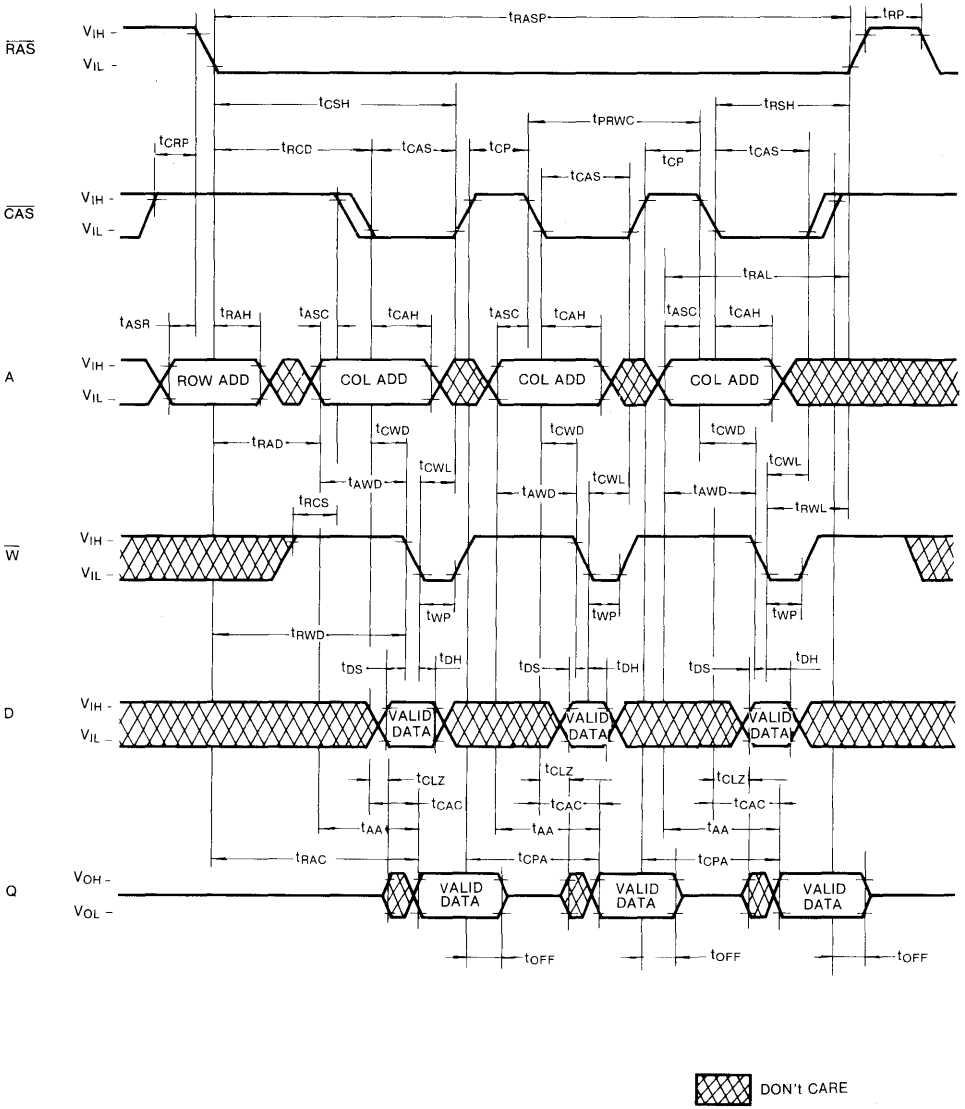
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

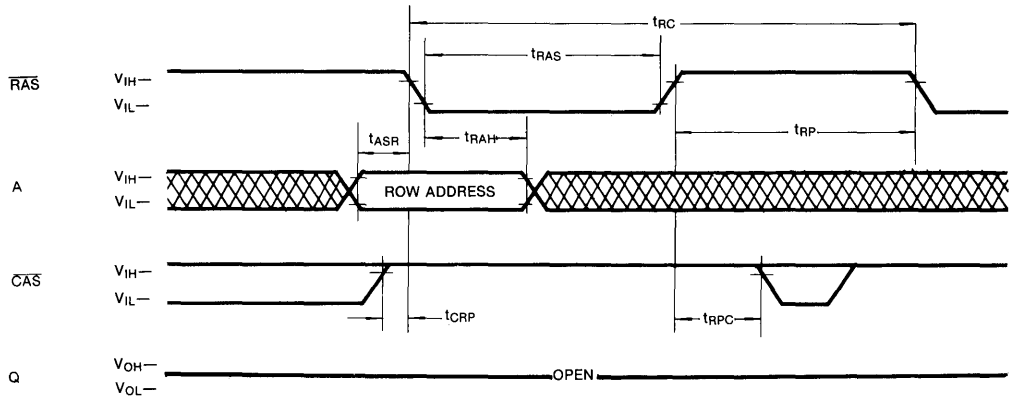
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

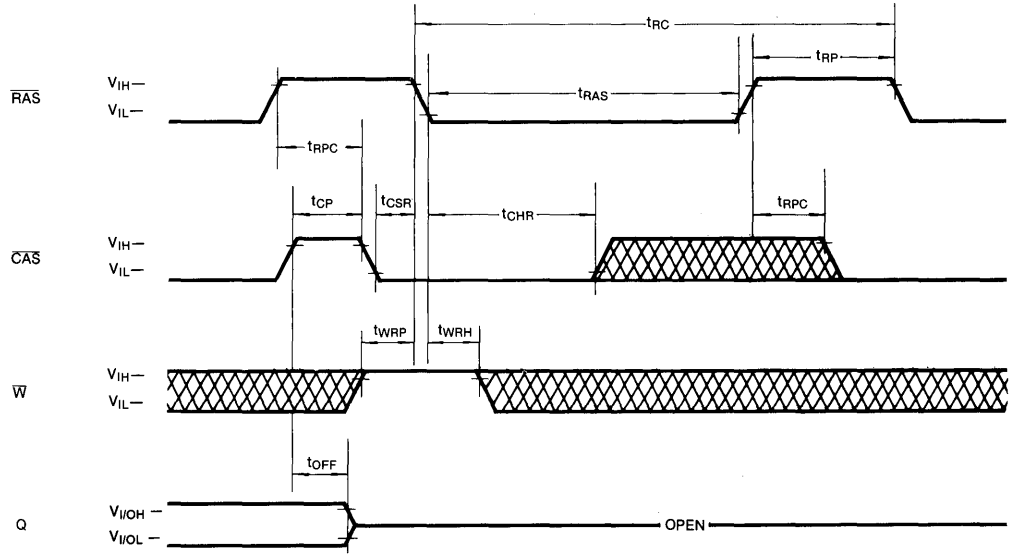
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



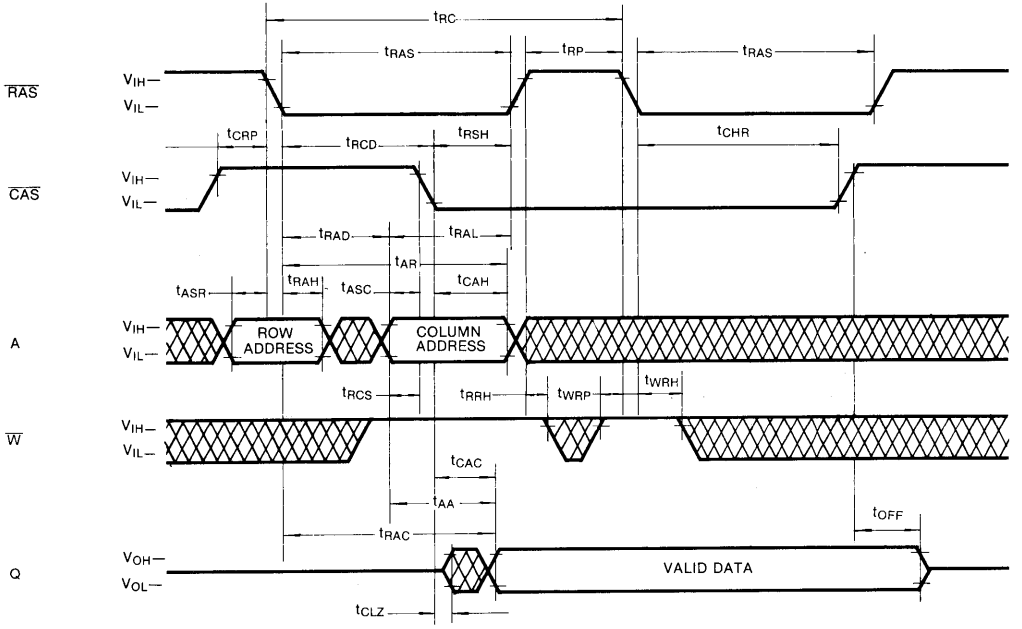
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

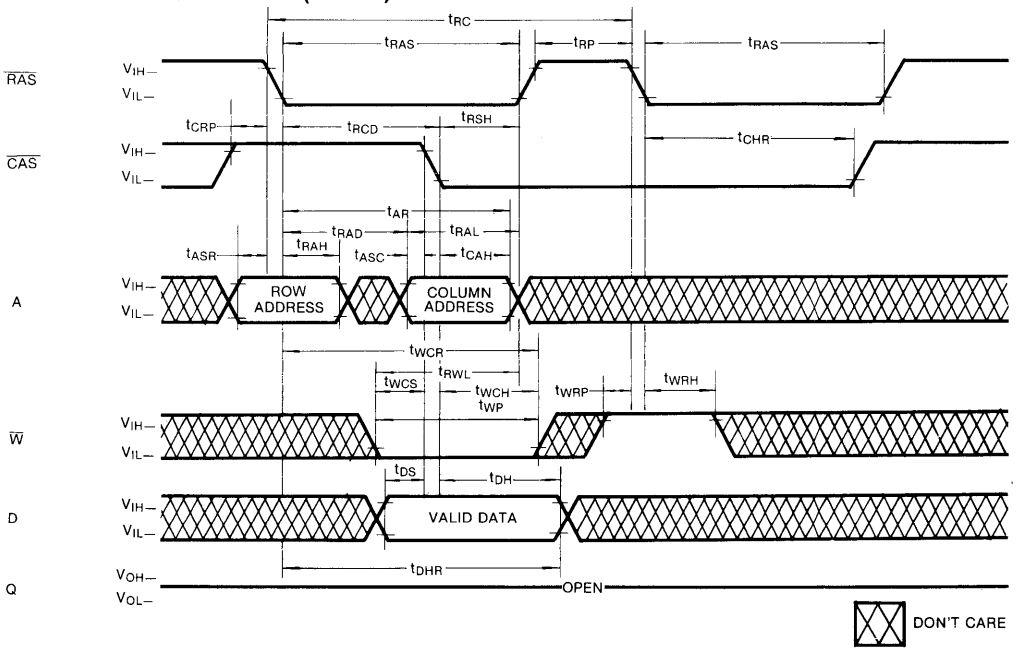


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

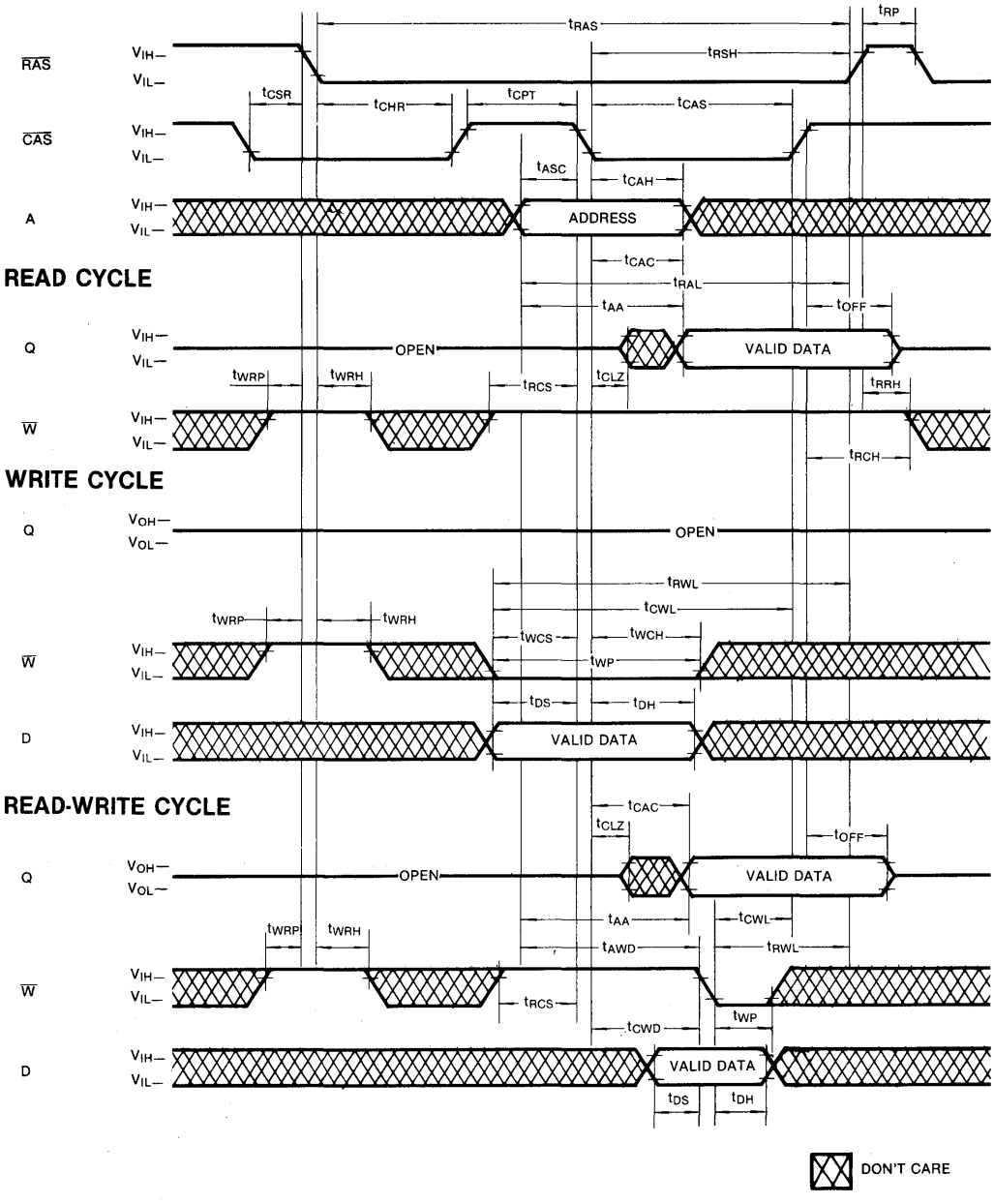


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

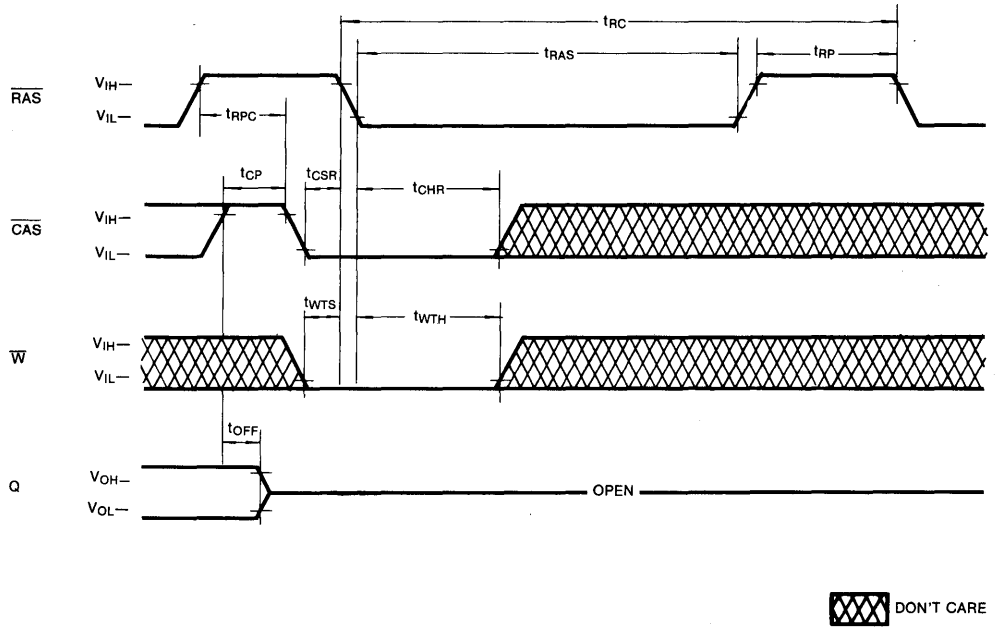
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address = Don't Care



TEST MODE DESCRIPTION

The KM41C4000A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000A begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000A has a three-state output buffer which which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

DEVICE OPERATION (Continued)

Refresh

The data in the KM41C4000A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000A has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

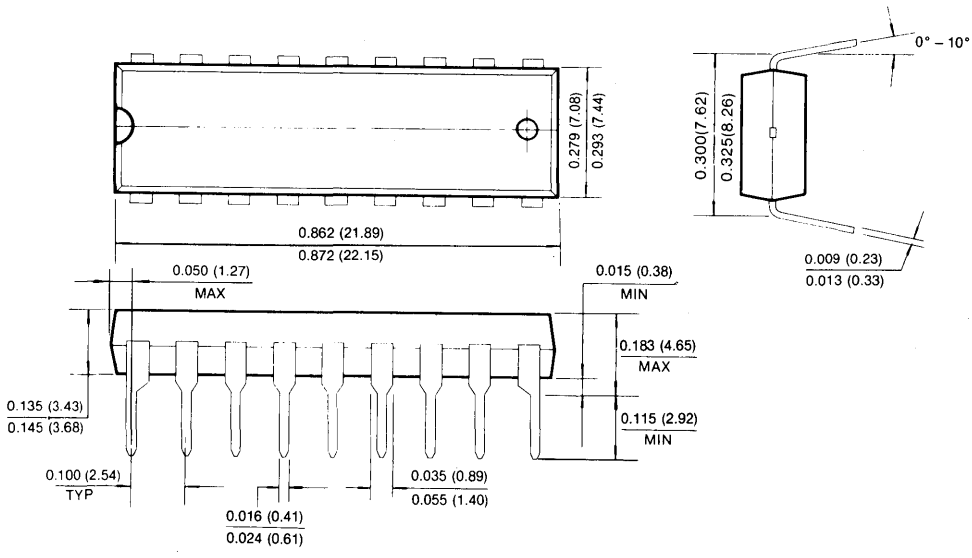
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4000A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

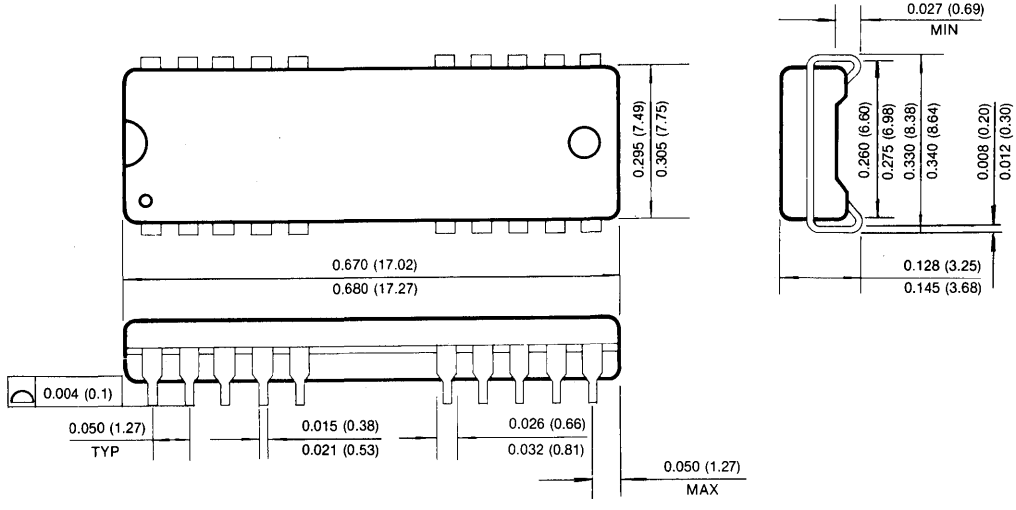
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



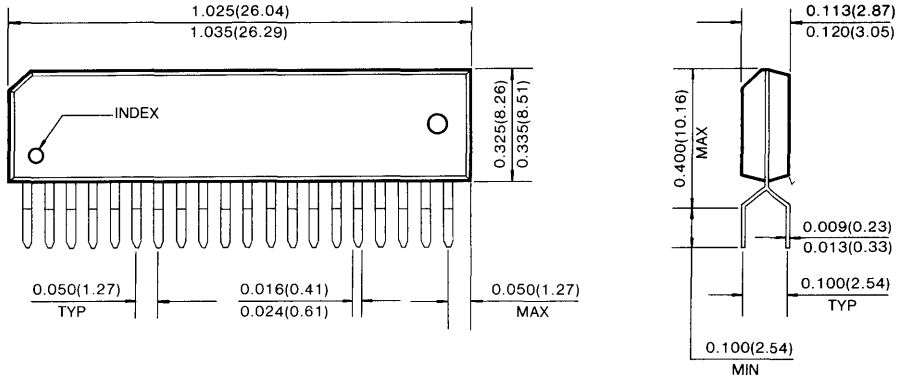
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



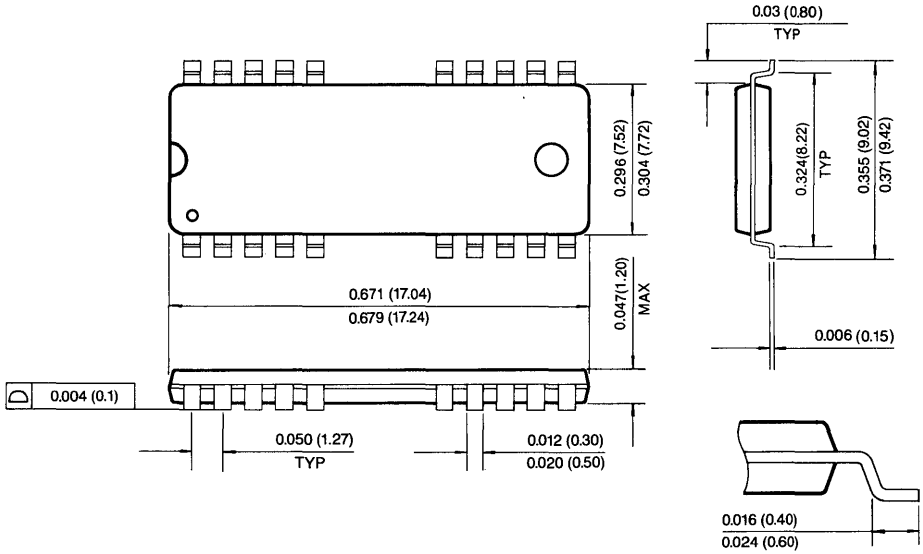
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000AL- 7	70ns	20ns	130ns
KM41C4000AL- 8	80ns	20ns	150ns
KM41C4000AL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/128ms refresh**
- **Low power dissipation**
  - **—Standby: 1.1mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

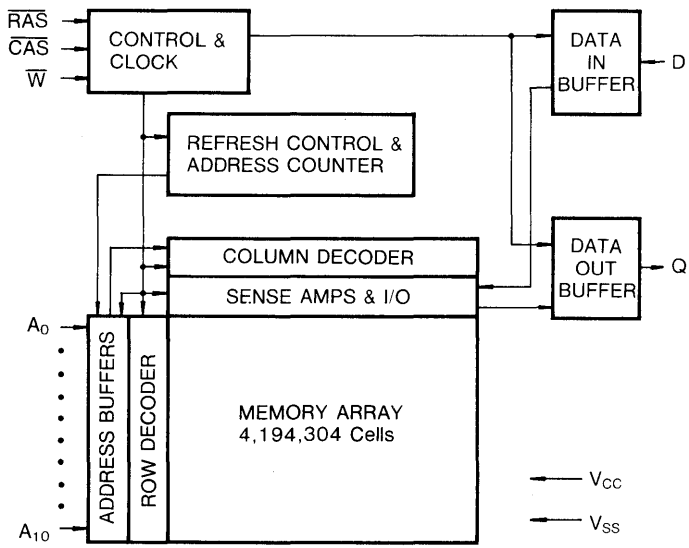
The Samsung KM41C4000AL is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000AL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

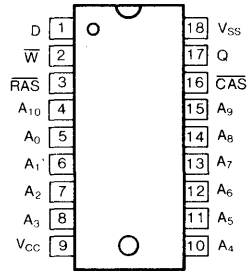
The KM41C4000AL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



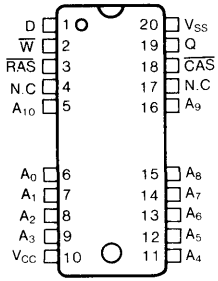
PIN CONFIGURATION (Top Views)

• KM41C4000ALP



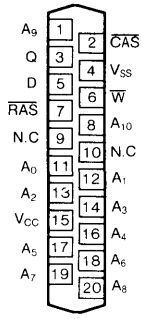
(DIP)

• KM41C4000ALJ



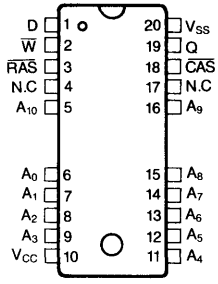
(SOJ)

• KM41C4000ALZ



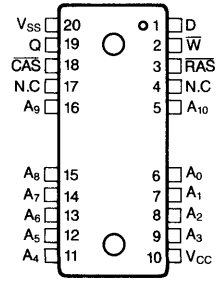
(ZIP)

• KM41C4000ALT



(TSOP(II)-Forward Type)

• KM41C4000ALTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000AL- 7	I_{CC1}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000AL- 7	I_{CC3}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000AL- 7	I_{CC4}	—	80	mA
	KM41C4000AL- 8		—	70	mA
	KM41C4000AL-10		—	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W} \geq V_{CC}-0.2V$)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000AL- 7	I_{CC6}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}=\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125μS, $T_{RAS}=t_{RAS}$ min.~1μS		I_{CC7}	—	300	μA
Standby Current ($\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

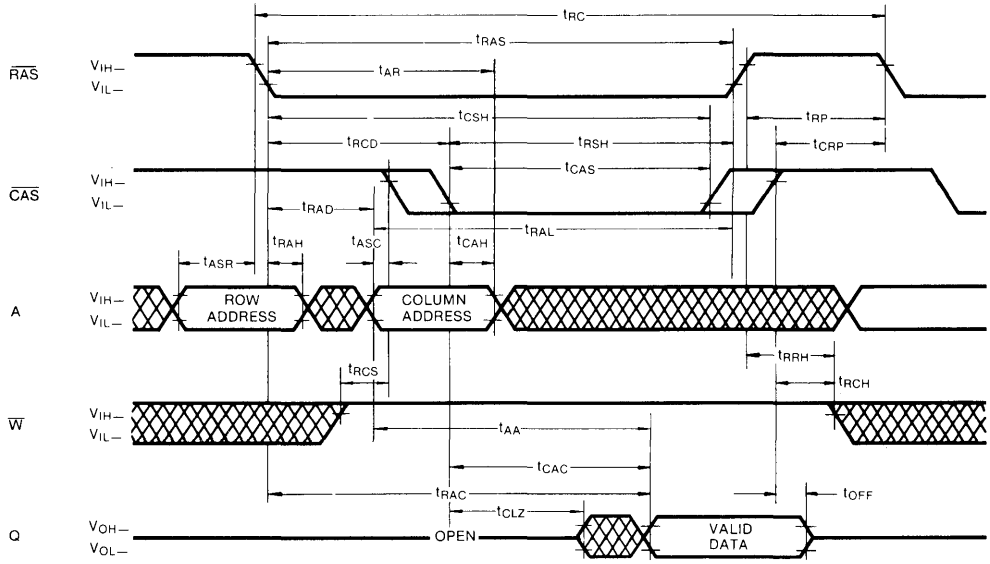
Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	$_{RWD}$	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

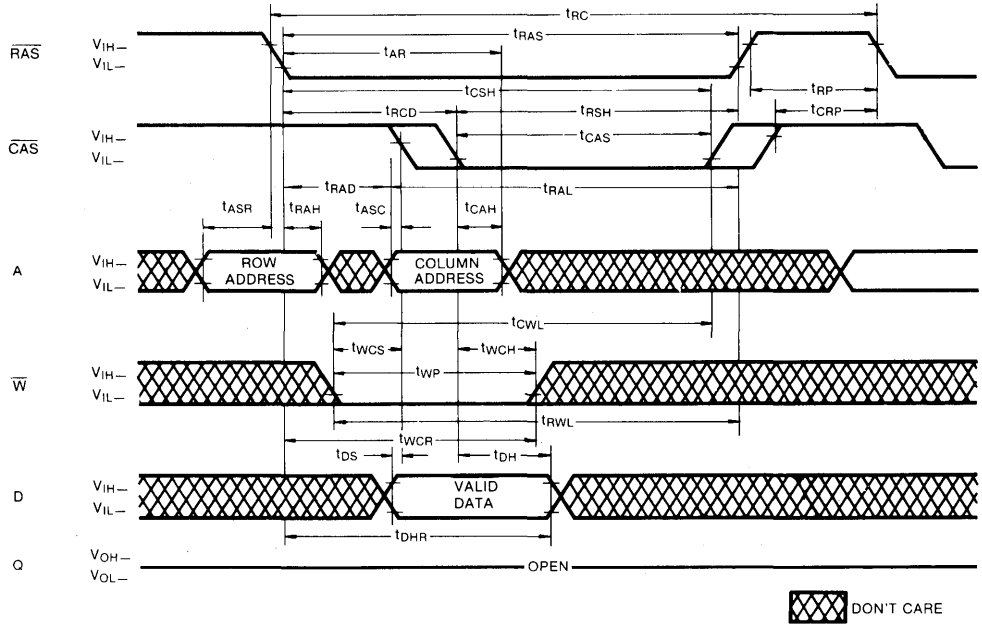
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE

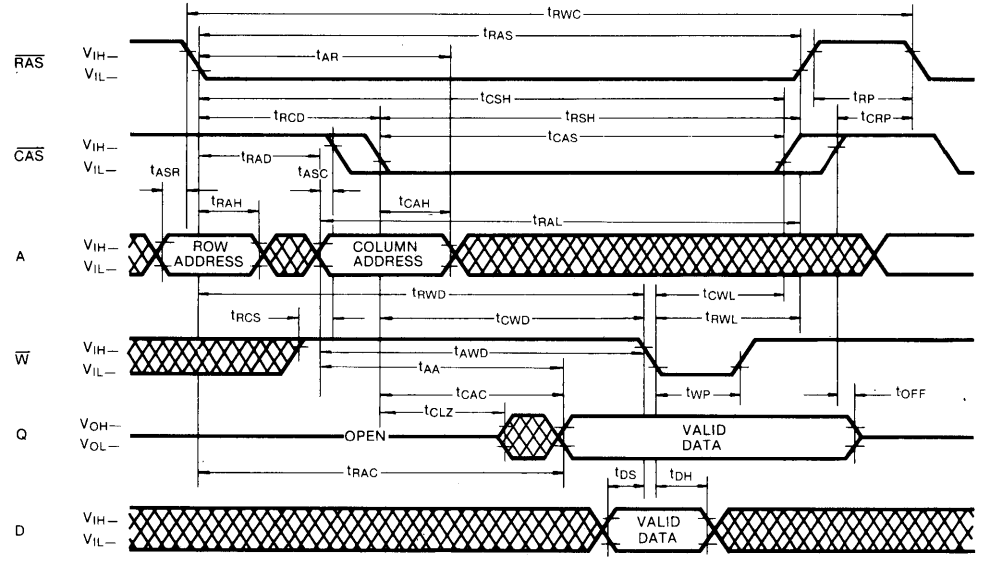


WRITE CYCLE (EARLY WRITE)

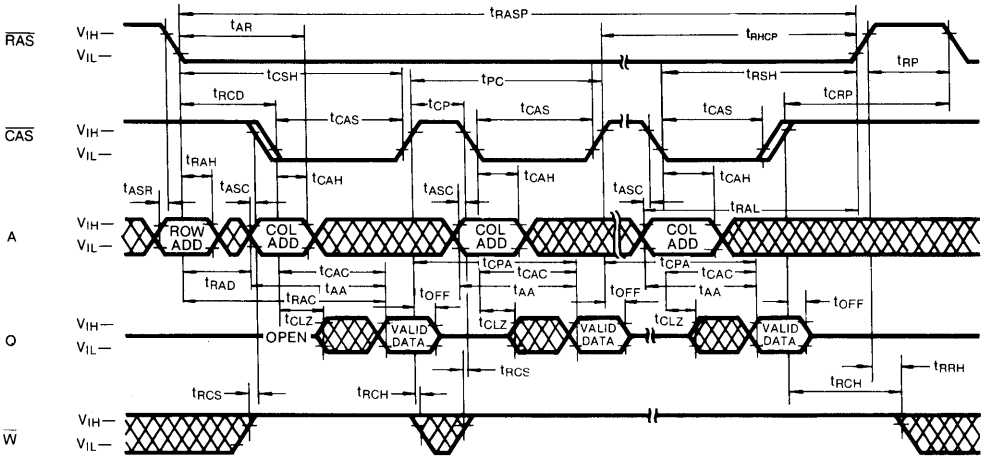


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



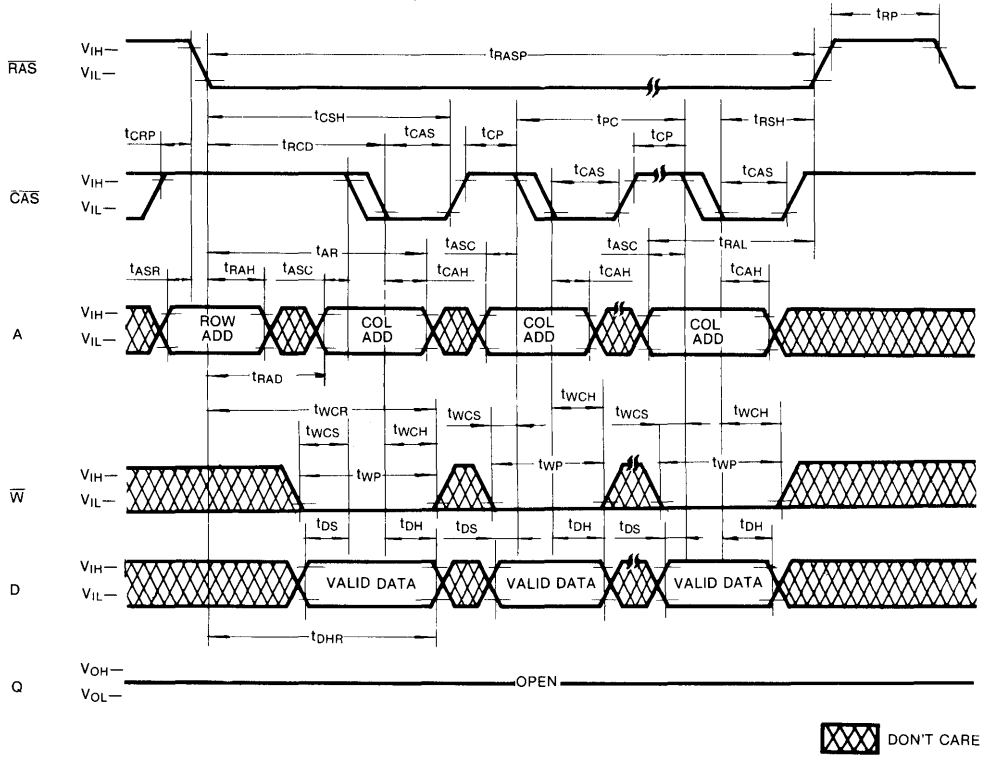
FAST PAGE MODE READ CYCLE



DON'T CARE

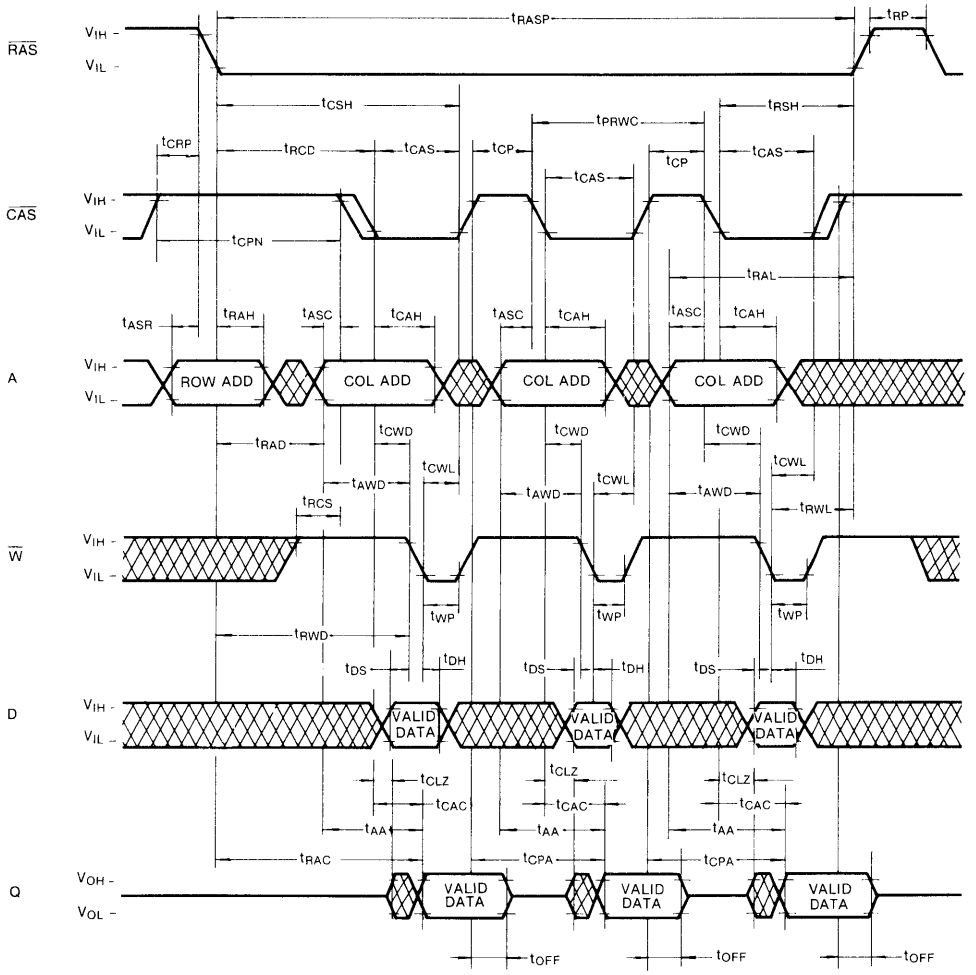
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

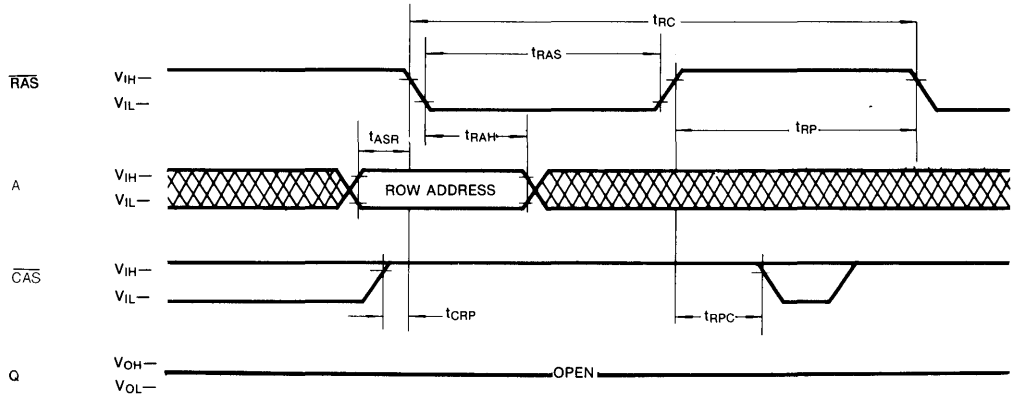
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

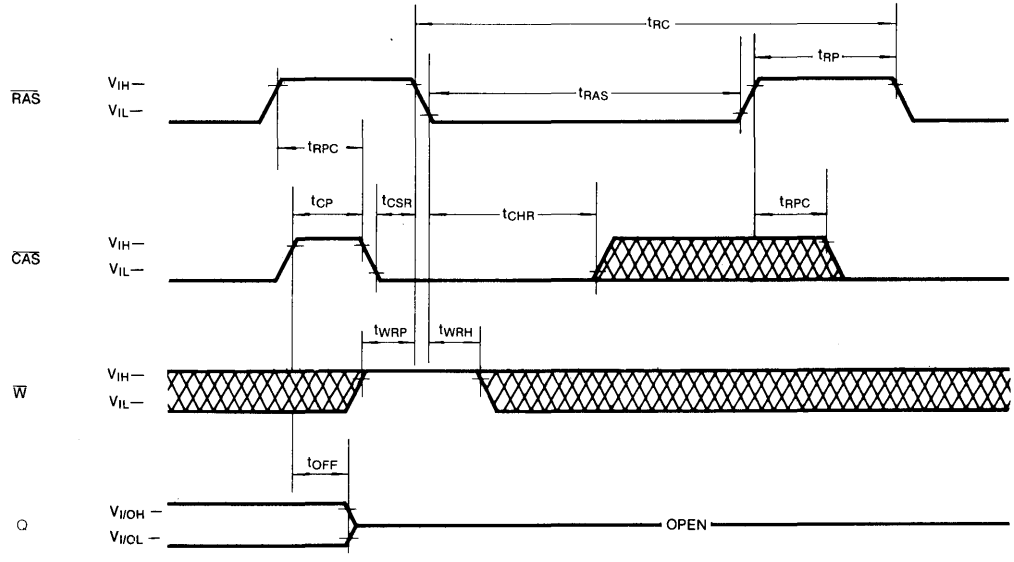
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



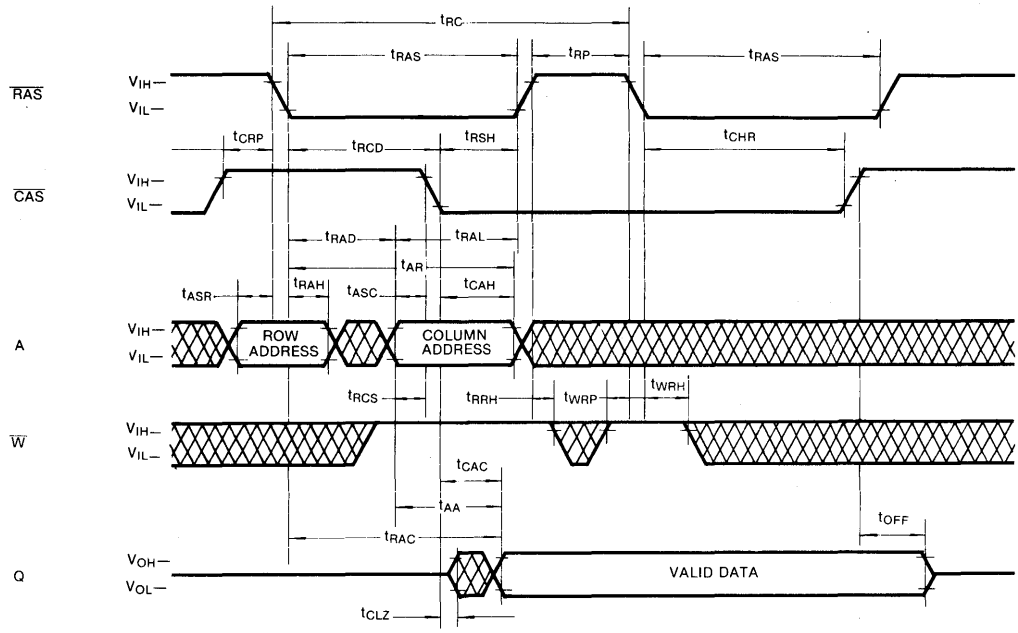
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

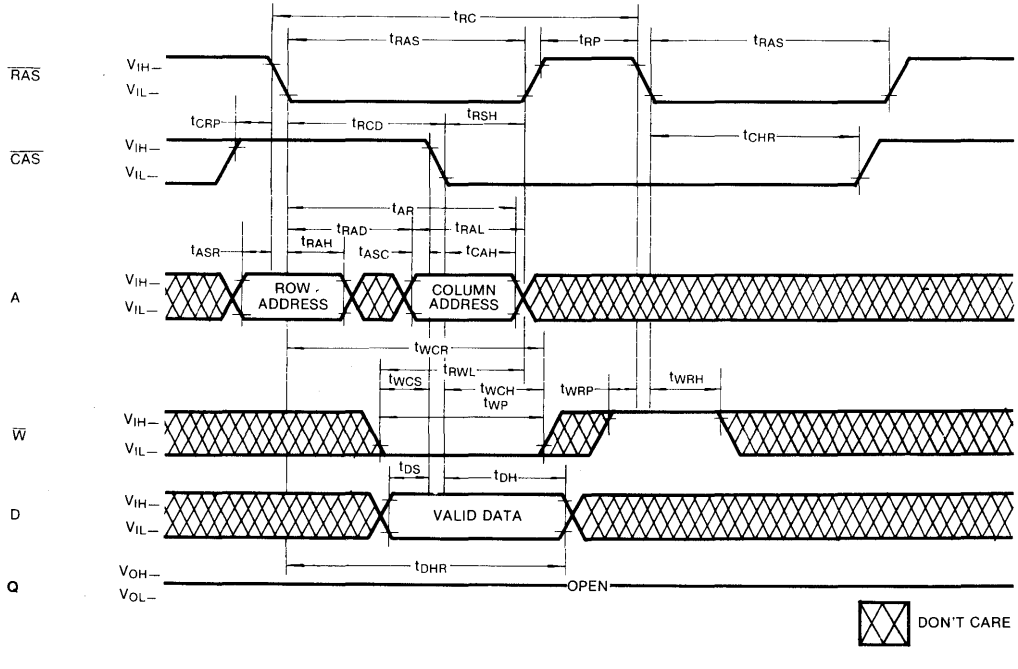


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

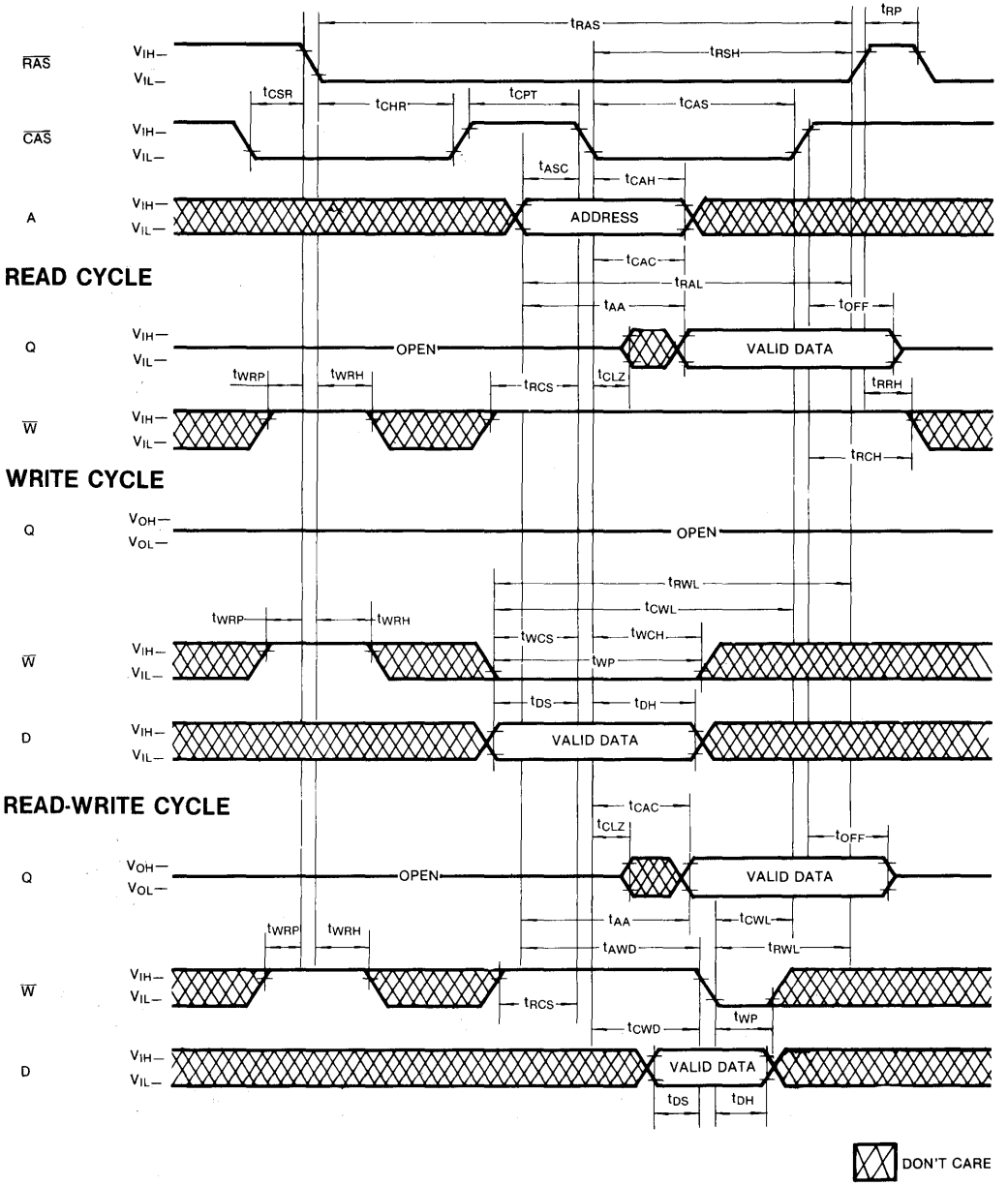


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

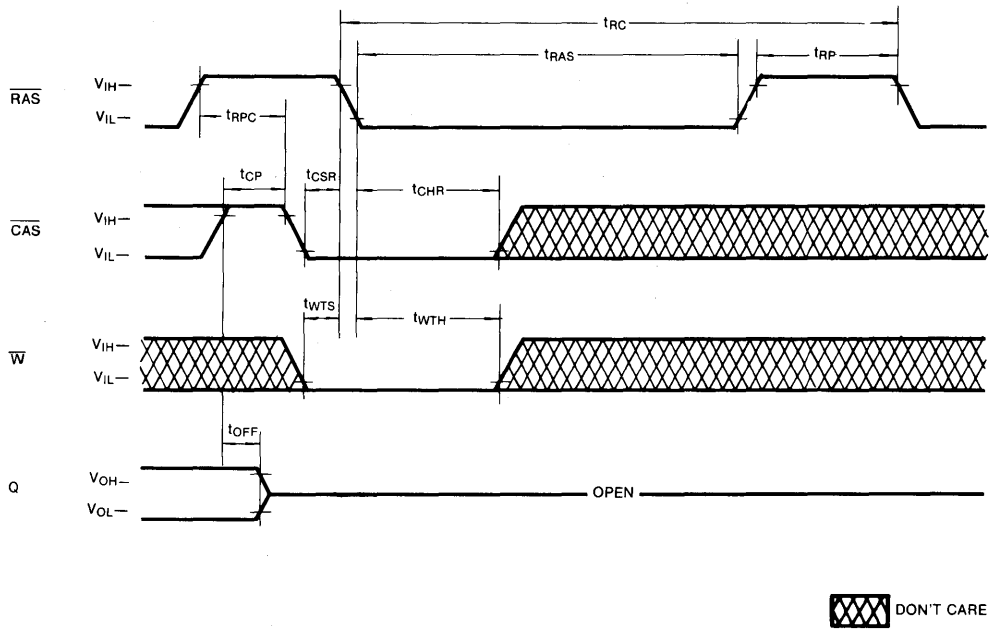
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address= Don't care



TEST MODE DESCRIPTION

The KM41C4000AL is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before $\overline{RAS}$-Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000AL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000AL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000AL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000AL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000AL begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000AL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000AL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000AL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000AL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000AL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000AL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000AL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000AL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

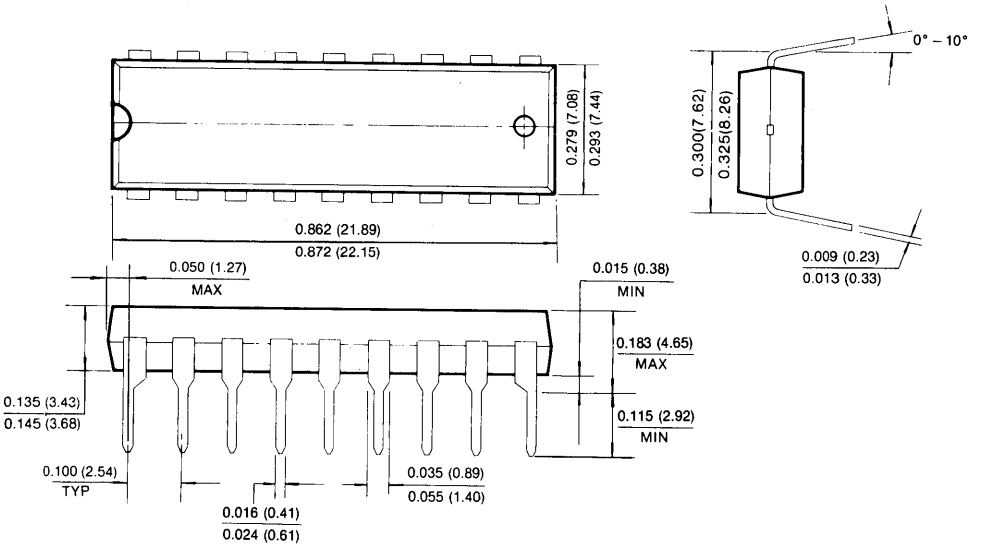
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4000AL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

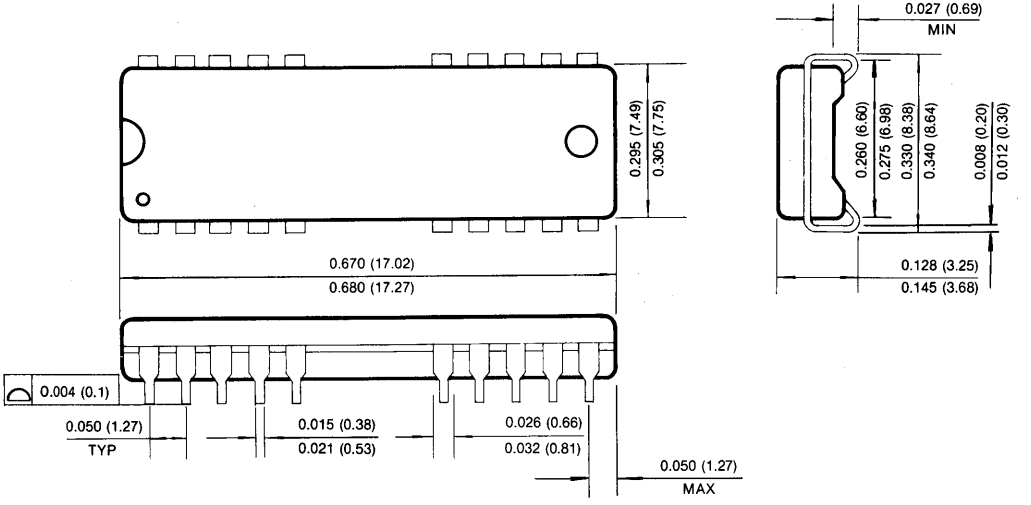
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



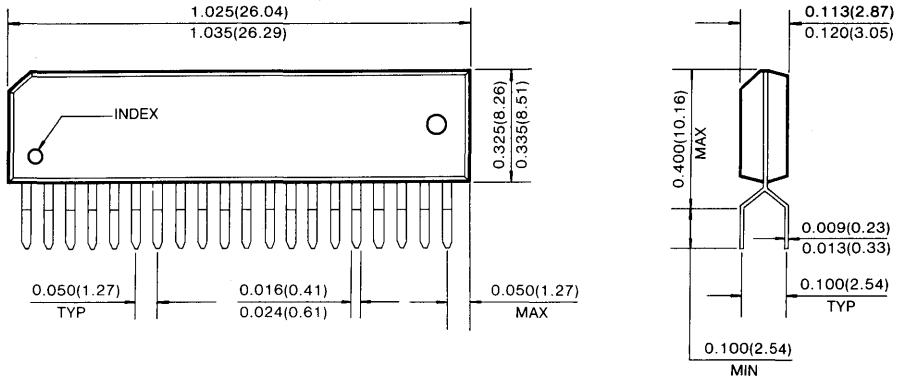
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



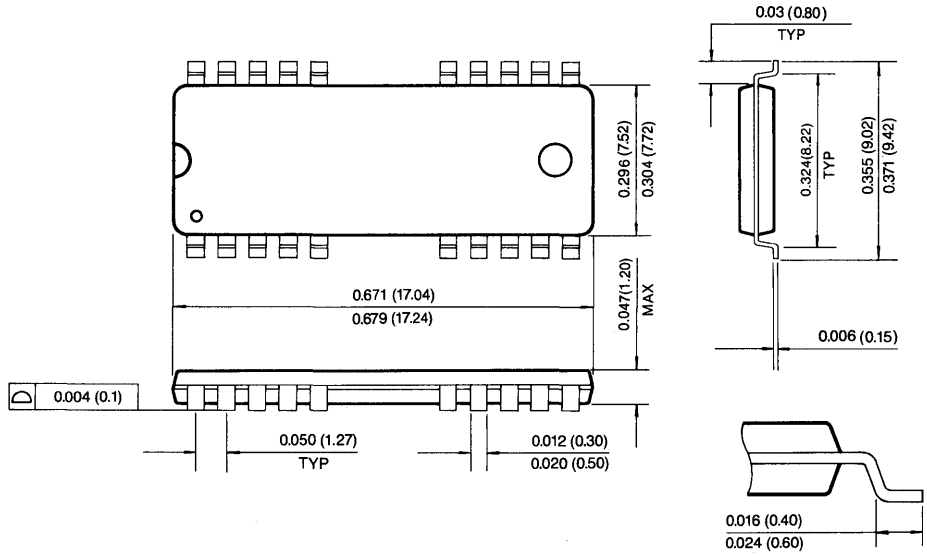
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000ASL- 7	70ns	20ns	130ns
KM41C4000ASL- 8	80ns	20ns	150ns
KM41C4000ASL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/256ms refresh**
- **Low power dissipation**
  - **—Standby: 0.6mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

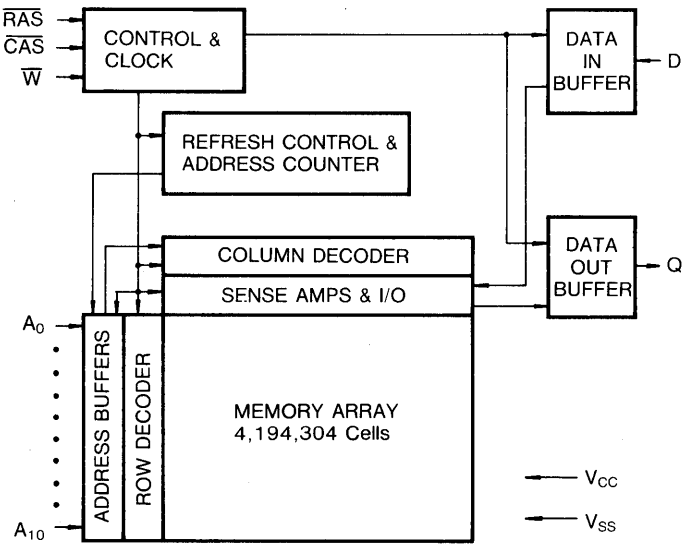
The Samsung KM41C4000ASL is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

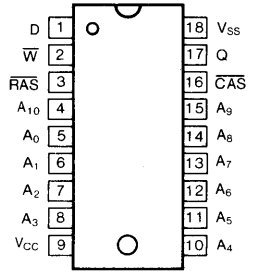
The KM41C4000ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



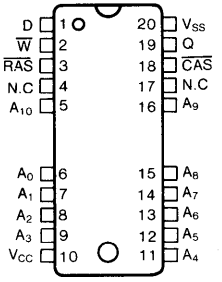
PIN CONFIGURATION (Top Views)

• KM41C4000ASLP



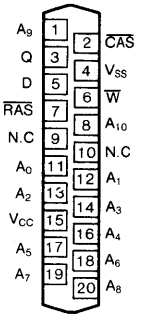
(DIP)

• KM41C4000ASLJ



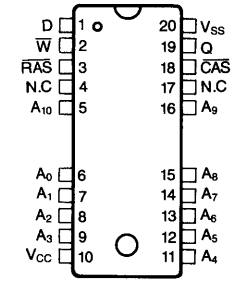
(SOJ)

• KM41C4000ASLZ



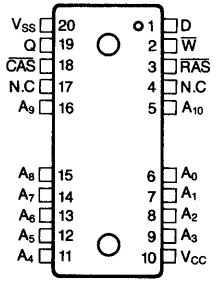
(ZIP)

• KM41C4000ASLT



(TSOP(II)-Forward Type)

• KM41C4000ASLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000ASL- 7	I_{CC1}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
RAS-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000ASL- 7	I_{CC3}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000ASL- 7	I_{CC4}	—	80	mA
	KM41C4000ASL- 8		—	70	mA
	KM41C4000ASL-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}−0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000ASL- 7	I_{CC6}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Battery Back Up CurrentAverage Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=250μS, T_{RAS}=t_{RAS} min.~1μS		I_{CC7}	—	150	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page mode read-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

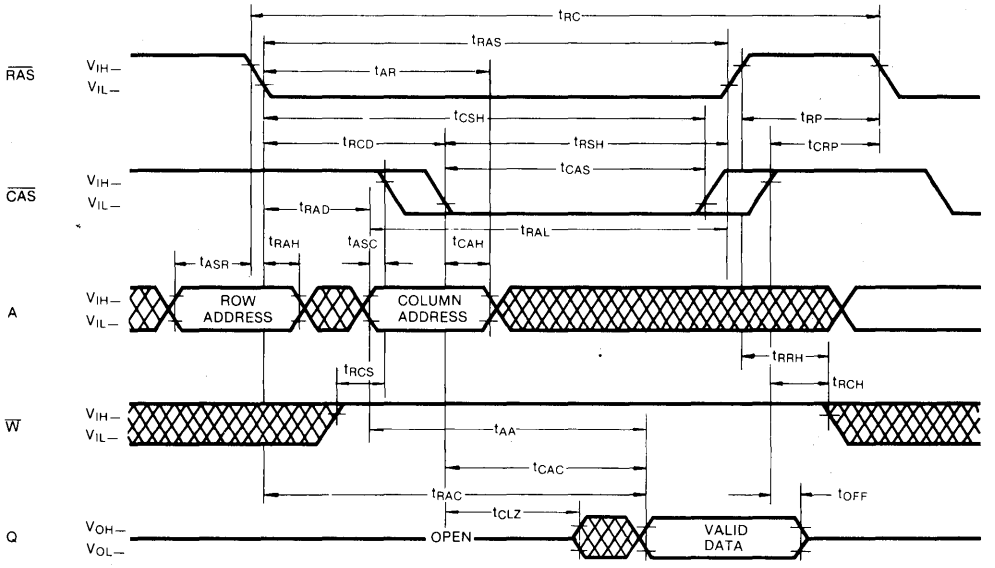
Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	$_{RWD}$	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

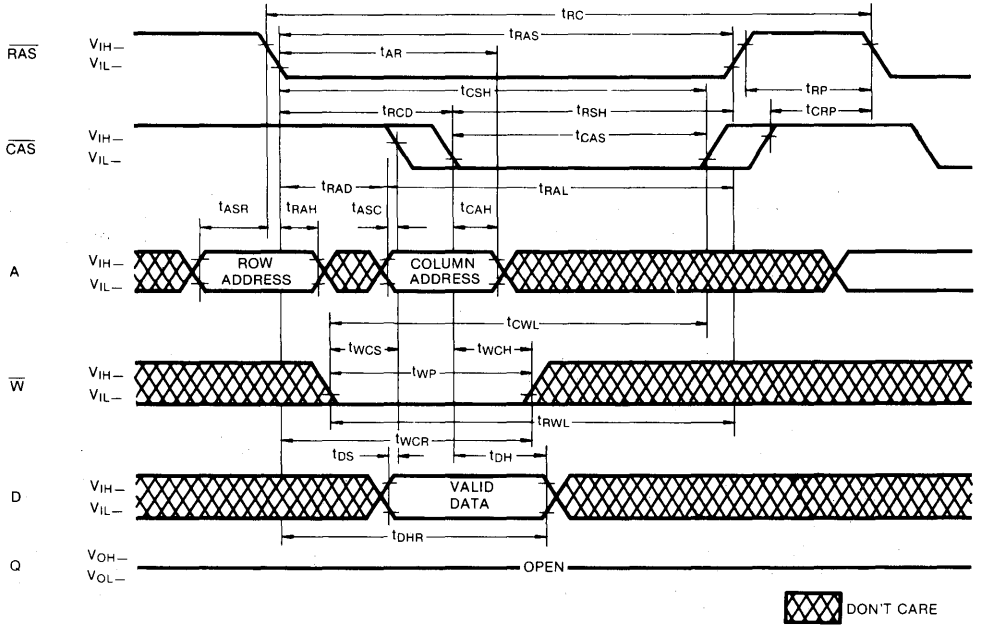
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refreferenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE

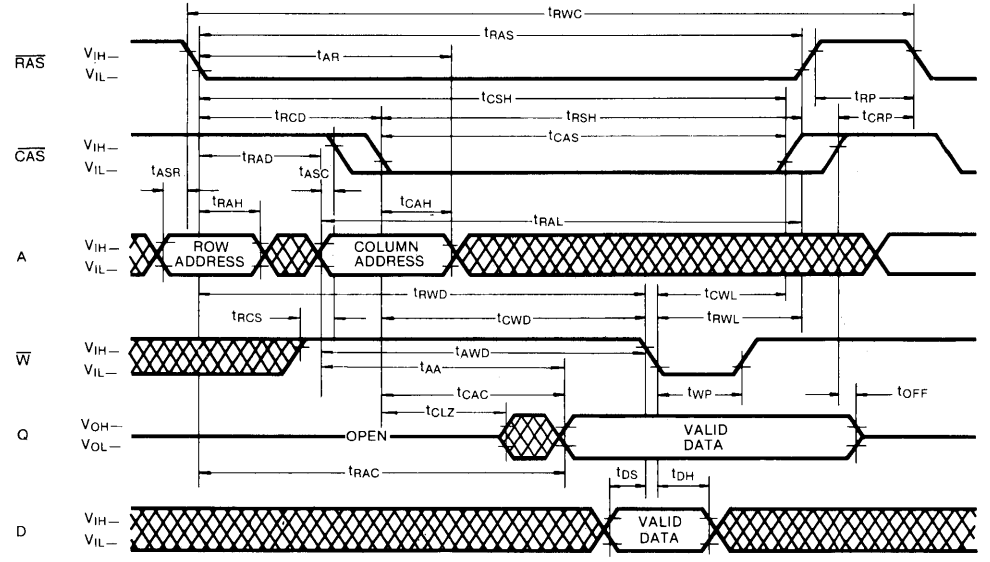


WRITE CYCLE (EARLY WRITE)

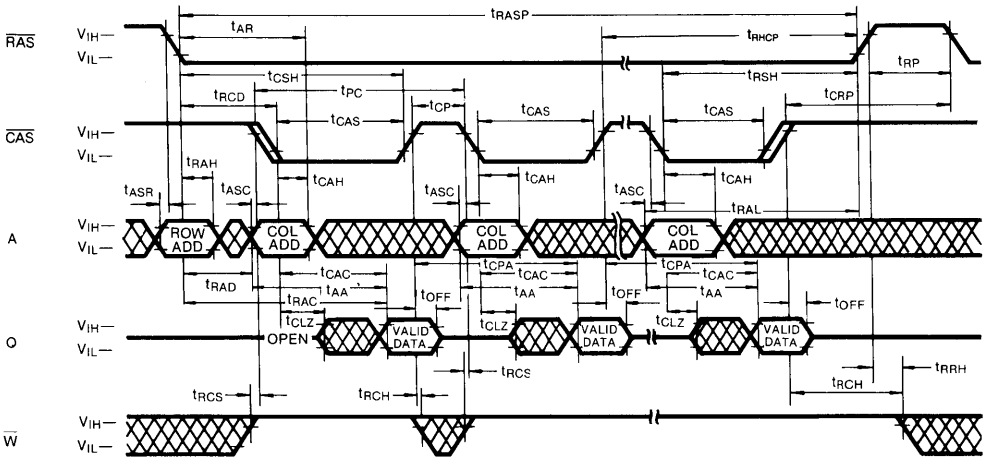


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



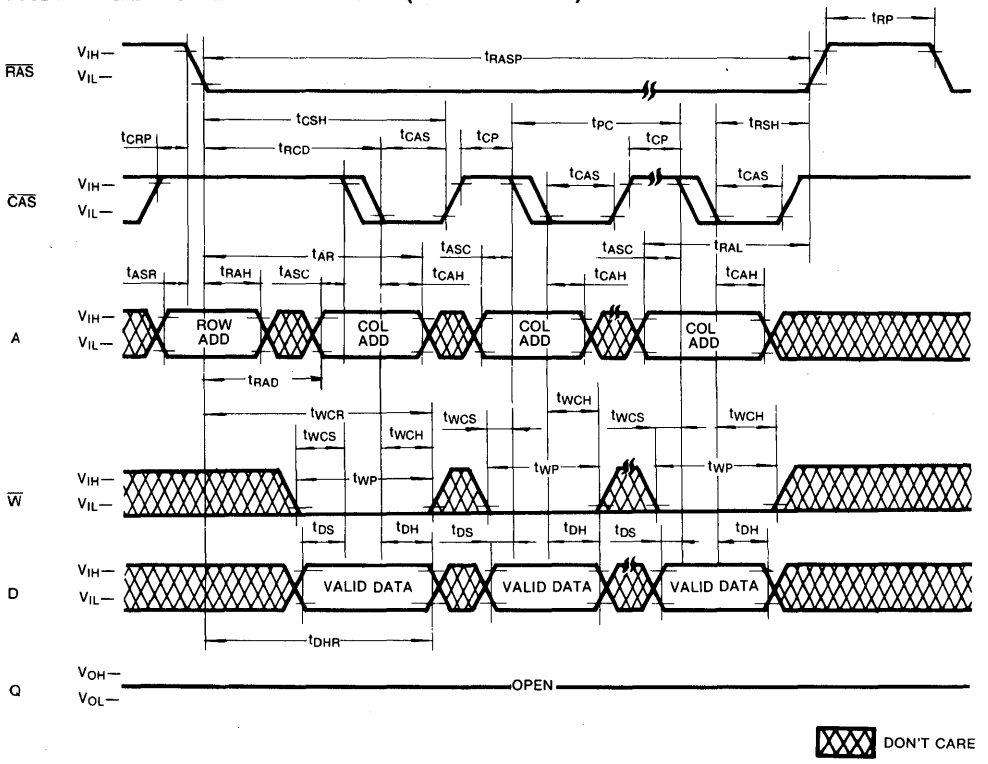
FAST PAGE MODE READ CYCLE



DON'T CARE

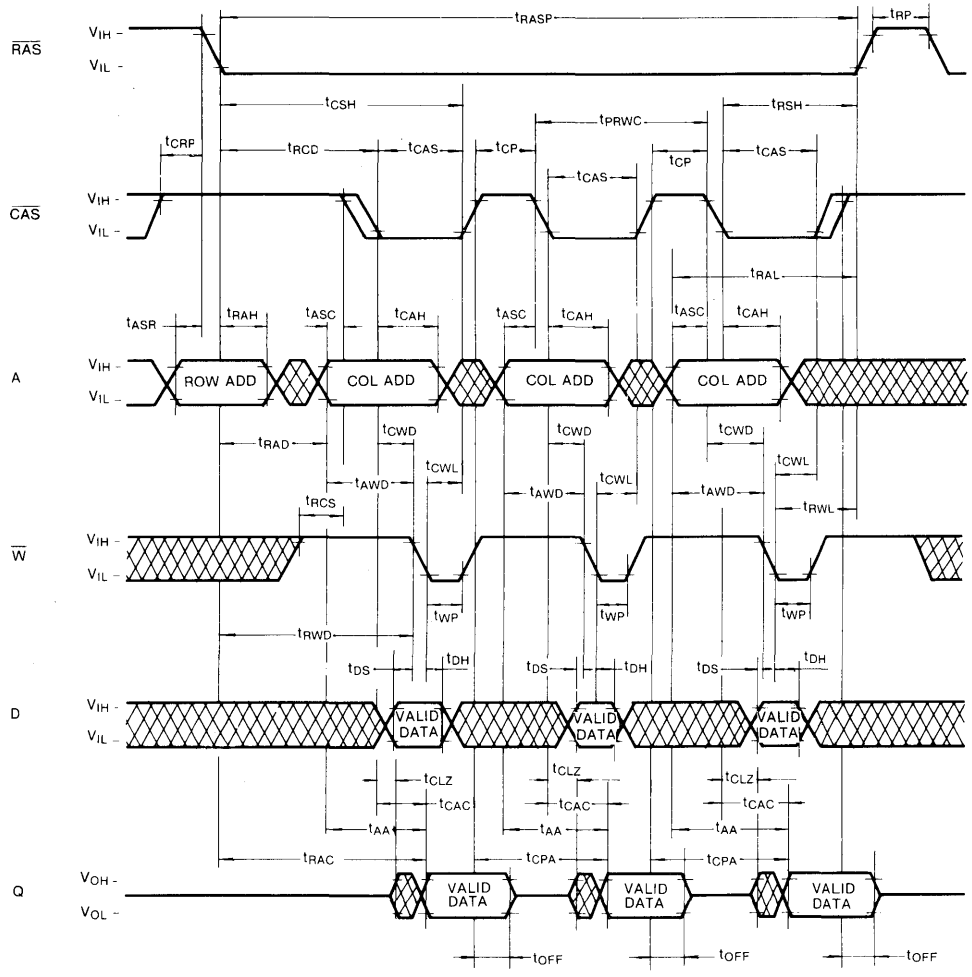
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



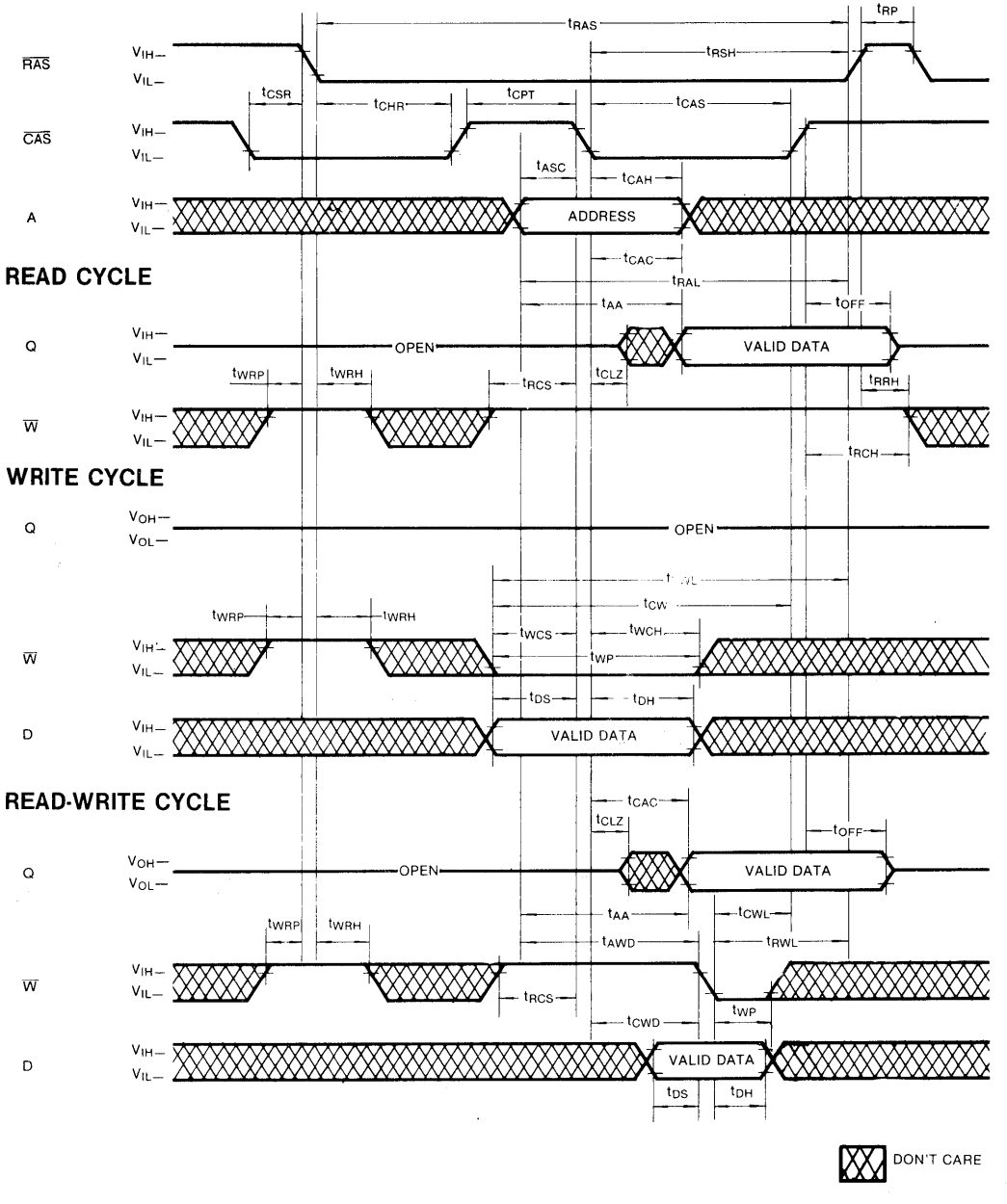
TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-WRITE CYCLE



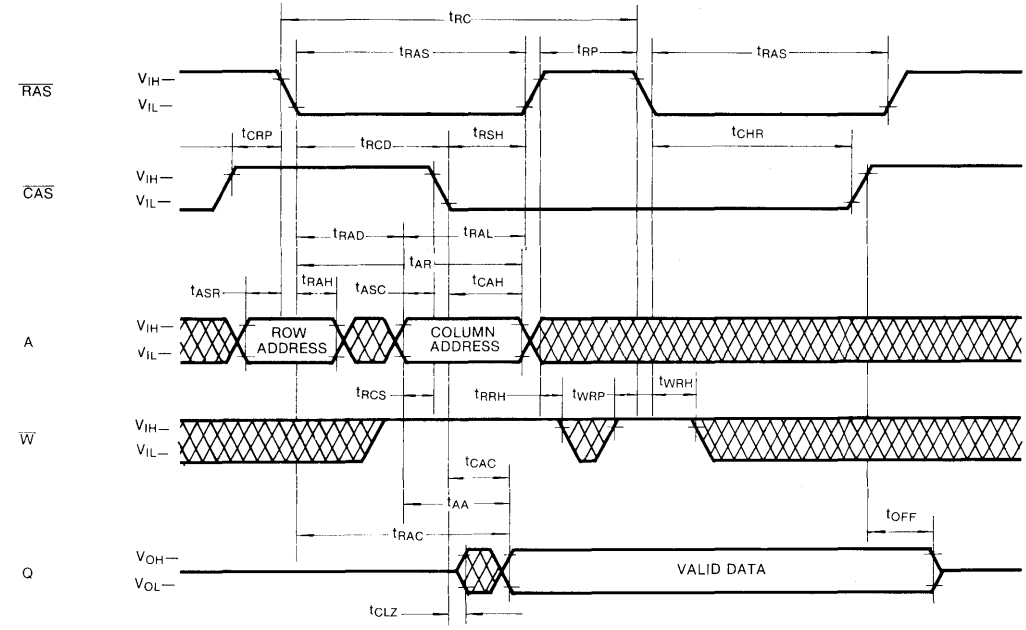
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

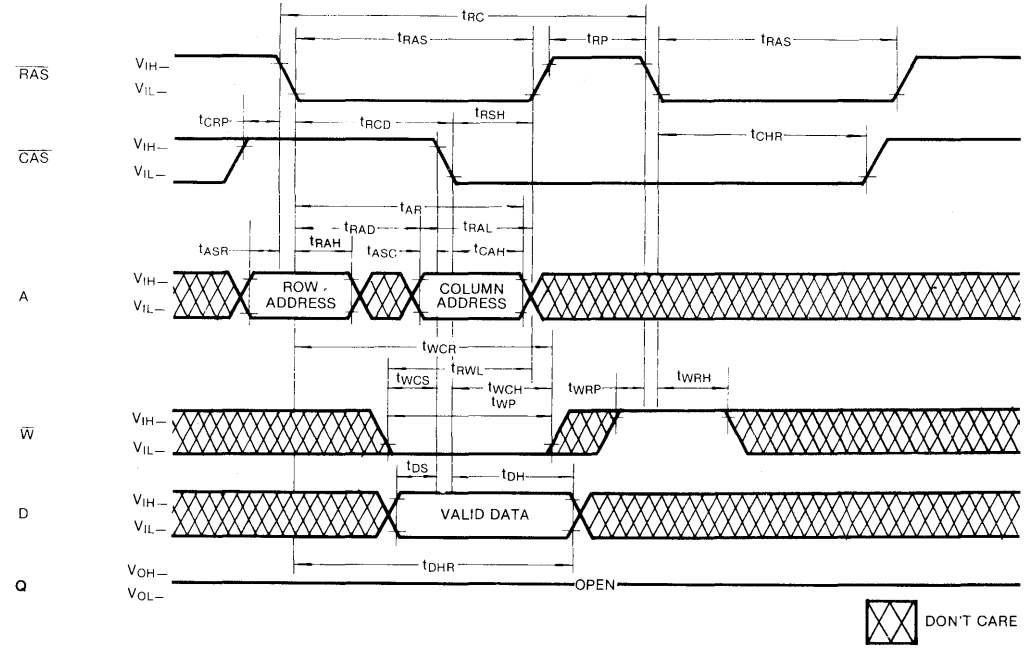


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

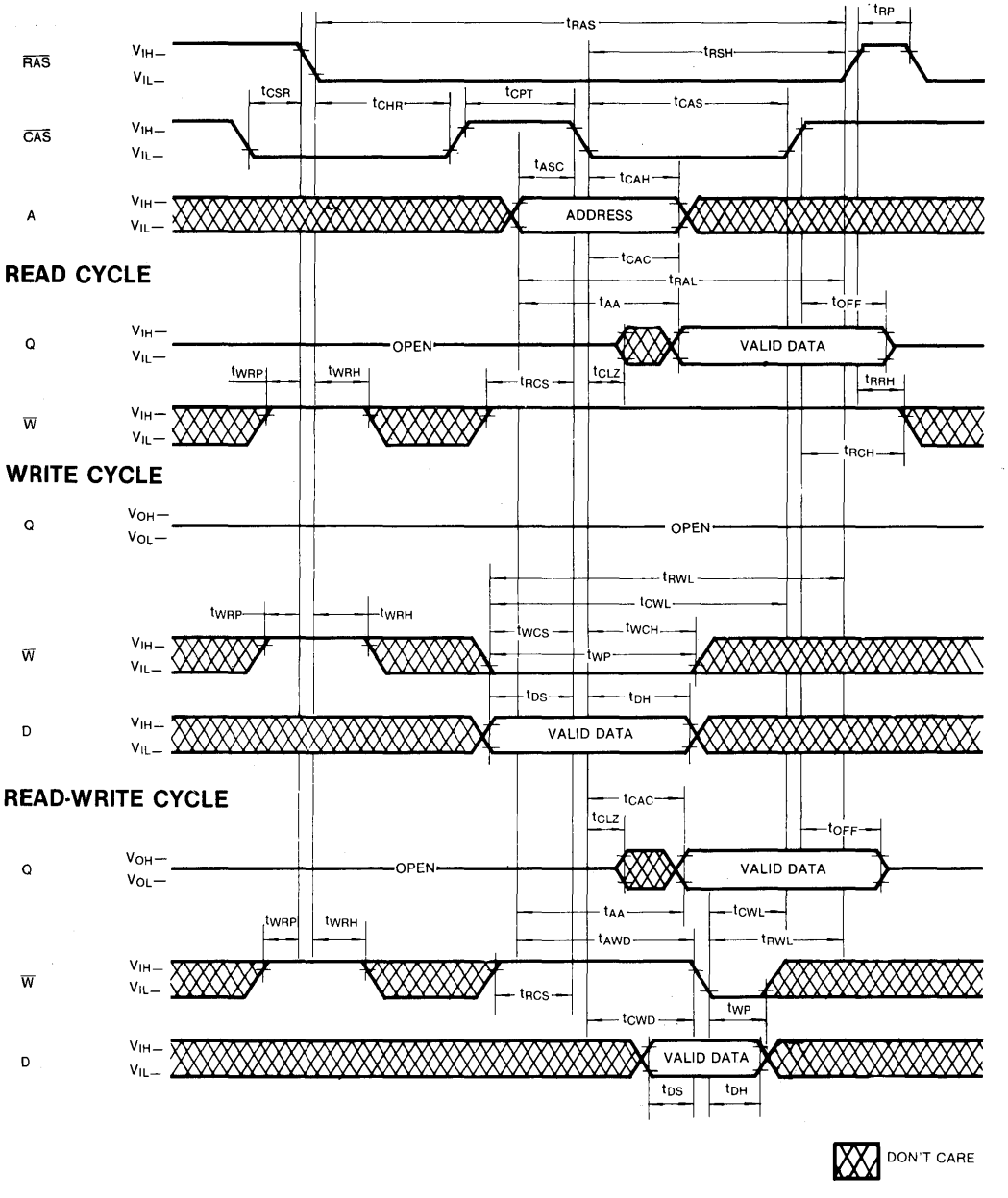


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

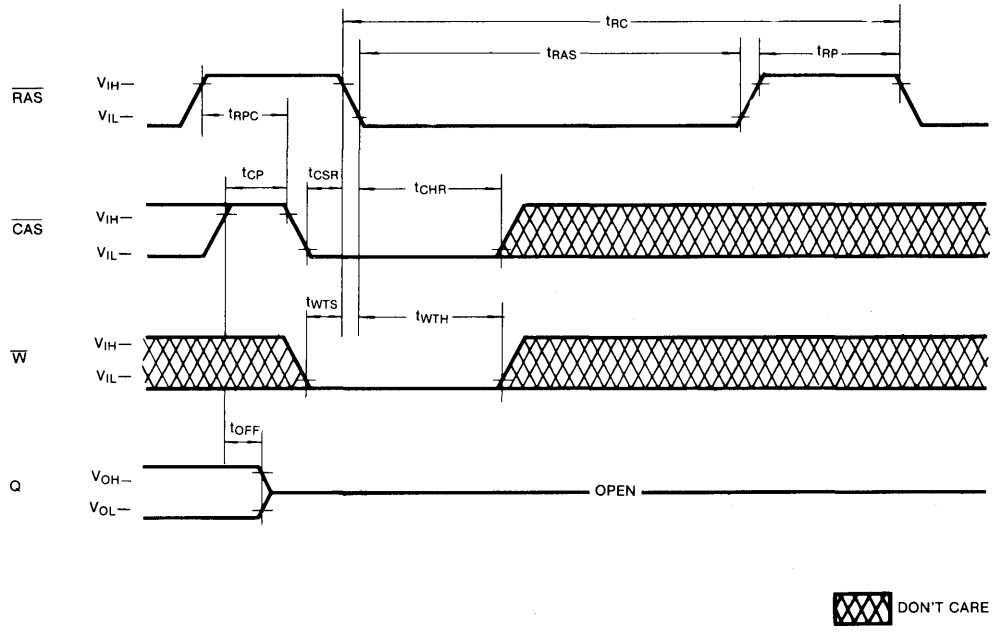
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D. Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4000ASL is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000ASL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000ASL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000ASL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000ASL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000ASL begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000ASL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000ASL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000ASL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000ASL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000ASL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000ASL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000ASL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000ASL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

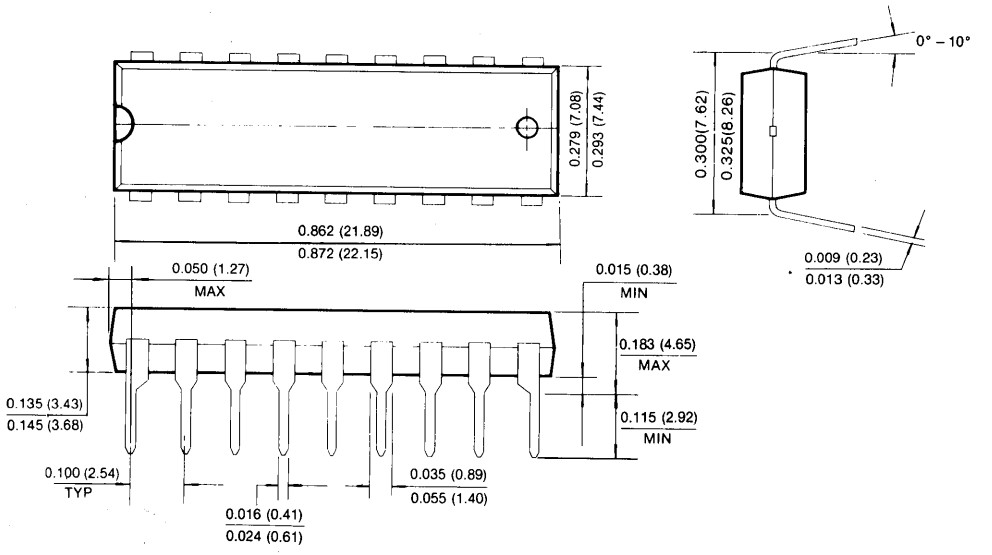
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4000ASL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

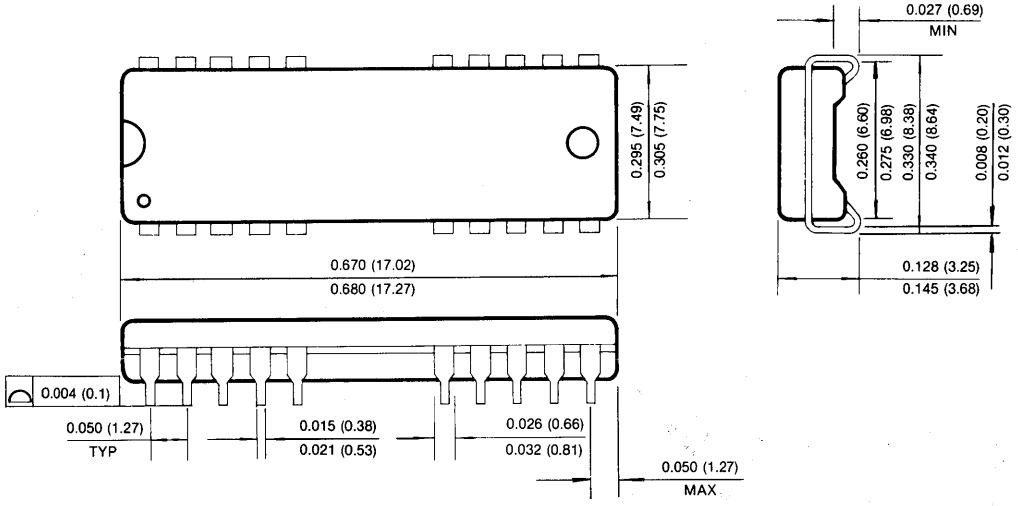
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



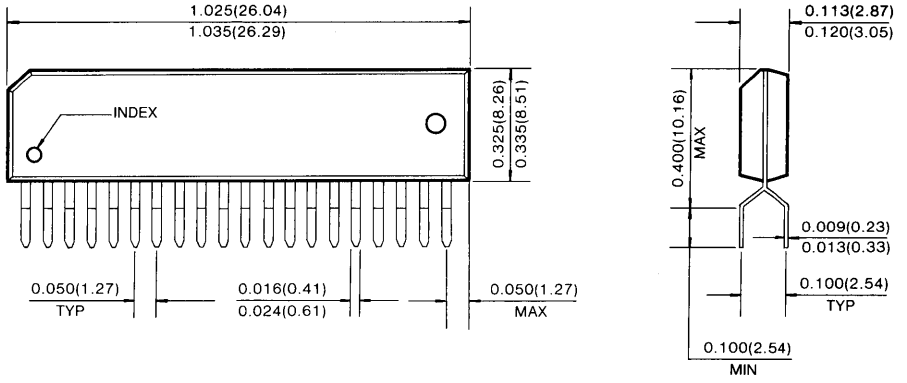
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



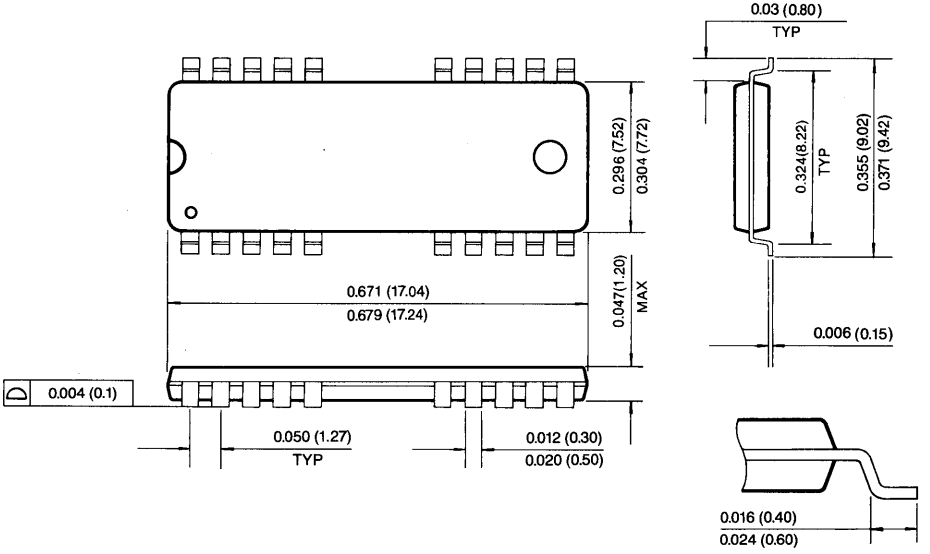
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4MX1 Bit CMOS Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4001A- 7	70ns	20ns	130ns
KM41C4001A- 8	80ns	20ns	150ns
KM41C4001A-10	100ns	25ns	180ns

- **Nibble Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

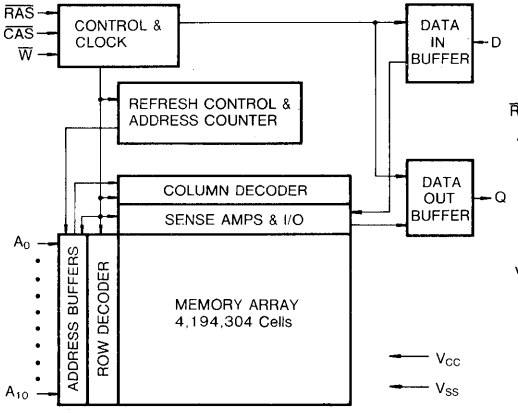
The Samsung KM41C4001A is a CMOS high speed 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4001A features Nibble Mode operation which allows high speed serial access of up to 4 bits of data.

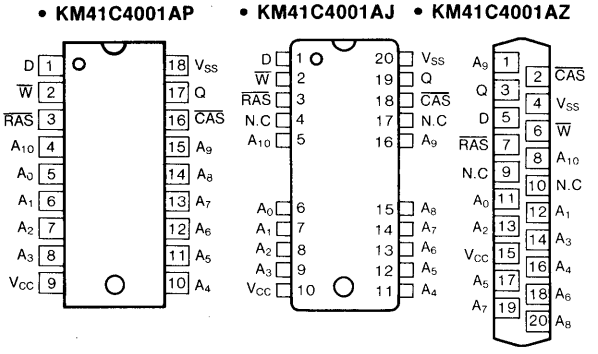
$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C4001A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, Ta=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4001A- 7	I_{CC1}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4001A- 7	I_{CC3}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Nibble Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address Cycling: t_{NC}=min.)	KM41C4001A- 7	I_{CC4}	—	80	mA
	KM41C4001A- 8		—	70	mA
	KM41C4001A-10		—	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W} \geq V_{CC}-0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4001A- 7	I_{CC6}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Standby Current ($\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Nibble mode cycle time	t_{NC}	40		40		45		ns	
Nibble mode read-write cycle time	t_{NRWC}	65		65		70		ns	
Nibble mode access time	t_{NCAC}		20		20		25	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		20		25		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10		10		10		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20		20		25		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{RAS}$ lead time	t_{NRWL}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	20		20		25		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

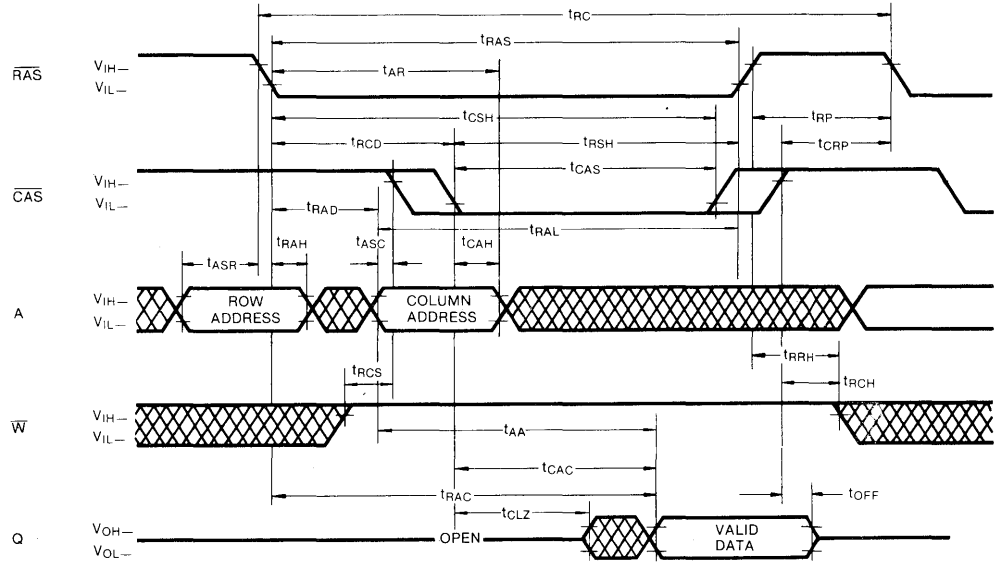
Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7

NOTES

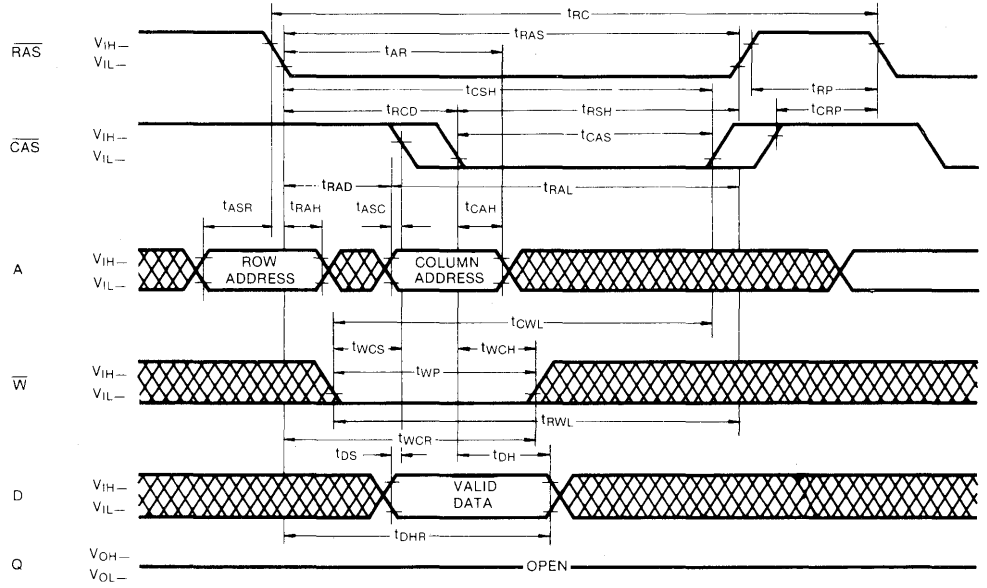
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



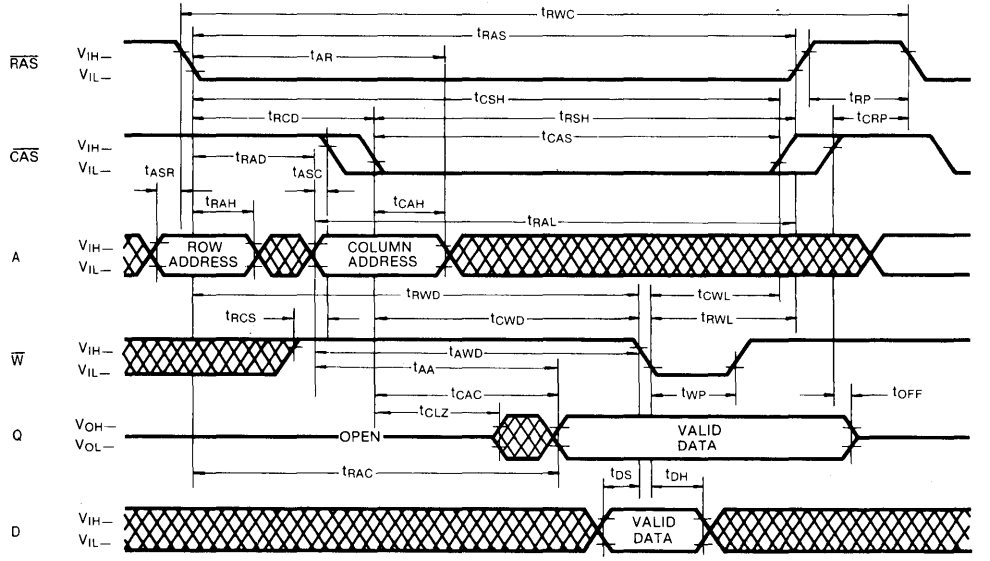
WRITE CYCLE (EARLY WRITE)



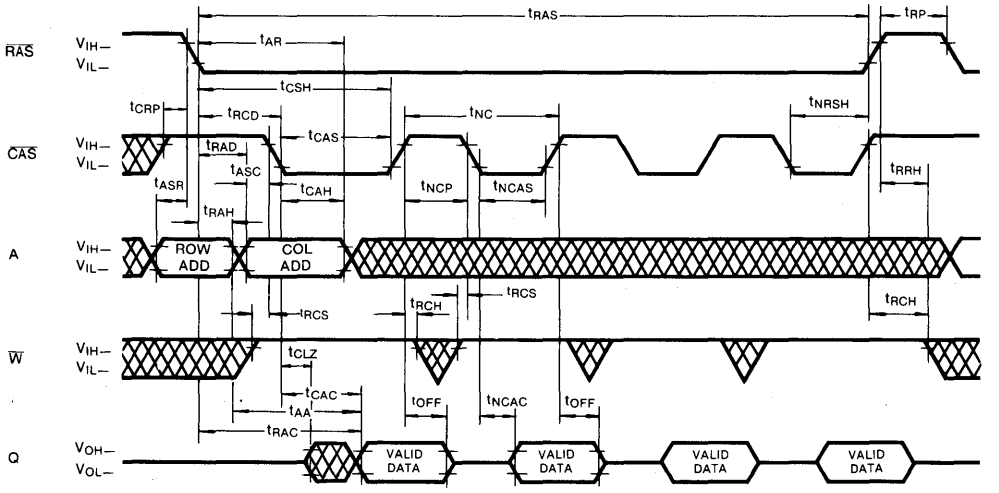
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



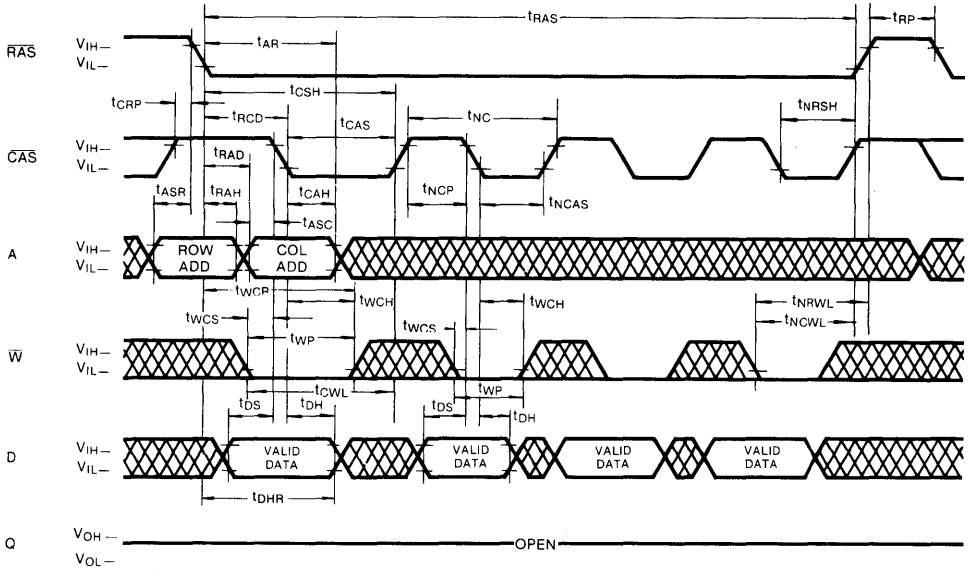
NIBBLE MODE READ CYCLE



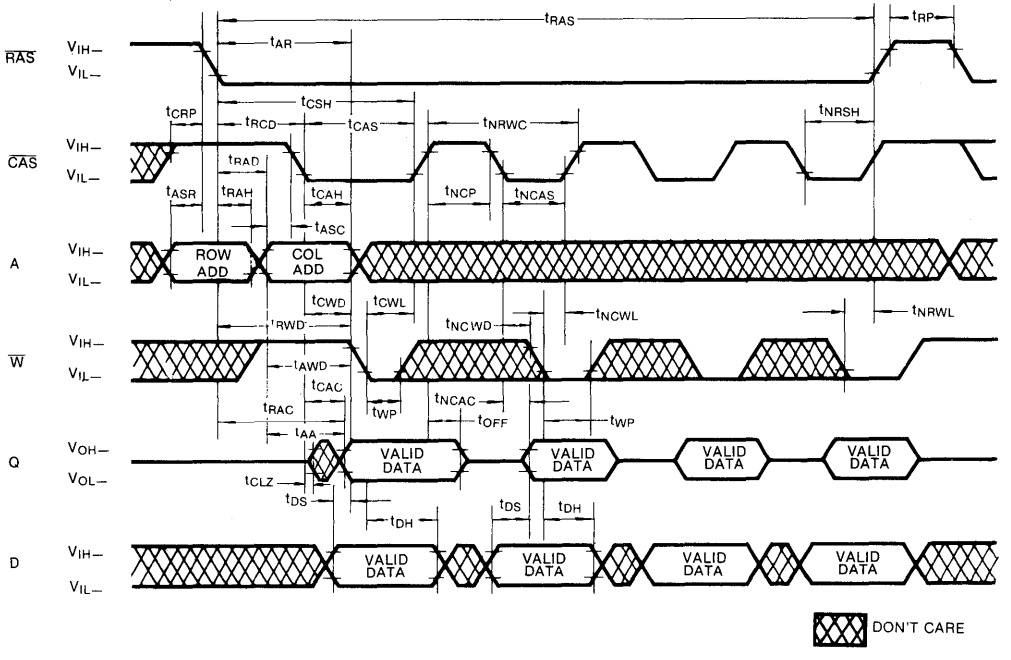
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE WRITE CYCLE (EARLY WRITE)



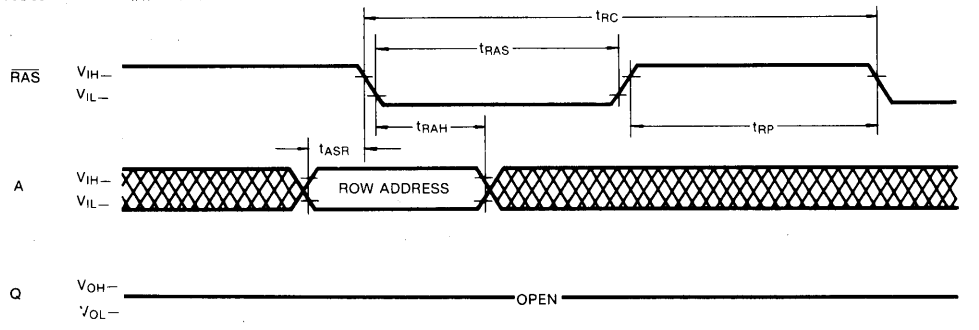
NIBBLE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

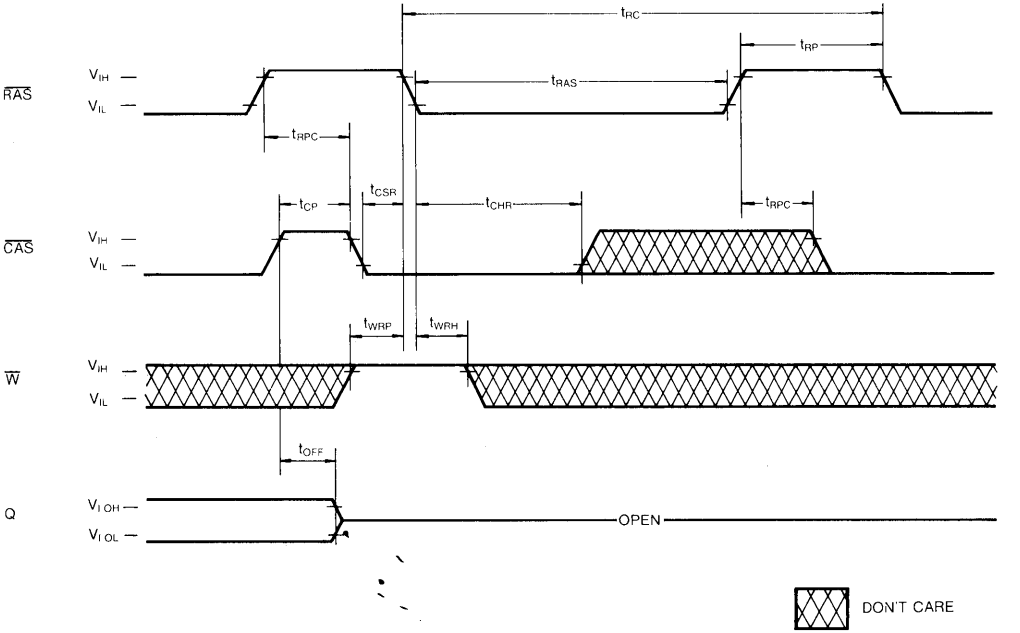
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{CAS}$=V_{IH}, $\overline{W}$,D, A_{10}=Don't Care



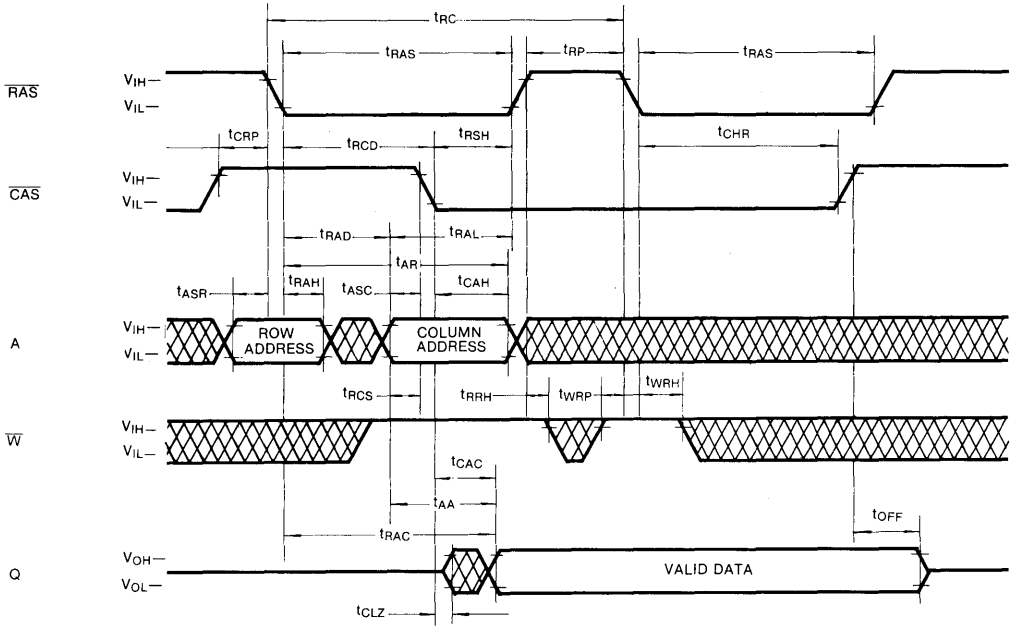
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

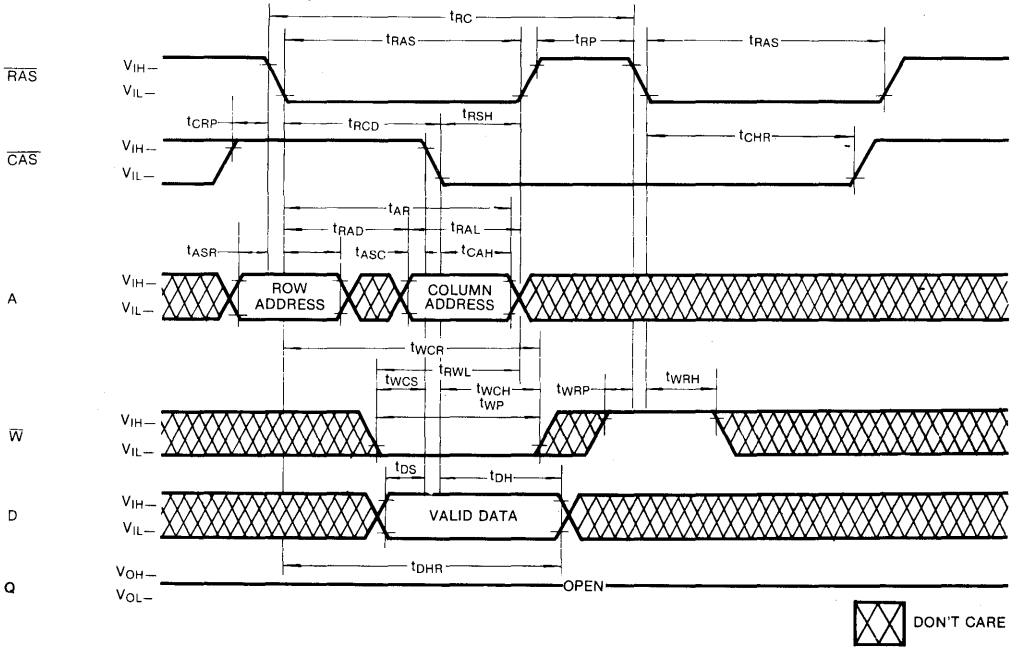


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

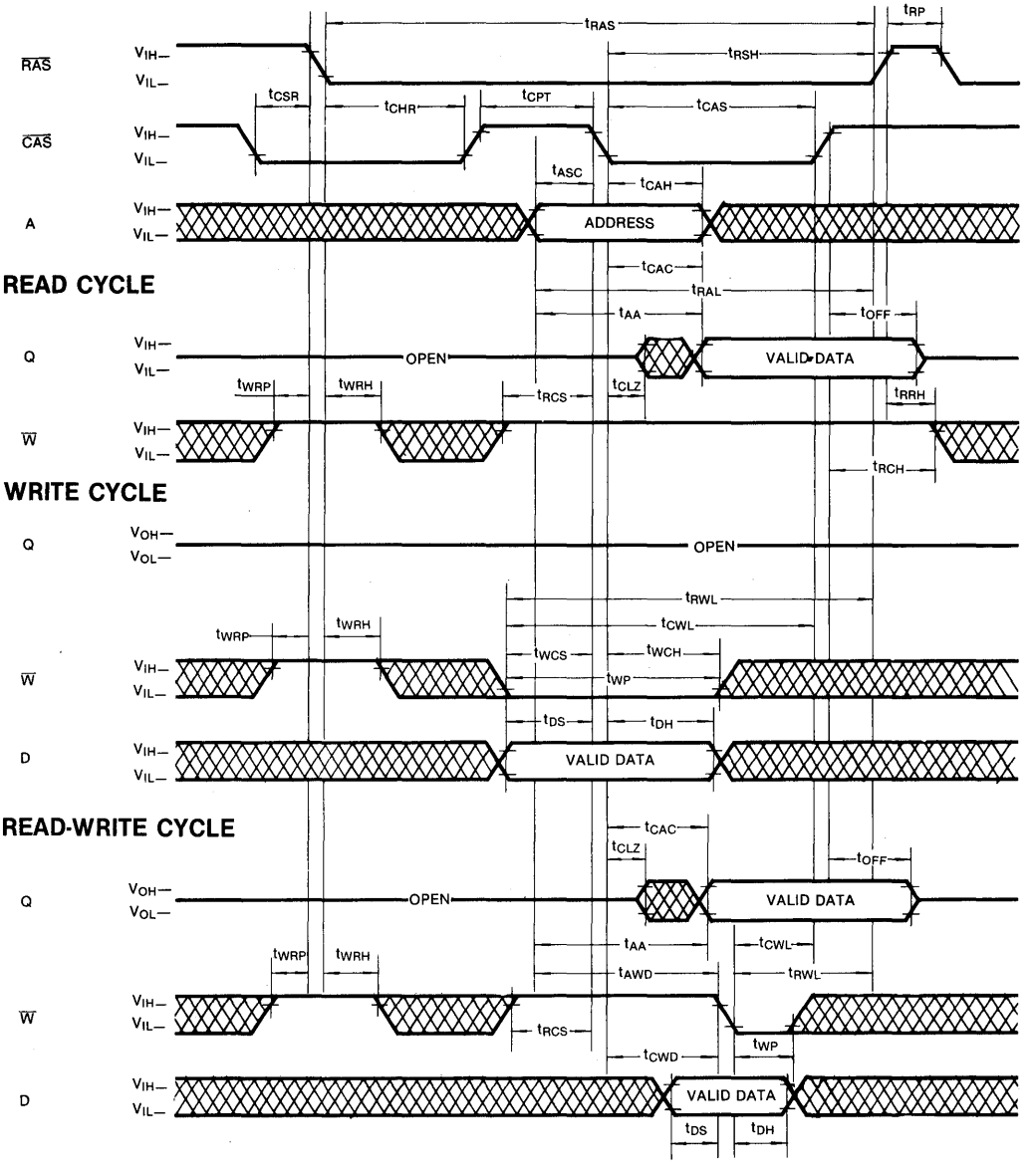


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

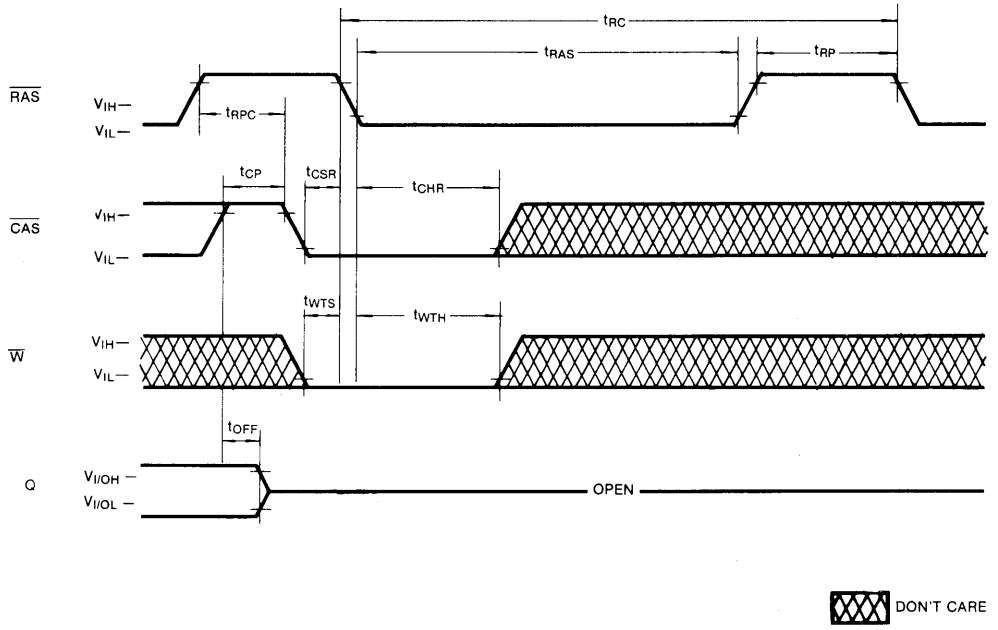
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4001A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C4001A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4001A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4001A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4001A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for porper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP} has been satisfied. Once a cycle begins internal clocks and other circuits within the KM41C4001A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4001A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4001A has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4001A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4001A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

DEVICE OPERATIONS (Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4001A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

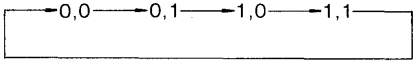
Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4001A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4001A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Nibble Mode

The KM41C4001A has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 10 row address bits (R_{A0}-R_{A9}) and 10 column address bits (C_{A0}-C_{A9}). The two address bits, C_{A10} and R_{A10} are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A10}, R_{A10}) as shown in the following diagram with R_{A10} being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble mode cycle can be a read, write or read-modify-write cycle. Any combinations of reads and writes or read-modify-write be allowed.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

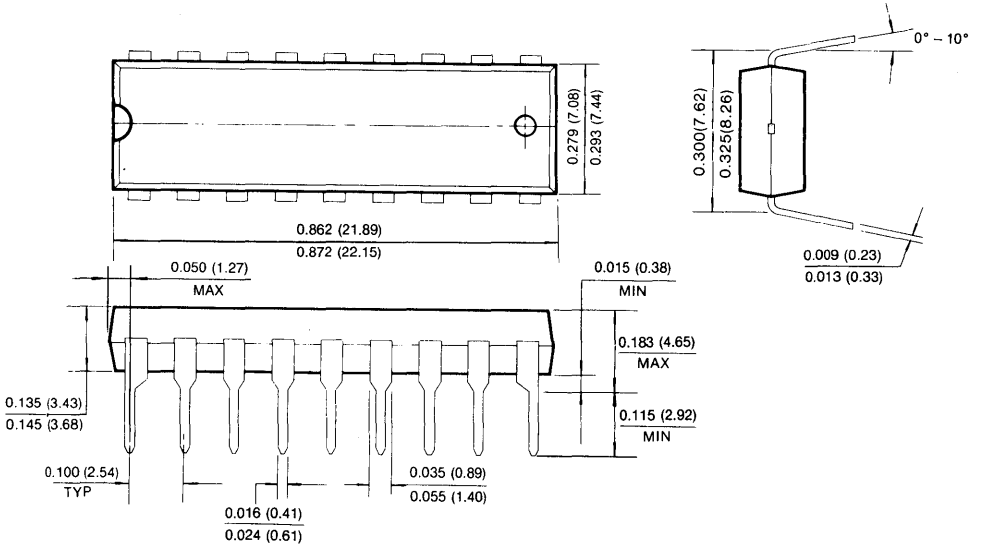
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4001A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

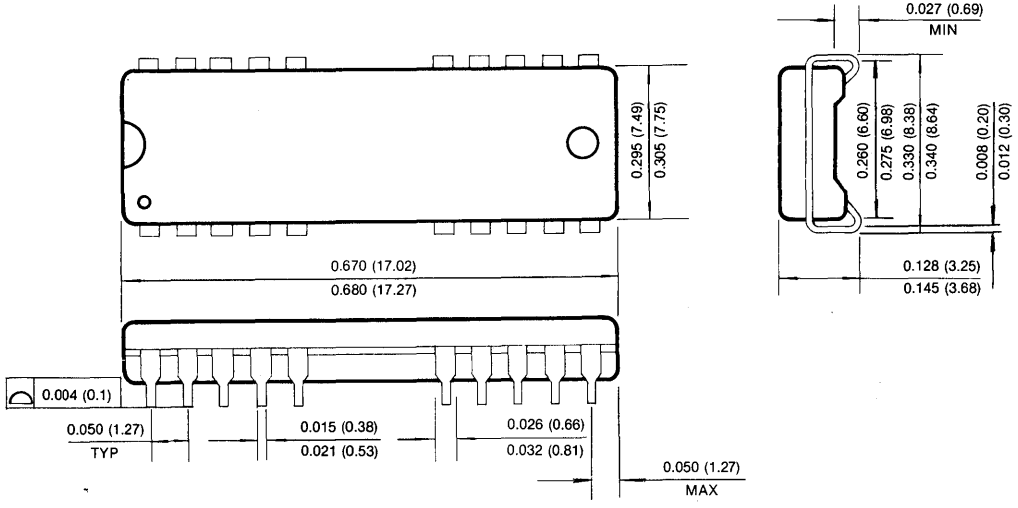
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



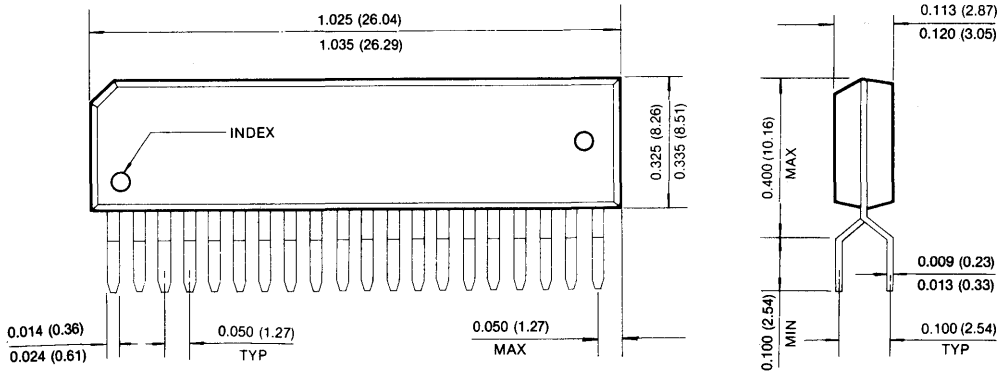
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



4MX1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4002A- 7	70ns	20ns	130ns
KM41C4002A- 8	80ns	20ns	150ns
KM41C4002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

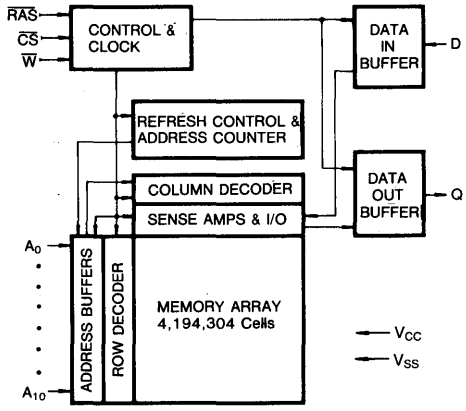
The Samsung KM41C4002A is a high speed CMOS 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4002A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

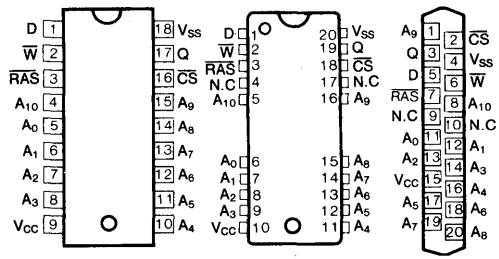
The KM41C4002A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM41C4002AP** - **KM41C4002AJ** - **KM41C4002AZ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM41C4002A- 7	I_{CC1}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM41C4002A- 7	I_{CC3}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM41C4002A- 7	I_{CC4}	—	80	mA
	KM41C4002A- 8		—	70	mA
	KM41C4002A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM41C4002A- 7	I_{CC6}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to write enable delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	70		80		100		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 13)

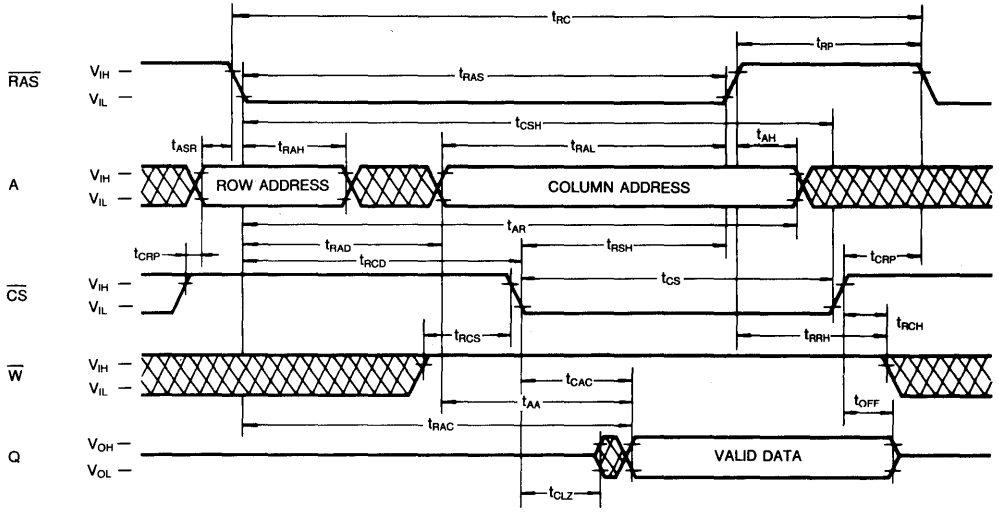
Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	25		25		30		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	75		85		105		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	

NOTES

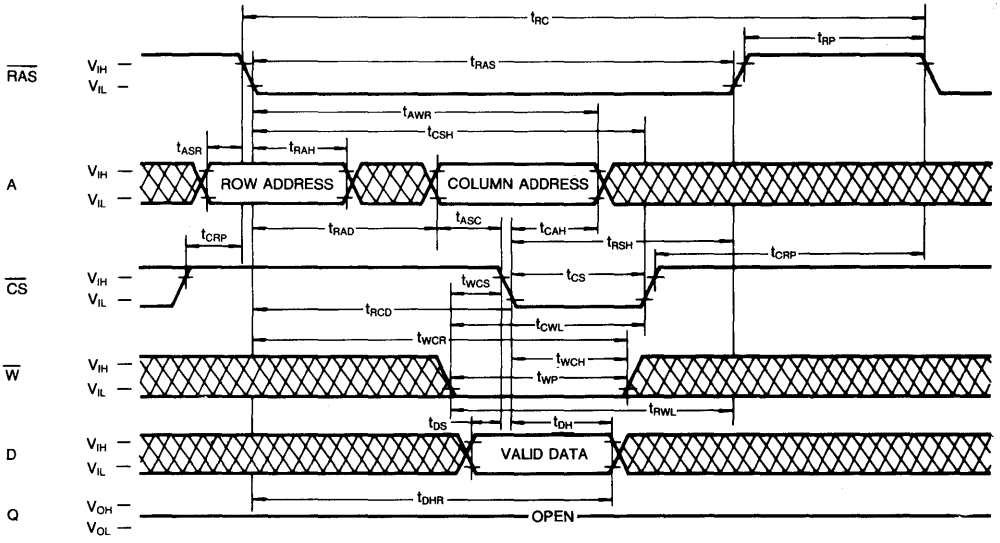
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycle before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE



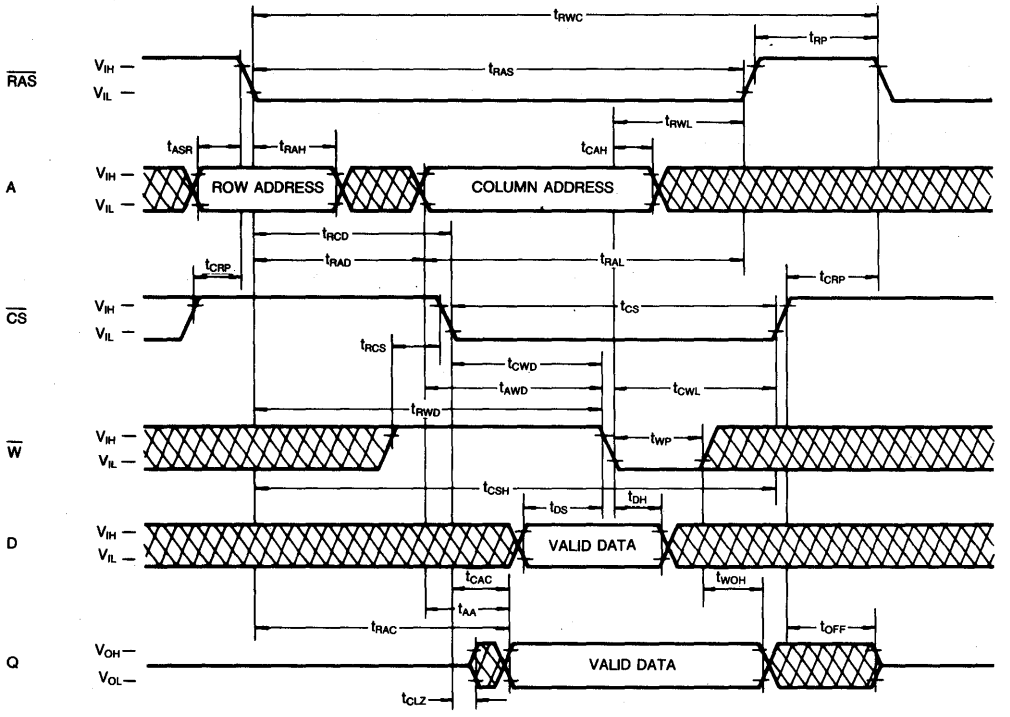
WRITE CYCLE (EARLY WRITE)



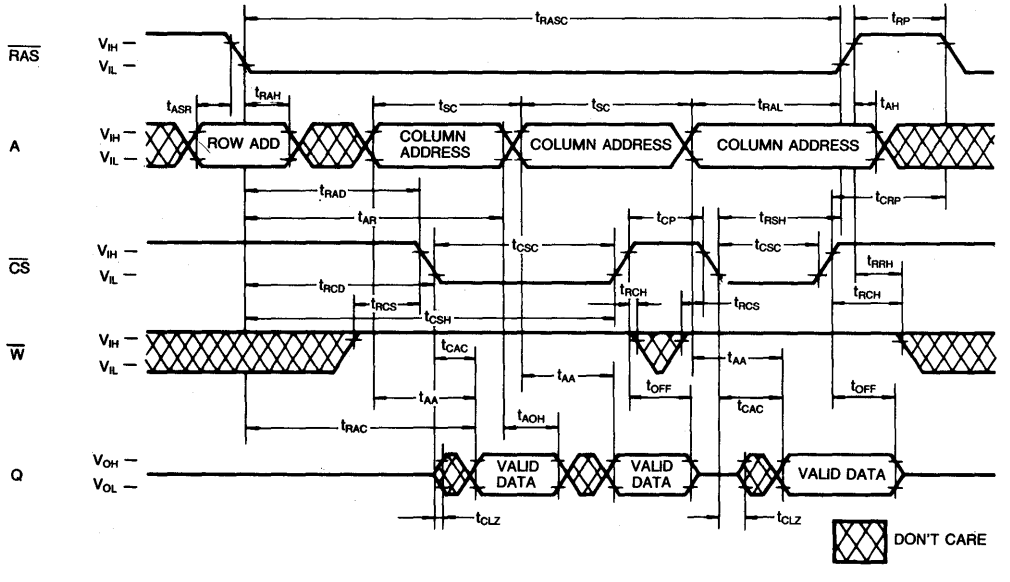
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

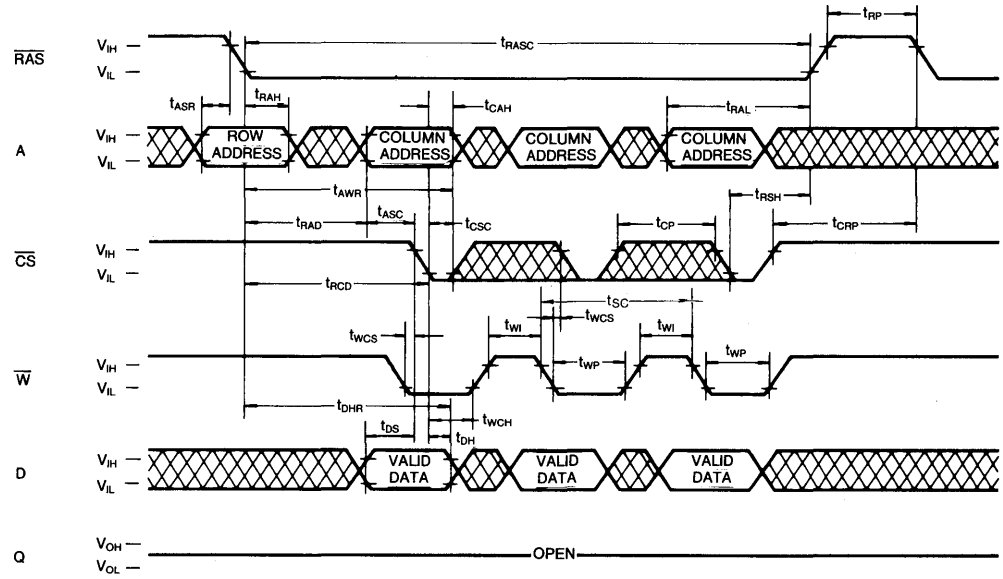


STATIC COLUMN MODE READ CYCLE

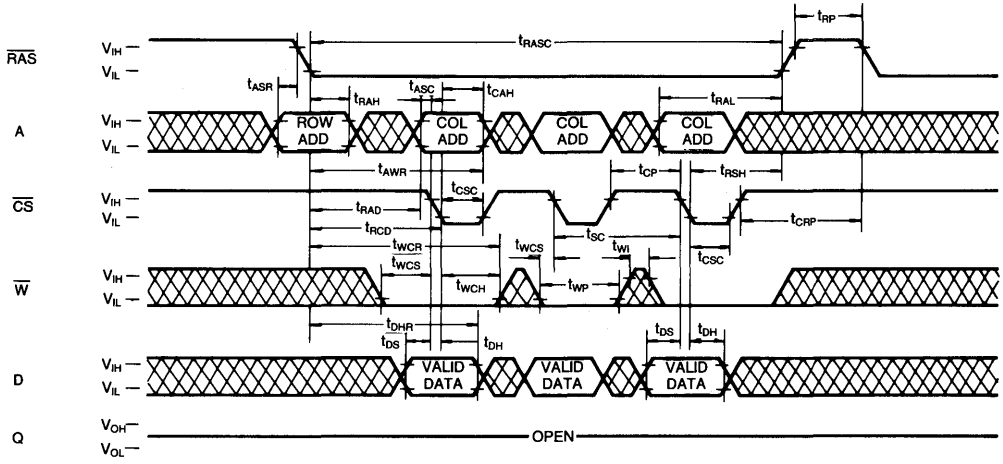


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)



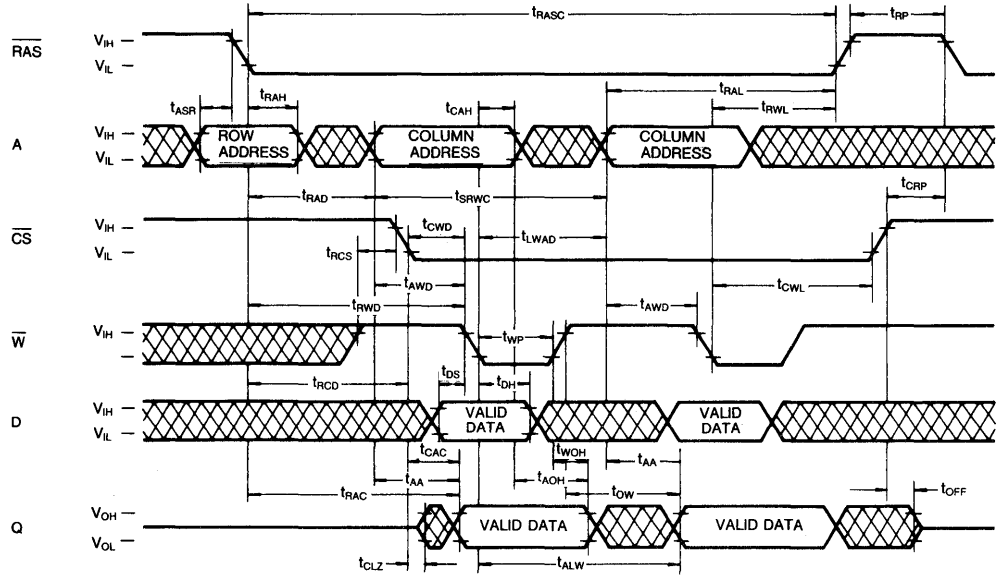
STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)



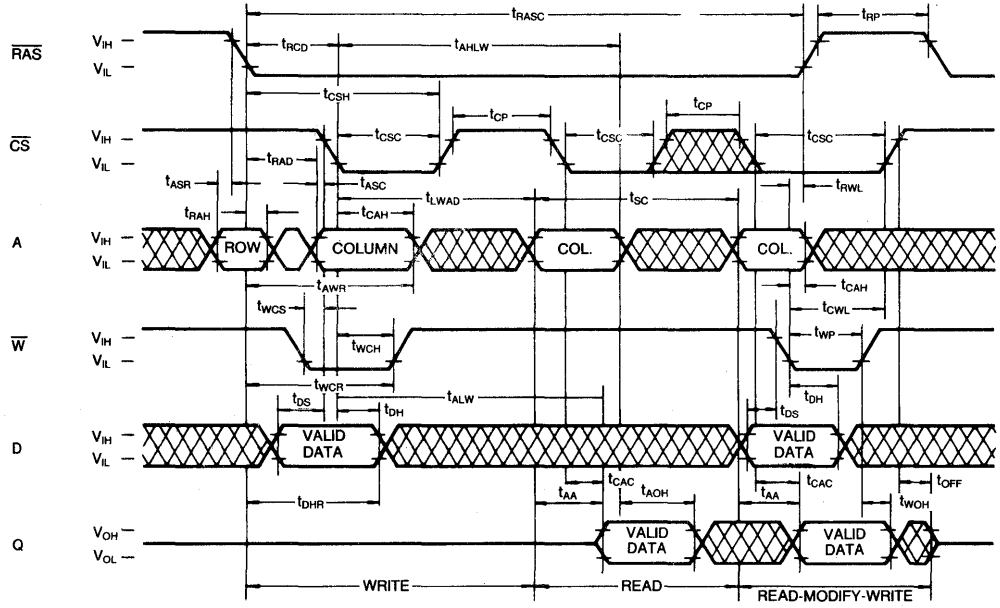
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

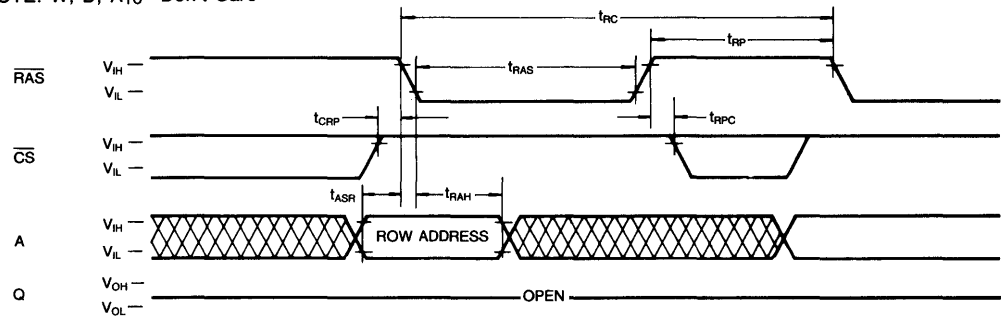


DONT'T CARE

TIMING DIAGRAMS (Continued)

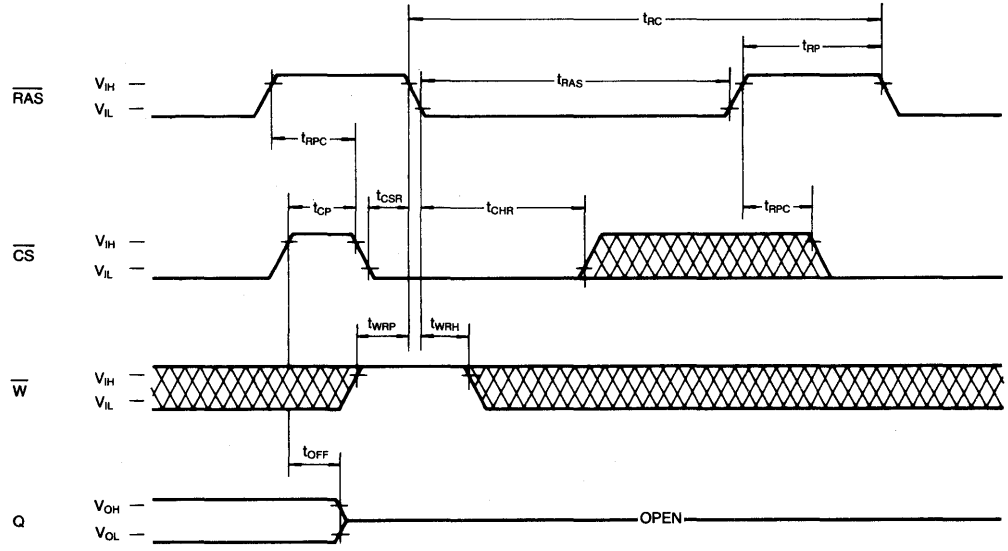
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D, A_{10}=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

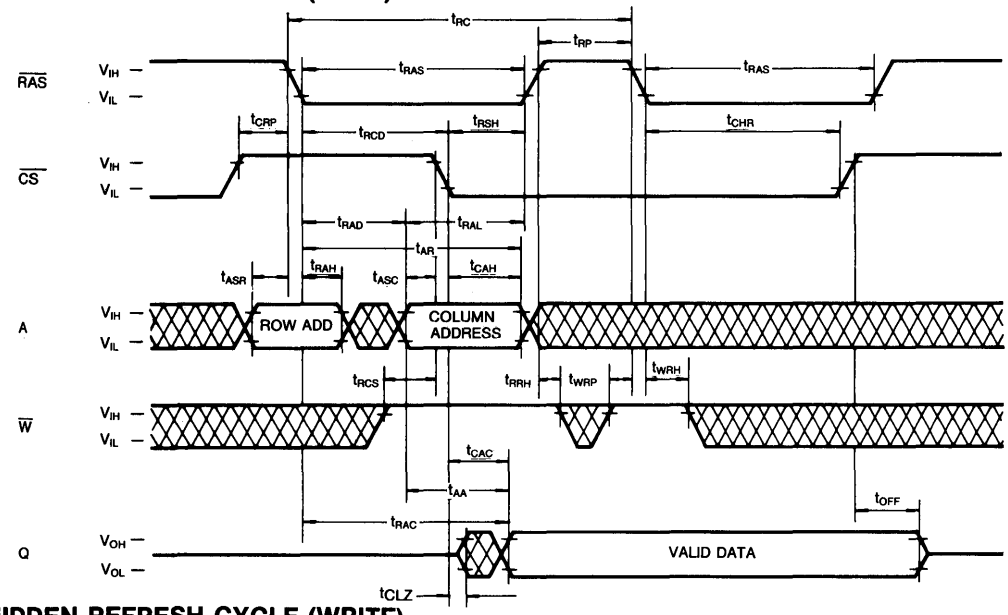
NOTE: Address=Don't Care



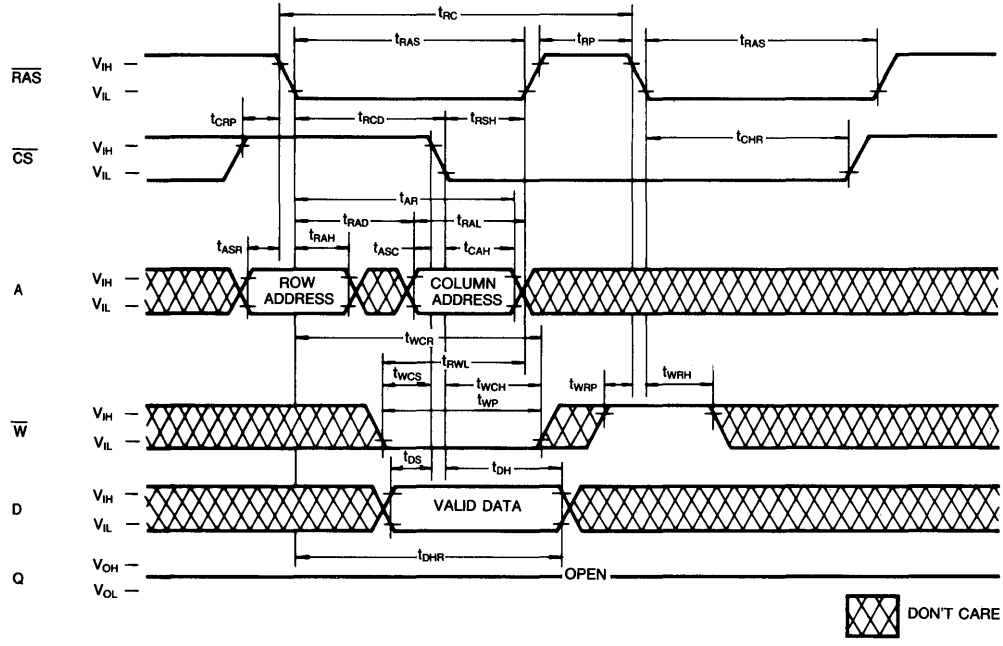
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

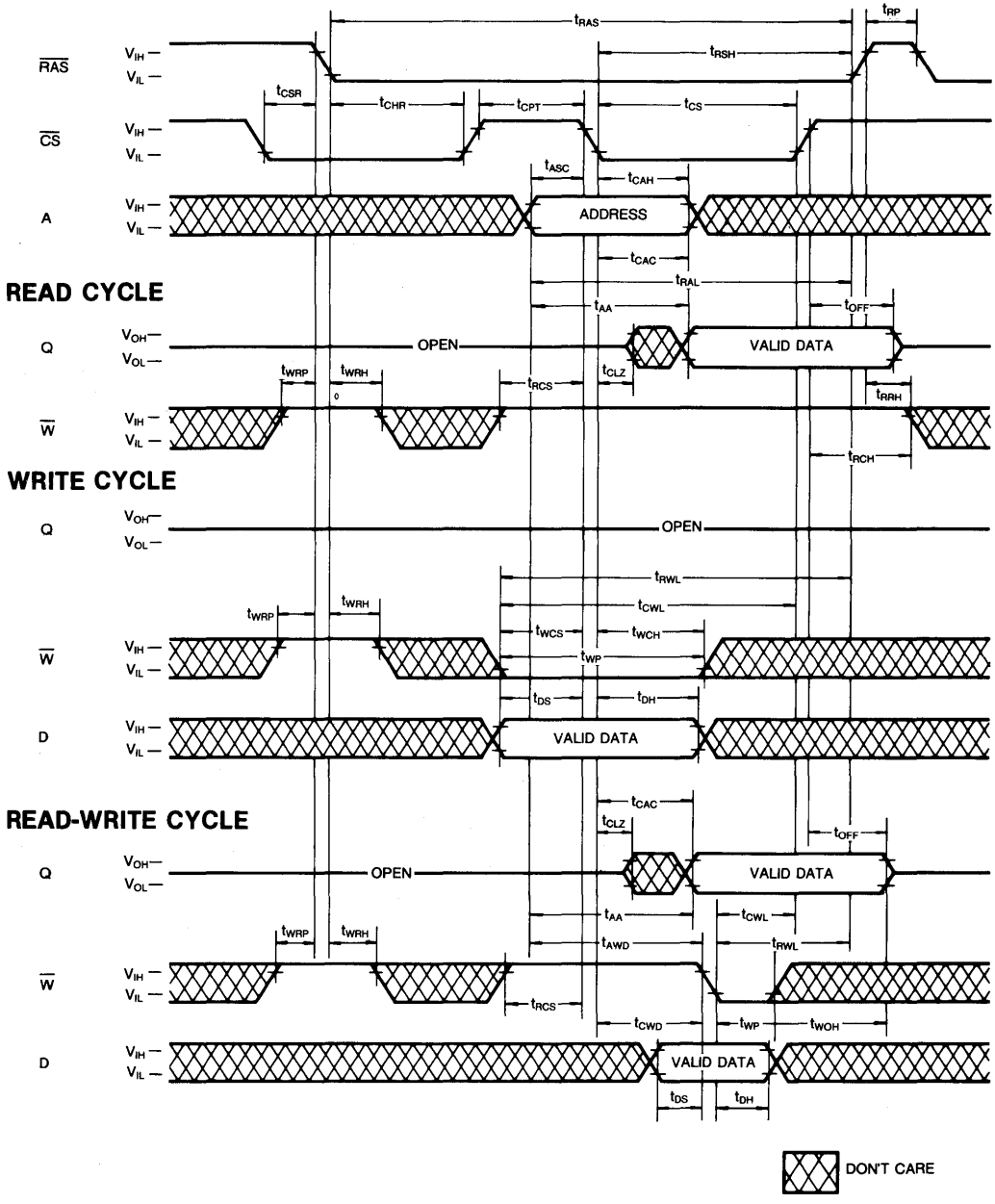


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

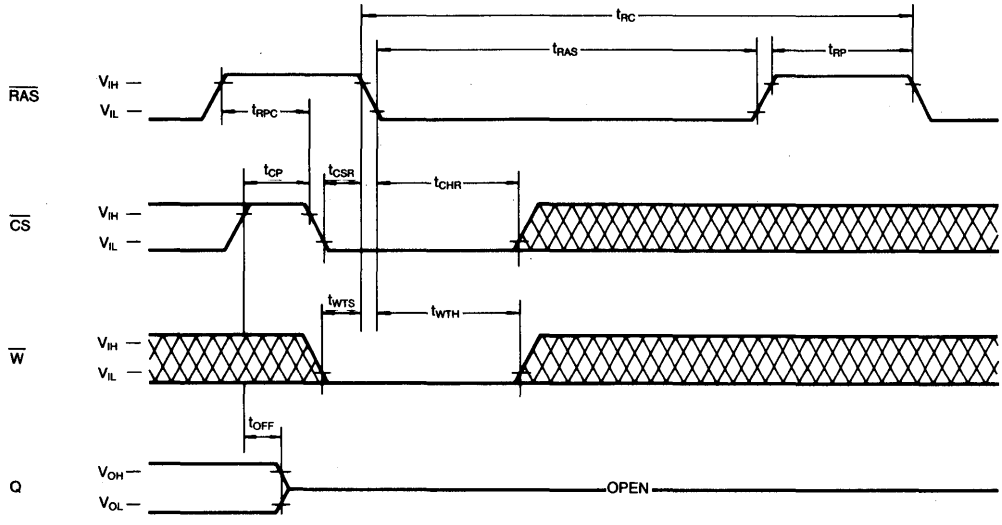
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{OC} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM41C4002A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM41C4002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C4002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C4002A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002A has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4002A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output Static: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-Before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.
Indeterminate Output State: Delayed Write.

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM41C4002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C4002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cy~ling $\overline{RAS}$. The KM41C4002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. The A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

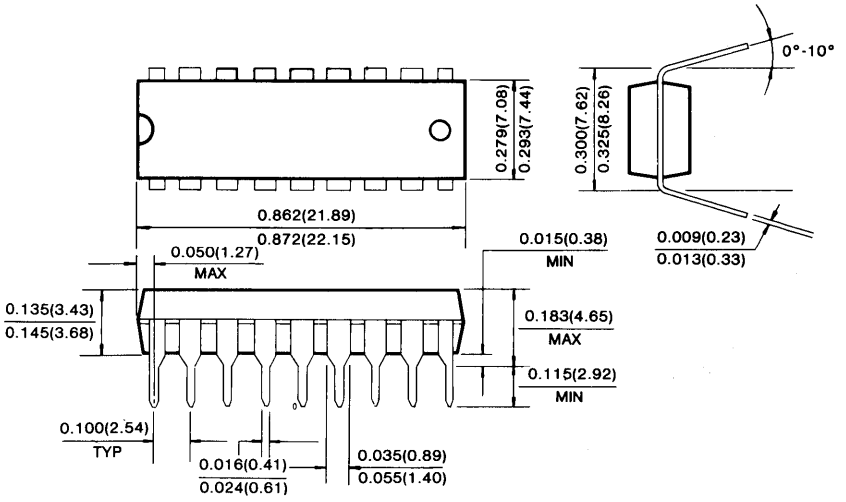
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

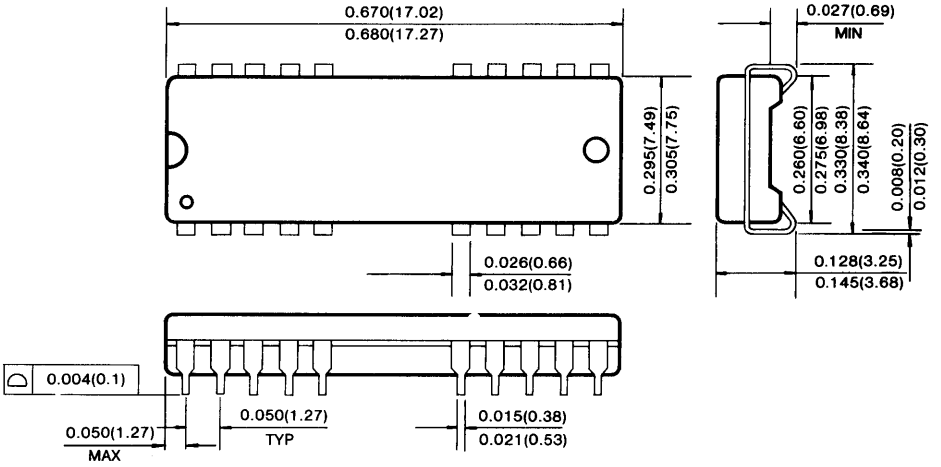
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



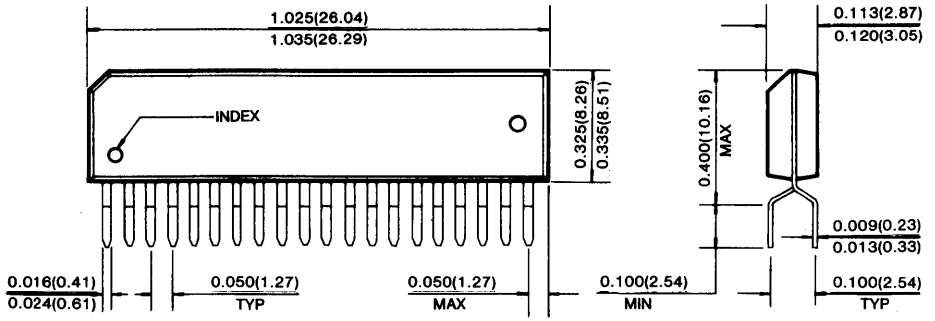
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1MX4 Bit CMOS Dynamic RAM with Fast Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000/L- 8	80ns	20ns	150ns
KM44C1000/L-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled wirte**
- **Single +5V±10% power supply**
- **Refresh cycles:**
  - **—1024 cycles/16ms**
  - **—1024 cycles/128ms (L-Version)**
- **Low Power:**
  - **—Standby: 5.5mW**
    1.7mW (L-Version)
  - **—Active: 550mW (80ns)**
    468mW (100ns)
- **JEDEC standard pinout**
- **Available in Plastic SOJ/ZIP**

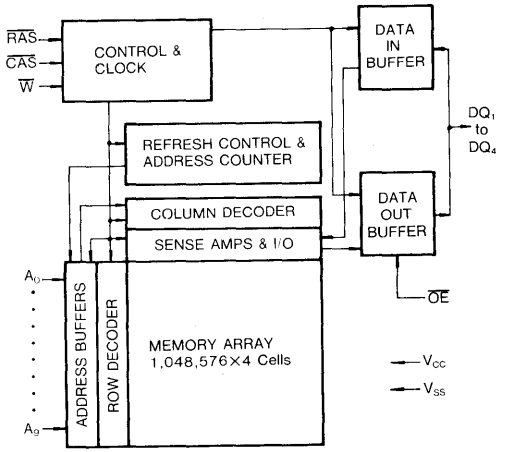
GENERAL DESCRIPTION

The Samsung KM44C1000/L is a high speed CMOS 1,048,576 bit X 4 dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000/L features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

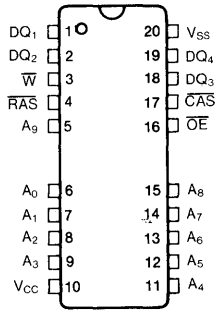
The KM44C1000/L is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

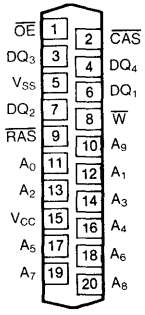


PIN CONFIGURATION (Top Views)

- **KM44C1000J/LJ**



- **KM44C1000Z/LZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ1-4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000/L- 8 KM44C1000/L-10	I_{CC1}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM44C1000/L- 8 KM44C1000/L-10	I_{CC3}	— —	100 85	mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000/L- 8 KM44C1000/L-10	I_{CC4}	— —	70 60	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)	KM44C1000-8/10 KM44C1000L-8/10	I_{CC5}	—	1 300	mA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000/L- 8 KM44C1000/L-10	I_{CC6}	— —	100 85	mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ1∼4=Don't Care T_{RC}=125μs, T_{RAS}=t_{RAS} min.∼1μs	KM44C1000L- 8 KM44C1000L-10	I_{CC7}	—	400	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} Dout Enable)		I_{CC8}	—	5	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. In I_{CC1}, I_{CC3}, I_{CC6}. Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%. See notes 1.2)

Standard Operation	Symbol	KM44C1000/L-8		KM44C1000/L-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		ns	
Read-modify-write cycle time	t_{RWC}	205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	3,4
Access time from column address	t_{AA}		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000/L-8		KM44C1000/L-10		Unit	Notes
		Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	9
Write command hold time	t_{WCH}	15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	6
Write command pulse width	t_{WP}	15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		ns	
Data-in set-up time	t_{DS}	0		0		ns	10
Data-in hold time	t_{DH}	15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16	ms	
Refresh period (for L-Version, 1024 cycles)	t_{REF}		128		128	ms	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		85		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		60	ns	3
Fast Page mode cycle time	t_{PC}	55		65		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50		60		ns	
Fast page mode read-modify-write	t_{PRWC}	105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100,000	100	100,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{WRH}	10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		ns	

TEST MODE CYCLE

(Note. 12)

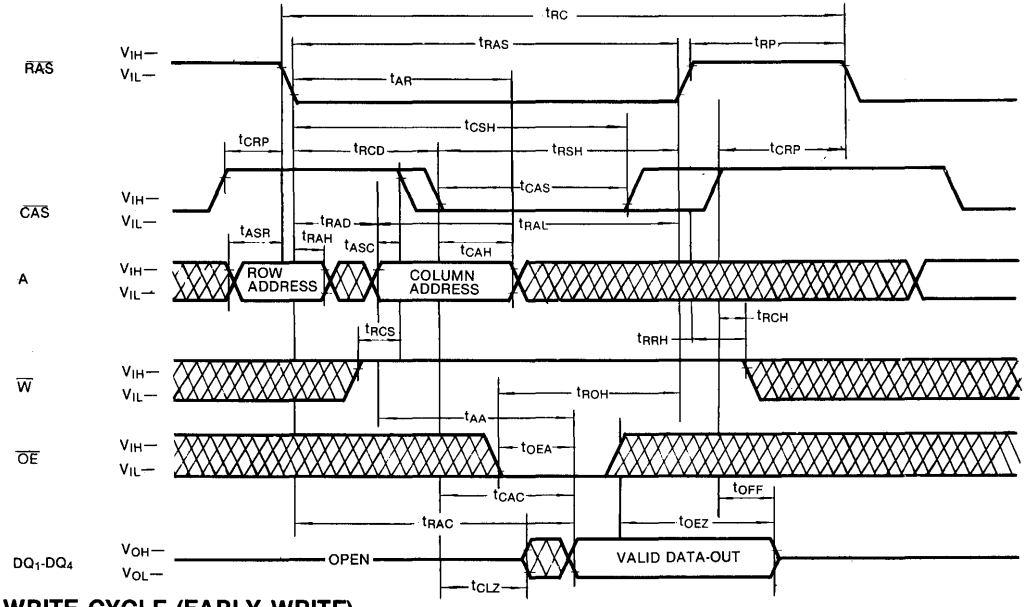
Standard Operation	Symbol	KM44C1000/L-8		KM44C1000/L-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	155		185		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		85		105	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	3,4,5
Access time from column address	t_{AA}		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	75		90		ns	8
Fast Page mode cycle time	t_{PC}	60		65		ns	
Fast page mode read-modify-write	t_{PRWC}	110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	85	100,000	105	100,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		55		65	ns	3
$\overline{OE}$ access time	t_{OEA}		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		30		ns	

NOTES

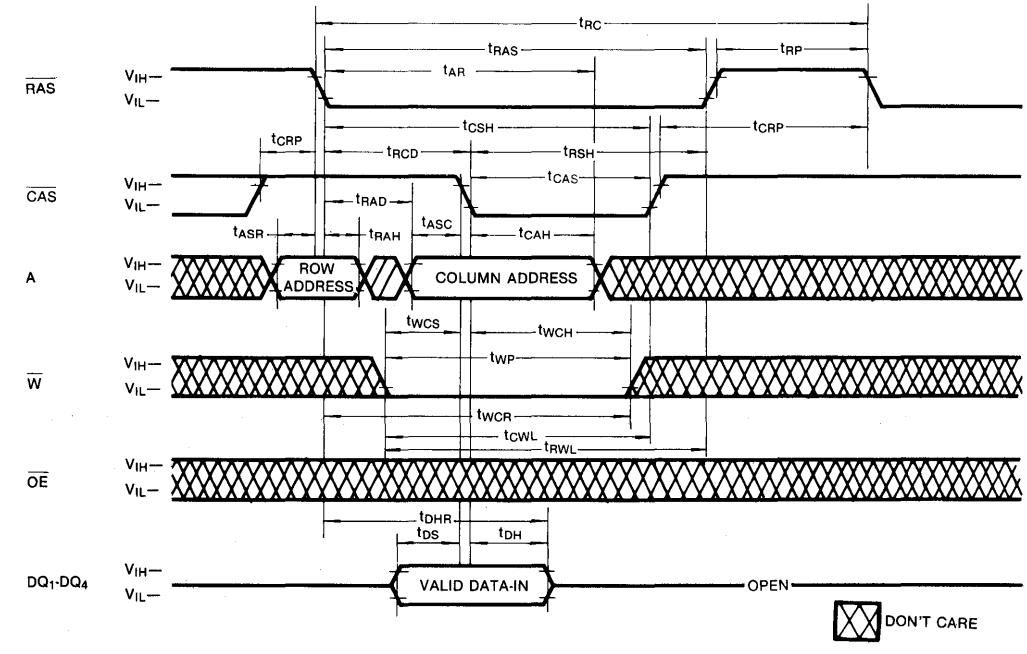
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

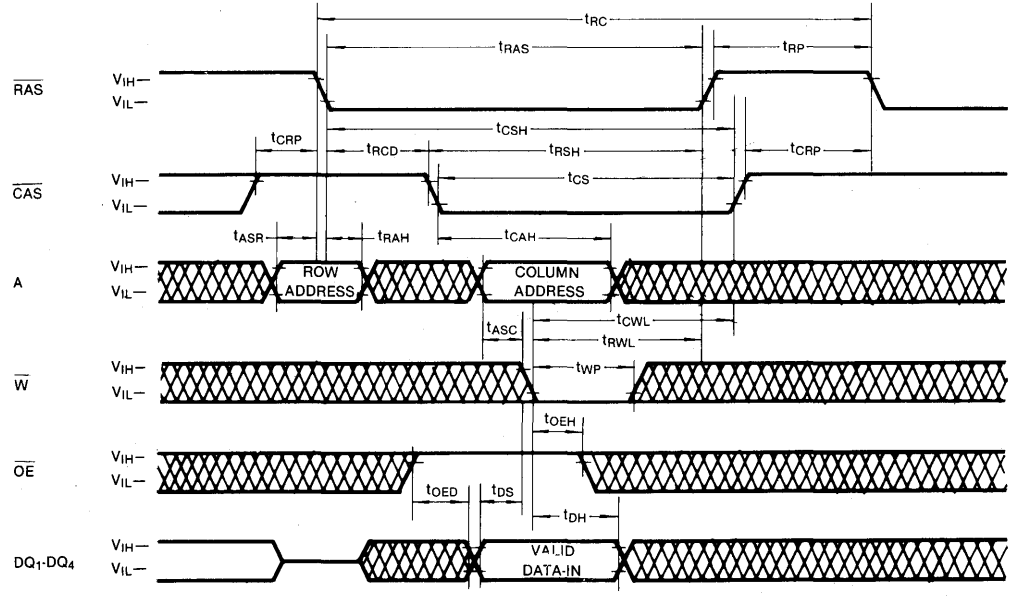


WRITE CYCLE (EARLY WRITE)

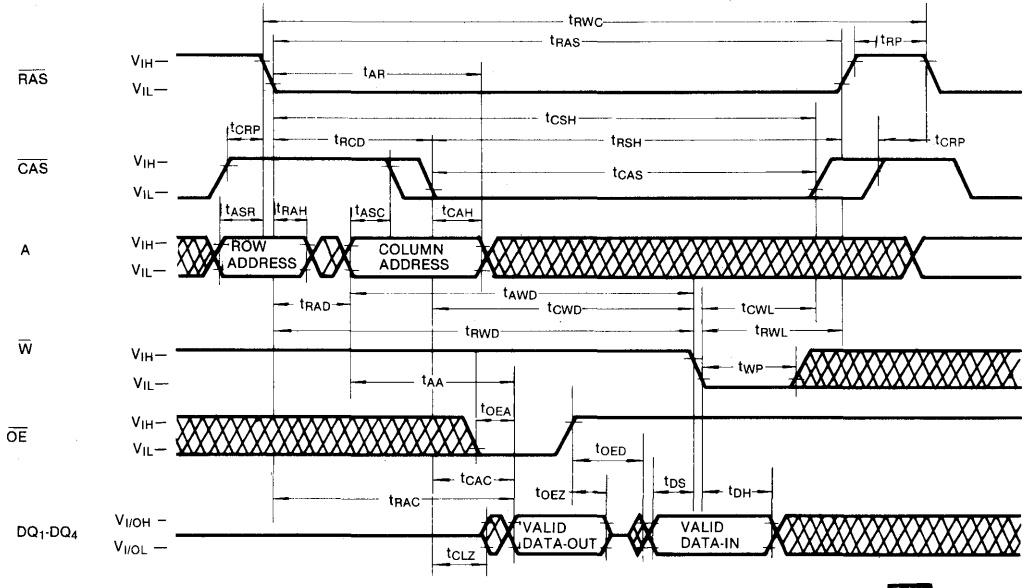


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

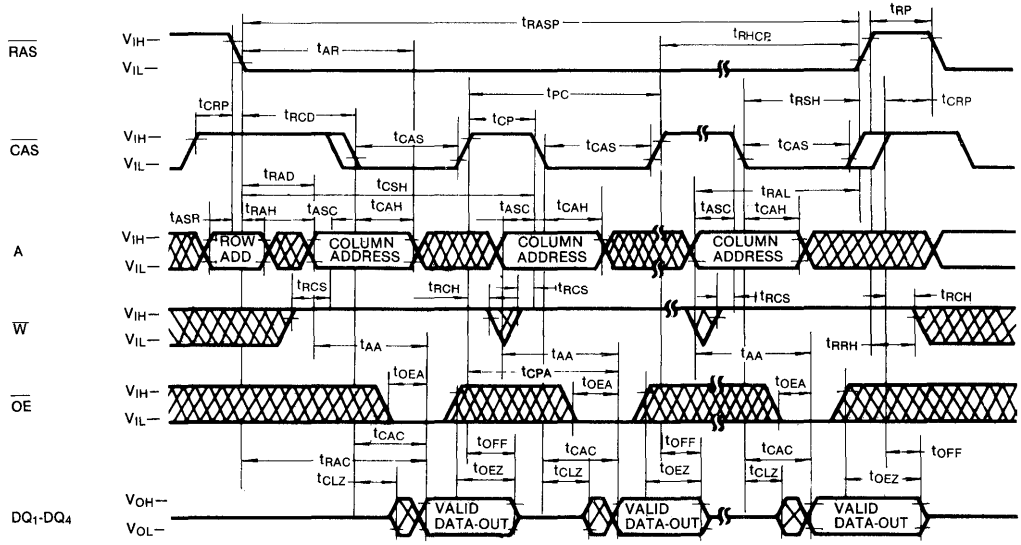


READ-MODIFY-WRITE CYCLE

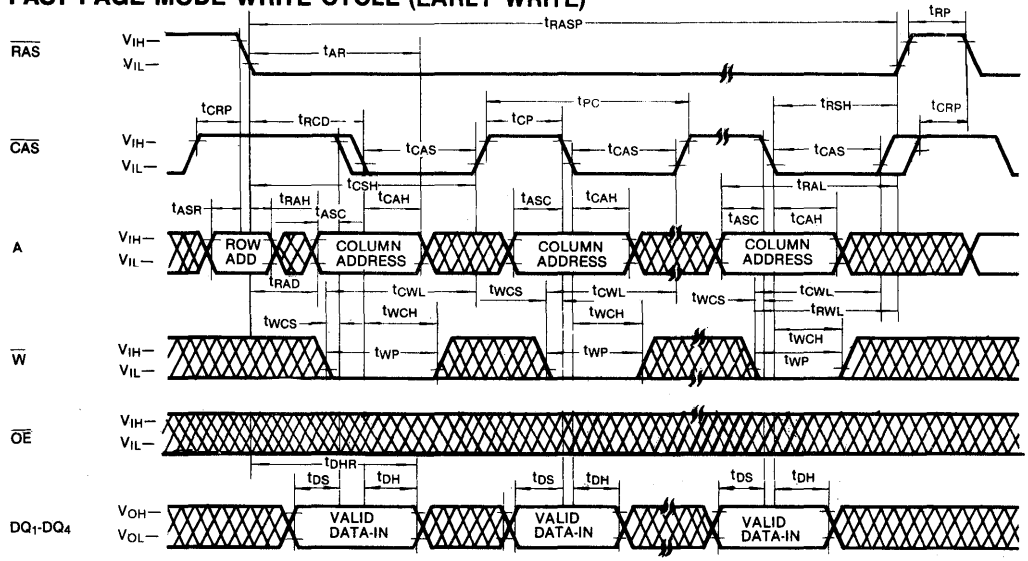


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



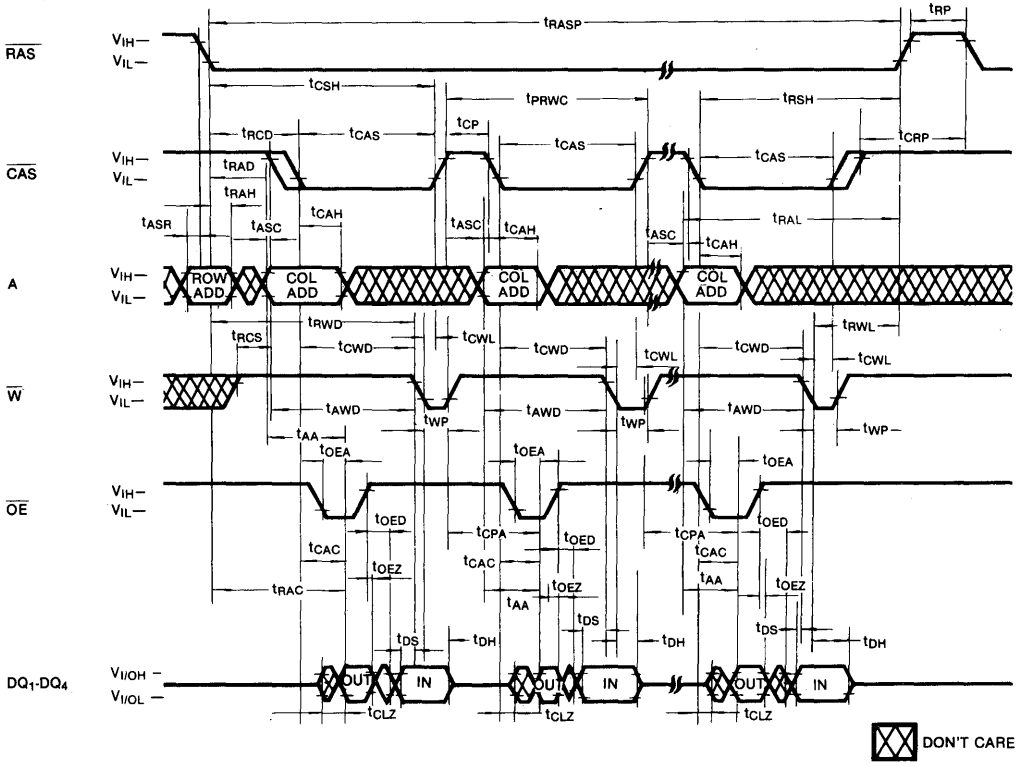
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

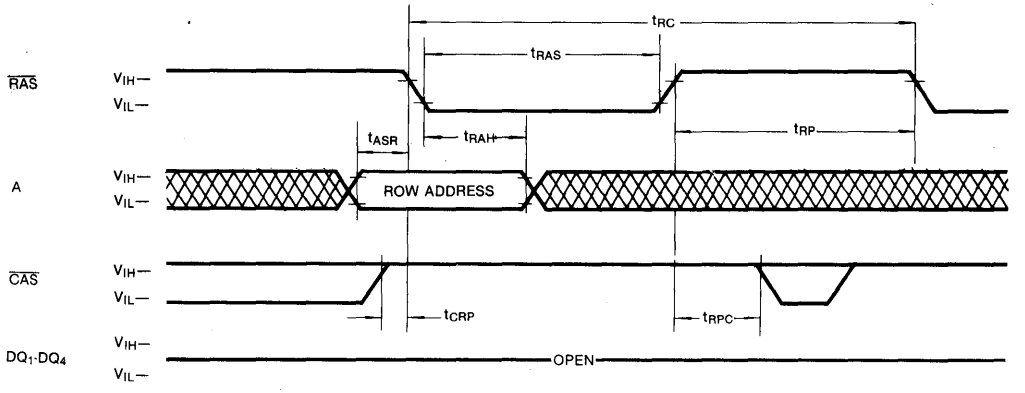
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

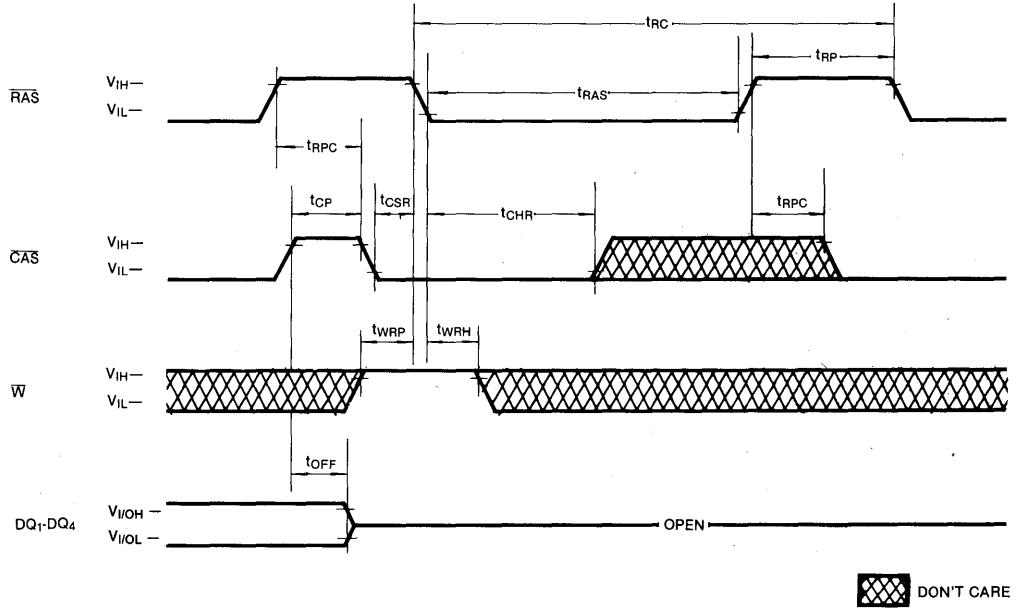
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



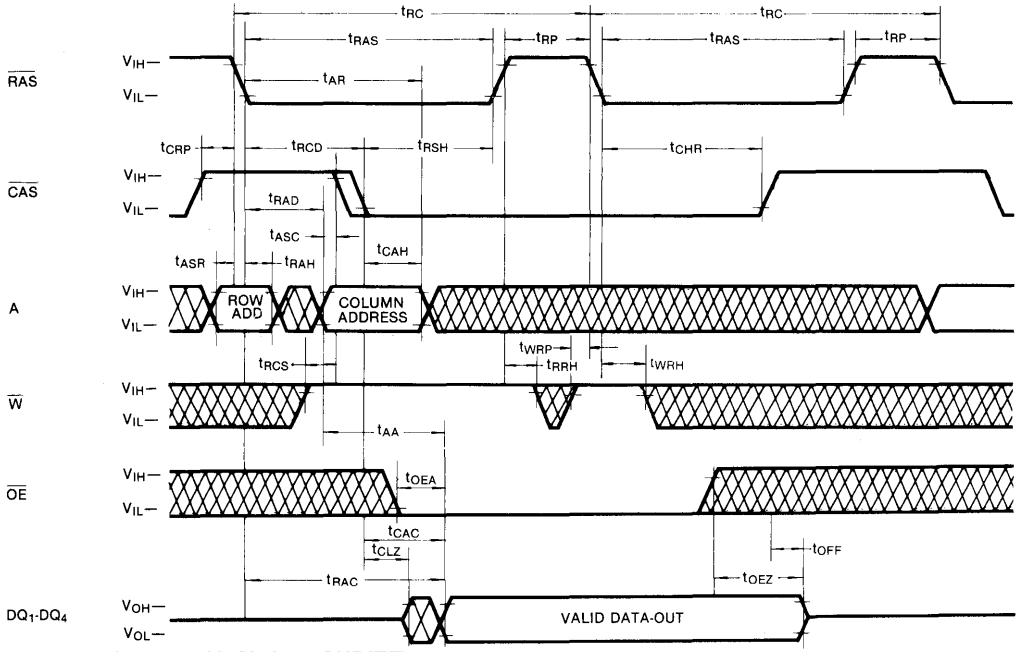
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

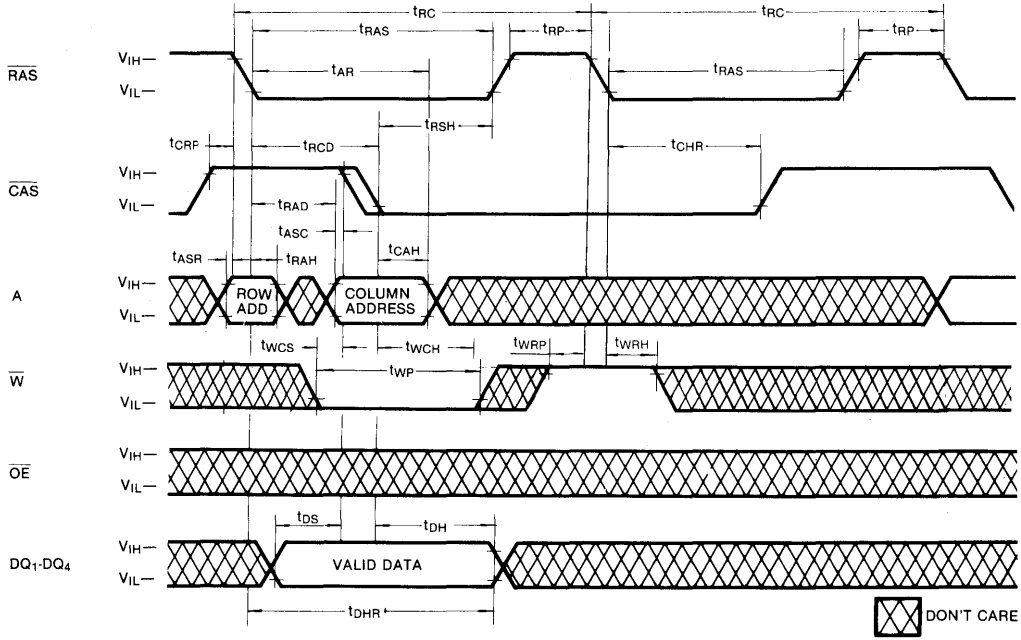


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

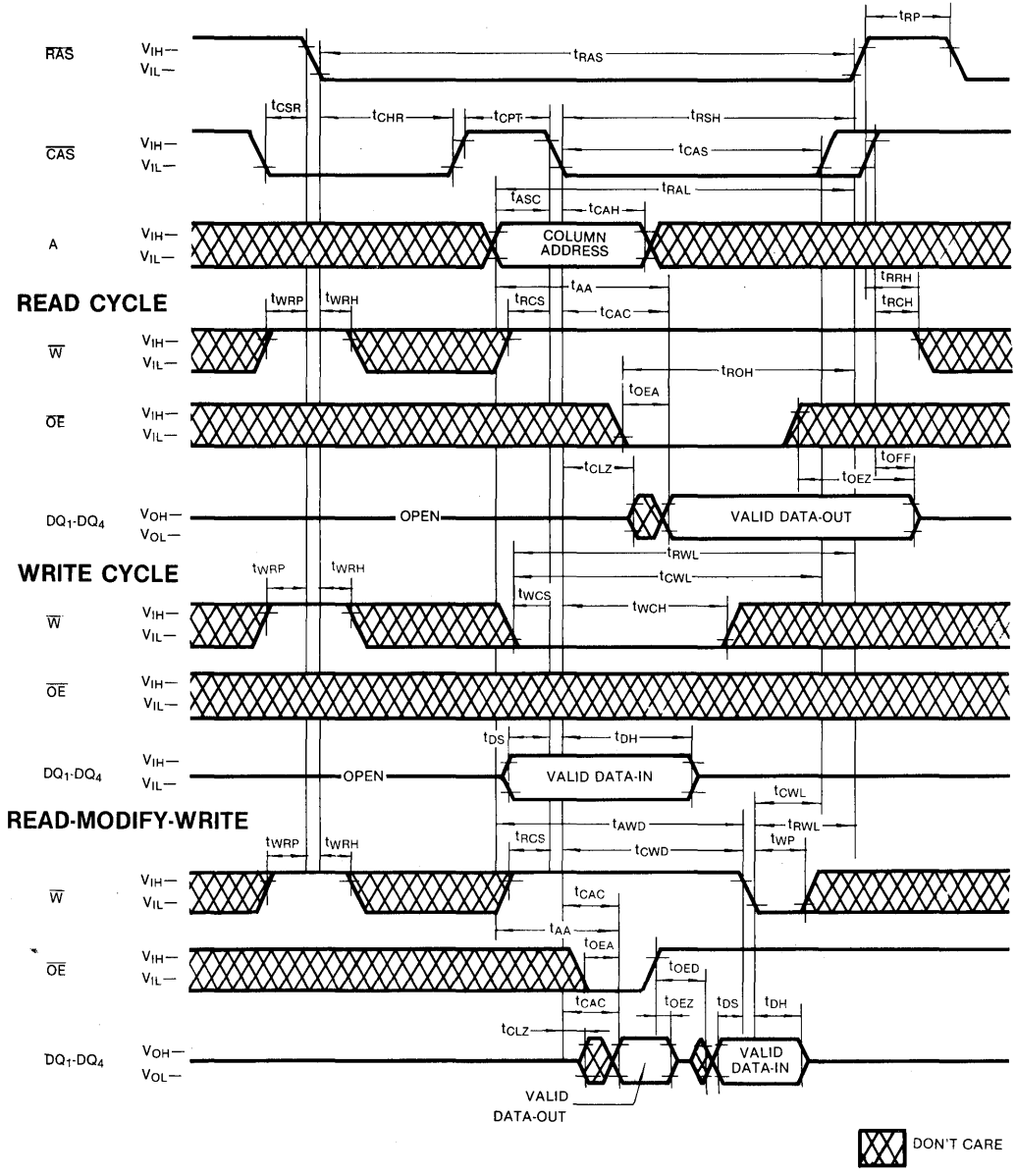


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

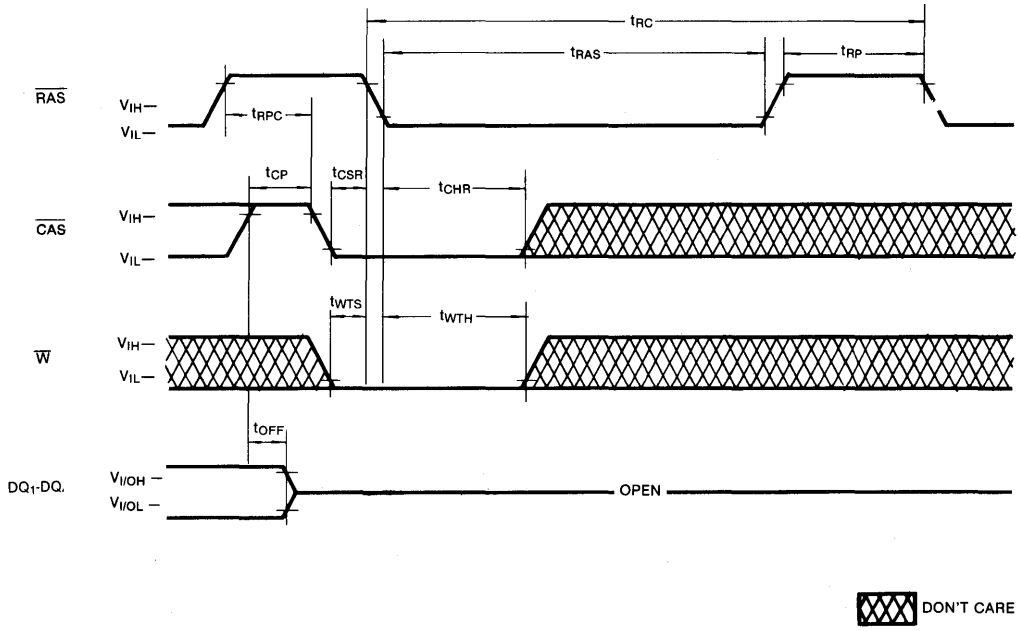
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000/L is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

"$\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test times (1/2 in case of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000/L contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000/L has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column address. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000/L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000/L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000/L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000/L can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000/L has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000/L operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000/L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

16/128 (L-version)ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000/L has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000/L hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000/L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000/L has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

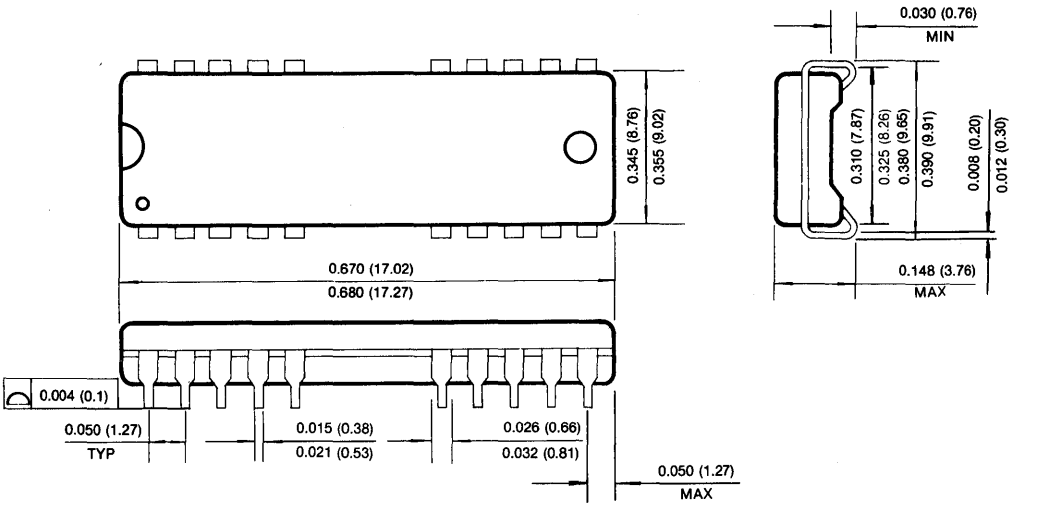
If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000/L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

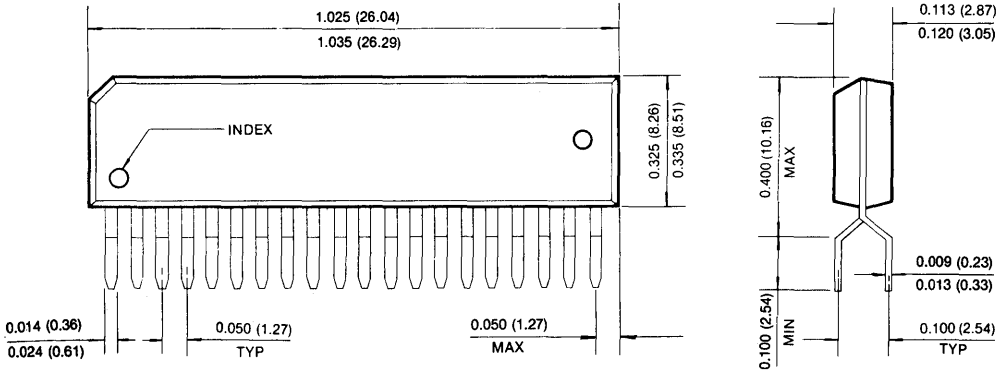
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



1M×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1002- 8	80ns	20ns	150ns
KM44C1002-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, ZIP**

GENERAL DESCRIPTION

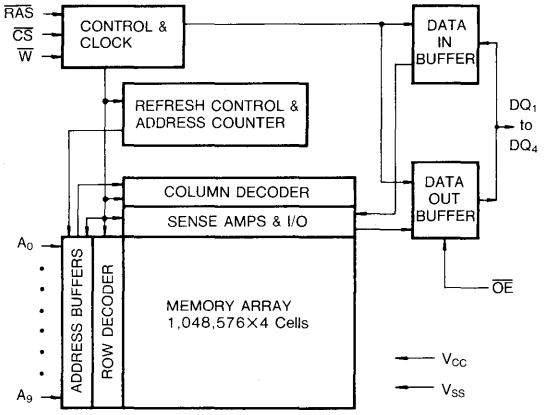
The Samsung KM44C1002 is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1002 features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

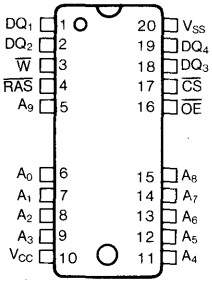
The KM44C1002 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

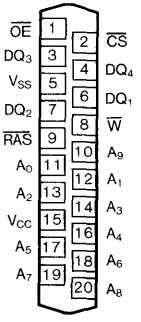


PIN CONFIGURATION (Top Views)

- **KM44C1002J**



- **KM44C1002Z**



Pin Name	Pin Function
A0-A9	Address Inputs
DQ_1-DQ_4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM44C1002- 8 KM44C1002-10	I_{CC1}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM44C1002- 8 KM44C1002-10	I_{CC3}	— —	100 85	mA mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address cycling: @ t_{SC}=min.)	KM44C1002- 8 KM44C1002-10	I_{CC4}	— —	70 60	mA mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ cycling @ t_{RC}=min.)	KM44C1002- 8 KM44C1002-10	I_{CC6}	— —	100 85	mA mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL} Dout=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. I_{CC} is specified as an average current. Specified value are obtained with the output open. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1002-8		KM44C1002-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	150		180		ns	
Read-modify-write cycle time	t_{RWC}	205		245		ns	
Static column mode cycle time	t_{SC}	45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	110		135		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		25	ns	3,4,5
Access time from column address	t_{AA}		40		50	ns	3,11
Access time from last write	t_{ALW}		75		95	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	20	ns	7
Output data hold time from column address	t_{AOH}	5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		50		70	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	25	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		10		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	65		75		ns	6
Column address hold referenced to $\overline{RAS}$	t_{AR}	60		75		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1002-8		KM44C1002-10		Unit	Notes
		Min	Max	Min	Max		
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		50		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	10		10		ns	
Last write to column address delay time	t_{LWAD}	25	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	75		95		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	9
Write command hold time	t_{WCH}	15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	6
Write command pulse width	t_{WP}	15		20		ns	
Write command inactive time	t_{WI}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		25		ns	
Data-in set-up time	t_{DS}	0		0		ns	10
Data-in hold time	t_{DH}	15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16	ms	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		85		ns	8
$\overline{CS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	30		30		ns	
$\overline{RAS}$ percharge to $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	40		50		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		ns	
Output buffer turn off delay time fron $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		ns	

TEST MODE CYCLE

(Note. 13)

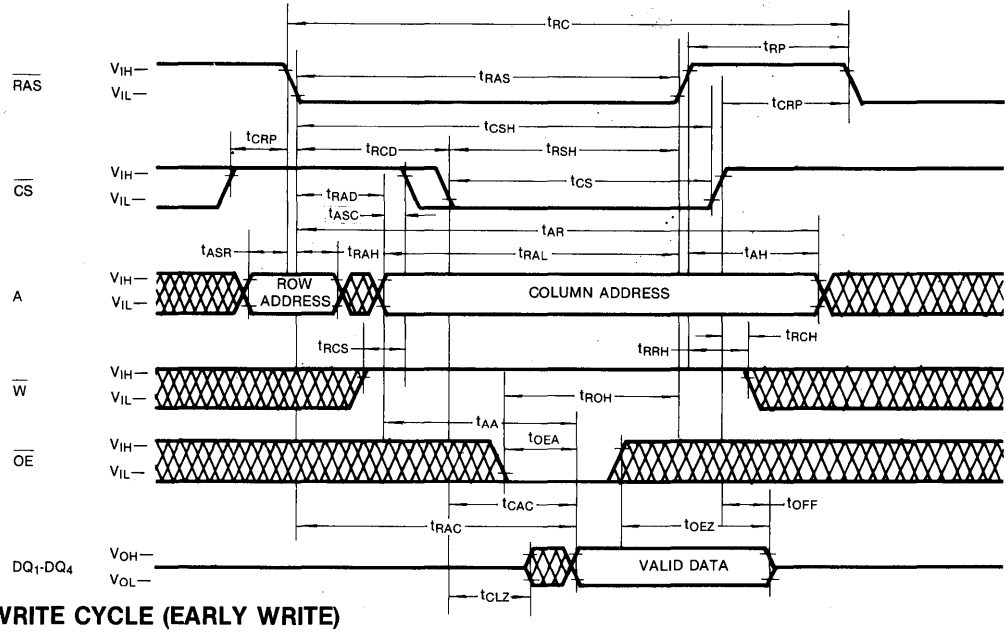
Parameter	Symbol	KM44C1002-8		KM44C1002-10		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	155		185		ns	
Read-modify-write cycle time	t_{RWC}	210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		30	ns	3,4,5
Access time from column address	t_{AA}		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		55		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	25		30		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	75		90		ns	8
Static column mode cycle time	t_{SC}	50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	115		140		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	30	100,000	ns	

NOTES

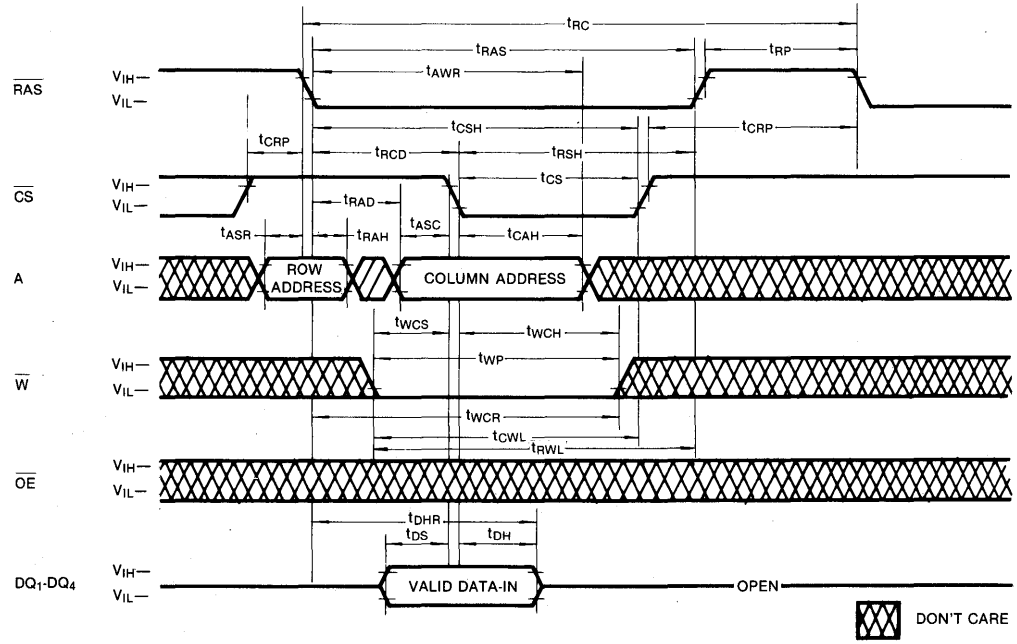
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. If t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

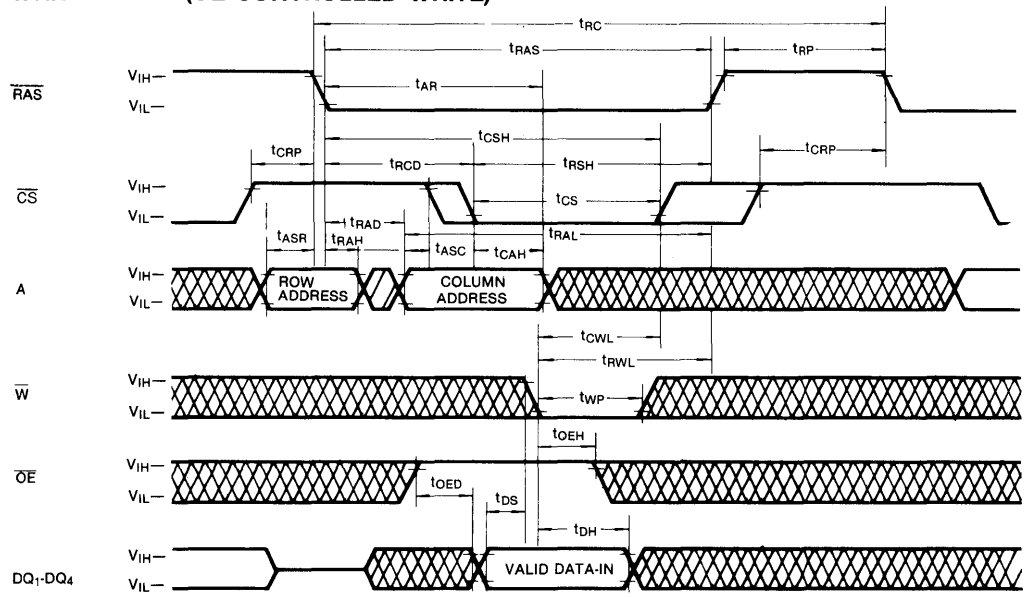


WRITE CYCLE (EARLY WRITE)

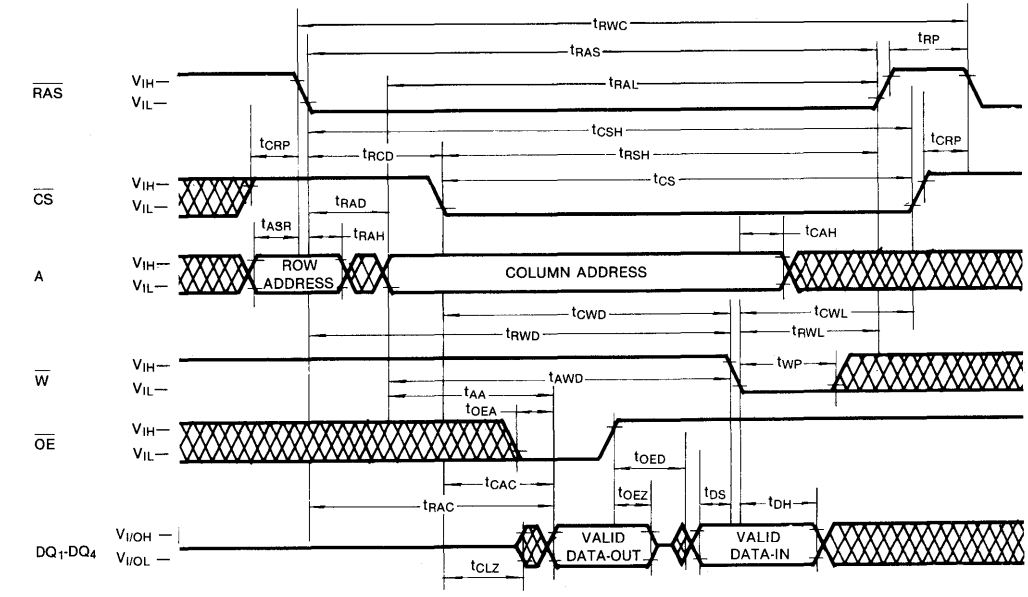


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



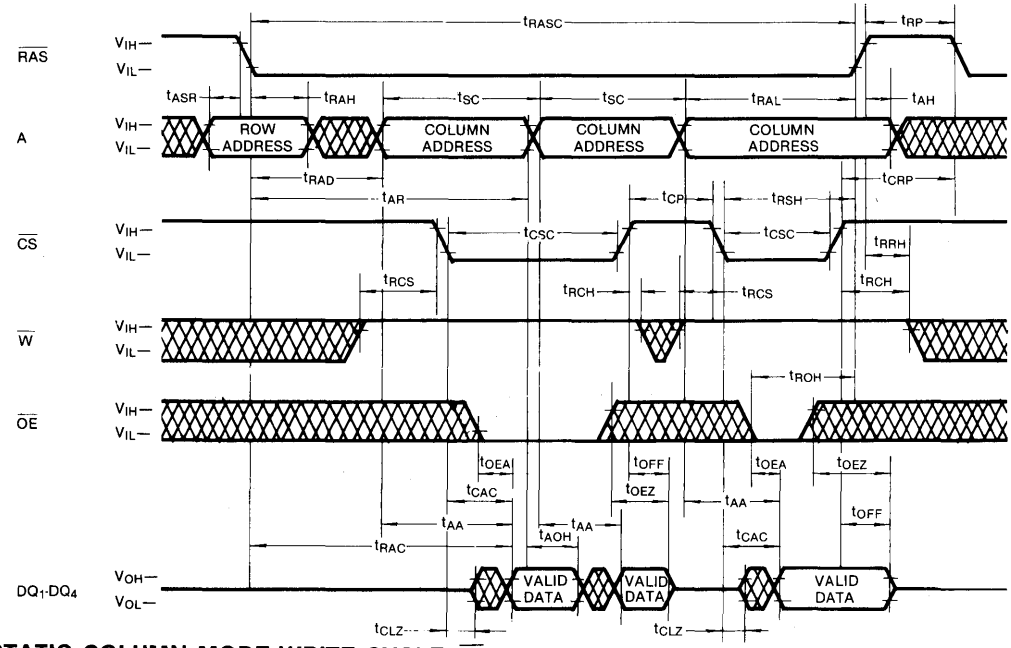
READ-WRITE/READ-MODIFY-WRITE CYCLE



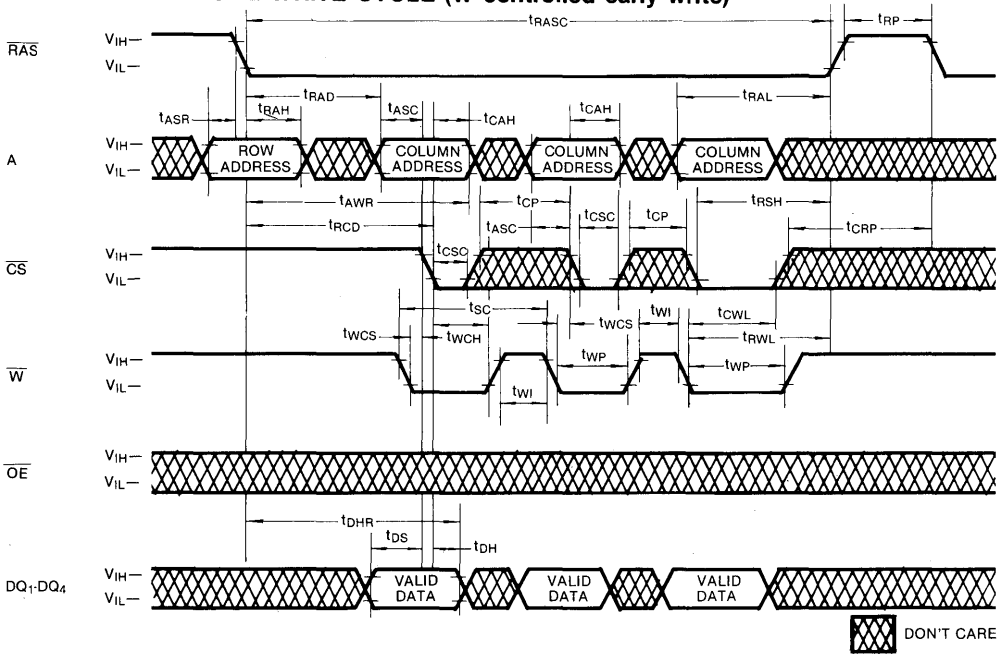
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

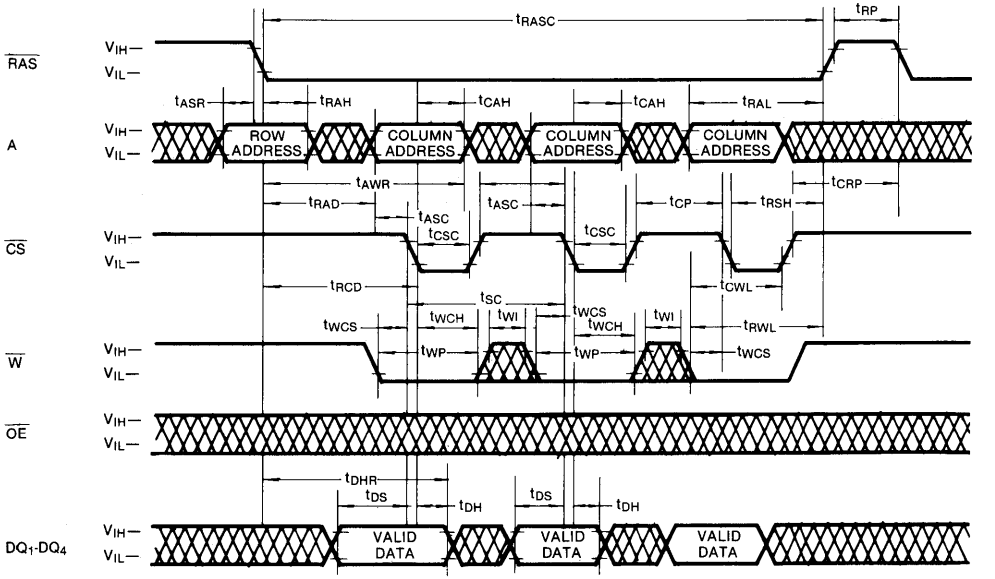


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

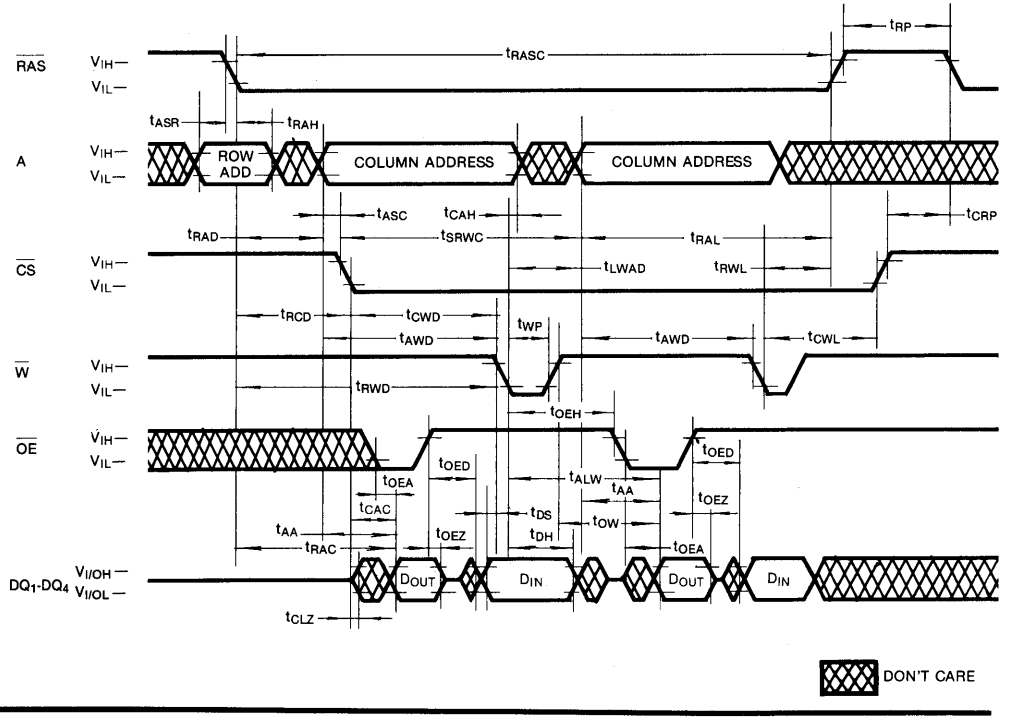


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

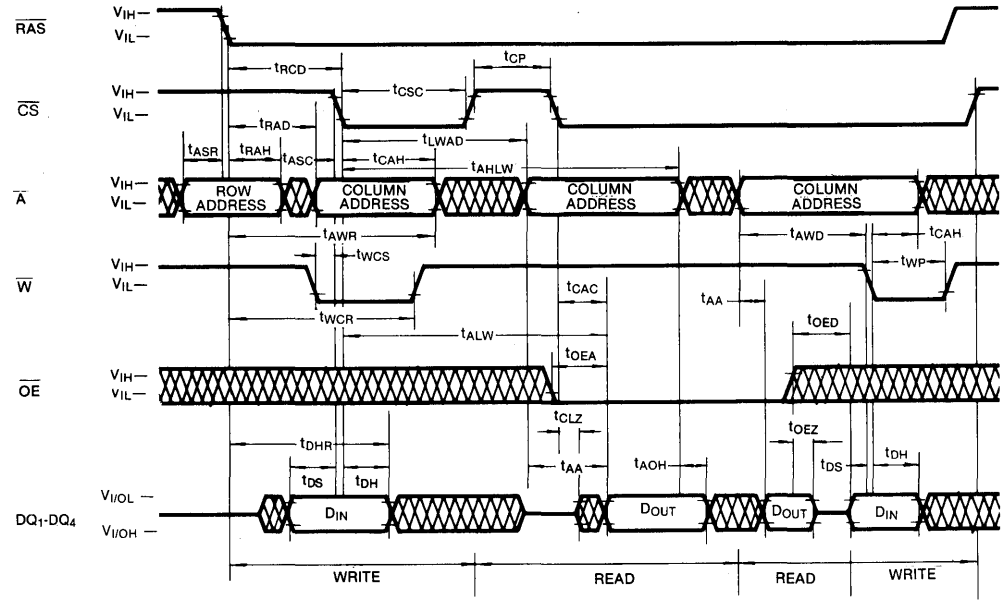


STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



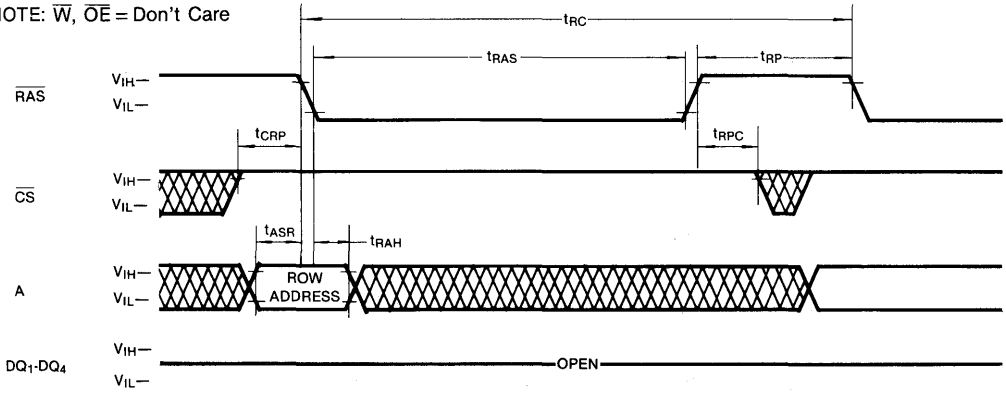
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



RAS-ONLY REFRESH CYCLE

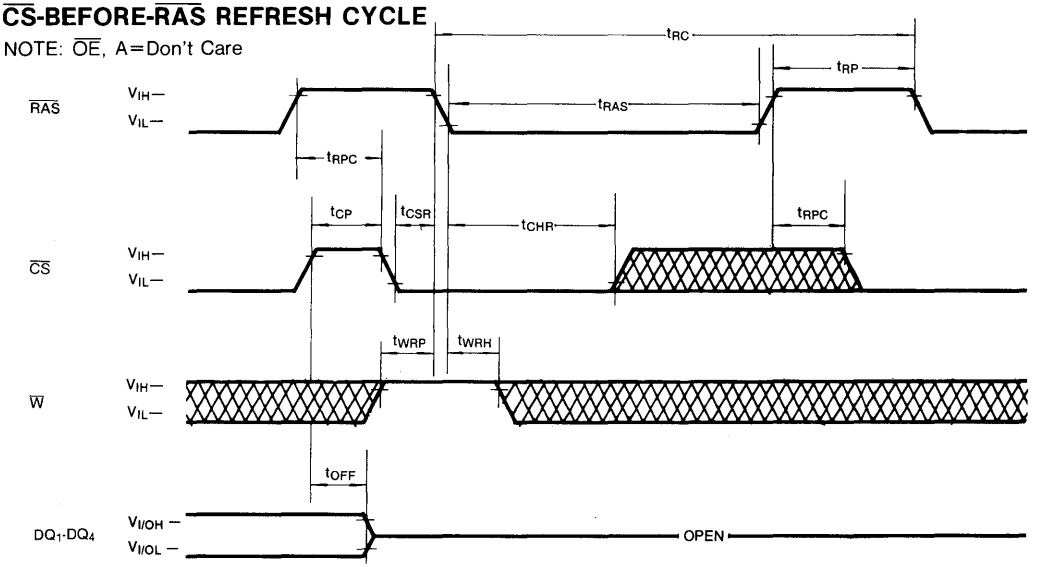
NOTE: W, OE = Don't Care



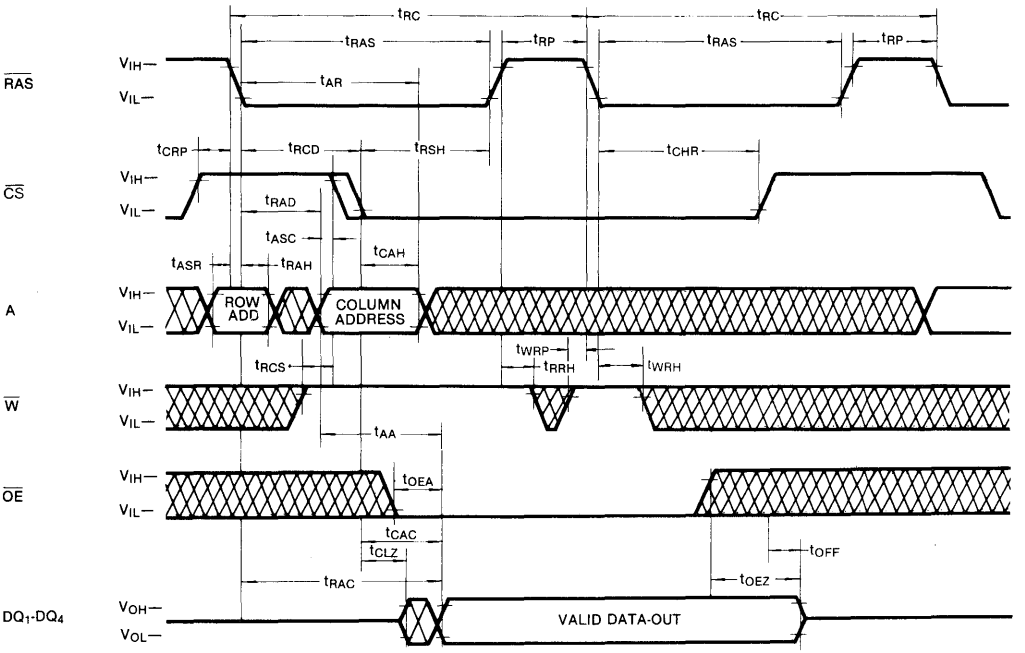
TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, A=Don't Care

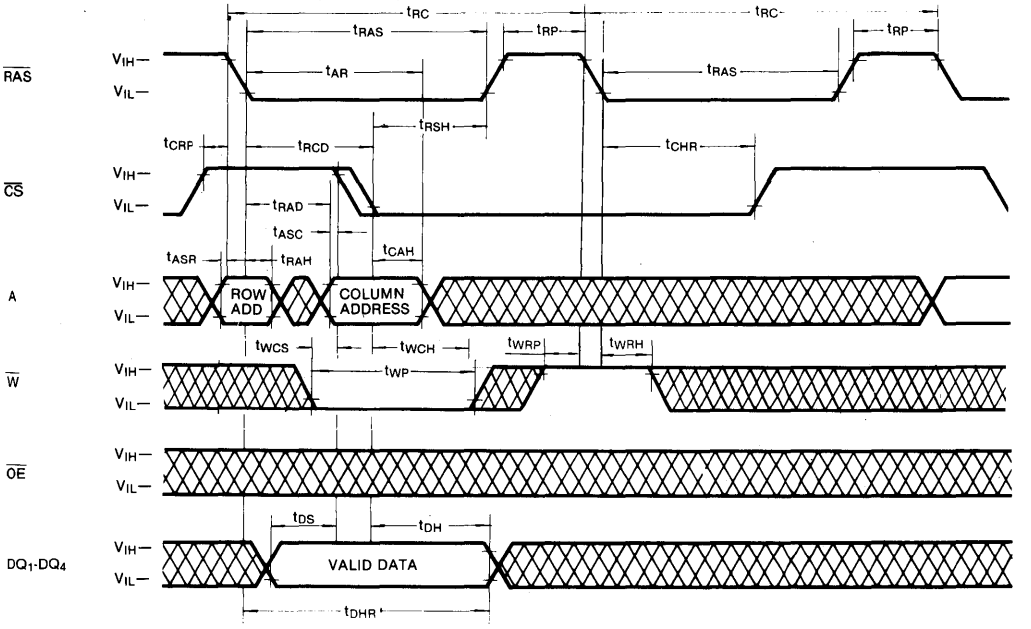


HIDDEN REFRESH CYCLE (READ)



TIMING DIAGRAMS (Continued)

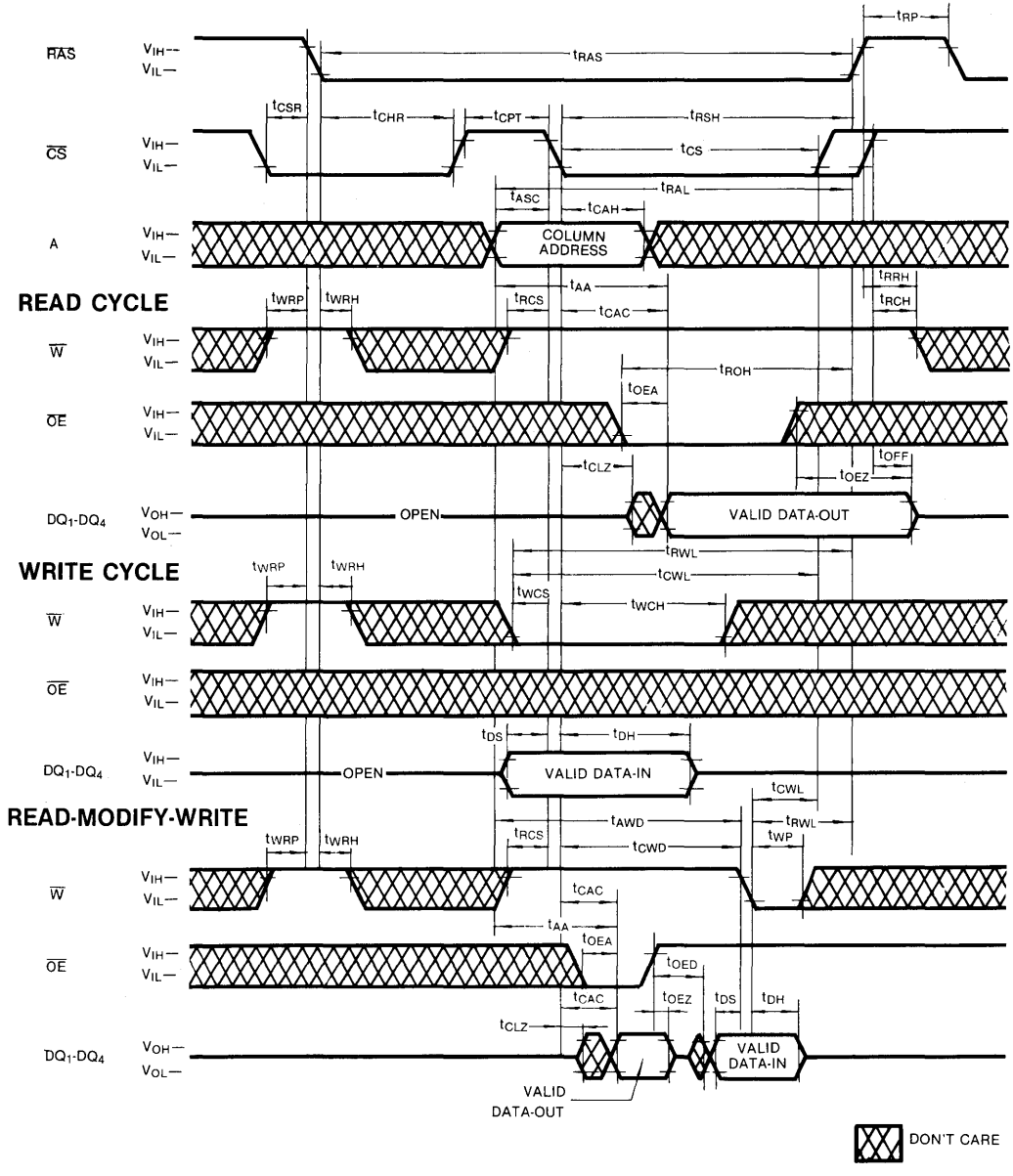
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

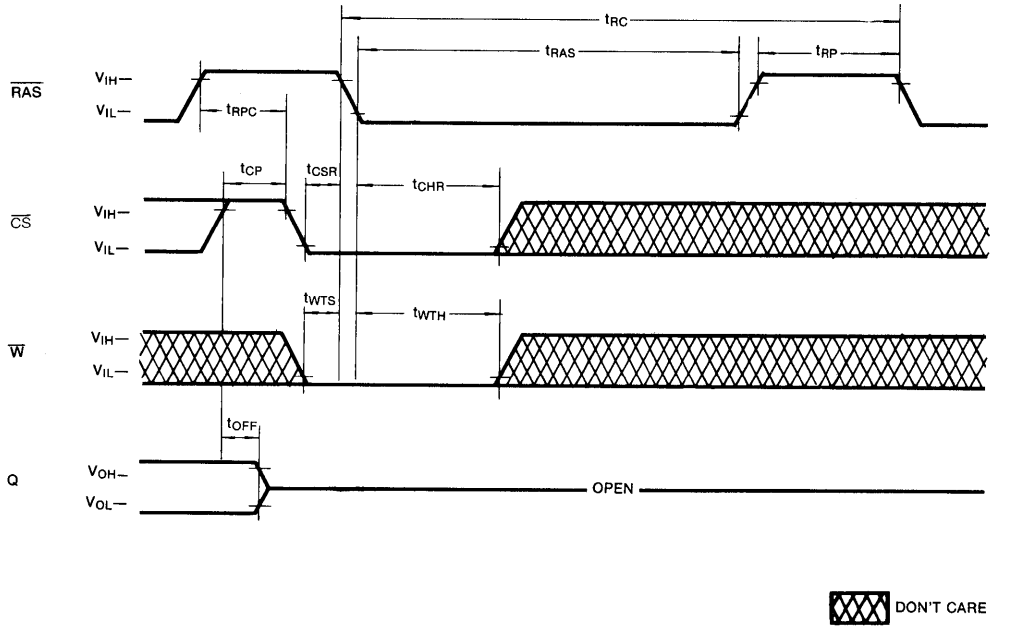
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002 is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1002 contains 4,194,304 memory locations organized as 1,048,576 four-bit words. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1002 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The mutliplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM44C1002 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1002 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C1002 has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1002 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1002's DQ pins.

Data Output

The KM44C1002 has a three-state output buffer which is controlled by $\overline{CS}$ and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1002 operating cycle is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle. $\overline{OE}$ controlled write.

DEVICE OPERATION (Continued)

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1002 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1002 has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1002 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triqered by the latter falling edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column ADdress—Bits A_0 through A_9 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

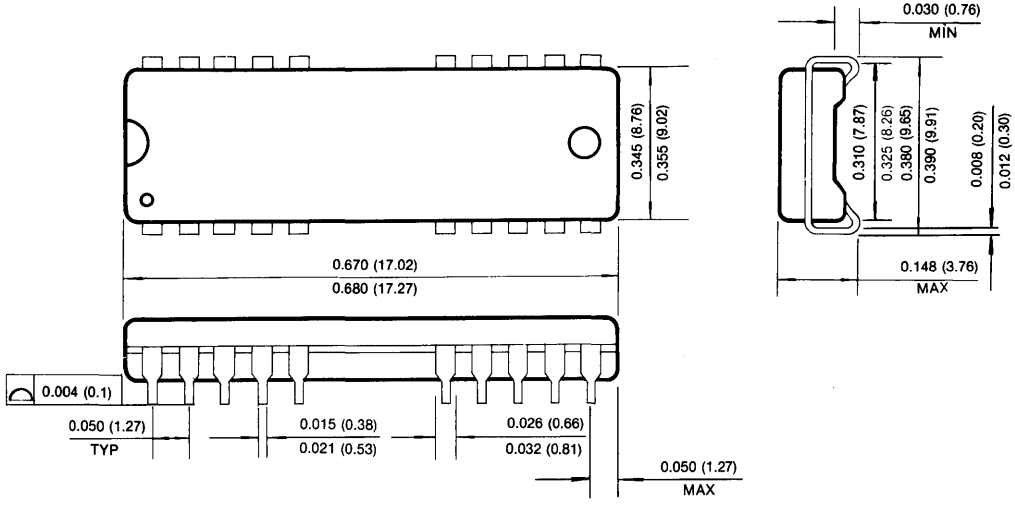
IF $\overline{RAS}=V_{SS}$ during power-up, the KM44C1002 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

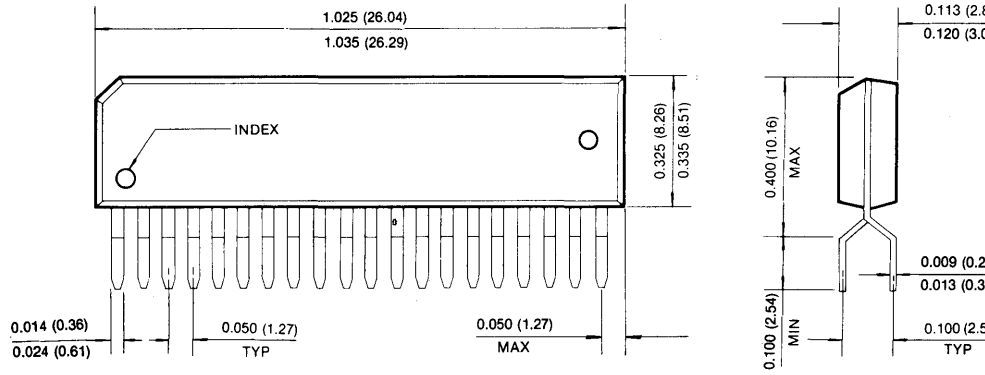
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000A- 7	70ns	20ns	130ns
KM44C1000A- 8	80ns	20ns	150ns
KM44C1000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fase parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

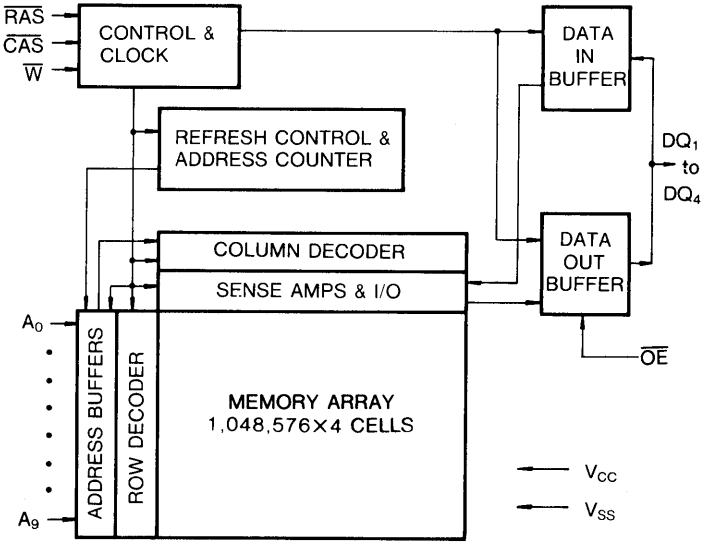
The Samsung KM44C1000A is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

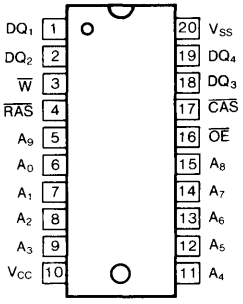
The KM44C1000A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



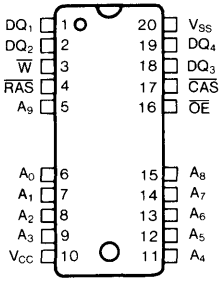
PIN CONFIGURATION (Top Views)

• KM44C1000AP



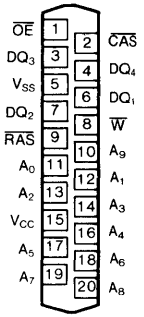
(DIP)

• KM44C1000AJ



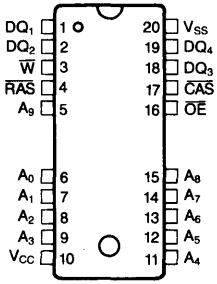
(SOJ)

• KM44C1000AZ



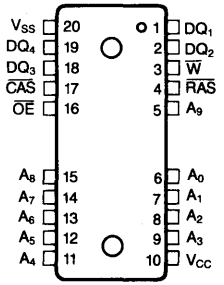
(ZIP)

• KM44C1000AT



(TSOP(II)-Forward Type)

• KM44C1000ATR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000A- 7	I_{CC1}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000A- 7	I_{CC3}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000A- 7	I_{CC4}	—	80	mA
	KM44C1000A- 8		—	70	mA
	KM44C1000A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=W≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000A- 7	I_{CC6}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4} Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

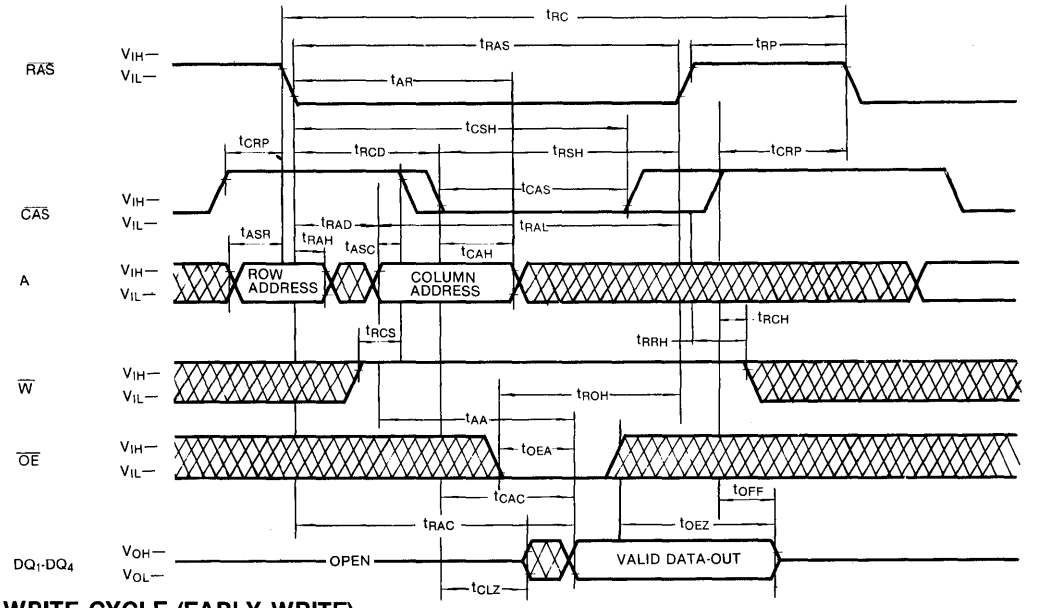
Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

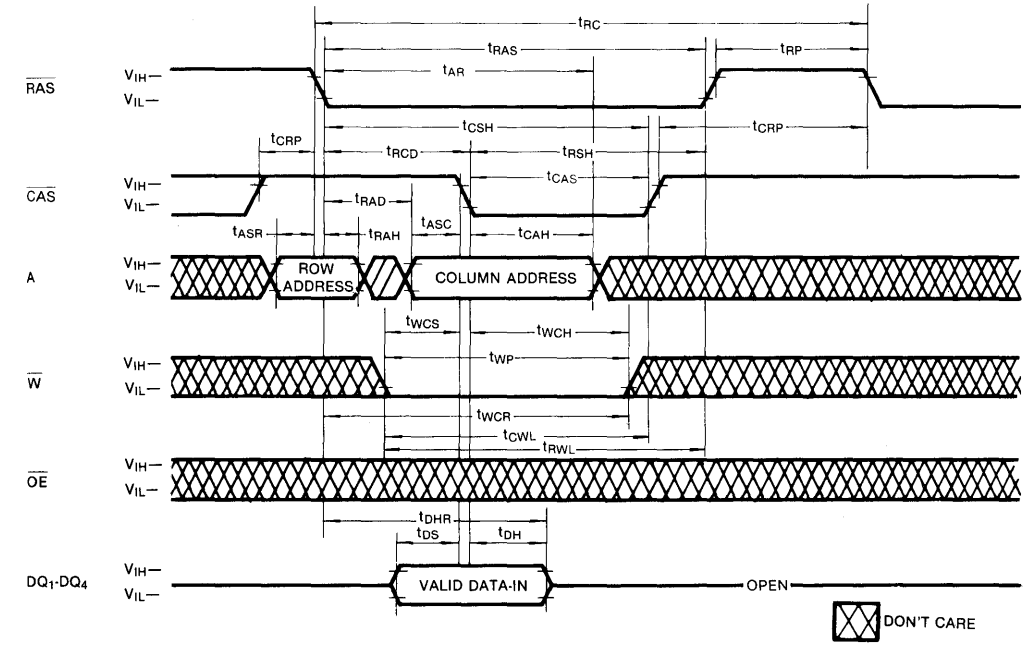
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

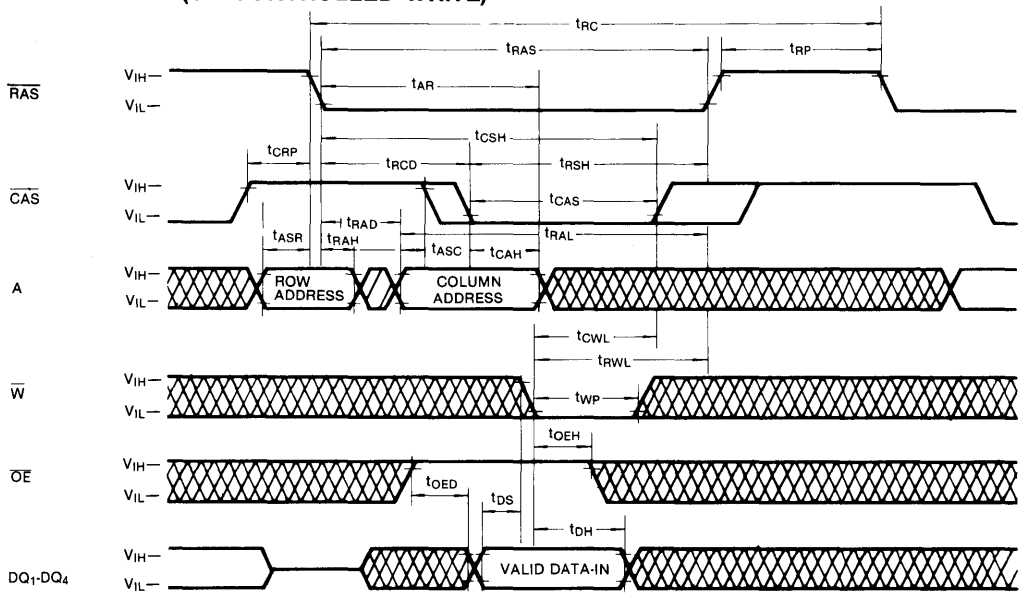


WRITE CYCLE (EARLY WRITE)

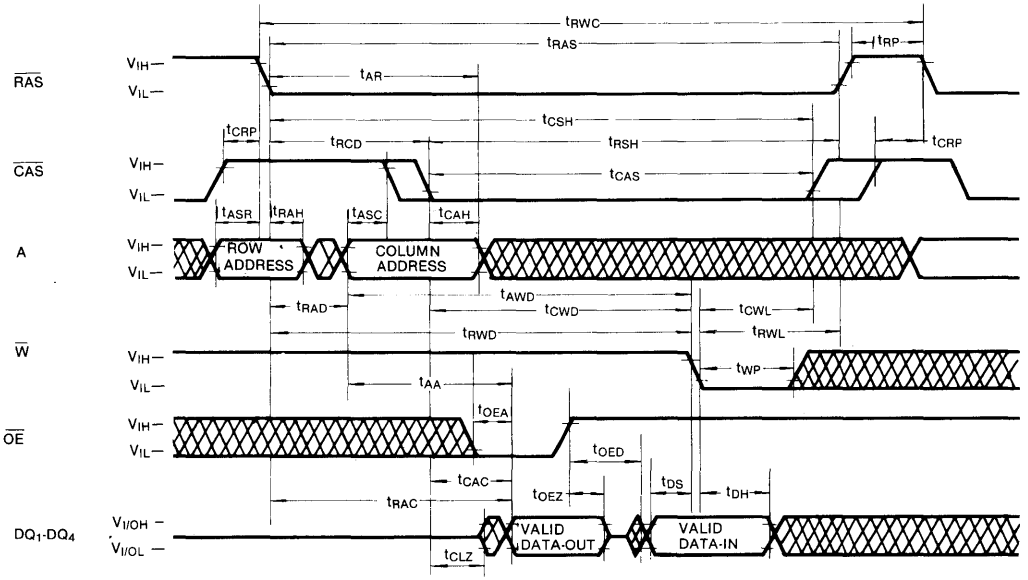


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



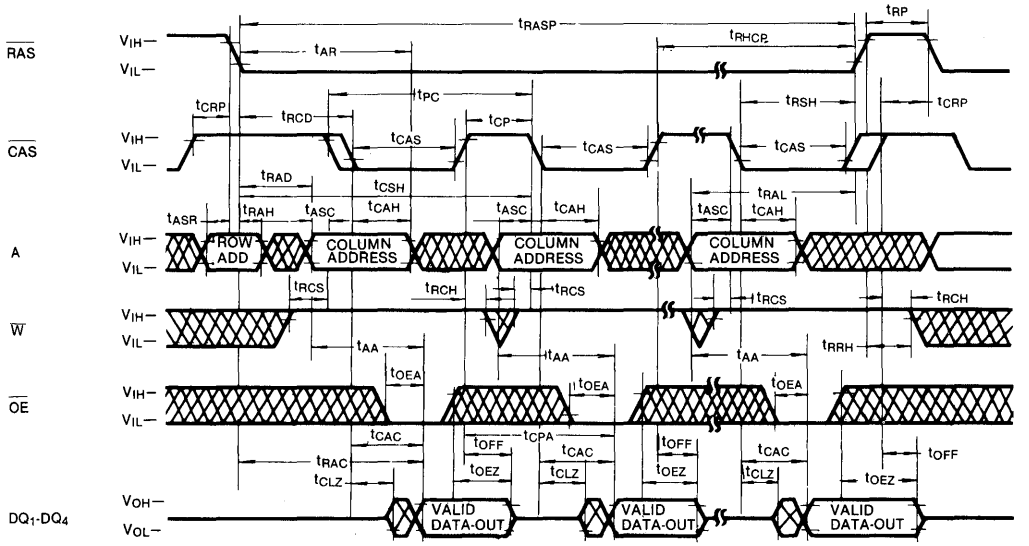
READ-MODIFY-WRITE CYCLE



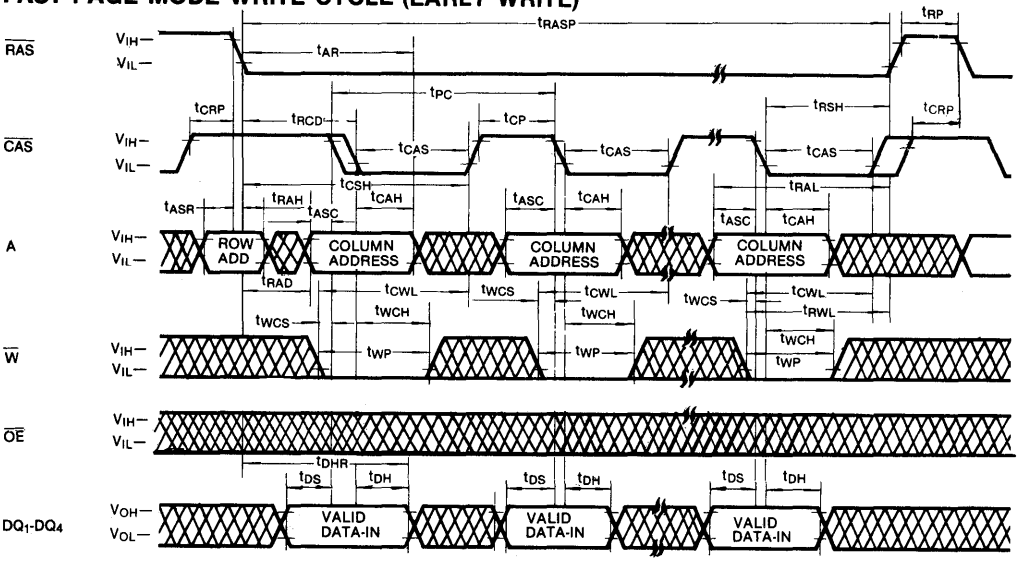
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



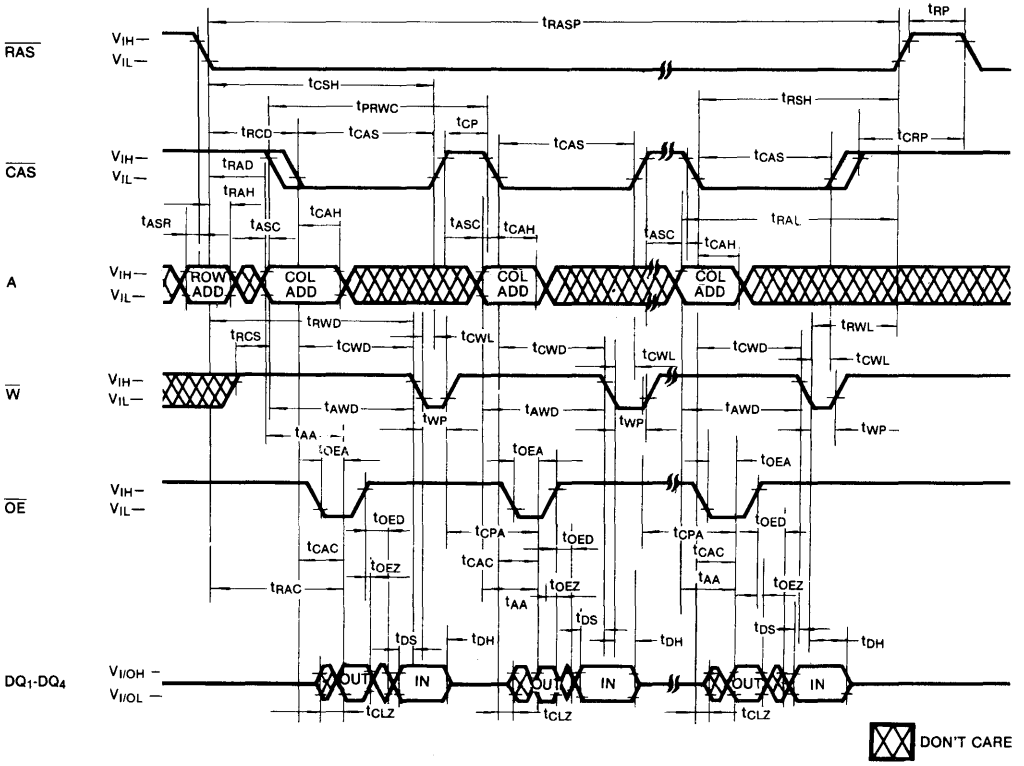
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

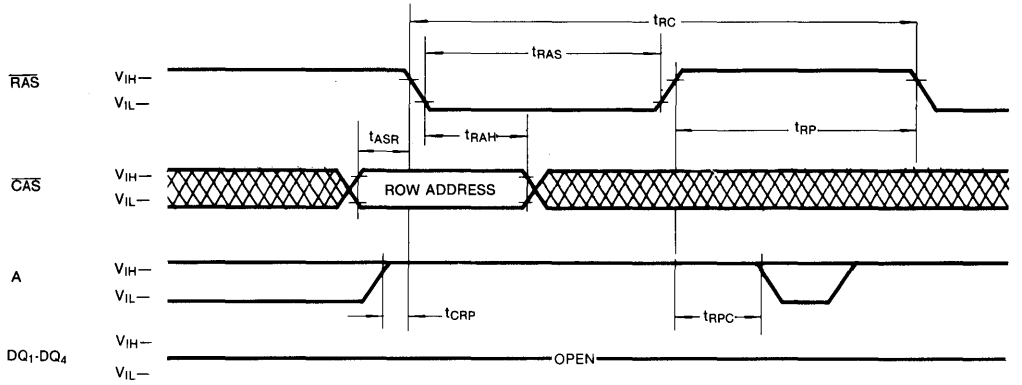
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

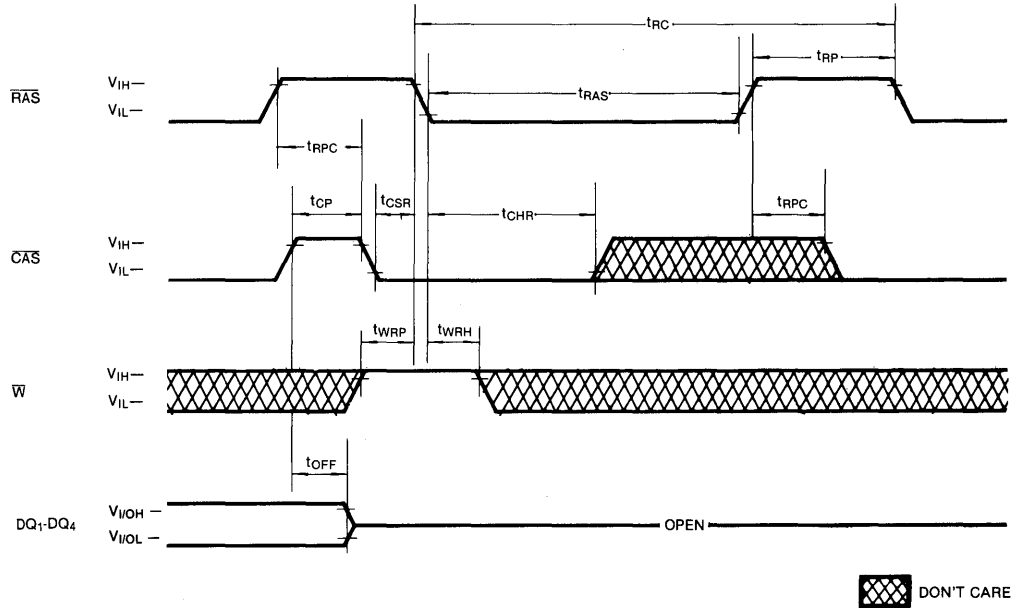
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



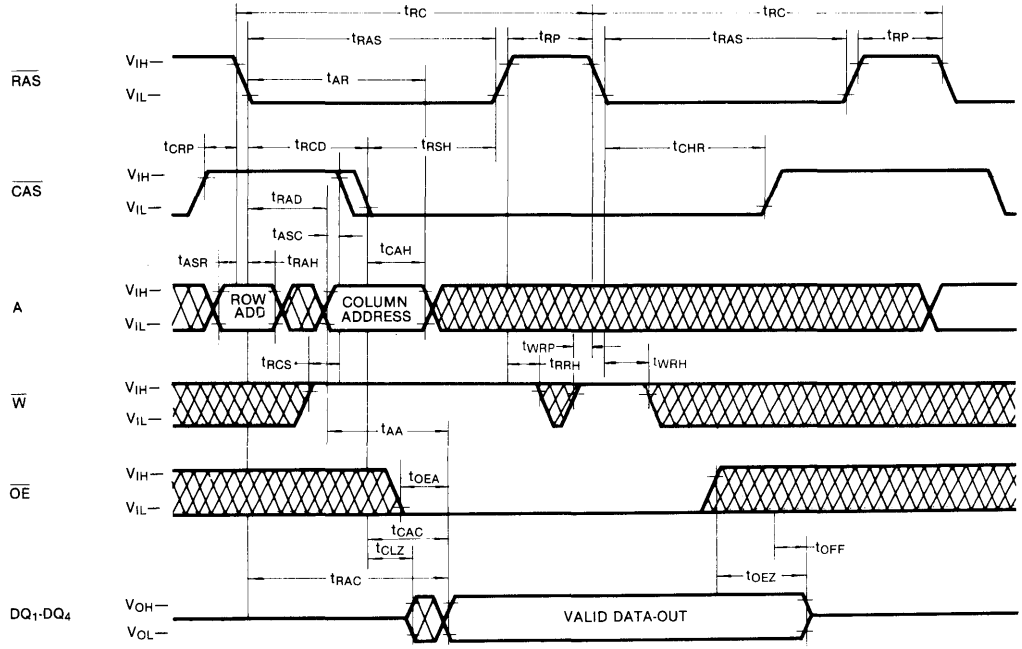
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

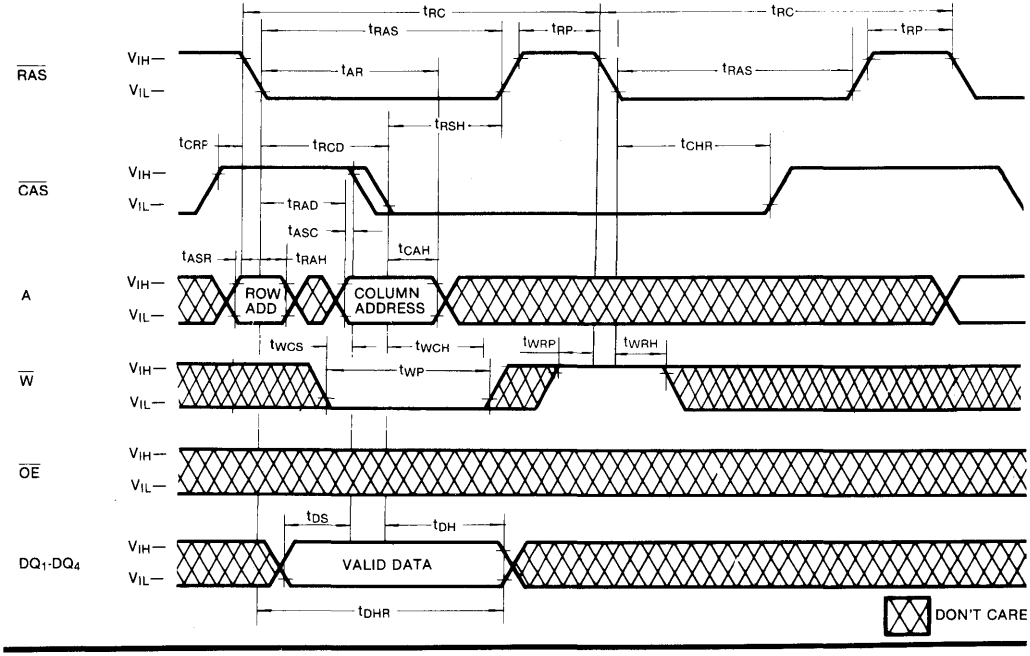


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

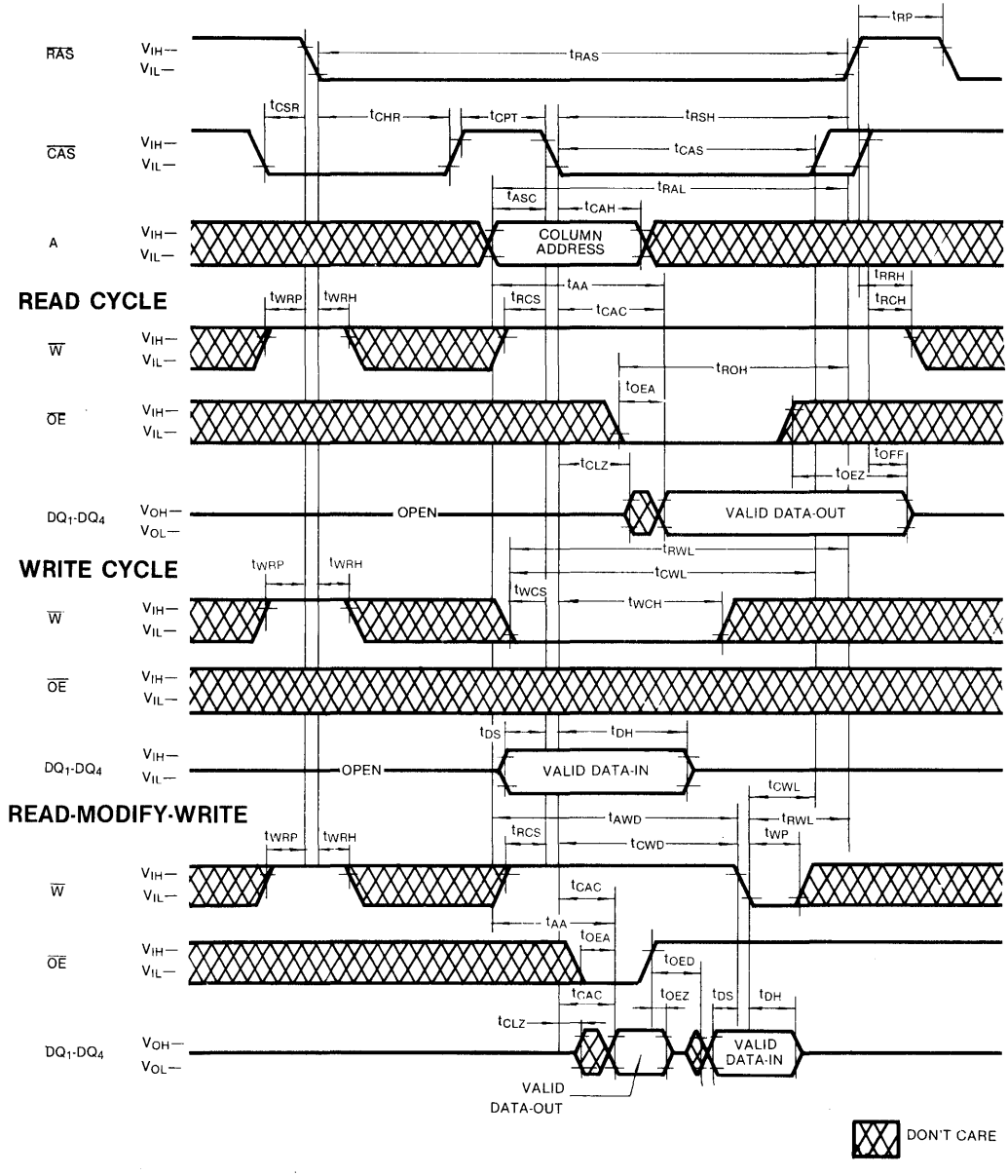


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

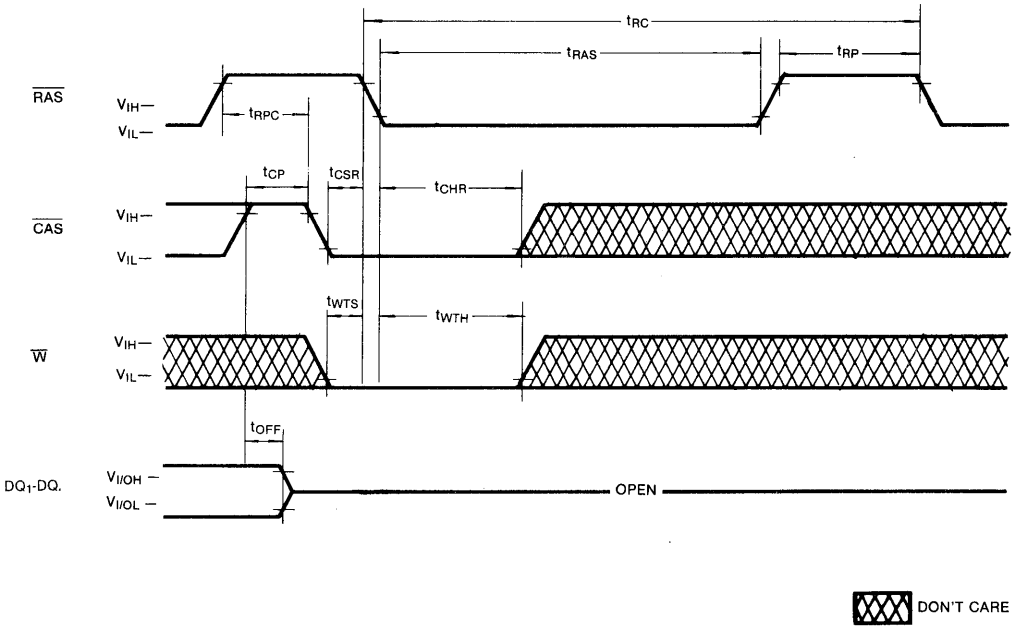
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000A contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000A has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000A has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

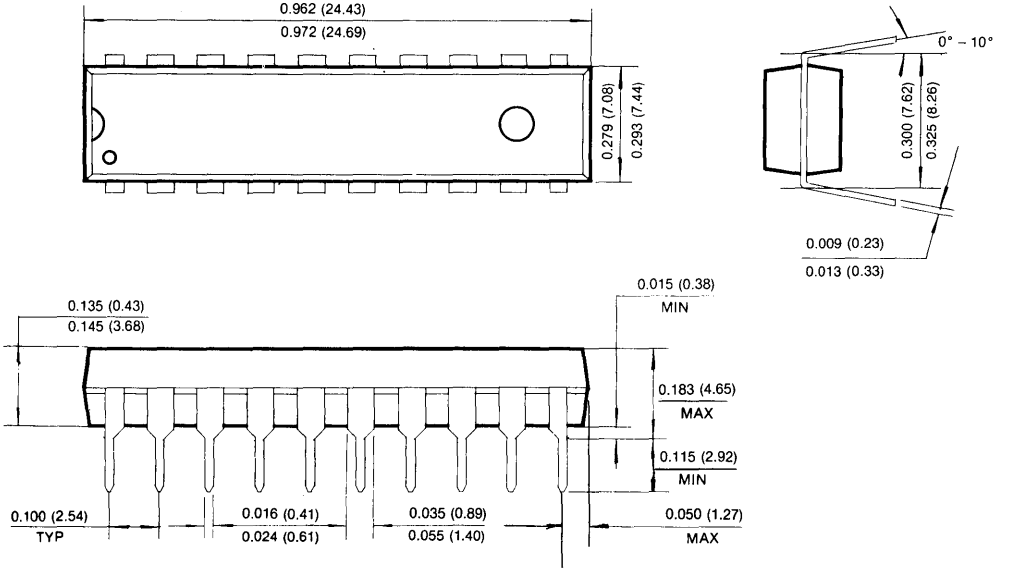
Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

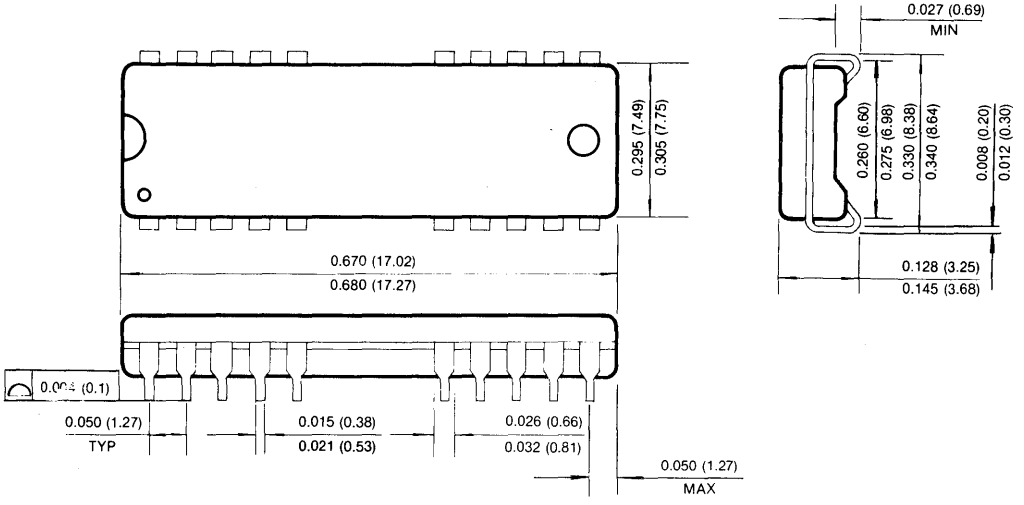
An initial pause of 200μs is required power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



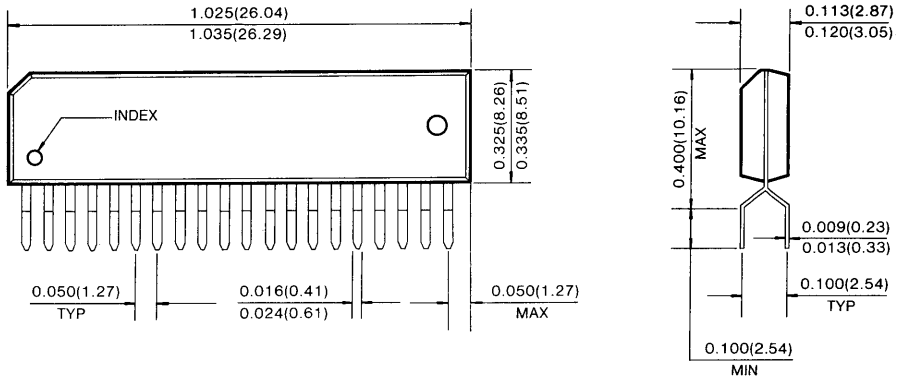
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



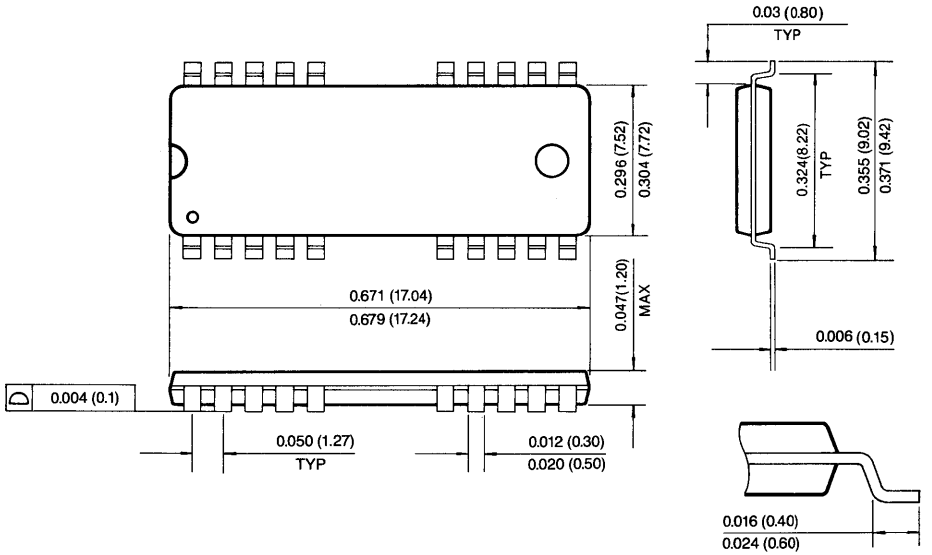
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000AL- 7	70ns	20ns	130ns
KM44C1000AL- 8	80ns	20ns	150ns
KM44C1000AL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/128ms refresh**
- **Low power dissipation**
  - **—Standby: 1.1mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

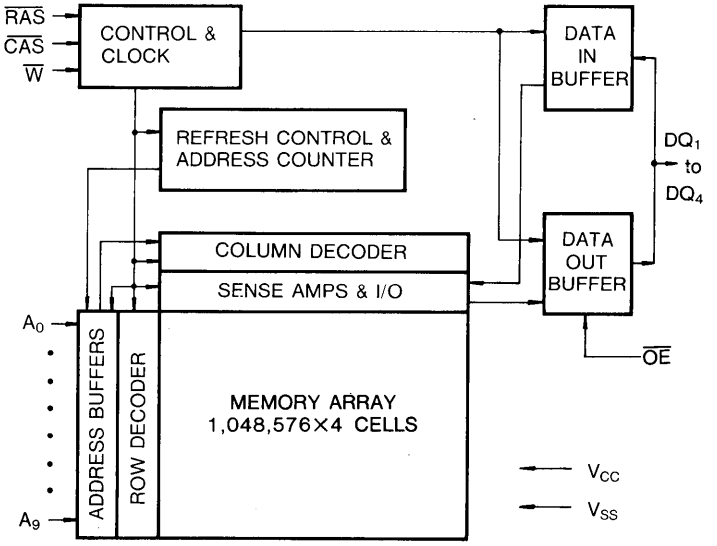
The Samsung KM44C1000AL is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000AL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

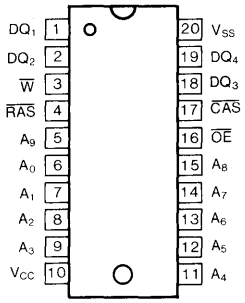
The KM44C1000AL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



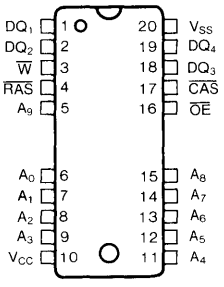
PIN CONFIGURATION (Top Views)

• KM44C1000ALP



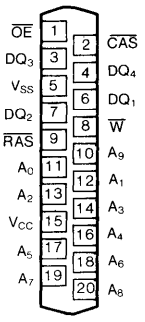
(DIP)

• KM44C1000ALJ



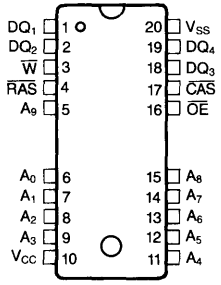
(SOJ)

• KM44C1000ALZ



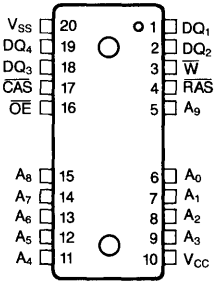
(ZIP)

• KM44C1000ALT



(TSOP (II)-Forward Type)

• KM44C1000ALTR



(TSOP (II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000AL- 7	I_{CC1}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000AL- 7	I_{CC3}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000AL- 7	I_{CC4}	—	80	mA
	KM44C1000AL- 8		—	70	mA
	KM44C1000AL-10		—	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=W \geq V_{CC}-0.2V$)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000AL- 7	I_{CC6}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}=\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care T_{RC}=125μS, $T_{RAS}=t_{RAS}$ min.~1μS		I_{CC7}	—	300	μA
Standby Current ($\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

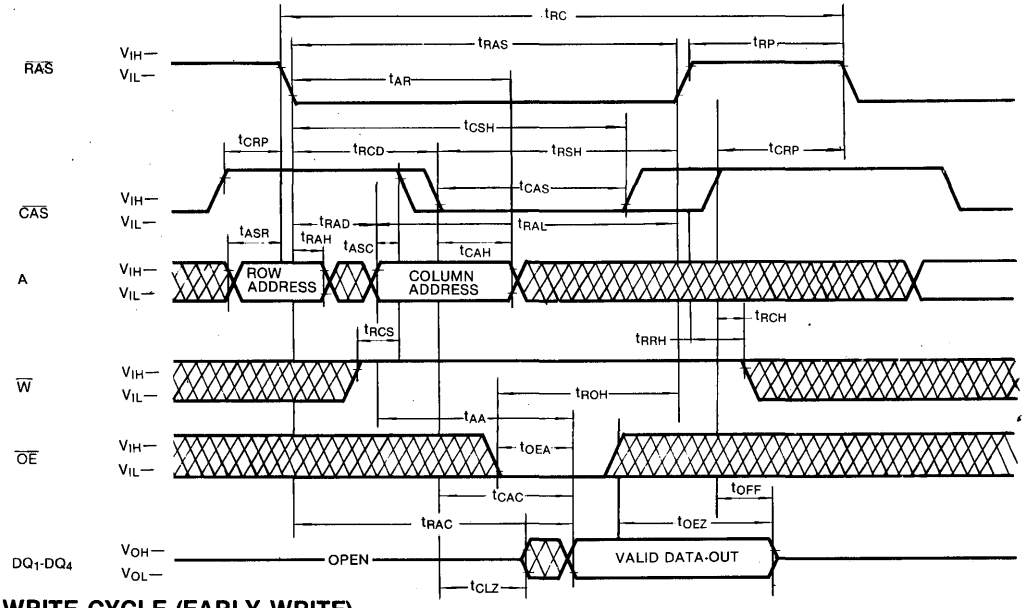
Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

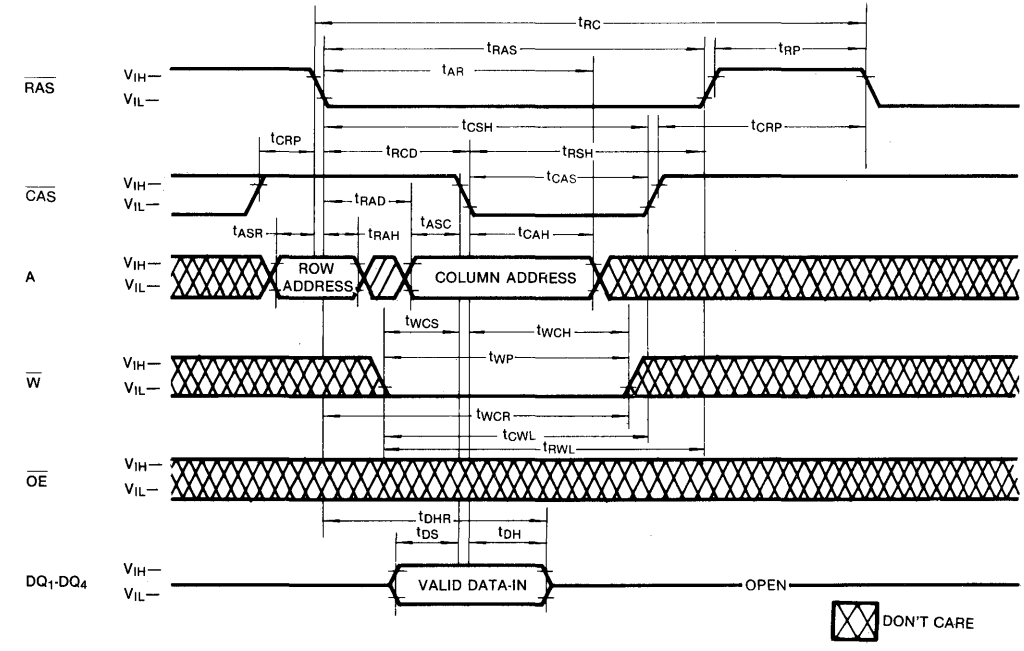
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

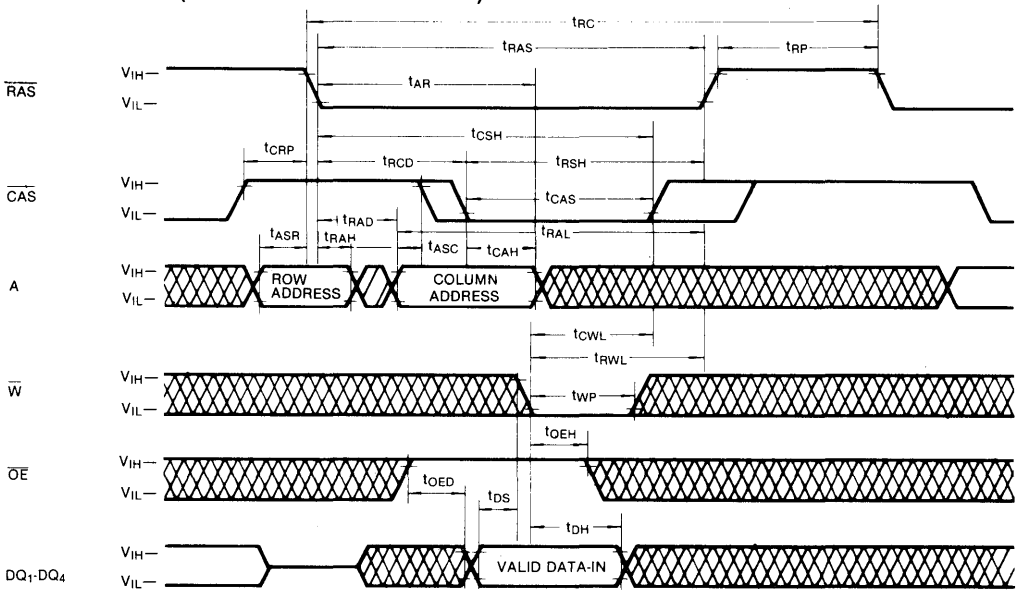


WRITE CYCLE (EARLY WRITE)

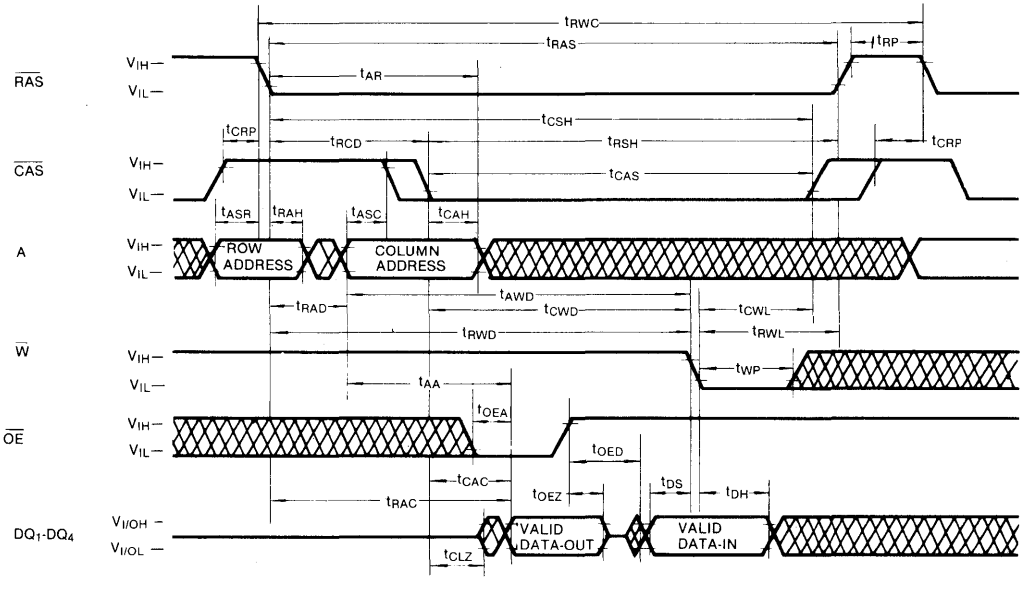


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



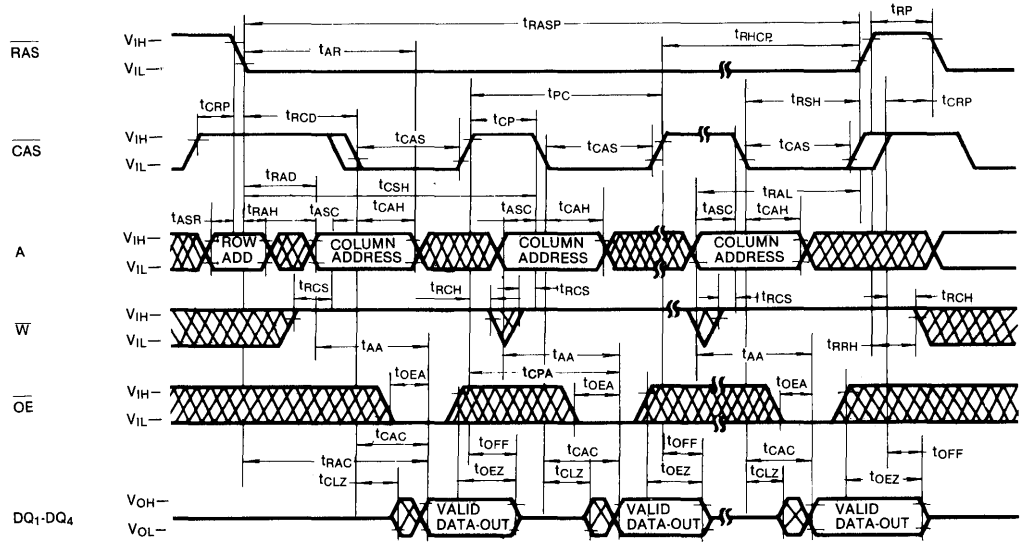
READ-MODIFY-WRITE CYCLE



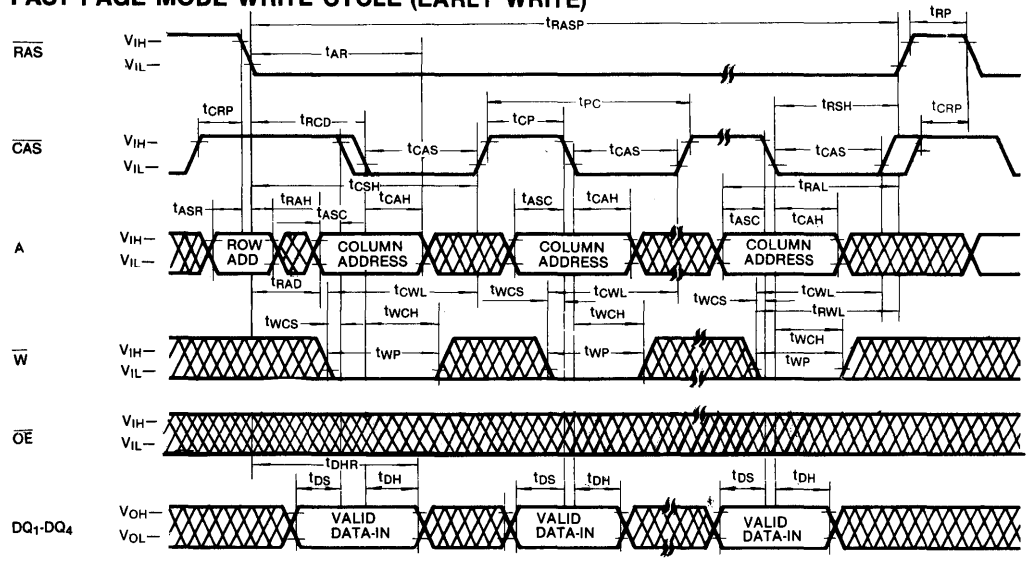
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



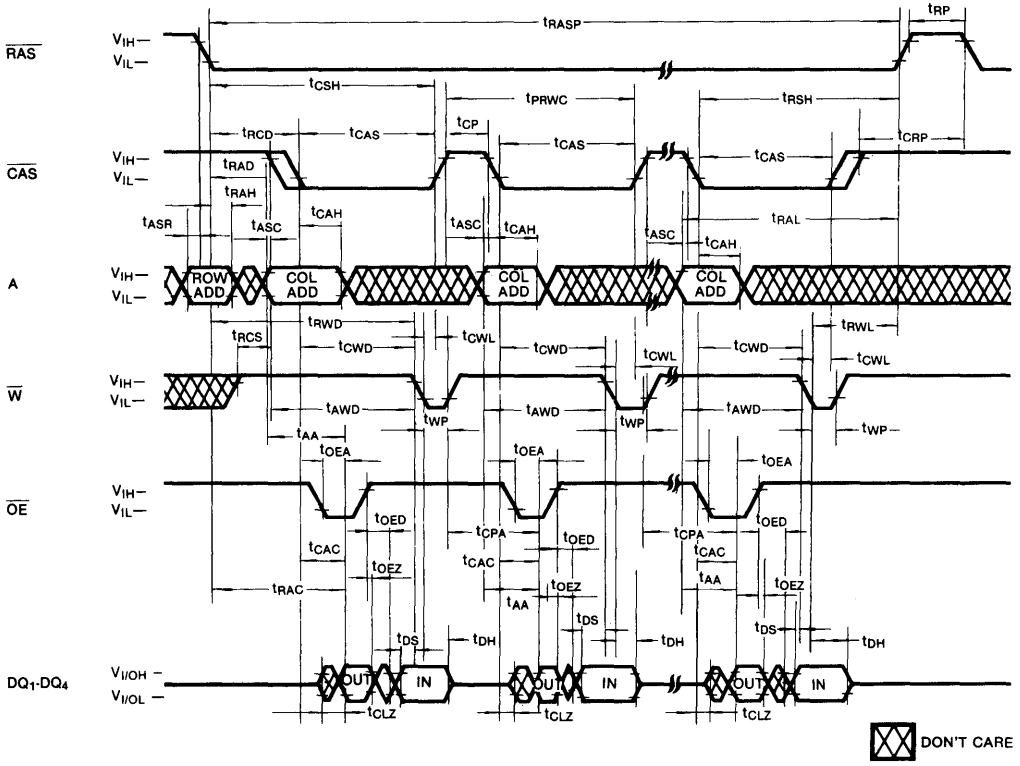
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

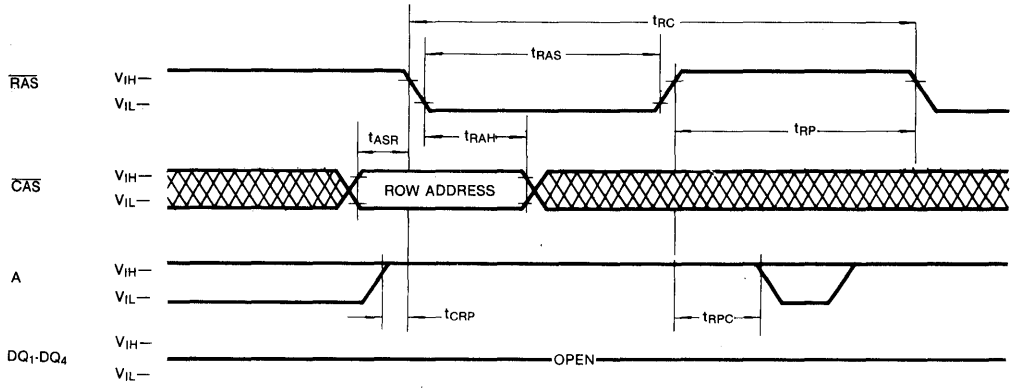
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

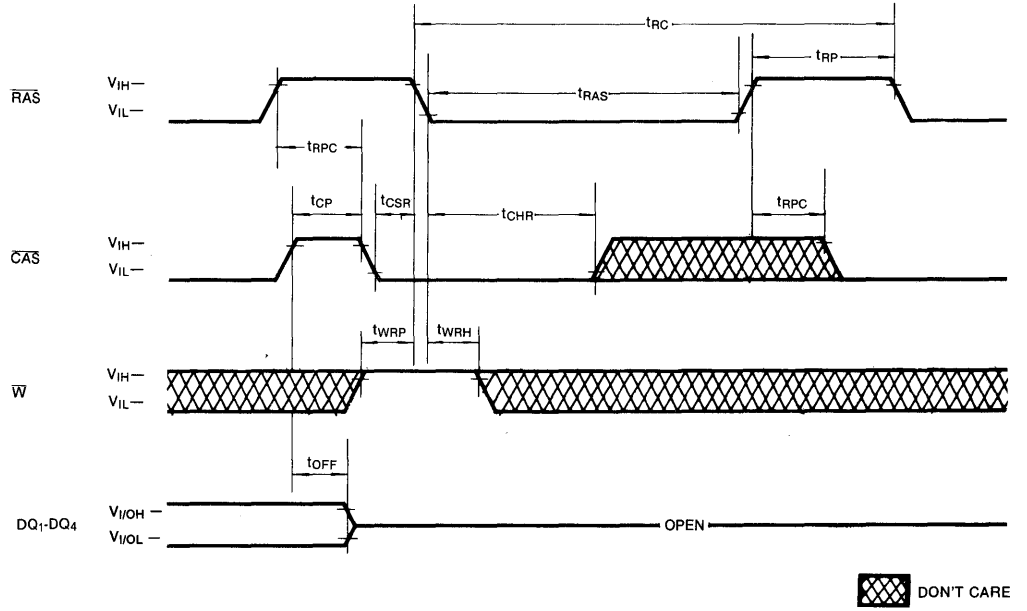
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



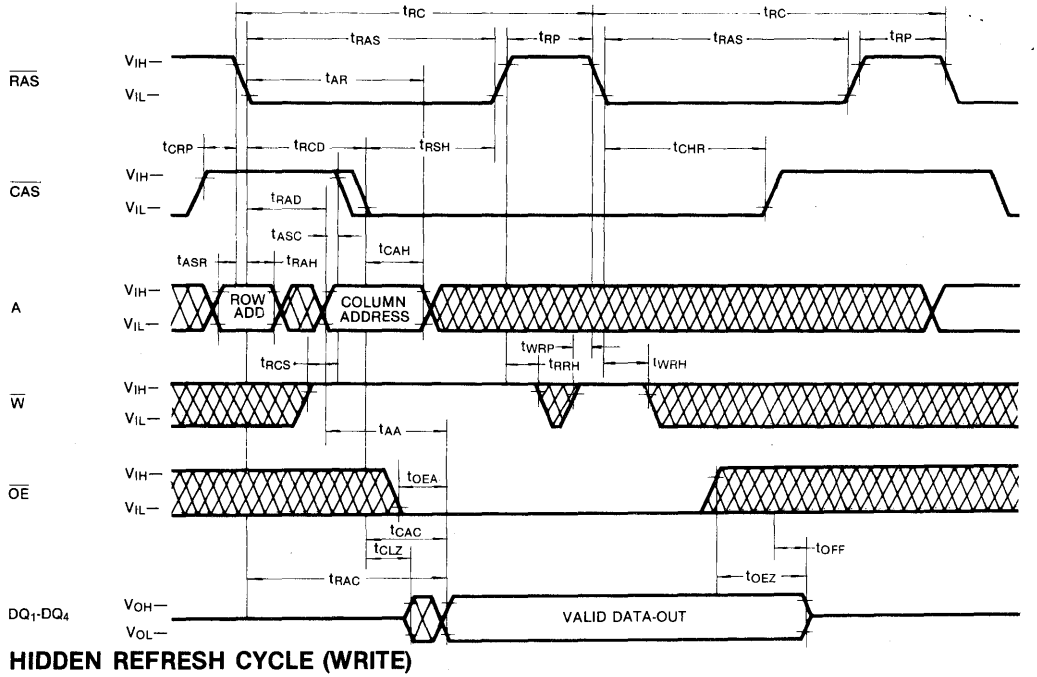
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

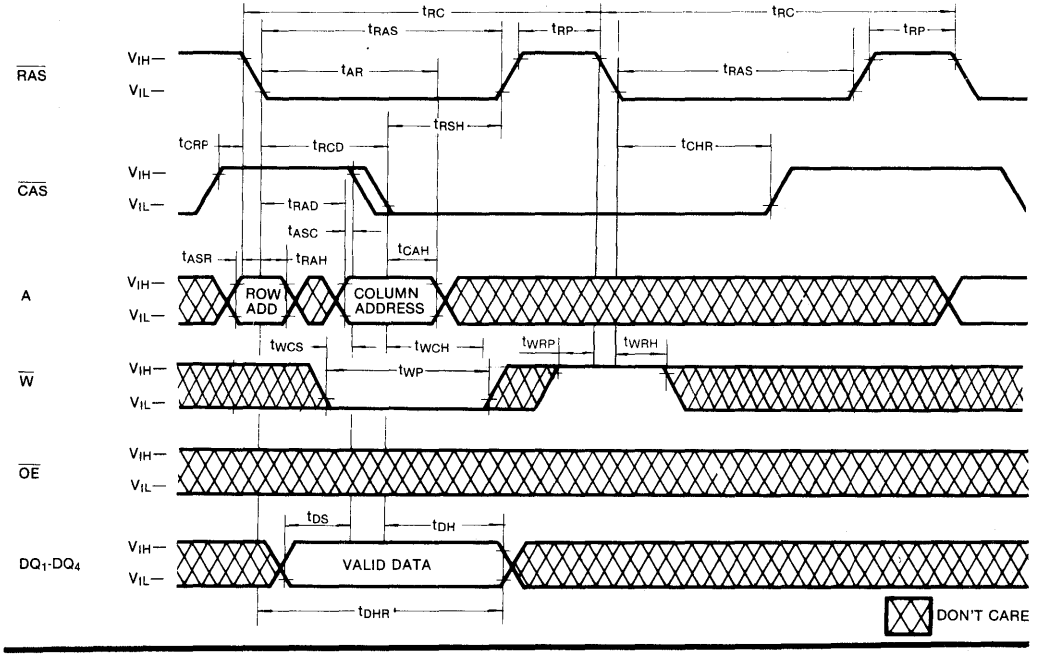


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

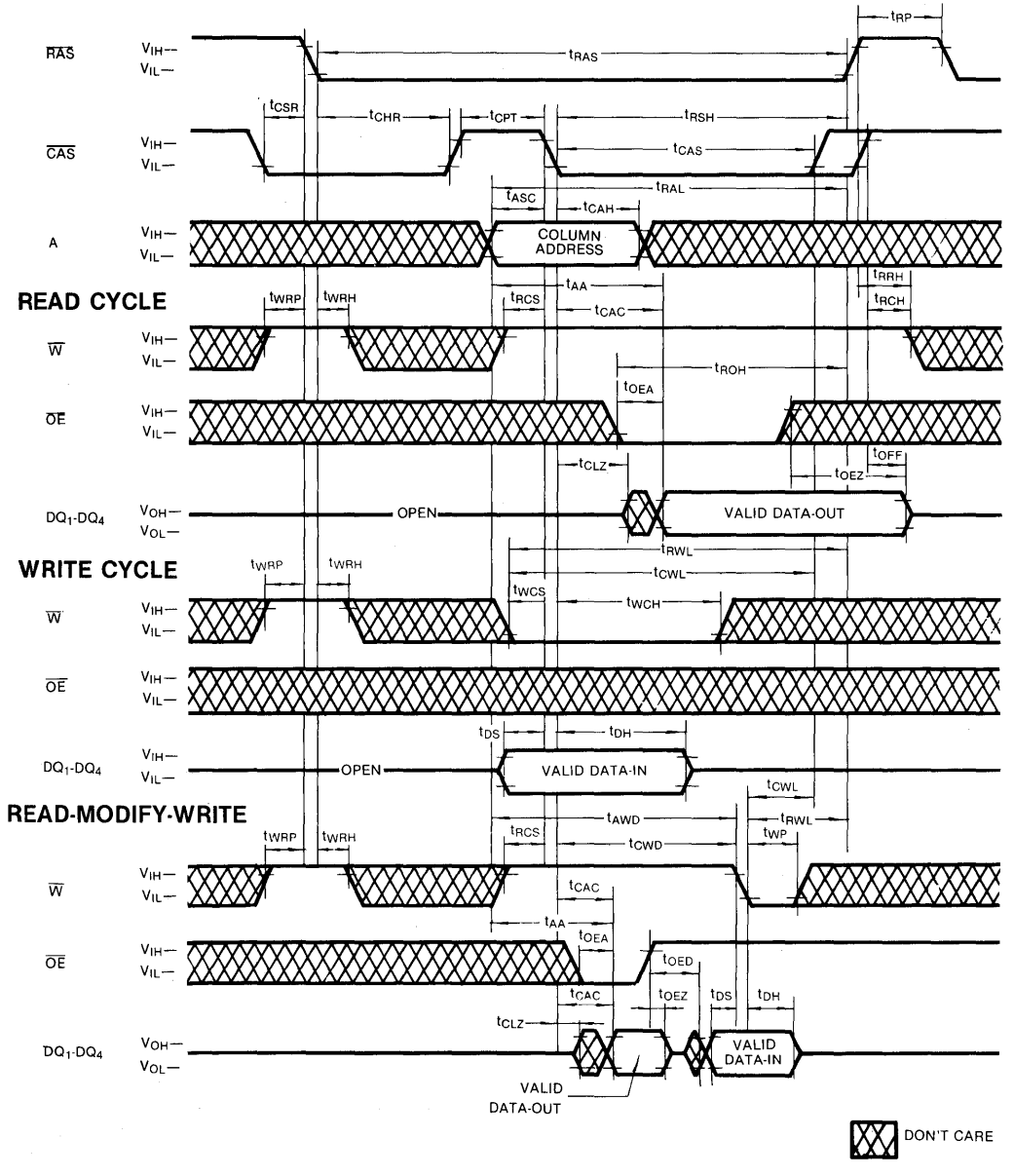


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

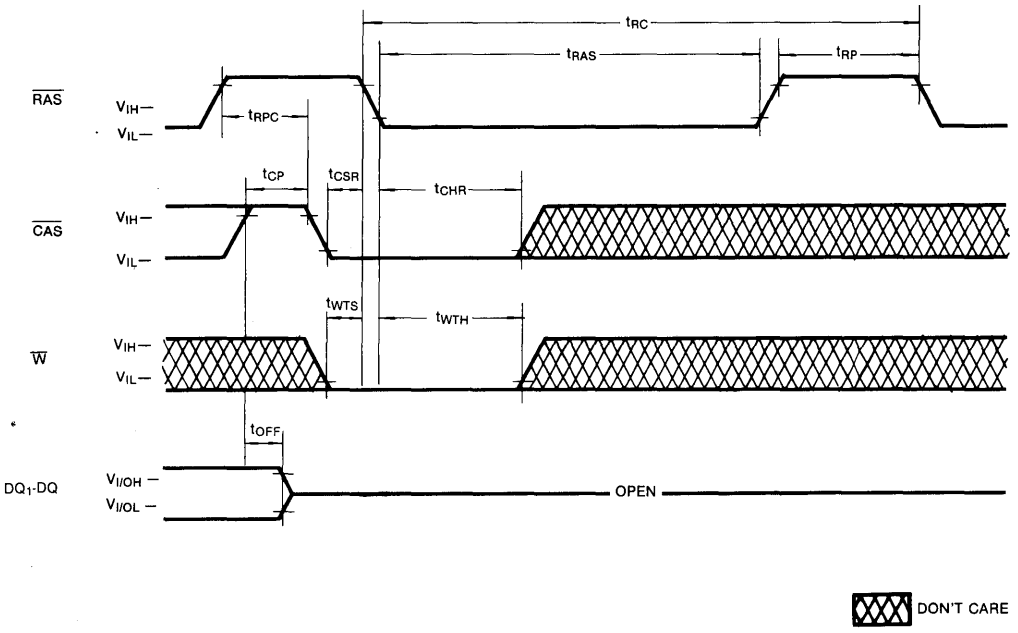
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000AL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000AL contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000AL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000AL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000AL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000AL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000AL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000AL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000AL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000AL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 128 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000AL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000AL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000AL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000AL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

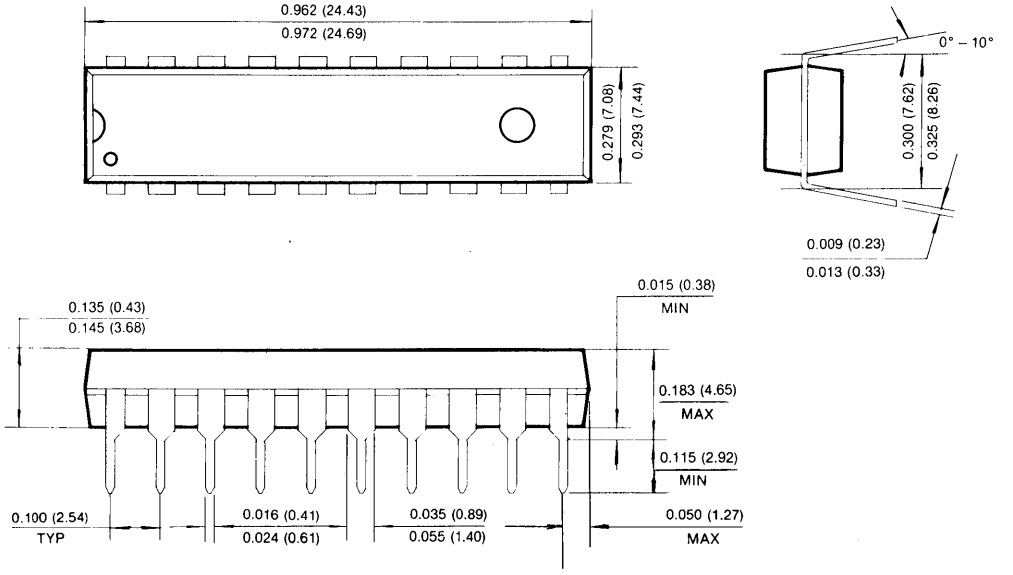
Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000AL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

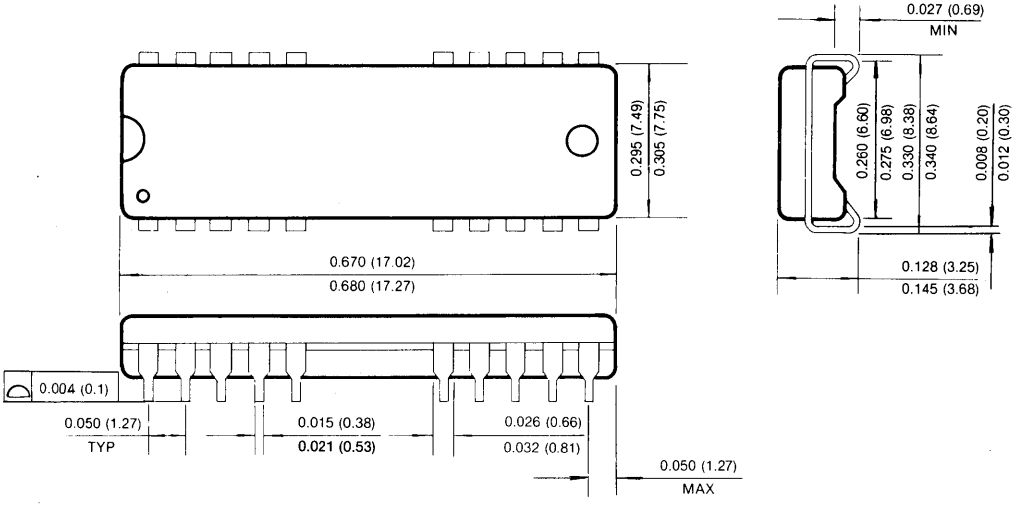
An initial pause of 200μs is required after power-up flowed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



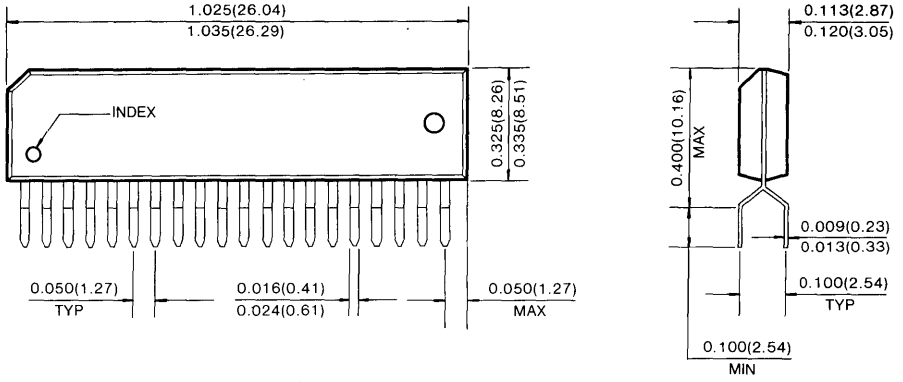
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



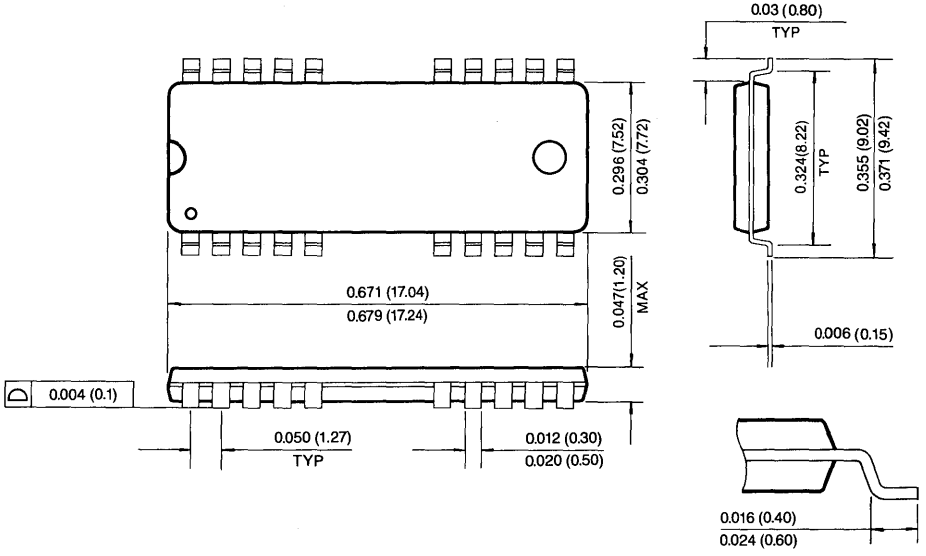
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000ASL- 7	70ns	20ns	130ns
KM44C1000ASL- 8	80ns	20ns	150ns
KM44C1000ASL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/256ms refresh**
- **Low power dissipation**
  - **—Standby: 0.6mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP, and TSOP (II)**

GENERAL DESCRIPTION

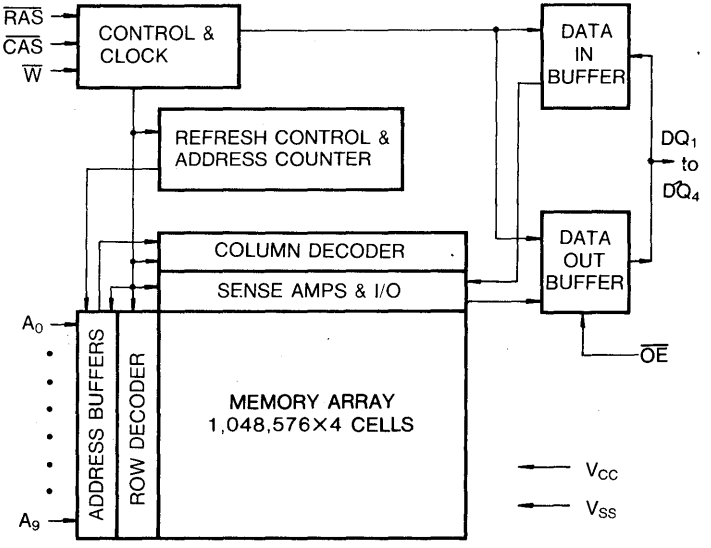
The Samsung KM44C1000ASL is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

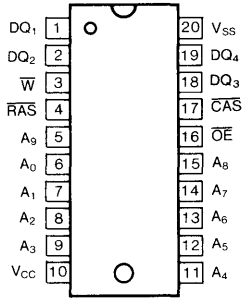
The KM44C1000ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



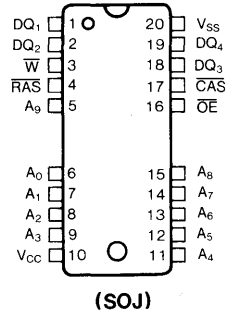
PIN CONFIGURATION (Top Views)

• KM44C1000ASLP



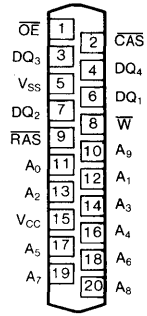
(DIP)

• KM44C1000ASLJ



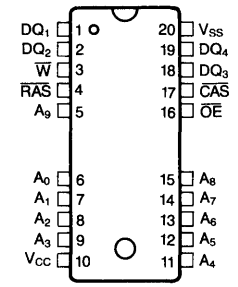
(SOJ)

• KM44C1000ASLZ



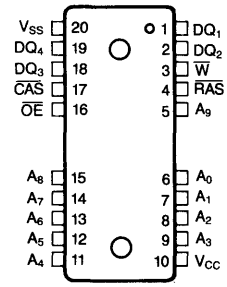
(ZIP)

• KM44C1000ASLT



(TSOP(II)-Forward Type)

• KM44C1000ASLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000ASL- 7	I_{CC1}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000ASL- 7	I_{CC3}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000ASL- 7	I_{CC4}	—	80	mA
	KM44C1000ASL- 8		—	70	mA
	KM44C1000ASL-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}−0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000ASL- 7	I_{CC6}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Battery Back Up CurrentAverage Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care T_{RC}=250μS, T_{RAS}=t_{RAS} min.~1μS		I_{CC7}	—	150	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page mode read-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

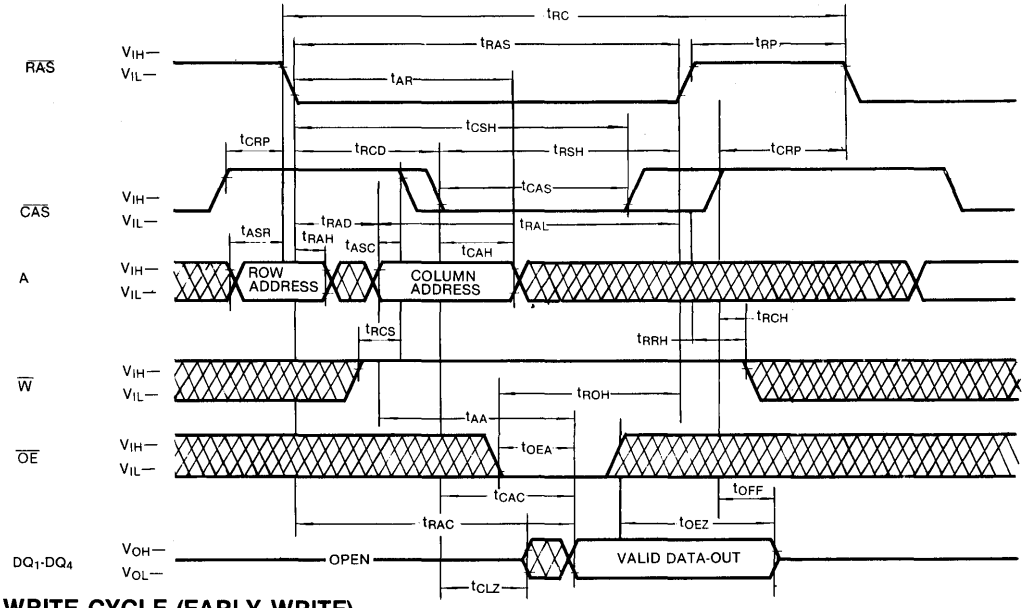
Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

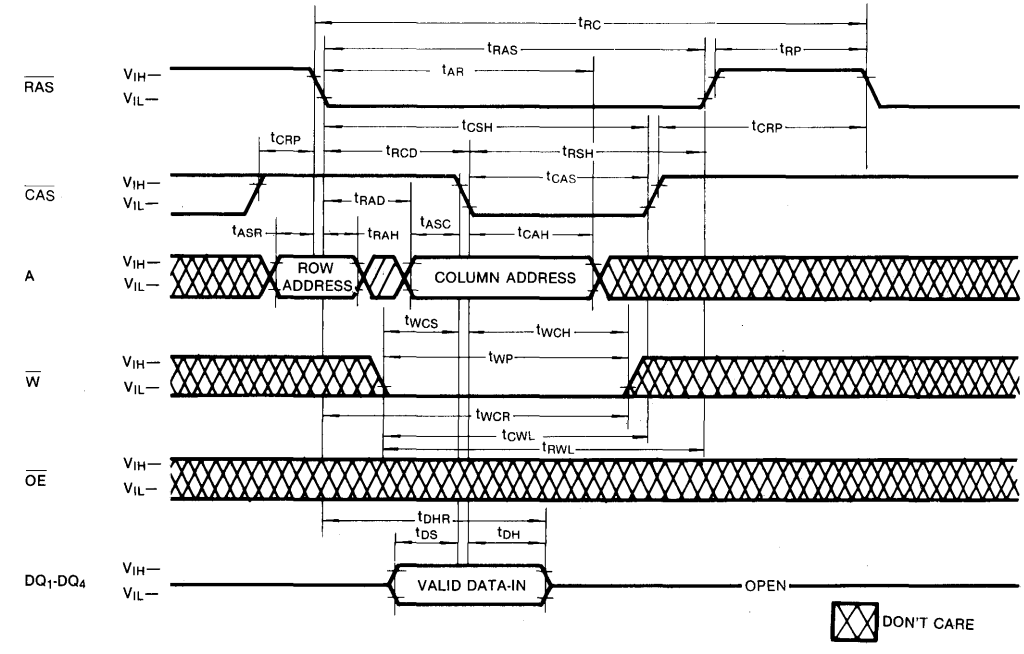
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

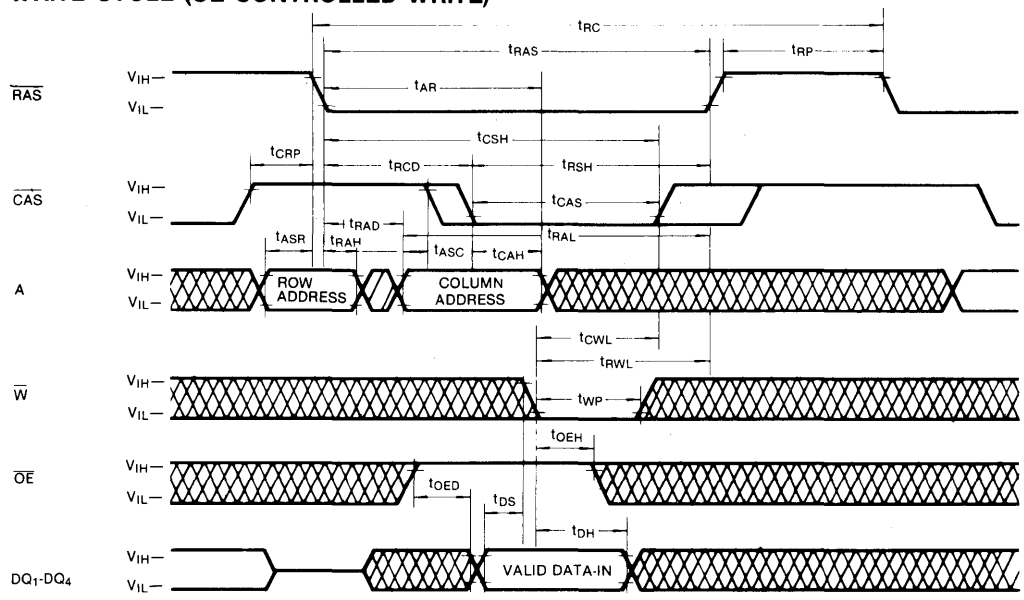


WRITE CYCLE (EARLY WRITE)

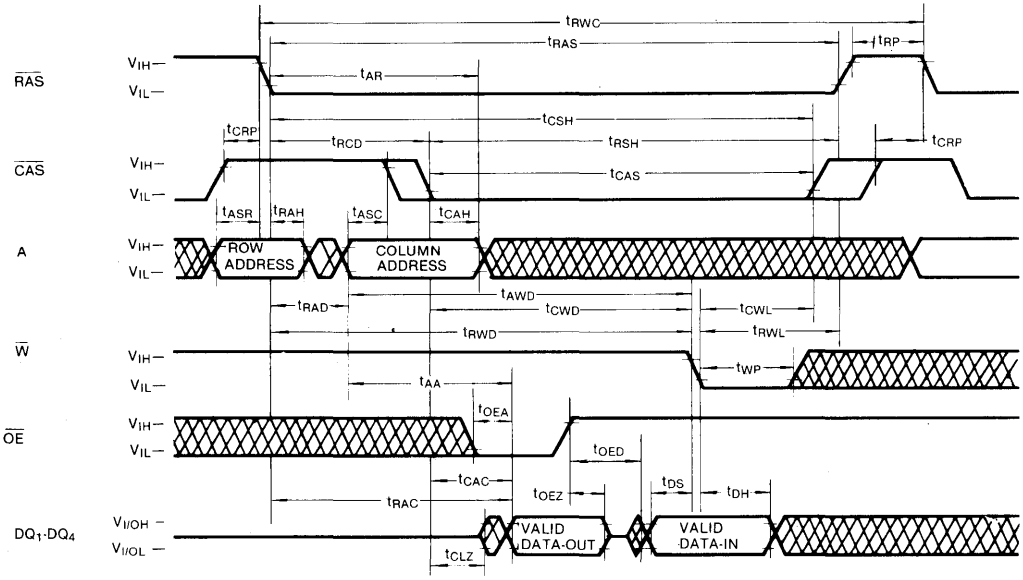


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



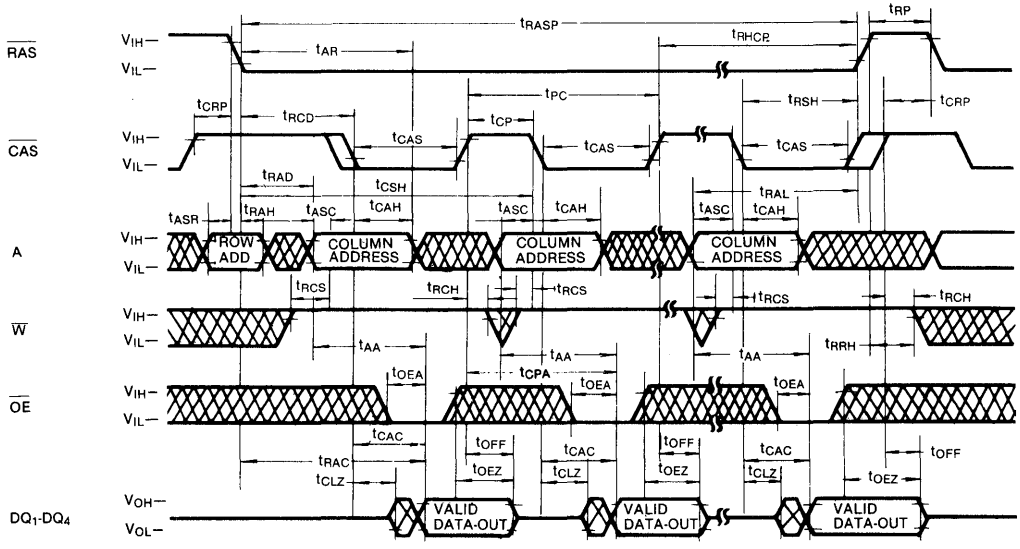
READ-MODIFY-WRITE CYCLE



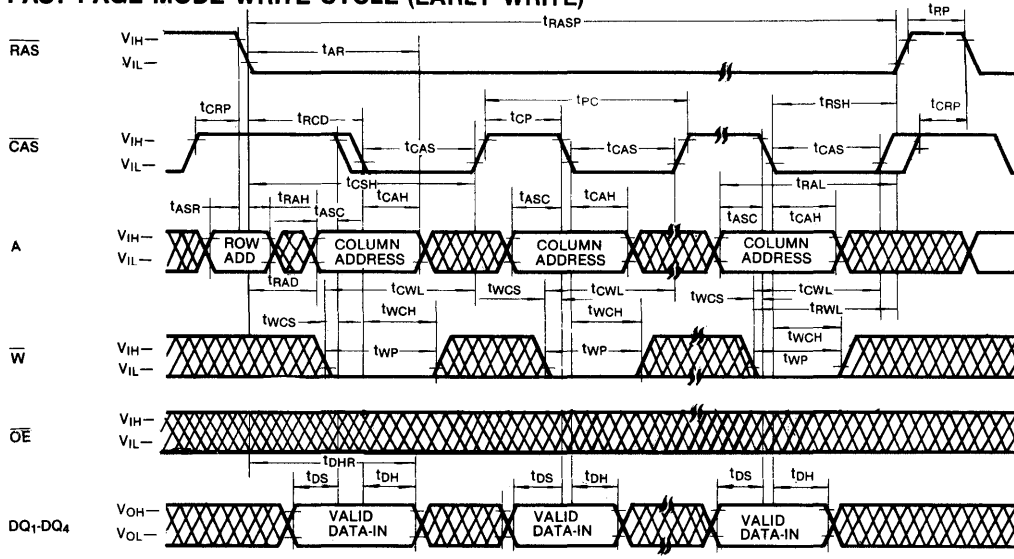
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



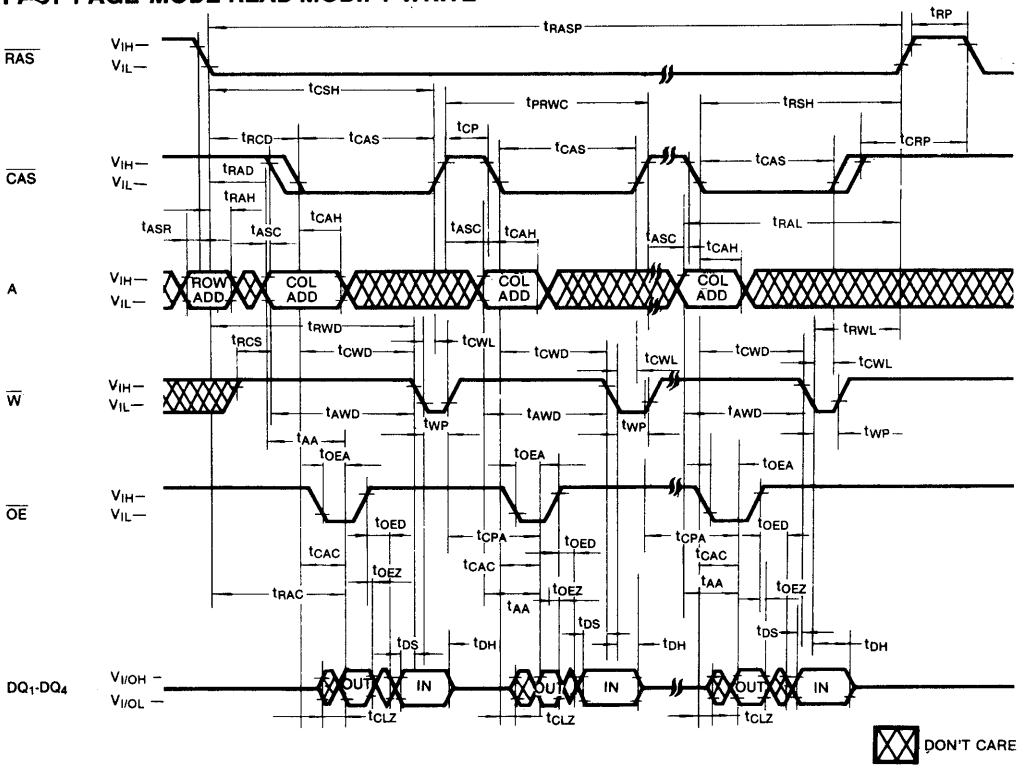
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

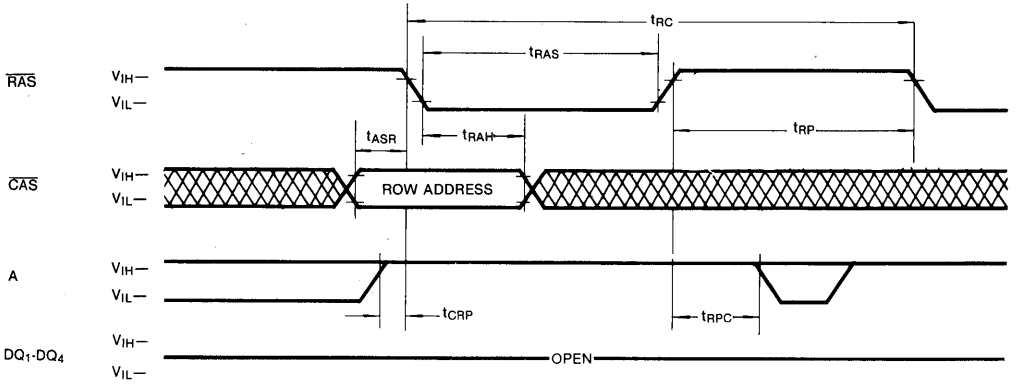
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

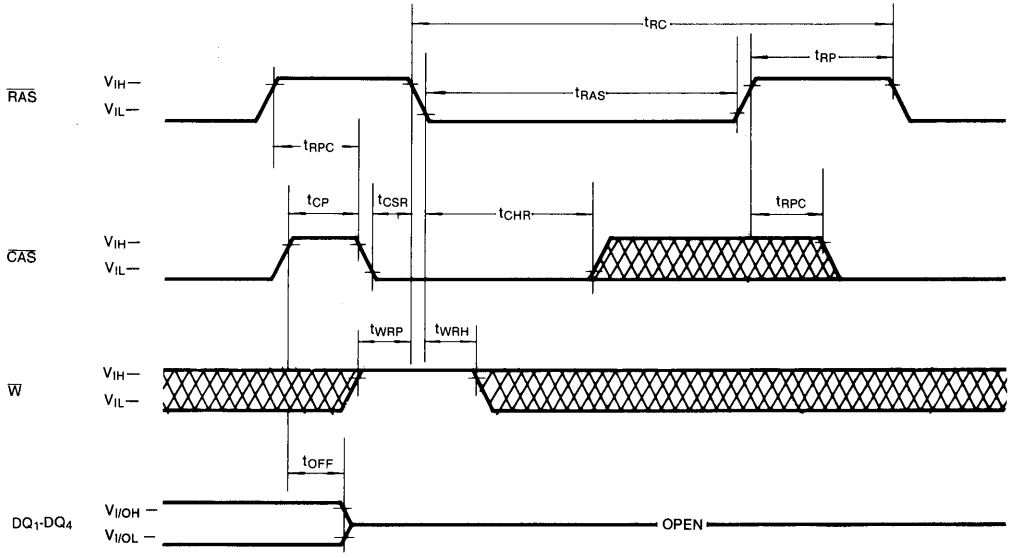
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



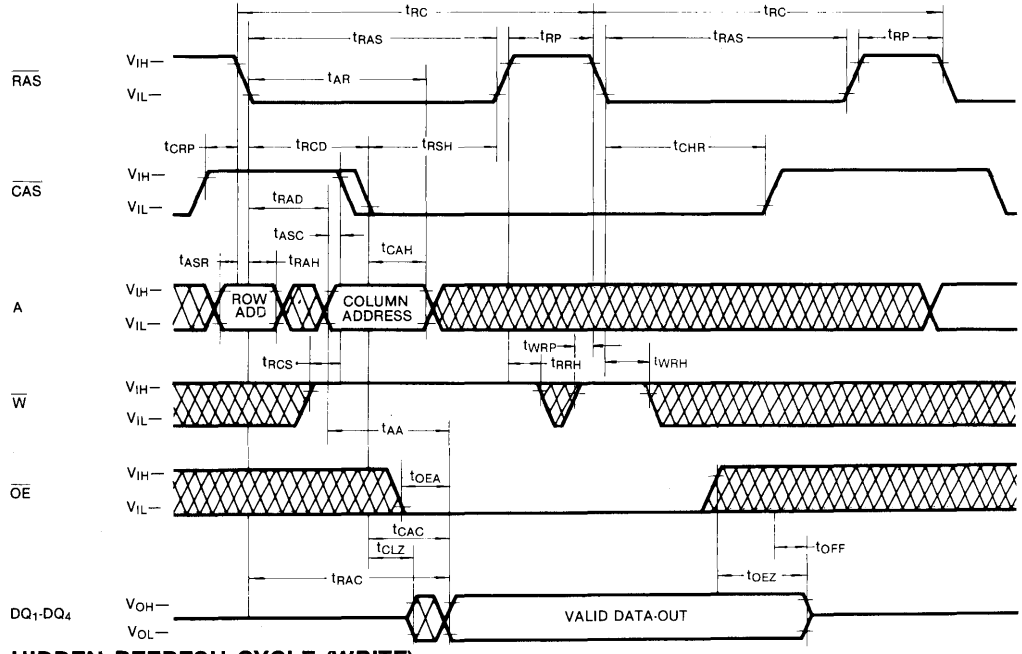
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

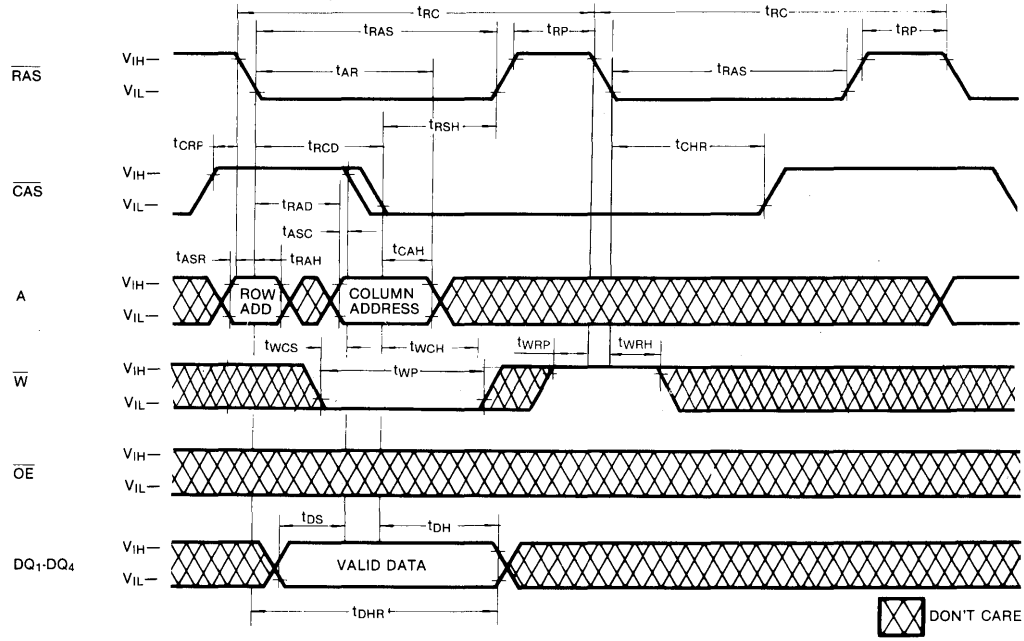


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

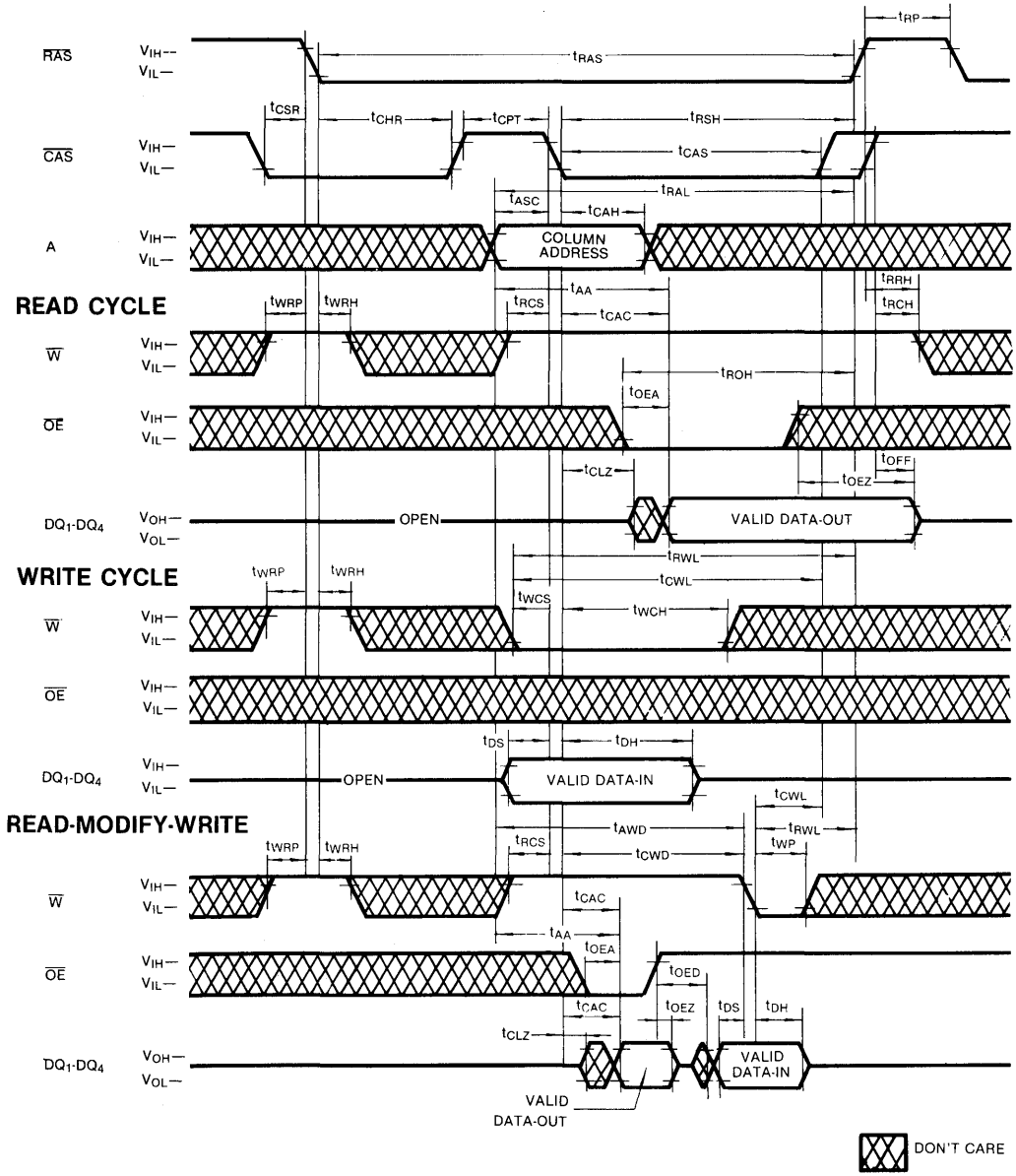


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

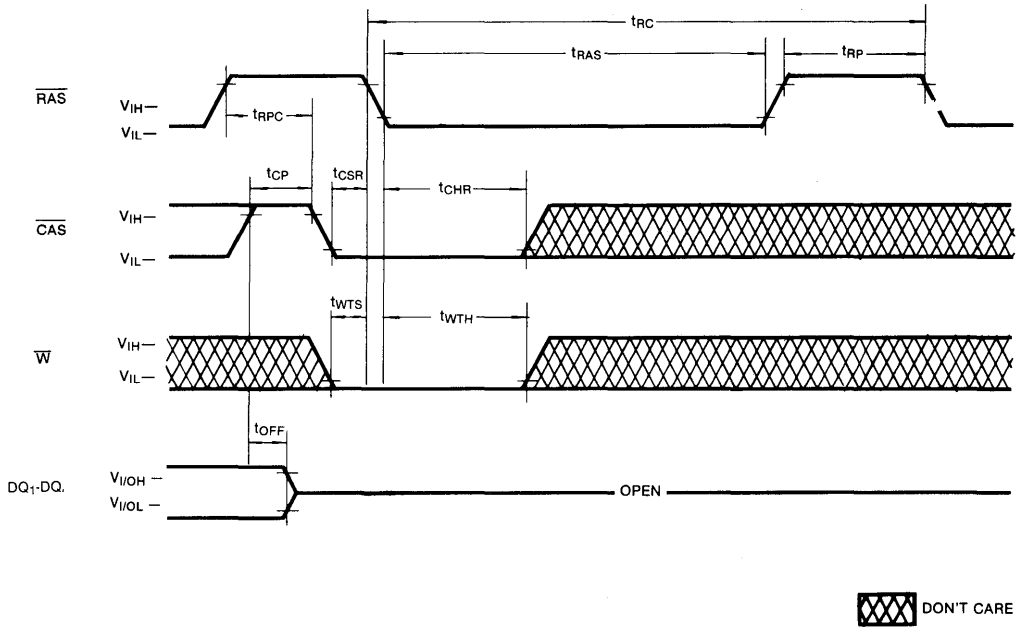
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000ASL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000ASL contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000ASL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000ASL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000ASL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000ASL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000ASL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000ASL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000ASL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000ASL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000ASL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000ASL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000ASL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000ASL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

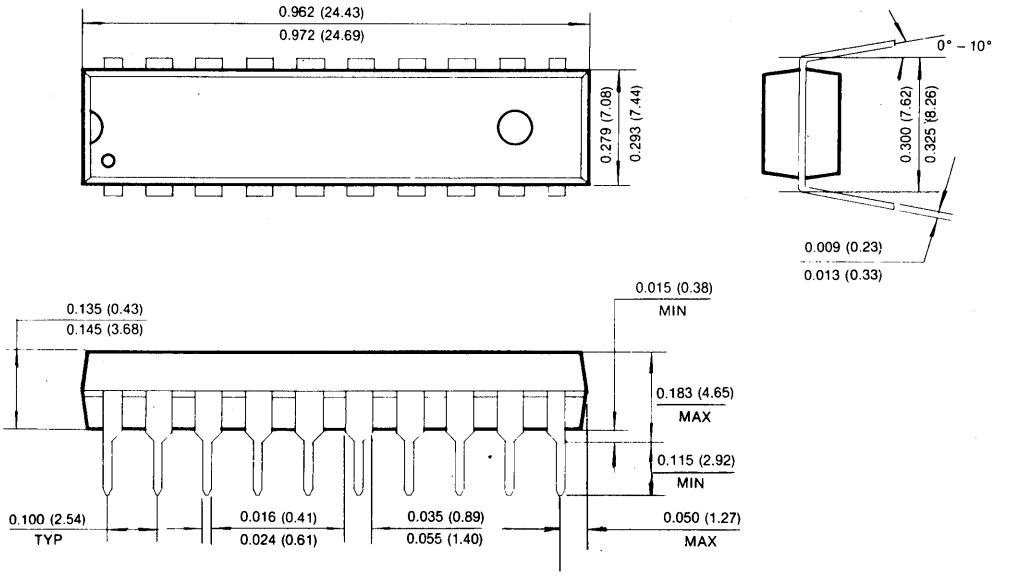
Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000ASL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

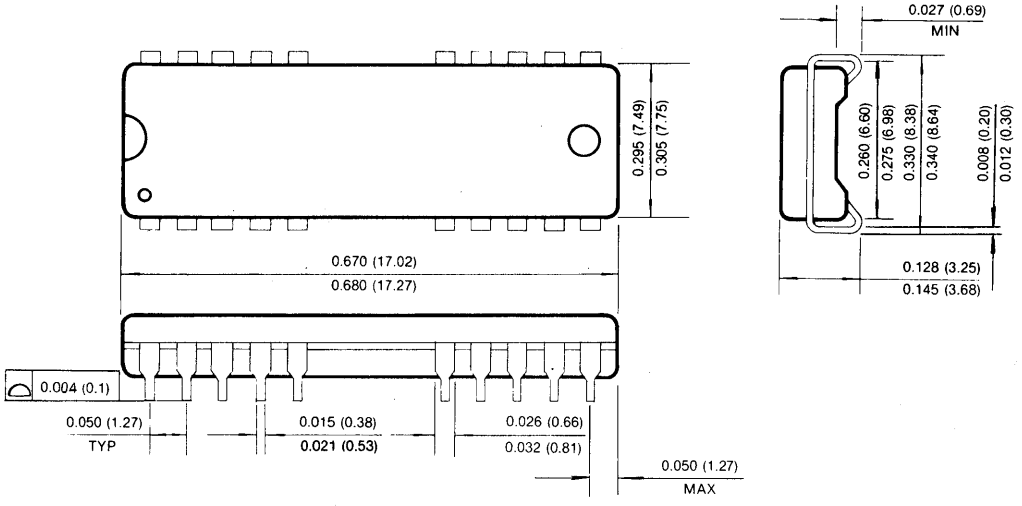
An initial pause of 200μs is required after power-up followed by 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



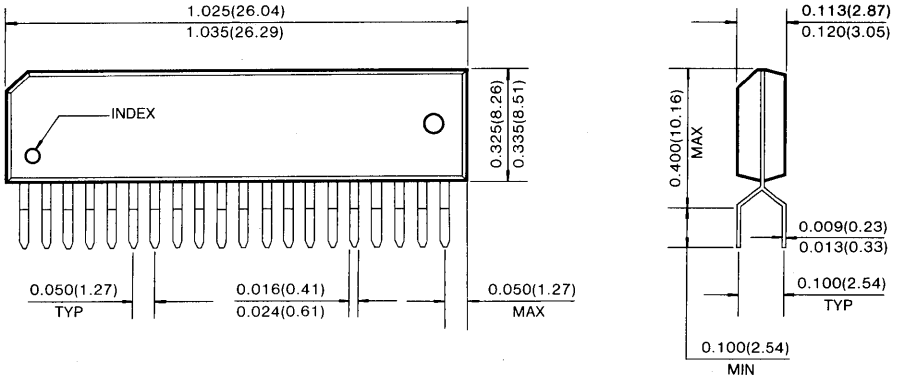
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



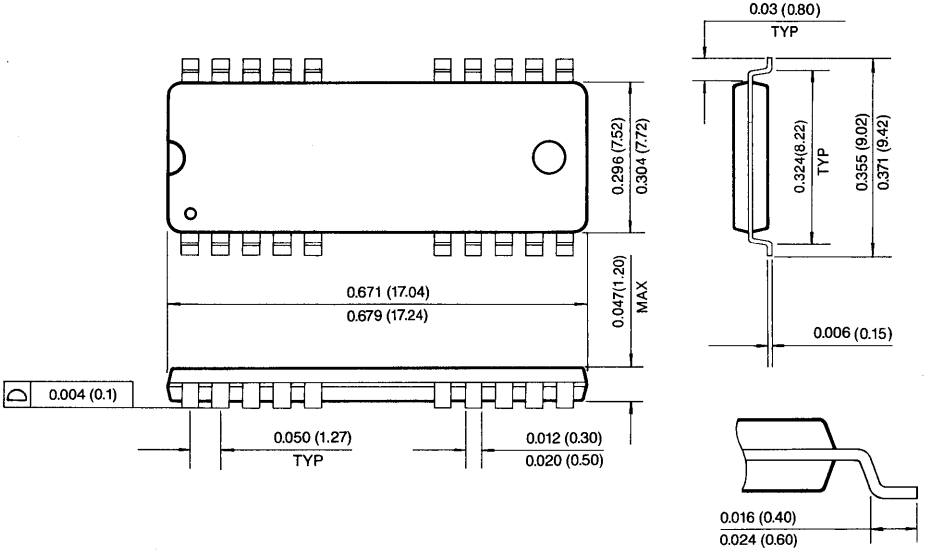
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



1MX4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1002A- 7	70ns	20ns	130ns
KM44C1002A- 8	80ns	20ns	150ns
KM44C1002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

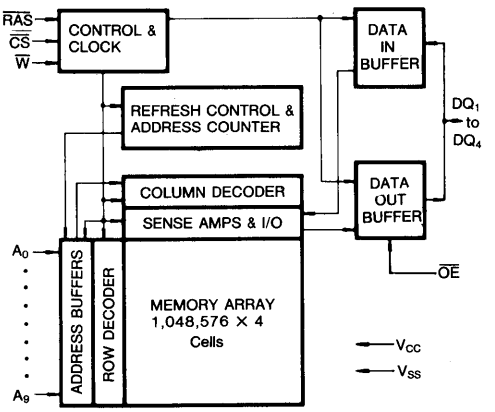
The Samsung KM44C1002A is a high speed CMOS 1,048,576 bit X 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1002A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

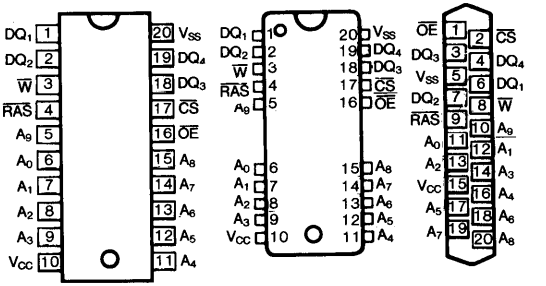
The KM44C1002A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM44C1002AP** - **KM44C1002AJ** - **KM44C1002AZ**



Pin Name	Pin Function
A0-A9	Address Inputs
DQ_1-DQ_4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM44C1002A- 7	I_{CC1}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM44C1002A- 7	I_{CC3}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM44C1002A- 7	I_{CC4}	—	80	mA
	KM44C1002A- 8		—	70	mA
	KM44C1002A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM44C1002A- 7	I_{CC6}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	100		110		135		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 13)

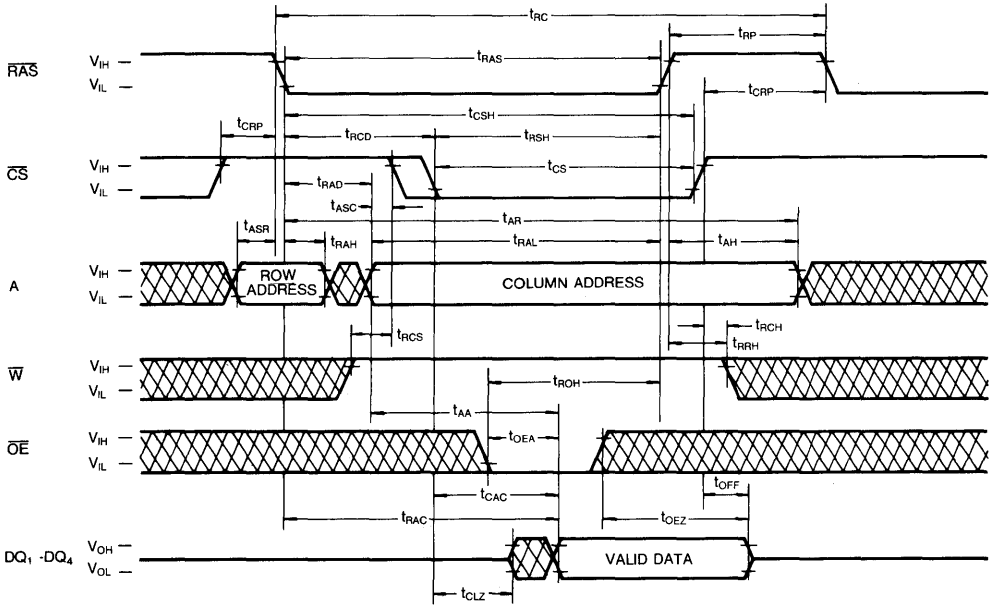
Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	185		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	105		115		135		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

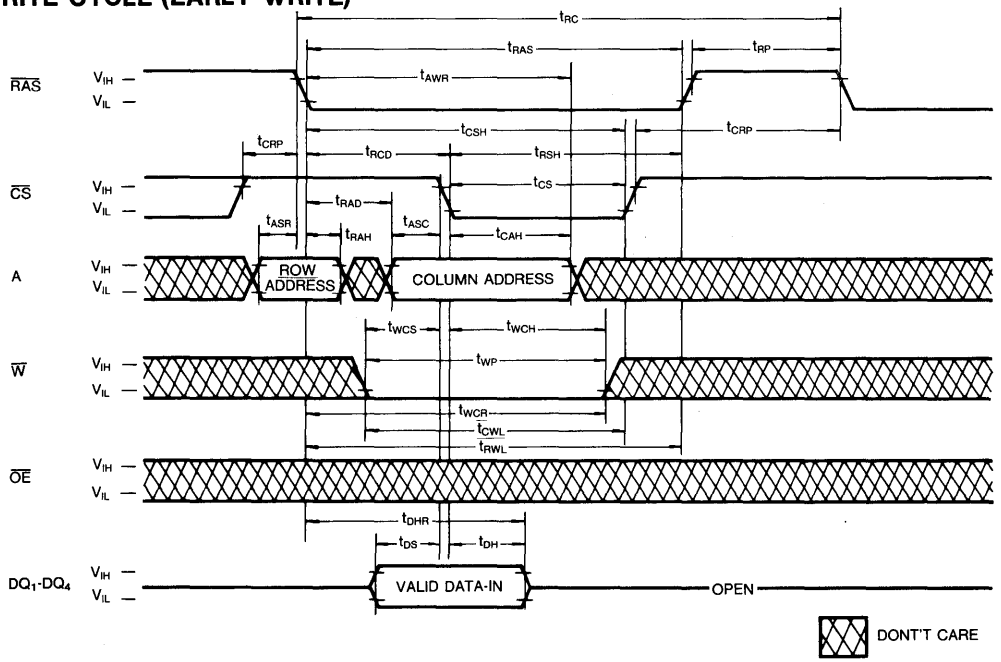
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

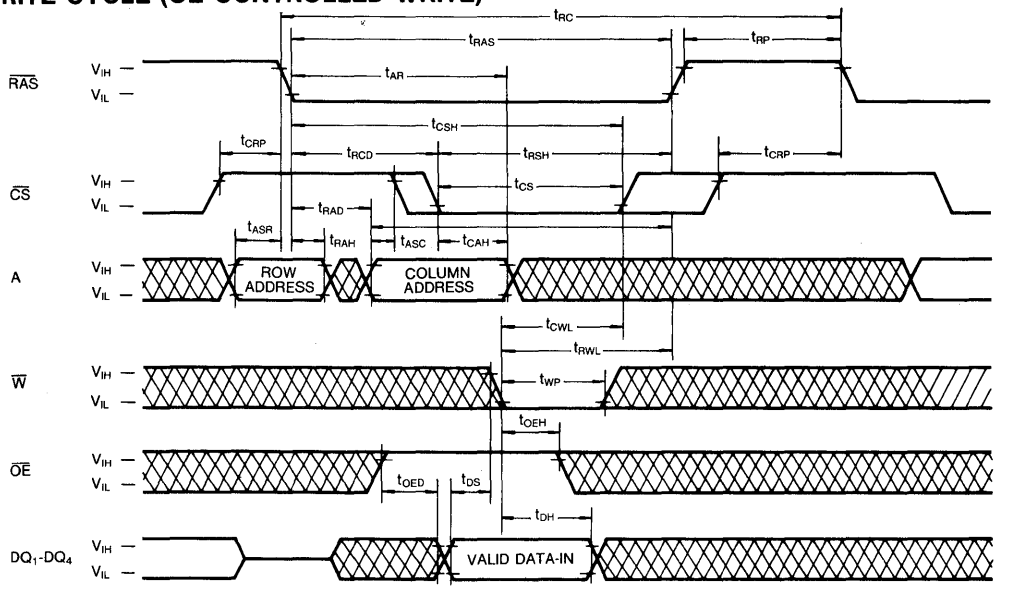


WRITE CYCLE (EARLY WRITE)

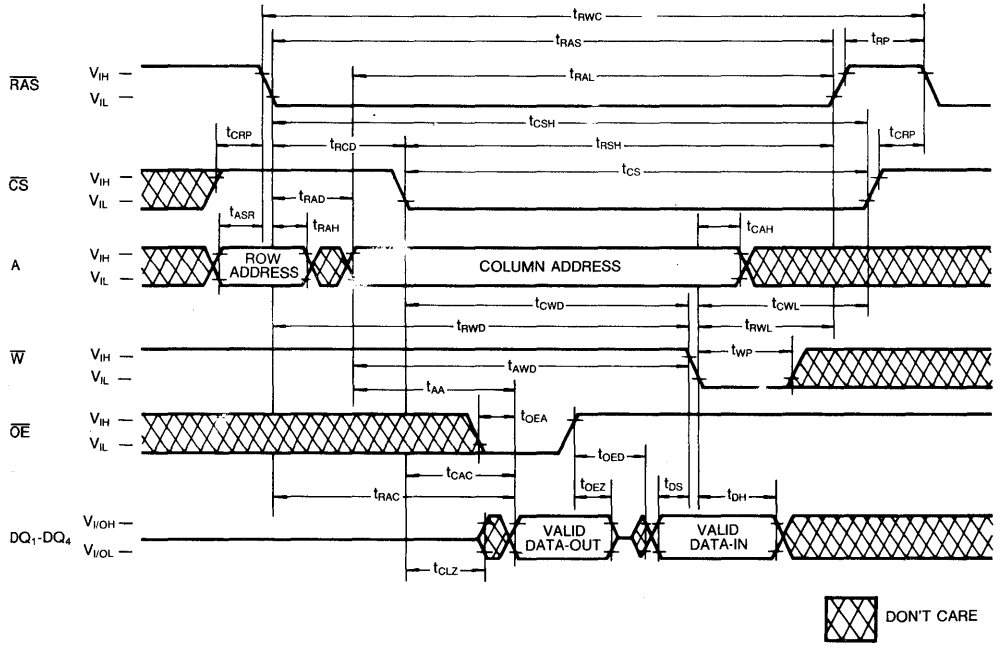


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

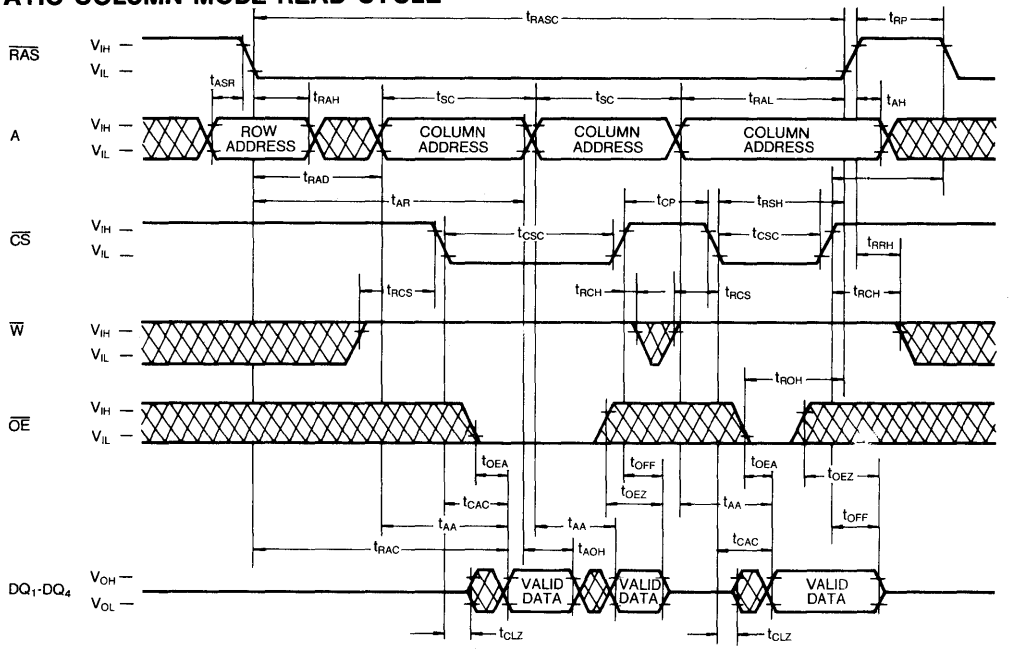


READ-WRITE/READ-MODIFY-WRITE CYCLE

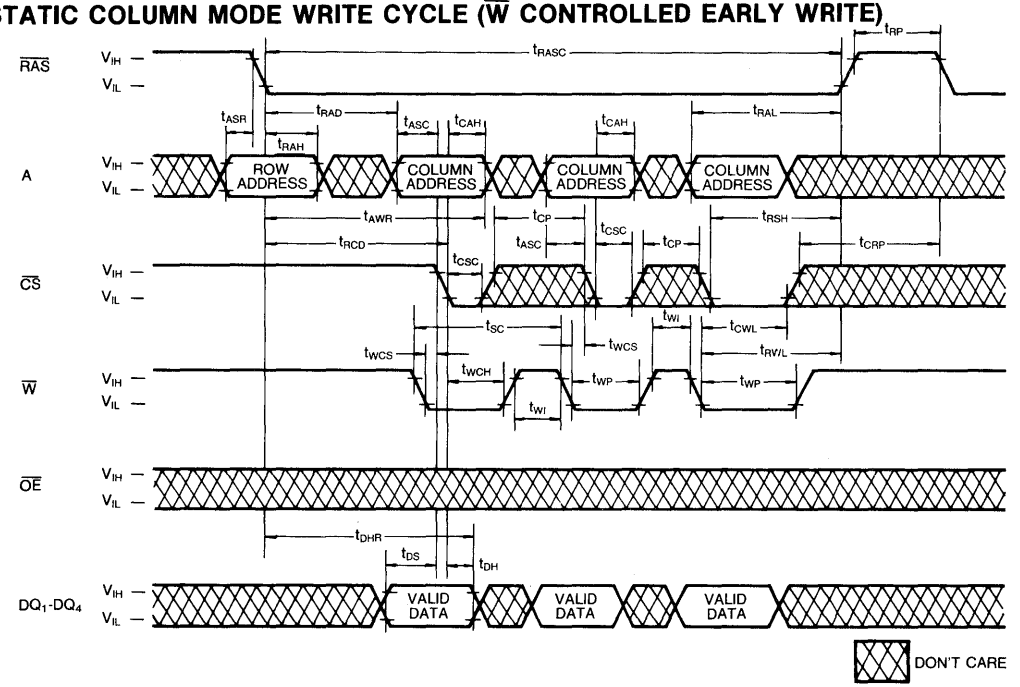


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

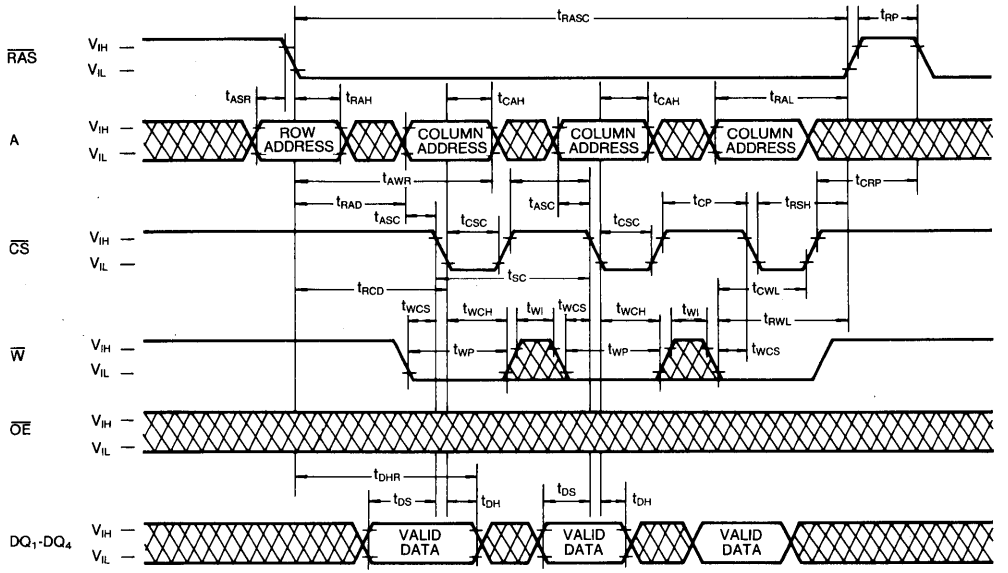


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)

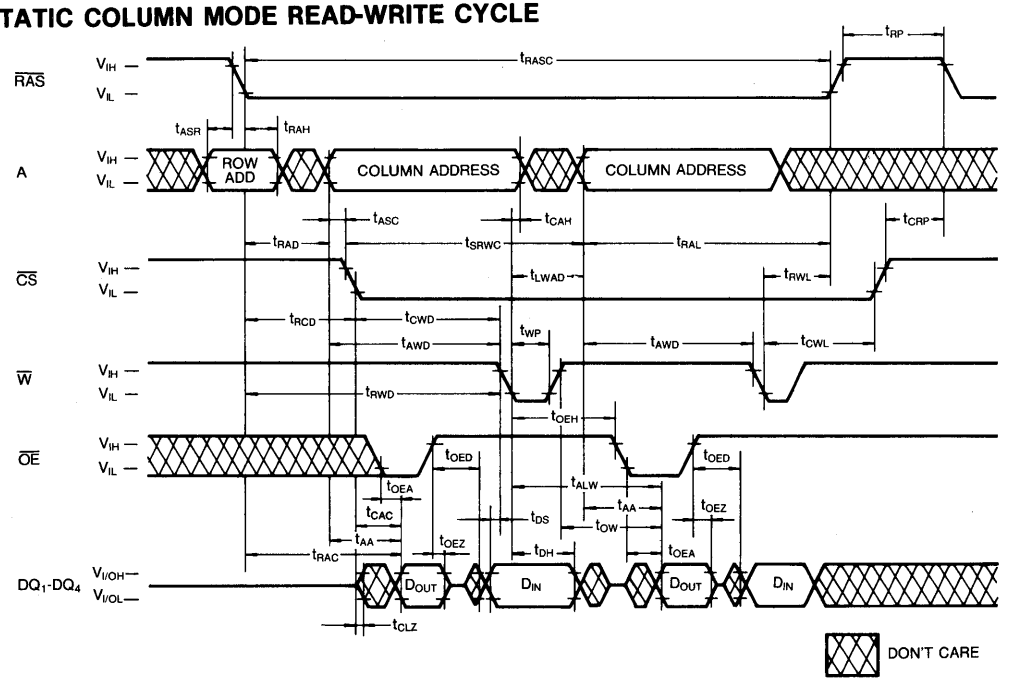


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)

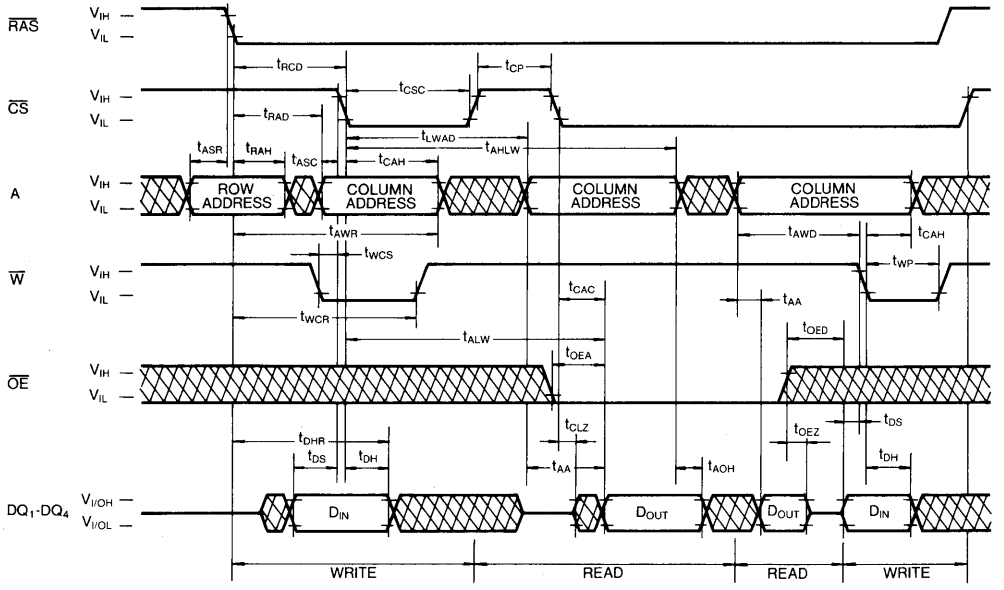


STATIC COLUMN MODE READ-WRITE CYCLE



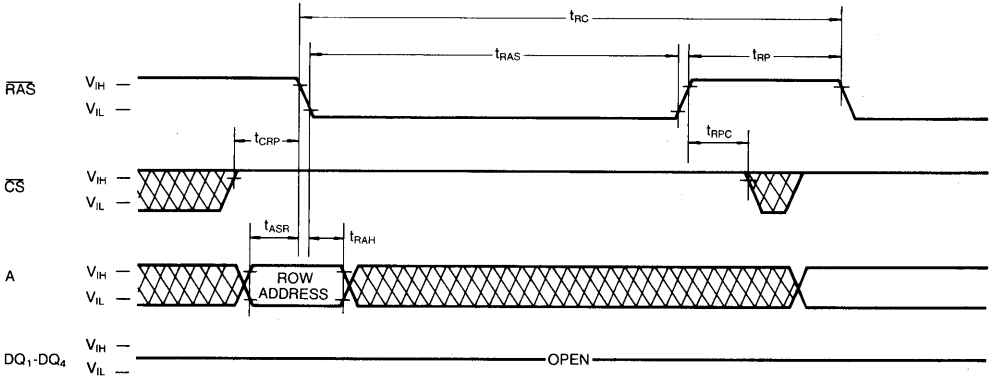
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



RAS-ONLY REFRESH CYCLE

NOTE: W, OE==Don't Care

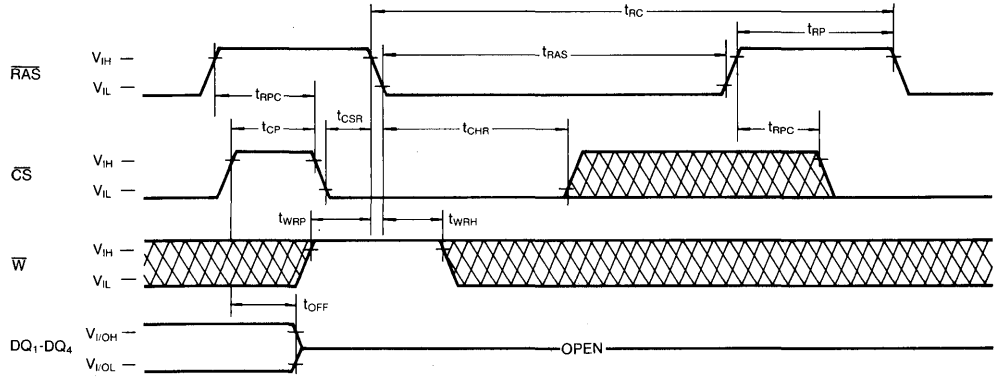


DON'T CARE

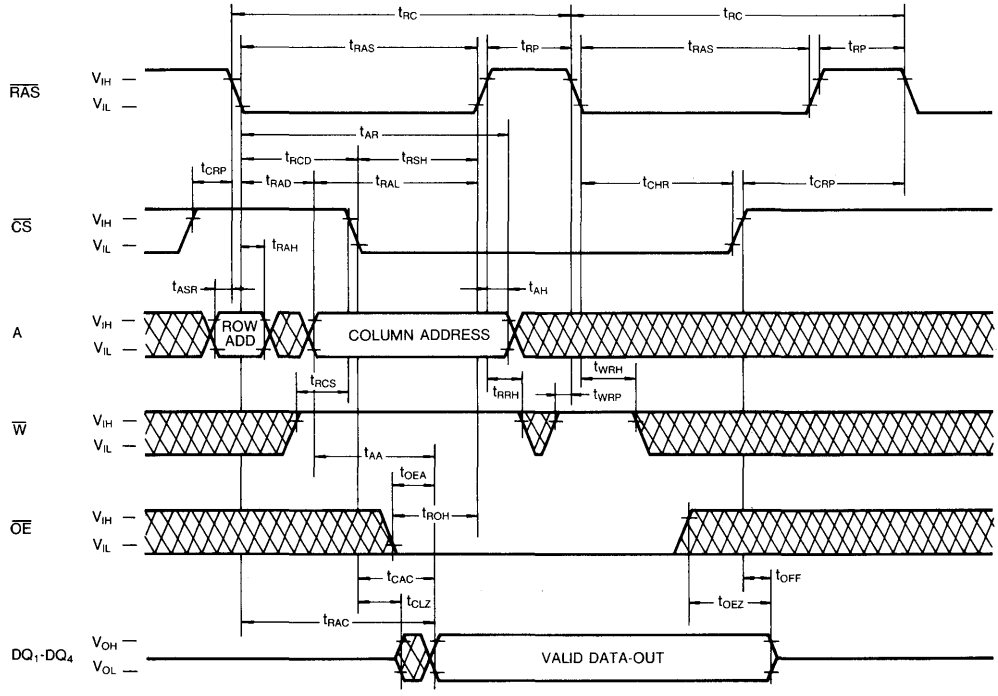
TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, A=Don't Care

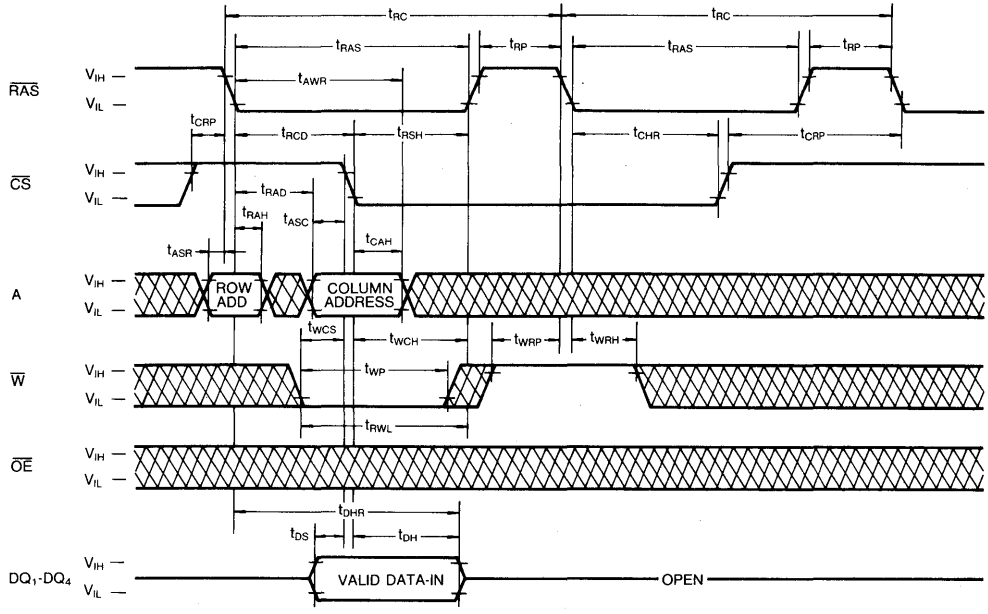


HIDDEN REFRESH CYCLE (READ)



TIMING DIAGRAMS (Continued)

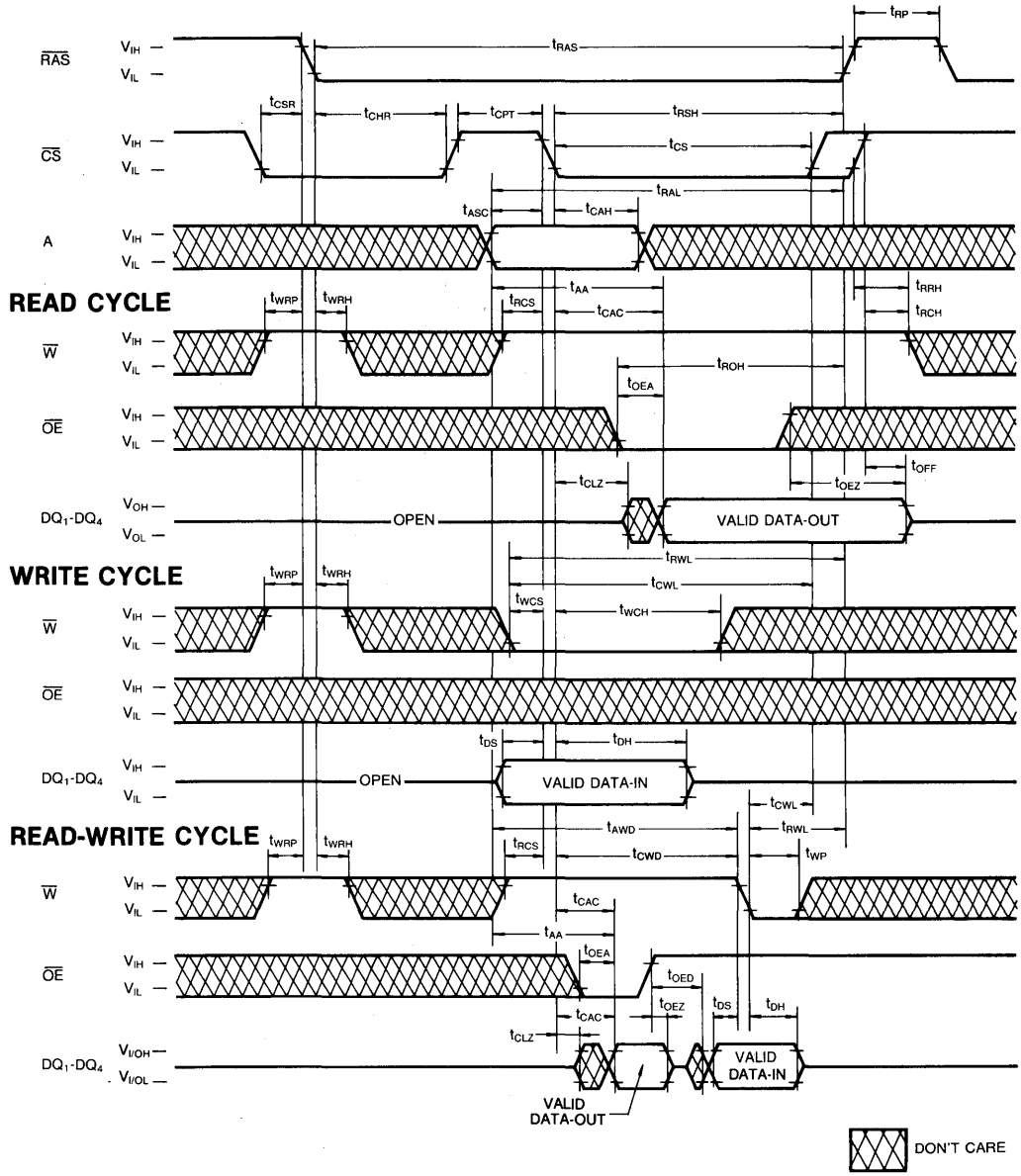
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

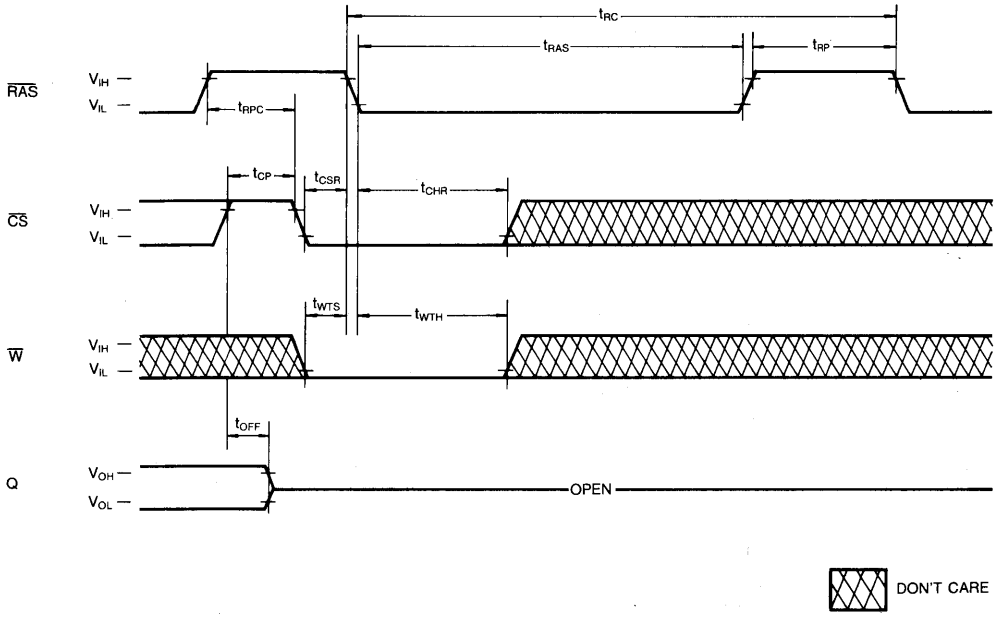
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM44C1002A contains 4,194,304 memory locations organized as 1,048,576 four-bit words. Twenty address bits are required to address a particular 4-bit word in the memory location. Since the KM44C1002A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM44C1002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C1002A has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been proviced so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1002A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the output. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing equirement prevents bus contention on the KM44C1002A's DQ pins.

Data Output

The KM44C1002A has a three-state output buffer which is controlled by $\overline{CS}$ and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1002A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle. $\overline{OE}$ Controlled write.
Indeterminate Output State: Delayed Write

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM44C1002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

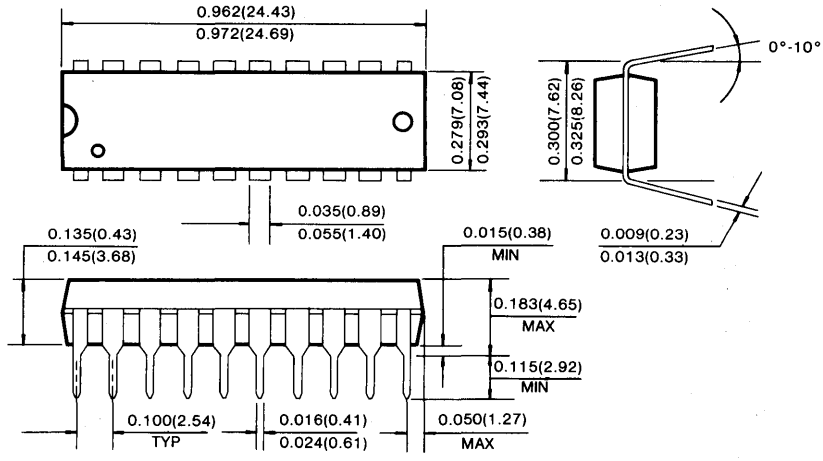
If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycle before proper device operation is achieved.

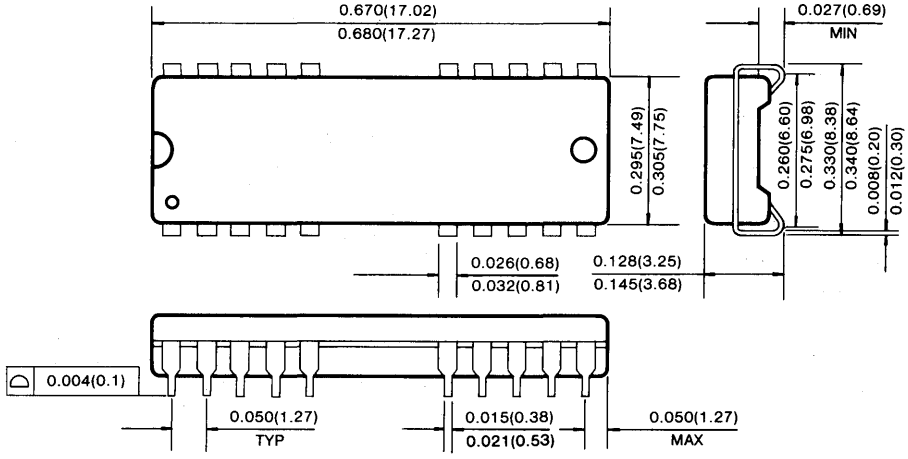
PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



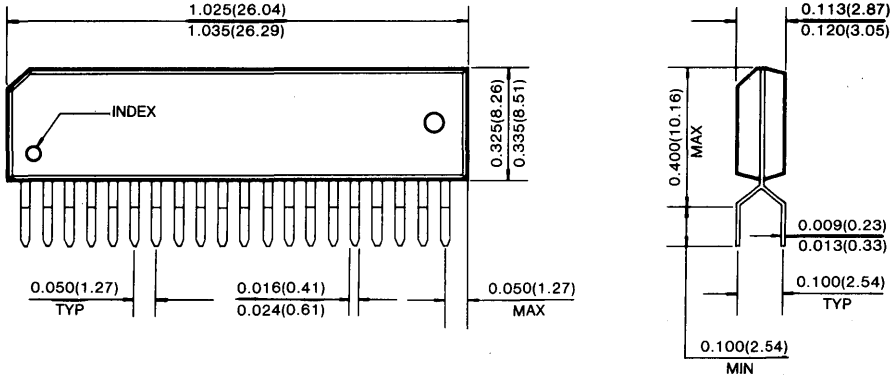
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



2

1M×4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1010A- 7	70ns	20ns	130ns
KM44C1010A- 8	80ns	20ns	150ns
KM44C1010A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Write Per Bit Mode Capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

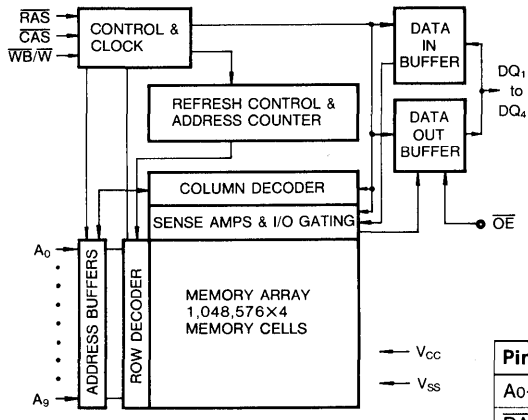
The Samsung KM44C1010A is a high speed CMOS 1,048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1010A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

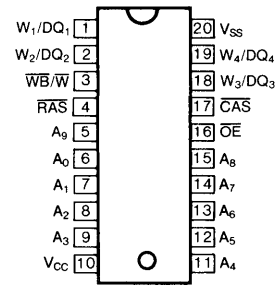
The KM44C1010A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

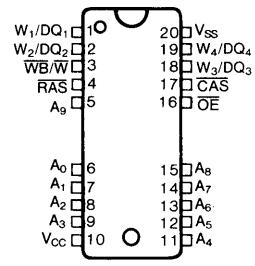


PIN CONFIGURATION (Top Views)

- **KM44C1010AP**

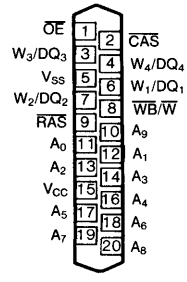


- **KM44C1010AJ**



Pin Name	Pin Function
A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{W}$	Write Per Bit/Read/ Write Input
$\overline{OE}$	Data Output Enable
W_1/DQ_1~ W_4/DQ_4	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground

- **KM44C1010AZ**



1MX4 Bit CMOS Dynamic RAM with Static Column Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1012A- 7	70ns	20ns	130ns
KM44C1012A- 8	80ns	20ns	150ns
KM44C1012A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **Write Per Bit Mode Capability**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

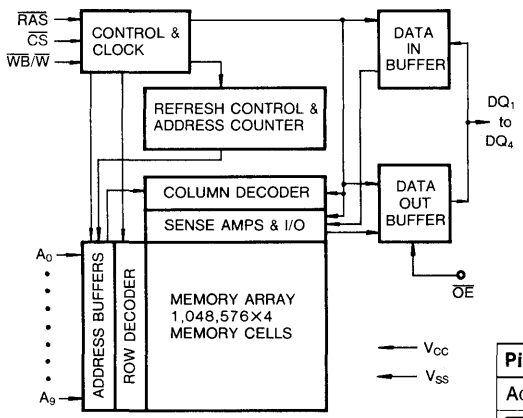
The Samsung KM44C1012A is a high speed CMOS 1,048,576×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

Static Column Mode Operation allows high speed random or sequential access within a row. The KM44C1012A offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

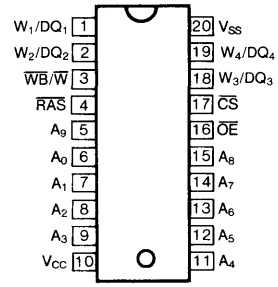
The KM44C1012A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

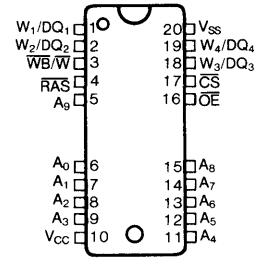


PIN CONFIGURATION (Top Views)

• KM44C1012AP

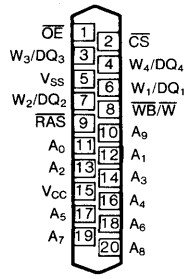


• KM44C1012AJ



Pin Name	Pin Function
A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{WB}/\overline{W}$	Write Per Bit/Read/ Write Input
$\overline{OE}$	Data Output Enable
W_1/DQ_1~ W_4/DQ_4	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground

• KM44C1012AZ



256KX16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C256- 7	70ns	20ns	130ns
KM416C256- 8	80ns	20ns	150ns
KM416C256-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

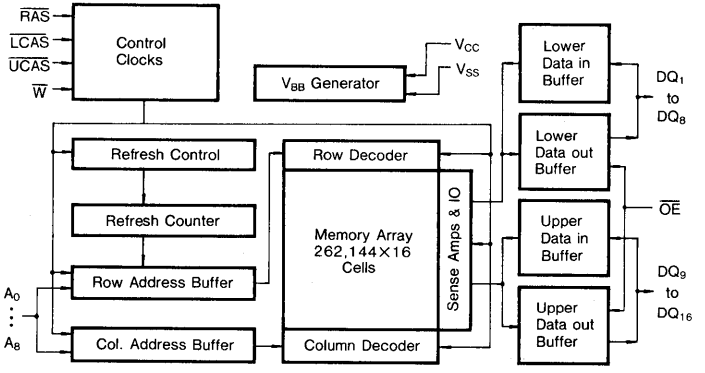
GENERAL DESCRIPTION

The Samsung KM416C256 is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computes.

The KM416C256 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

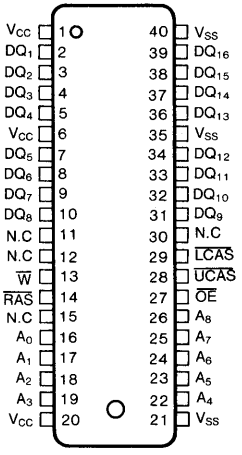
The KM416C256 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM416C256J**



Pin Name	Pin Function
A_0-A_8	Address Inputs
DQ_{1-16}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @ t_{RC}=min)	KM416C256- 7	I_{CC1}	—	145	mA
	KM416C256- 8		—	125	mA
	KM416C256-10		—	105	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM416C256- 7	I_{CC3}	—	145	mA
	KM416C256- 8		—	125	mA
	KM416C256-10		—	105	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @ t_{PC}=min)	KM416C256- 7	I_{CC4}	—	90	mA
	KM416C256- 8		—	80	mA
	KM416C256-10		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$≥V_{CC}-0.2V		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @ t_{RC}=min)	KM416C256- 7	I_{CC6}	—	145	mA
	KM416C256- 8		—	125	mA
	KM416C256-10		—	105	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{UCAS}$ or $\overline{LCAS}$=V_{IL} Dout=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is spedified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{LCAS}$ =V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN3}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM416C256-7		KM416C256-8		KM416C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	10		10		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWI}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

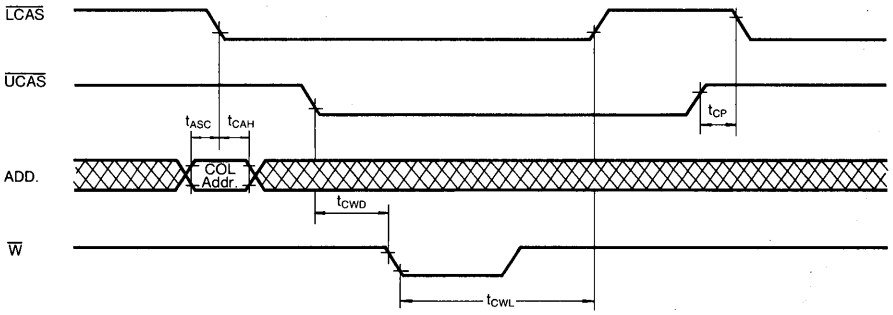
Parameter	Symbol	KM416C256-7		KM416C256-8		KM416C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		120		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM416C256 Truth Table

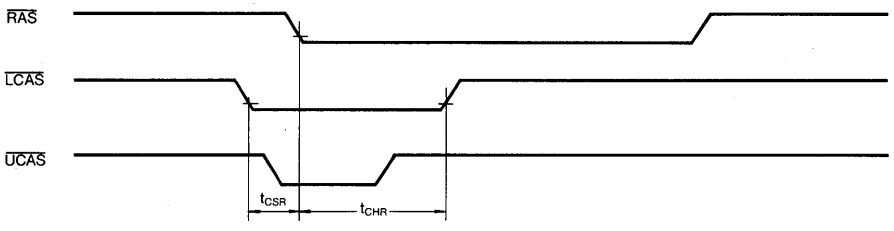
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim8}$	$DQ_{9\sim16}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

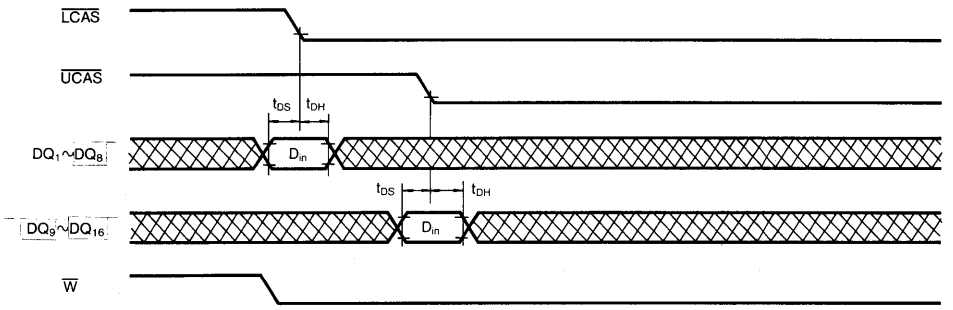
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

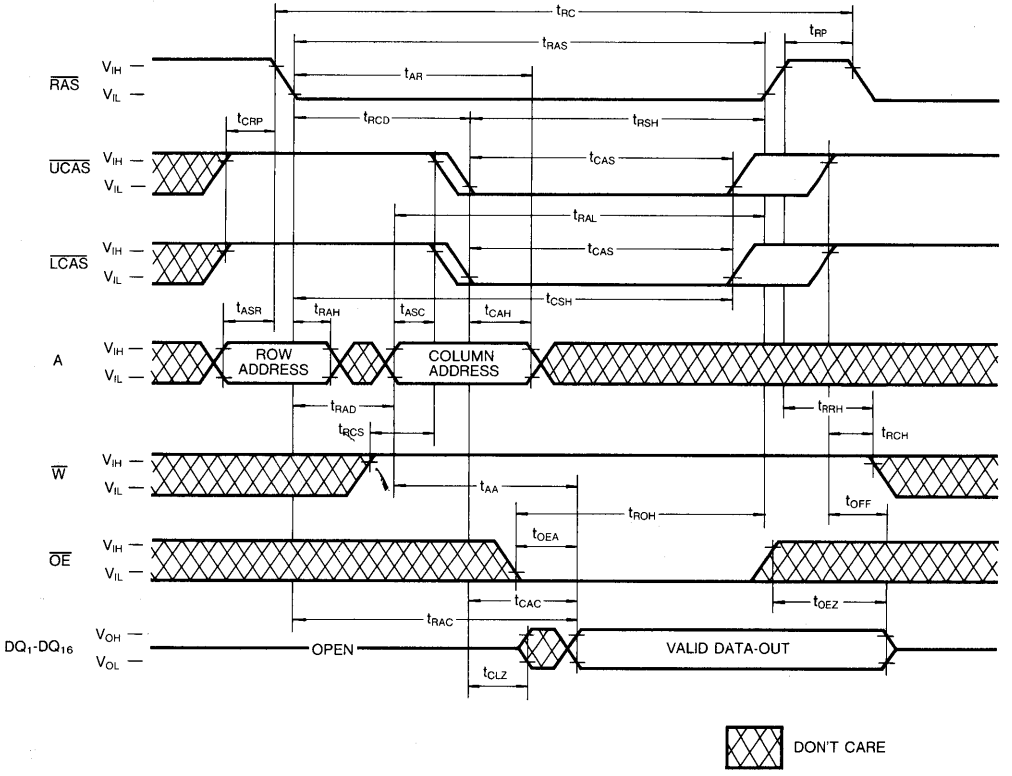


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



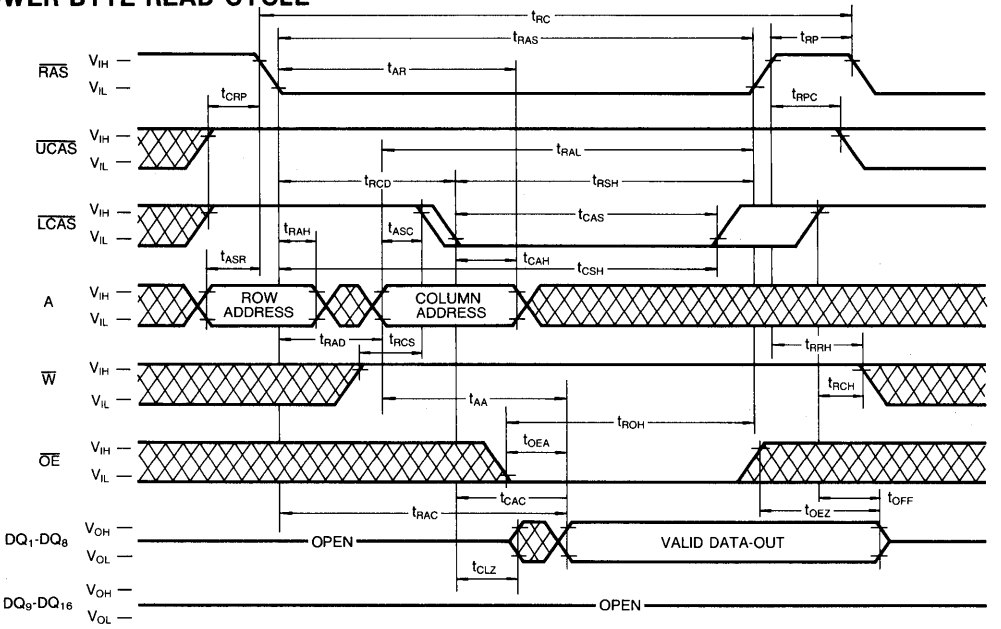
TIMING DIAGRAMS

WORD READ CYCCLE

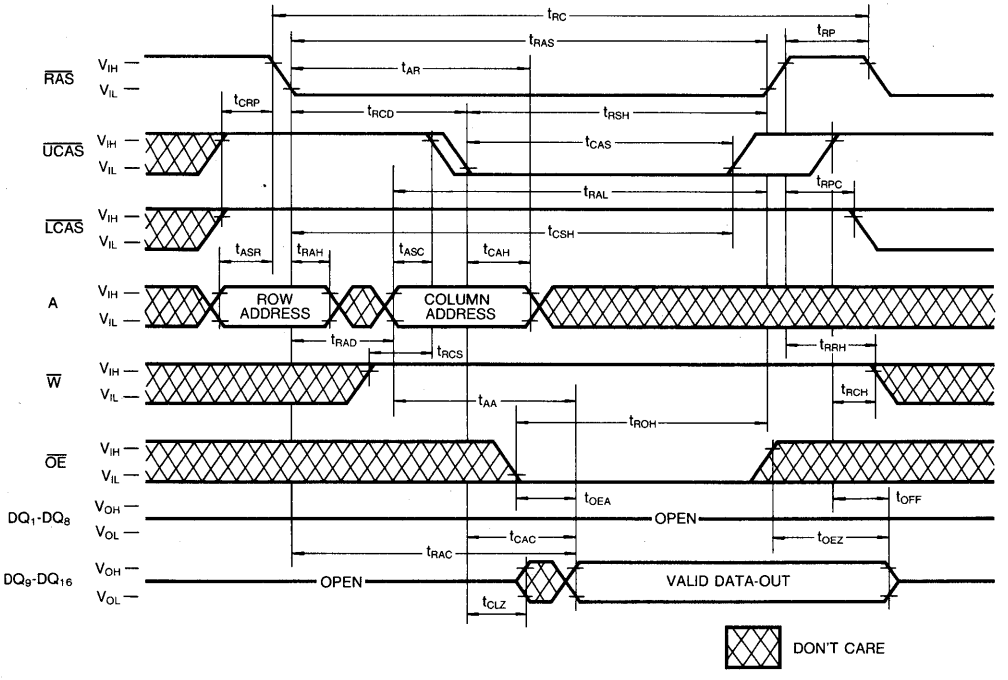


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

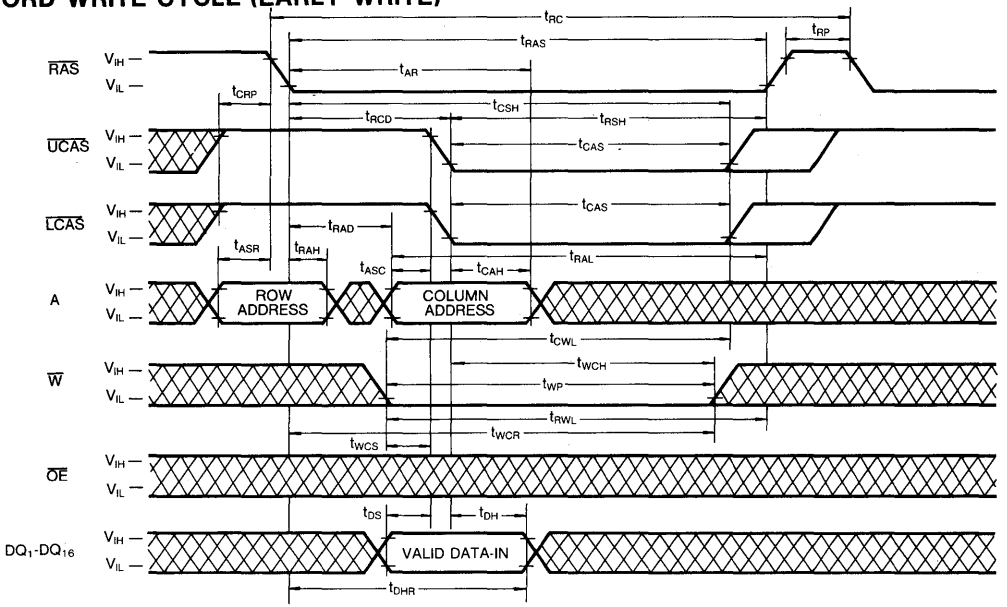


UPPER BYTE READ CYCLE

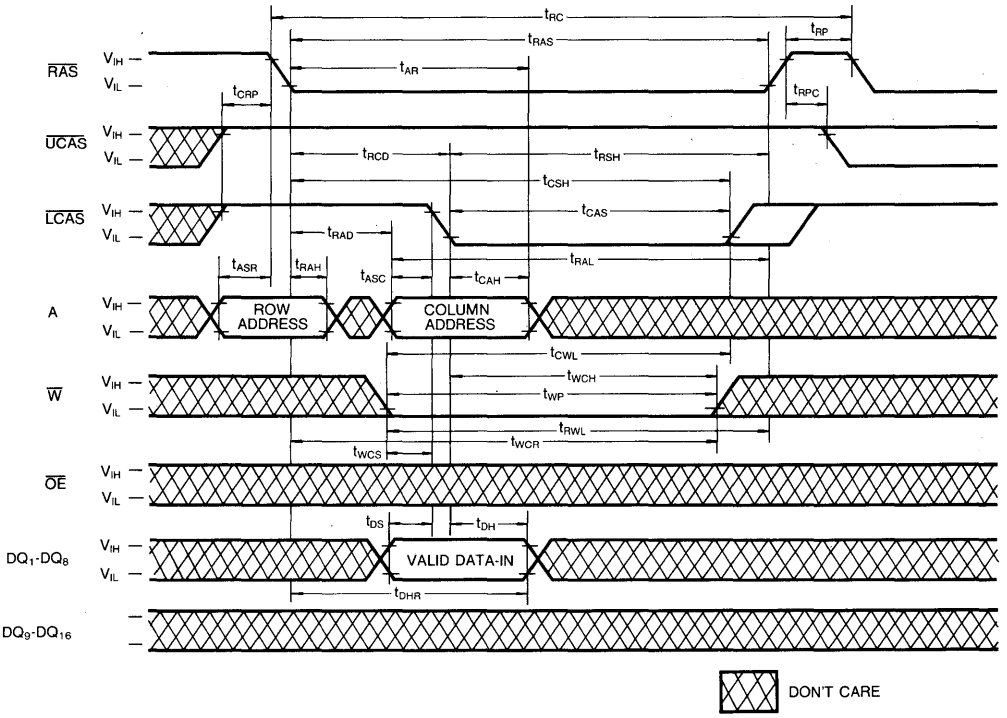


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

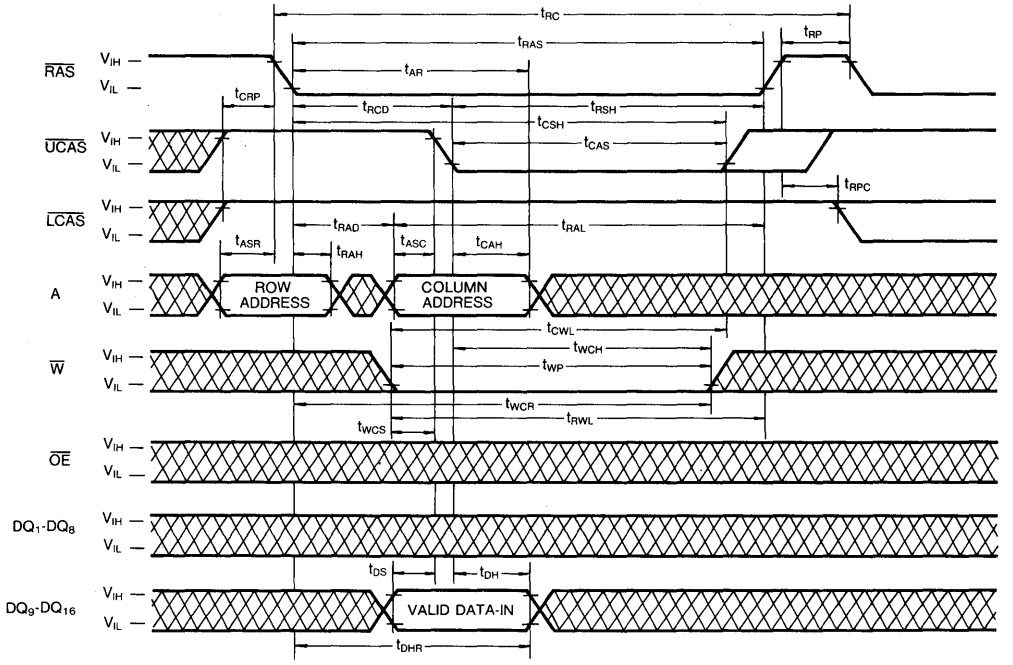


LOWER BYTE WRITE CYCLE (EARLY WRITE)

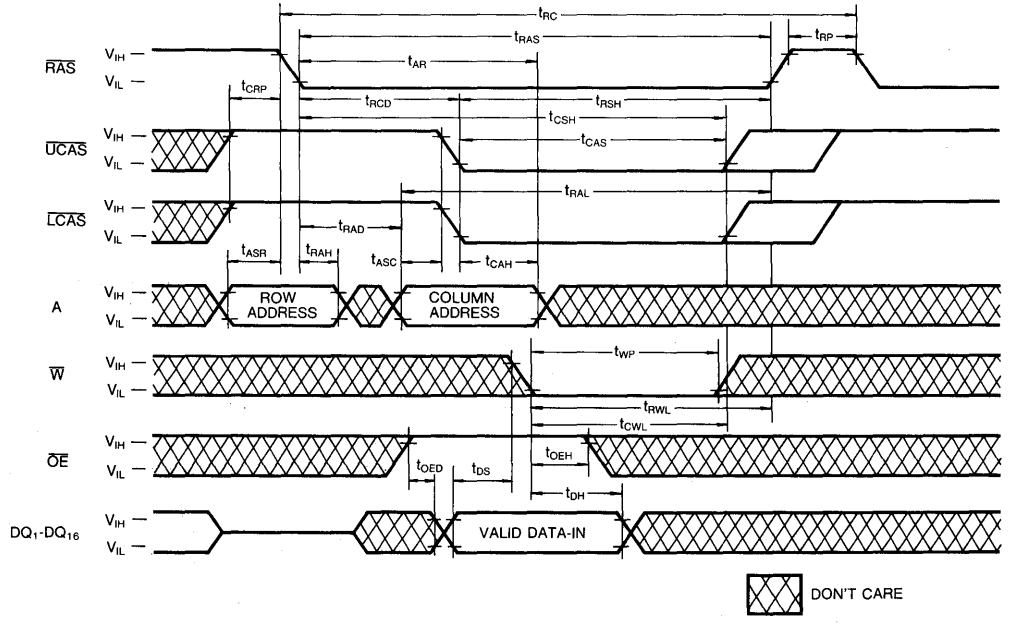


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

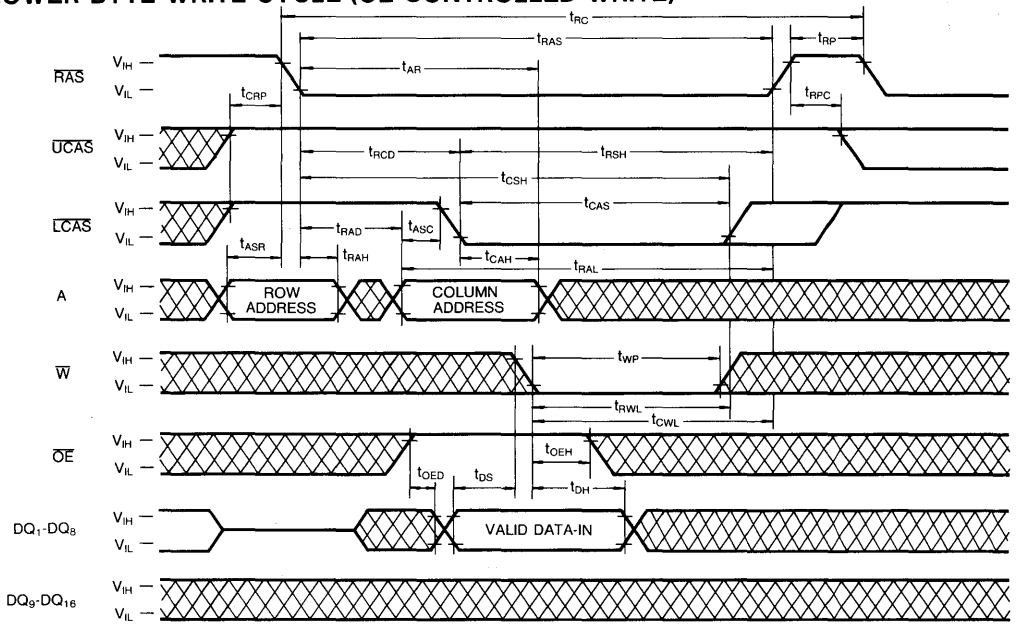


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

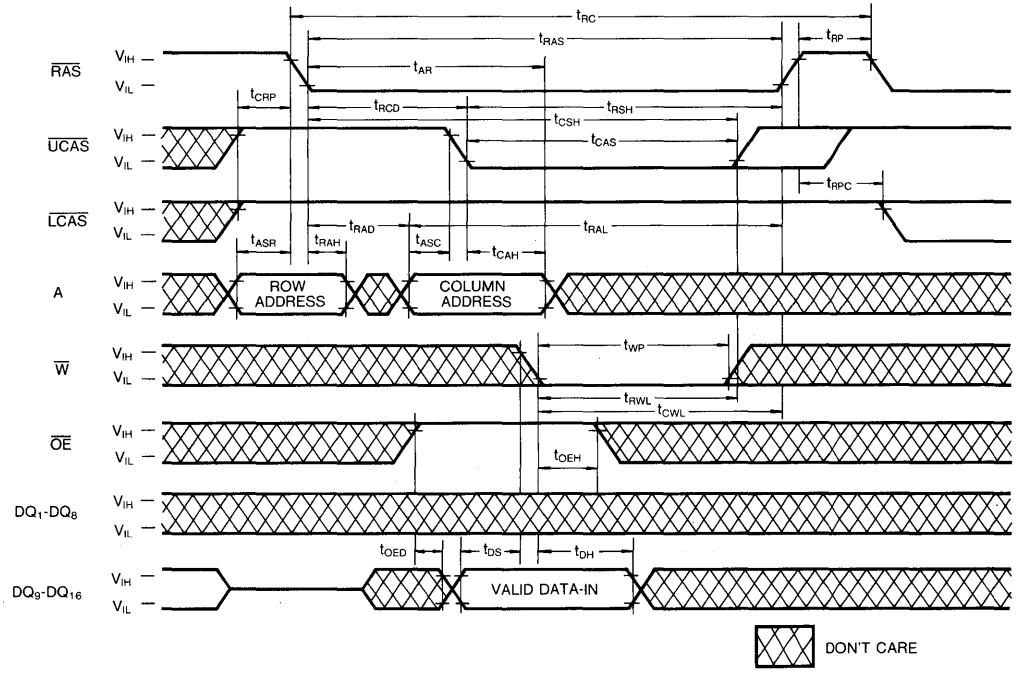


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

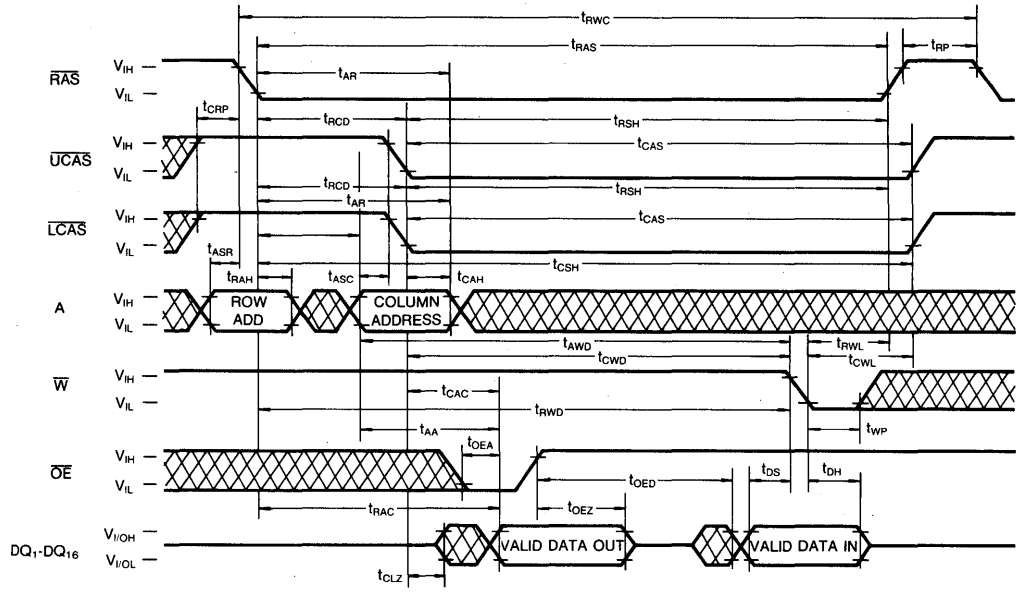


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

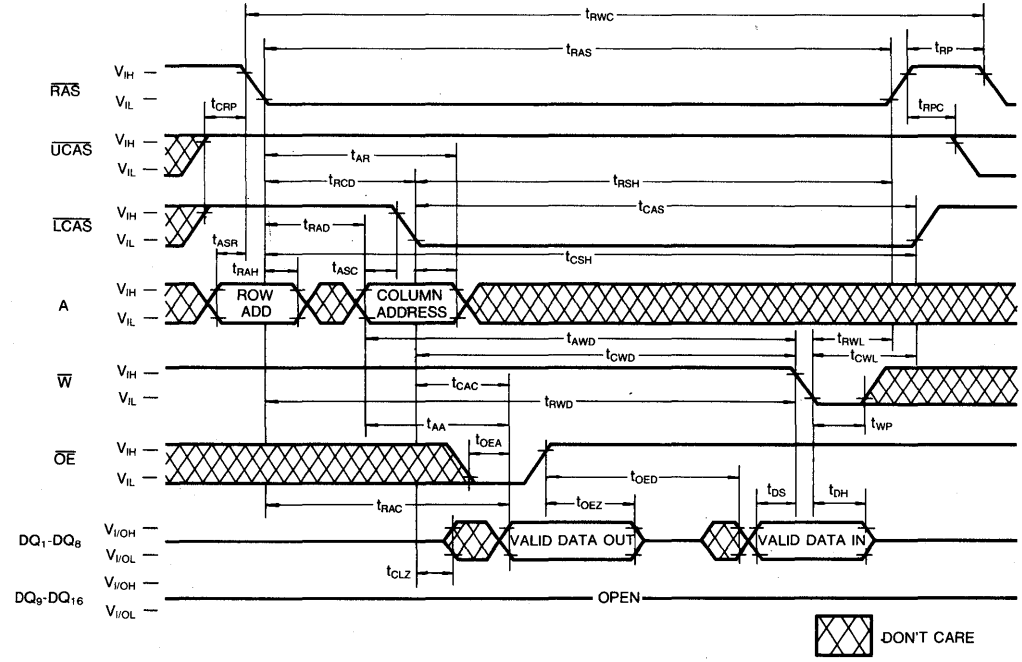


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

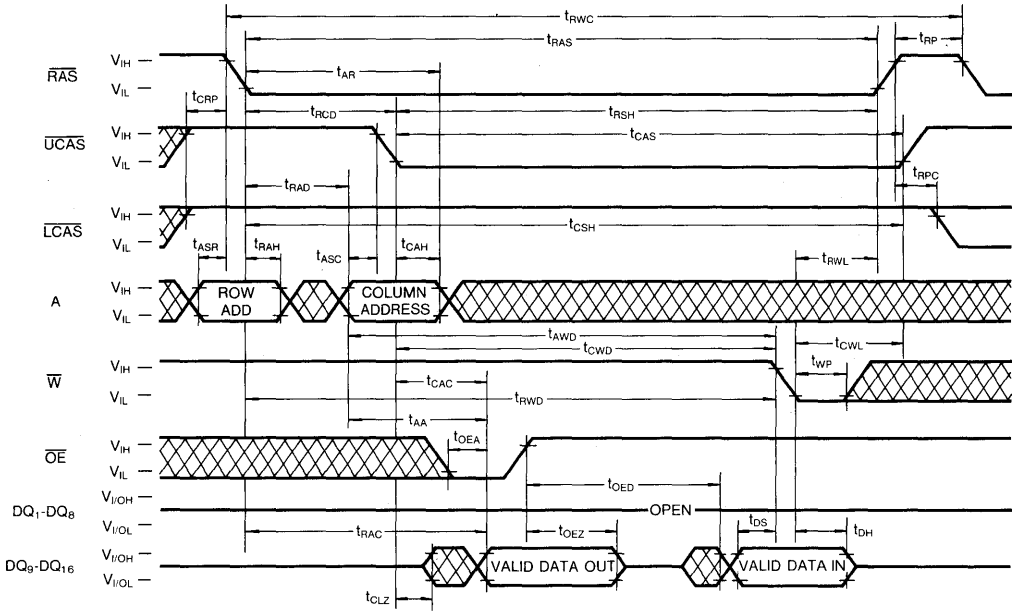


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

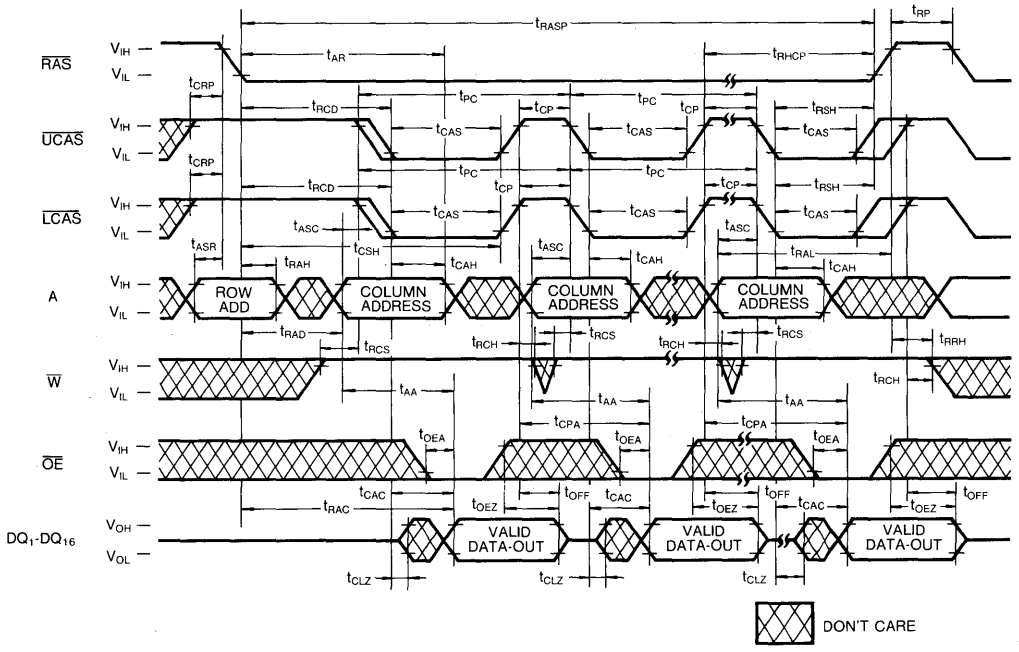


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

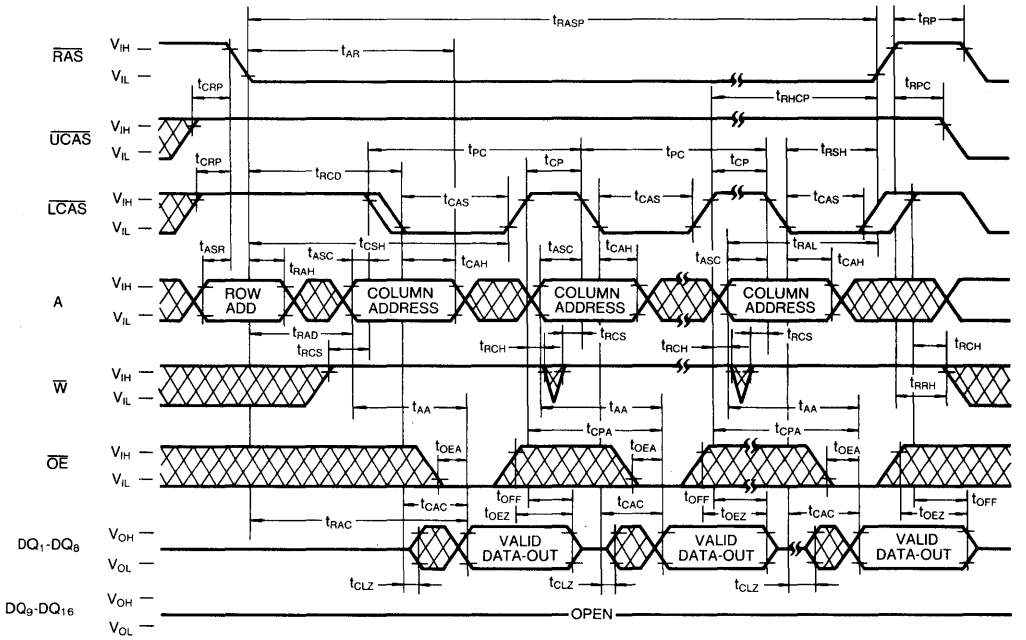


FAST PAGE MODE WORD READ CYCLE

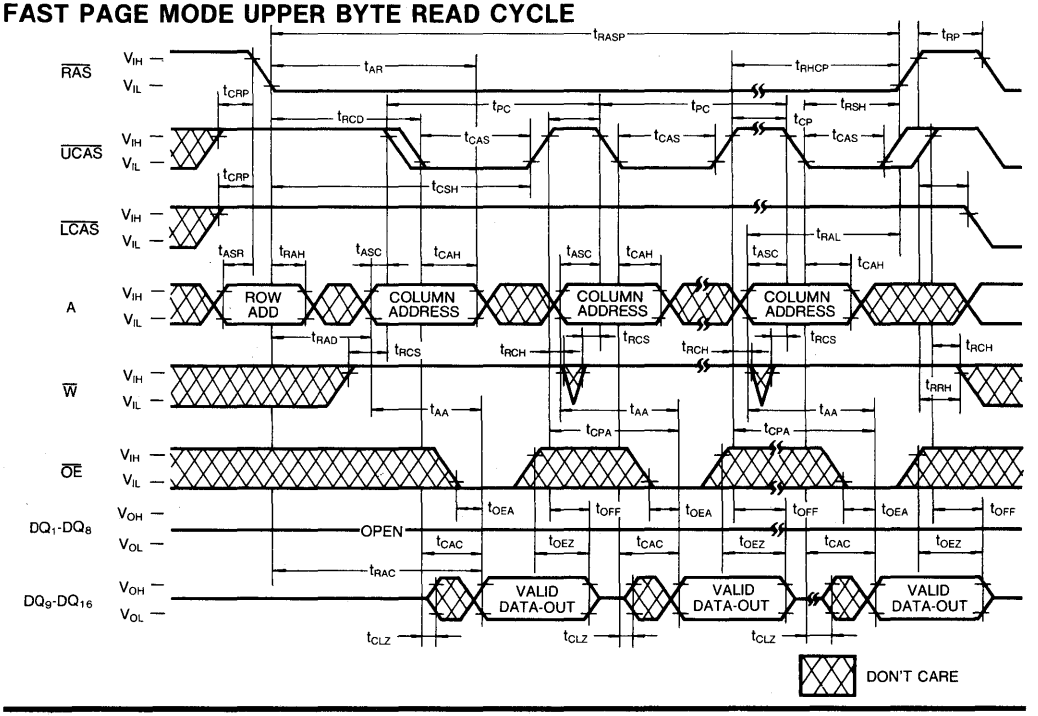


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

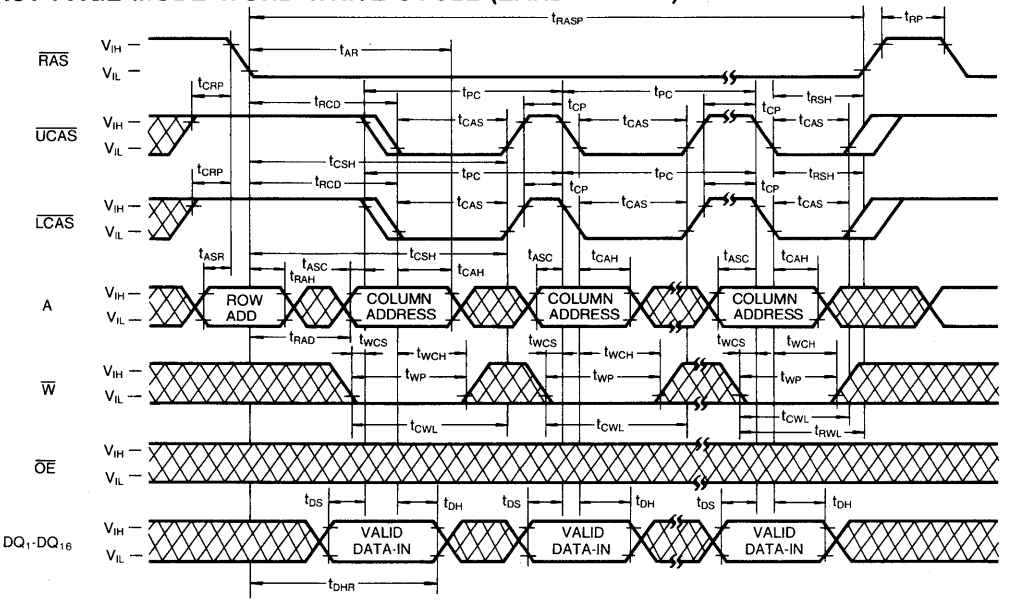


FAST PAGE MODE UPPER BYTE READ CYCLE

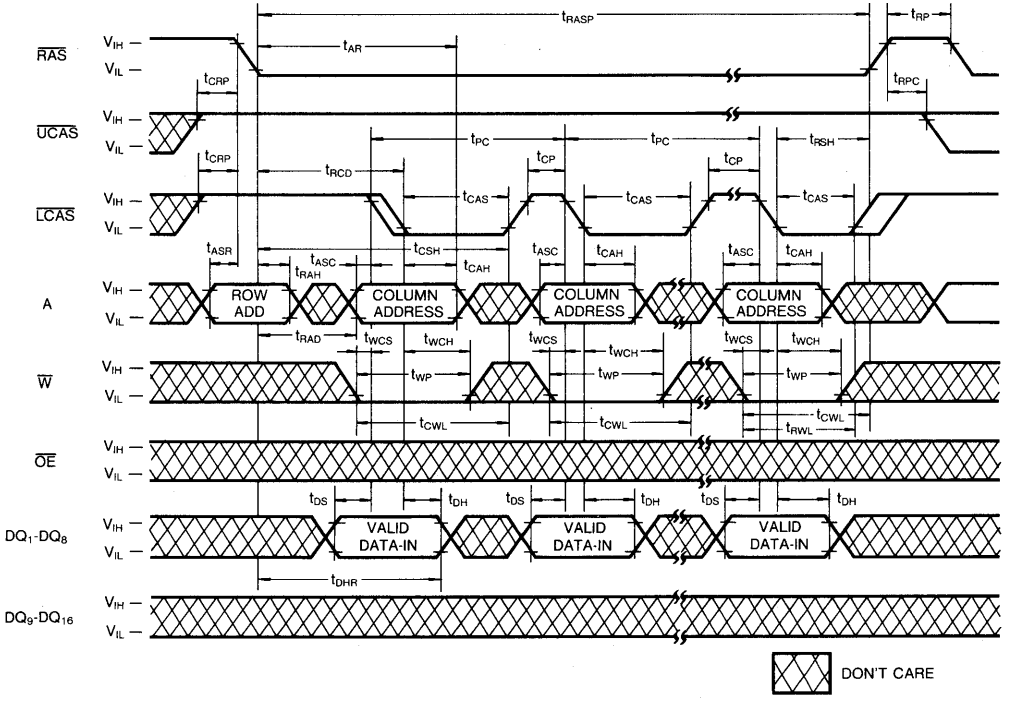


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

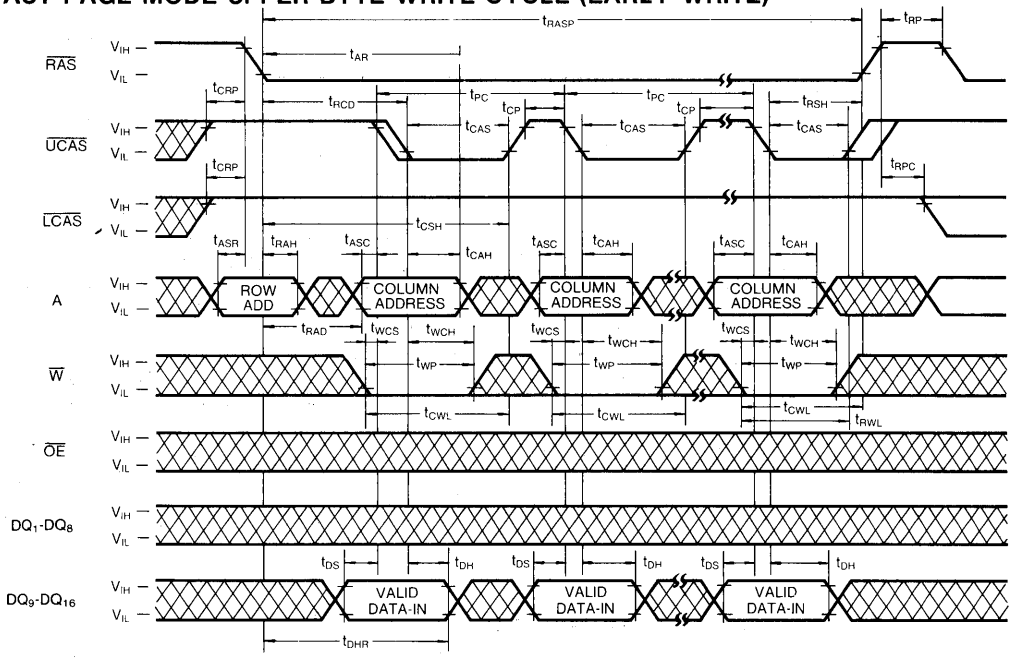


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

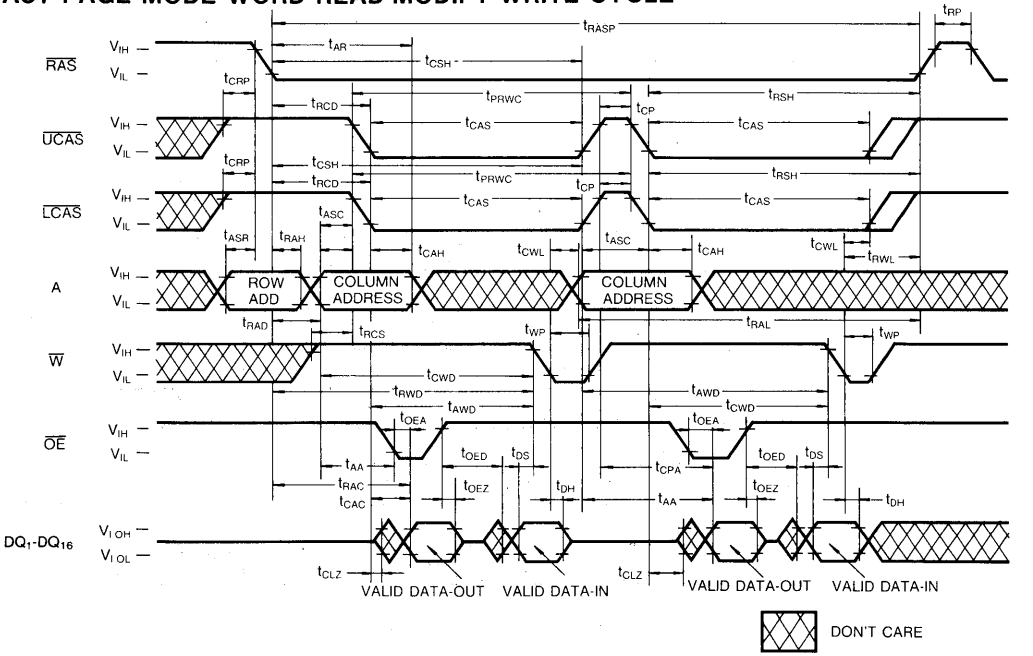


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

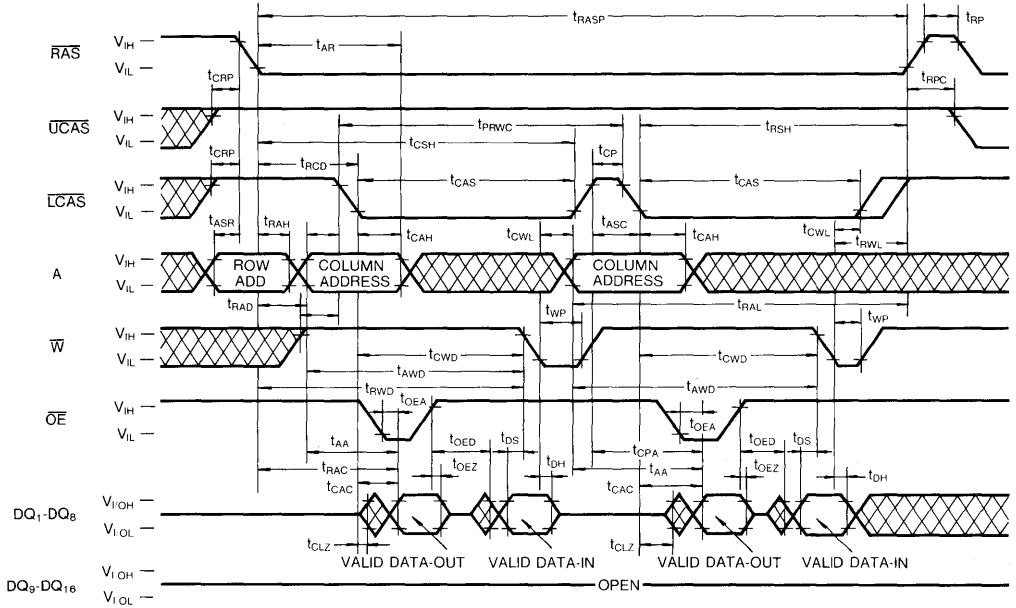


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

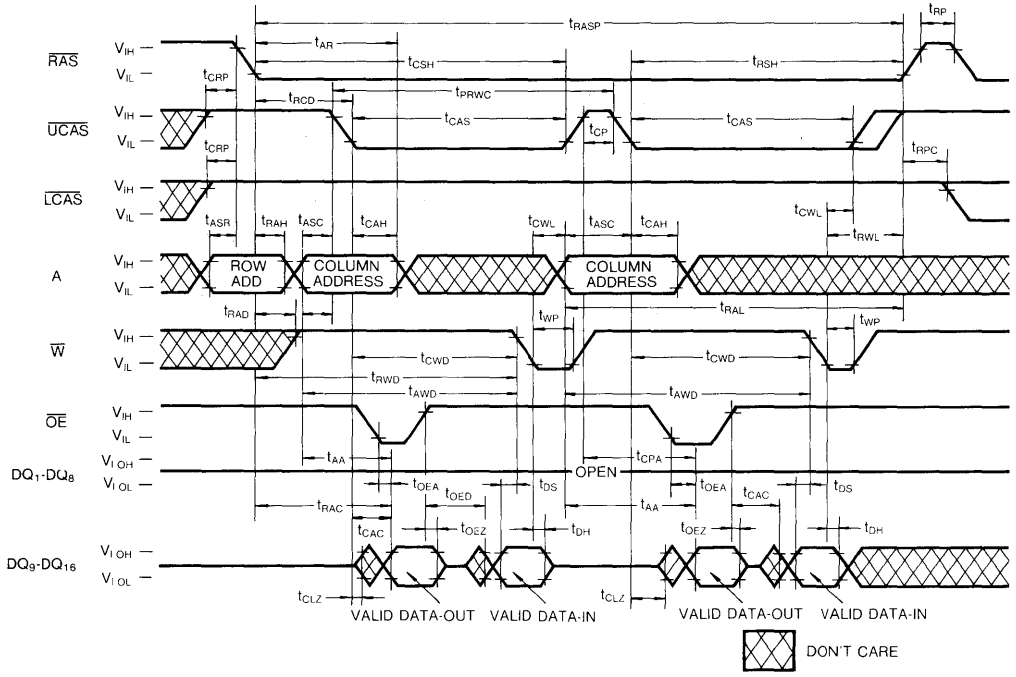


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



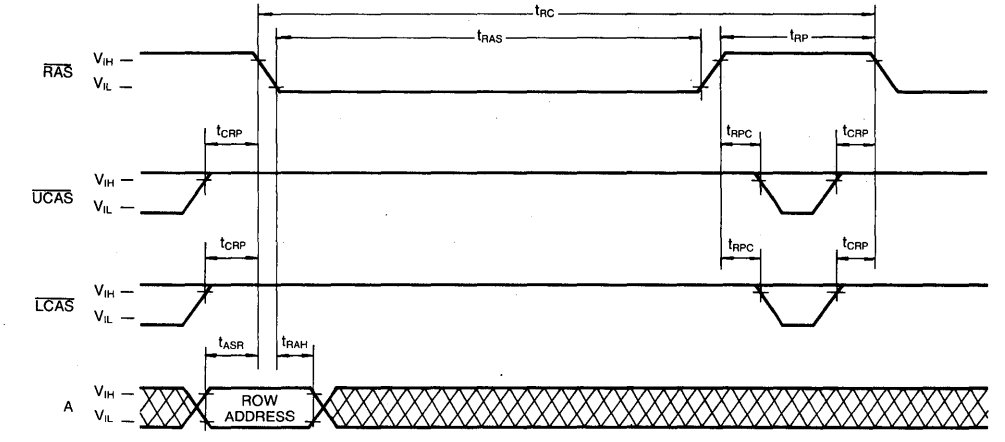
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

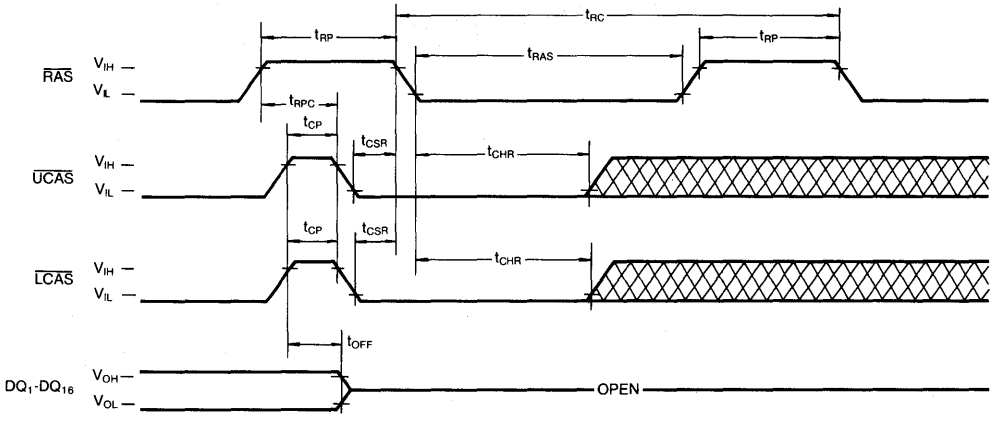
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

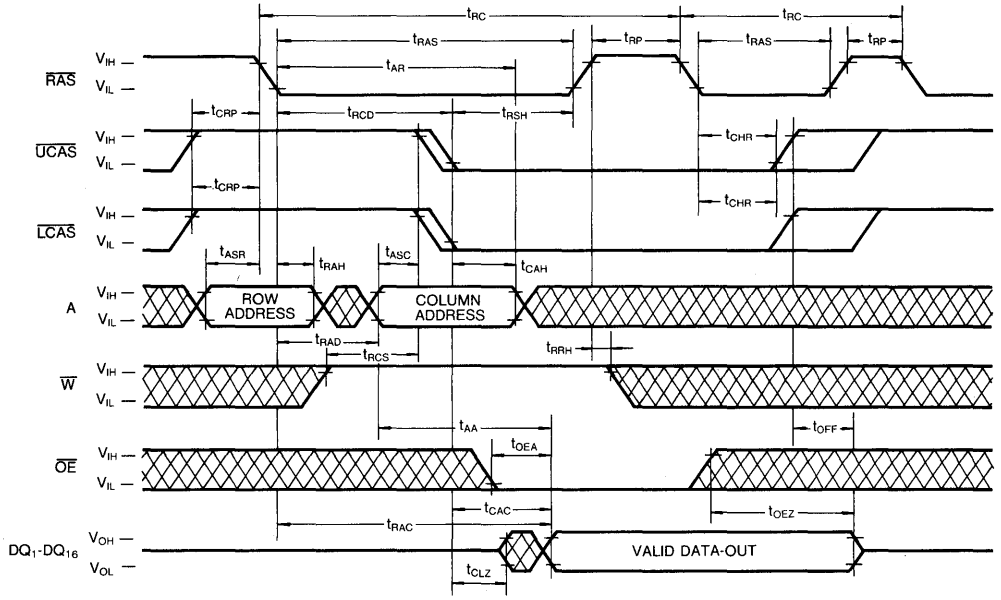
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



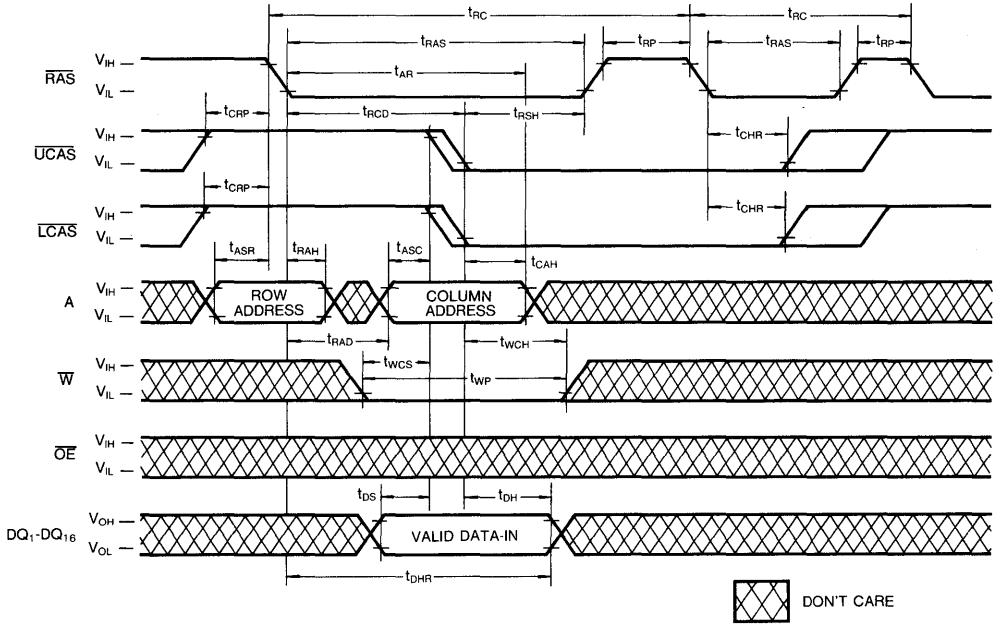
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

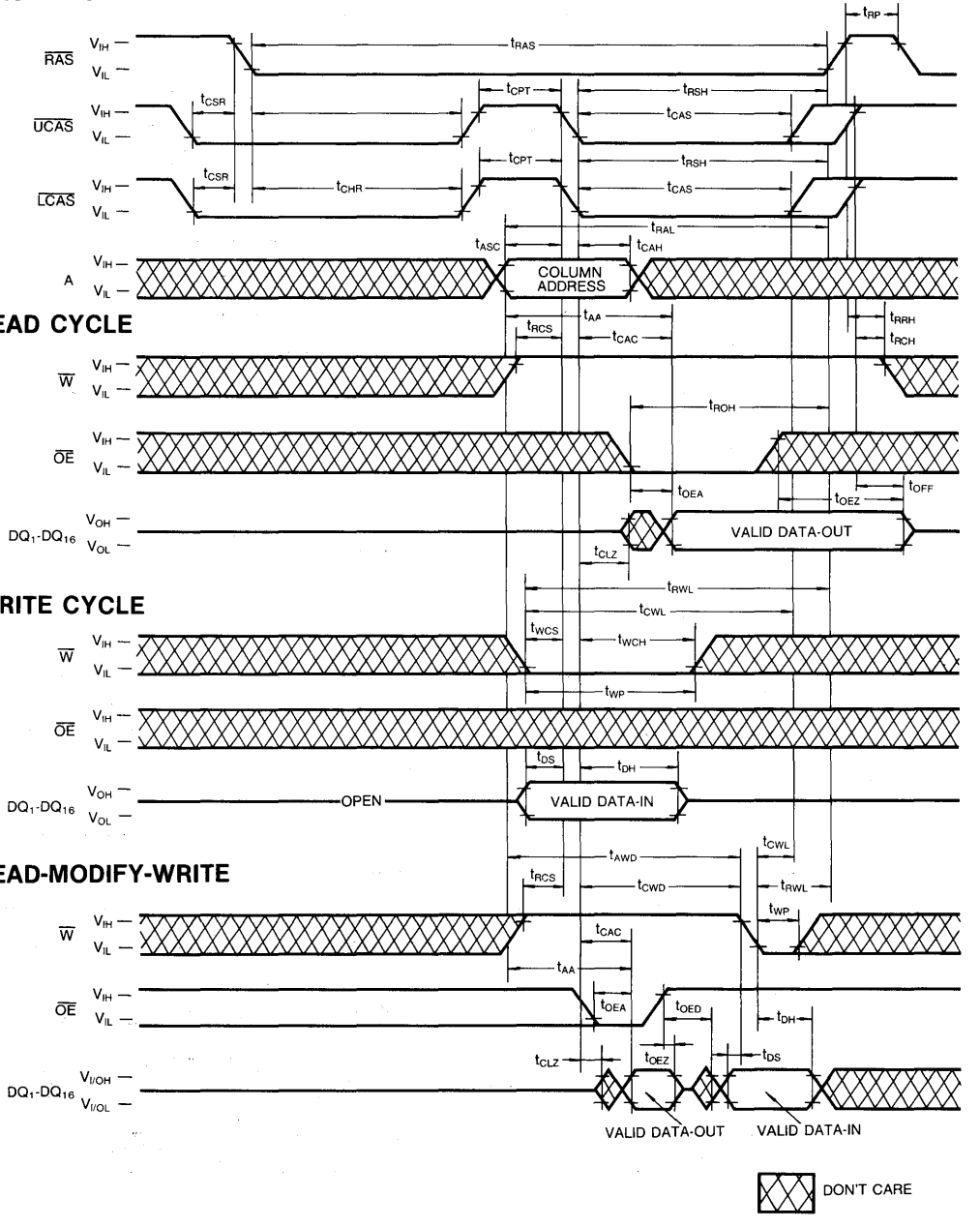


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM416C256 contains 4,194,304 memory locations arranged in 16 groups of 262,144×1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM416C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM416C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/x$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If x$\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if x$\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM416C256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of W or x$\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before x$\overline{CAS}$. The 16 Bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C256 DQ pins.

Data Output

The KM416C256 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM416C256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM416C256 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 8ms. There are several ways to accomplish this:

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM416C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM416C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM416C256 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

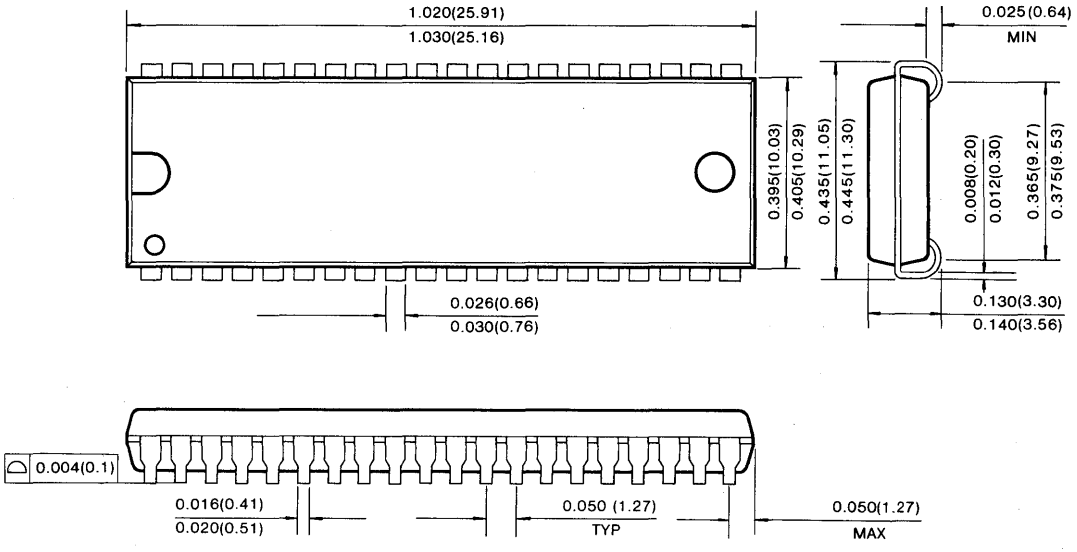
Power-Up

If $\overline{RAS}=V_{SS}$ during power-up, the KM416C256 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



256K×18 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM418C256- 7	70ns	20ns	130ns
KM418C256- 8	80ns	20ns	150ns
KM418C256-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL and CMOS compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

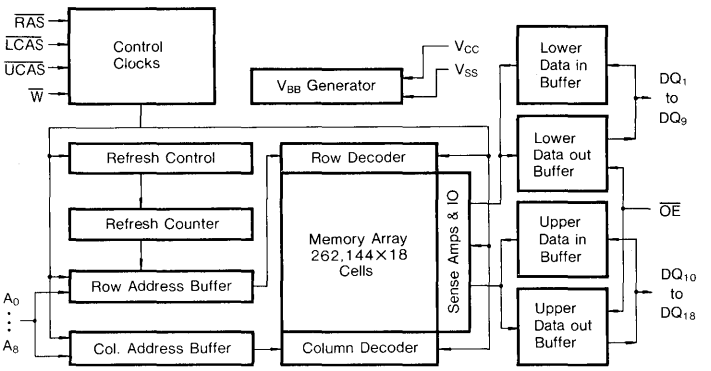
GENERAL DESCRIPTION

The Samsung KM418C256 is a CMOS high speed 262,144 bit × 18 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and performance portable computers.

The KM418C256 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

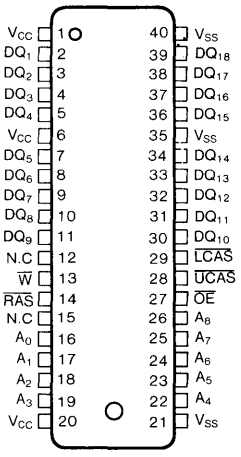
The KM418C256 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM418C256J**



Pin Name	Pin Function
A_0-A_8	Address Inputs
$DQ_{1\text{-}18}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @ t_{RC}=min)	KM418C256- 7	I_{CC1}	—	150	mA
	KM418C256- 8		—	130	mA
	KM418C256-10		—	110	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM418C256- 7	I_{CC3}	—	150	mA
	KM418C256- 8		—	130	mA
	KM418C256-10		—	110	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @ t_{PC}=min.)	KM418C256- 7	I_{CC4}	—	90	mA
	KM418C256- 8		—	80	mA
	KM418C256-10		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @ t_{RC}=min)	KM418C256- 7	I_{CC6}	—	150	mA
	KM418C256- 8		—	130	mA
	KM418C256-10		—	110	mA
Standby Currnet ($\overline{RAS}$=V_{IH}, $\overline{UCAS}$ or $\overline{LCAS}$=V_{IL} Dout=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is spedified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4} address can be changed maximum once while $\overline{UCAS}$ and $\overline{LCAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{18})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM418C256-7		KM418C256-8		KM418C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	10		10		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

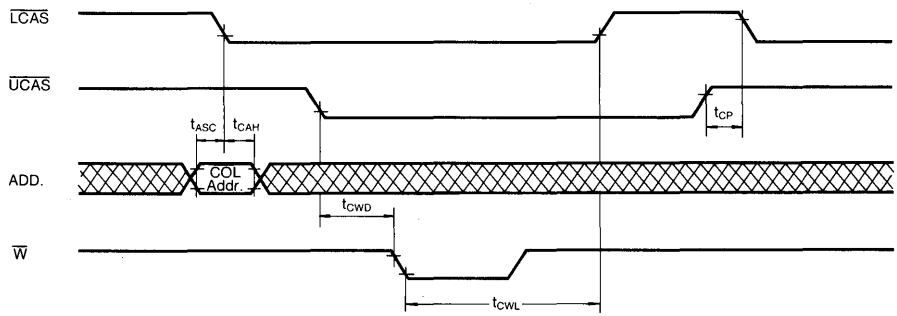
Parameter	Symbol	KM418C256-7		KM418C256-8		KM418C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		120		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM418C256 Truth Table

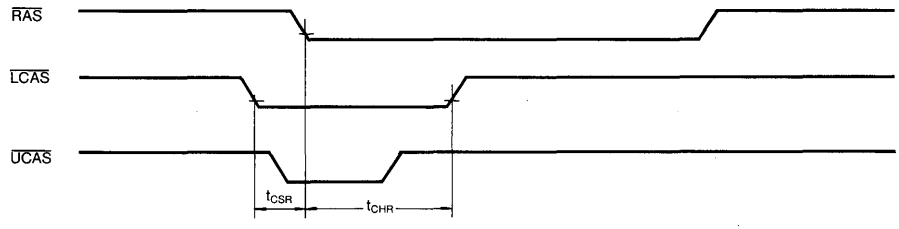
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim9}$	$DQ_{10\sim18}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

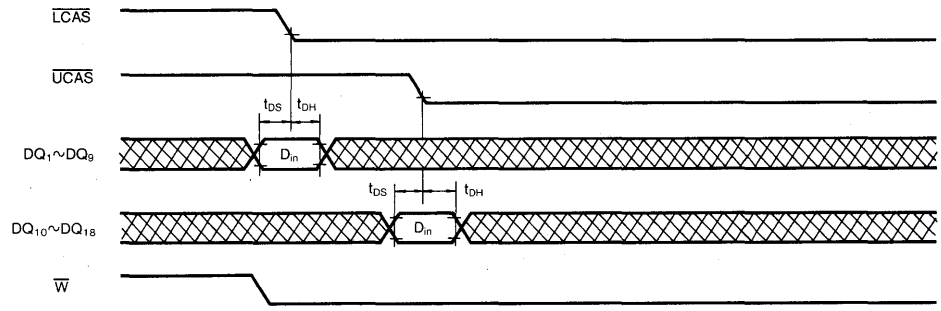
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

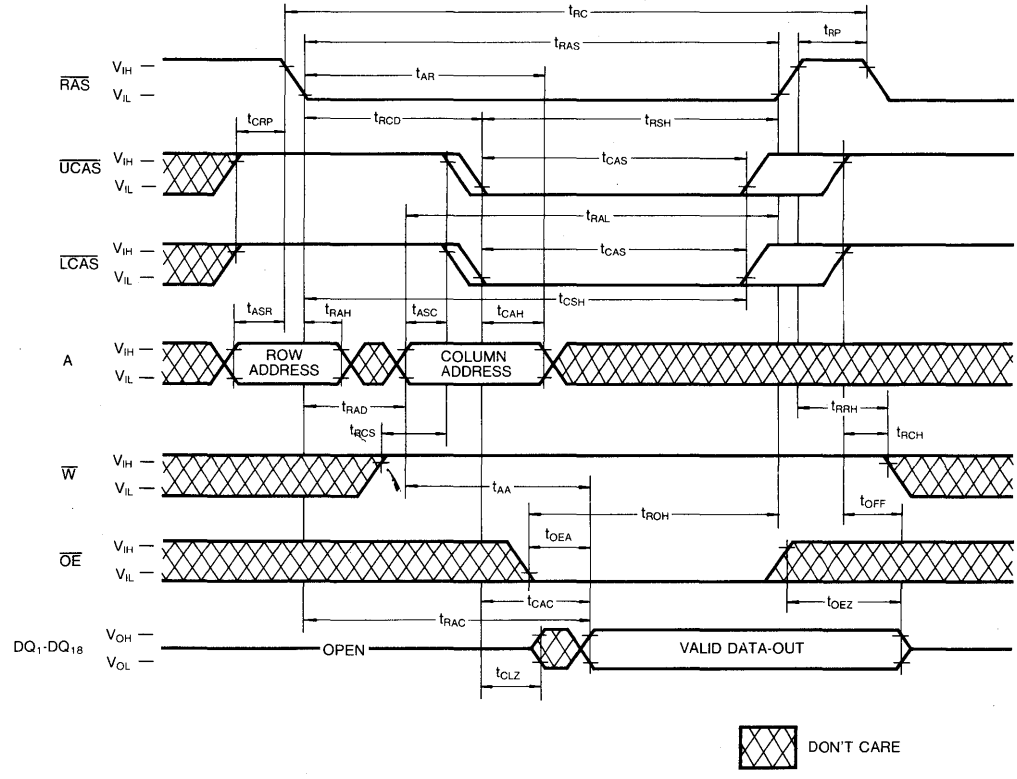


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



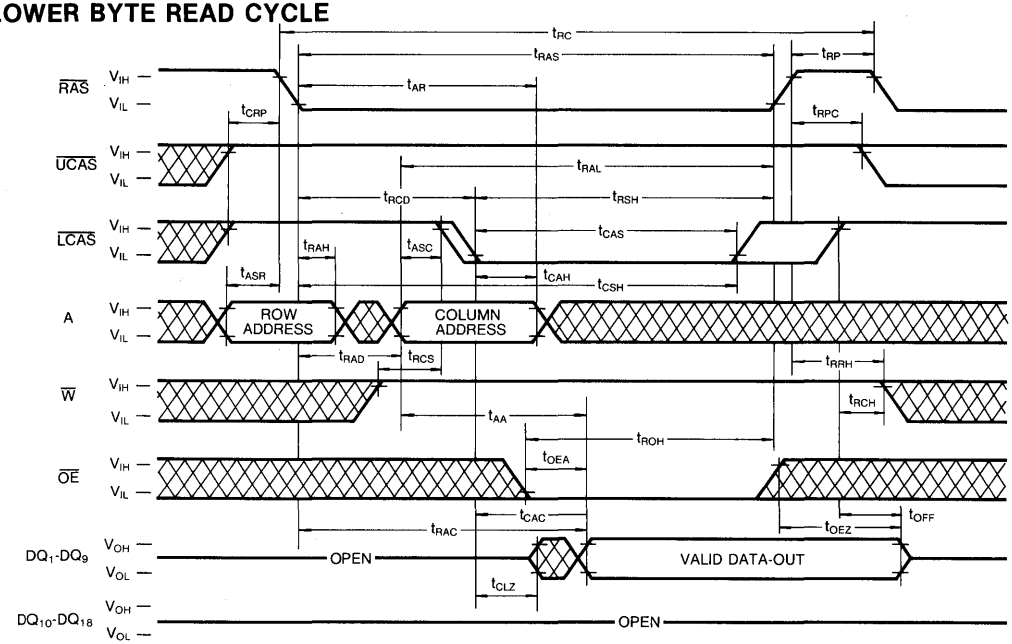
TIMING DIAGRAMS

WORD READ CYCCLE

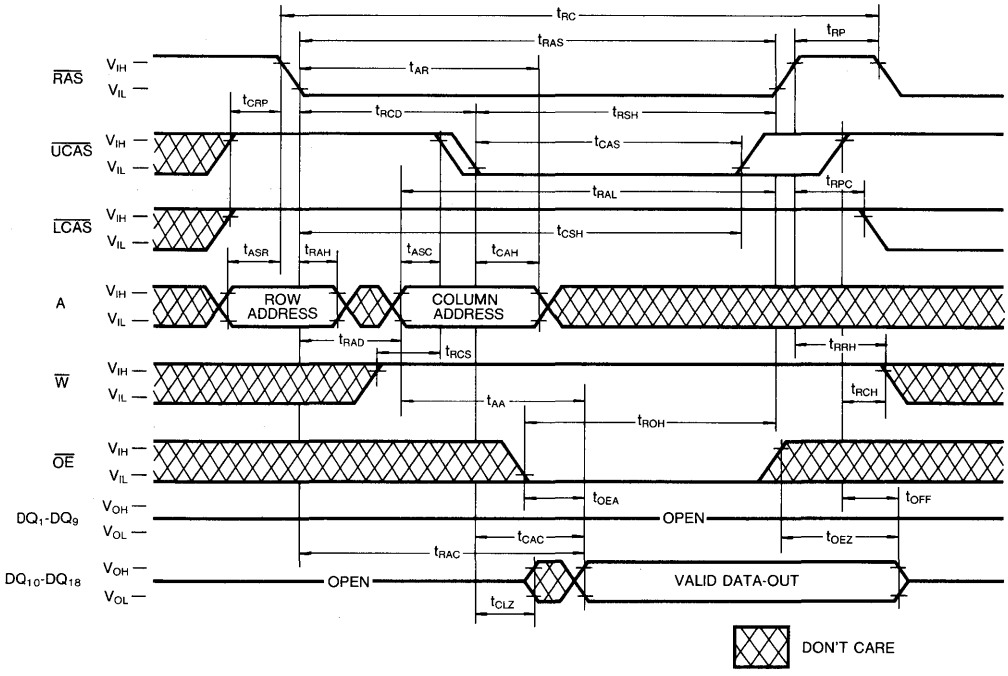


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

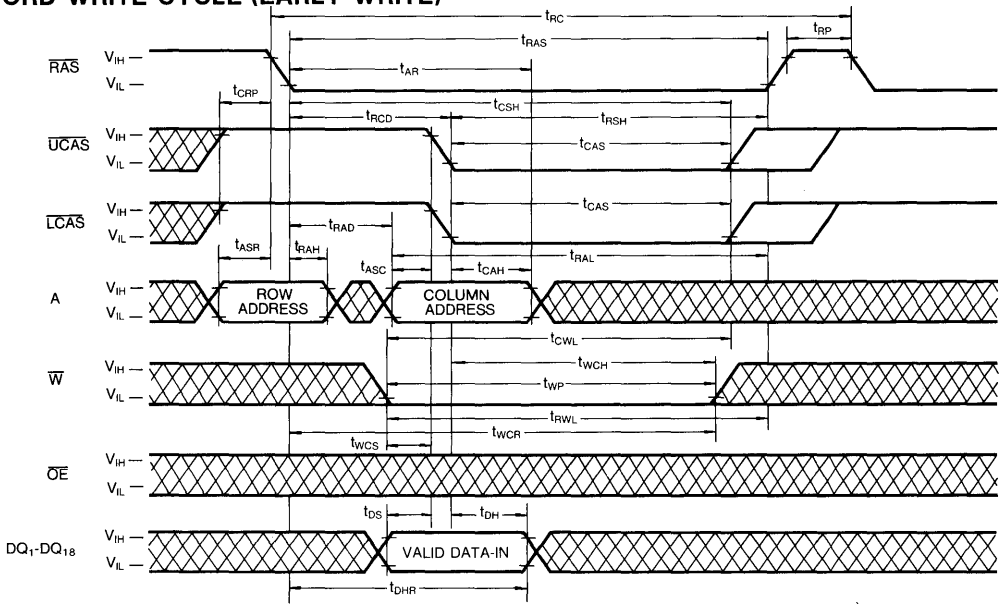


UPPER BYTE READ CYCLE

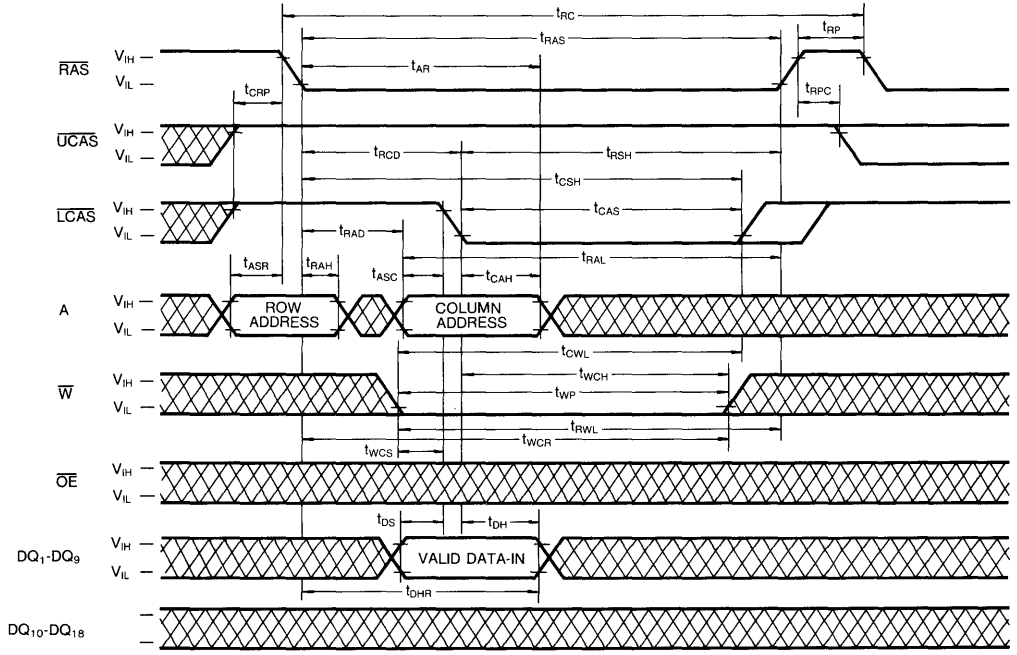


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

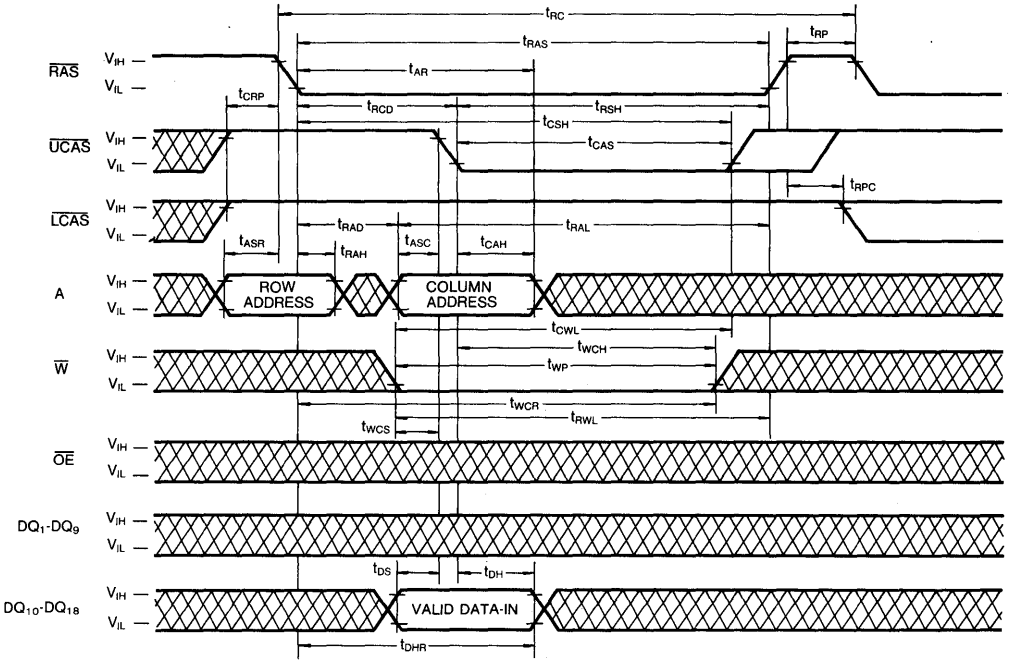


LOWER BYTE WRITE CYCLE (EARLY WRITE)

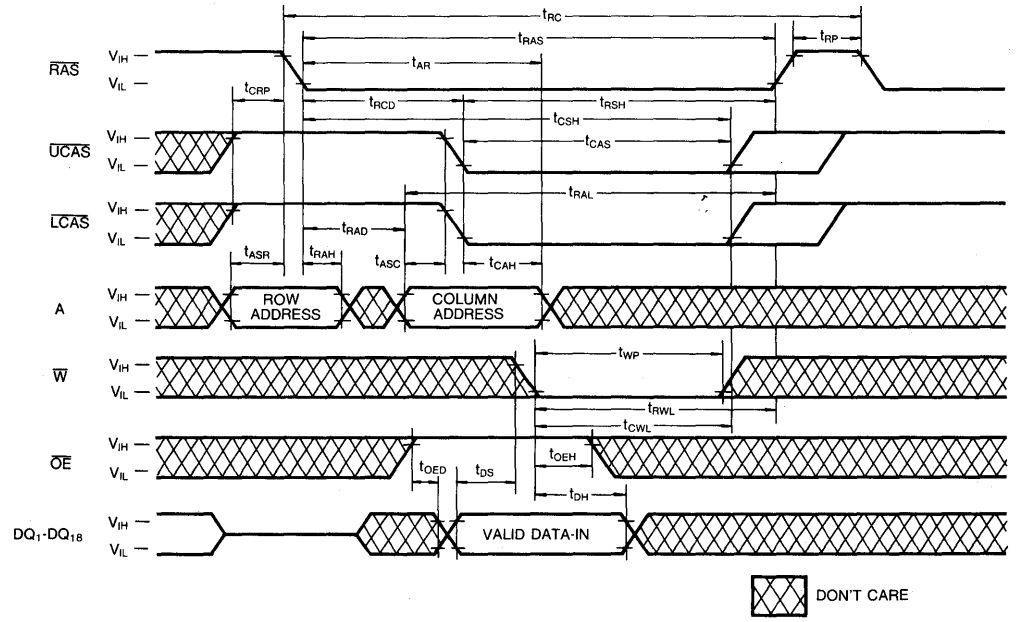


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

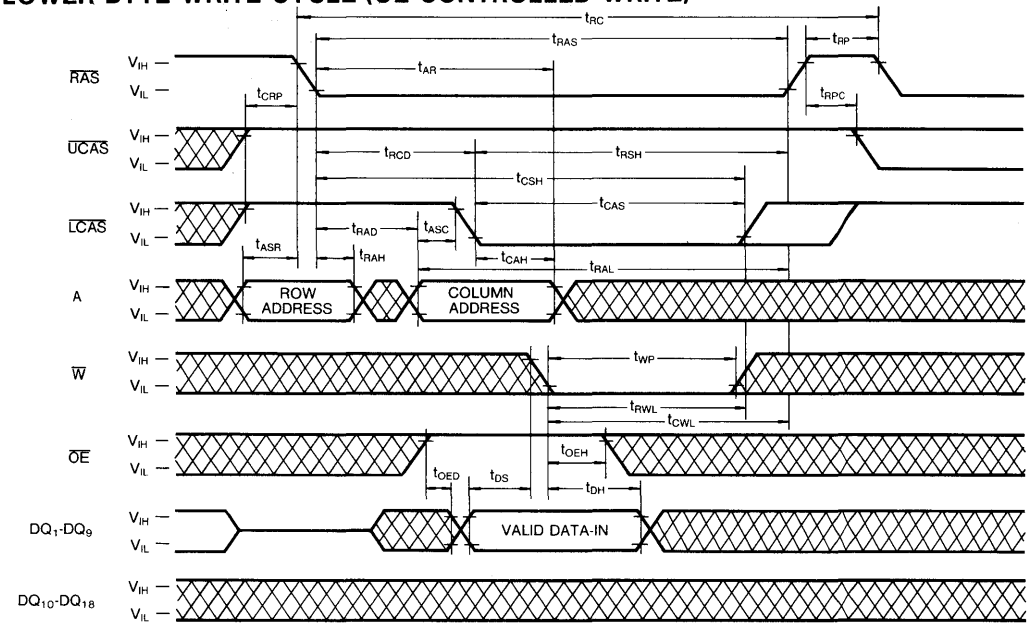


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

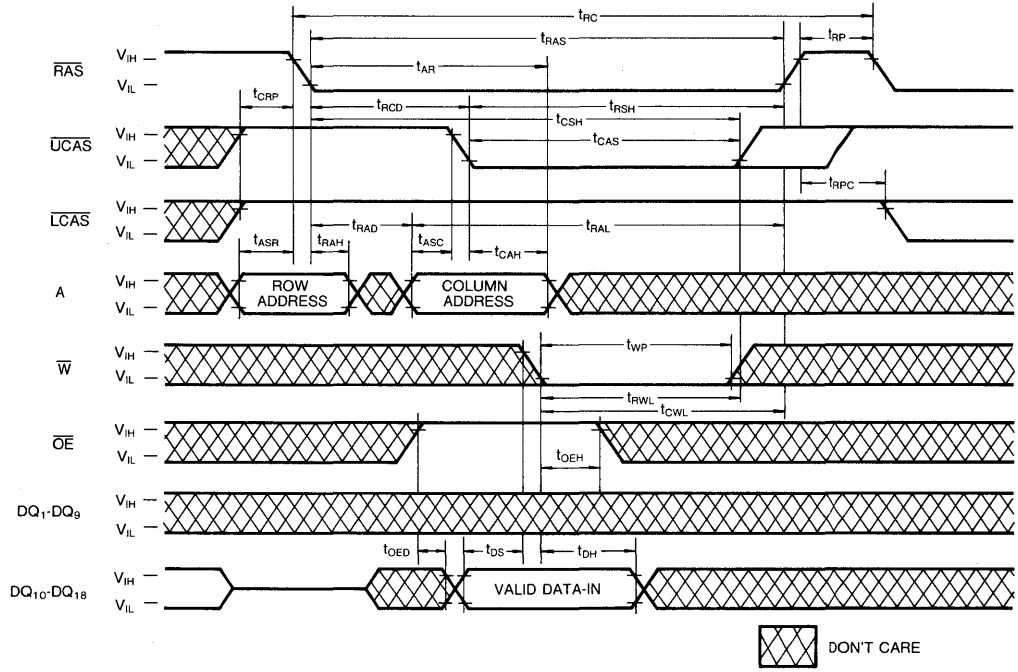


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

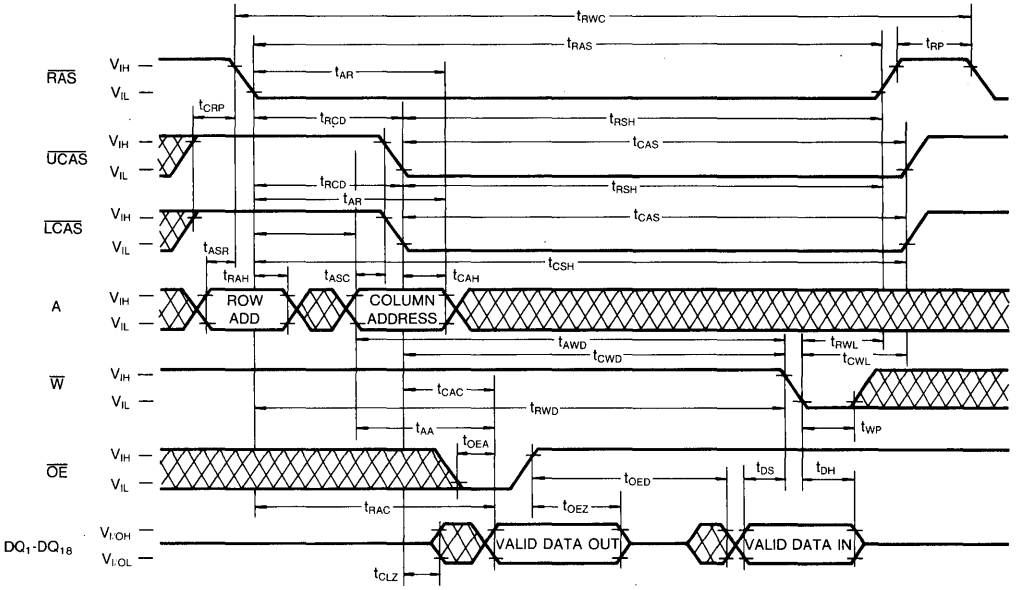


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

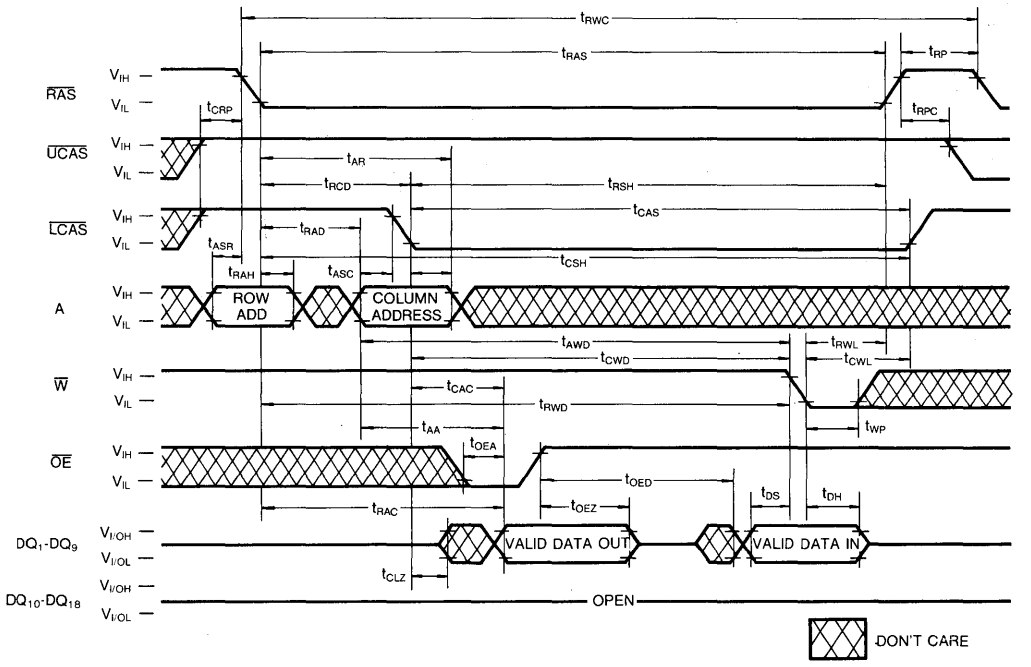


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

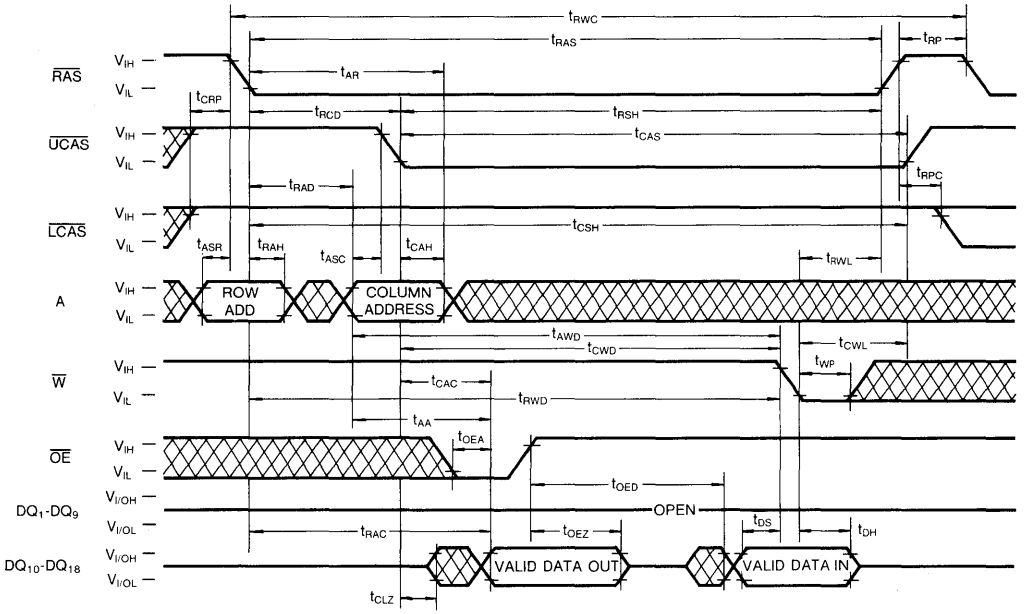


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

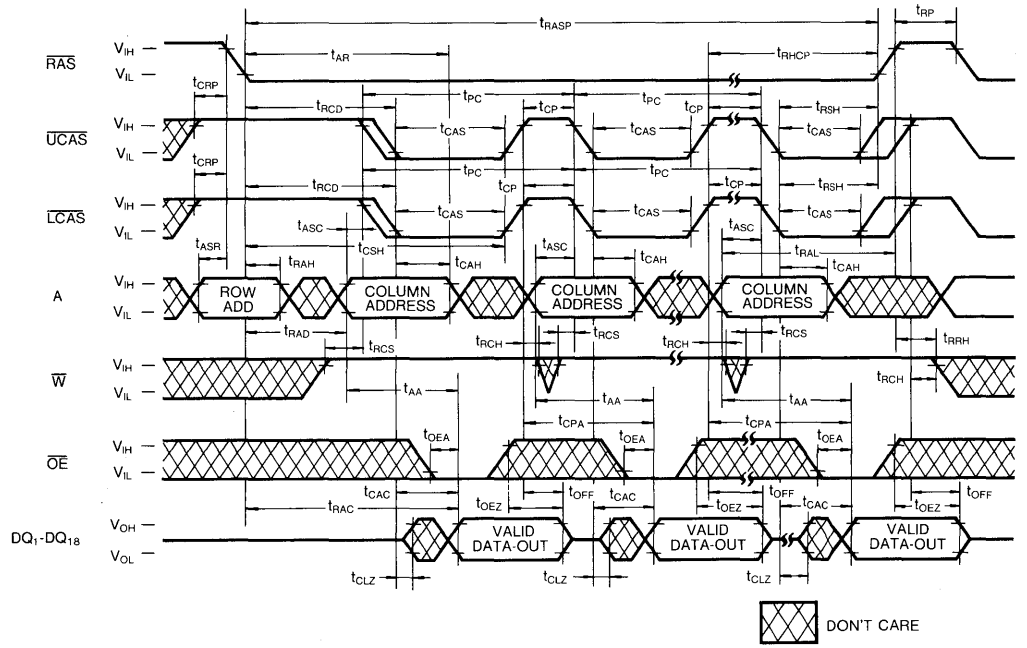


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

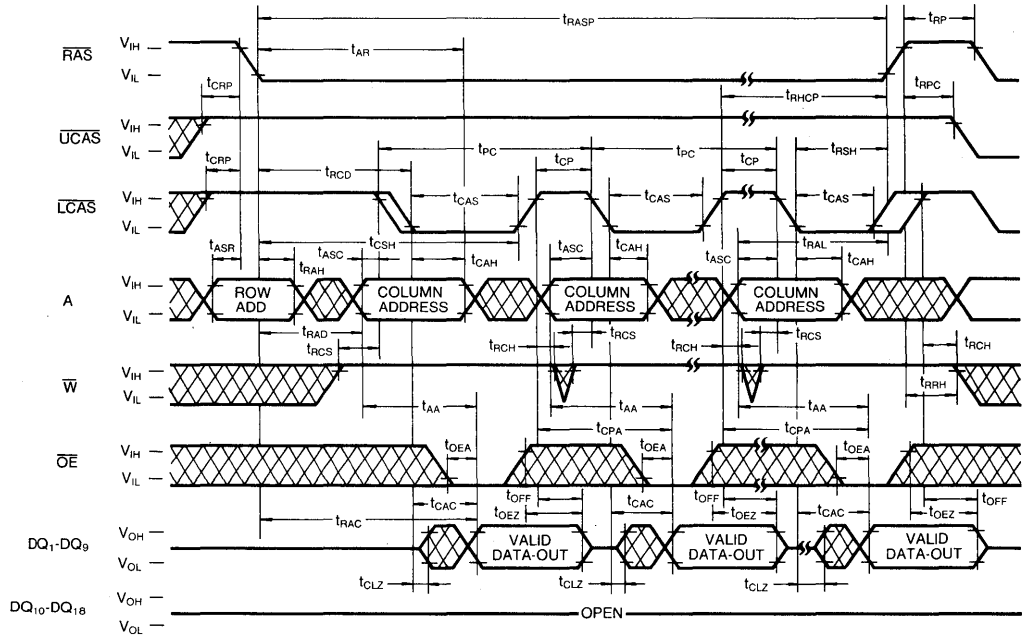


FAST PAGE MODE WORD READ CYCLE

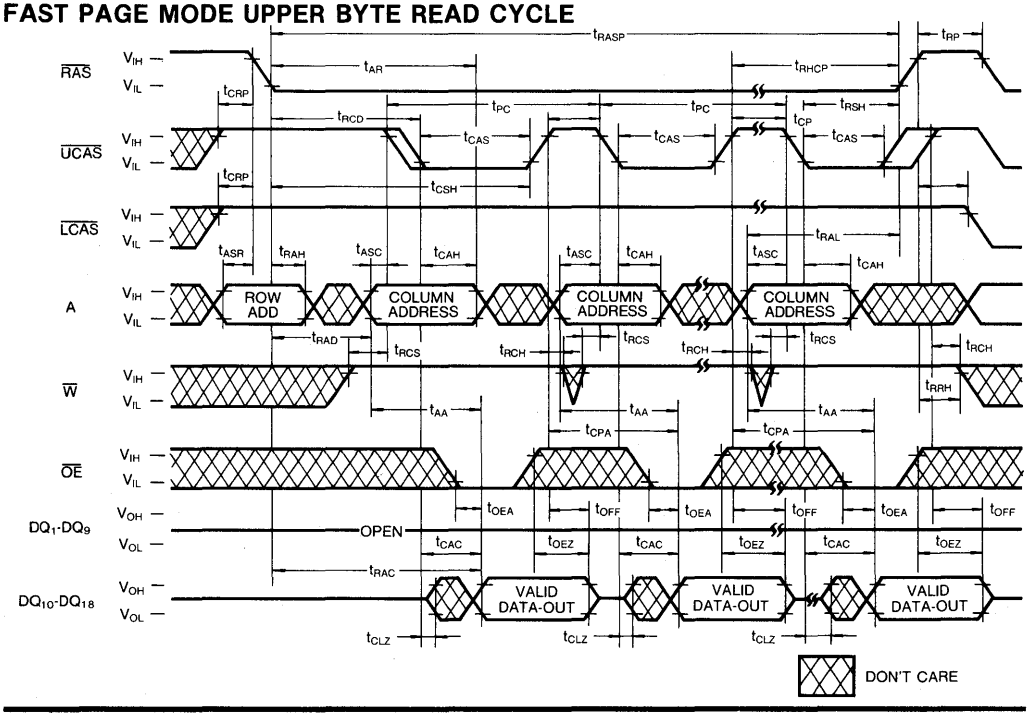


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

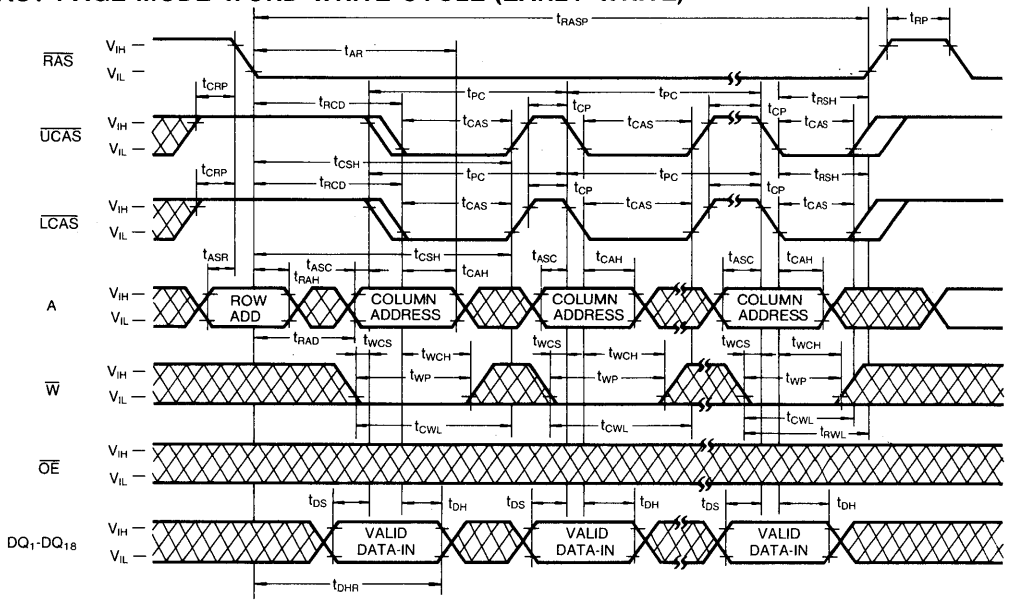


FAST PAGE MODE UPPER BYTE READ CYCLE

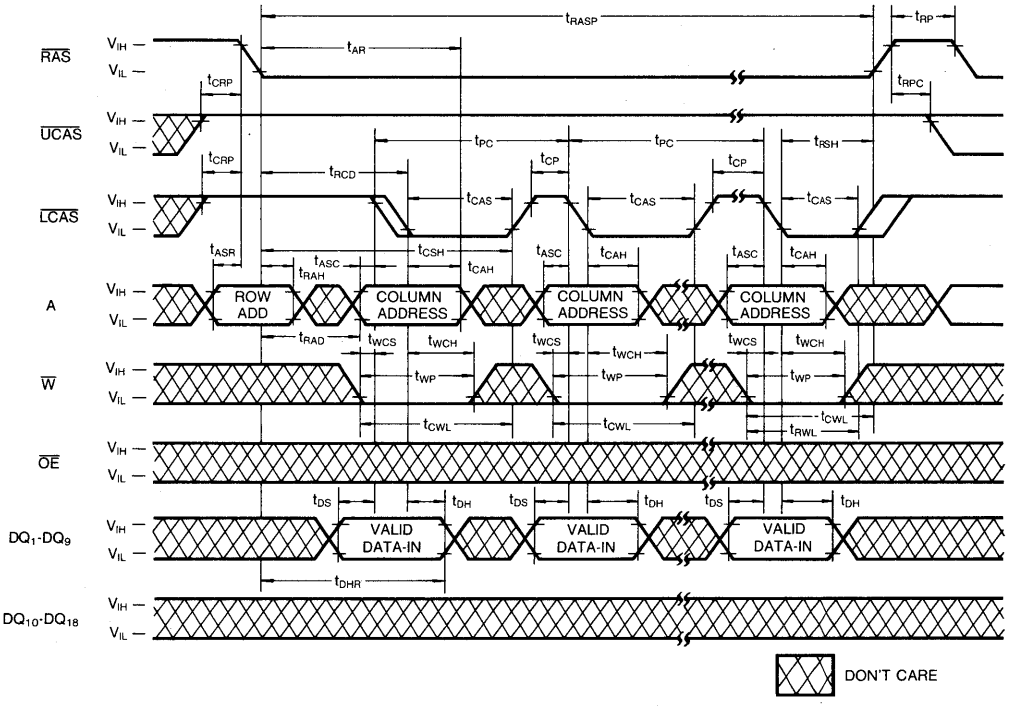


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

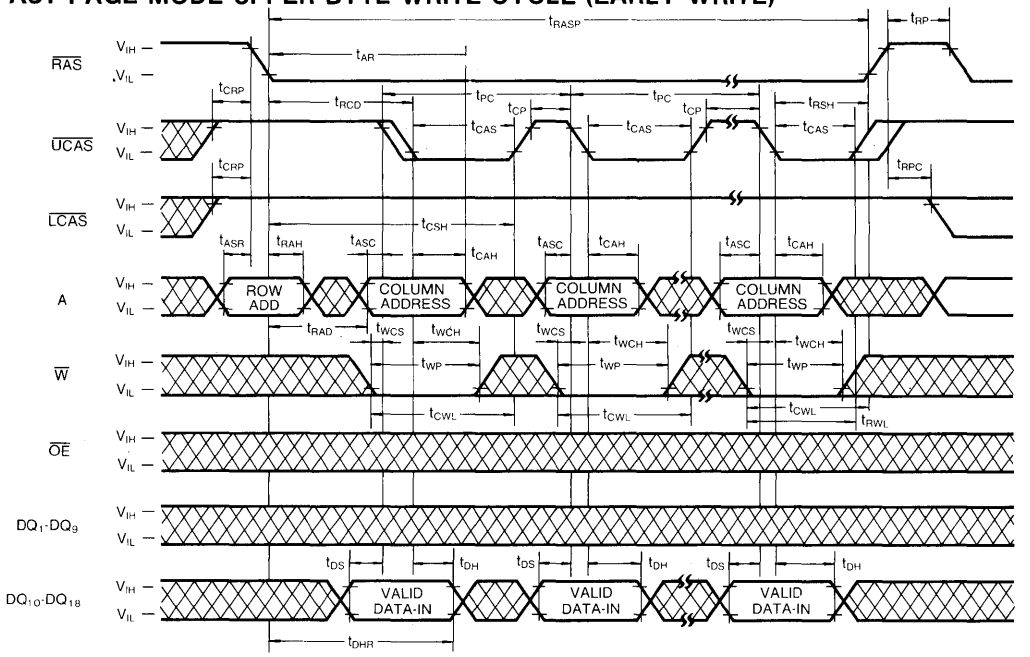


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

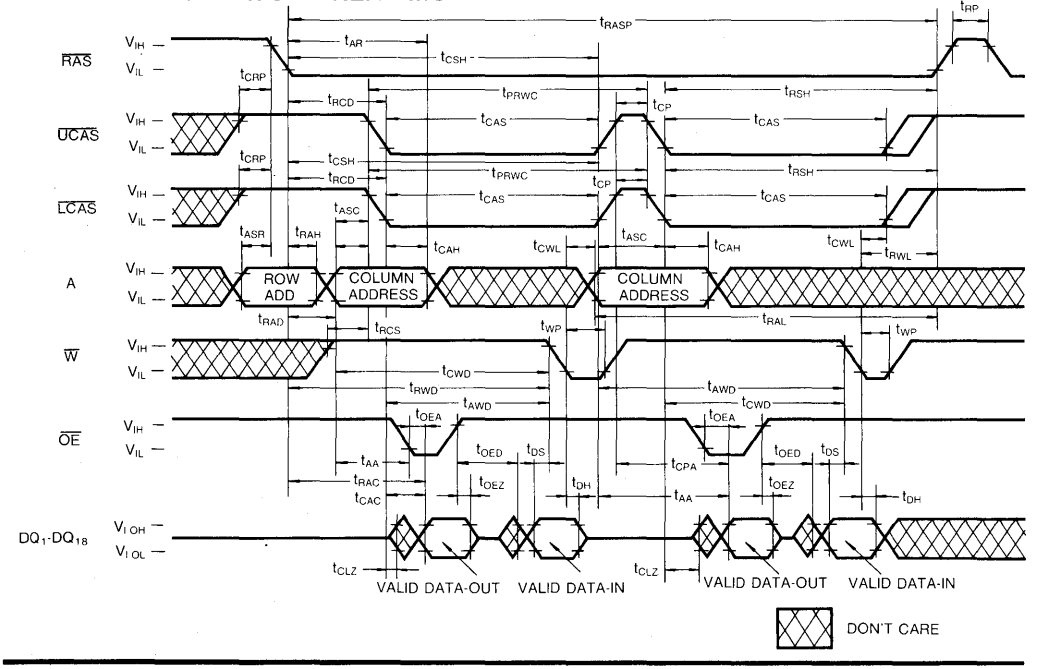


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

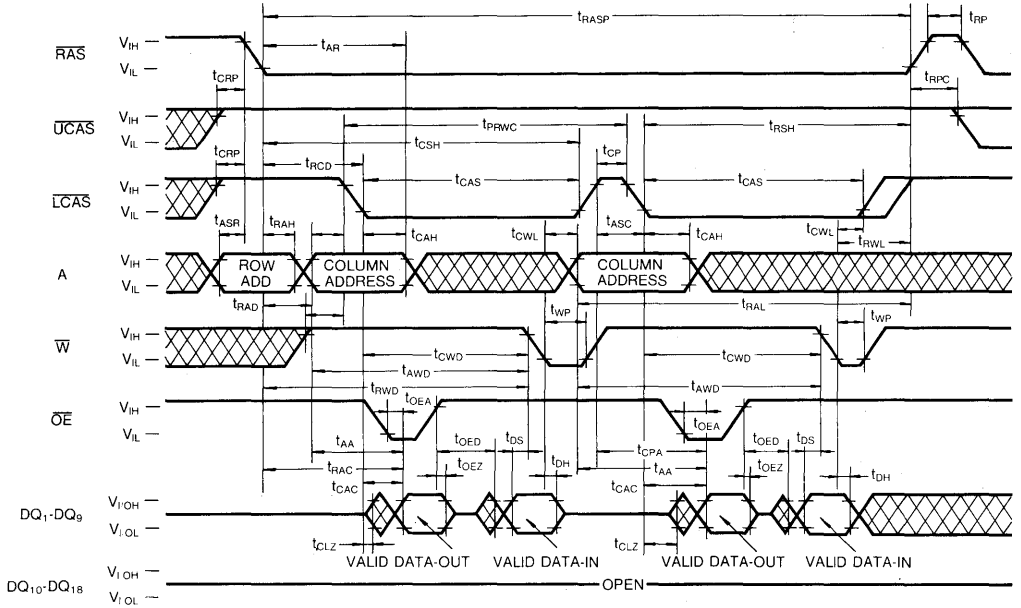


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

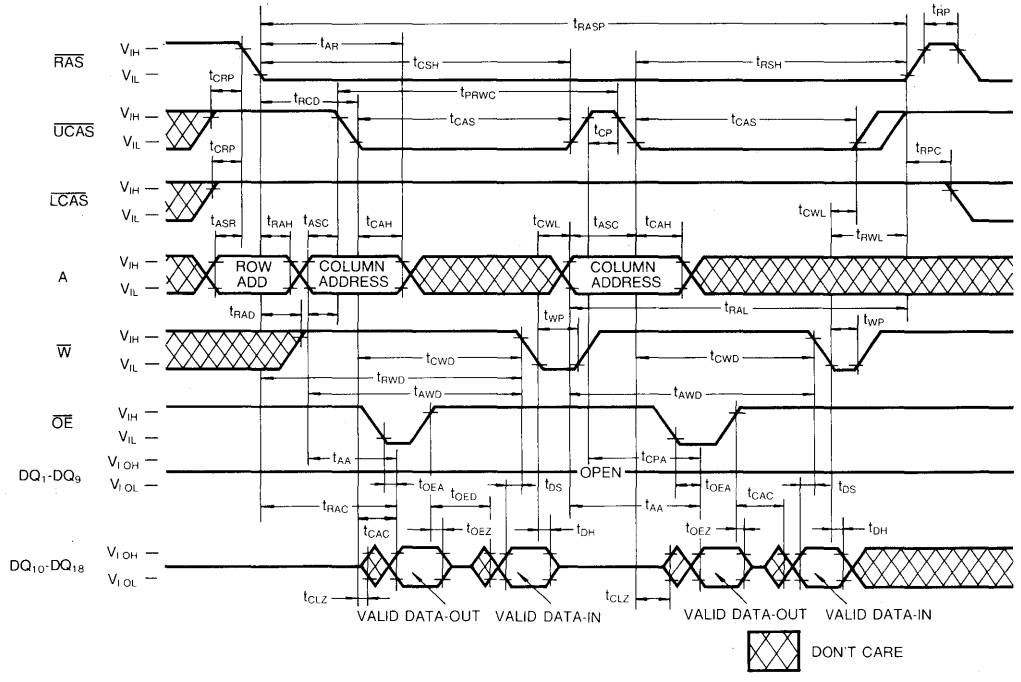


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



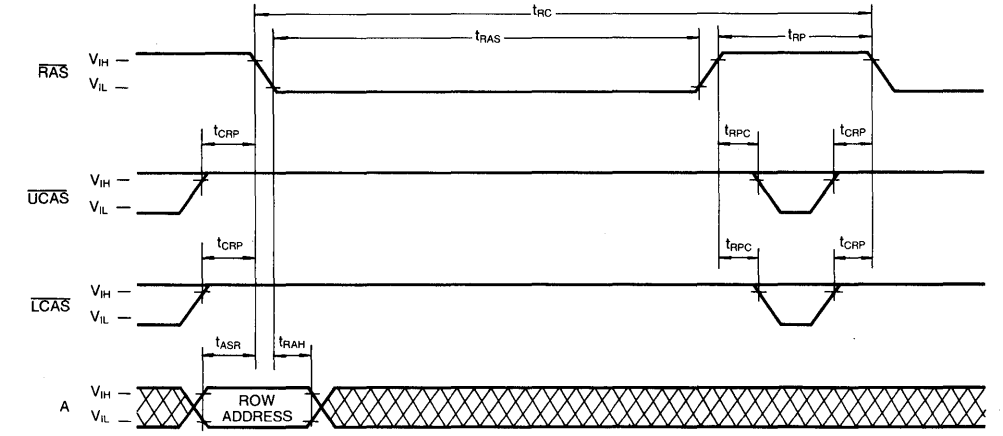
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

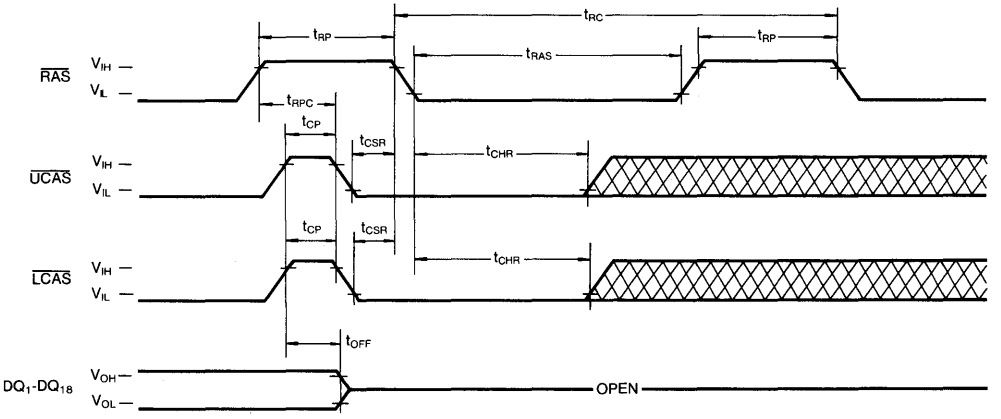
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

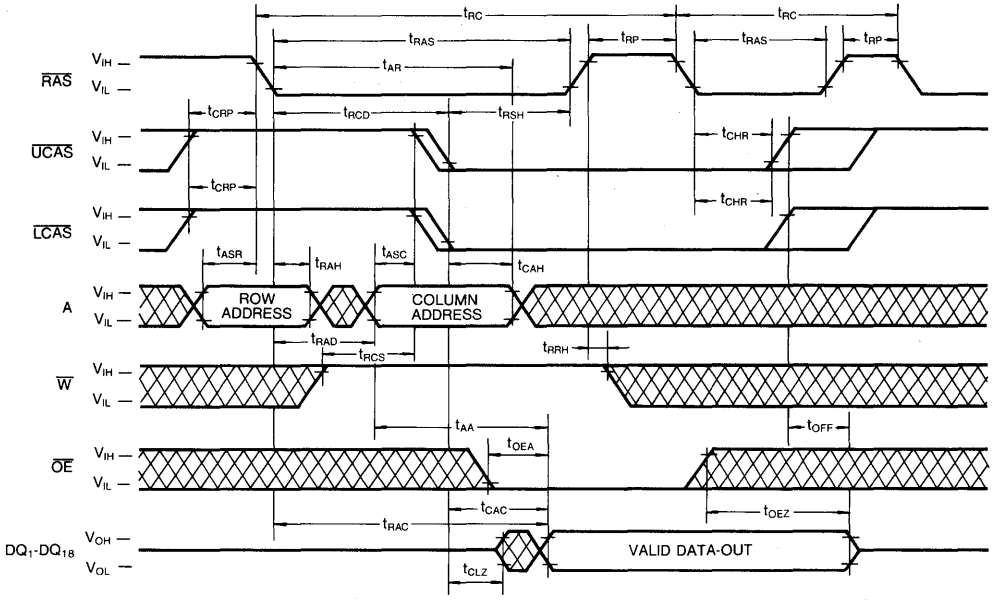
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



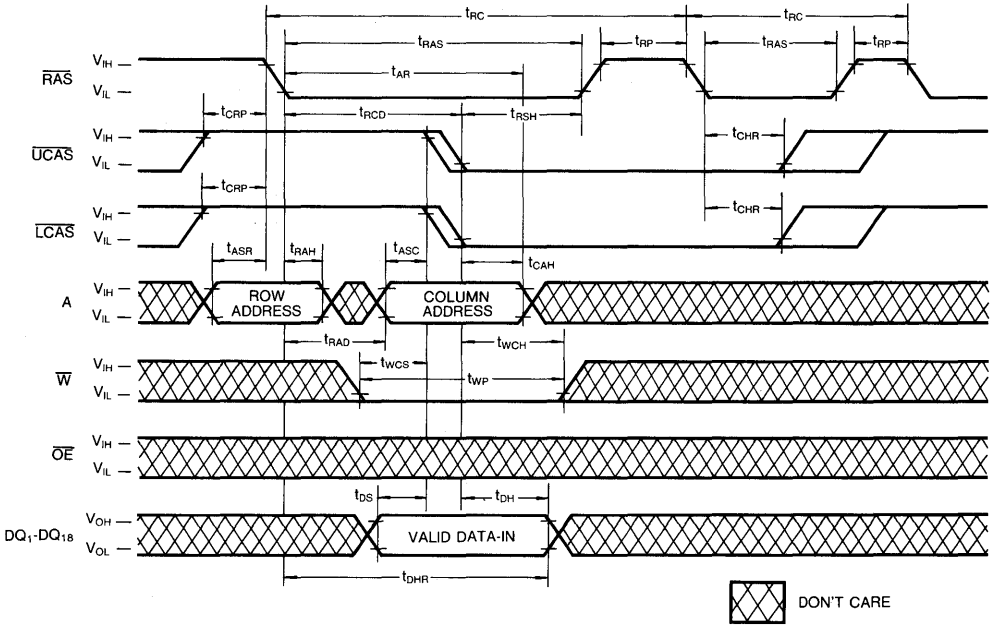
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

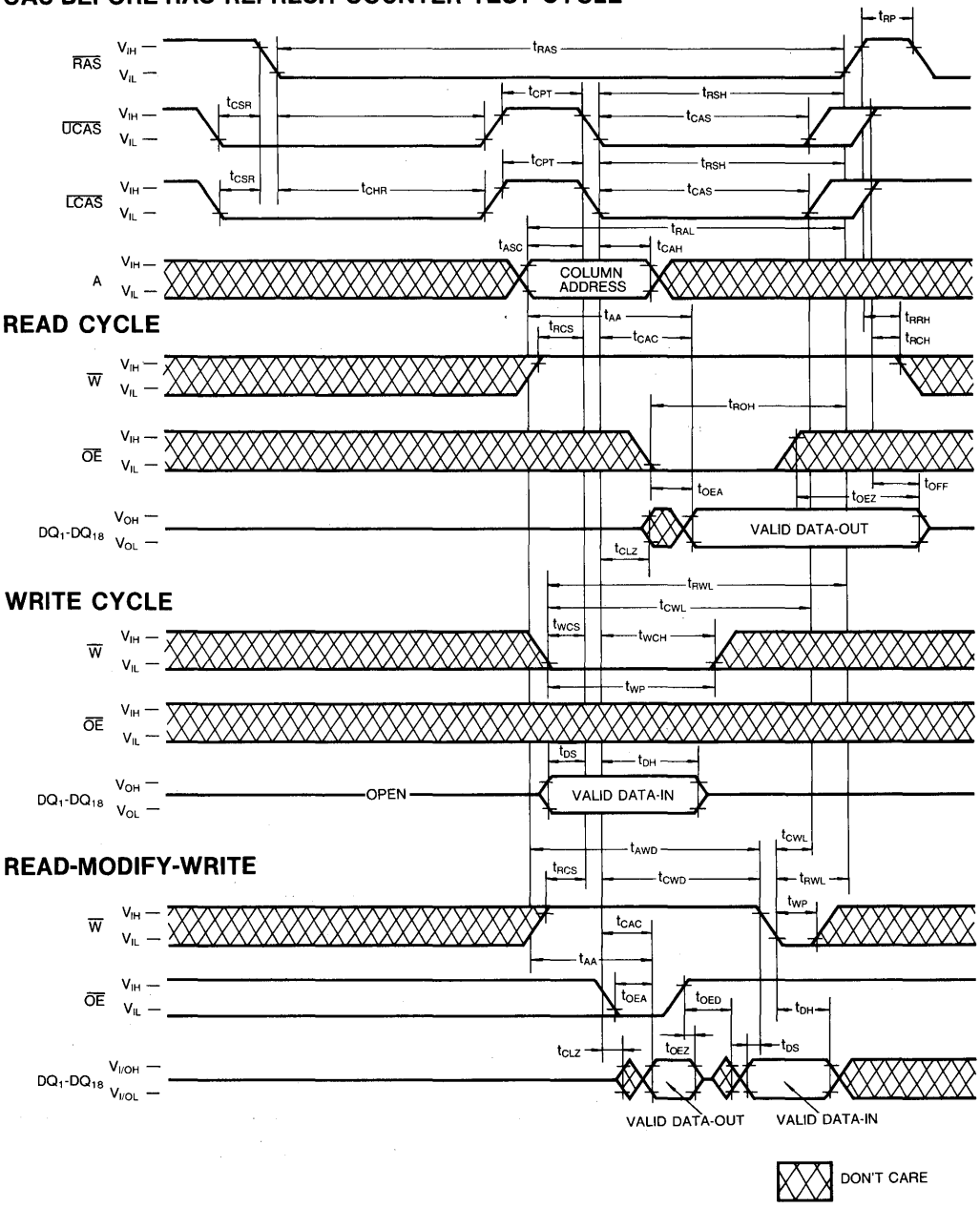


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM418C256 contains 4,718,592 memory locations arranged in 18 groups of 262,144×1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM418C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM418C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM418C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM418C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/x$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If x$\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if x$\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM418C256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or x$\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before x$\overline{CAS}$. The 18 Bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM418C256 DQ pins.

Data Output

The KM418C256 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM418C256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM418C256 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

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DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 8ms. There are several ways to accomplish this:

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM418C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM418C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-RAS refresh is the preferred method.

Fast Page Mode

The KM418C256 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

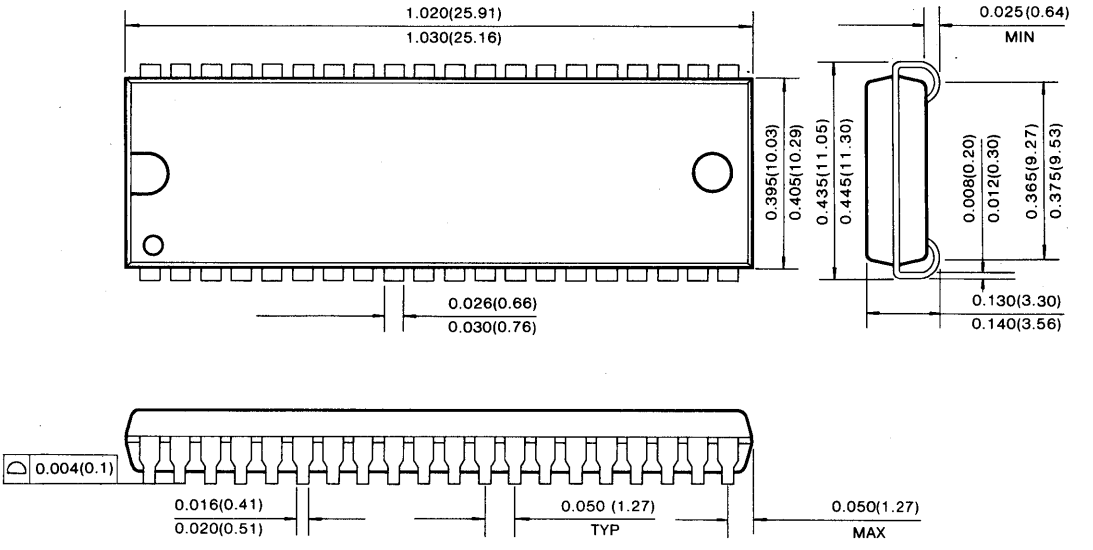
Power-Up

If $\overline{RAS}=V_{SS}$ during power-up, the KM418C256 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



512KX8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C512- 7	70ns	20ns	130ns
KM48C512- 8	80ns	20ns	150ns
KM48C512-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

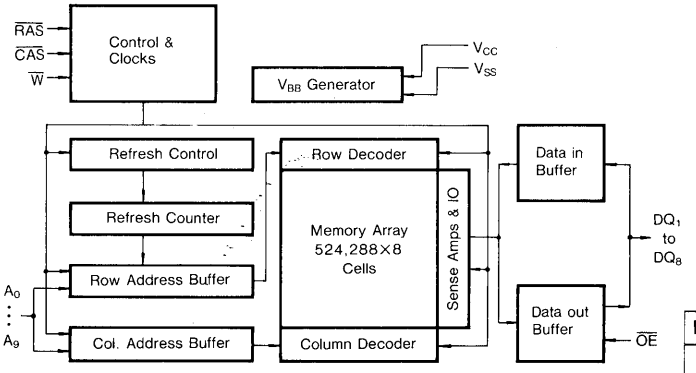
GENERAL DESCRIPTION

The Samsung KM48C512 is a CMOS high speed 524,288 bit X 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

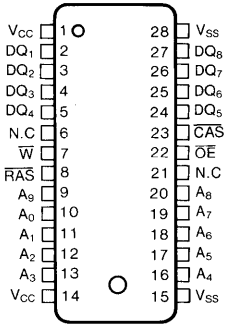
The KM48C512 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM48C512J**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	KM48C512- 7	I_{CC1}		105	mA
	KM48C512- 8			90	mA
	KM48C512-10			75	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}		2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM48C512- 7	I_{CC3}		105	mA
	KM48C512- 8			90	mA
	KM48C512-10			75	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM48C512- 7	I_{CC4}		85	mA
	KM48C512- 8			75	mA
	KM48C512-10			65	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}		1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	KM48C512- 7	I_{CC6}		105	mA
	KM48C512- 8			90	mA
	KM48C512-10			75	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} Dout=Enable)		I_{CC7}		5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is spedified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM48C512-7		KM48C512-8		KM48C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	10		10		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWI}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

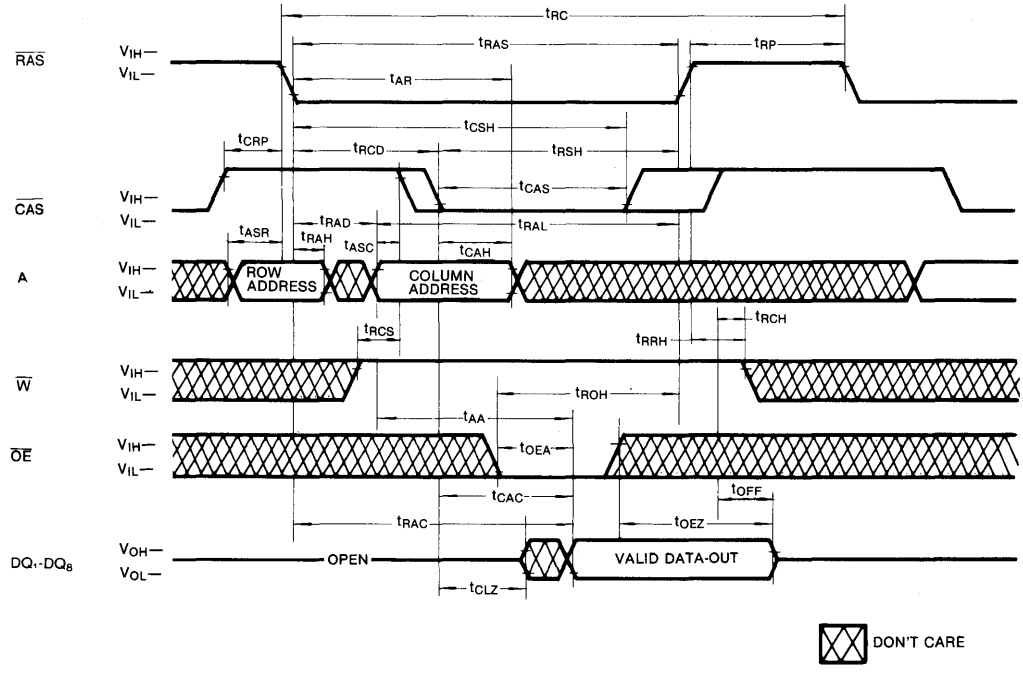
Parameter	Symbol	KM48C512-7		KM48C512-8		KM48C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		120		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

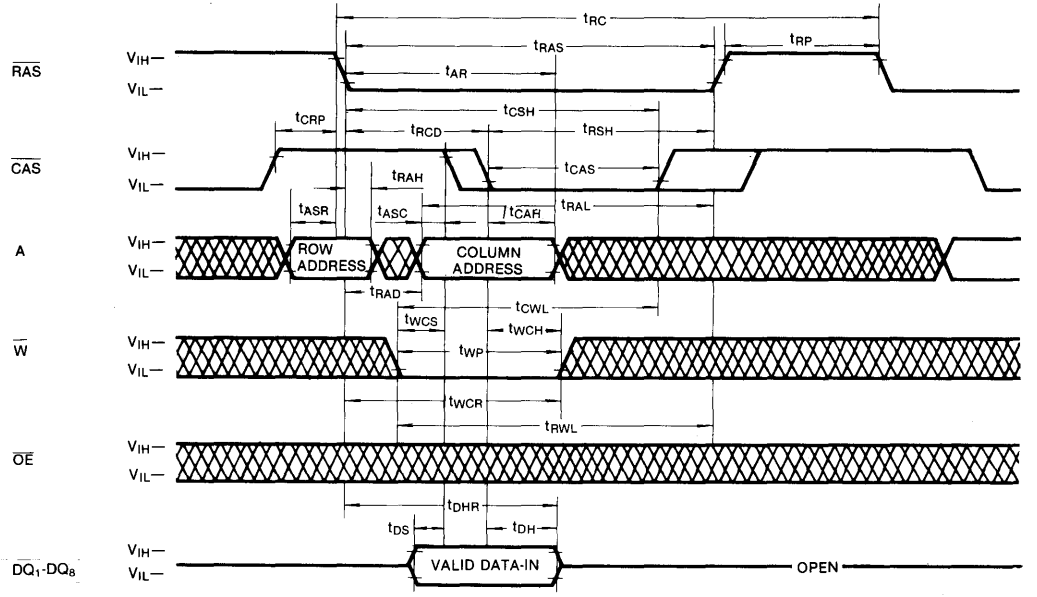
TIMING DIAGRAMS

READ CYCLE

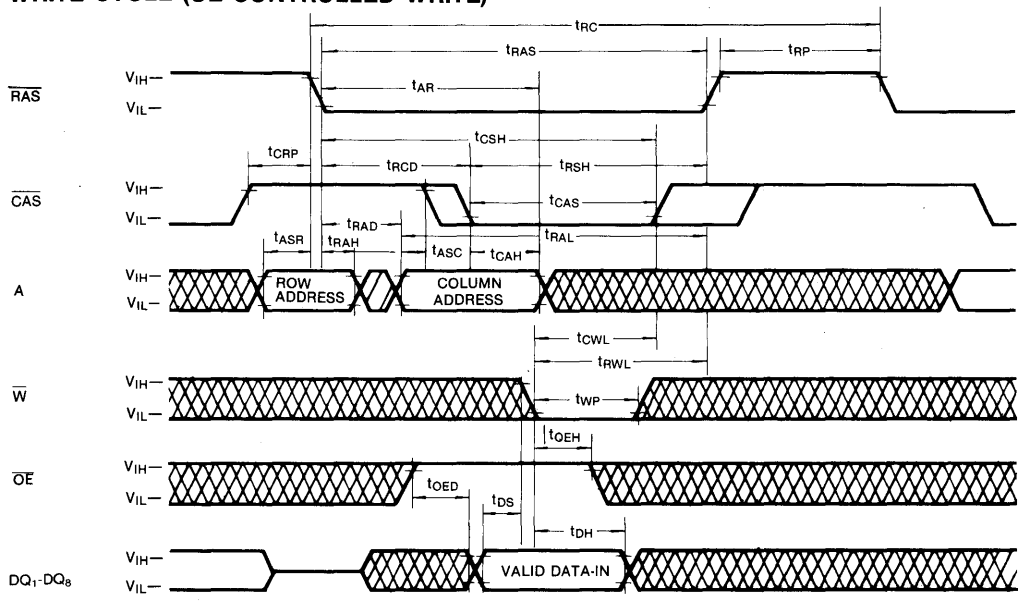


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



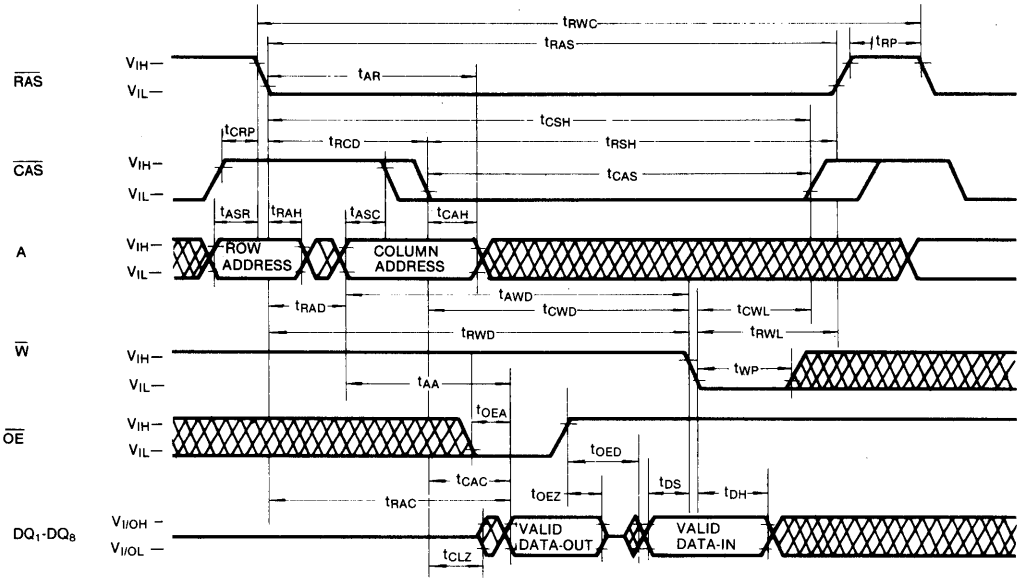
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



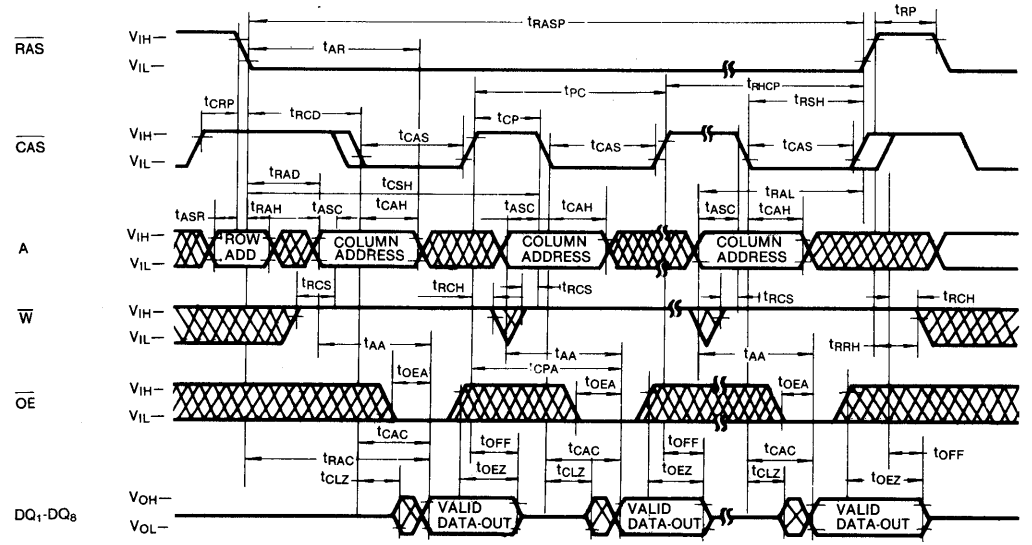
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



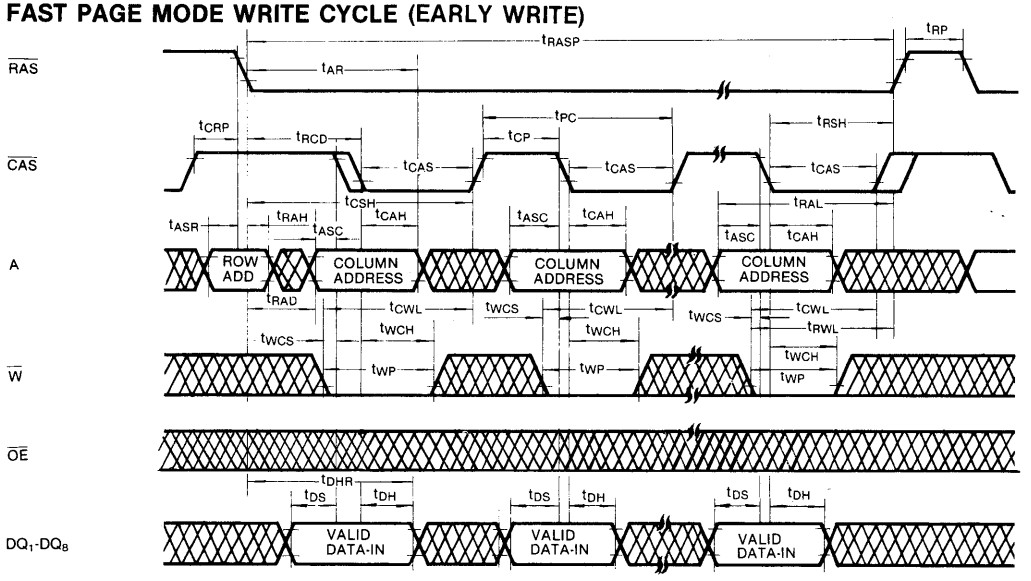
FAST PAGE MODE READ CYCLE



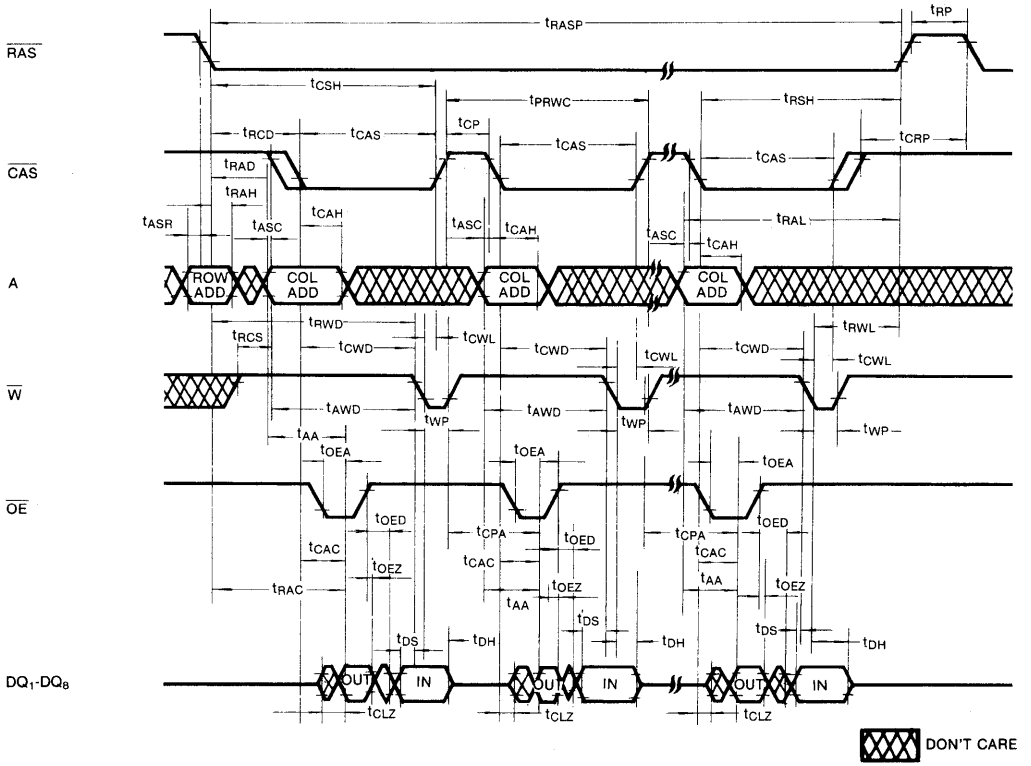
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



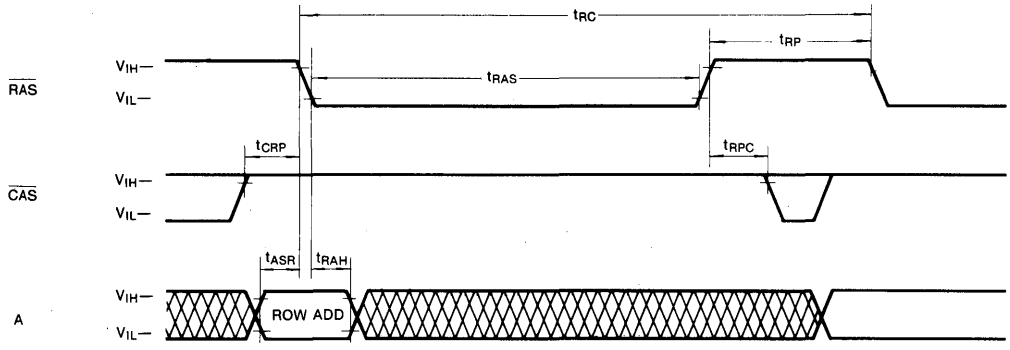
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

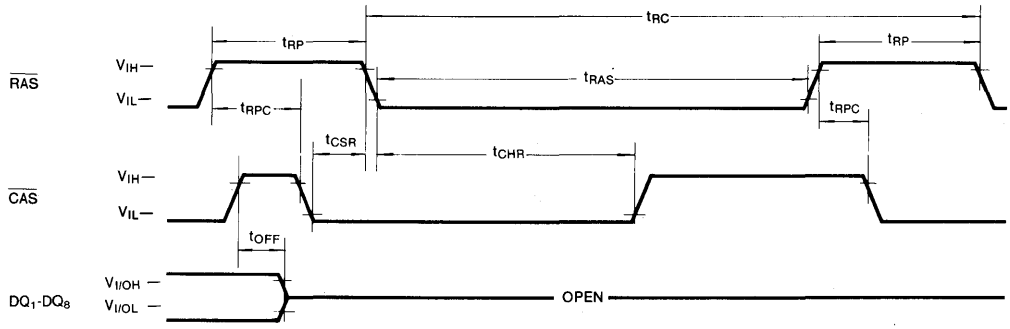
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

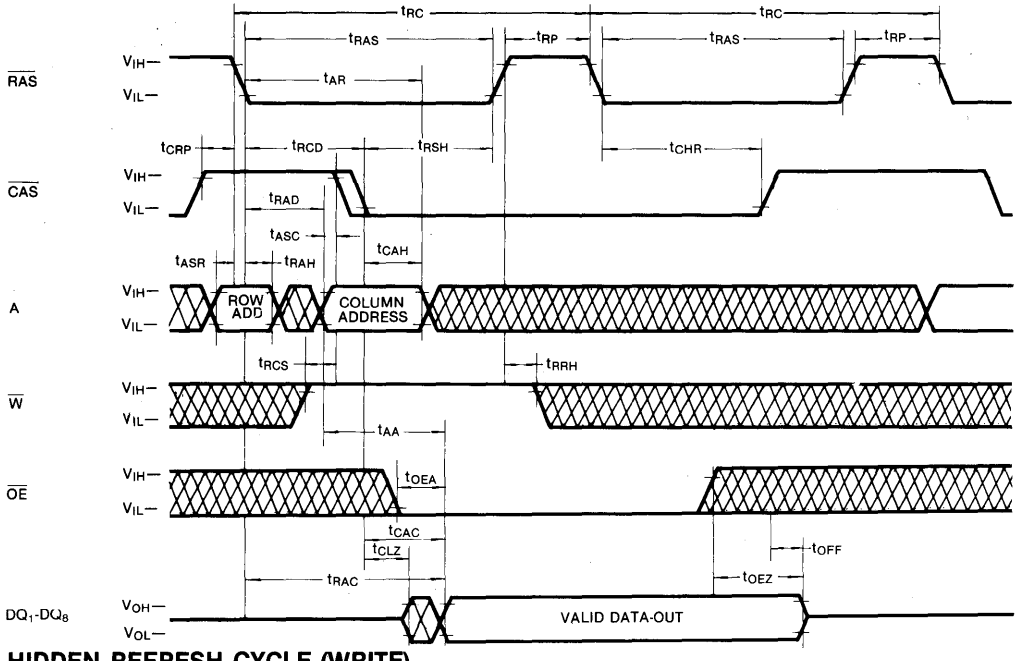
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



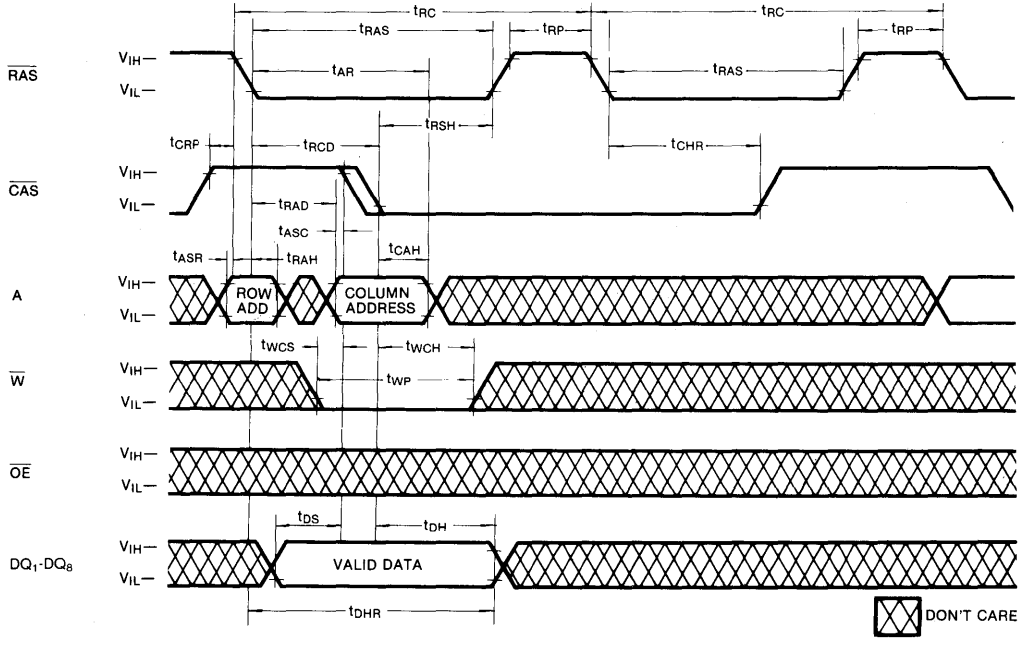
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

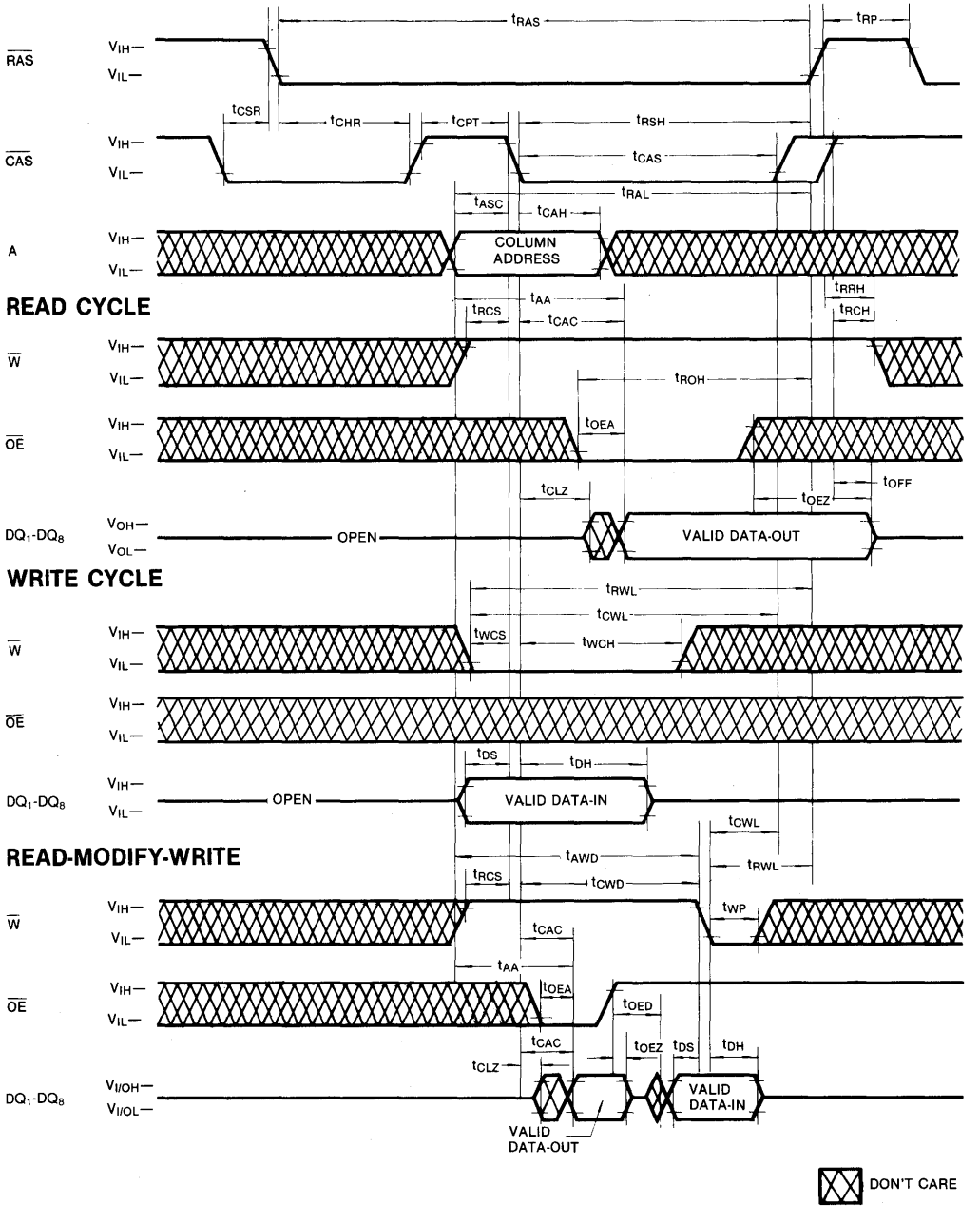


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C512 contains 4,194,304 memory locations arranged in 8 groups of 524,288×1 bit each. Twenty address bits are required to address a particular memory location. Since the KM48C512 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C512 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C512 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C512 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C512 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C512 DQ pins.

Data Output

The KM48C512 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C512 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM48C512 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 16ms. There are several ways to accomplish this:

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C512 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM48C512 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C512 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

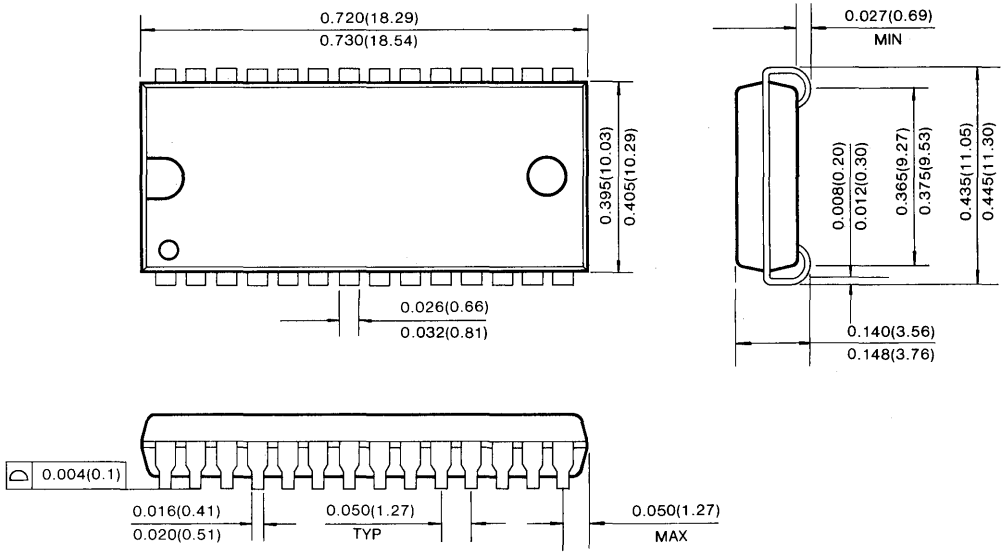
Power-Up

If $\overline{RAS}=V_{SS}$ during power-up, the KM48C512 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



512KX9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM49C512- 7	70ns	20ns	130ns
KM49C512- 8	80ns	20ns	150ns
KM49C512-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

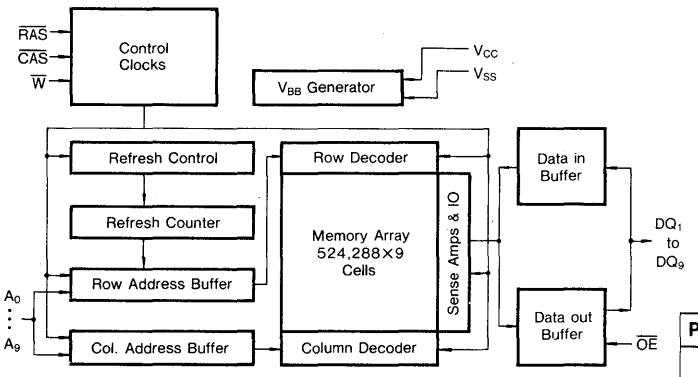
GENERAL DESCRIPTION

The Samsung KM49C512 is a CMOS high speed 524,288 bit X 9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

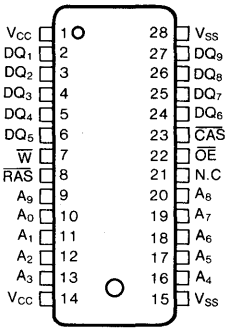
The KM49C512 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM49C512J**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-9}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	KM49C512- 7	I_{CC1}		110	mA
	KM49C512- 8			95	mA
	KM49C512-10			80	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}		2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KM49C512- 7	I_{CC3}		110	mA
	KM49C512- 8			95	mA
	KM49C512-10			80	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM49C512- 7	I_{CC4}		85	mA
	KM49C512- 8			75	mA
	KM49C512-10			65	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}		1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min)	KM49C512- 7	I_{CC5}		110	mA
	KM49C512- 8			95	mA
	KM49C512-10			80	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} Dout=Enable)		I_{CC7}		5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is spedified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_9)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM49C512-7		KM49C512-8		KM49C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	10		10		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWI}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

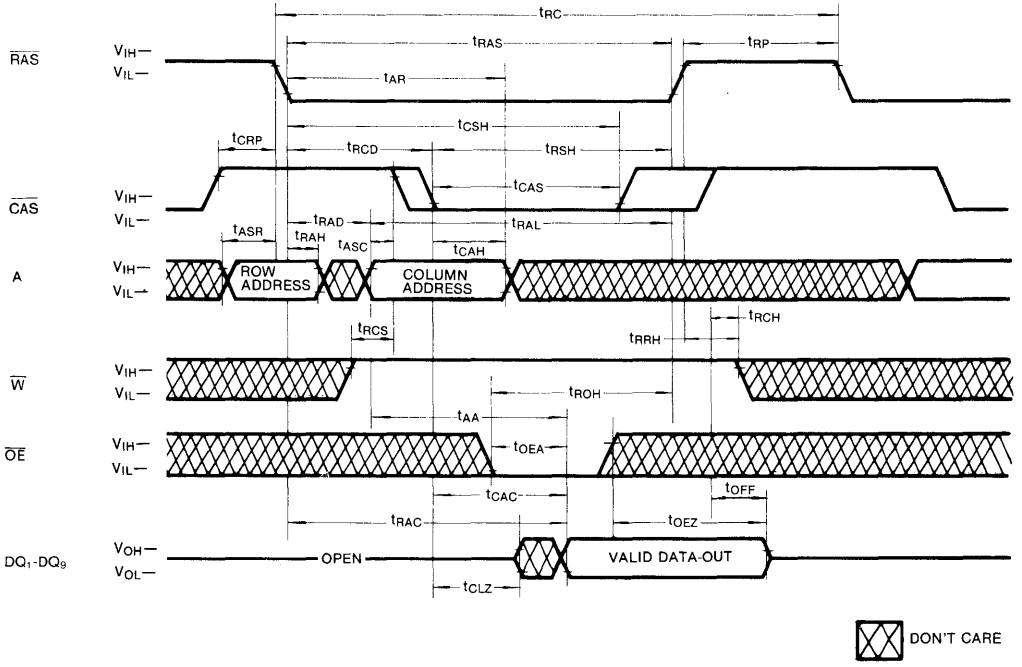
Parameter	Symbol	KM49C512-7		KM49C512-8		KM49C512-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		120		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

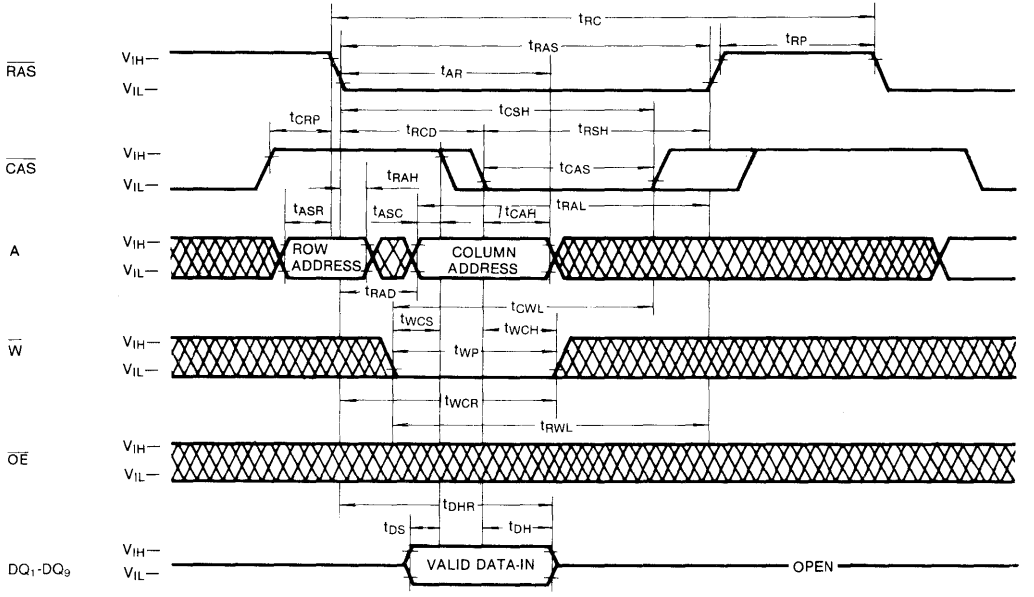
TIMING DIAGRAMS

READ CYCLE

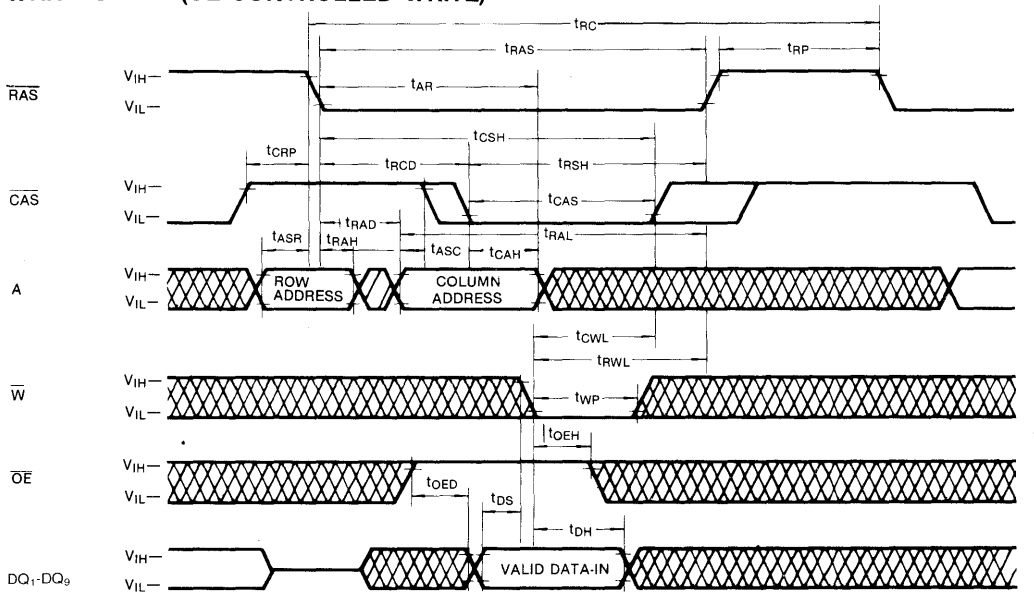


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



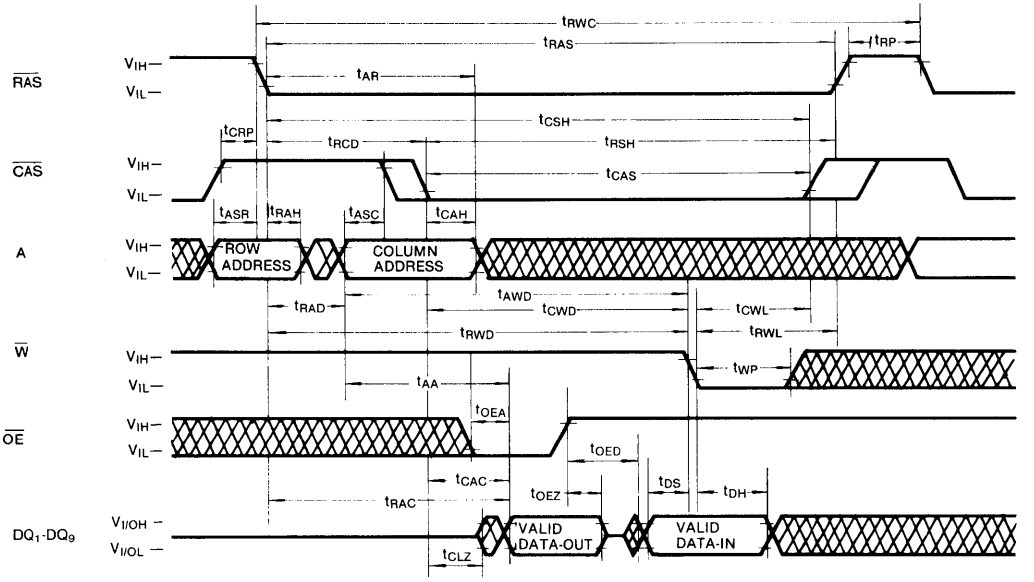
WRITE CYCLE (OE CONTROLLED WRITE)



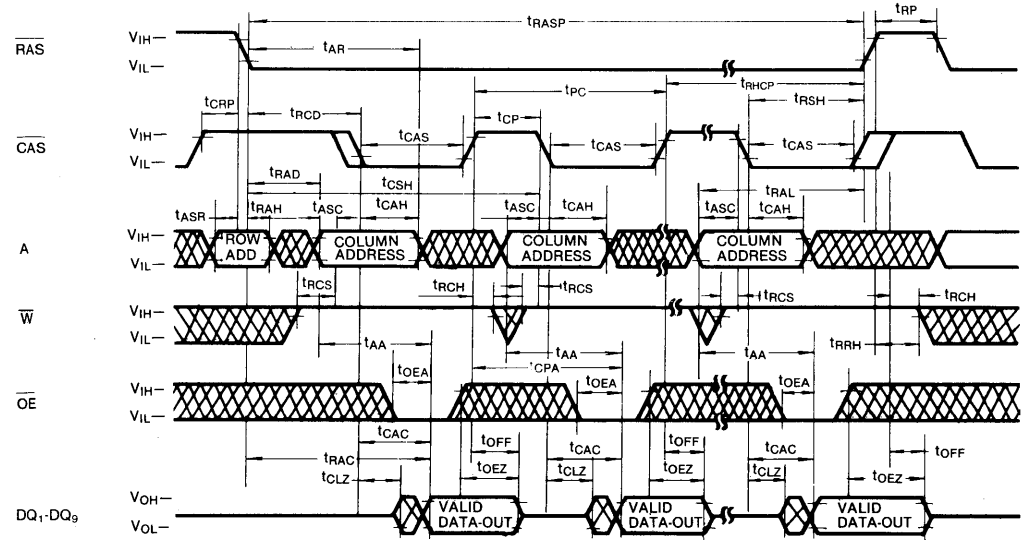
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



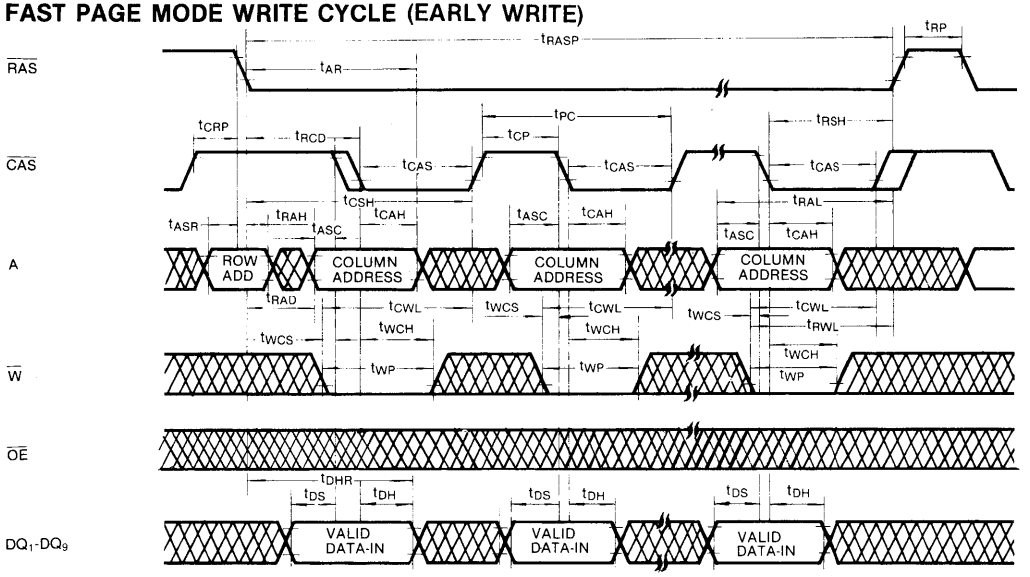
FAST PAGE MODE READ CYCLE



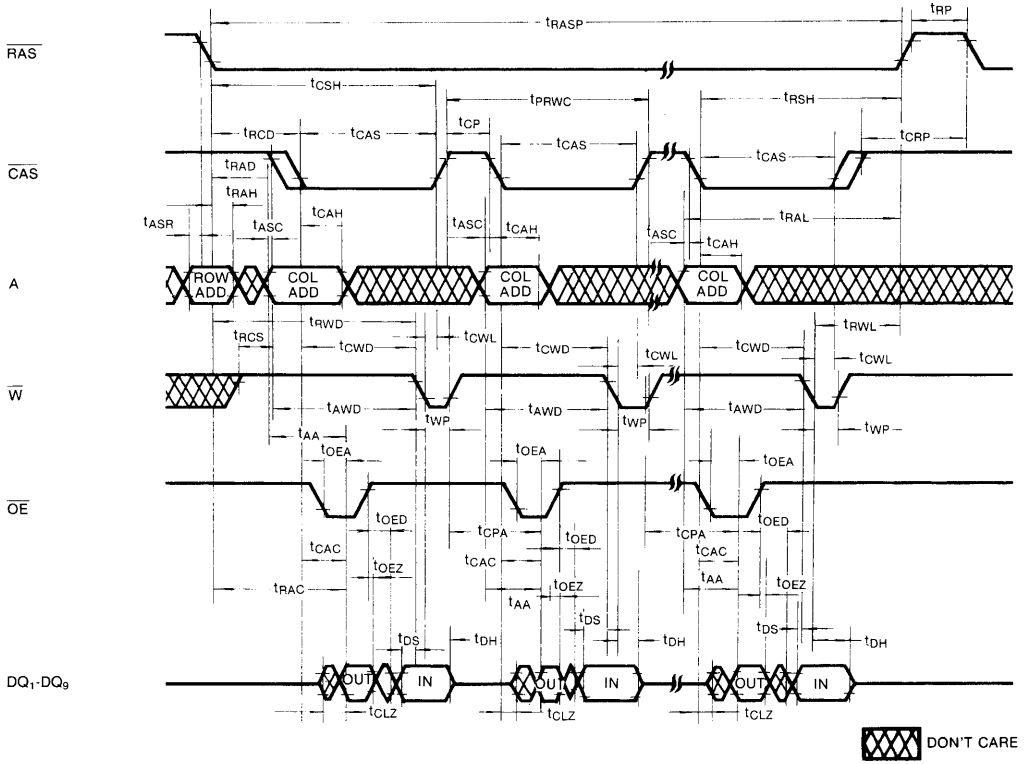
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



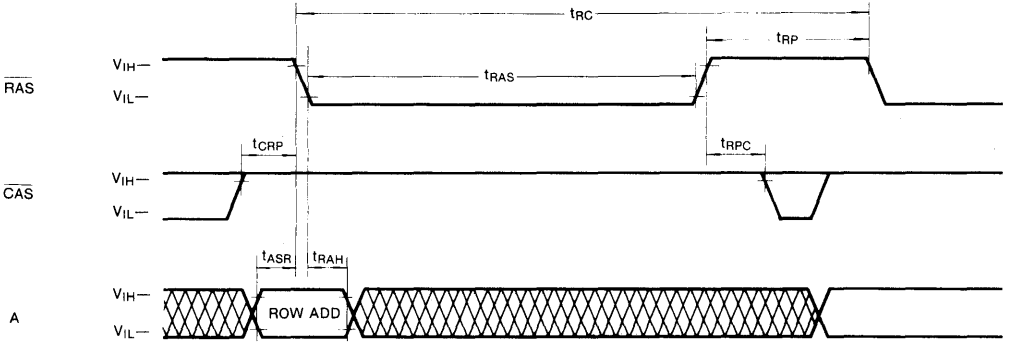
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

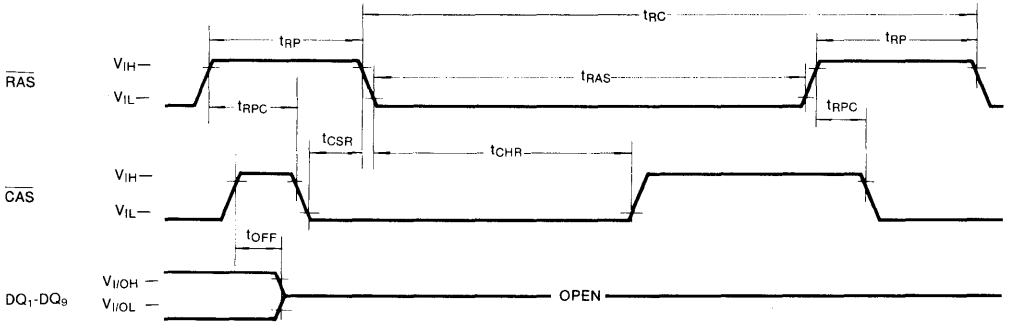
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

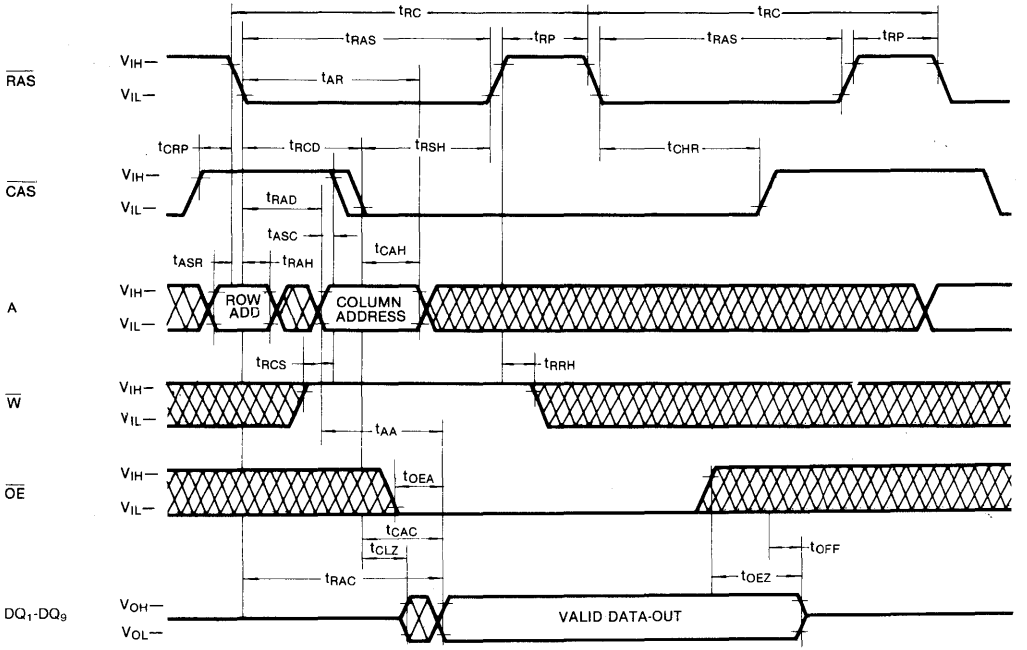
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



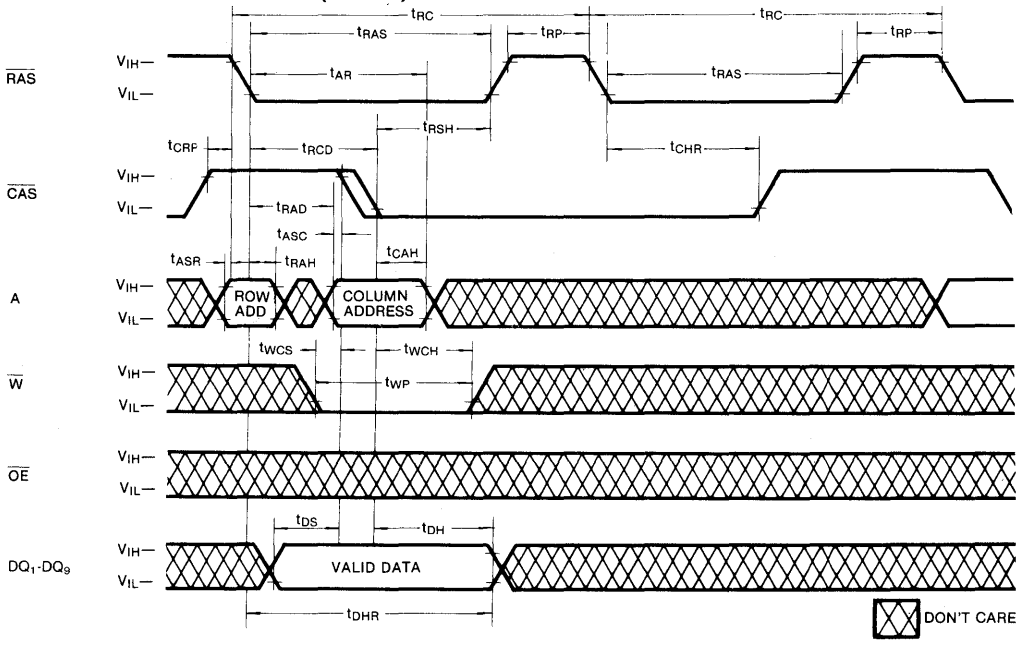
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

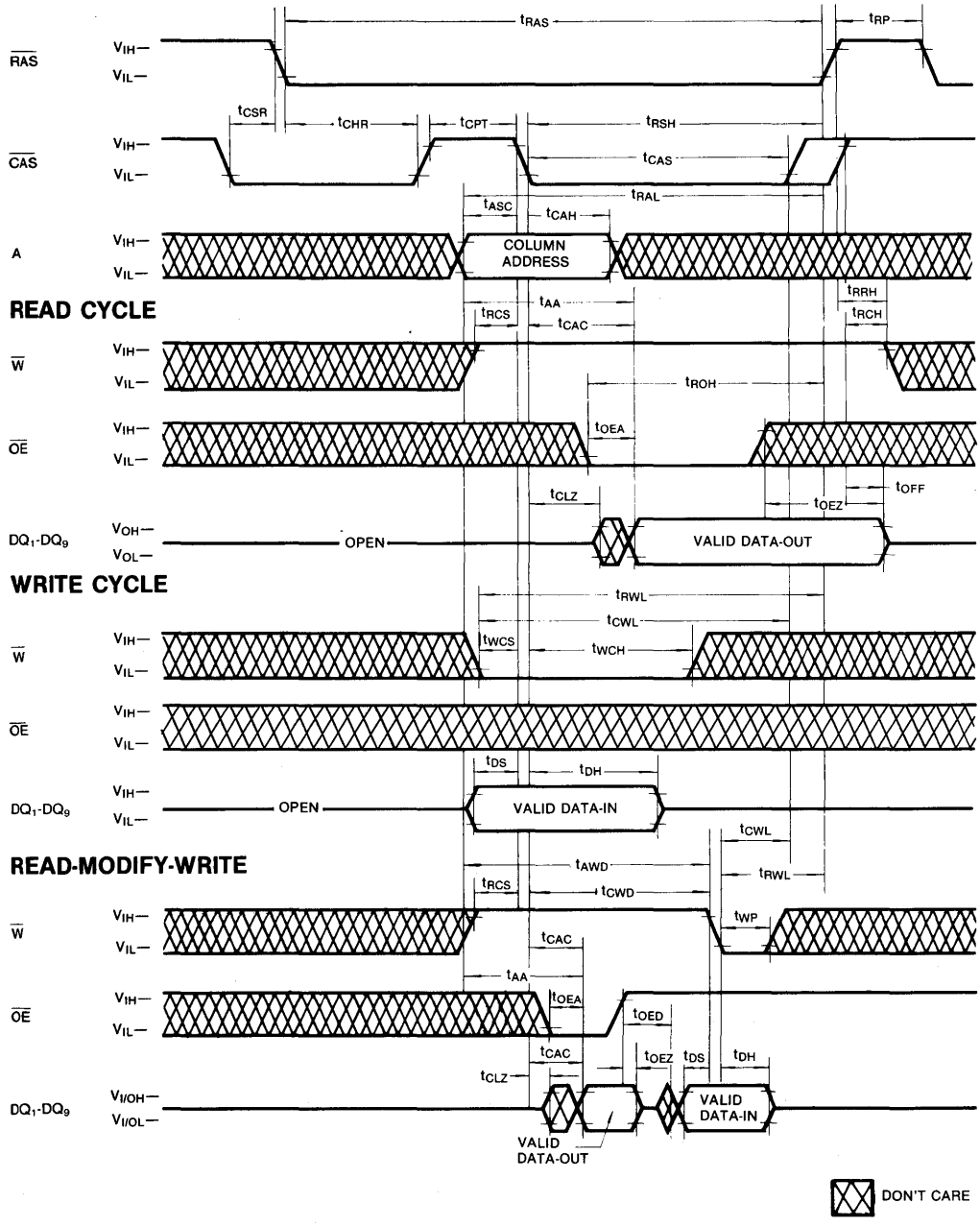


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM49C512 contains 4,718,592 memory locations arranged in 9 groups of 524,288×1 bit each. Twenty address bits are required to address a particular memory location. Since the KM49C512 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM49C512 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM49C512 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM49C512 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM49C512 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 9-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM49C512 DQ pins.

Data Output

The KM49C512 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM49C512 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM49C512 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 16ms. There are several ways to accomplish this:

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM49C512 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM49C512 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM49C512 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

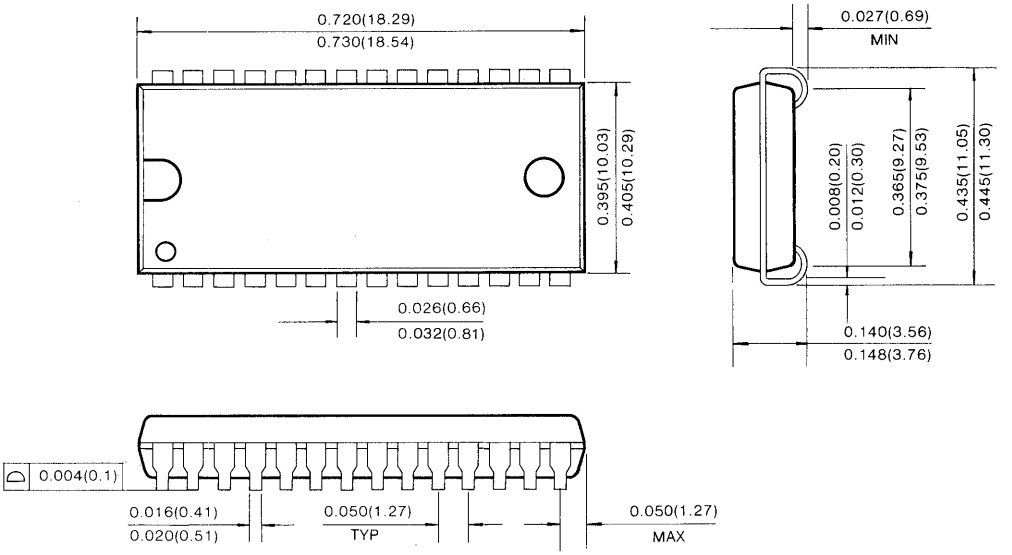
Power-Up

If $\overline{RAS}=V_{SS}$ during power-up, the KM49C512 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

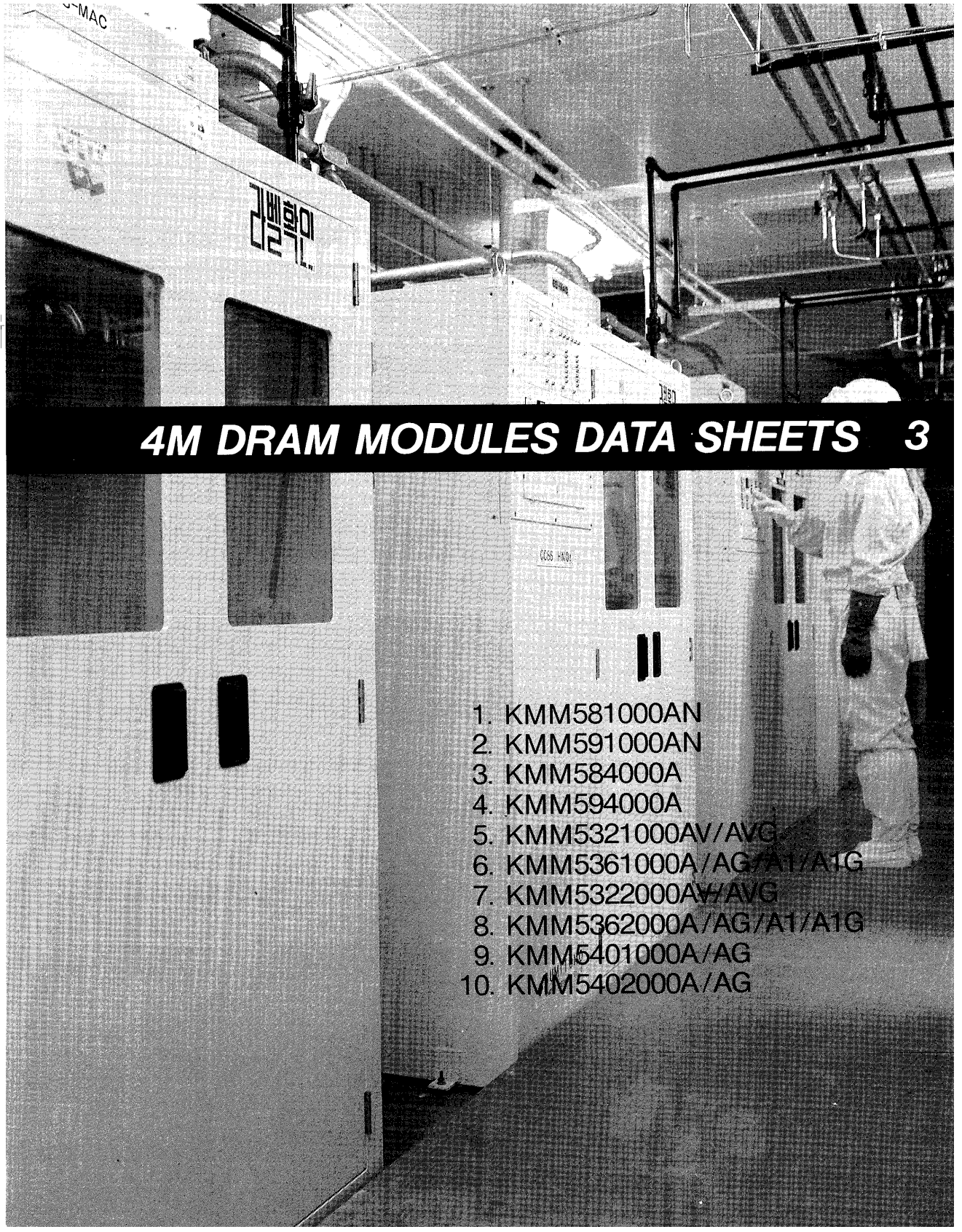
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



NOTES



4M DRAM MODULES DATA SHEETS 3

1. KMM581000AN
2. KMM591000AN
3. KMM584000A
4. KMM594000A
5. KMM5321000AV/AVG
6. KMM5361000A/AG/A1/A1G
7. KMM5322000AV/AVG
8. KMM5362000A/AG/A1/A1G
9. KMM5401000A/AG
10. KMM5402000A/AG

1M×8 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM581000AN- 7	70ns	20ns	130ns
KMM581000AN- 8	80ns	20ns	150ns
KMM581000AN-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

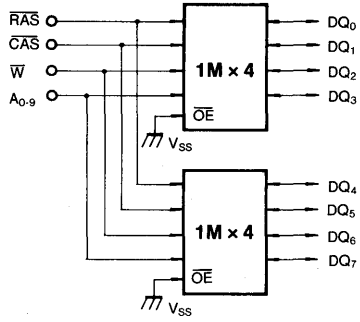
GENERAL DESCRIPTION

The Samsung KMM581000AN is a 1M bit × 8 Dynamic RAM high density memory module. The Samsung KMM581000AN consist of two 4M bit DRAMs (KM44C1000AJ - 1M×4) in 20-pin SOJ package mounted on a 30-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted for each DRAM.

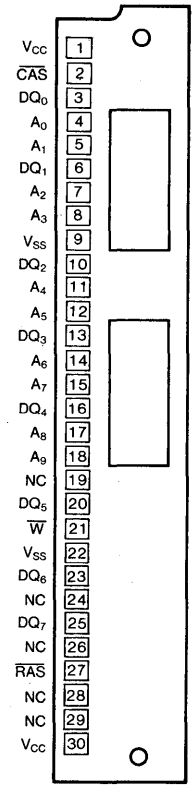
The KMM581000AN is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{0-7}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM581000AN- 7	I_{CC1}	—	210	mA
	KMM581000AN- 8		—	190	mA
	KMM581000AN-10		—	170	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	4	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM581000AN- 7	I_{CC3}	—	210	mA
	KMM581000AN- 8		—	190	mA
	KMM581000AN-10		—	170	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM581000AN- 7	I_{CC4}	—	160	mA
	KMM581000AN- 8		—	140	mA
	KMM581000AN-10		—	120	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	2	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM581000AN- 7	I_{CC6}	—	210	mA
	KMM581000AN- 8		—	190	mA
	KMM581000AN-10		—	170	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−20	20	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN1}	—	25	pF
Input/Output Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM581000AN-7		KMM581000AN-8		KMM581000AN-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6

AC CHARACTERISTICS (Continued)

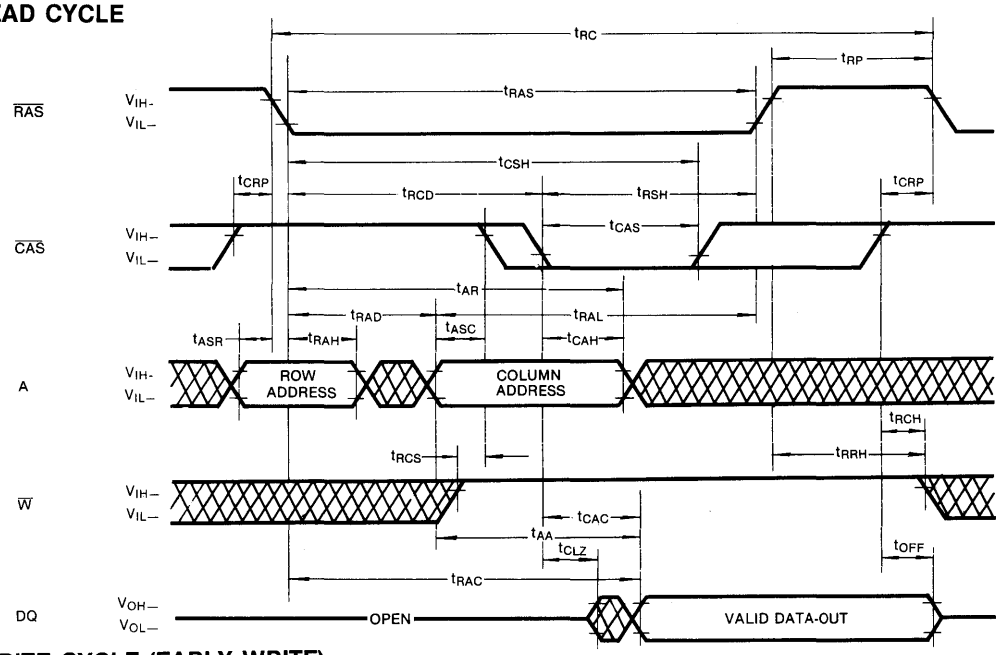
Standard Operation	Symbol	KMM581000AN-7		KMM581000AN-8		KMM581000AN-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	45		45		55		ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

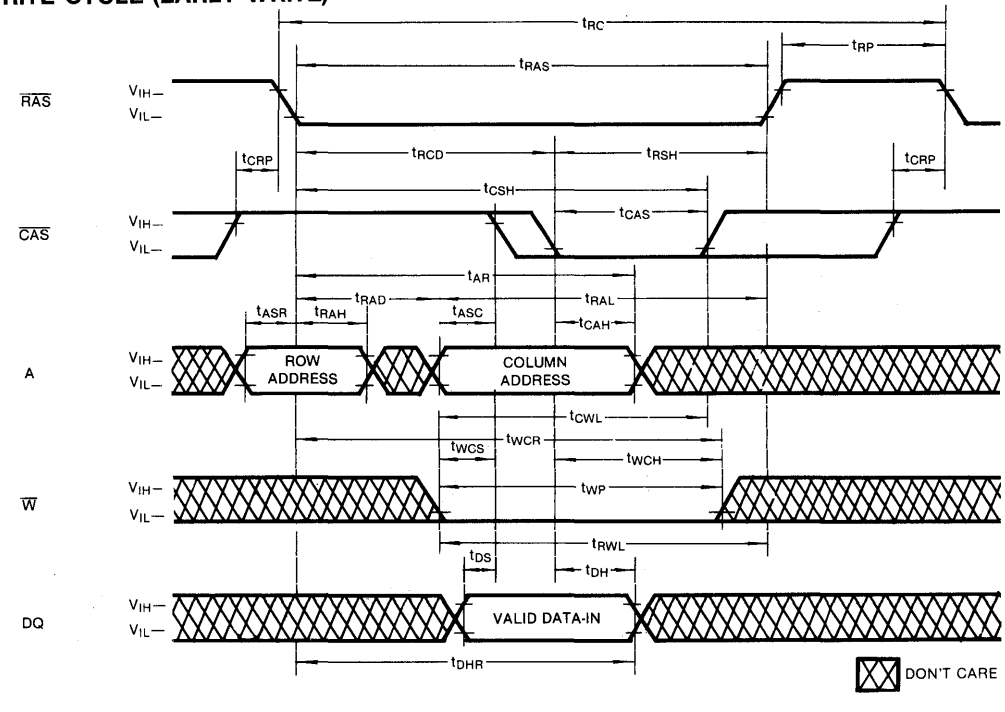
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

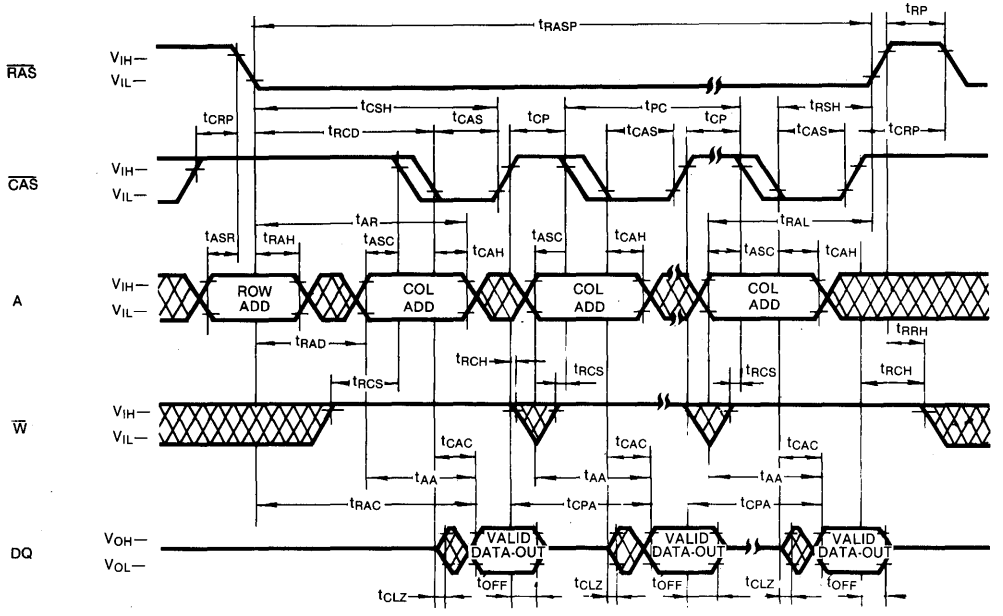


WRITE CYCLE (EARLY WRITE)

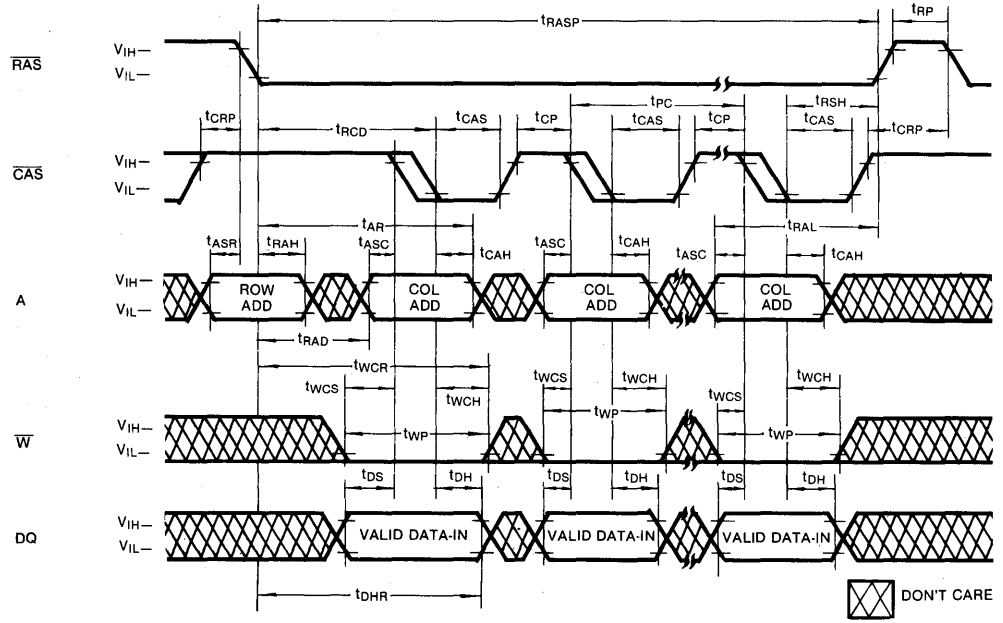


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



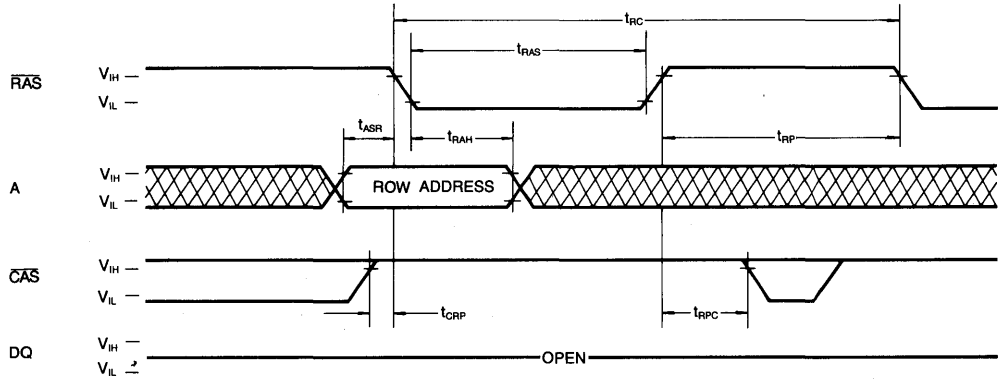
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

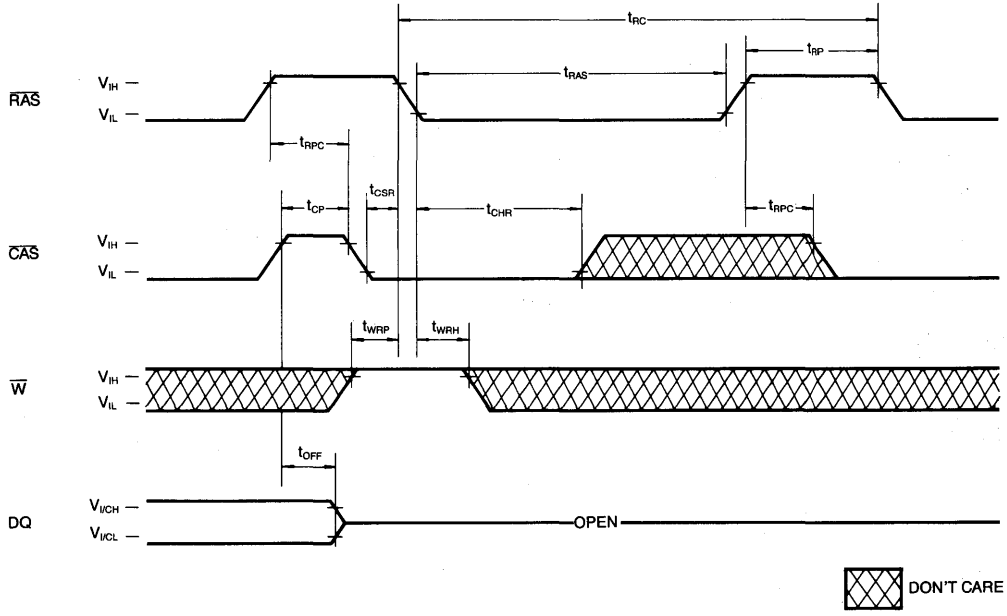
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



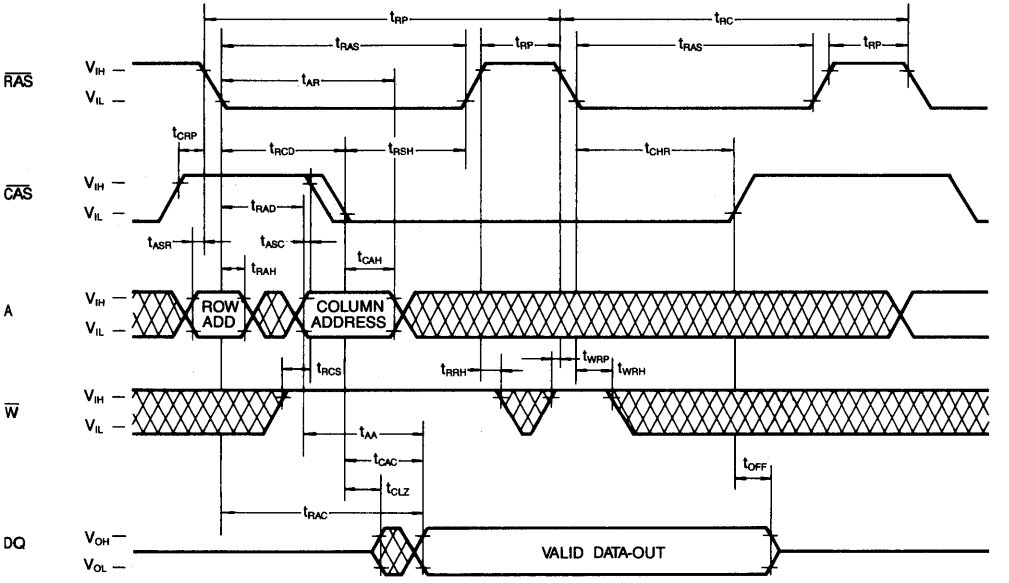
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

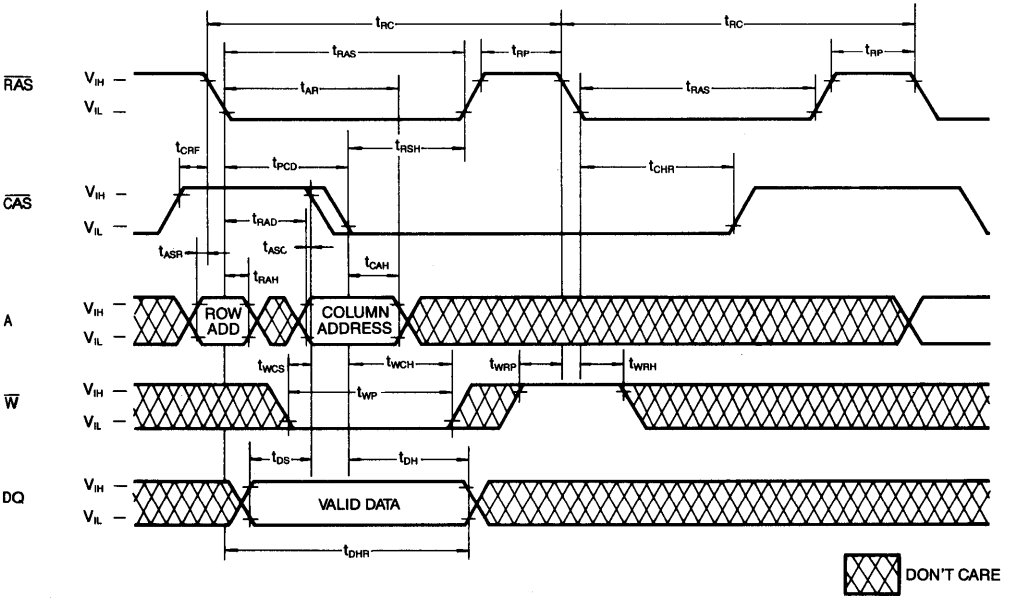


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

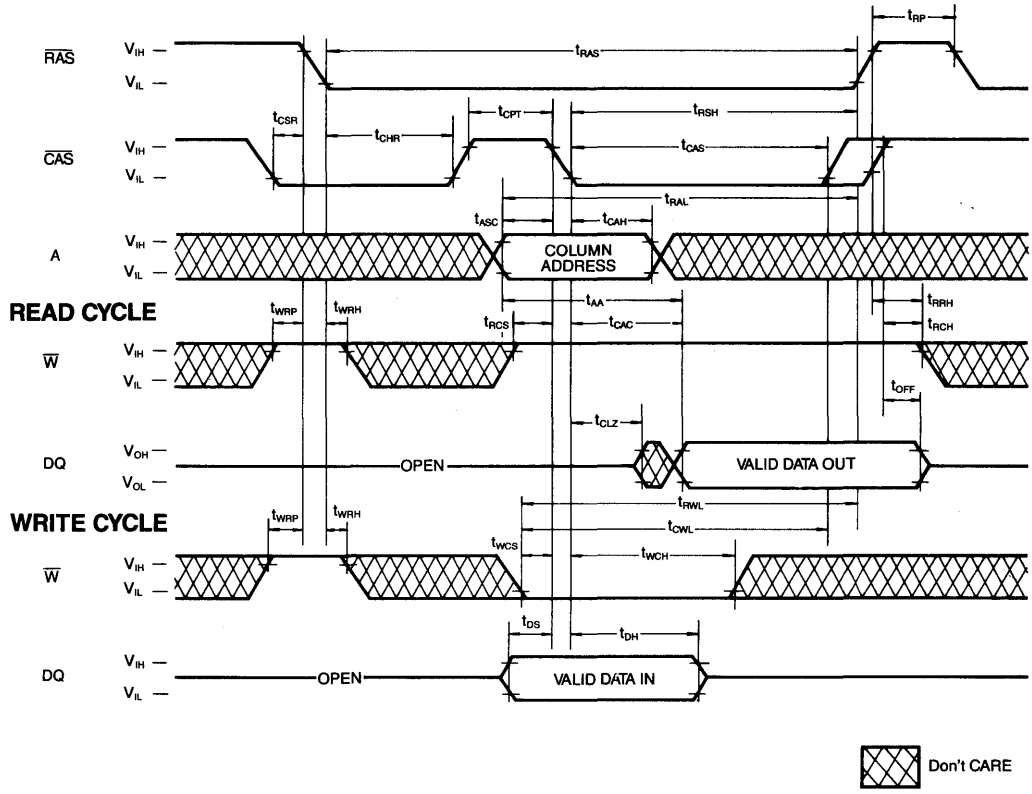


HIDDEN REFRESH CYCLE (WRITE)



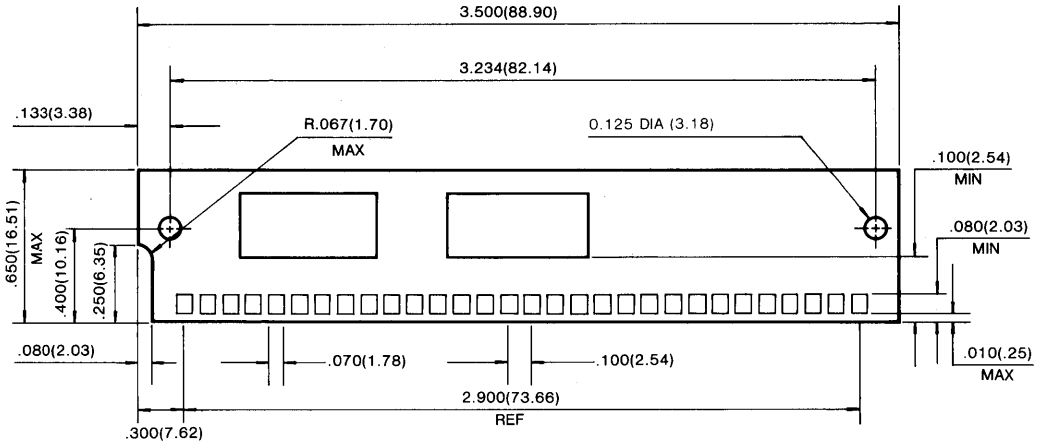
TIMING DIAGRAMS (Continued)

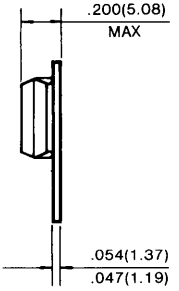
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSIONS

Units: Inches (millimeters)





Tolerances: ±.005(.13) unless otherwise specified

1MX9 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM591000AN- 7	70ns	20ns	130ns
KMM591000AN- 8	80ns	20ns	150ns
KMM591000AN-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

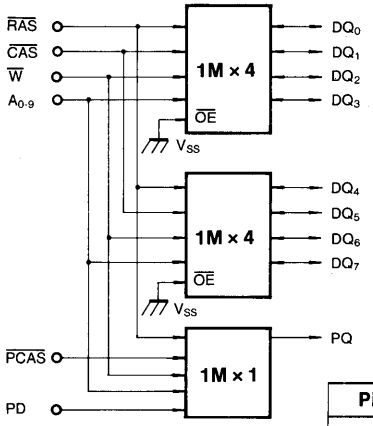
GENERAL DESCRIPTION

The Samsung KMM591000AN is a 1M bit × 9 Dynamic RAM high density memory module. The Samsung KMM591000AN consist of two 4M bit DRAMs (KM44C1000AJ - 1M×4) in 20-pin SOJ package and 1M bit DRAM (KM41C1000BJ - 1M×1) in 20-pin SOJ package mounted on a 30-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted for each DRAM.

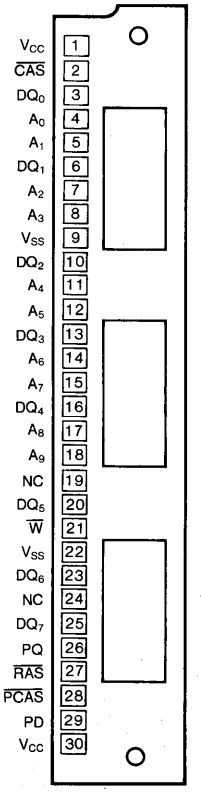
The KMM591000AN is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{0-7}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	CAS for Parity
PD	Data In for Parity
PQ	Data Out for Parity
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM591000AN- 7	I_{CC1}	—	290	mA
	KMM591000AN- 8		—	260	mA
	KMM591000AN-10		—	230	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	6	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM591000AN- 7	I_{CC3}	—	290	mA
	KMM591000AN- 8		—	260	mA
	KMM591000AN-10		—	230	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM591000AN- 7	I_{CC4}	—	220	mA
	KMM591000AN- 8		—	190	mA
	KMM591000AN-10		—	160	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	3	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM591000AN- 7	I_{CC6}	—	290	mA
	KMM591000AN- 8		—	260	mA
	KMM591000AN-10		—	230	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−30	30	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN1}	—	25	pF
Input Capacitance (PD, $\overline{PCAS}$)	C_{IN2}	—	10	pF
Input/Output Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF
Output Capacitance (PQ)	C_Q	—	10	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM591000AN-7		KMM591000AN-8		KMM591000AN-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS (Continued)

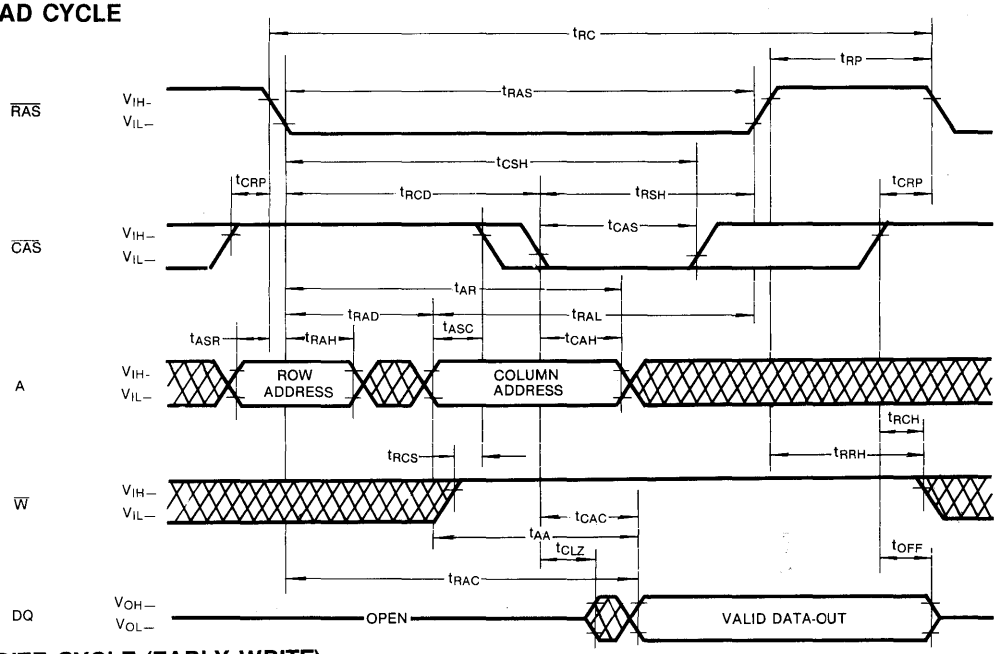
Standard Operation	Symbol	KMM591000AN-7		KMM591000AN-8		KMM591000AN-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

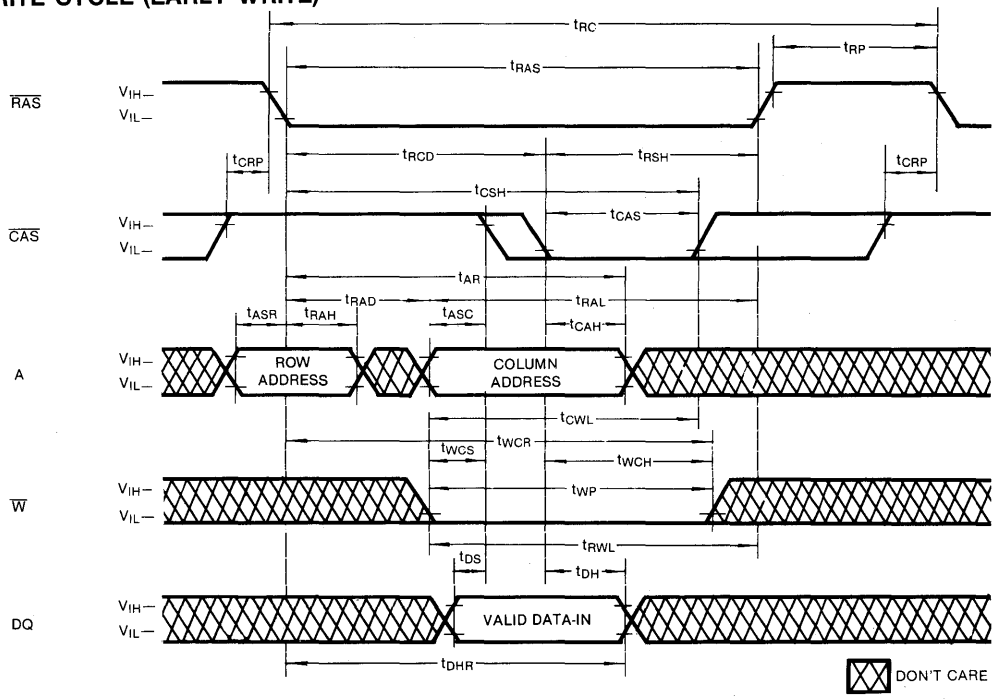
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

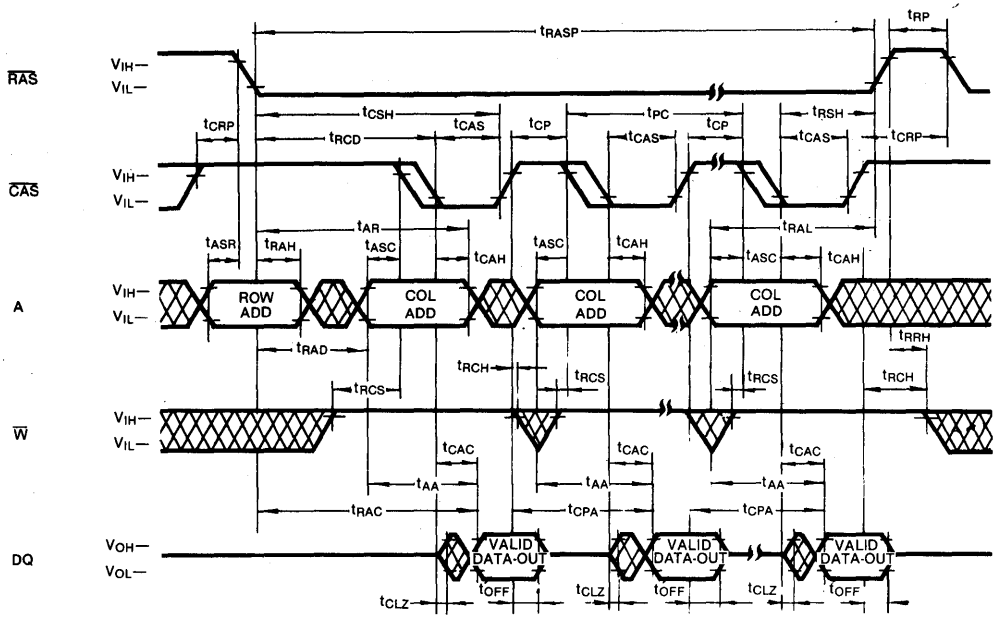


WRITE CYCLE (EARLY WRITE)

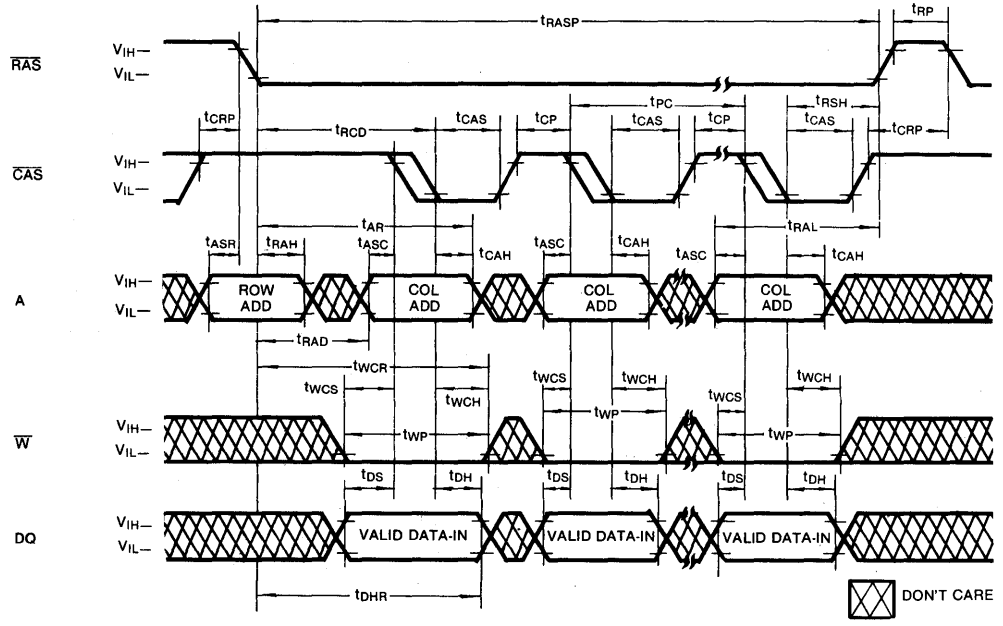


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



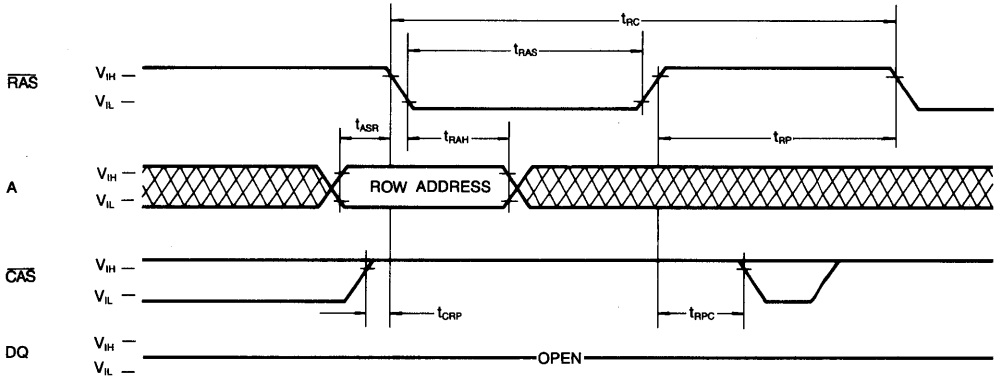
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

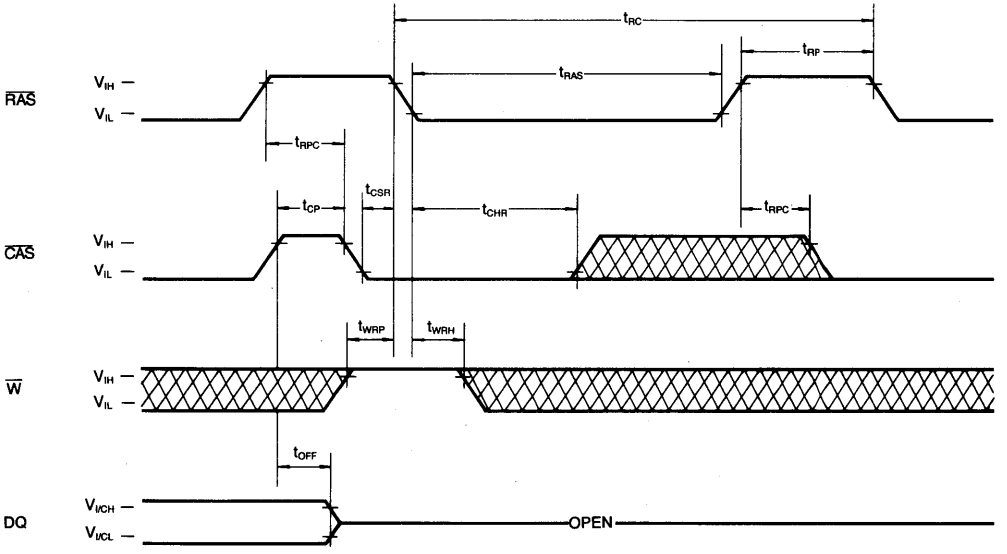
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



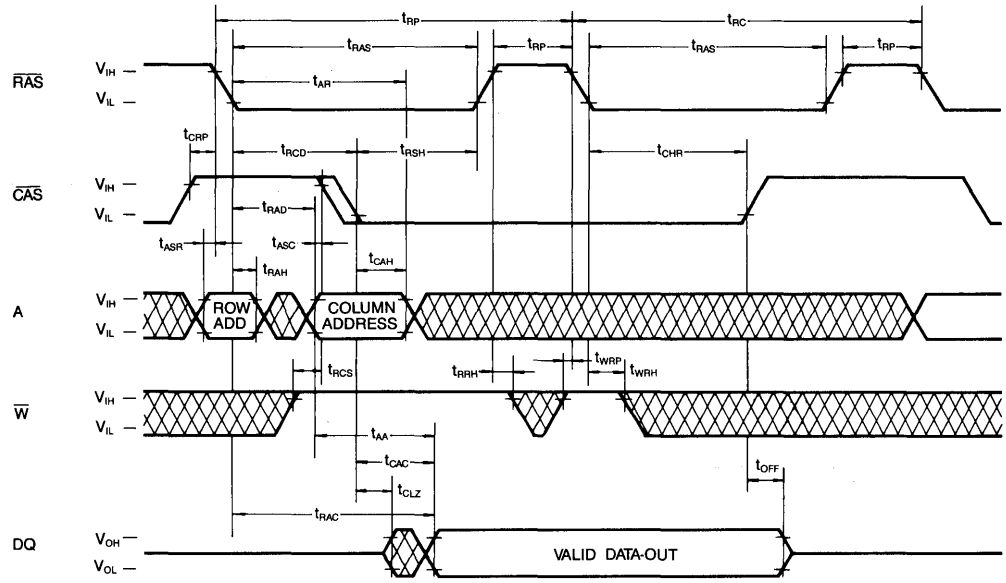
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

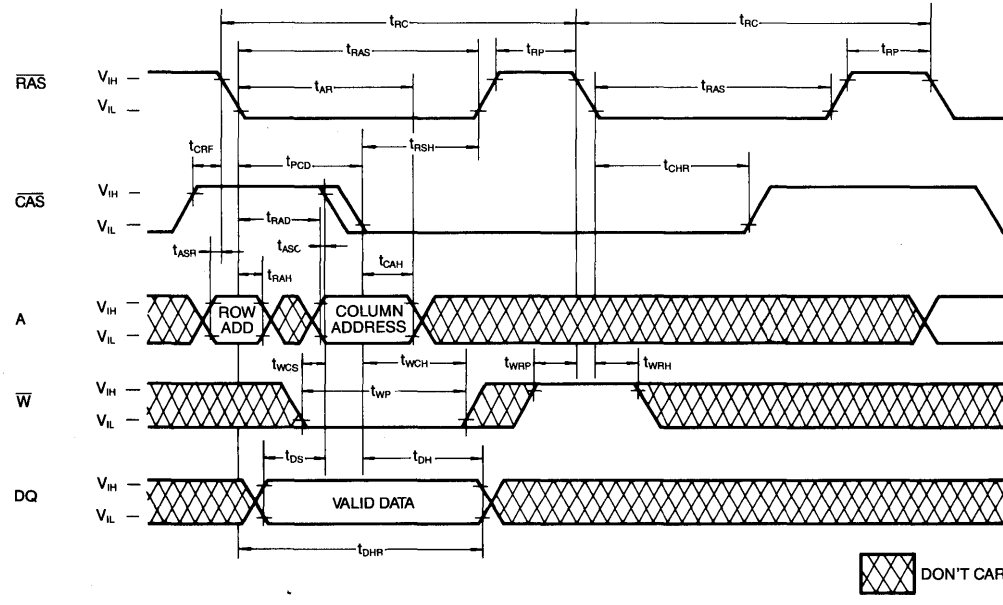


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

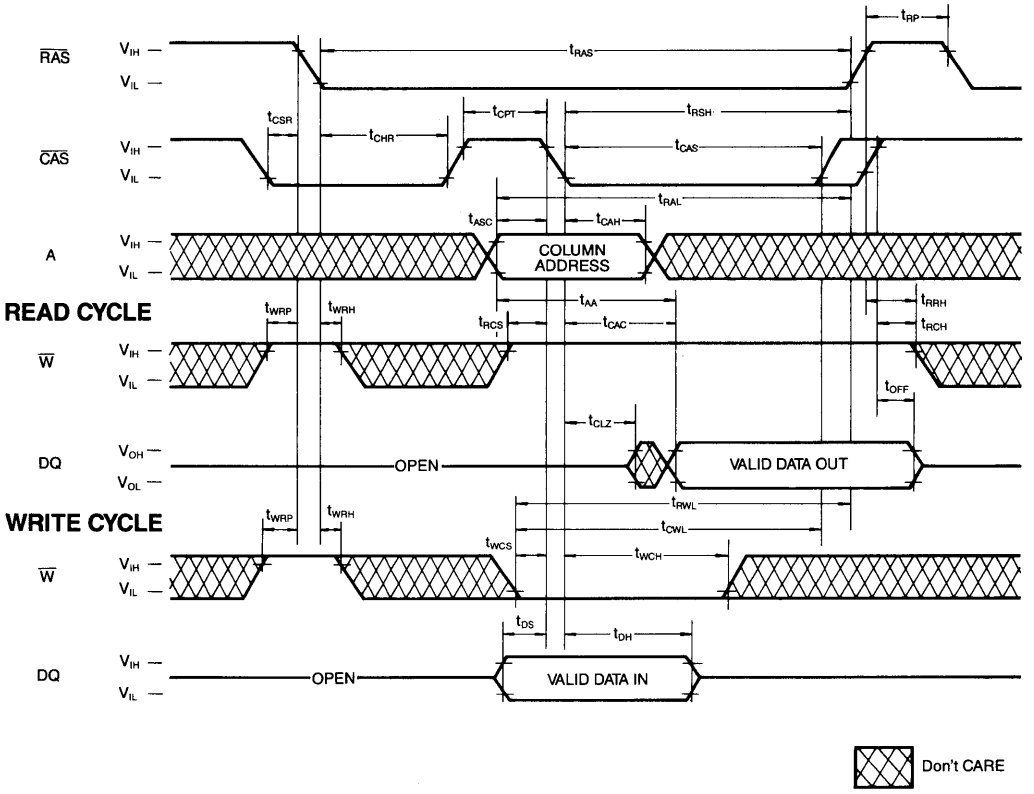


HIDDEN REFRESH CYCLE (WRITE)



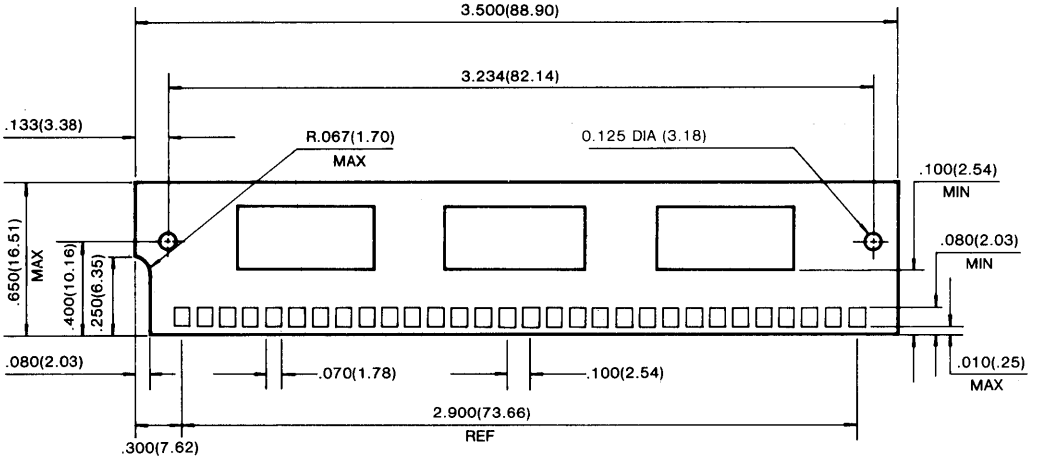
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

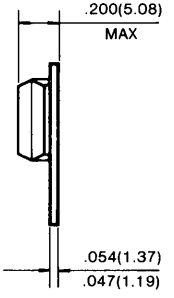


PACKAGE DIMENSIONS

Units: Inches (millimeters)



Tolerances: ±.005(.13) unless otherwise specified



4MX8 CMOS DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM584000A- 7	70ns	20ns	130ns
KMM584000A- 8	80ns	20ns	150ns
KMM584000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

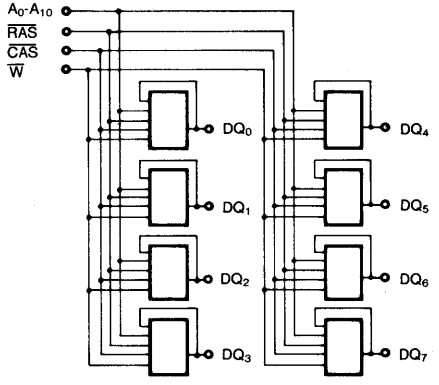
GENERAL DESCRIPTION

The Samsung KMM584000A is a 4M bit X 8 Dynamic RAM high density memory module. The Samsung KMM584000A consist of eight KM41C4000AJ DRAMs in 20-pin SOJ package mounted on a 30-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each 4M Bit DRAM.

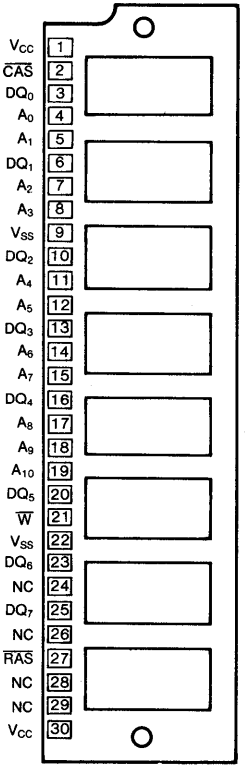
The KMM584000A is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{0-7}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	4.8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM584000A- 7	I_{CC1}	—	840	mA
	KMM584000A- 8		—	760	mA
	KMM584000A-10		—	680	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	16	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM584000A- 7	I_{CC3}	—	840	mA
	KMM584000A- 8		—	760	mA
	KMM584000A-10		—	680	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM584000A- 7	I_{CC4}	—	640	mA
	KMM584000A- 8		—	560	mA
	KMM584000A-10		—	480	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	8	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM584000A- 7	I_{CC6}	—	840	mA
	KMM584000A- 8		—	760	mA
	KMM584000A-10		—	680	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−80	80	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	50	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	55	pF
Input/Output Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM584000A-7		KMM584000A-8		KMM584000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS (Continued)

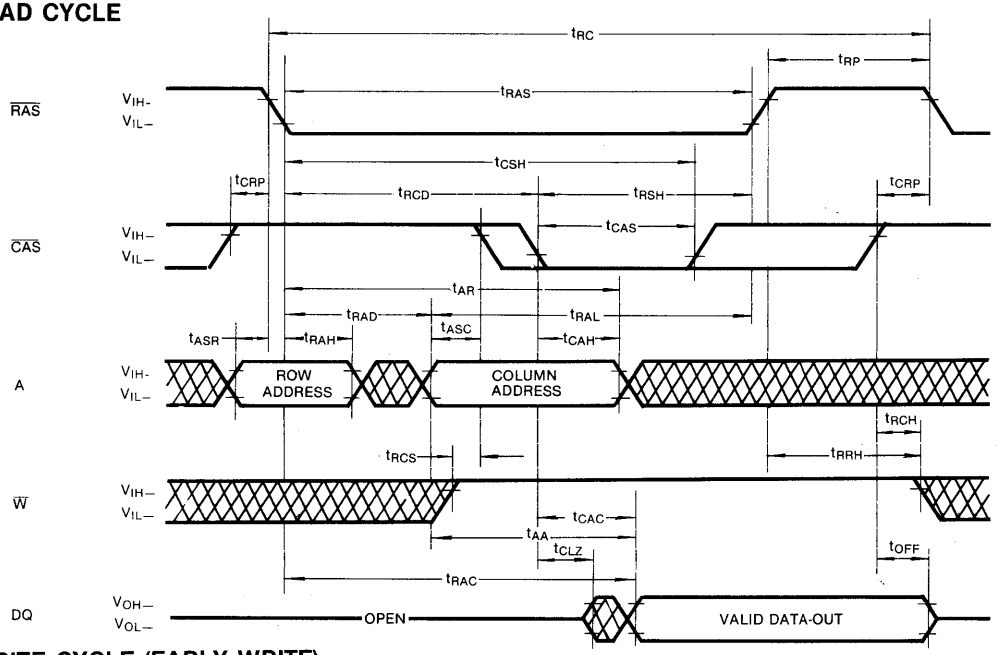
Standard Operation	Symbol	KMM584000A-7		KMM584000A-8		KMM584000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ percharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

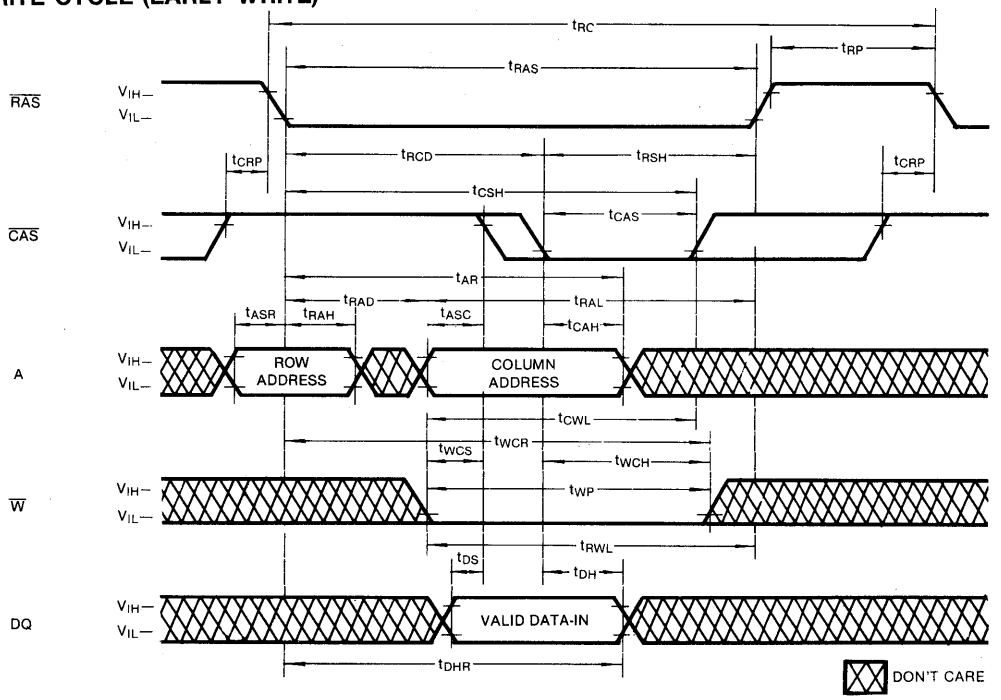
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

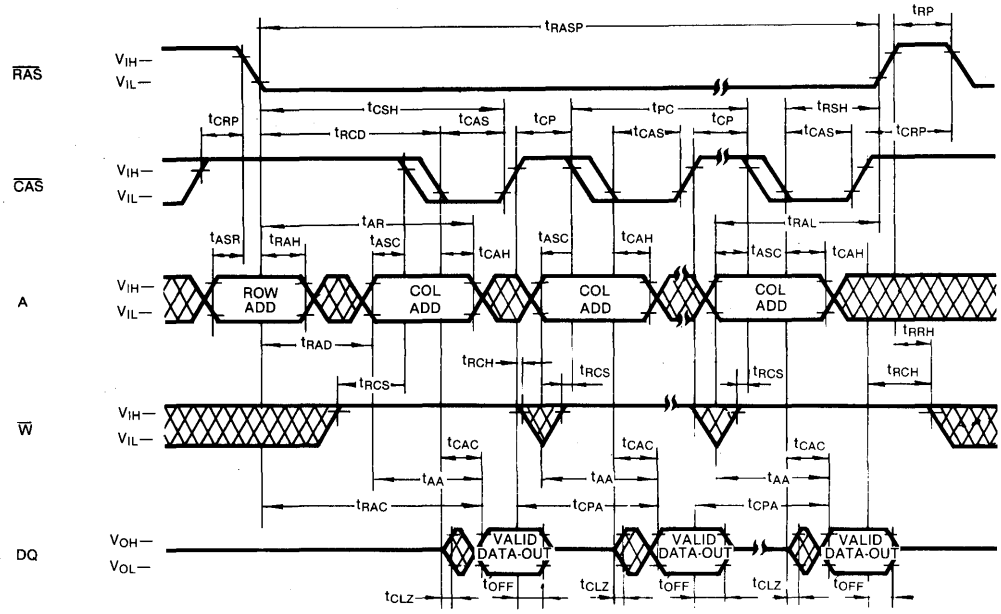


WRITE CYCLE (EARLY WRITE)

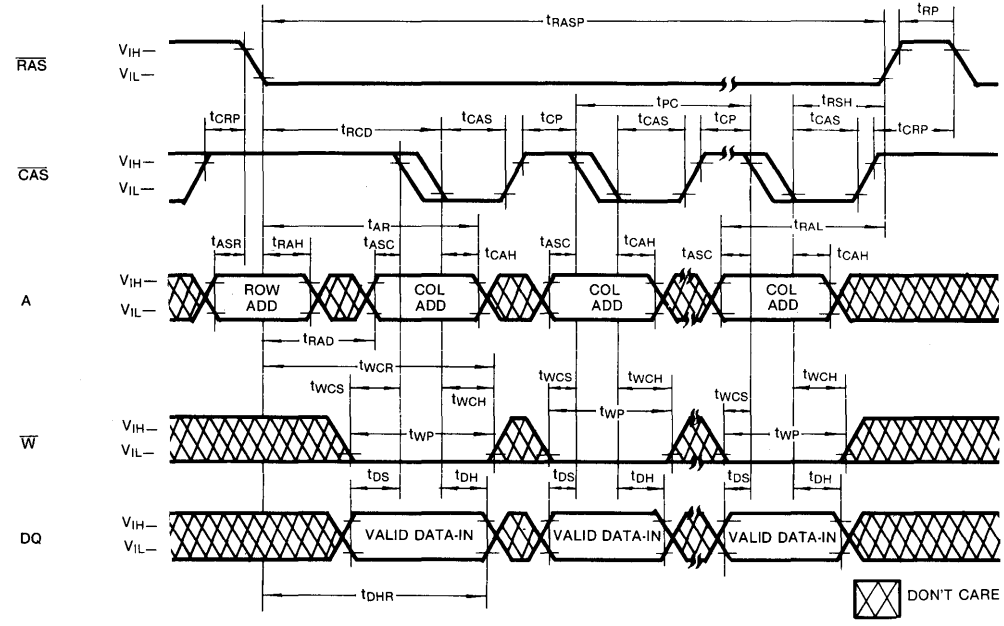


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



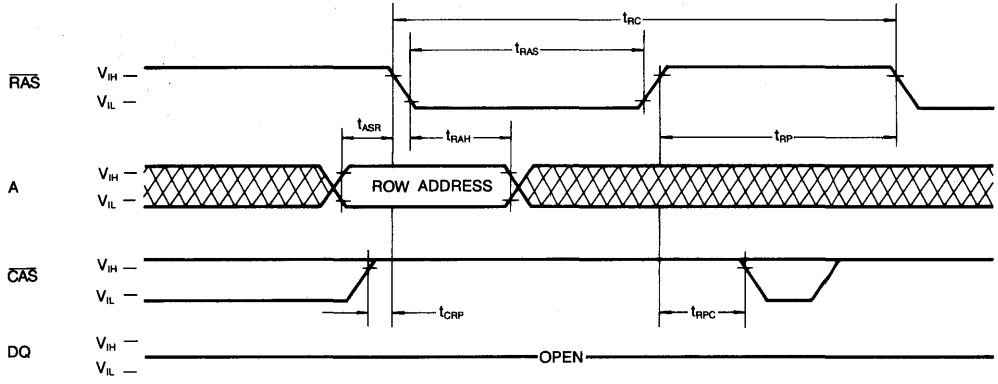
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

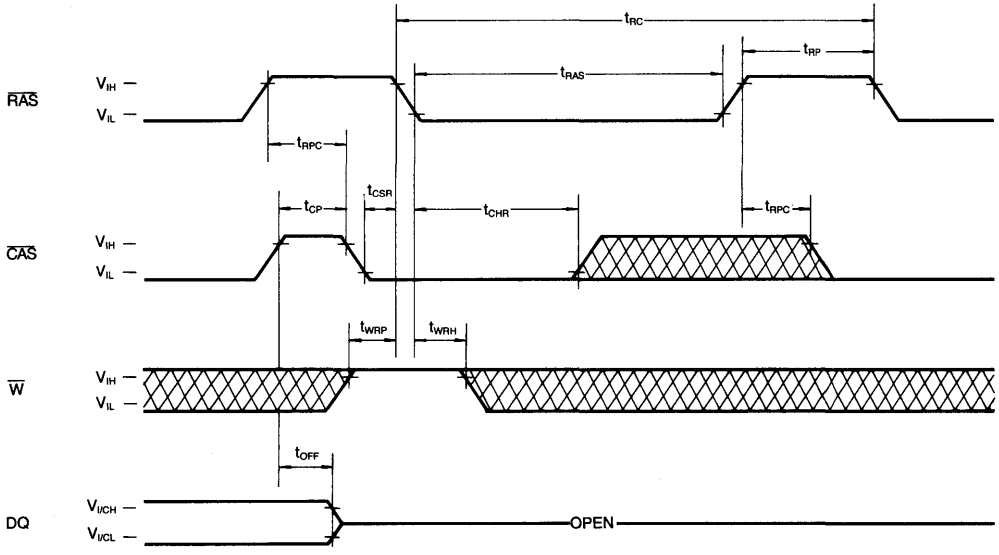
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



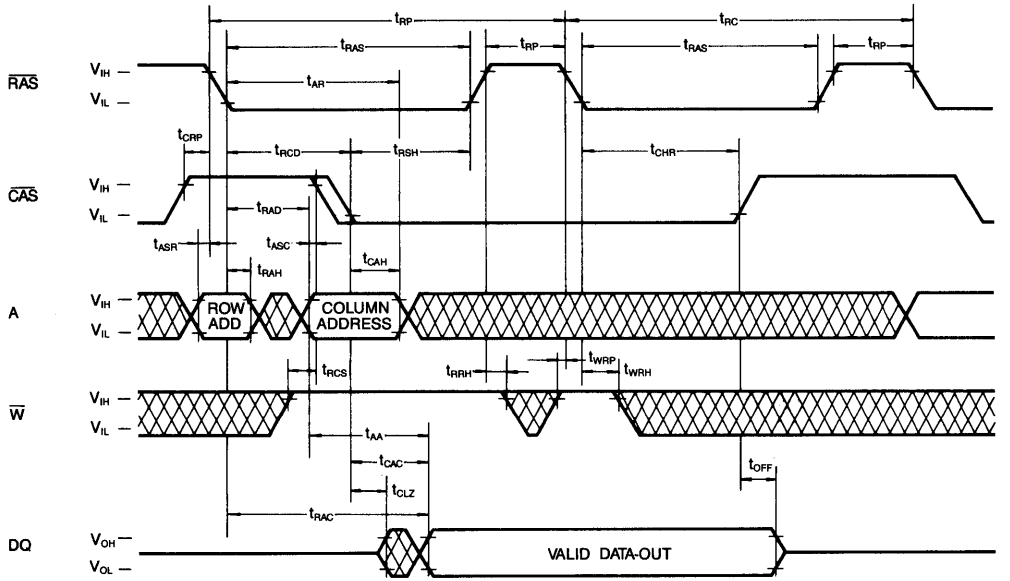
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

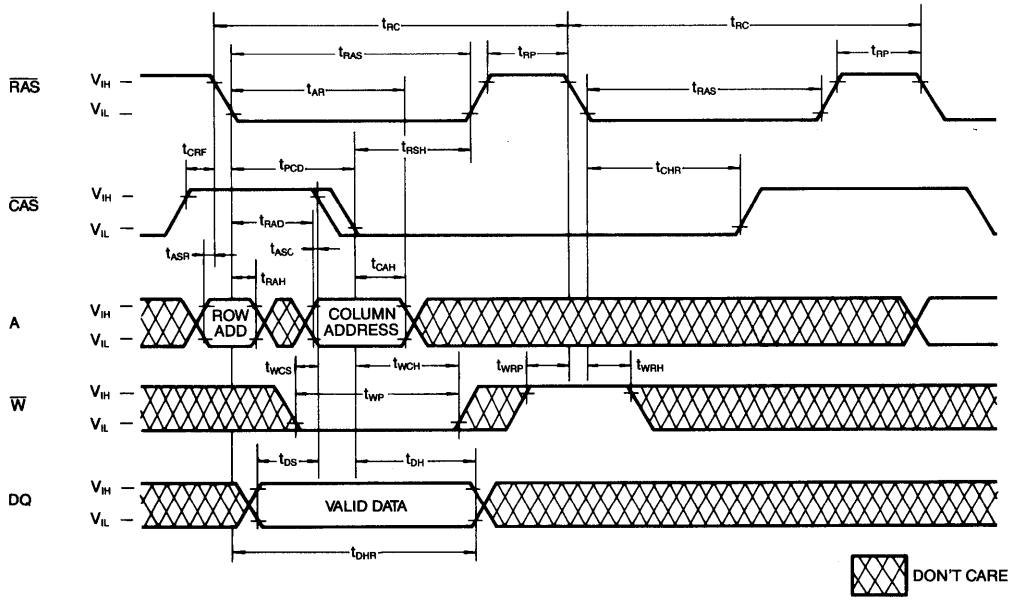


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

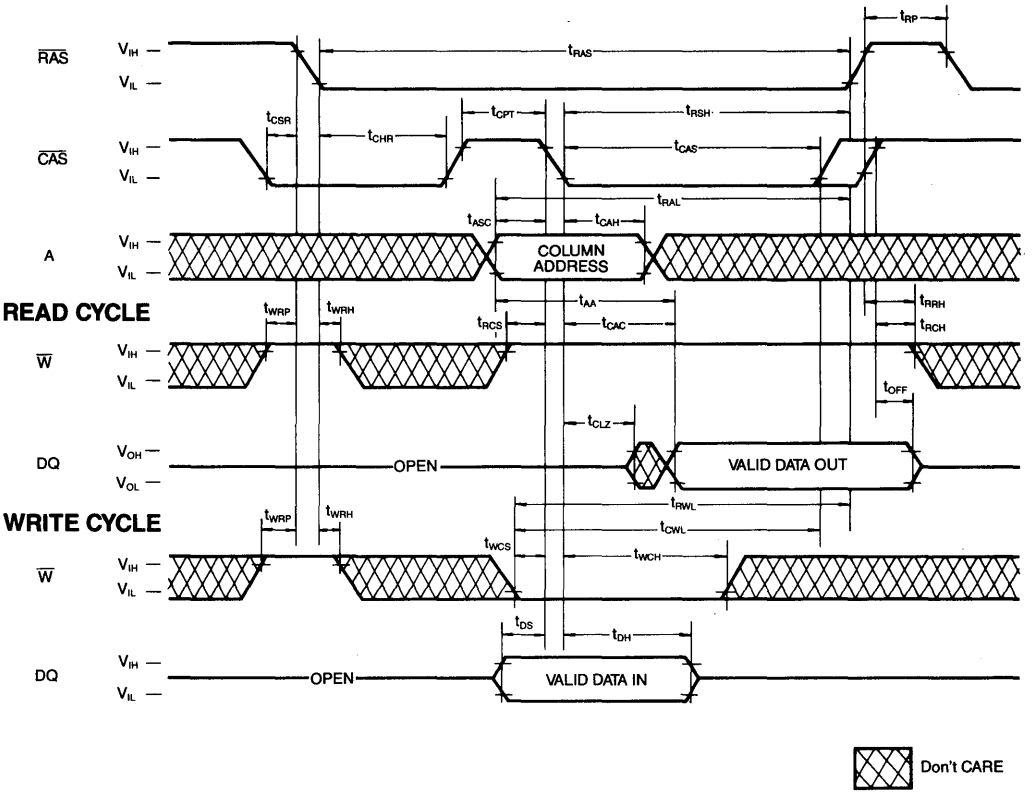


HIDDEN REFRESH CYCLE (WRITE)



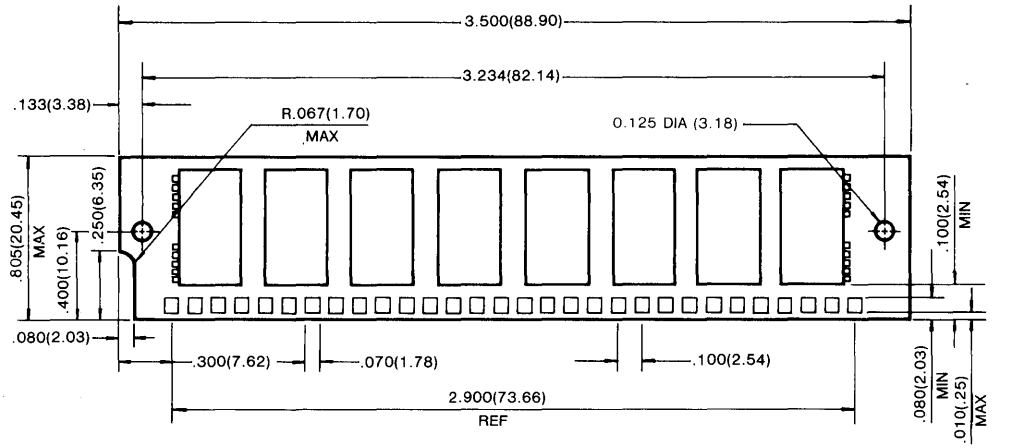
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

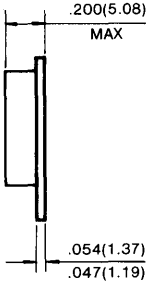


PACKAGE DIMENSIONS

Units: Inches (millimeters)



Tolerances: ±.005(.13) unless otherwise specified



4MX9 CMOS DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM594000A- 7	70ns	20ns	130ns
KMM594000A- 8	80ns	20ns	150ns
KMM594000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

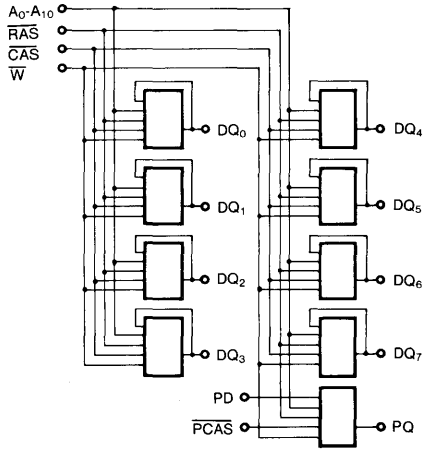
GENERAL DESCRIPTION

The Samsung KMM594000A is a 4M bit X 9 Dynamic RAM high density memory module. The Samsung KMM594000A consist of nine KM41C4000AJ DRAMs in 20-pin SOJ package mounted on a 30-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each 4M Bit DRAM.

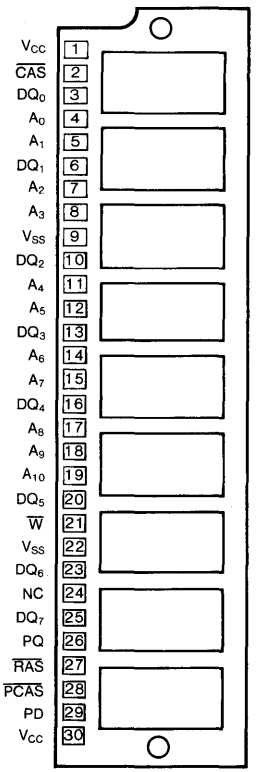
The KMM594000A is a Single In-line Memory Module with edge connections and is intended for mounting into 30-pin edge connector sockets.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{0-7}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	CAS for Parity
PD	Data In for Parity
PQ	Data Out for Parity
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	5.4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM594000A- 7	I_{CC1}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	18	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM594000A- 7	I_{CC3}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM594000A- 7	I_{CC4}	—	720	mA
	KMM594000A- 8		—	630	mA
	KMM594000A-10		—	540	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	9	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM594000A- 7	I_{CC6}	—	945	mA
	KMM594000A- 8		—	855	mA
	KMM594000A-10		—	765	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−90	90	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	55	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	65	pF
Input Capacitance (PD, $\overline{PCAS}$)	C_{IN3}	—	10	pF
Input/Output Capacitance (DQ_0-DQ_7)	C_{DQ}	—	15	pF
Output Capacitance (PQ)	C_Q	—	10	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM594000A-7		KMM594000A-8		KMM594000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

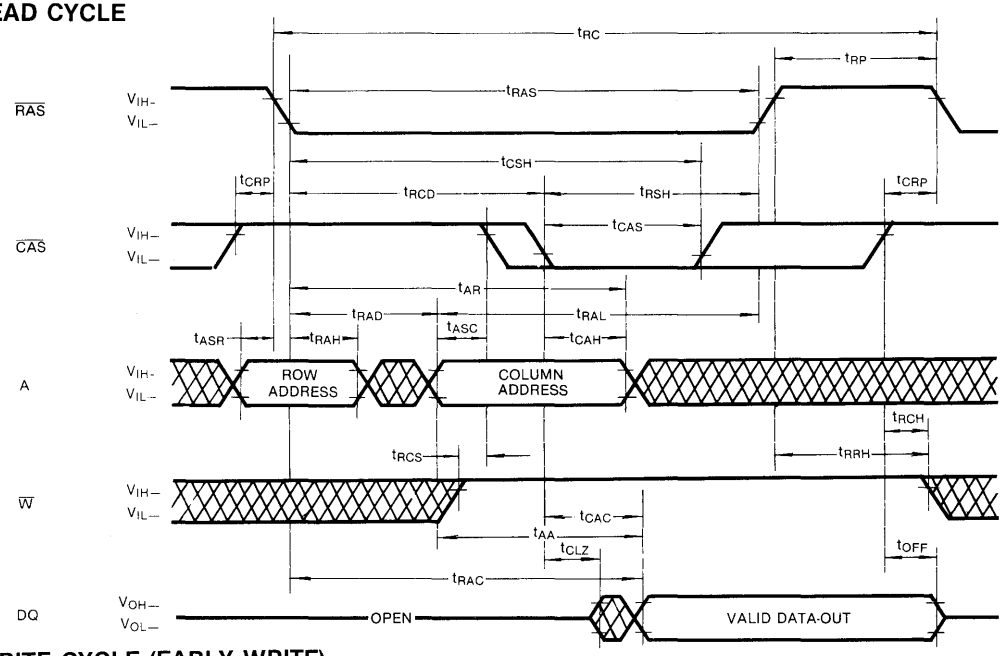
Standard Operation	Symbol	KMM594000A-7		KMM594000A-8		KMM594000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

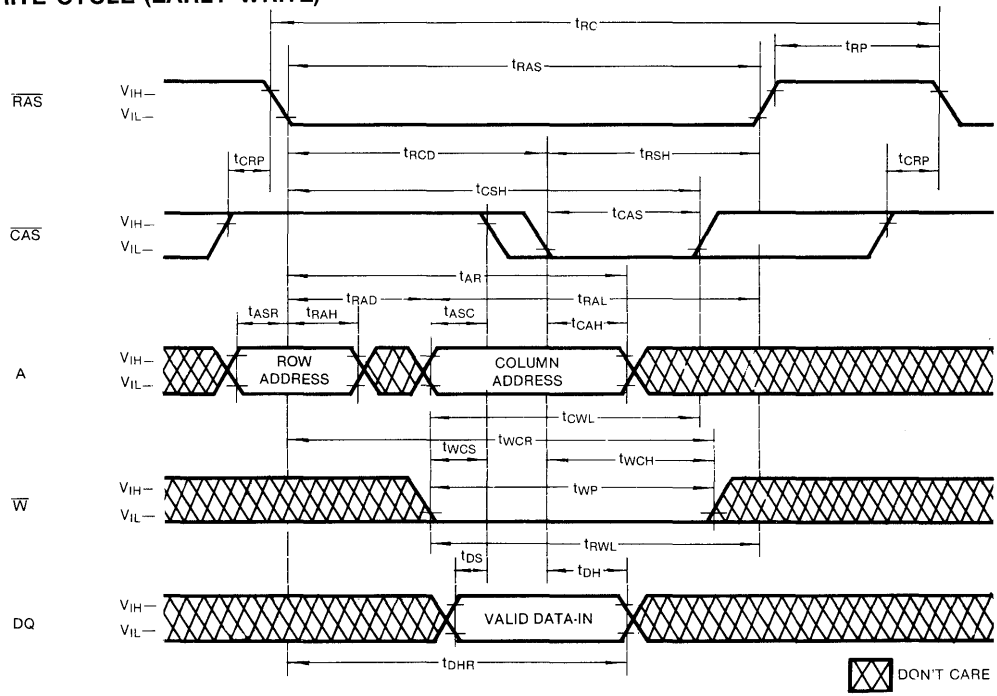
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

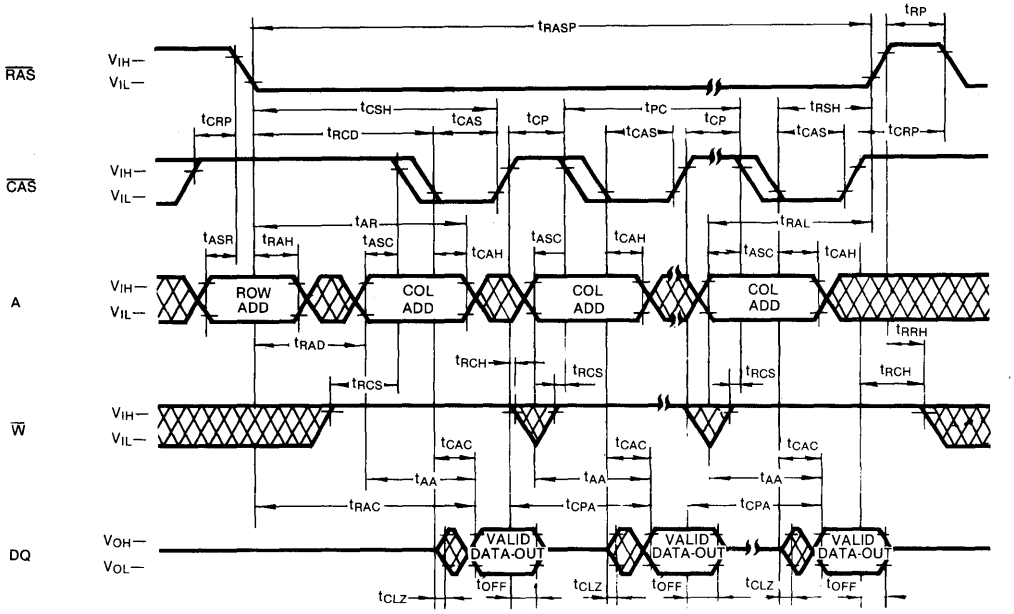


WRITE CYCLE (EARLY WRITE)

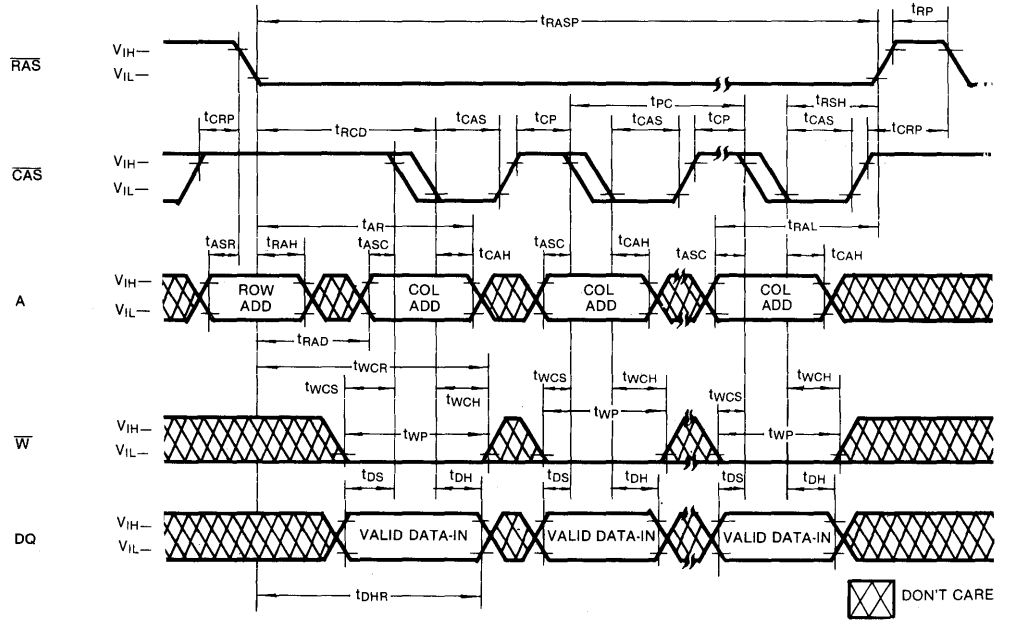


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



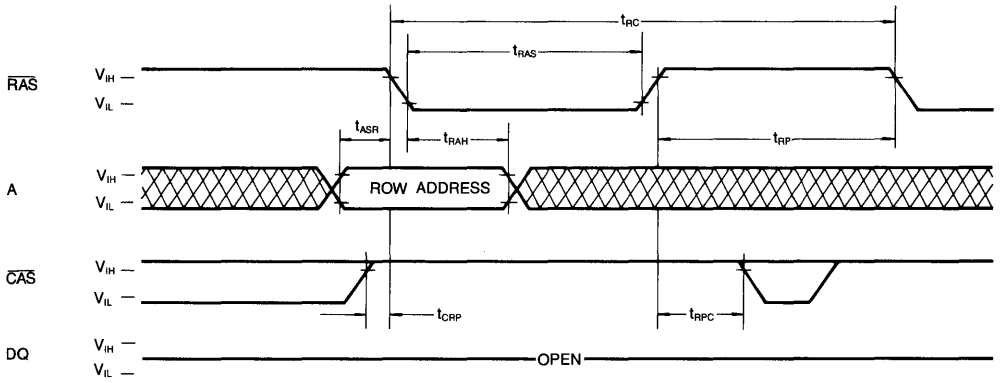
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

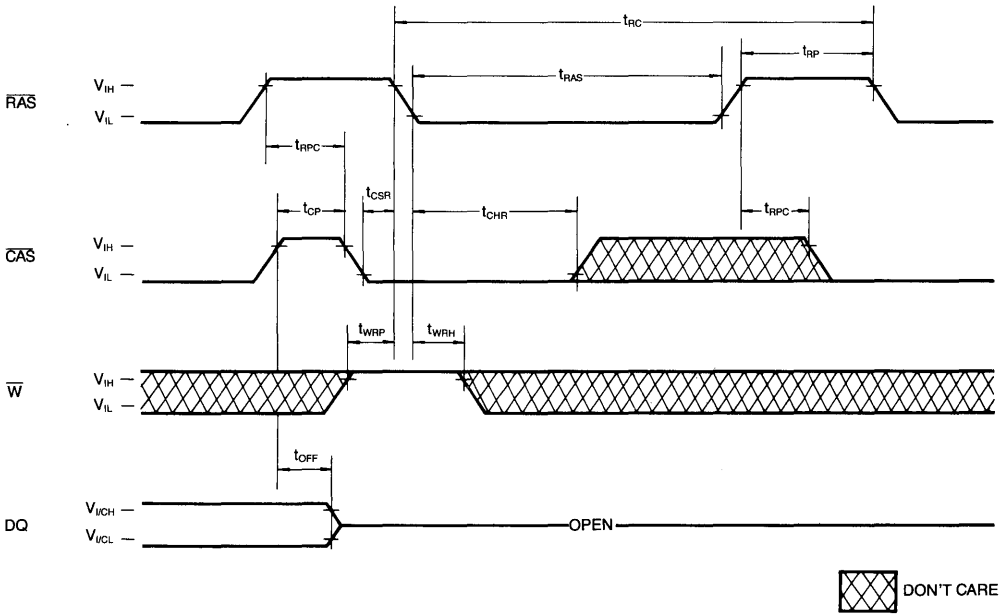
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



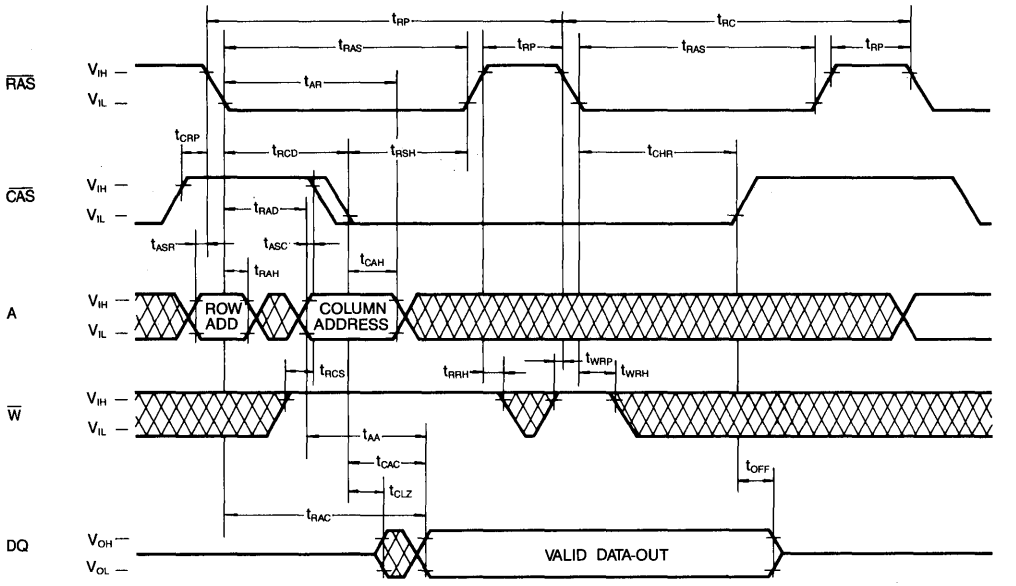
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

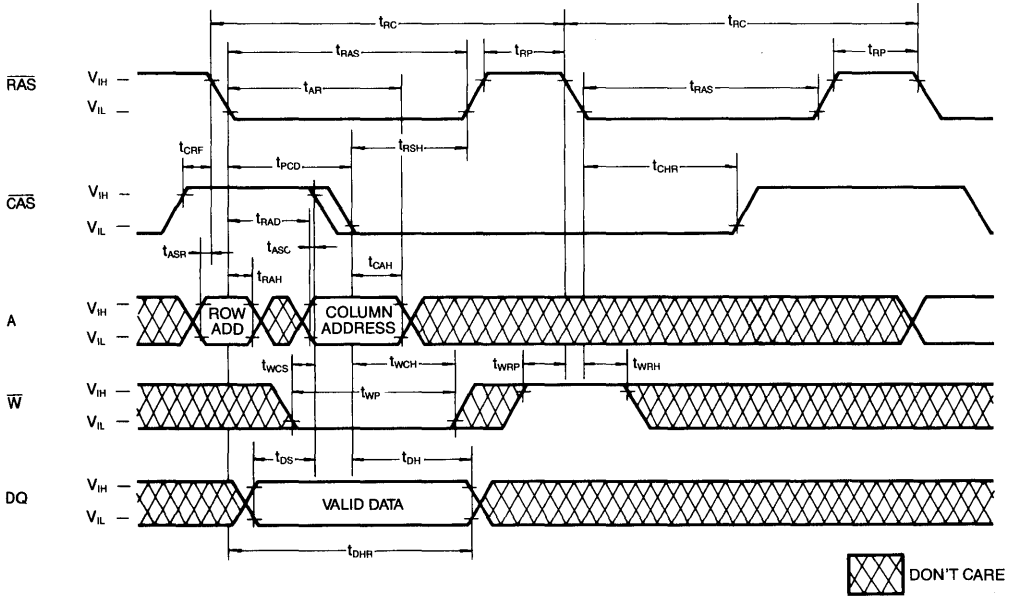


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

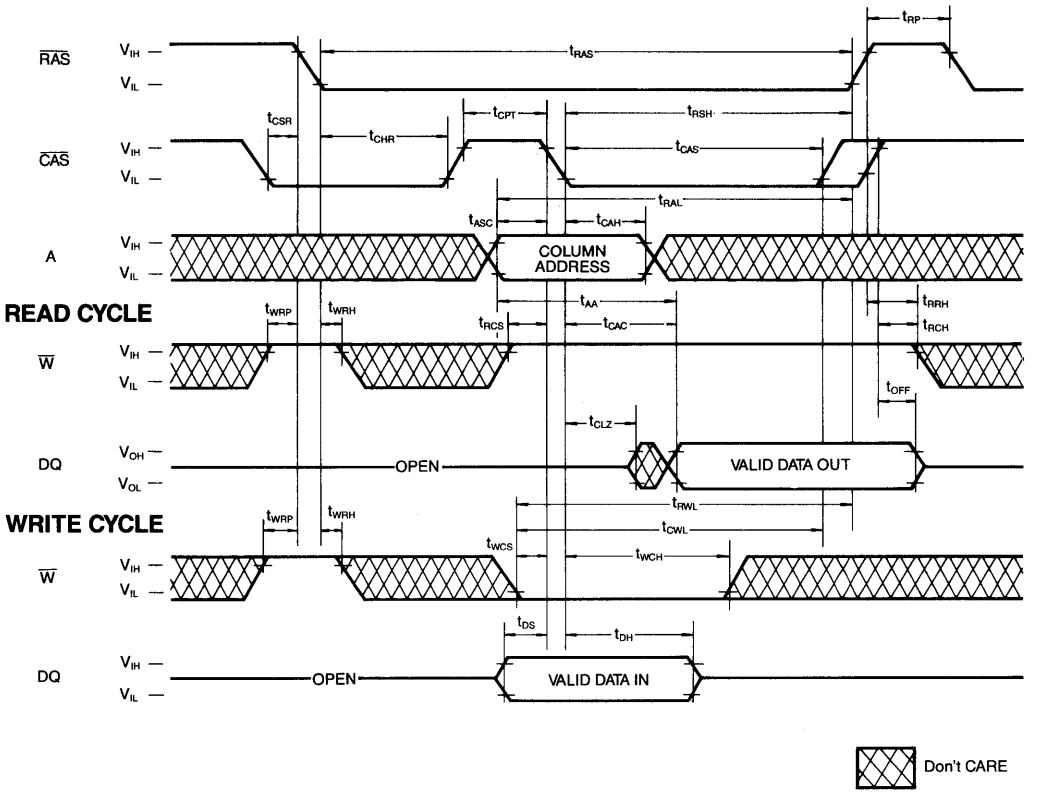


HIDDEN REFRESH CYCLE (WRITE)



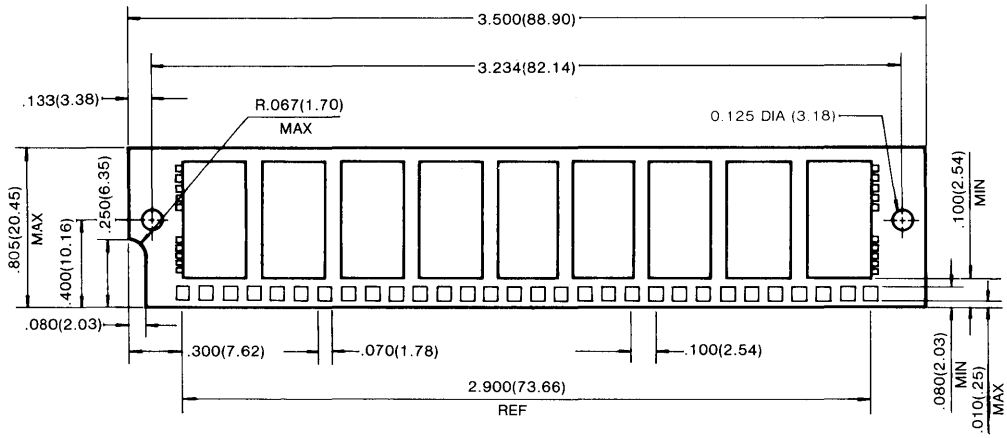
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

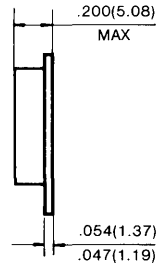


PACKAGE DIMENSIONS

Units: Inches (millimeters)



Tolerances: ±.005(.13) unless otherwise specified



1M×32 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5321000AV- 7	70ns	20ns	130ns
KMM5321000AV- 8	80ns	20ns	150ns
KMM5321000AV-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

The Samsung KMM5321000AV is a 1M bits×32 Dynamic RAM high density memory module. The Samsung KMM5321000AV consist of eight CMOS 1M×4 bit DRAMs in 20-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5321000AV is a Single in-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

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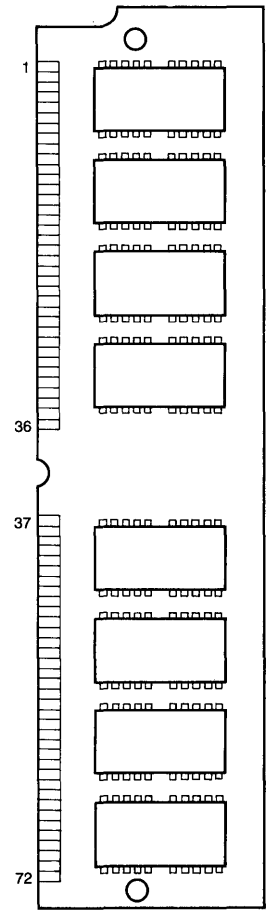
PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	NC
2	DQ_0	38	NC
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS_0}$
5	DQ_{19}	41	$\overline{CAS_2}$
6	DQ_2	42	$\overline{CAS_3}$
7	DQ_{20}	43	$\overline{CAS_1}$
8	DQ_3	44	$\overline{RAS_0}$
9	DQ_{21}	45	NC
10	V_{CC}	46	NC
11	NC	47	$\overline{W}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS_2}$	70	PD_4
35	NC	71	NC
36	NC	72	V_{SS}



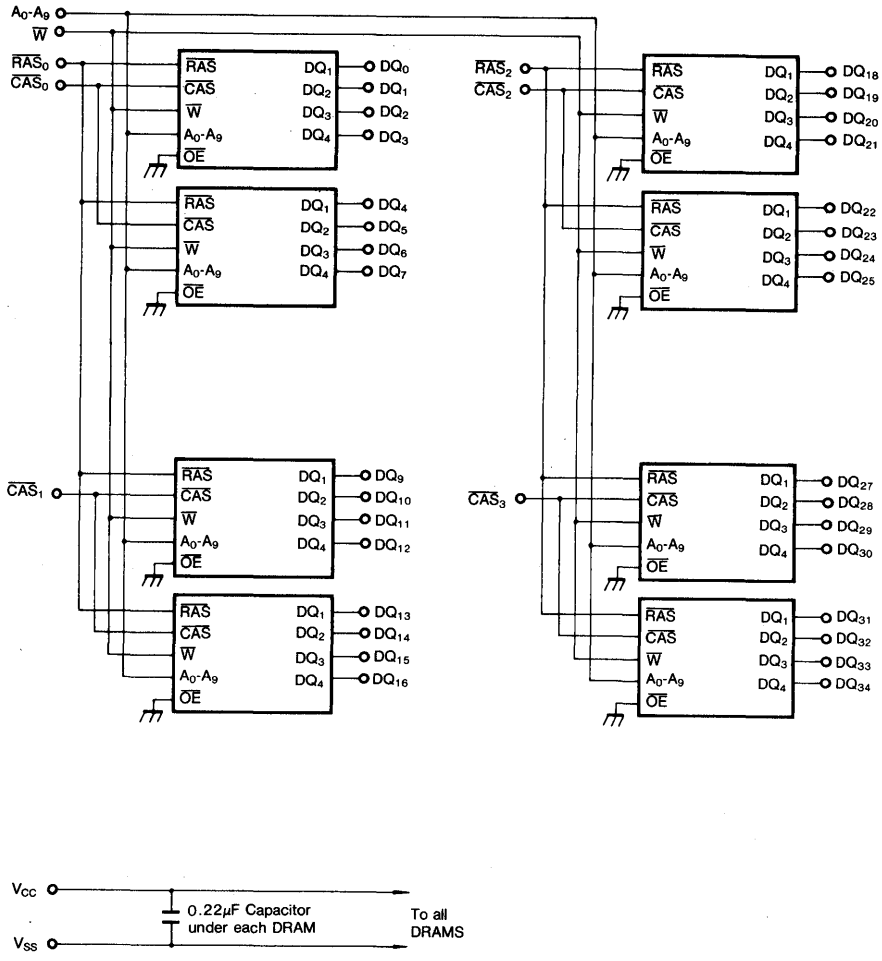
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{35} (except $DQ_{8, 17, 26, 35}$)	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS_0}$, $\overline{RAS_2}$	Row Address Strobe
$\overline{CAS_0}$-$\overline{CAS_3}$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	V_{SS}	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	4.8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A =0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5321000AV- 7	I_{CC1}	—	840	mA
	KMM5321000AV- 8		—	760	mA
	KMM5321000AV-10		—	680	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	16	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM5321000AV- 7	I_{CC3}	—	840	mA
	KMM5321000AV- 8		—	760	mA
	KMM5321000-10		—	680	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5321000AV- 7	I_{CC4}	—	640	mA
	KMM5321000AV- 8		—	560	mA
	KMM5321000AV-10		—	480	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	8	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5321000AV- 7	I_{CC6}	—	840	mA
	KMM5321000AV- 8		—	760	mA
	KMM5321000AV-10		—	680	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−80	80	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	64	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	70	pF
Input Capacitance ($\overline{RAS_0}$,$\overline{RAS_2}$)	C_{IN3}	—	42	pF
Input Capacitance ($\overline{CAS_0}$-$\overline{CAS_3}$)	C_{IN4}	—	36	pF
Input/Output Capacitance ($DQ_{0\text{-}7, 9\text{-}16, 18\text{-}25, 27\text{-}34}$)	CDQ_1	—	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V ± 10%, See notes 1, 2)

Standard Operation	Symbol	KMM5321000AV-7		KMM5321000AV-8		KMM5321000AV-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column addressdelay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up-time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

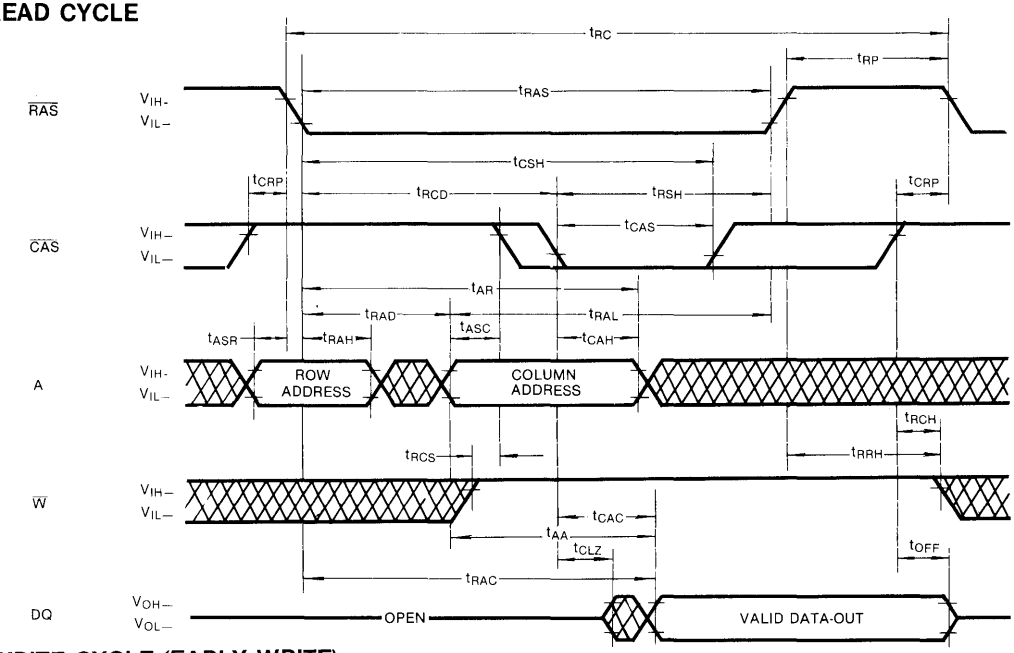
Standard Operation	Symbol	KMM5321000AV-7		KMM5321000AV-8		KMM5321000AV-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

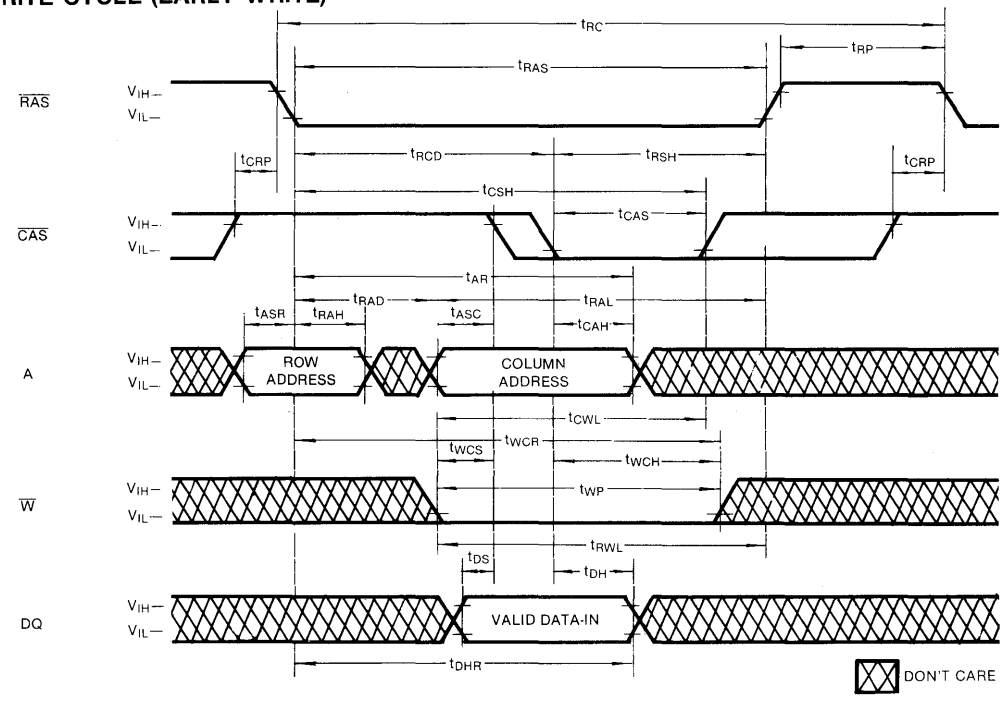
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the out-put achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write clcle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

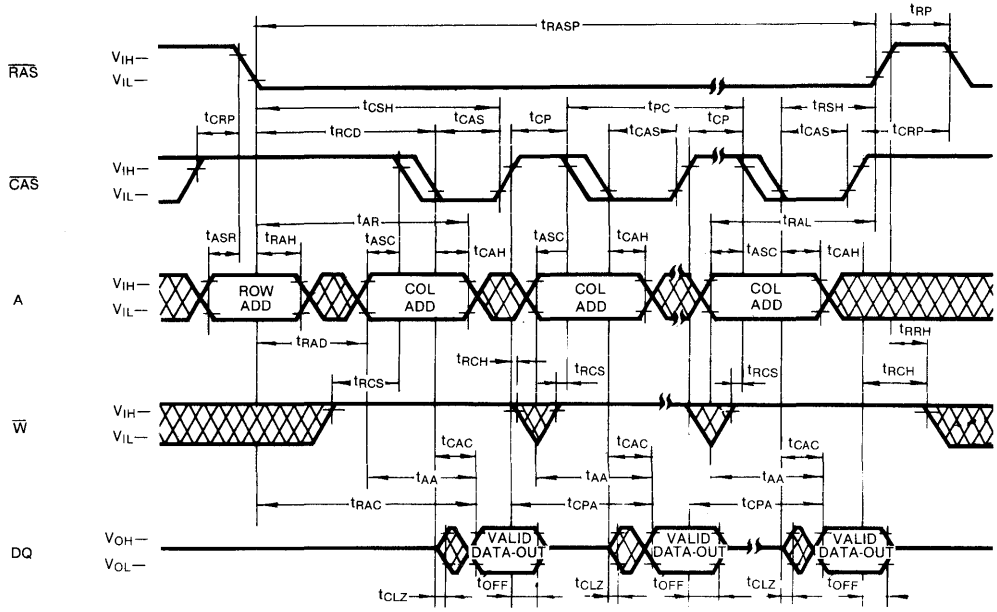


WRITE CYCLE (EARLY WRITE)

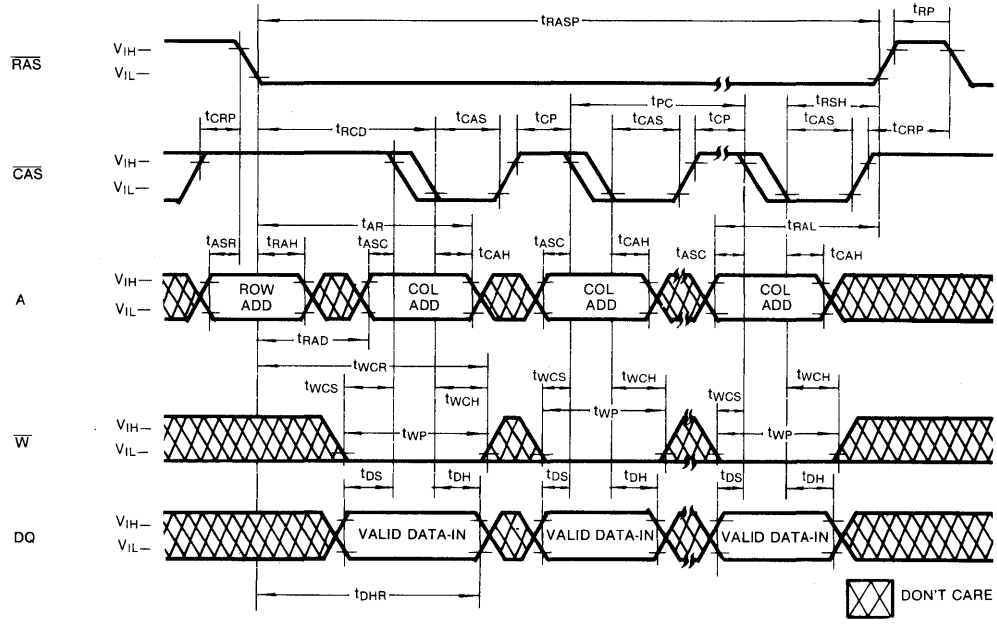


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



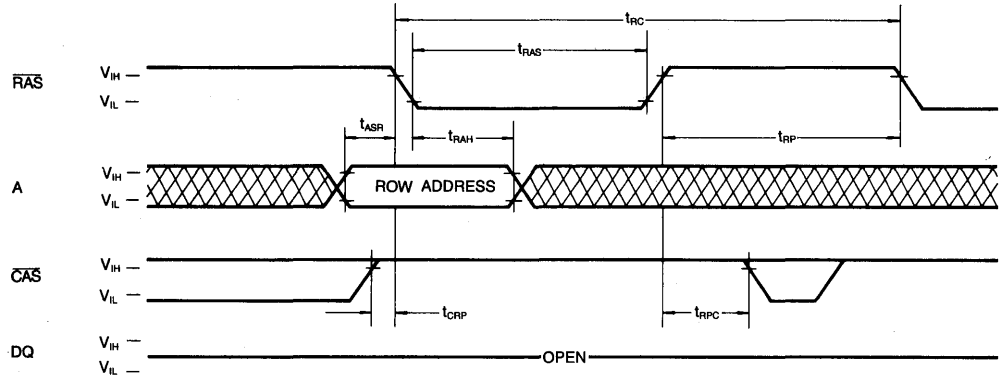
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

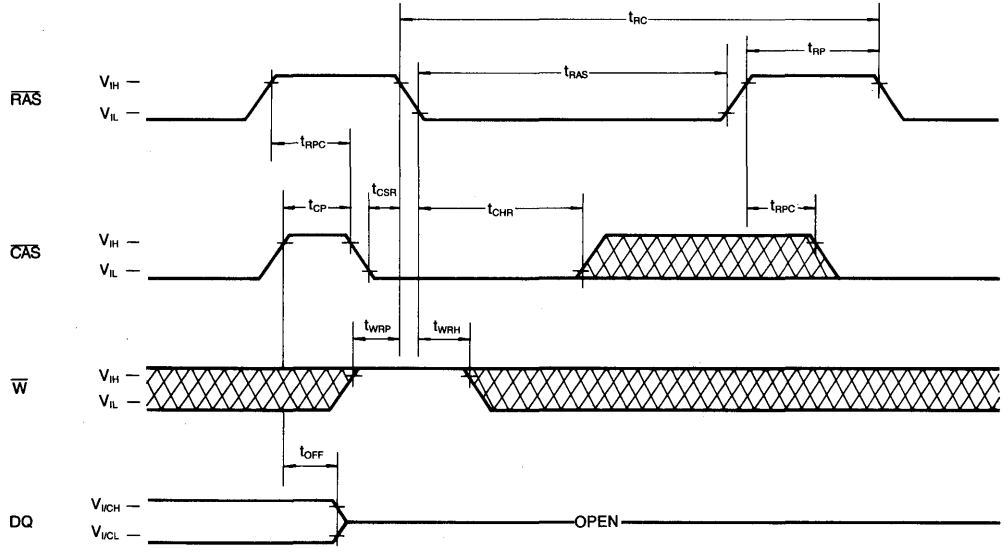
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



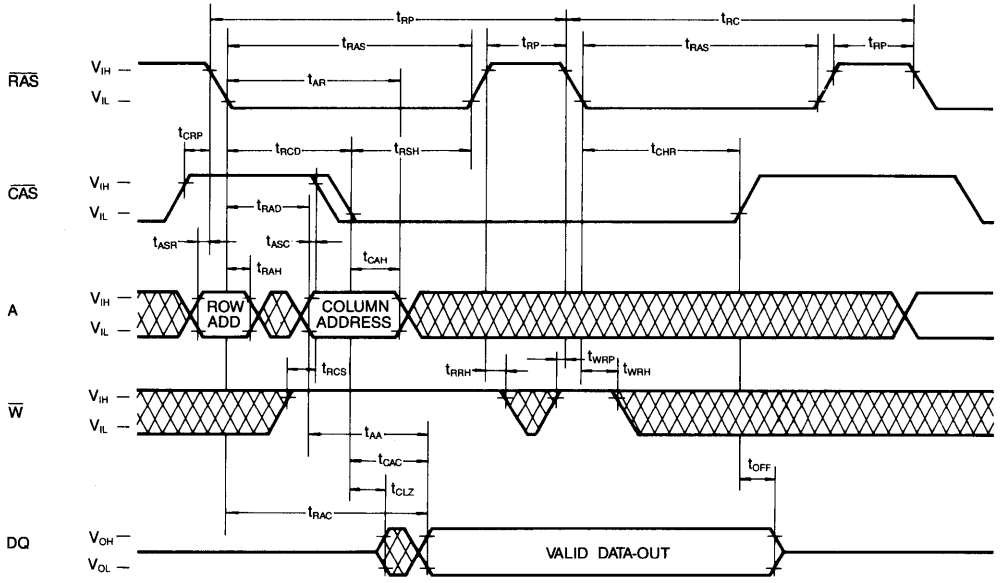
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

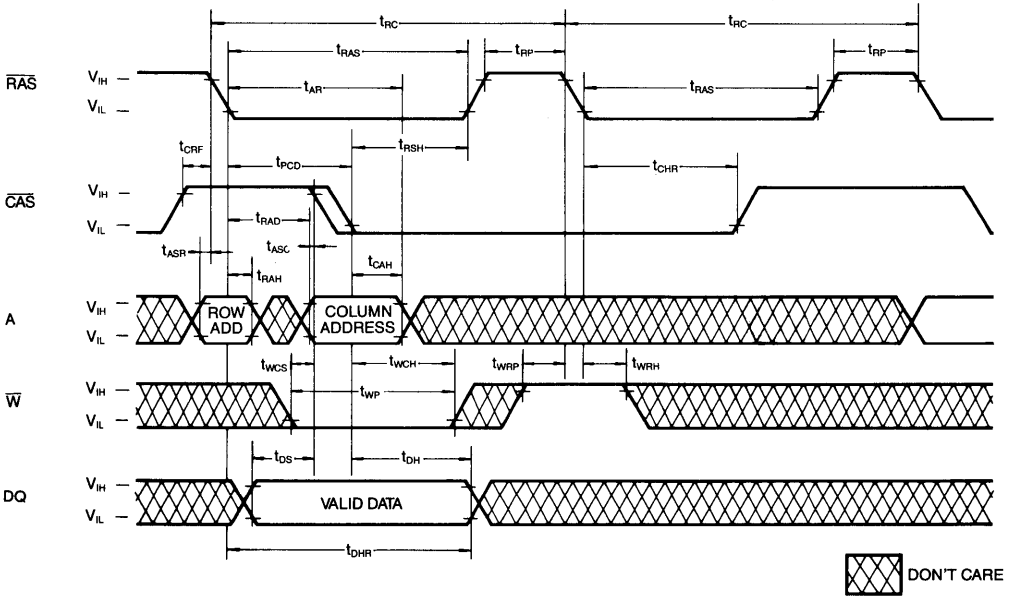


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

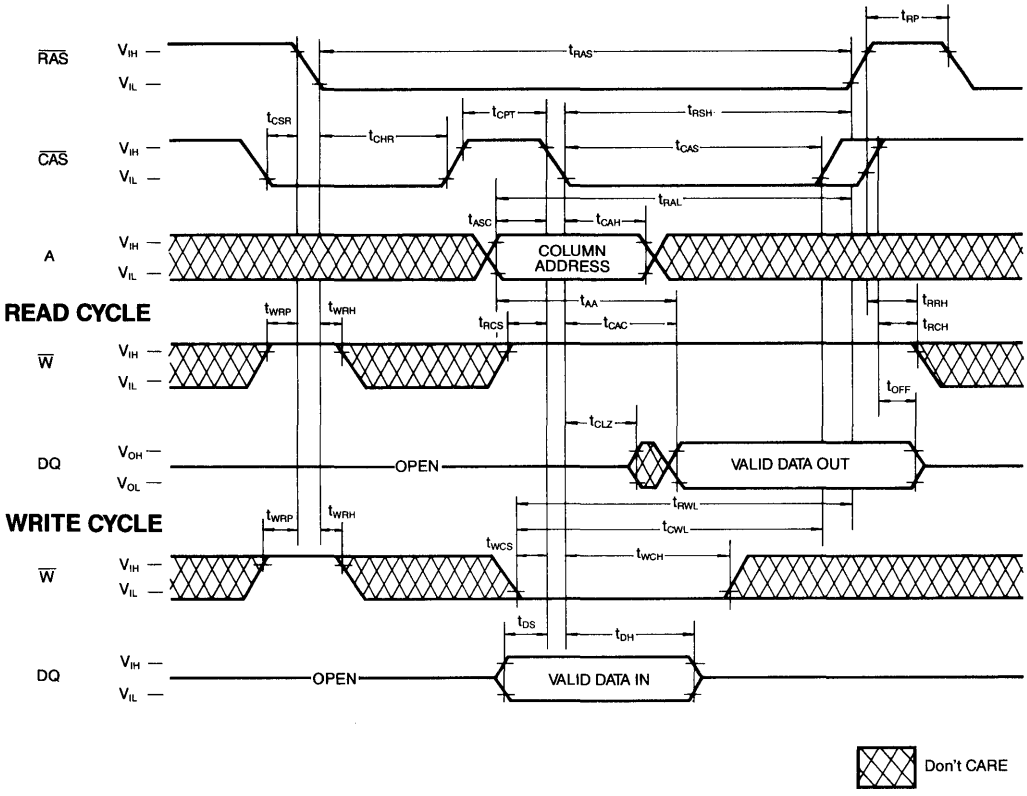


HIDDEN REFRESH CYCLE (WRITE)



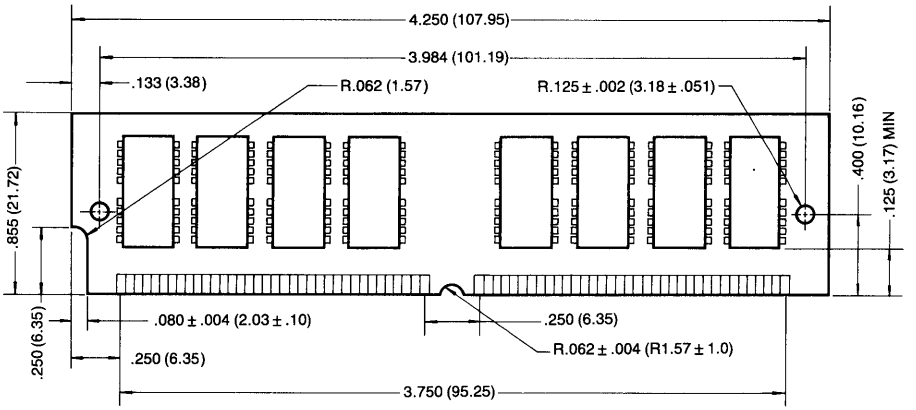
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

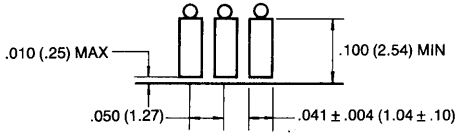


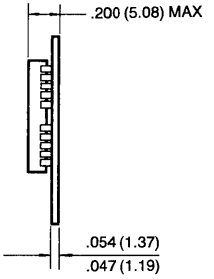
PACKAGE DIMENSIONS

Units: Inches (millimeters)

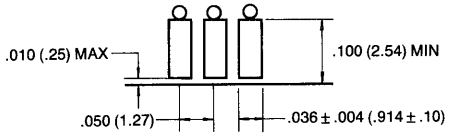


KMM5321000AVG: DETAIL OF CONTACTS (Gold plating lead)





KMM5321000AV: DETAIL OF CONTACTS (Solder plating lead)



Tolerances: ± .005 (.13) unless otherwise specified

1MX36 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5361000A- 7	70ns	20ns	130ns
KMM5361000A- 8	80ns	20ns	150ns
KMM5361000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

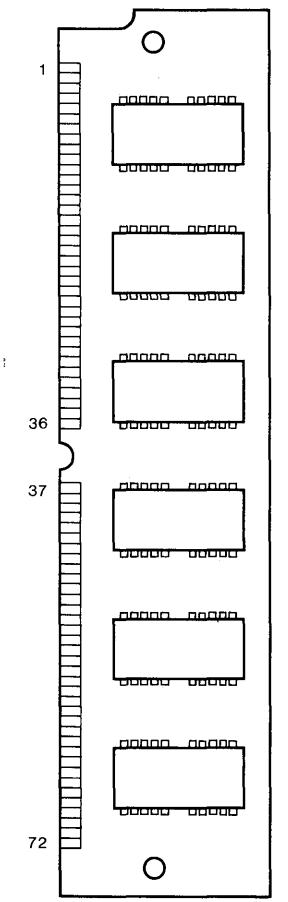
GENERAL DESCRIPTION

The Samsung KMM5361000A is a 1M bits×36 Dynamic RAM high density memory module. The Samsung KMM5361000A consist of eight CMOS 1M×4 bit DRAMs in 20-pin SOJ package and four CMOS 1M×1 bit DRAMs in 20-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5361000A is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS}_0$
5	DQ_{19}	41	$\overline{CAS}_2$
6	DQ_2	42	$\overline{CAS}_3$
7	DQ_{20}	43	$\overline{CAS}_1$
8	DQ_3	44	$\overline{RAS}_0$
9	DQ_{21}	45	NC
10	V_{CC}	46	NC
11	NC	47	$\overline{W}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS}_2$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}



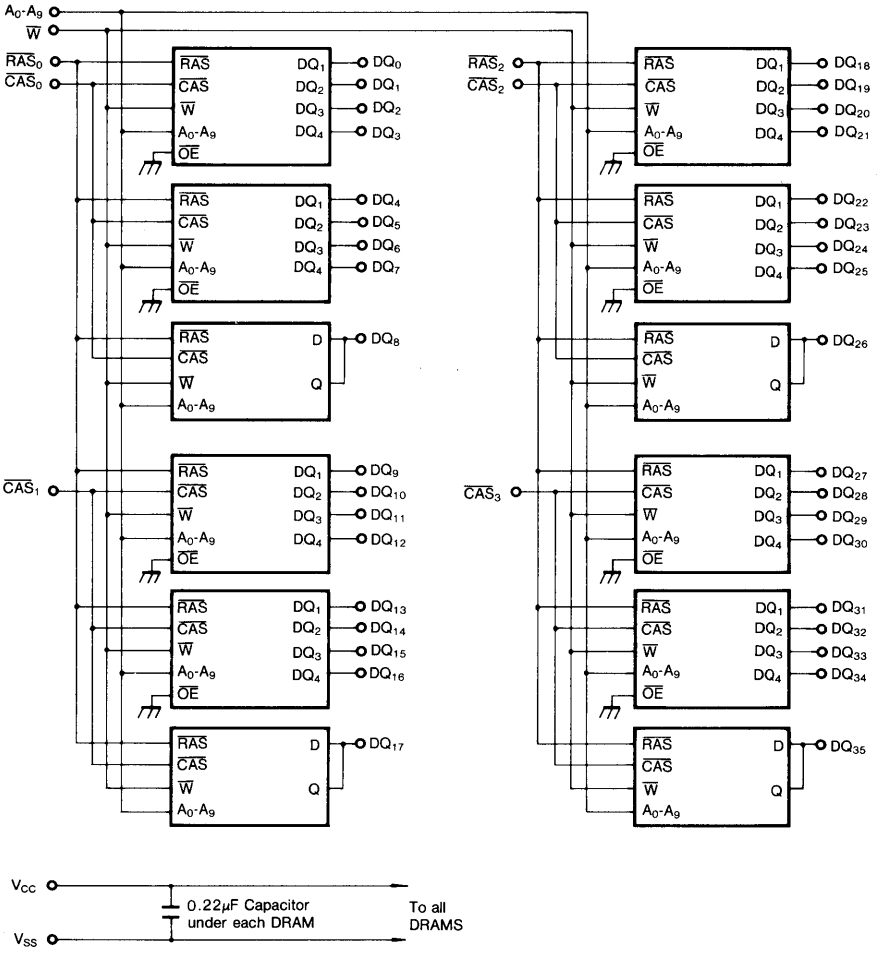
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Address Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	V_{SS}	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	7.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5361000A- 7	I_{CC1}	—	1160	mA
	KMM5361000A- 8		—	1040	mA
	KMM5361000A-10		—	920	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	24	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM5361000A- 7	I_{CC3}	—	1160	mA
	KMM5361000A- 8		—	1040	mA
	KMM5361000A-10		—	920	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5361000A- 7	I_{CC4}	—	880	mA
	KMM5361000A- 8		—	760	mA
	KMM5361000A-10		—	640	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	12	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5361000A- 7	I_{CC6}	—	1160	mA
	KMM5361000A- 8		—	1040	mA
	KMM5361000A-10		—	920	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−120	120	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	88	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	94	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_2$)	C_{IN3}	—	42	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	36	pF
Input/Output Capacitance ($DQ_{0\text{-}7,9\text{-}16,18\text{-}25,27\text{-}34}$)	CDQ_1	—	17	pF
Input/Output Capacitance ($DQ_{8,17,26,35}$)	CDQ_2	—	22	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM5361000A-7		KMM5361000A-8		KMM5361000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

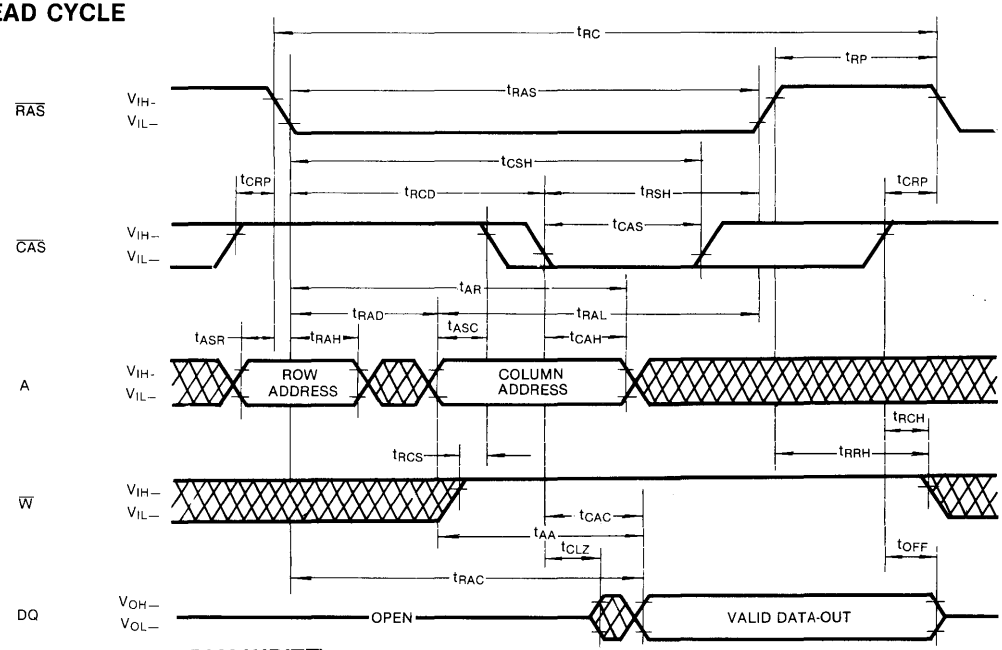
Standard Operation	Symbol	KMM5361000A-7		KMM5361000A-8		KMM5361000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		25		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

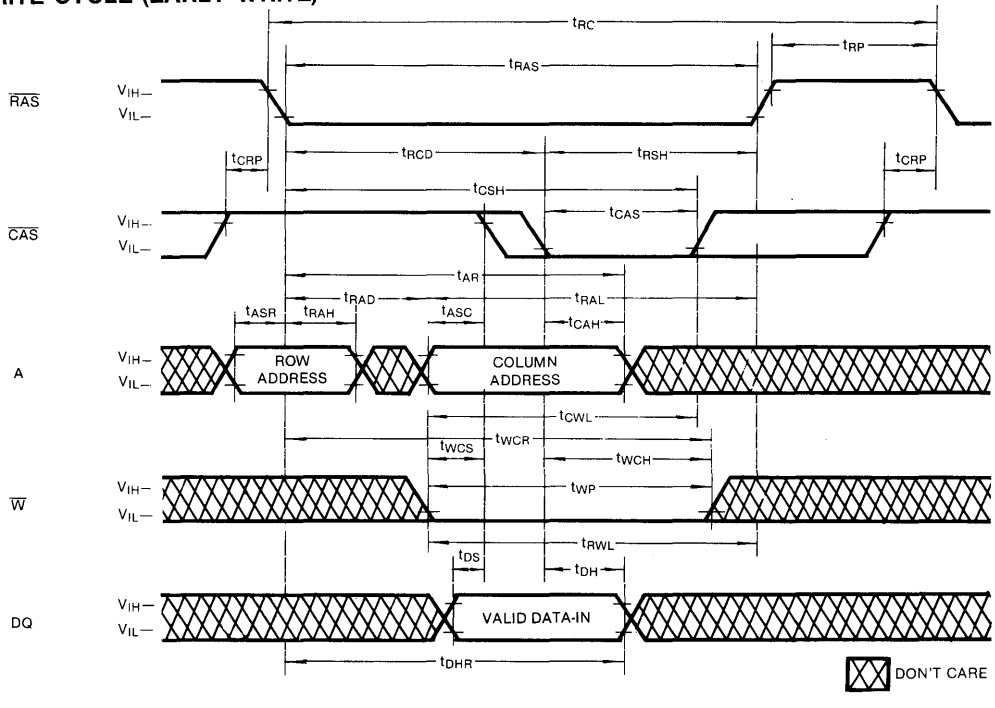
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

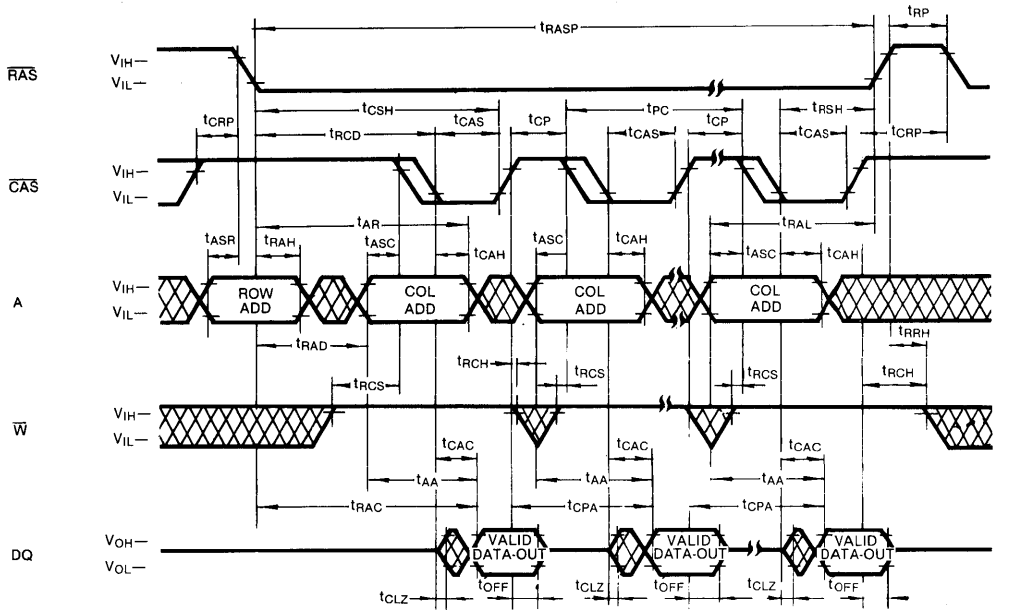


WRITE CYCLE (EARLY WRITE)

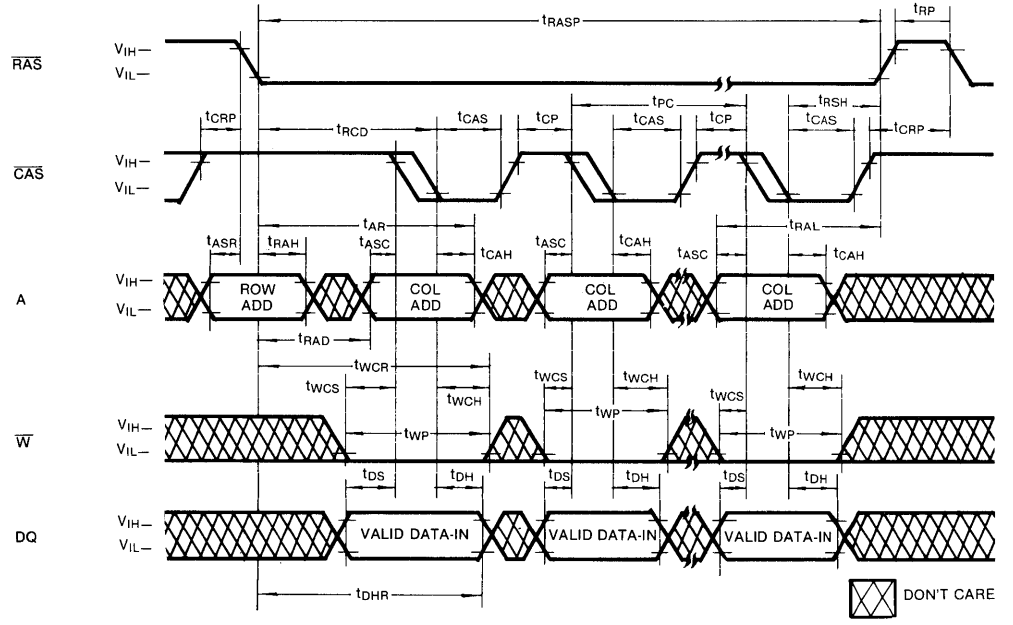


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



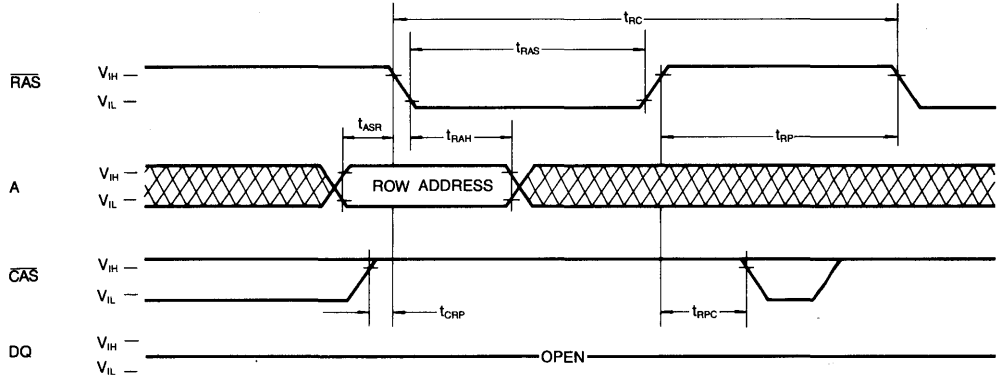
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

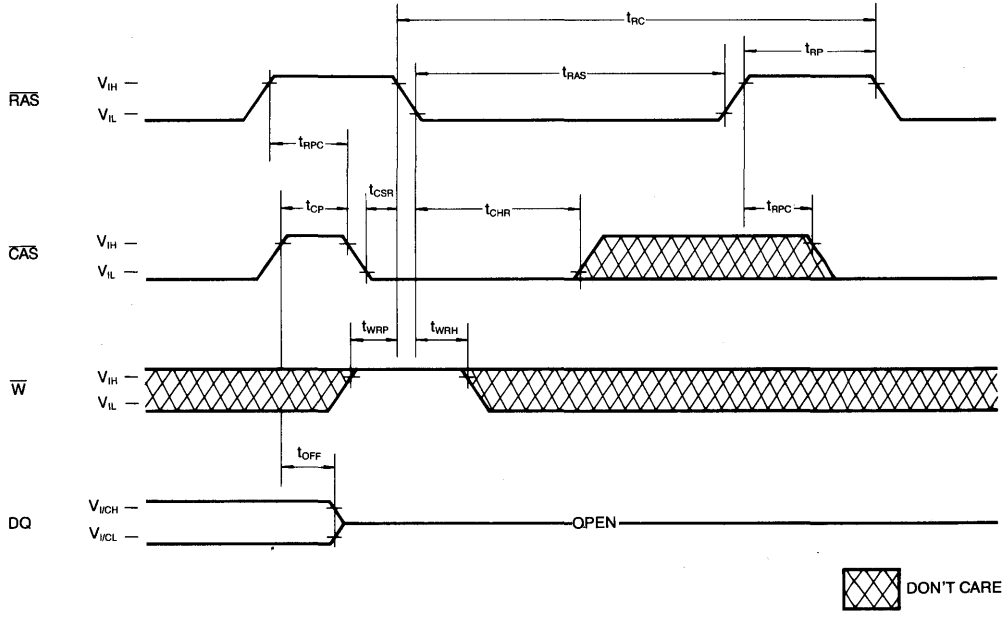
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



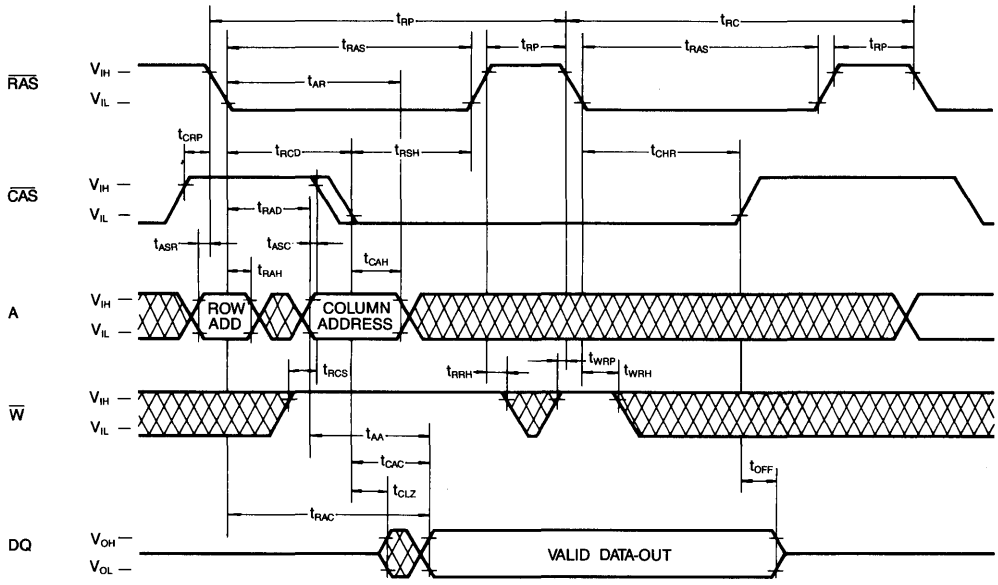
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

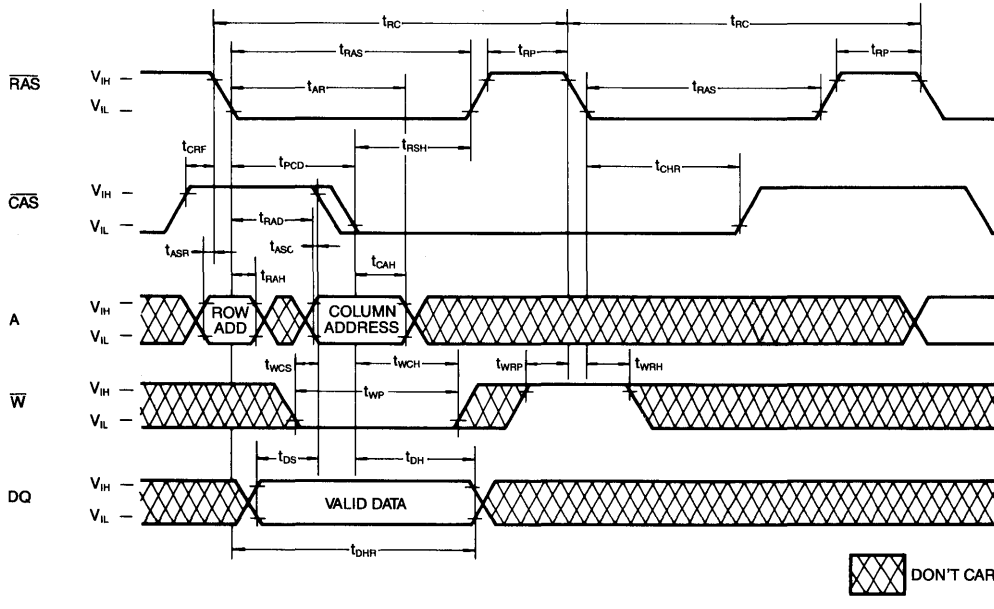


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

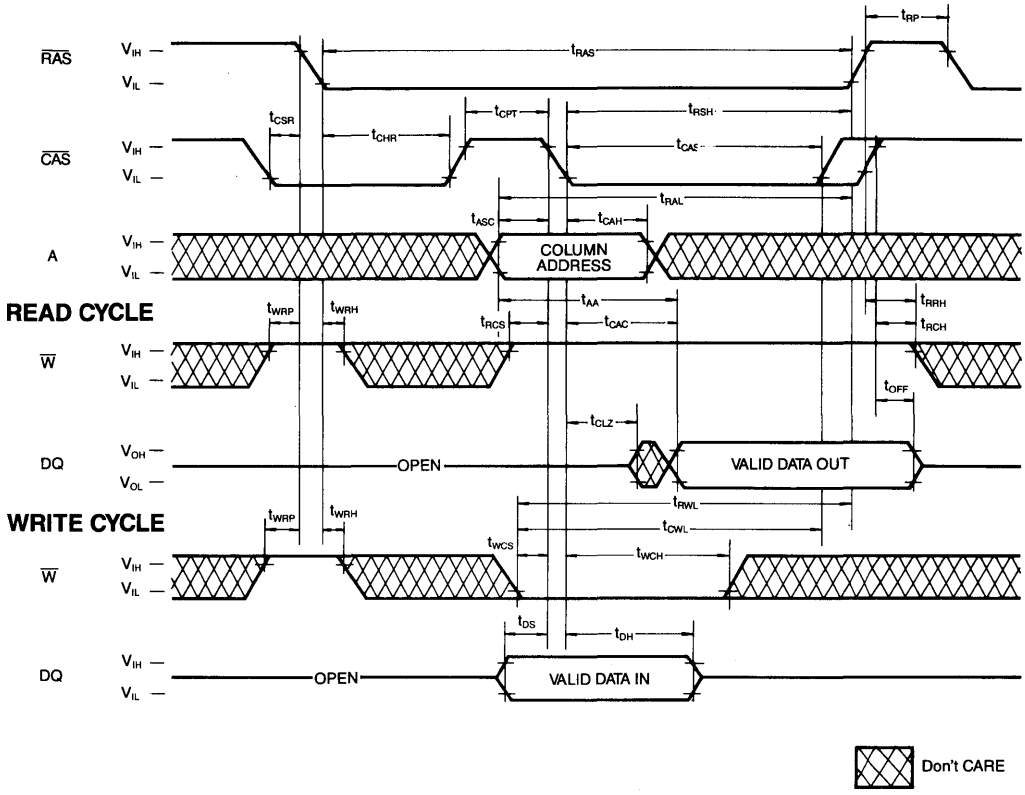


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

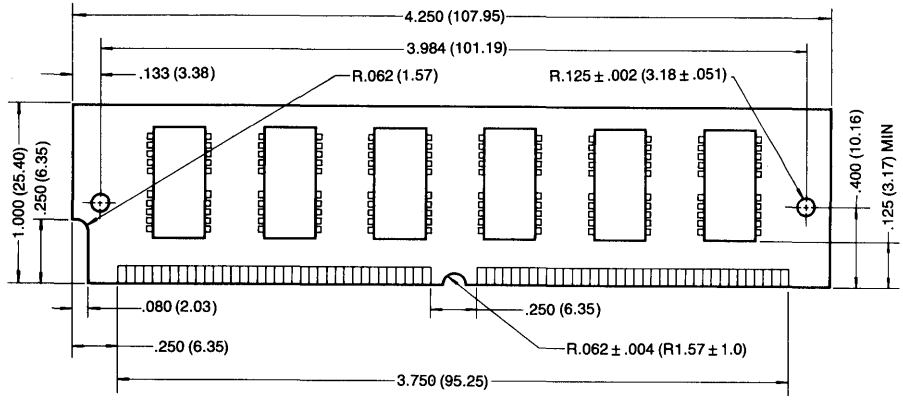
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



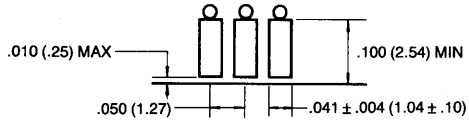
PACKAGE DIMENSIONS

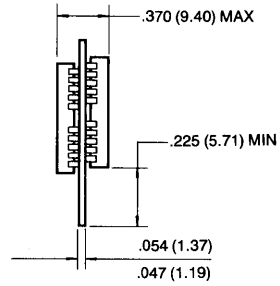
KMM5361000A/AG (1M×4 (SOJ)* 8+1M×1 (SOJ) *4)

Units: Inches (millimeters)

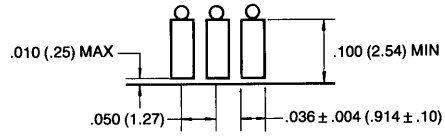


KMM5361000AG/A1G: DETAIL OF CONTACTS (Gold plating lead)

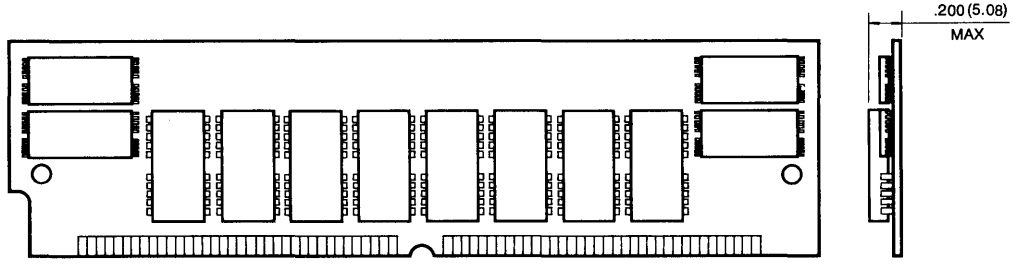




KMM5361000A/A1: DETAIL OF CONTACTS (Solder plating lead)



KMM5361000 A1/A1G (1M×4 (SOJ) *8+1M×1 (TSOPI) *4)



(The dimensions of this PCB are the same as those of the above one.)

Tolerances: ± .005 (.13) unless otherwise specified

2Mx32 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5322000AV- 7	70ns	20ns	130ns
KMM5322000AV- 8	80ns	20ns	150ns
KMM5322000AV-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

GENERAL DESCRIPTION

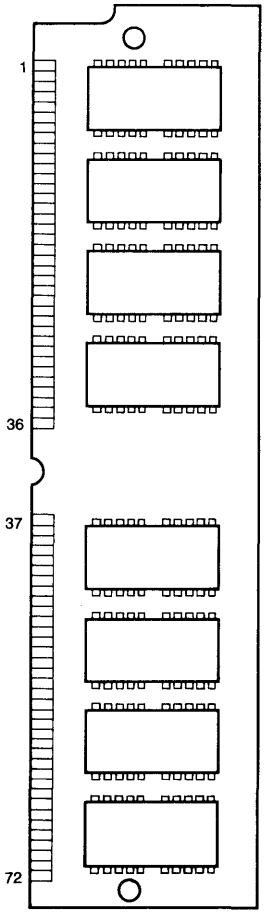
The Samsung KMM5322000AV is a 2M bits x 32 Dynamic RAM high, density memory module. The Samsung KMM5322000AV consist of sixteen CMOS 1M x 4 bit DRAMs in 20-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5322000AV is a Single in-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

3

PIN CONFIGURATIONS Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	NC
2	DQ_0	38	NC
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS_0}$
5	DQ_{19}	41	$\overline{CAS_2}$
6	DQ_2	42	$\overline{CAS_3}$
7	DQ_{20}	43	$\overline{CAS_1}$
8	DQ_3	44	$\overline{RAS_0}$
9	DQ_{21}	45	$\overline{RAS_1}$
10	V_{CC}	46	NC
11	NC	47	$\overline{W}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	$\overline{RAS_3}$	69	PD_3
34	$\overline{RAS_2}$	70	PD_4
35	NC	71	NC
36	NC	72	V_{SS}



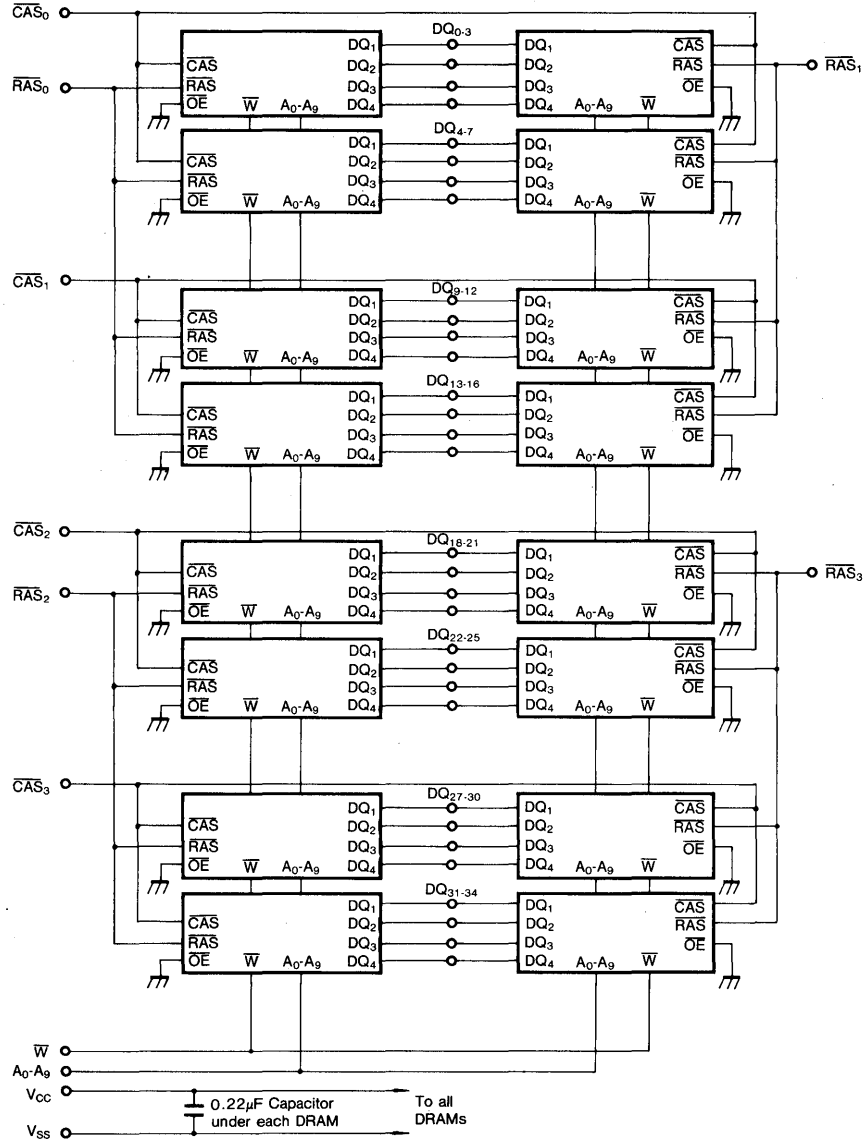
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{35} except $DQ_{8, 17, 26, 35}$)	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS_0}$-$\overline{RAS_3}$	Row Address Strobe
$\overline{CAS_0}$-$\overline{CAS_3}$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	NC	NC	NC
PD_2	NC	NC	NC
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	9.6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5322000AV- 7	I_{CC1}	—	856	mA
	KMM5322000AV- 8		—	776	mA
	KMM5322000AV-10		—	696	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	32	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM5322000AV- 7	I_{CC3}	—	856	mA
	KMM5322000AV- 8		—	776	mA
	KMM5322000-10		—	696	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5322000AV- 7	I_{CC4}	—	656	mA
	KMM5322000AV- 8		—	576	mA
	KMM5322000AV-10		—	496	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	16	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5322000AV- 7	I_{CC6}	—	856	mA
	KMM5322000AV- 8		—	776	mA
	KMM5322000AV-10		—	696	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−160	160	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A = 2.5°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	128	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	140	pF
Input Capacitance ($\overline{RAS}_0$-$\overline{RAS}_3$)	C_{IN3}	—	42	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	42	pF
Input/Output Capacitance ($DQ_{0\text{-}7, 9\text{-}16, 18\text{-}25, 27\text{-}34}$)	CDQ_1	—	29	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Standard Operation	Symbol	KMM5322000AV-7		KMM5322000AV-8		KMM5322000AV-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3, 4, 5
Access time from column address	t_{AA}		35		40		50	ns	3, 11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address-delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up-time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

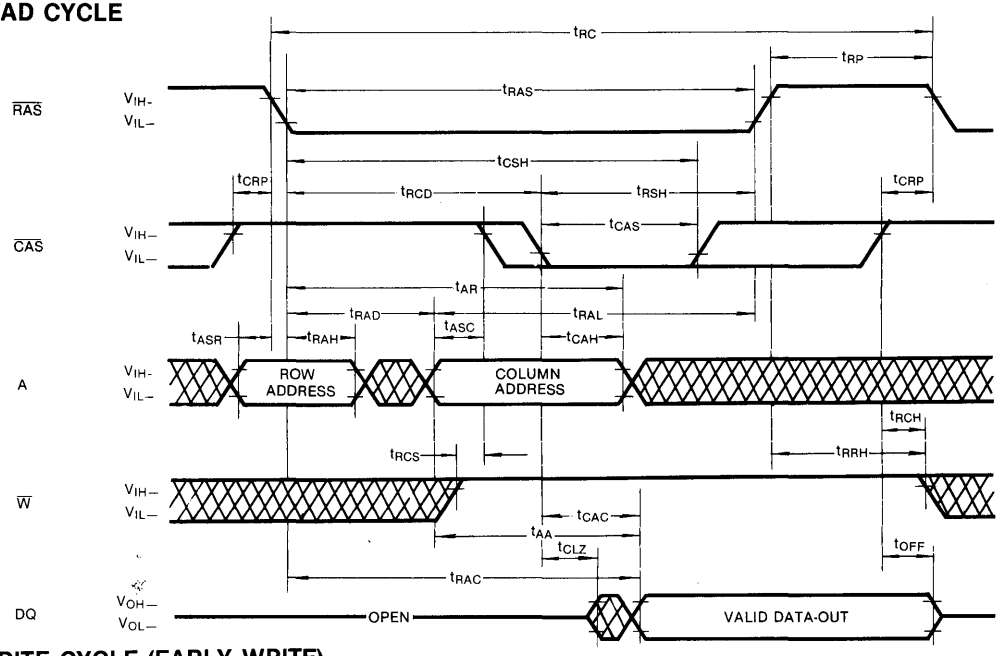
Standard Operation	Symbol	KMM5322000AV-7		KMM5322000AV-8		KMM5322000AV-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ Precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

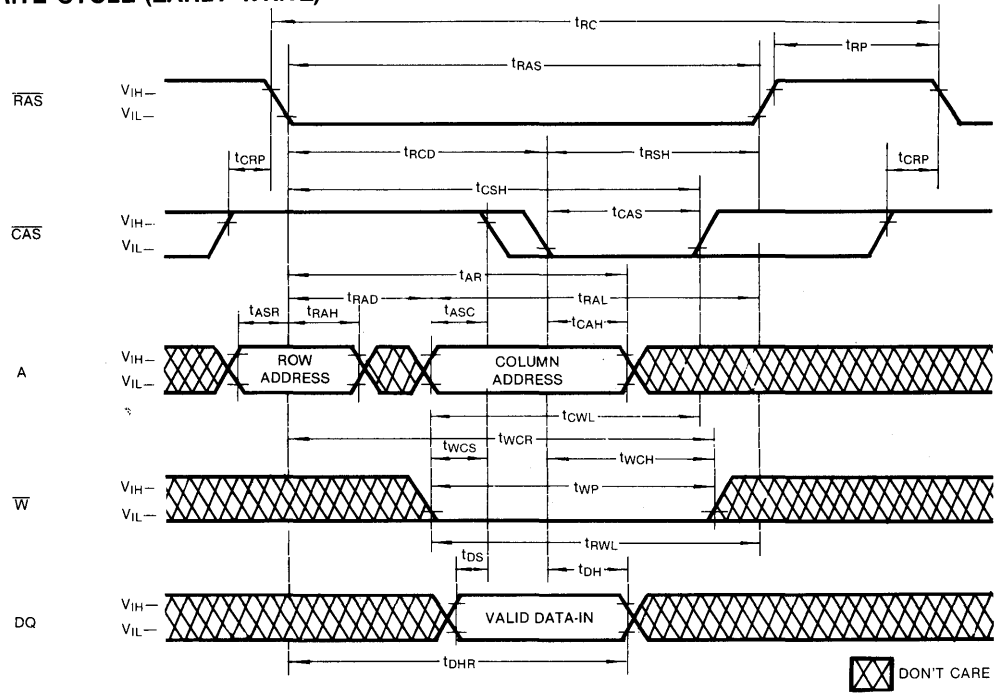
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH\,(min)}$ and $V_{IL\,(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH\,(min)}$ and $V_{IL\,(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD\,(max)}$ limit insures that $t_{RAC\,(max)}$ can be met. $t_{RCD\,(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \leq t_{RCD\,(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \leq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

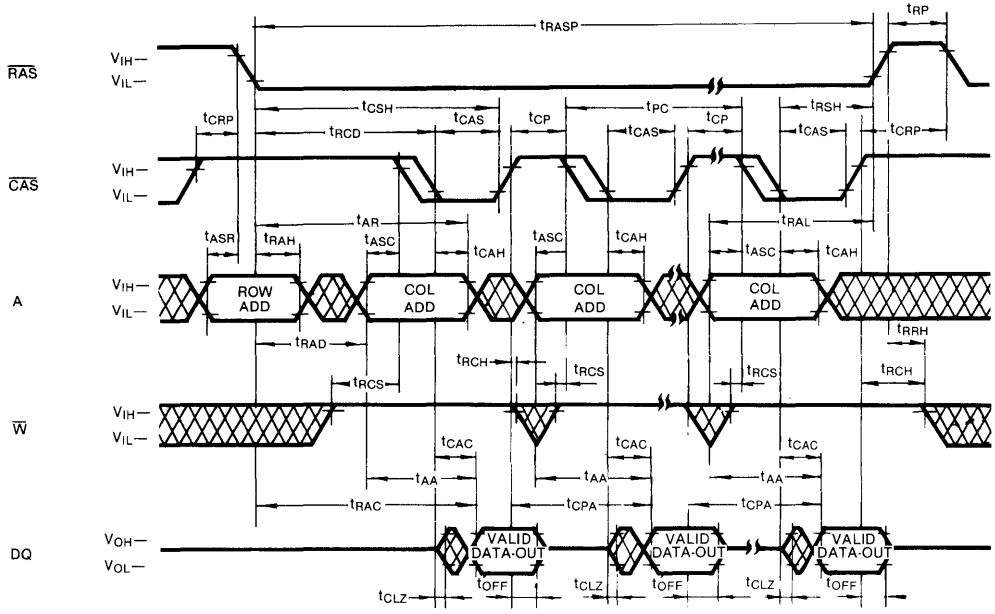


WRITE CYCLE (EARLY WRITE)

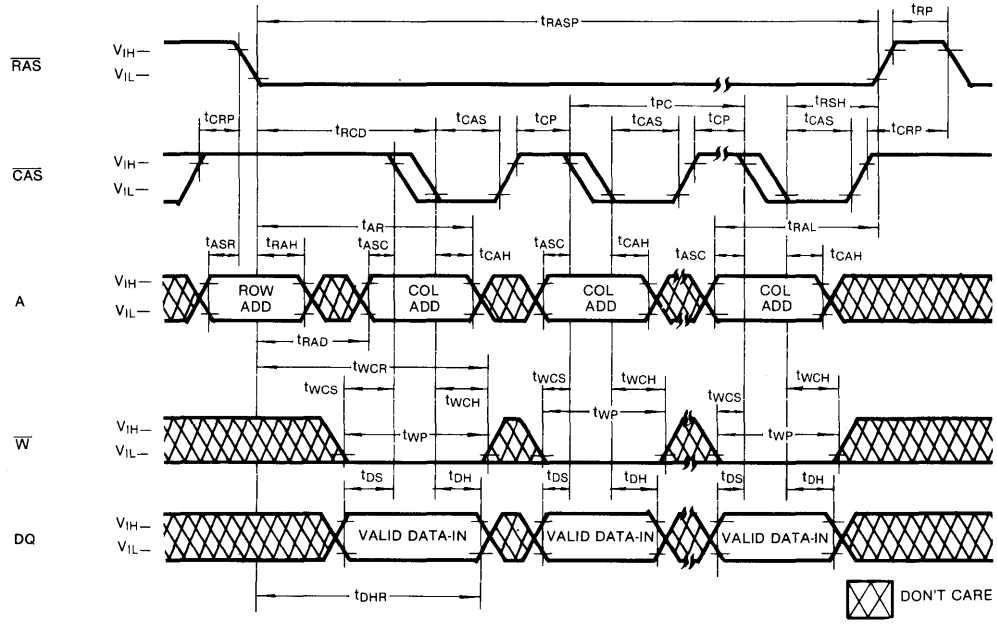


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



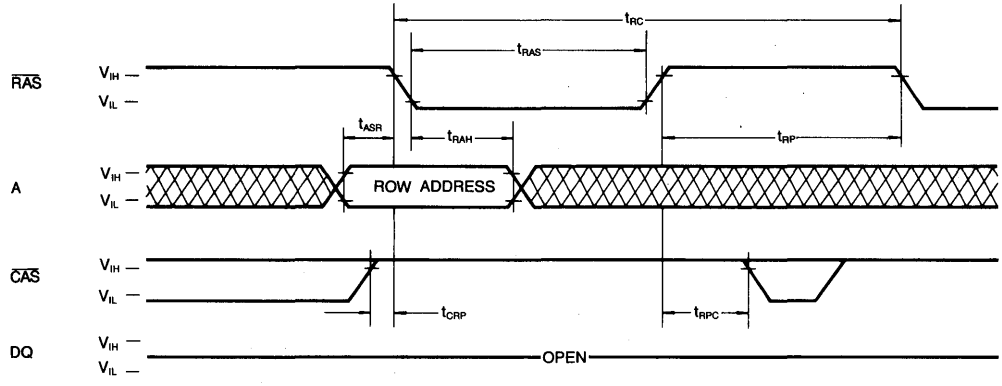
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

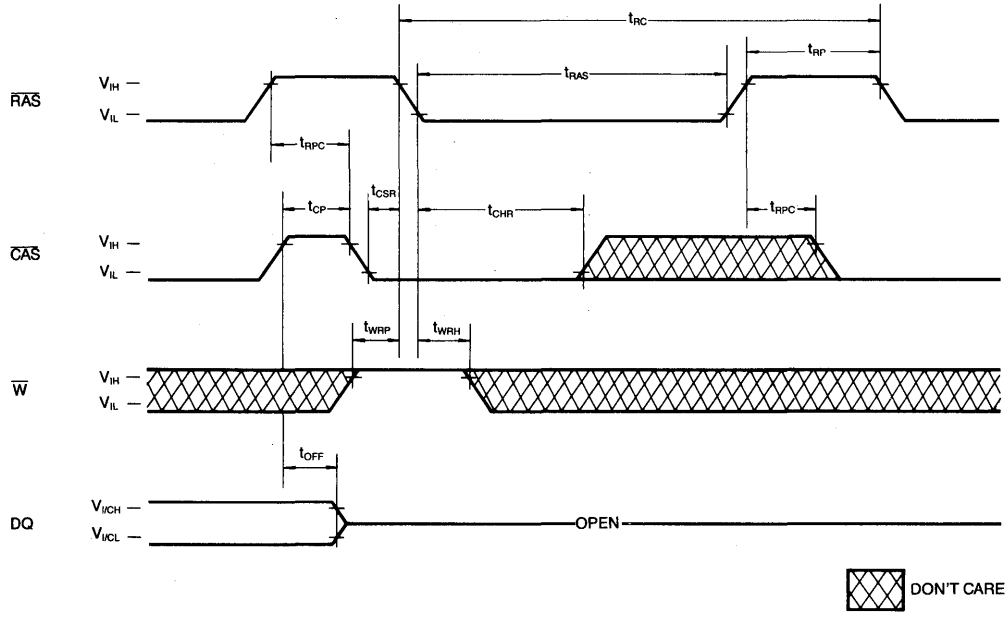
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



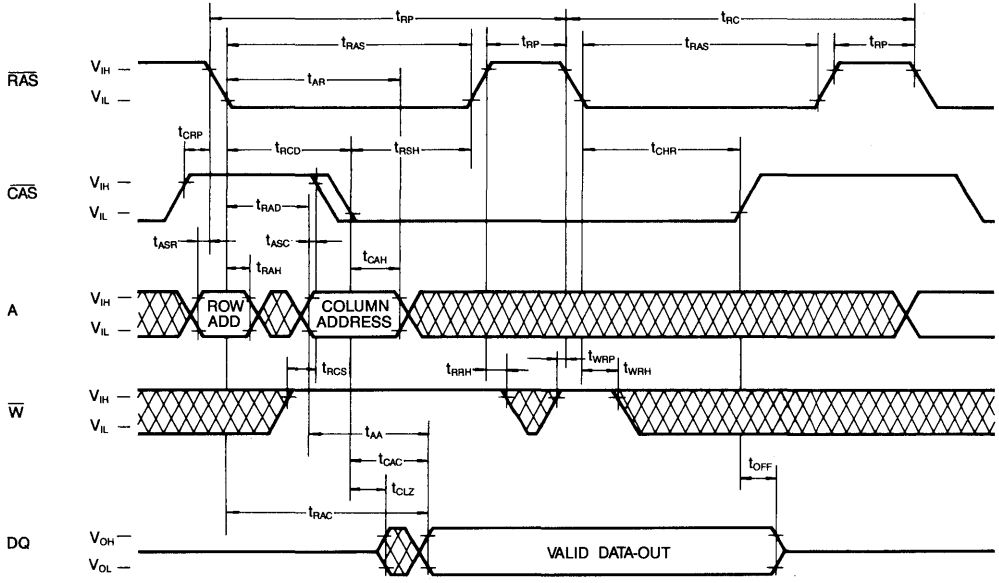
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

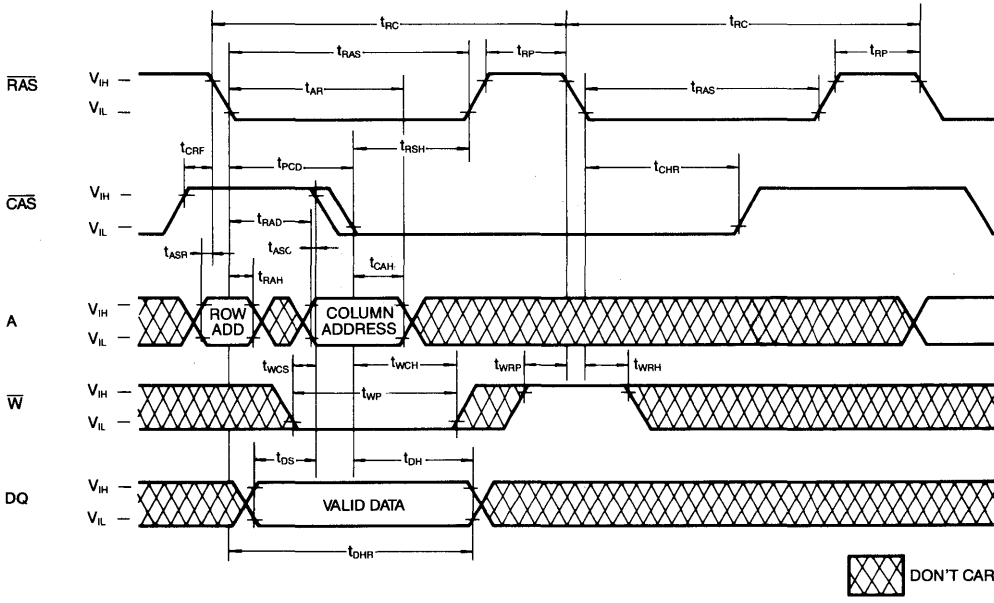


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

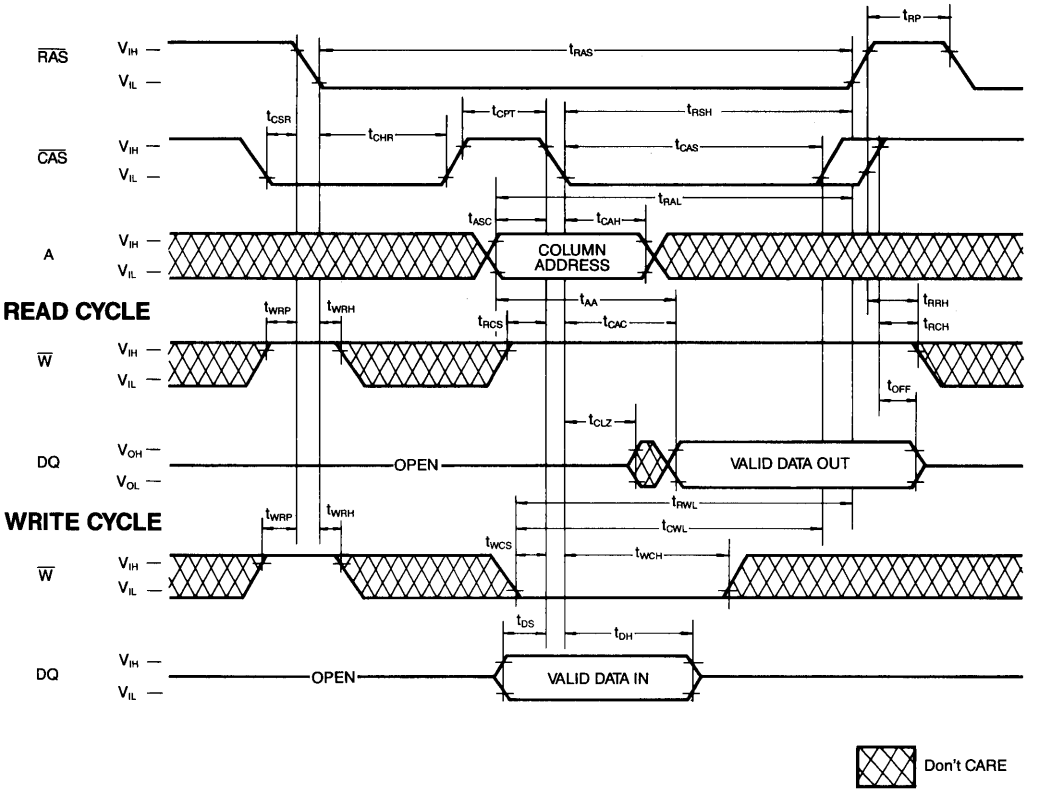


HIDDEN REFRESH CYCLE (WRITE)



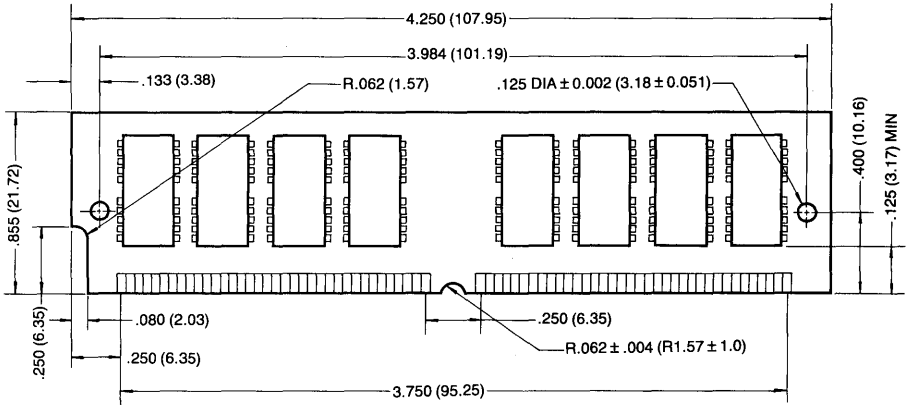
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

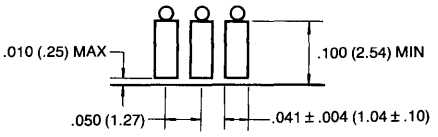


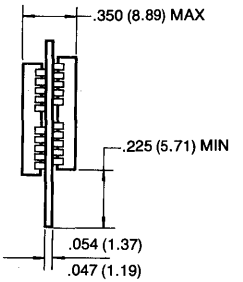
PACKAGE DIMENSIONS

Units: Inches (millimeters)

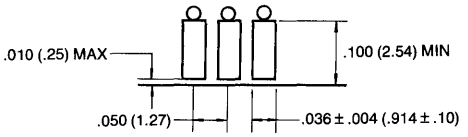


KMM5322000AVG DETAIL OF CONTACTS (Gold plating lead)





KMM5322000AV DETAIL OF CONTACTS (Solder plating lead)



Tolerances: ± .005 (.13) unless otherwise specified

2M×36 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5362000A- 7	70ns	20ns	130ns
KMM5362000A- 8	80ns	20ns	150ns
KMM5362000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**

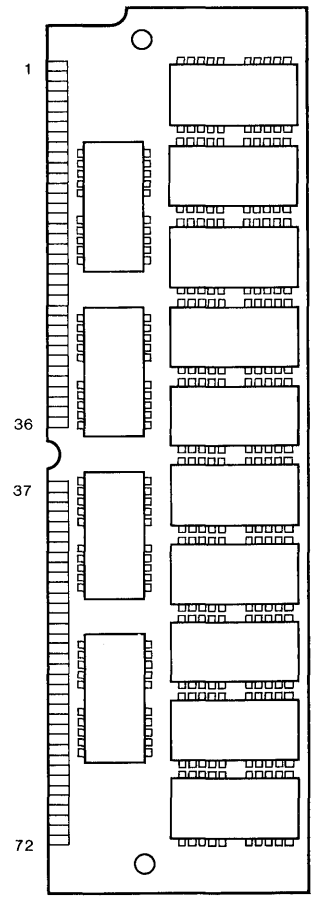
GENERAL DESCRIPTION

The Samsung KMM5362000A is a 2M bits×36 Dynamic RAM high density memory module. The Samsung KMM5362000A consist of sixteen CMOS 1M×4 bit DRAMs in 20-pin SOJ package and eight CMOS 1M×1 bit DRAMs in 20-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5362000A is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS}_0$
5	DQ_{19}	41	$\overline{CAS}_2$
6	DQ_2	42	$\overline{CAS}_3$
7	DQ_{20}	43	$\overline{CAS}_1$
8	DQ_3	44	$\overline{RAS}_0$
9	DQ_{21}	45	$\overline{RAS}_1$
10	V_{CC}	46	NC
11	NC	47	$\overline{W}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	$\overline{RAS}_3$	69	PD_3
34	$\overline{RAS}_2$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}



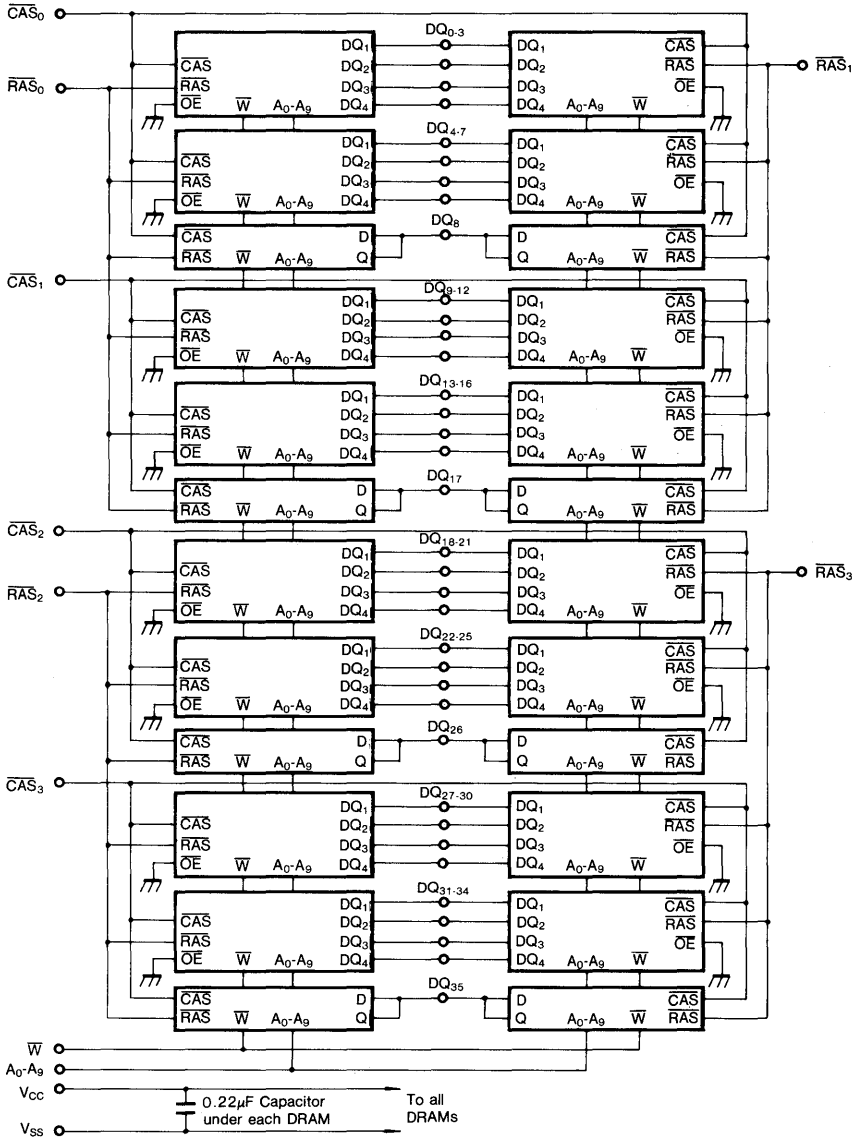
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$-$\overline{RAS}_3$	Row Address Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	NC	NC	NC
PD_2	NC	NC	NC
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	14.4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5362000A- 7	I_{CC1}	—	1184	mA
	KMM5362000A- 8		—	1064	mA
	KMM5362000A-10		—	944	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	48	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM5362000A- 7	I_{CC3}	—	1184	mA
	KMM5362000A- 8		—	1064	mA
	KMM5362000A-10		—	944	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5362000A- 7	I_{CC4}	—	904	mA
	KMM5362000A- 8		—	784	mA
	KMM5362000A-10		—	664	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	24	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5362000A- 7	I_{CC6}	—	1184	mA
	KMM5362000A- 8		—	1064	mA
	KMM5362000A-10		—	944	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−240	240	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	161	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	168	pF
Input Capacitance ($\overline{RAS}_0$-$\overline{RAS}_3$)	C_{IN3}	—	42	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_3$)	C_{IN4}	—	42	pF
Input/Output Capacitance ($DQ_{0\text{-}7,9\text{-}16,18\text{-}25,27\text{-}34}$)	CDQ_1	—	29	pF
Input/Output Capacitance ($DQ_{8,17,26,35}$)	CDQ_2	—	39	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM5362000A-7		KMM5362000A-8		KMM5362000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	

AC CHARACTEROSTOCS (Continued)

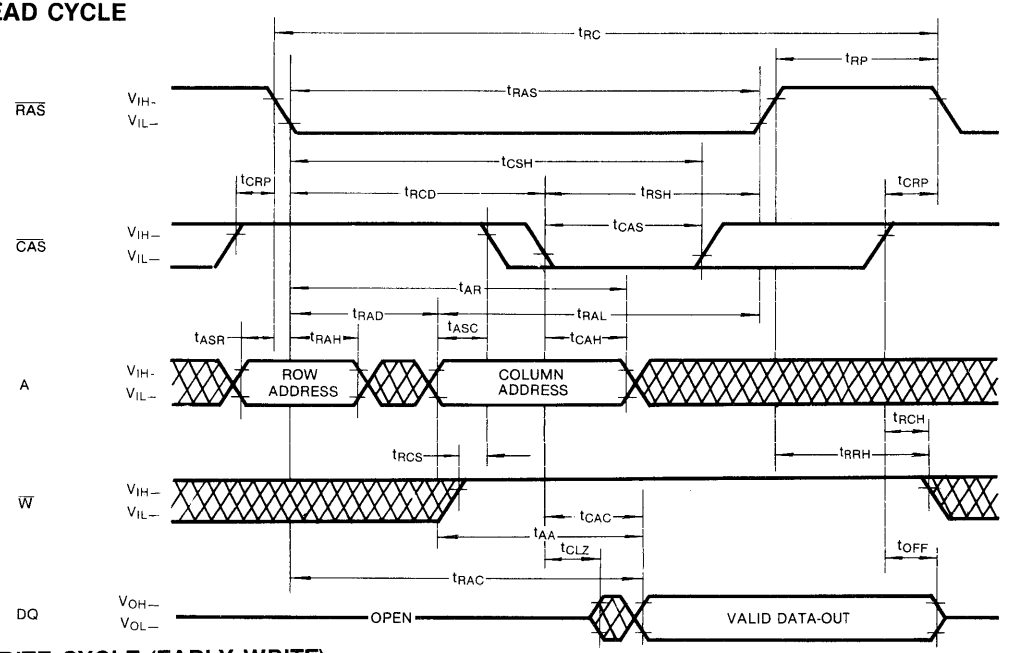
Standard Operation	Symbol	KMM5362000A-7		KMM5362000A-8		KMM5362000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

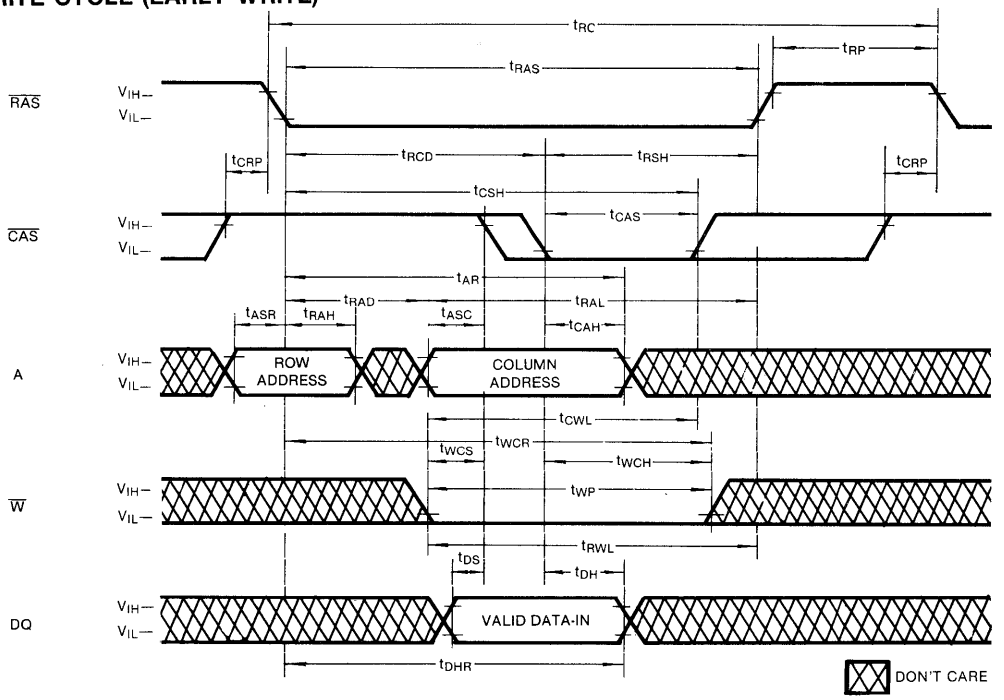
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

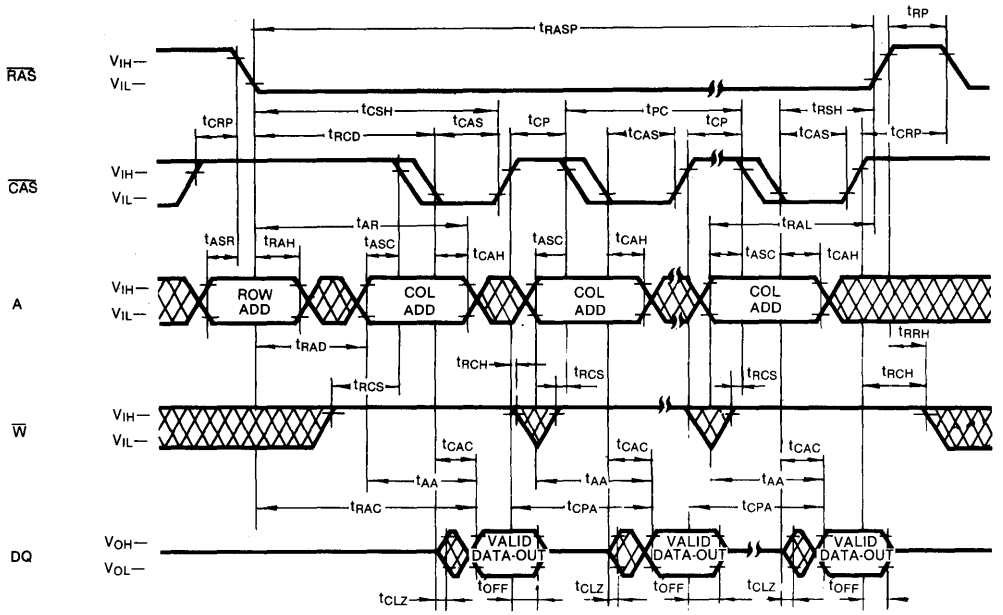


WRITE CYCLE (EARLY WRITE)

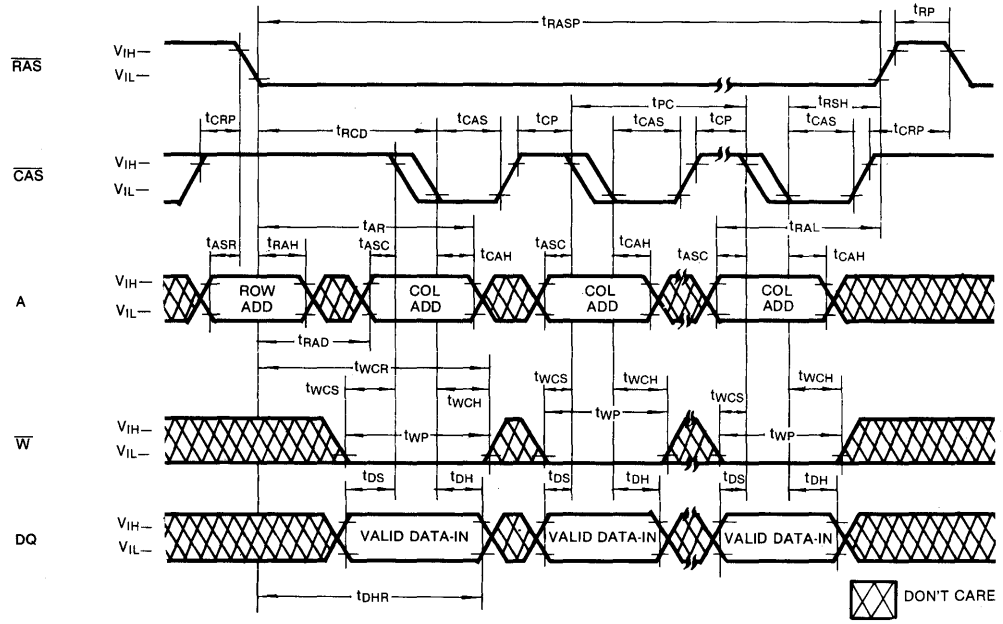


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



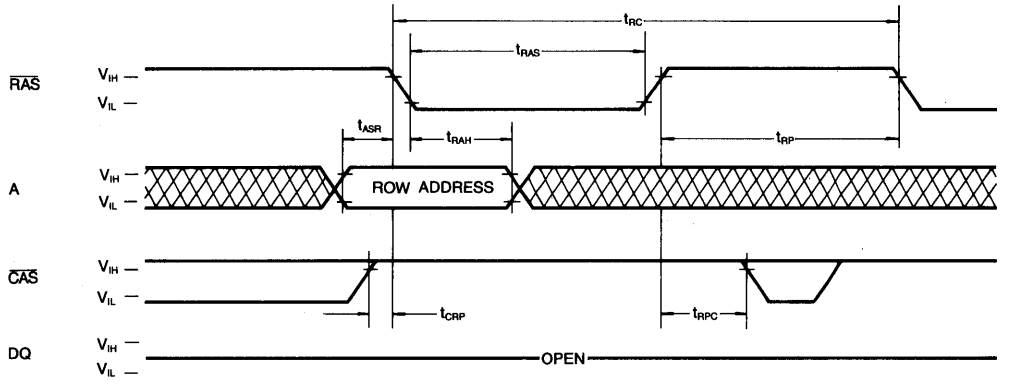
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

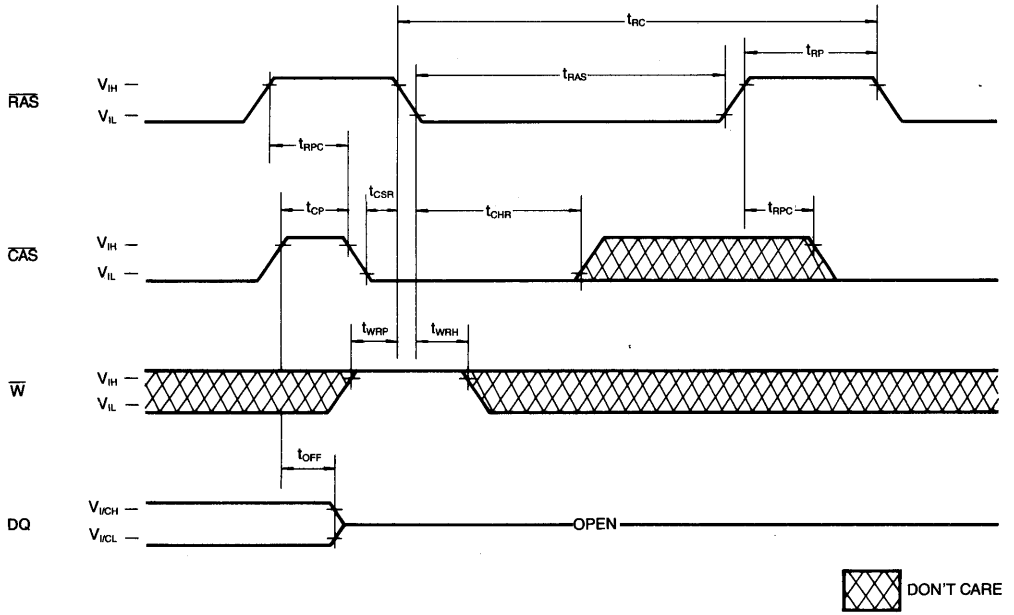
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$=Don't Care



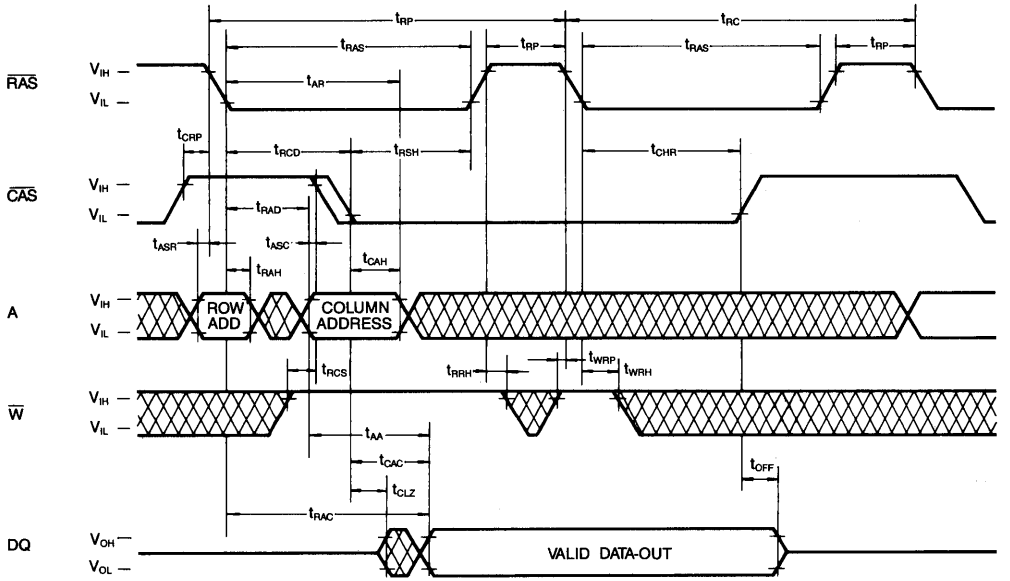
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

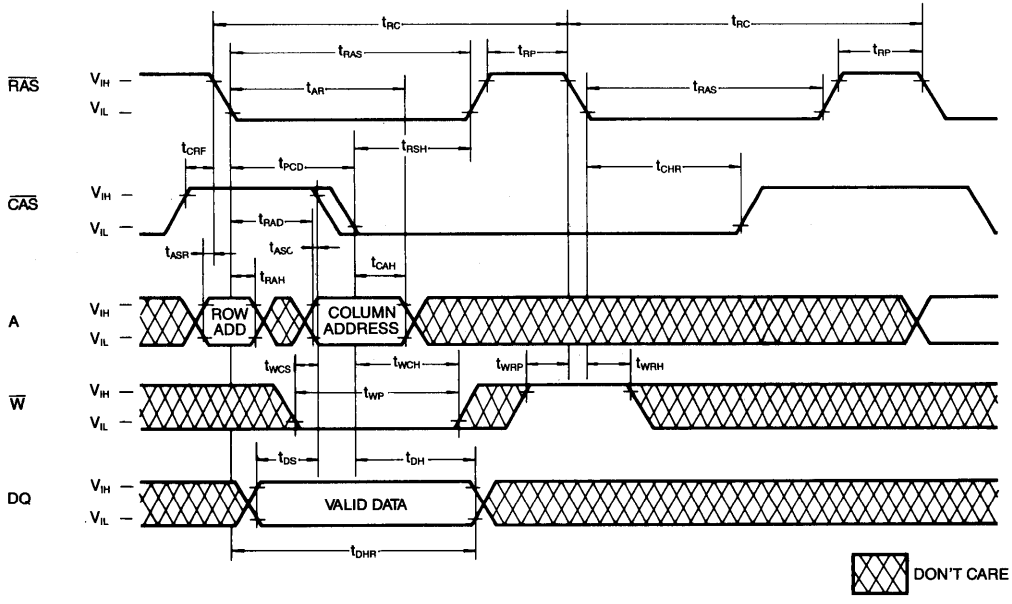


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

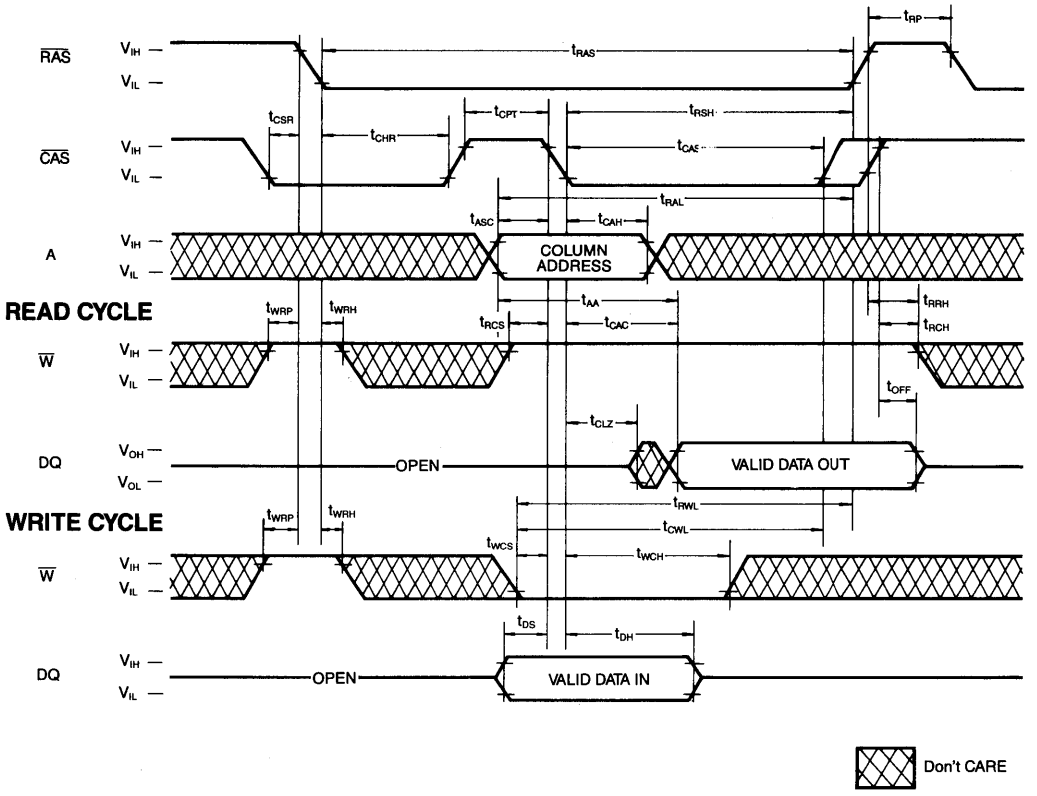


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

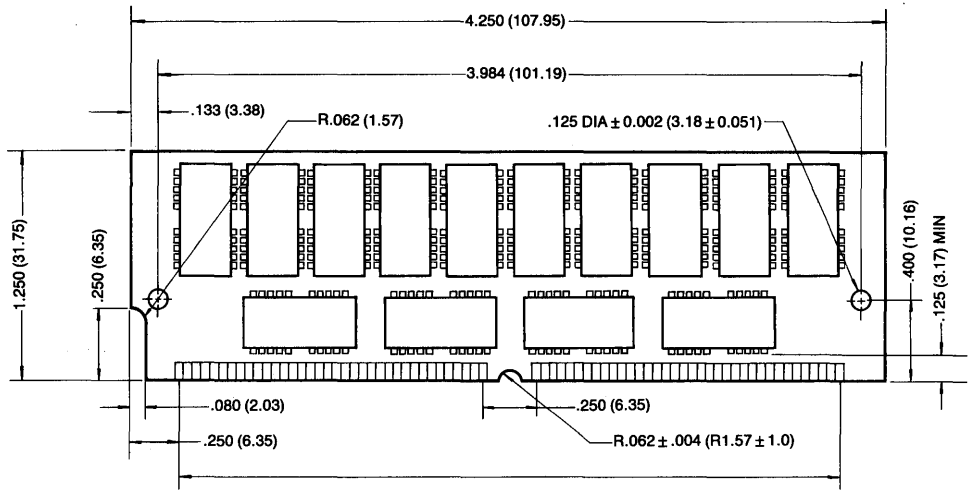
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



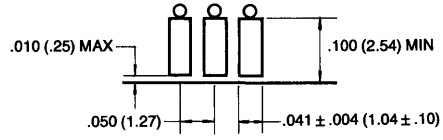
PACKAGE DIMENSIONS

KMM5362000A/AG (1M×4 (SOJ)*16+1M×1 (SOJ)*8)

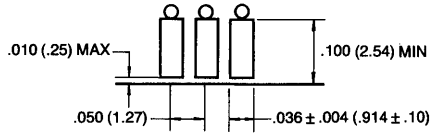
Units: Inches (millimeters)

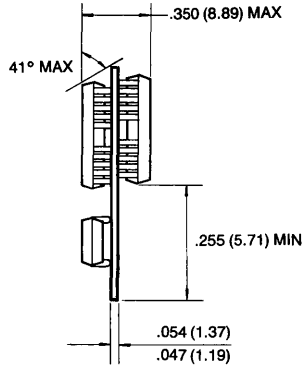


KMM5362000AG/A1G DETAIL OF CONTACTS (Gold plating lead)

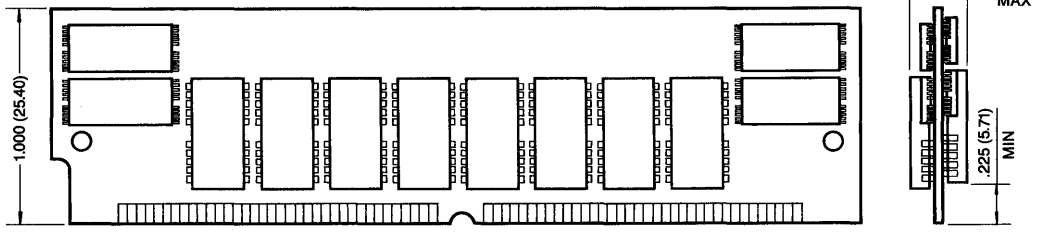


KMM5362000A/A1 DETAIL OF CONTACTS (Solder plating lead)





KMM5362000A1/A1G (1M×4 (SOJ)* 16+1M×1 (TSOPI)* 8)



(The dimensions of this PCB are the same as those of the above one)

Tolerances: ± .005 (.13) unless otherwise specified

1M×40 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5401000A- 7	70ns	20ns	130ns
KMM5401000A- 8	80ns	20ns	150ns
KMM5401000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cydes/16ms refresh**
- **JEDEC standard pinout**

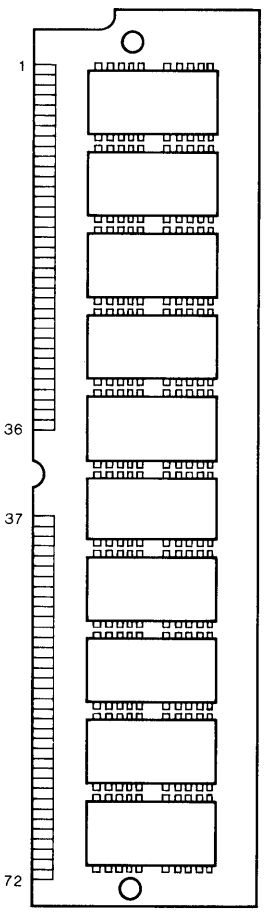
GENERAL DESCRIPTION

The Samsung KMM5401000A is a 1M bits × 40 Dynamic RAM high density memory module. The Samsung KMM5401000A consist of ten CMOS 1M × 4 bit DRAMs in 20-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM.

The KMM5401000A is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ_{19}
2	DQ_0	38	DQ_{20}
3	DQ_1	39	V_{SS}
4	DQ_2	40	$\overline{CAS}_0$
5	DQ_3	41	NC
6	DQ_4	42	NC
7	DQ_5	43	NC
8	DQ_6	44	$\overline{RAS}_0$
9	DQ_7	45	NC
10	V_{CC}	46	DQ_{21}
11	NC	47	$\overline{W}$
12	A_0	48	V_{SS}
13	A_1	49	DQ_{22}
14	A_2	50	DQ_{23}
15	A_3	51	DQ_{24}
16	A_4	52	DQ_{25}
17	A_5	53	DQ_{26}
18	A_6	54	DQ_{27}
19	$\overline{OE}$	55	DQ_{28}
20	DQ_8	56	DQ_{29}
21	DQ_9	57	DQ_{30}
22	DQ_{10}	58	DQ_{31}
23	DQ_{11}	59	V_{CC}
24	DQ_{12}	60	DQ_{32}
25	DQ_{13}	61	DQ_{33}
26	DQ_{14}	62	DQ_{34}
27	DQ_{15}	63	DQ_{35}
28	A_7	64	DQ_{36}
29	DQ_{16}	65	DQ_{37}
30	V_{CC}	66	DQ_{38}
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	NC	70	PD_4
35	DQ_{17}	71	DQ_{39}
36	DQ_{18}	72	V_{SS}



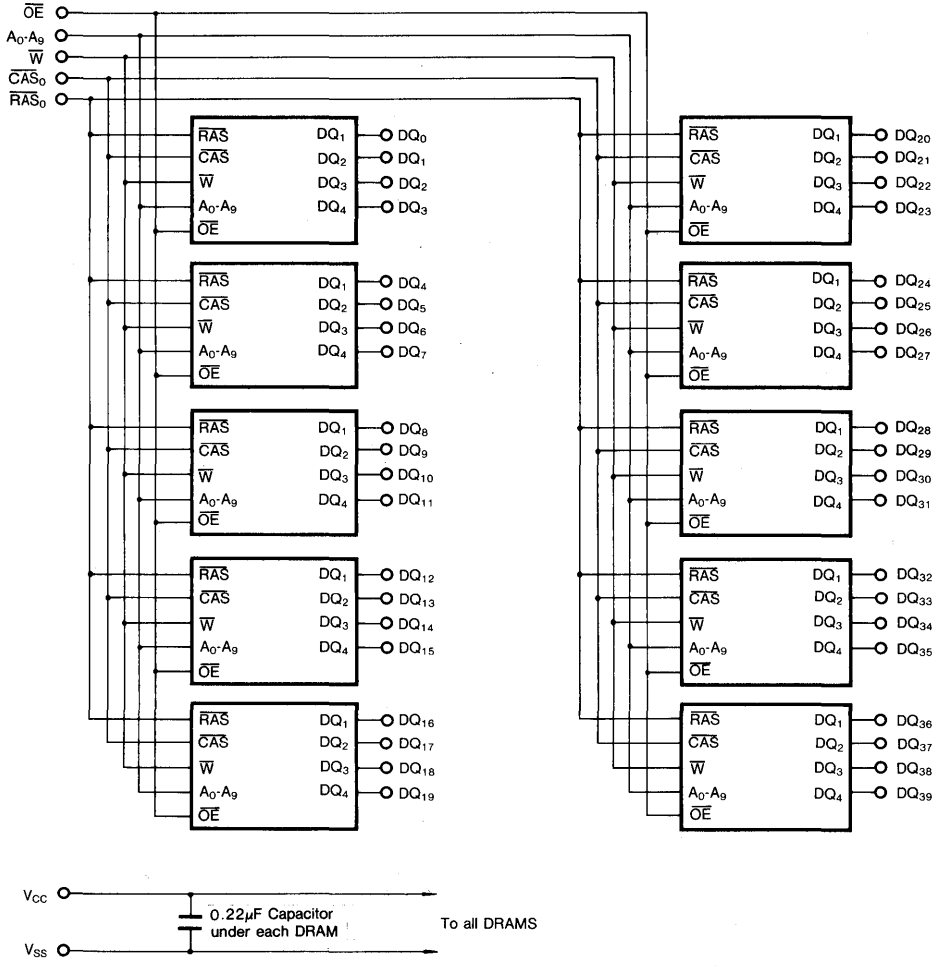
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{39}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$	Row Address Strobe
$\overline{CAS}_0$	Column Address Strobe
$\overline{OE}$	Output Enable
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	V_{SS}	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	6	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5401000A- 7	I_{CC1}	—	1050	mA
	KMM5401000A- 8		—	950	mA
	KMM5401000A-10		—	850	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	20	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min)	KMM5401000A- 7	I_{CC3}	—	1050	mA
	KMM5401000A- 8		—	950	mA
	KMM5401000A-10		—	850	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5401000A- 7	I_{CC4}	—	800	mA
	KMM5401000A- 8		—	700	mA
	KMM5401000A-10		—	600	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	10	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5401000A- 7	I_{CC6}	—	1050	mA
	KMM5401000A- 8		—	950	mA
	KMM5401000A-10		—	850	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−100	100	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	70	pF
Input Capacitance ($\overline{W}$, $\overline{OE}$)	C_{IN2}	—	80	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{CAS}_0$)	C_{IN3}	—	80	pF
Input/Output Capacitance (DQ_0-DQ_{39})	CDQ_1	—	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM5401000A-7		KMM5401000A-8		KMM5401000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

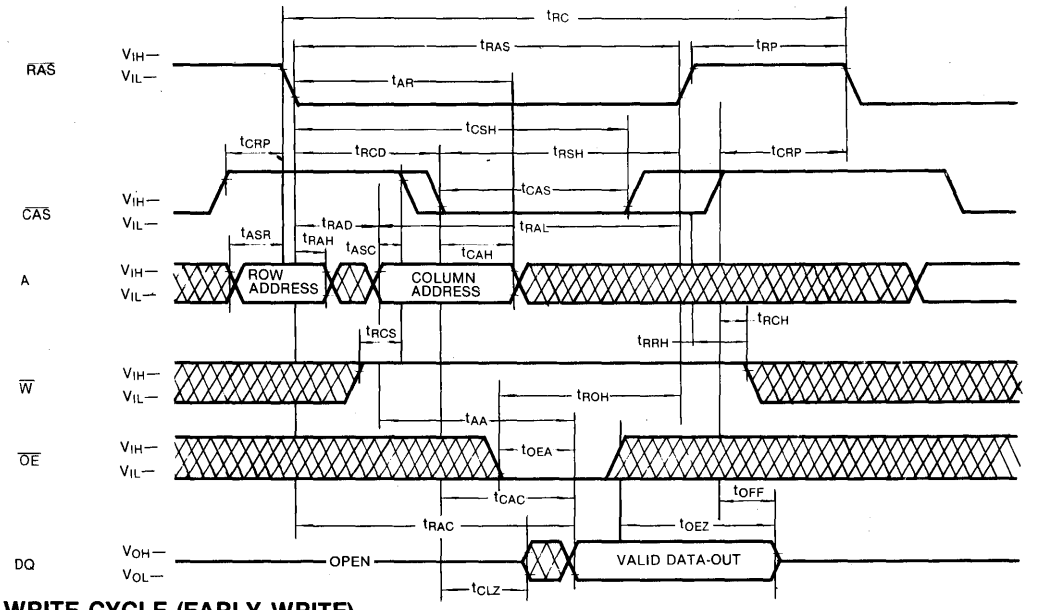
Standard Operation	Symbol	KMM5401000A-7		KMM5401000A-8		KMM5401000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

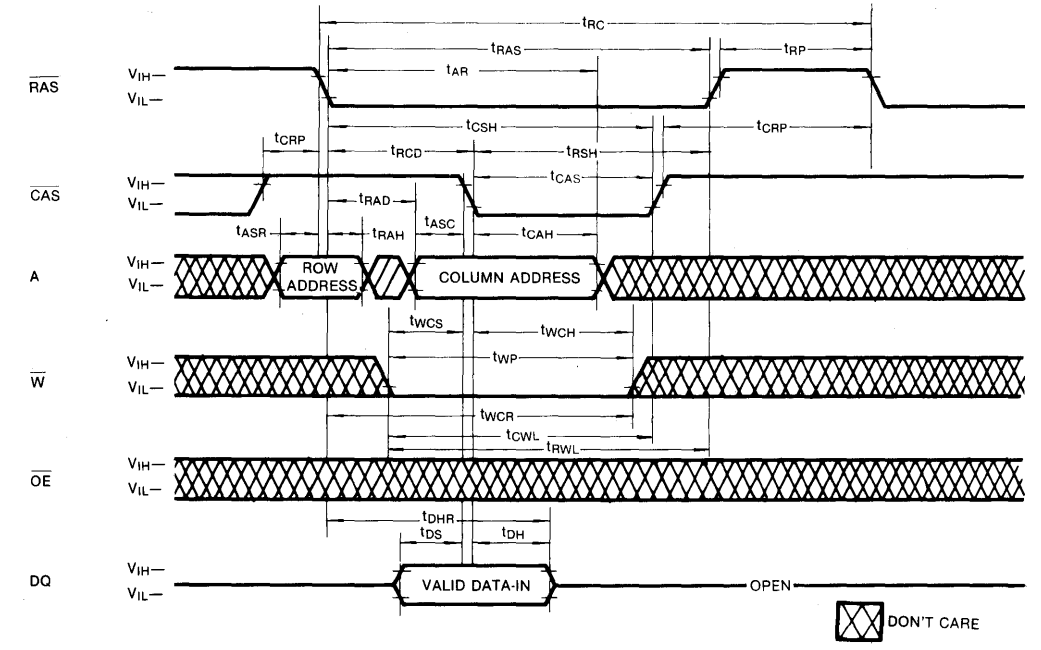
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAC}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

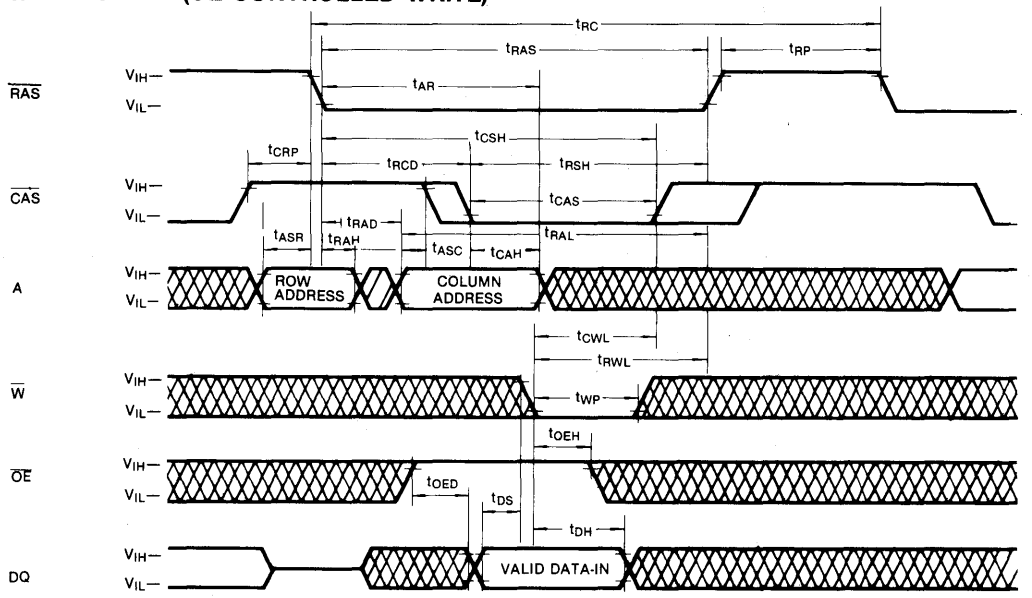


WRITE CYCLE (EARLY WRITE)

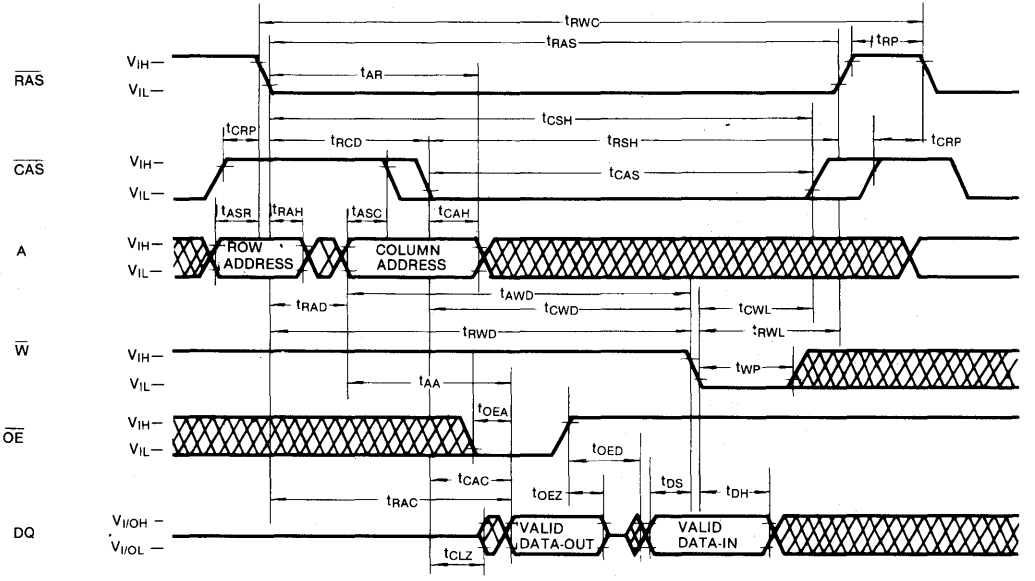


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



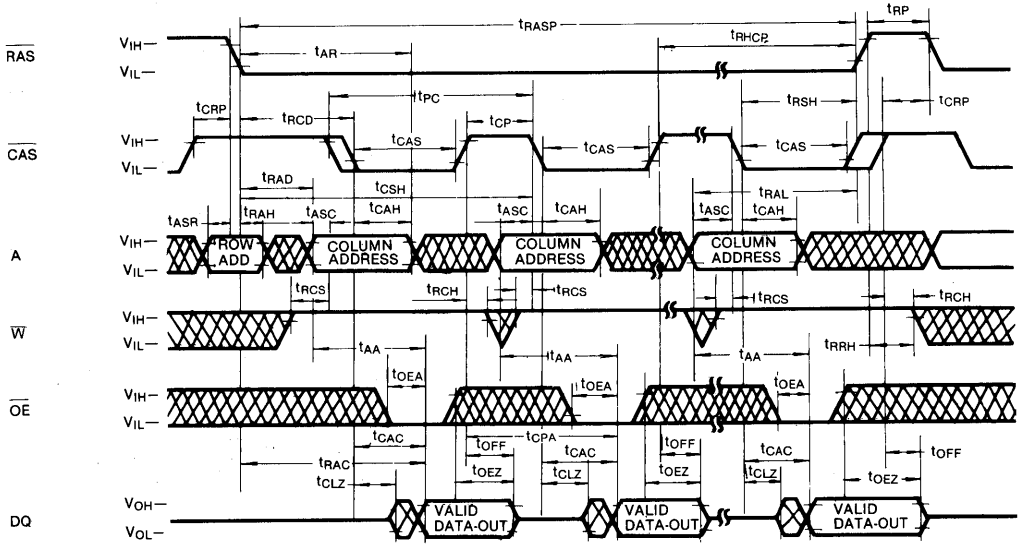
READ-MODIFY-WRITE CYCLE



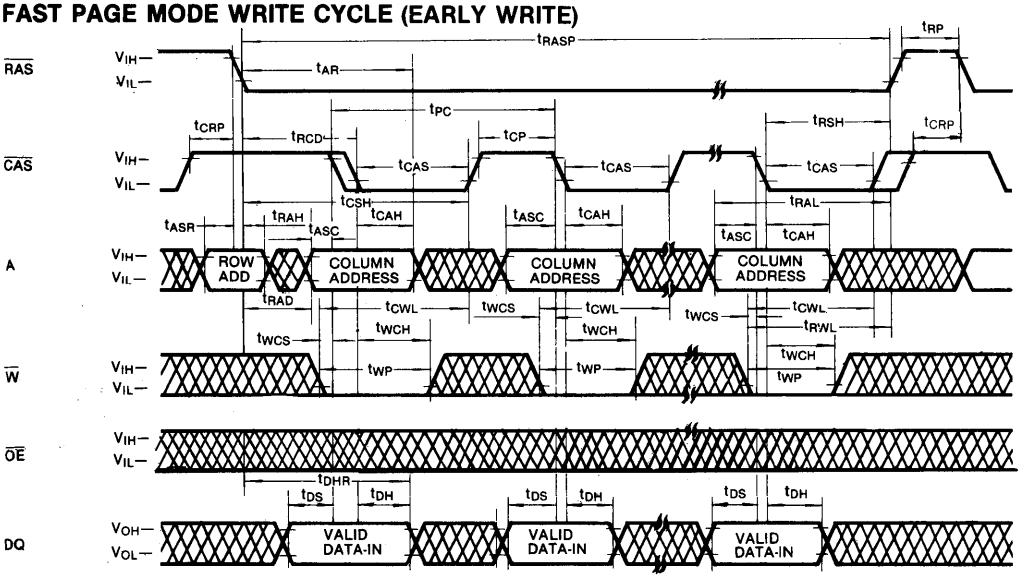
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



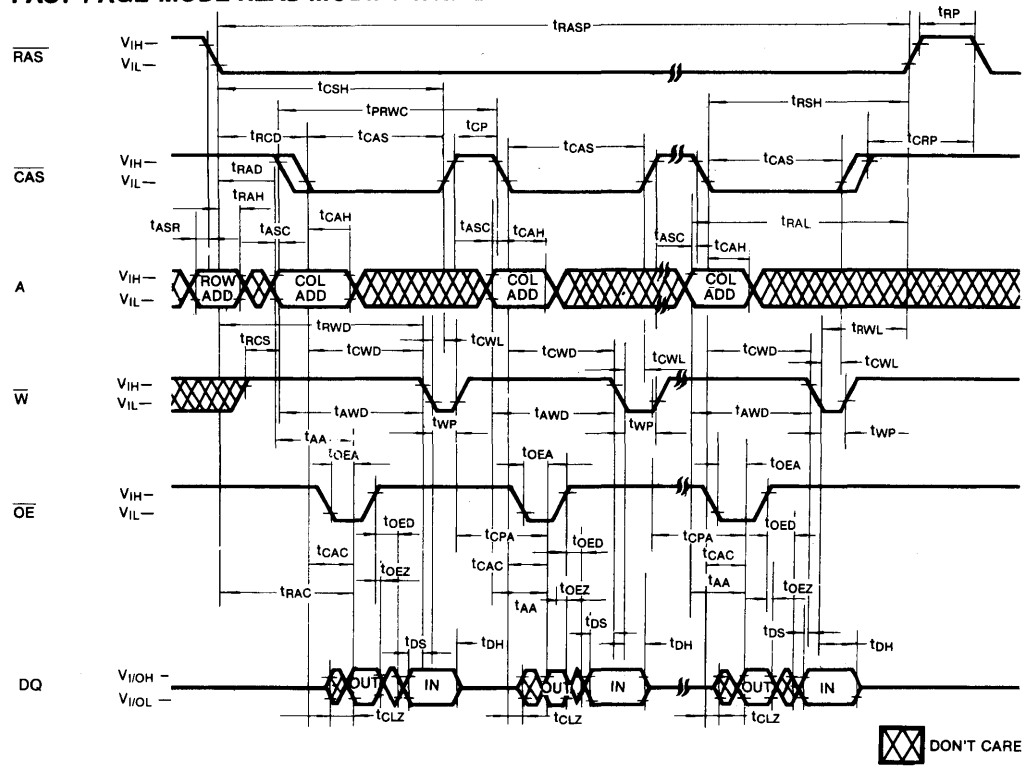
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

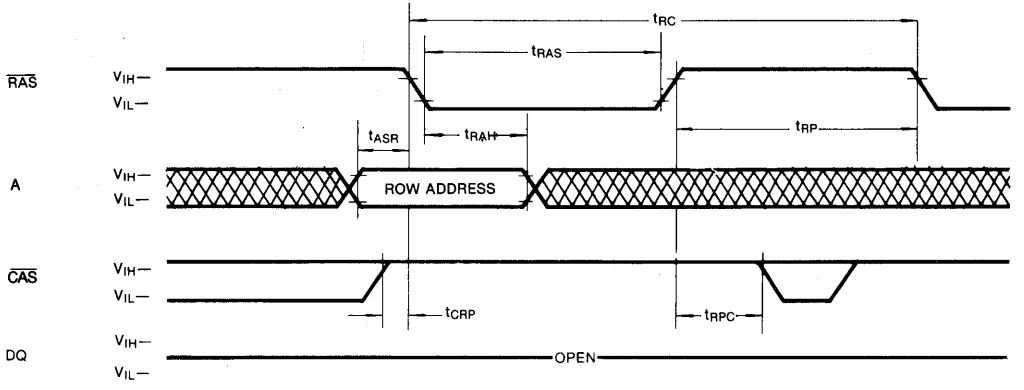
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

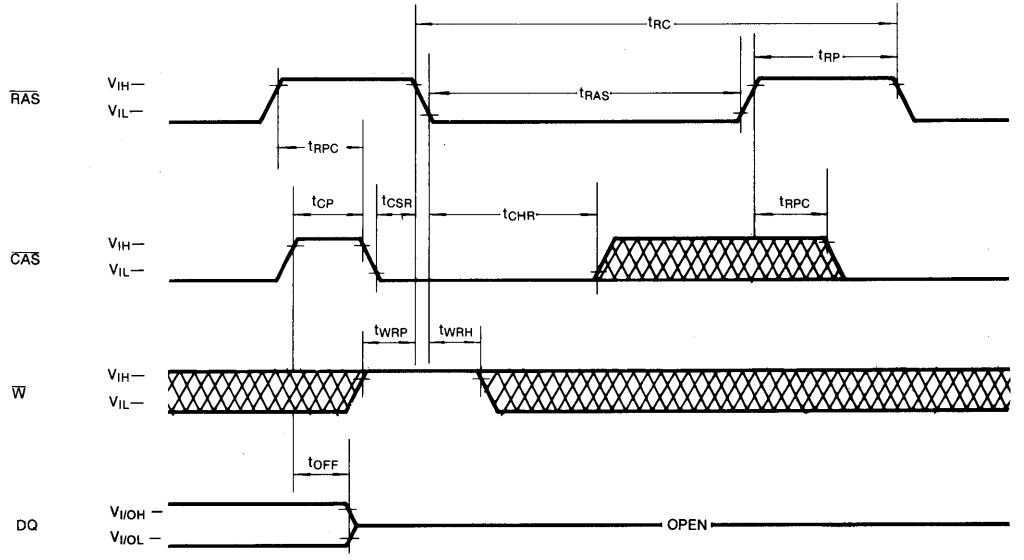
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



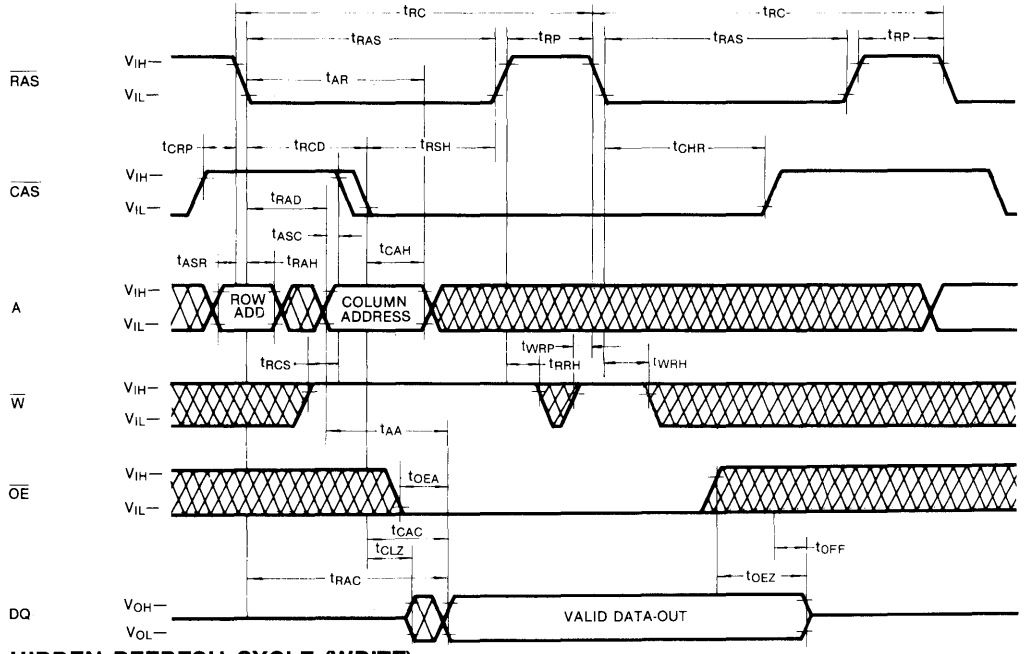
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

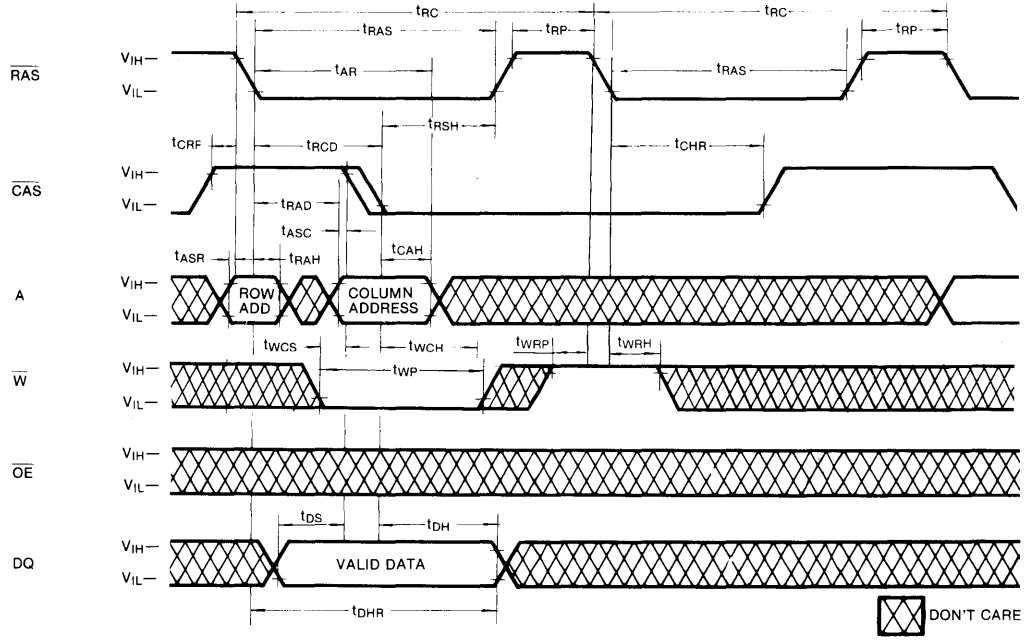


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

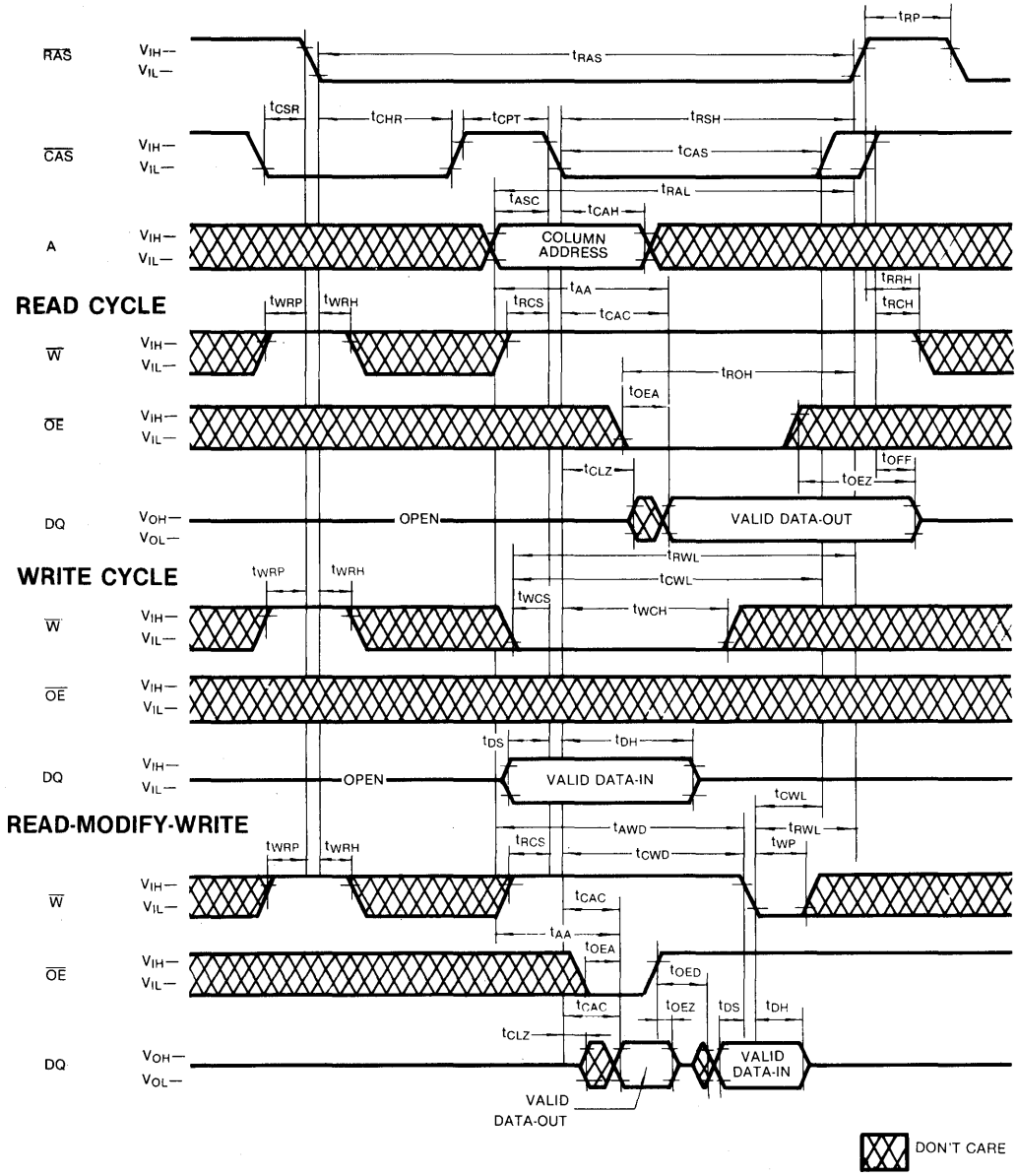


HIDDEN REFRESH CYCLE (WRITE)



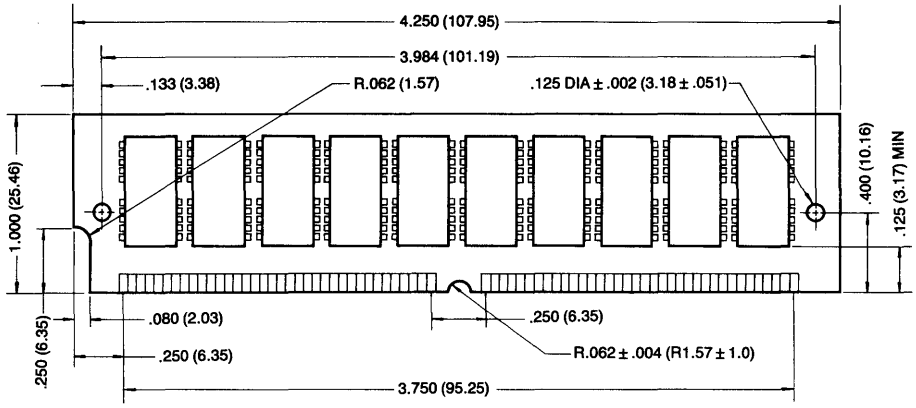
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

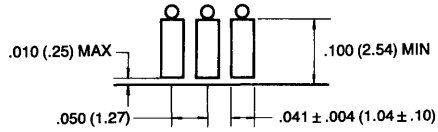


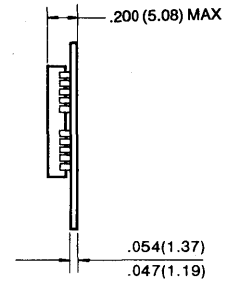
PACKAGE DIMENSIONS

Units: Inches (millimeters)

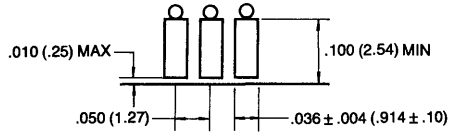


KMM5401000AG DETAIL OF CONTACTS (Gold plating lead)





KMM5401000A DETAIL OF CONTACTS (Solder plating lead)



Tolerances: ± .005 (.13) unless otherwise specified

2MX40 DRAM SIMM Memory Module

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KMM5402000A- 7	70ns	20ns	130ns
KMM5402000A- 8	80ns	20ns	150ns
KMM5402000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Single +5V±10% power supply**
- **1024 cydes/16ms refresh**
- **JEDEC standard pinout**

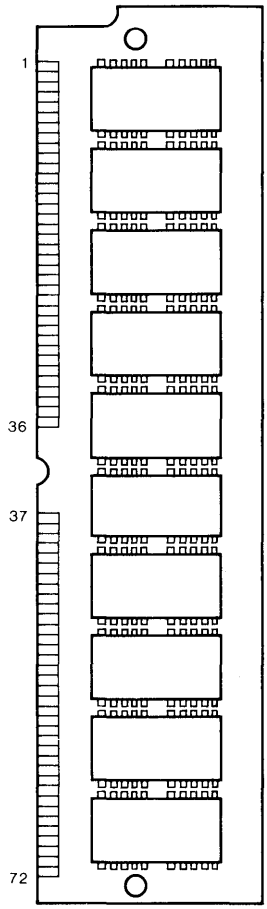
GENERAL DESCRIPTION

The Samsung KMM5402000A is a 2M bits X 40 Dynamic RAM high density memory module. The Samsung KMM5402000A consist of twenty CMOS 1M X 4 bit DRAMs in 20-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22μF decoupling capacitor is mounted under each DRAM of front side.

The KMM5402000A is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PIN CONFIGURATIONS (Front View)

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	DQ_{19}
2	DQ_0	38	DQ_{20}
3	DQ_1	39	V_{SS}
4	DQ_2	40	$\overline{CAS}_0$
5	DQ_3	41	NC
6	DQ_4	42	NC
7	DQ_5	43	$\overline{CAS}_1$
8	DQ_6	44	$\overline{RAS}_0$
9	DQ_7	45	$\overline{RAS}_1$
10	V_{CC}	46	DQ_{21}
11	NC	47	$\overline{W}$
12	A_0	48	V_{SS}
13	A_1	49	DQ_{22}
14	A_2	50	DQ_{23}
15	A_3	51	DQ_{24}
16	A_4	52	DQ_{25}
17	A_5	53	DQ_{26}
18	A_6	54	DQ_{27}
19	[illegible]	55	DQ_{28}
20	[illegible]	56	DQ_{29}
21	DQ_9	57	DQ_{30}
22	DQ_{10}	58	DQ_{31}
23	DQ_{11}	59	V_{CC}
24	DQ_{12}	60	DQ_{32}
25	DQ_{13}	61	DQ_{33}
26	DQ_{14}	62	DQ_{34}
27	DQ_{15}	63	DQ_{35}
28	A_7	64	DQ_{36}
29	DQ_{16}	65	DQ_{37}
30	V_{CC}	66	DQ_{38}
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	NC	70	PD_4
35	DQ_{17}	71	DQ_{39}
36	DQ_{18}	72	V_{SS}



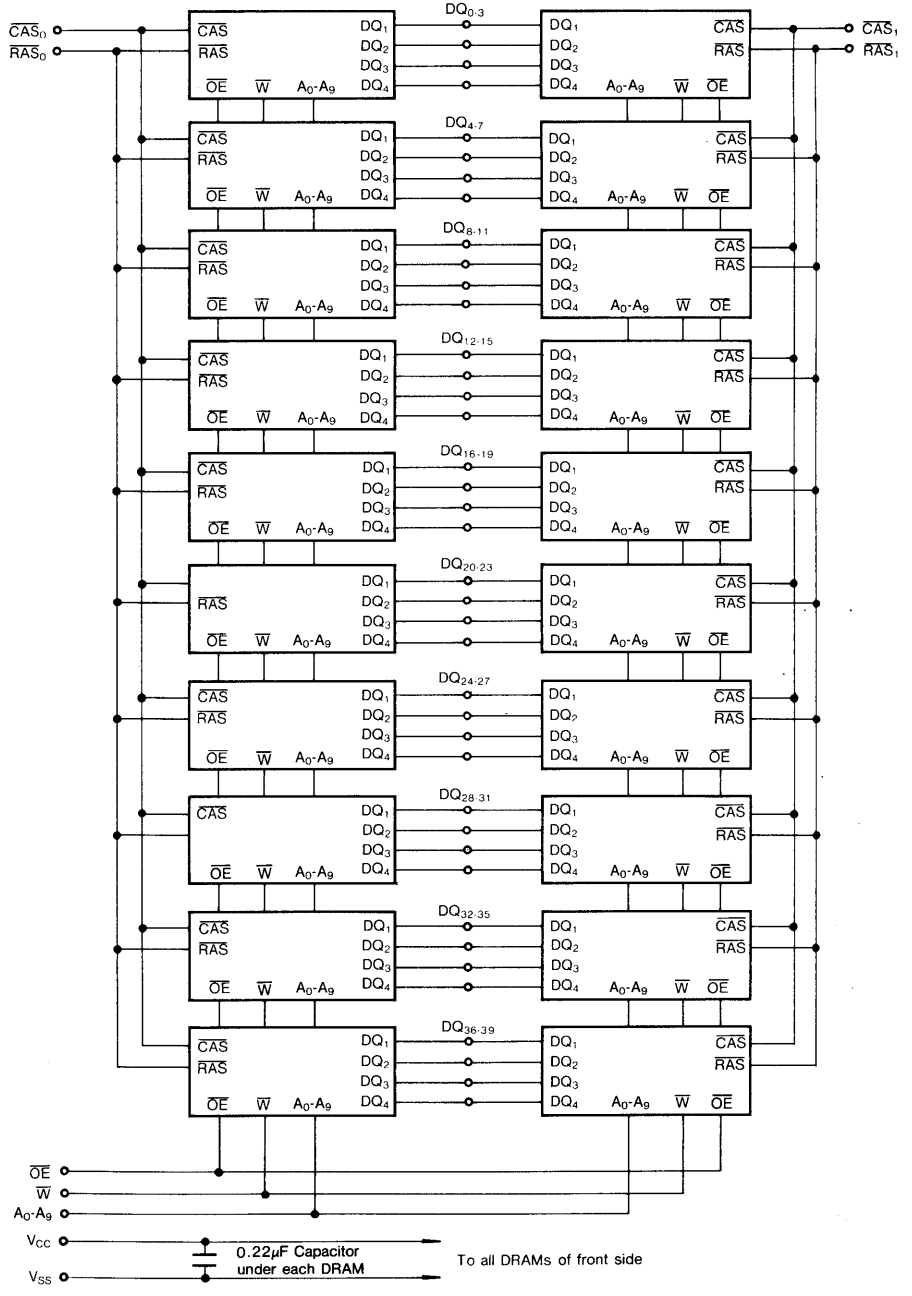
Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_0-DQ_{39}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_{0-1}$	Row Address Strobe
$\overline{CAS}_{0-1}$	Column Address Strobe
$\overline{OE}$	Output Enable
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

Presence Detect Pins (Optional)

Pin	70ns	80ns	100ns
PD_1	NC	NC	NC
PD_2	NC	NC	NC
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KMM5402000A- 7	I_{CC1}	—	1070	mA
	KMM5402000A- 8		—	970	mA
	KMM5402000A-10		—	870	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	40	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, RAS Cycling @ t_{RC}=min)	KMM5402000A- 7	I_{CC3}	—	1070	mA
	KMM5402000A- 8		—	970	mA
	KMM5402000A-10		—	870	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=min.)	KMM5402000A- 7	I_{CC4}	—	820	mA
	KMM5402000A- 8		—	720	mA
	KMM5402000A-10		—	620	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	20	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KMM5402000A- 7	I_{CC6}	—	1070	mA
	KMM5402000A- 8		—	970	mA
	KMM5402000A-10		—	870	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−200	200	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	130	pF
Input Capacitance ($\overline{W}$, $\overline{OE}$)	C_{IN2}	—	150	pF
Input Capacitance ($\overline{RAS}_{0-1}$, $\overline{CAS}_{0-1}$)	C_{IN3}	—	80	pF
Input/Output Capacitance (DQ_0-DQ_{39})	CDQ_1	—	29	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KMM5402000A-7		KMM5402000A-8		KMM5402000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

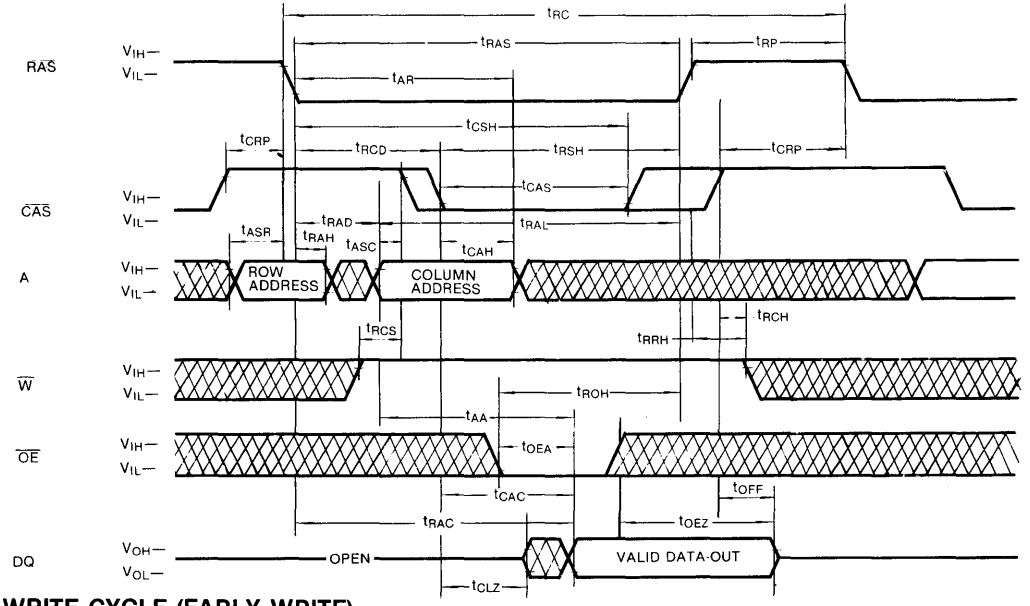
Standard Operation	Symbol	KMM5402000A-7		KMM5402000A-8		KMM5402000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	

NOTES

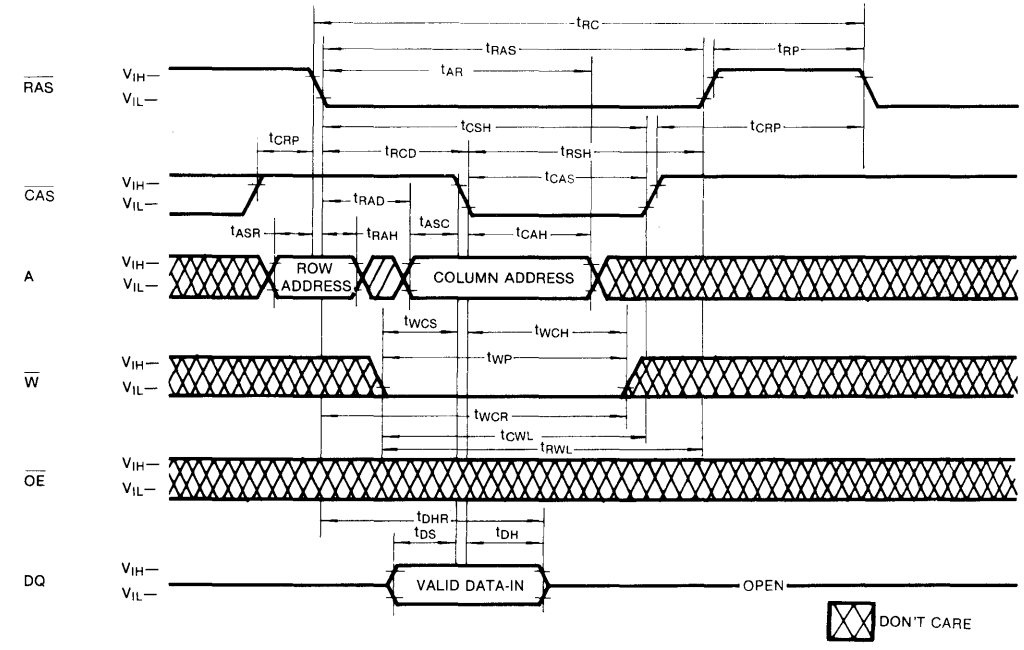
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAC(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

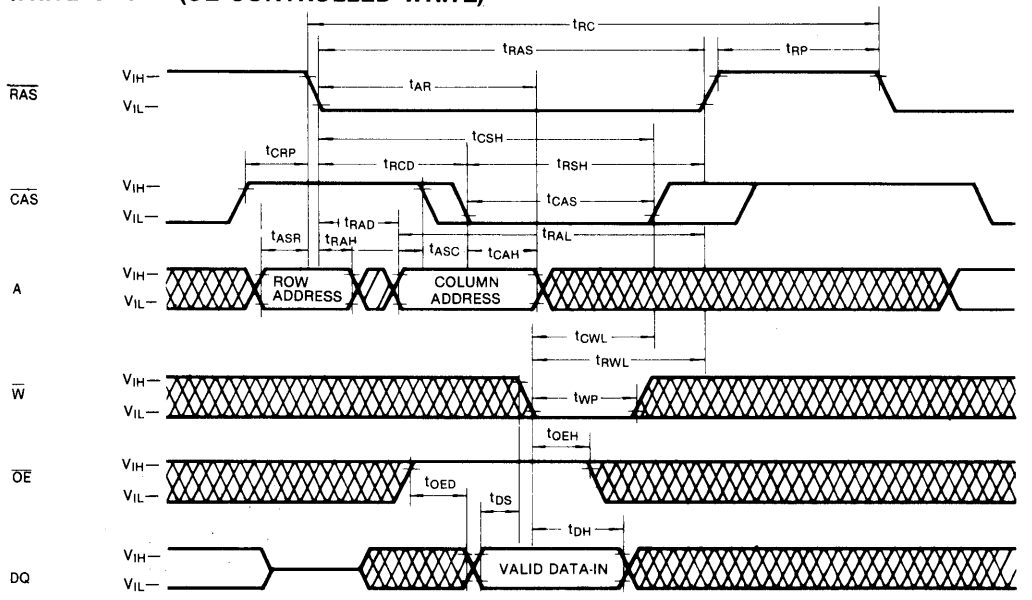


WRITE CYCLE (EARLY WRITE)

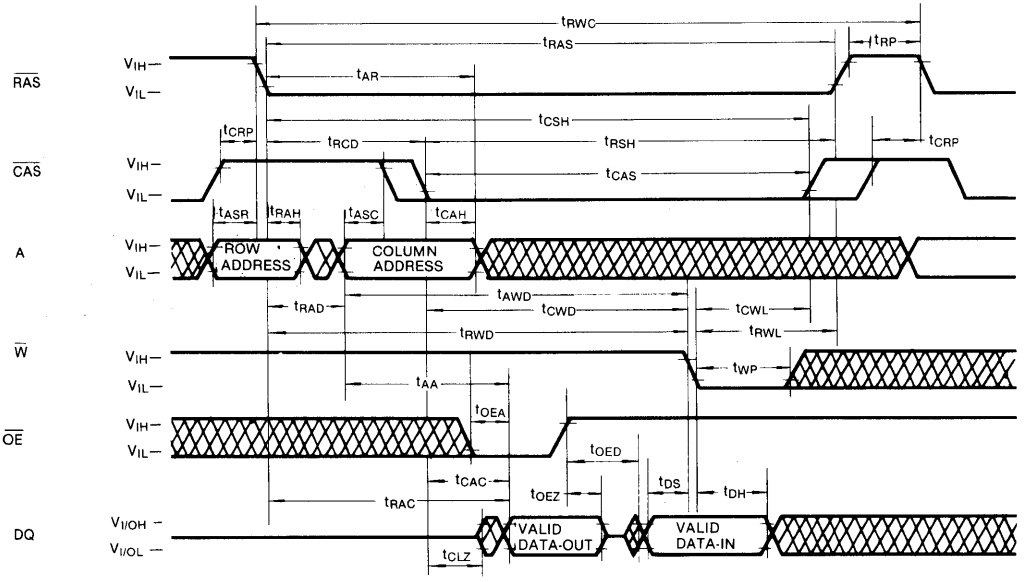


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



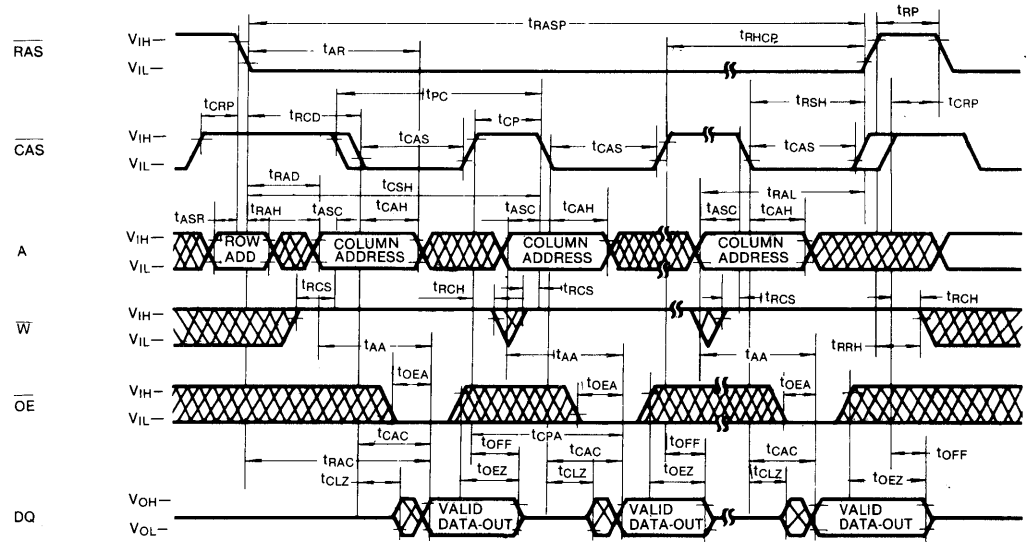
READ-MODIFY-WRITE CYCLE



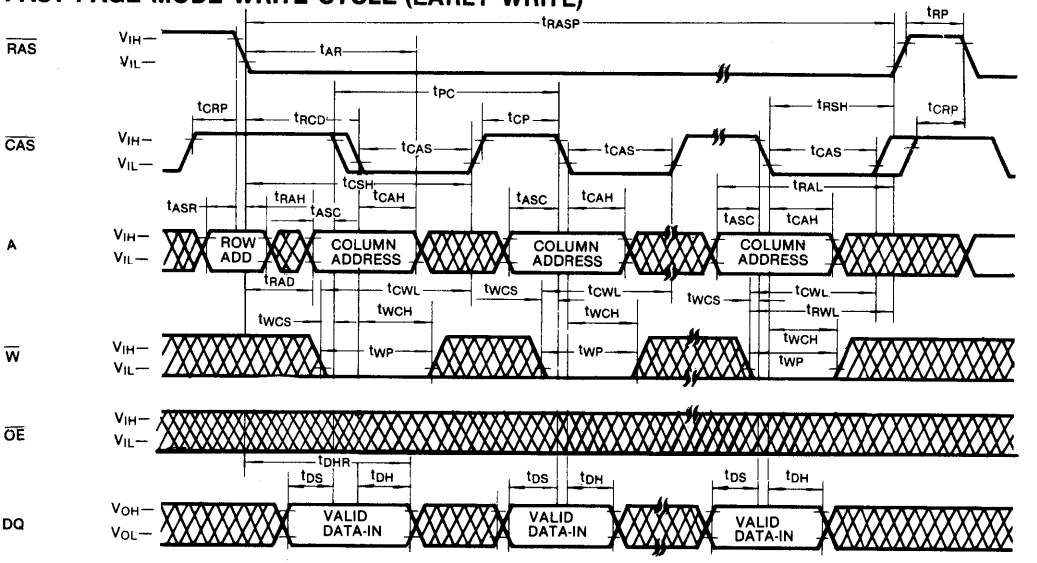
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



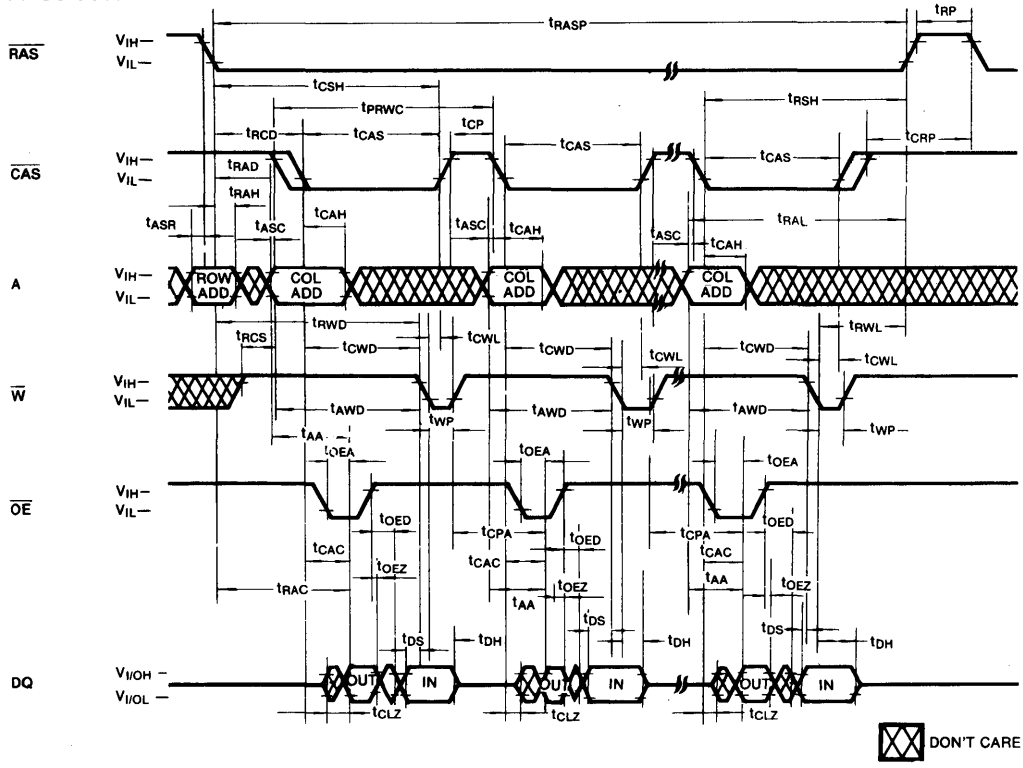
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

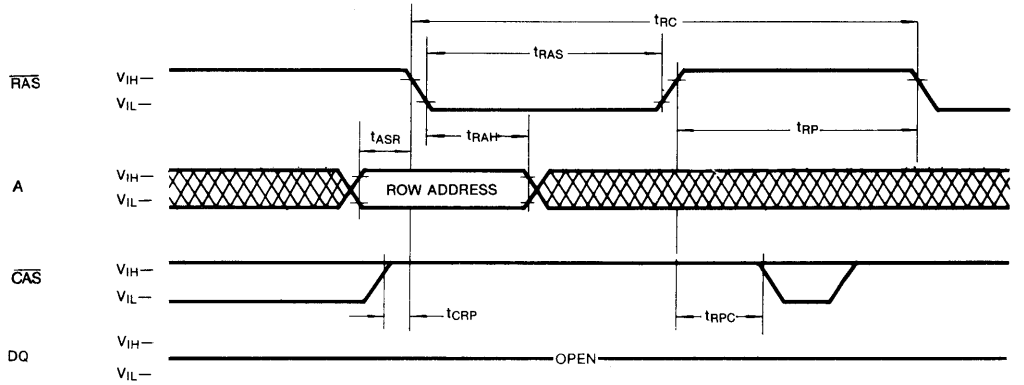
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

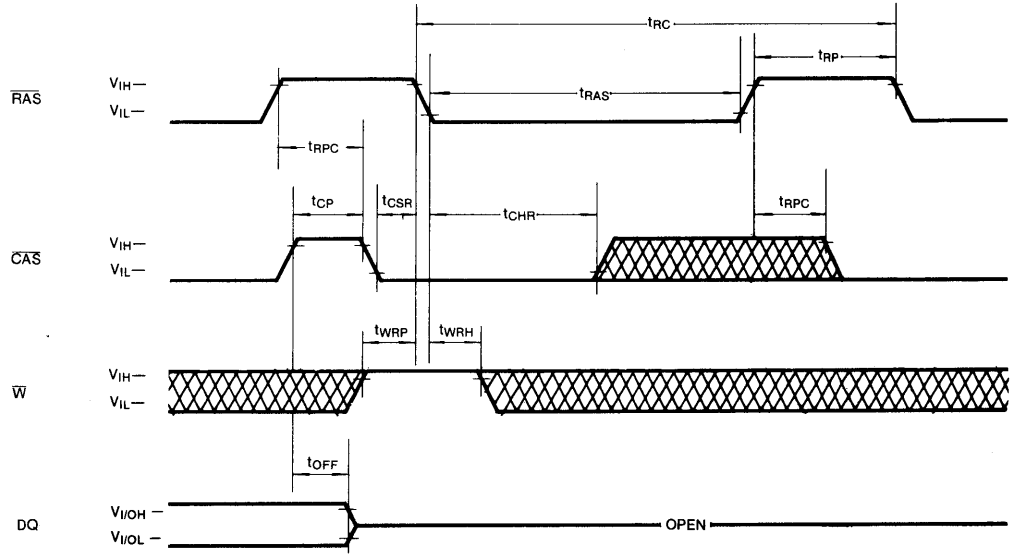
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



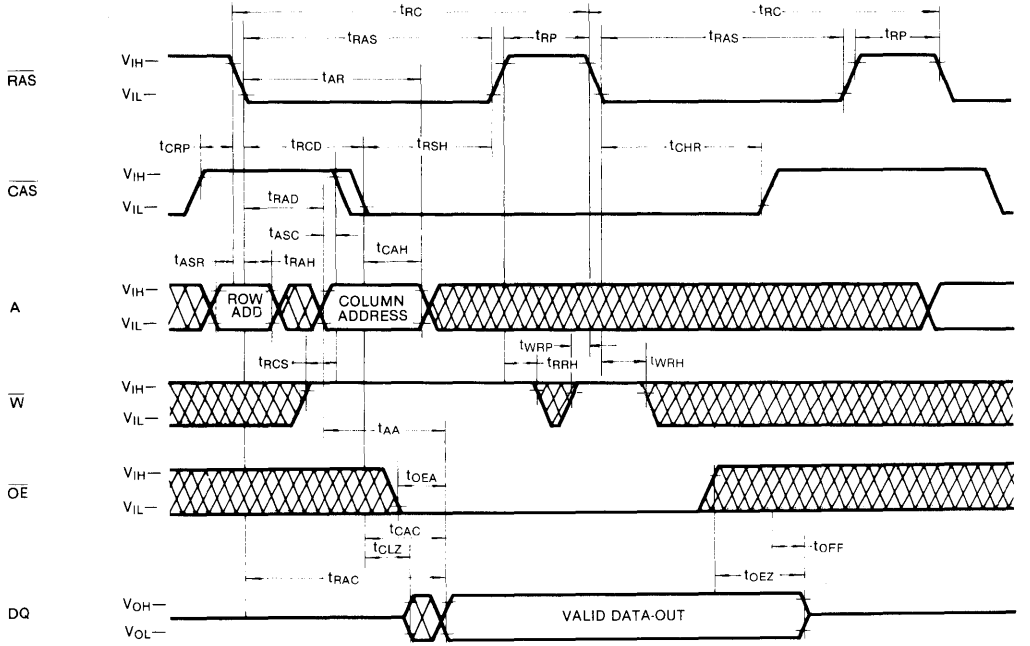
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

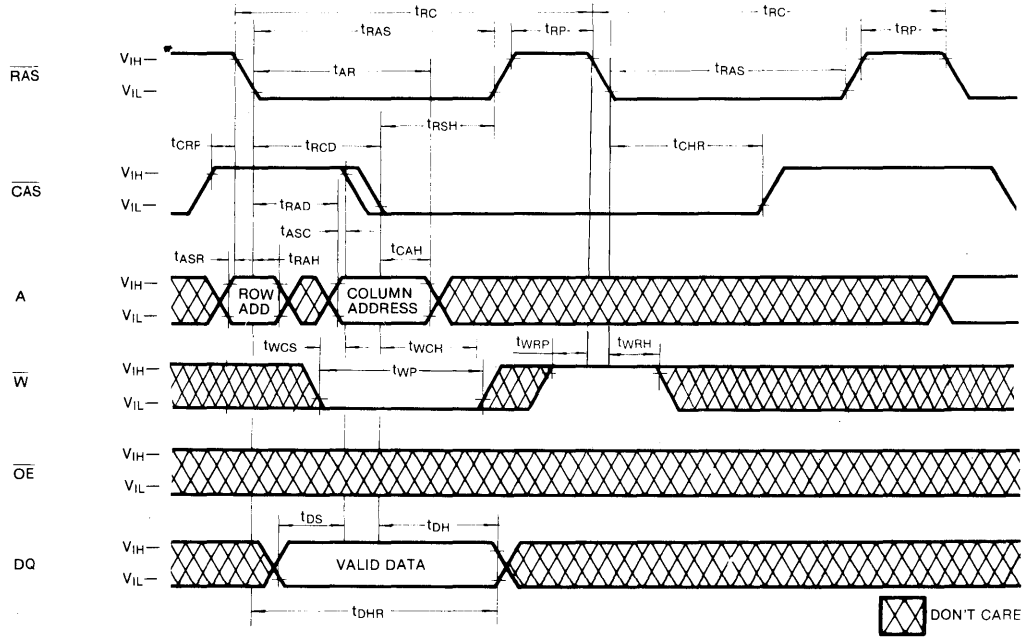


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

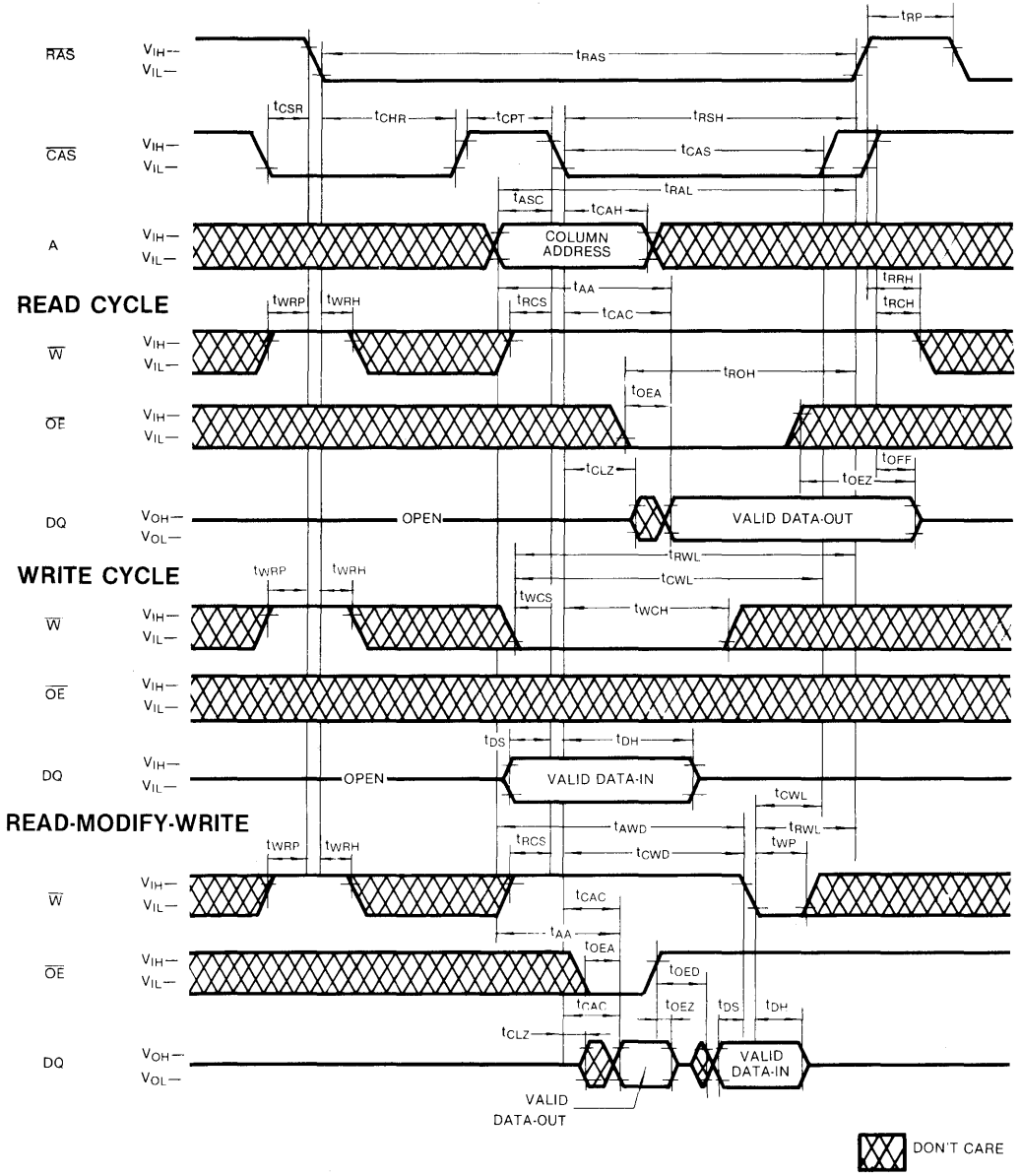


HIDDEN REFRESH CYCLE (WRITE)



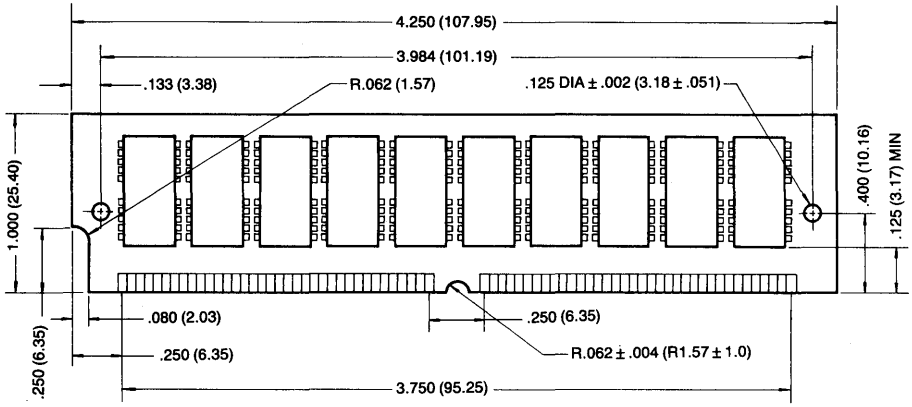
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

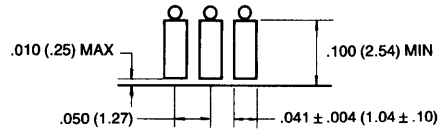


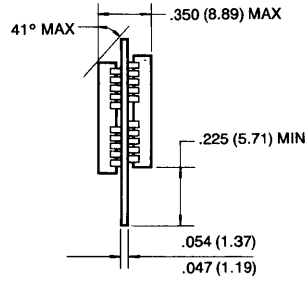
PACKAGE DIMENSIONS

Units: Inches (millimeters)

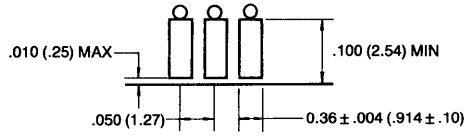


KMM5402000AG DETAIL OF CONTACTS (Gold plating lead)

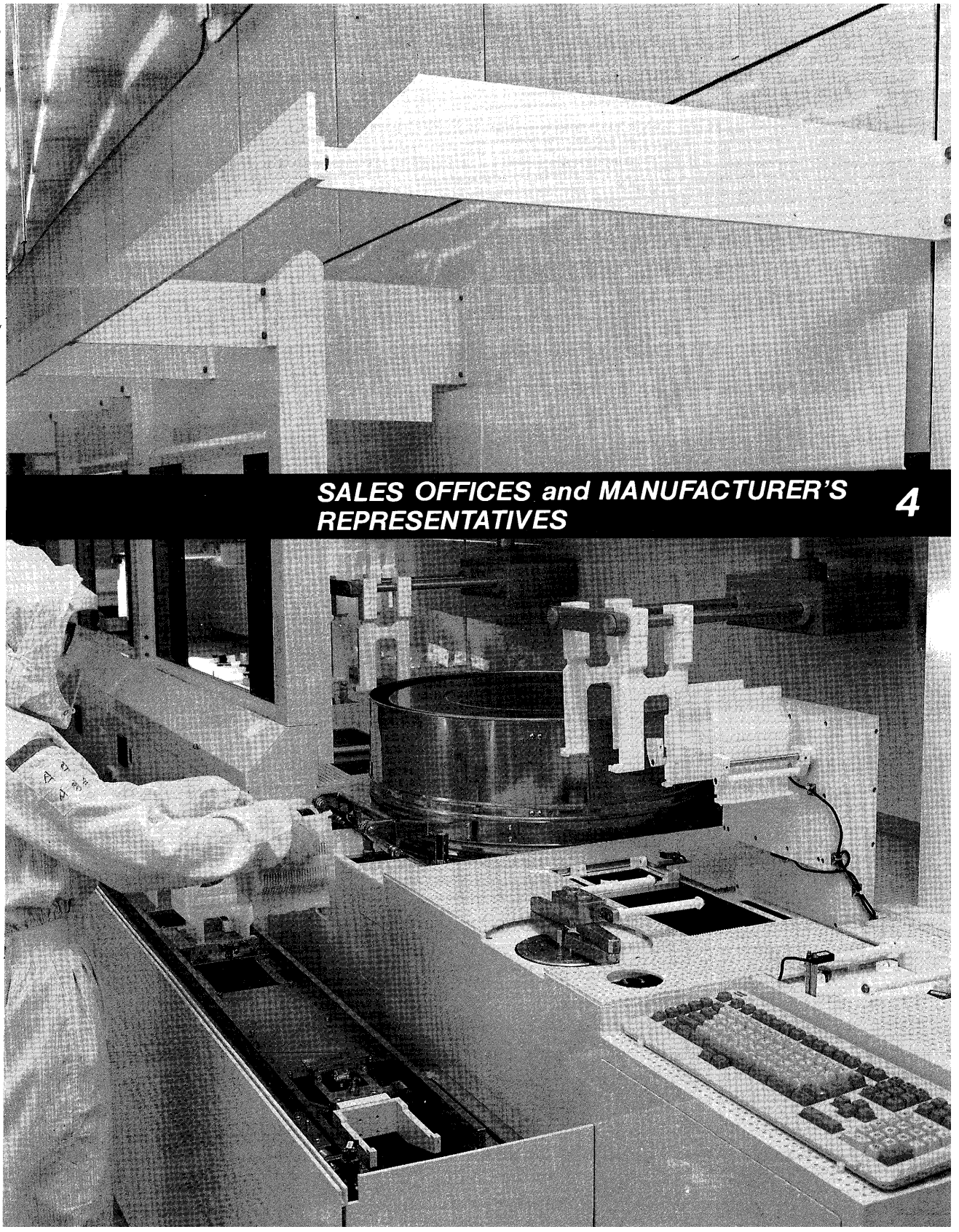




KMM5402000A DETAIL OF CONTACTS (Solder plating lead)



Tolerances: ± .005 (.13) unless otherwise specified



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