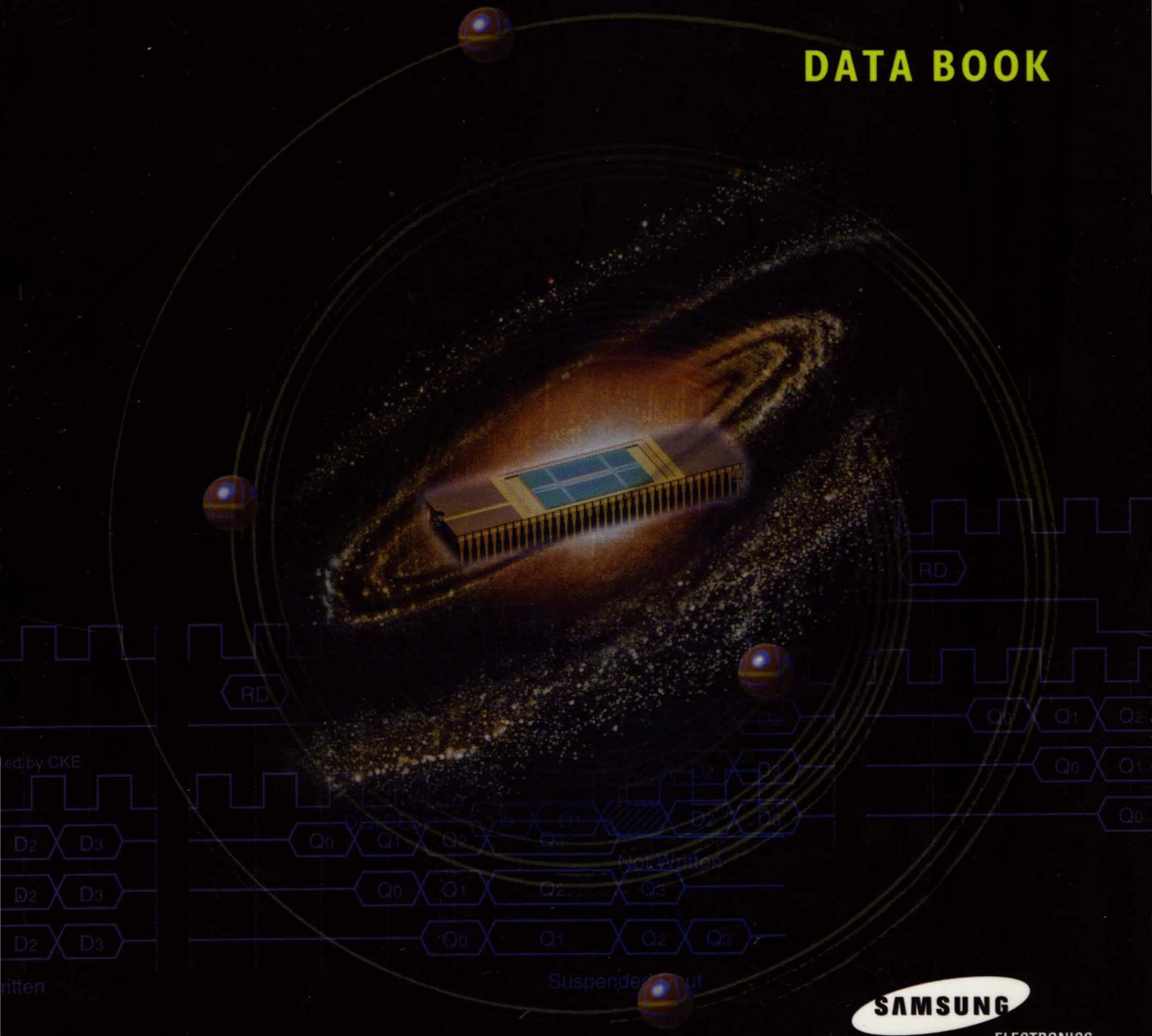
1997

SDRAM

1181-9704
April 1997

DATA BOOK



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Certificate No FM 24651

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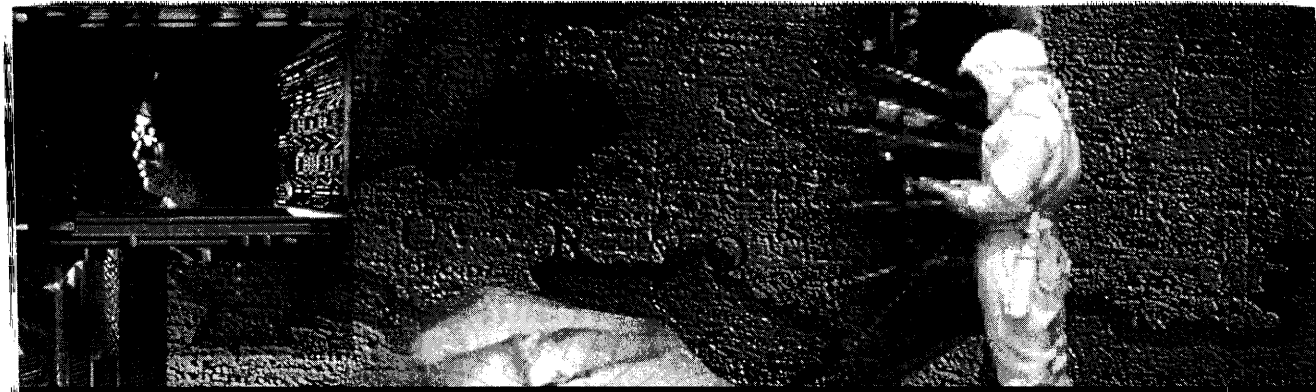
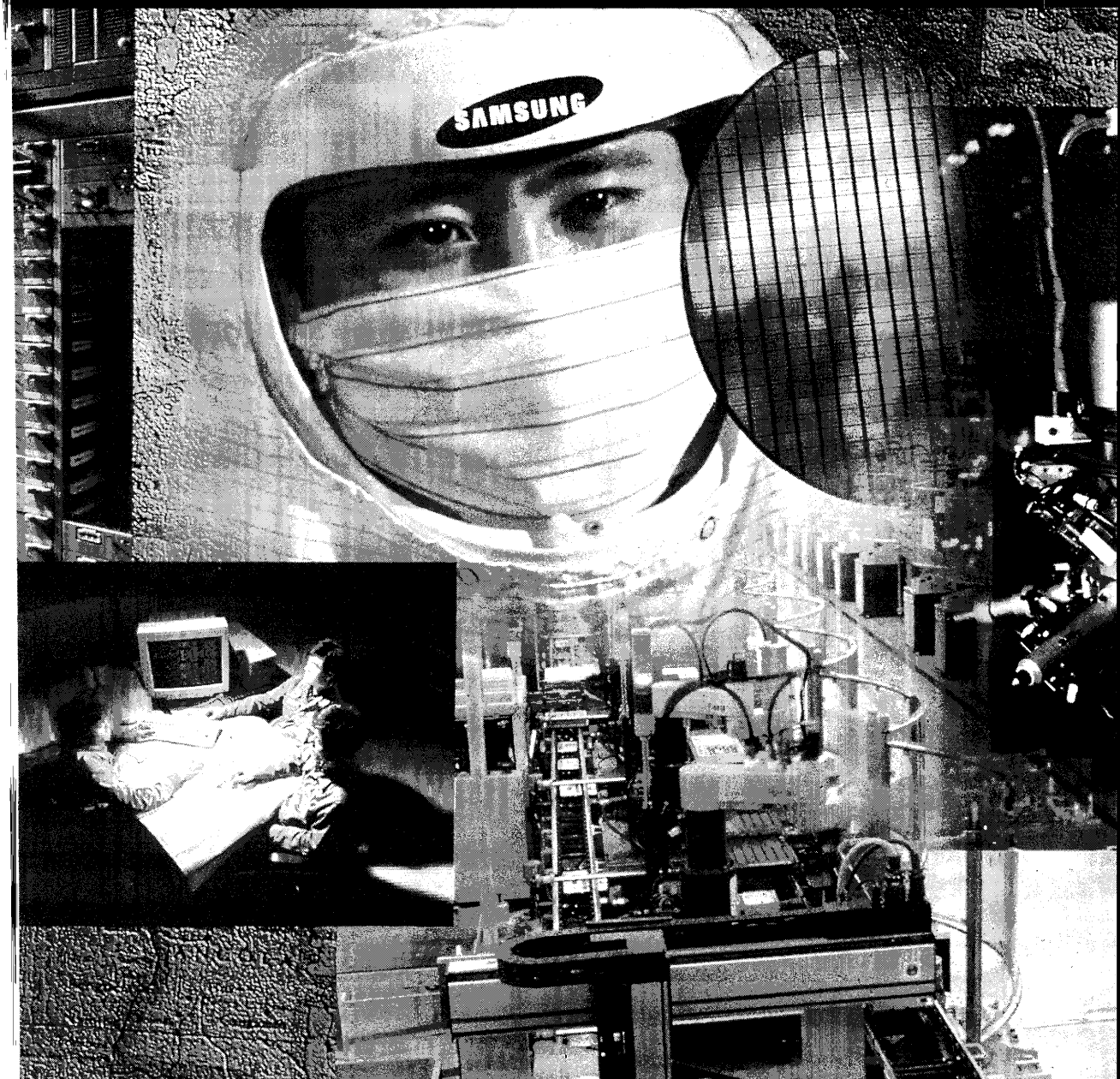


Component Specifications 1



16M SDRAM (B-die)

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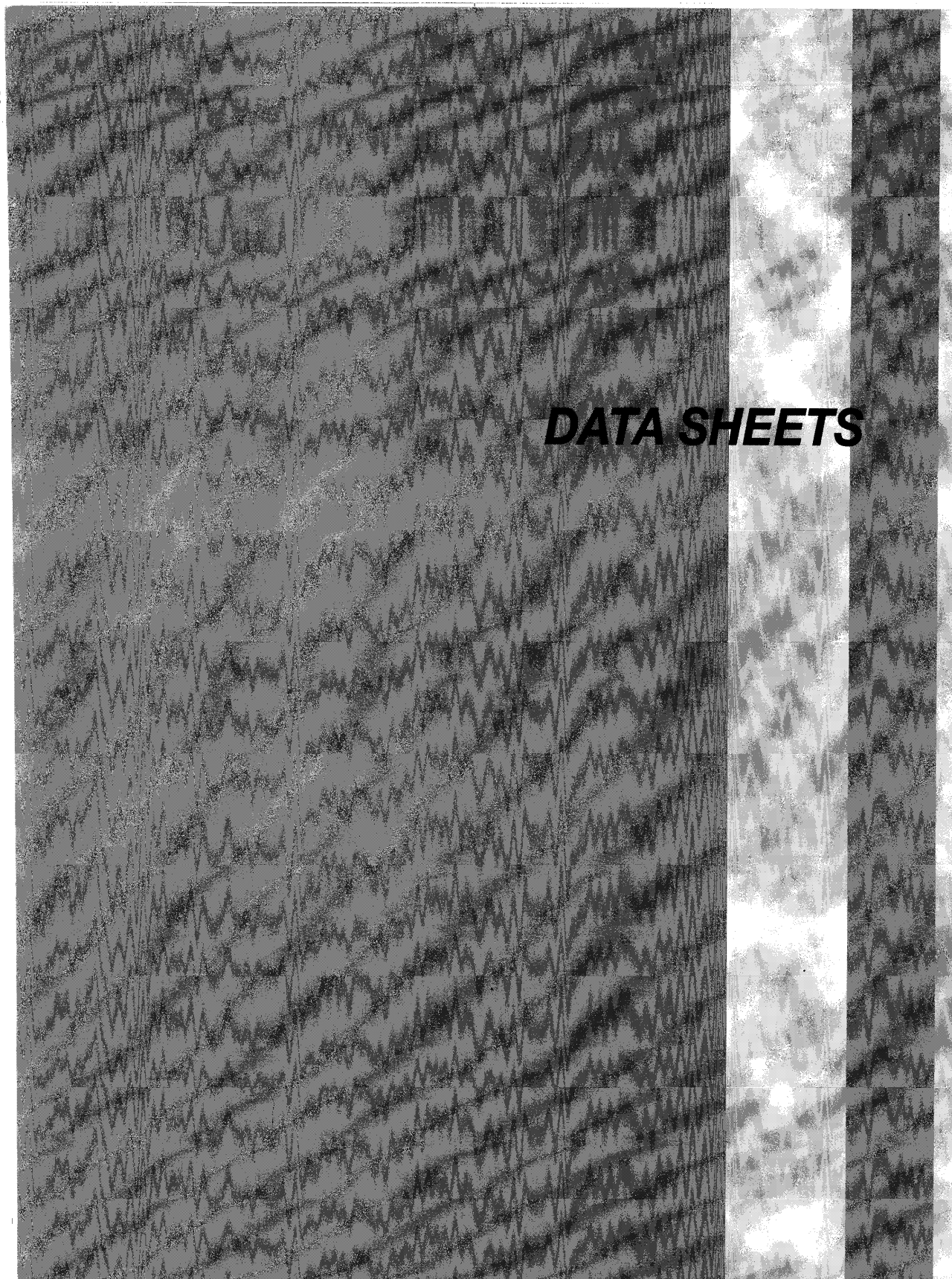

DATA SHEETS

2M x 4Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (1, 2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

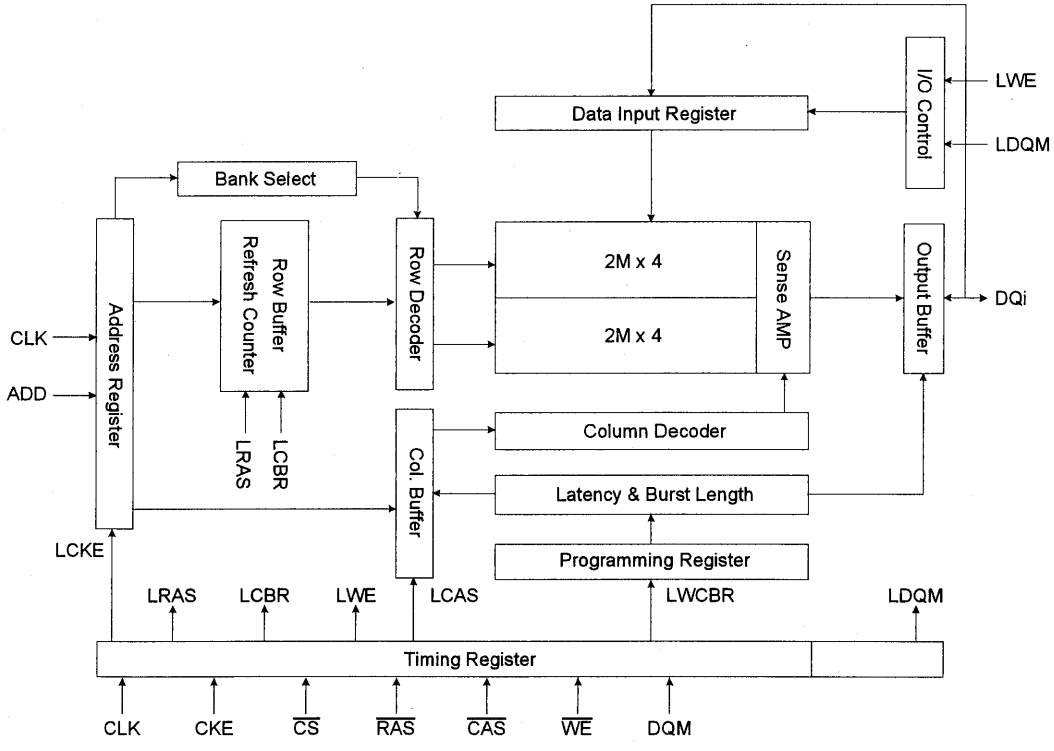
GENERAL DESCRIPTION

The KM44S4020B is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 2,097,152 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
KM44S4020BT-G/F8	125MHz	LVTTL	44 TSOP(II)
KM44S4020BT-G/F10	100MHz		
KM44S4020BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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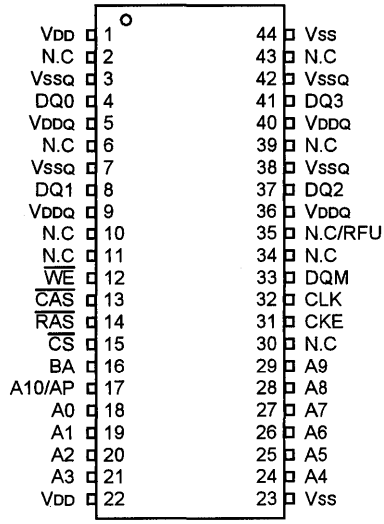
PIN CONFIGURATION (TOP VIEW)



44PIN TSOP (II)
(400mil x 725mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_9
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
DQ_0 ~ 3	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_3)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

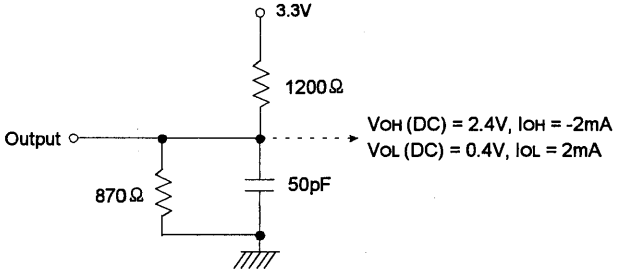
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1, $t_{RC} \geq t_{RC}$(min), I_{OL} = 0 mA		120	115	100	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		1			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		1				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns, Input signals are changed one time during 30ns		25			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞, Input signals are stable		12				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		3				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns, Input signals are changed one time during 30ns		40			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞, Input signals are stable		25			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst, t_{CCD} = 2CLKs, @ Same Row	3	130	105	90	mA	1
			2	100	90	80		
			1	65	60	55		
		@ Different Row	3	190	170	145	mA	1
			2	160	145	125		
			1	130	120	105		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		85			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		1			mA	3
				250			uA	4

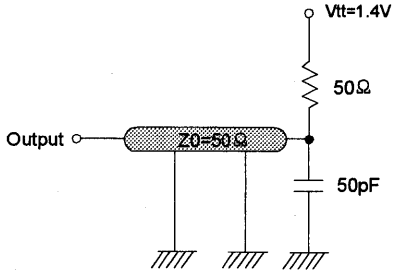
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM44S4020BT-G**
4. KM44S4020BT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS Latency=2		12		13		15			
	CAS Latency=1		24		26		30			
CLK to valid output delay	CAS Latency=3	tSAC		6		7		8	ns	1, 2
	CAS Latency=2			7		8		9		
	CAS Latency=1			20		22		24		
Output data hold time	CAS Latency=3	tOH	3		3		3		ns	2
	CAS Latency=2		3		3		3			
	CAS Latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM44S4020BT-8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KM44S4020BT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM44S4020BT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don' t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

1M x 8Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (1, 2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

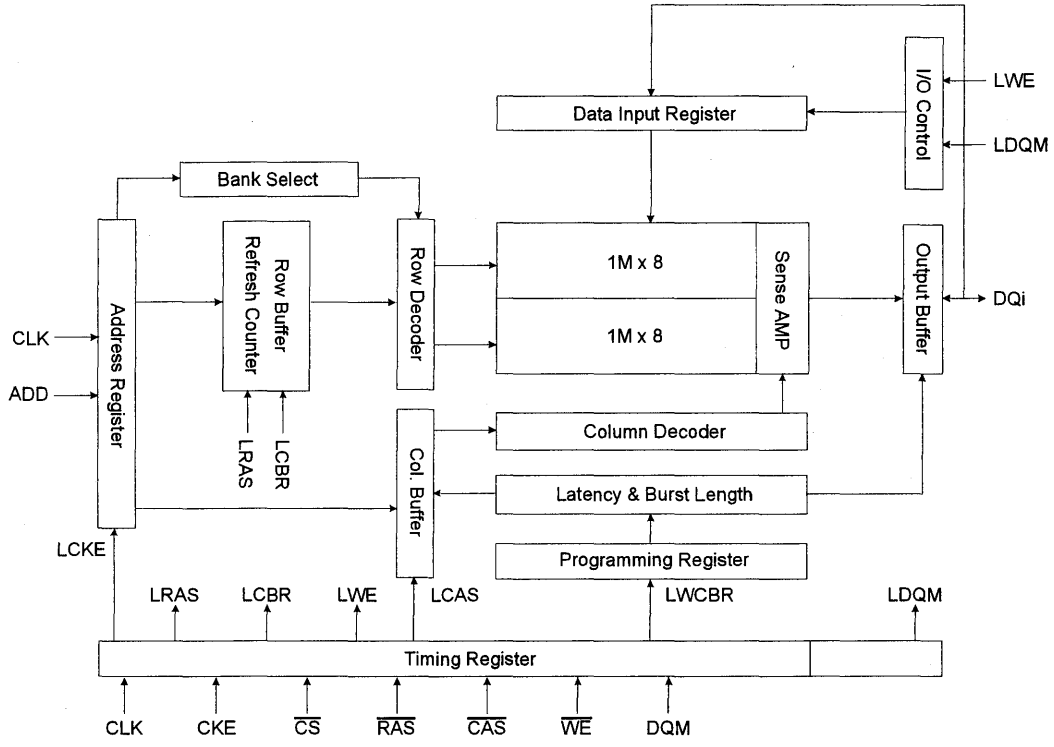
GENERAL DESCRIPTION

The KM48S2020B is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 1,048,576 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

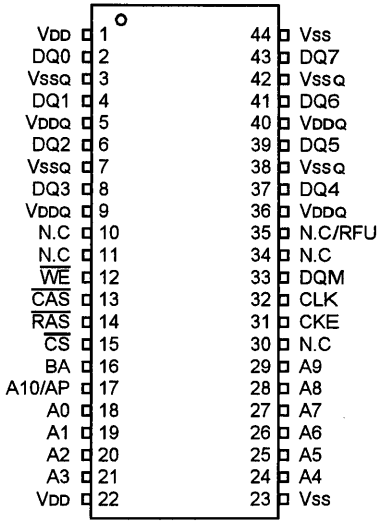
Part NO.	MAX Freq.	Interface	Package
KM48S2020BT-G/F8	125MHz	LVTTL	44 TSOP(II)
KM48S2020BT-G/F10	100MHz		
KM48S2020BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



44PIN TSOP (II)
(400mil x 725mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_8
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
DQ_0 ~ 7	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_7)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

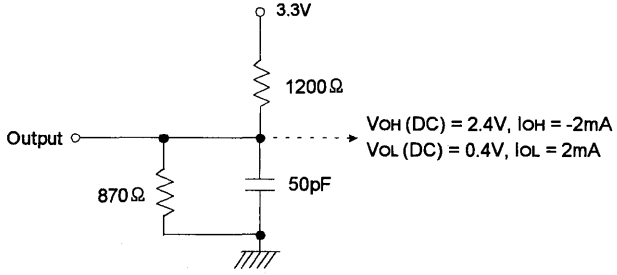
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition		CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA			125	120	105	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns			1			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞			1				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns			25			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable			12				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns			4			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞			3				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns			40			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable			25			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row	3	135	110	95	mA	1
				2	100	90	80		
				1	65	60	55		
			@ Different Row	3	200	180	155	mA	1
				2	165	150	130		
				1	135	125	110		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)			85			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V			1			mA	3
					250			uA	4

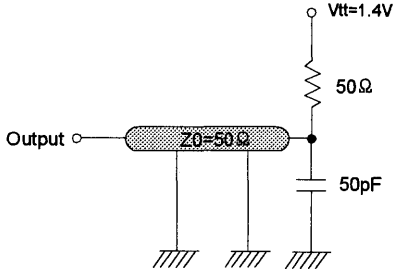
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM48S2020BT-G**
4. KM48S2020BT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS Latency=2		12		13		15			
	CAS Latency=1		24		26		30			
CLK to valid output delay	CAS Latency=3	tSAC		6		7		8	ns	1, 2
	CAS Latency=2			7		8		9		
	CAS Latency=1			20		22		24		
Output data hold time	CAS Latency=3	tOH	3		3		3		ns	2
	CAS Latency=2		3		3		3			
	CAS Latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM48S2020BT-8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KM48S2020BT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM48S2020BT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

512K x 16Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (1, 2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

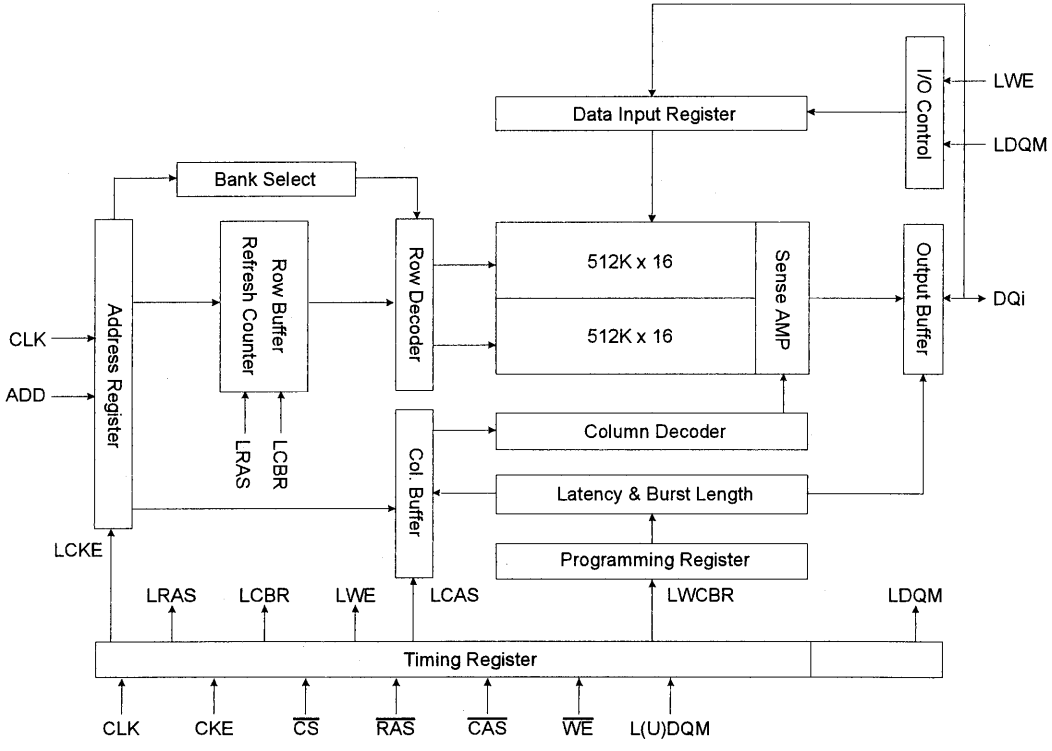
GENERAL DESCRIPTION

The KM416S1020B is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
KM416S1020BT-G/F8	125MHz	LVTTL	50 TSOP(II)
KM416S1020BT-G/F10	100MHz		
KM416S1020BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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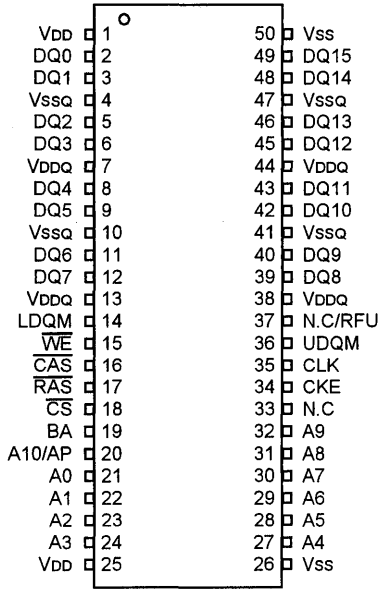
PIN CONFIGURATION (TOP VIEW)



50PIN TSOP (II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

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DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	2	5	pF

DC CHARACTERISTICS

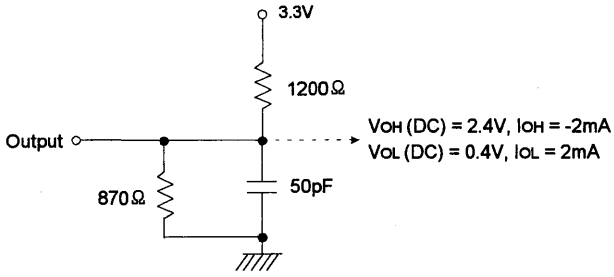
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		135	130	115	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		1			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		1				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		25			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		12				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		3				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		40			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		25			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	140	120	100	mA	1
			@ Same Row 2	105	100	85		
			@ Same Row 1	70	65	60		
			@ Different Row 3	215	200	175	mA	1
			@ Different Row 2	175	160	140		
			@ Different Row 1	140	130	115		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		85			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		1			mA	3
				250			uA	4

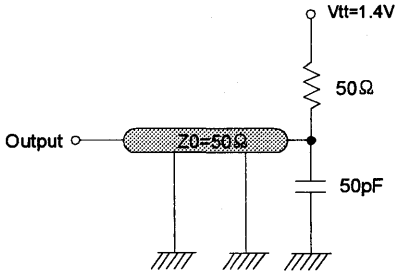
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM416S1020BT-G**
4. KM416S1020BT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	24	26	30	ns	1
Row precharge time		$t_{RP(min)}$	20	26	30	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	80	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS Latency=2		12		13		15			
	CAS Latency=1		24		26		30			
CLK to valid output delay	CAS Latency=3	tSAC		6		7		8	ns	1, 2
	CAS Latency=2			7		8		9		
	CAS Latency=1			20		22		24		
Output data hold time	CAS Latency=3	tOH	3		3		3		ns	2
	CAS Latency=2		3		3		3			
	CAS Latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S1020BT-8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KM416S1020BT-10 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM416S1020BT-12 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

512K x 16Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- SSTL_3 (Class II) compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

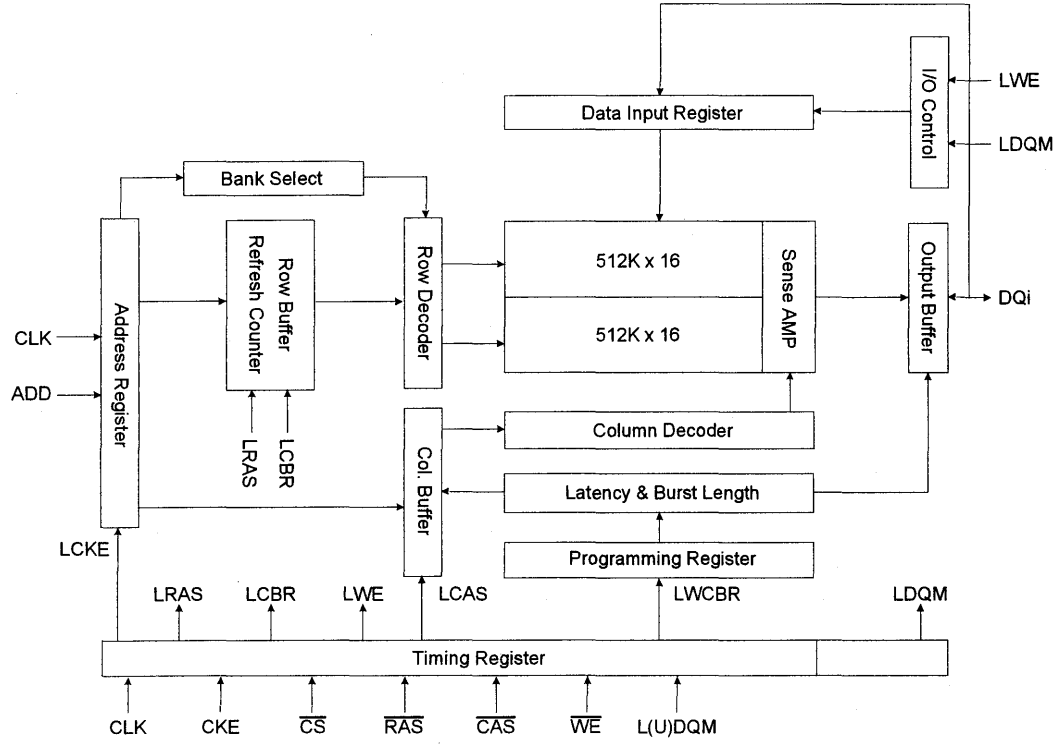
GENERAL DESCRIPTION

The KM416S1021B is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

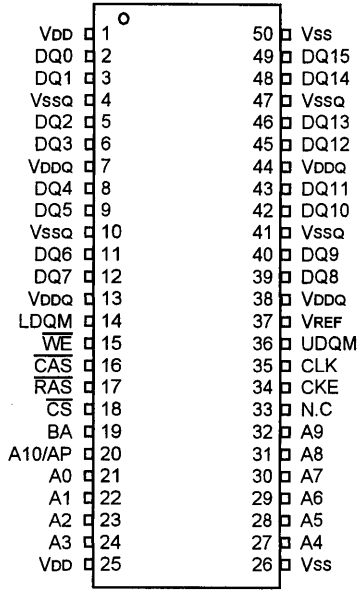
Part NO.	MAX Freq.	Interface	Package
KM416S1021BT-G7	143MHz	SSTL_3 (Class II)	50 TSOP(II)
KM416S1021BT-G8	125MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



50PIN TSOP (II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	*Reference Voltage*	Reference voltage for inputs.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device supply voltage	V_{DD}	V_{DDQ}	-	3.6	V	1
Output supply voltage	V_{DDQ}	3.0	3.3	3.6	V	1
Input reference voltage	V_{REF}	1.3	1.5	1.7	V	2, 3
Termination voltage	Vtt	V_{REF}-0.05	V_{REF}	V_{REF}+0.05	V	
Input logic high votlage	V_{IH}	V_{REF}+0.2	-	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	V_{REF}-0.2	V	2
Output logic high voltage	V_{OH}	Vtt+0.8	-	-	V	5
Output logic low voltage	V_{OL}	-	-	Vtt-0.8	V	5
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	7

Note : 1. Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
2. Typically, the value of V_{REF} is expected to be about 0.45 *V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
3. Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF} (DC)
4. Vtt of transmitting device must track V_{REF} of receiving device.
5. Voltage level measured at device pin with I_{OH}/I_{OL} = -16mA/16mA.
6. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
7. Dout buffer is disabled, 0V ≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	2	5	pF

DC CHARACTERISTICS

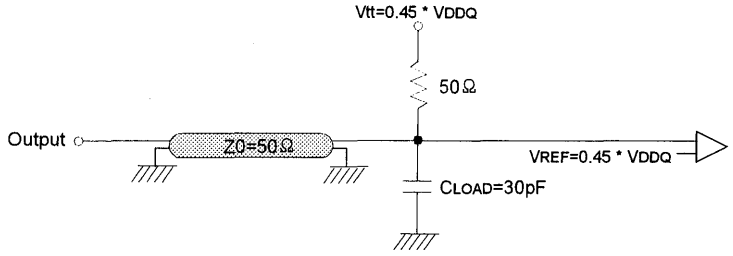
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -7	Version -8	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) Io = 0 mA		145	130	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), tcc = 15ns		2		mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		2			
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		30		mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		15			
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), tcc = 15ns		5		mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		4			
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		50		mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		35		mA	
Operating Current (Burst Mode)	I_{CC4}	Io = 0 mA Page Burst t_{CCD} = 2CLKs	3	170	150	mA	1
			2	105	100		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		95	85	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq V_{IL}$(max)		2		mA	3

Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM416S1021BT-G**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input reference voltage	0.45 *V_{DDQ}	V
Input signal maximum peak swing	2.0	V
Inout signal minimum slew rate	1.0	V / ns
AC Input levels (Vih/Vil)	V_{REF}+0.4 / V_{REF}-0.4	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	Vtt	V
Output load condition	See Fig. 1	



(Fig. 1) Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Veraion		Unit	Note
			-7	-8		
Row active to row active delay		$t_{RRD(min)}$	14	16	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	21	24	ns	1
Row precharge time		$t_{RP(min)}$	21	24	ns	1
Row active time		$t_{RAS(min)}$	48	56	ns	1
		$t_{RAS(max)}$	100		us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	ns	1
	@Auto refresh	$t_{RFC(min)}$	77	88	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1		CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1		CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1		CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		1			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-7		-8		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7	1000	8	1000	ns	1
	CAS latency=2		13		15			
CLK to valid output delay	CAS latency=3	tSAC		5.5		6	ns	1, 2
	CAS latency=2			7		8		
Output data hold time		tOH	2.5		2.5		ns	2
CLK high pulse width		tCH	3		3		ns	3
CLK low pulse width		tCL	3		3		ns	3
Input setup time		tSS	2		2.5		ns	3
Input hold time		tSH	1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.5		6	ns	
	CAS latency=2			7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S1021BT-G7 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	21ns	14ns	21ns	7ns	7ns	7ns
143MHz (7.0ns)	3	10	7	3	2	3	1	1	1
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	9	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	7	4	2	2	2	1	1	1

KM416S1021BT-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	56ns	24ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	7	3	2	3	1	1	1
100MHz (10.0ns)	3	8	6	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	3	6	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_9~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

DEVICE OPERATIONS-I

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA	A_{10}/AP	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A_8	A_7	Type	A_6	A_5	A_4	Latency	A_3	Type	A_2	A_1	A_0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A_9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : x4 (1024), x8 (512), x16 (256)

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	0	1	2	3	0	1	0	3	2
1	1	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tss" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESS (BA)

: In case x 4

This SDRAM is organized as two independent banks of 2,097,152 words x 4 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank select BA is latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as two independent banks of 1,048,576 words x 8 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank select BA is latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as two independent banks of 524,288 words x 16 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank select BA is latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A10/AP)

: In case x 4

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}/AP). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

: In case x 8

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}/AP). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

: In case x 16

The 19 address bits are required to decode the 524,288 word locations are multiplexed into 11 address input pins (A_0 ~ A_{10}/AP). The 11 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

DEVICE OPERATIONS (Continued)

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_{10}/AP and BA in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) uses A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP and BA. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP, BA must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has two internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of two banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid BA of the bank to be procharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precahrge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after both banks have satisfied t_{RAS}(min) requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, both banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RFC}(min). The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

SELF REFRESH

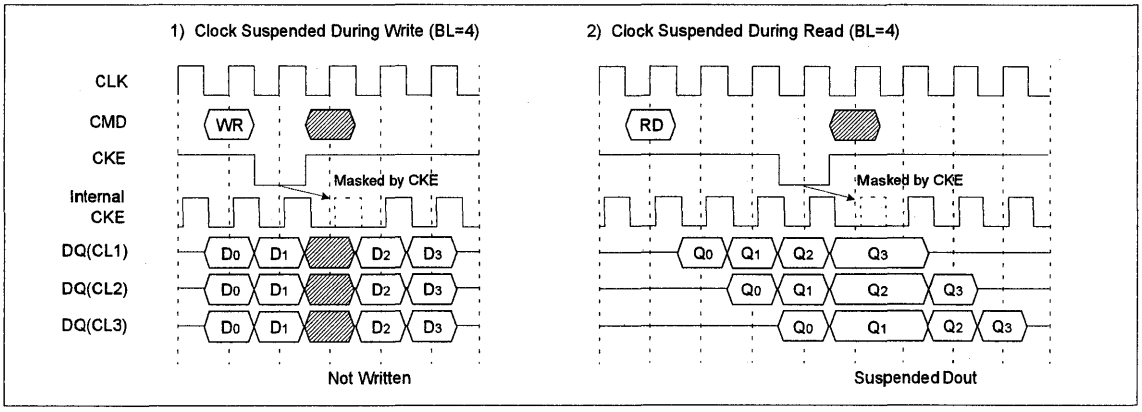
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from both banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.

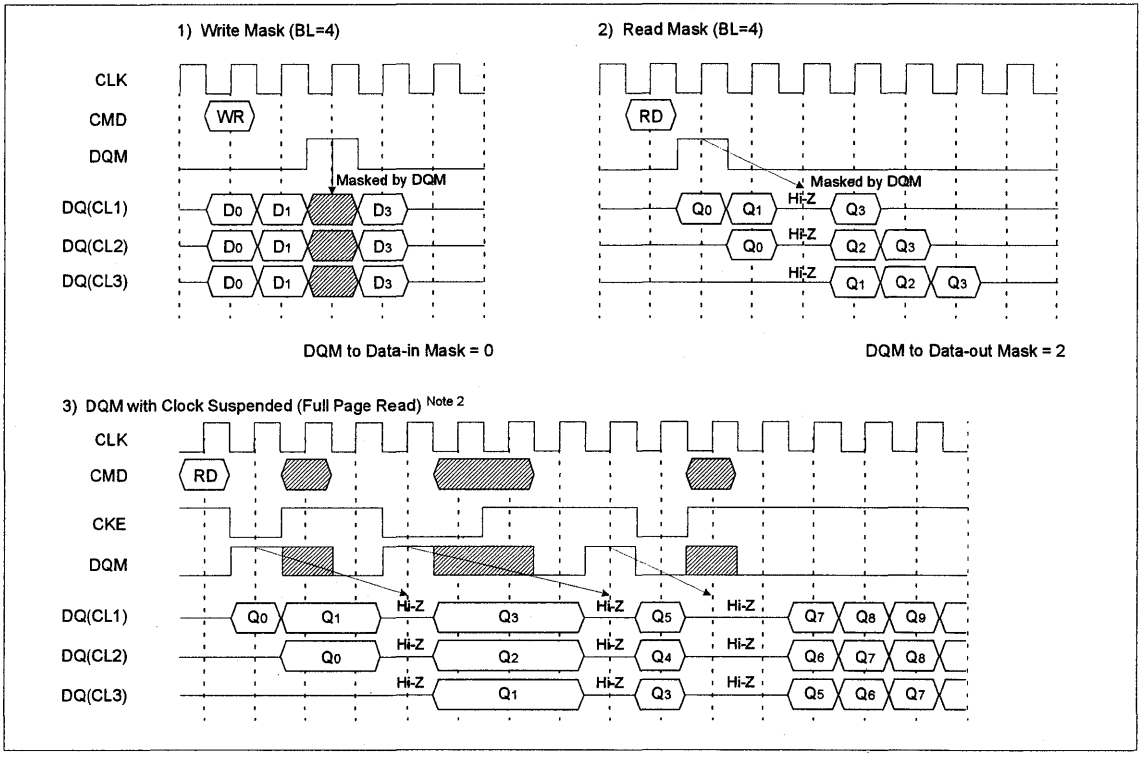
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend



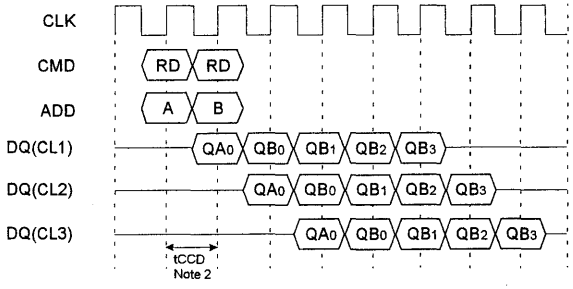
2. DQM Operation



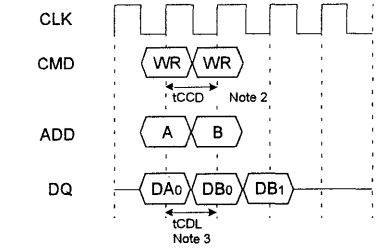
***Note :** 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)

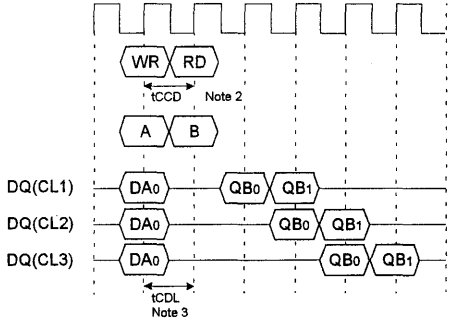
1) Read interrupted by Read (BL=4) Note 1



2) Write interrupted by Write (BL=2)

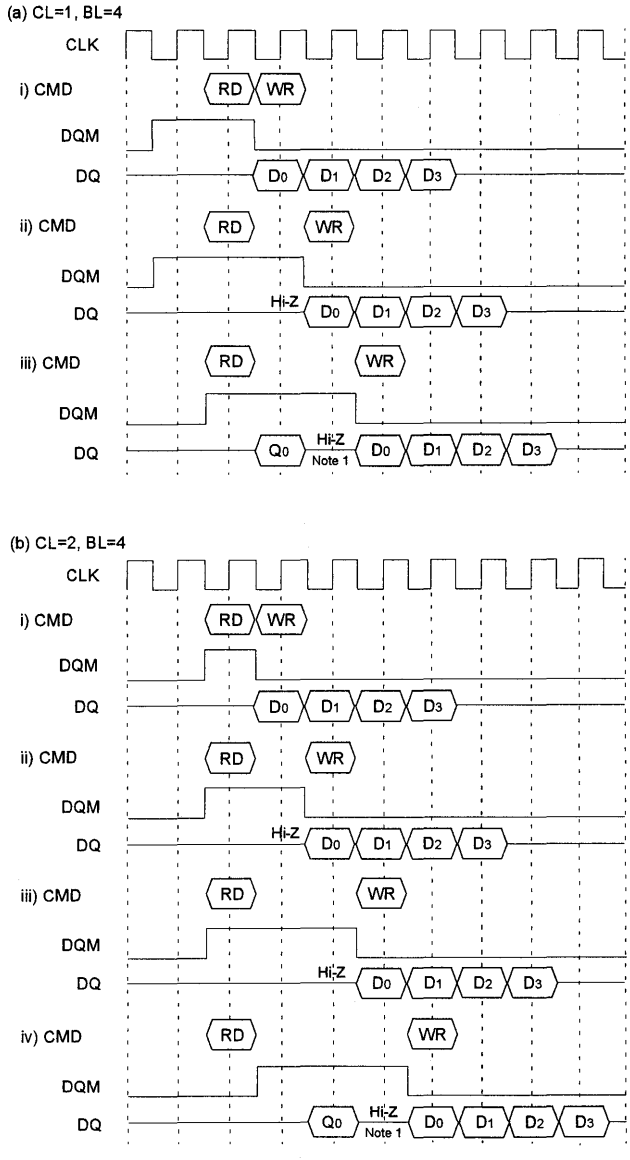


3) Write interrupted by Read (BL=2)



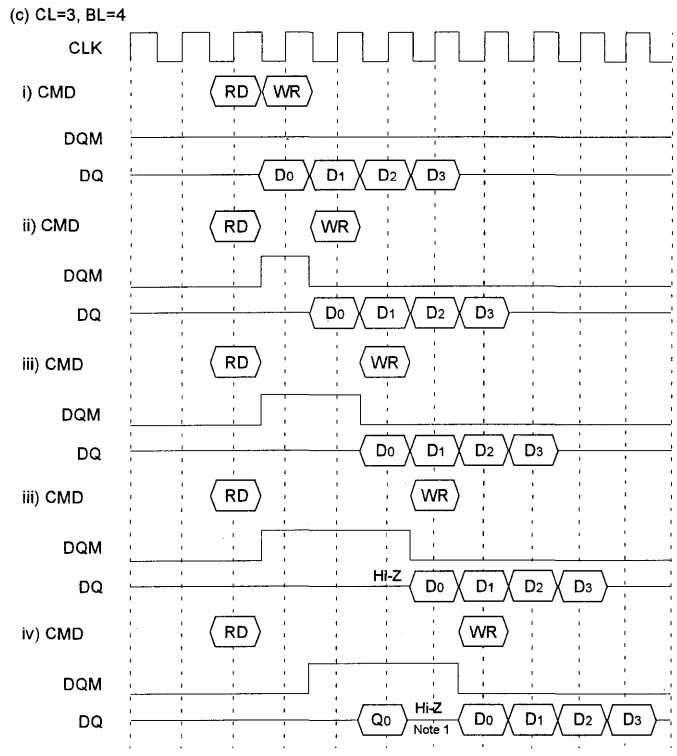
***Note :** 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM

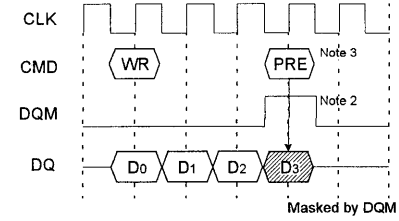


***Note :** 1. To prevent bus contention, there should be at least one gap between data in and data out.

(Continued)



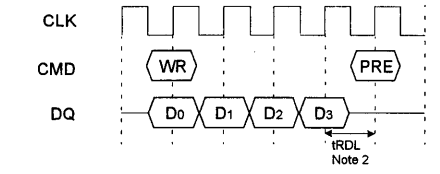
5. Write Interrupted by Precharge & DQM



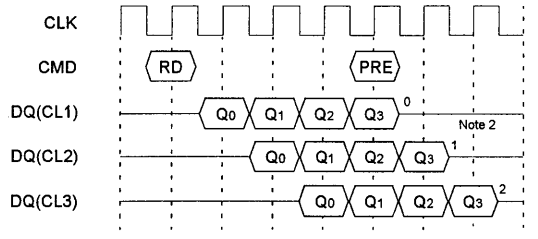
***Note :** 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only the other bank precharge of dual banks operation.

6. Precharge

1) Normal Write (BL=4)

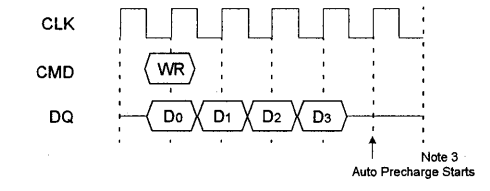


2) Normal Read (BL=4)

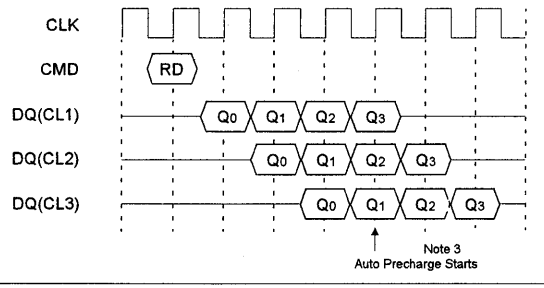


7. Auto Precharge

1) Normal Write (BL=4)



2) Normal Read (BL=4)

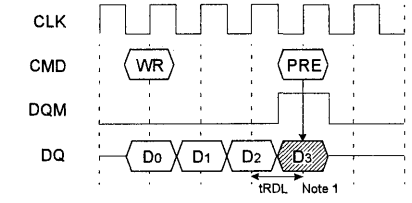


***Note :** 1. t_{RDL} : Last data in to row precharge delay

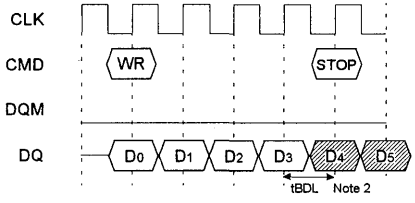
2. Number of valid output data after row precharge : 0, 1, 2 for CAS Latency =1, 2, 3 respectively.
3. The row active command of the precharge bank can be issued after t_{RP} from this point.
   The new read/write command of the other activated bank can be issued from this point.
   At burst read/write with auto precharge, CAS interrupt of the same/other bank is illegal.

8. Burst Stop & Interrupted by Precharge

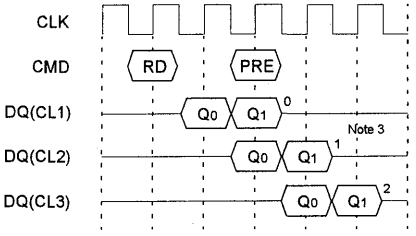
1) Normal Write (BL=4)



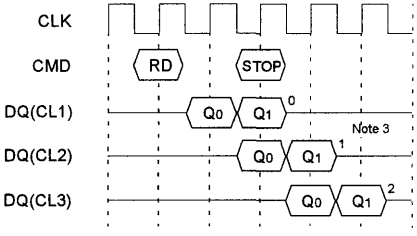
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

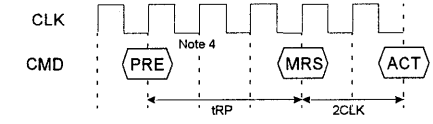


4) Read Burst Stop (BL=4)



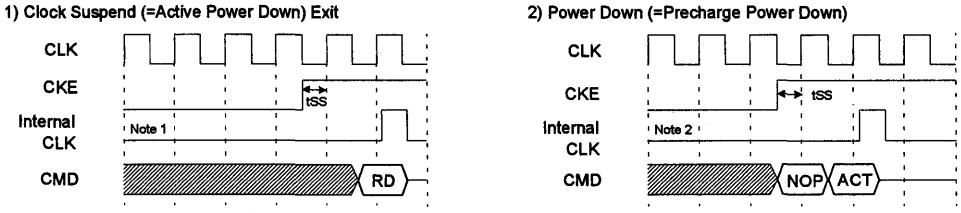
9. MRS

1) Mode Register Set

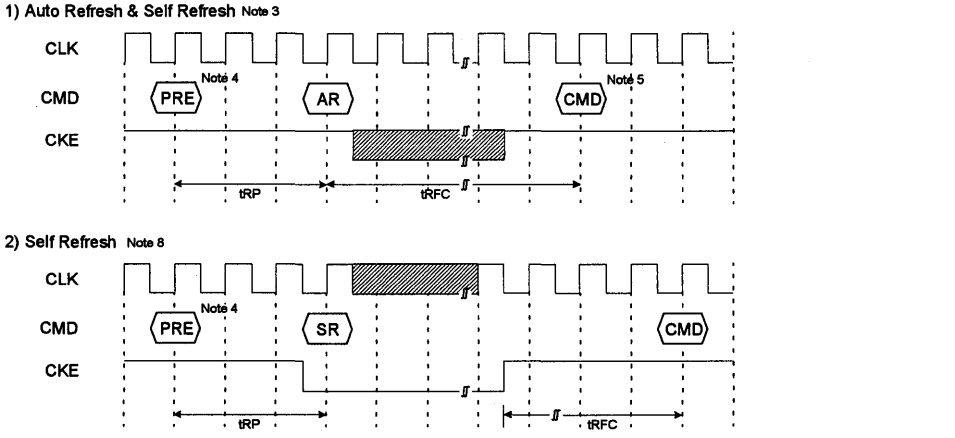


***Note :** 1. t_{RDL} : 1 CLK
2. t_{BDL} : 1 CLK ; Last data in to burst stop delay.
Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 0, 1, 2 for CAS latency=1, 2, 3 respectiviely.
4. PRE : Both banks precharge if necessary.
MRS can be issued only at both banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



***Note :** 1. Active power down : one or both banks active state.

2. Precharge power down : both banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
   No precharge commands are required after auto refresh command.
   During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refreh mode, refresh interval and refresh operation are perfomed internally.
   After self refresh entry, self refresh mode is kept while CKE is low.
   During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
   For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted. Before/After self refresh mode, burst auto refresh cycle (4096 cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4,8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4,8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". At the end of the burst length, burst will be stop automatically.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 0, 1, 2 for CAS latency 1, 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 1 with DQM, valid DQ after burst stop is 0, 1, 2 for CAS latency 1, 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after tRP	
	L	H	H	H	X	X	NOP --> Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP --> Idle after tRP	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clcok and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clcok Suspend	

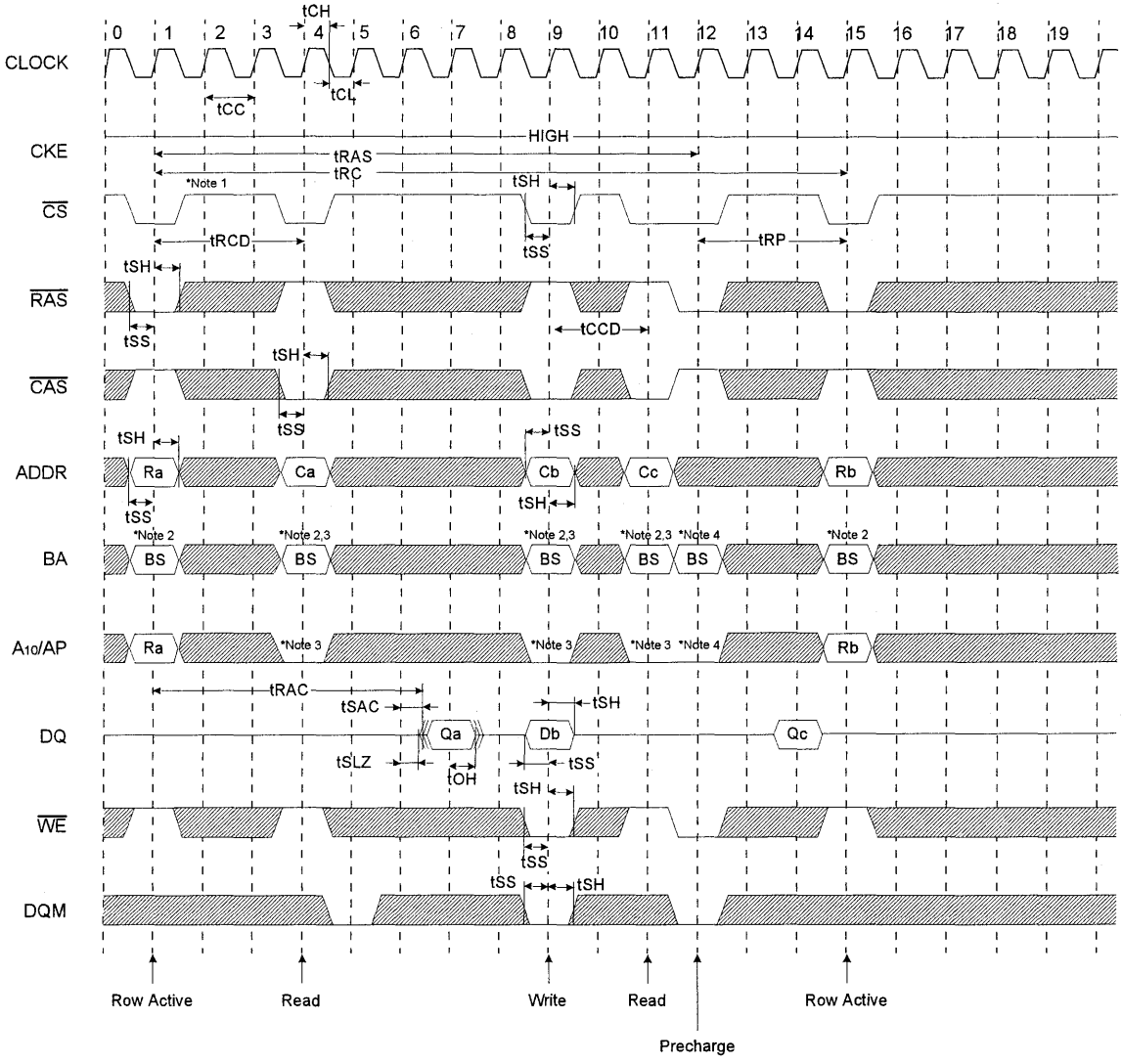
Abbreviations : ABI = All Banks Idle, RA = Row Address

***Note :** 6. CKE low to high transition is asynchronous.

7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + tss must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the both banks idle state.
9. Must be a legal command.

TIMING DIAGRAM-I

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



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*Note : 1. All inputs expect CKE & DQM can be don ' t care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

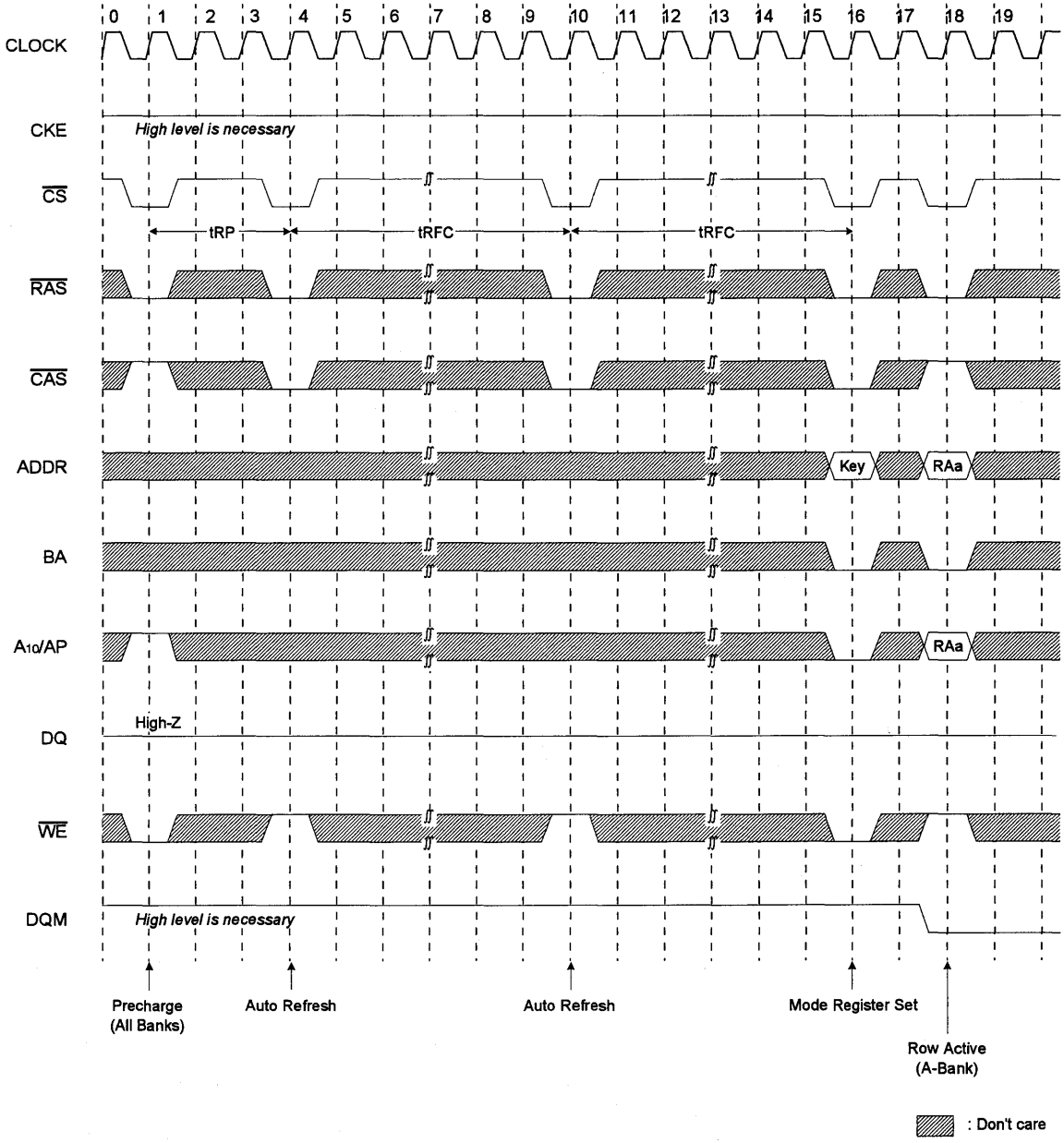
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

4. A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

Power Up Sequence



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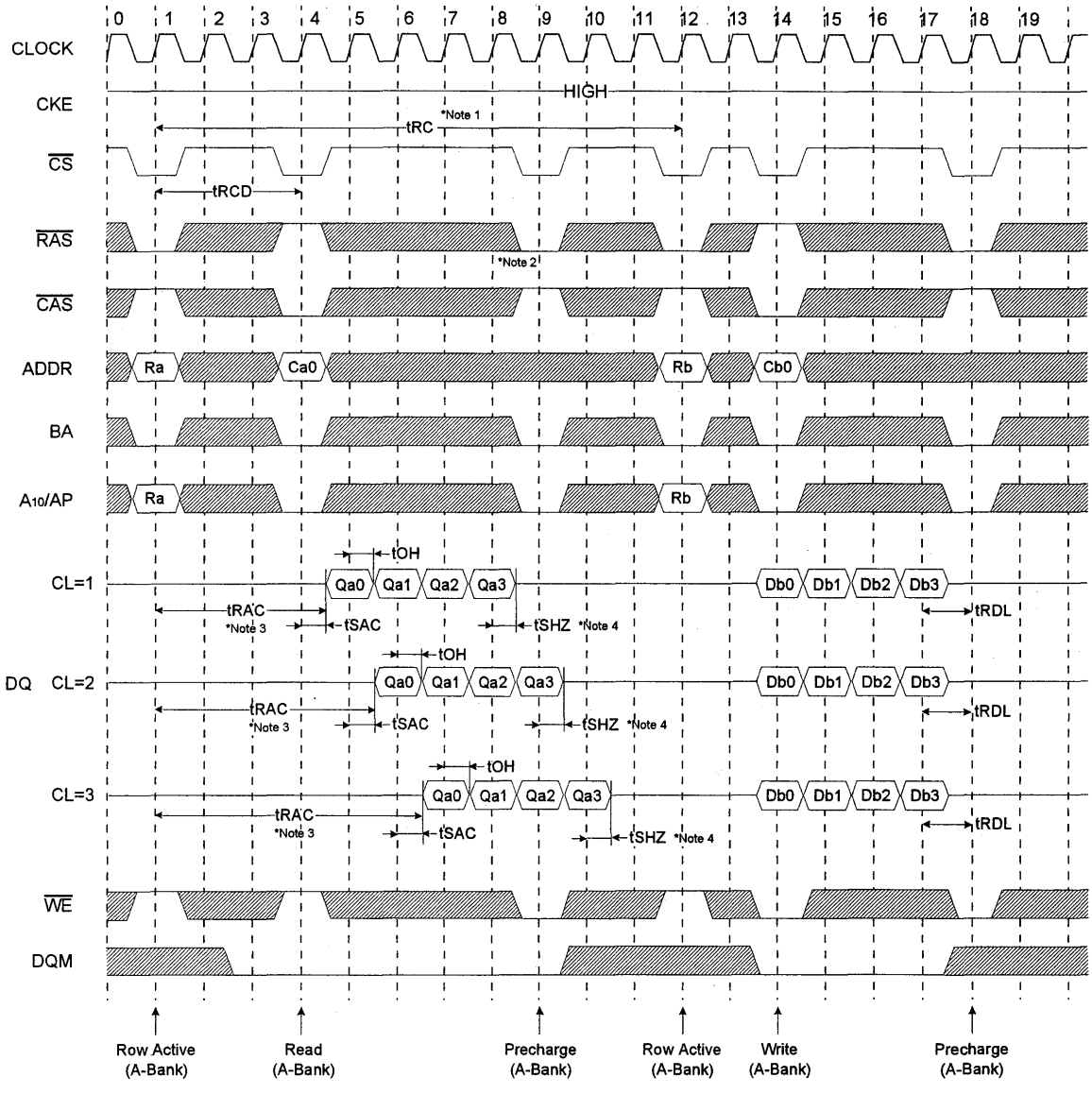
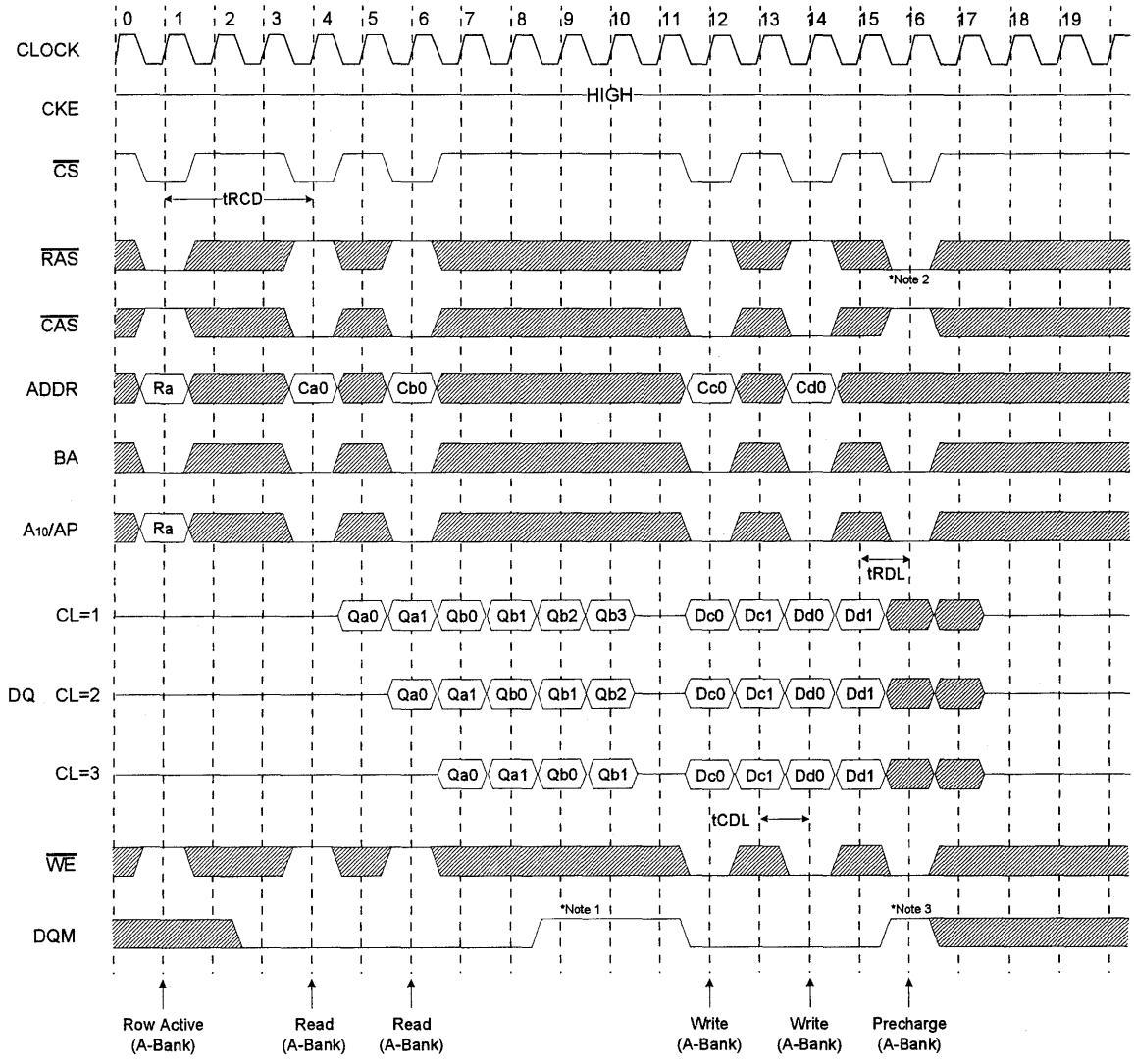
Read & Write Cycle at Same Bank @Burst Length=4



: Don't care

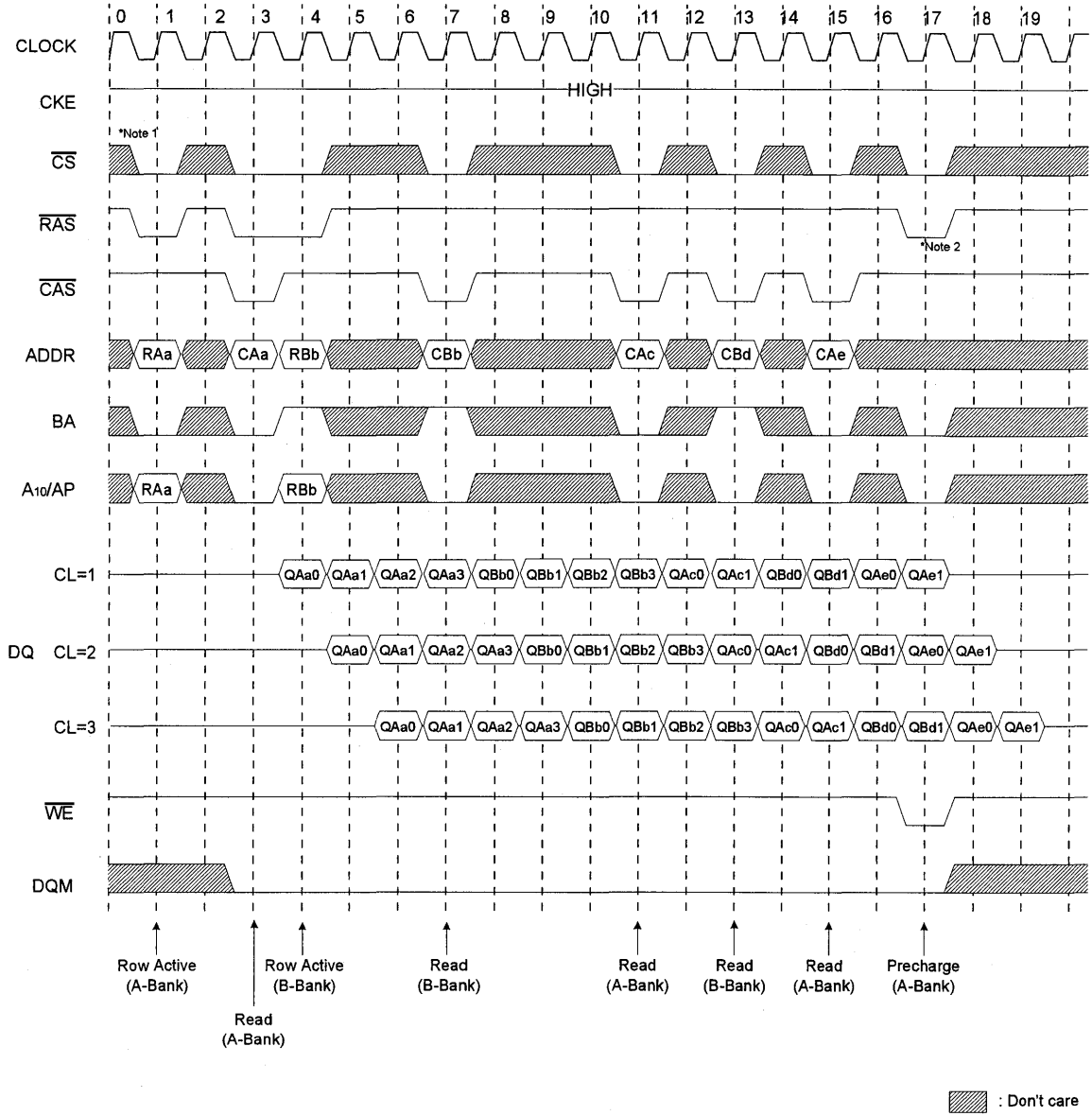
***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @Burst Length=4



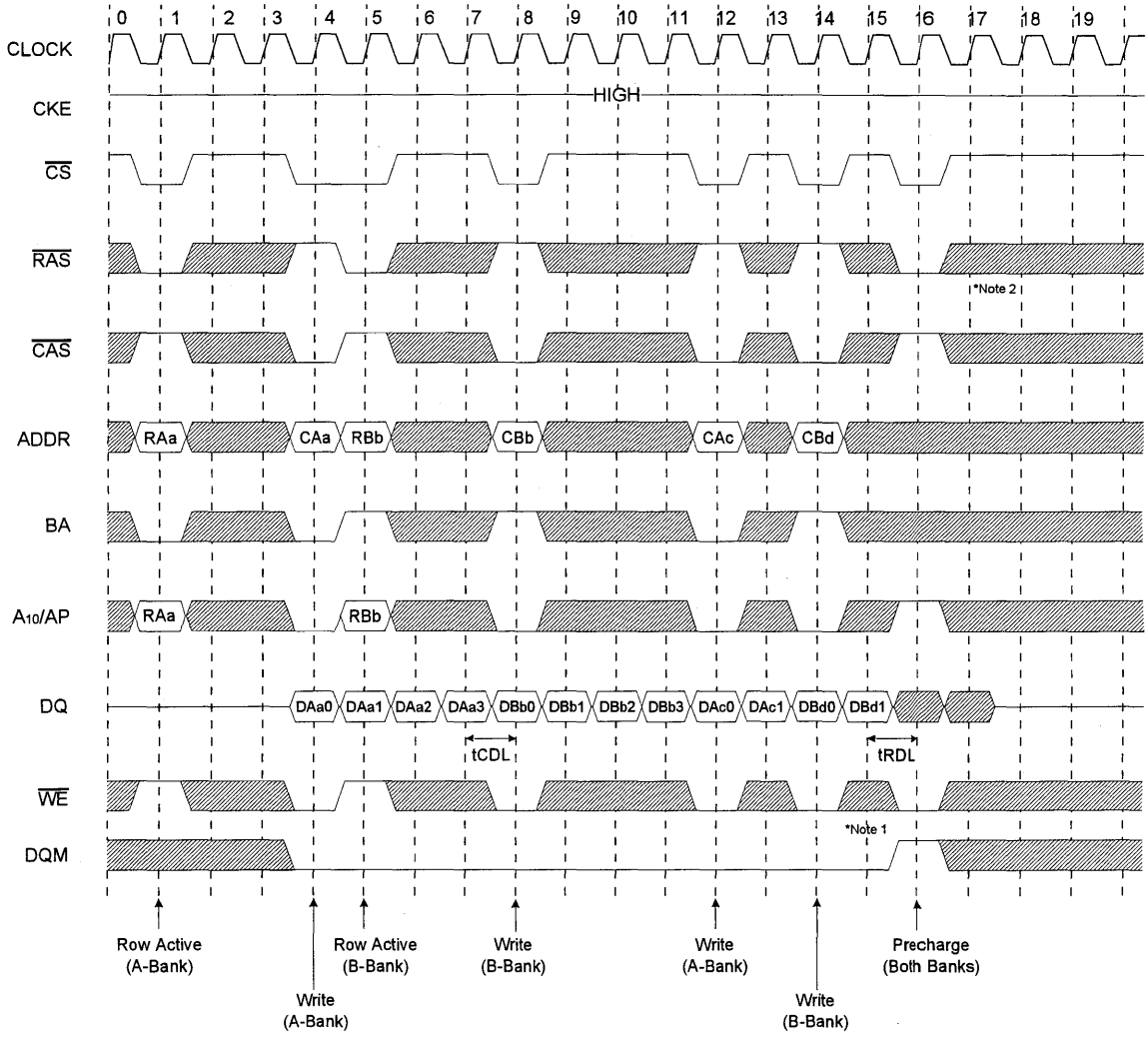
***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, tRDL before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Page Read Cycle at Different Bank @Burst Length=4



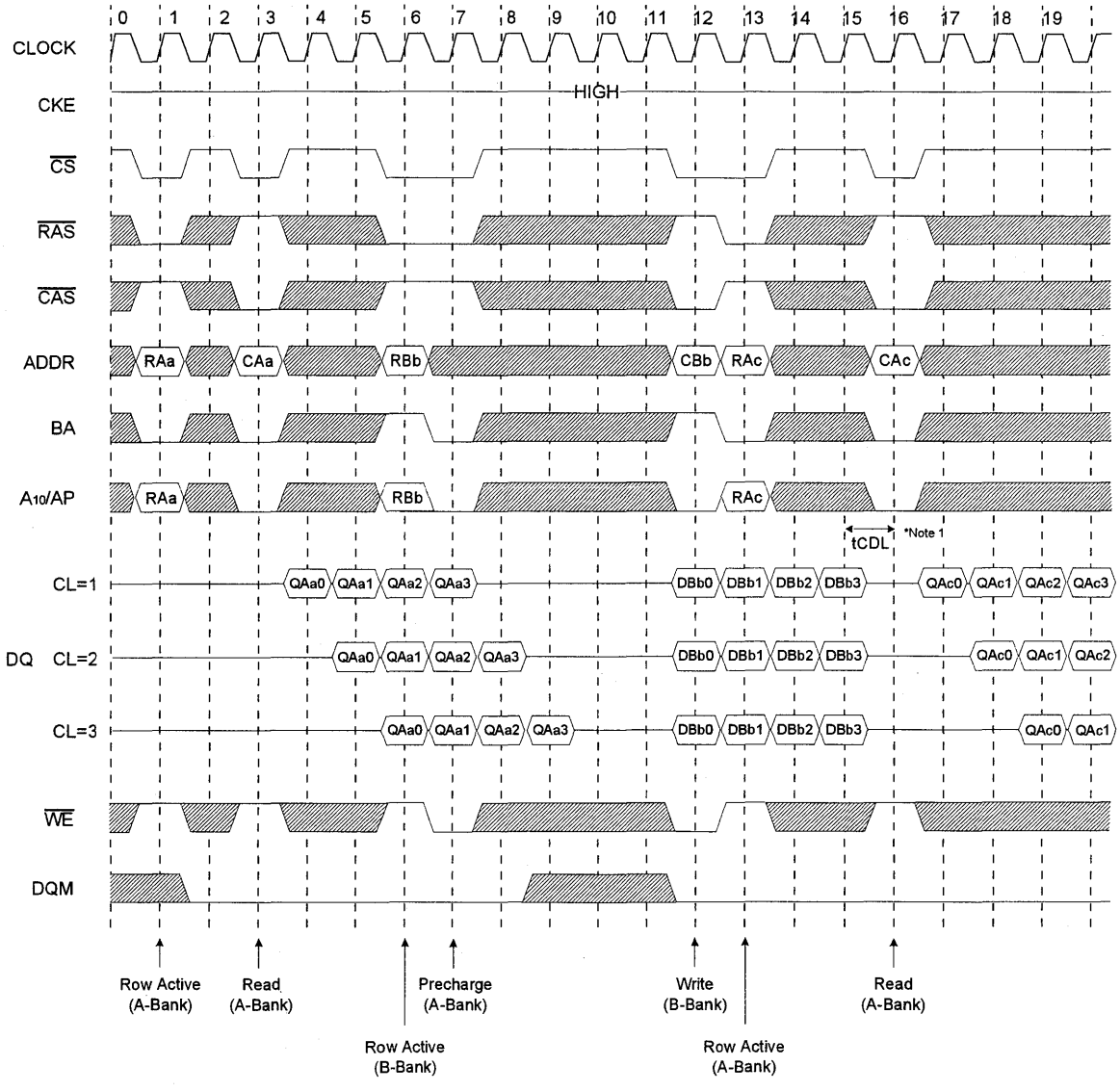
***Note :** 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



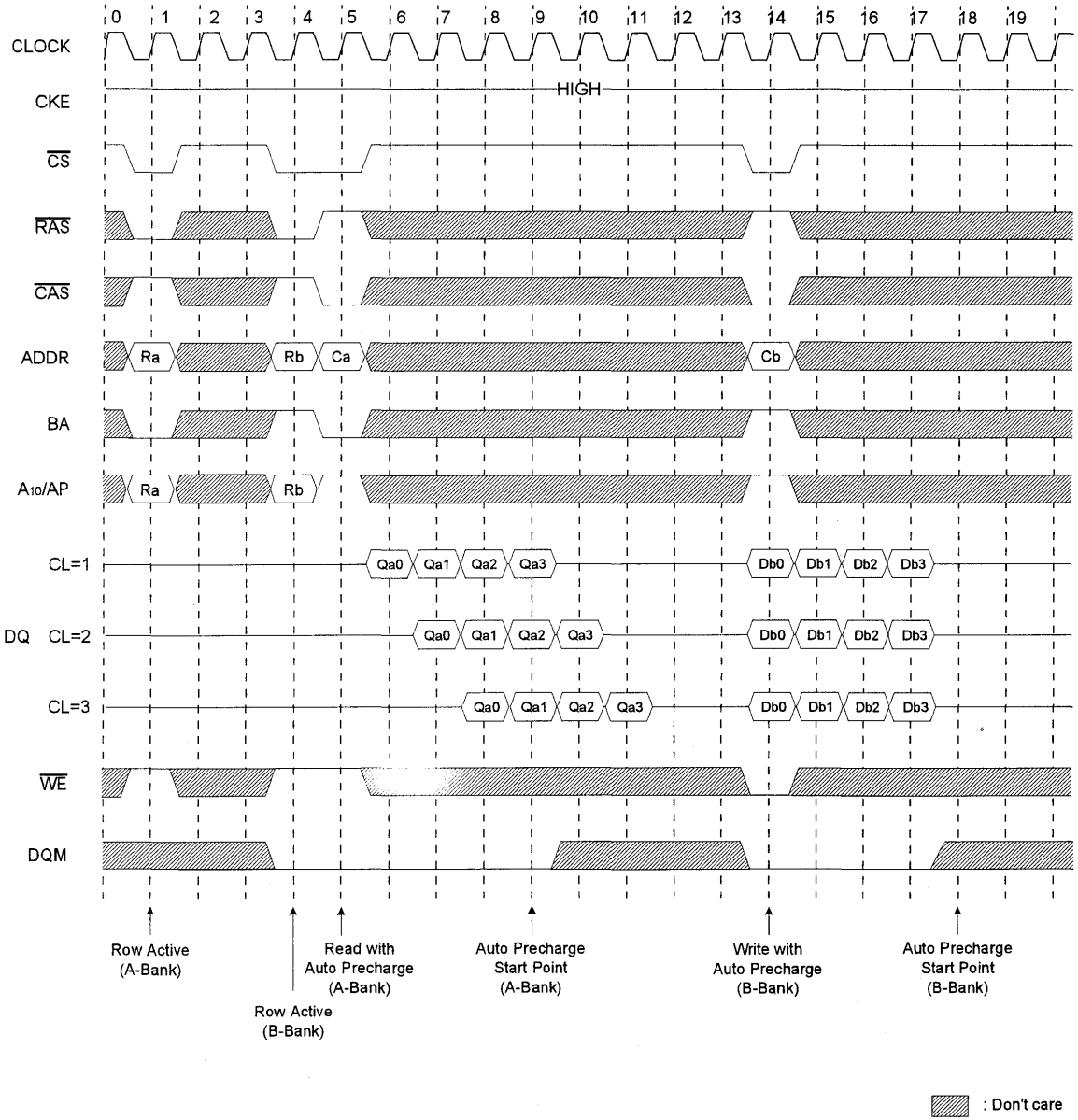
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



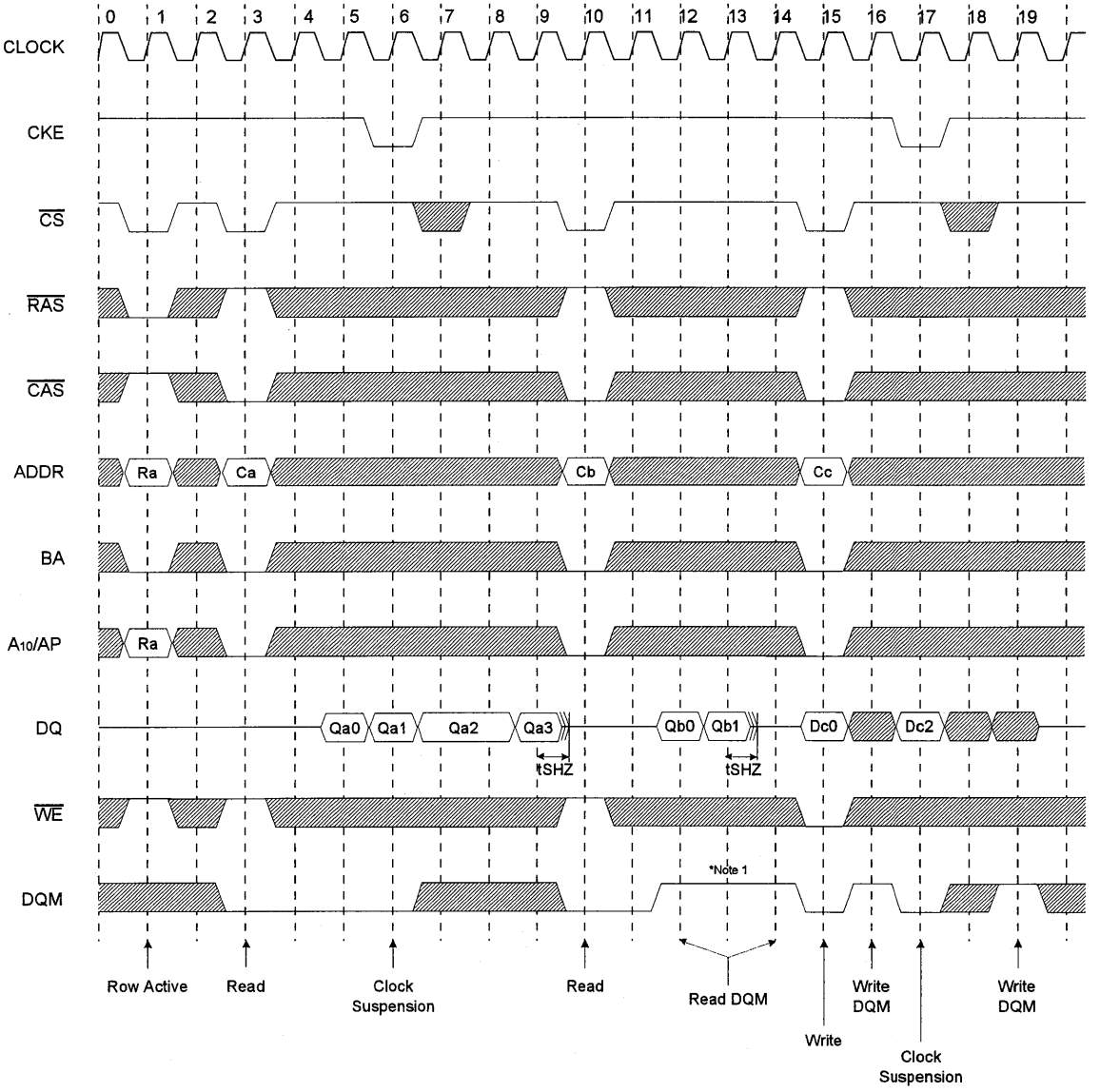
***Note :** 1. t_{CDL} should be met to complete write.

Read & Write Cycle with Auto Precharge @Burst Length=4



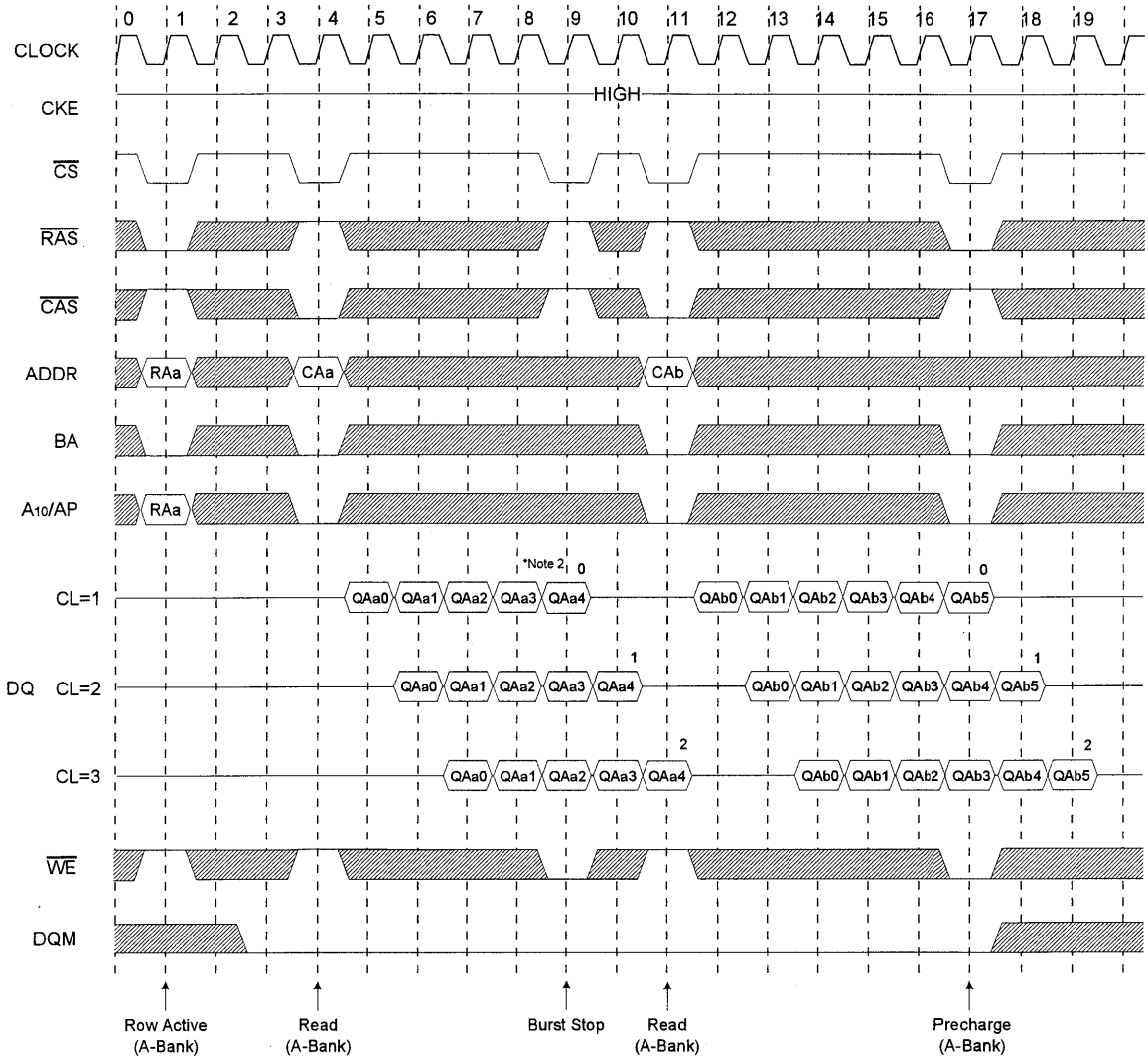
***Note :** 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



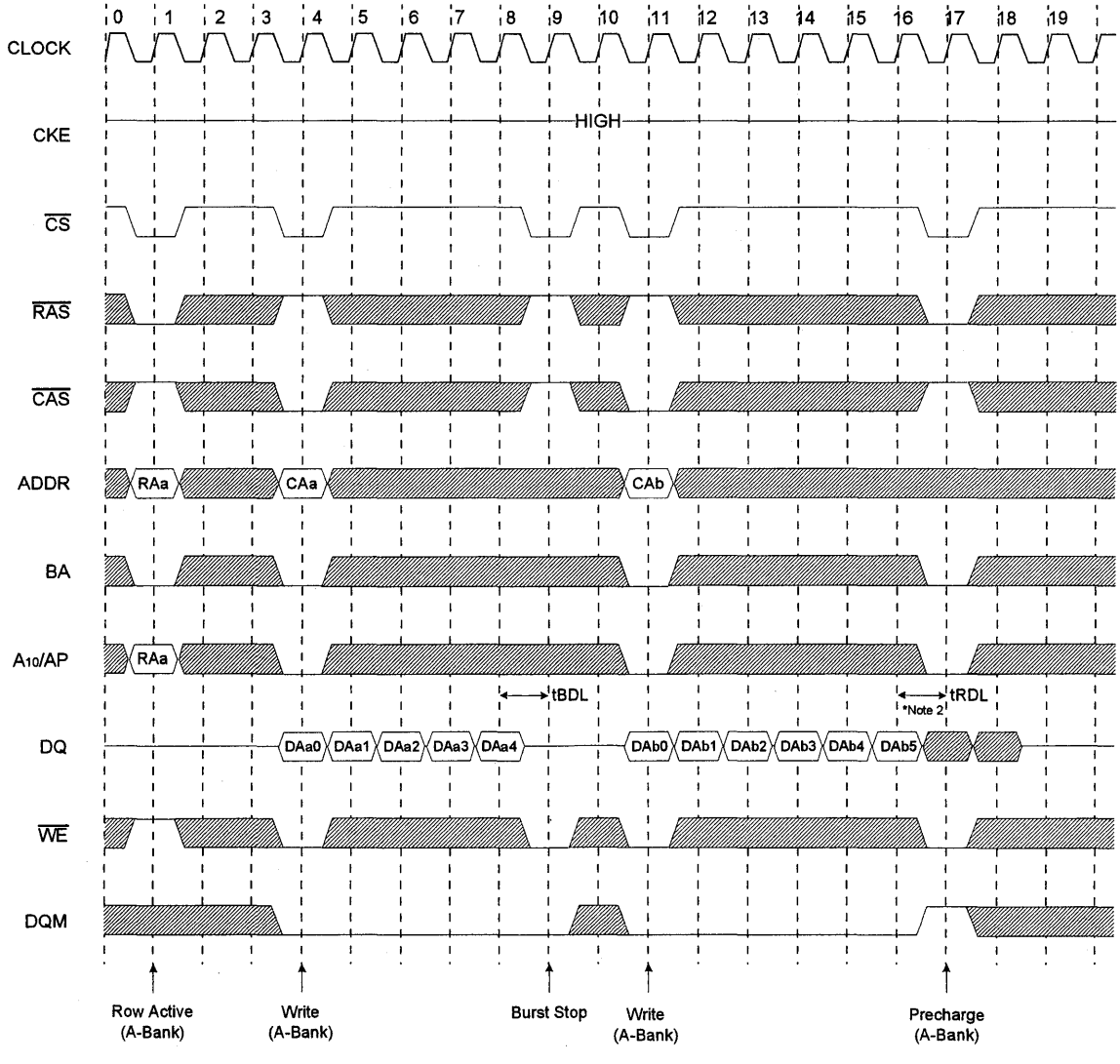
***Note :** 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length=Full page



***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 0. 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

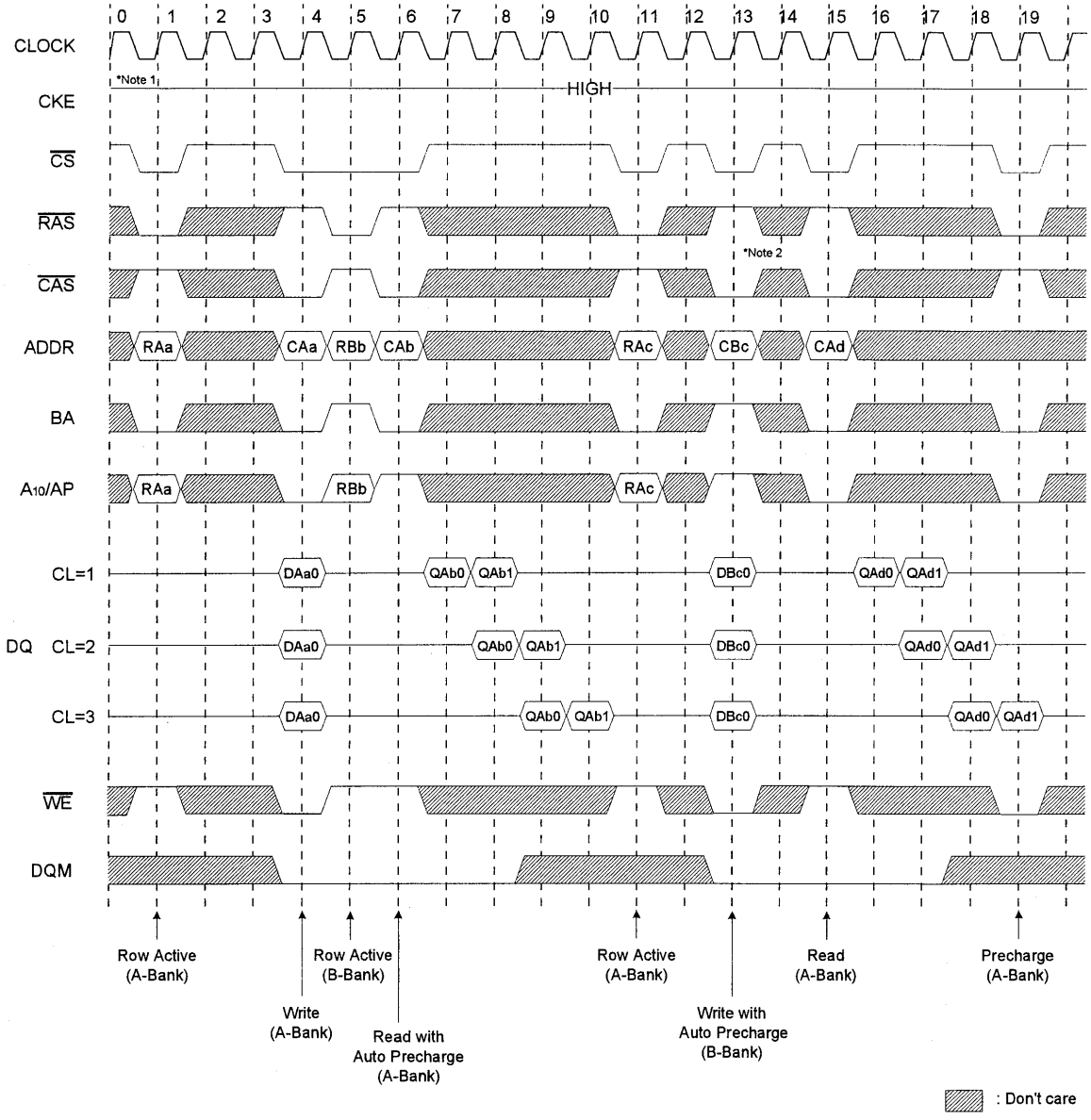
Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length=Full page



***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

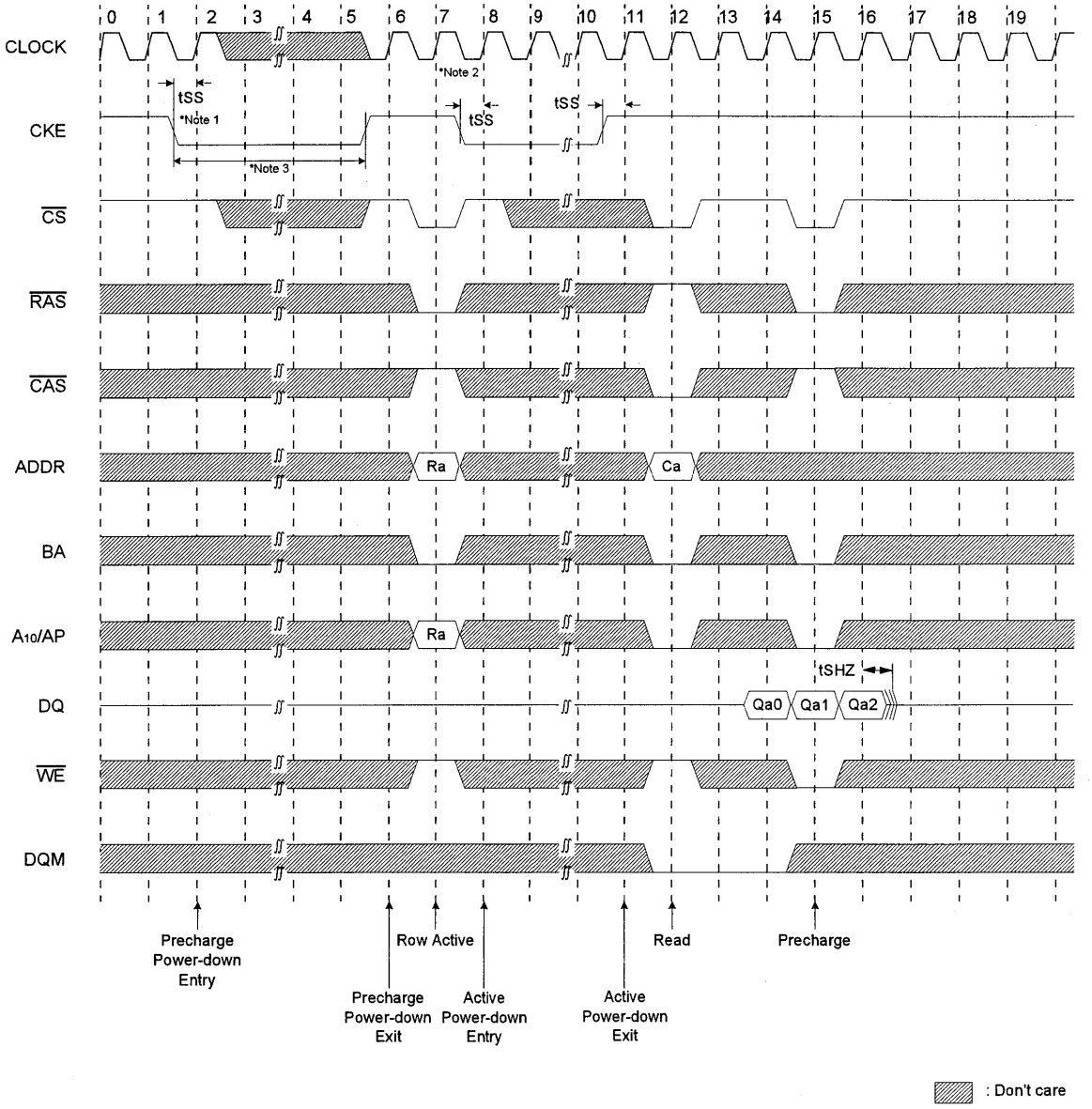
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



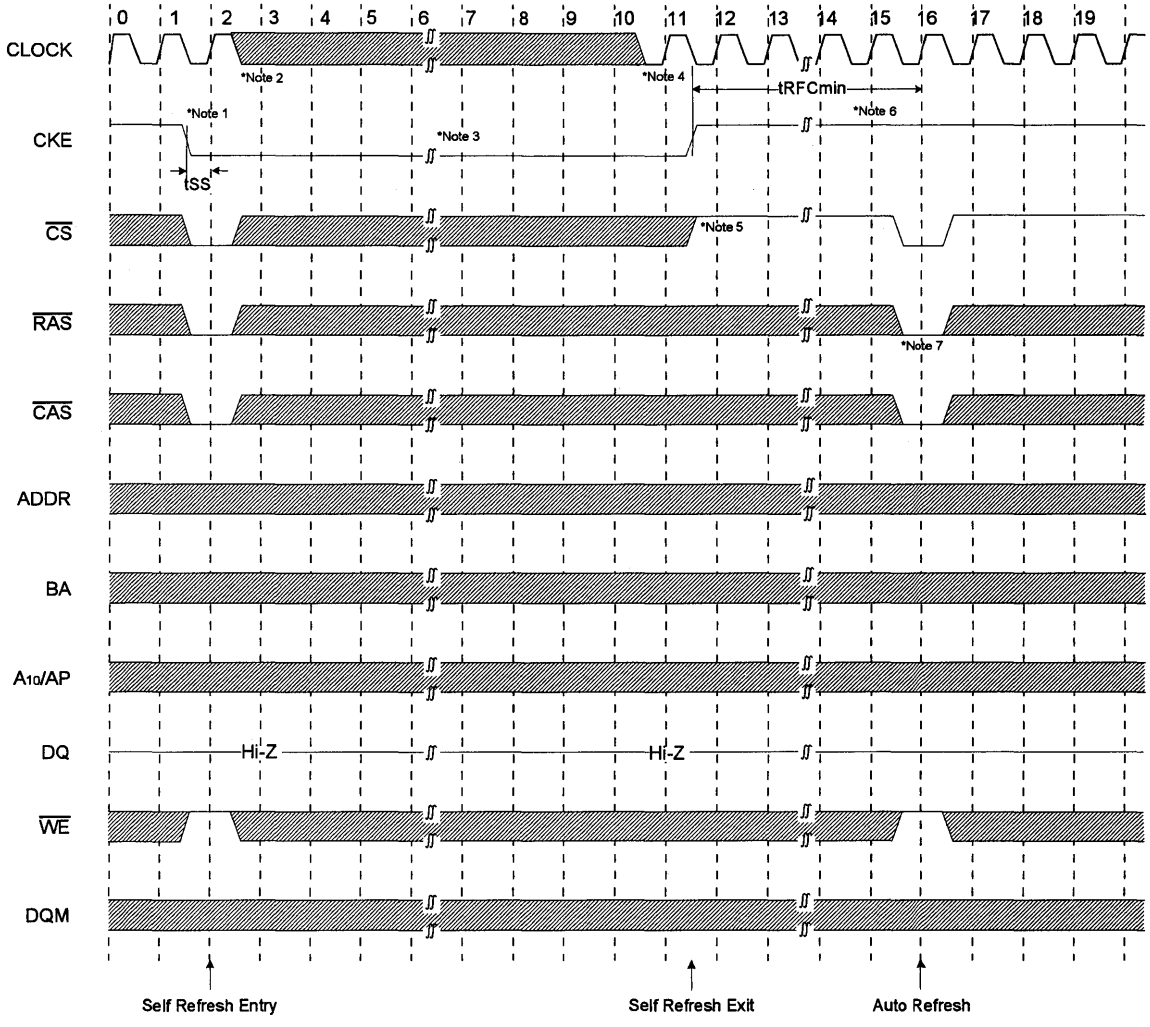
***Note :** 1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regaredless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



***Note :** 1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



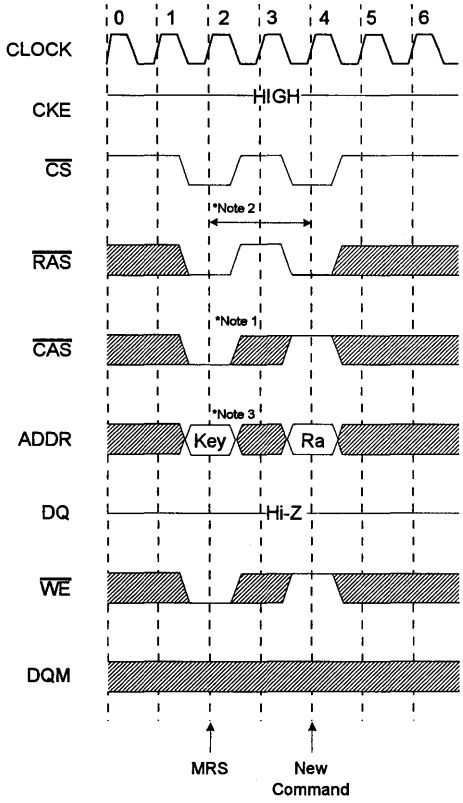
***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

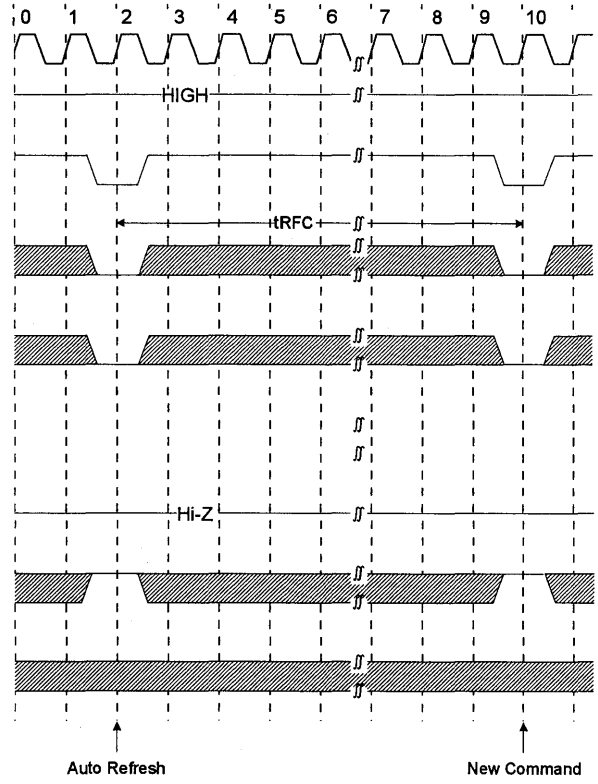
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

* Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

***Note :** 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

64M 2Banks SDRAM (A-die)

- DATA SHEETS
- DEVICE OPERATIONS-II
- TIMING DIAGRAM-II

DATA SHEETS

8M x 4Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

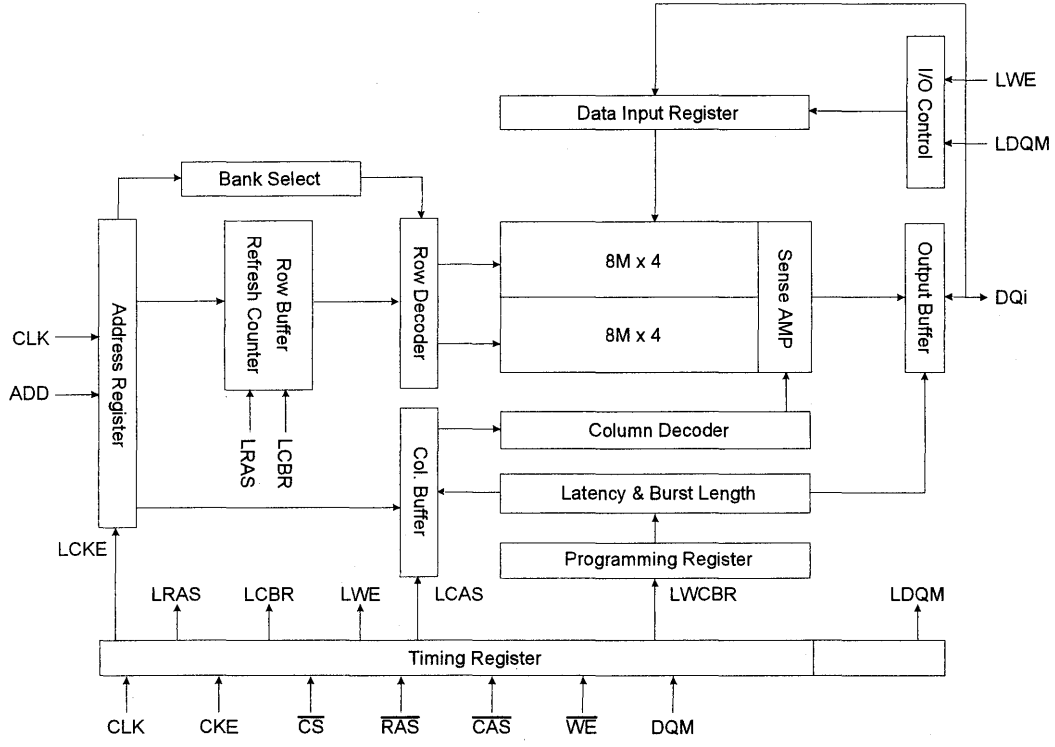
GENERAL DESCRIPTION

The KM44S16020A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 8,388,608 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
KM44S16020AT-G/F8	125MHz	LVTTL	54 TSOP(II)
KM44S16020AT-G/F10	100MHz		
KM44S16020AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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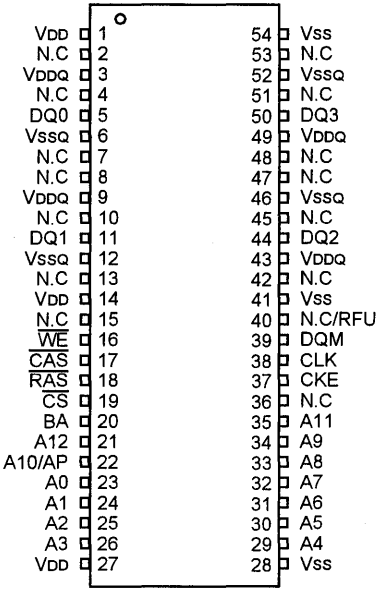
PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{12}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{12}, column address : CA_0 ~ CA_9
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
DQ_0 ~ 3	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_3)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

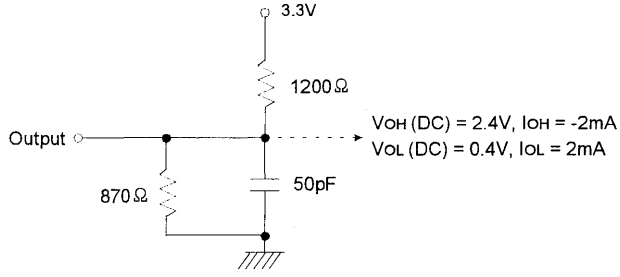
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		125	110	95	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		45			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		30			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD}=2CLKs	3	175	140	120	mA	1
			2	120	110	95		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		3			mA	3
				500			uA	4

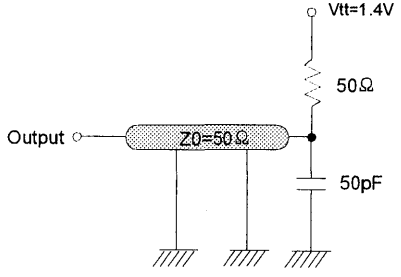
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM44S16020AT-G**
4. KM44S16020AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM44S16020AT-8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM44S16020AT-10 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM44S16020AT-12 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

4M x 8Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The KM48S8020A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 4,194,304 words by 8 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

1

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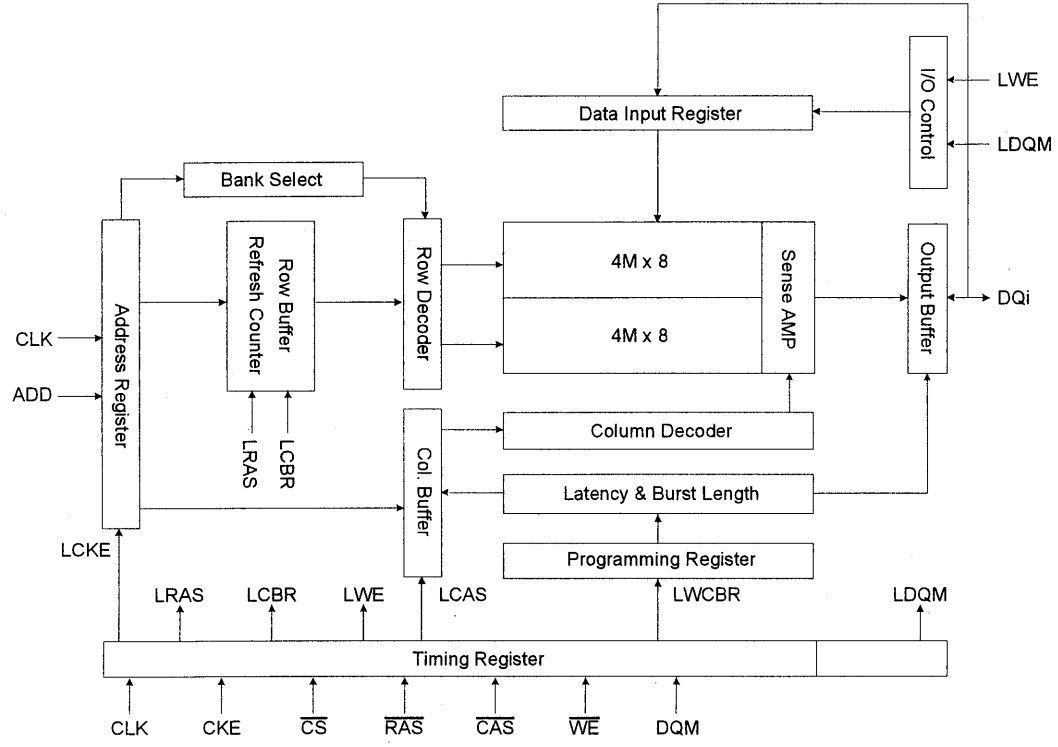
Part NO.	MAX Freq.	Interface	Package
KM48S8020AT-G/F8	125MHz	LVTTL	54 TSOP(II)
KM48S8020AT-G/F10	100MHz		
KM48S8020AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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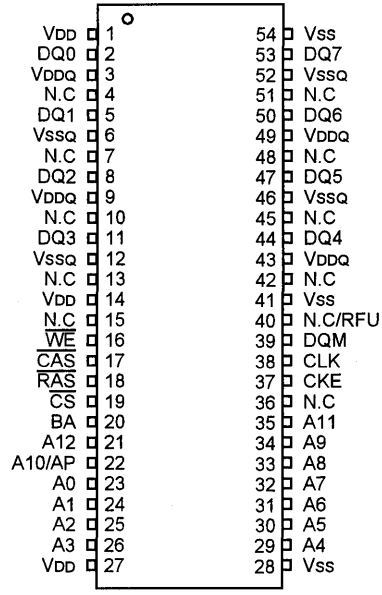
PIN CONFIGURATION (TOP VIEW)



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CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
$A_0 \sim A_{12}$	*Address*	Row / column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{12}$, column address : $CA_0 \sim CA_8$
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim 7}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_7)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

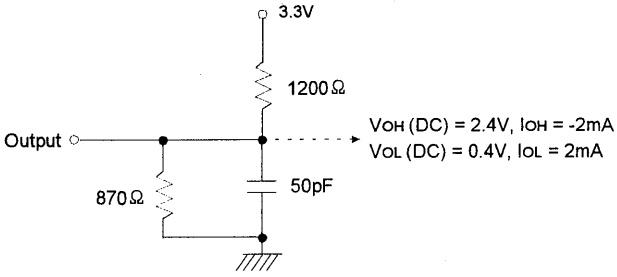
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		130	115	95	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		45			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		30			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	185	150	125	mA	1
			2	125	115	100		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		3			mA	3
				500			uA	4

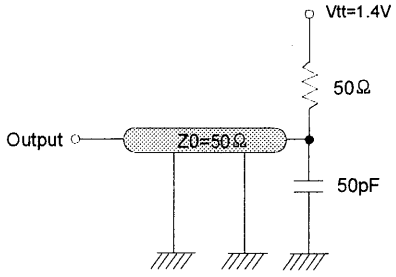
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM48S8020AT-G**
4. KM48S8020AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM48S8020AT-8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM48S8020AT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM48S8020AT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

2M x 16Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

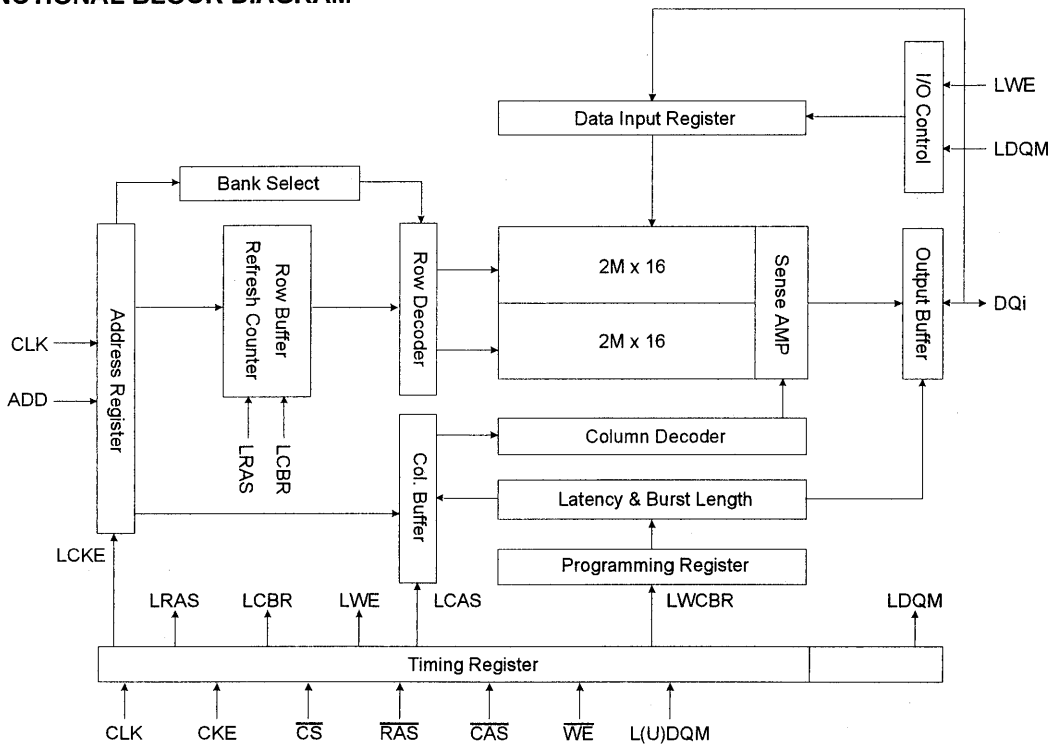
GENERAL DESCRIPTION

The KM416S4020A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

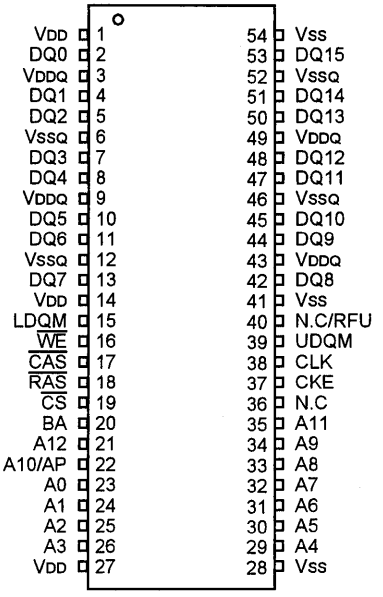
Part NO.	MAX Freq.	Interface	Package
KM416S4020AT-G/F8	125MHz	LVTTL	54 TSOP(II)
KM416S4020AT-G/F10	100MHz		
KM416S4020AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{12}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{12}, column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when L(U)DQM active.
DQ_0 ~ 15	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

1

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	2	5	pF

DC CHARACTERISTICS

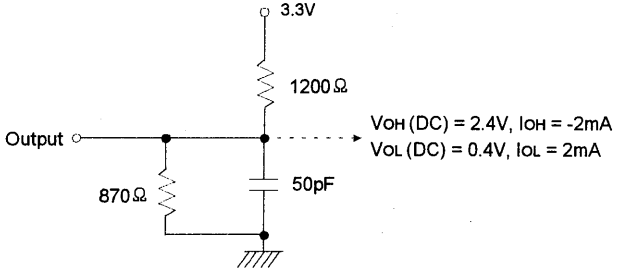
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		140	125	105	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		50			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		35			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	200	165	135	mA	1
			2	140	130	115		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		3			mA	3
				500			uA	4

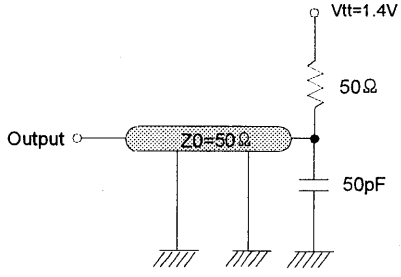
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM416S4020AT-G**
4. KM416S4020AT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S4020AT-8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM416S4020AT-10 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM416S4020AT-12 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don' t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

DEVICE OPERATIONS-II

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA	A_{12} ~ A_{10}/AP	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A_8	A_7	Type	A_6	A_5	A_4	Latency	A_3	Type	A_2	A_1	A_0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A_9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : x4 (1024), x8 (512), x16 (256)

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	0	1	2	3	0	1	0	3	2
1	1	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between VIL and VIH. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tss" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESS (BA)

: In case x 4

This SDRAM is organized as two independent banks of 8,388,608 words x 4 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank address BA is latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as two independent banks of 4,194,304 words x 8 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank address BA is latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as two independent banks of 2,097,152 words x 16 bits memory arrays. The BA input is latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank address BA is latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A12)

: In case x 4

The 23 address bits are required to decode the 8,388,608 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

: In case x 8

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

: In case x 16

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 13 address input pins (A_0 ~ A_{12}). The 13 bit row addresses are latched along with $\overline{RAS}$ and BA during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

DEVICE OPERATIONS (Continued)

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_{12} and BA in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) use A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP ~ A_{12} and BA. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP ~ A_{12} and BA must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has two internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of two banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before the other bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid BA of the bank to be procharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when both banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precahrge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after both banks have satisfied t_{RAS}(min) requirement, performs precharge on both banks. At the end of t_{RP} after performing precharge all, both banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RFC}(min). The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

SELF REFRESH

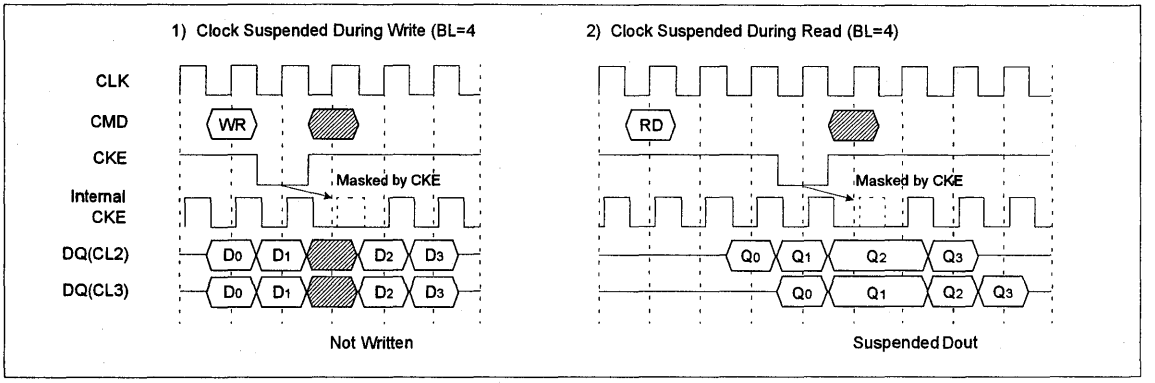
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from both banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.

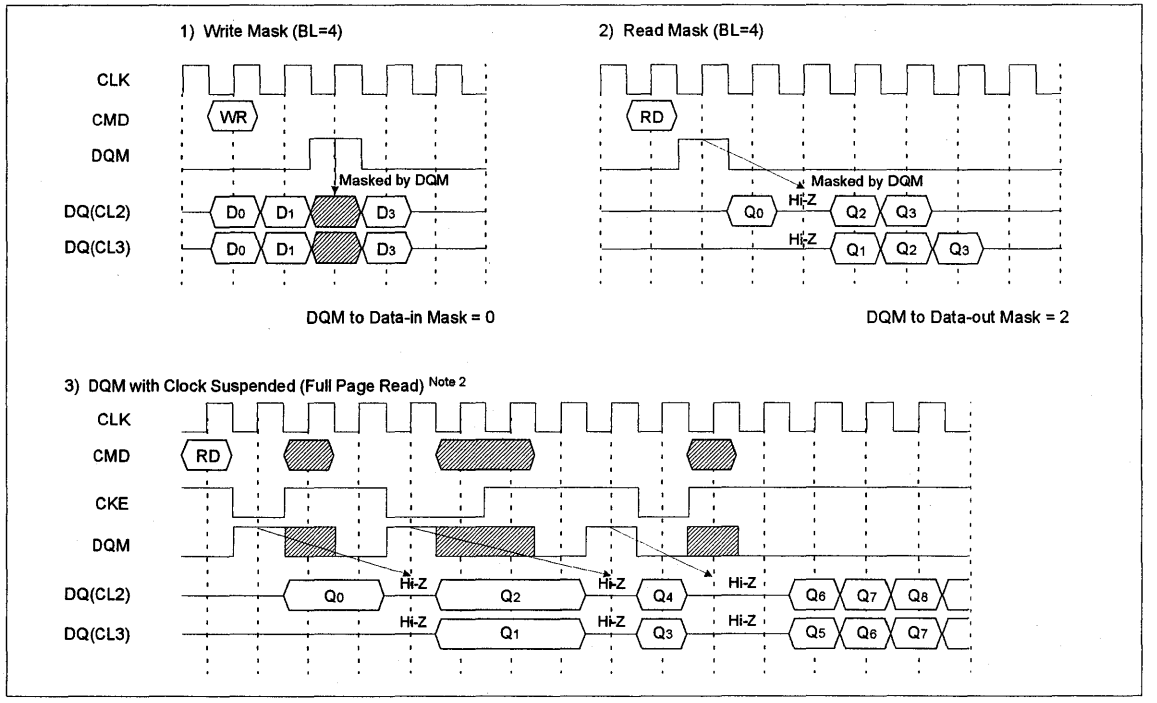
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend



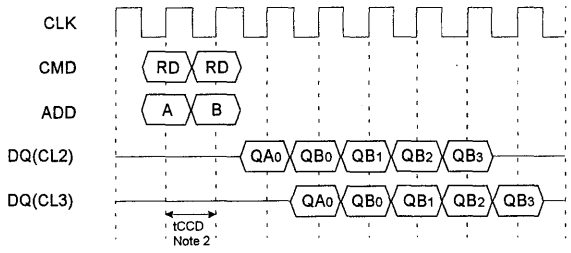
2. DQM Operation



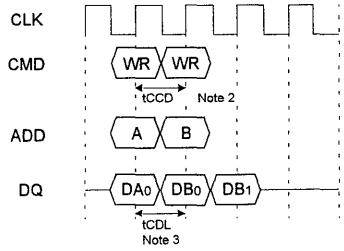
***Note :** 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)

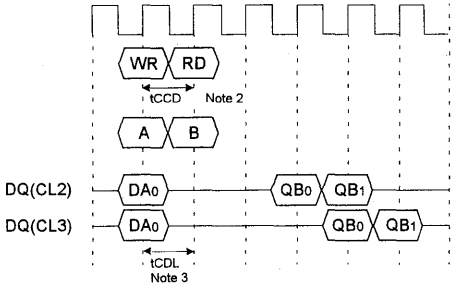
1) Read interrupted by Read (BL=4) Note 1



2) Write interrupted by Write (BL=2)

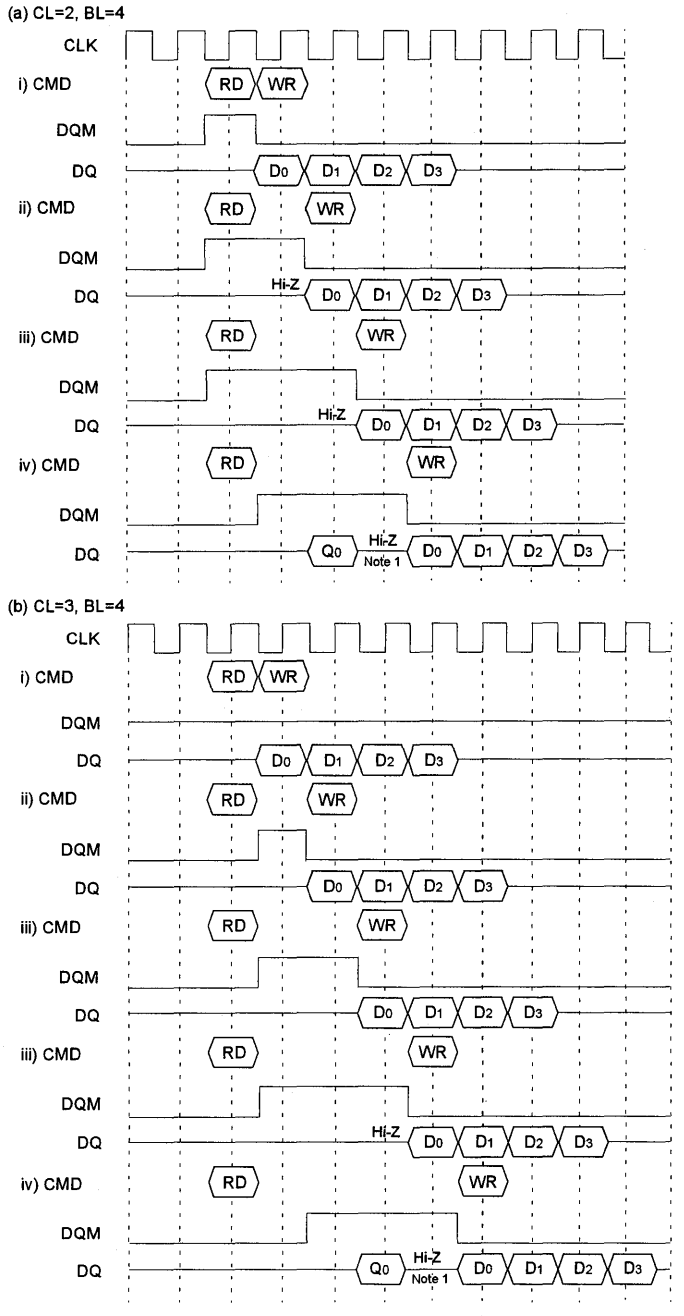


3) Write interrupted by Read (BL=2)



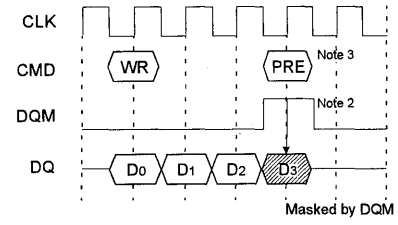
***Note :** 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



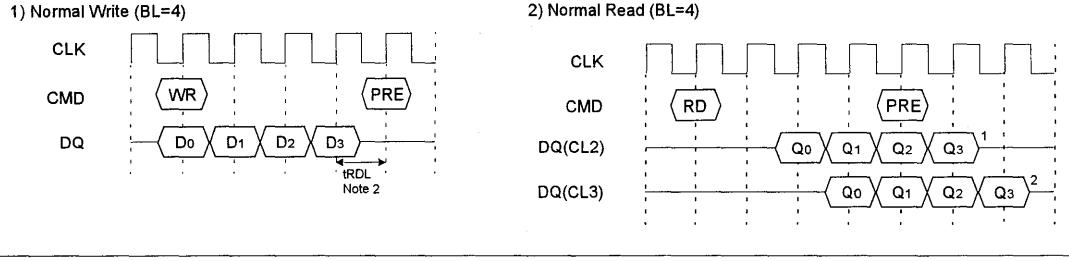
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

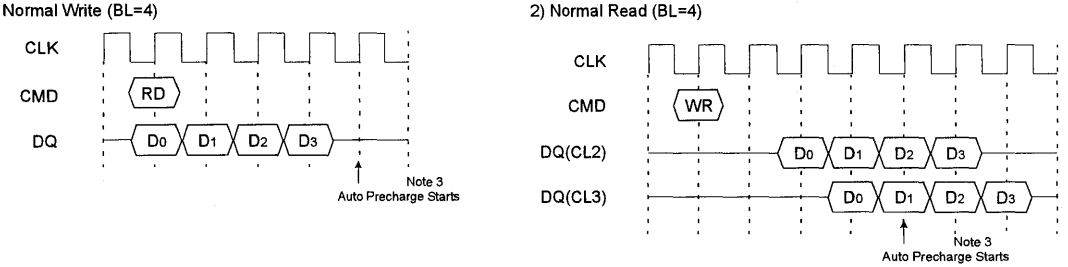


*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only the other bank precharge of dual banks operation.

6. Precharge



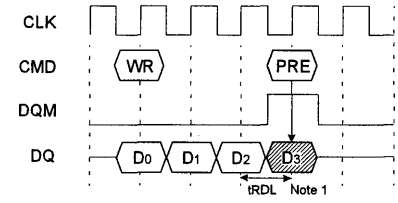
7. Auto Precharge



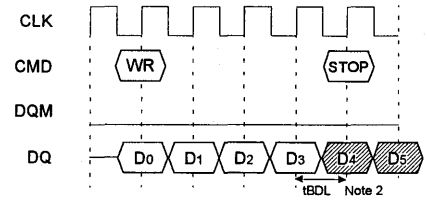
*Note : 1. t_{RDL} : Last data in to row precharge delay
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same/other bank is illegal.

8. Burst Stop & Interrupted by Precharge

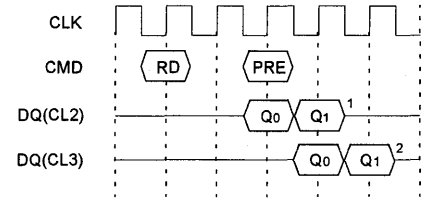
1) Normal Write (BL=4)



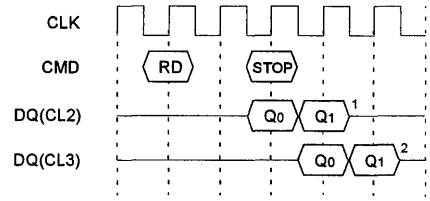
2) Write Burst Stop (BL=8)



3) Read Interrupted by Precharge (BL=4)

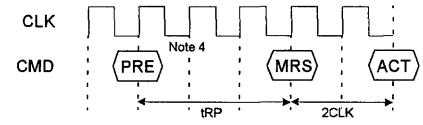


4) Read Burst Stop (BL=4)



9. MRS

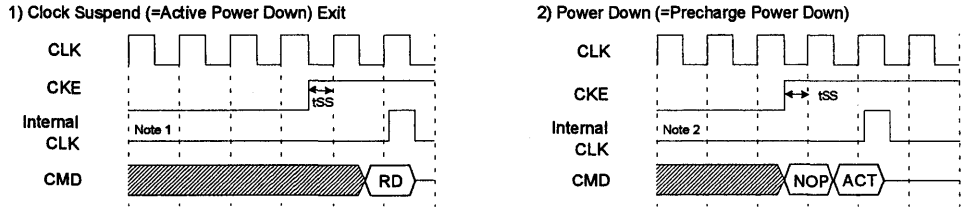
1) Mode Register Set



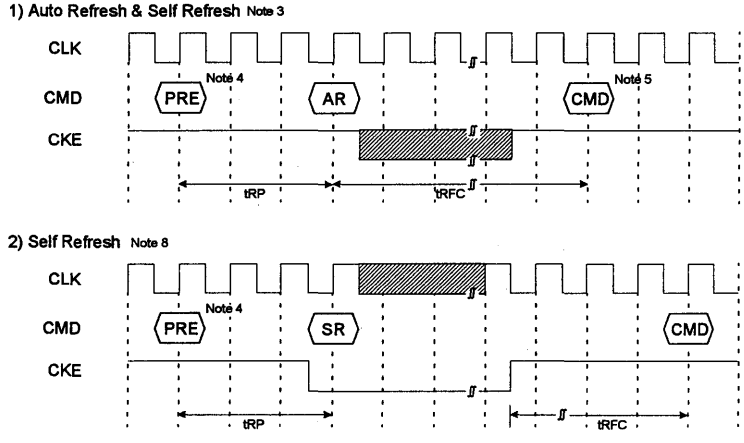
***Note :** 1. t_{RDL} : 1 CLK

2. t_{BDL} : 1 CLK ; Last data in to burst stop delay.
   Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectiviely.
4. PRE : Both banks precharge if necessary.
   MRS can be issued only at both banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



***Note :** 1. Active power down : one or both banks active state.
2. Precharge power down : both banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, both banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refreh mode, refresh interval and refresh operation are perfomed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4096 cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". At the end of the burst length, burst will be stop automatically.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 1 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after tRP	
	L	H	H	H	X	X	NOP --> Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP --> Idle after tRPL	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clcok and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clcok Suspend	

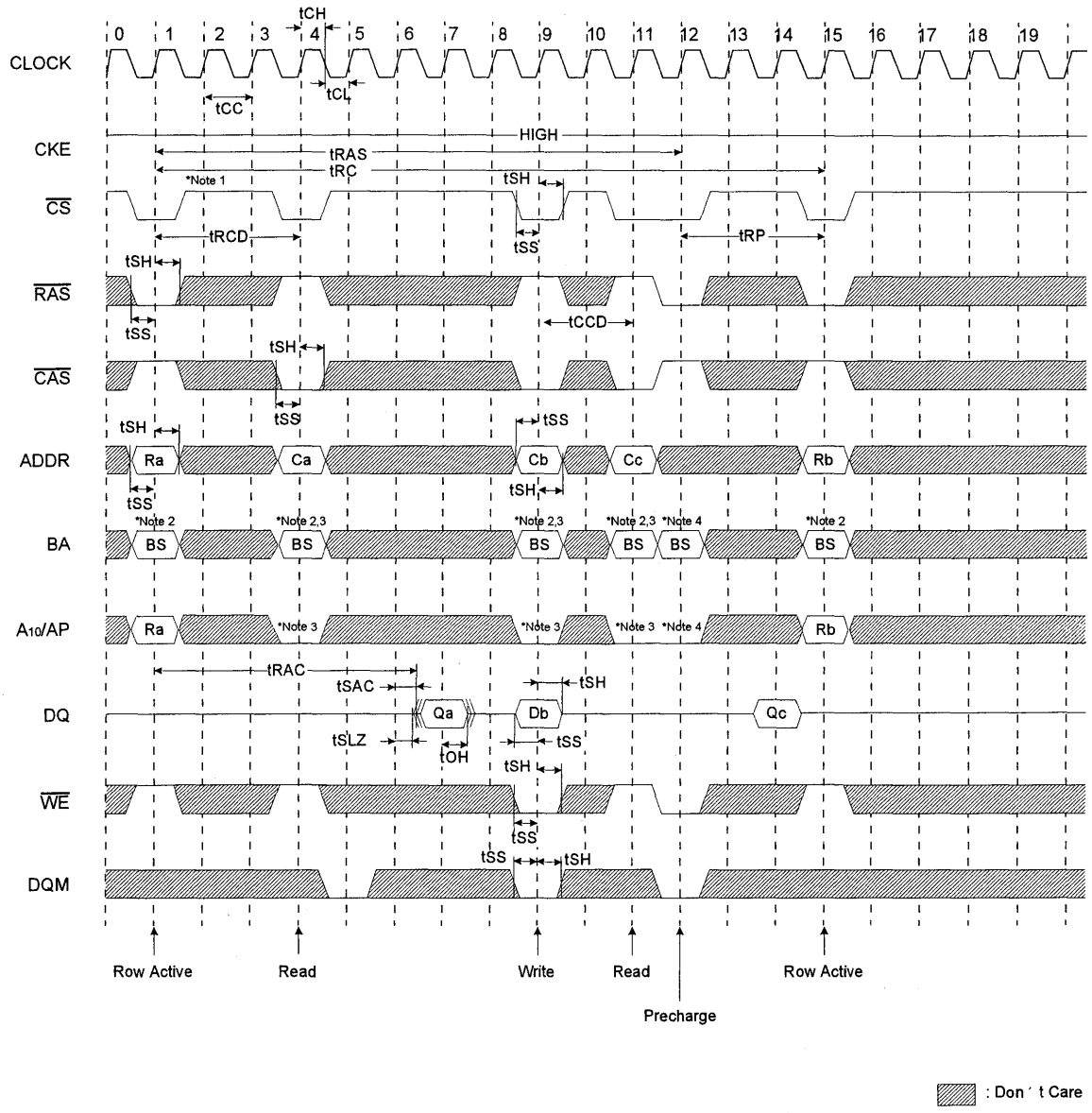
Abbreviations : ABI = All Banks Idle, RA = Row Address

***Note :** 6. CKE low to high transition is asynchronous.

7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + tss must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the both banks idle state.
9. Must be a legal command.

TIMING DIAGRAM-II

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



*Note : 1. All inputs expect CKE & DQM can be don´t care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

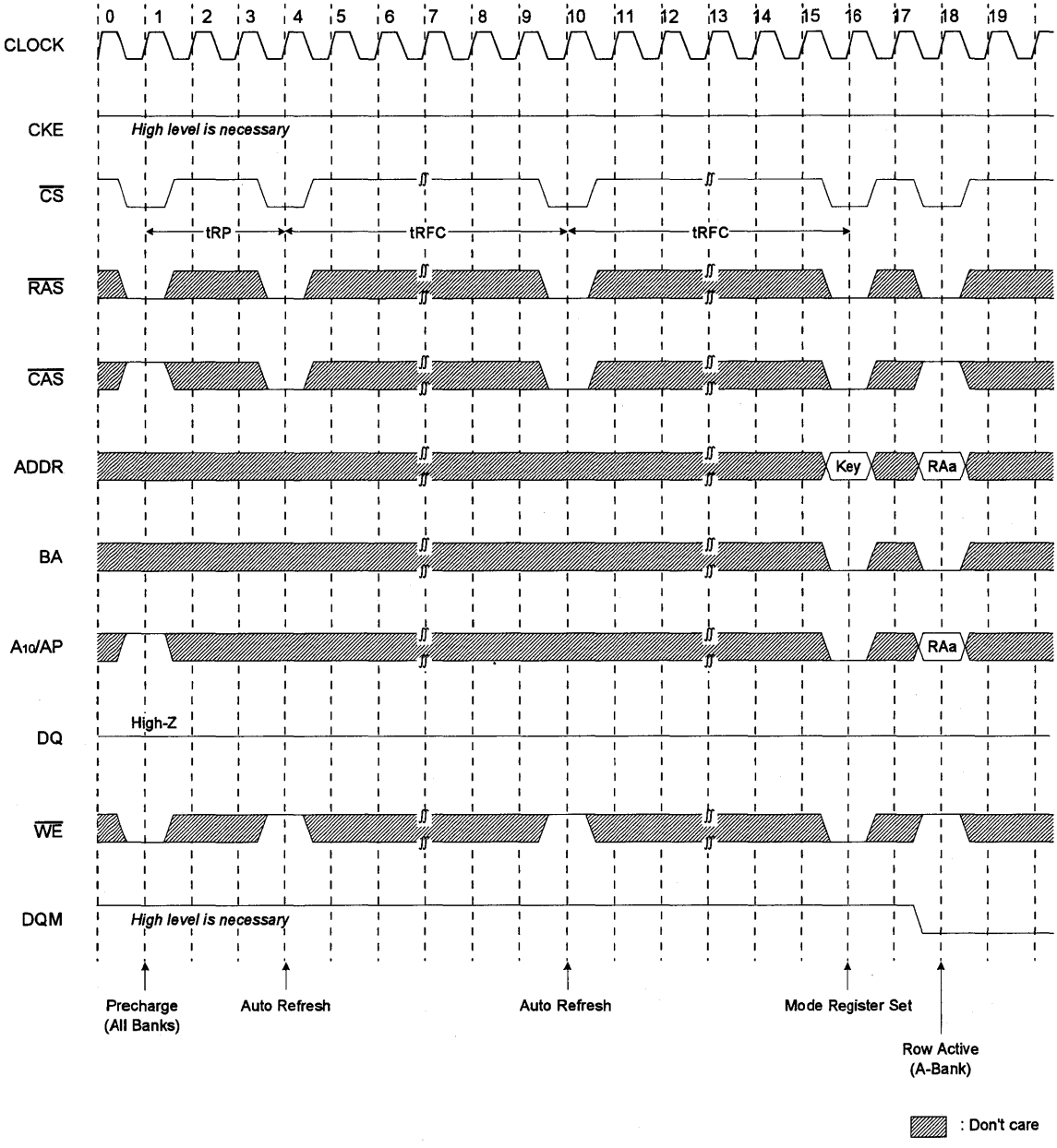
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

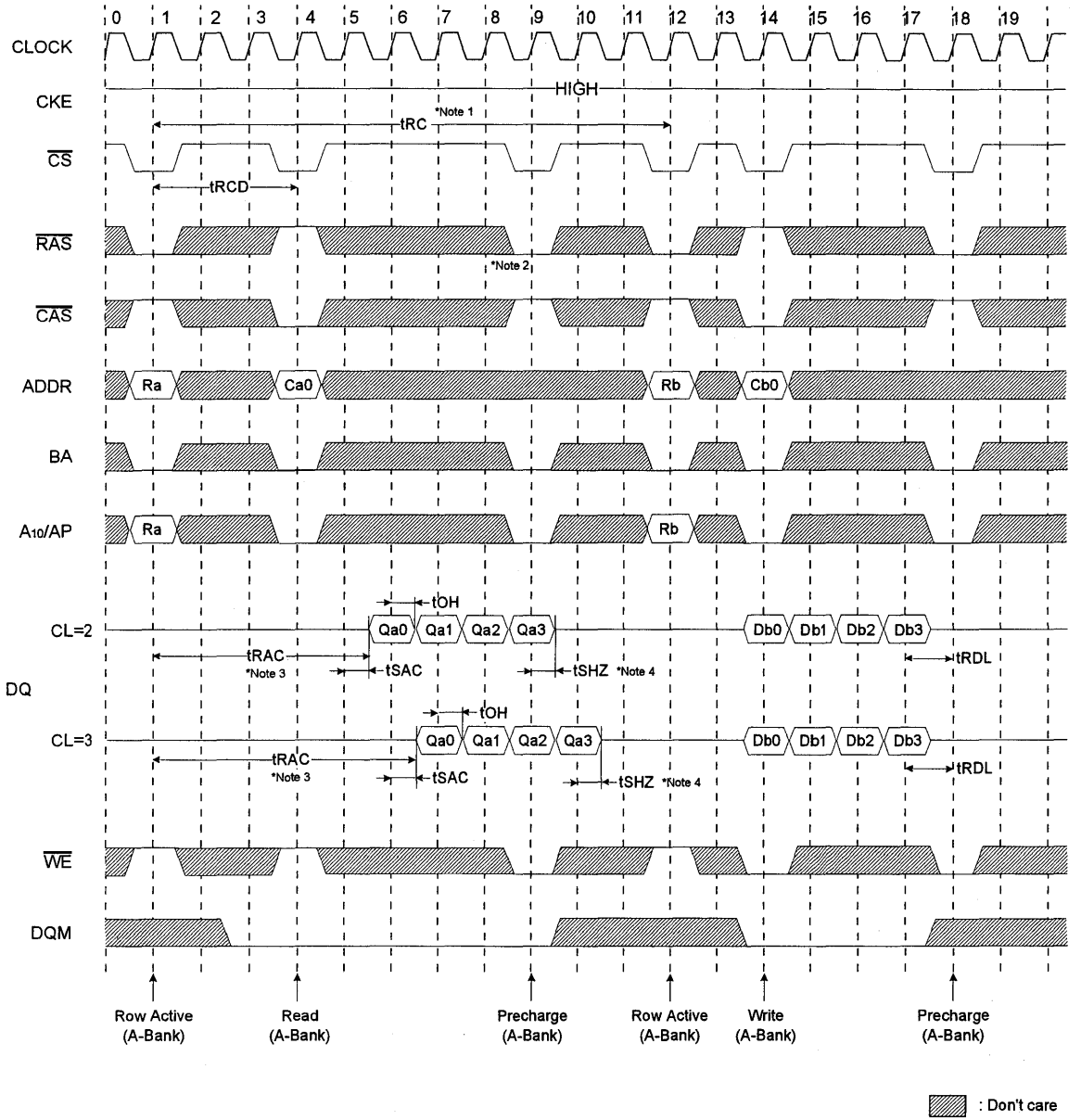
4. A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

Power Up Sequence

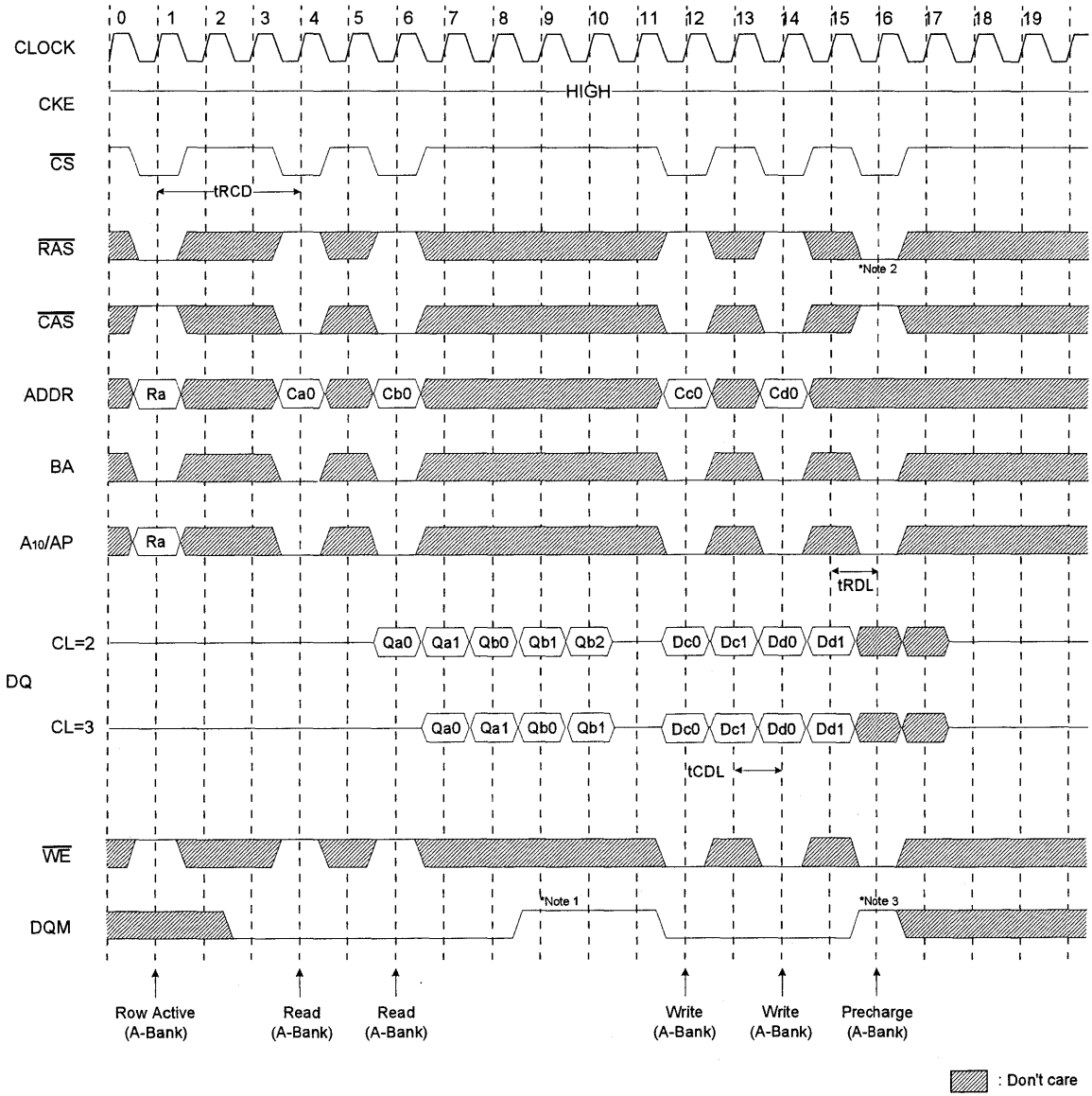


Read & Write Cycle at Same Bank @Burst Length=4



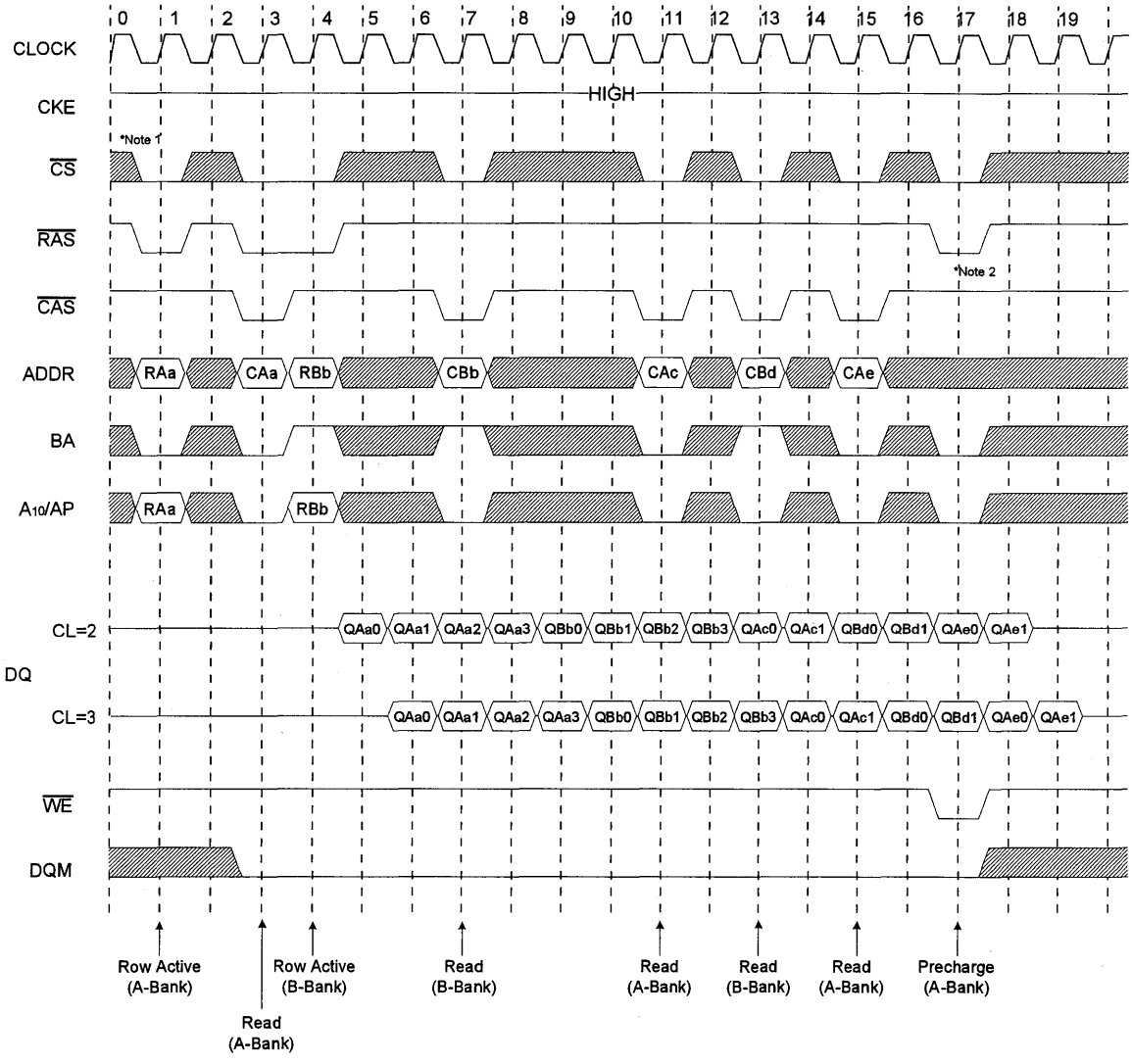
***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @Burst Length=4



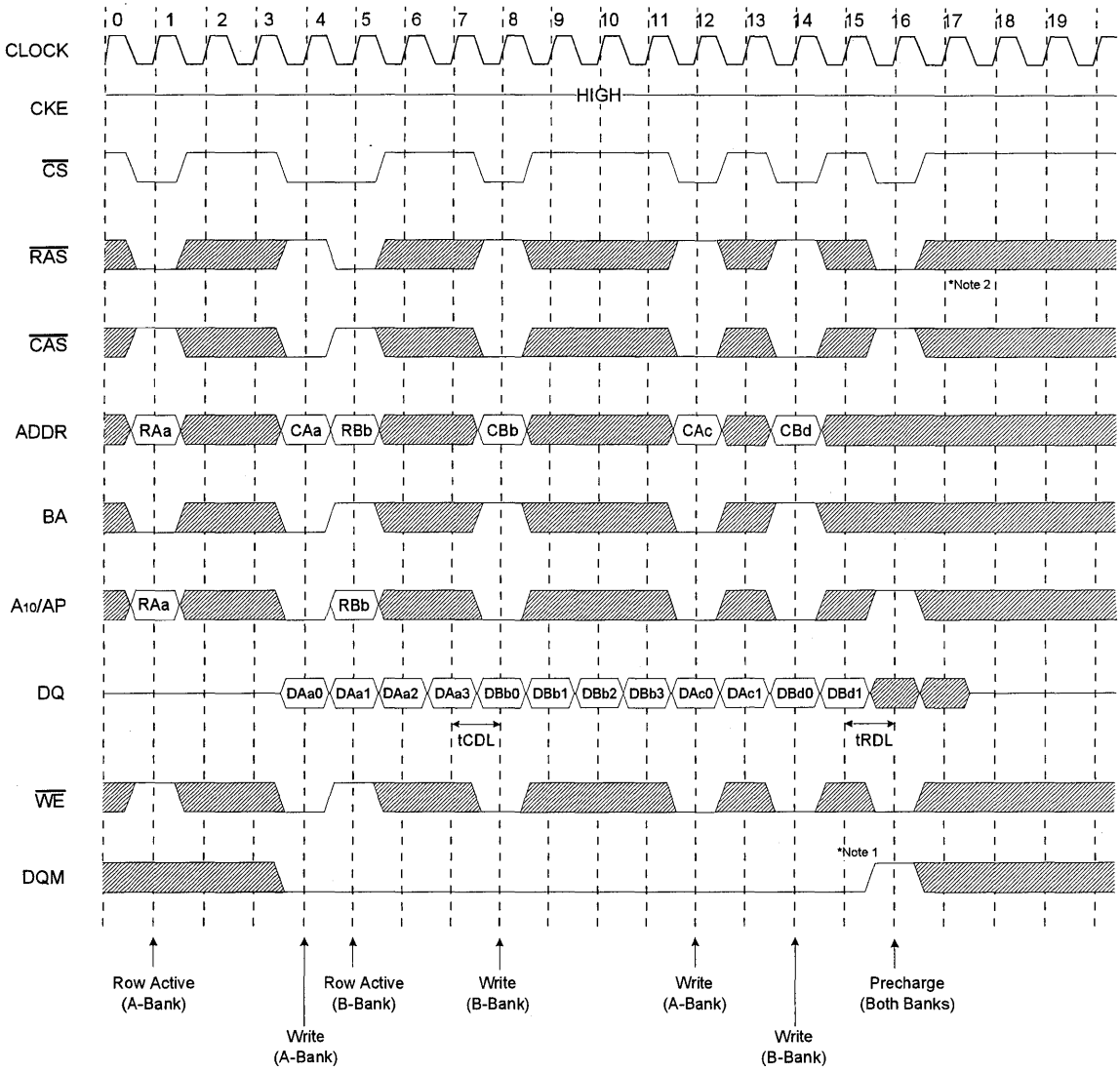
***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Page Read Cycle at Different Bank @Burst Length=4



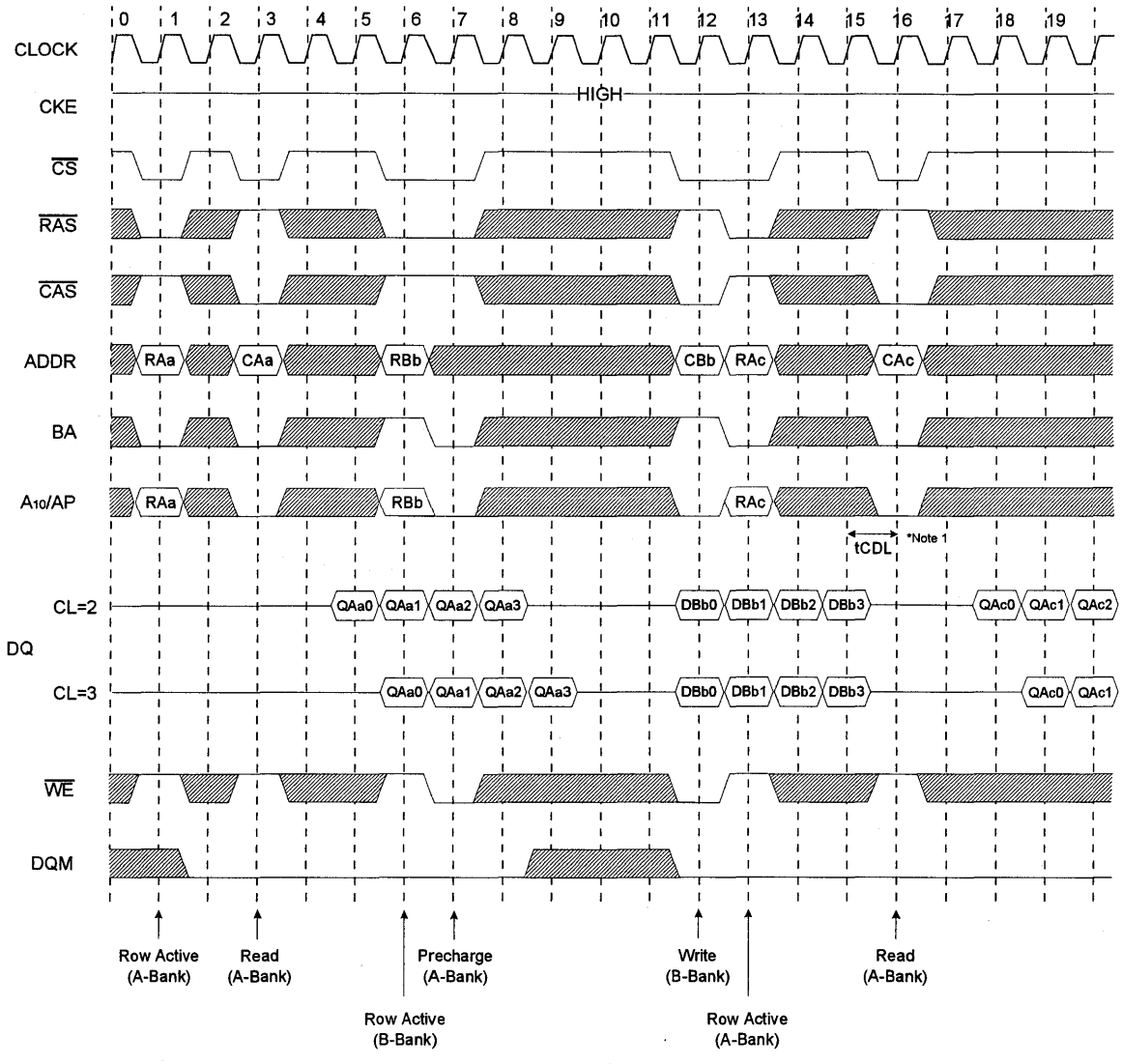
*Note : 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



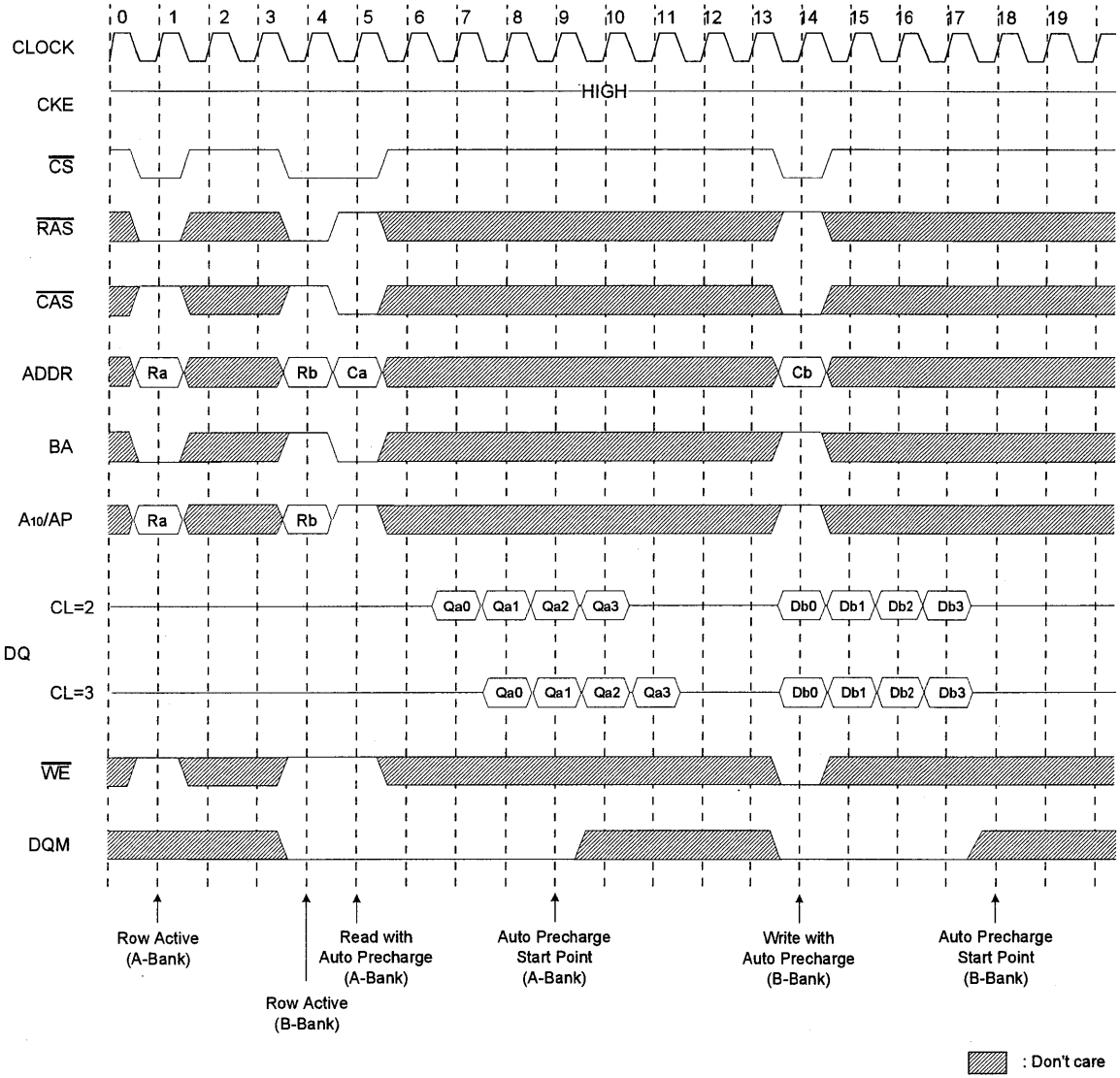
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



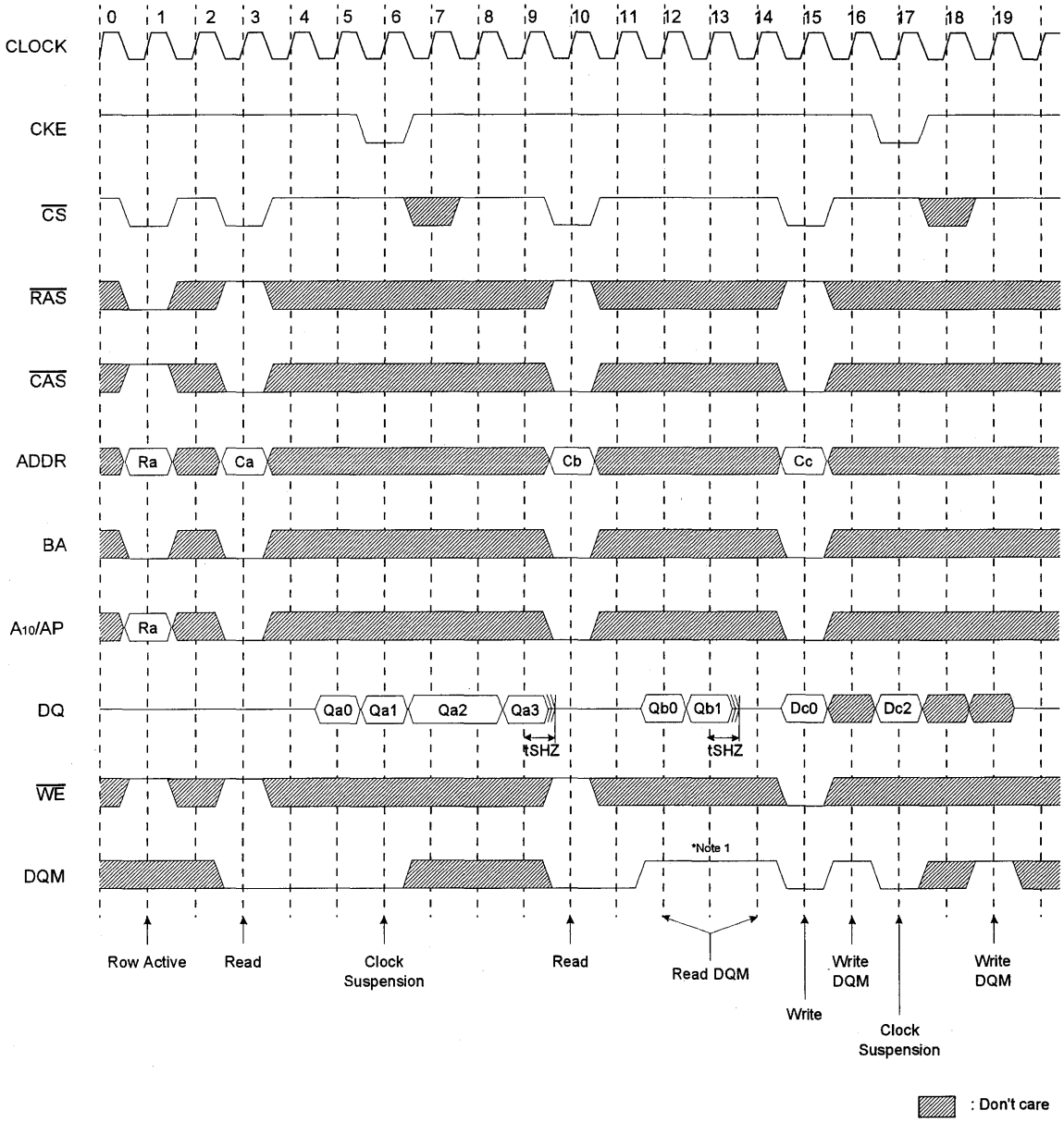
***Note :** 1. tCDL should be met to complete write.

Read & Write Cycle with Auto Precharge @Burst Length=4



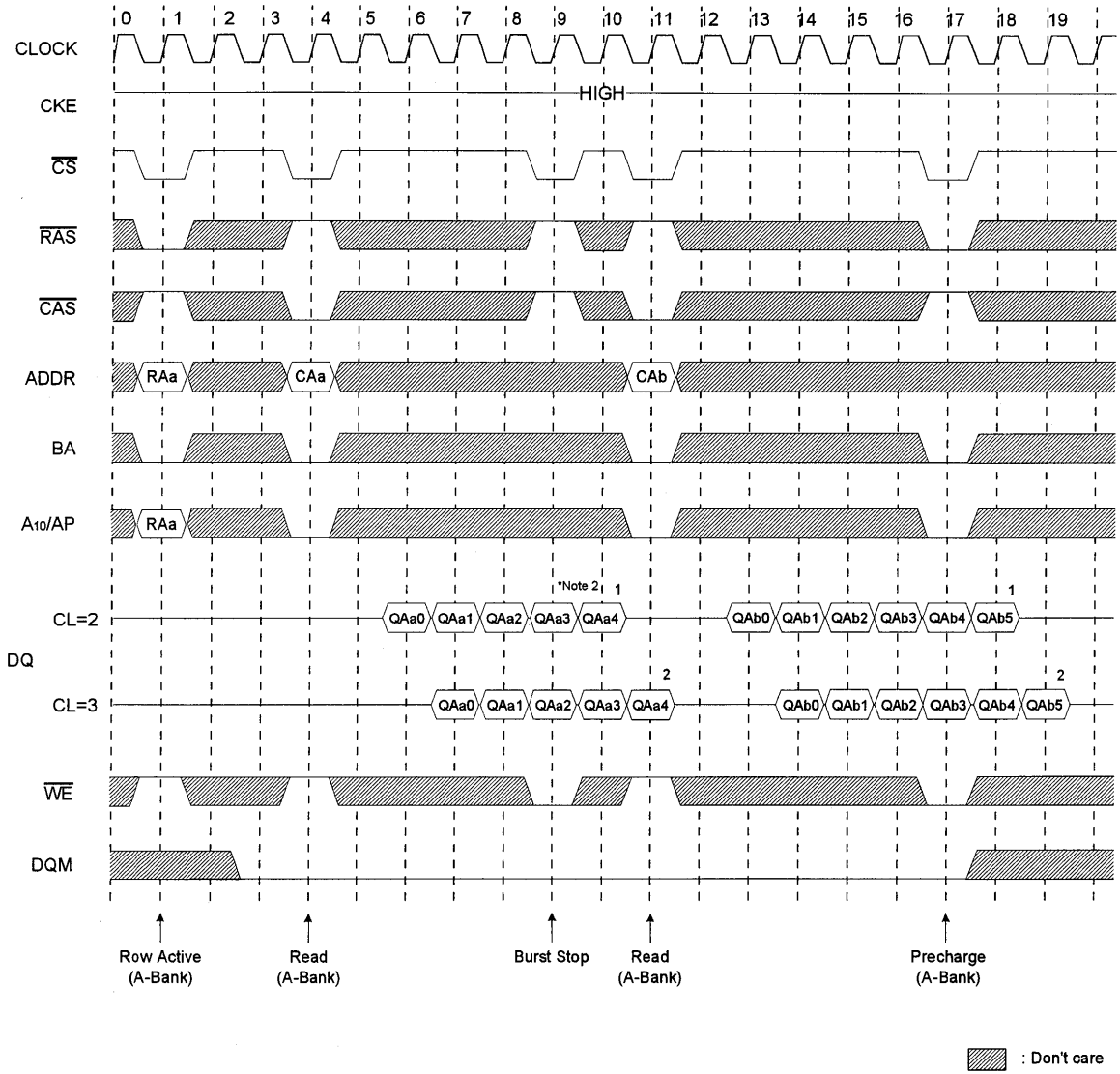
***Note :** 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



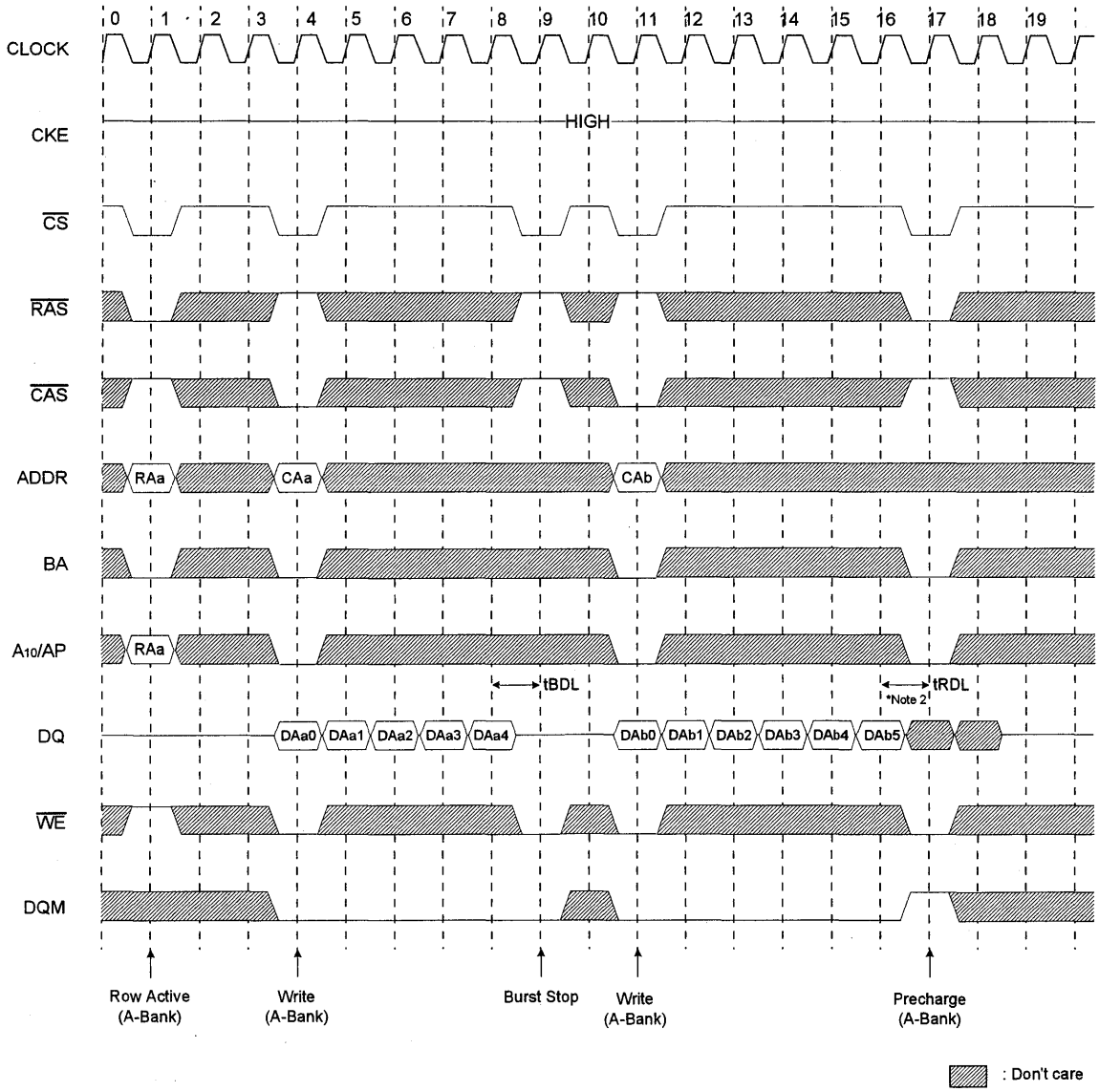
***Note :** 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length=Full page



***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length=Full page

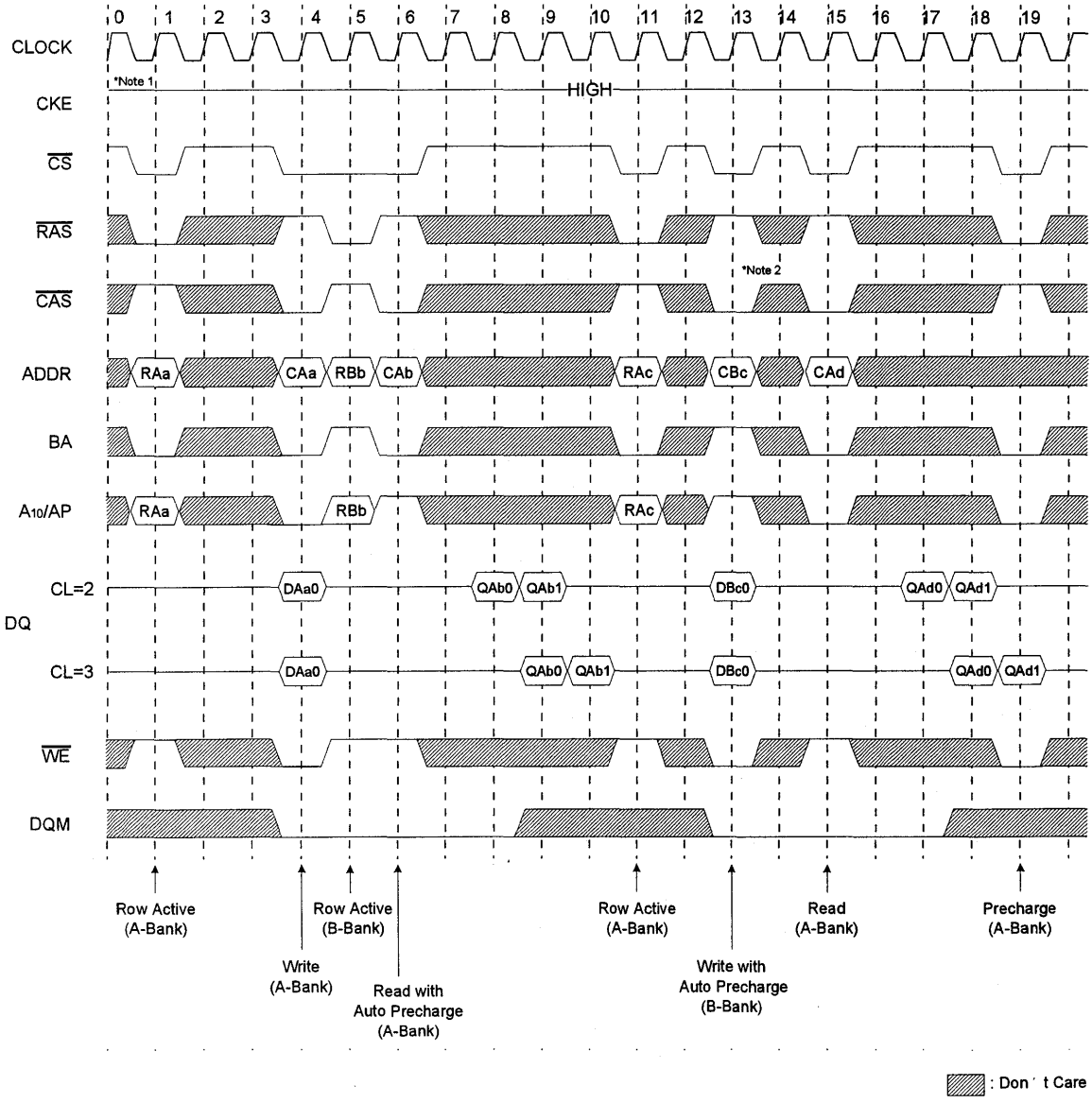


*Note : 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

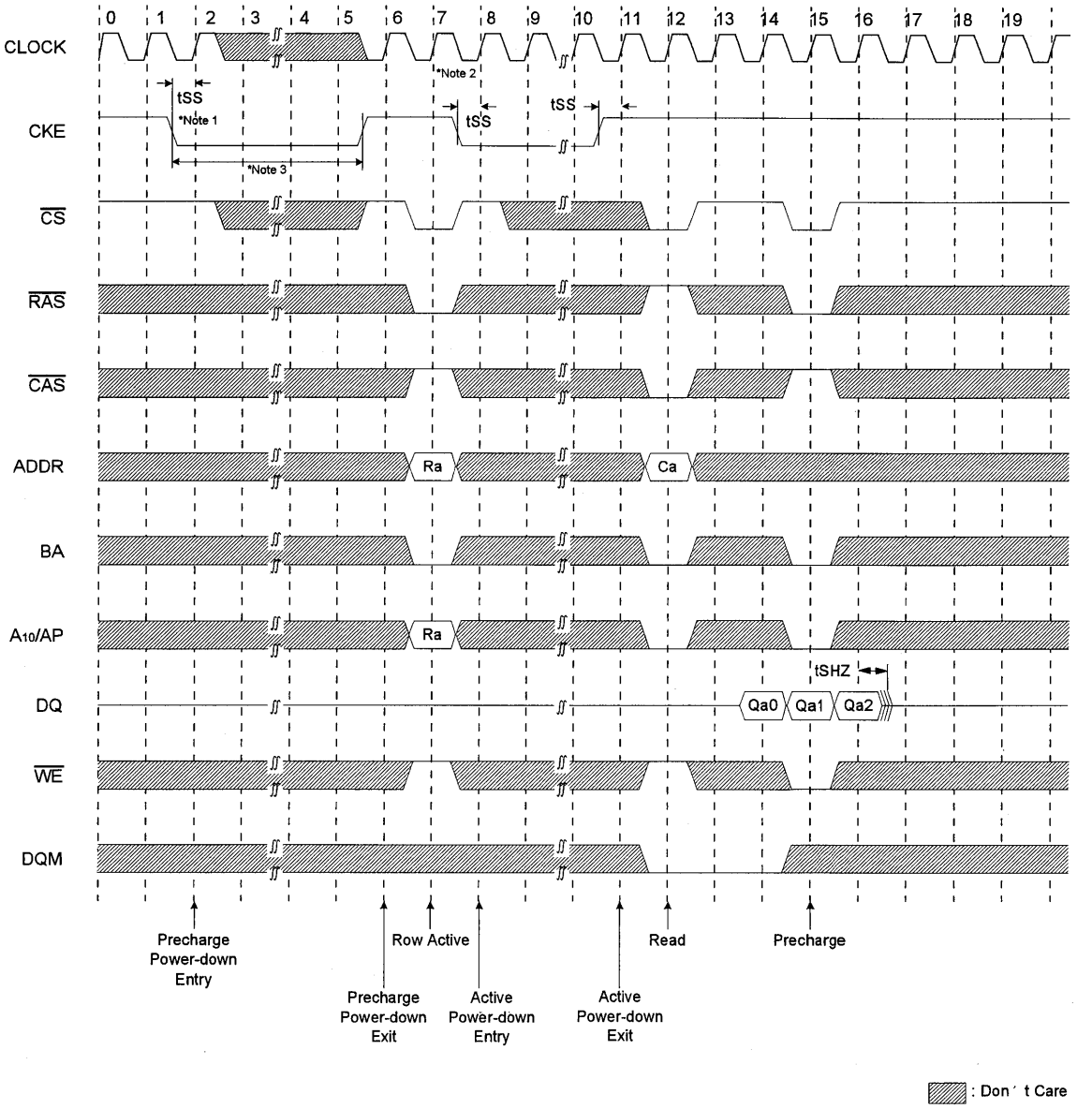
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



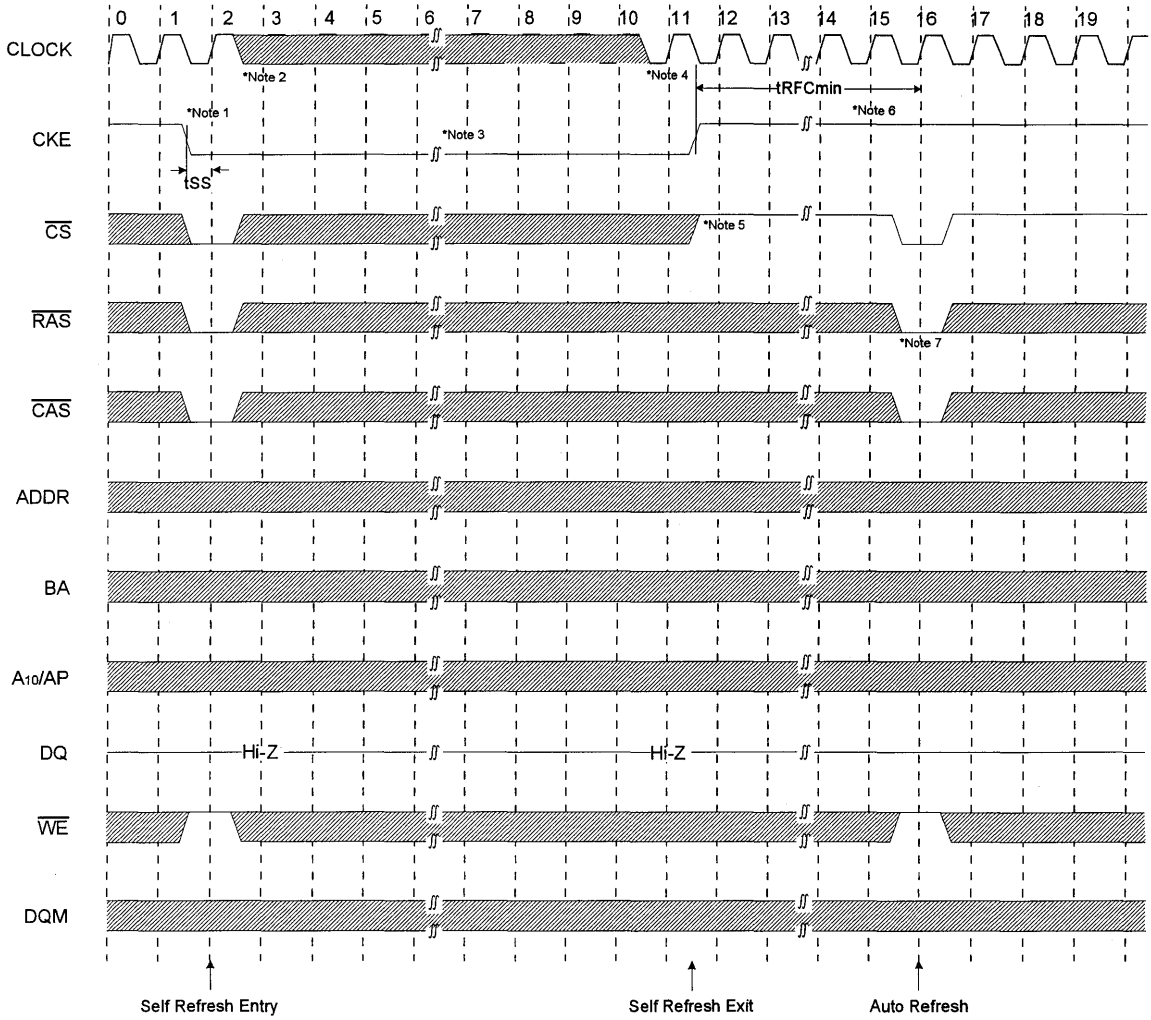
***Note :** 1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regaredless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



*Note :
1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



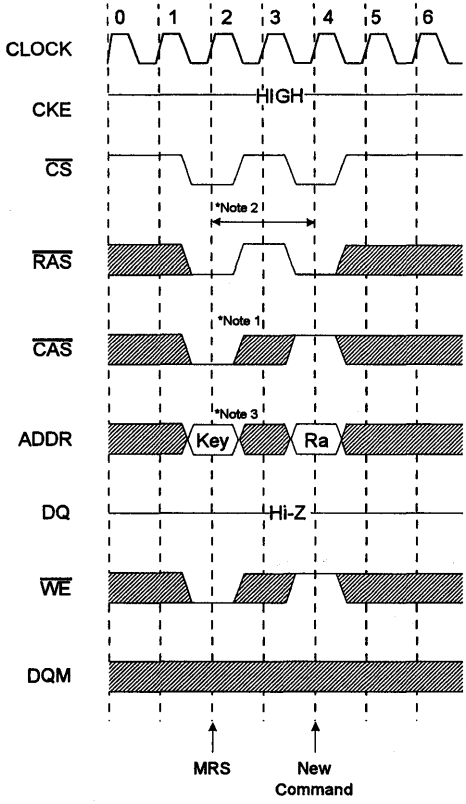
***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

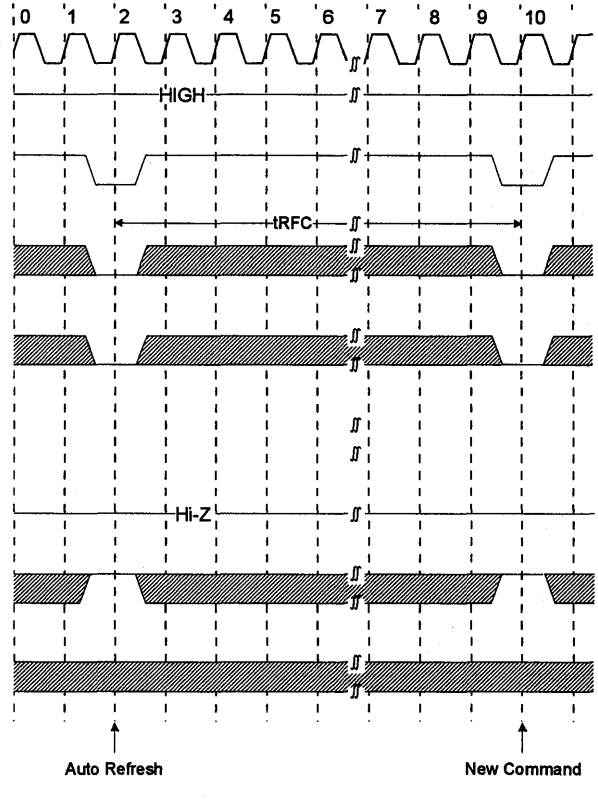
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

* Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

64M 4Banks SDRAM (A-die)

- DATA SHEETS
- DEVICE OPERATIONS-III
- TIMING DIAGRAM-III

DATA SHEETS

4M x 4Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

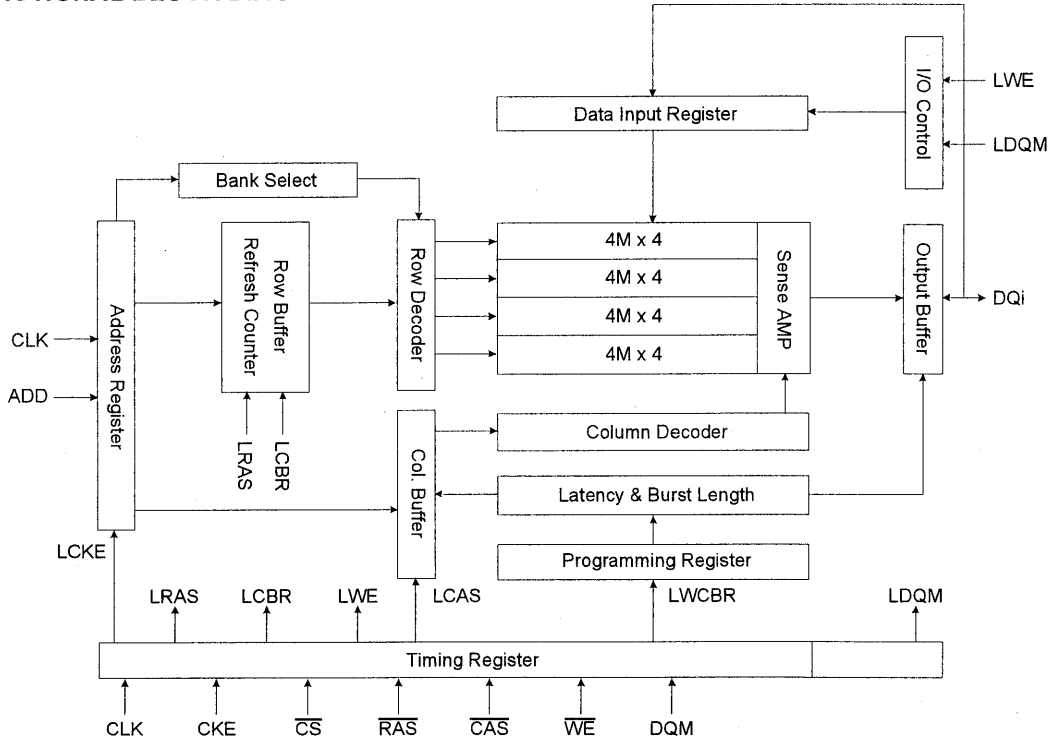
GENERAL DESCRIPTION

The KM44S16030A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 4,194,304 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

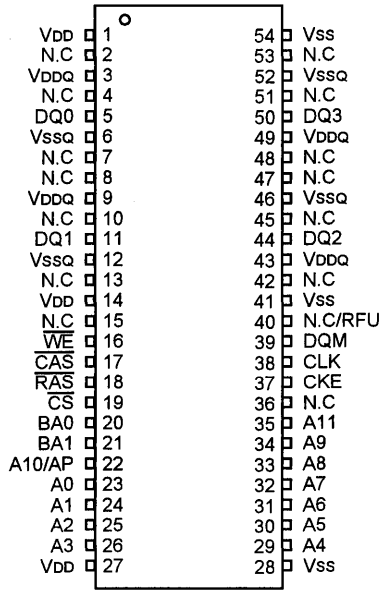
Part NO.	MAX Freq.	Interface	Package
KM44S16030AT-G/F8	125MHz	LVTTL	54 TSOP(II)
KM44S16030AT-G/F10	100MHz		
KM44S16030AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, column address : CA_0 ~ CA_9
BA_0 ~ BA_1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
DQ_0 ~ 3	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_3)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

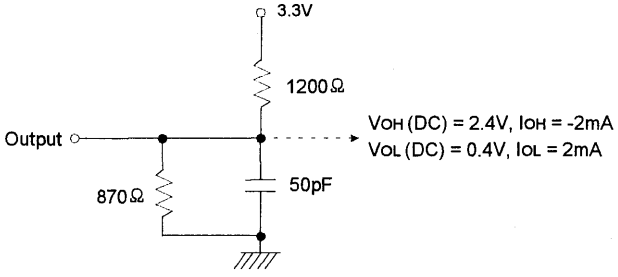
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		125	110	95	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		45			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		30			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	175	140	120	mA	1
			2	120	110	95		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		3			mA	3
				500			uA	4

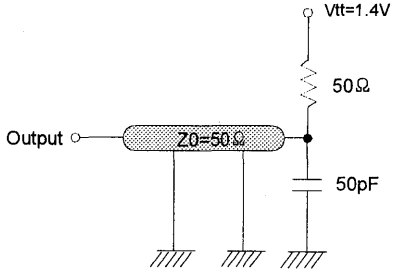
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM44S16030AT-G**
4. KM44S16030AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM44S16030AT-8

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM44S16030AT-10

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM44S16030AT-12

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry											
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

2M x 8Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
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KM48S8030AT-G/F12	83MHz		

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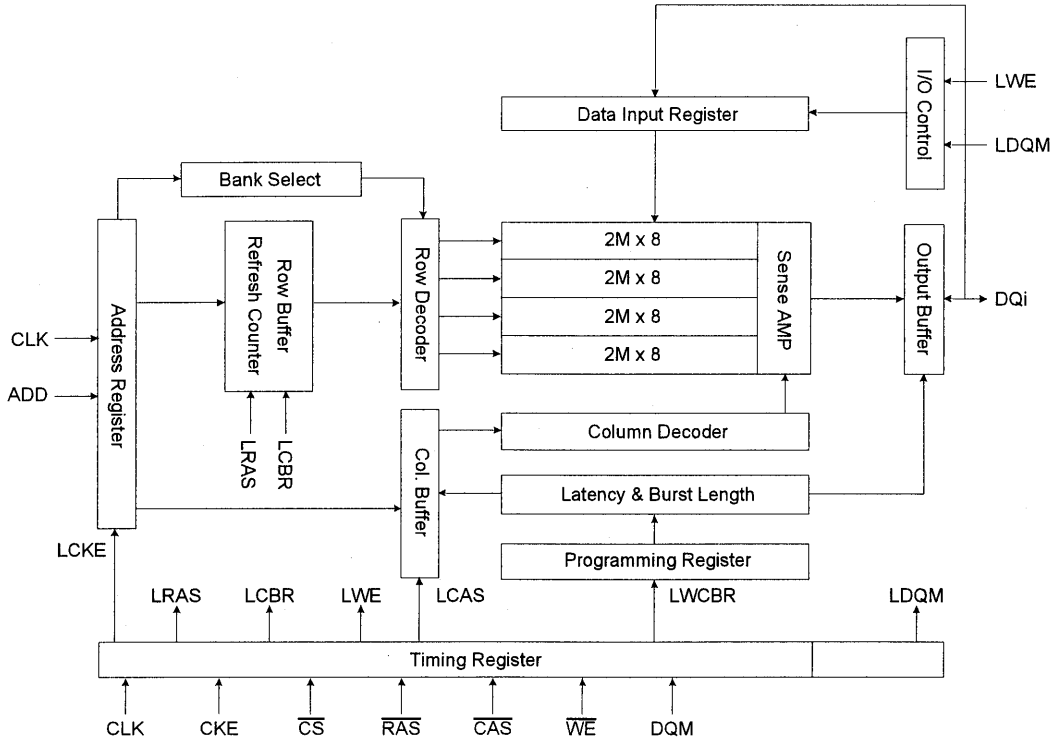

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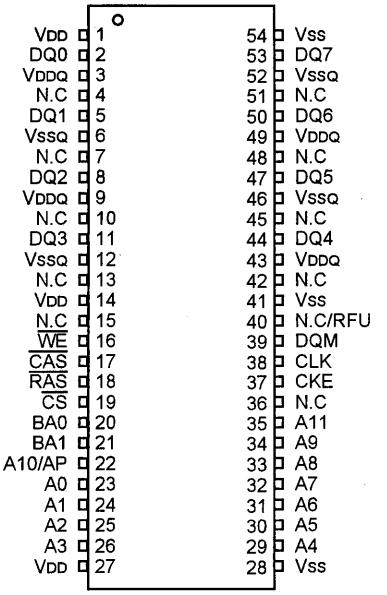
PIN CONFIGURATION (TOP VIEW)



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A_0 ~ A_{11}	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, column address : CA_0 ~ CA_8
BA_0 ~ BA_1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active.
DQ_0 ~ 7	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_7)	C_{OUT}	2	5	pF

DC CHARACTERISTICS

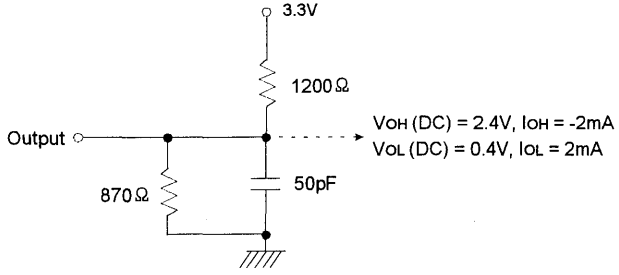
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		130	115	95	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		45			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		30			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	185	150	125	mA	1
			2	125	115	100		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		3			mA	3
				500			uA	4

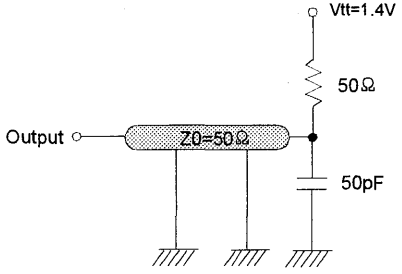
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM48S8030AT-G**
4. KM48S8030AT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM48S8030AT-8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM48S8030AT-10 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM48S8030AT-12 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

1M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

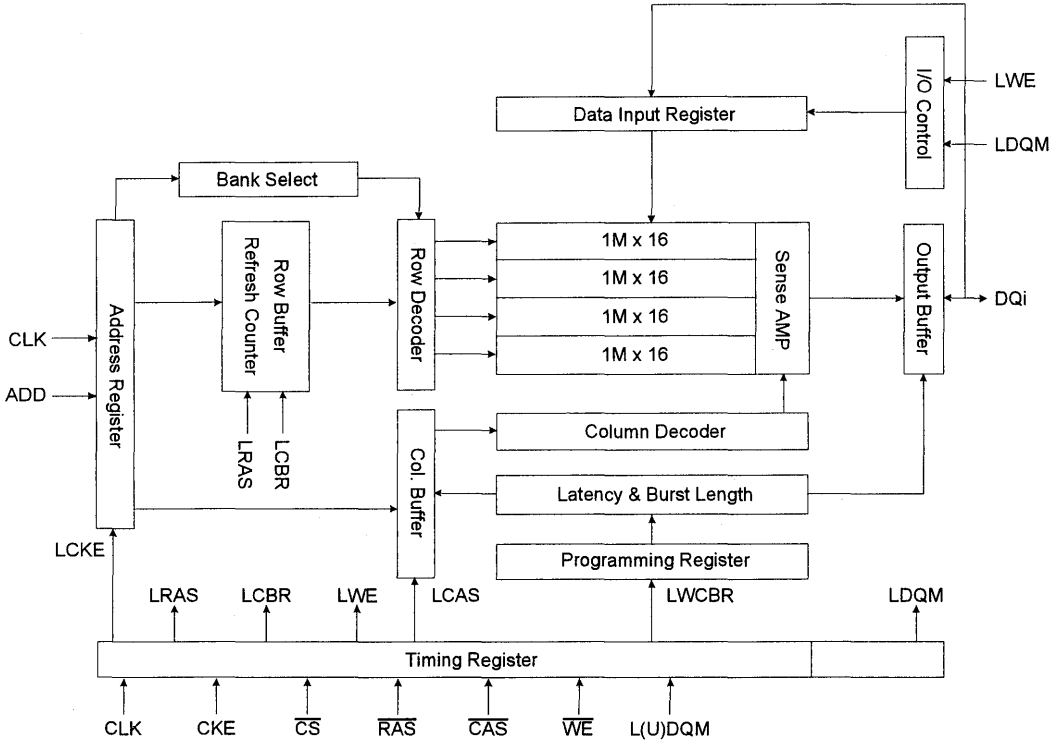
GENERAL DESCRIPTION

The KM416S4030A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

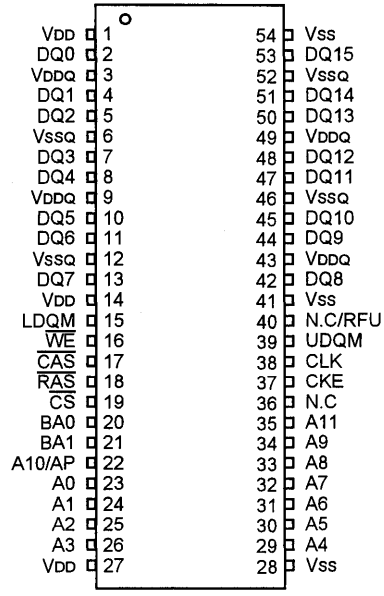
Part NO.	MAX Freq.	Interface	Package
KM416S4030AT-G/F8	125MHz	LVTTL	54 TSOP(II)
KM416S4030AT-G/F10	100MHz		
KM416S4030AT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

PIN CONFIGURATION (TOP VIEW)



54PIN TSOP (II)
(400mil x 875mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
$A_0 \sim A_{11}$	*Address*	Row / column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{11}$, column address : $CA_0 \sim CA_7$
$BA_0 \sim BA_1$	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA_0 ~ BA_1)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	2	5	pF

DC CHARACTERISTICS

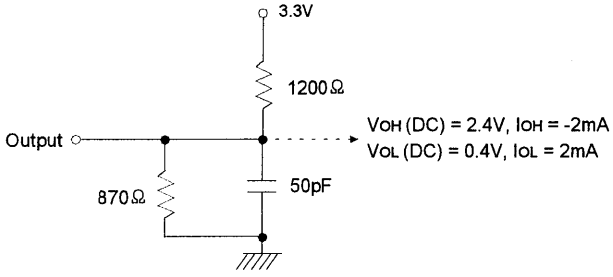
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		140	125	105	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		50			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		35			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	200	165	135	mA	1
			2	140	130	115		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		210			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		3			mA	3
				500			uA	4

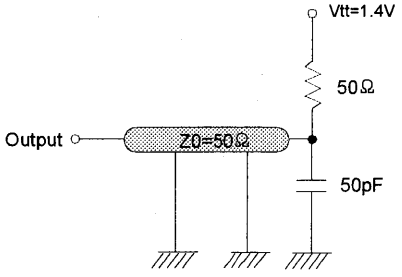
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM416S4030AT-G**
4. KM416S4030AT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM416S4030AT-8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM416S4030AT-10 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM416S4030AT-12 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9~A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don' t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

DEVICE OPERATIONS-III

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA0 ~ BA1	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : x4 (1024), x8 (512), x16 (256)

POWER UP SEQUENCE

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	0	1	2	3	0	1	0	3	2
1	1	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of set-up and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE (CKE)

The clock enable(CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + tss" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (BA0 ~ BA1)

: In case x 4

This SDRAM is organized as four independent banks of 4,194,304 words x 4 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 8

This SDRAM is organized as four independent banks of 2,097,152 words x 8 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

: In case x 16

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The BA_0 ~ BA_1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The bank addresses BA_0 ~ BA_1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0 ~ A11)

: In case x 4

The 22 address bits are required to decode the 4,194,304 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 10 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 8

The 21 address bits are required to decode the 2,097,152 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 9 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

: In case x 16

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A_0 ~ A_{11}). The 12 bit row addresses are latched along with $\overline{RAS}$ and BA_0 ~ BA_1 during bank activate command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA_0 ~ BA_1 during read or write command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, the SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

DEVICE OPERATIONS (Continued)

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A_0 ~ A_{11} and BA_0 ~ BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A_0 ~ A_2, burst type uses A_3, CAS latency (read latency from column address) use A_4 ~ A_6, vendor specific options or test mode use A_7 ~ A_8, A_{10}/AP ~ A_{11} and BA_0 ~ BA_1. The write burst length is programmed using A_9. A_7 ~ A_8, A_{10}/AP ~ A_{11} and BA_0 ~ BA_1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD}(min) from the time of bank activation. t_{RCD} is an internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD}(min) with cycle time of the clock and then rounding off the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD}(min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS}(min). Every SDRAM bank activate command must satisfy t_{RAS}(min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS}(max). The number of cycles for both t_{RAS}(min) and t_{RAS}(max) can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least t_{RCD}(min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of the burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DEVICE OPERATIONS (Continued)

DQM OPERATION

The DQM is used to mask input and output operations. It works similar to $\overline{OE}$ during read operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is not required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge operation is performed on an active bank by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A_{10}/AP with valid $BA_0 \sim BA_1$ of the bank to be procharged. The precharge command can be asserted anytime after t_{RAS}(min) is satisfied from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing t_{RP} with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by t_{RAS}(max). Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to Power down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy t_{RAS}(min) and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst read or burst write by asserting high on A_{10}/AP. If burst read or burst write by asserting high on A_{10}/AP, the bank is left active until a new command is asserted. Once auto precahrge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A_{10}/AP after all banks have satisfied t_{RAS}(min) requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by t_{RFC}(min). The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. All banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or a burst of 4096 auto refresh cycles once in 64ms.

SELF REFRESH

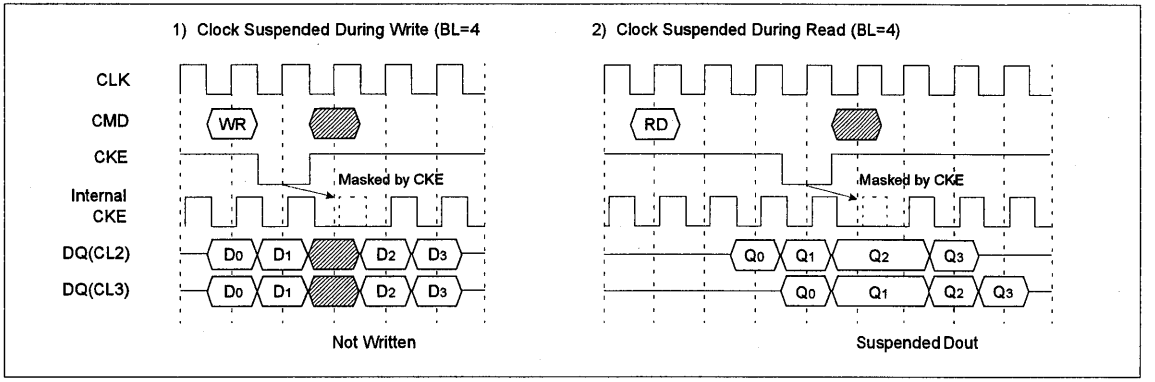
The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the self refresh.

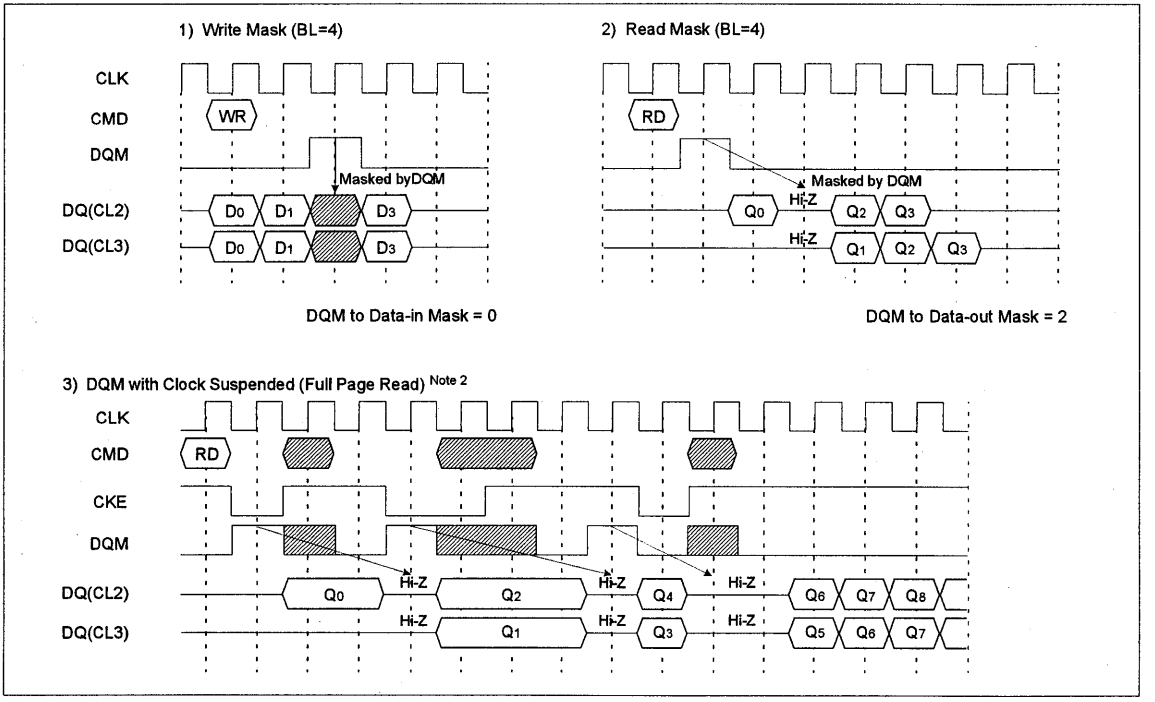
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

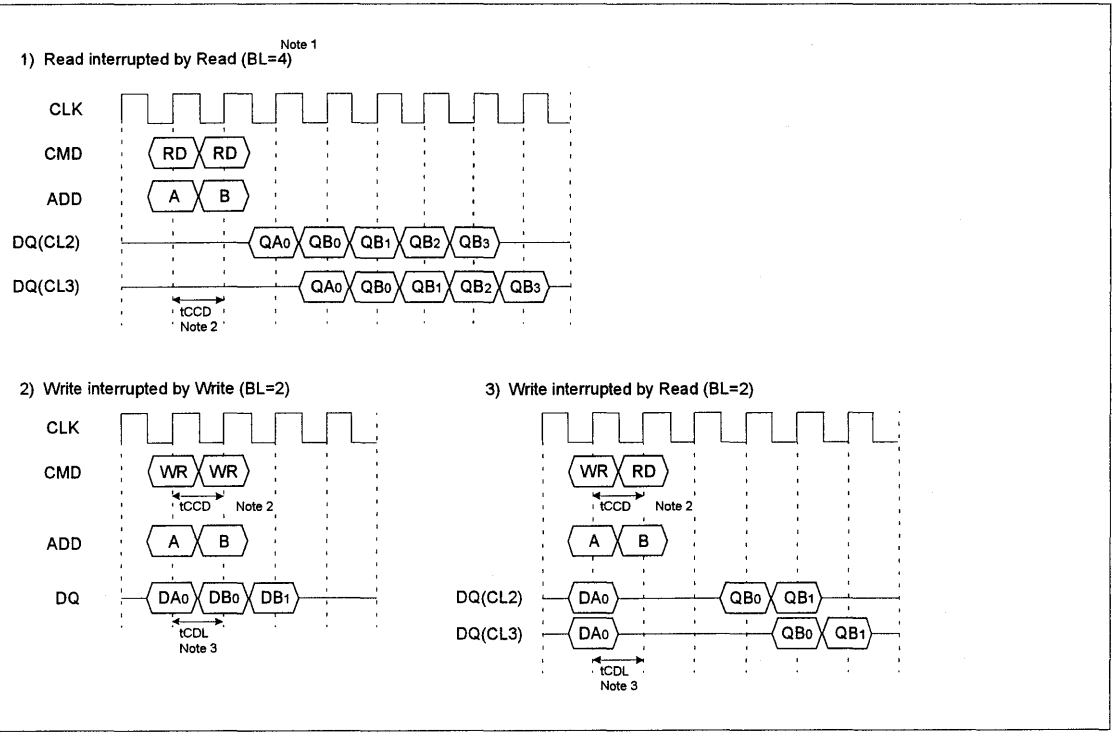


2. DQM Operation



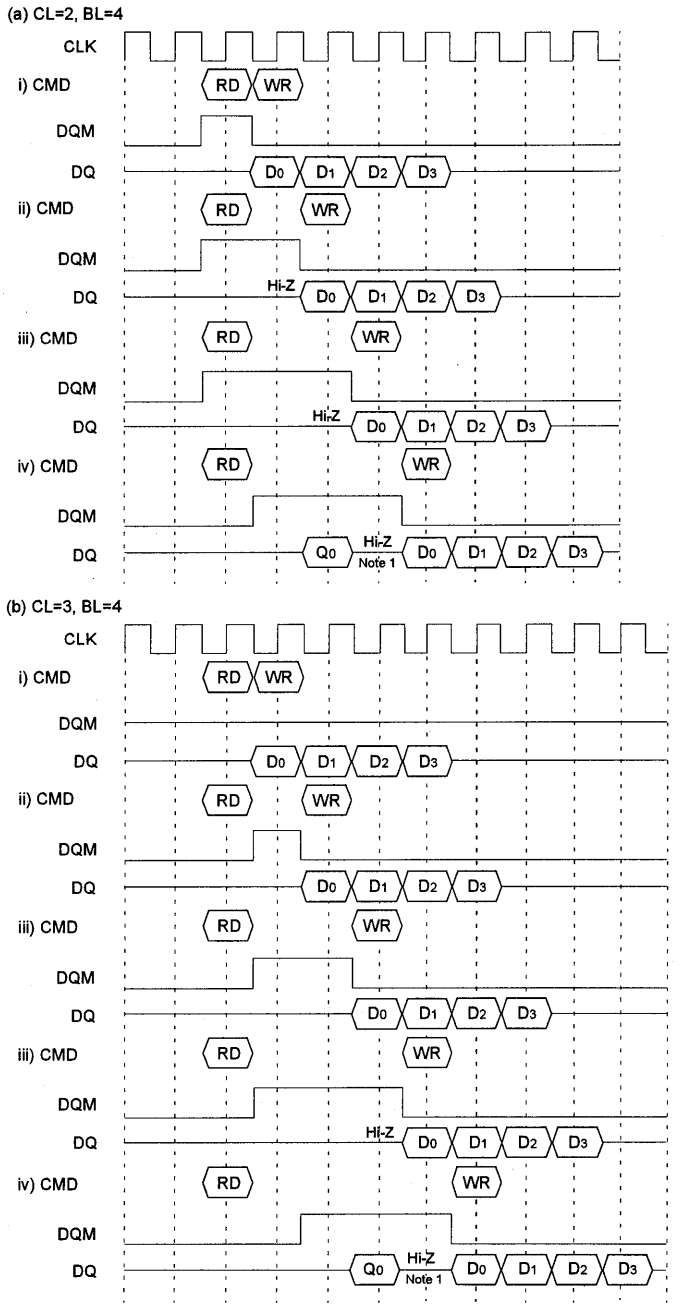
*Note : 1. CKE to CLK disable/enable = 1CLK.
2. DQM makes data out Hi-Z after 2CLKs which should masked by CKE " L"
3. DQM masks both data-in and data-out.

3. $\overline{CAS}$ Interrupt (I)



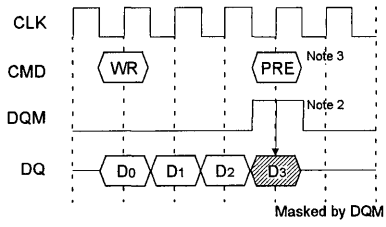
*Note : 1. By " Interrupt", It is meant to stop burst read/write by external command before the end of burst.
By "$\overline{CAS}$ Interrupt", to stop burst read/write by $\overline{CAS}$ access ; read and write.
2. t_{CCD} : $\overline{CAS}$ to $\overline{CAS}$ delay. (=1CLK)
3. t_{CDL} : Last data in to new column address delay. (=1CLK)

4. $\overline{CAS}$ Interrupt (II) : Read Interrupted by Write & DQM



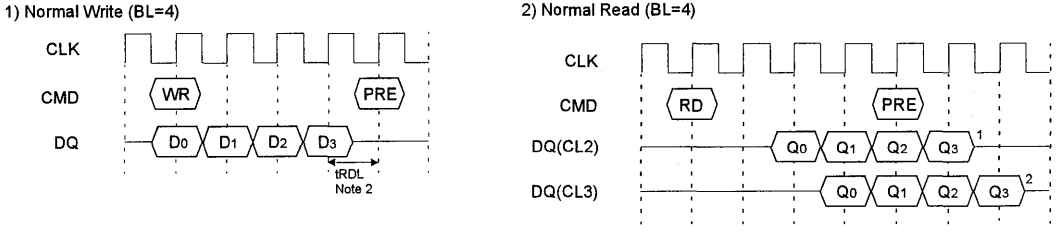
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

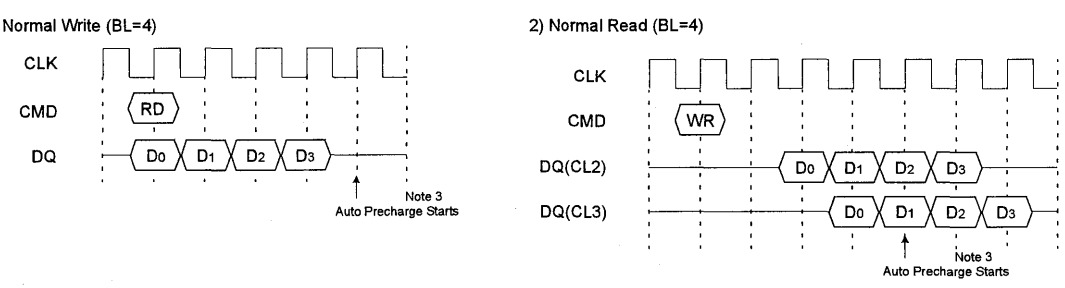


*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge

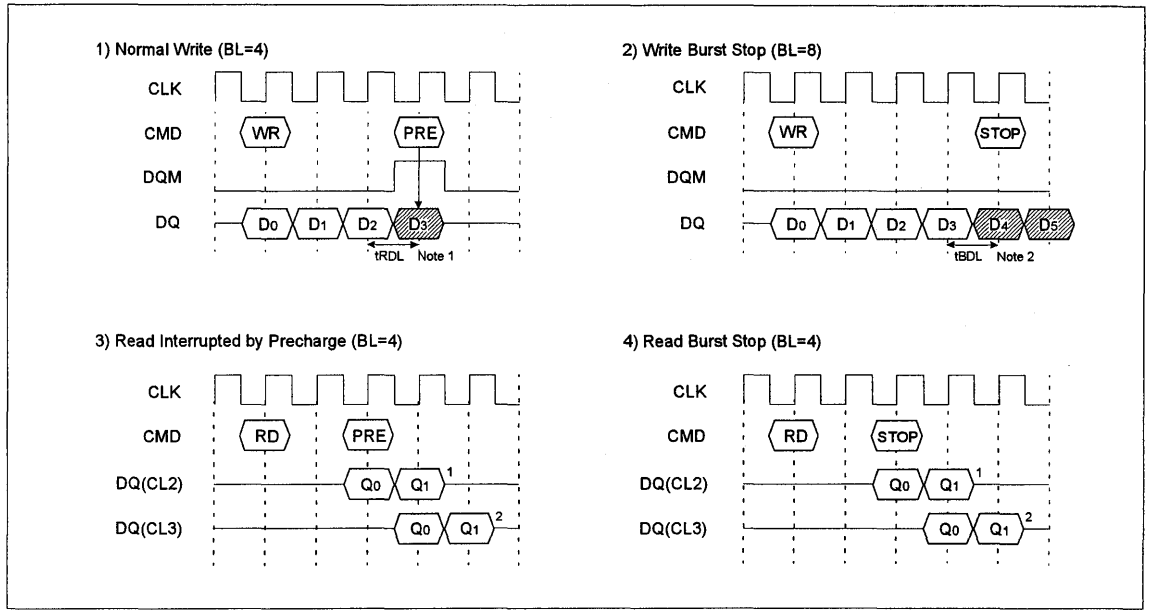


7. Auto Precharge

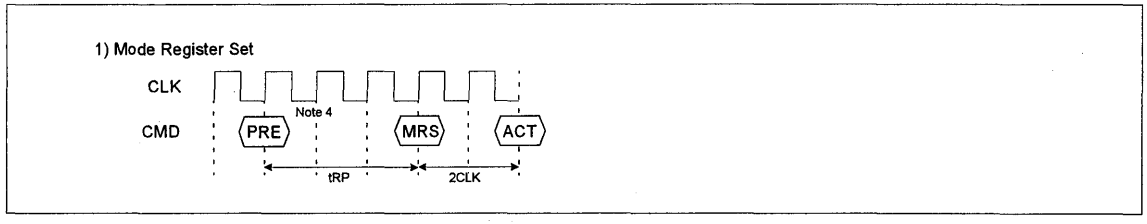


*Note : 1. tRDL : Last data in to row precharge delay
2. Number of valid output data after row precharge : 1, 2 for CAS Latency = 2, 3 respectively.
3. The row active command of the precharge bank can be issued after tRP from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

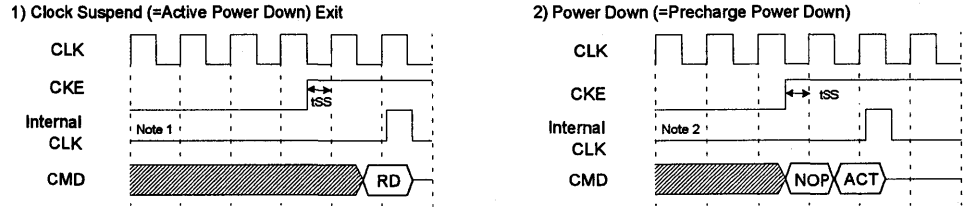


9. MRS

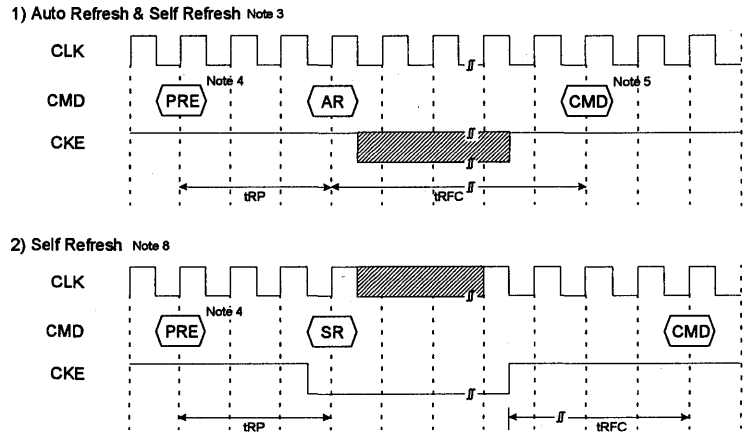


***Note :** 1. t_{RDL} : 1 CLK
2. t_{BDL} : 1 CLK ; Last data in to burst stop delay.
Read or write burst stop command is valid at every burst length.
3. Number of valid output data after row precharge or burst stop : 1, 2 for CAS latency= 2, 3 respectiviely.
4. PRE : All banks precharge if necessary.
MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



***Note :** 1. Active power down : one or more banks active state.
2. Precharge power down : all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
No precharge commands are required after auto refresh command.
During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refreh mode, refresh interval and refresh operation are perfomed internally.
After self refresh entry, self refresh mode is kept while CKE is low.
During self refresh mode, all inputs expect CKE will be don't cared, and outputs will be in Hi-Z state.
For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted.
Before/After self refresh mode, burst auto refresh cycle (4096 cycles) is recommended.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A_3 = "0". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A_3 = "1". See the BURST SEQUENCE TABLE. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Random MODE	Random column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS $A_{2,1,0}$ = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS $A_{2,1,0}$ = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS $A_{2,1,0}$ = "010".
	8	At MRS $A_{2,1,0}$ = "011".
	Full Page	At MRS $A_{2,1,0}$ = "111". At the end of the burst length, burst will be stop automatically.
Special MODE	BRSW	At MRS A_9 = "1". Read burst =1, 2, 4, 8, full page write Burst =1 At auto precharge of write, t_{RAS} should not be violated.
Random MODE	Burst Stop	t_{BDL}= 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{RAS}$ Interrupt (Interrupted by Precharge)	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL}= 1 with DQM, valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (& Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Row Active)	
	L	H	H	L	X	X	Term burst --> Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	H	X	X	NOP (Continue Burst to End --> Precharge)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Pre-charging	H	X	X	X	X	X	NOP --> Idle after tRP	
	L	H	H	H	X	X	NOP --> Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP --> Idle after tRPL	4

FUNCTION TRUTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Row Activating	L	L	L	X	X	X	ILLEGAL	
	H	X	X	X	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	H	X	X	NOP --> Row Active after t_{RCD}	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A_{10}/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	H	X	X	X	NOP --> Idle after t_{RFC}	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP --> Idle after 2 clocks	
	L	H	H	H	X	X	NOP --> Idle after 2 clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

***Note :** 1. All entries assume the CKE was active (High) during the precharge clcok and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and A_{10}/AP).
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (TABLE 2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RFC} (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Power Down --> ABI	
	L	H	L	H	H	H	X	Exit Power Down --> ABI	7
	L	H	L	H	H	L	X	ILLEGAL	7
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table 1	
	H	L	H	X	X	X	X	Enter Power Down	
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	8
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clcok Suspend	

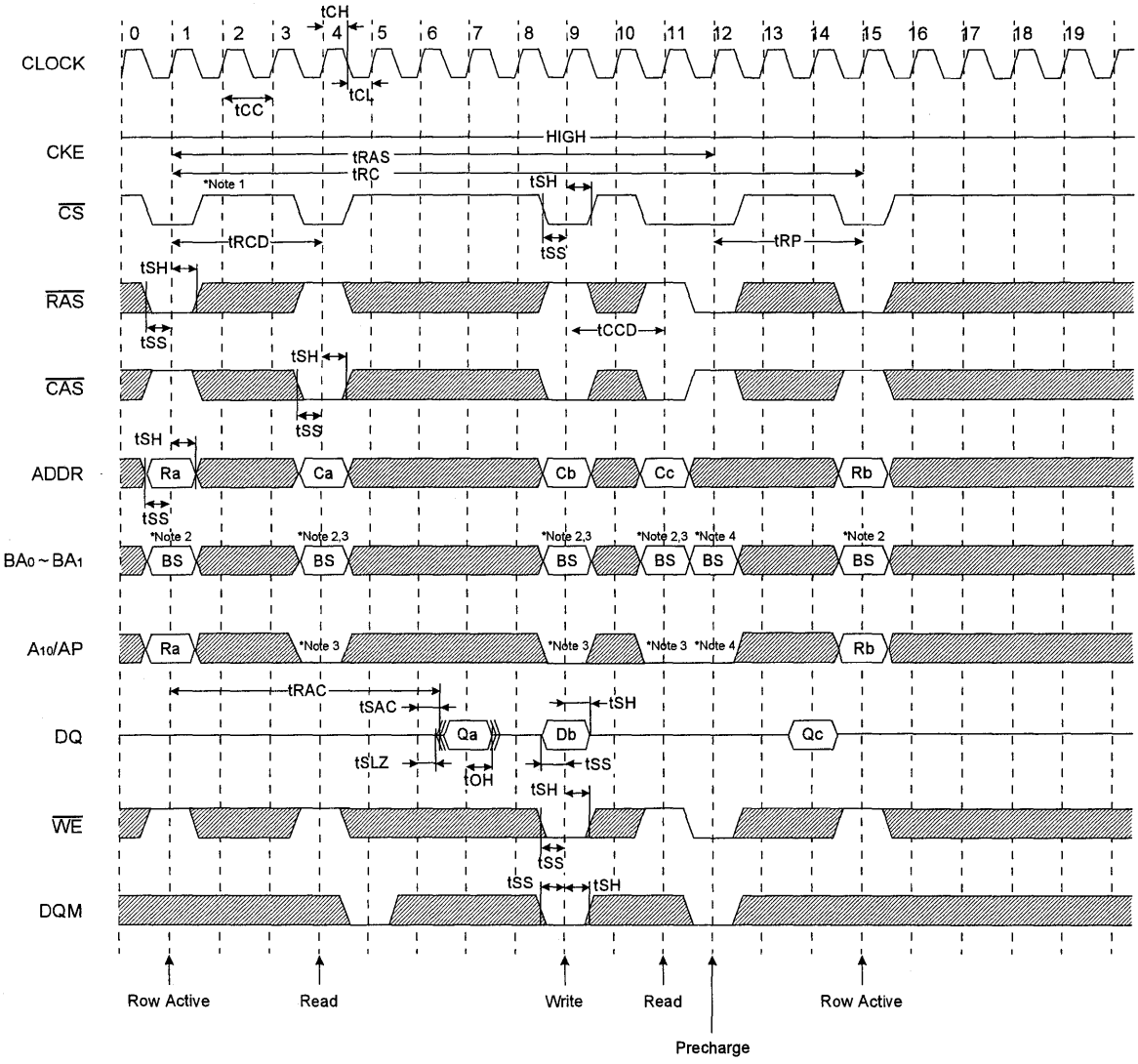
Abbreviations : ABI = All Banks Idle, RA = Row Address

***Note :** 6. CKE low to high transition is asynchronous.

7. CKE low to high transition is asynchronous if restarts internal clock.
   A minimum setup time 1CLK + tss must be satisfied before any command other than exit.
8. Power down and self refresh can be entered only from the all banks idle state.
9. Must be a legal command.

TIMING DIAGRAM-III

Single Bit Read-Write-Read Cycle(Same Page) @CAS Latency=3, Burst Length=1



***Note :** 1. All input expect CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & read/write are controlled by BA0~BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

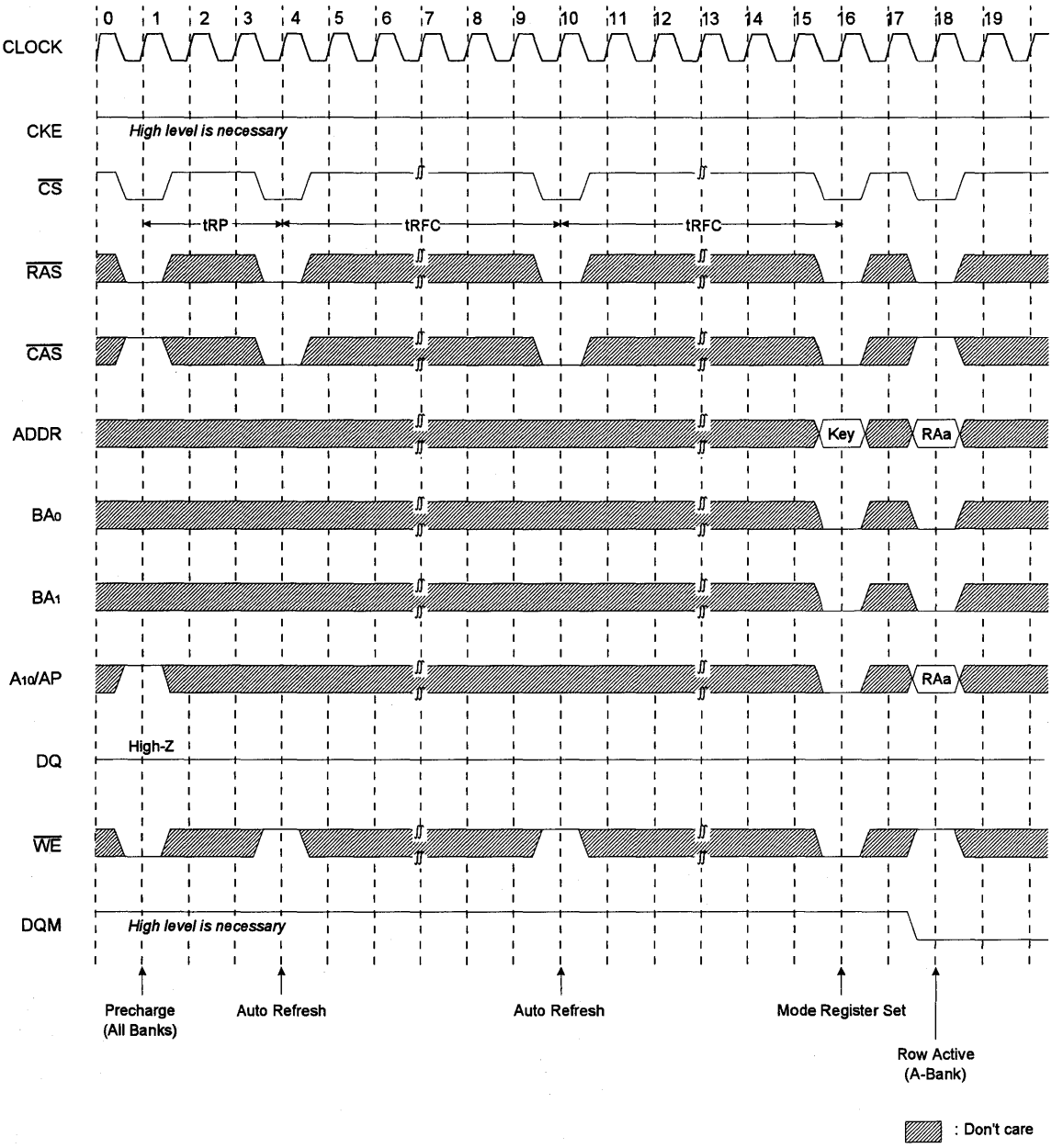
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operation
0	0	0	Disable auto precharge, leave bank A active at end of burst.
	0	1	Disable auto precharge, leave bank B active at end of burst.
	1	0	Disable auto precharge, leave bank C active at end of burst.
	1	1	Disable auto precharge, leave bank D active at end of burst.
1	0	0	Enable auto precharge, precharge bank A at end of burst.
	0	1	Enable auto precharge, precharge bank B at end of burst.
	1	0	Enable auto precharge, precharge bank C at end of burst.
	1	1	Enable auto precharge, precharge bank D at end of burst.

4. A10/AP and BA0~BA1 control bank precharge when precharge command is asserted.

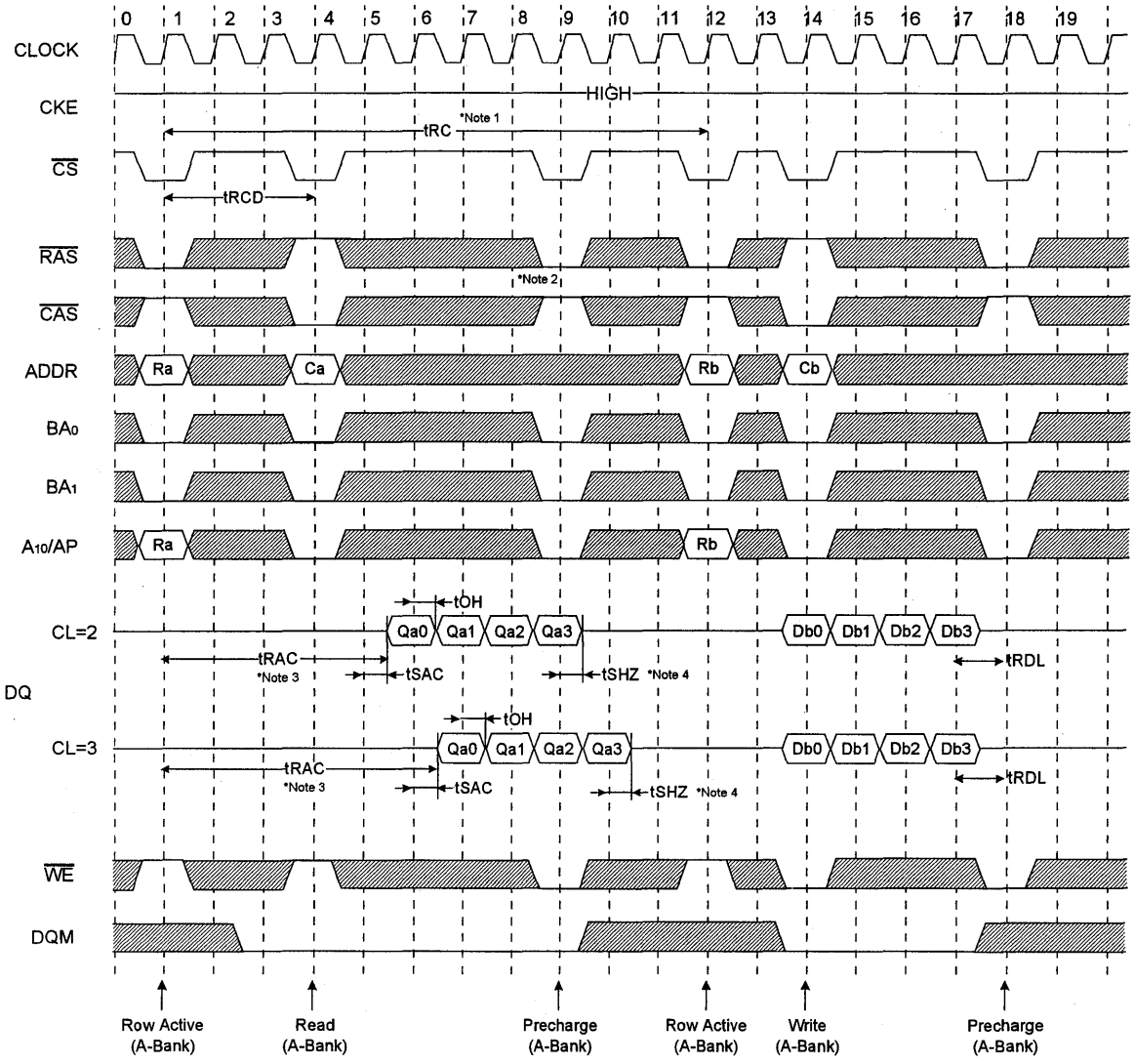
A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	0	Bank B
0	1	1	Bank C
0	1	1	Bank D
1	x	x	All Banks

Power Up Sequence



SAMSUNG ELECTRONICS

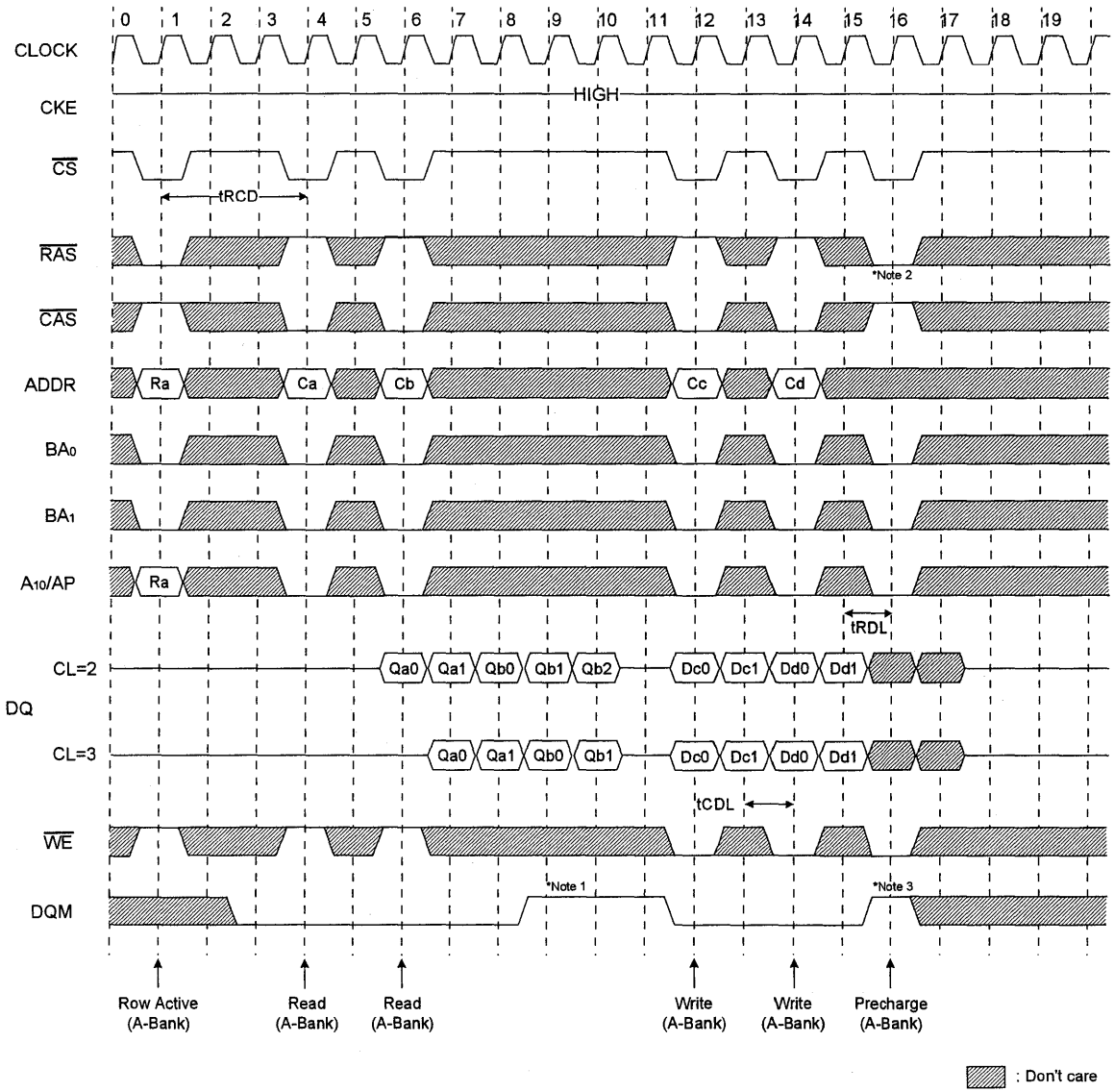
Read & Write Cycle at Same Bank @Burst Length=4



***Note :** 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clcok.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS latency - 1) + t_{SAC}
4. Ouput will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @Burst Length=4

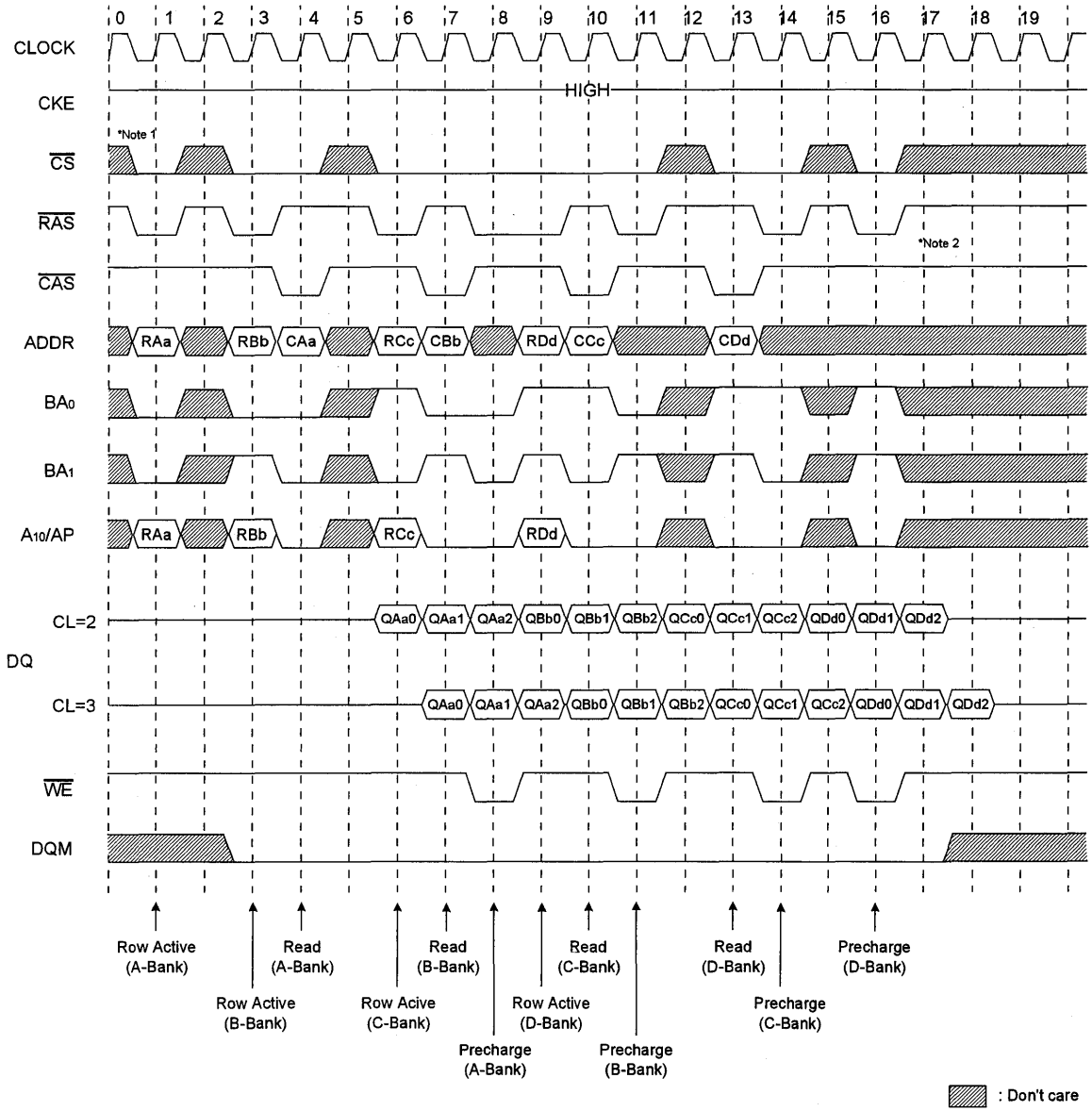


***Note :** 1. To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

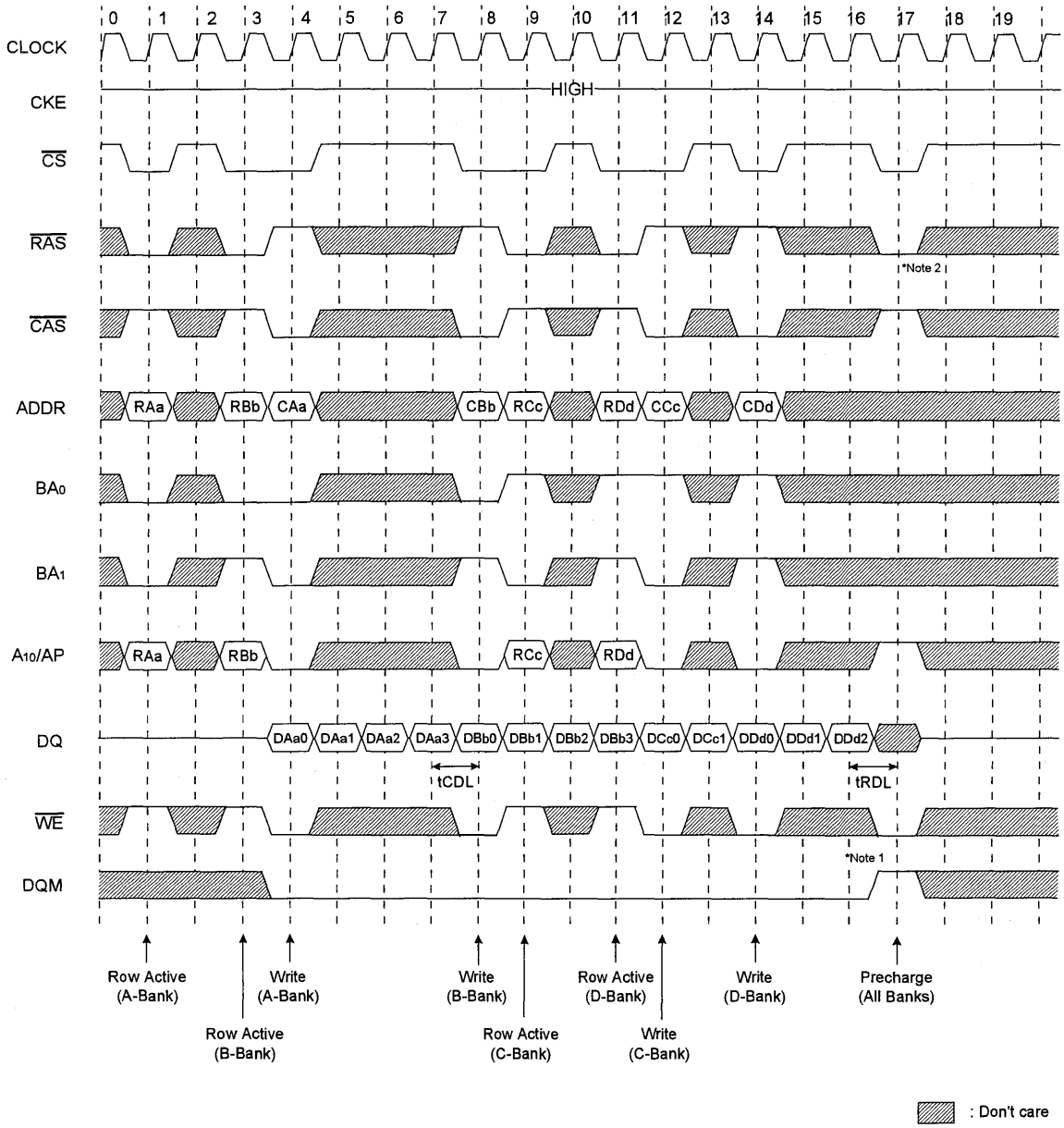
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Page Read Cycle at Different Bank @Burst Length=4



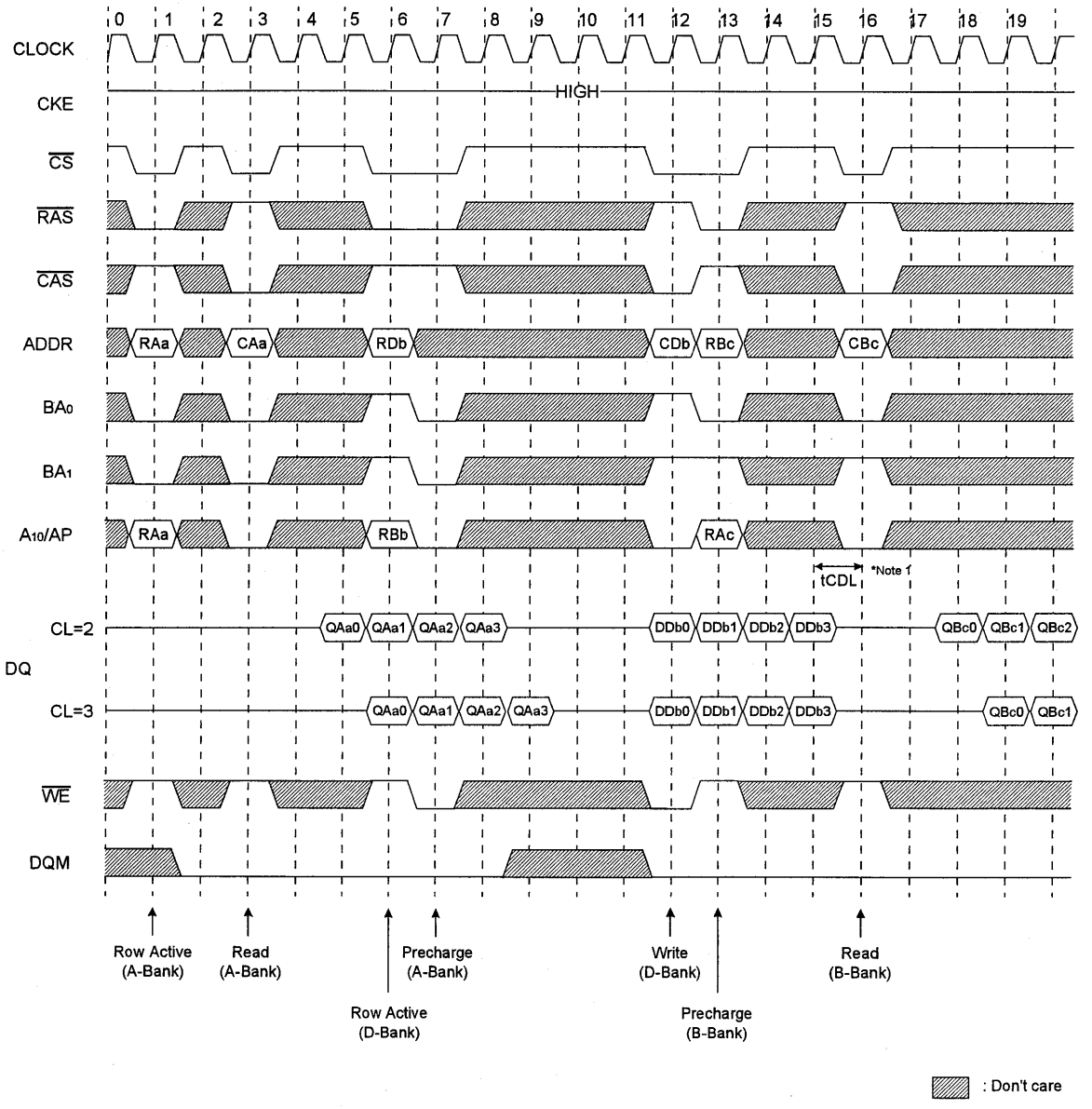
*Note : 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going dege.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @Burst Length=4



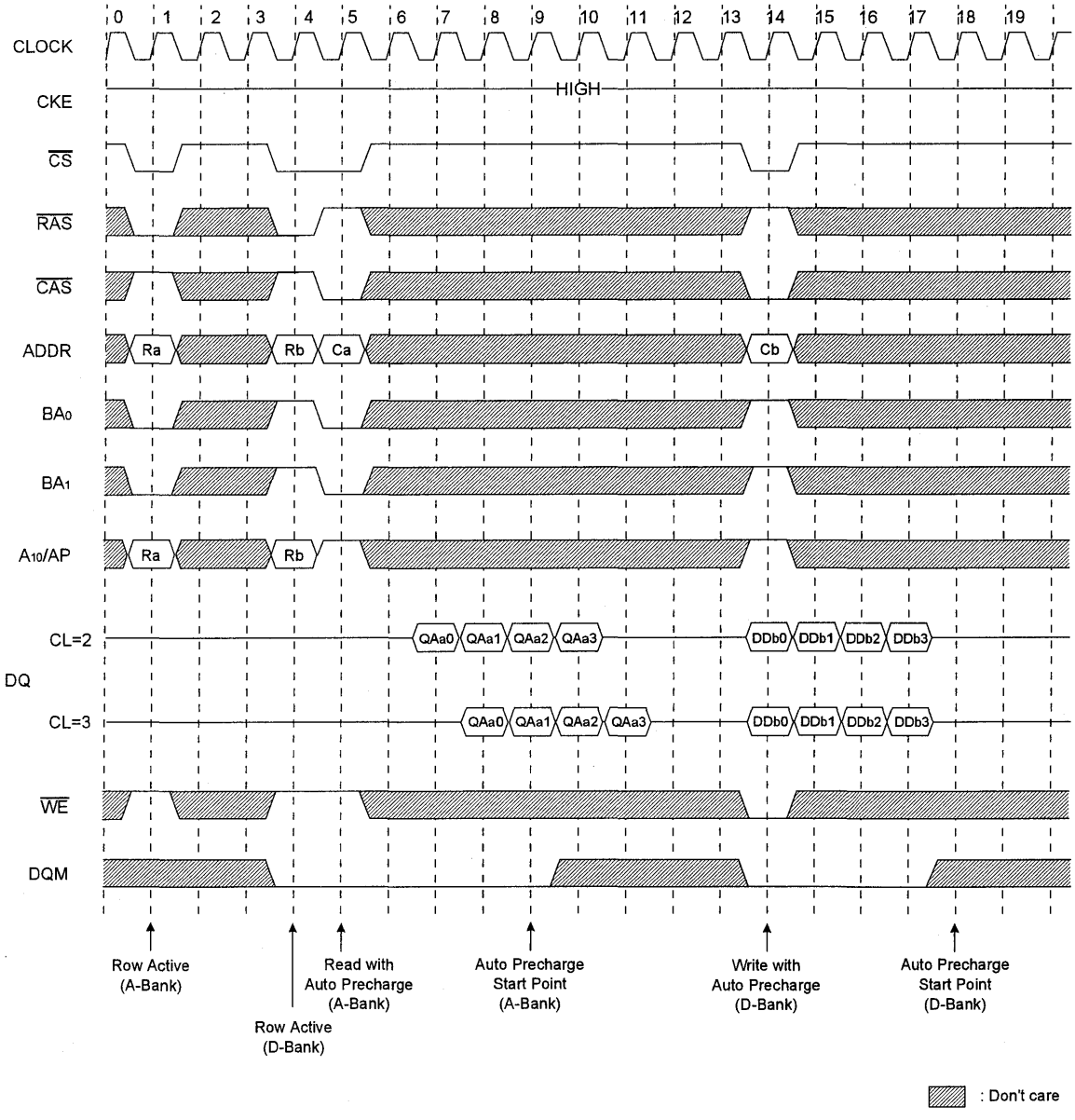
***Note :** 1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @Burst Length=4



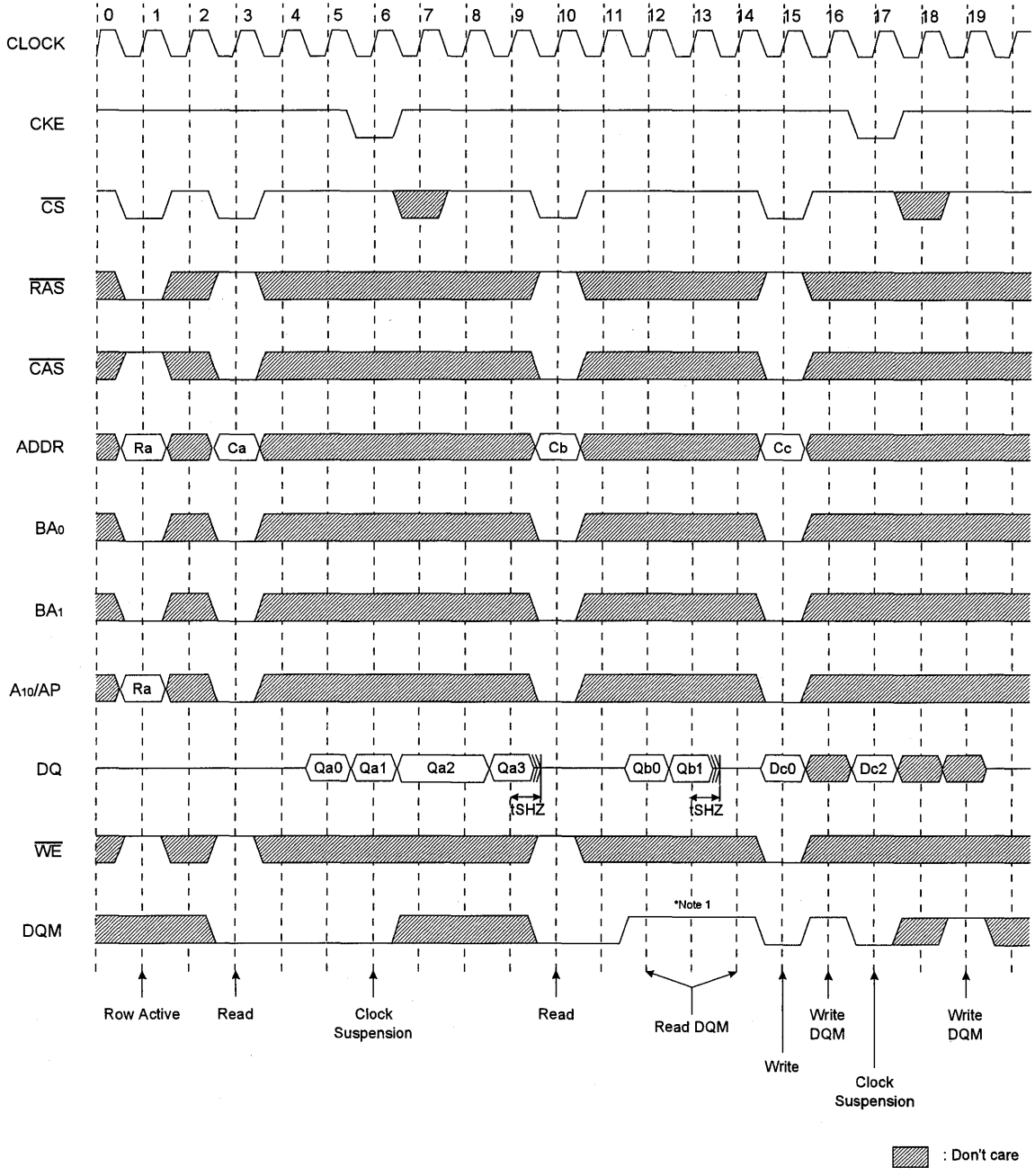
***Note :** 1. t_{CDL} should be met to complete write.

Read & Write Cycle with Auto Precharge @Burst Length=4



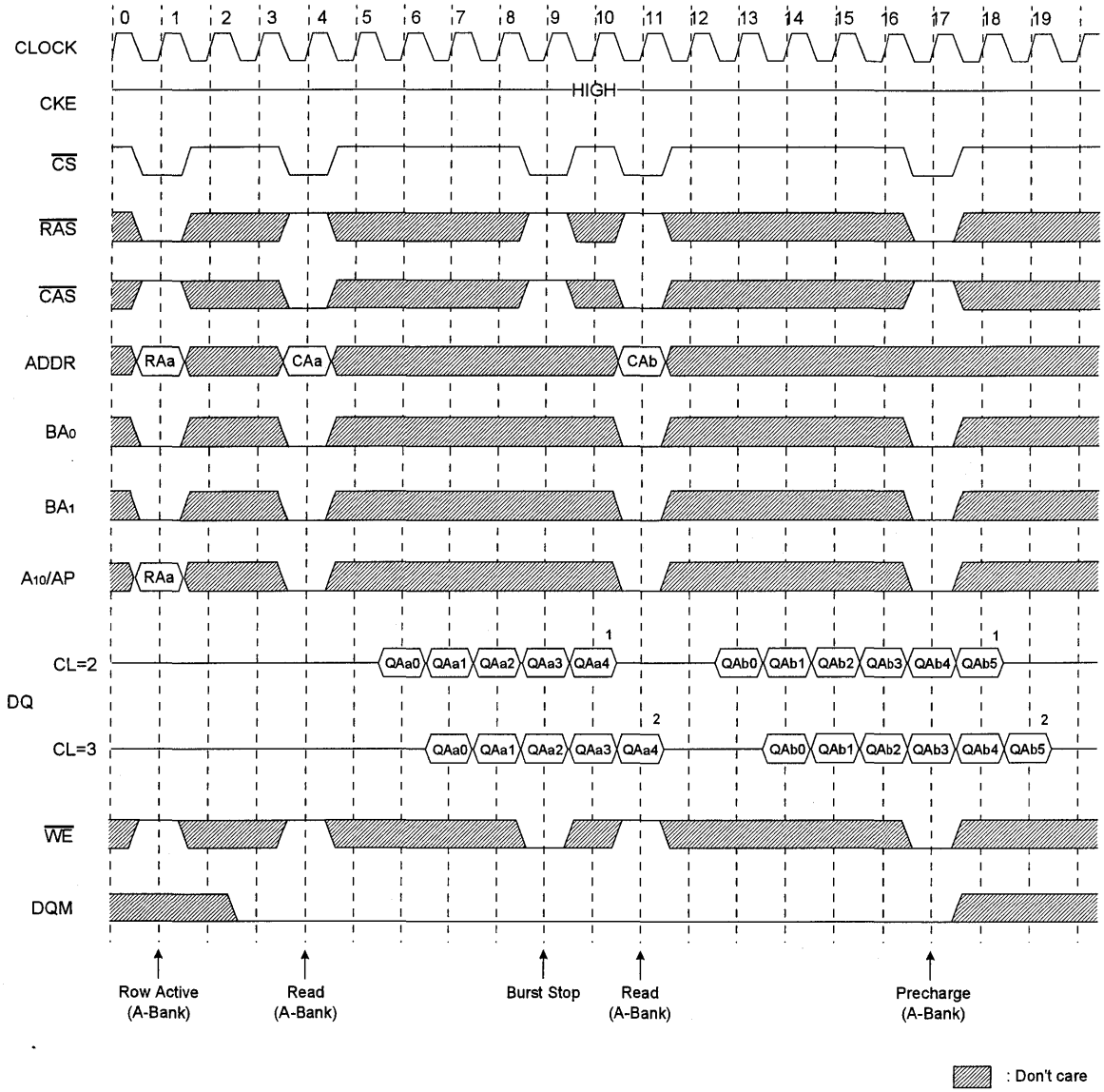
*Note : 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



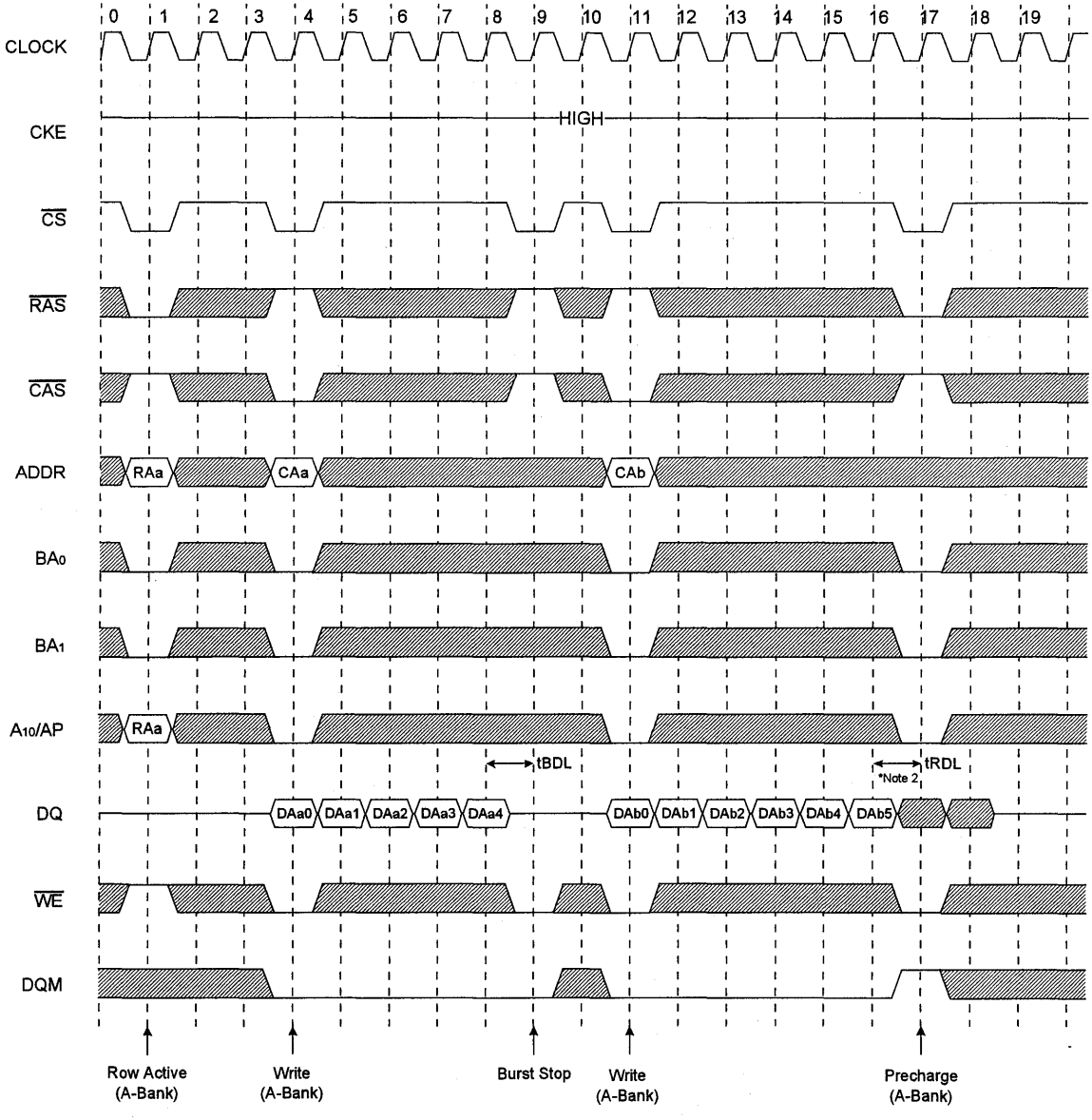
*Note : 1. DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length=Full page



***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1, 2 on them.
But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length=Full page

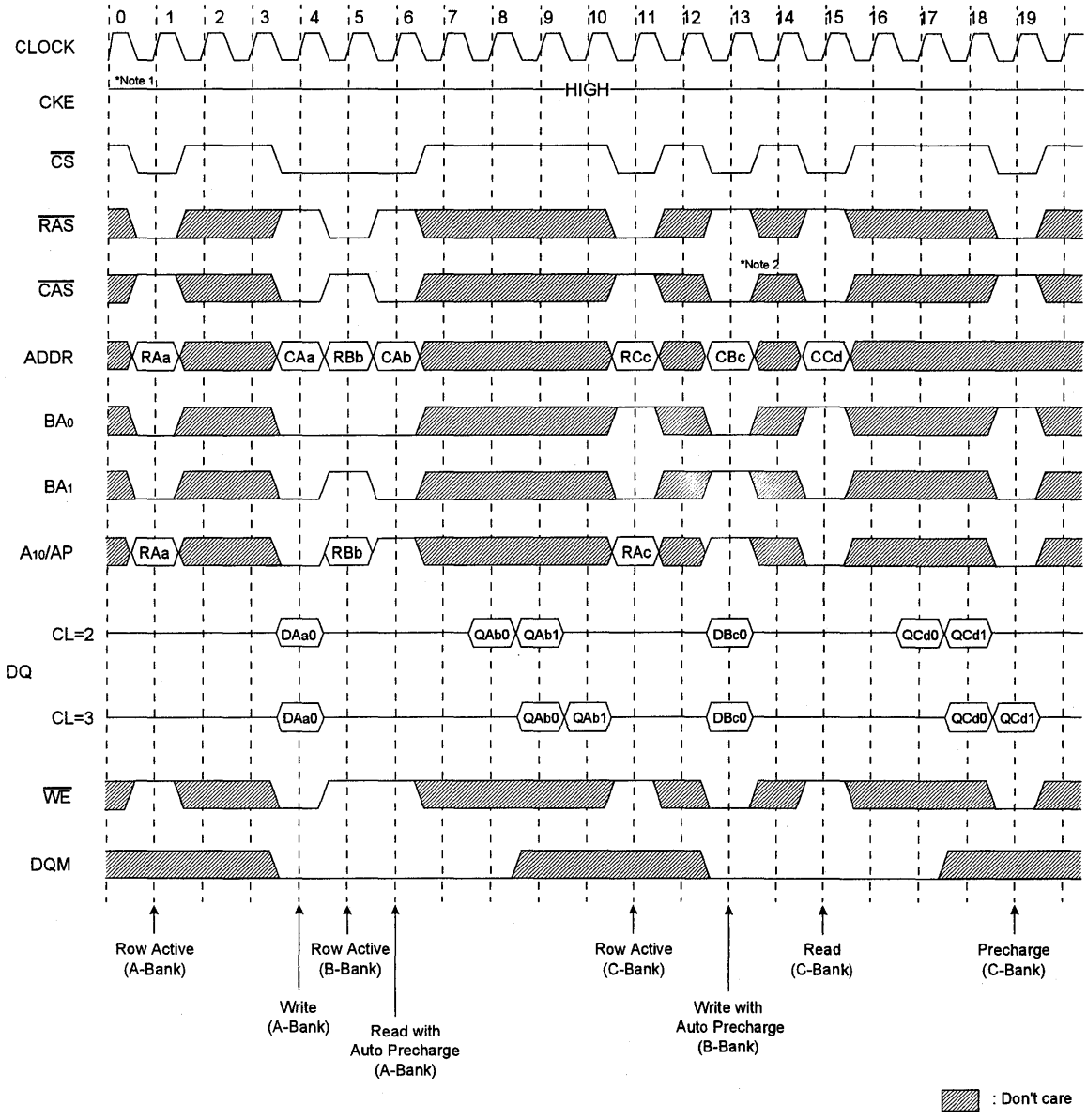


***Note :** 1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write.
   DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

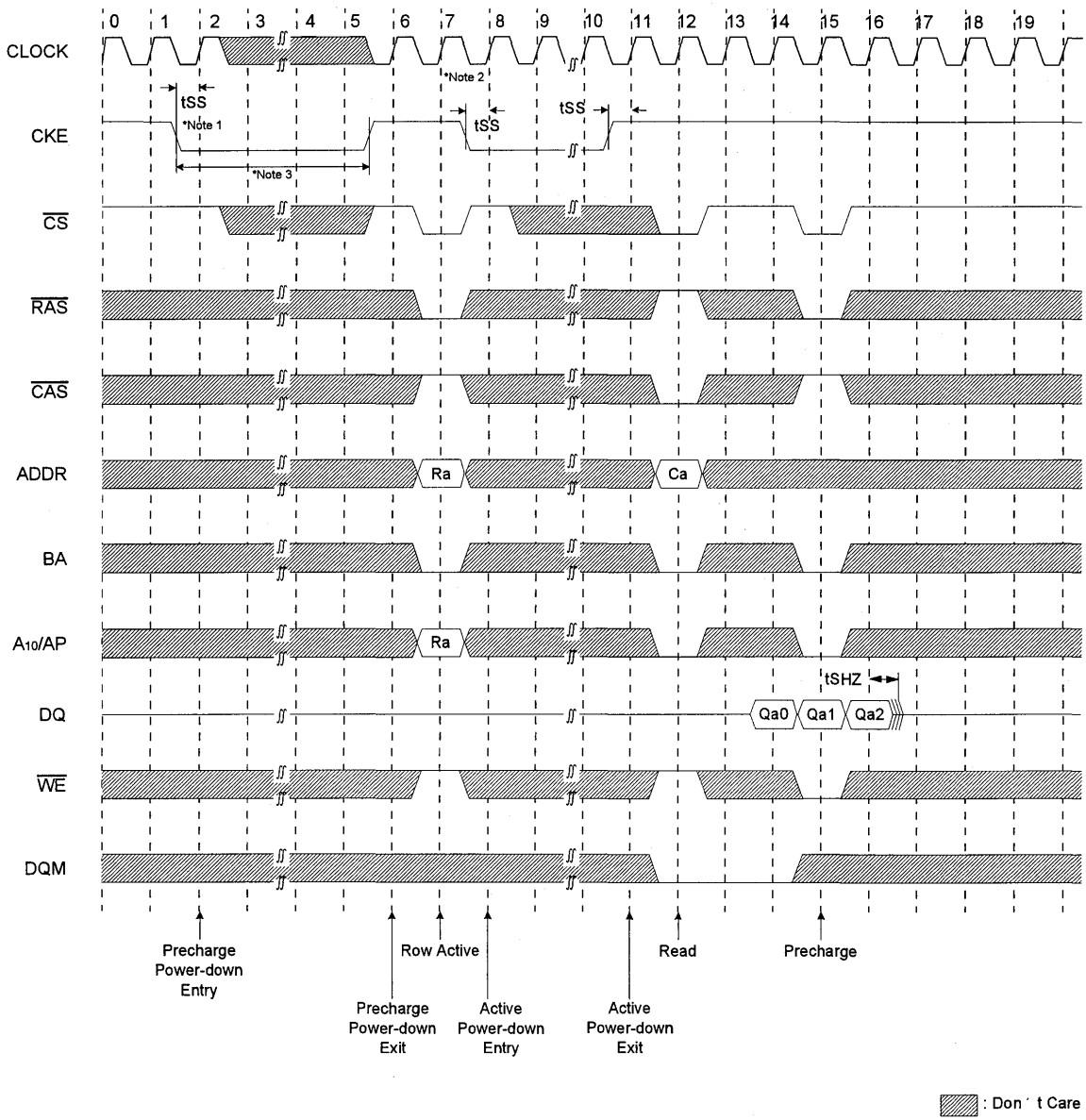
3. Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



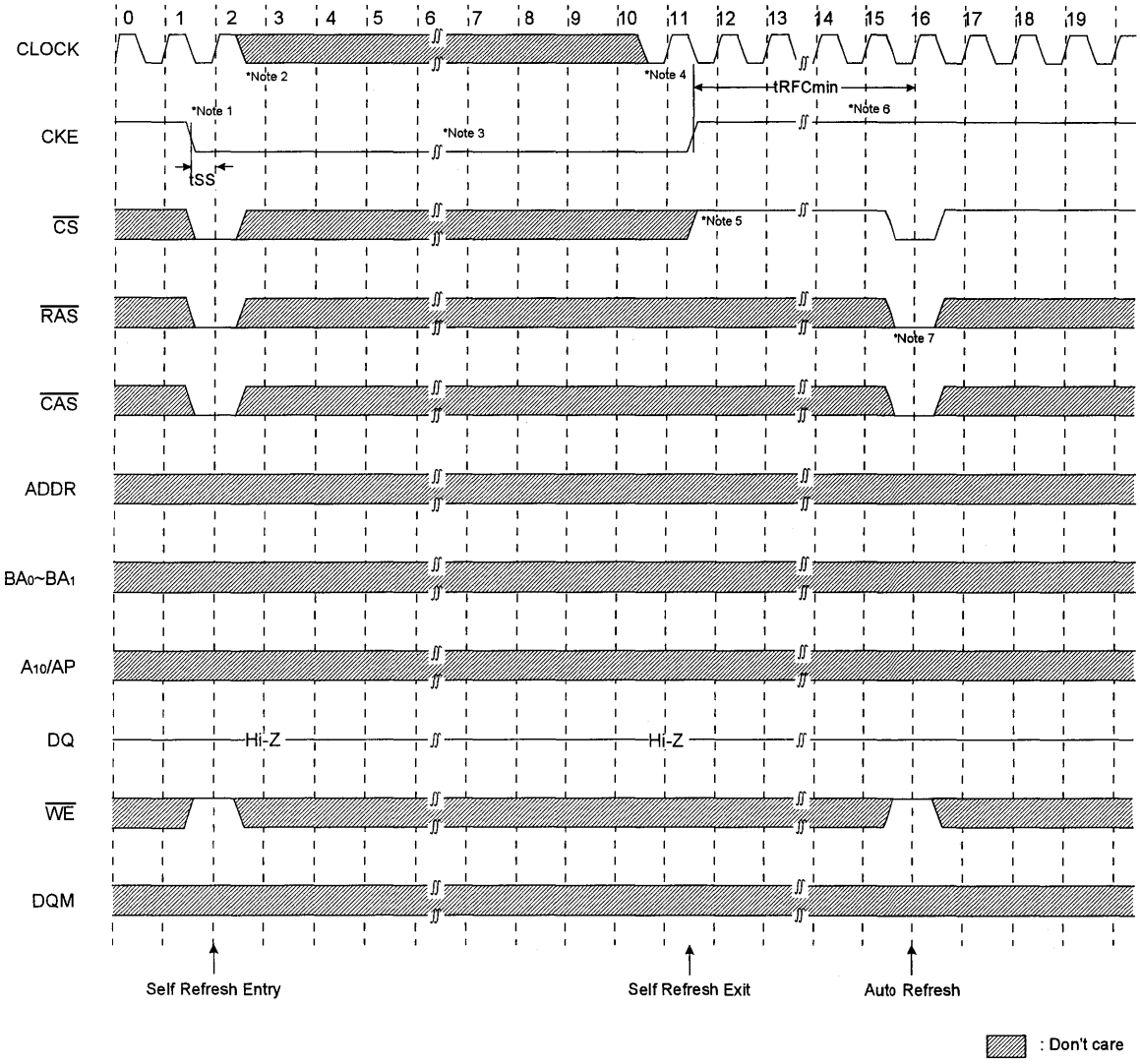
*Note : 1. BRSW modes is enabled by setting A_9 "High" at MRS (Mode Register Set).
At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.
Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command,
the next cycle starts the precharge.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4



*Note : 1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + tss prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



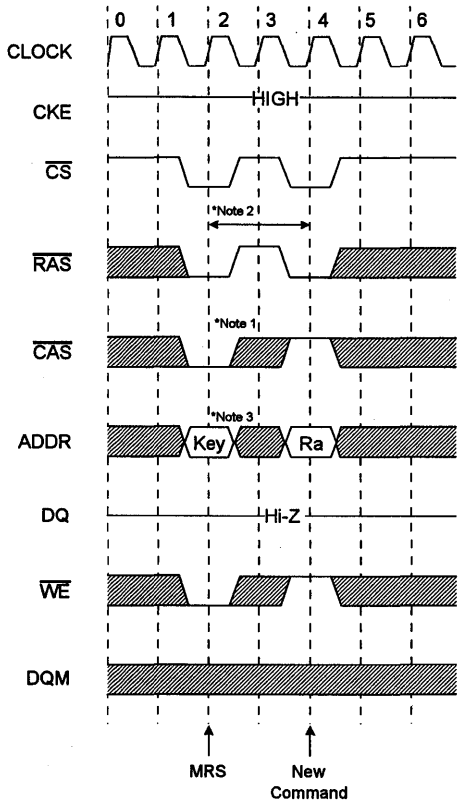
***Note : TO ENTER SELF REFRESH MODE**

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clcok cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

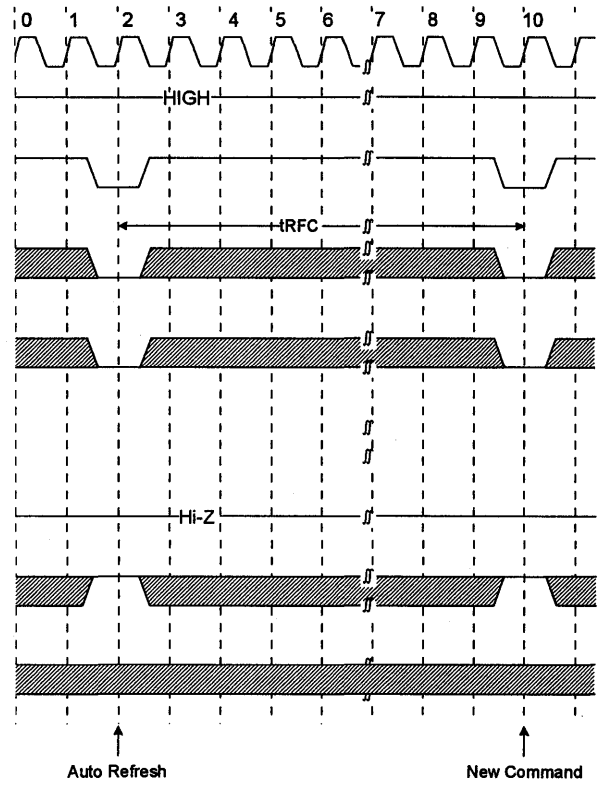
TO EXIT SELF REFRESH MODE

4. System colck restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



: Don't care

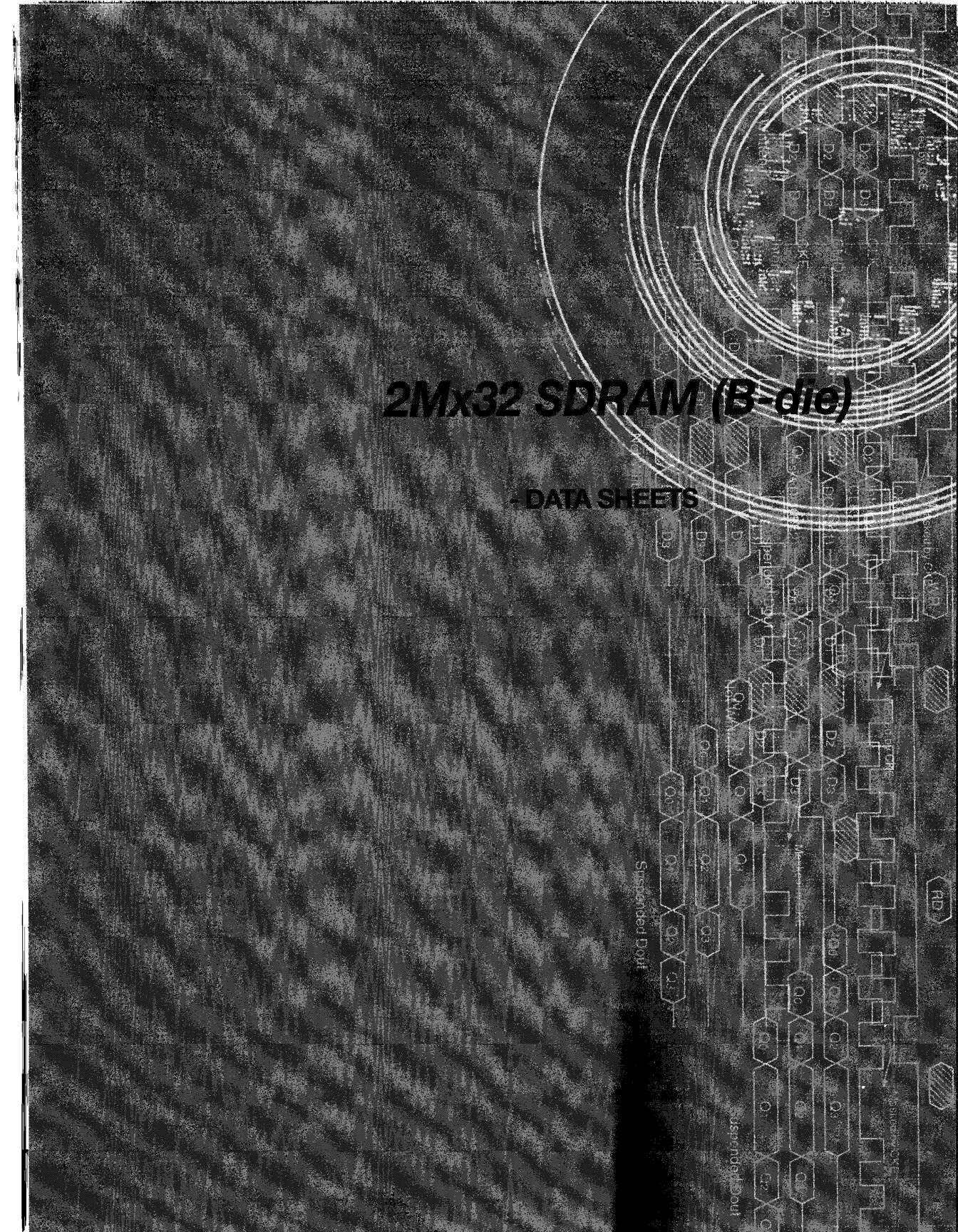
* All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

MODE REGISTER SET CYCLE

*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

2Mx32 SDRAM (B-die)

- DATA SHEETS



DATA SHEETS

1M x 32Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

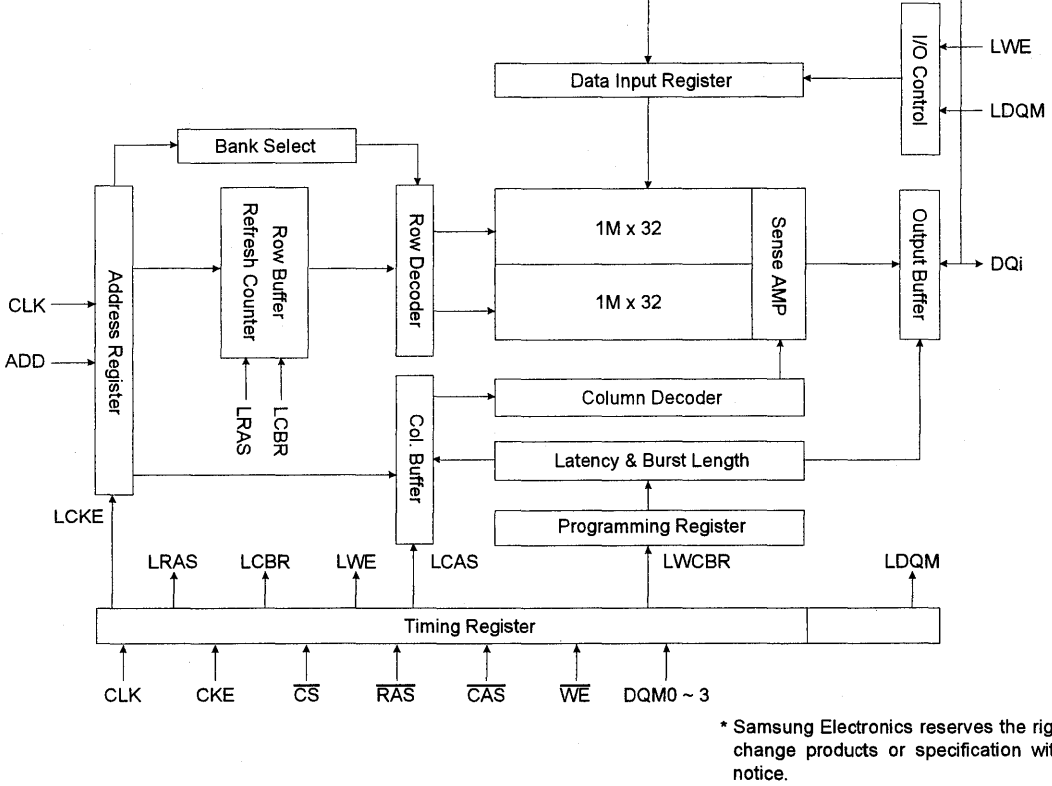
GENERAL DESCRIPTION

The KM432S2020B is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 1,048,576 words by 32 bits, fabricated with SAMSUNG' s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clcok cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part NO.	MAX Freq.	Interface	Package
KM432S2020BT-G/F8	125MHz	LVTTL	86 TSOP (II)
KM432S2020BT-G/F10	100MHz		
KM432S2020BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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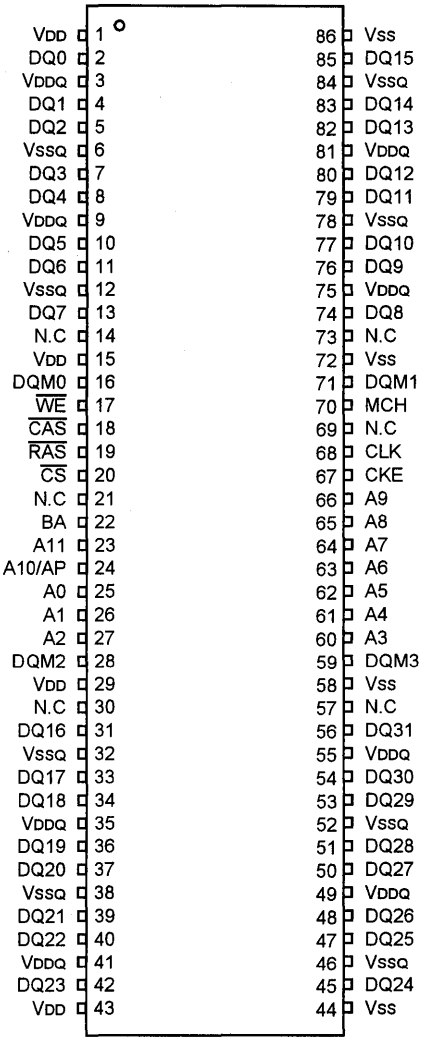
PIN CONFIGURATION (TOP VIEW)



86PIN TSOP (II)
(400mil x 875mil)
(0.5 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQMn.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down mode.
$A_0 \sim A_{11}$	*Address*	Row / column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{11}$, column address : $CA_0 \sim CA_7$
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 3	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQMn active.
$DQ_0 \sim _{31}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
MCH	*Must Connect High*	This pin is to be connected to logic "High" all the time after power on.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance ($A_0 \sim A_{11}$, BA, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM0 - 3)	C_{IN1}	2.5	5.0	pF
Input capacitance (CLK)	C_{IN2}	2.5	4.0	pF
Data input/output capacitance (DQ_0 - DQ_{31})	C_{OUT}	4.0	6.5	pF

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

DC CHARACTERISTICS

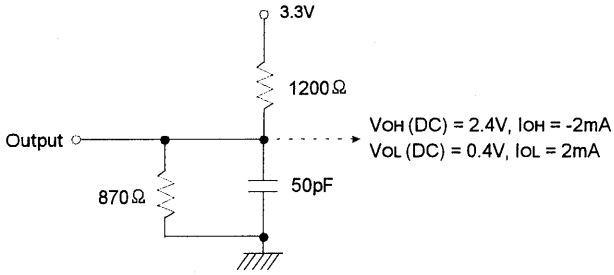
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 t_{RC}≥t_{RC}(min) I_{OL} = 0 mA		110	90	80	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		25			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		10				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		15			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	220	180	150	mA	1
			2	155	145	125		
Refresh Current	I_{CC5}	t_{RC}≥t_{RC}(min)		150			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		3			mA	3
				450			uA	4

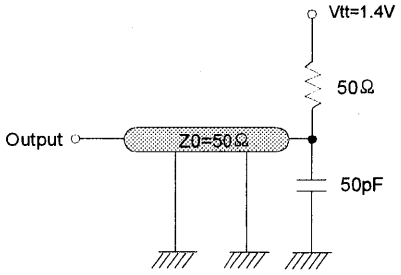
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM432S2020BT-G**
4. KM432S2020BT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	20	26	ns	1
Row precharge time		$t_{RP(min)}$	20	20	26	ns	1
Row active time		$t_{RAS(min)}$	48	48	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	70	86	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	86	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		7	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
Output data hold time with no load		tOHN	1.8		2		2		ns	4
CLK high pulse width		tCH	3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3.5		ns	3
Input setup time		tSS	2		2		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		7	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. This parameter is guaranteed by design not by test.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM432S2020BT-8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM432S2020BT-10

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	7	5	3	2	3	1	1	1
83MHz (12.0ns)	3	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM432S2020BT-12

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		86ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11}, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command for another bank can be issued.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

512K x 32Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS Latency (2 & 3)
  - -. Burst Length (1, 2, 4, 8 & full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system colck
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

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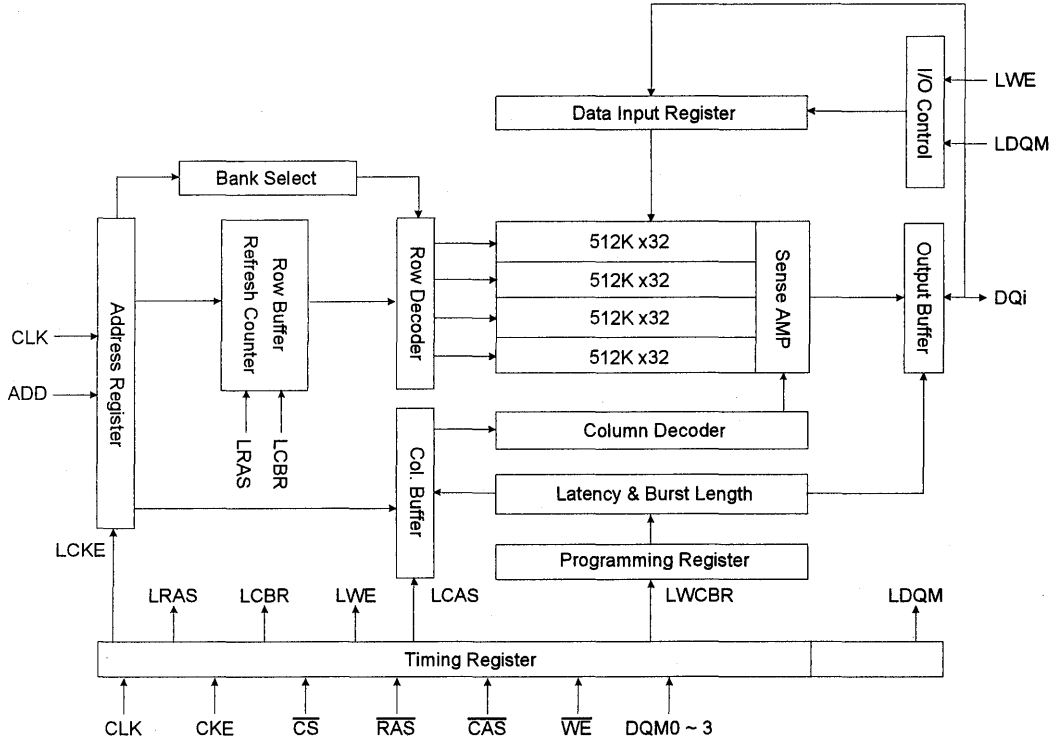
KM432S2030BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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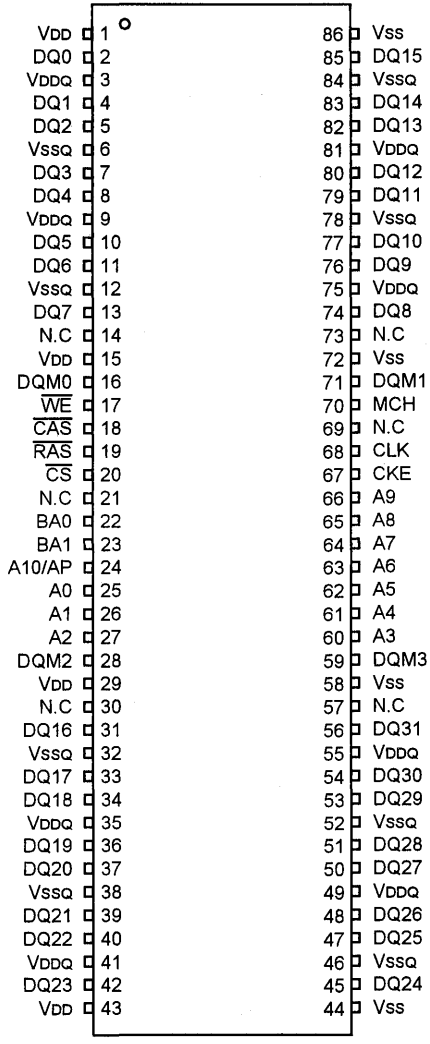
PIN CONFIGURATION (TOP VIEW)



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(400mil x 875mil)
(0.5 mm PIN PITCH)

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CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down mode.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_7
BA_0 ~ BA_1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 3	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQMn active.
DQ_0 ~ 31	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
MCH	*Must Connect High*	This pin is to be connected to logic "High" all the time after power on.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE (V_{DD} = 3.3V, T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA_0 ~ BA_1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & DQM0 ~ 3)	C_{IN1}	2.5	5.0	pF
Input capacitance (CLK)	C_{IN2}	2.5	4.0	pF
Data input/output capacitance (DQ_0 - DQ_{31})	C_{OUT}	4.0	6.5	pF

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}.

DC CHARACTERISTICS

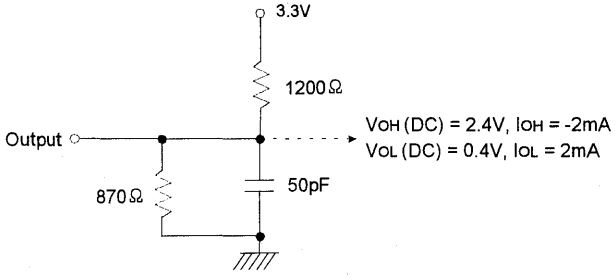
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 t_{RC}≥t_{RC}(min) I_{OL} = 0 mA		110	90	80	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		25			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		10				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		30			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		15			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	220	180	150	mA	1
			2	155	145	125		
Refresh Current	I_{CC5}	t_{RC}≥t_{RC}(min)		150			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		3			mA	3
				450			uA	4

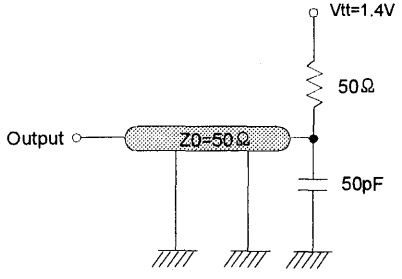
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. KM432S2030BT-G**
4. KM432S2030BT-F**

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	20	26	ns	1
Row precharge time		tRP(min)	20	20	26	ns	1
Row active time		tRAS(min)	48	48	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	70	86	ns	1
	@Auto refresh	tRFC(min)	80	80	86	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		10		12		13			
CLK to valid output delay	CAS latency=3	tSAC		6		6		7	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
Output data hold time with no load		tOHN	1.8		2		2		ns	4
CLK high pulse width		tCH	3		3		3.5		ns	3
CLK low pulse width		tCL	3		3		3.5		ns	3
Input setup time		tSS	2		2		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		7	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

4. This parameter is guaranteed by design not by test.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM432S2030BT-8

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM432S2030BT-10

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	7	5	3	2	3	1	1	1
83MHz (12.0ns)	3	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM432S2030BT-12

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		86ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP & BA_0 ~ BA_1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

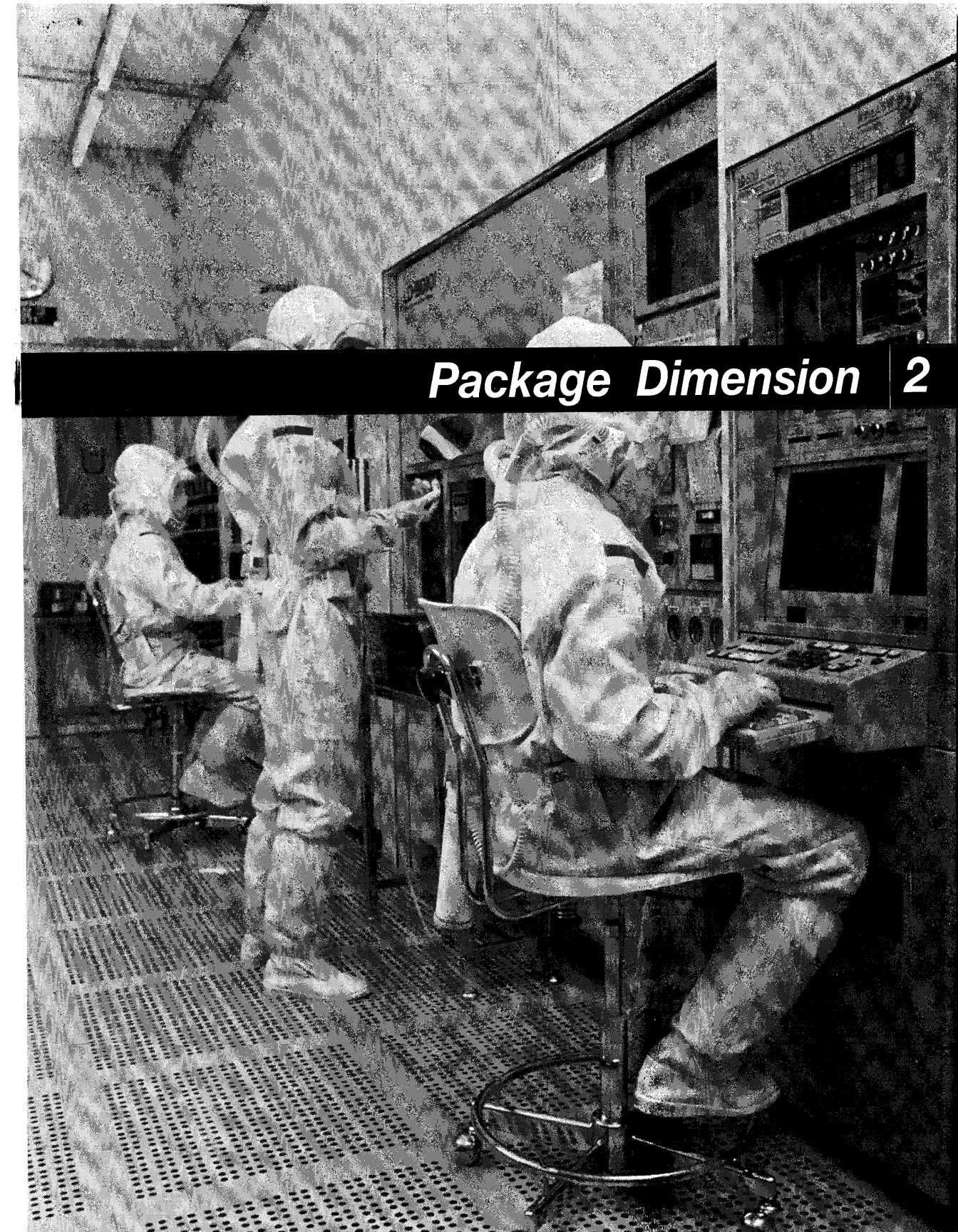
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command for another bank can be issued.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

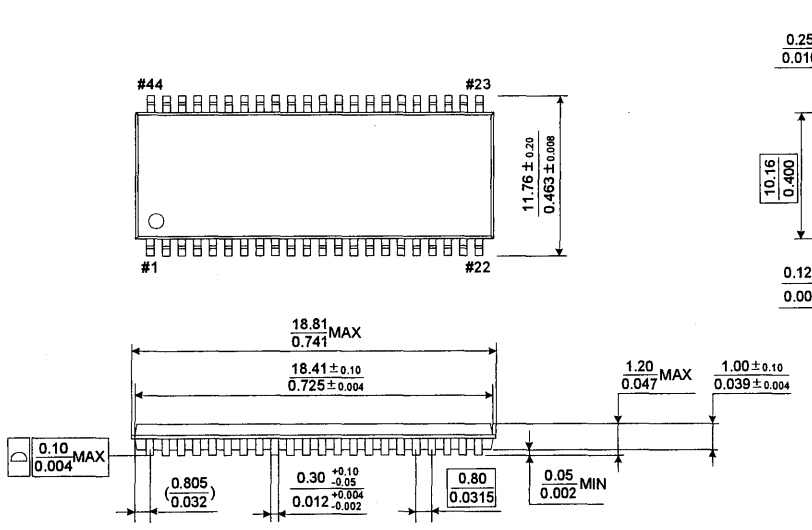


Package Dimension 2

PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

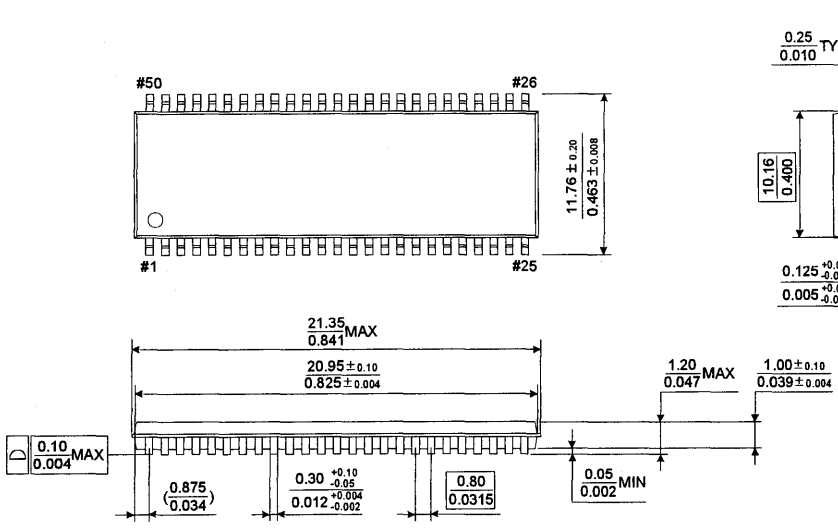
44-TSOP2-400F

Unit : Millimeters



50-TSOP2-400F

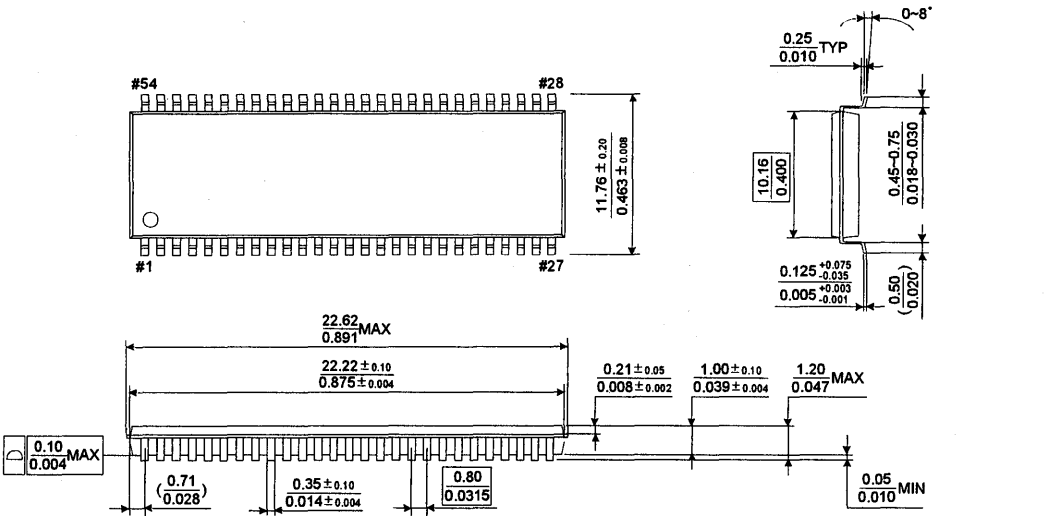
Unit : Millimeters



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

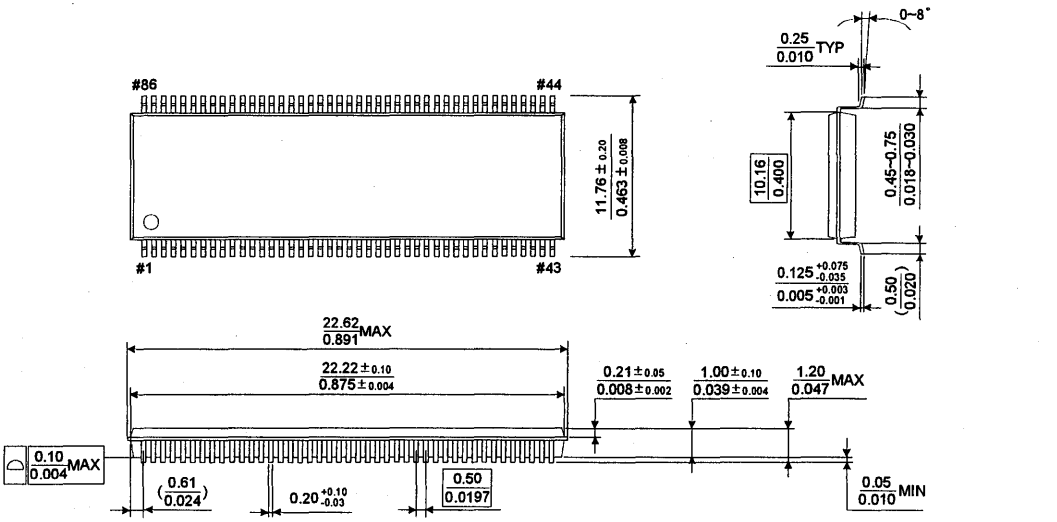
54-TSOP2-400F

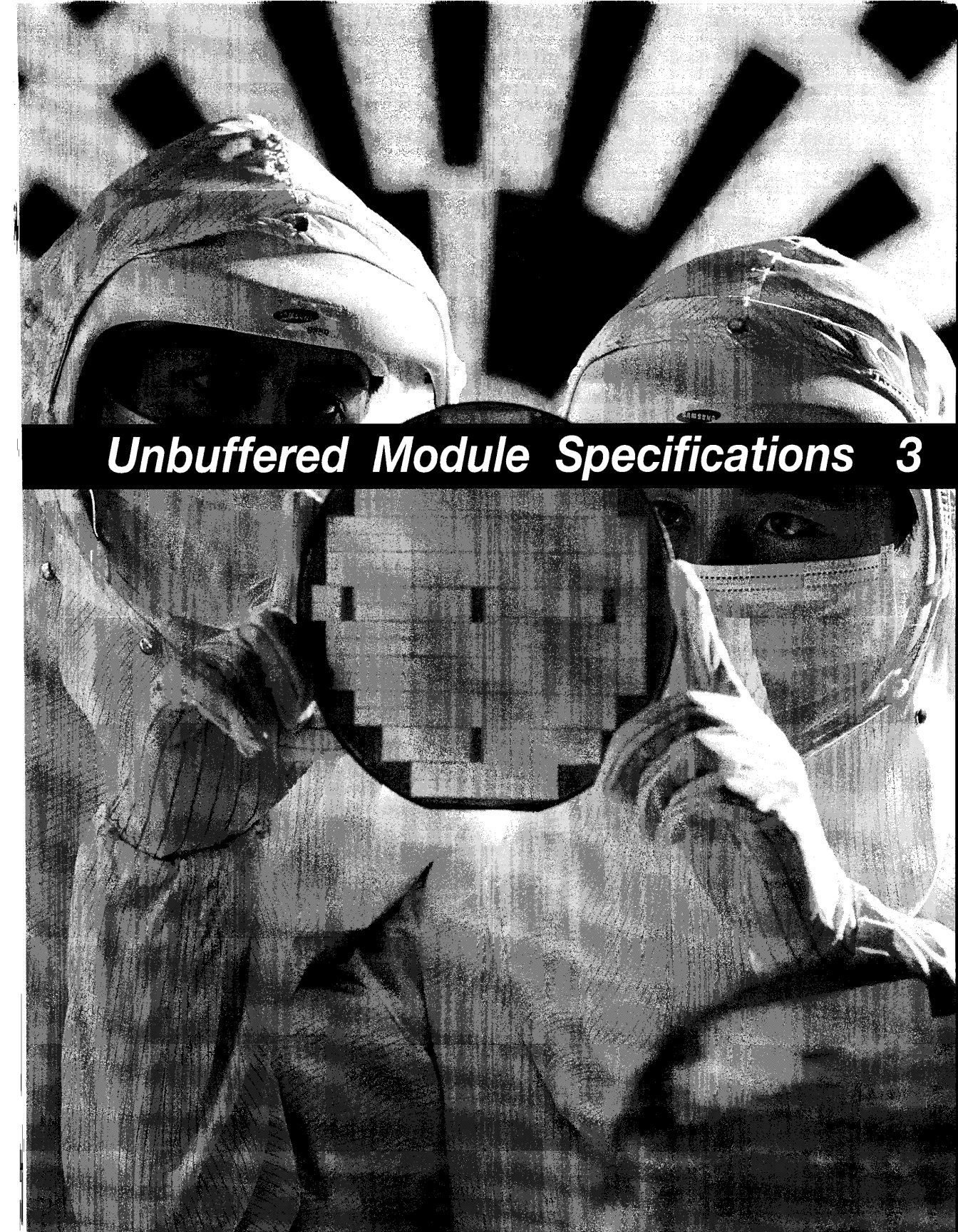
Unit : Millimeters



86-TSOP2-400F

Unit : Millimeters

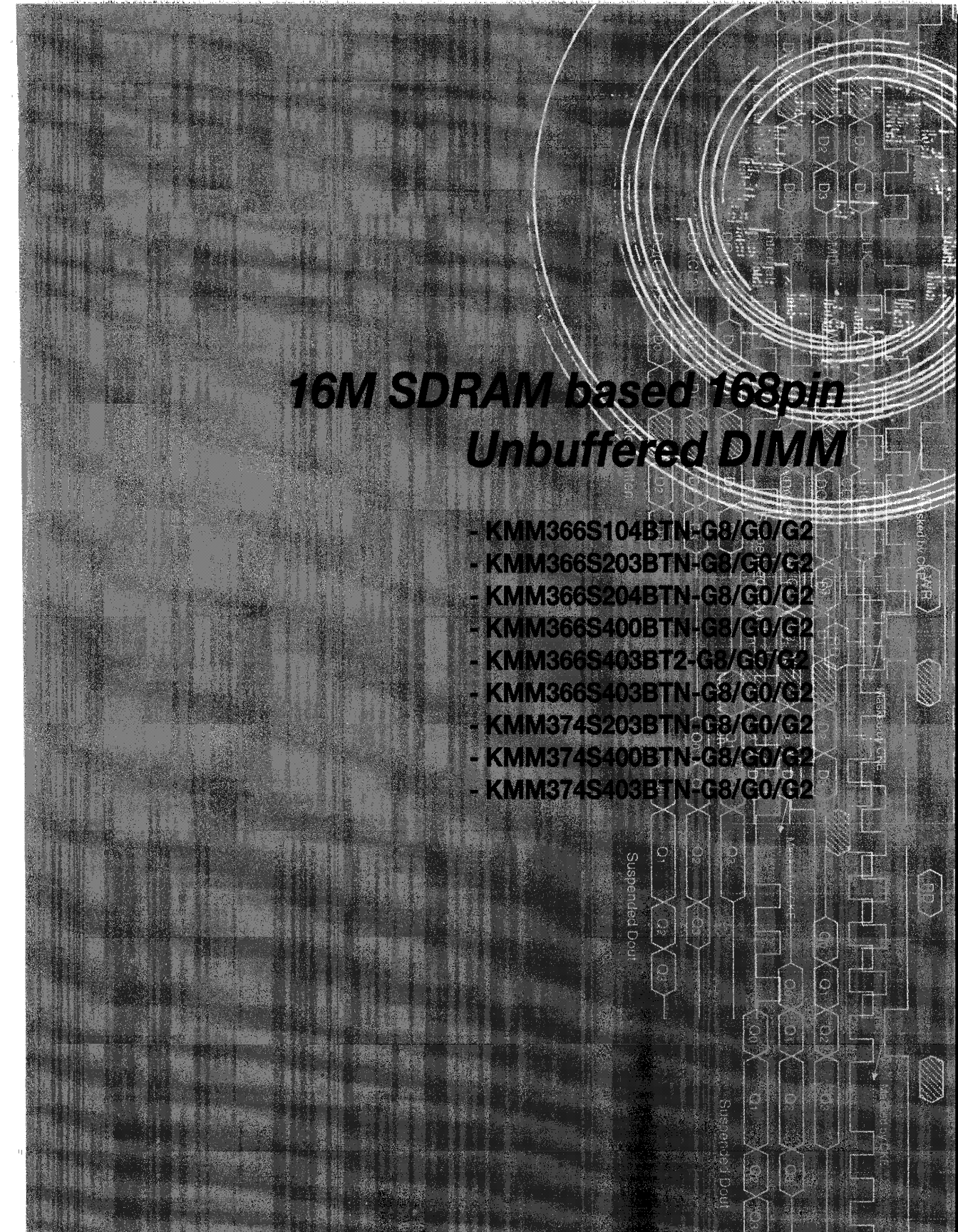




Unbuffered Module Specifications 3

16M SDRAM based 168pin Unbuffered DIMM

- KMM366S104BTN-G8/G0/G2
- KMM366S203BTN-G8/G0/G2
- KMM366S204BTN-G8/G0/G2
- KMM366S400BTN-G8/G0/G2
- KMM366S403BT2-G8/G0/G2
- KMM366S403BTN-G8/G0/G2
- KMM374S203BTN-G8/G0/G2
- KMM374S400BTN-G8/G0/G2
- KMM374S403BTN-G8/G0/G2



KMM366S104BTN SDRAM DIMM

1Mx64 SDRAM DIMM based on 1Mx16, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S104BTN is a 1M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S104BTN consists of four CMOS 1M x 16 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S104BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S104BTN-G8	125MHz (8ns)
KMM366S104BTN-G0	100MHz (10ns)
KMM366S104BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, single sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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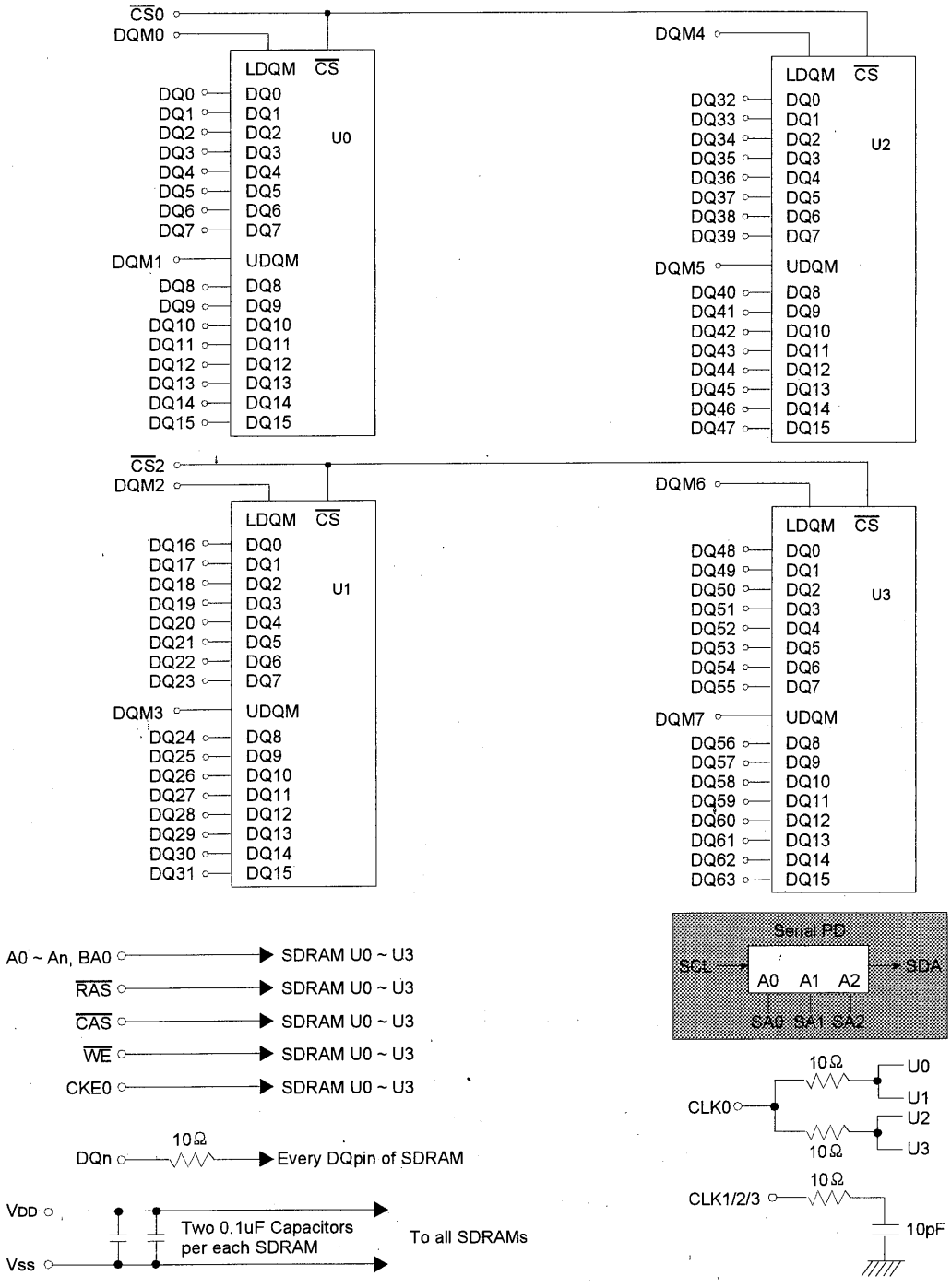
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

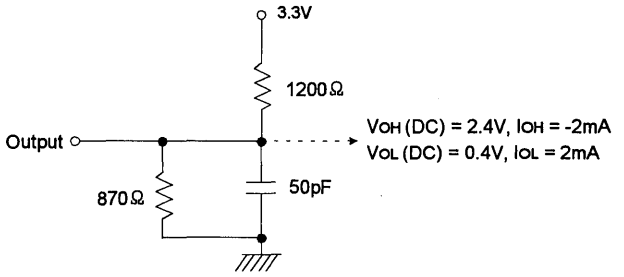
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition		CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA			460	440	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns			2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞			2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns			80			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable			20				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns			12			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞			8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns			140			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable			80			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row	3	540	440	380	mA	1
				2	380	360	320		
				1	260	240	220		
			@ Different Row	3	800	720	640	mA	1
				2	620	560	480		
				1	480	440	380		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$			280			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V			2			mA	

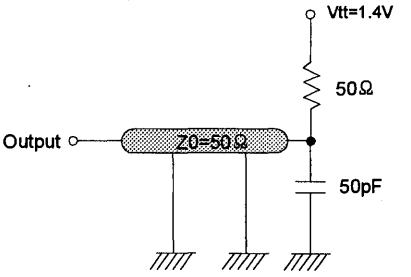
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	24	26	30	ns	1
Row precharge time		$t_{RP(min)}$	20	26	30	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	80	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S104BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S104BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S104BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

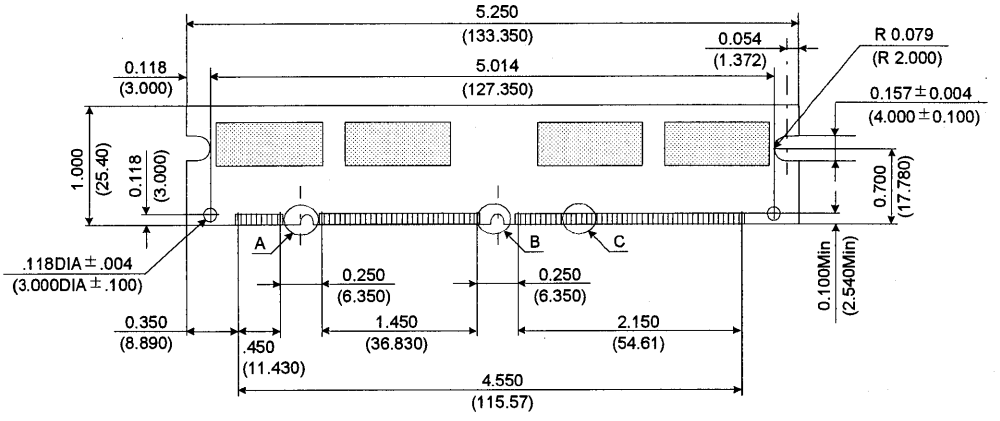
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

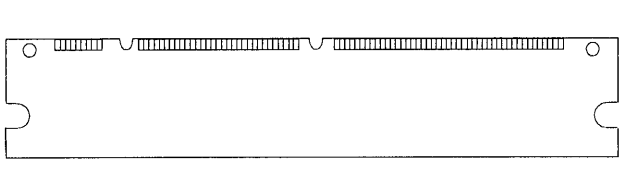
6. Burst stop command is valid at every burst length.

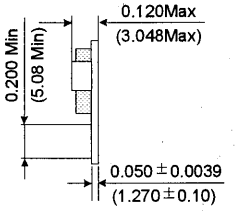
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

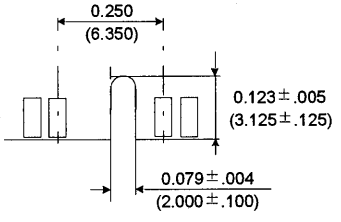
PACKAGE DIMENSIONS

Units : Inches (millimeters)

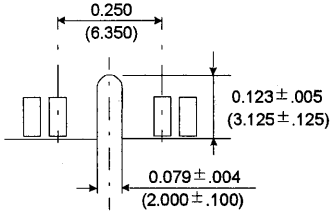




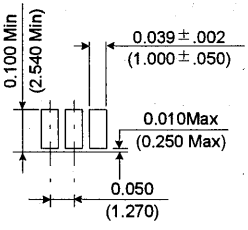




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S1020BT

KMM366S203BTN SDRAM DIMM

2Mx64 SDRAM DIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S203BTN is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S203BTN consists of eight CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S203BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S203BTN-G8	125MHz (8ns)
KMM366S203BTN-G0	100MHz (10ns)
KMM366S203BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

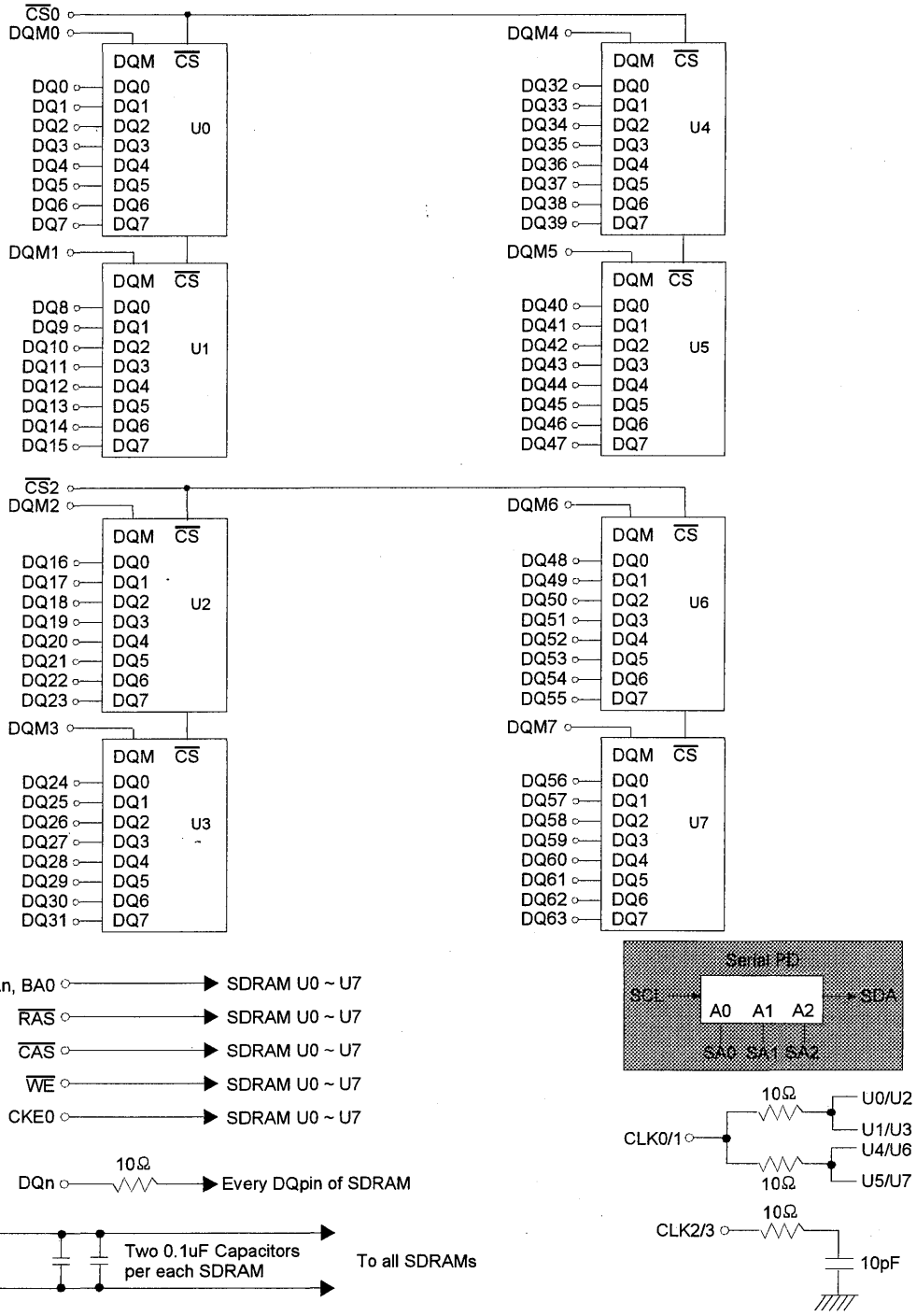
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

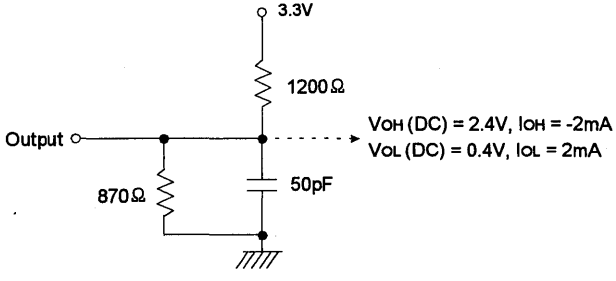
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		840	800	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		4				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		40				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		280			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,000	800	720	mA	1
			@ Same Row 2	720	640	600		
			@ Same Row 1	480	440	400		
			@ Different Row 3	1,440	1,280	1,120	mA	1
			@ Different Row 2	1,160	1,040	880		
			@ Different Row 1	920	840	720		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		560			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

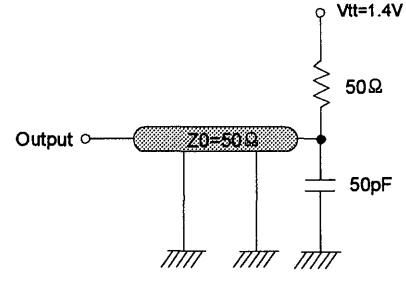
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S203BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S203BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S203BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

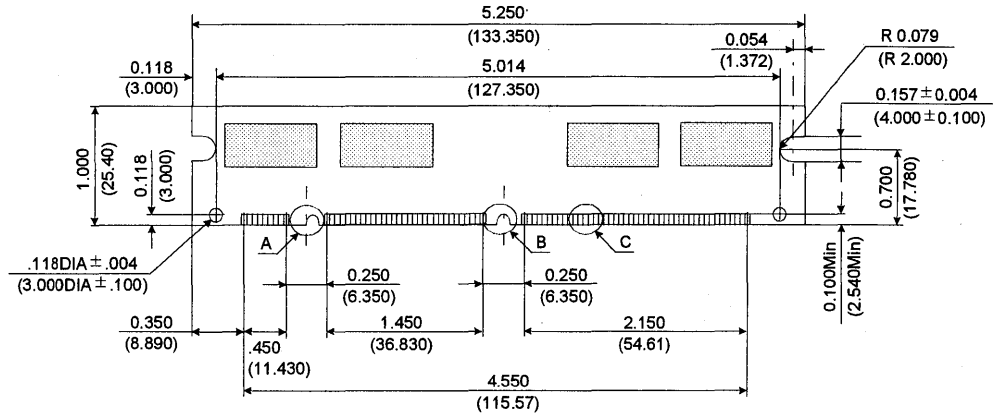
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H			X			V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

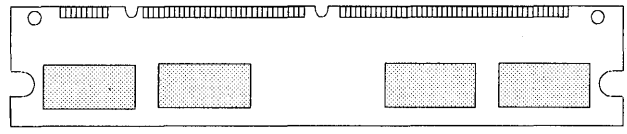
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

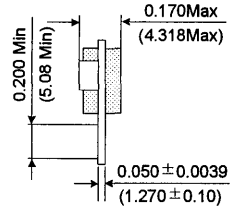
Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

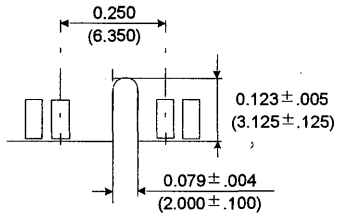
PACKAGE DIMENSIONS

Units : Inches (millimeters)

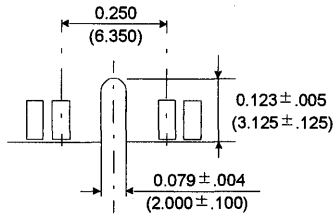




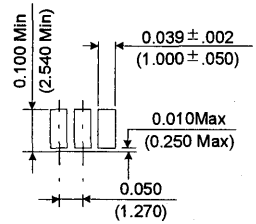




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

KMM366S204BTN SDRAM DIMM

2Mx64 SDRAM DIMM based on 1Mx16, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S204BTN is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S204BTN consists of eight CMOS 1M x 16 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S204BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S204BTN-G8	125MHz (8ns)
KMM366S204BTN-G0	100MHz (10ns)
KMM366S204BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

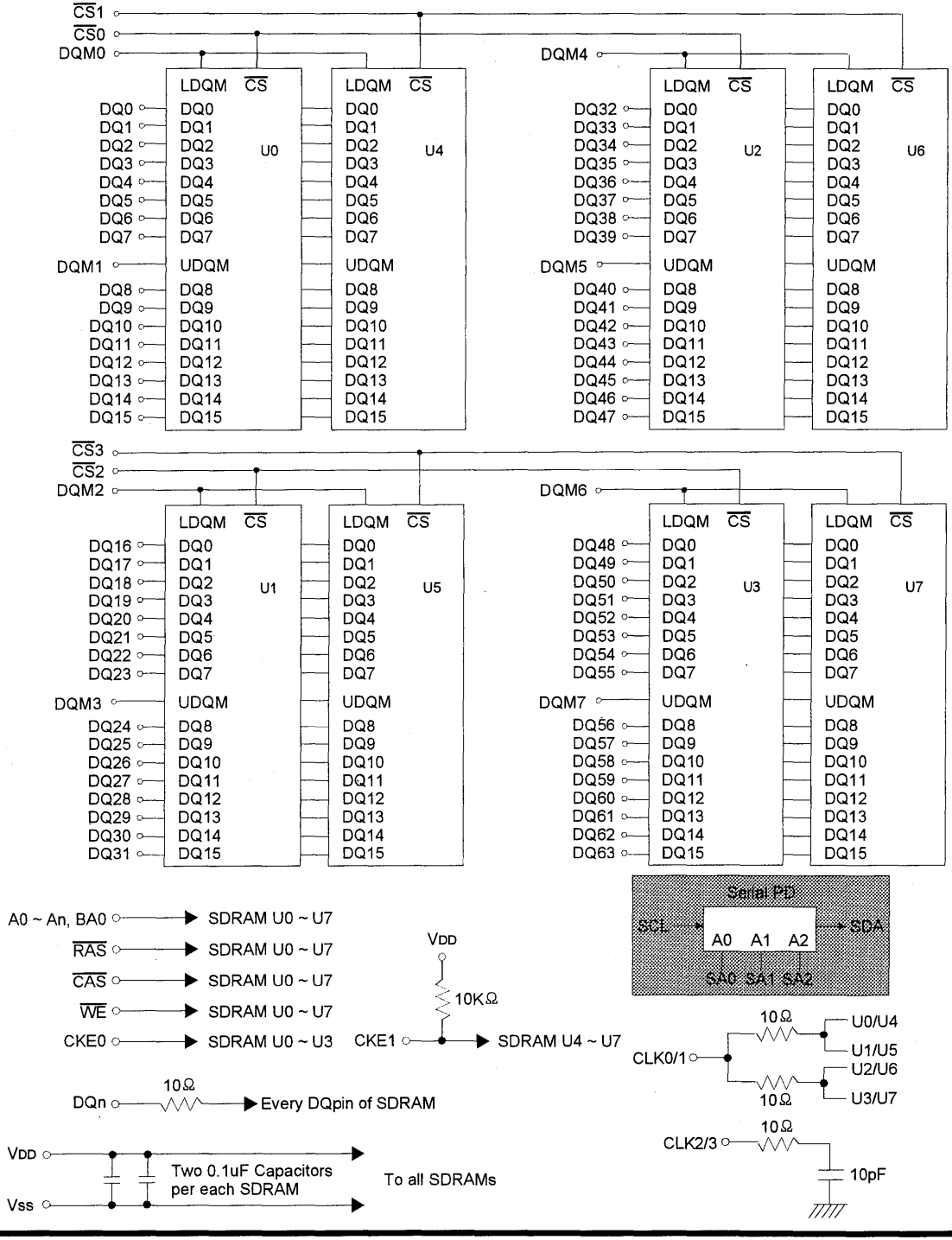
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

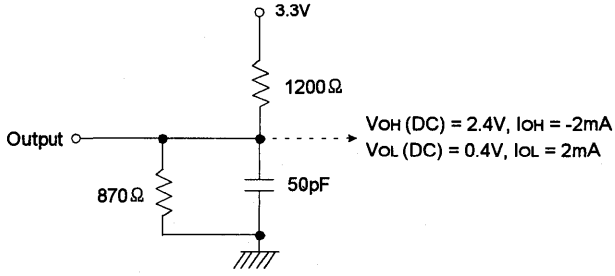
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	520	480	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		4				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		40				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		280			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	620	520	460	mA	1
			@ Same Row 2	460	440	400		
			@ Same Row 1	340	320	300		
			@ Different Row 3	880	800	720	mA	1
			@ Different Row 2	700	640	560		
			@ Different Row 1	560	520	460		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		560			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

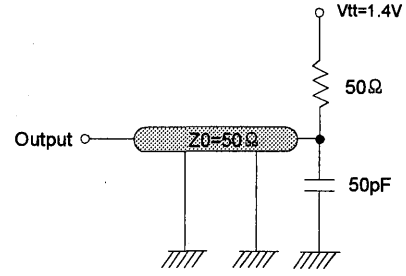
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	24	26	30	ns	1
Row precharge time		$t_{RP(min)}$	20	26	30	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	80	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S204BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S204BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S204BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

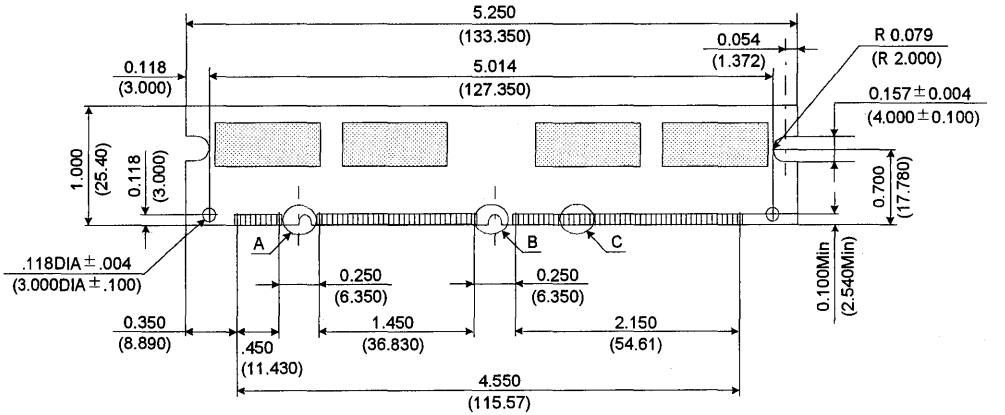
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

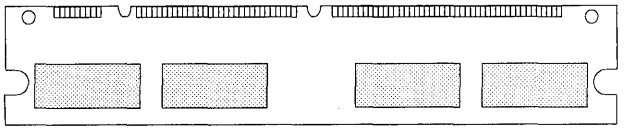
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

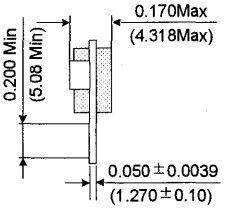
Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

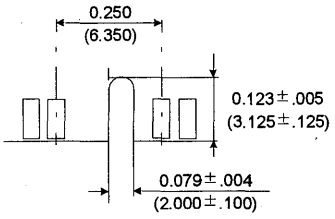
PACKAGE DIMENSIONS

Units : Inches (millimeters)

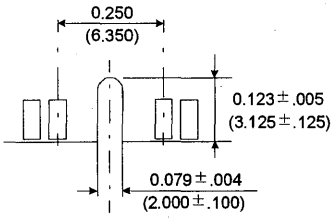




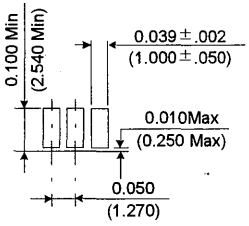




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S1020BT

KMM366S400BTN SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx4, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S400BTN is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S400BTN consists of sixteen CMOS 4M x 4 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S400BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S400BTN-G8	125MHz (8ns)
KMM366S400BTN-G0	100MHz (10ns)
KMM366S400BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

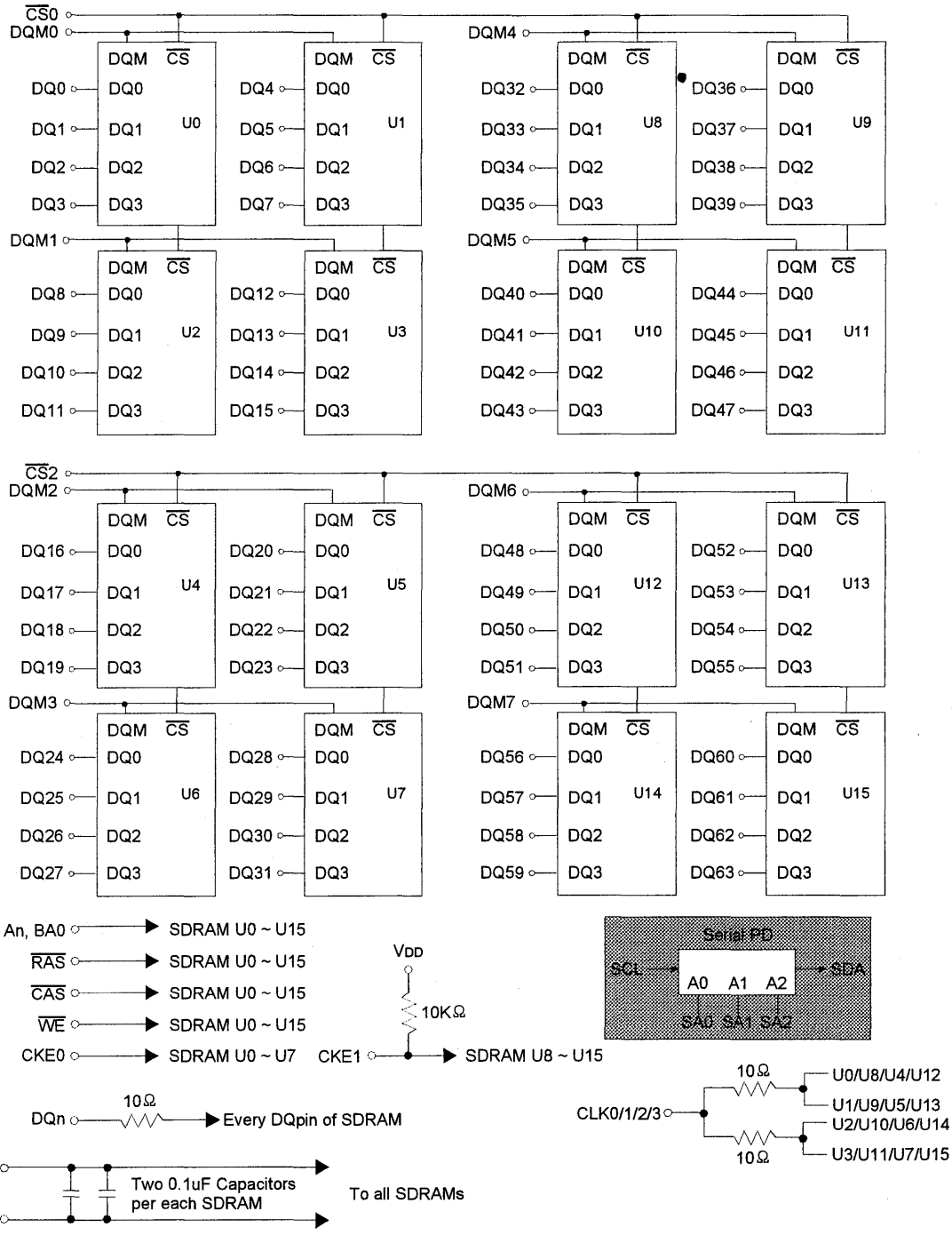
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA9
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

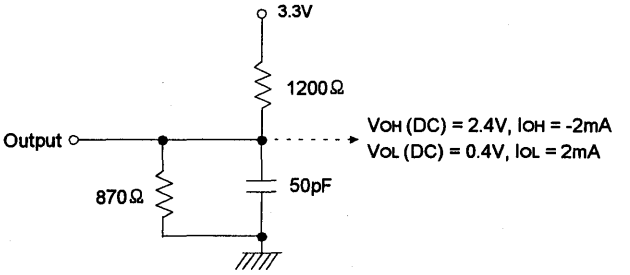
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,600	1,520	1,360	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		560			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,920	1,520	1,360	mA	1
			@ Same Row 2	1,440	1,280	1,200		
			@ Same Row 1	960	880	800		
			@ Different Row 3	2,720	2,400	2,080	mA	1
			@ Different Row 2	2,240	2,000	1,680		
			@ Different Row 1	1,760	1,600	1,360		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		1,120			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		8			mA	

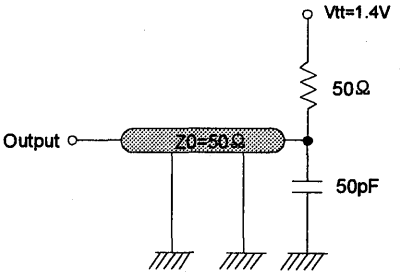
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	24	26	30	ns	1
Row precharge time		$t_{RP(min)}$	20	26	30	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	80	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S400BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S400BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S400BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.

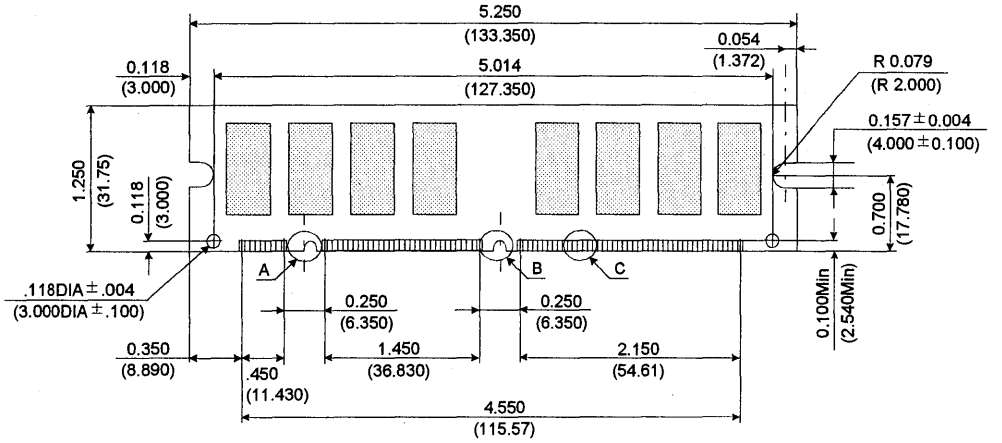
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

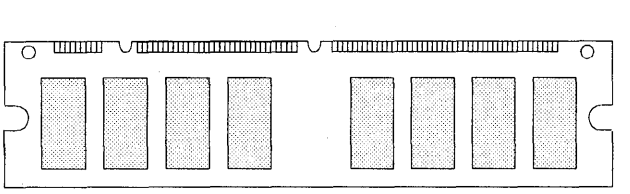
6. Burst stop command is valid at every burst length.

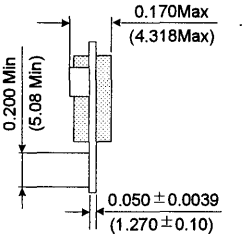
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

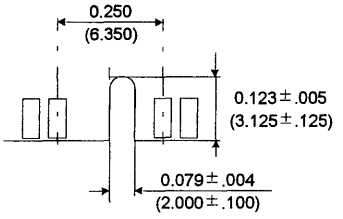
PACKAGE DIMENSIONS

Units : Inches (millimeters)

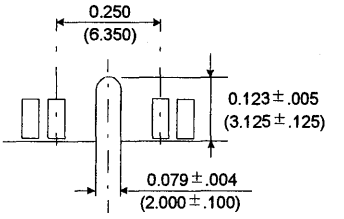




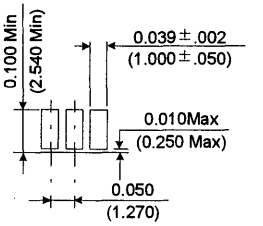




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S4020BT

KMM366S403BT2 SDRAM DIMM

4Mx64 SDRAM DIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S403BT2 is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S403BT2 consists of sixteen CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S403BT2 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S403BT2-G8	125MHz (8ns)
KMM366S403BT2-G0	100MHz (10ns)
KMM366S403BT2-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,150mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

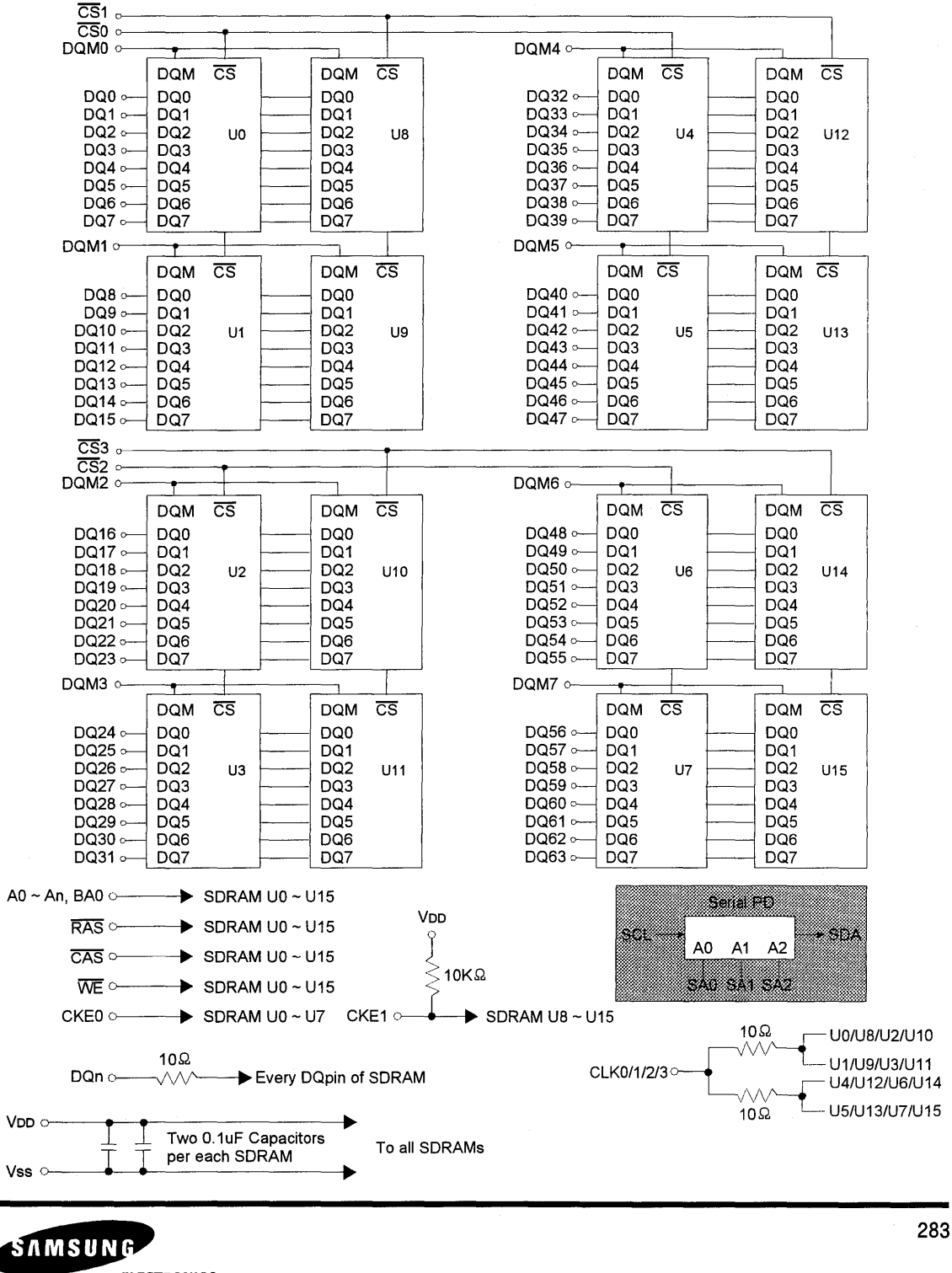
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, tsHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

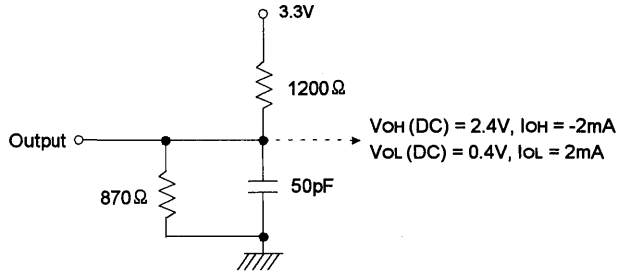
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	960	880	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		560			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,160	960	880	mA	1
			@ Same Row 2	880	800	760		
			@ Same Row 1	640	600	560		
			@ Different Row 3	1,600	1,440	1,280	mA	1
			@ Different Row 2	1,320	1,200	1,040		
			@ Different Row 1	1,080	1,000	880		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		1,120			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		8			mA	

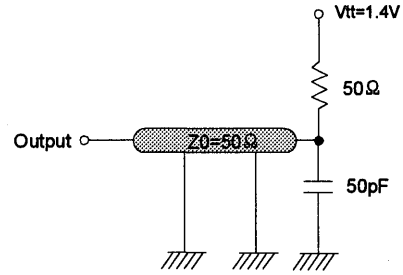
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S403BT2-G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S403BT2-G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S403BT2-G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.

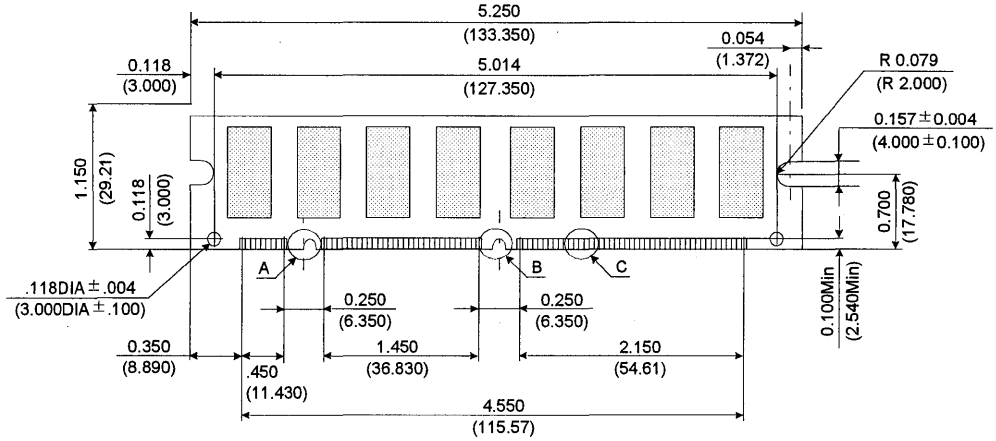
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

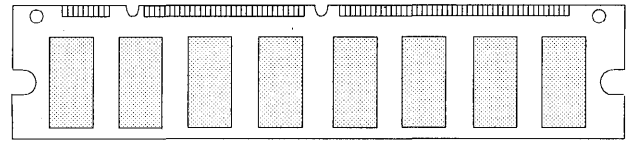
6. Burst stop command is valid at every burst length.

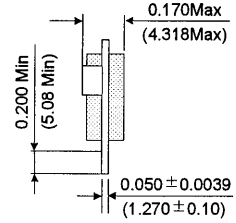
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

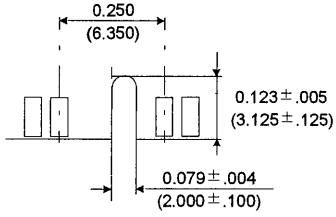
PACKAGE DIMENSIONS

Units : Inches (millimeters)

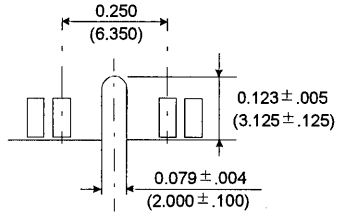




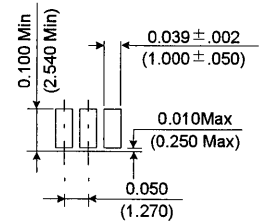




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

KMM366S403BTN SDRAM DIMM

4Mx64 SDRAM DIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S403BTN is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S403BTN consists of sixteen CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board in parellel for each SDRAM. The KMM366S403BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S403BTN-G8	125MHz (8ns)
KMM366S403BTN-G0	100MHz (10ns)
KMM366S403BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

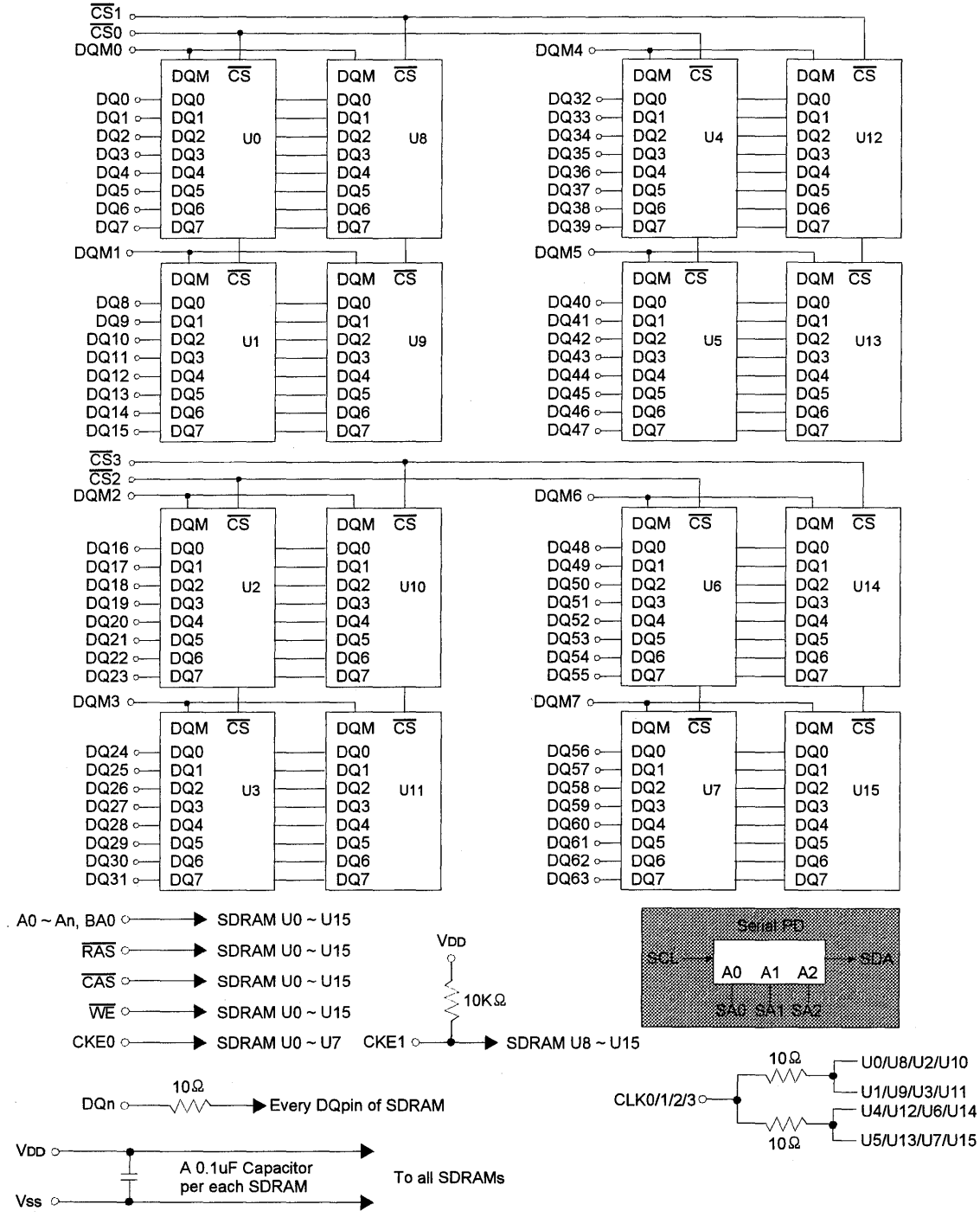
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS}$0 ~ $\overline{CS}$3)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

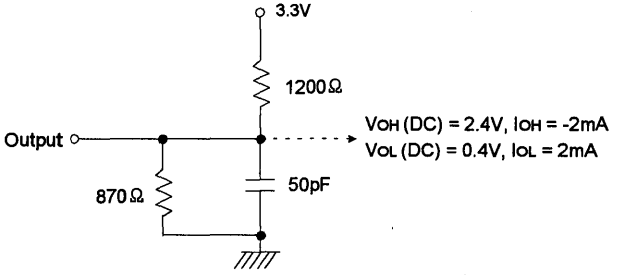
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	960	880	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		32				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		560			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		320			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,160	960	880	mA	1
			@ Same Row 2	880	800	760		
			@ Same Row 1	640	600	560		
			@ Different Row 3	1,600	1,440	1,280	mA	1
			@ Different Row 2	1,320	1,200	1,040		
			@ Different Row 1	1,080	1,000	880		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		1,120			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		8			mA	

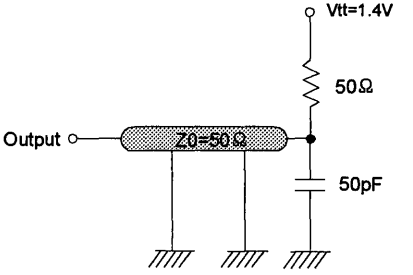
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (VDD = 3.3V±0.3V, TA = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S403BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM366S403BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S403BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

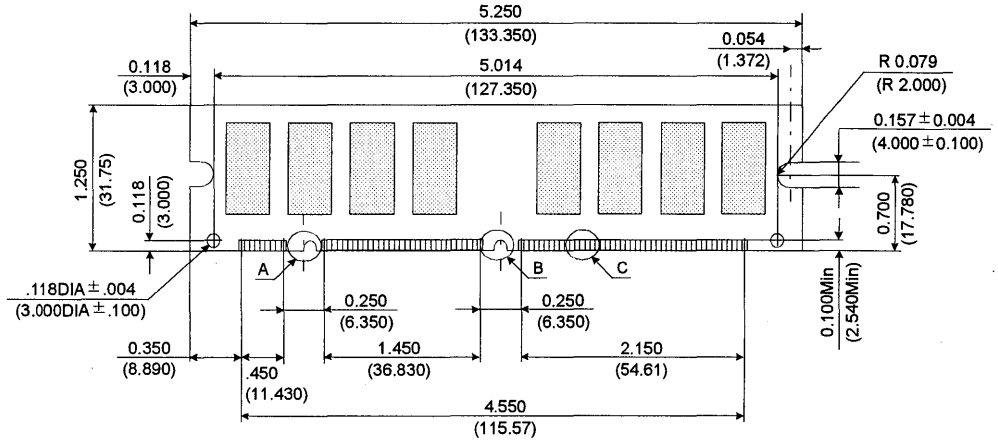
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

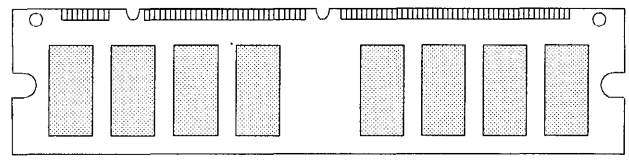
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

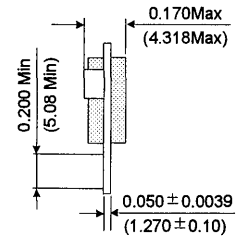
Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

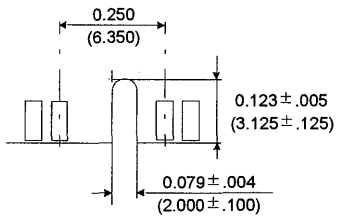
PACKAGE DIMENSIONS

Units : Inches (millimeters)

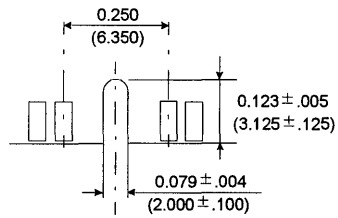




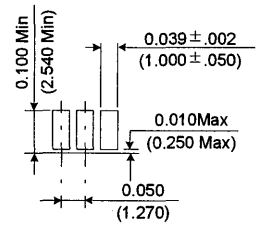




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

KMM374S203BTN SDRAM DIMM

2Mx72 SDRAM DIMM with ECC based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S203BTN is a 2M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S203BTN consists of nine CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S203BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S203BTN-G8	125MHz (8ns)
KMM374S203BTN-G0	100MHz (10ns)
KMM374S203BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

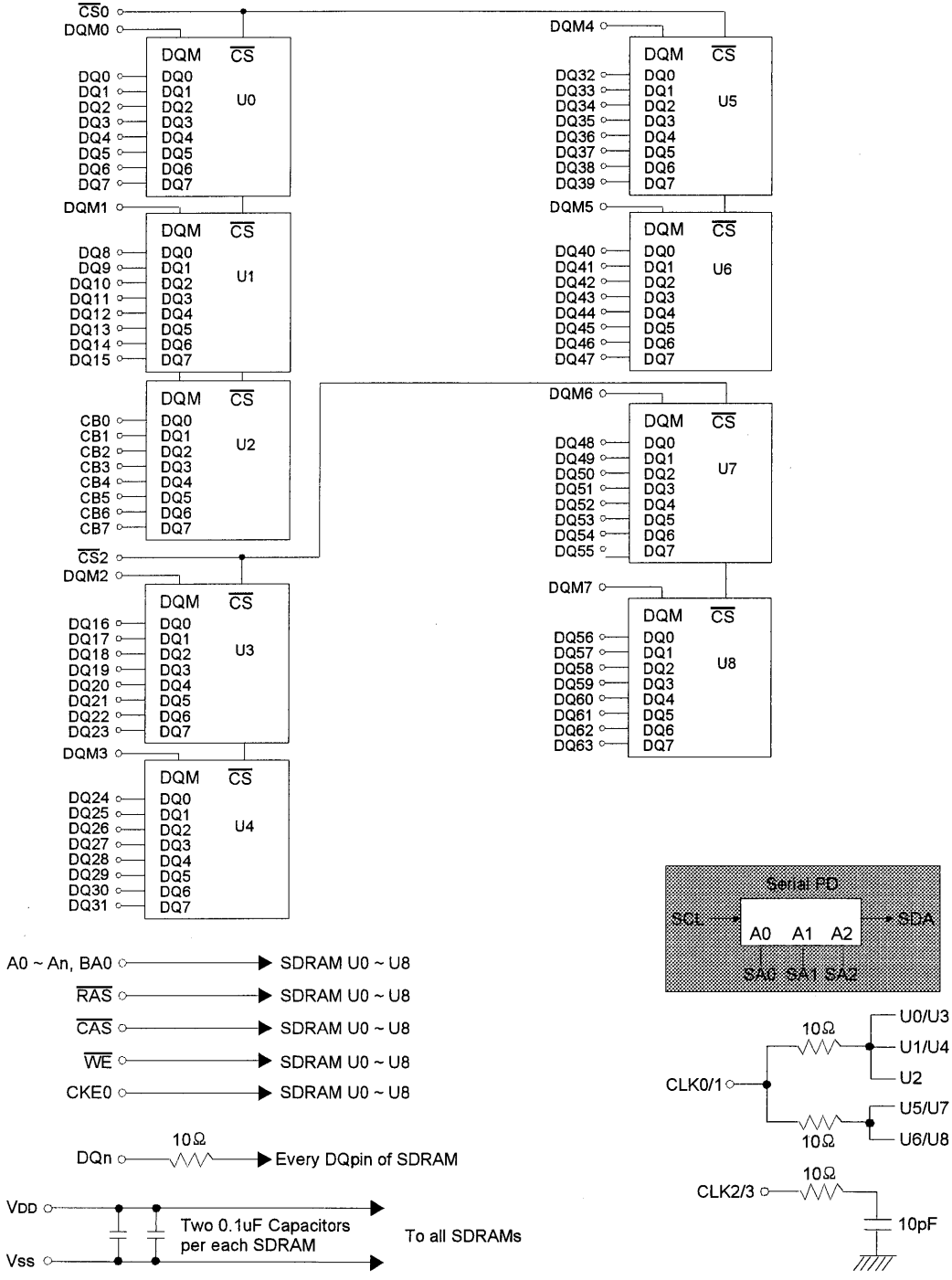
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check Bit (data-in / data-out)
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-45	-	45	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	60	pF
Input capacitance (CKE0)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

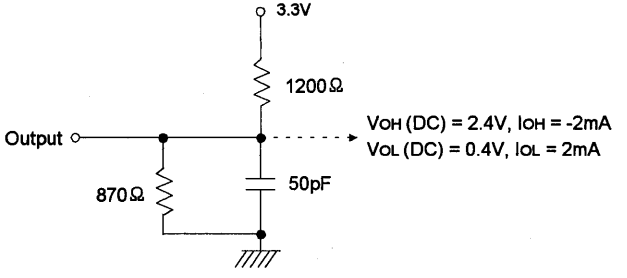
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC(min)}$ I_{OL} = 0 mA		945	900	810	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		4.5			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		4.5				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		45				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		27			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		18				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		315			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		180			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,125	900	810	mA	1
			@ Same Row 2	810	720	675		
			@ Same Row 1	540	495	450		
			@ Different Row 3	1,620	1,440	1,260	mA	1
			@ Different Row 2	1,305	1,170	990		
			@ Different Row 1	1,035	945	810		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		630			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4.5			mA	

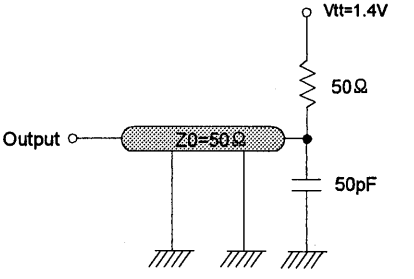
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S203BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM374S203BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S203BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.

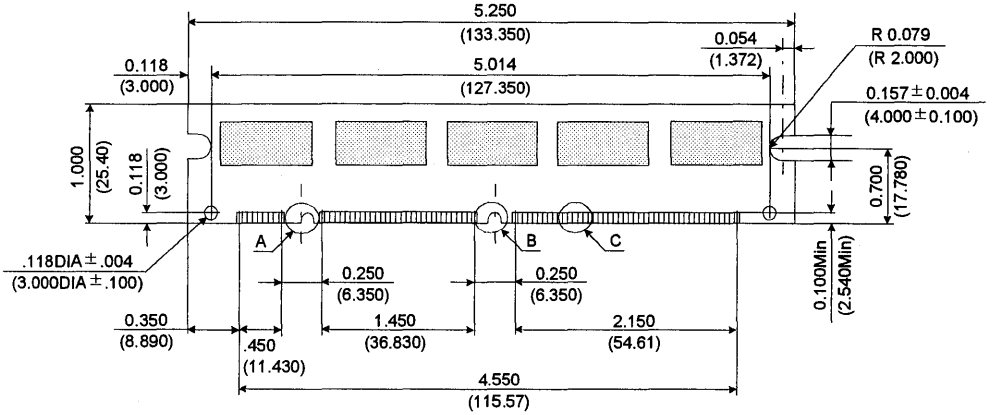
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

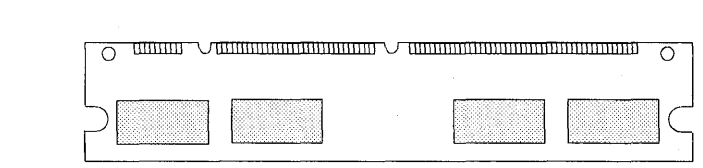
6. Burst stop command is valid at every burst length.

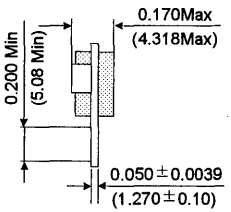
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

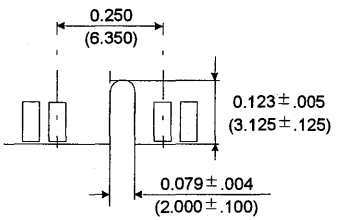
PACKAGE DIMENSIONS

Units : Inches (millimeters)

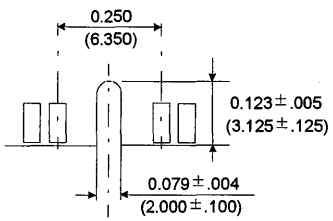




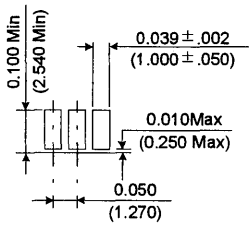




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

KMM374S400BTN SDRAM DIMM

4Mx72 SDRAM DIMM with ECC based on 4Mx4, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S400BTN is a 4M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S400BTN consists of eighteen CMOS 4M x 4 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S400BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S400BTN-G8	125MHz (8ns)
KMM374S400BTN-G0	100MHz (10ns)
KMM374S400BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

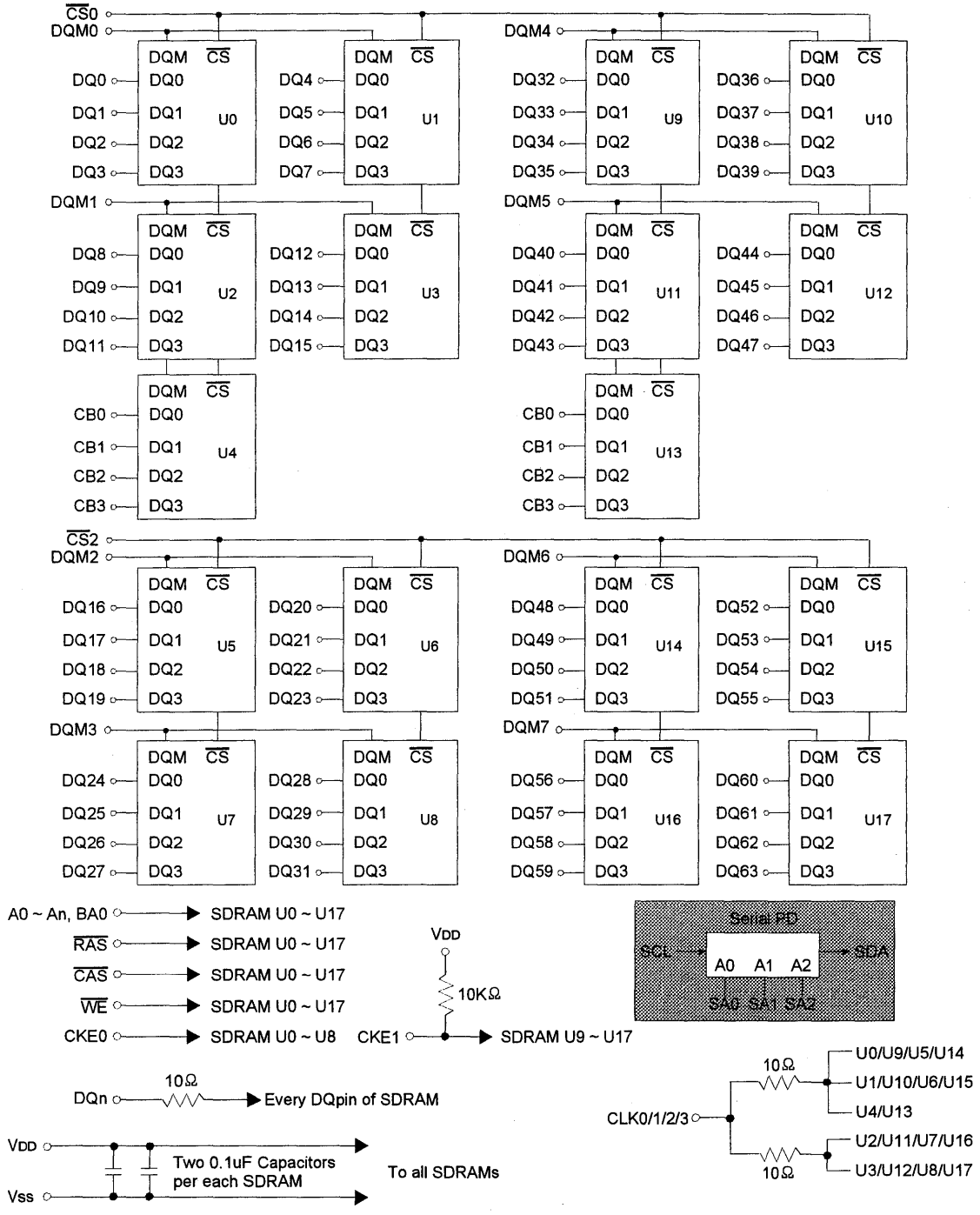
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA9
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	65	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	30	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

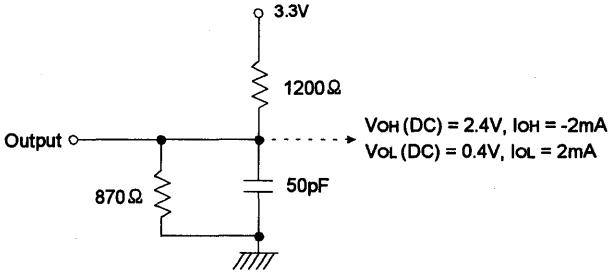
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,800	1,710	1,530	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		9			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		9				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		90				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		54			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		36				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		630			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		360			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	2,160	1,710	1,530	mA	1
			@ Same Row 2	1,620	1,440	1,350		
			@ Same Row 1	1,080	990	900		
			@ Different Row 3	3,060	2,700	2,340	mA	1
			@ Different Row 2	2,520	2,250	1,890		
			@ Different Row 1	1,980	1,800	1,530		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		1,260			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		9			mA	

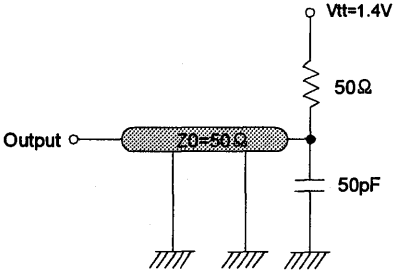
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S400BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM374S400BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S400BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

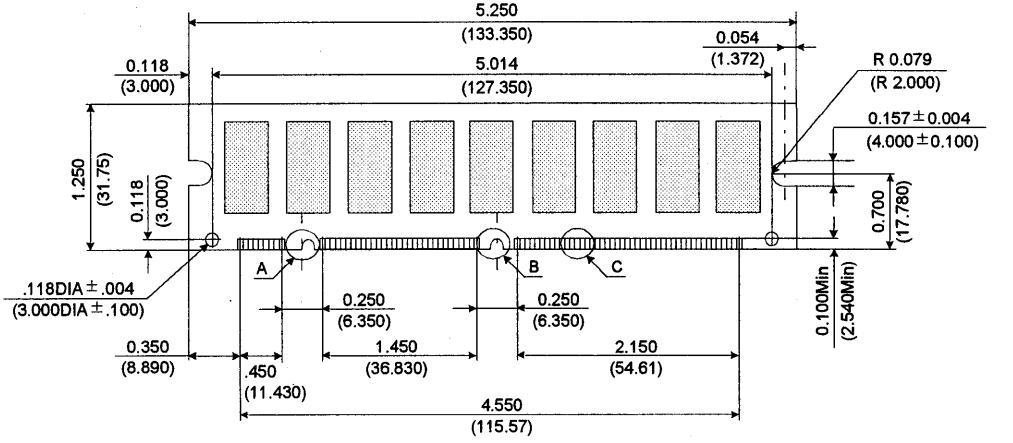
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

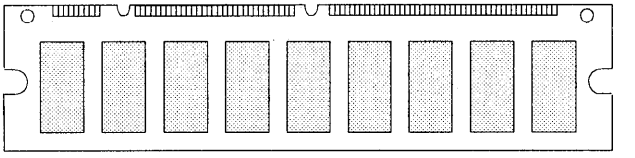
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

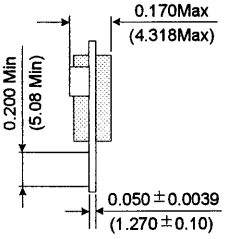
Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

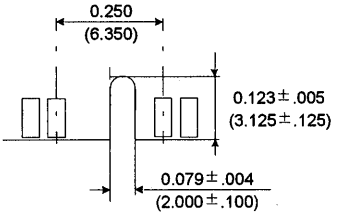
PACKAGE DIMENSIONS

Units : Inches (millimeters)

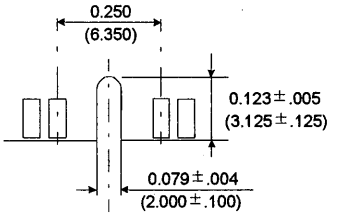




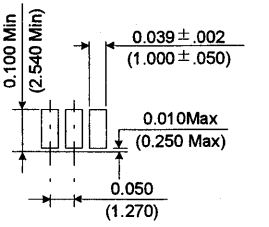




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S4020BT

KMM374S403BTN SDRAM DIMM

4Mx72 SDRAM DIMM with ECC based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S403BTN is a 4M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S403BTN consists of eighteen CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. A 0.1uF decoupling capacitor is mounted on the printed circuit board in parellel for each SDRAM. The KMM374S403BTN is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S403BTN-G8	125MHz (8ns)
KMM374S403BTN-G0	100MHz (10ns)
KMM374S403BTN-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ 7	Check Bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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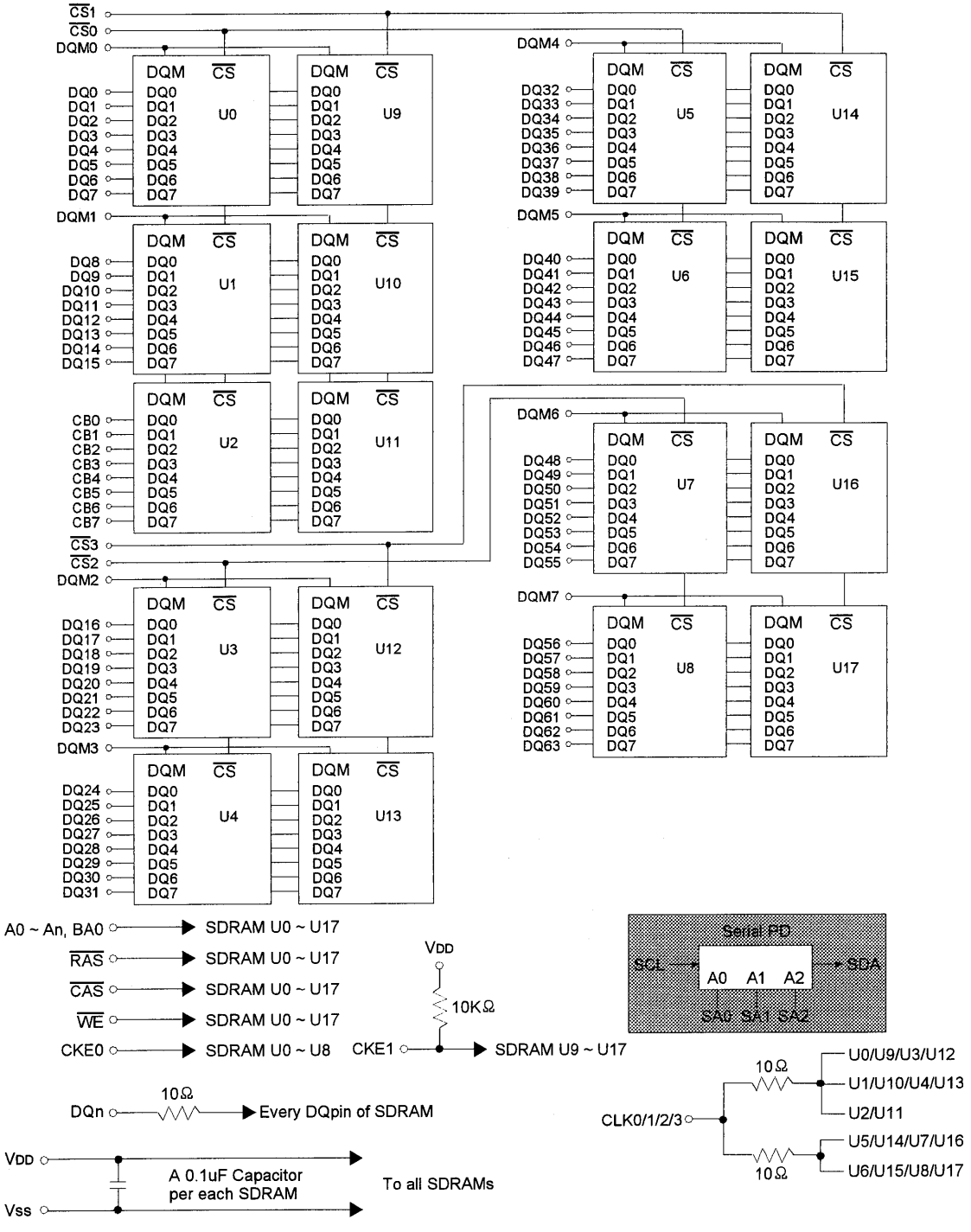
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	35	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	25	pF
Data input/output capacitance (CB0 ~CB7)	C_{OUT2}	-	25	pF

DC CHARACTERISTICS

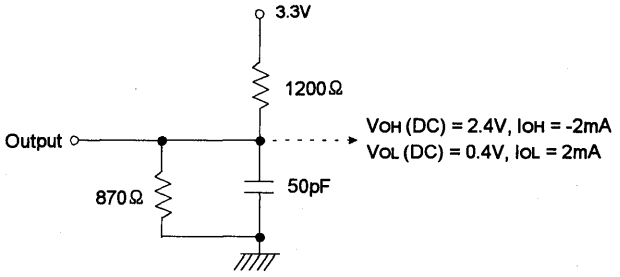
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,125	1,080	990	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		9			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		9				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		90				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		54			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		36				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		630			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		360			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,305	1,080	990	mA	1
			@ Same Row 2	990	900	855		
			@ Same Row 1	720	675	630		
			@ Different Row 3	1,800	1,620	1,440	mA	1
			@ Different Row 2	1,485	1,350	1,170		
			@ Different Row 1	1,215	1,125	990		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$		1,260			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		9			mA	

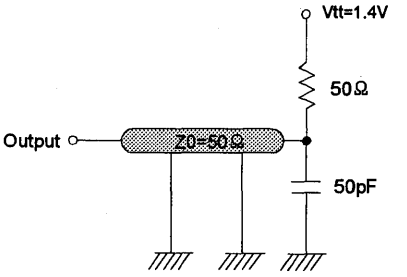
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual componenet, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S403BTN-G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM374S403BTN-G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S403BTN-G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

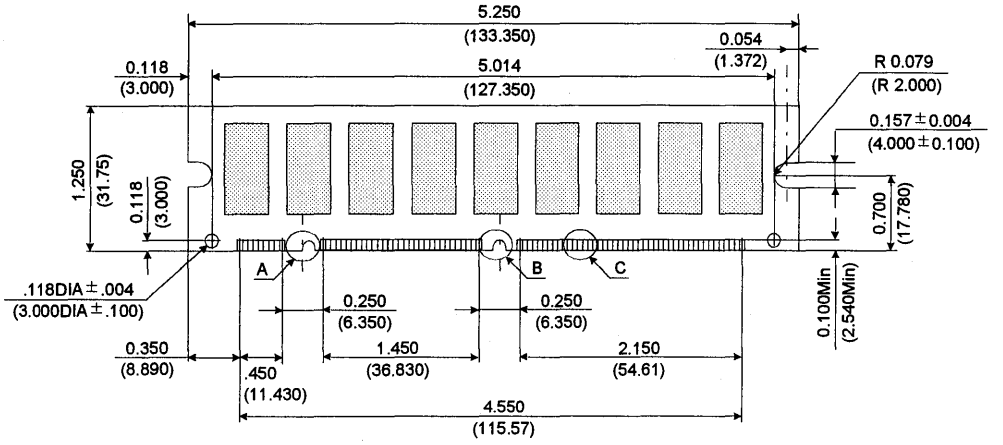
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

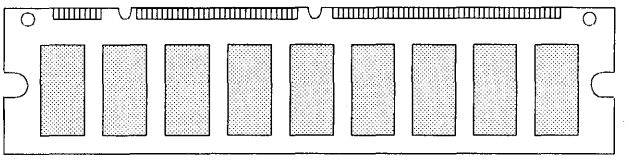
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

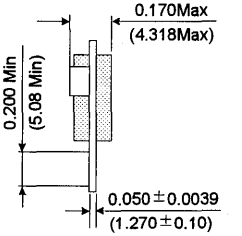
Note : 1. OP Code : Operand Code
A0 ~ A10/AP, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

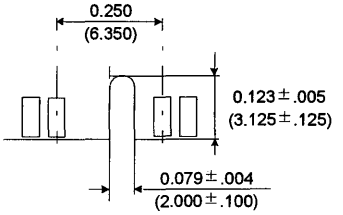
PACKAGE DIMENSIONS

Units : Inches (millimeters)

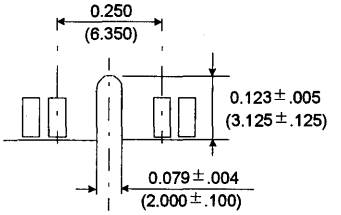




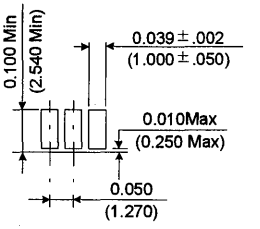




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

64M SDRAM based 168pin Unbuffered DIMM

- KMM366S404AT-G8/G0/G2
- KMM366S424AT-G8/G0/G2
- KMM366S803AT-G8/G0/G2
- KMM366S823AT-G8/G0/G2
- KMM366S804AT-G8/G0/G2
- KMM366S824AT-G8/G0/G2
- KMM366S1600AT-G8/G0/G2
- KMM366S1620AT-G8/G0/G2
- KMM366S1603AT-G8/G0/G2
- KMM366S1623AT-G8/G0/G2
- KMM374S803AT-G8/G0/G2
- KMM374S823AT-G8/G0/G2
- KMM374S1600AT-G8/G0/G2
- KMM374S1620AT-G8/G0/G2
- KMM374S1603AT-G8/G0/G2
- KMM374S1623AT-G8/G0/G2

KMM366S404AT SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S404AT is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S404AT consists of four CMOS 4M x 16 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S404AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S404AT-G8	125MHz (8ns)
KMM366S404AT-G0	100MHz (10ns)
KMM366S404AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, single sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

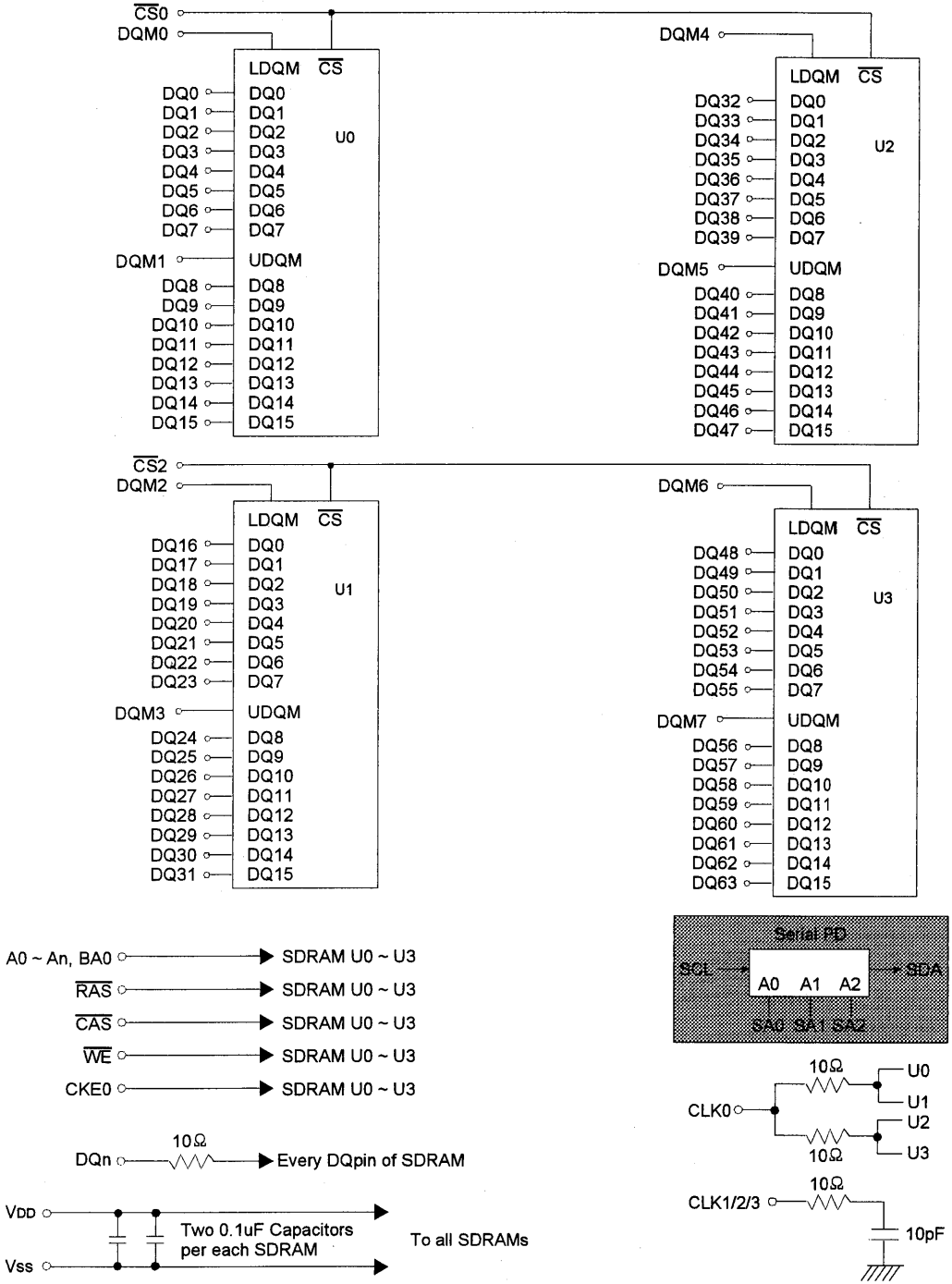
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, tSHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

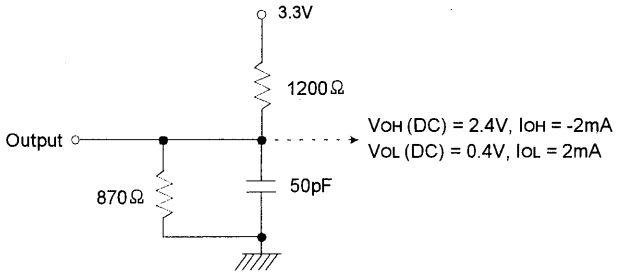
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	480	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		24				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		120			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	740	600	500	mA	1
			2	520	480	440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		720			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		6			mA	

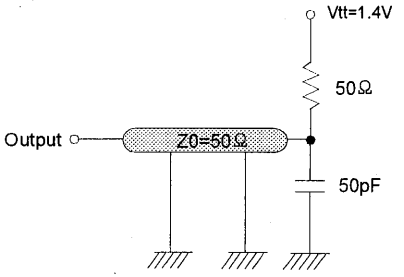
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S404AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S404AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S404AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

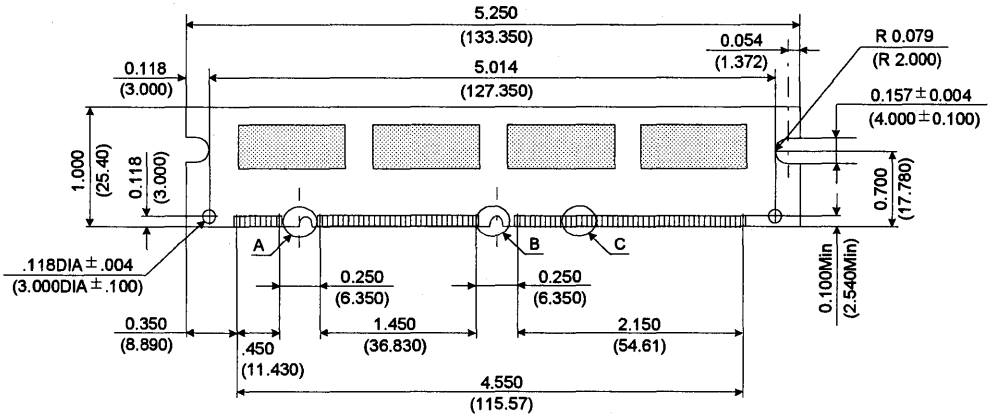
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

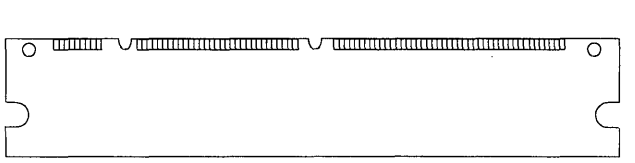
6. Burst stop command is valid at every burst length.

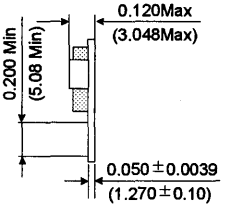
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

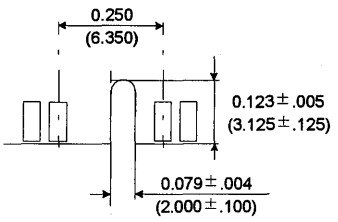
PACKAGE DIMENSIONS

Units : Inches (millimeters)

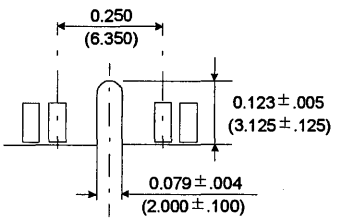




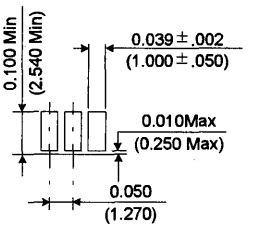




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4020AT

KMM366S424AT SDRAM DIMM

4Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S424AT is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S424AT consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S424AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S424AT-G8	125MHz (8ns)
KMM366S424AT-G0	100MHz (10ns)
KMM366S424AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, single sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

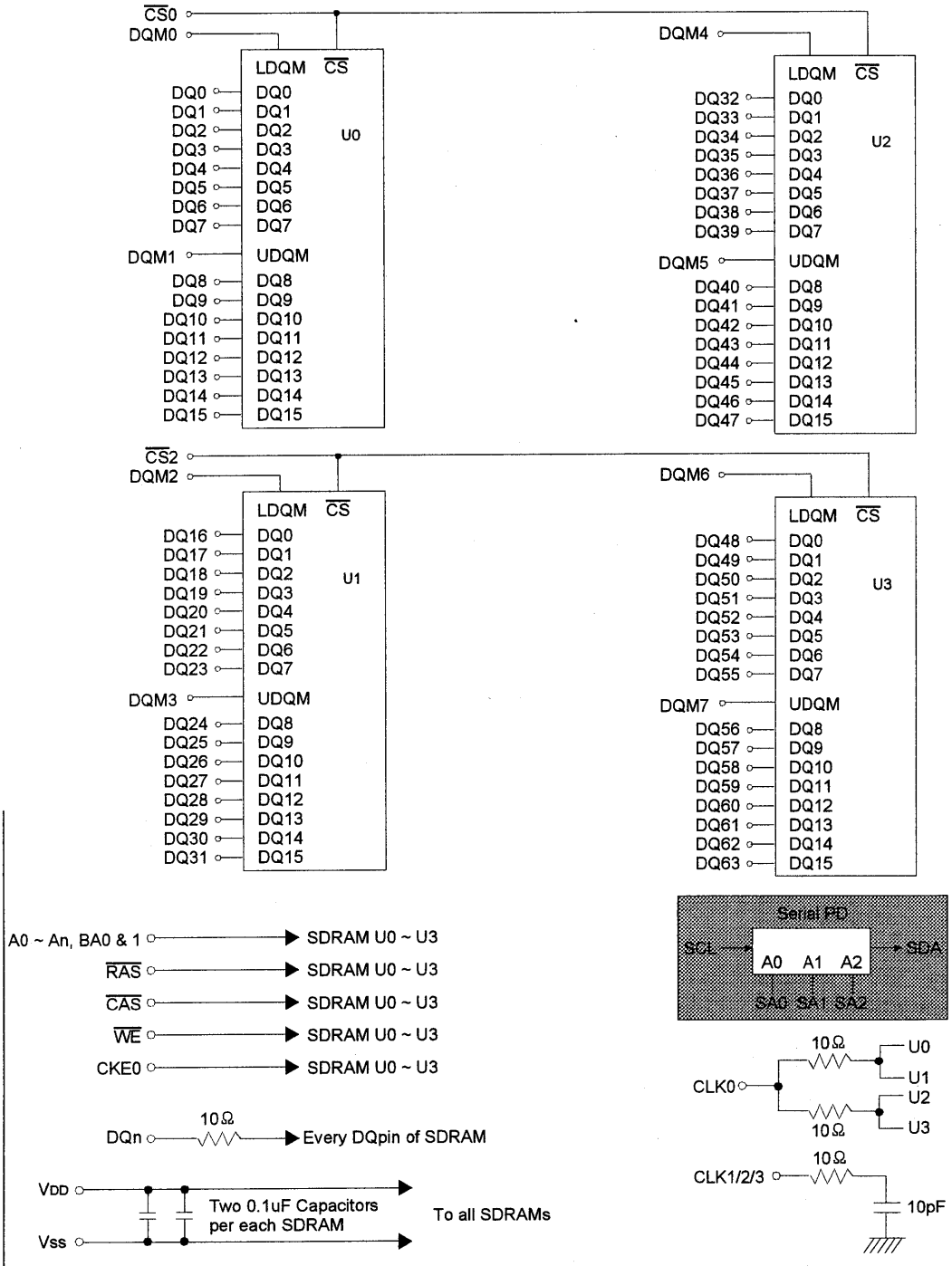
Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, tsHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

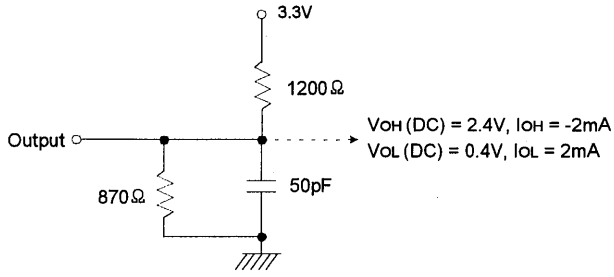
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	480	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		24				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		120			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	740	600	500	mA	1
			2	520	480	440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		720			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		6			mA	

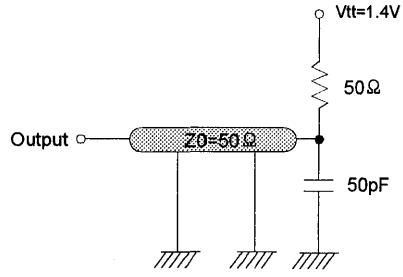
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S424AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S424AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S424AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

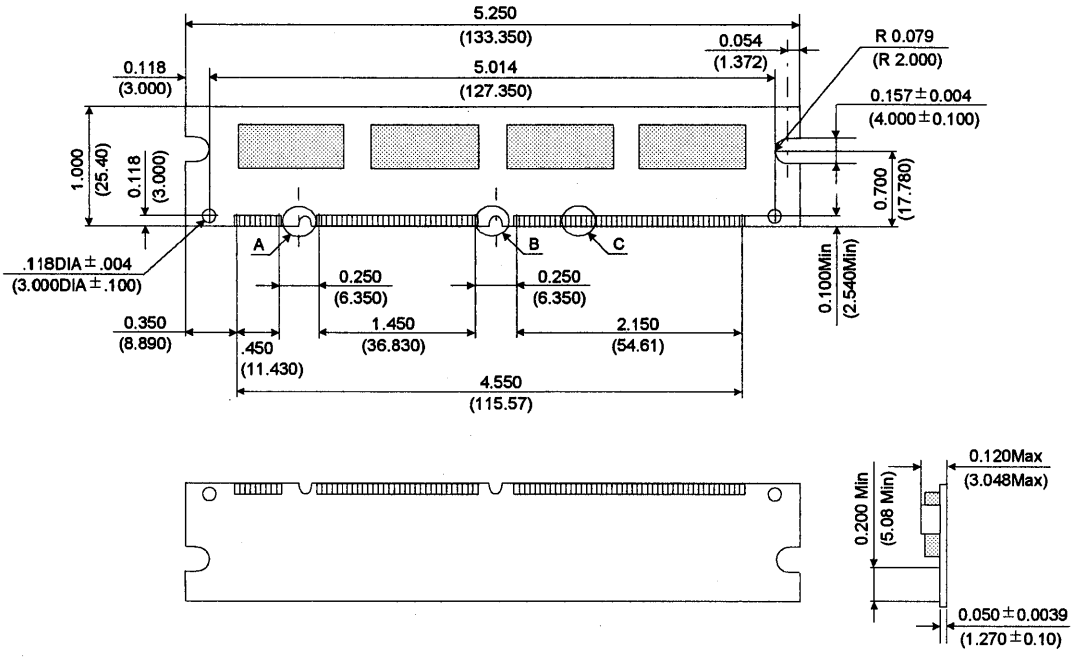
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

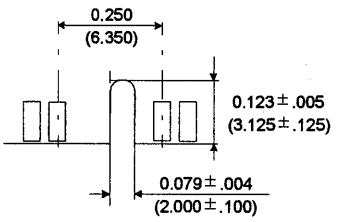
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

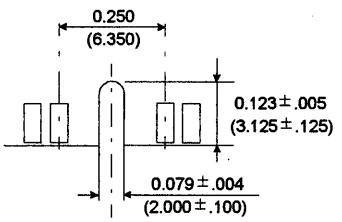
PACKAGE DIMENSIONS

Units : Inches (millimeters)

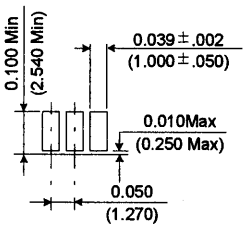




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4030AT

KMM366S803AT SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S803AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S803AT consists of eight CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S803AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S803AT-G8	125MHz (8ns)
KMM366S803AT-G0	100MHz (10ns)
KMM366S803AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

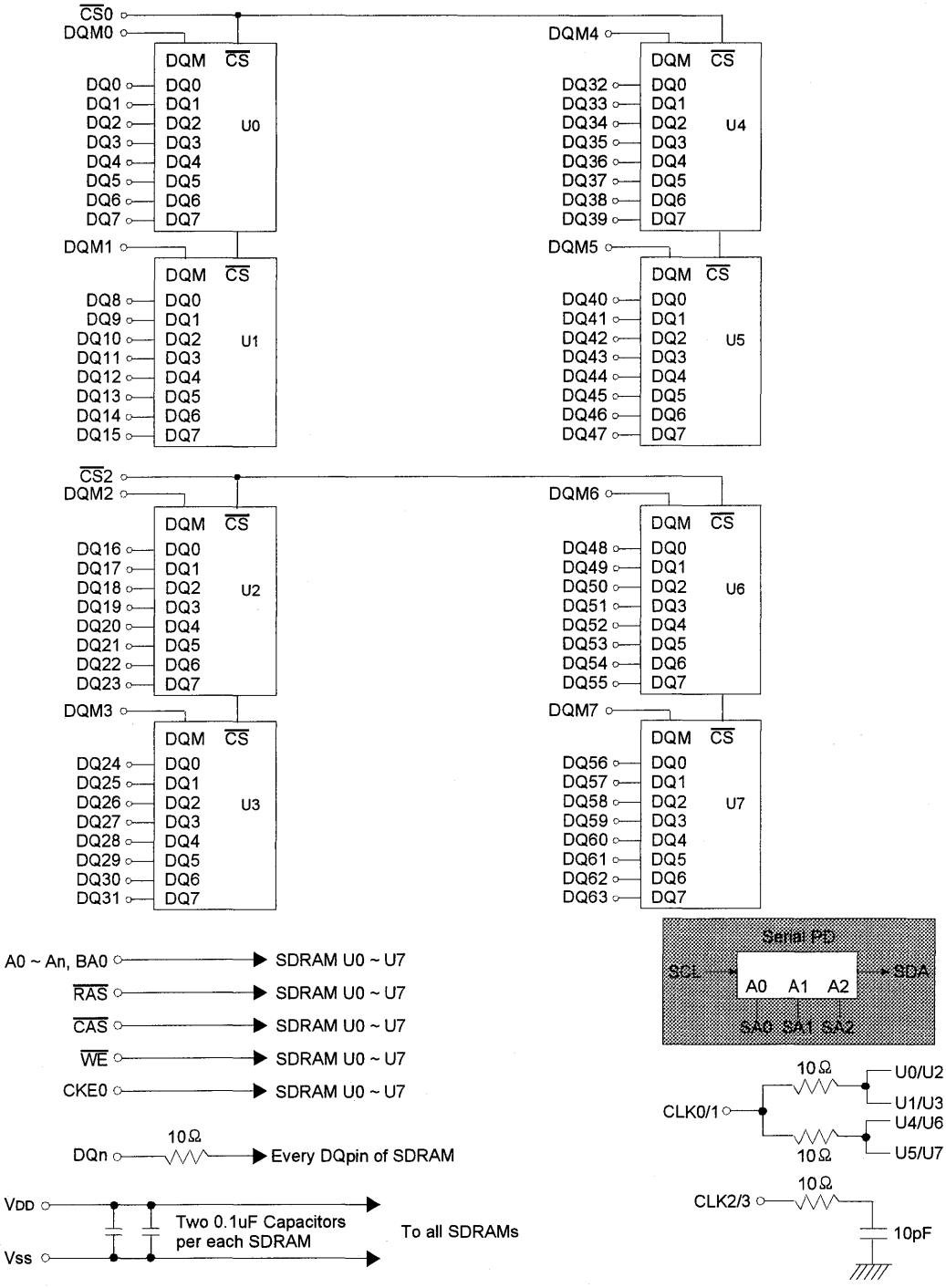
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

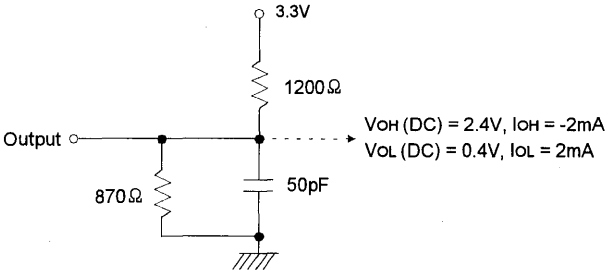
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		12			mA	

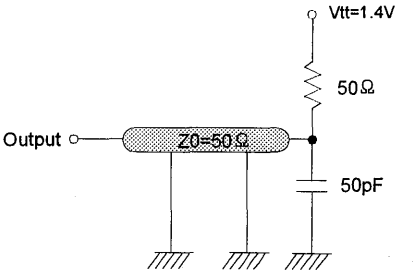
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S803AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S803AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S803AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

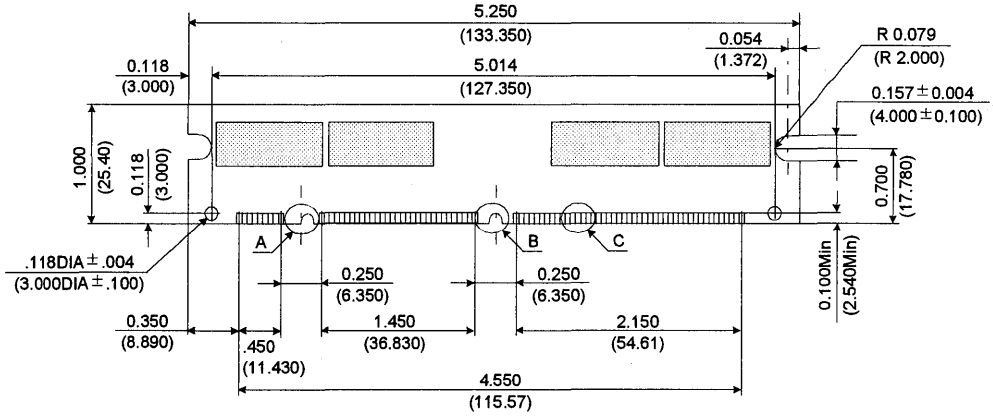
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

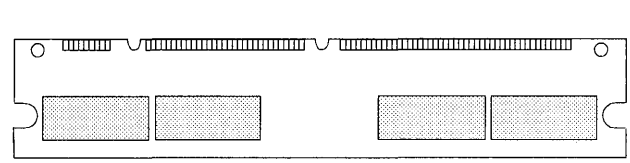
6. Burst stop command is valid at every burst length.

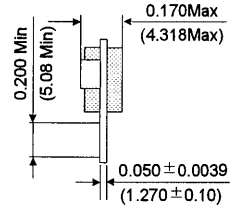
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

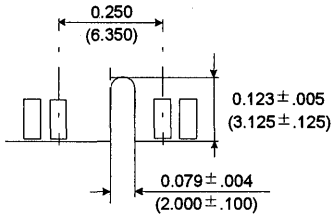
PACKAGE DIMENSIONS

Units : Inches (millimeters)

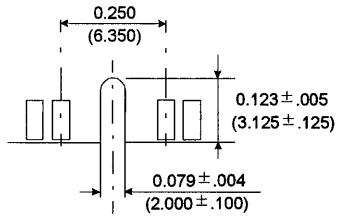




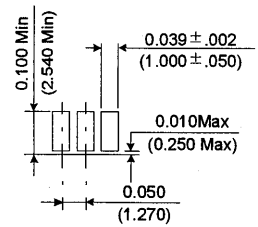




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM366S823AT SDRAM DIMM

8Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S823AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S823AT consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S823AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S823AT-G8	125MHz (8ns)
KMM366S823AT-G0	100MHz (10ns)
KMM366S823AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

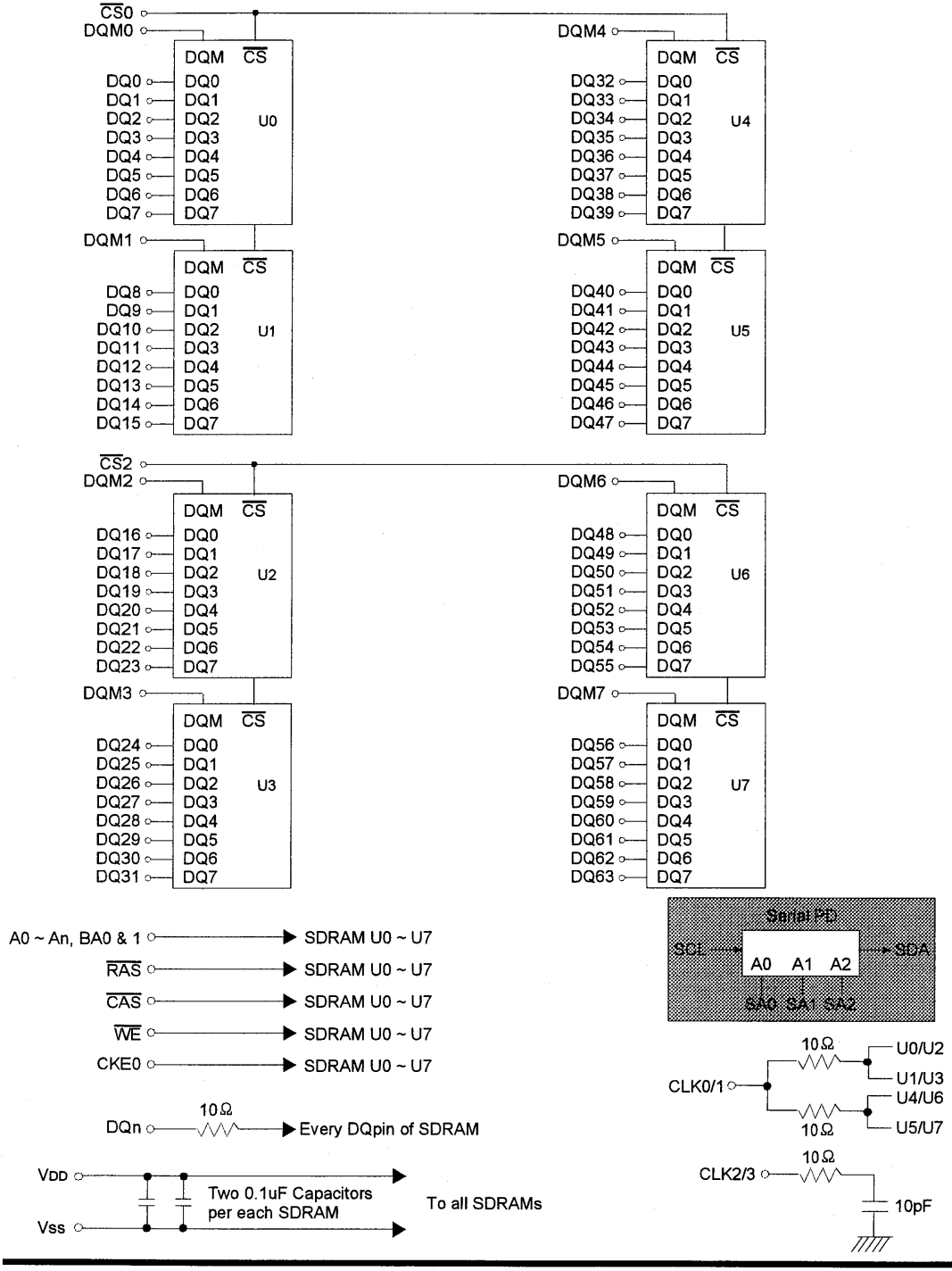
Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, tSHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

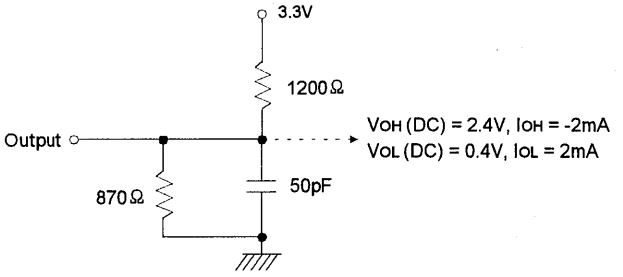
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		12			mA	

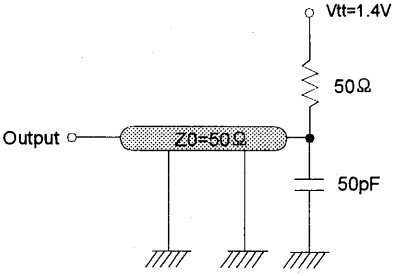
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S823AT- G8

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S823AT- G0

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S823AT- G2

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

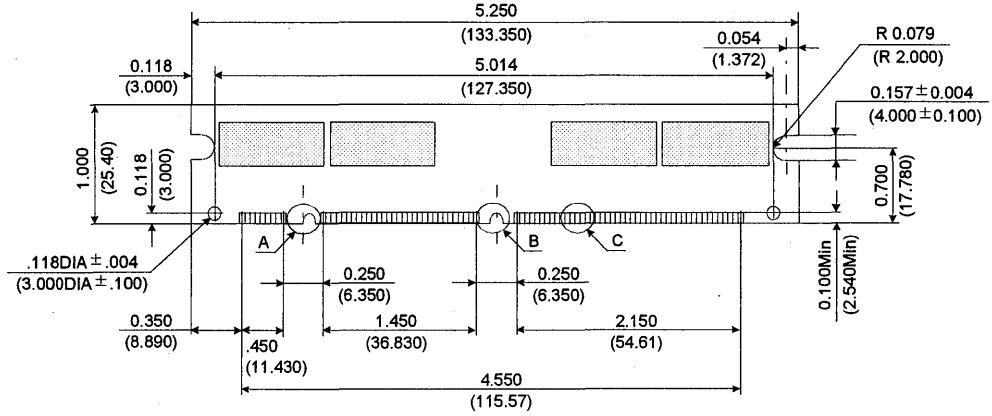
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

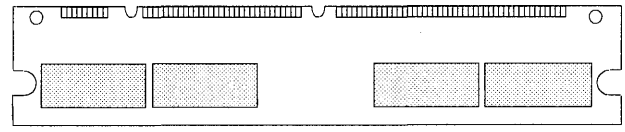
6. Burst stop command is valid at every burst length.

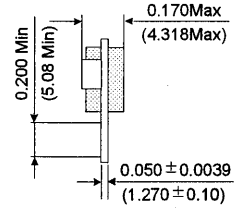
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

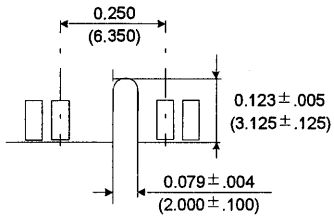
PACKAGE DIMENSIONS

Units : Inches (millimeters)

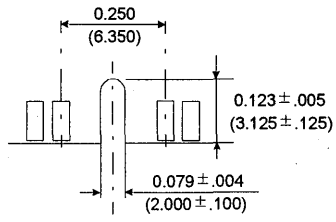




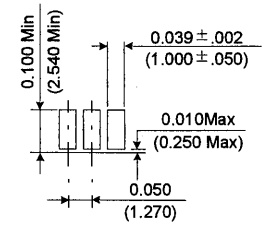




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

KMM366S804AT SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S804AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S804AT consists of eight CMOS 4M x 16 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S804AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S804AT-G8	125MHz (8ns)
KMM366S804AT-G0	100MHz (10ns)
KMM366S804AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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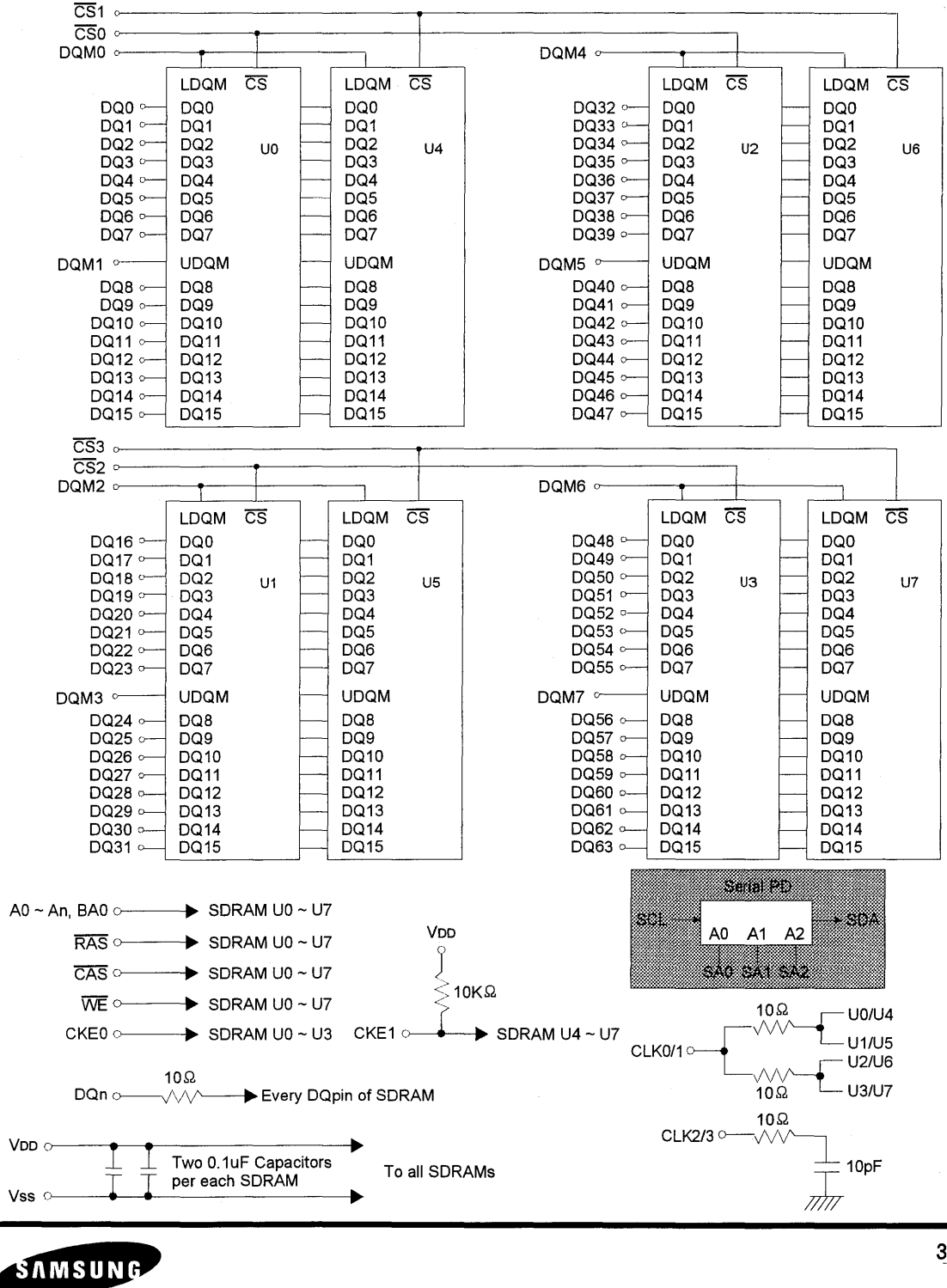
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

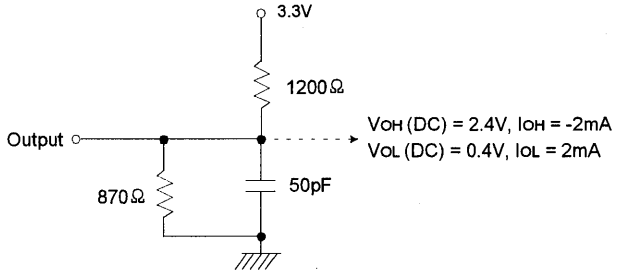
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		12			mA	

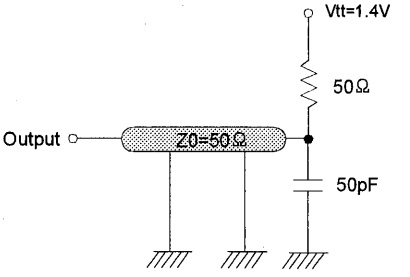
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S804AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S804AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S804AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

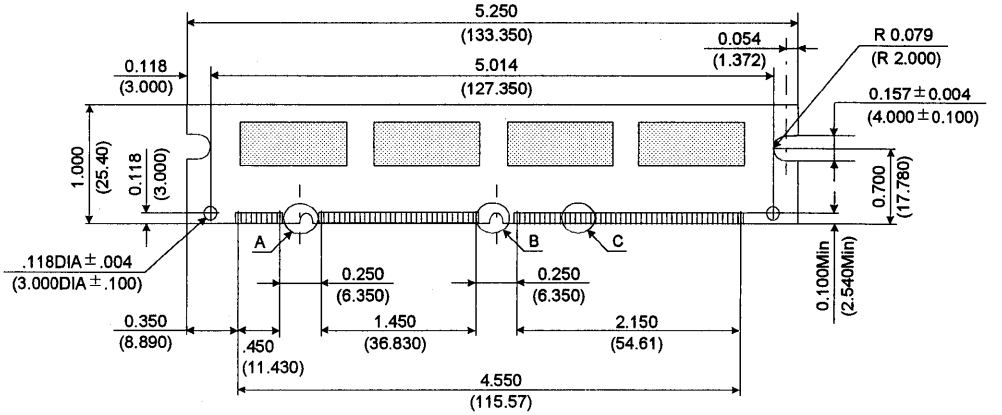
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

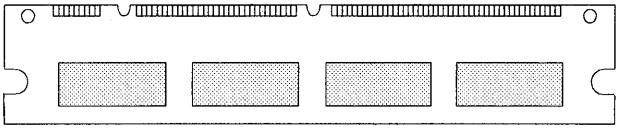
6. Burst stop command is valid at every burst length.

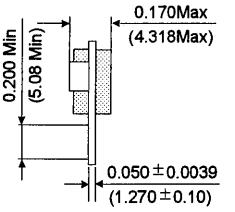
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

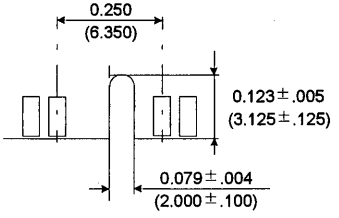
PACKAGE DIMENSIONS

Units : Inches (millimeters)

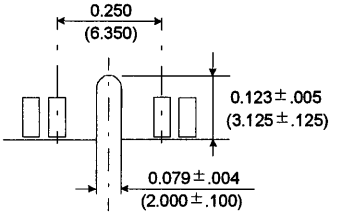




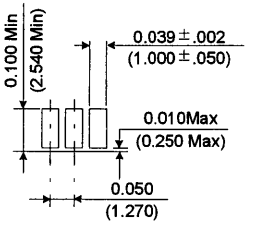




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4020AT

KMM366S824AT SDRAM DIMM

8Mx64 SDRAM DIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S824AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S824AT consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S824AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S824AT-G8	125MHz (8ns)
KMM366S824AT-G0	100MHz (10ns)
KMM366S824AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

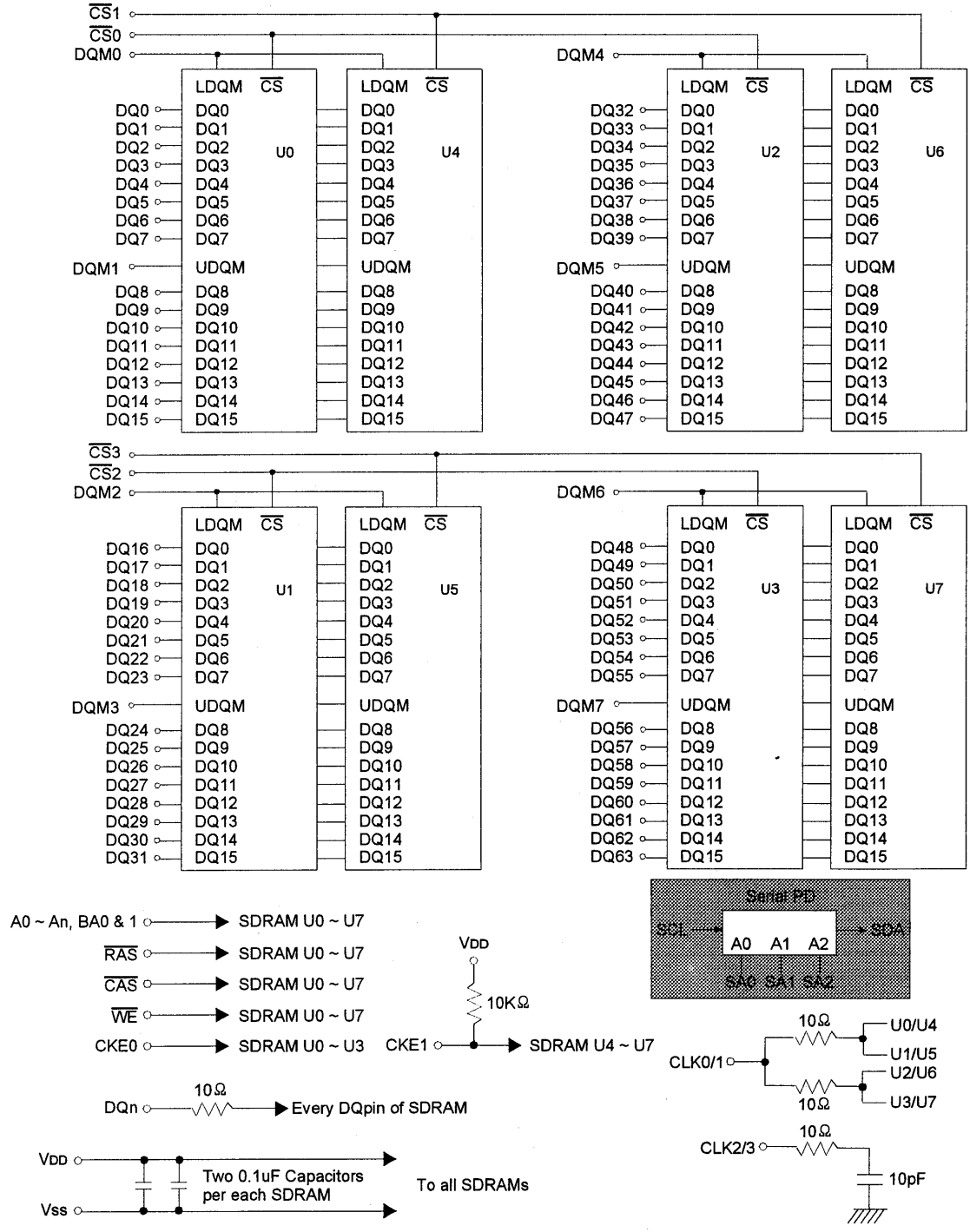
Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS}$0 ~ $\overline{CS}$3)	C_{IN5}	-	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

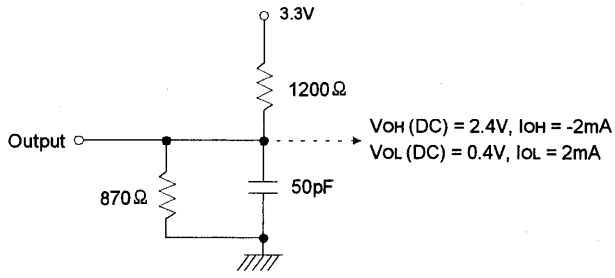
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		12			mA	

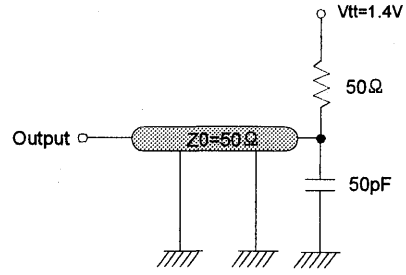
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S824AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S824AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S824AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

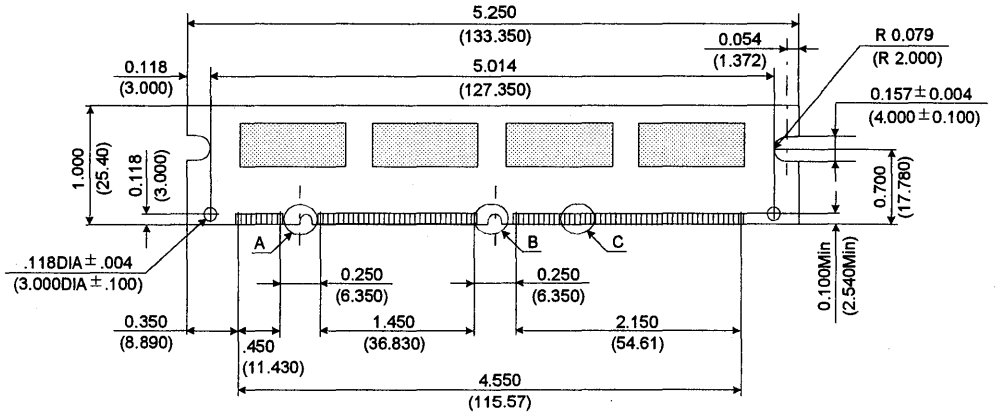
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

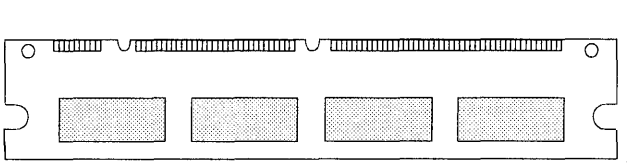
6. Burst stop command is valid at every burst length.

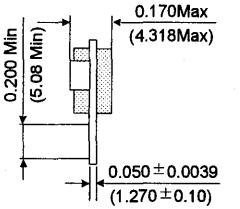
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

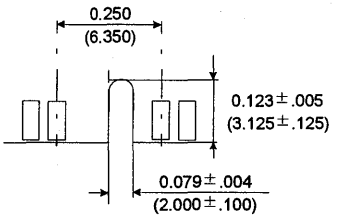
PACKAGE DIMENSIONS

Units : Inches (millimeters)

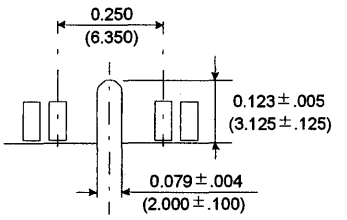




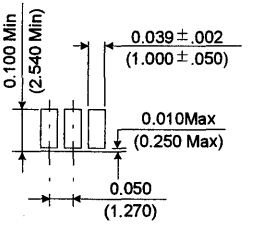




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4030AT

KMM366S1600AT SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx4, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S1600AT is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S1600AT consists of sixteen CMOS 16M x 4 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S1600AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S1600AT-G8	125MHz (8ns)
KMM366S1600AT-G0	100MHz (10ns)
KMM366S1600AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

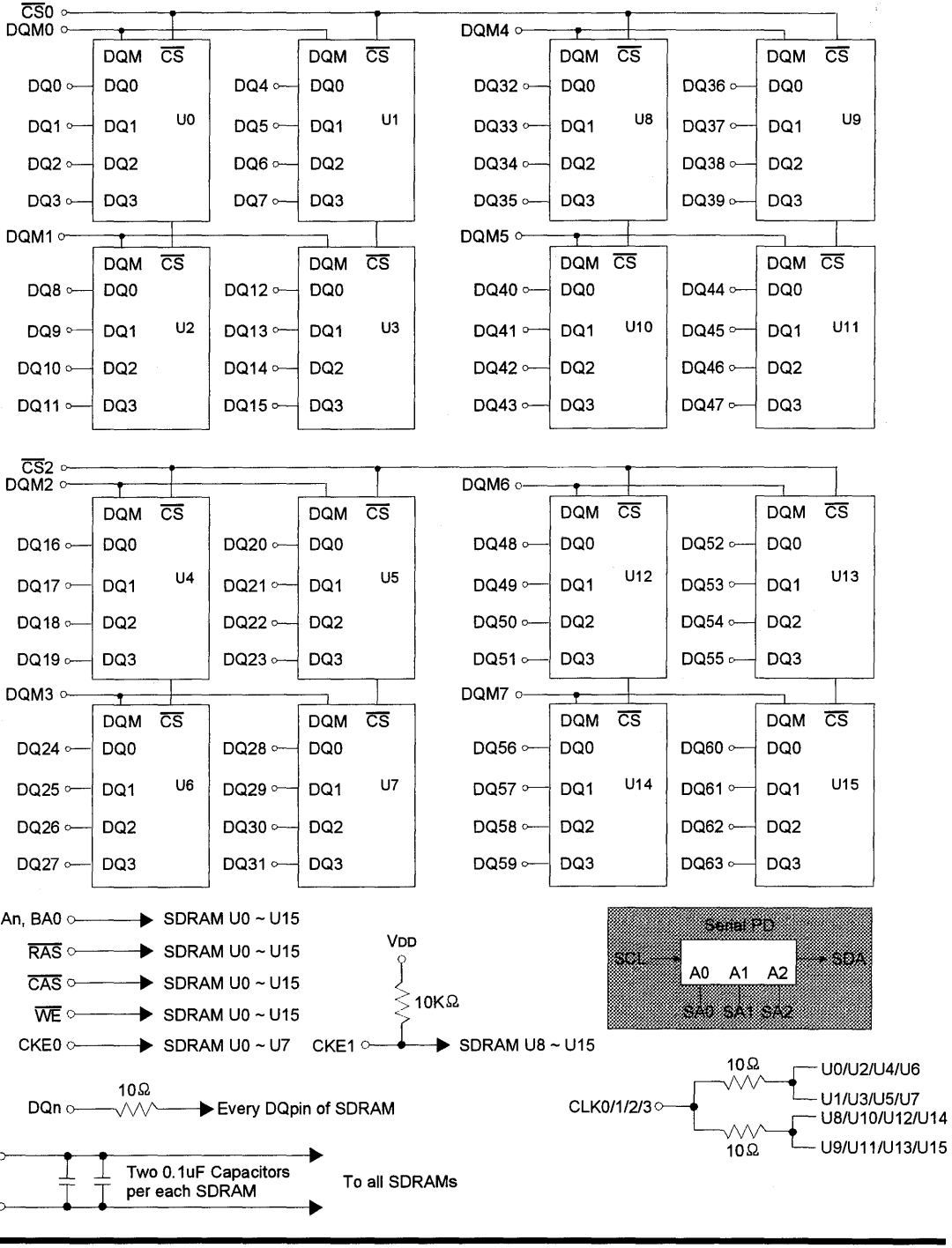
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA9
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

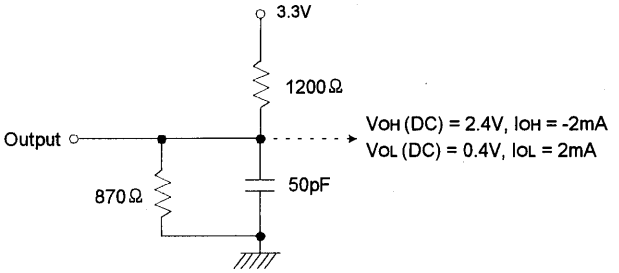
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,920	1,680	1,440	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		32			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		480			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		96			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		96				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		640			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		400			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	2,560	2,000	1,760	mA	1
			2	1,760	1,600	1,440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,880			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24			mA	

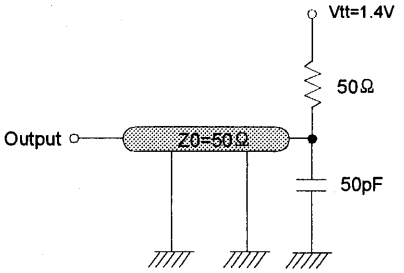
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S1600AT- G8

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S1600AT- G0

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S1600AT- G2

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

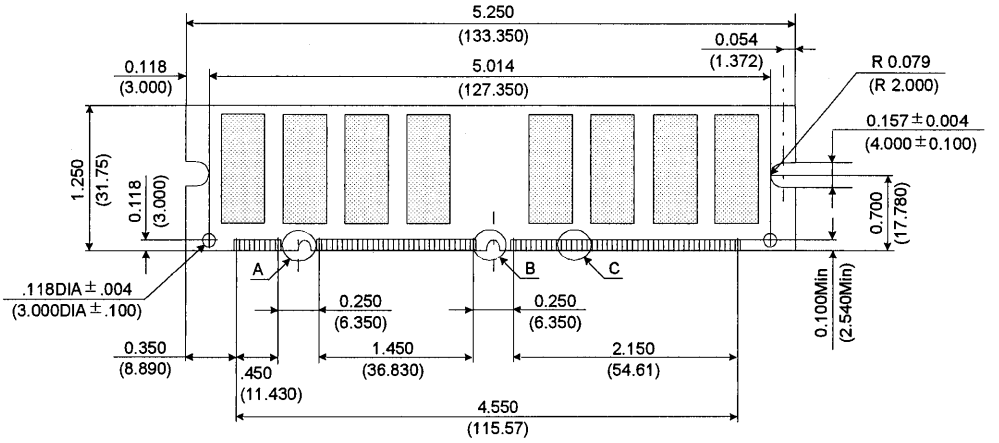
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

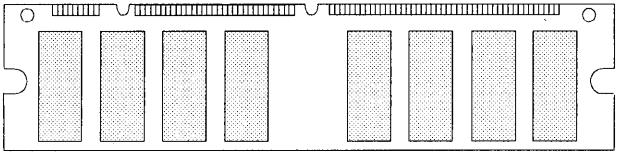
6. Burst stop command is valid at every burst length.

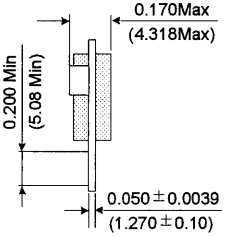
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

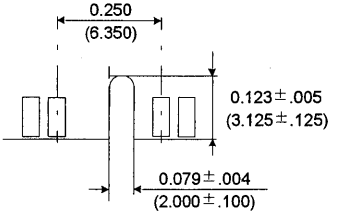
PACKAGE DIMENSIONS

Units : Inches (millimeters)

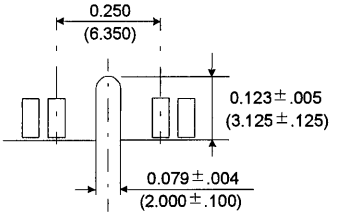




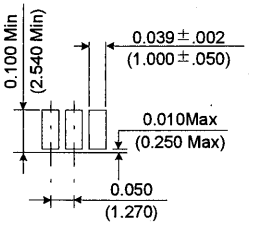




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S16020AT

KMM366S1620AT SDRAM DIMM

16Mx64 SDRAM DIMM based on 16Mx4, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S1620AT is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S1620AT consists of sixteen CMOS 16M x 4 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S1620AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S1620AT-G8	125MHz (8ns)
KMM366S1620AT-G0	100MHz (10ns)
KMM366S1620AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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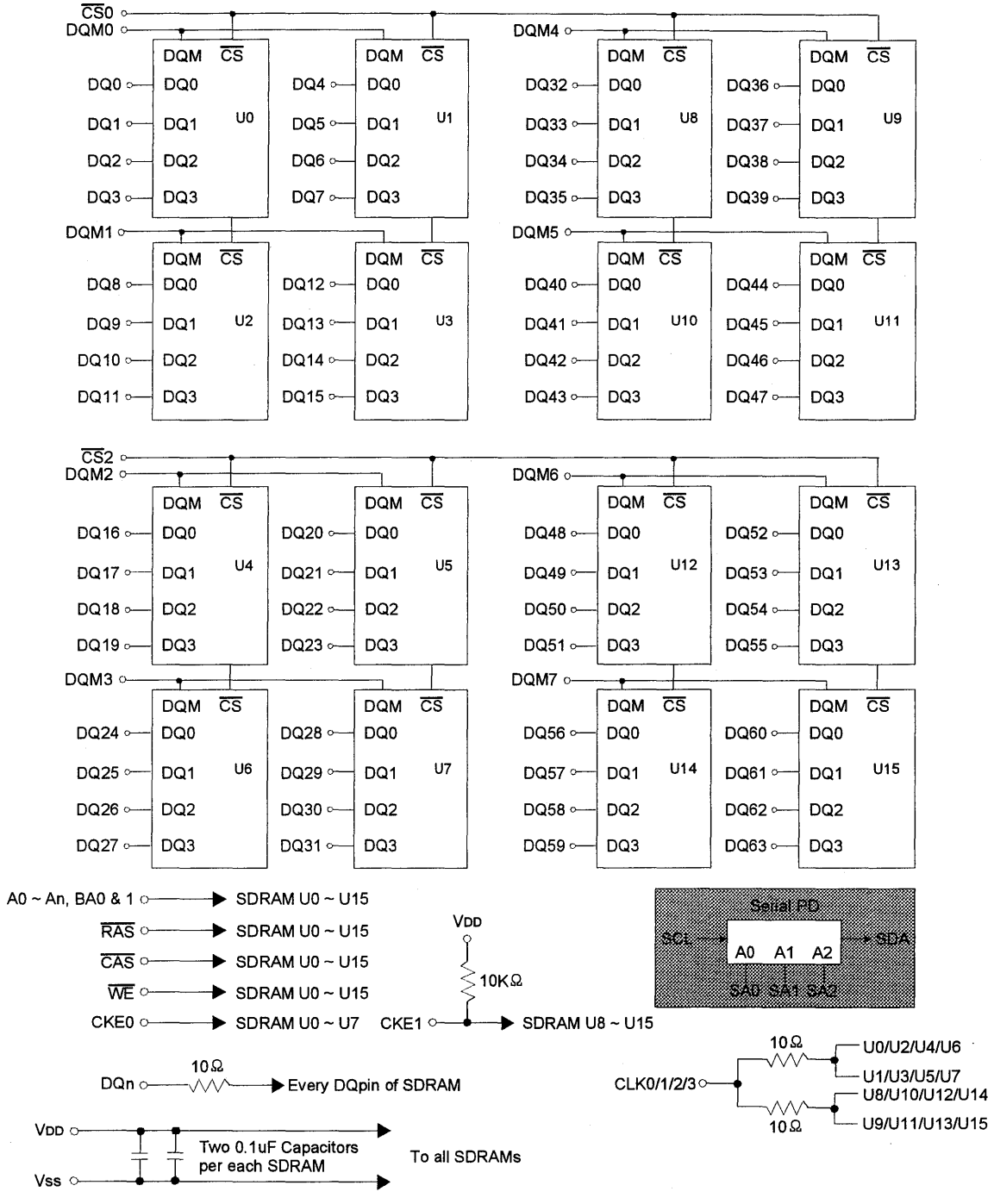
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA9
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, tSHZ after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

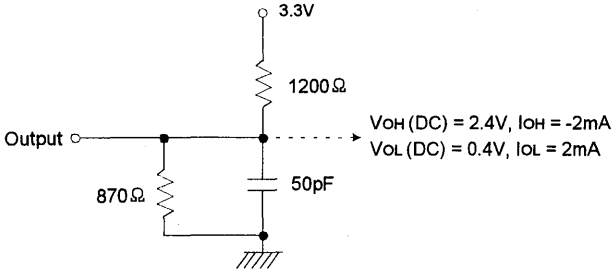
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,920	1,680	1,440	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		32			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		480			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		96			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		96				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		640			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		400			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	2,560	2,000	1,760	mA	1
			2	1,760	1,600	1,440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,880			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24			mA	

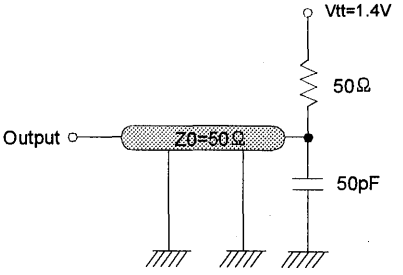
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S1620AT- G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S1620AT- G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S1620AT- G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don' t Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

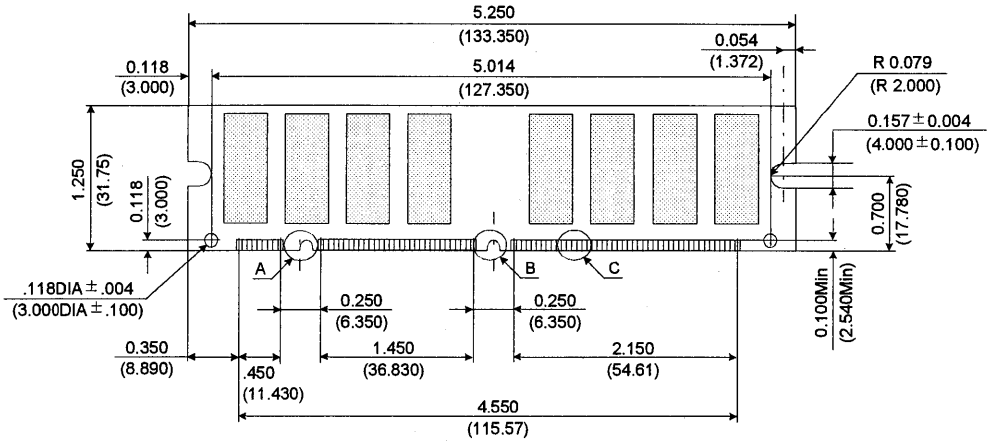
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

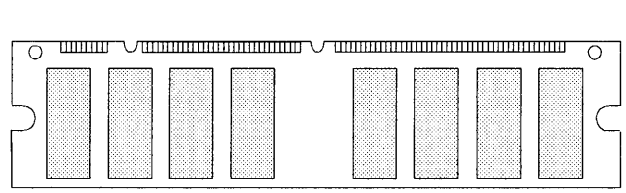
6. Burst stop command is valid at every burst length.

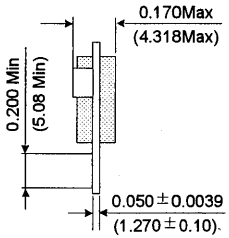
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

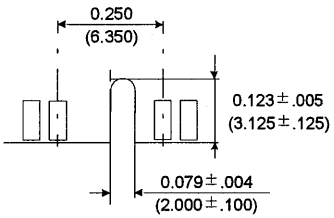
PACKAGE DIMENSIONS

Units : Inches (millimeters)

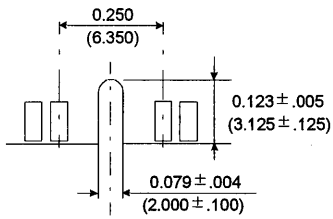




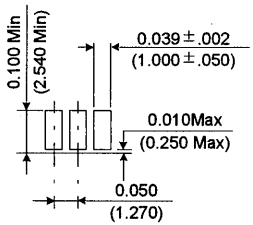




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S16030AT

KMM366S1603AT SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S1603AT is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S1603AT consists of sixteen CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S1603AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S1603AT-G8	125MHz (8ns)
KMM366S1603AT-G0	100MHz (10ns)
KMM366S1603AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

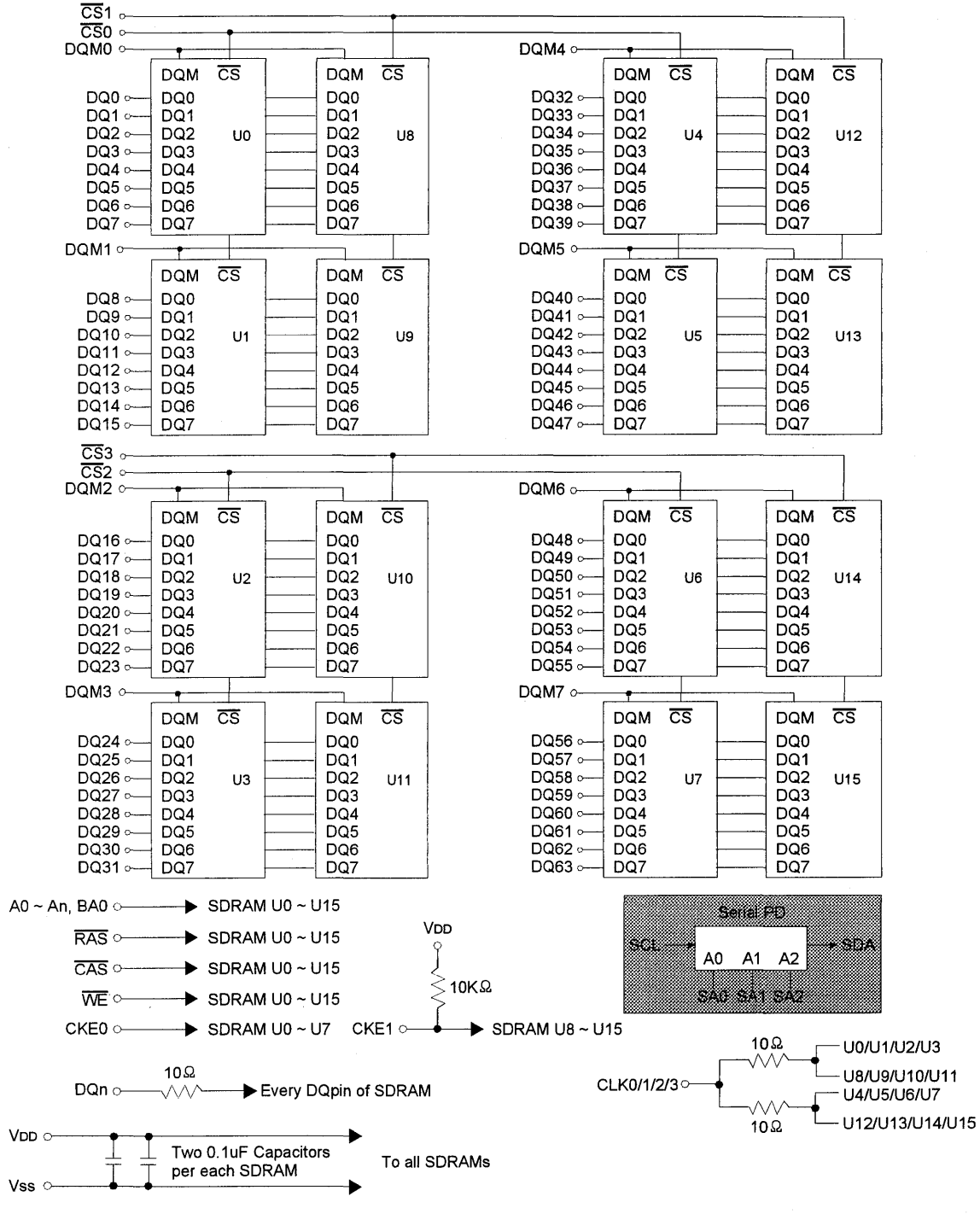
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

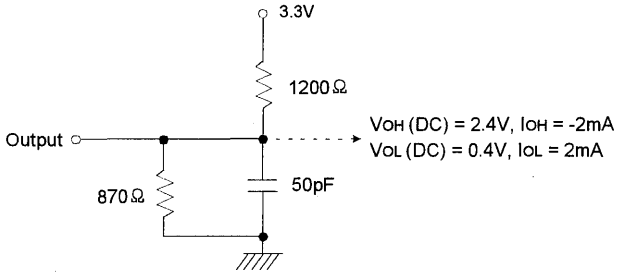
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,240	1,120	960	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		32			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		480			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		96			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		96				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		640			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		400			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,600	1,320	1,160	mA	1
			2	1,160	1,080	1,000		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,880			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24			mA	

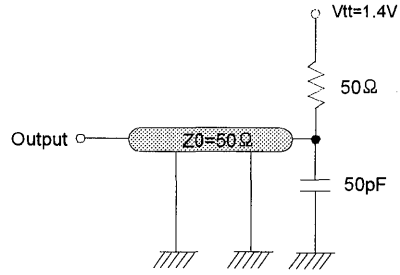
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S1603AT- G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S1603AT- G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S1603AT- G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

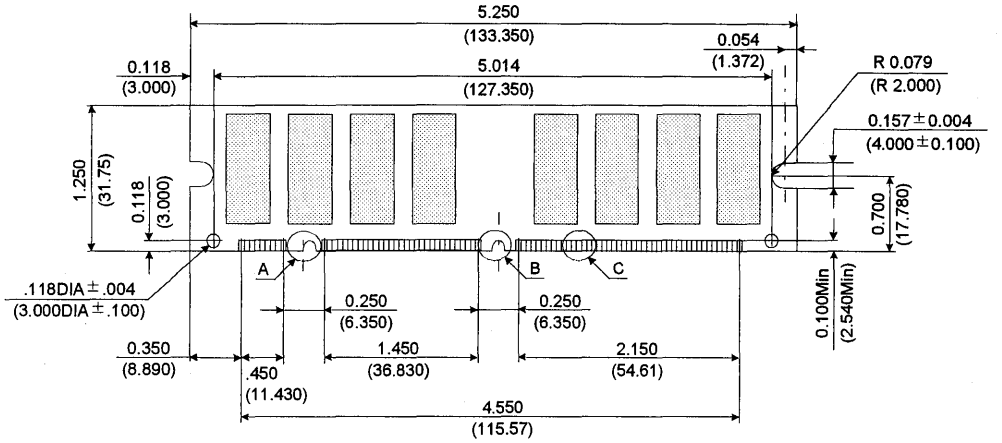
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0	A10/AP	A12 ~ A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

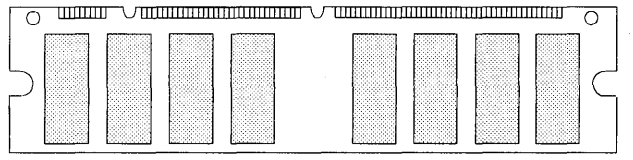
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

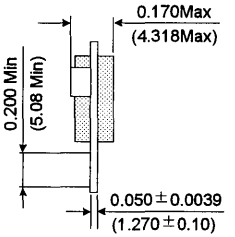
Note : 1. OP Code : Operand Code
A0 ~ A12, BA0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A10/AP is "High" at row precharge, BA0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

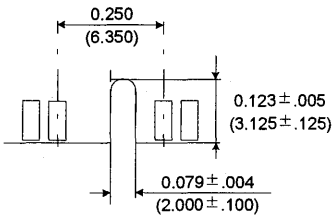
PACKAGE DIMENSIONS

Units : Inches (millimeters)

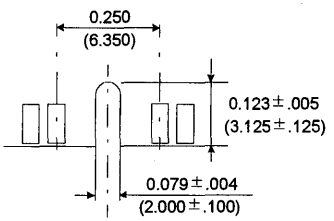




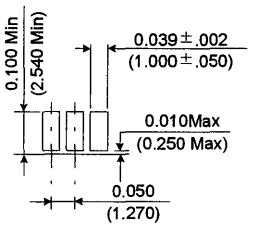




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM366S1623AT SDRAM DIMM

16Mx64 SDRAM DIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM366S1623AT is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM366S1623AT consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM366S1623AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM366S1623AT-G8	125MHz (8ns)
KMM366S1623AT-G0	100MHz (10ns)
KMM366S1623AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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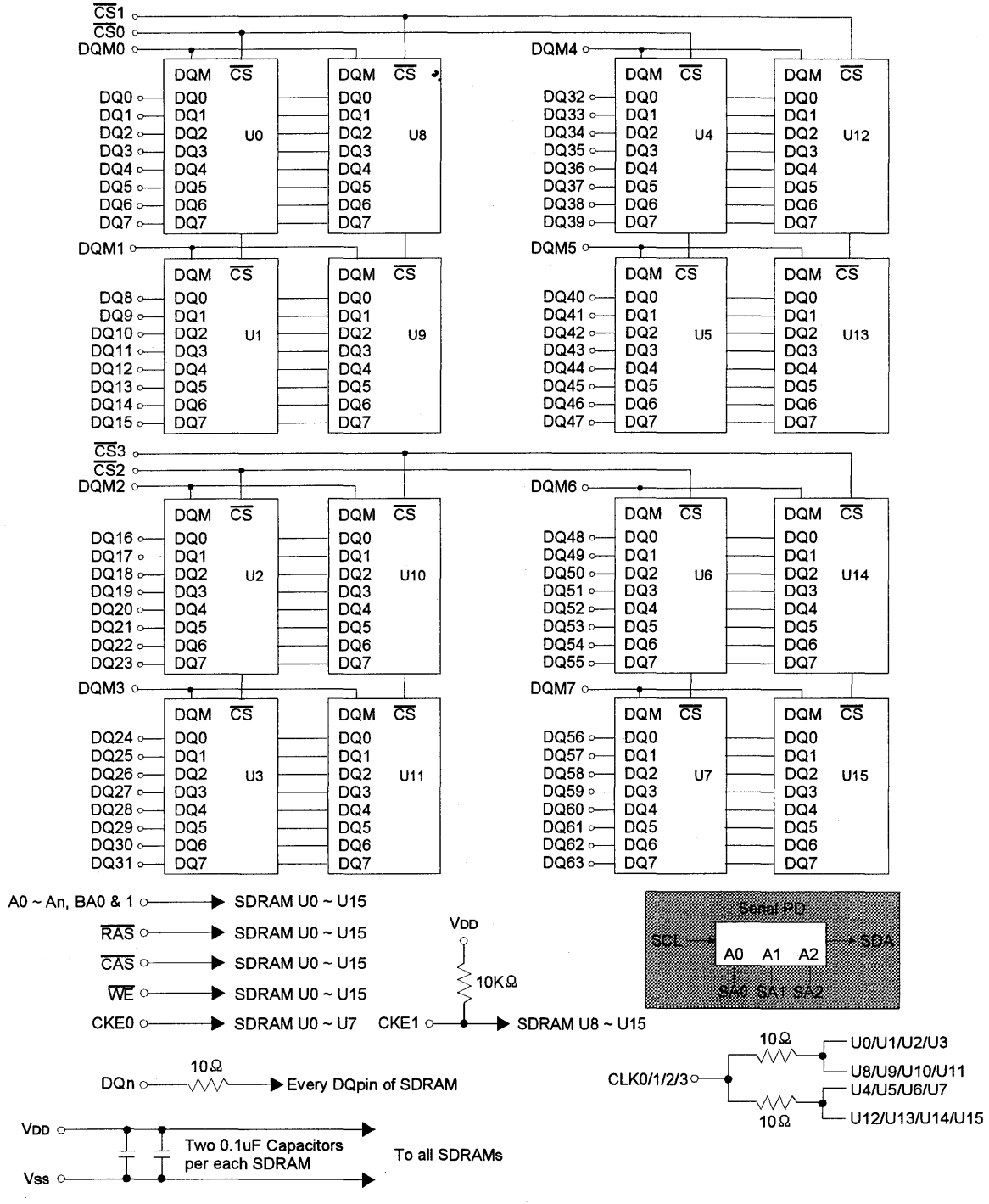
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	Ios	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-80	-	80	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	90	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS}$0 ~ $\overline{CS}$3)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

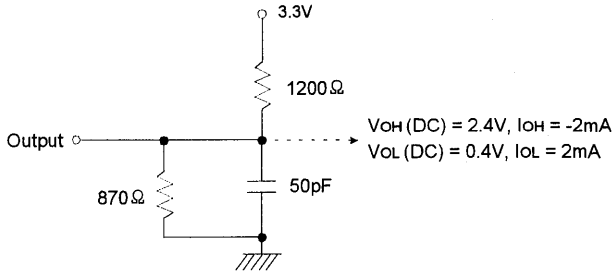
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,240	1,020	960	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		32			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		32				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		480			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		320				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		96			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		96				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		640			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		400			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,600	1,320	1,160	mA	1
			2	1,160	1,080	1,000		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		2,880			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		24			mA	

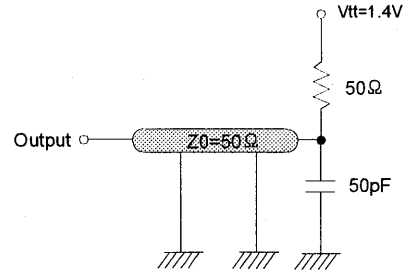
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM366S1623AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM366S1623AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM366S1623AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

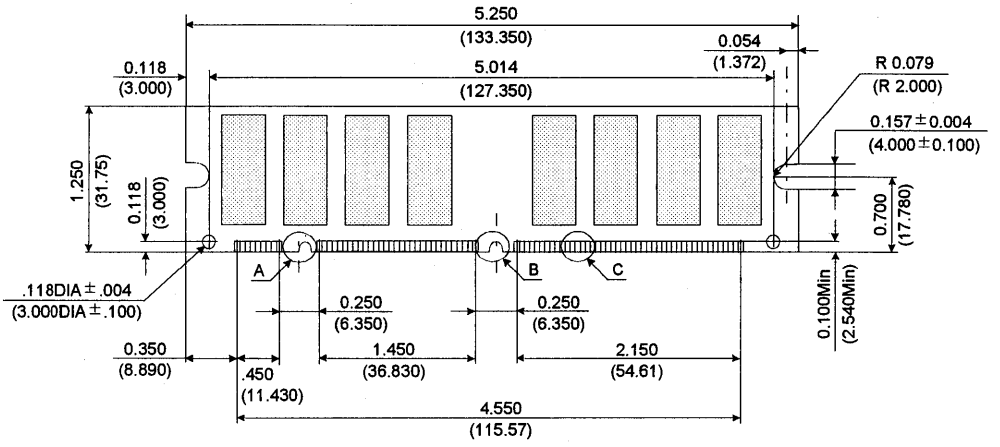
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

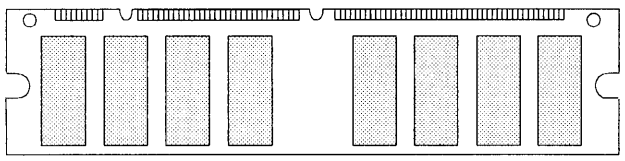
6. Burst stop command is valid at every burst length.

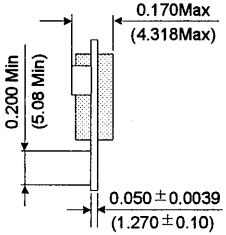
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

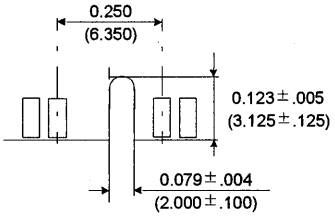
PACKAGE DIMENSIONS

Units : Inches (millimeters)

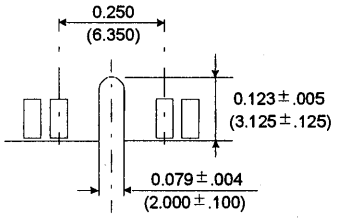




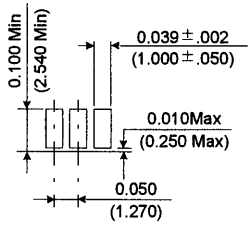




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

KMM374S803AT SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S803AT is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S803AT consists of nine CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S803AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S803AT-G8	125MHz (8ns)
KMM374S803AT-G0	100MHz (10ns)
KMM374S803AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

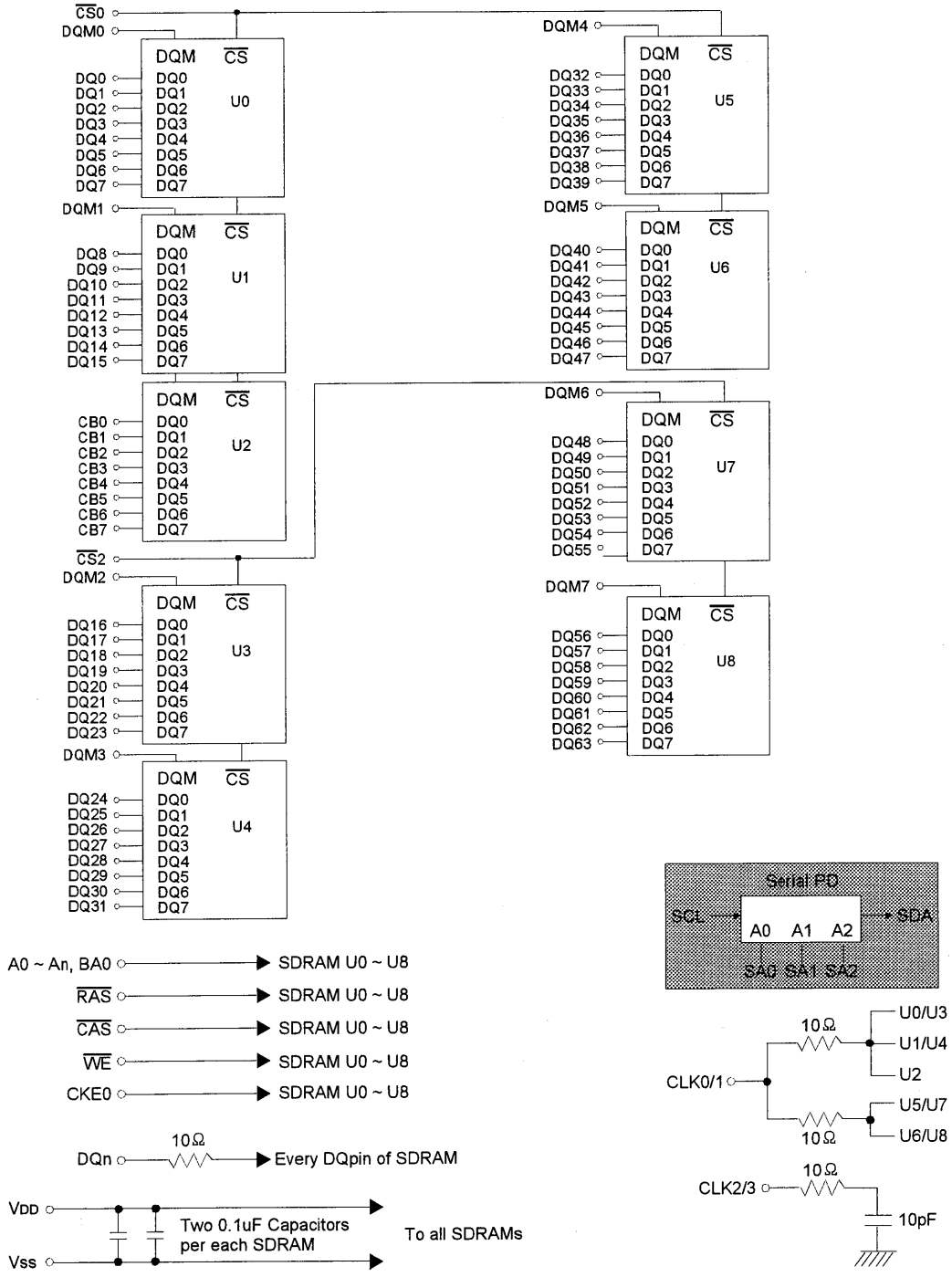
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check bit (data-in / data-out)
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-45	-	45	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	60	pF
Input capacitance (CKE0)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

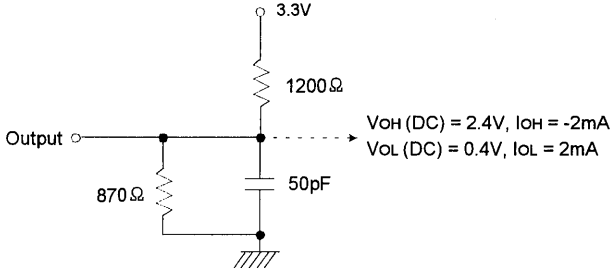
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,125	990	810	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		18			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		18				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		270			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		180				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		54			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		54				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		225			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,530	1,215	1,035	mA	1
			2	1,035	945	855		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,620			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		13.5			mA	

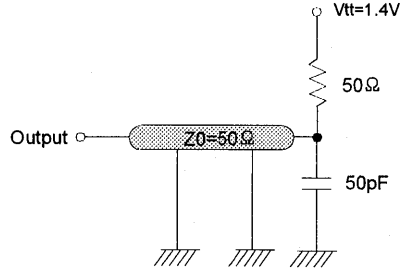
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S803AT- G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S803AT- G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S803AT- G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

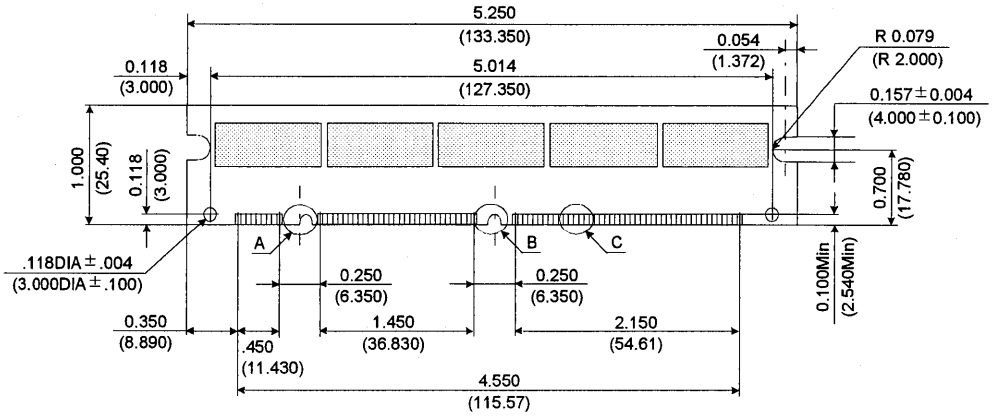
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

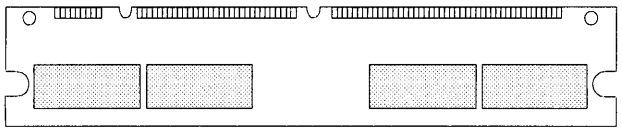
6. Burst stop command is valid at every burst length.

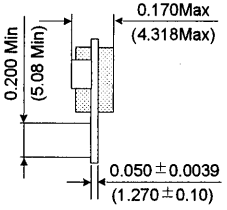
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

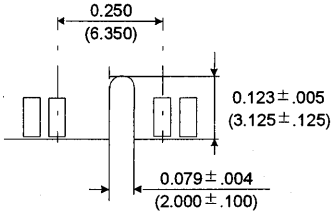
PACKAGE DIMENSIONS

Units : Inches (millimeters)

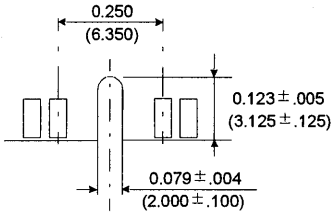




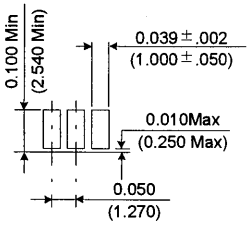




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM374S823AT SDRAM DIMM

8Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S823AT is a 8M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S823AT consists of nine CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S823AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S823AT-G8	125MHz (8ns)
KMM374S823AT-G0	100MHz (10ns)
KMM374S823AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

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PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check bit (data-in / data-out)
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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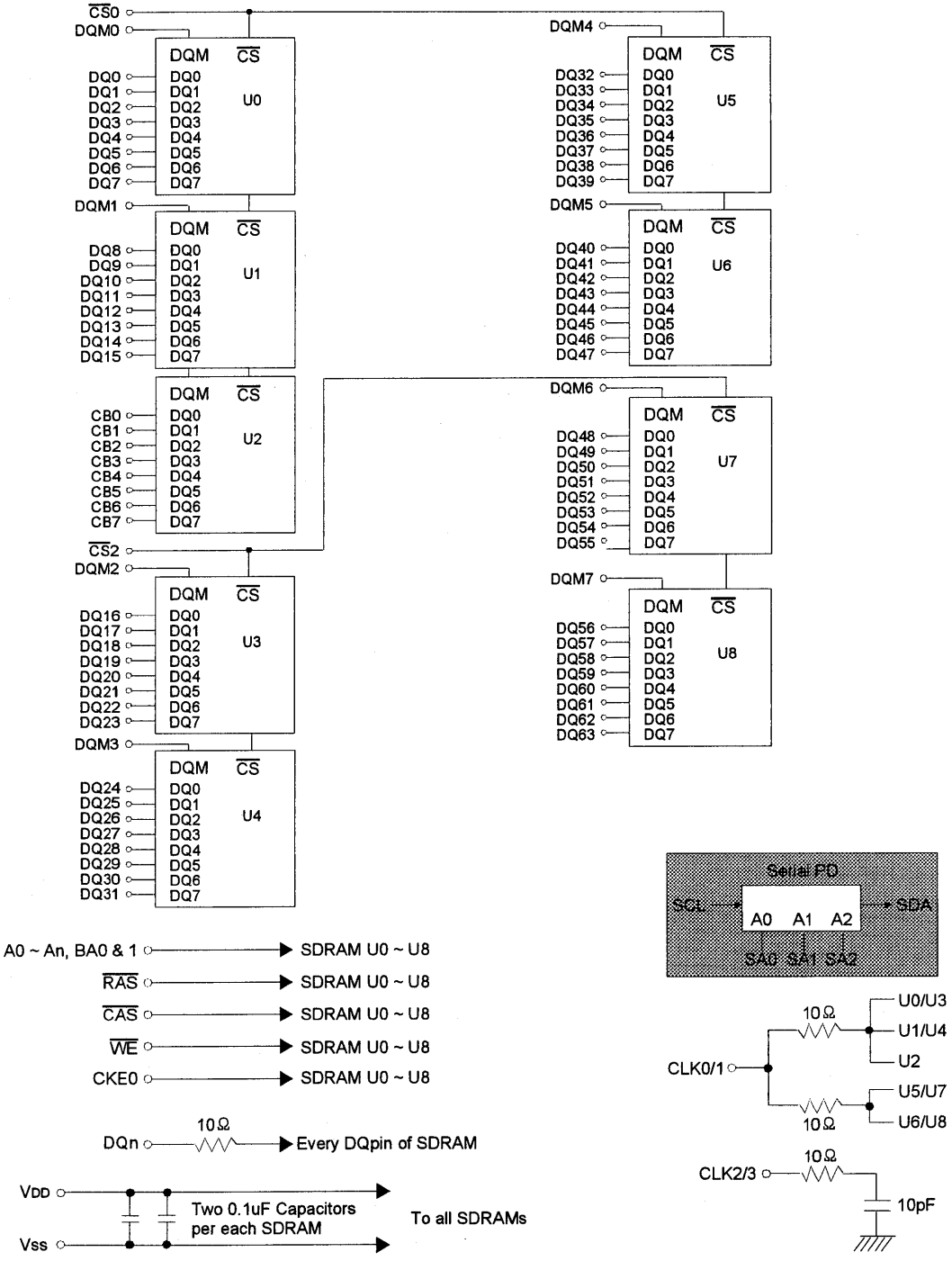
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-45	-	45	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	60	pF
Input capacitance (CKE0)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

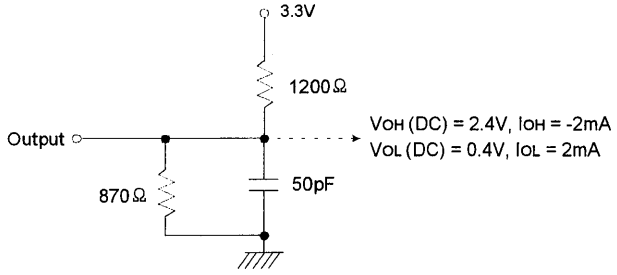
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,125	990	810	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		18			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		18				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		270			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		180				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		54			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		54				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		225			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,530	1,215	1,035	mA	1
			2	1,035	945	855		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,620			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		13.5			mA	

Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

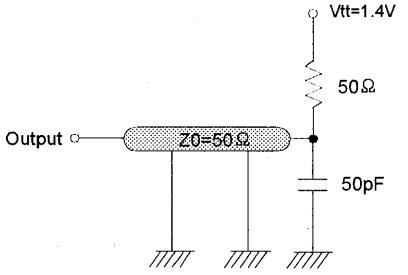
3

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S823AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S823AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S823AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

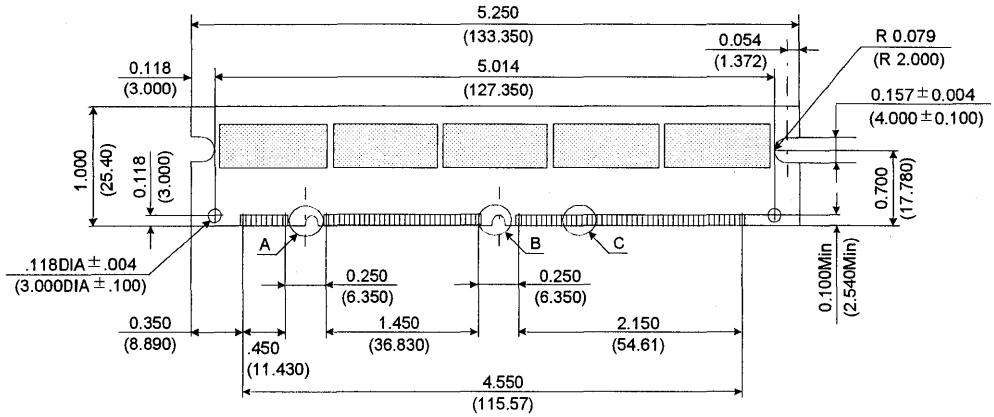
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

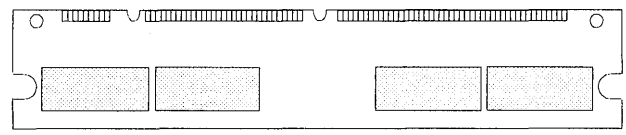
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

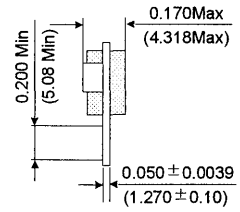
Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

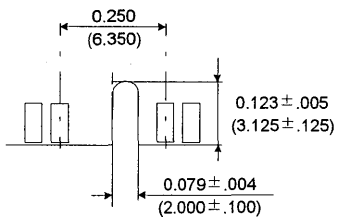
PACKAGE DIMENSIONS

Units : Inches (millimeters)

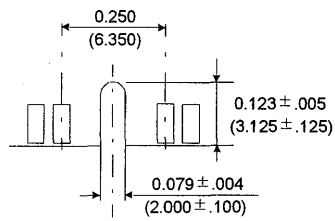




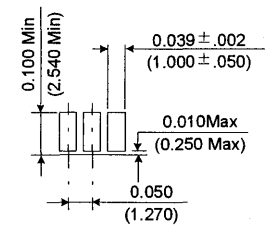




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

KMM374S1600AT SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx4, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S1600AT is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S1600AT consists of eighteen CMOS 16M x 4 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S1600AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S1600AT-G8	125MHz (8ns)
KMM374S1600AT-G0	100MHz (10ns)
KMM374S1600AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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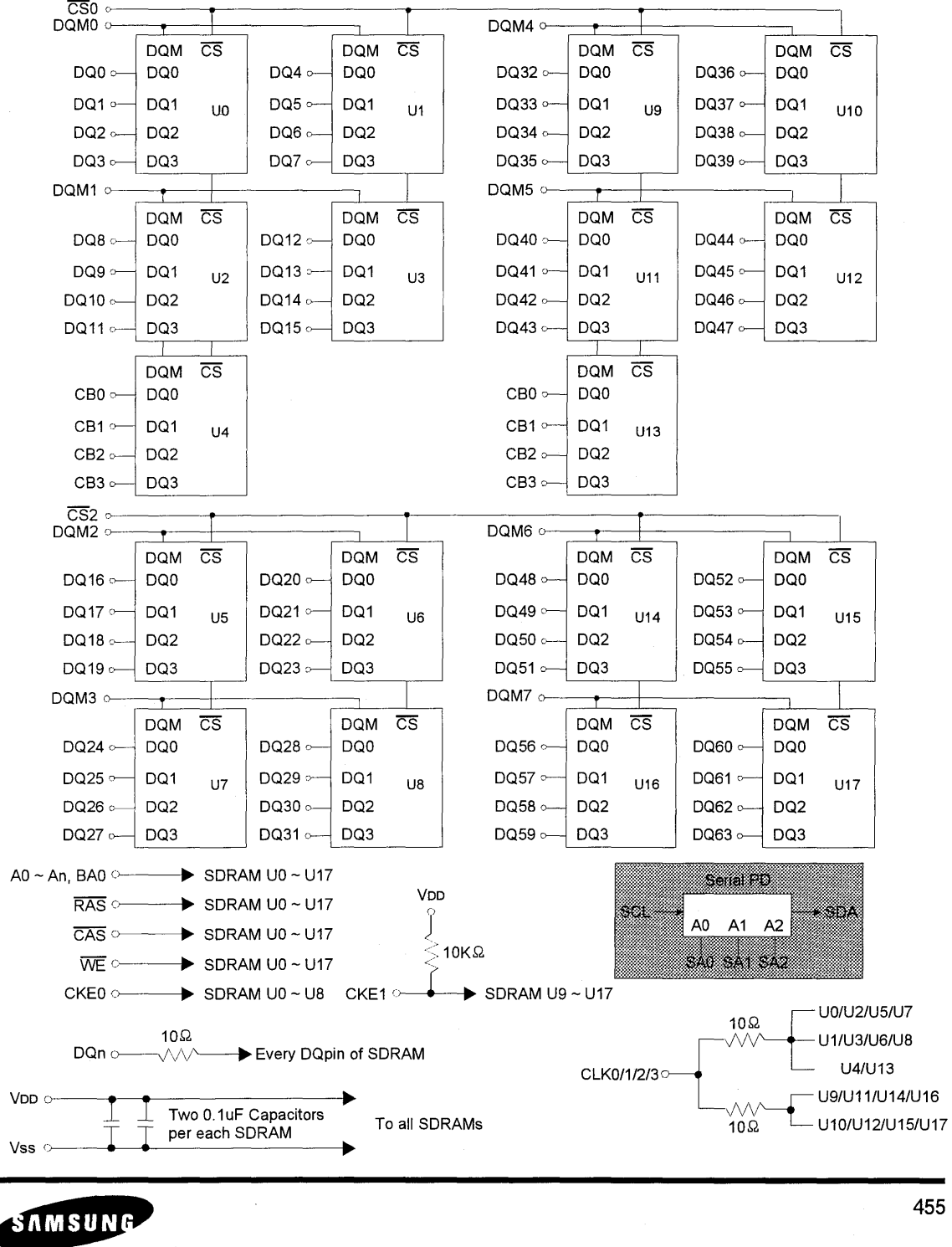
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA9
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	65	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	30	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

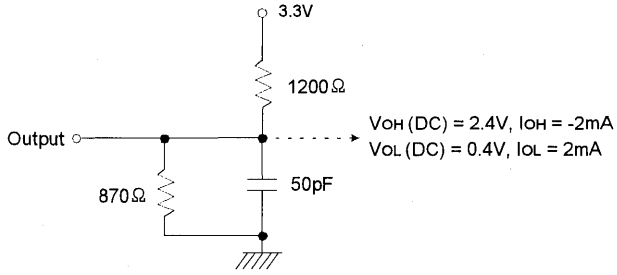
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		2,160	1,890	1,620	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		36			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		36				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		540			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		360				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		108			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		108				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		720			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		450			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	2,880	2,250	1,980	mA	1
			2	1,980	1,800	1,620		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		3,240			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		27			mA	

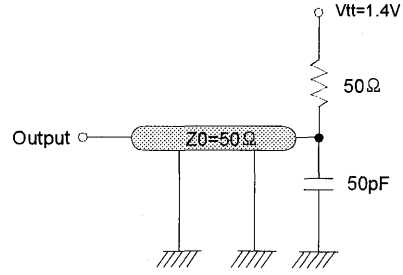
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S1600AT- G8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S1600AT- G0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S1600AT- G2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

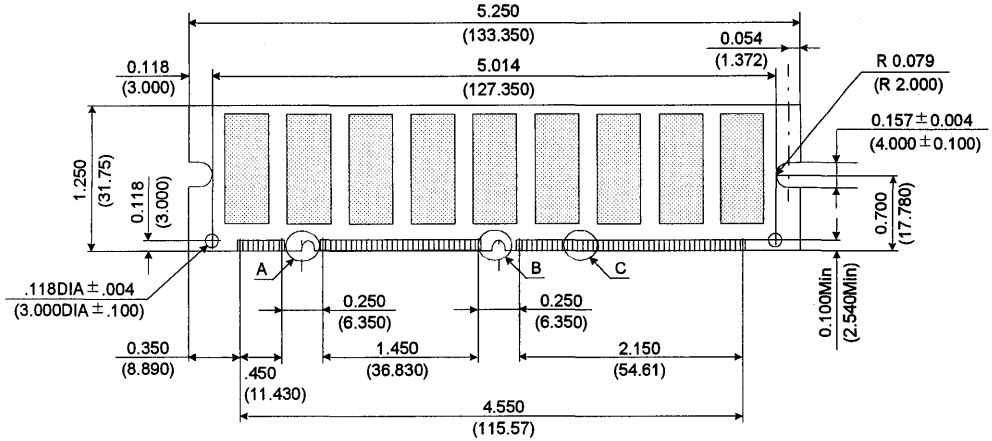
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

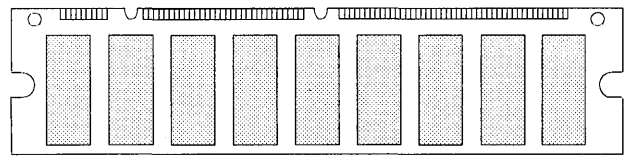
6. Burst stop command is valid at every burst length.

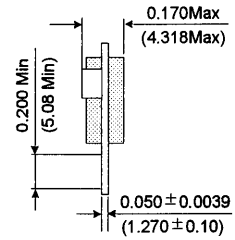
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

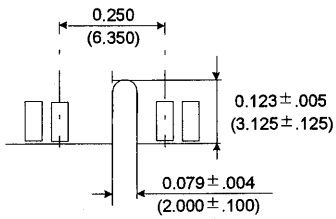
PACKAGE DIMENSIONS

Units : Inches (millimeters)

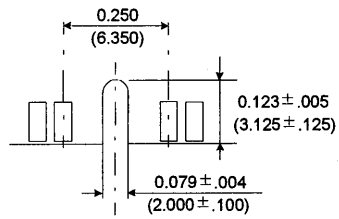




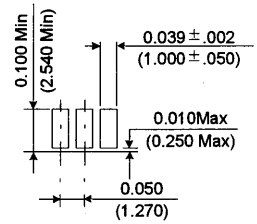




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S16020AT

KMM374S1620AT SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 16Mx4, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S1620AT is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S1620AT consists of eighteen CMOS 16M x 4 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S1620AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S1620AT-G8	125MHz (8ns)
KMM374S1620AT-G0	100MHz (10ns)
KMM374S1620AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ CB7	Check bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$, $\overline{CS2}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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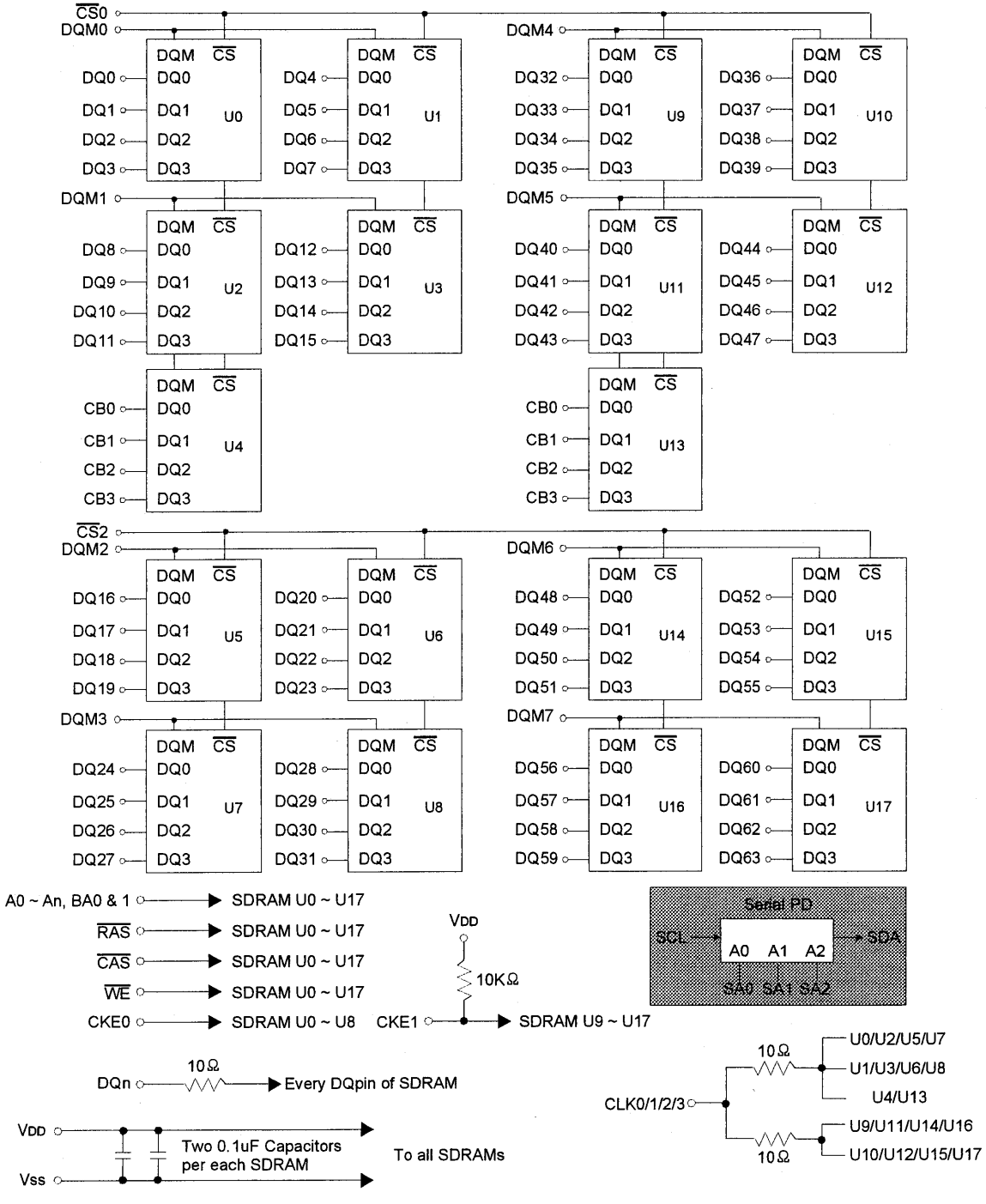
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA9
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	65	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	30	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	20	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	20	pF

DC CHARACTERISTICS

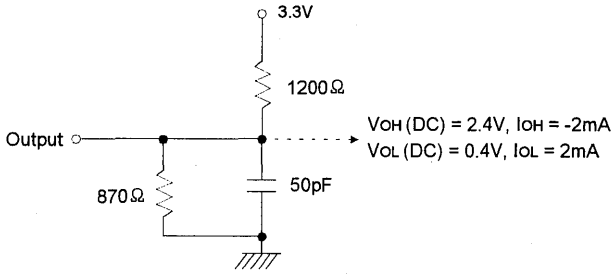
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		2,160	1,890	1,620	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), tcc = 15ns		36			mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		36				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		540			mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		360				
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), tcc = 15ns		108			mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		108				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		720			mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		450			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	2,880	2,250	1,980	mA	1
			2	1,980	1,800	1,620		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		3,240			mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V		27			mA	

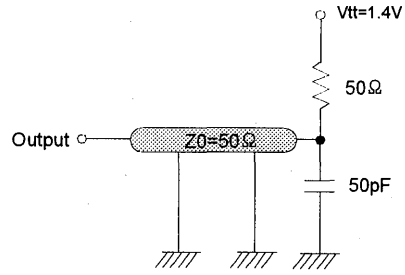
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S1620AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S1620AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S1620AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_9)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

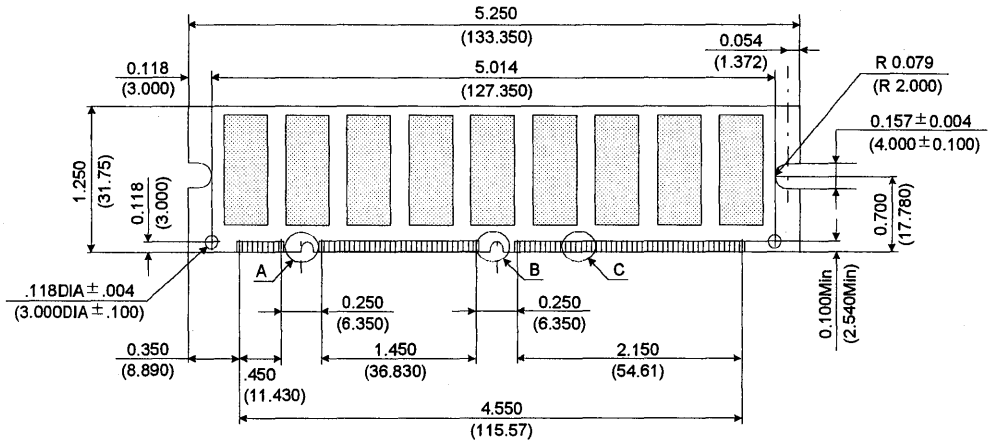
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

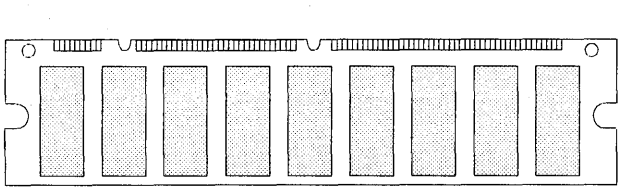
6. Burst stop command is valid at every burst length.

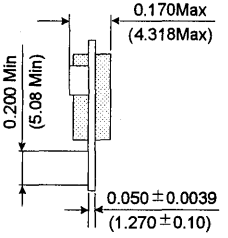
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

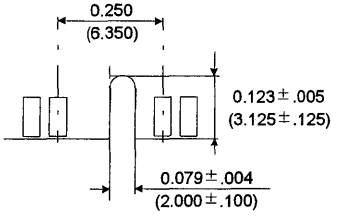
PACKAGE DIMENSIONS

Units : Inches (millimeters)

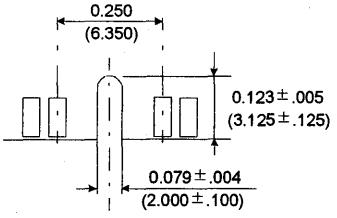




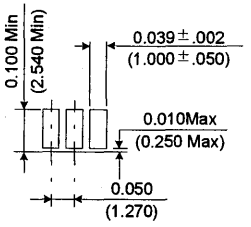




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP
SDRAM Part No. : KM44S16030AT

KMM374S1603AT SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S1603AT is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S1603AT consists of sixteen CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S1603AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S1603AT-G8	125MHz (8ns)
KMM374S1603AT-G0	100MHz (10ns)
KMM374S1603AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	***BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

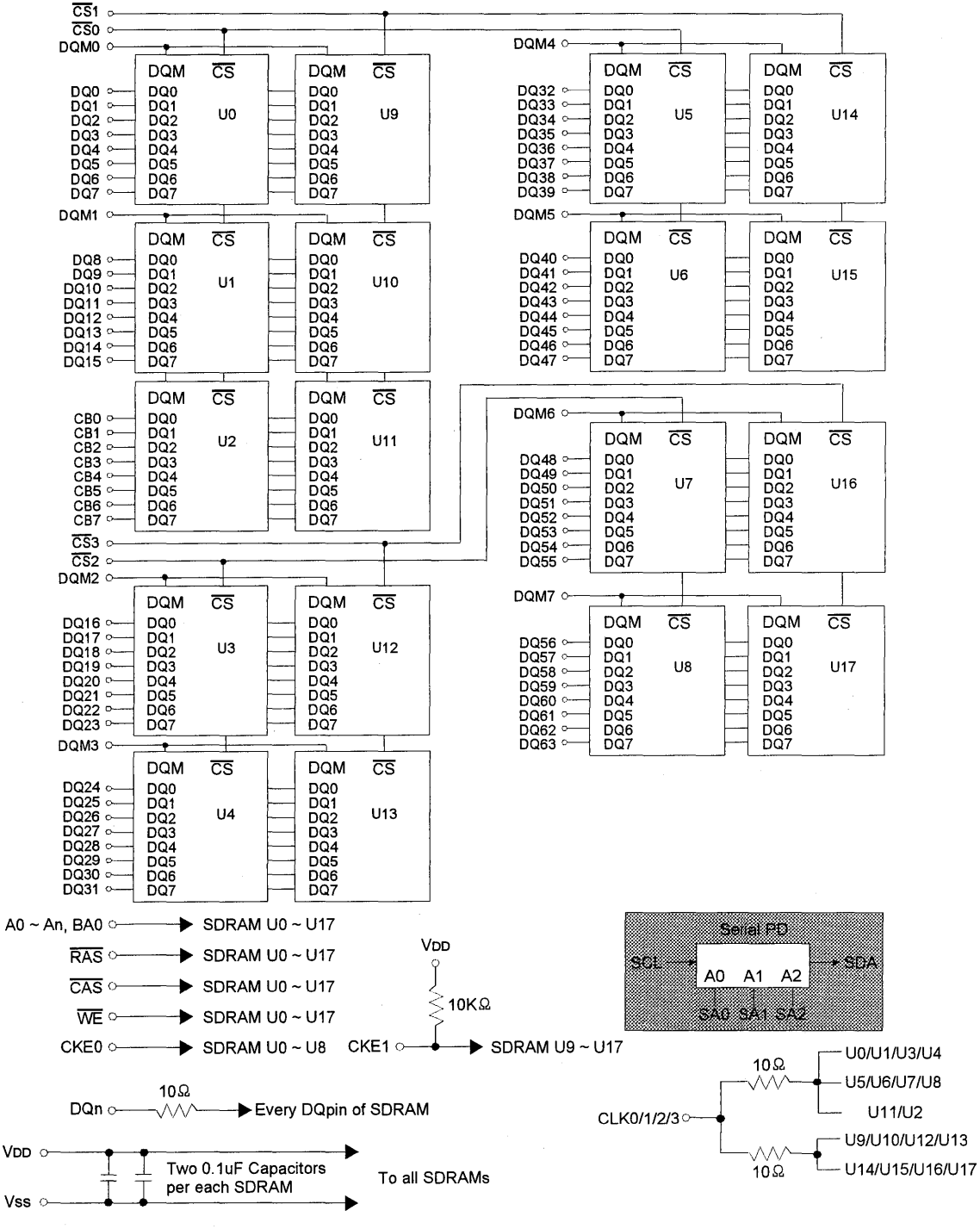
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ 7	Check bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/Vss	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	35	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	25	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	25	pF

DC CHARACTERISTICS

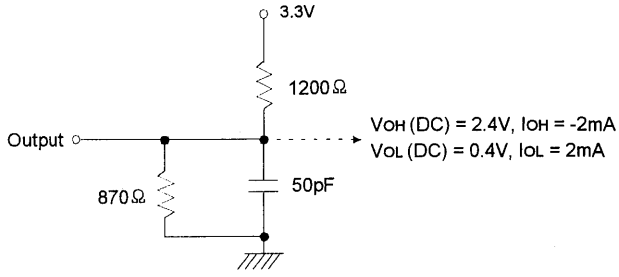
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,395	1,260	1,080	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		36			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		36				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		540			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		360				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		108			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		108				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		720			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		450			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,800	1,485	1,305	mA	1
			2	1,305	1,215	1,125		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		3,240			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		27			mA	

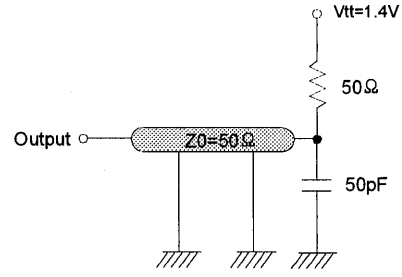
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S1603AT- G8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S1603AT- G0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S1603AT- G2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

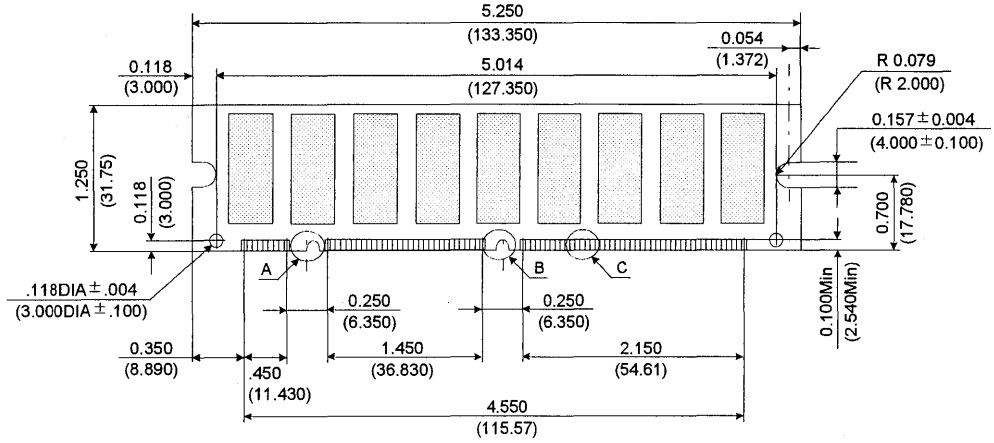
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

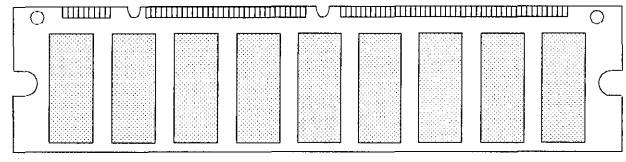
6. Burst stop command is valid at every burst length.

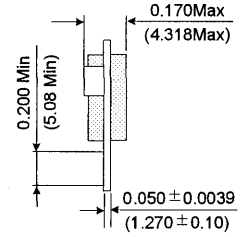
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

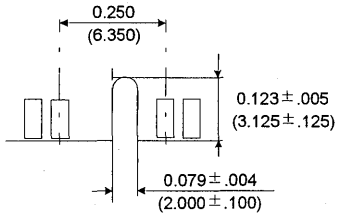
PACKAGE DIMENSIONS

Units : Inches (millimeters)

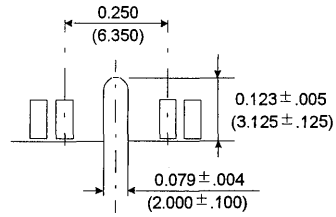




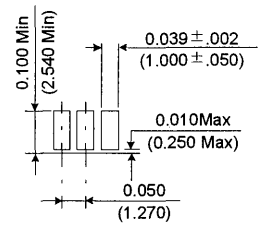




Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM374S1623AT SDRAM DIMM

16Mx72 SDRAM DIMM with ECC based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM374S1623AT is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung KMM374S1623AT consists of sixteen CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin SOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM374S1623AT is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM374S1623AT-G8	125MHz (8ns)
KMM374S1623AT-G0	100MHz (10ns)
KMM374S1623AT-G2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	$\overline{CS1}$	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	**BA0**	150	DQ54
11	DQ8	39	**BA1**	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CB0 ~ 7	Check bit (data-in / data-out)
CLK0 ~ CLK3	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS3}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
*VREF	Power Supply for Reference
**SDA	Serial Data I/O
**SCL	Serial Clock
**SA0 ~ 2	Address in EEPROM
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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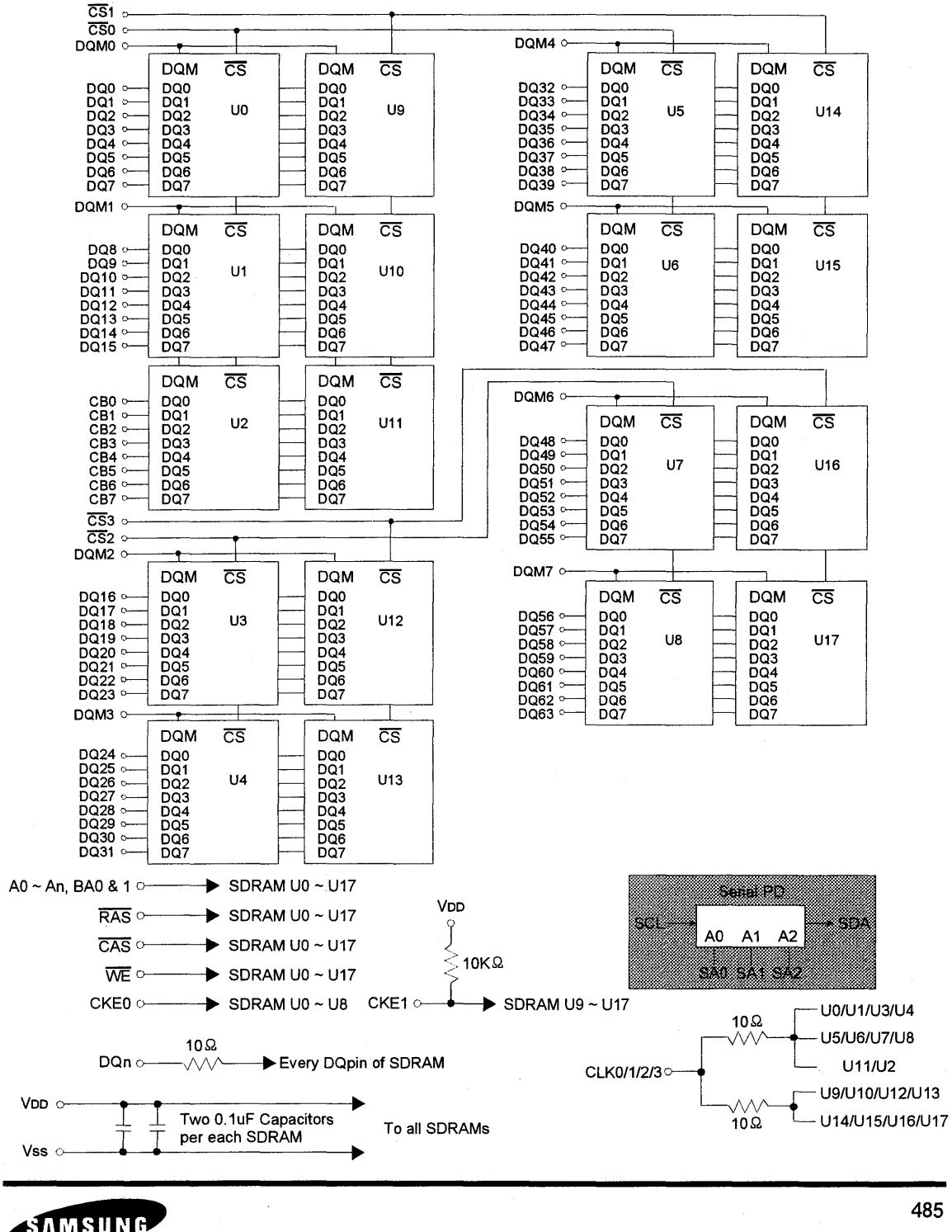
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-90	-	90	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	95	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	95	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	-	45	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS3}$)	C_{IN5}	-	40	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	35	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT1}	-	25	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT2}	-	25	pF

DC CHARACTERISTICS

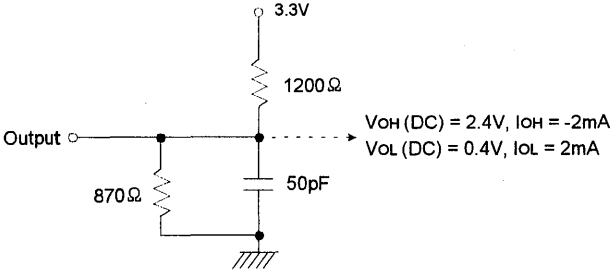
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,395	1,260	1,080	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		36			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		36				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		540			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		360				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		108			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		108				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		720			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		450			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,800	1,485	1,305	mA	1
			2	1,305	1,215	1,125		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		3,240			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		27			mA	

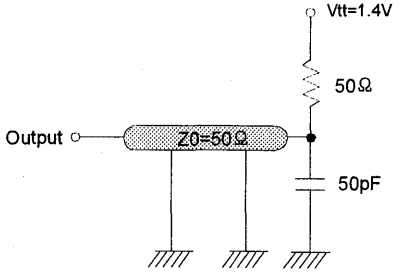
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM374S1623AT- G8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM374S1623AT- G0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM374S1623AT- G2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

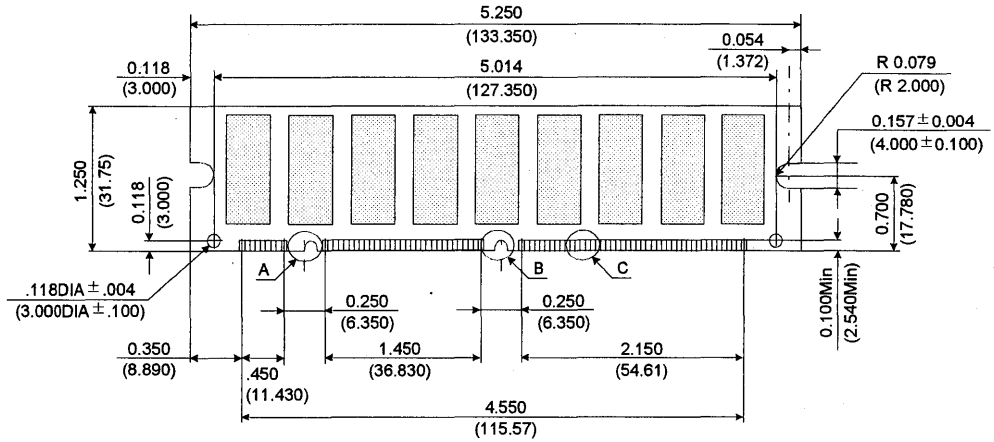
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

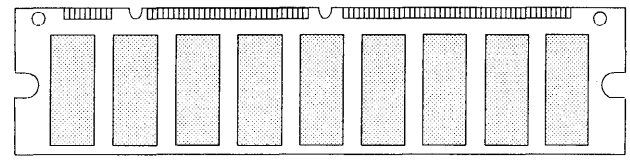
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

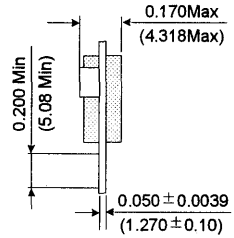
Note : 1. OP Code : Operand Code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

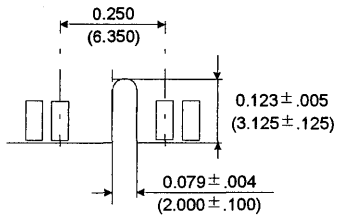
PACKAGE DIMENSIONS

Units : Inches (millimeters)

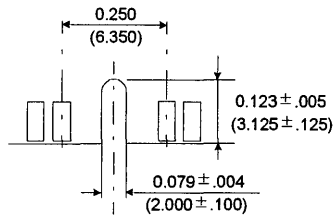




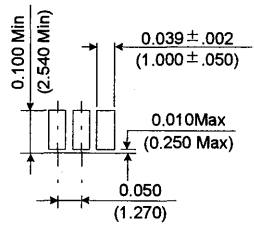




Detail A



Detail B



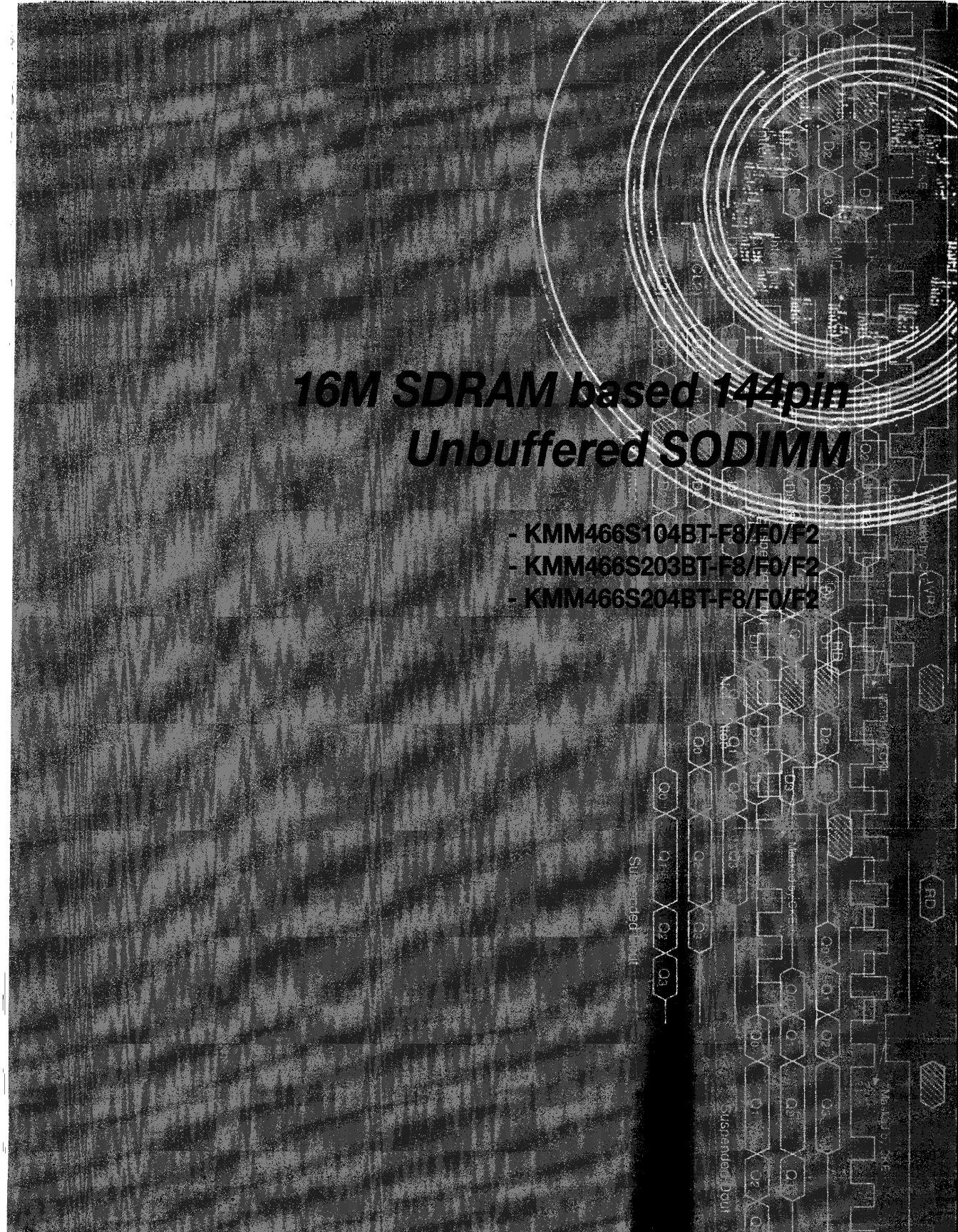
Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

16M SDRAM based 144pin Unbuffered SODIMM

- KMM466S104BT-F8/F0/F2
- KMM466S203BT-F8/F0/F2
- KMM466S204BT-F8/F0/F2



KMM466S104BT SDRAM SODIMM

1Mx64 SDRAM SODIMM based on 1Mx16, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S104BT is a 1M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S104BT consists of four CMOS 1M x 16 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S104BT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S104BT-F8	125MHz (8ns)
KMM466S104BT-F0	100MHz (10ns)
KMM466S104BT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	*A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

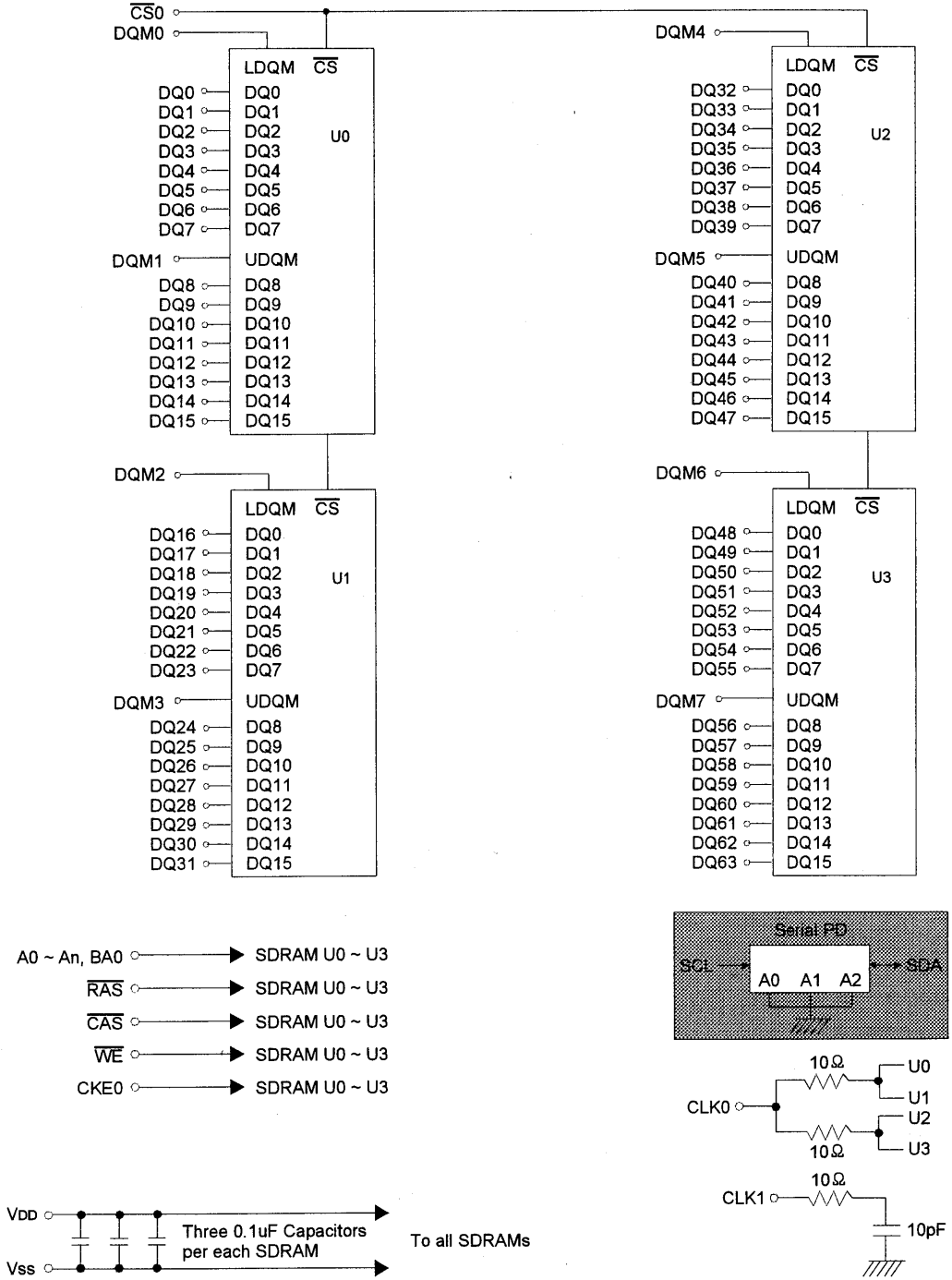
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

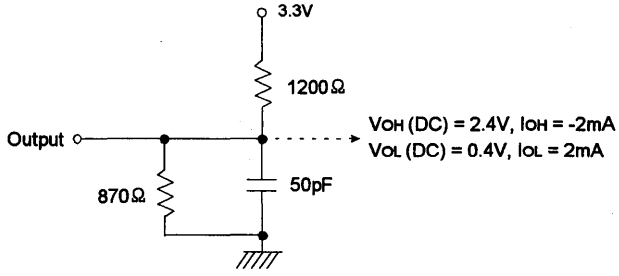
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1, $t_{RC} \geq t_{RC}$(min), I_{OL} = 0 mA		460	440	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		2			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		2				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns, Input signals are changed one time during 30ns		80			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞, Input signals are stable		20				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		12			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns, Input signals are changed one time during 30ns		140			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞, Input signals are stable		80			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst, t_{CCD} = 2CLKs, @ Same Row	3	540	440	380	mA	1
			2	380	360	320		
			1	260	240	220		
		@ Different Row	3	800	720	640	mA	1
			2	620	560	480		
			1	480	440	380		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		280			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		1			mA	

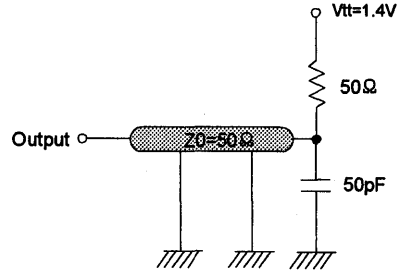
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S104BT- F8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM466S104BT- F0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S104BT- F2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_9~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

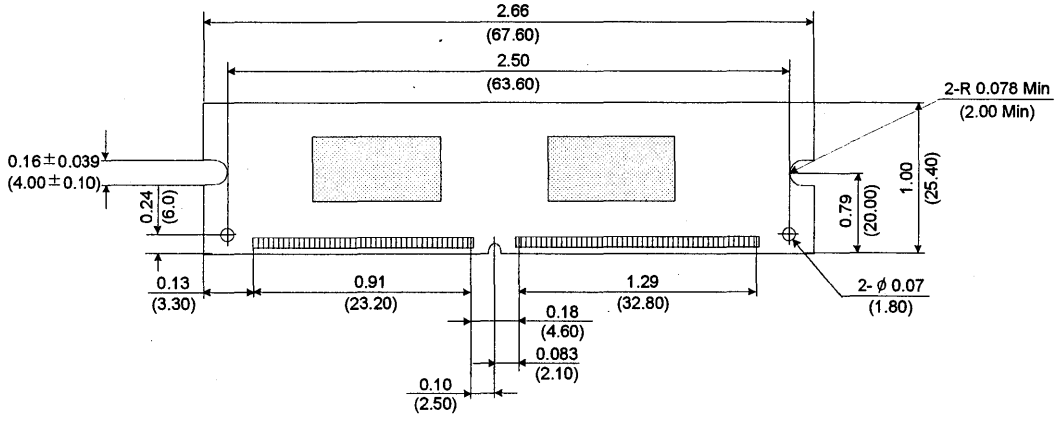
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

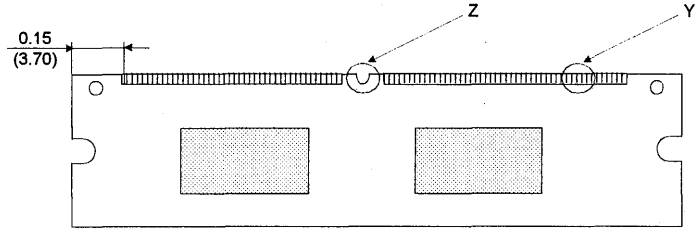
6. Burst stop command is valid at every burst length.

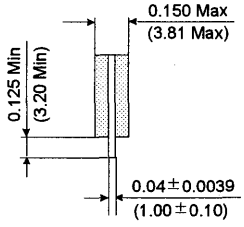
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

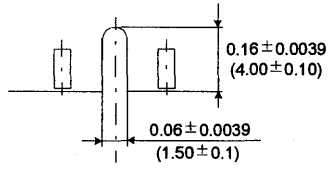
PACKAGE DIMENSIONS

Units : Inches (millimeters)

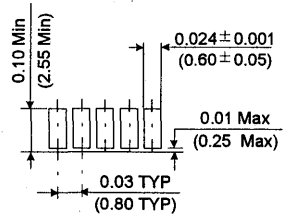








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S1020BT

KMM466S203BT SDRAM SODIMM

2Mx64 SDRAM SODIMM based on 2Mx8, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S203BT is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S203BT consists of eight CMOS 2M x 8 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S203BT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S203BT-F8	125MHz (8ns)
KMM466S203BT-F0	100MHz (10ns)
KMM466S203BT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	**BA0**
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	*A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

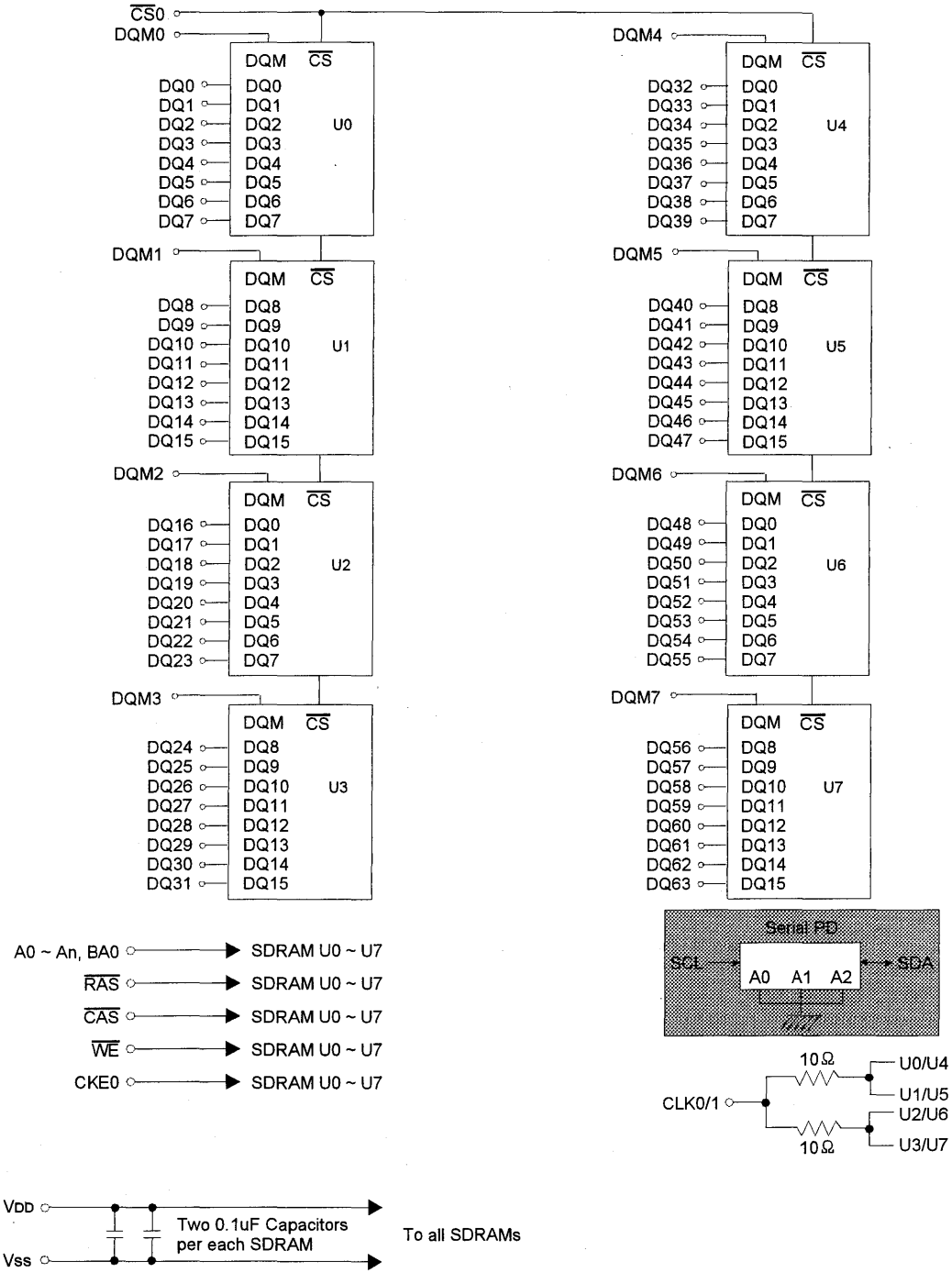
Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

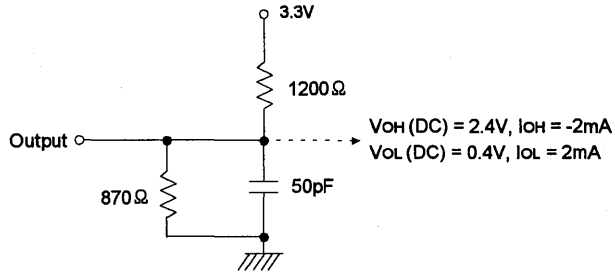
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		840	800	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		4				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		40				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		280			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	1,000	800	720	mA	1
			@ Same Row 2	720	640	600		
			@ Same Row 1	480	440	400		
			@ Different Row 3	1,440	1,280	1,120	mA	1
			@ Different Row 2	1,160	1,040	880		
			@ Different Row 1	920	840	720		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		560			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2			mA	

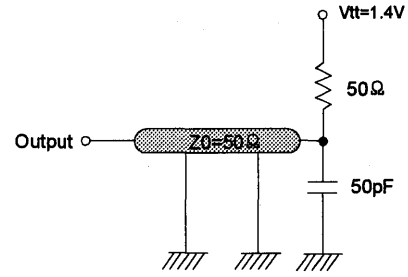
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	24	26	30	ns	1
Row precharge time		tRP(min)	20	26	30	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	80	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S203BT- F8

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM466S203BT- F0

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S203BT- F2

(Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_9~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry											
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

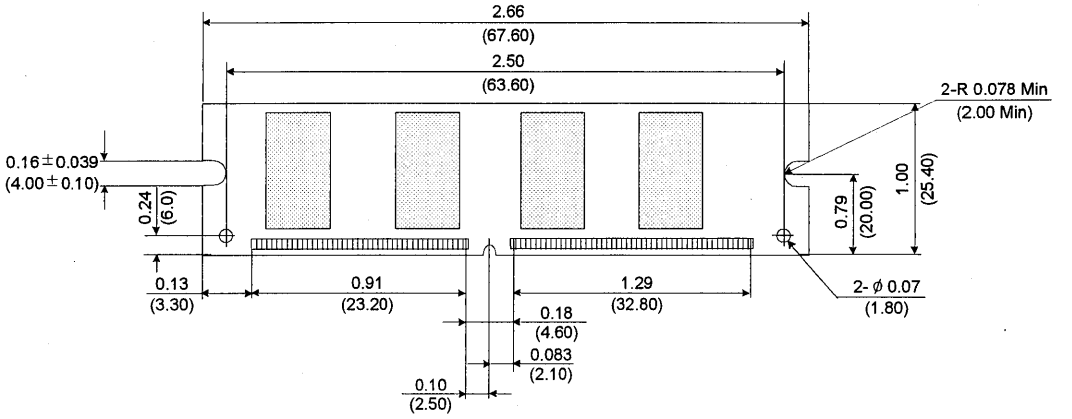
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

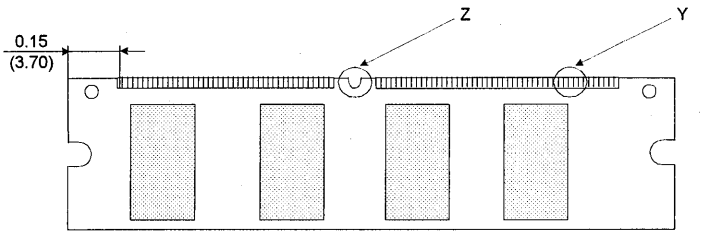
6. Burst stop command is valid at every burst length.

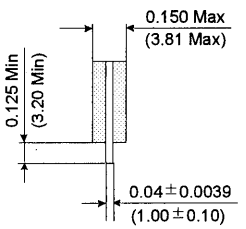
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

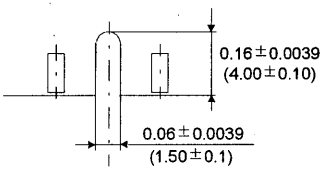
PACKAGE DIMENSIONS

Units : Inches (millimeters)

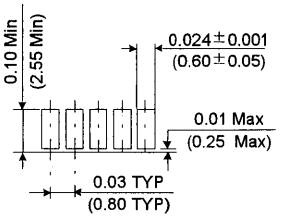








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S2020BT

KMM466S204BT SDRAM SODIMM

2Mx64 SDRAM SODIMM based on 1Mx16, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S204BT is a 2M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S204BT consists of eight CMOS 1M x 16 bit Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S204BT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S204BT-F8	125MHz (8ns)
KMM466S204BT-F0	100MHz (10ns)
KMM466S204BT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,050mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	*A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A10/AP	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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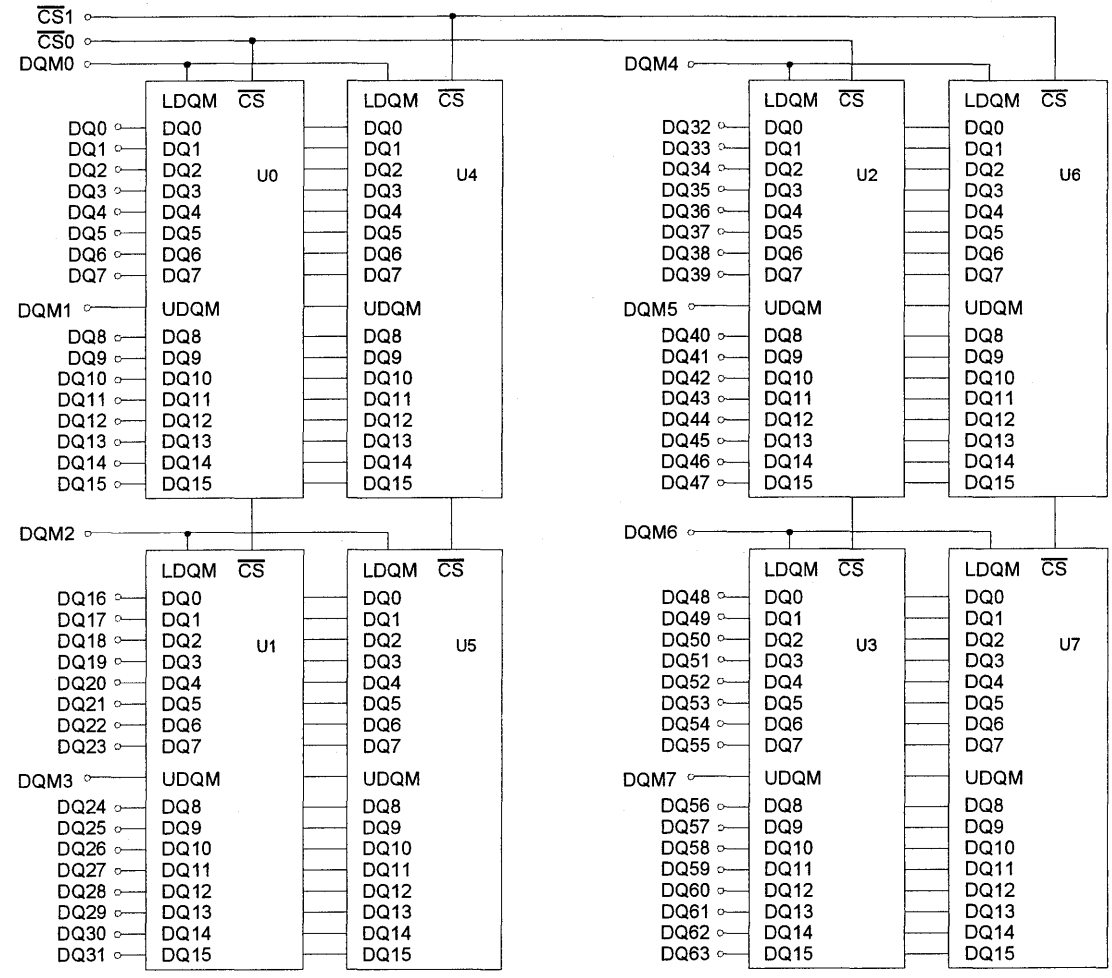
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{10}/AP, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

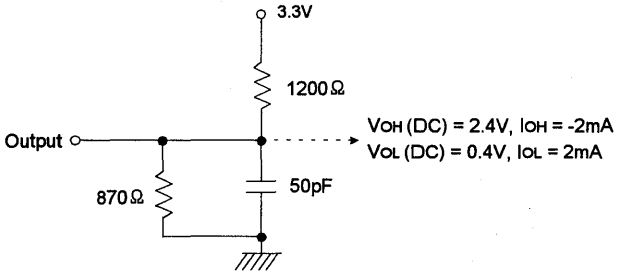
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	520	480	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		4			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		4				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		160			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		40				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		16				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		280			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		160			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst t_{CCD} = 2CLKs	@ Same Row 3	620	520	460	mA	1
			@ Same Row 2	460	440	400		
			@ Same Row 1	340	320	300		
			@ Different Row 3	880	800	720	mA	1
			@ Different Row 2	700	640	560		
			@ Different Row 1	560	520	460		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		540			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		2			mA	

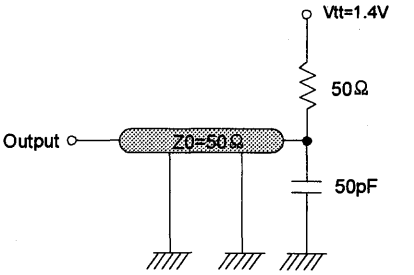
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	24	26	30	ns	1
Row precharge time		$t_{RP(min)}$	20	26	30	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	80	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		0				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
	CAS latency=1		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			7		8		9		
	CAS latency=1			20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
	CAS latency=1		5		5		5			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			7		8		9		
	CAS latency=1			15		15		15		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S204BT- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	48ns	20ns	16ns	24ns	8ns	8ns	8ns
125MHz (8.0ns)	3	10	6	3	2	3	1	1	1
100MHz (10.0ns)	3	8	5	2	2	3	1	1	1
83MHz (12.0ns)	2	7	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

KMM466S204BT- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	3	2	3	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S204BT- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	3	2	3	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

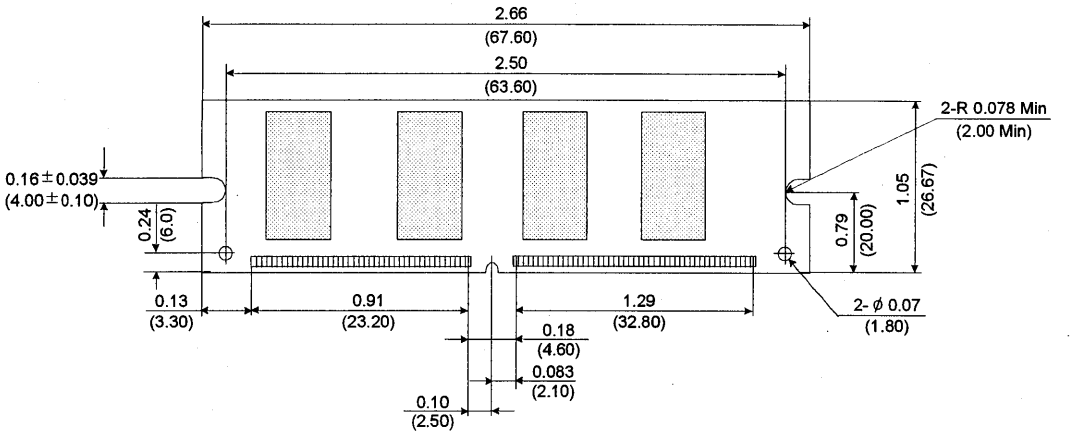
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_9~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

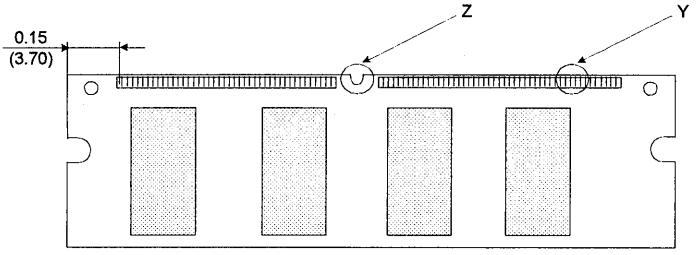
(V=Valid, X=Don' t Care, H=Logic High, L=Logic Low)

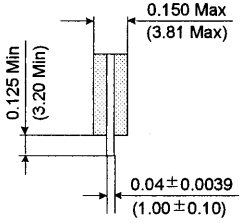
Note : 1. OP Code : Operand Code
A_0 ~ A_{10}/AP, BA_0 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.
4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

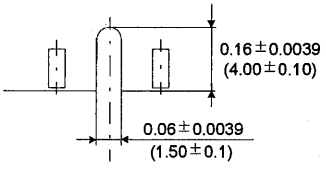
PACKAGE DIMENSIONS

Units : Inches (millimeters)

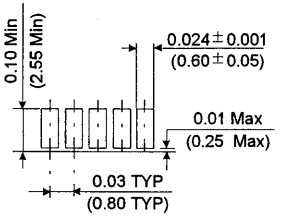








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 1Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S1020BT

64M SDRAM based 144pin Unbuffered SODIMM

- KMM466S404AT-F8/F0/F2
- KMM466S424AT-F8/F0/F2
- KMM466S803AT-F8/F0/F2
- KMM466S823AT-F8/F0/F2
- KMM466S803AT2-F8/F0/F2
- KMM466S823AT2-F8/F0/F2
- KMM466S804AT-F8/F0/F2
- KMM466S823AT-F8/F0/F2
- KMM466S804AT2-F8/F0/F2
- KMM466S824AT2-F8/F0/F2

KMM466S404AT SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S404AT is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S404AT consists of four CMOS 4M x 16 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S404AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S404AT-F8	125MHz (8ns)
KMM466S404AT-F0	100MHz (10ns)
KMM466S404AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

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PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	**BA0**
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don't use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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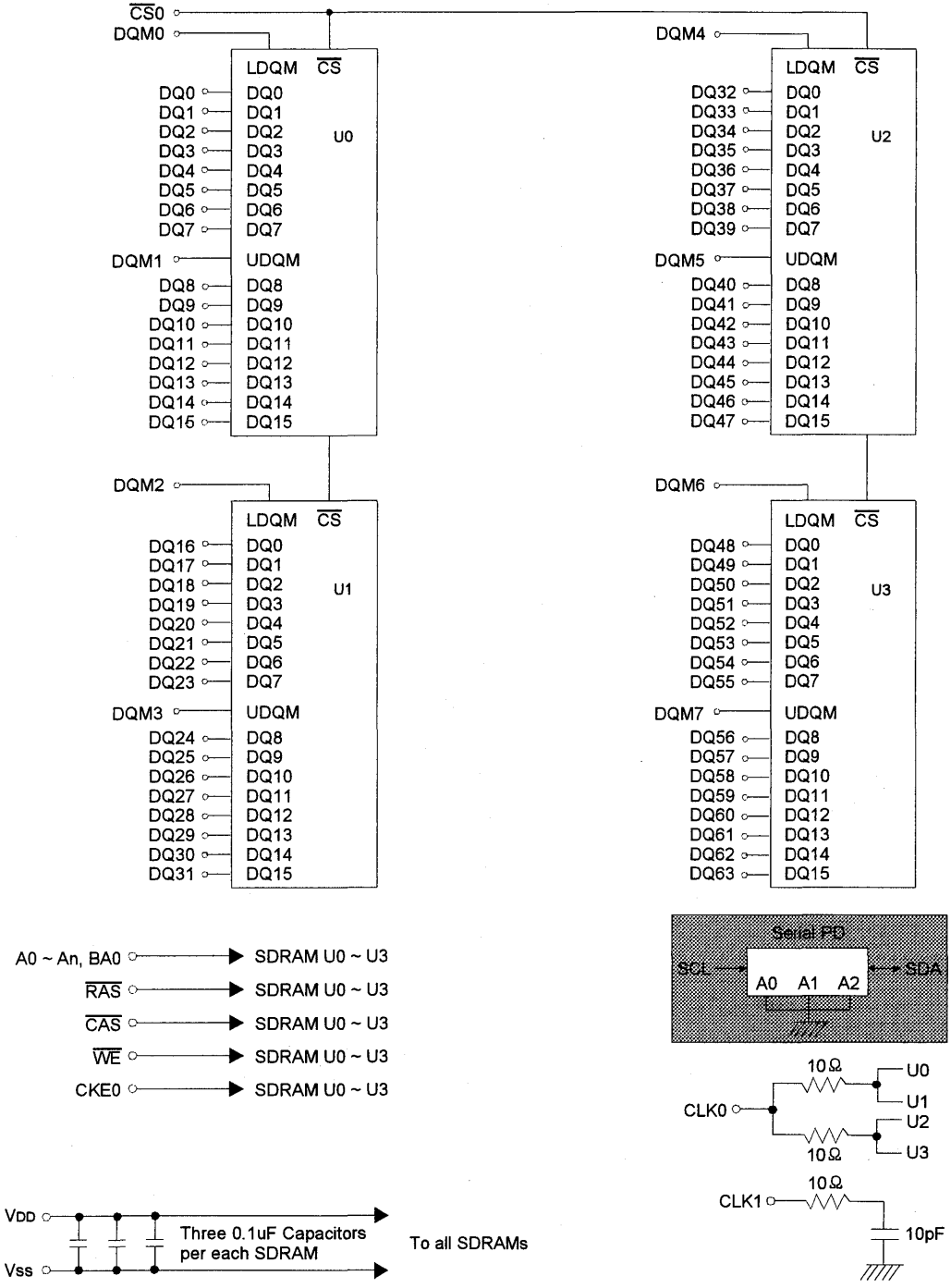
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

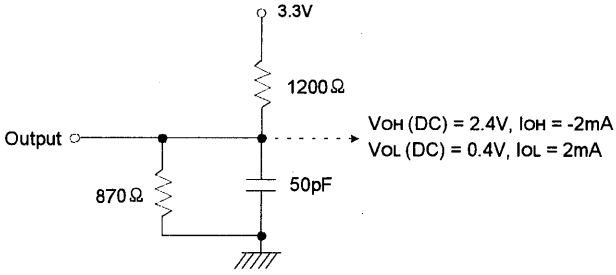
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	480	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		24				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		120			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	740	600	500	mA	1
			2	520	480	440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		720			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2			mA	

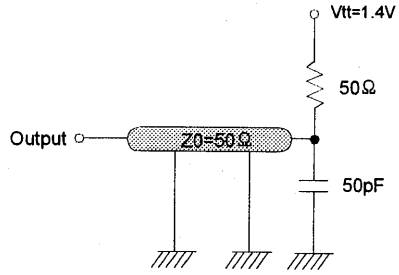
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S404AT- F8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S404AT- F0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S404AT- F2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

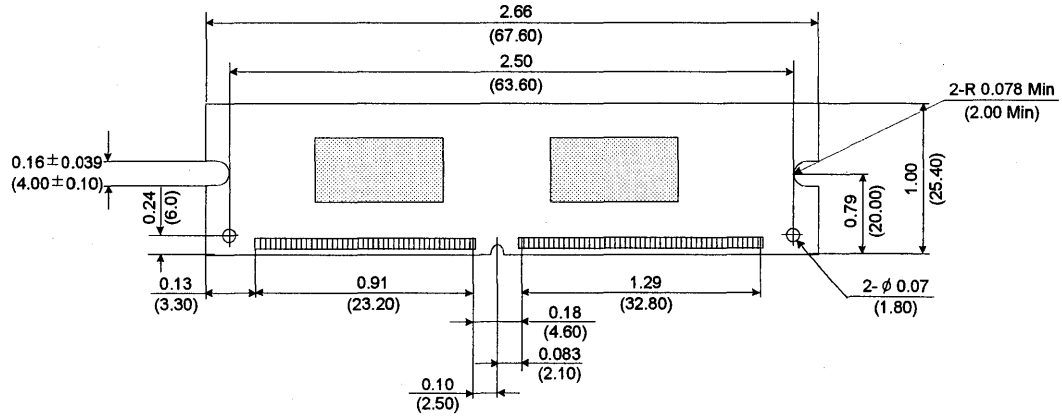
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

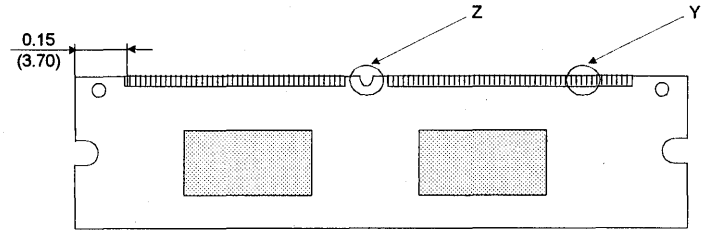
6. Burst stop command is valid at every burst length.

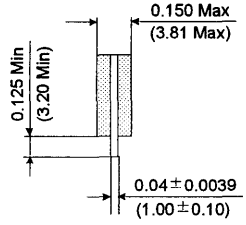
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

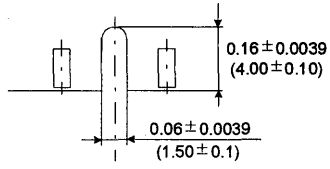
PACKAGE DIMENSIONS

Units : Inches (millimeters)

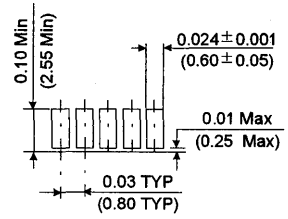








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4020AT

KMM466S424AT SDRAM SODIMM

4Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S424AT is a 4M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S424AT consists of four CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S424AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S424AT-F8	125MHz (8ns)
KMM466S424AT-F0	100MHz (10ns)
KMM466S424AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,000mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	**BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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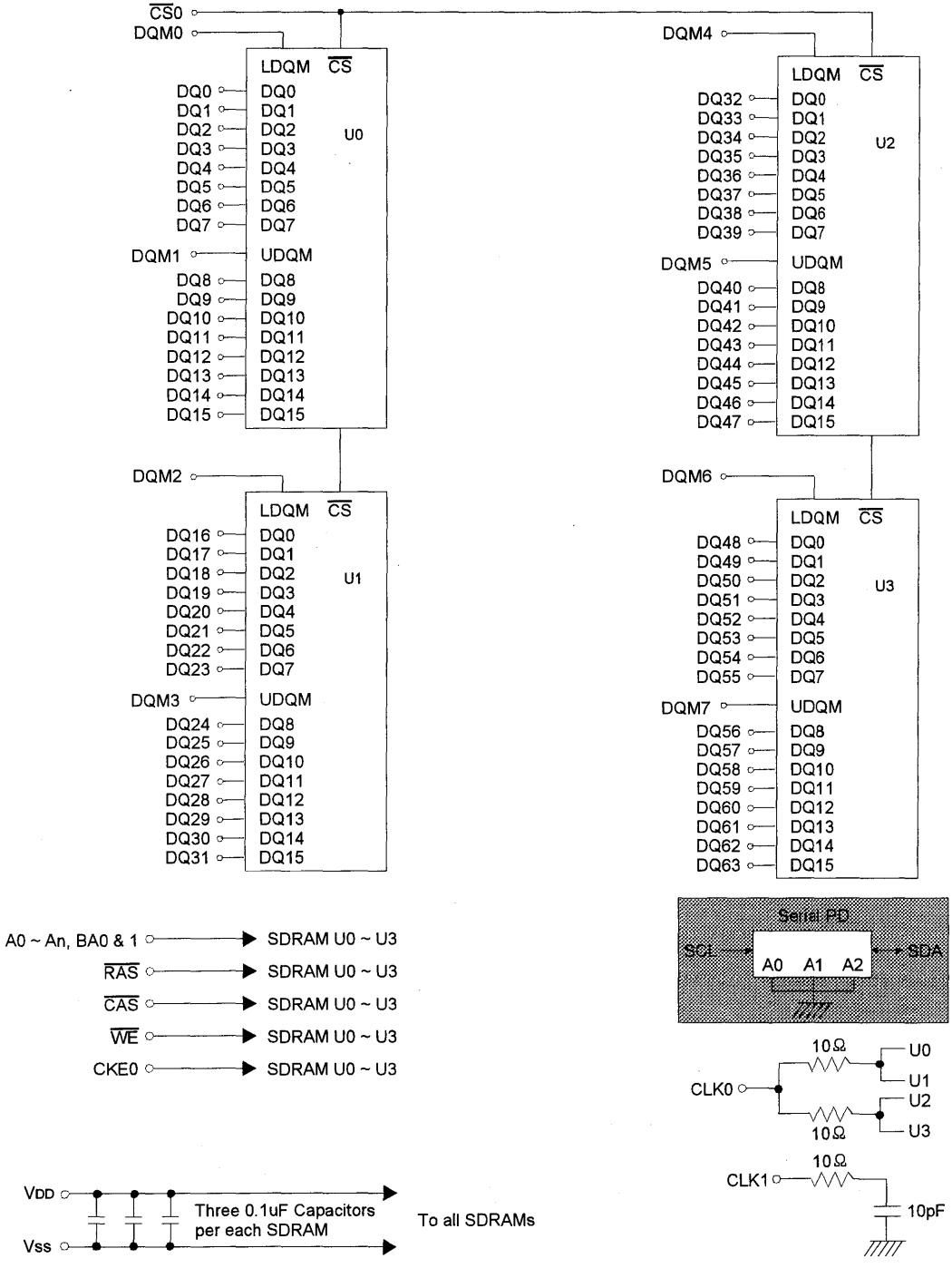
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	4	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-20	-	20	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	35	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	35	pF
Input capacitance (CKE0)	C_{IN3}	-	35	pF
Input capacitance (CLK0)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

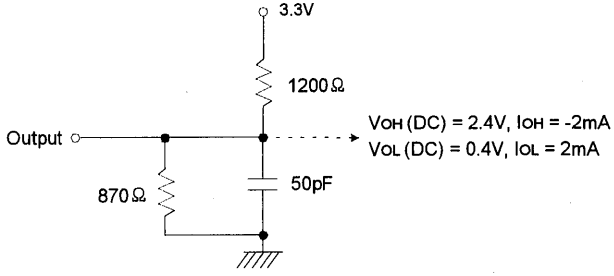
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		540	480	400	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		8			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		8				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		120			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		80				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		24			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		24				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		180			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		120			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	740	600	500	mA	1
			2	520	480	440		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		720			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2			mA	

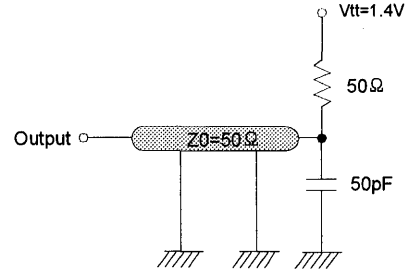
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S424AT- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S424AT- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S424AT- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.

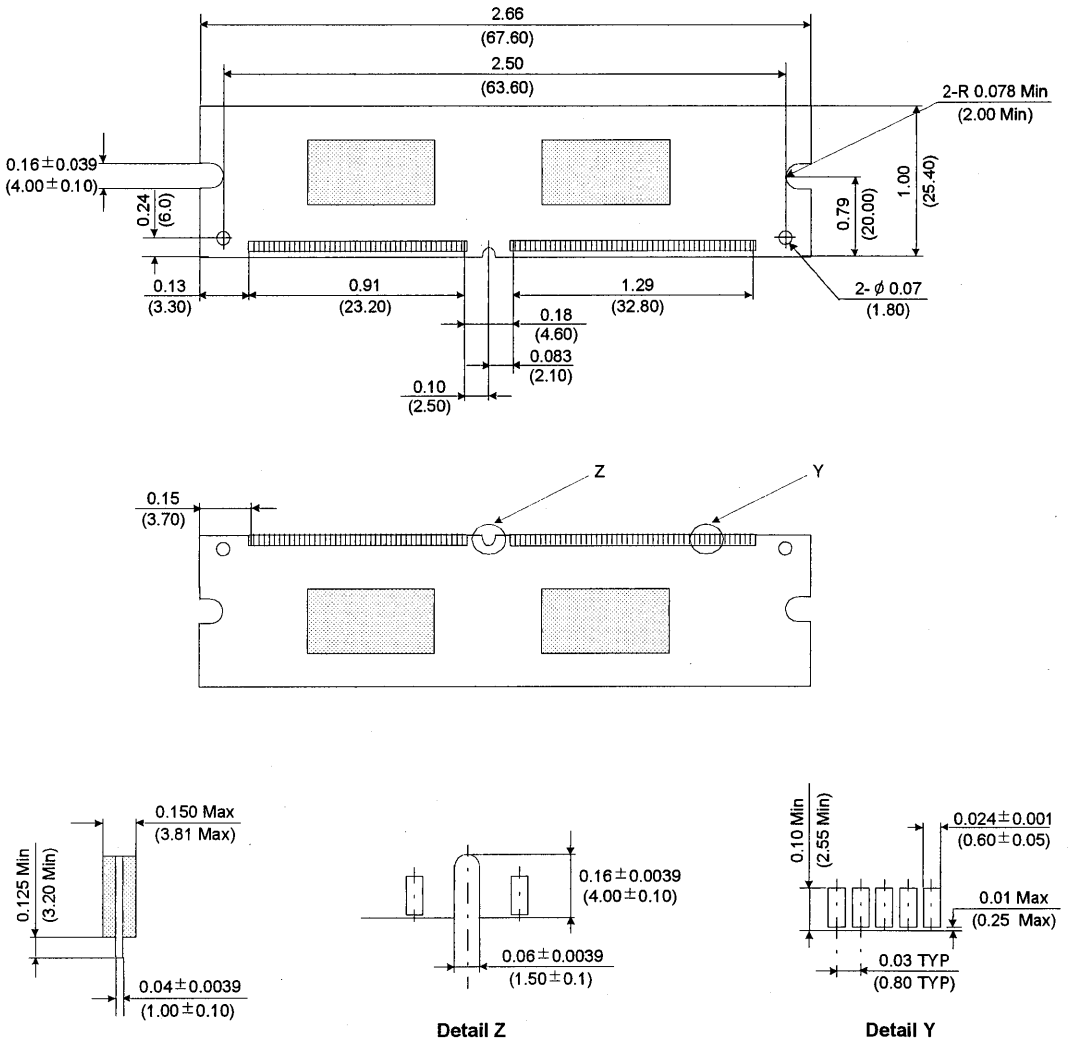
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4030AT

KMM466S803AT SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S803AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S803AT consists of eight CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S803AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S803AT-F8	125MHz (8ns)
KMM466S803AT-F0	100MHz (10ns)
KMM466S803AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

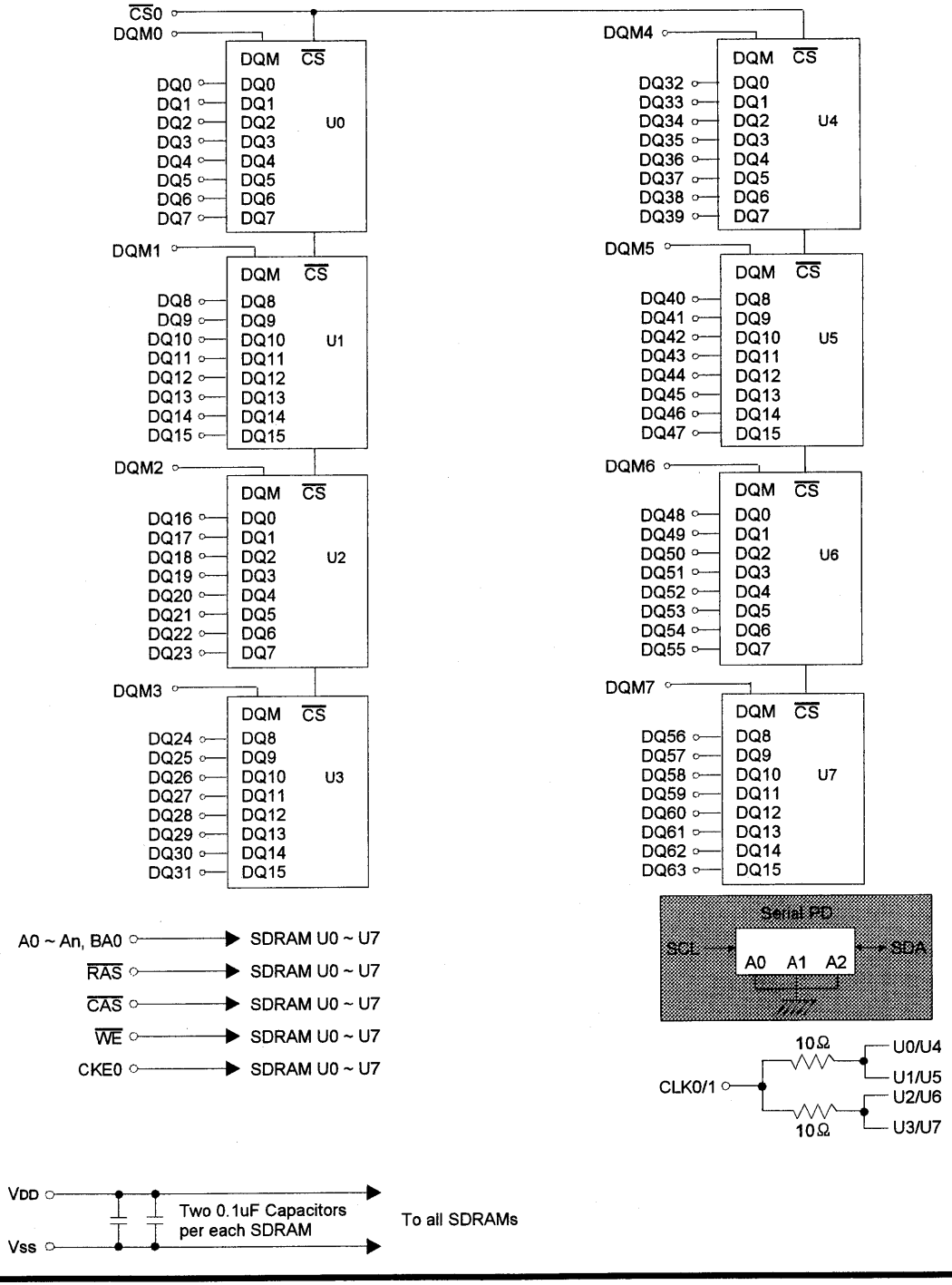
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

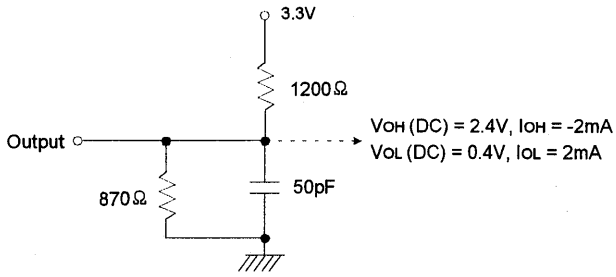
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V		4			mA	

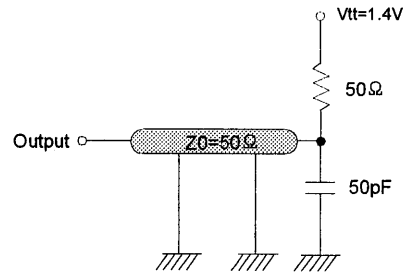
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S803AT- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S803AT- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S803AT- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

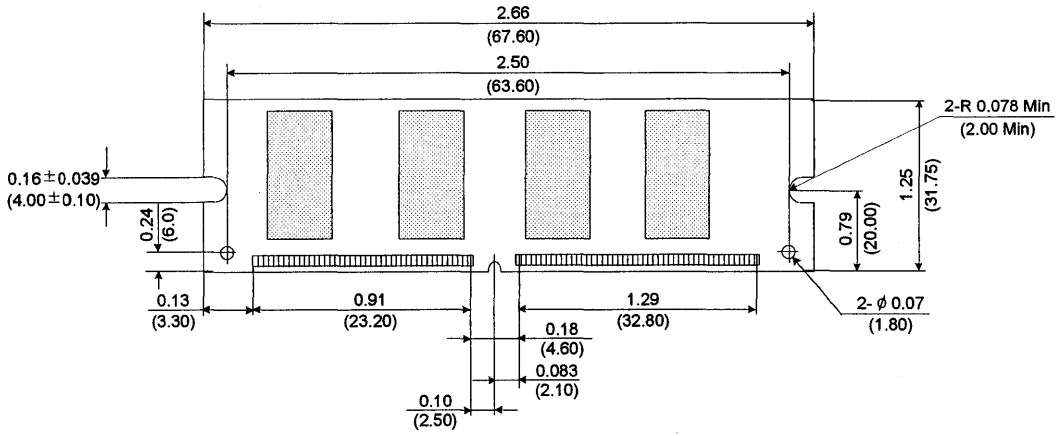
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

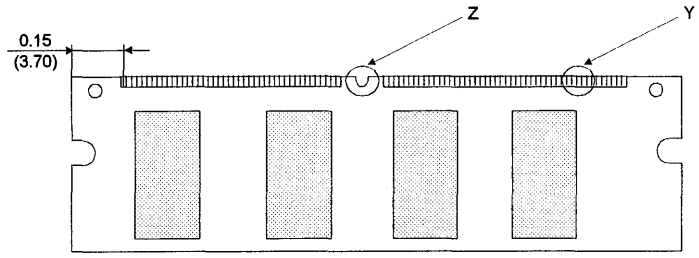
6. Burst stop command is valid at every burst length.

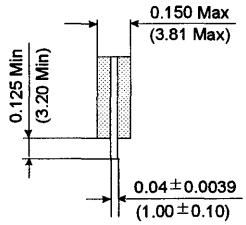
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

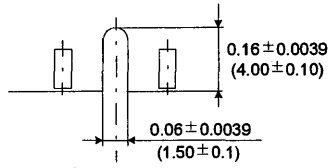
PACKAGE DIMENSIONS

Units : Inches (millimeters)

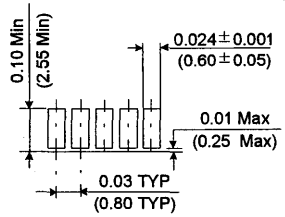








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM466S823AT SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S823AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S823AT consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S823AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S823AT-F8	125MHz (8ns)
KMM466S823AT-F0	100MHz (10ns)
KMM466S823AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	**BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

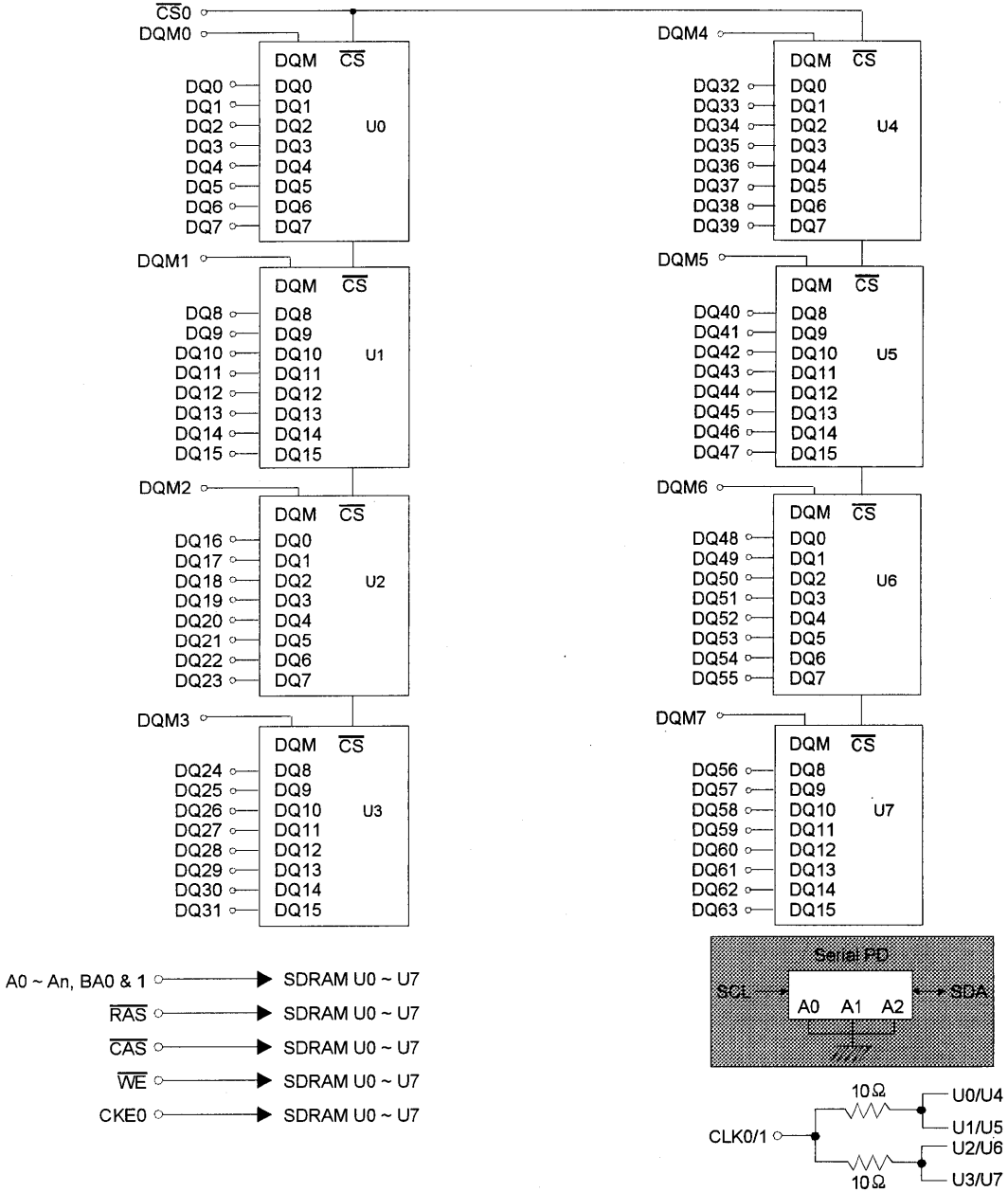
Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

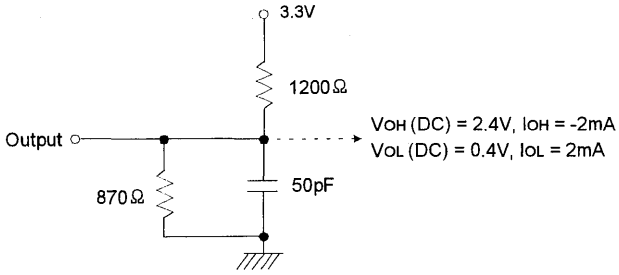
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

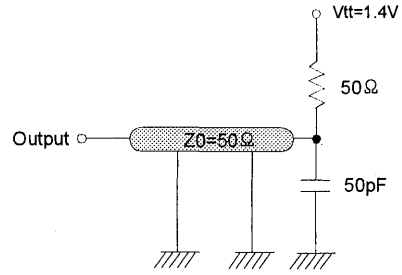
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S823AT- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S823AT- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S823AT- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

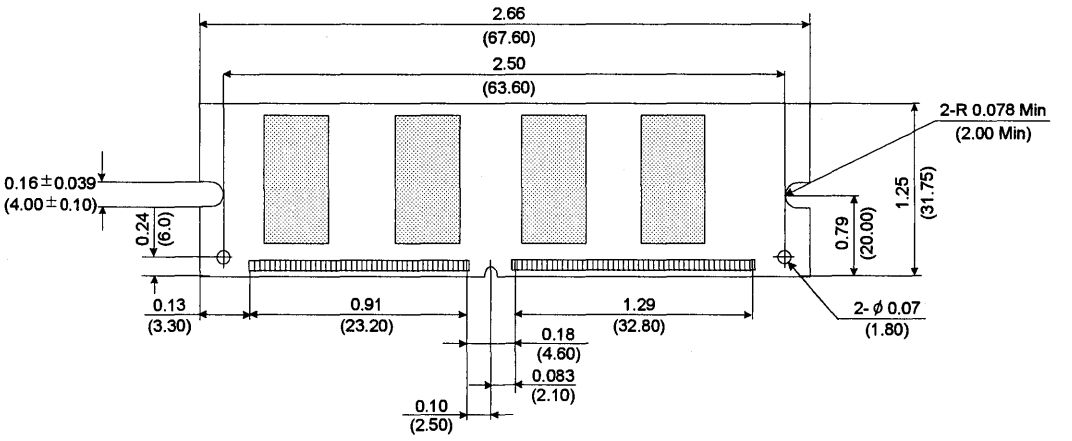
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

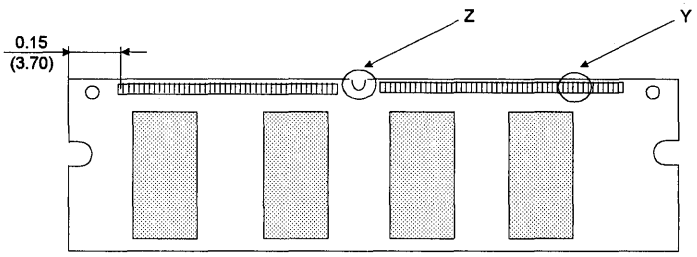
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

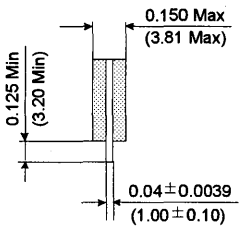
Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

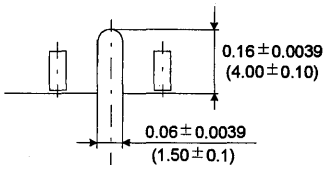
PACKAGE DIMENSIONS

Units : Inches (millimeters)

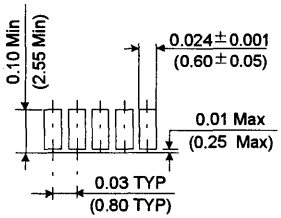








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

KMM466S803AT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S803AT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S803AT2 consists of eight CMOS 8M x 8 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S803AT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S803AT2-F8	125MHz (8ns)
KMM466S803AT2-F0	100MHz (10ns)
KMM466S803AT2-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,150mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

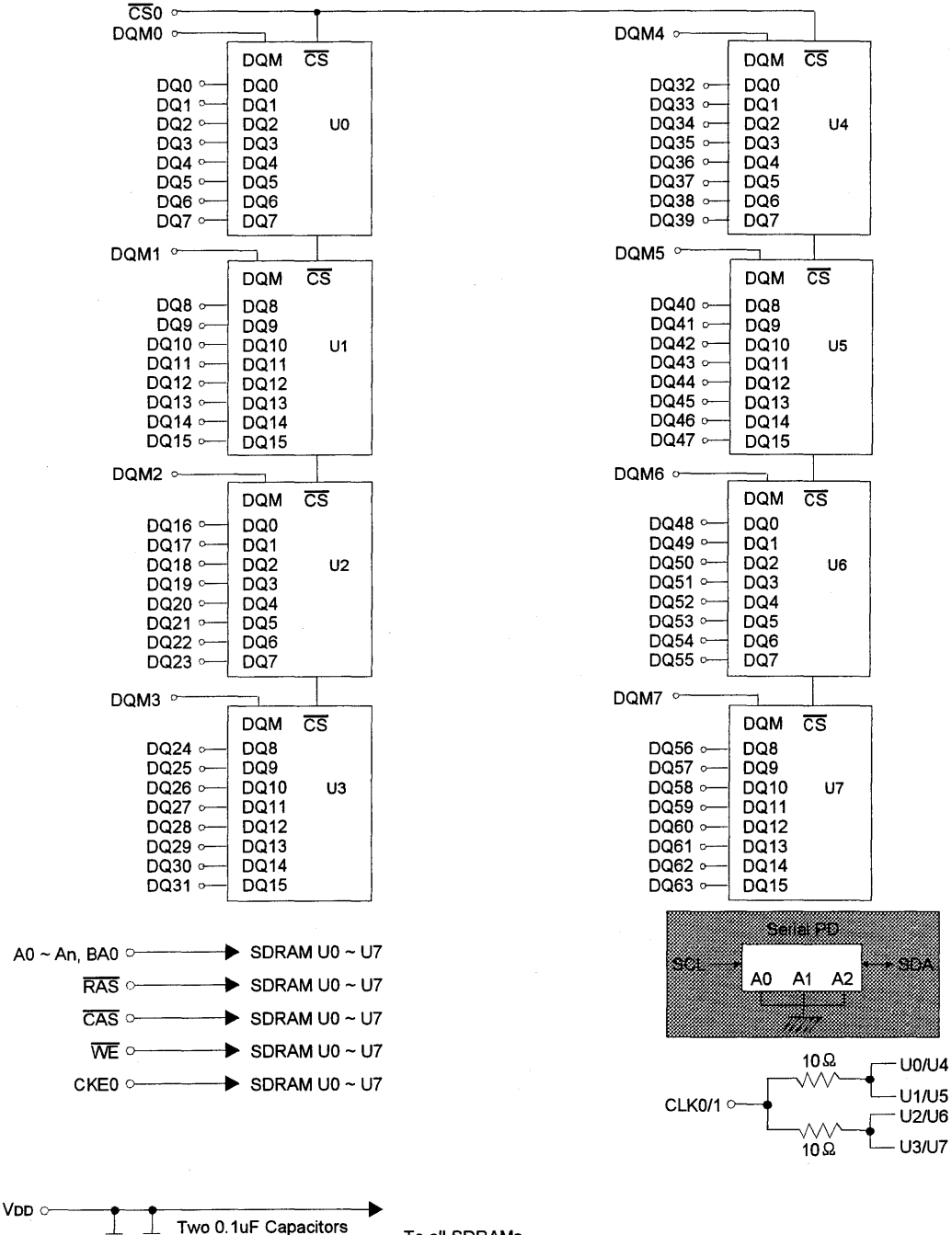
Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA8
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

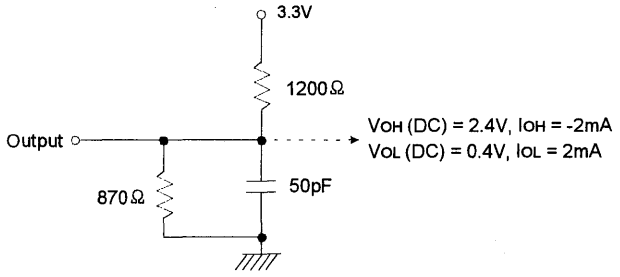
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

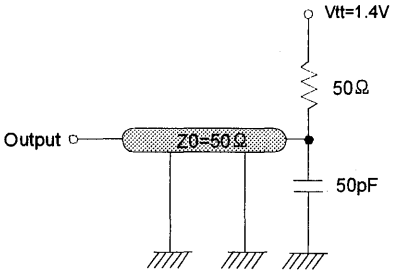
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S803AT2- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S803AT2- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S803AT2- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

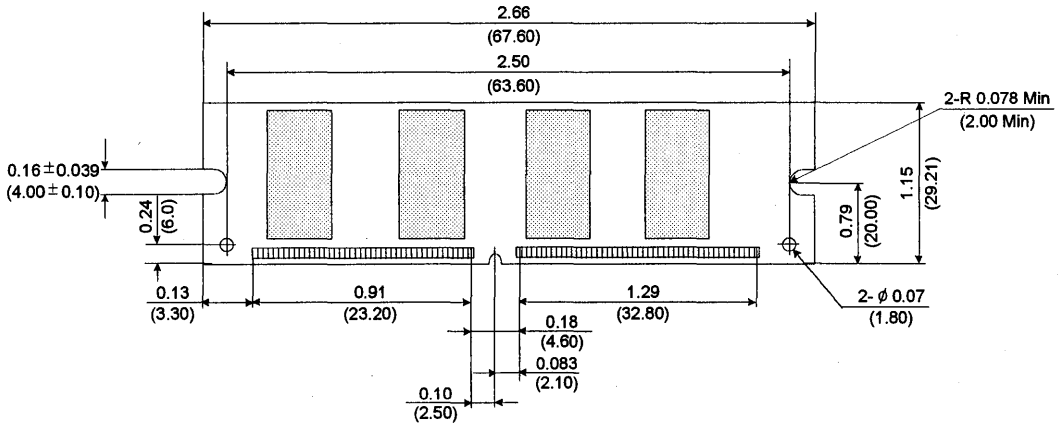
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

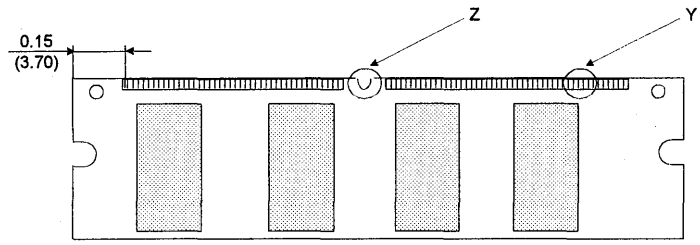
6. Burst stop command is valid at every burst length.

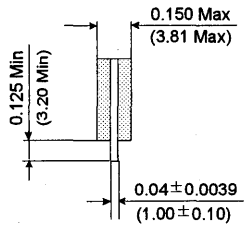
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

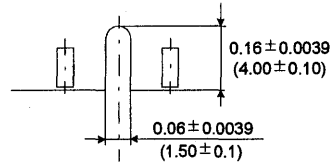
PACKAGE DIMENSIONS

Units : Inches (millimeters)

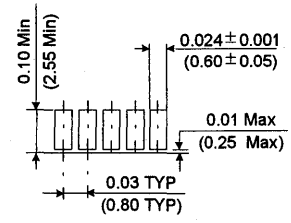








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8020AT

KMM466S823AT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S823AT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S823AT2 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S823AT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S823AT2-F8	125MHz (8ns)
KMM466S823AT2-F0	100MHz (10ns)
KMM466S823AT2-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,150mil)**, double sided component

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	**BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0	Clock Enable Input
$\overline{CS0}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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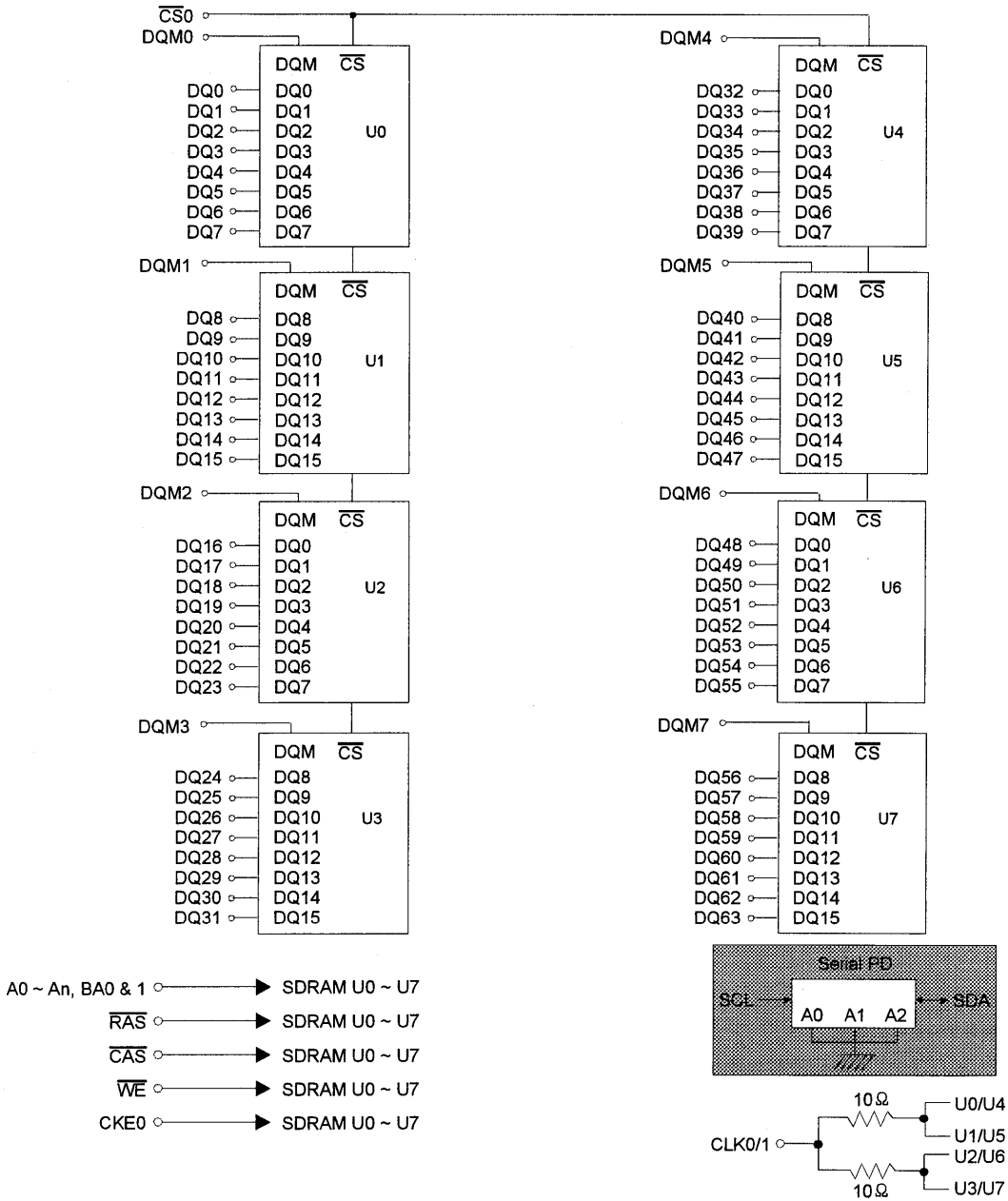
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA8
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0)	C_{IN3}	-	55	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$)	C_{IN5}	-	55	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	20	pF

DC CHARACTERISTICS

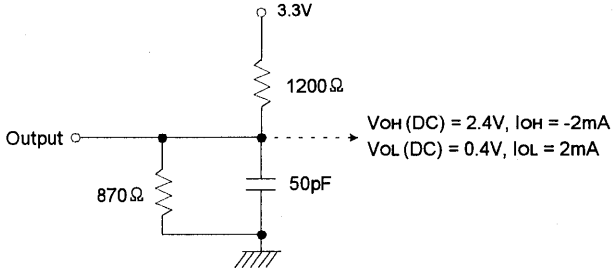
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		1,000	880	720	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE≤V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		320			mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), tcc = ∞ Input signals are stable		200			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	1,360	1,080	920	mA	1
			2	920	840	760		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		4			mA	

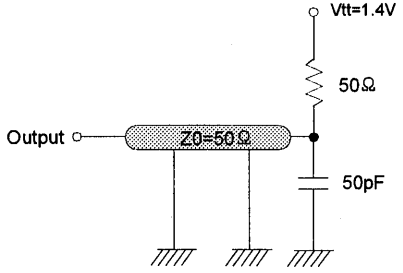
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S823AT2- F8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S823AT2- F0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S823AT2- F2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

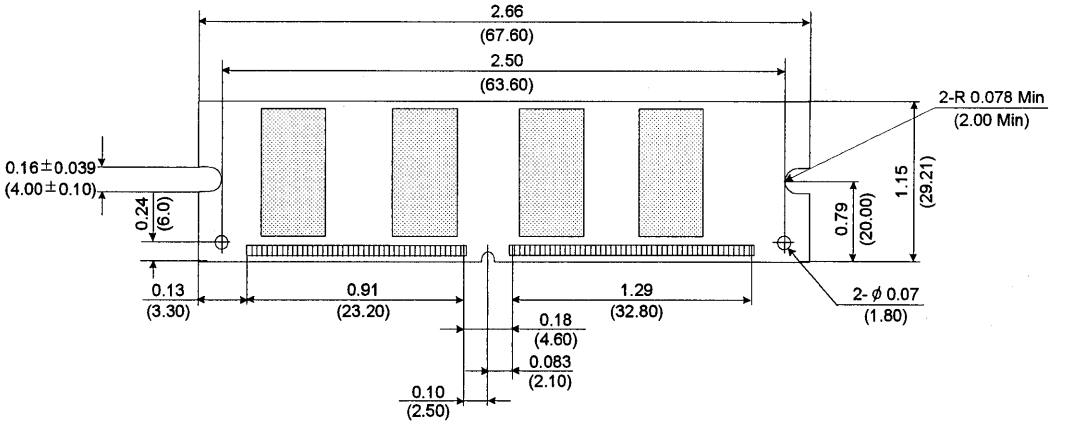
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

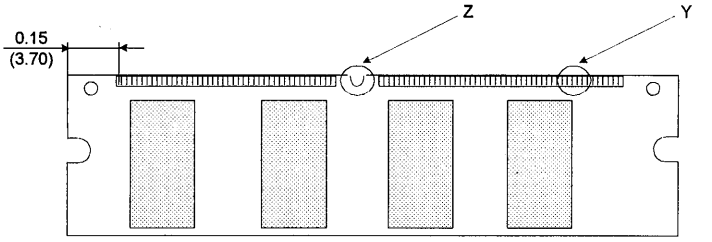
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

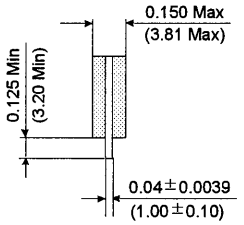
Note : 1. OP Code : Operand Code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

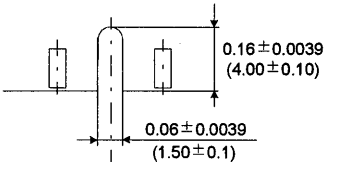
PACKAGE DIMENSIONS

Units : Inches (millimeters)

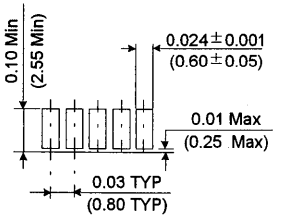








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 SDRAM, TSOP
SDRAM Part No. : KM48S8030AT

KMM466S804AT SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S804AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S804AT consists of eight CMOS 4M x 16 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S804AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S804AT-F8	125MHz (8ns)
KMM466S804AT-F0	100MHz (10ns)
KMM466S804AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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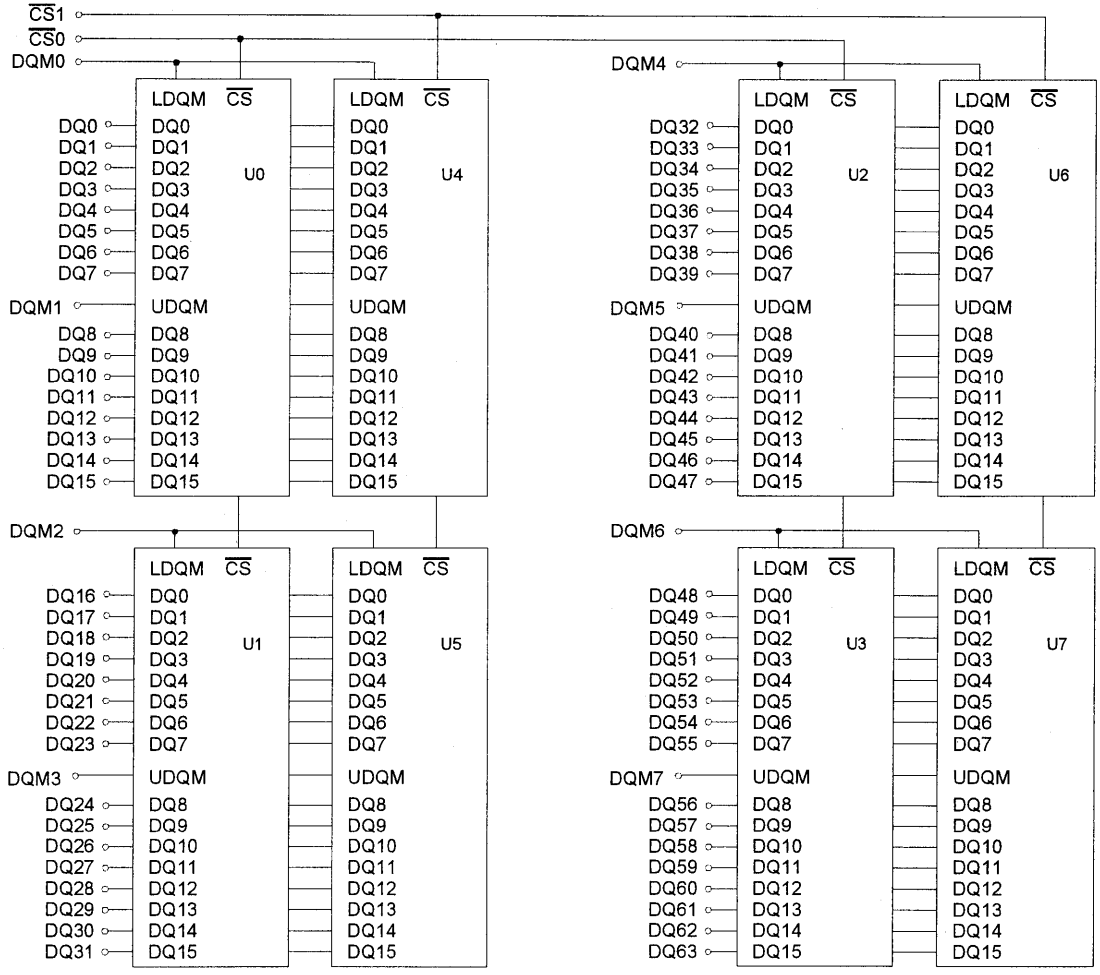
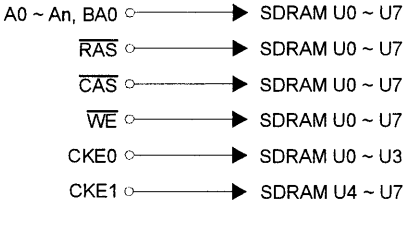
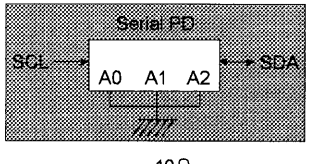
PIN CONFIGURATION DESCRIPTION

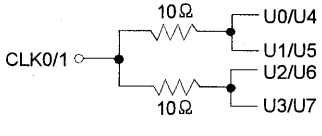
Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

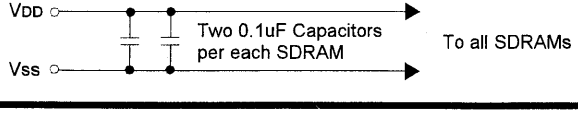
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS}$0 ~ $\overline{CS}$1)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

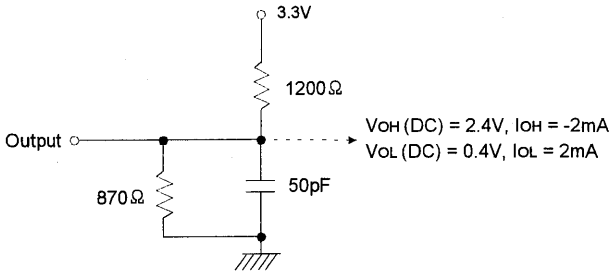
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS} \geq V_{IH}$(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

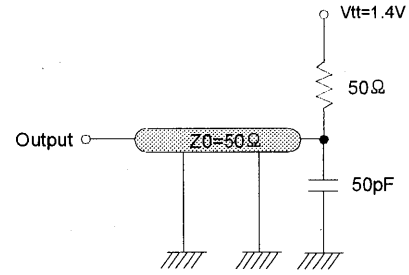
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S804AT- F8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S804AT- F0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S804AT- F2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12}~A_{11}, A_9~A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

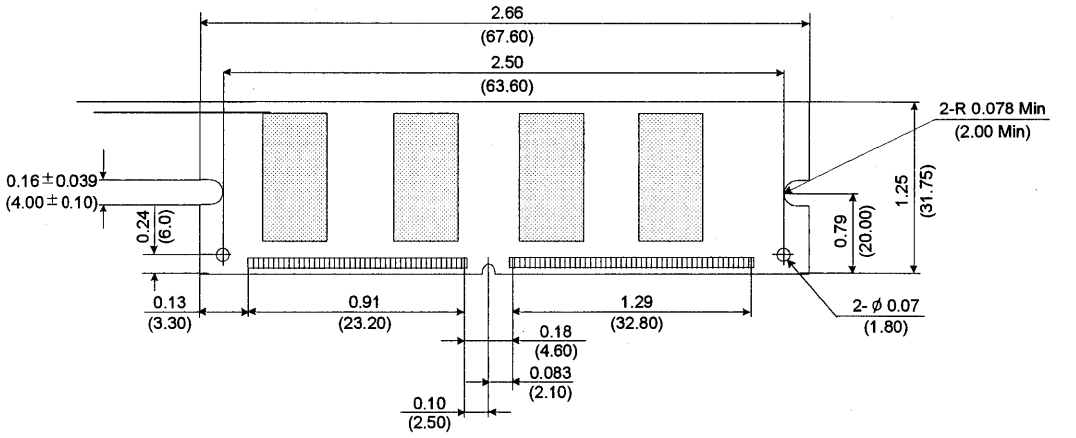
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

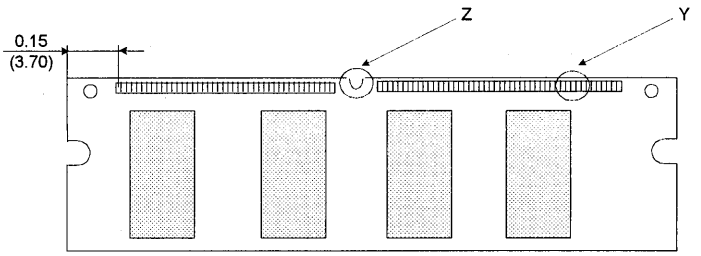
6. Burst stop command is valid at every burst length.

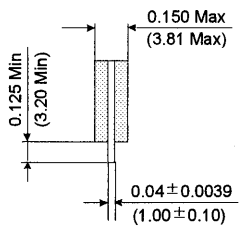
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

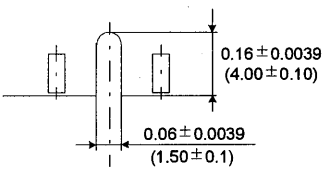
PACKAGE DIMENSIONS

Units : Inches (millimeters)

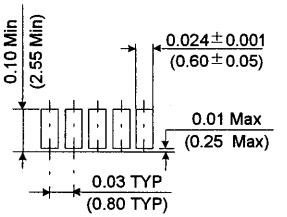








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4020AT

KMM466S824AT SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S824AT is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S824AT consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S824AT is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S824AT-F8	125MHz (8ns)
KMM466S824AT-F0	100MHz (10ns)
KMM466S824AT-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,250mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD					105	A8	106	**BA0**
13	DQ4	14	DQ36		**Voltage Key**			107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	**BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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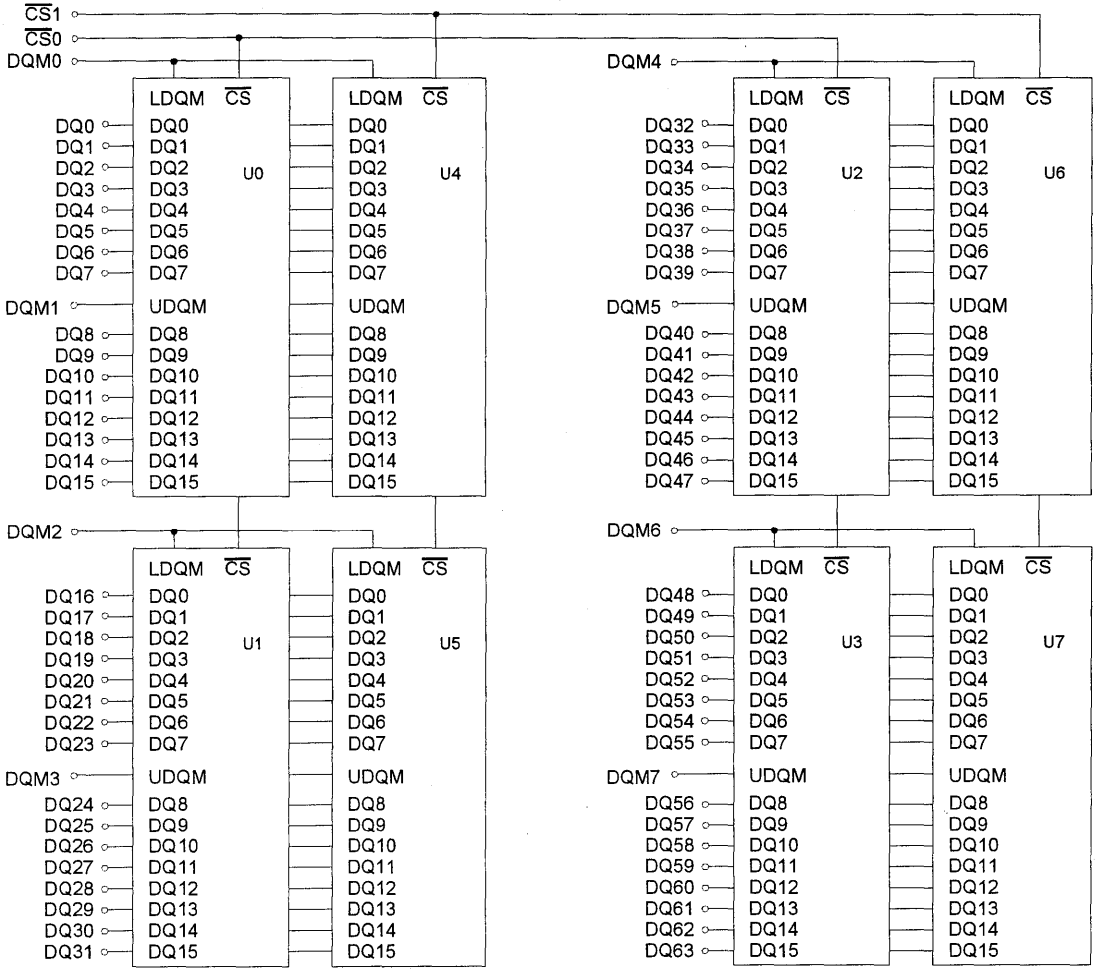
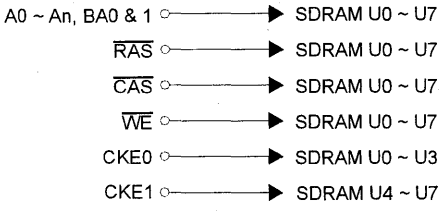
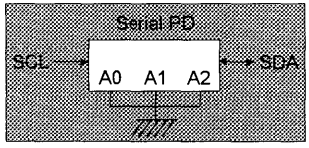
PIN CONFIGURATION DESCRIPTION

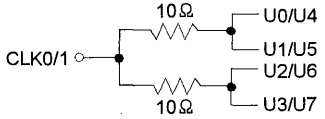
Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

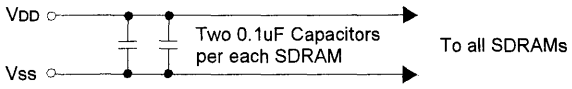
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

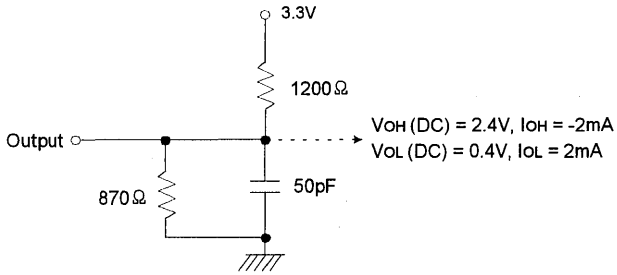
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

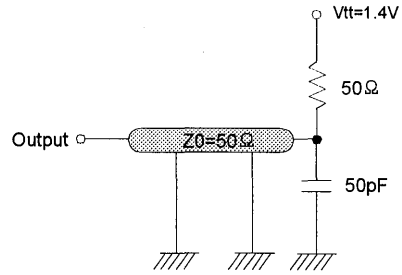
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70℃)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		$t_{RRD(min)}$	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	20	24	26	ns	1
Row precharge time		$t_{RP(min)}$	20	24	26	ns	1
Row active time		$t_{RAS(min)}$	48	50	60	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@Operation	$t_{RC(min)}$	70	80	90	ns	1
	@Auto refresh	$t_{RFC(min)}$	80	80	90	ns	1, 5
Last data in to new col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	1			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S824AT- F8 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S824AT- F0 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S824AT- F2 (Unit : number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

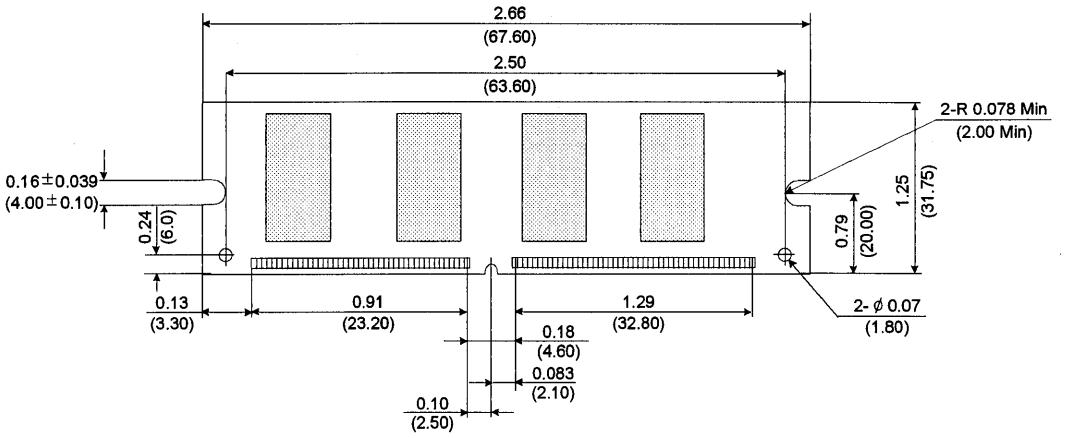
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11, A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

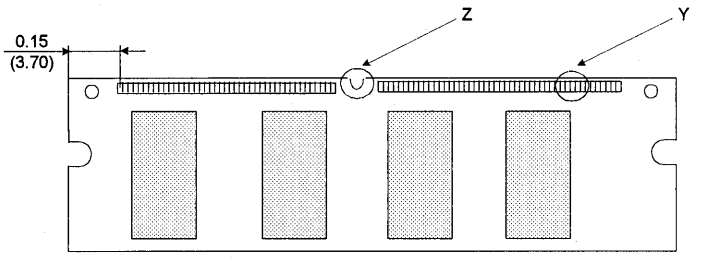
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

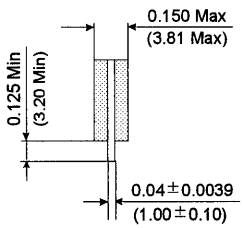
Note : 1. OP Code : Operand Code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

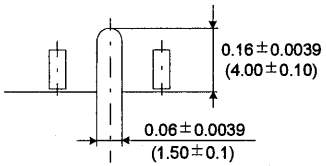
PACKAGE DIMENSIONS

Units : Inches (millimeters)

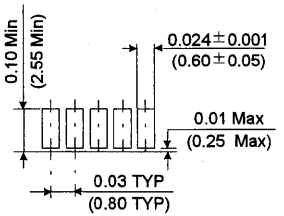








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4030AT

KMM466S804AT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 2Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S804AT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S804AT2 consists of eight CMOS 4M x 16 bit with 2banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S804AT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S804AT2-F8	125MHz (8ns)
KMM466S804AT2-F0	100MHz (10ns)
KMM466S804AT2-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,150mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	**BA0**
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	***BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

Pin Name	Function
A0 ~ A12	Address Input (multiplexed)
BA0	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

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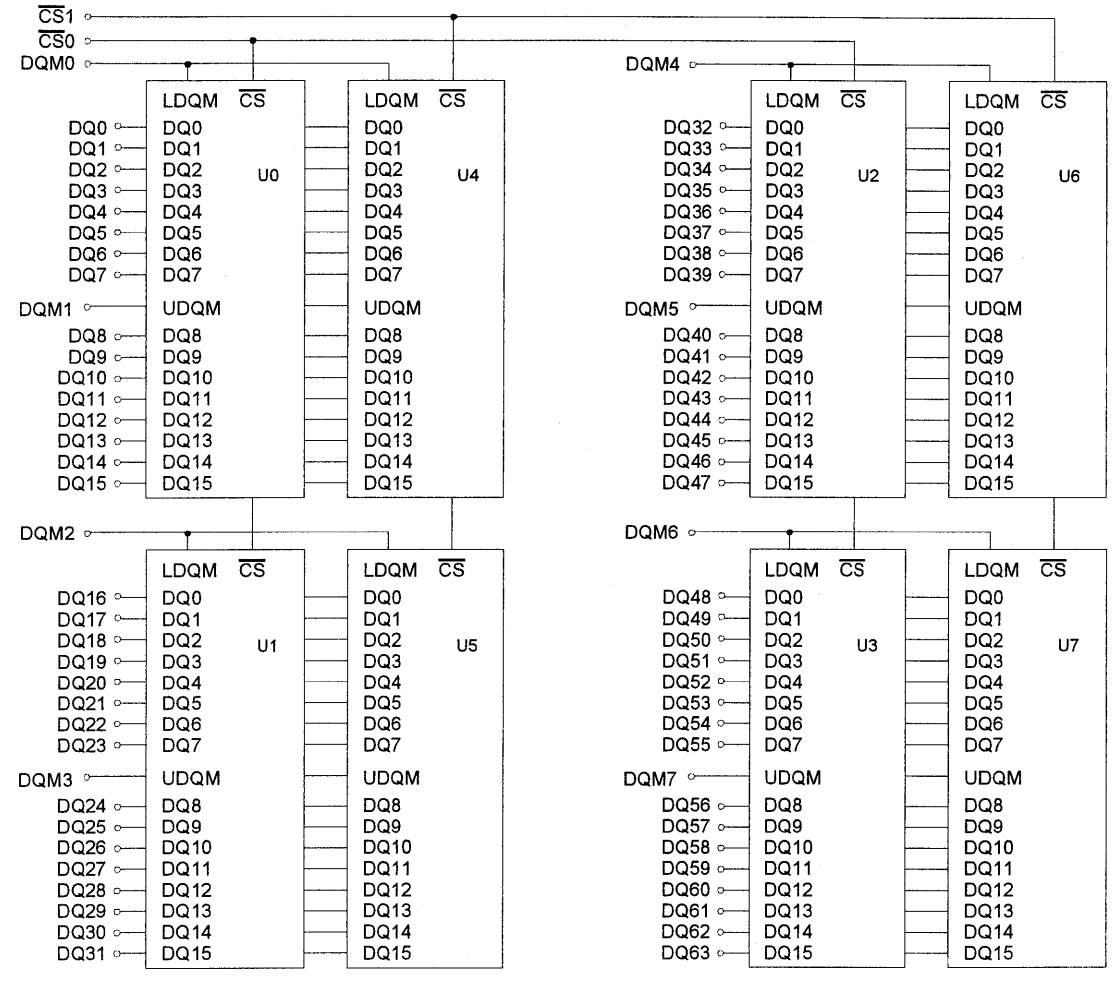
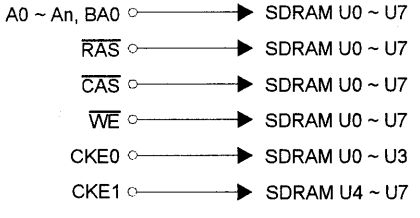
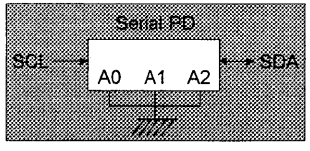
PIN CONFIGURATION DESCRIPTION

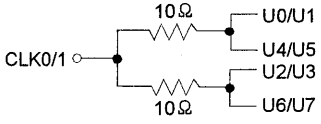
Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, column address : CA0 ~ CA7
BA0	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

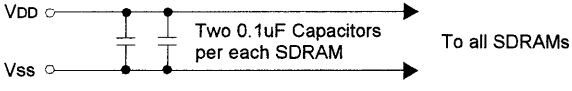
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12}, BA0)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

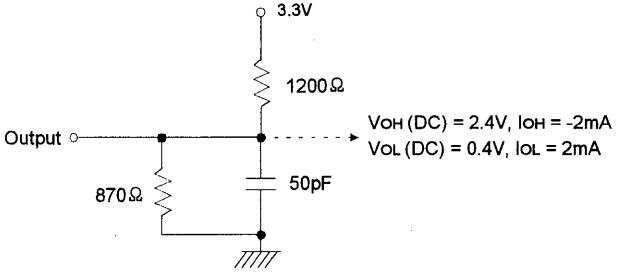
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version -8	Version -10	Version -12	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

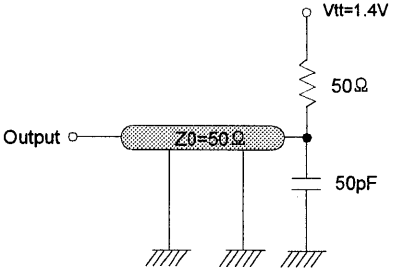
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S804AT2- F8

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S804AT2- F0

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S804AT2- F2

(Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA_0	A_{10}/AP	A_{12} ~ A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	Both Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{12}, BA_0 : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.
A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at both banks precharge state.

4. BA_0 : Bank select address.
If "Low" at read, write, row active and precharge, bank A is selected.
If "High" at read, write, row active and precharge, bank B is selected.
If A_{10}/AP is "High" at row precharge, BA_0 is ignored and both banks are selected.

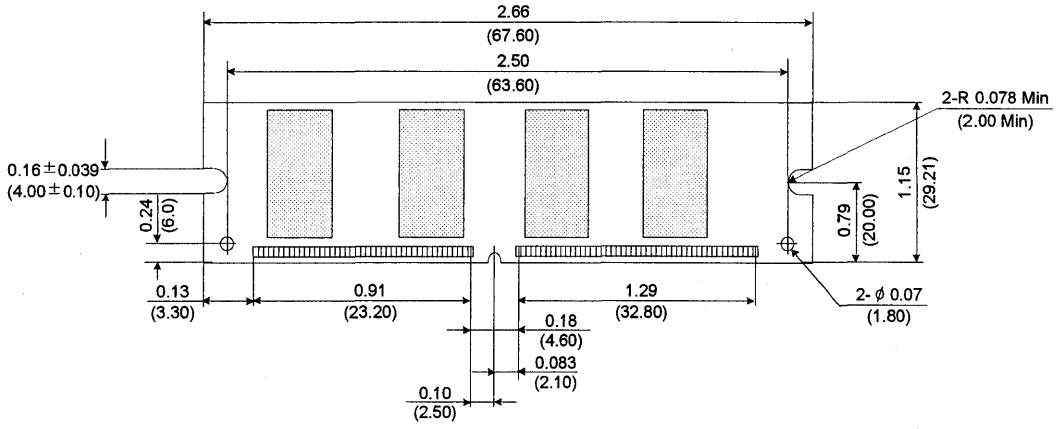
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.

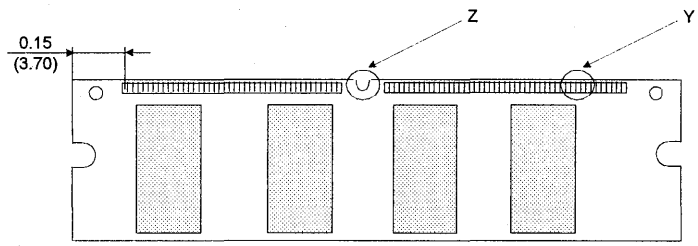
6. Burst stop command is valid at every burst length.

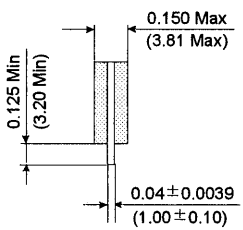
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

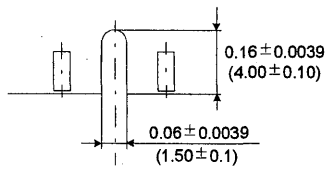
PACKAGE DIMENSIONS

Units : Inches (millimeters)

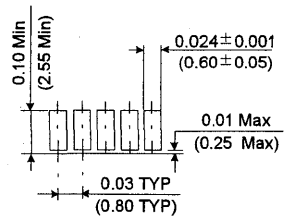








Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4020AT

KMM466S824AT2 SDRAM SODIMM

8Mx64 SDRAM SODIMM based on 4Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung KMM466S824AT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung KMM466S824AT2 consists of eight CMOS 4M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 1K or 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parellel for each SDRAM. The KMM466S824AT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

	Max Freq. (Speed)
KMM466S824AT2-F8	125MHz (8ns)
KMM466S824AT2-F0	100MHz (10ns)
KMM466S824AT2-F2	83MHz (12ns)

- Burst Mode Operation
- Auto & Self Refresh Capability (4096 cycles / 64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- WCBR cycle with address key programs
  Latency (Access from column address)
  Burst Length (1, 2, 4, 8 & Full page)
  Data Scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM
- PCB : **Height(1,150mil)**, double sided component

3

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	Voltage Key				105	A8	106	**BA0**
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37					109	A9	110	**BA1**
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	*A12	119	Vss	120	Vss
27	VDD	28	VDD	71	$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

PIN NAMES

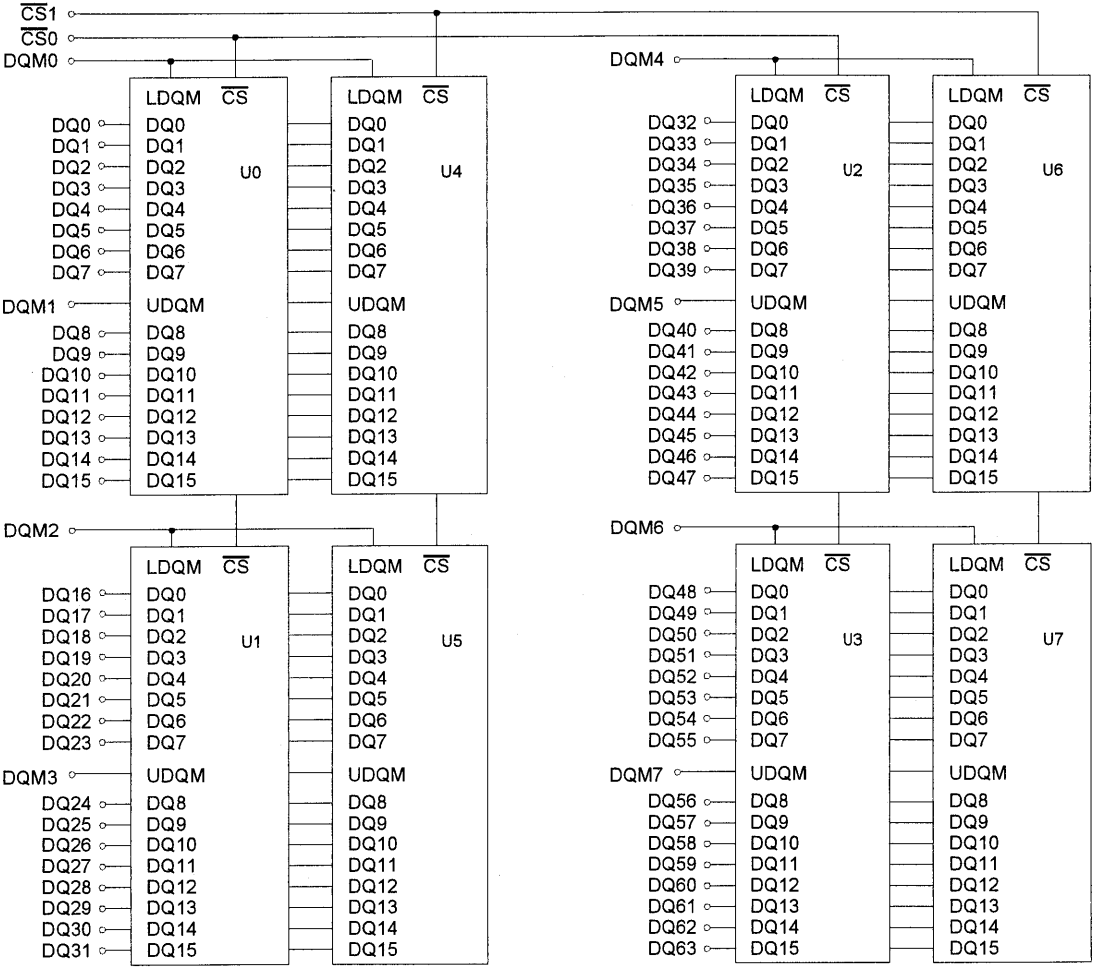
Pin Name	Function
A0 ~ A11	Address Input (multiplexed)
BA0 ~ BA1	Select Bank
DQ0 ~ DQ63	Data Input / Output
CLK0 ~ CLK1	Clock Input
CKE0 ~ CKE1	Clock Enable Input
$\overline{CS0}$ ~ $\overline{CS1}$	Chip Select Input
$\overline{RAS}$	Row Address Storbe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Data I/O
**SCL	Serial Clock
DU	Don' t use
NC	No Connection

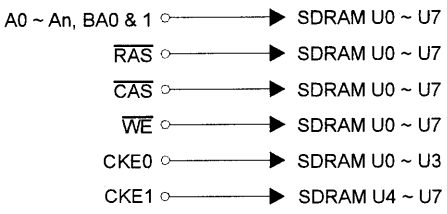
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

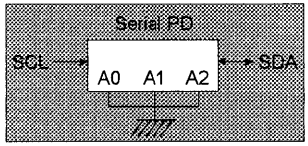
PIN CONFIGURATION DESCRIPTION

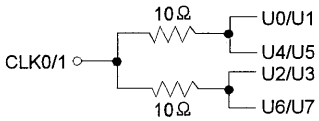
Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock Enable*	Masks system colck to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, column address : CA0 ~ CA7
BA0 ~ BA1	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the colck and masks the output. Blocks data input when DQM active. (Byte masking)
$DQ_{0 \sim 63}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.

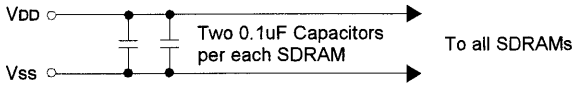
FUNCTIONAL BLOCK DIAGRAM











ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	8	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high votlage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-40	-	40	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note : 1. V_{IH} (max) = 4.6V AC for pulse width ≤10ns acceptable.
2. V_{IL} (min) = -1.5V AC for pulse width ≤10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V
4. Dout is disabled, 0V≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (T_A = 25℃, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11}, BA0 ~ BA1)	C_{IN1}	-	55	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	55	pF
Input capacitance (CKE0 ~ CKE1)	C_{IN3}	-	35	pF
Input capacitance (CLK0 ~ CLK1)	C_{IN4}	-	40	pF
Input capacitance ($\overline{CS}$0 ~ $\overline{CS}$1)	C_{IN5}	-	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	25	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	25	pF

DC CHARACTERISTICS

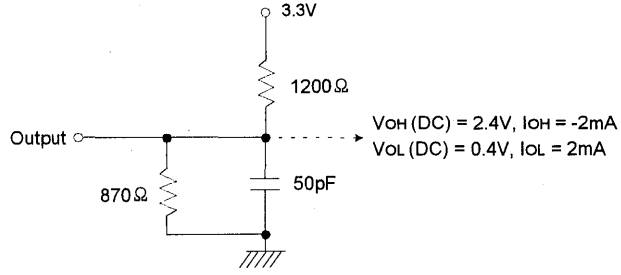
(Recommended operating condition unless otherwise noted, T_A = 0 to 70℃)

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-8	-10	-12		
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		660	600	520	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 15ns		16			mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		16				
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		240			mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		160				
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 15ns		48			mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞		48				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 15ns Input signals are changed one time during 30ns		360			mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable		240			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst 2 Banks activated t_{CCD} = 2CLKs	3	860	720	620	mA	1
			2	640	600	560		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		1,440			mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		4			mA	

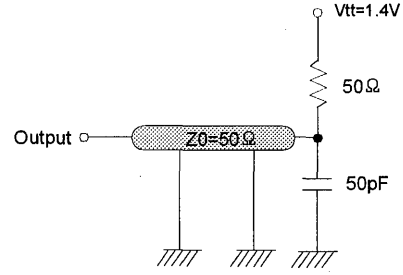
Note : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-8	-10	-12		
Row active to row active delay		tRRD(min)	16	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	24	26	ns	1
Row precharge time		tRP(min)	20	24	26	ns	1
Row active time		tRAS(min)	48	50	60	ns	1
		tRAS(max)	100			us	
Row cycle time	@Operation	tRC(min)	70	80	90	ns	1
	@Auto refresh	tRFC(min)	80	80	90	ns	1, 5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to row precharge		tRDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given tRFC after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	-8		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		13		15			
CLK to valid output delay	CAS latency=3	tSAC		6		7		8	ns	1, 2
	CAS latency=2			6		7		8		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		3		3		3			
CLK high pulse width		tCH	3		3.5		4		ns	3
CLK low pulse width		tCL	3		3.5		4		ns	3
Input setup time		tSS	2		2.5		3		ns	3
Input hold time		tSH	1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		8	ns	
	CAS latency=2			6		7		8		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)=1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KMM466S824AT2- F8 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KMM466S824AT2- F0 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KMM466S824AT2- F2 (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	1
75MHz (13.0ns)	3	7	5	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

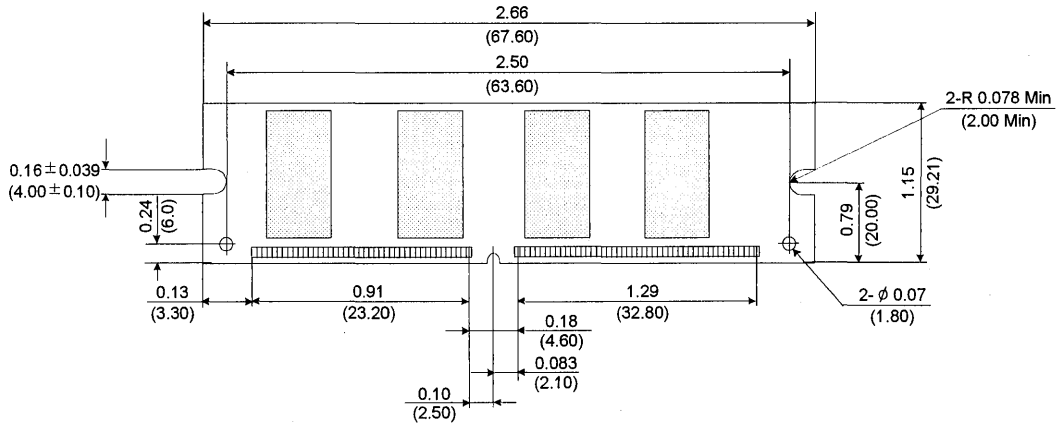
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

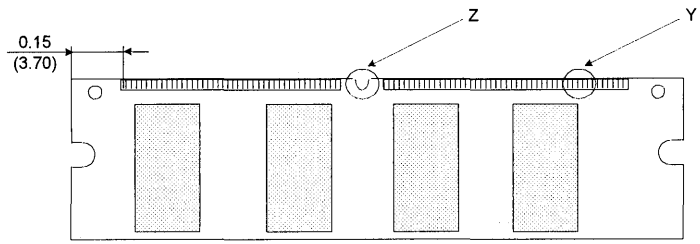
(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

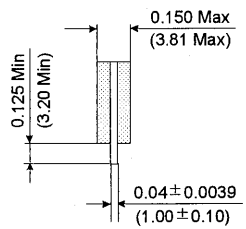
Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the assoiated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

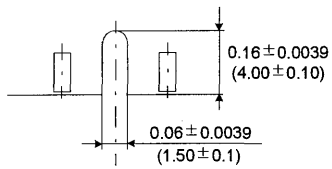
PACKAGE DIMENSIONS

Units : Inches (millimeters)

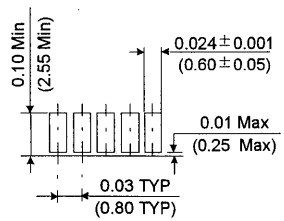








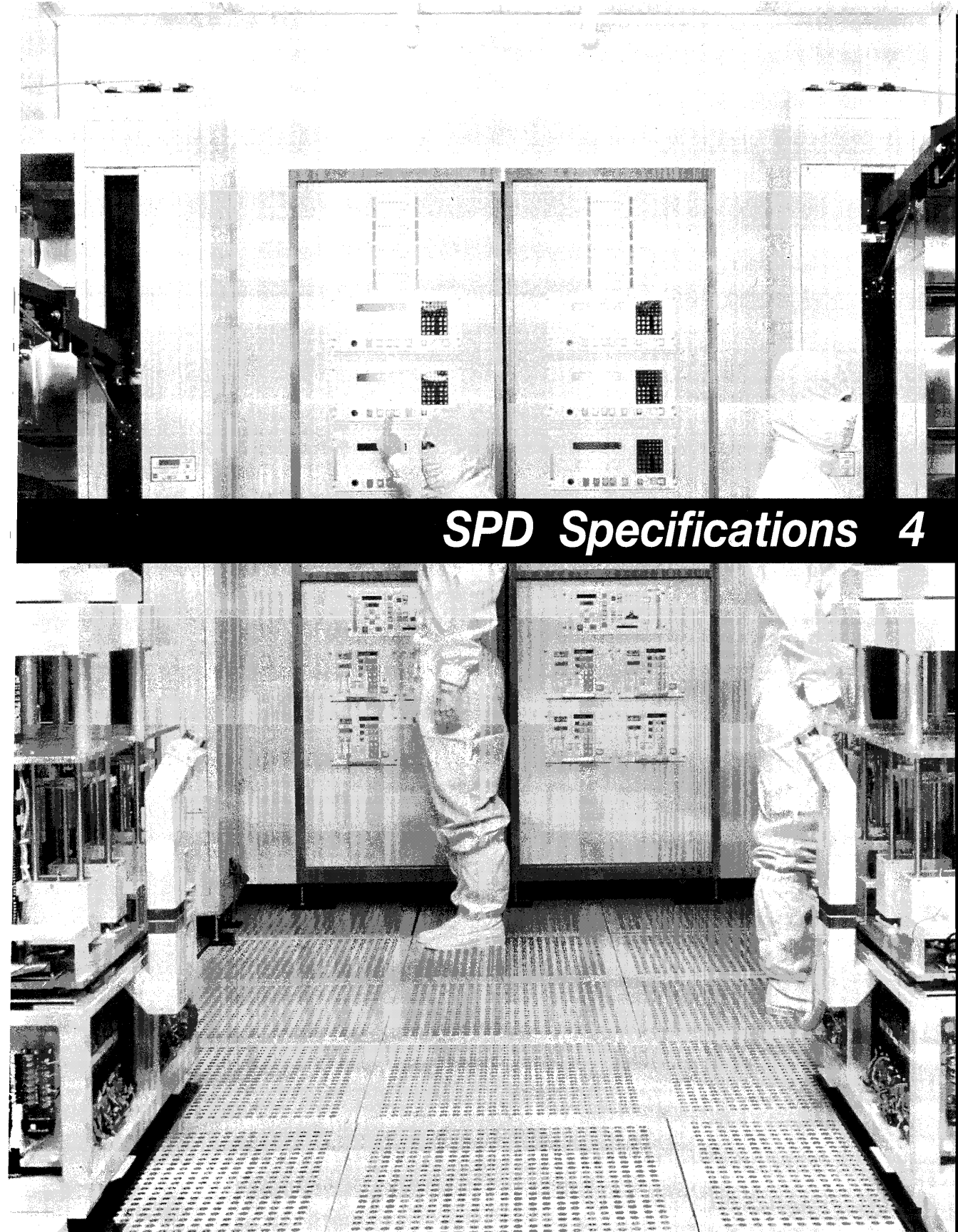
Detail Z



Detail Y

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 SDRAM, TSOP
SDRAM Part No. : KM416S4030AT



SPD Specifications 4

Unbuffered SDRAM DIMM(168pin) & SODIMM(144pin) SPD Specifications

REV. 1

March, 1997

Part I : General Information

General Description

This appendix describes the Presence Detects for Synchronous DRAM modules. These PD are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced ; that is, after the identification of the Fundamental memory type and before identification of whether there is any Super-srt Features presented.

Address Map

The following is the SPD address map for Synchronous DRAM. It describes where the individual LUT-Entries will be held in the serial EEPROM ;

Byte #	Function Described	Function Supported	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	1
1	Total # of bytes of SPD memory device	256 bytes (2K bit)	2
2	Fundamental memory type	SDRAM	
3	# of row address on this assembly	*	3
4	# of column address on this assembly	*	3
5	# of module banks on this assembly	*	3
6	Data width of this assembly	*	3
7	... Data width of this assembly	*	3
8	Voltage interface standard of this assembly	LVTTL	
9	SRAM cycle time from clock @CAS latency of 3	*	3
10	SRAM access time from clock @CAS latency of 3	*	3
11	DIMM configuration type	*	3
12	Refresh rate & type	15.625us, support self refresh	
13	Primary SDRAM width	*	3
14	Error checking SDRAM width	*	3
15	Minimum clock delay for back-to-back random column address	tCCD = 1 CLK	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	
17	SDRAM device attributes : # of banks on SDRAM device	*	3
18	SDRAM device attributes : CAS latency	*	3
19	SDRAM device attributes : CS latency	0 CLK	
20	SDRAM device attributes : Write latency	0 CLK	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing (RFU)	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all & auto precharge	
23	SDRAM cycle time @CAS latency of 2	*	3
24	SDRAM access time @CAS latency of 2	*	3
25	SDRAM cycle time @CAS latency of 1	*	3
26	SDRAM access time @CAS latency of 1	*	3

Byte #	Function Described	Function Supported	Note
27	Minimum row precharge time (=tRP)	*	3
28	Minimum row active to row active delay (=tRRD)	*	3
29	Minimum RAS to CAS delay (=RCD)	*	3
30	Minimum activate to precharge time (=tRAS)	*	3
31	Module bank density	*	3
32 ~ 61	Superset information (may be used in future)	-	4
62	SPD data revision code	2nd edition	
63	Checksum for bytes 0 ~ 62	*	3
64 ~ 71	Manufacturer JEDEC ID code	Samsung	
72	Manufacturing location	Onyang Korea	
73 ~ 90	Manufacturer part #	*	3
91 ~ 92	Manufacturer revision code	*	3
93	Manufacturing date (Week)	*	5
94	Manufacturing date (Year)	'97	6
95 ~ 98	Assembly serial #	-	4
99 ~ 125	Manufacturer specific data	-	7
126	System frequency for 66MHz	66MHz	
127	CAS latency for 66MHz	Support CL=2 & 3 for 66MHz	
128 +	Unused storage locations	-	7

<Note>

1. This will be 128 bytes for Synchronous DRAM.
2. This will be typically 256 bytes.
3. This field is different, module by module. So, if more detail information is needed, see the Part III, Individual SPD Datasheets.
4. Any specific data are not included in this field. Currently, this field is programmed by "00h".
5. This value is increased sequently from "01h" whenever the manufacturing week is varied.
6. This field describes manufacturing year and currently is programmed by "61h", which signifies '97.
7. Any specific data are not included in this field. Currently, this field is programmed by "FFh".

Part II : Detail Byte Assignments

Byte 0 : # of bytes written into serial memory at module manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any(optional) specific supplier information. The byte count includes the fields for all required and optional data ;

Number of bytes	Byte 0
Undefined	00h
1 bytes	01h
. . .	. . .
128 bytes	80h
. . .	. . .

Byte 1 : Total # of bytes of SPD memory device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes serial memory densities(in bytes) along with the corresponding descriptor ;

SPD memory size	Byte 1
RFU	00h
2 bytes	01h
. . .	. . .
128 bytes	07h
256 bytes	08h
. . .	. . .

Byte 2 : Fundamental memory type

This field describes the fundamental memory type (or technology) implemented on the module ;

fundamental memory type	Byte 2
Reserved	00h
Standard FPM DRAM	01h
EDO DRAM	02h
. . .	. . .
SDRAM	04h
. . .	. . .

Byte 3 : # of row address on this assembly

This field describes the number of row address bits in the SDRAM array. That is, the number of row address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of row address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the row addressing for bank1 and bits 7:4 describe the row addressing for bank2 ;

# of row address	Bits 3:0	Bits 7:4
Undefined	0h	0h
. . .	. . .	. . .
10	Ah	Ah
11	Bh	Bh
12	Ch	Ch
13	Dh	Dh
14	Eh	Eh
. . .	. . .	. . .

Byte 4 : # of column address on this assembly

This field describes the number of column address bits in the SDRAM array. That is, the number of column address bits does not include the bank selects(BA0, BA1). If the module has only one bank or if the module has two banks of the same size and organization, then bits 3:0 describe the number of column address bits and bits 7:4 are 0. If the module has two banks with different size/organization, then bits 3:0 describe the column addressing for bank1 and bits 7:4 describe the column addressing for bank2 ;

# of column address	Bits 3:0	Bits 7:4
Undefined	0h	0h
. . .	. . .	. . .
7	7h	7h
8	8h	8h
9	9h	9h
10	Ah	Ah
11	Bh	Bh
. . .	. . .	. . .

Byte 5 : # of module banks on this assembly

This field describes the number of module banks on the SDRAM module ;

# of module bank	Byte 5
Undefined	00h
1	01h
2	02h
. . .	. . .

Byte 6 & 7 : Data width of this assembly

Byte 6 & 7 are used to designate the data width of the module. The data width is presented as a 16bit word ; bit 0 of byte 6 becomes the LSB of the 16bit width identifier and bit 7 of byte 7 becomes MSB. Consequently, if the module has a data width less than 255 bits wide, byte 7 will be "00h". If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width ;

# of row address	Byte 6	Byte 7
Undefined	00h	00h
. . .	. . .	. . .
32	20h	00h
36	24h	00h
. . .	. . .	. . .
64	40h	00h
72	48h	00h
80	50h	00h
. . .	. . .	. . .

Byte 8 : Voltage interface standard of this assembly

This field describes the SDRAM module voltage & interface ;

Voltage & interface	Byte 8
5.0V/TTL	00h
LVTTL	01h
HSTL 1.5V	02h
SSTL 3.3V	03h
SSTL 2.5V	04h
TBD	05h
TBD	06h
. . .	. . .
New table	FFh

Byte 9 : SDRAM cycle time from clock @CAS latency of 3

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1(as indicated in byte 18), this byte defines tCC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 10 : SDRAM access time from clock @CAS latency of 3

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 3. The byte is broken into two nibbles : the higher order nibble(bit4 ~7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different access time @CAS latency of 3, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 11 : DIMM configuration type

This field describes the module error detection and correction scheme ;

Error detect & correct	Byte 11
None	00h
Parity	01h
ECC	02h
. . .	. . .
TBD	FFh

Byte 12 : Refresh rate & type

This field describes the module's refresh rate and type. The bit 7 is especially used for self refresh flag ; if SDRAM supports self refresh, bit 7 is "1" and if not, bit 7 is "0" ;

Refresh rate/type	Byte 12
Normal(15.625us)	00h
. . .	. . .
Self refresh	
Normal(15.625us)	80h
. . .	. . .
Extended(2x) ... 31.3us	83h
. . .	. . .

Byte 13 : Primary SDRAM width

This field describes the data width of the primary SDRAM components used on the module. The primary SDRAM is that which is used for data ;

SDRAM data width	Byte 13
Undefined	00h
. . .	. . .
4	04h
. . .	. . .
8	08h
. . .	. . .
16	10h
. . .	. . .
127	7Fh

Byte 14 : Error checking SDRAM width

If the module incorporates error checking and if the primary data SDRAM does not include these bits ; i.e. there are separate error checking SDRAMs, then the error checking SDRAM width is expressed in this byte ;

ECC SDRAM data width	Byte 14
Undefined	00h
. . .	. . .
4	04h
. . .	. . .
8	08h
. . .	. . .
16	10h
. . .	. . .
127	7Fh

Byte 15 : Minimum clock delay for back-to-back random column addresses

Number of clocks	Byte 15
Undefined	00h
1	01h
2	02h
. . .	. . .
256	FFh

Byte 16 : SDRAM device attributes : Burst lengths supported

This field describes various burst lengths supported. If the burst length is supported, then the corresponding bit is "1". Samsung value for this field is "8Fh" because the burst lengths of 1, 2, 4, 8 and full page are supported ;

Burst length supported	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	Full page	TBD	TBD	TBD	8	4	2	1

Byte 17 : SDRAM device attributes : Number of banks on SDRAM device

This field describes the number of banks internal to the SDRAM devices ;

# of banks in component	Byte 17
Undefined	00h
1	01h
2	02h
. . .	. . .
256	FFh

Byte 18 : SDRAM device attributes : CAS latency

This field describes which CAS latencies are supported for the module. If the bit is "1", then that CAS latency is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	7	6	5	4	3	2	1

Byte 19 : SDRAM device attributes : CS latency

This field describes which CS latencies are acceptable for the module. If the bit is "1", then that CS latency is supported. Samsung value for this field is "01h" because CS latency of 0 is supported ;

CAS latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 20 : SDRAM device attributes : WE latency

This field describes which WE latencies are accptable for the module. If the bit is "1", then that WE latency is supported. Samsung value for this field is "01h" because WE latency of 0 is supported ;

WE latency	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	6	5	4	3	2	1	0

Byte 21 : SDRAM module attributes: General

This field describes various aspects of the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "00h" ;

Module attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	redundant addressing	differential CLK input	registered DQMB input	buffered DQMB input	On-card PLL	registered Add/Cntr input	buffered Add/Cntr input

Byte 22 : SDRAM device attributes : General

This field describes various aspects of the SDRAMs on the module. If the aspect is TRUE, then the corresponding bit is "1". Samsung value for this field is "0Eh" ;

Device attributes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If supported, the bit is "1"	TBD	TBD	upper Vdd tolerance 0=10% 1=5%	lower Vdd tolerance 0=10% 1=5%	support BRSW	support precharge all	support auto precharge	support early RAS precharge

Byte 23 : SDRAM cycle time from clock @CAS latency of 2

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 24 : SDRAM access time from clock @CAS latency of 2

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 2. The byte is broken into two nibbles : the higher order nibble(bit4 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order nibble has a granularity of 1/10ns and is added to the value of the higher nibble. Samsung SDRAM has the different cycle time @CAS latency of 2, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 25 : SDRAM cycle time from clock @CAS latency of 1

This field describes the total minimum cycle time(clock period) for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tCC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the cycle time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different cycle time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 26 : SDRAM access time from clock @CAS latency of 1

This field describes the total maximum clock to data out for the SDRAM. For example, if the SDRAM supports CAS latency of 3, 2 and 1 (as indicated in byte 18), this byte defines tSAC for CAS latency of 1. The byte is broken into two pieces : the higher order piece(bit2 ~ 7) designates the access time to a granularity of 1ns ; the value presented by the lower order piece has a granularity of 1/4ns and is added to the value of the higher piece. Samsung SDRAM has the different access time @CAS latency of 1, generation by generation. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 27 : Minimum row precharge time (=tRP)

Bit 0 ~ 5 of this byte describe the precharge to active minimum(=tRP) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 28 : Minimum row active to row active delay (=tRRD)

Bit 0 ~ 5 of this byte describe the minimum row activate to row activate delay(=tRRD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 29 : Minimum RAS to CAS delay (=tRCD)

Bit 0 ~ 5 of this byte describe the minimum RAS to CAS delay(=tRCD) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 30 : Minimum activate to precharge time (=tRAS)

Bit 0 ~ 5 of this byte describe the minimum activate to precharge time(=tRAS) using 1ns granularity. Bits 7 and 6 are reserved for future use. Samsung SDRAM has the different value, generation by generation and binning by binning. So, more detail information is needed, please refer to the Part III, Individual SPD Datasheets.

Byte 31 : Module bank density

This field describes the density of each physical bank on the SDRAM DIMM. This field will have at least one bit to "1" to represent at least one bank density. If there are more than one bank on the module(as indicated in byte 5) and they have the same density, then only one bit is set in this field. If the module has more than one bank of different sizes, then more than one bit will be set for each density represented ;

Module bank density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
If YES, the bit is "1"	512MByte	256MByte	128MByte	64MByte	32MByte	16MByte	8MByte	4MByte

Byte 32 ~ 61 : Superset information (may be used in future)

This field are reserved for superset information. Currently, these fields are programmed by "00h" because the standardization for these fields are not fixed yet.

Byte 62 : SPD data revision code

This field identifies the SDRAM DIMM SPD data revision to which the module conforms. Currently, this field is programmed by "01h"

SPD data revision code	Byte 62
Initial release	00h
2nd edition	01h
3rd edition	02h
. . .	. . .

Byte 63 : Checksum for bytes 0 ~ 62

This field is the checksum for bytes 0 through 62. Currently, this byte contains the value of the low 8bits of arithmetic sum of bytes 0 through byte 62.

Byte 64 ~ 71 : Manufacturer JEDEC ID code

This field describes the manufacturer JEDEC ID code per EIA/JEP106-E. The unique code for Samsung is "CBh" only for byte64 and another bytes, bytes 65 ~ 71 are programmed by "00h" ;

JEDEC ID code	Byte 64	Byte 65	Byte 66	Byte 67	Byte 68	Byte 69	Byte 70	Byte 71
Samsung	CEh	00h	00h	00h	00h	00h	00h	00h

Byte 72 : Manufacturing location

This field identifies the manufacturing location and is programmed by binary code not ASCII ;

Manufacturing location	Byte 72
Kiheung Korea	00h
Onyang Korea	01h
. . .	. . .

Byte 73 ~ 90 : Manufacturer part # (ASCII code)

This fields describe the manufacturer part number and are programmed by ASCII code not binary.

Byte 73 : Samsung memory (ASCII code)

Samsung Korea	Byte 73
K	4Bh
. . .	. . .

Byte 74 : Samsung memory (ASCII code)

Samsung Korea	Byte 74
M	4Dh
. . .	. . .

Byte 75 : Samsung module (ASCII code)

Samsung Korea	Byte 75
M	4Dh
. . .	. . .

Byte 76 : Memory type (ASCII code)

Memory type	Byte 76
3 (168 or 200pin DIMM)	33h
4 (144pin SODIMM)	34h
. . .	. . .

Byte 77 ~ 79 : Data bits (ASCII code)

Data bits	Byte 77	Byte 78	Byte 79
64(x64, 168pin, buffered)	20h	36h	34h
. . .	. . .	. . .	. . .
66(x64, 168pin, unbuffered & SPD)	20h	36h	36h
67(x64, 168pin, unbuffered, PLL & SPD)	20h	36h	37h
. . .	. . .	. . .	. . .
72(x72, 168pin, buffered)	20h	37h	32h
. . .	. . .	. . .	. . .
74(x72, 168pin, unbuffered & SPD)	20h	37h	34h
75(x72, 168pin, register, PLL & SPD)	20h	37h	35h
. . .	. . .	. . .	. . .
79(x72, 200pin, register, PLL)	20h	37h	39h

Byte 80 : Mode & operating voltage (ASCII code)

Mode & operating voltage	Byte 80
F (EDO 3.3V)	46h
S (Sync. DRAM)	53h
. . .	. . .

Byte 81 ~ 82 : Module density (ASCII code)

Module density	Byte 81	Byte 82
1M	20h	31h
2M	20h	32h
4M	20h	34h
8M	20h	38h
16M	31h	36h
. . .	. . .	. . .

Byte 83 : Refresh, # of banks in Comp. & interface (ASCII code)

Features	Byte 83
0 (4K ref., 2banks, LVTTL)	30h
1 (2K ref., 2banks, LVTTL)	31h
2 (4K ref., 4banks, LVTTL)	32h
. . .	. . .

Byte 84 : Composition component (ASCII code)

Composition component	Byte 84
0 (x4)	30h
3 (x8)	31h
4 (x16)	32h
. . .	. . .

Byte 85 : Component revision (ASCII code)

Component revision	Byte 85
Blank (Mother die)	20h
A (1st Rev.)	41h
B (2nd Rev.)	42h
. . .	. . .

Byte 86 : Package type (ASCII code)

Package type	Byte 86
T (400mil TSOP II - forward)	54h

Byte 87 : PCB revision (ASCII code)

This field is used for the expression of PCB height and distinction between new JEDEC DIMM & old JEDEC DIMM. The marked by "N" refers to 16M SDRAM based 168pin unbuffered DIMM only ;

PCB revision	Byte 87
Blank	54h
N	4Eh
1	31h
2	32h
3	33h
. . .	. . .

Byte 88 : Hyphen (ASCII code)

Hyphen	Byte 88
" - "	2Dh

Byte 89 : Power (ASCII code)

Power	Byte 89
G (Auto & self Ref., normal power)	47h
F (Auto & self Ref., low power)	46h

Byte 90 : Minimum cycle time (ASCII code)

Minimum cycle time	Byte 90
7 (7ns=143MHz)	37h
8 (8ns=125MHz)	38h
. . .	. . .
0 (10ns=100MHz)	30h
. . .	. . .
2 (12ns=83MHz)	32h
. . .	. . .

Byte 91 : Manufacturer revision code for PCB (ASCII code)

This field is refered to the module PCB revision and has the same programming code with byte 87.

Byte 92 : Manufacturer revision code for component (ASCII code)

This field is refered to the component revision and has the same programming code with byte 85.

Byte 93 : Manufacturing date ; Week (Binary code)

This field describes manufacturing week and is increased sequently from "01h" whenever manufacturing week is varied.

Byte 94 : Manufacturing date ; Year (Binary code)

This field describes manufacturing year and currently is programmed by "61h", which signifies '97.

Byte 95 ~ 98 : Assembly serial number (Binary code)

These fields describe assembly serial number. But, all of the Samsung modules are controlled by another way, not assembly serial #. Currently, this field is programmed by "00h".

Byte 99 ~ 125 : Manufacturer specific data (may be used in future)

Any specific data are not included in this field yet. Currently, this field is programmed by "FFh".

Byte 126 : System frequency for 66MHz

System frequency	Byte 126
66MHz	66h

Byte 127 : CAS latency for 66MHz

CAS latency for 66MHz	Byte 127
Support 2 & 3 for 66MHz	06h

Byte 128 ~ 255 : Unused storage locations

Any specific data are not included in this field yet. Currently, this field is programmed by "FFh".

Part III : Individual SPD Datasheets

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64M SDRAM based 168pin unbuffered SDRAM DIMM

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16M SDRAM based 144pin unbuffered SDRAM SODIMM

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64M SDRAM based 144pin unbuffered SDRAM SODIMM

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KMM366S104BTN-G8/G0/G2

- Organization : 1Mx64
- Composition : 1Mx16 *4
- Used component part # : KM416S1020BT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 8MB			02h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			49h	B7h	45h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	1			31h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S203BTN-G8/G0/G2

- Organization : 2Mx64
- Composition : 2Mx8 *8
- Used component part # : KM48S2020BT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			44h	B2h	40h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module) -	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S204BTN-G8/G0/G2

- Organization : 2Mx64
- Composition : 1Mx16 *8
- Used component part # : KM416S1020BT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 8MB			02h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			4Ah	B8h	46h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S400BTN-G8/G0/G2

- Organization : 4Mx64
- Composition : 4Mx4 *16
- Used component part # : KM44S4020BT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			45h	B3h	41h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S403BT2-G8/G0/G2

- Organization : 4Mx64
- Composition : 2Mx8 *16
- Used component part # : KM48S2020BT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			45h	B3h	41h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	2			32h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	2			32h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S403BTN-G8/G0/G2

- Organization : 4Mx64
- Composition : 2Mx8 *16
- Used component part # : KM48S2020BT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			45h	B3h	41h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S203BTN-G8/G0/G2

- Organization : 2Mx72
- Composition : 2Mx8 *9
- Used component part # : KM48S2020BT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			56h	C4h	52h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S400BTN-G8/G0/G2

- Organization : 4Mx72
- Composition : 4Mx4 *18
- Used component part # : KM44S4020BT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	x4			04h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			53h	C1h	4Fh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S403BTN-G8/G0/G2

- Organization : 4Mx72
- Composition : 2Mx8 *18
- Used component part # : KM48S2020BT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			57h	C5h	53h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	N			4Eh			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	N			4Eh			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S404AT-G8/G0/G2

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : KM416S4020AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	t_{CCD} = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Ch	EAh	5Ch	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S424AT-G8/G0/G2

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : KM416S4030AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & single sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S803AT-G8/G0/G2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8020AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S823AT-G8/G0/G2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8030AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S804AT-G8/G0/G2

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4020AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S824AT-G8/G0/G2

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4030AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S1600AT-G8/G0/G2

- Organization : 16Mx64
- Composition : 16Mx4 *16
- Used component part # : KM44S16020AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 128MB			20h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			9Ah	F8h	6Ah	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S1620AT-G8/G0/G2

- Organization : 16Mx64
- Composition : 16Mx4 *16
- Used component part # : KM44S16030AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 128MB			20h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			9Bh	F9h	6Bh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S1603AT-G8/G0/G2

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : KM48S8020AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	t_{CCD} = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=t_{RP})	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (t_{RRD})	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=t_{RCD})	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=t_{RAS})	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM366S1623AT-G8/G0/G2

- Organization : 16Mx64
- Composition : 8Mx8 *16
- Used component part # : KM48S8030AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Fh	EDh	5Fh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S803AT-G8/G0/G2

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : KM48S8020AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			9Fh	FDh	6Fh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S823AT-G8/G0/G2

- Organization : 8Mx72
- Composition : 8Mx8 *9
- Used component part # : KM48S8030AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			A0h	FEh	70h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S1600AT-G8/G0/G2

- Organization : 16Mx72
- Composition : 16Mx4 *18
- Used component part # : KM44S16020AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	x4			04h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 128MB			20h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			A8h	06h	78h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S1620AT-G8/G0/G2

- Organization : 16Mx72
- Composition : 16Mx4 *18
- Used component part # : KM44S16030AT-G8/G10/G12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	10			0Ah			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x4			04h			
14	Error checking SDRAM width	x4			04h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 128MB			20h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			A9h	07h	79h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	0			30h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S1603AT-G8/G0/G2

- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : KM48S8020AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			0Bh			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			A0h	FEh	70h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM374S1623AT-G8/G0/G2

- Organization : 16Mx72
- Composition : 8Mx8 *18
- Used component part # : KM48S8030AT-G8/G10/G12
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			0Bh			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	72 bits			48h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	ECC			02h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	x8			08h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			A1h	FFh	71h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	3			33h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	7			37h			
79	..... Manufacturer part # (Data bits)	4			34h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	1			31h			
82	..... Manufacturer part # (Module density)	6			36h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	G			47h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S104BT-F8/F0/F2

- Organization : 1Mx64
- Composition : 1Mx16 *4
- Used component part # : KM416S1020BT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms:
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 8MB			02h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			49h	B7h	45h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	1			31h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S203BT-F8/F0/F2

- Organization : 2Mx64
- Composition : 2Mx8 *8
- Used component part # : KM48S2020BT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 16MB			04h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			44h	B2h	40h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S204BT-F8/F0/F2

- Organization : 2Mx64
- Composition : 1Mx16 *8
- Used component part # : KM416S1020BT-F8/F10/F12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms:
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	11			0Bh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	1, 2 & 3			07h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	7ns	8ns	9ns	70h	80h	90h	2
25	SDRAM cycle time @CAS latency of 1	24ns	26ns	30ns	60h	68h	78h	2
26	SDRAM access time @CAS latency of 1	20ns	22ns	24ns	50h	58h	60h	2
27	Minimum row precharge time (=tRP)	20ns	26ns	30ns	14h	1Ah	1Eh	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	24ns	26ns	30ns	18h	1Ah	1Eh	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 8MB			02h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			4Ah	B8h	46h	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	2			32h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	B			42h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S404AT-F8/F0/F2

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : KM416S4020AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Ch	EAh	5Ch	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S424AT-F8/F0/F2

- Organization : 4Mx64
- Composition : 4Mx16 *4
- Used component part # : KM416S4030AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	4			34h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S803AT-F8/F0/F2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8020AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S823AT-F8/F0/F2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8030AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S803AT2-F8/F0/F2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8020AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 2 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	2			32h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	2			32h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S823AT2-F8/F0/F2

- Organization : 8Mx64
- Composition : 8Mx8 *8
- Used component part # : KM48S8030AT-F8/F10/F12
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	9			09h			1
5	# of module banks on this assembly	1 bank			01h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x8			08h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	1 bank of 64MB			10h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	3			33h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	2			32h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	2			32h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S804AT-F8/F0/F2

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4020AT-F8/F10/F12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S824AT-F8/F0/F2

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4030AT-F8/F10/F12
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,250mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	Blank			20h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	Blank (Mother PCB)			20h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S804AT2-F8/F0/F2

- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4020AT-F8/F10/F12
- # of banks in module : 2 banks
- # of banks in component : 2 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	2 banks			02h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Dh	EBh	5Dh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	0			30h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	2			32h			
88	Manufacturer part # (Hyphen)	" - "			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	2			32h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

KMM466S824AT2-F8/F0/F2

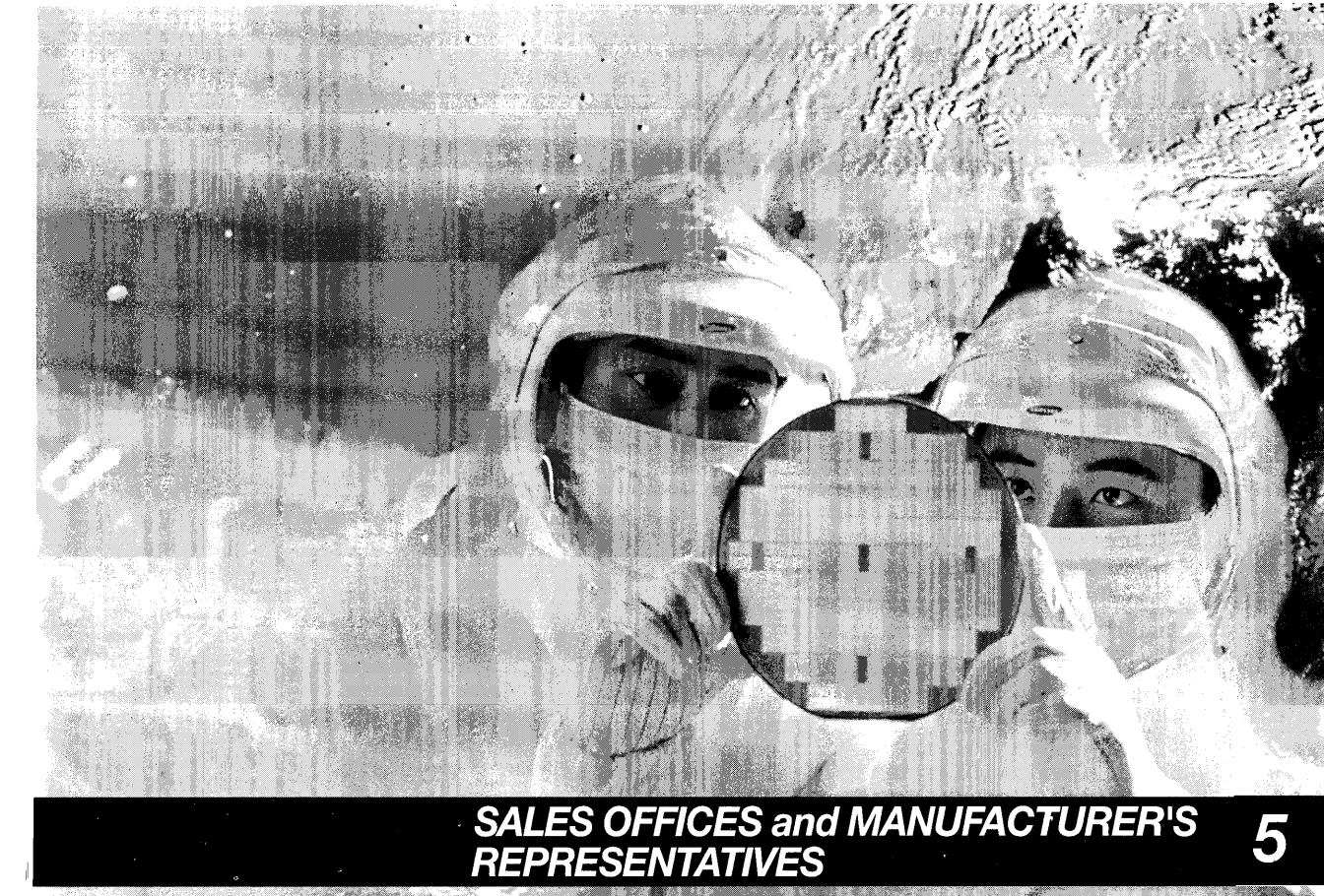
- Organization : 8Mx64
- Composition : 4Mx16 *8
- Used component part # : KM416S4030AT-F8/F10/F12
- # of banks in module : 2 banks
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
0	# of bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM			04h			
3	# of row address on this assembly	12			0Ch			1
4	# of column address on this assembly	8			08h			1
5	# of module banks on this assembly	2 banks			02h			
6	Data width of this assembly	64 bits			40h			
7	..... Data width of this assembly	-			00h			
8	Voltage interface standard of this assembly	LVTTL			01h			
9	SDRAM cycle time from clock @CAS latency of 3	8ns	10ns	12ns	80h	A0h	C0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	7ns	8ns	60h	70h	80h	2
11	DIMM configuraion type	Non parity			00h			
12	Refresh rate & type	15.625us, support self refresh			80h			
13	Primary SDRAM width	x16			10h			
14	Error checking SDRAM width	None			00h			
15	Minimum clock dealy for back-to-back random column address	tCCD = 1CLK			01h			
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page			8Fh			
17	SDRAM device attributes : # of banks on SDRAM device	4 banks			04h			
18	SDRAM device attributes : CAS latency	2 & 3			06h			
19	SDRAM device attributes : CS latency	0 CLK			01h			
20	SDRAM device attributes : Write latency	0 CLK			01h			
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing			00h			
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge			0Eh			
23	SDRAM cycle time @CAS latency of 2	12ns	13ns	15ns	C0h	D0h	F0h	2
24	SDRAM access time @CAS latency of 2	6ns	7ns	8ns	60h	70h	80h	2
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h	
26	SDRAM access time @CAS latency of 1	-	-	-	00h	00h	00h	
27	Minimum row precharge time (=tRP)	20ns	24ns	26ns	14h	18h	1Ah	
28	Minimum row active to row active delay (tRRD)	16ns	20ns	24ns	10h	14h	18h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	24ns	26ns	14h	18h	1Ah	
30	Minimum activate precharge time (=tRAS)	48ns	50ns	60ns	30h	32h	3Ch	
31	Module bank density	2 banks of 32MB			08h			
32~61	Superset information (maybe used in future)	-			00h			
62	SPD data revision code	2nd edition			01h			
63	Checksum for bytes 0 ~ 62	-			8Eh	ECh	5Eh	

Byte #	Function Described	Function Supported			Hex value			Note
		-8	-10	-12	-8	-10	-12	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65~71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Samsung memory)	K			4Bh			
74	Manufacturer part # (Samsung memory)	M			4Dh			
75	Manufacturer part # (Memory module)	M			4Dh			
76	Manufacturer part # (Memory type & edge connector)	4			34h			
77	Manufacturer part # (Data bits)	Blank			20h			
78	..... Manufacturer part # (Data bits)	6			36h			
79	..... Manufacturer part # (Data bits)	6			36h			
80	Manufacturer part # (Mode & operating voltage)	S			53h			
81	Manufacturer part # (Module density)	Blank			20h			
82	..... Manufacturer part # (Module density)	8			38h			
83	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2			32h			
84	Manufacturer part # (Compositon component)	4			34h			
85	Manufacturer part # (Component revision)	A			41h			
86	Manufacturer part # (Package type)	T			54h			
87	Manufacturer part # (PCB revision)	2			32h			
88	Manufacturer part # (Hyphen)	"-"			2Dh			
89	Manufacturer part # (Power)	F			46h			
90	Manufacturer part # (Minimum cycle time)	8	0	2	38h	30h	32h	
91	Manufacturer revision code (For PCB)	2			32h			
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)			41h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	'97			61h			
95~98	Assembly serial #	-			00h			
99~125	Manufacturer specific data (may be used in future)	-			FFh			
126	System frequency for 66MHz	66MHz			66h			
127	CAS latency for 66MHz	CAS latency of both 2 & 3			06h			
128+	Unused storage locations	-			FFh			

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. This value is increased sequently from '01h' whenever the manufacturing week is varied.

NOTES



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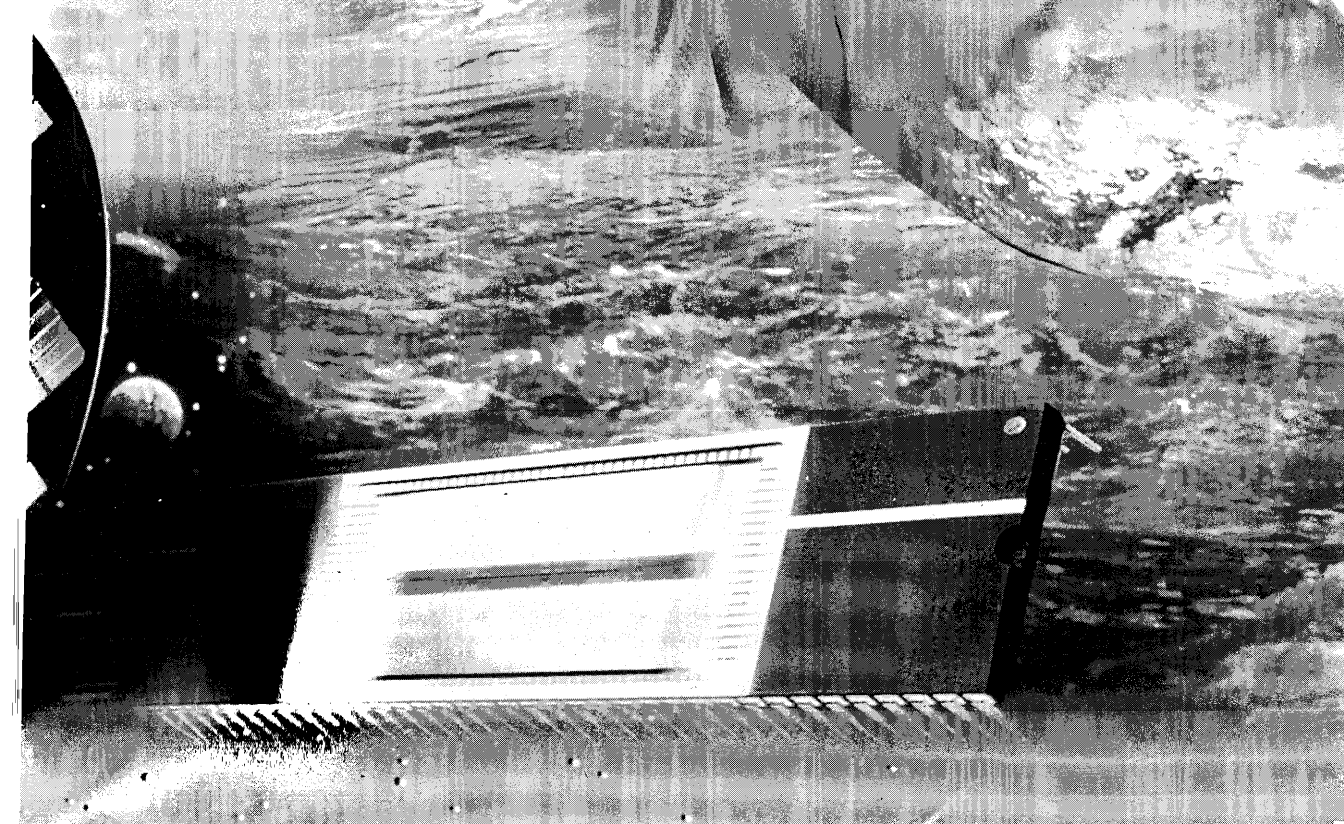

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