

## 16M-Bit (2M X 8/1M X 16) CMOS MASK ROM

### FEATURES

- Switchable organization  
2,097,152x8(byte mode)  
1,048,576x16(word mode)
- Fast access time  
Random Access : 120ns (max.)  
Page Access : 50ns(max.)
- Supply voltage : single +5V
- Current consumption  
Operating : 100 mA(max.)  
Standby : 50  $\mu$ A (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Polarity programmable chip enable and output enable pin
- Package  
- KM23C16005AG : 44-SOP-600

### GENERAL DESCRIPTION

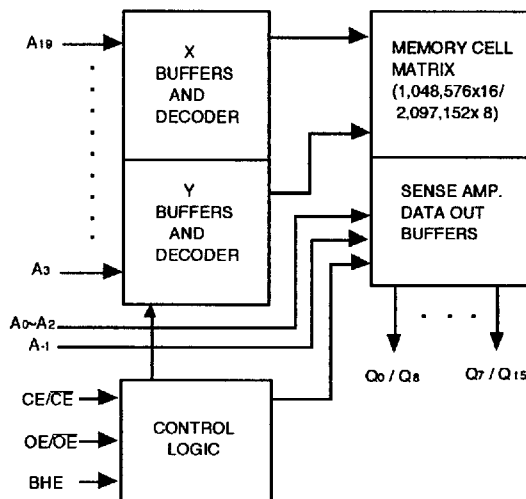
The KM23C16005AG is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152x8bit(byte mode) or as 1,048,576x16bit(word mode) depending on BHE voltage level.(See mode selection table)

This device includes page read mode function,page read mode allows four to eight words of data to read fast in the same page,CE and A<sub>3</sub> ~ A<sub>19</sub> should not be changed. This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible. Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of micro-processor, and data memory, character generator.

The KM23C16005AG is packaged in a 44-SOP and provides polarity programmable CE and OE buffer as user option mode.

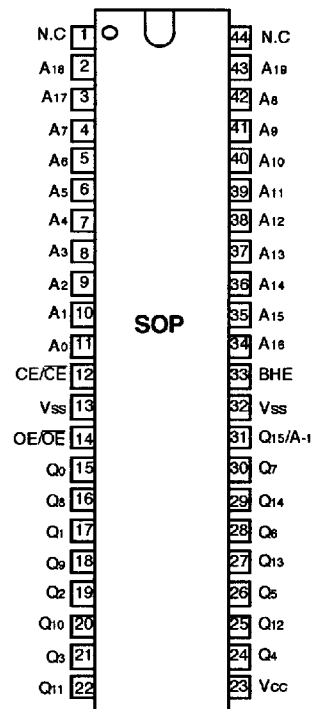
### FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A <sub>0</sub> -A <sub>2</sub>	Page Address Inputs
A <sub>3</sub> -A <sub>19</sub>	Address Inputs
Q <sub>0</sub> -Q <sub>14</sub>	Data Outputs
Q <sub>15</sub> /A-1	Output 15(Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/CE*	Chip Enable
OE/OE*	Output Enable
V <sub>cc</sub>	Power (+5V)
V <sub>ss</sub>	Ground
N.C	No Connection

\* User Selectable Polarity

### PIN CONFIGURATION



KM23C16005AG

### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub>	-0.3 to +7.0	V
Temperature Under Bias	T <sub>bias</sub>	-10 to +85	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T<sub>A</sub>=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>ss</sub>	0	0	0	V

### DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I <sub>cc</sub>	$\overline{CE}=\overline{OE}=V_{IL}$ , f=6.7MHz all outputs open	-	100	mA
Standby Current (TTL)	I <sub>SB1</sub>	$\overline{CE}=V_{IH}$ , all outputs open	-	1	mA
Standby Current (CMOS)	I <sub>SB2</sub>	$\overline{CE}=V_{cc}$ , all outputs open	-	50	μA
Input Leakage Current	I <sub>I</sub>	V <sub>IN</sub> =0 to V <sub>cc</sub>	-	10	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>cc</sub>	-	10	μA
Input High Voltage, All Inputs	V <sub>IH</sub>		2.2	V <sub>cc</sub> + 0.3	V
Input Low Voltage, All Inputs	V <sub>IL</sub>		-0.3	0.8	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4	-	V
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	-	0.4	V

### CAPACITANCE (T<sub>A</sub>=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	-	12	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	-	12	pF

Note : Capacitance is periodically sampled and not 100% tested.

### MODE SELECTION

CE/ $\overline{CE}$	OE/ $\overline{OE}$	BHE	Q15/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	Q <sub>0</sub> -Q <sub>15</sub> :Dout	Active
		L	Input	Operating	Q <sub>0</sub> -Q <sub>7</sub> :Dout Q <sub>8</sub> -Q <sub>14</sub> :High-Z	Active

**AC CHARACTERISTICS** (TA= 0°C to +70°C, Vcc = 5V ±10%, unless otherwise noted.)

**TEST CONDITIONS**

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

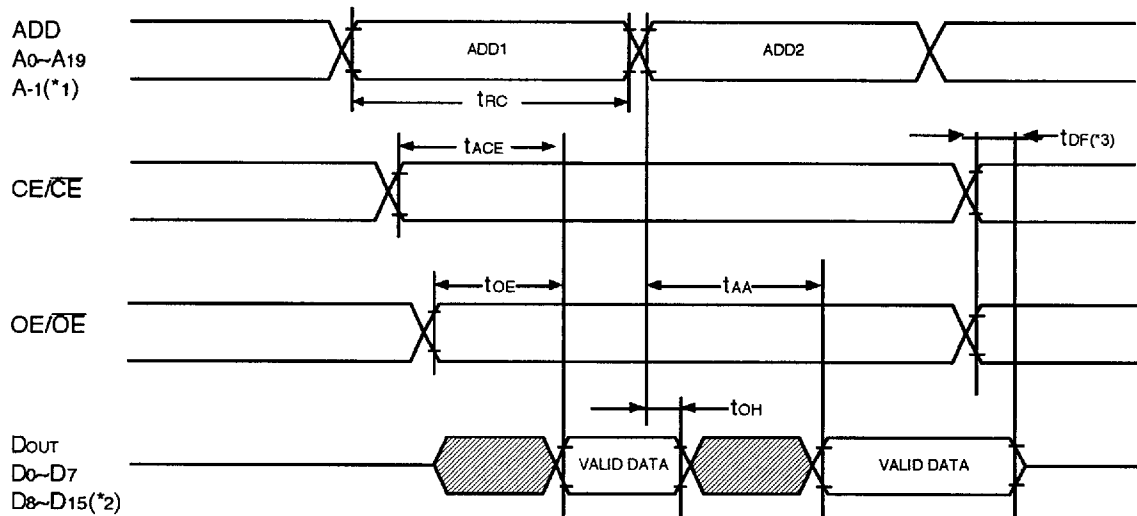
**READ CYCLE**

Parameter	Symbol	KM23C16005AG-12		KM23C16005AG-15		KM23C16005AG-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	120		150		200		ns
Chip Enable Access Time	tACE		120		150		200	ns
Address Access Time	tAA		120		150		200	ns
Page Address Access Time	tPA		50		60		70	ns
Output Enable Access Time	tOE		50		60		70	ns
Output or Chip Disable to Output High-Z	tDF		20		30		40	ns
Output Hold from Address Change	tOH	0		0		0		ns

\* Page Address : A0, A1, A2

## TIMING DIAGRAM

### READ

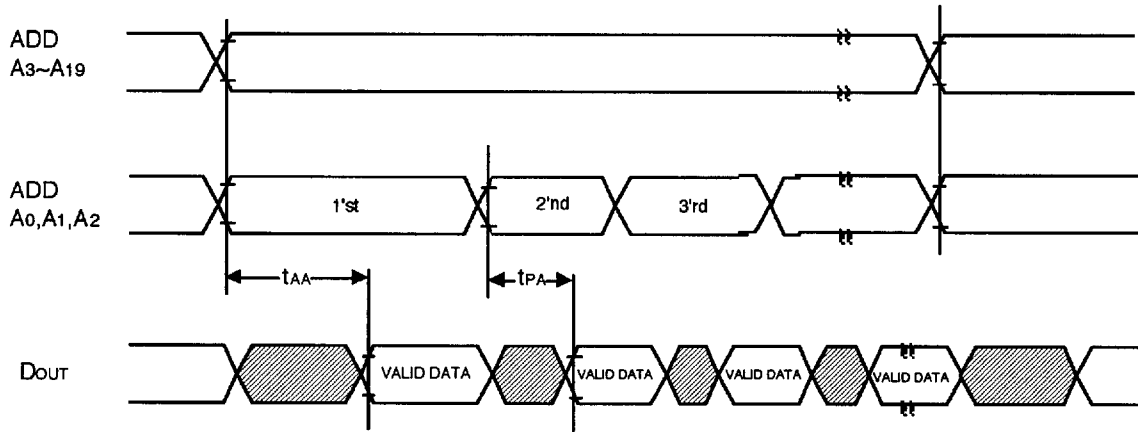


(\*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE=VIL)

(\*2) Word Mode only. (BHE=VIH)

(\*3) tDF is defined as the time which the outputs achieve the open circuit condition and is not referenced to VOH or VOL level.

### PAGE READ



**PACKAGE DIMENSION**

**44 LEAD SMALL OUTLINE PACKAGE**

Unit : mm/Inch

